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Colin Hinson
In the village of Blunham, Bedfordshire.

T I 9 9 / 4 H O M E C O M P U T E R

S E R V I C I N G M A N U A L

COMPILED AND EDITED
BY
JON STANFORD

FIRST REVISION, NOVEMBER, 1982

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INTRODUCTION

The TI 99/4 Home Computer was initially presented at the Consumer Electronics Show in June 1979 by Texas Instruments. The TI 99/4 is a TMS 9900-based microprocessor system. presently, the 99/4A mainframe is being manufactured by the Consumer Products Division of Texas Instruments, Inc. in Lubbock, Texas.

The TI 99/4A has many key features. Some of these feature include 16-color graphics, music and sound over four octaves. The TI 99/4A also makes use of an expanded TI Basic. This feature plus the capability for up to 72K bytes of memory (16K RAM internal, 26K ROM, and up to 30K ROM interfaced via the Command Module peripherals) make the TI 99/4A Home Computer a very powerful tool. These key features and the general operation of the TI 99/4A will be presented in the following pages.

SYSTEM BLOCK DIAGRAM:

The TI 99/4A Home Computer effectively combines each of the individual features of the unit into a complete and complex system. The basic blocks of the system include the CPU, sound generation, video display, I/O control, plus timing and control logic. These features are interfaced to produce the complete microprocessor system. The system block diagram of the TI 99/4A is shown in Figure 1, p. 2.

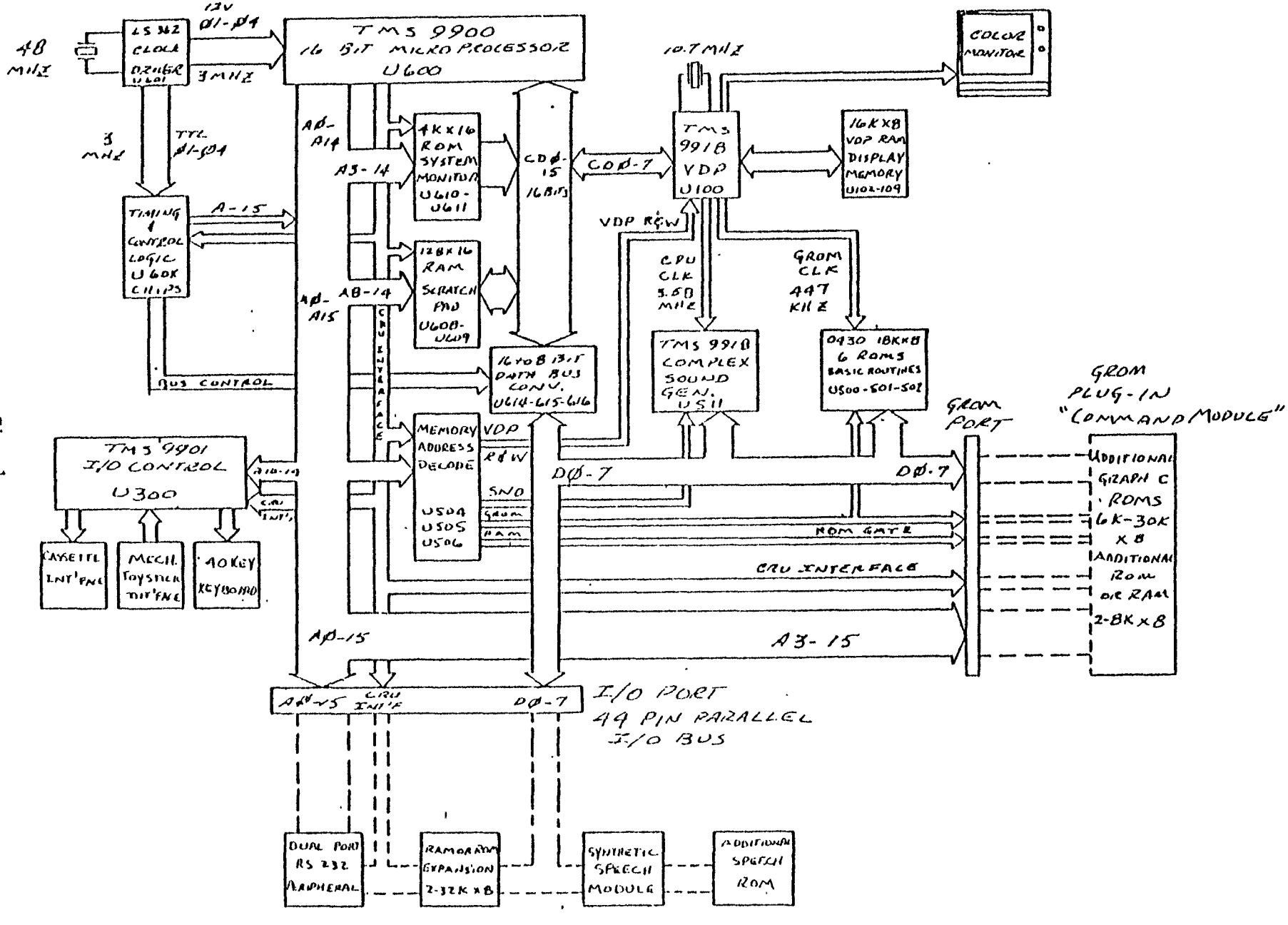


FIG. 1

99/4 SYSTEM BLOCK DIAGRAM

HOME COMPUTER
KEY ARCHITECTURAL FEATURES

- 9900 CPU
- VIDEO PROCESSOR WITH 10.74 MHz CRYSTAL OSCILLATOR FOR NTSC COMPOSITE VIDEO GENERATION AND CONTROL OF GRAPHICS RAM
- 3 GRAPHICS ROMS ONBOARD WITH 6K BYTES EACH, EXPANSION PORT FOR SOFTWARE MODULES WITH UP TO FIVE 6K X 8 GROMS AND 8K ROM OR RAM
- 48 KEY KEYBOARD
- TV INTERFACE VIA VIDEO MODULATOR
- PERIPHERAL CONNECTORS WITH CRU AND 8 BIT MEMORY INTERFACE
- 1200 BAUD HOME CASSETT INTERFACE

HOME COMPUTER
TMS 9918 VIDEO DISPLAY PROCESSOR KEY FEATURES

- REFRESH THE TV SCREEN AT 60 Hz WITHOUT INTERLACE FOR COMPOSITE NTSC VIDEO OUTPUT
- 24 LINES OF 32 CHARACTERS WITH 8 X 8 DOT RESOLUTION
- 32 MOVABLE CHARACTERS WITH MAGNIFICATION
- 24 LINES OF 40 CHARACTERS WITH 6 X 8 DOT RESOLUTION
- 48 LINES OF 64 INDEPENDENT SPOTS
- EXTERNAL VIDEO INPUT WITH SYNC
- PROVIDE 8 COLORS WITH 2 LUMINOUS LEVELS EACH
- PROVIDE 8 SETS OF COLOR SELECT REGISTERS TO PROVIDE SEPARATE COLOR FOR ONES AND ZEROS
- ADDRESS 4-16K BYTES OF RAM FOR CPU OR DISPLAY
- SINGLE 5 VOLT POWER SUPPLY
- 10.74 MHz ONBOARD CRYSTAL OSCILLATOR
- GROM CLOCK
- 40 PIN PLASTIC PACKAGE

HOME COMPUTER
TMC Q430 GRAPHICS ROM KEY FEATURES

- 6144 BYTES MASK PROGRAMMABLE ROM
- 16 BIT ADDRESS REGISTER WITH INCREMENTER
- CHIP SELECT FROM 3 MOST SIGNIFICANT ADDRESS BITS
- INSTRUCTION DECODE FOR FOUR OPERATIONS
  - READ BYTE AND INCREMENT
  - WRITE HIGH ADDRESS BYTE AND TRANSFER HIGH TO LOW
  - READ LOW ADDRESS BYTE
  - SPARE TO WRITE RAM OR PROM
- LOW COST P CHANNEL MOS
- 9us CYCLE TIME
- +5, -5 POWER SUPPLIES WITH TTL INTERFACE
- 447.5 KHz CLOCK INPUT
- 16 PIN PACKAGE

HOME COMPUTER
TIM 9919 SOUND GENERATOR KEY FEATURES

- 3 VOICES WITH 4 OCTAVE MUSCIAL RESOLUTION
- 15 BIT PROGRAMMABLE NOISE SHIFT REGISTER
- 100 MW AUDIO DRIVE WITH 30DB CONTROL IN 2DB STEPS
- 8 BIT CPU INTERFACE
- 5V POWER SUPPLY
- I^2L TECHNOLOGY
- 16 PIN PACKAGE

SYSTEM POWER UP

POWER IS TURNED ON:

- 9900 CPU RESETS AND ADDRESSES LOW EPROM LOCATIONS
- 9900 INITIALIZES
- 9900 SETS UP WORKSPACE REGISTERS IN 6810 RAM
- 9900 BEGINS READING FROM GROMS
- 9900 ENTERS TIME DELAY LOOP TO ALLOW STABILIZATION - ¼ SEC
- 9919 SOUND CHIP IS TURNED OFF
- 9918 VDP IS INITIALIZED
- 4116 RAM IS CLEARED - REQUIRES APPROXIMATELY 1 SEC
- FRONT PANEL DISPLAY IS WRITTEN INTO VDP
- 9919 SOUND CHIP EMITS BEEP
- 9900 CPU ENTERS KEYBOARD SCAN ROUTINE

SYSTEM IS NOW READY FOR USER INPUT

ITEMS TO CHECK DURING DEBUG

1 - CHECK IF FRONT PANEL IS UP "TI LOGO"

2 - CHECK ±5, +12 VOLT LEVELS THROUGHOUT BOARDS

3 - CHECK IF READY PIN 64 OF 9900 IS LOCKED UP

4 - CHECK THE FOUR 12 VOLT CLOCKS FROM 74362 to 9900

5 - CHECK

GROM SELECT PIN 10 0430
GROM READY PIN 15 0430
GROM CLOCK PIN 13 0430

6 - CHECK PIN 38 OF 9918 FOR 3.579520 MHz CLOCK

7 - CHECK VDP (9918) READ PIN 15 9918
WRITE PIN 14 9918 .

8 - CHECK DATA OUT OF 4116 RAM PIN 14

9 - CHECK COMPOSITE VIDEO FROM DIN CONNECTOR

HOME COMPUTER CASSETTE INTERFACE

1. Operates with byte/manchester encoding format.

2. Utilizes redundancy to gain increased reliability.

3. Uses wave shaping on input and output to increase reliability.

4. Has two motor control circuits which allow computer to control decks.

5. Has capability of reading from one deck and writing to another, under computer control.

6. The interface is software intensive and relies on 9901 internal timer for it's timing.

PROBLEM AREA OF CASSETTE INTERFACE

1. Reliable recovery of data is dependant on recorder used during save.

2. Reliability is directly proportional to frequency response of cassette deck.

3. Reliability can be observed by looking for the "eye" or "jitter" phenomenon with an oscilloscope.

   A. Present reliability is dependant on amount of jitter.
      If jitter is less than 60 ms cassette should work.

4. Cassette is also adversely affected by speed changes.

   A. Motor control curcuit can under special circumstances cause this.

GENERAL DESCRIPTION OF THE 99/4A

The following paragraphs provide a description of the 99/4A system hardware, the VDP chip (TMS 9918), the sound chip (TMS 9919), the GROM (TMC 0430), the associated timing diagrams, the cassette interface circuitry and power supply.

99/4 SYSTEM HARDWARE

The 99/4 has been built around the TMS 9900 microprocessor. Fig. 1 shows a block diagram of the system. In this description the logic of the 99/4A is grouped into the following functional sections.

- Clock generator/driver
- Microprocessor unit
- Memory selection logic
- System ROM & RAM
- 16 to 8 bit interfacing circuit
- Timing and control logic
- GROM memory
- TMS 9901 programmable system interface
- TMS 9918 video display processor
- TMS 9919 sound generator
- Keyboard, remote handheld unit
- Cassette interfacing circuit
- I/O port
- Power supply
- European power supply
- Audio board

The purpose and composition of these functional sections is to provide an overview of the 99/4A system with a detailed description in the succeeding paragraphs.

- The clock generator/driver provides 4 non-overlapping clock signals for the TMS 9900 microprocessor and also internal latch which is used in the reset circuitry.

- The microprocessor unit with the TMS 9900 handles all the processing as required by the on board software as well as the off board software (DSR's and command modules), interrupts, and power-up initialization.

- The memory address/decode logic provides enabling signals to the various RAM's, ROM's, GROM's and interface circuit.

- System RAM consists of 256 bytes static RAM used as a scratch pad memory for all system operations. The system ROM consists of 8K bytes of the following system programs.

  - The GPL interpreter.
  - Floating point routines.
  - String conversation routines.
  - Cassette interfacing and I/O programs.
  - Basic programs.

- The 16 to 8 bit interfacing circuit enable the 99/4 to access 8 bit devices by multiplexing and demultiplexing the 16 bit data bus of the TMS 9900.

- Timing and control logic provides the timing and enable signals for the 16 to 8 bit interfacing circuit. It also handles the READY and WE signal for memory operations.

- The TMS 9901 I/O controller is the interface used by the keyboard scanning circuit and the cassette interfacing circuit. It also handles interrupts and has an on-chip timer.

- GROM memory consists of 18K bytes of graphics program. (Graphics is the intermediate language used in the 99/4) It contains the following system routines:

  GROM 0 : - Monitor routines
  - First part of the equation calculator.
  - The cassette device subroutine contain ROM.

  GROM 1 : - The editor
  - The prescan routine for basic.
  - The first part of the basic executing program.

  GROM 2 : - The file management programs.
  - The second part of the BASIC executing program.
  - The second part of the equation calculator.

Grom memory is expandable up to a limit of 48K through the grom I/O Port.

The GROM port enables the user to run preprogrammed sofware in up to 5 GROM's in a software module. This module may also contain in ROM processing for generating the composite video signal. A part of the 16K byte user RAM contains the character code table which is downloaded in the RAM during the power-up sequence.

- The TMS 9919 sound generator is a one chip device capable of generating 3 tones and noise programmable by the user.

- The keyboard interface is using the TMS 9901 I/O chip. The keyboard scanning is using the multiplexing technique.

- The I/O port provides the capability to the 99/4 to access the ROM in the various peripherals containing the device service routines (DSR's) and is takes care of the data exchange.

- The audio board houses an audio amplifier to drive the 8 ohm loadspeaker in the European version of the 99/4. Volume control is by a slide pot.

OSCILLATOR CIRCUIT

GENERAL DESCRIPTION

The TMS 9900 microprocessor, as used in the TI99/4, uses four non overlapping clock signals generated by a 74LS362 clock generator/driver. These four clock signals Q1, Q2, Q3, and Q4 have a 12 volt swing.
For system synchronization purposes the inverted clock signals (Q1, Q2, Q3 and Q4) are available at TTL level.
A timing diagram for the clock signals is given in figure 35, As can be seen from the internal schematics of the 74LS362 figure 35, there is also a D type latch available. This latch, clocked by Q3, is in the reset circuitry.

HARDWARE DESCRIPTION (see figure 2, p 14.)

POWER CONNECTIONS

Power connection points are pin 10 for ground, pin 13 for the +12 volt, and pin 20 for the +5 volt supply.
L603, L604, C604, C605 and C607 are used for decoupling of noise generated by the 74LS362.

POWER UP

Pin 17, conected to the 5 volt power supply by serie resistor R604 enables the clock outputs.

RESONATOR PART

A third overtone, 48MHz crystal, connected between pin 18 and 19 determines the clock frequency. The tank circuit with L602 and L603 connected between PINS 1 and 2 selects the third overtone. Some units may use a RMHZ crystal with tank components to select the primary frequency.

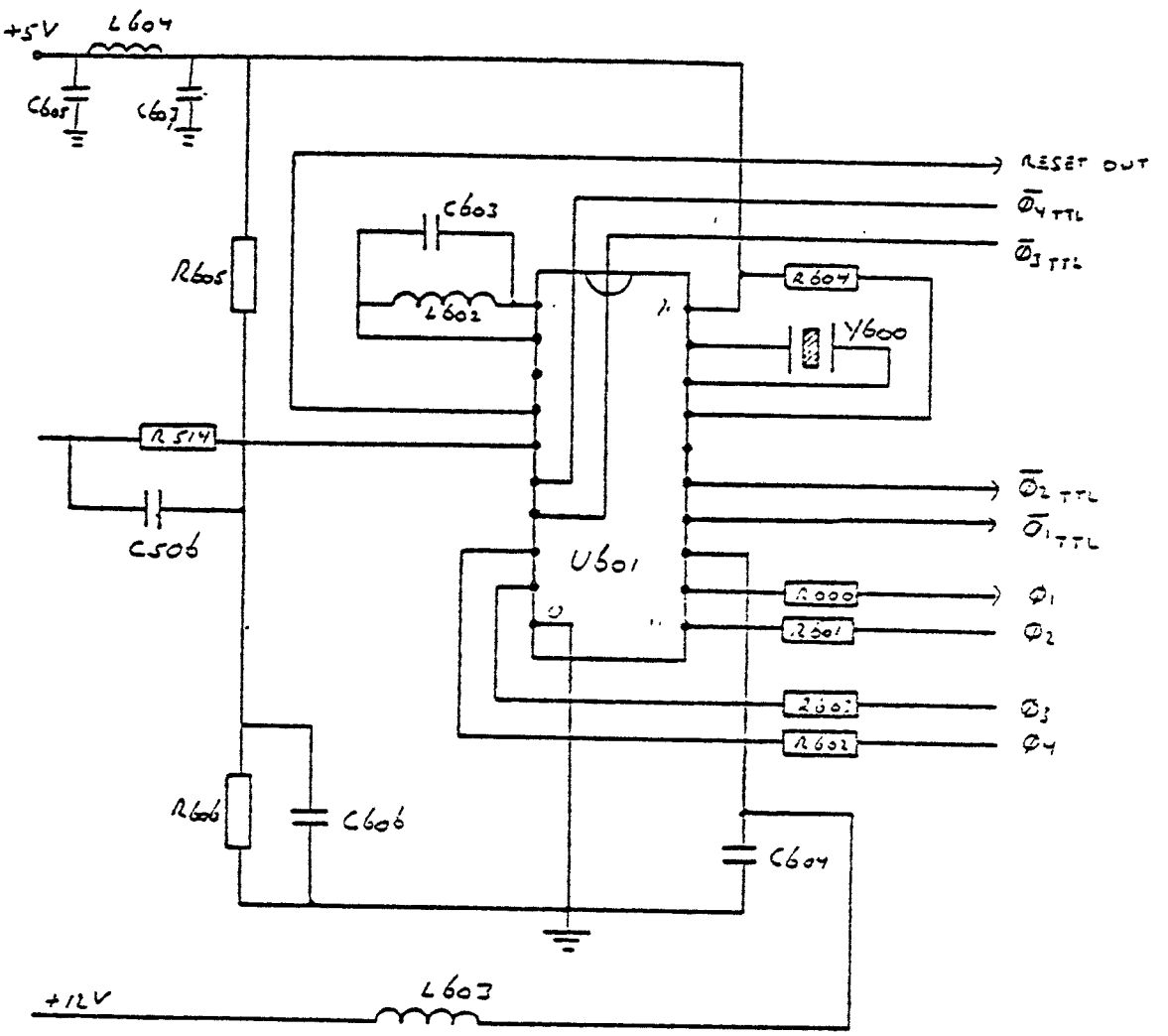
CLOCK SIGNALS

Pin 8, 9, 11 and 12 are the four 12 volt clock outputs for the TMS 9900. The four series resistors R601, R602 and R603 minimize over and undershoot.
The inverted clock signals on pin 6, 7, 14 and 15 are used internally in the 99/4 for timing purposes.

RESET

Reset is accomplished during power-up and when a solid state software command module is inserted.
C606 will be slowly charged by resistor R605 after applying power to the console. Thus for a short period the D input of pin 5 of the 74LS362 is low. The 74LS362 clocks this zero binary value to the reset out of pin 4. This signal resets the TMS 9900 until a binary 1 value is sensed on pin 5. When the system is switched off, R606 discharges C606, thus enabling a new reset. When a solid state software command module is inserted, the reset line is connected to -5 volt. C606 is then partly discharged by C506, thus dropping the voltage at pin 5 for a short time to the binary low level, generating a reset. When the solid state software command module is removed, resistor R514 will descharge C506 to enable a new reset.

CLOCK CIRCUITRY



R514	47 kΩ	C506	15 μF	Y600	XTAL 4d m Hz
R600	22 Ω	C603	22 pF	U601	74 LS 362
R601	22 Ω	C604	.1 μF		
R602	22 Ω	C605	10 pF		
R603	22 Ω	C606	15 pF		
R604	1 kΩ	C607	1 NF		
R605	12 kΩ				
R606	150 kΩ				

Fig. 2

CENTRAL PROCESSING UNIT

GENERAL DESCRIPTION

The 99/4 Home Computer uses the Texas Instruments TMS 9900 microprocessor. It provides the system with a 15 bit address and 16 bit data bus for communication with external memory. It also has input and output pins for serial in and output, interrupt handling and memory control (see figures 3 and 4, pp 20-23)

MEMORY INTERFACING

The TMS 9900 interfaces with memory by means of a 16 bit data bus (D0-D15), the 15 bit address bus (A0-A14) and the following control signals.

MEMEN MEMORY ENABLE. When active (low), MEMEN indicates that the address bus contains a memory address.

WE WRITE ENABLE. When active (low), WE indicate that memory write data is available from the TMS 9900 to be written into memory.

DBIN DATA BUS IN. .When active (high), DBIN indicates that the TMS 9900 has diabled its output buffers to allow memory to place read data on the data bus during MEMEN.

READY READY. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not ready is indicated during a memory operation, the TMS 9900 suspends further operating (e.g. enters a wait state) until READY becomes active again, after which the memory read/write cycle is completed. This signal enables the use of slow memory devices with the TMS 9900.

WAIT WAIT. When active (high), WAIT indicates that the TMS 9900 has entered a wait state because of a not-ready condition from memory.

Timing diagrams for read and write cycles, with and without wait states, are given in figures 5-8, pp. 25-28.

DIRECT MEMORY ACCESS

Performing memory access without interference of the TMS 9900 is called direct memory access (DMA). For this purpose the following control lines are available.

HOLD HOLD. When active (low), HOLD indicates to the processor that an external controller disires to use address, data and memory control signals. The TMS 9900 enters the hold state following a hold signal when it has completed its present memory cycle. The processor then places the address and data buses in the high-impedance state along with MEMEN, WE and DBIN and responds with a holdackowledge signal (HOLDA). When HOLD is removed, the processor returns to normal operation.

HOLDA HOLD ACKNOWLEDGE. When active (high), HOLDA indicates that the processor is in the hold state and that the outputs (MEMEN, WE and DBIN) are in the high inpedance state thus making is possible for an external device to use the buses and access memory.

The timing diagram for direct memory access is given if figure 9, p. 29.

IN AND OUTPUT (I/O)

The TMS 9900 has two possibilities for communicating with external devices:

A. Addressing the device as memory.
B. Using the communication resister unit (CRU).

The CRU makes it possible to communicate with external devices with fewer lines. Only A3 through A14, CRUIN, CRUOUT and CRUCLK are used. The CRU I/O bus makes it also possible to address bits instead of bytes or words.

OUTPUT

Output with the CRU interface is performed as follow. The processor addresses the bit to be set. This address is decoded and enables a latch to the data present on the CRUOUT line on CRUCLK.

INPUT

Input is performed only with the address bus and CRUIN. Again the processor addresses the bit to be read.
The system hardware decodes the bit address on A3 through A14 and enables the addressed bit to put its value on the CRUIN line. The bit is then fetched by the TMS 9900.

TIMING DIAGRAM

A timing diagram of CRU operations is given in figure 10, p. 30.

The TI 99/4 home computer uses both ways of I/O to communicate with internal and external devices.

INTERRUPT HANDLING

Interrupt processing logic on the TMS 9900 uses the following inputs.

INTREQ INTERRUPT REQUEST. When active (low) INTREQ indicates that an external interrupt is requested. If INTREQ is active, the processor loads the data on the interrupt-code input lines IC0 through IC3 into the internal interrupt-code storage resister. This code is compared to the interrupt mask bits of the enabled interrupt level, the TMS 9900 interrupt sequences is initiated. If the comparison fails, the processor ignores the request. INTREQ should remain active and the processor will continue to sample IC0 through IC3 until the program enables a sufficiently low priority to accept the requested interrupt.

IC0
IC1
IC2
IC3 INTERRUPT CODES. IC0 is the most significant bit of the interrupt code, which is sampled when INTREQ is active. When IC0 through IC3 are LLLH, the highest external priority interrupt and when HHHH the lowest priority interrupt is being requested.

In this system, IC0, IC's, and IC2 are tied to VSS, and IC3 is tied to VCC, thus if INTREQ is active, it is always considered the highest priority.

TIMING SIGNAL

The TMS 9900 has an additional timing signal IAQ which becomes high during any memory cycle when the TMS 9900 is acquiring an instruction. This signal can be used for timing purposes.

SUPPLY VOLTAGES

The TMS 9900 requires 3 voltages with respect to ground.

VBB	- 5 volt supply voltage
VCC	+ 5 volt supply voltage
VDD	+12 volt supply voltage
VSS	system ground

CLOCK INPUTS

Four clock signals Q1, Q2, Q3 and Q4 have to be provided on the four clock input pins for internal timing of the TMS 9900. Note that these inputs require a 12 volt swing.

SYSTEM START UP

The following signals can be used for system start up.

RESET RESET. When active (low), RESET resets the processor. When RESET is released the TMS 9900 starts execution of its programs with the first memory address fetched from memory location 0002.

LOAD LOAD. When active (low), the processor starts execution of its programs on the address in memory location FFFE.

During a reset or load the microprocessor also fetches the workspace pointer. This is the starting address of a memory field of 16 words in RAM memory which is used as a register field. During reset the workspace pointer is fetched from adress 0000, during load from address FFFC.

HARDWARE DESCRIPTION

A drawing of the connections to the TMS 9900 as used in the 99/4 is given in figure 1, p. 21.
The following list describes the connections in more detail.

POWER CONNECTIONS

+ 5 volt. The +5 volt power supply is connected to PIN 2 and 59 of the TMS 9900. L600, C600 and C611 are acting as a filter to reduce system noise on PIN 2 and C603 is used for the same purpose on PIN 59.

+12 volt. The +12 volt power supply is connected to PIN 27 L601 and C612 are acting as a filter to reduce noise.

- 5 volt. The -5 volt power supply is connected to PIN 1 with C602 for decoupling.

GROUND Pin connections 26 and 40 are for ground.

CLOCK INPUTS
Clock inputs Q1, Q2, Q3 and Q4 are input on pins 8, 9, 25 and 28 respectively.

ADDRESS BUS
The 99/4 uses the address bus internally without further buffering, except for A14, which is used on the GROMS (see I/O bus description).

DATA BUS
Internal ROM and RAM uses the data bus without buffering. To connect the data bus to internal 8 bit devices and for in and output, a special 16 to 8 bit interfacing circuit is used.

CRU BUS
CRUOUT, CRUIN and CRUCLK are used internally without buffering.

INTERRUPT HANDLING
Interrupt vector pins 33 through 36 are preset to code LLLH, the highest external priority interrupt. So the 99/4 knows only one interrupt level. The INTREQ line is connected to the TMS 9901, which handles the interrupts.

RESET
The system resets during power up or when a solid state software command module is inserted. This is done by connecting RESET pin 6 to pin 4 of the system clock generator (U601).

LOAD
The load function or pin 4 is connected to the I/O Port via resistor R523.

WRITE ENABLE
The WE function or pin 61 is used by fast system RAM without buffering and is modified by timing and control for other devices.

IAQ/HOLDA
The instruction aquisition signal on pin 7 and the hold acknowledge signal on pin 5 are combined on OR-gate U605 to generate a combined signal.

MEMORY ENABLE (MEMEN)
This signal is buffered by OR-gate U605 for further use in and outside the 99/4. R607 is used as a pull up resistor to +5 volt to assure that memory is disabled during power up.

DBIN
The DBIN signal on pin 29 is buffered twice by inverting gates U602 for use within the 99/4 system.

READY/HOLD
READY and HOLD on pins 62 and 64 are combined to form one signal.

A study of 9900's internal structure is useful when trying to understand the operation of the IC. The architecture of the 9900 microprocessor is shown in the diagram of Fig. 3, p. 20. This shows the internal features within the CPU. These features include:

* The ALU
* 3 Multiplexer Busses
* Control Logic and Control ROM
* Internal Registers:
  Memory address register, shift register, status register, source data register, shift counter, workspace register, instruction register, and auxillary register T1 and T2.

The ALU (Arithmetic Logic Unit) is a 16-bit, parallel logic network used in the execution of the 9900's instructions. The unit performs arithmetic functions, log, and comparisons. The multiplexer busses are used in the transfer of flow of data in the CPU. The control circuitry provides the signals necessary for correct gating.

The control logic and control ROM provide the necessary signals for the correct sequencing or operation of the CPU's instructions. This is accomplished with the aid of the input control signals and master timing. Among the internal registers there are three which are key architectural features of the CPU. These registers are the workspace pointer, the program counter, and the status register. the workspace pointer contains the location of the first word in the workspace. The program counter contains the address for the next word which is to be used in the execution of an instruction. The status register determines if the conditions necessary for an instruction execution have been met. This is done by the setting of flags.

In the operation of the 9900, sixty-nine instruction words can be used. A list of the 9900's instruction set can be found in Table 1, p. 31. These instructions are used to perform arithmetic operations, logic, comparisons, and manipulation operations on data. They are also used for the loading and storing of data within the CPU's internal registers. Data transfer between the external memory system and external devices is also made possible with the instructions via the CRU. Instructions are also used as control functions within the CPU.

The external memory used with the TMS 9900 in the TI99/4 and TI99/4A consists of two TMS 4732's and two MCM 6810P's. The TMS 4732's are 4K X 8 bit ROMS and are addressed via lines A3-A14 of the address bus. However, one of the 4732's uses the D1-D7 lines on the data bus while the other uses data lines D8-D15, thus combining the two 4732's into a 4K X 16 bit ROM. The MCB 6810P's are 128 X 8 bit static RAM and are used as a scratch pad by the CPU. In a manner similar to the 4732's the two 6810's are combined to form a 128 X 16 bit RAM. One slight difference from the 4732's is that the 6810's are addressed by address lines A8-A14.

The 9900 uses three control signals during operation of the external memory read and write to control the use of the address and data busses. These signals are DBN, -MEMEN, and -WE. During memory read, DBIN and -MEMEN are active, while -WE is not. The active signals allow an output onto the address buss indicating the disired memory lacation to be read. DBIN and -MEMEN are deactivate the data bus output.

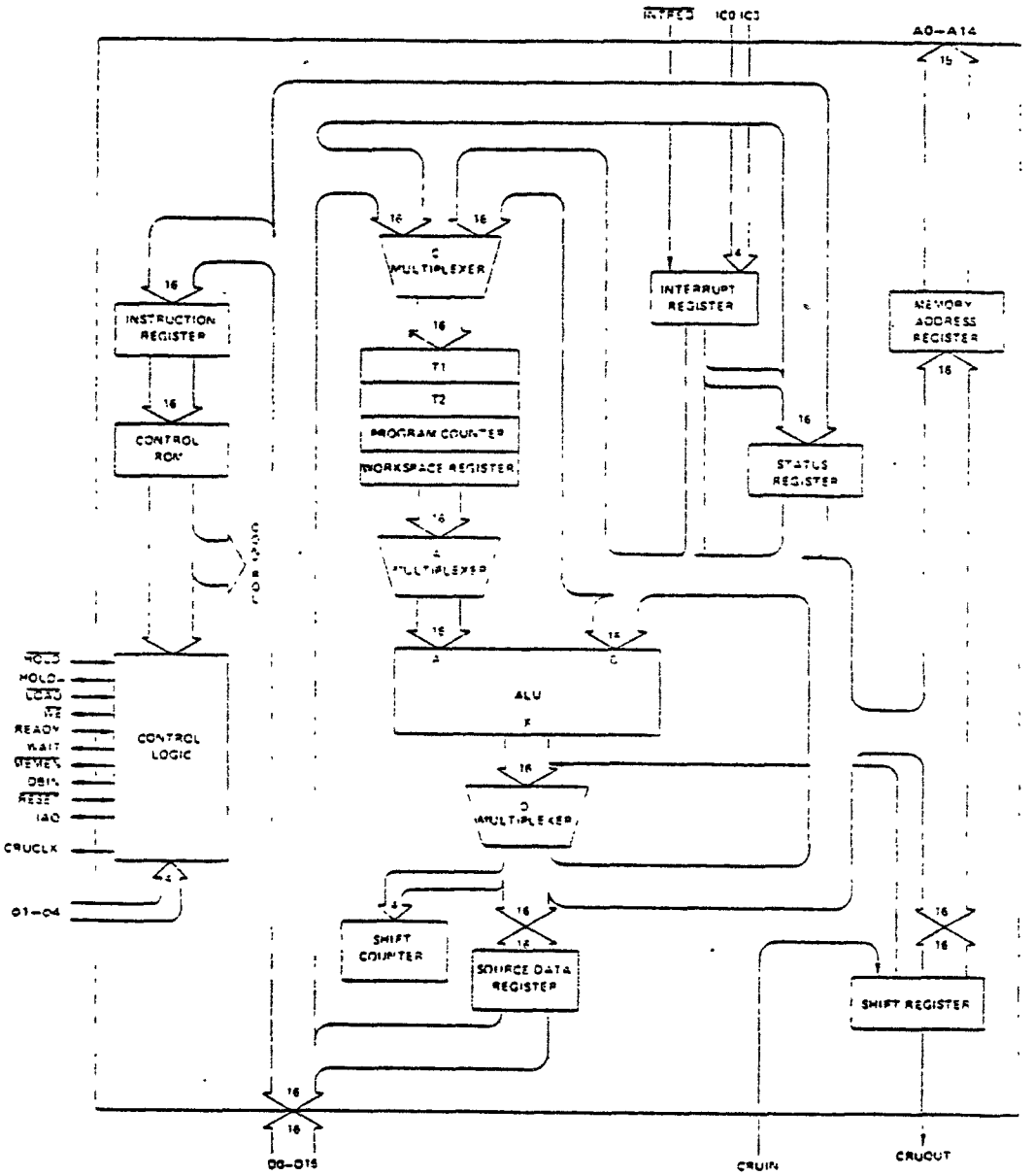


FIGURE 1 – ARCHITECTURE

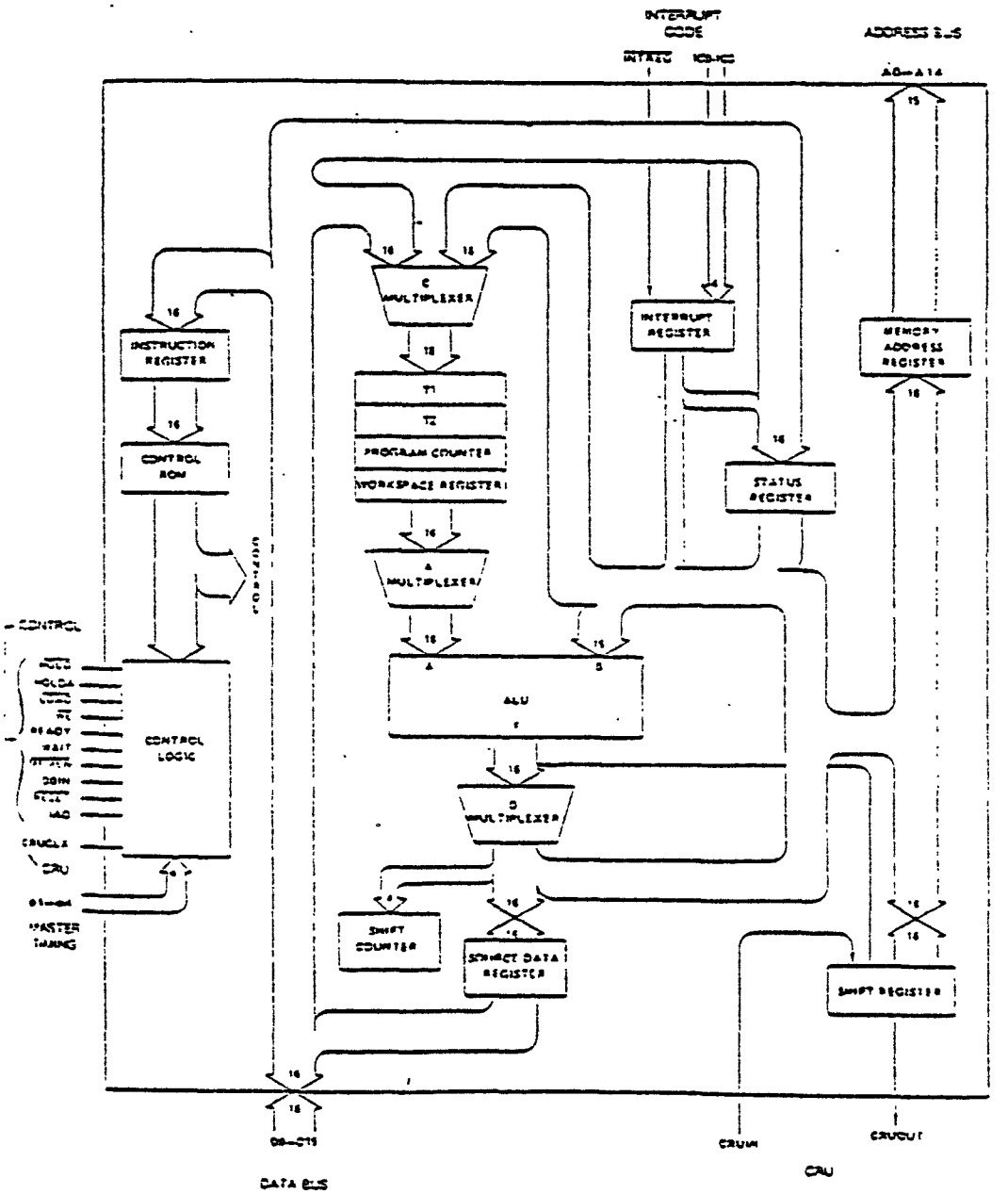


Figure 2. TMS 9900 ARCHITECTURE

Fig. 3

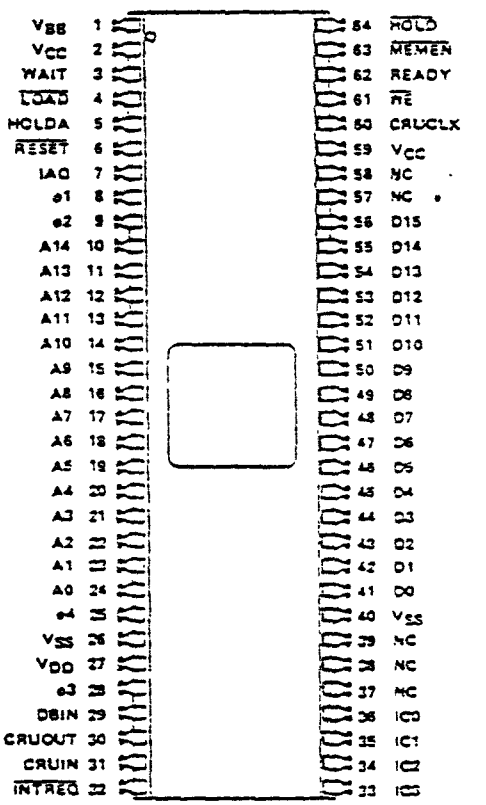
2.8 TMS 9900 PIN DESCRIPTION

Table 2 defines the TMS 9900 pin assignments and describes the function of each pin.

TABLE 2
TMS 9900 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
			ADDRESS BUS
A0 (MSB)	24	OUT	A0 through A14 comprise the address bus. This 3-state bus provides the memory-address vector to the external-memory system when MEMEN is active and I/O-bit addresses and external-instruction addresses to the I/O system when MEMEN is inactive. The address bus assumes the high-impedance state when HOLDA is active.
A1	23	OUT	
A2	22	OUT	
A3	21	OUT	
A4	20	OUT	
A5	19	OUT	
A6	18	OUT	
A7	17	OUT	
A8	16	OUT	
A9	15	OUT	
A10	14	OUT	
A11	13	OUT	
A12	12	OUT	
A13	11	OUT	
A14 (LSB)	10	OUT	
			DATA BUS
D0 (MSB)	41	I/O	D0 through D15 comprise the bidirectional 3-state data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when MEMEN is active. The data bus assumes the high-impedance state when HOLDA is active.
D1	42	I/O	
D2	43	I/O	
D3	44	I/O	
D4	45	I/O	
D5	46	I/O	
D6	47	I/O	
D7	48	I/O	
D8	49	I/O	
D9	50	I/O	
D10	51	I/O	
D11	52	I/O	
D12	53	I/O	
D13	54	I/O	
D14	55	I/O	
D15 (LSB)	56	I/O	
			POWER SUPPLIES
V_{BB}	1		Supply voltage (−5 V NOM)
V_{CC}	2,59		Supply voltage (5 V NOM). Pins 2 and 59 must be connected in parallel.
V_{DD}	27		Supply voltage (12 V NOM)
V_{SS}	26,40		Ground reference. Pins 26 and 40 must be connected in parallel.
			CLOCKS
ϕ1	8	IN	Phase-1 clock
ϕ2	9	IN	Phase-2 clock
ϕ3	28	IN	Phase-3 clock
ϕ4	25	IN	Phase-4 clock

TMS 9900 PIN ASSIGNMENTS



NC = No internal connection

Fig. 4

TABLE 2 (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
			BUS CONTROL
DBIN	29	OUT	Data bus in. When active (high), DBIN indicates that the TMS 9900 has disabled its output buffers to allow the memory to place memory-read data on the data bus during MEMEN. DBIN remains low in all other cases except when HOLDA is active.
MEMEN	63	OUT	Memory enable. When active (low), MEMEN indicates that the address bus contains a memory address.
WE	61	OUT	Write enable. When active (low), WE indicates that memory-write data is available from the TMS 9900 to be written into memory.
CRUCLK	60	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A0 through A2.
CRUIN	31	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A3 through A14).
CRUOUT	30	OUT	CRU data out. Serial I/O data appears on the CRUOUT line when an LDCR, SBZ, or SBO instruction is executed. The data on CRUOUT should be sampled by external I/O interface logic when CRUCLK goes active (high).
			INTERRUPT CONTROL
INTREQ	32	IN	Interrupt request. When active (low), INTREQ indicates that an external interrupt is requested. If INTREQ is active, the processor loads the data on the interrupt-code-input lines IC0 through IC3 into the internal interrupt-code-storage register. The code is compared to the interrupt mask bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal or less than status register bits 12 through 15) the TMS 9900 interrupt sequence is initiated. If the comparison fails, the processor ignores the request. INTREQ should remain active and the processor will continue to sample IC0 through IC3 until the program enables a sufficiently low priority to accept the request interrupt.
IC0 (MSB)	36	IN	Interrupt codes. IC0 is the MSB of the interrupt code, which is sampled when INTREQ is active. When
IC1	35	IN	IC0 through IC3 are LLLH, the highest external-priority interrupt is being requested and when HHHH,
IC2	34	IN	the lowest-priority interrupt is being requested.
IC3 (LSB)	33	IN	
			MEMORY CONTROL
HOLD	64	IN	Hold. When active (low), HOLD indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The TMS 9900 enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with WE, MEMEN, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When HOLD is removed, the processor returns to normal operation.
HOLDA	5	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs (WE, MEMEN, and DBIN) are in the high-impedance state.
READY	62	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the TMS 9900 enters a wait state and suspends internal operation until the memory systems indicate ready.
WAIT	3	OUT	Wait. When active (high), WAIT indicates that the TMS 9900 has entered a wait state because of a not-ready condition from memory.

*If the cycle following the present memory cycle is also a memory cycle, it, too, is completed before the TMS9900 enters the hold state. The maximum number of consecutive memory cycles is three.

Fig. 4 (Continued)

TABLE 2 (CONCLUDED)

SIGNATURE	PIN	I/O	DESCRIPTION
			TIMING AND CONTROL
IAQ	7	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the TMS 9900 is acquiring an instruction. IAQ can be used to detect illegal op codes.
$\overline{\text{LOAD}}$	4	IN	Load. When active (low), $\overline{\text{LOAD}}$ causes the TMS 9900 to execute a nonmaskable interrupt with memory address $FFFC_{16}$ containing the trap vector (WP and PC). The load sequence begins after the instruction being executed is completed. $\overline{\text{LOAD}}$ will also terminate an idle state. If $\overline{\text{LOAD}}$ is active during the time $\overline{\text{RESET}}$ is released, then the $\overline{\text{LOAD}}$ trap will occur after the $\overline{\text{RESET}}$ function is completed. $\overline{\text{LOAD}}$ should remain active for one instruction period. IAQ can be used to determine instruction boundaries. This signal can be used to implement cold start ROM loaders. Additionally, front panel routines can be implemented using CRU bits as front panel interface signals and software control routines to control the panel operations.
$\overline{\text{RESET}}$	6	IN	Reset. When active (low), $\overline{\text{RESET}}$ causes the processor to be reset and inhibits $\overline{\text{WE}}$ and CRUCLK. When $\overline{\text{RESET}}$ is released, the TMS 9900 then initiates a level zero interrupt sequence that acquires WP and PC from locations 0000 and 0002, sets all status register bits to zero, and starts execution. $\overline{\text{RESET}}$ will also terminate an idle state. $\overline{\text{RESET}}$ must be held active for a minimum of three clock cycles.

Fig. 4 (continued)

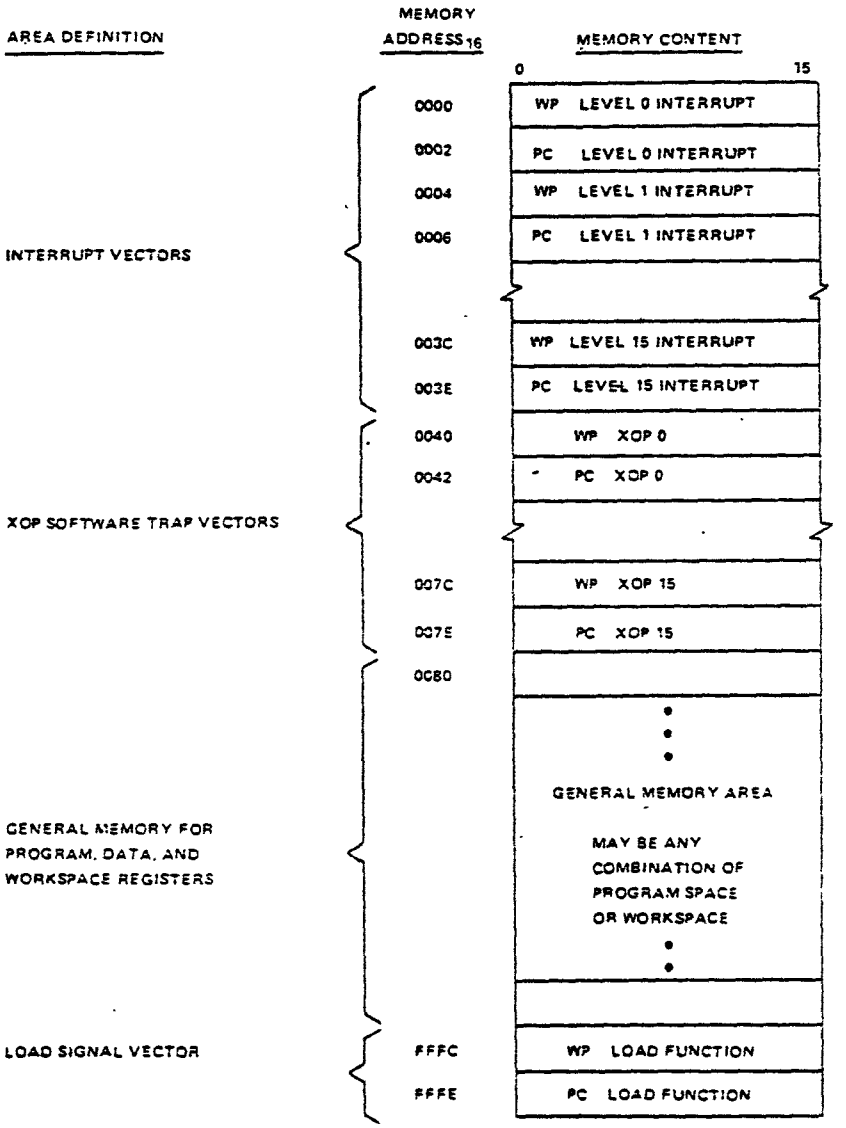


FIGURE 2 – MEMORY MAP

Three internal registers are accessible to the user. The program counter (PC) contains the address of the instruction following the current instruction being executed. This address is referenced by the processor to fetch the next instruction from memory and is then automatically incremented. The status register (ST) contains the present state of the processor and will be further defined in Section 3.4. The workspace pointer (WP) contains the address of the first word in the currently active set of workspace registers.

A workspace register file occupies 16 contiguous memory words in the general memory area (see Figure 2). Each workspace register may hold data or addresses and function as operand registers, accumulators, address registers, or

Drivers are deactivated to prevent the input data from conflicting with output data. Memory write makes use of -MEMEN also -WE both active, and DBIN deactivated. Under these conditions the 9900 ouputs on the address and data busses and holds these outputs for the duration required by RAM.

CRU ALLOCATION

Of the available 4K of CRU bits, the first 1K (addresses 0000-07FE) are used internally in the Home Computer. The second 1K (adresses 0800-0FFE) are reserved for future use. The last 2K (addresses 1000-1FFE) are reserved for the peripherals to be plugged in the I/O port. A block of 128 CRU bits is assigned to each peripheral as listed below..

CRU ASSIGNMENTS

CRU ADDRESSES	A3	A4	A5	A6	A7	USE
0000-0FFE	0	X	X	X	X	INTERNAL USE
1000-10FE	1	0	0	0	0	RESERVED
1100-11FE	1	0	0	0	1	DISK CONTROLLER
1200-12FE	1	0	0	1	0	RESERVED
1300-13FE	1	0	0	1	1	RS 232 (I)
1400-14FE	1	0	1	0	0	RESERVED
1500-15FE	1	0	1	0	1	RS 232 (11)
1600-16FE	1	0	1	1	0	RESERVED
1700-17FE	1	0	1	1	1	RESERVED
1800-18FE	1	1	0	0	0	THERMAL PRINTER
1900-1FFE	1	1	X	X	X	FUTURE EXPANSION

INTERRUPT HANDLING

The interrupt available on the I/O port is one of the maskable interrupts of the TMS 9901 Programmable Systems Interface.

9900 INTERRUPTS

INTERRUPT LEVEL	VECTOR LOC. (MEMORY ADDR. IN HEX)	CPU PIN	DEVICE ASSIGNMENT
(Highest Priority) 0	0000	RESET	RESET
1	FFFC	LOAD	LOAD
	0004	INT1	EXT DEV (9901)

Lower priority CPU interrupt are not used. The additional interrupts available are implemented on 9901.

MEMORY READ CYCLE TIMING

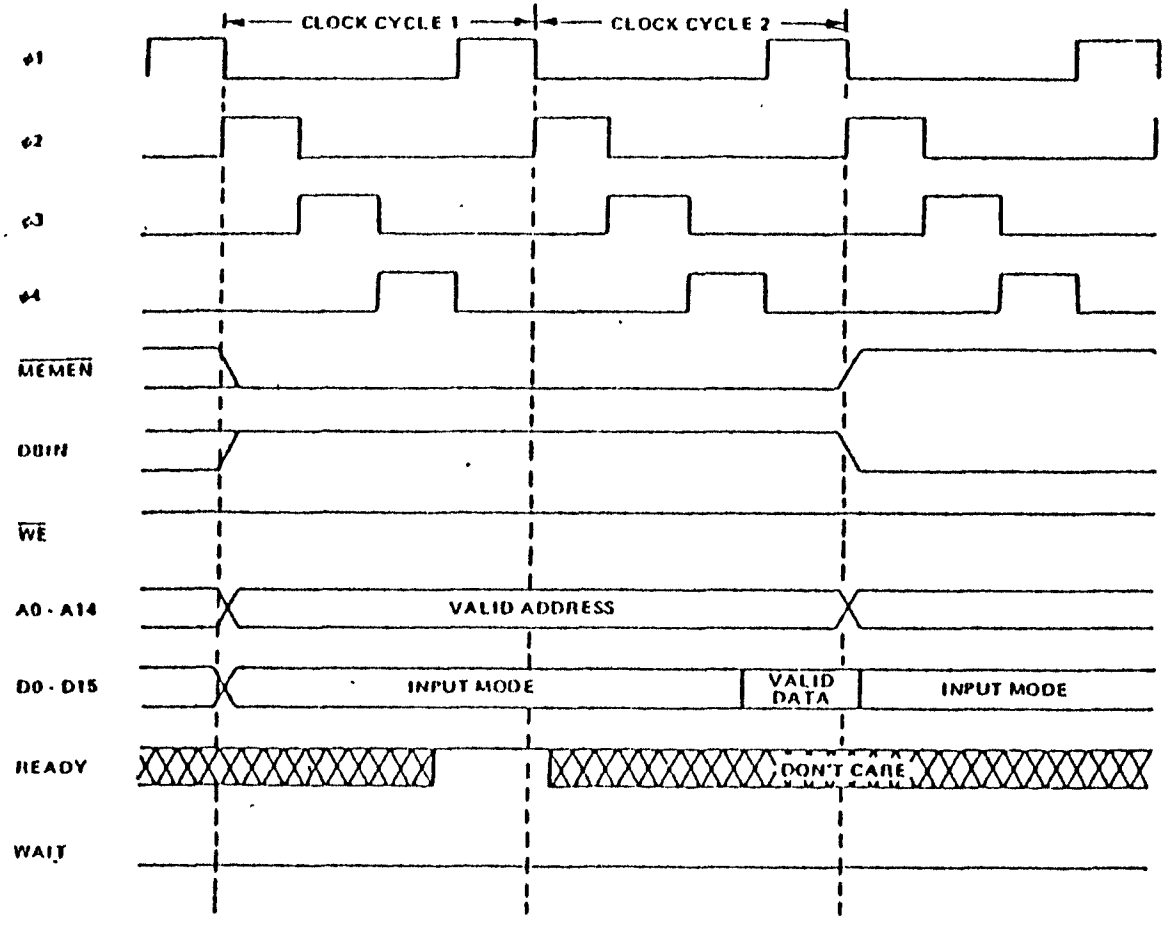


Fig. 5

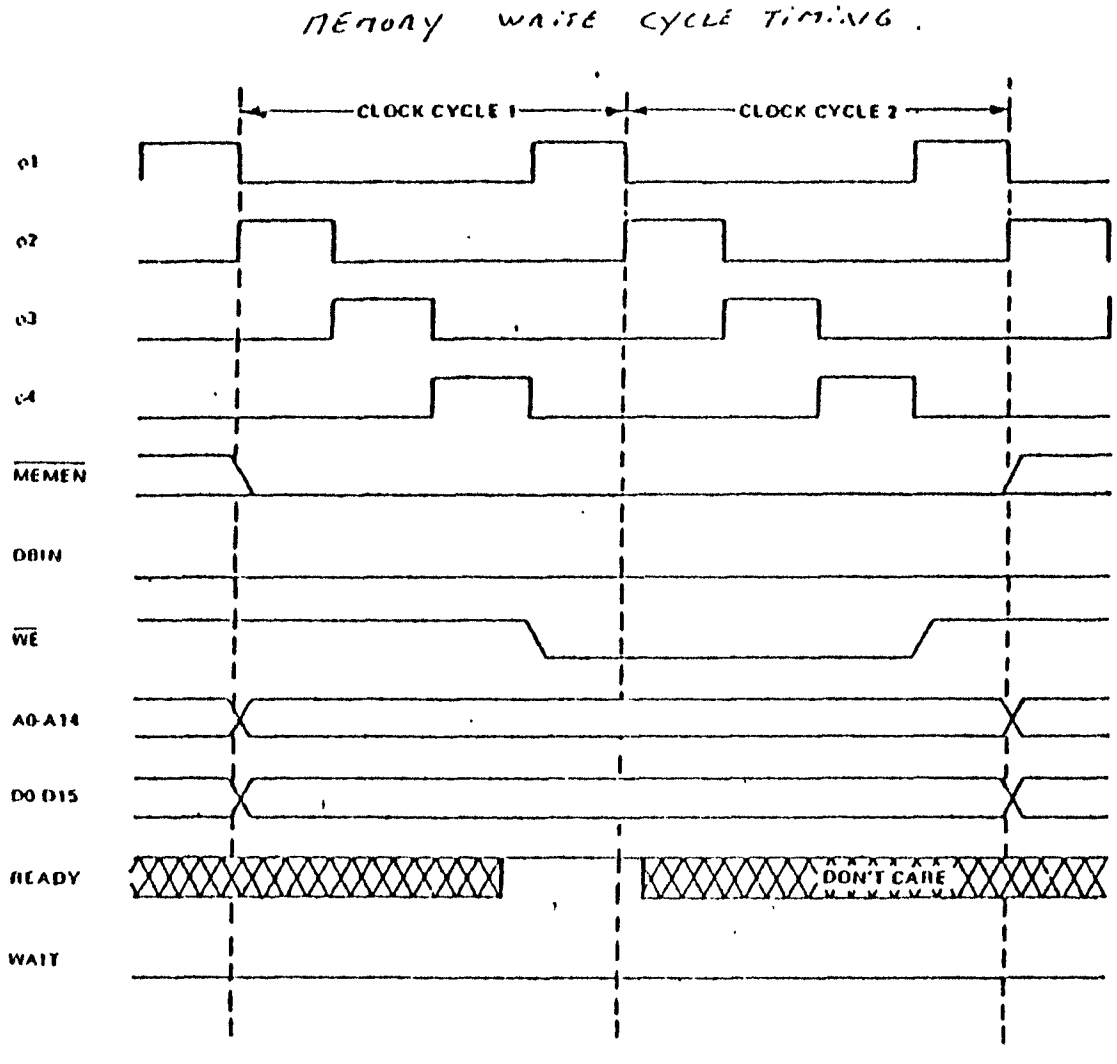

MEMORY WRITE CYCLE TIMING.
CLOCK CYCLE 1
CLOCK CYCLE 2
φ1
φ2
φ3
φ4
MEMEN
DBIN
WE
A0-A14
D0 D15
READY
DON'T CARE
WAIT

Fig. 6

MEMORY-READ CYCLE TIMING WITH ONE WAIT STATE

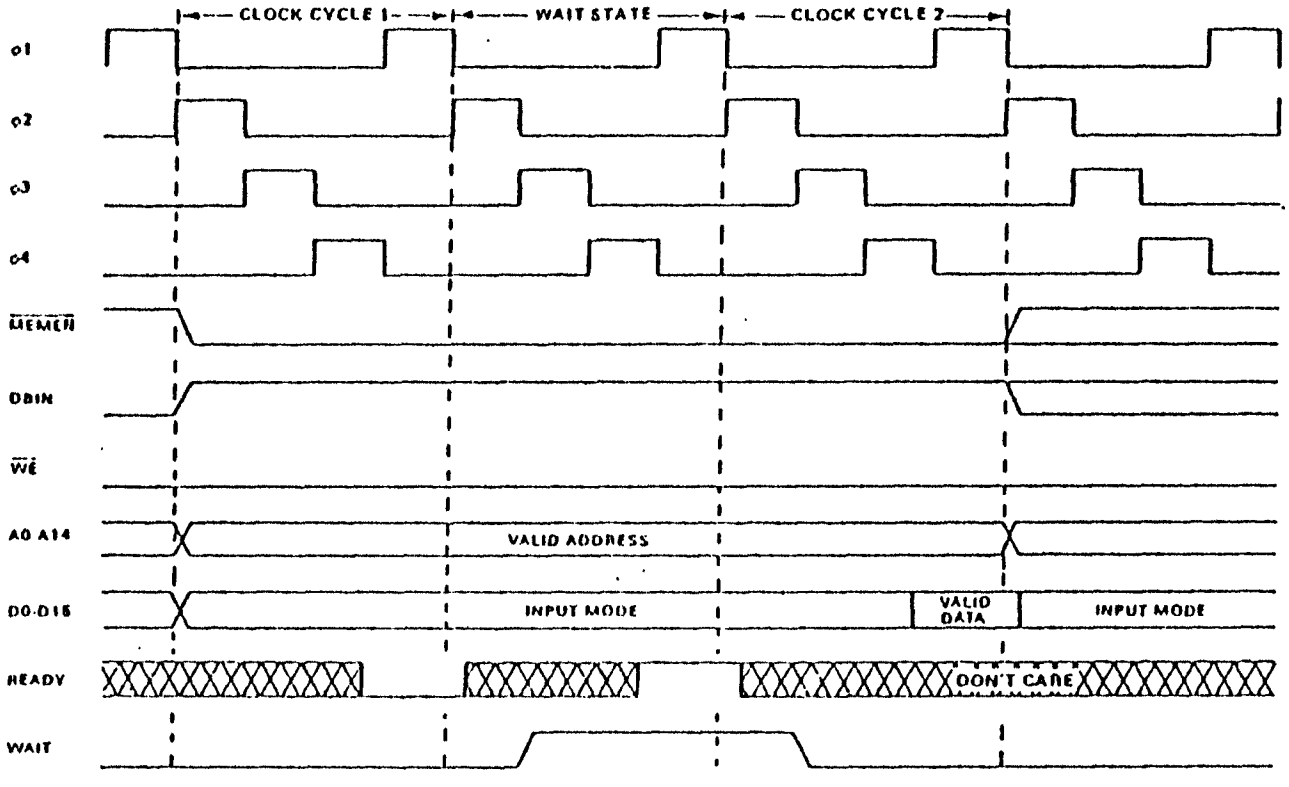


Fig. 7

DIRECT MEMORY ACCESS TIMING

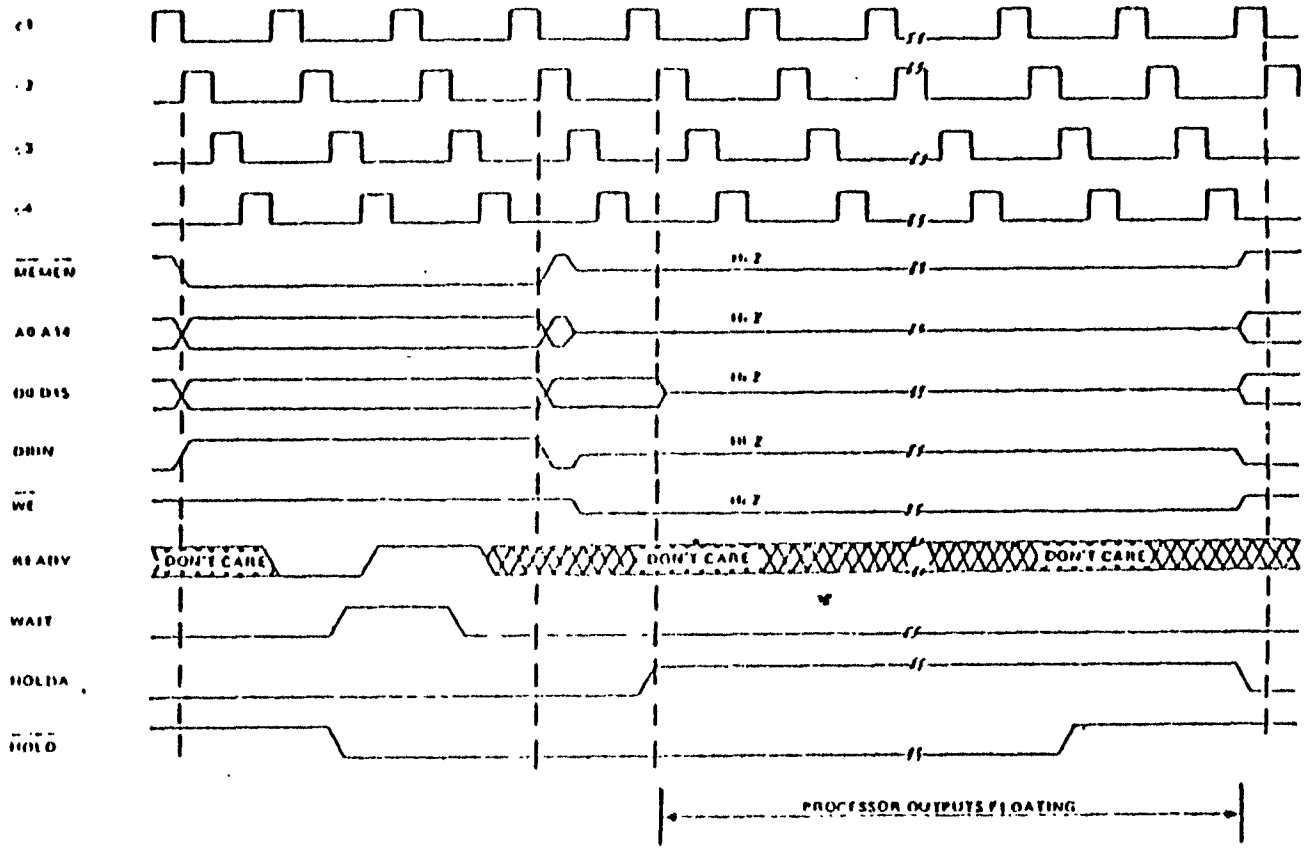


Fig. 9

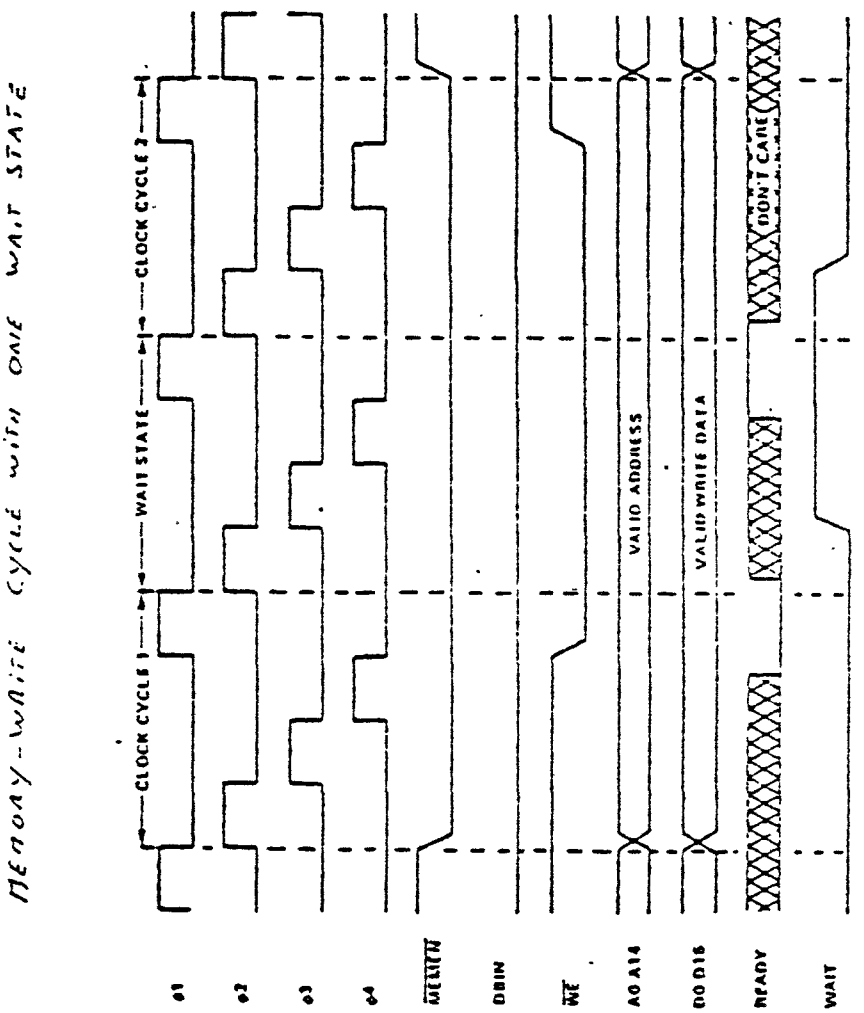

MEMORY-WRITE CYCLE WITH ONE WAIT STATE
CLOCK CYCLE 1
WAIT STATE
CLOCK CYCLE 2
Φ1
Φ2
Φ3
Φ4
MEMW
DBIN
WE
A0 A15
D0 D15
READY
WAIT
VALID ADDRESS
VALID WRITE DATA
DON'T CARE

Fig. 8

CRU INTERFACE TIMING.

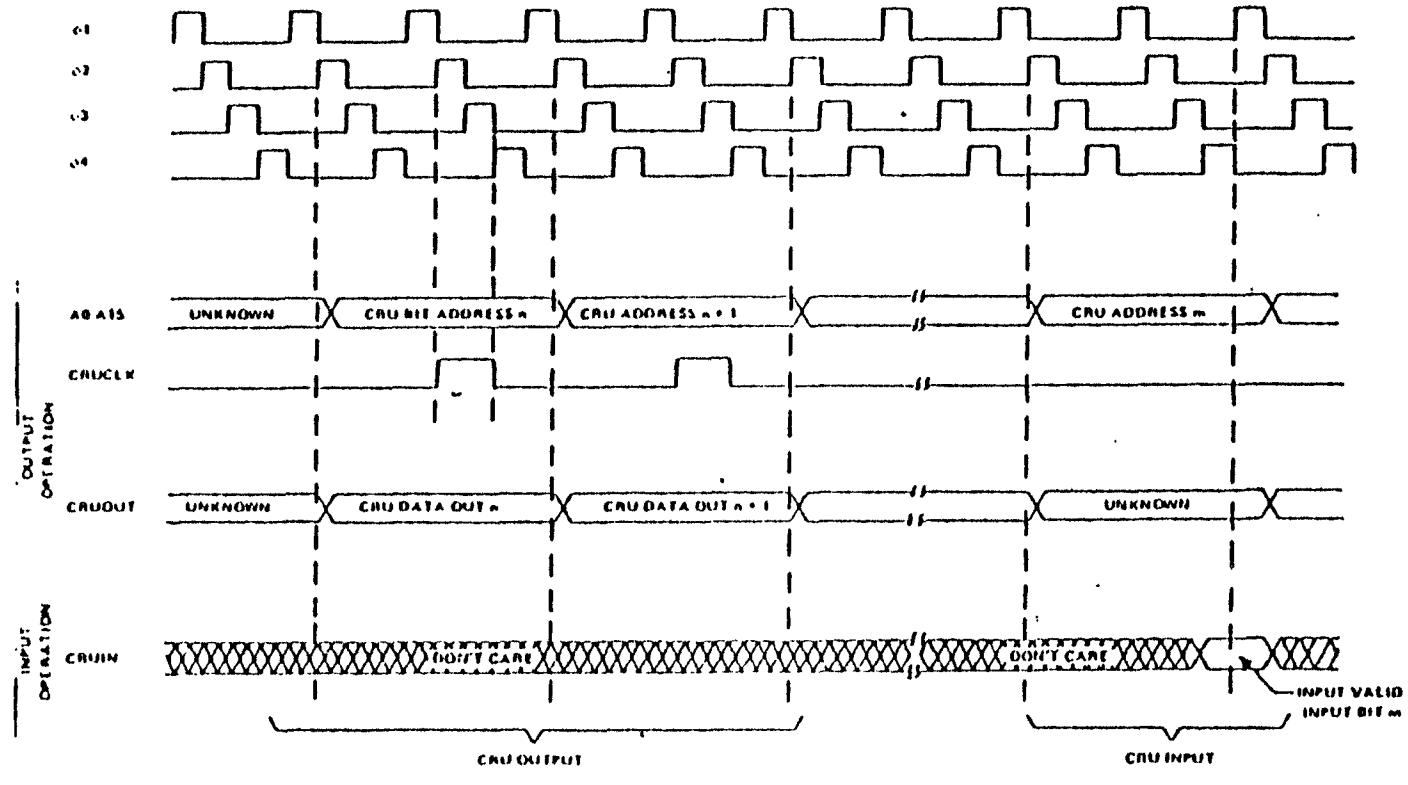


Fig. 10

TABLE 1. SUMMARY OF 9900 MICROPROCESSOR INSTRUCTIONS

Mnemonic	Instruction Code Description
A	Add Words
AB	Add Bytes
ABS	Absolute Value
AI	Add Immediate
ANDI	AND Immediate
B	Branch
BL	Branch and Link
BLWP	Branch and Load Workspace Pointer
C	Compare Words
CB	Compare Bytes
CI	Compare Immediate
CKOF	Clock Off (control instruction)
CKON	Clock On (control instruction)
CLR	CLEAR
COC	Compare Ones Corresponding
CZC	Compare Zeroes Corresponding
DEC	Decrement
DECT	Decrement By Two
DIV	Divide
IDLE	Idle (control instruction)
INC	Increment
INCT	Increment By TWO
INV	Invert

SUMMARY OF 9900 MICROPROCESSOR INSTRUCTIONS (CONTINUED)

Mnemonic	Instruction code Description
JEQ	Jump If Equal to
JGT	Jump If Greater Than
JH	Jump If Greater Than (Logic)
JHE	Jump If Greater Than Or Equal To (Logic)
JL	Jump If Less Than
JLE	Jump If Less Than Or Equal To (Lcgic)
JLT	Jump If Less Than
JMP	Unconditioned Jump
JNC	Jump If No Carry
JNE	Jump If Not Equal
JNO	Jump If No Overflow
JOC	Jump On Carry
JOP	Jump On Odd Parity
LDCR	Load CRU
LI	Load Immediate
LIMI	Load Interrupt Mask Immediate
LREX	Restart (control instruction)
LWPI	Load Workspace Pointer Immediate
MOV	Move (word)
MOVB	Move Byte
MPY	Multiply
NEG	Negative
ORI	OR Immediate
RSET	Reset (control instruction)

SUMMARY OF 9900 MICROPROCESSOR INSTRUCTIONS (continued)

Mnemonic	Instruction Code Description
RTWP	Return With Workspace Pointer
S	Subtract Words
SB	Subtract Bytes
SBO	Set Bit To Logic One
SBZ	Set Bit To Logic Zero
SETO	Set To One
SLA	Shift Left Arithmetic
SOC	Set One Corresponding
SOCB	Set Ones Corresponding
SRA	Shift Right Arithmetic
SRC	Shift Right Circular
SRL	Shift Right Logical
STCR	Store CRU
STST	Store Status
STWP	Store Workspace Pointer
SWPB	Swap Bytes
SZC	Set To Zeroes Corresponding
SZCB	Set To Zeroes Corresponding Bytes
TB	Test Bit
X	Execute
XOP	Extended Operation
XOR	Exclusive OR

MEMORY SELECTION LOGIC

GENERAL DESCRIPTION

The memory selection logic decodes the more significant address lines for selecting fast ROM and RAM memory. Also the output of the decoder is used for a second decoder, which selects internal devices such as VDP, sound etc...

HARDWARE DESCRIPTION

The schematics of the memory selection logic with a memory map is given in figure 11, p. 35.
When MEMEN is active, U504 (74LS138) decodes the three most significant address lines A0 through A3, dividing the address space in the following 8 blocks of 8 bytes.

BLOCK 0
Memory Block 0 (>0000->1FFF) is used to select the system read only memory (ROM).

BLOCK 1
Memory Block 1 (>2000->3FFF) is reserved for memory expansion.

BLOCK 2
Memory Block 2 (>4000->5FFF) is used to select read only memory in external devices, such as RS232 interface. The ROM in these devices contains the device service routine (MBE).

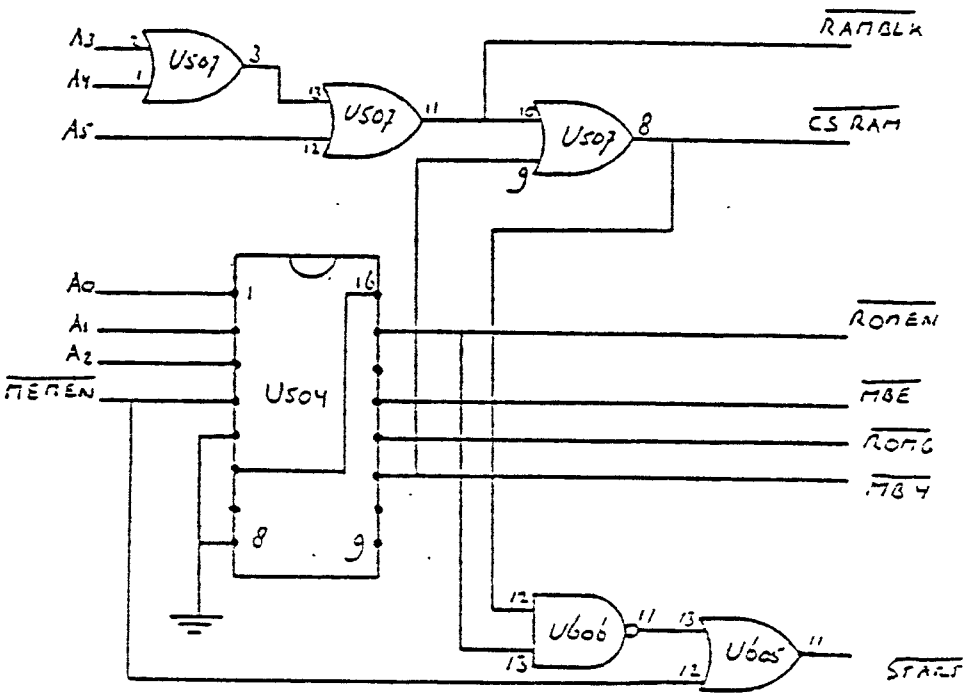
BLOCK 3
Memory block 3 (>6000->7FFF) is used for the optional read only memory in solid state software command modules (ROMG).

BLOCK 4
Memory block 4 (>8000->9FFF) is used divided in several parts. Memory locations >8000 to >83FF are used for the fast system read-and-write memory. This further decoding of the address space is done in or-gates U507. This part of the circuitry also generate the RAMBLK signed, which is used to select the TMS 9901 programmable system interface. Furthermore the MB4 signal is used to select a second 74LS138 which divides memory block 4 in more parts.

BLOCK 5, 6 AND 7
These blocks are used along with Block 1 for memory expansion.

START SIGNAL
By combining the CSRAM and ROMEN signals, together with MEMEN in NAND-gate U606 and OR-gate U605 the START signal is developed. This signal is used in the a16 to 8 bit interfacing circuit.

MEMORY SELECTION LOGIC



SIGNAL	ADDRESSED MEMORY LOCATION	USE
$\overline{\text{ROMEN}}$	0000 - 1FFF	SYSTEM ROM SELECT
$\overline{\text{MBE}}$	4000 - 5FFF	EXT. DEVICE ROM SELECT
$\overline{\text{ROMG}}$	6000 - 7FFF	SOFTWARE MODULE ROM SELECT
$\overline{\text{MB4}}$	8000 - 9FFF	MEMORY BLOCK 4

Fig. 11

MEMORY ALLOCATION

The memory address space is broken into 8 blocks of 8K bytes of memory. The third block (addresses 4000 - 5FFF) is predecoded and made available at the I/O port for the peripherals. The second sixth, seventh and eighth blocks (addresses 2000-3FFF and A000 - FFFF) are available for further expansion. For the speech module, (addresses 9000 - 97FF), a predecoded line is available at the I/O port.

SYSTEM MEMORY MAP

HEX ADDRESS

0 - 1FFF	Console ROM Space
2000 - 3FFF	Future Expansion (internal/console)
4000 - 5FFF	Peripheral expansion (predecoded to I/O Connector)
6000 - 7FFF	Game cartridge ROM/RAM (predecoded to GROM Connector)
8000 - 9FFF	Microprocessor RAM, VDP, GROM, SOUND and SPEECH select.
A000 - BFFF	Future Expansion
C000 - DFFF	Future Expansion
E000 - FFFF	Future Expansion

MEMORY MAPPED DEVICES

Addresses	A0	A1	A2	A3	A4	A5	A14	A15	USE
8000	1	0	0	0	0	0	0	0	Internal RAM (8300-83FF)
8400	1	0	0	0	0	1	0	0	Sound
8800	1	0	0	0	1	0	0	0	VDP Read Data
8802	1	0	0	0	1	0	1	0	VDP Read Status
8C00	1	0	0	0	1	1	0	0	VDP Write Data
8C02	1	0	0	0	1	1	1	0	VDP Write Address
9000	1	0	0	1	0	0	0	0	Speech Read
9400	1	0	0	1	0	1	0	0	Speech Write
9800	1	0	0	1	1	0	0	0	GROM Read Data
9802	1	0	0	1	1	0	1	0	GROM Read Address
9C00	1	0	0	1	1	1	0	0	GROM Write Data
9C02	1	0	0	1	1	1	1	0	GROM Write Address

ROM & RAM MEMORY

GENERAL DESCRIPTION

The 99/4A Home Computer uses 8K bytes of read only memory for execution of fast system routines.
It has also 256 bytes of random access memory which is used as a scratchpad memory.

READ ONLY MEMORY

The 99/4A uses the TMS 4732 as a read-only memory. This device contains 32K bits of read-only memory. It is housed in a 24 pin dual in line package and uses a single 5 volt supply voltage. 12 address lines are used to select 4K bytes of 8 bits.
The device uses two chip select inputs, which both have to be active (low) to select the device.

READ-AND-WRITE MEMORY

The 99/4A uses the MCM 6810 as random access memory. The MCM 6810 is housed in a 24 pin dual in line package and uses a single 5 volt supply voltage. 7 address lines are used to select 128 fields of 8 bits. 6 pins are available for device selection, of which two have to be low and four have to be high to select the RAM.
Another pin (R/W) is provided to distinguish between writing and reading of data.

HARDWARE DESCRIPTION

Hardware connections to ROM and RAM memory are given in figure 12, p. 38.

RAM MEMORY

Two RAMS (U608 & U609) are connected in parallel to generate a 16 bit data bus, as is required by the TMS 9900. The devices are selected by the RAMCS signal, generated by the memory selection logic. Distinction between reading and writing is made by connecting the WE signal of the TMS 9900 to the R/W PIN 16. Address lines A8 through A14 are used to select the proper memory locations.

ROM MEMORY

Both ROMS are connected in paralel to generate the required 16 bit data bus.
The ROMS are selected by the ROMEN signal, generated by the memory selection logic. This signal is applied on pin 20.
Address lines A3 through A14 are used to select the proper memory locations.

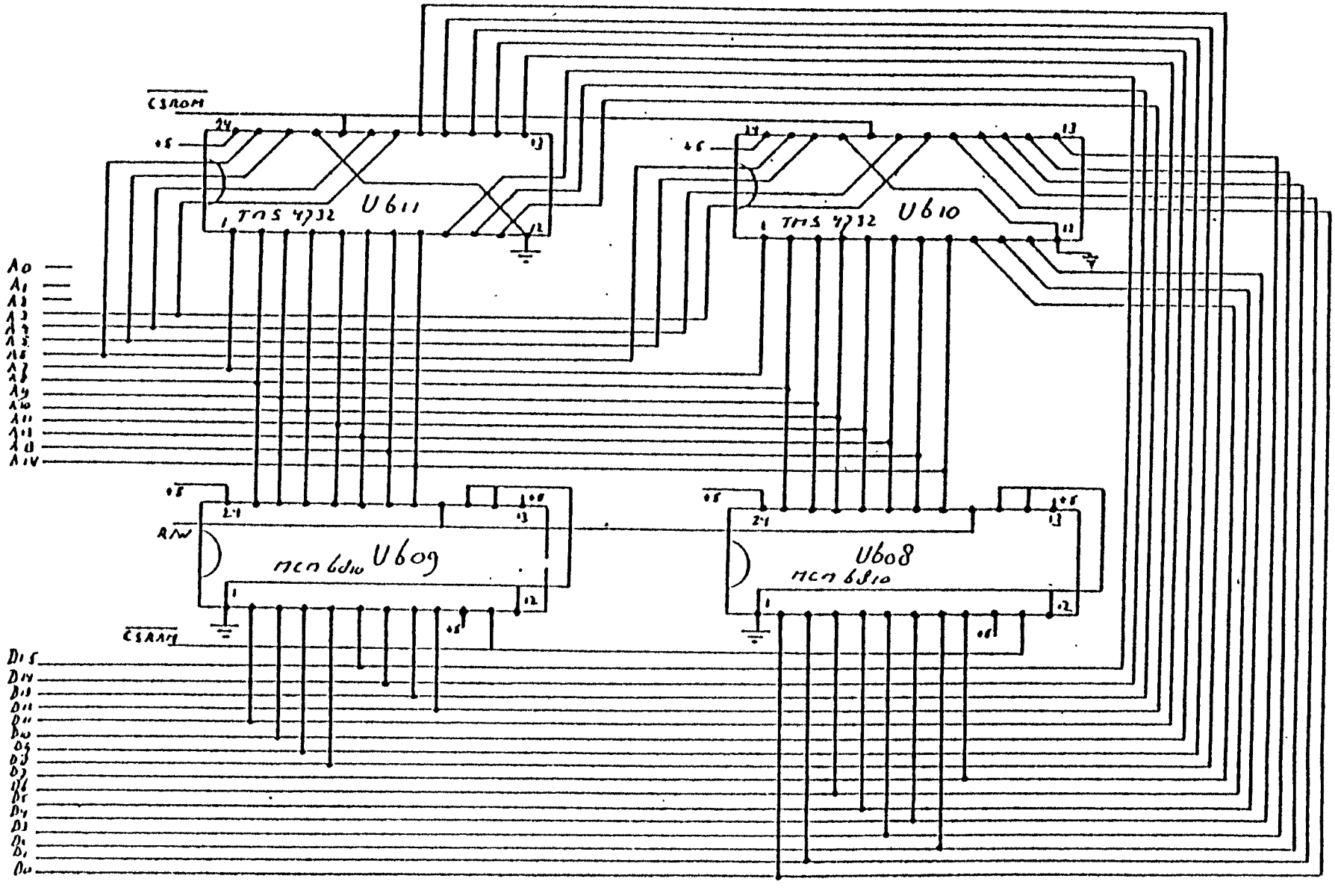

ROM & RAM Memory.
CSROM
TMS 4732
U611
TMS 4732
U610
MCM 6810
U609
MCM 6810
U608
CSRAM
R/W

Fig. 12

16 TO 8 BIT INTERFACING CIRCUIT.

GENERAL DESCRIPTION

The 16 to 8 bit interfacing circuit is used to interface 8 bit devices such as Video Display Processor (VDP). The sound chip, graphics-read-only memory (GROM) and external 8 bit peripherals to the 16 bit data bus of the TMS 9900. It does so by successively placing the least significant and most significant byte of a word on the 8 bit system data bus during a write operation. During a read operation adjecent bytes are placed in the least significant and most significant byte of the 16 bit word. To enable 8 bit devices to destinguish between the bytes, an additional address line A15 is generated. The interfacing circuit also performs the synchronization between devices connected to the 8 bit system databus and the the TMS 9900 by generating adequate timing of the WE and READY signals.
A schematic of the interfacing circuit is given in figure 13, p. 41.

HARDWARE DESCRIPTION

The hardware description is divided in the following parts:

A. Description of the 16 to 8 bit multiplexing circuit.
B. Generation of the control signals for the multiplexing circuit.
C. READY/HOLD generation.
D. WE gernation.

A. 16 TO 8 BIT MULTIPLEXING CIRCUIT

An overview of the hardware used to interface the 16 to 8 bit data uses is given in figure 13, p. 41.
During a write operation the data on the 16 bit bus is gated to the 8 bit system bus by enabling U616 and U614 in succession. During a read operation the least significant byte on the 8 bit data bus is stored in the 8 bit latch U615. Then the most significant byte is gated to the 16 bit data bus by enabling bidirectional buffer U614 and the total word is fetched by the TMS 9900. The DIOG and DBIN on U614, DING and A15 on U615 and the DOG on U616 are used for enabling IC's and for determining the direction of the data flow.
If no interfacing occurs, the 16 bit data bus is kept floating to allow the TMS 9900 to access ROM or RAM memory.

B. CONTROL SIGNAL GENERATION

Control signal for the multiplexing circuit are generated by the circuit in figure 14, p. 42.
U613 is a 4 bit shift register of which the outputs are used for timing purposes.
When the START signal is high, pin 2 of U604 is low. This pin, connected to pin 1 of U613, sets all the outputs of the shift register to a binary zero. Since the START signal is also connected to pin 10, the shift register is disabled. Control signal generation is started when START becomes low, pin 10 which becomes also low selects the right shift mode of shift register U613.
Shift operation is then started as soon as pin 9 of U613 becomes high,

depending on the system ready status. When the shift operation has begun shift output QC on pin 13 inverted in U602 and fed back to the right shift input on pin 2. On every rising flank of Q1 (pin 11) the contents of the shift registers are shifted one position, giving timing signals on the outputs Qa, Qb and Qc (see figures 7-10, pp. 45-46).
These outputs are used for generating the control signals in NAND-gates U603 and U606. Both DBIN and $\overline{\text{DBIN}}$ are used for selecting the direction of the data flow.
CSVDPR disables U614 if a read from the video display processor occurs, this because the VDP data bus is directly connected to D1-D7 of the TMS 9900.

C. READY GENERATION

The READY generation circuit as shown in fig. 15, p 43 has two operation modes. In the normal mode the system ready signal is input on pin 12 of U607. The pull-up resistor R508 assures that under normal circumstances the READY signal is true.
Slow devices can add wait states by connecting pin 12 of U607 to ground. The READY signal is sampled on Q2 and available on pin 9 of U607.

THERE ARE NOW TWO POSSIBILITIES:

ROM OR RAM IS SELECTED

In this case shift register U613 is not enabled and the READY signal is gated directly via U603 and U602 to the READY/HOLD input of the TMS 9900. Note that in this case PIN 12 of U603 has to be high.

EXTERNAL READY TIMING

If other devices than ROM or RAM are selected, the 16 to 8 bit interfacing circuit will be used. This means that the TMS 9900 has to be put in a WAIT state until two bytes of data are written or read by the interfacing circuit. This is accomplished by decoding the Qa and Qc outputs of the shift register in NAND-gates U612 and U603 to provide a low READY signal until both bytes are processed by the interfacing circuit.
If during this operation a device generates a not READY, the shift register will stop its operation until ready becomes high again. Timing diagrams for the READY signal can be seen in figures 7-8, pp 27-28.

$\overline{\text{WE}}$ GENERATION

The WE circuit as given in fig. 16, p 44 generates the $\overline{\text{WE}}$ signals when writing data to an external device. In that case $\overline{\text{WE}}$ of the system has to be low every time a byte of information is transferred.
To accomplish this, outputs Qb, on PIN 14 and Qc on pin 13 of U613 are used to set and preset flip flop U607 on pin 2 and 4. In this way two periods of 2 clock cycles long for which $\overline{\text{WE}}$ is low are generated on pin 3 of U606. Q4 is used to clock U607 to assure that $\overline{\text{WE}}$ is going low on the rising edge of Q4, which is in agreement with TMS 9900 timing. $\overline{\text{WE}}$ is only gated to external devices when a memory write is accomplished by combining the $\overline{\text{WE}}$ of the TMS 9900 after inverting in U602 with the $\overline{\text{WE}}$ of the interfacing circuit. The total signal is then available of pin 3 of U606.

16 TO 8 BIT MULTIPLEXING CIRCUIT

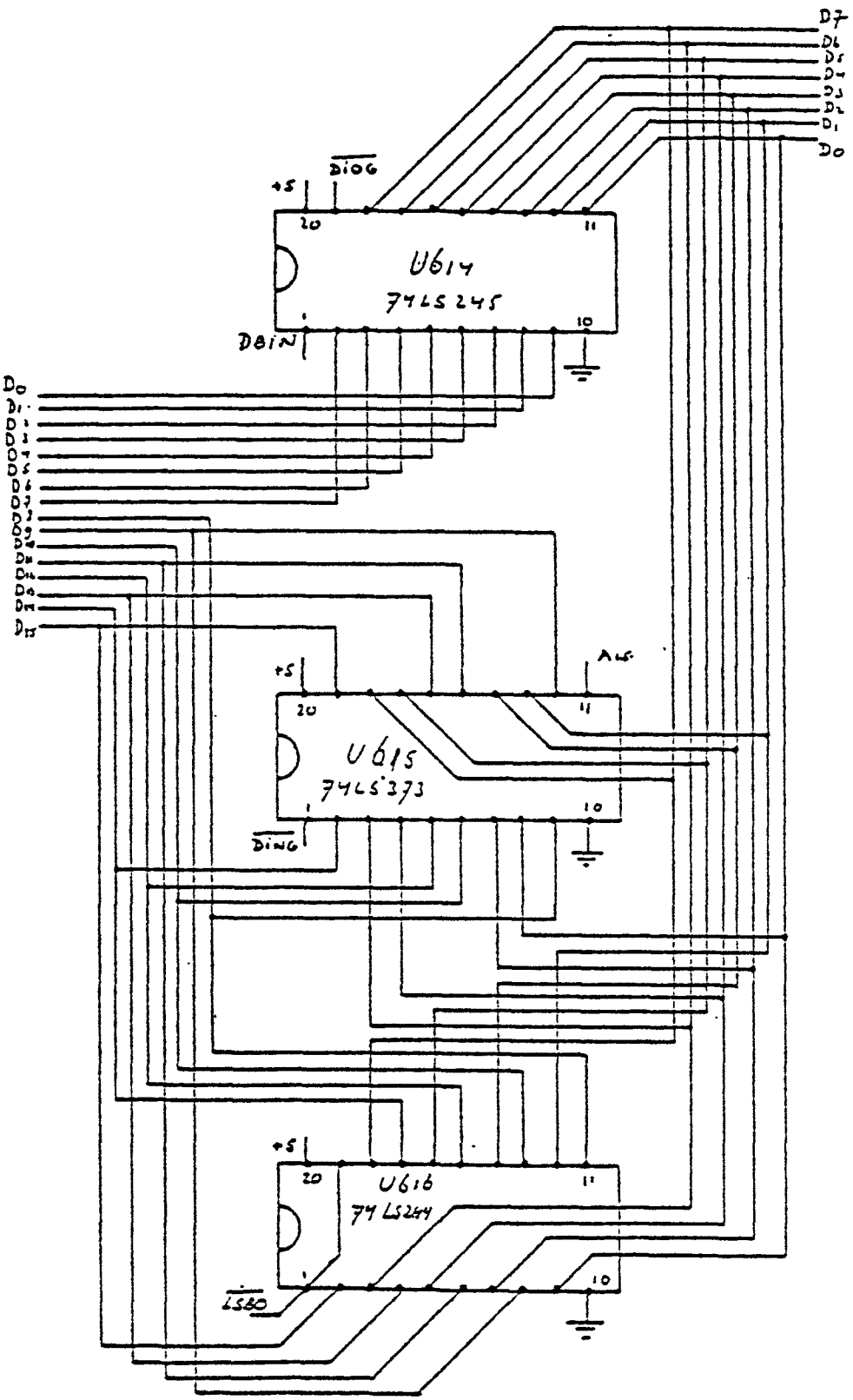
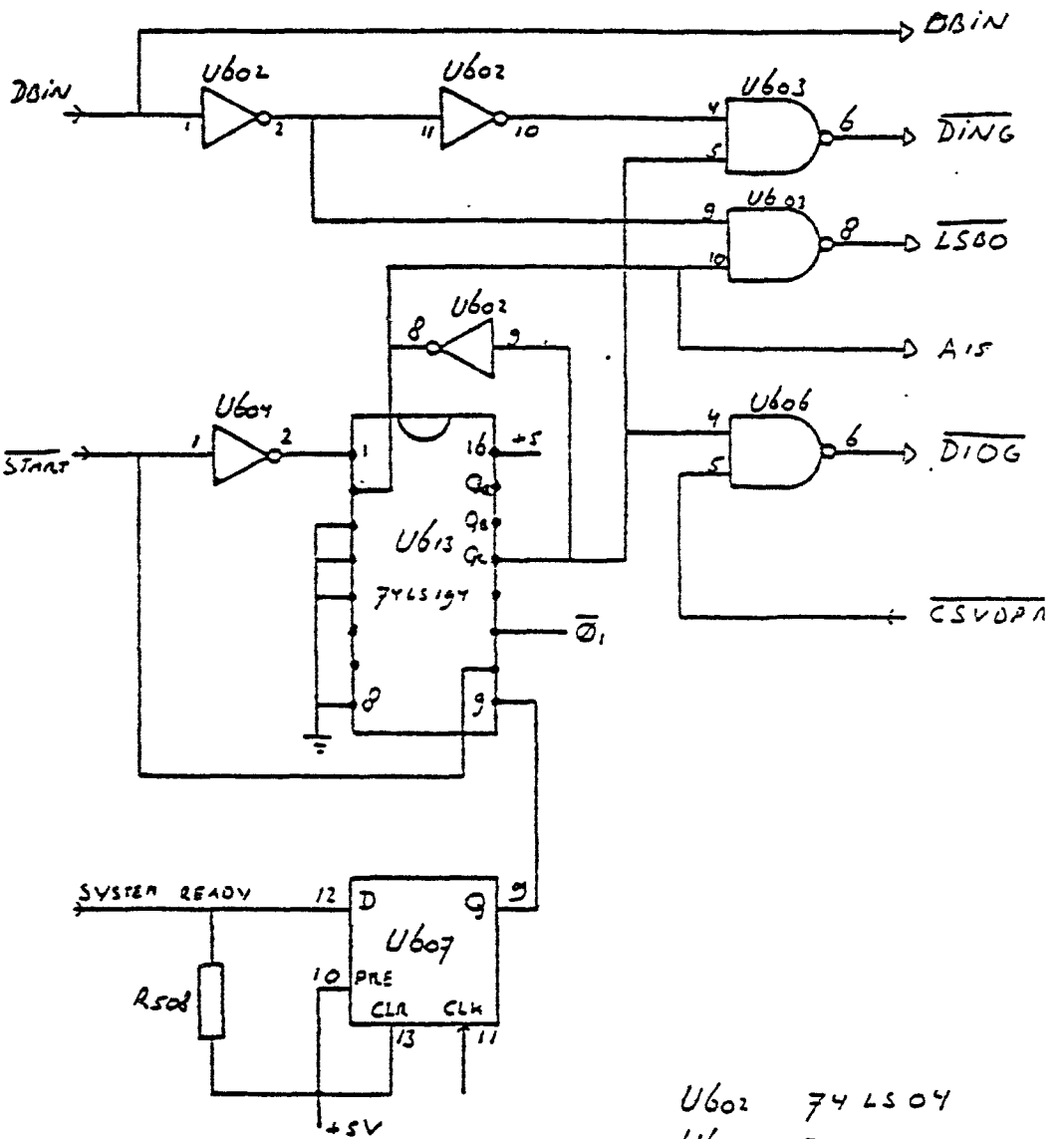


Fig. 13

CONTROL SIGNAL GENERATION.



U602	74 LS 04
U603	74 LS 00
U604	74 LS 04
U606	74 LS 00
U607	74 LS 74
U613	74 LS 194
R508	4.7 KΩ

Fig. 14

CPU READY GENERATION.

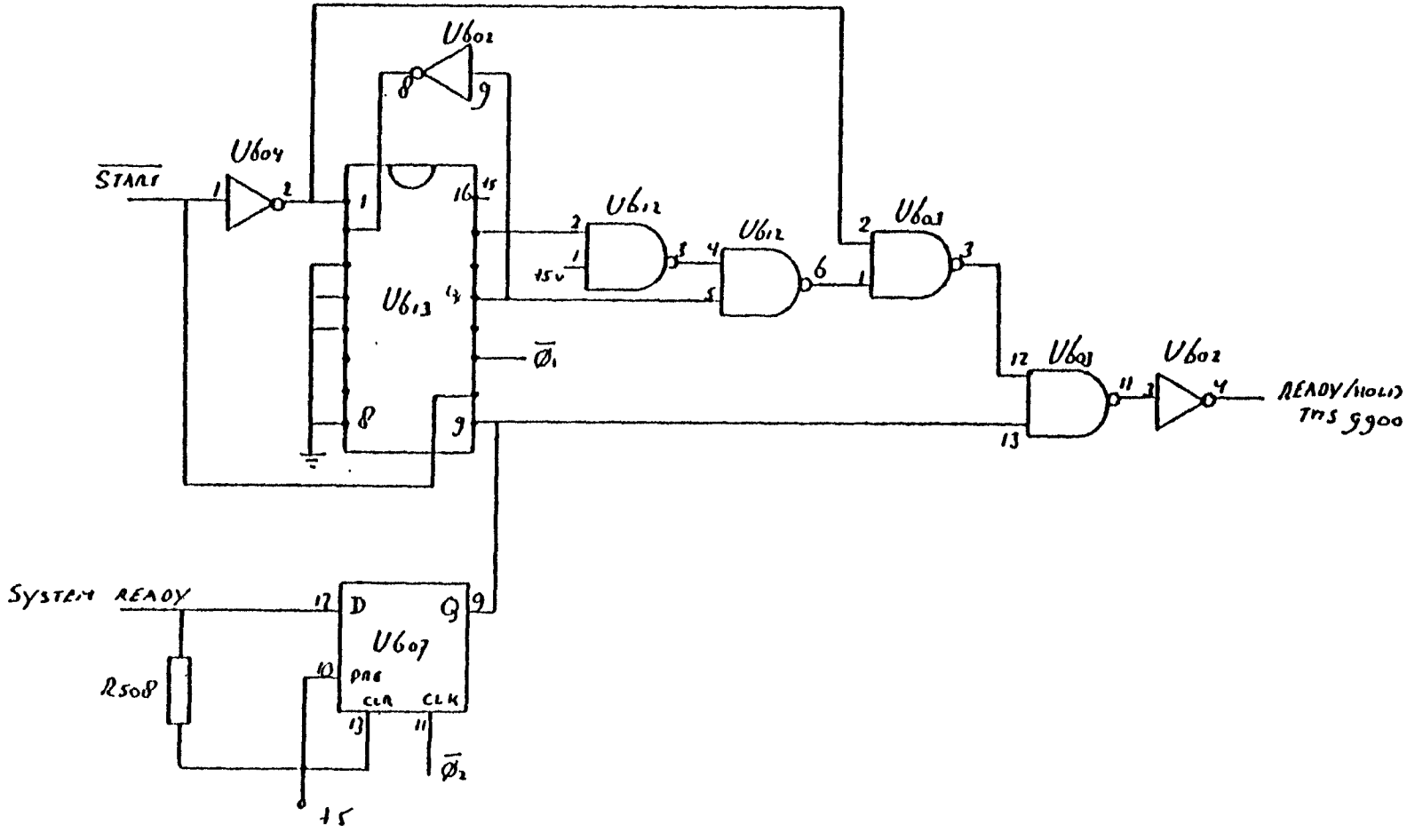


Fig. 15

$\overline{WE}$ GENERATION

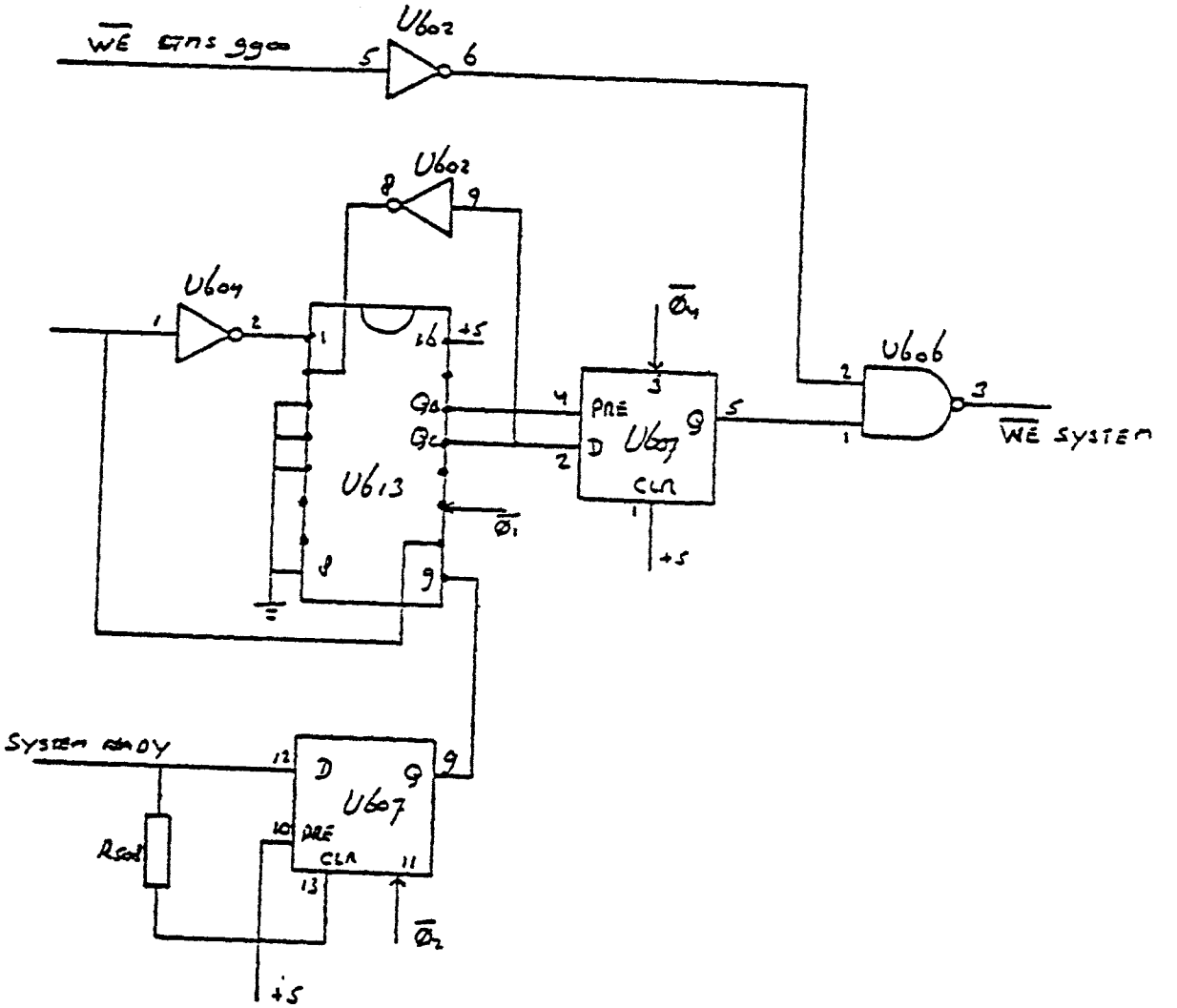


Fig. 16

EXTERNAL CPU - WRITE TIMING

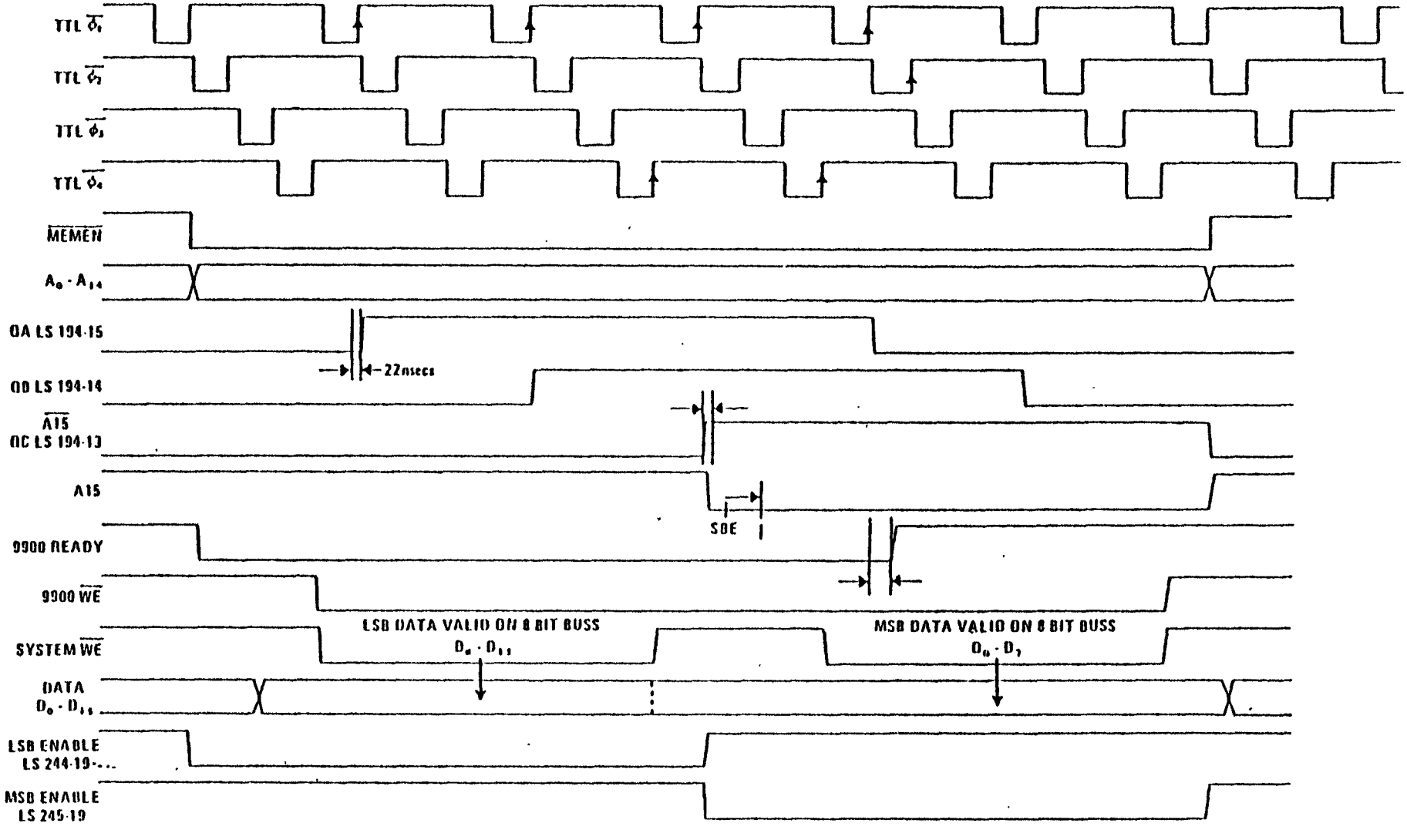


Fig. 17

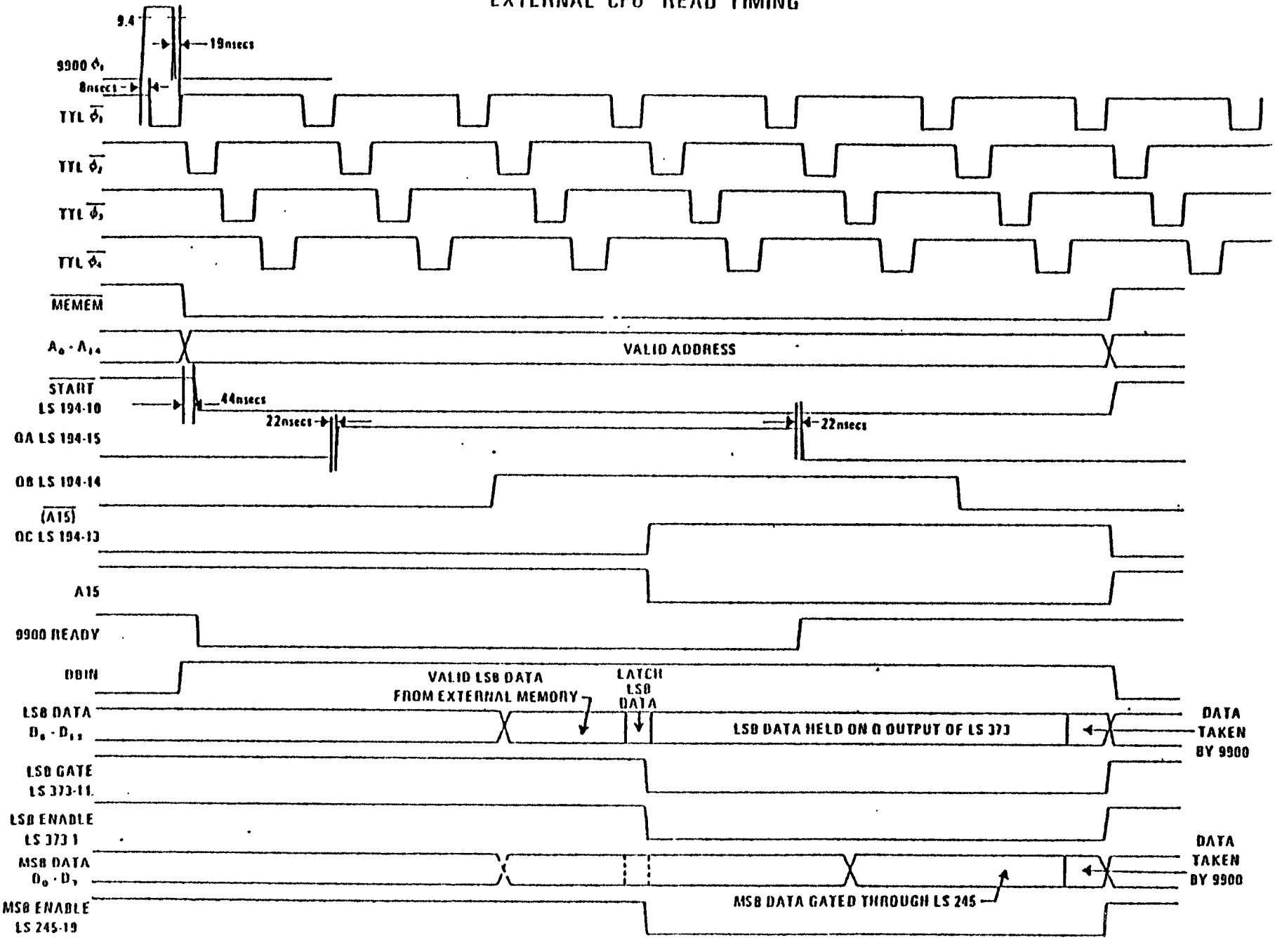

EXTERNAL CPU READ TIMING
9.4
19nsecs
9900 ϕ_1
8nsecs
TTL $\overline{\phi_1}$
TTL $\overline{\phi_2}$
TTL $\overline{\phi_3}$
TTL $\overline{\phi_4}$
MEMEM
A_0 - A_{14}
VALID ADDRESS
START
LS 194-10
44nsecs
22nsecs
22nsecs
QA LS 194-15
QB LS 194-14
(A15)
QC LS 194-13
A15
9900 READY
DBIN
VALID LSB DATA
FROM EXTERNAL MEMORY
LATCH
LSB
DATA
LSB DATA
D_8 - D_{15}
LSB DATA HELD ON Q OUTPUT OF LS 373
DATA
TAKEN
BY 9900
LSB GATE
LS 373-11
LSB ENABLE
LS 373 1
MSB DATA
D_0 - D_7
DATA
TAKEN
BY 9900
MSB DATA GATED THROUGH LS 245
MSB ENABLE
LS 245-19

Fig. 18

GROM READ TIMING

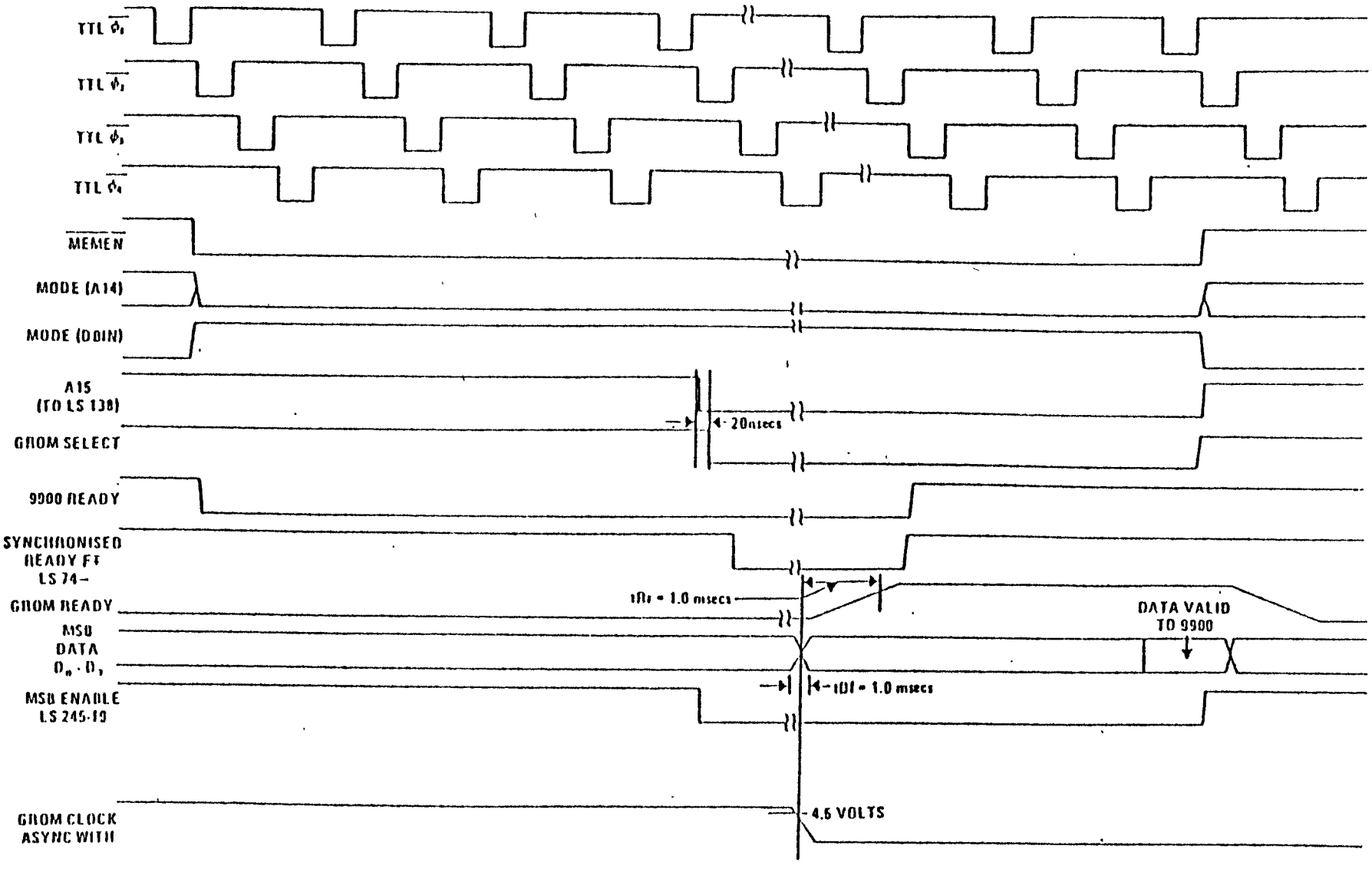


Fig. 19

GRAPHIC READ ONLY MEMORY

GENERAL DESCRIPTION

The TMC 0430 GROM is a P-channel read only memory containing 6144 8-bit bytes.
The circuit has an on chip autoincrementing address counter which selects one of the 6144 memory bytes.

FUNCTIONAL DESCRIPTION

CPU INTERFACE

The GROM interfaces to the CPU through the parallel data bus and the memory control lines as shown in fig. 3.9.32. The CPU interface consists of 8 data I/O lines (D0-D7), chip enable (CE), READY, and 2 mode control lines (M0, M1). The GROM also requires a nominal 500 kHz clock input (OSC).

GROM PAGING

The GROM has a 16-bit address register of which the lower 13-bits are used to address the 6144-byte ROM matrix. The most significant 3-bit field is used to select on of eight GROM pages. Each GROM has fixed 3-bit page number which is determined during manufacture. The GROM compares this number with the address register page select field. If a match occurs, then the GROM is the "selected page" or "current page". The GROM data bus is placed into the output mode during a read data operation only if the GROM is the current page. The other GROM functions are not affected by the page select field. The page select field permits up to eight GROMs to be used in parallel. Each GROM is tied to same chip enable, memory control, and data lines as the other GROMs. Since the page select field does not affect the data register or address register operations, all parallel GROMs are synchronized following initialization. However, since only one GROM is the current page, only one GROM outputs data on the data bus during a read data operation. If no GROM is selected (the address register page field does not match the page number of any GROM), then no GROM is placed into slaced into the output mode during a read data operation. During a read address operation. During a read address operation, all GROMs output the address byte. Since all GROMs are synchronized following initialization no data bus conflict occurs.

ADDRESS REGISTER AUTINCREMENTATION

The address counter is autoincremented following a read data, write data, or a pair of consecutive write address opetations. When the current address is 8191, the next autoincrement cycle will result in a zero address value. The page select field is not affected by the autoincrement.

When the value of the address register lower 13-bit field is greater than 6143, the GROM will continue to fetch data from the 6144 byte array. This condition should be avoided in order to prevent invalid data fetches and transfers.

INITIALIZATION

During the power up sequence, the microprocessor should execute a

"dummy" read data operation. This will guarantee that a newly powered up GROM will not respond to the first write address operation as if it were the second write address operation.
The microprocessor should then initialize the GROM address registers with two consecutive write-address operations.

READY

The GROM ready line is normaly low and is high only when the GROM has an active CE and has read in the contents of the data bus during a write operation or has placed data on the bus during a ready operation. The READY line control is independent of the page select. Typical READY line timing is shown in figure 21, p. 53.

ACCESS DELAY

The GROM requires that a second I/O operation not occur before it has completed the first operation. Consequently, CE must remain high at least 2.5 GROM clock cycles following the trailing edge of the last I/O operation. For a nominal 500 kHz OSC input, the minimal required delay between the rising edge of CE and the next falling edge is 5 microseconds.

I/O OPERATIONS

When CE becomes active (low), the mode lines determine which one of four GROM I/O operations is to occur as shown in table .

TABLE 2 GROM I/O OPERATIONS

MODE		
MO	M1	I/O OPERATION
0	0	WRITE DATA - The write data operation in included for use in future read/write versions of the GROM. The write data operation does not result in a data transfer to the TMC 0430 GROM. The address register is then autoincremented. The addressed ROM byte is fetched and placed into the GROM data register.
0	1	READ DATA - The read data operation transfers the data byte in the data register to the CPU if the GROM is the current page. The address register is then autoincremented. The addressed ROM byte is fetched and placed into the GROM data register.
1	0	WRITE ADDRESS - The write address operation transfers the data byte on the GROM data I/O bus to the least significant byte (LSB) of the GROM address register. The old address register (LSB) is transferred to the address register most significant byte (MSB). Two consecutive write addressoperations cause the addressed ROM byte to be fetched and placed into the GROM data register; the address register is then autoincremented. A

A write address operation immediately following a read data, read address, or write data operation does not result in a data fetch and address autoincrementation.

1 1 READ ADDRESS - The read address operation transfers the MSB of the address register to the CPU if the GROM is the current page. The address register LSB is automatically transferred to the MSB.

It should be noted that the M0 line controls whether the data or address register is to be affected and the M1 line controls whether the operation is an input or output cycle.

HARDWARE DESCRIPTION

The 99/4 has three internal GROMS (TMC 0430) and the possibility to add 5 more external GROMs via the GROM port. All GROMs are connected in parallel as can be seen in figure 52, p. 132.

GROM CLOCK

The clock signals for the GROMs are derived from the TMS 9918 video display processor. The clock cycle time is 2.24 usec. A 1K ohm pull-up resistor is used to ensure proper functioning of the P-channel device with TTL logic.

DATA BUS INTERFACING

All GROMs are connected in parallel to the 8 bit data bus.

MODE CONTROL

The type of operation performed by the GROM is determined by connections DBIN to M1 and address line A14 to M0. Thus a read operation is performed when DBIN is high and a write operation when DBIN is low. Address line A14 distinguishes between data and address operations.

GROM SELECT

GROM selection is performed by the circuit in fig. 93, p. 152. when MEMEN is low, U504 decodes address lines A0, A1 and A2. Decoder output Y4 is used to select a second 3 to 8 decoder U505. This device is enabled when A15 and one or both signals DBIN and A5 are low. Decoding of address lines A3, A4 and A5 are then used to select the GROMs by "ANDing" outputs Y6 and Y7 by mean of the NAND U506 and inverter U508.

GROM READY

The GROM ready signal is connected to the READY/HOLD via U508 and U506. U508 inverts the GROM READY signal. This signal is then combined in NAND-GATE U506 with the GROM select signal to get the appropriate signal for the system READY/HOLD line.

MEMORY MAP

Table 3 shows the memory map for the successive GROM instructions.

TABLE 3

GROM MEMORY MAP

ADDRESS	TYPE OF INSTRUCTION
9800	READ GROM DATA
9802	READ GROM ADDRESS
9C00	WRITE GROM DATA
9C02	WRITE GROM ADDRESS

As can be seen address A14 distinguishes between an address and data instruction. Distinction between read and write instructions is made by DBIN and the different addresses. This is done because when writing data or address information, the 9900uP executes a dummy read which would otherwise influence the address counter in the GROM.

GROM SELECTION & READY LOGIC.

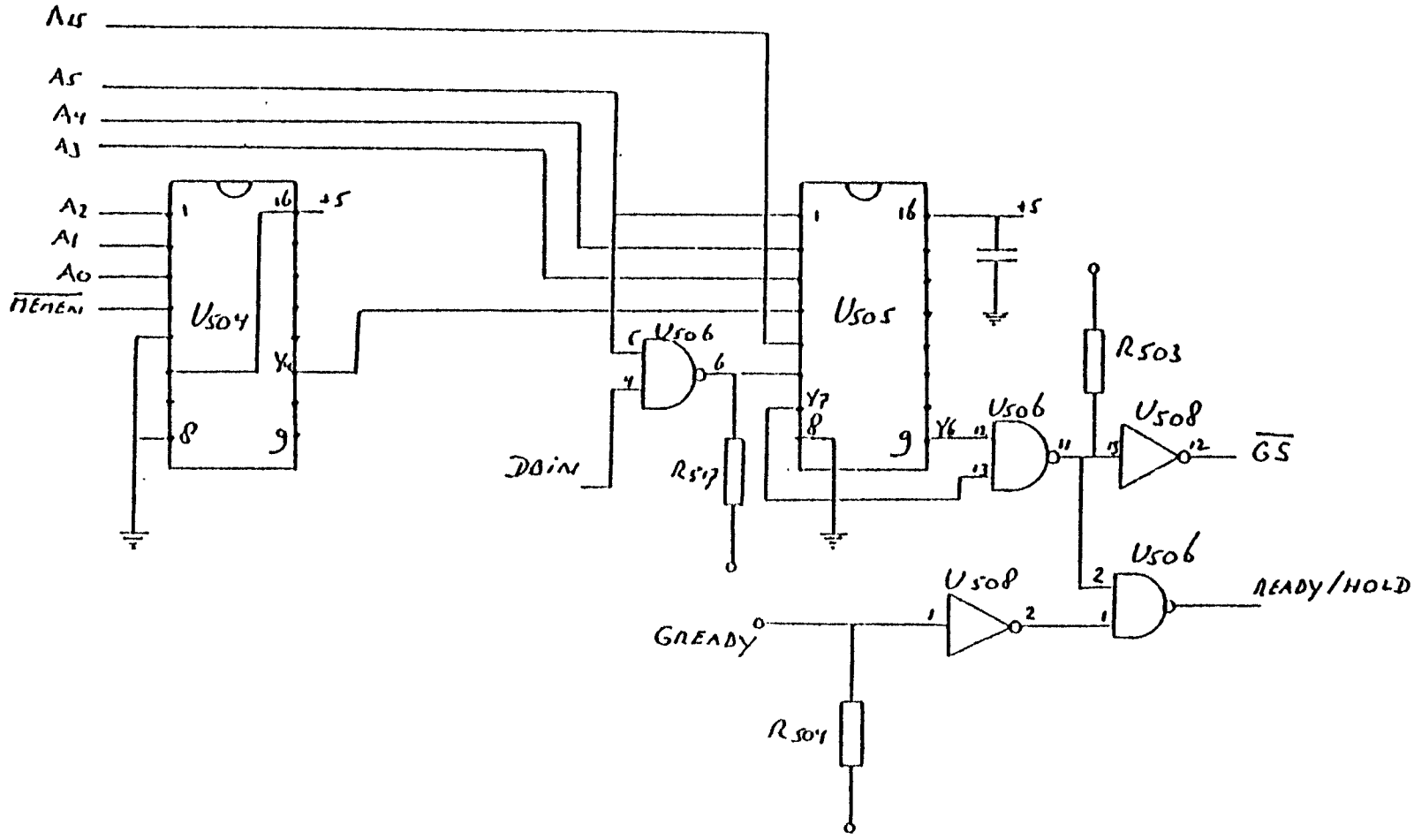
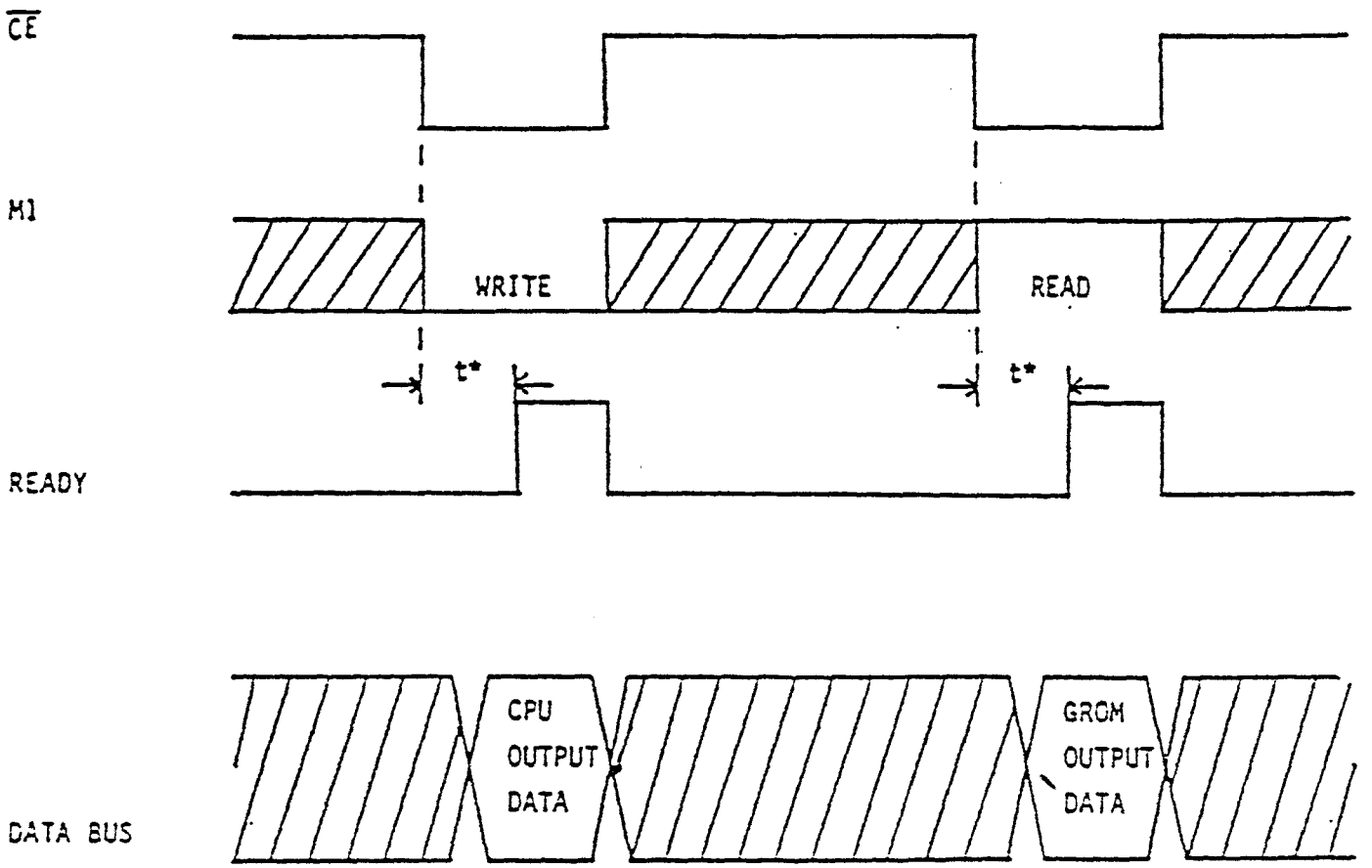


Fig. 20

FIGURE 21 READY TIMING



* t $\overline{CE}$ to READY time $\sim$ 6 µsec

Fig. 21

TMS 9901 PROGRAMMABLE SYSTEM INTERFACE

GENERAL DESCRIPTION

The TMS 9901 is a programmable system interface (PSI), which can be used for input, output and interrupt priority handling. It also features an on chip programmable interval timer. The TMS 9901 is used for keyboard, remote handheld control unit, cassette recorder interfacing and VDP interrupt handling in the 99/4 system.

The TMS 9901 PSI interfaces to the CPU through the Communication Register Unit (CRU) and the interrupt control lines. The TMS 9901 occupies 32 bits of CRU input and output space. The five least significant bits of the address bus are connected to the PSI to address one of the 32 CRU bits of the TMS 9901. The most significant bits of the address bus are decoded on CRU cycles to select the PSI by taking its chip enable (CE) line active (low).

Interrupt inputs to the TMS 9901 PSI are sychronized with Q3, inverted, and then ANDed with the appropriate mask bit. Once every Q3 clock time, the prioritizer looks at the 15 interrupt input AND gates & generates the interrupt control code. The interrupt control code and the interrupt request line constitute the interrupt interface to the CPU.

After reset all I/O ports are programmed as inputs. By writing to any I/O port, that port will be programmed as an output port until another reset occurs, either software or hardware. Data at the inputs pins are buffered on the TMS 9901. Data to the output ports is latched and then buffered on-chip by the PSI's MOS to TTL buffers.

The interval timer on the TMS 9901 is accessed by writing a one to select bit zero (control bit) which puts the PSI CRU interface in the clock mode. Once in the clock mode the 14 bits clock contents can be read or written. Writing to the clock register will reinitialize the clock and cause it to start decrementing. When the clock counts to zero, it will cause and interrupt and reload to its initial value. Reading the clock contents permits the user to see the decrementer contents at the point in time just before entering the clock mode. The clock read register is not updated when the PSI is in the clock mode.

A block diagram of the TMS 9901 PSI is given in figure 35, p. 62.

CRU INTERFACE

The CPU communicates with the TMS 9901 PSI via the CRU. The TMS 9901 occupies 32 bits in CRU read space and 32 bits in CRU write space.
The CRU interface consist of 5 address select lines (S0-S4), chip enable (CE), and three CRU lines (CRUIN, CRUOUT, CRUCLK). The select lines (S0-S4) are connected to the five least significant bits of the address bus (A10-A14). Chip enable (CE) is generated by decoding the most significant bits of the address bus on CRU cycles: When CE goes active (low), the five selected lines point to the CRU bit being accessed . When CE is inactive (high), the PSI's CRU interface is disabled. In case of a write operation, the TMS 9901 strokes data off the CRUOUT line with CRUCLK. For read operation, the data is sent to the CPU on the CRUIN line.

INTERRUPT INTERFACE

A block diagram of the interrupt control section is show in fig. 24, p. 61 The interrupt inputs (6 dedicated (INT1-INT6), and 9 programmable) are sampled on the falling edge of Q3 and latched onto the chip for one Q3 time by the SYNC LATCH, each Q3 time. The output of the SYNC LATCH is inverted (interrupts are active low) and ANDed with its respective mask bit (mask=1, interrupt enabled). On the rising edge of Q3, the prioritizer and encoder senses the masked interrupts and produces a four-bit prioritized code and INTREQ are latched off chip with a SYNC LATCH on the falling edge of the next Q3, which ensures proper synchronization to the processor. The interrupt mask bits on the TMS 9901 PSI are individually set or reset under software control. Any unused interrupt line should have its associated mask disabled to avoid false interrupt: to do this, the control bit (CRU bit zero), is first set to a zero for interrupt mode operation. Writing to TMS 9901 CRU bits 1-15 indicates the status of the respective interrupt inputs; thus, the disigner can employ the unused (disabled) interrupt input lines as data inputs (true data in).

INPUT/OUTPUT INTERFACE

A block diagram of the TMS 9901 I/O interface is shown in fig. 25, p. 60. Up to 16 individually controlled I/O ports are available (seven dedicated, P0-P6, and nine programmable) and as discussed above, the unused dedicated interrupt lines also can be used as input lines (true data in). Thus the TMS 9901 can be configured to have more than 16 inputs. RST1 (power-up-reset) will program all I/O ports to input mode. Writing data to a port will automatically switch that port to the the output mode. Once programmed as an output, a port will remain in that state until RST1 or RST2 (command bit) is executed. An output port can be read and indicates the present state of the pin. A pin programmed to the output mode cannot be used as an input pin: applying an input current to an output pin may cause damage to the TMS 9901. The TMS 9901 outputs are latched and buffered on chip, and inputs are buffered onto the chip. The output buffers are MOS-to-TTL buffers and can drive two standard TTL loads.

PROGRAMMABLE PORTS

A total of nine pins on the TMS 9901 are user programmable as either I/O ports or interrupts. These pins will assume all characteristics of the type pin they are programmed to be. Any pin which is not being used for interrupt should have the appropriate interupt mask disabled (mask=0) to avoid erroneous interrupt to the CPU. To program one of the pins as an interrupt, its interrupts mask simply is enabled and the line may be used as if it were one of the dedicated interrupt lines. To program a pin as an I/O port, disable the interrupt mask and use that pin as if it were one of the dedicated I/O ports.

INTERVAL TIMER

Fig. 3e.f63is a block diagram of the TMS 9901 interval timer section. The clock consist of a 14 bit counter that decrements at a rate of f(Q3)/64 (at 3MHz this results in a maximum interval 349 milliseconds with a resolution of 21.3 microseconds). The clock can be used as either an interval timer or an event timer. To access the clock, select bit zero (control bit) must be set to a one. The clock is enabled to cause interrupts by writing a nonzero value to it and is then disabled from interrupting by writing zero to it or by a RST1. The clock starts operating at no more than two Q3 times after it is loaded. When the clock decrementer is running, it will decrement down to zero and will also be reloaded from the clock register and decrementing will start again. (The zero state is counted as any other decrementer state). The decrementer always runs, but is will not issue interrupts until enabled; of course the contents of the not enabled clock read registers are meaningless.

POWER UP

During hardware reset, RST1 must be active (low) for a minimum of two clock cycles to force the TMS 9901 into a known state. RST1 will disable all interrupts, disable the clock, program all I/O ports to the input mode, and force IC1-IC3 to all zero's with INTREQ held high. The system software must enable the appropriate interrupts, program the clock, and configure the I/O ports as required. After initianal power-up the TMS 9901 is accessed only as needed to service the clock, enable (or disable) interrupts, or read (write) data to the I/O ports. The I/O ports can be configured by use of the RST2 software reset command bit.

HARDWARE DESCRIPTION

Connections to the TMS 9901 as used in the 99/4 are given in figure A9, p. 57.
The TMS 9901 is reset during power up by using the buffered reset signal of the TMS 9900.
The TMS 9901 enabled by the RAMBLK signal (see memory selection part, figure
When enabled the 9901 communicates with the TMS 9900 through the CRUIN, CUROUT and CRUCLK lines. The CRU bits are selected by decoding A10 through A14.
Connections with the devices which interface to the TMS 9901 are discussed in other sections.

2.7 Pin Descriptions

Table 4 defines the TMS 9901 pin assignments and describes the function of each pin.

TABLE 4
TMS 9901 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{INTREQ}$	11	OUT	INTERRUPT Request. When active (low) $\overline{INTREQ}$ indicates that an enabled interrupt has been received. $\overline{INTREQ}$ will stay active until all enabled interrupt inputs are removed.
IC0 (MSB)	15	OUT	Interrupt Code lines. IC0-IC3 output the binary code corresponding to the highest priority enabled interrupt. If no enabled interrupts are active IC0—IC3 = (1,1,1,1).
IC1	14	OUT	
IC2	13	OUT	
IC3 (LSB)	12	OUT	
$\overline{CE}$	5	IN	Chip Enable. When active (low) data may be transferred through the CRU interface to the CPU. $\overline{CE}$ has no effect on the interrupt control section.
S0	29	IN	Address select lines. The data bit being accessed by the CRU interface is specified by the 5-bit code appearing on S0-S4.
S1	26	IN	
S2	25	IN	
S3	25	IN	
S4	24	IN	
CRUIN	4	OUT	CRU data in (to CPU). Data specified by S0-S4 is transmitted to the CPU by CRUIN. When $\overline{CE}$ is not active, CRUIN is in a high-impedance state.
CRUOUT	2	IN	CRU data out (from CPU). When $\overline{CE}$ is active, data present on the CRUOUT input will be sampled during CRUCLK and written into the command bit specified by S0-S4.
CRUCLK	3	IN	CRU Clock (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{RST1}$	1	IN	Power Up Reset. When active (low) $\overline{RST1}$ resets all interrupt masks to "0", resets IC0 – IC3 = (0 0 0 0), $\overline{INTREQ}$ = 1, disables the clock, and programs all I/O ports to inputs. $\overline{RST1}$ has a Schmitt trigger input to allow implementation with an RC circuit as shown in Figure 7.
V_{CC}	40		Supply Voltage: +5 V nominal.
V_{SS}	16		Ground Reference.
$\overline{\phi}$	10	IN	System clock (Ø3 in TMS 9900 system, $\overline{CKOUT}$ in TMS 9980 system).
$\overline{INT1}$	17	IN	Group 1, interrupt inputs. When active (Low) the signal is ANDed with its corresponding mask bit and if enabled sent to the interrupt control section. $\overline{INT1}$ has highest priority.
$\overline{INT2}$	18	IN	
$\overline{INT3}$	9	IN	
$\overline{INT4}$	8	IN	
$\overline{INT5}$	7	IN	
$\overline{INT6}$	6	IN	
$\overline{INT7}$ P15	34	I/O	Group 2, programmable interrupt (active low) or I/O pins (true logic). Each pin is individually programmable as an interrupt, an input port, or an output port.
$\overline{INT8}$/ P14	33	I/O	
$\overline{INT9}$/ P13	32	I/O	
$\overline{INT10}$/P12	31	I/O	
$\overline{INT11}$/P11	30	I/O	
$\overline{INT12}$/P10	29	I/O	
$\overline{INT13}$ P9	28	I/O	
$\overline{INT14}$/P8	27	I/O	
$\overline{INT15}$/P7	23	I/O	
P0	38	I/O	Group 3, I/O ports (true logic). Each pin is individually programmable as an input port or an output port.
P1	37	I/O	
P2	36	I/O	
P3	22	I/O	
P4	21	I/O	
P5	20	I/O	
P6	19	I/O	

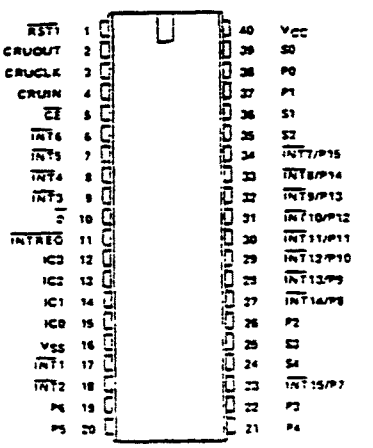


Fig. 22

TABLE 4

9901 INTERRUPT MAPPING

ADDRESS	CRU BIT	9901	PIN	FUNCTION
0000	0	Control		Control
0002	1	INT1	17	External
004C	2	INT2	18	Video Display Processor Vertical Sync
0006	3	INT3	9	Clock Interrupt, Keyboard "ENTER" line, Joystick "FIRE"
0008	4	INT4	8	Keyboard "L" line, Joystick "LEFT"
000A	5	INT5	7	Keyboard "P" line, Joystick "RIGHT"
000C	6	INT6	6	Keyboard "O" line, Joystick "DOWN"
000E	7	INT7 (P15)	34	Keyboard "SHIFT" line, Joystick "UP"
0010	8	INT8 (P14)	33	Keyboard space line
0012	9	INT9 (P13)	32	Keyboard "Q" line
0014	10	INT10 (P12)	31	Keyboard "1" line
0016	11	INT11 (P11)	30	Not Used
0018	12	INT12 (P12)	29	Reserved
001A-1E	13-15	INT13-INT15	28,27 & 23	Not Used

TABLE 5

9901 I/O MAPPING

ADDRESS	CRU BIT	9901	PIN	FUNCTION
0020	16	P0	38	Reserved
0022	17	P1	37	Reserved
0024	18	P2	26	BIT2 (LSB) of Keyboard Select
0026	19	P3	22	BIT1 of Keyboard Select
0028	20	P4	21	BIT0 (MSB) of Keyboard Select
002A	21	P5	20	Not used
002C	22	P6	19	Cassette Control 1
002E	23	P 7 (INT15)	23	Cassette Control 2
0030	24	P 8 (INT14)	27	Audio Gate
0032	25	P10 (INT12)	28	Mag Tape Out
0036	27	P11 (INT11)	30	Mag Tape Input
0038-003E	28-31	P12-P15	31-34	Not used

TMS 9902 I/O Interface section.

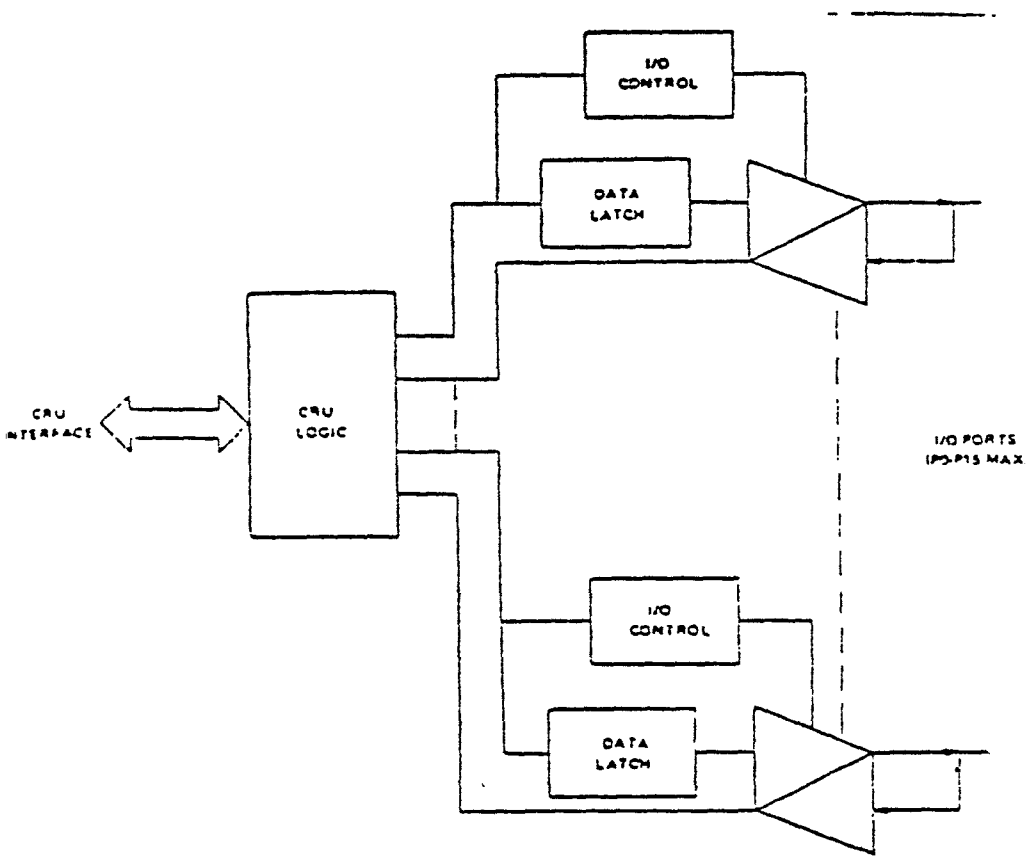


Fig. 23

TABLE 6 PERIPHERAL ADDRESSES ON CRU BUS

CRU Addresses	A3	A4	A5	A6	A7	Use (Peripheral)	Device Number
>0000 - >0FFE	0	x	x	x	x	Internal use	
>1000 - >10FE	1	0	0	0	0	Reserved	0
>1100 - >11FE	1	0	0	0	1	Disk controller	1
>1200 - >12FE	1	0	0	1	0	Reserved	2
>1300 - >13FE	1	0	0	1	1	RS232, ports 1 and 2	3
>1400 - >14FE	1	0	1	0	0	Reserved	4
>1500 - >15FE	1	0	1	0	1	RS232, ports 3 and 4	5
>1600 - >16FE	1	0	1	1	0	Reserved	6
>1700 - >17FE	1	0	1	1	1	Reserved	7
>1800 - >18FE	1	1	0	0	0	Thermal Printer	8
>1900 - >19FE	1	1	0	0	1	Future expansion	9
>1A00 - >1AFE	1	1	0	1	0	Future expansion	10
>1B00 - >1BFE	1	1	0	1	1	Future expansion	11
>1C00 - >1CFE	1	1	1	0	0	Future expansion	12
>1D00 - >1DFE	1	1	1	0	1	Future expansion	13
>1E00 - >1EFE	1	1	1	1	0	Future expansion	14
>1F00 - >1FFE	1	1	1	1	1	P-Code peripheral	15

TMS 9901 interrupt handling logic.

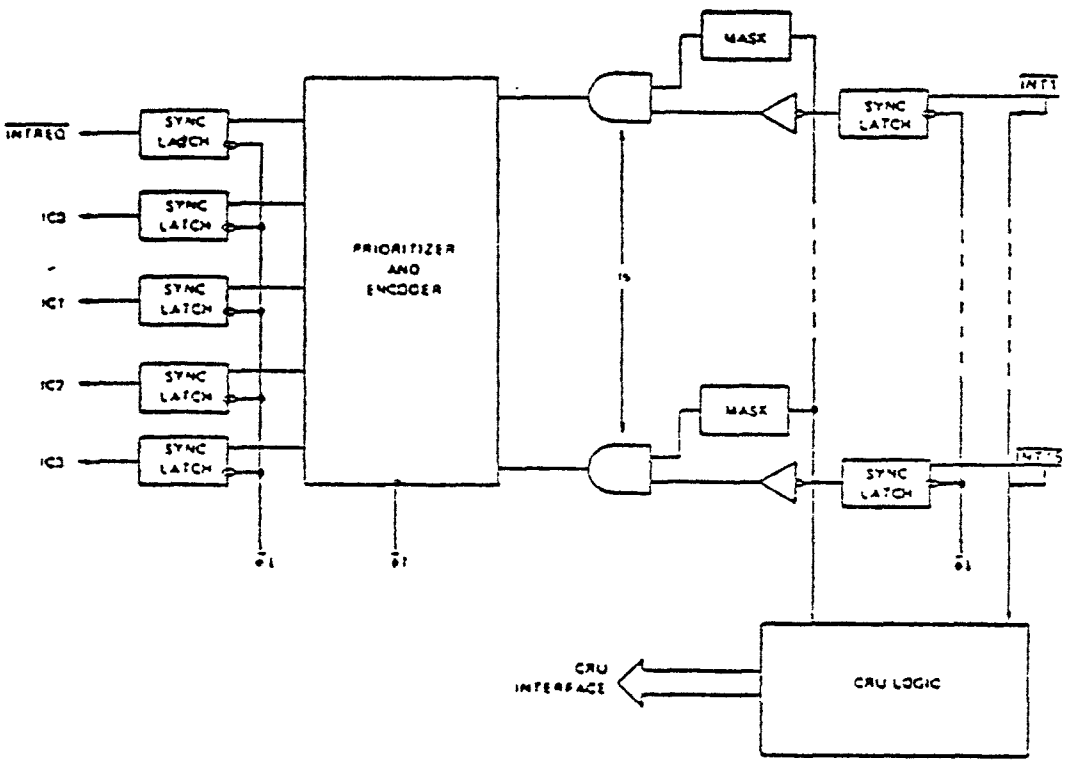


Fig. 24

TMS 9901
Programmable system interface.

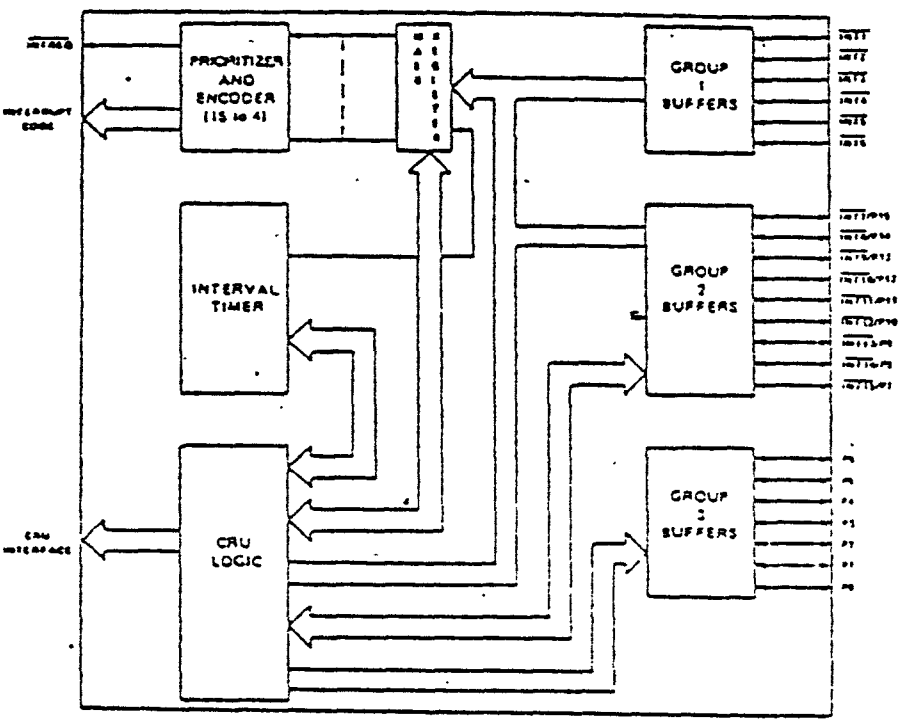


Fig. 25

TMS 9901 Internal Timer section

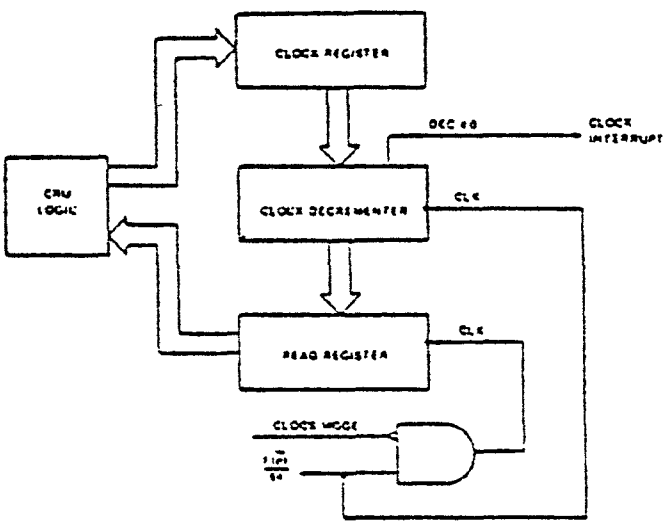


Fig. 26

VIDEO DISPLAY PROCESSOR

GENERAL DESCRIPTION

The TMS 9918 video display processor is capable of generating a complete NTSC color television video signal. The information to be displayed is stored in dynamic ram the TMS 9918 generating all the necessary interfacing signals.

The VDP will generate a solid color border and background on which a 32 X 24 matrix of 8 X 8 picture element patterns is superimposed. In addition a high degree of mobility and resolution is provided in the form of the sprites, or dynamic patterns, which are further superimposed on the pattern display.

An option can be selected whereby the VDP can function as a 40 X 24 character alphanumeric terminal by setting the text command bit to one.

ARCHITECTURE

Fig. 24, p. 71 shows the block diagram of the video display processor. Interface to the CPU is via an 8 bit bidirectional port controlled by two select and one address line. Interface to the refresh RAM is via an 8 bit data bus, an 8 bit address/data bus, and 3 control lines. The VDP provides clock and synchronization signals to the system via the GROM CLK, CPU, CLK, and CPU INT signal lines.

Interface to the target television is provided by a composite video output signal.

OSCILLATOR AND CLOCK GENERATION

The video display system designed to operate with a 10.738635 mHz +/- 50 PPM crystal input to generate the required internal clock signals. A fundamental frequency parallel mode crystal is used as the frequency reference for the internal clock oscillator, which is the master time base for all system operation. This master clock is divided by two to generate the dot clock rate of 5.3 mHz. The master clock is divided by 3 to provide the CPU clock. The GROM clock is developed from the master clock divided by 24. Additional, the master clock and its compliment are divided by 3 in two stages to provided the 6 basic color phase frequencies which generates the color on the target color tv.

COLOR PHASE GENERATION

The 10.7+ mHz master clock and its complement are used to generate a 6 phase 3.57545 MHz(+/-10Hz) clock to provide the video color signals and the color burst reference for use in developing the composite video output signal. Table 7 shows the six colors, the standard phase shifts, and the color approximations provided by the VDP. While the VDP signals are not exact equivalencies, the differences can easily be adjusted by the color and tint control of the target color television. To insure compatibility with monochrome television receivers, an intensity level on the gray scale is assigned to each color signal.

TABLE 7

Color vector relationships to the 3.079545 MHz color reference.

COLOR	STANDARD PHASE	VDP FIRST APPROXIMATION	GOAL*
Yellow	12 +/- 10	00	10 +/- 5
Red	76 +/- 10	60	70 +/- 5
Magenta	120 +/- 10	120	120 +/- 5
Blue	192 +/- 10	180	190 +/- 5
Cyan	256 +/- 10	240	250 +/- 5
Green	300 +/- 10	300	300 +/- 5

* Electrical design will attempt to provide these color signals.

VIDEO SYNC AND CONTROL GENERATION

The vertical and horizontal control signals are generated by decoding the output of the horizontal counter increments the vertical counter. Table 8 gives the relative count values of the screen display parameters. Within the active display area, the three least significant bits of the horizontal counter addresses the individual picture elements of each pattern displayed. Also, during the vertical active vertical counter addresses each individual line in the 8 X 8 patterns.

The VDP operates at 264 lines per frame and approximately 60 frames per second in a non-interlaced mode of operation.

TABLE 8
SCREEN DISPLAY PARAMETERS

HORIZONTAL	DOT CLOCK CYCLES
Horizontal active display	256
Right border	15
Right blanking	8
Horizontal sync	26
Left blanking	2
Color burst	14
Left blanking	8
Left border	13
TOTAL	342

VERTICAL	LINE
Vertical active display	192
Bottom border	26
Bottom Blanking	3
Vertical sync	3
Top blanking	13
Top border	27
TOTAL	264

TELEVISION SCREEN DISPLAY

The VDP assembles three major elements into a composite for display on the target television: background, pattern matrix, and sprites. In normal operation the background is composed of the border of the active display area. The color of this region is specified by loading the specific code for the color desired into the screen background color register. All color of this region is specified by loading the specific code for the color desired into the screen background color register. All color information is described by four bit codes composed of three color select bits and an intensity bit giving a total range of 15 colors with one code reserved for the transparent state.

PATTERN GENERATION

The second element of the screen display is the 32 X 24 matrix of patterns formed and is the active display area. Each pattern is composed of an 8 X 8 matrix of picture elements.

In a raster scanned television system each line of video information must be built and displayed. To accomplish this, a list of 768 8-bit names - one for each pattern to be displayed - is assembled in the screen refresh memory. The 8-bit name contains both color and display information.

EXTERNAL VIDEO OPERATION

In this mode any VDP - generated signal, other than the background, will be display as generated. When no signal is generated, the external signal is gated through. In both modes, however, the external sync, blanking, and color burst signals are controlling the VDP and the target tv system. No internal synchronization is made to the color burst. Therefore, if a color VDP generated signal is desired, an externally generated 10.7 MHz (i.e., 3x the color frequency) must be provided to the XTL1 input and its non-overlapping complement to the XTL2 input.

VDP RESET

The VDP is reset by applying a low signal to the RSET pin. This signal must last for at least 2 usec. Reset does the following: Synchronizes all clocks to its negative going edge (this includes Q1-Q4 control clocks, CPUCLK, GROMCLK and color burst), sets horizontal and vertical counters to known state, clears the internal command registrs, gets the text color and border color to black, and clears all status flags.

POWER UP

VBB must be applied to the 4116's either before or at the same time as the other supplies and removed last. Failure to observe this precaution will cause dissipation in excess of the absolute maximum ratngs due to internal forward bias conditions. This also applies to system use, where failure of the VBB supply must immediately shut down the other supplies. After power up, eight memory cycles must be performed to achieve proper device operation.

HARDWARE DESCRIPTION

OSCILLATOR CIRCUITRY

An overview of the connections to the TMS 9918 VDP are given in fig. 36, p 71

Timing signals for the TMS 9918 are derived from an on-chip oscillator which uses on external 10.7 mHz crystal. This crystal (Y100) in series with L100 is connected between pin 39 and 40. L100 is adjustable to set the frequency. C100 and C101 are the capacitors in the frequency determing network. R103 is added in parallel to Y100 and L100 to lower the impedance of the network, thus assuring a proper voltage swing at pin 39. Also a 5 volt voltage is fed to pin 39, R102 and L107 for decoupling. This voltage is used for proper start-up of the oscillator.

POWER CONNECTIONS

The TMS 9918 uses only one power supply voltage pin 12 (VSS) is connected to the system ground, PIN 33 (VCC) to the +5 volt power supply.
C102, C103, C104 and L101 are used to suppress noise on the 5 volt line.

GROM CLOCK

The 10.7 mHz oscillator frequency is internally divided by 24. This gives a frequency of 445.8 kHz. This frequency is buffered and fed to pin 37 and used as the GROM clock.

CPU CLOCK

The 3.58 mHz CPU clock on PIN 38 is used by TMS 9919 sound processor (on units which use the SN76489).

RESET

The TMS 9918 is reset during power up or when a solid state software command module by using the reset signal of U601 pin 4.
This signal is monitored by the 9918 on pin 34.

CHIP SELECTION LOGIC

The VDP is selected when CSW on pin 14 or CSR on pin 15 are low.

When CSW is low the micro processor can write to the VDP, when CSR is low, data can be read from the VDP. The MODE signal on pin 13 is used in combination with CSW and CSM to select four basic modes of operation.

The selection logic which enables CSW or CSR is given in figure 37, p 69.

Selection pins Y2 (pin 13) and Y13 (pin 12) of U505 (74LS138) are used to distinguish between a write or read operation.
The write selection from pin 12 is combined with the WE signal in OR-gate U507. Thus only a VDP write can occur when WE is low.

DATABUS INTERFACING

Pins 17 through 24 (data lines CD0 through CD7) are directly connected to D0 through D7 of the TMS 9900.

Thus circumventing the 16 to 8 bit interfacing circuit.

DYNAMIC RAM INTERFACNG

Dynamic RAM memory is given in fig.53, p.133. The TMS 9918 uses pins 1 through 11 and 25 through 32 for interfacing the dynamic RAM.
Pins 3 through 10 are the address/data lines for the TMS 4116 (line 10 only for data). RAS on pin 1 and CAS or pin 2 are the row and address strobe lines for loading the address in the 4116's (and refresh operation), and are connected to the corresponding pins 4 and 14 of the RAM's. R/W on pin 11 of the TMS 9918 distinguishes between a read or write to the RAM. This signal is delayed by the four inverting buffers U101 for timing purposes.in units manufactured not using the TMS 9918A.
During a read all 8 seperate output bits of the RAM's form an eight bit data bus which is connected to RD0 through RD7 (pin 25 through 32) of the TMS 9918.

VIDEO OUTPUT

The composite NTSC video signal is available on PIN 36 of the TMS 9900. This signal if fed to the video amplifier in fig.53, p.133. This amplifier has two purposes:

1. To amplify the video signal.

2. To provide the desired output impedance of 75 ohms.

99/4

The first stage of the amplifier consisting of Q200 is a common base amplifier which has enough bandwidth to amplify the video signal. R201 is used to adjust the gain of the video amplifier. The second stage with Q201 has no voltage amplification since this stage is used as an emitter follower, but is used as an impedance transformer to provide the 75 ohm output inpedance. R208 and C205 is a filter which decouples the video noise from the +12 volt power line. L200 and C207 have the same purpose and the voltage from this filter can be used to supply power for an RF modulator.

99/4A

In the 99/4A, the first stage of the video amplifier (Q200) is a PNP transistor connected in the common collector configuration. Input to Q200 is through a filter which is designed to roll off signal frequencies above the GMHz video bandwidth. Diodes R200 & CR201 clamp the DC level after C201. Q201 is an emitty-follower and is use as an impedence transformer to achieve the required 75 ohm video output.

VDP SELECTION LOGIC.

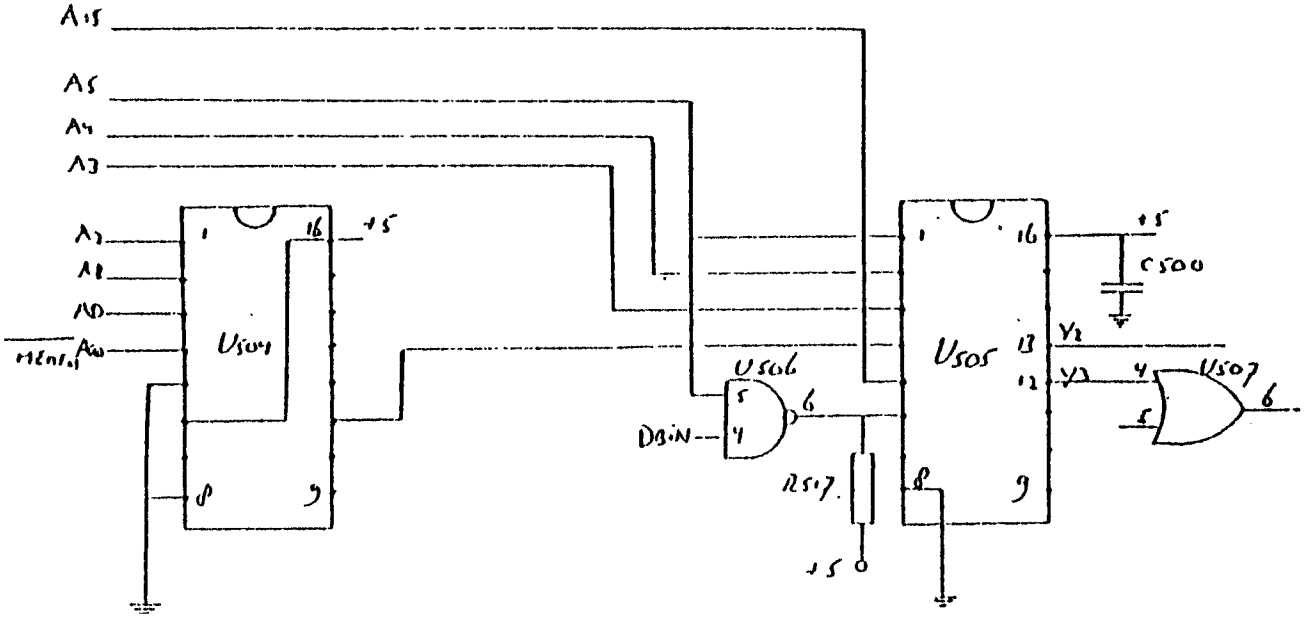


Fig. 27

VIDEO DISPLAY PROCESSOR

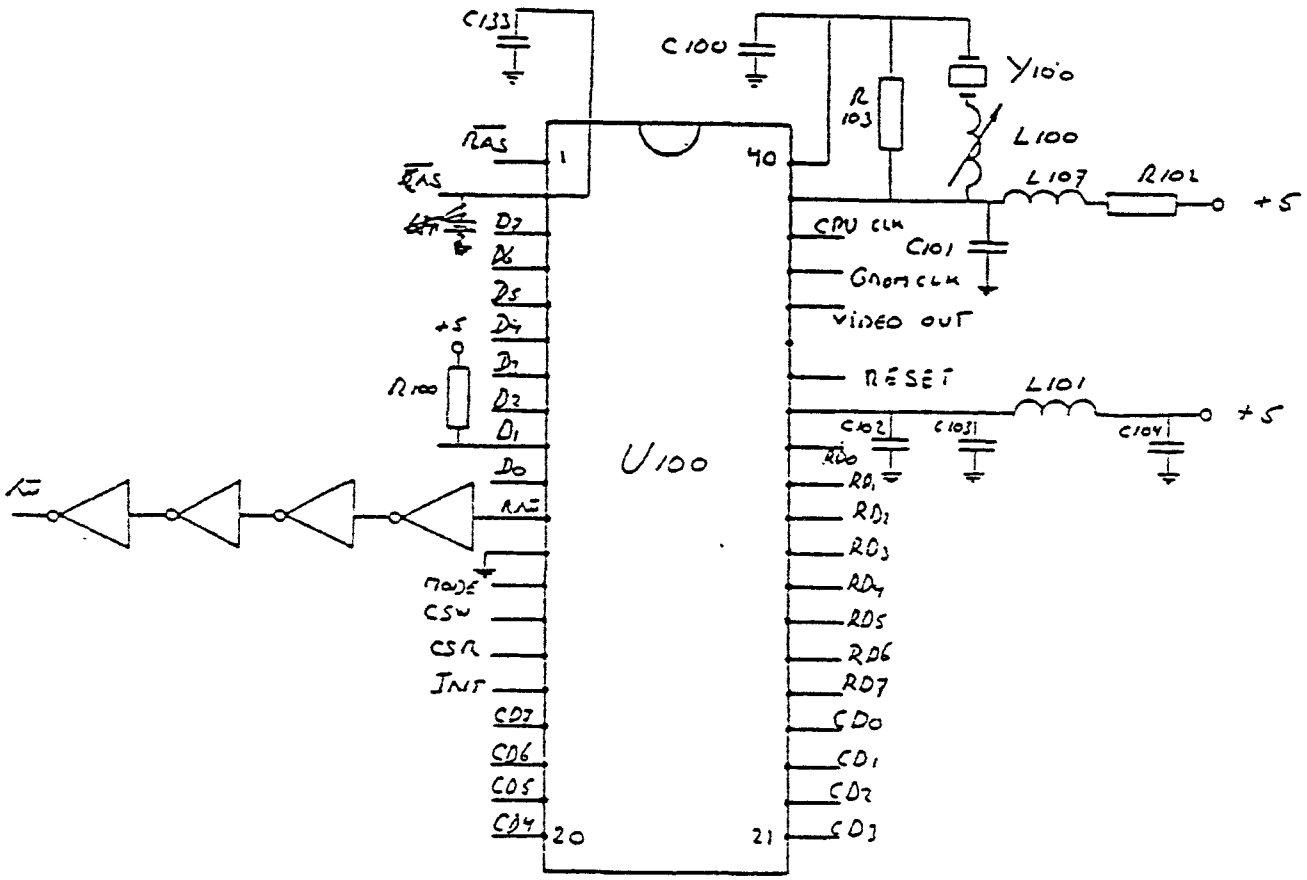


Fig. 28

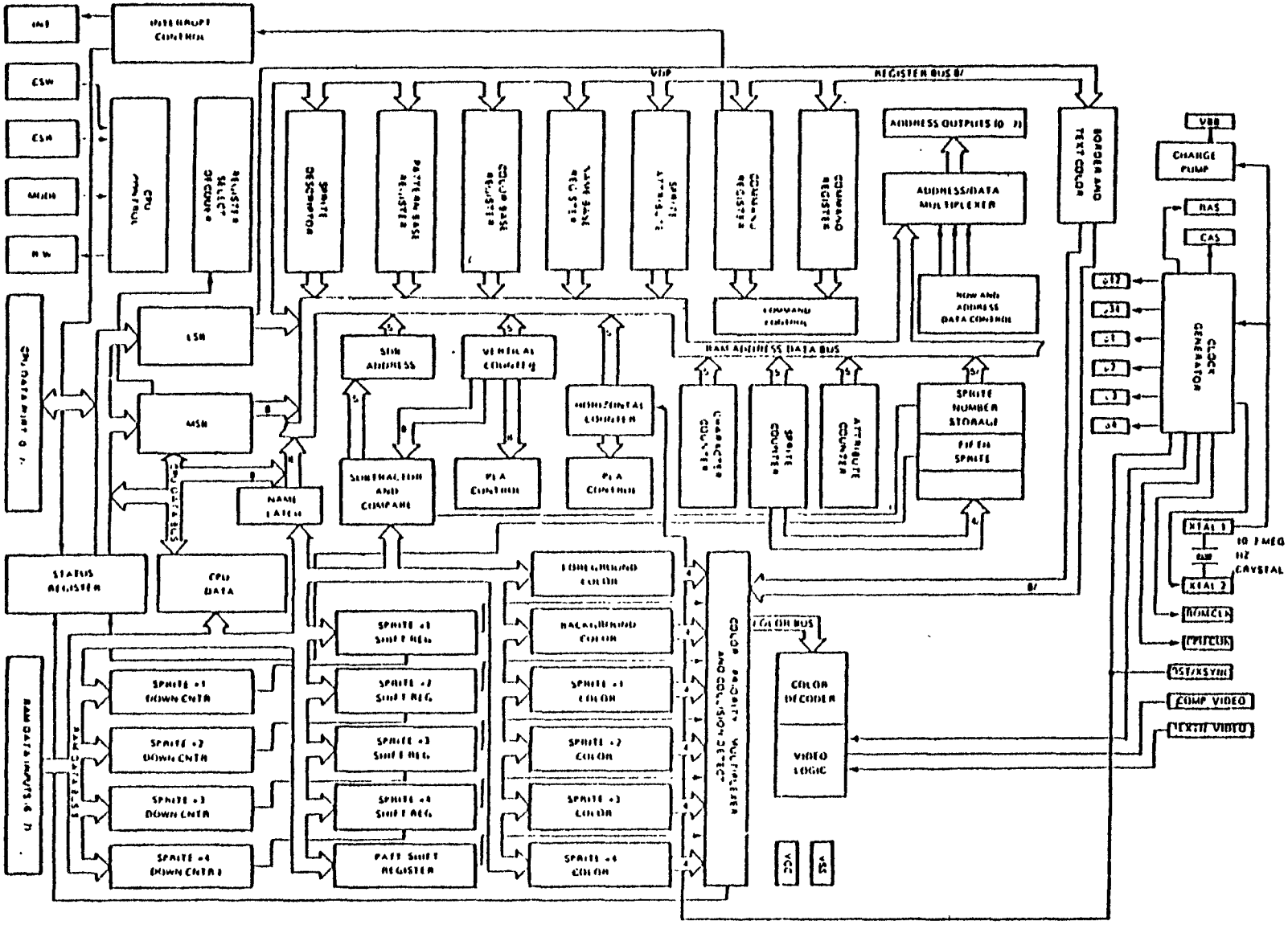


FIGURE 2-1 – TMS 9918 VDP BLOCK DIAGRAM

Fig. 29

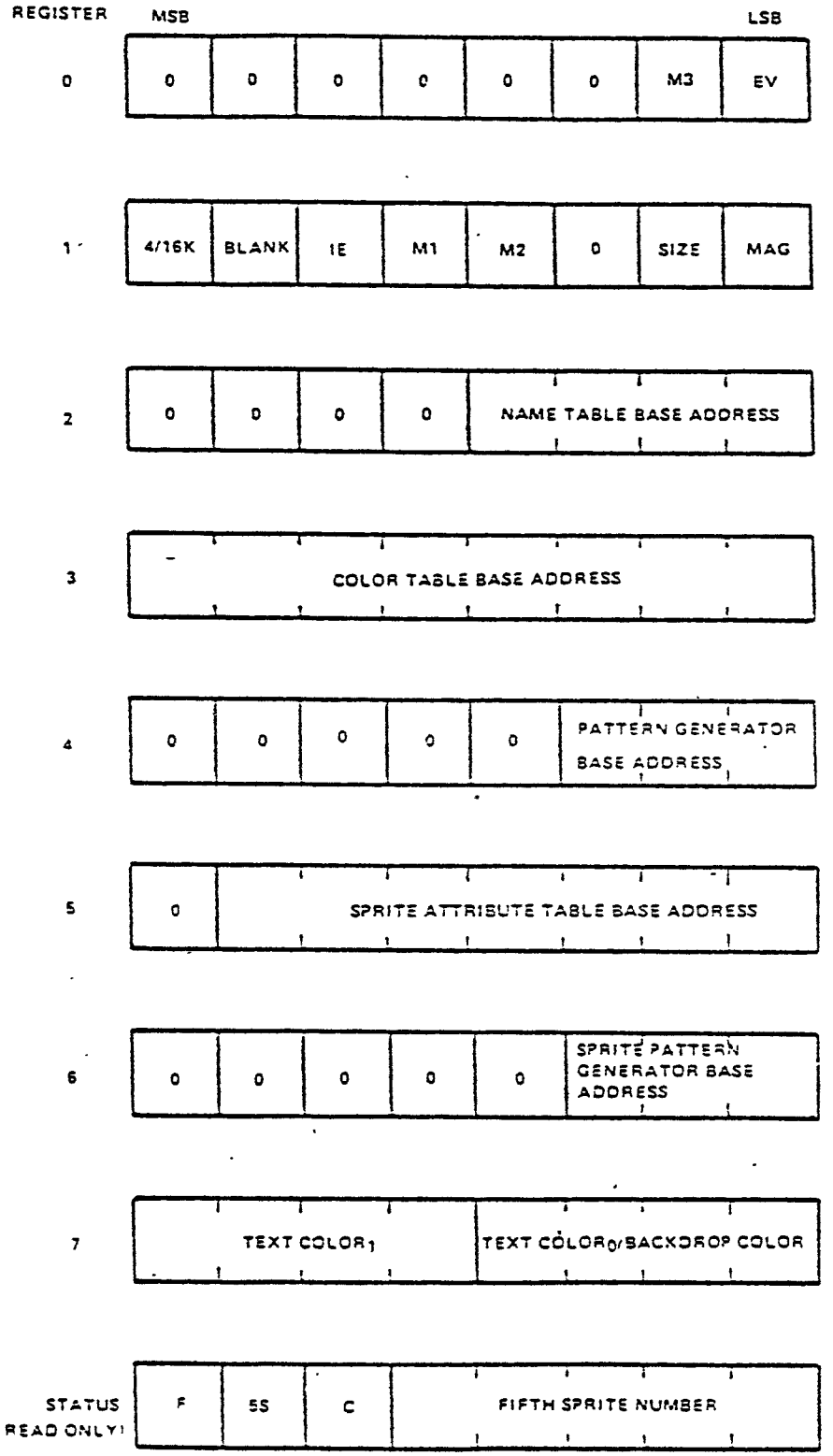


TABLE 9

VDP REGISTERS

SOUND GENERATION CONTROLLER

GENERAL DESCRIPTION

The TMS 9919 Sound Generation Controller (SGC) is an I^2L component designed to provide low cost tone/noise generation capability in microprocessor systems. The SGC is a data bus based I/O peripheral.

KEY FEATURES

* 3 programmable tone generators
* Programmable white noise generator
* Programmable attenuation
* 8 ohm speaker drive capability
* External audio input
* 16 PIN package
* I^2L technology

DEVICE ARCHITECTURE

The device consists of three programmable tone generators, a programmable noise generator, a clock scaler, and an audio summer output buffer. The SGC has a parallel 8 bit interface through which the microprocessor transfers the data which controls the audio output.

TONE GENERATORS

Each tone generator consist of a frequency synthesis section and an attenuation section. The frequency synthesis section requires 10 bits of information (F0-F9) to define half the period of the desired frequency (n). This information is loaded into a 10 stage tone counter, which is decremented at a N/16 rate where N is the input clock frequency. When the tone counter decrements to zero, a borrow signal is produced. this borrow signal toggles the frequency flip-flop and also reloads the tone counter. Thus, the period of the desired frequency is twice the value of the period register.
The frequency can be calculated by the following:

$$f = \frac{N}{32n}$$

The output of the frequency flip-flop will feed into a four state attenuator. The attenuator values, along with their bit position in the data word, are shown in table Multiple attenuation control bits may be true simultaniously. Thus, the maximum attenuation is 28 db.

TABLE 10 : ATTENUATION CONTROL

BIT POSITION				
A0	A1	A2	A3	WEIGHT
0	0	0	1	2 dB
0	0	1	0	4 dB
0	1	0	0	8 dB
1	0	0	0	16 dB
1	1	1	1	OFF

NOISE GENERATOR

The noise generator consists of a noise source and an attenuator.

The noise source is a 15 stage shift register with an exclusive OR feedback network.
The feedback network will have provisions to protect the shift register from geing locked in the zero state.

The feedback network will have two feedback tap configurations as determined by the FB control bit.

TABLE 11 : NOISE FEEDBACK CONTROL

FB	CONFIGURATION
0	"Periodic" noise
1	"White" noise

Whenever the FB bit is changed, the shift register is cleared. The shift register wil shift at one of four rates as determined by the two NF bits. The fixed shift rates are derived from the input clock.

TABLE 12 NOISE GENERATOR FREQUENCY CONTROL

BITS NF0	BITS NF1	SHIFT RATE
0	0	N/512
0	1	N/1024
1	0	N/2048
1	1	Tone Gen. #3 output

The output of the noise source is feed to an attenuator similar to the tone generator attenuator.

AUDIO SUMMER/OUTPUT BUFFER

The summer is a conventional I^2L operational amplifier summing circuit. It will sum the three tone generator outputs, noise generator output, and an external audio source. The output buffer will generate up to 100 milliamperes into a 8 ohm load, if all sources are operating at maximum levels. It is assumed that the speaker will be AC coupled to the chip.

CPU/SGC INTERFACE

The microprocessor interfaces with the SGC by means of the 8 data lines and 3 control lines (WE, CE and READY). Each tone generator requires 10 bits of information to select the frequency and 4 bits of information to select the attenuation. A frequency update requires a double byte transfer, while an attenuator update requires a single byte transfer.

CONTROL REGISTERS

The SGC has eight internal registers which are used to control the three tone generators and the noise source. During all data transfers to the SGC,

the first byte contains a three bit field which determines the destination control register. The register address codes are shown in Table 3.

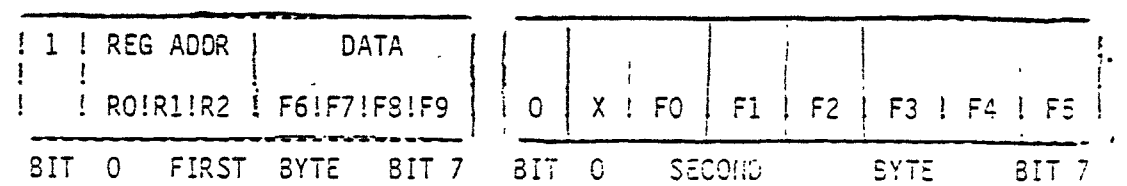
TABLE 3 : REGISTER ADDRESS FIELD

R0	R1	R2	DESTINATION CONTROL RESISTOR
0	0	0	Tone 1 frequency
0	0	1	Tone 1 attenuation
0	1	0	Tone 2 frequency
0	1	1	Tone 2 attenuation
1	0	0	Tone 3 frequency
1	0	1	Tone 3 attentuation
1	1	0	Noise control
1	1	1	Noise attenuation

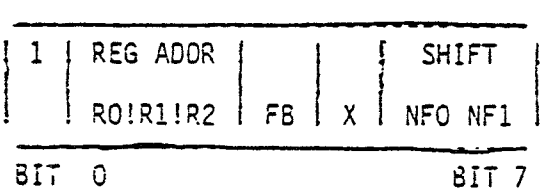
DATA FORMATS

The formats required to transfer data are shown below.

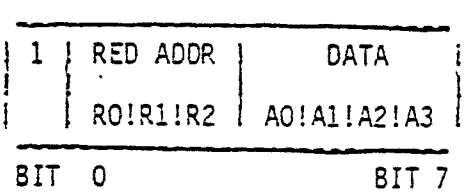
UPDATE FREQUENCY (2 BYTE TRANSFER)



UPDATED NOISE SOURCE (SINGLE BYTE TRANSFER)



UPDATE ATTENUATOR (SINGLE BYTE TRANSFER)



HARDWARE DESCRIPTION

POWER CONNECTIONS

The TMS 9919 uses a single 5 volt power supply on PIN 16, L500 and C501 used to decouple the power line.

CLOCK

The TMS 9919 use a 3.58 mHz clock signal on PIN 14, derived from the TMS 9918 video display processor. The SN94624 uses the 447.5 Khz Grom Clock.

DATA BUS

The TMS 9919 uses an eight bit parallel data bus connected directly to the 99/4 data bus.

SOUND PROCESSOR SELECTION LOGIC

The logic which selects the sound processor is given in figure 30, p 77.

READY

The ready line of the TMS 9919 is directly connected to the system ready line. This wired-OR convention is possible because NAND gate U506 is open collector.

$\overline{WE}$

The $\overline{WE}$ signal distinguishes between a write to or a read from the TMS 9919.

EXTERNAL SOUND

External sound is fed to PIN 9 of the TMS 9919. The 99/4 system uses two sound signals on PIN 9.

1. External sound from the cassette interface connector
2. Sound from the speech unit

R510 is used to reduce the speech signal to an appropriate level.

SOUND OUTPUT

Sound is available on PIN 7. C502 and R511 are used to reduce the bandwidth. C503, C504 and L501 are used for the same purpose.

TMS 9919 SOUND PROCESSOR SELECTION LOGIC:

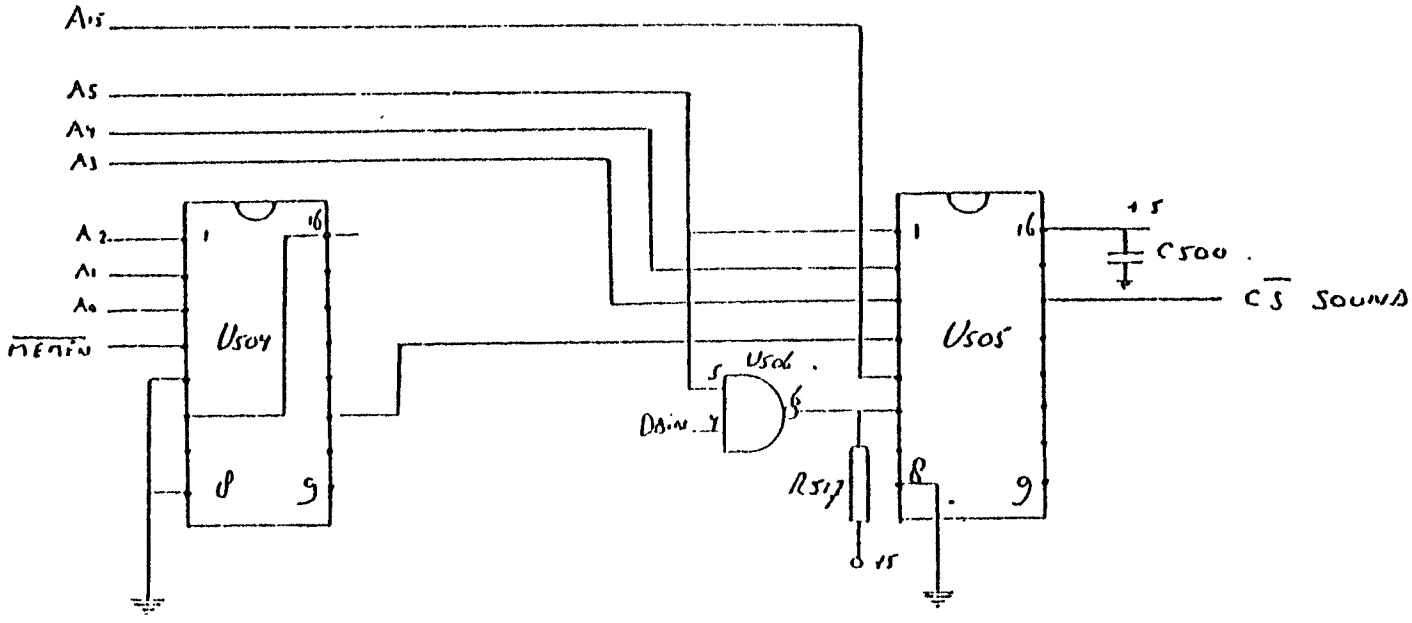


Fig. 30

KEYBOARD & REMOTE HANDHELD CONTROL UNIT INTERFACING

GENERAL DESCRIPTION

Keyboard and remote control are scanned under software control. The keyboard is scanned by 6 select lines. The 9 detect lines are monitored by the TMS 9901 programmable system interface (see figure 47, p.127).

Two other select lines are used for selecting the remote handheld control unit, the five detect lines of these units are shared with those of the keyboard.

HARDWARE DESCRIPTION

The keyboard and remote handheld unit interfaces to the microprocessor via the TMS 9901 programmable system interface. Pin P2, P3 and P4 of the 9901 are programmed as outputs and used as input for U302 (74LS156), a dual 2 to 4 decoder. This IC is wired as a three to eight line decoder. Outputs are used to scan the keyboard and joystick port.

Two outputs of U302 (pin 4 and 5) are used to select the remote handheld control units. Pull up resistors R322 and R329 are used to supply enough current when the outputs are in the logic high state (+5 volt). CR 301 in combination with R321 and CR302 with R320 are used to get a good defined logic zero state, since R320 and R321 which are connected to the -5 volt supply generates a -.6 volt drop over CR301 and CR302.

KEYBOARD SCANNING

The keyboard is divided in two parts. Each part consisting of 4 rows with 5 keys. The outputs of the right four rows (INT 3, 4, 5 and 6) and the left four rows (INT 7, 8, 9 and 10) are connected to the preprogrammed inputs of the TMS 9901 with the same names. These inputs are scanned under software control to determine which key is pressed down. The keyboard uses pull-up resistors for putting all lines in the logic one state when no key is hit. The capacitors are used for reducing RF intrference.

REMOTE HANDHELD CONTROL UNIT

The handheld units uses the same inputs to the TMS 9901 as the righthand keyboard side.

99/4 KEYBOARD DESIGN

The 99/4A keyboard circuit is significantly changed from the design used in the 99/4, although the principle of operation is the same. Seven outputs are used on U302, and one additional interupt line (PS), in order to scan the additional keys used on the 99/4 keyboard.

CASSETTE INTERFACING CIRCUITRY

GENERAL DESCRIPTION

The cassette interfacing circuit enables the 99/4 to store and read data from a normal cassette recorder. The interfacing circuitry consists of 3 distinct parts: the control circuity, the write circuitry and read circuitry.

CASSETTE CONTROL CIRCUITRY

This part consists of two solid state switches which are used for remote controlling of up to two cassette recorders.

WRITE CIRCUITRY

The write circuitry supplies the signal with digital data to the cassette recorder. It uses a TMS 9901 output gate and a second order filter to supply a signal of the desired shape and amplitude.
If two cassette recorders are used, then both will use the same write signal, but only one recorder is selected at a time by the control circuitry.

DATA FORMAT

The 99/4 uses a biphase coding technique to generate the serial data stream.
A standard time interval (bit cel) is used in the encoding software, in the following way:

A. A binary one is represented by 2 bit cells both bit cells of opposite polarity.
B. A binary zero if represented by 2 bit cells, both bit cells of the same polarity.
C. After a binary bit is written, the next bit will start with an opposite polarity refered to the last bit cell.

AUDIO GATE

A special feature is incorporated which consists of a solid state switching circuit. This circuit can switch the audio signal of the cassette recorder to the sound processor.

CONTROL CIRCUITRY

Since the two control circuits are identical only a description of one cassette control circuitry is given (see figure 5-7, p.134).
Pin 19 (P6) of the TMS 9901 programmable system interface is used to enable or disable Q402.
When enabled, the LED in opto couplor U401 turns on. R415 is used to reduce the current through the LED. Outputs 4 and 5 of the opto coupler are used to put transistor Q401 in the conductive state, thus enabling the motor drive of the cassette recorder.

WRITE CIRCUITRY

The write signal is generated on PIN 28 of 407 the TMS 9901. The differentiating filter consisting of R402, C408, C407, R400, R401 and C400 shapes the signal.

READ CIRCUITRY

First part of the read circuitry consists of an operational amplifier which performs amplification and pulse shaping of the read signal.
R408 and R410 determine the gain of the amplifier. C402, C409 and C411 are for pulse shaping purposes. R406 is the resistive load for the cassette recorder.

GROUNDING

Since the definition for ground and signal on the output jack of the cassette recorder depends on the type used, R409 is applied to allow operation with both types of recorders.

HYSTERESIS CIRCUIT

The hysteresis circuit consists of a second amplifier with positive feedback, the feedback network consisting of R412 and R411.
C410 is used to make the circuit less succeptible to undesired signals.
CR402 is used to limit the negative output swing, thus avoiding damage to the TMS 9901. R413 is used to limit the current through diode CR402.

I/O BUS

GENERAL DESCRIPTION

The 99/4 I/O bus provides maximum flexibility for operation with external devices. It provides peripherals with memory and CRU I/O buses.
The memory bus (with 8 bit data bus) is used for instruction fetch from control ROM in the peripherals and for data transfer to/from memory mapped peripherals.
The CRU bus is used for peripherals enable/disable and for device control and data transfer to/from CRU mapped pheripherals.

The TMS 9900 accesses each peripheral to obtain instructions from the device service routine (DSR) read only memory. Since each peripheral contains its own DSR, the 99/4 does not have to be designed to anticipate future peripheral requirements.
The dual I/O bus capability, along with interrupt handling and external DSR's provide flexibility of low cost.

MEMORY ALLOCATION

The third memory block (addresses 4000 - 5FFF) of the 99/4 is predecoded and made available at the I/O port for the peripherals.
Addresses A000 - FFFF are available for future expansion. For the speech module (addresses 9000 - 97FF), a predecoded line is available at the I/O bus.

CRU ALLOCATION

Of the available 4K of CRU bits, the first 1K (addresses 0000 - 07FE) are used internally in the Home Computer. The second 1K (addresses 0800 - 0FFE) are reserved for future use. The last 2K (addresses 1000 - 1FFE) are reserved for the peripherals to be plugged in the I/O port. A block of 128 CRU bits is assigned to each peripheral as listed below.

CRU ADDRESS	PERIPHERAL
1000	Disk
1100	Reserved
1200	Home Security
1300	RS-232
1400	Modem
1500	Reserved
1600	Digital Cassette
1700	Student Typing
1800	Thermal Printer
1900	Not Assigned Yet
1A00	Not Assigned Yet
1B00	Not Assigned Yet
1C00	Not Assigned Yet
1D00	Not Assigned Yet
1E00	Not Assigned Yet
1F00	Not Assigned Yet

INTERRUPT HANDLING

The interrupt available on the I/O port is one of the maskable interrupt of the TMS 9901 programmable systems interface.

BUFFERING

All I/O signals must be able to drive two LS-type LOADS (with exception of the data bus).
In addition, peripherals generating CRUIN, READY/HOLD, LOAD and EXT INT schall buffer these signals before putting them on the I/O bus.

I/O READ

A CPU read cycle for the external device consists of two 8-bit read cycles (Fig 18, page).
The two bytesread are assembled as a 16 bit word before they are presented to the 9900.

MEMEN goes low true at the beginning of clock cycle 1. At the same time DBIN goes high true. WE stays high false during the entire cycle. At the same time that MEMEN goes true, the address bus goes active. In order for the noise and the glitches (associated with crostalk and simultaneous switching) to go away we allow a minimum of 100 ns for the address lines to settle. MBE (see memory selection logic) goes true during the leading edge of Q2 of clock cycle 1. Data read from the peripherals will be valid 750 ns after the start of clock cycle 1. The CPU will look at the full 16 bit data bus during the leading adge of Q1, of clock cycle 2. Under worse-case conditions, data must be valid 100 ns before that time.

I/O WRITE

Fig 19, page 35 shows a 16 bit I/O write cycle. As described earlier it is composed of two 8-bit writes. A write cycle wil always be preceded by a ALU cycle. MEMEN and DBIN go true at the start of the cycle. A settling time of 100 ns (min) is allowed for the address lines t settle down. WE goes true (low) on the leading edge of Q2, during the wait states, and stays true for 660 ns (typ). Both during a read or a write the odd byte is accessed first, followed by an even byte. A15/CRU out changes its state 990 ns (typ) after the cycle is initiated. The second 8-bit write cycle is identical to the first 8-bit write. MBE stays true (low) during the entire (1.8 usec) cycle.

SPEECH INTERFACE

The I/O part has 4 lines dedicated for use by the speech module : +5, -5, speech block enable (SBE) and audio in. SBE is decoded by the 99/4 for addresses 9000 and 9400 (write and read). For the write cycle, SBE goes active after the address and data lines are valid.

GROM INTERFACE ON I/O PORT

All signals are provided to use GROM's in external devices. Decode for grom select must be performed in the external device.

CRU TIMING

CRU interface timing is shown in fig 5, p 130. The CRUOUT cycle is composed of 2 clock cycles. The CRU bit address when placed on the address bus A0 through A14 is allowed to settle for 100 ns (min). CRUCLK is a 80 ms low true signal which occurs on the trailing adge of Q1, of clock cycle 2. CRUOUT data is valid at the start of clock cycle 1, and is latched by the CRUCLK in the repective peripheral.

CRUIN also consists of 2 clock cycles of 660 ns (typ). Again we allow 100 ns for the address bus to settle down. The CPU samples the CRUIN line on the leading edge of Q1 of clock cycle 2. Data must be valid 40 ns (min) before that.

HARDWARE DESCRIPTION

An overview of the hardware used to buffer the IN and output signals on the I/O bus is given in figure 4, p 128 and 5, p 131.

ADDRESS BUS BUFFERING

U503, U509 and U510 are used to buffer address lines A0 throgh A14. U510 is only used A0, A1, A2 and A15/CRUOUT. This last signal has a series resistor R512 to reduce transients on the line.

WE is buffered by U510 on the output (PIN 10). A series resistor R505 is used to reduce transients.

CRUCLK

The CRUCLK signal from the 99/4 is inverted in U602 and then buffered by U510. Again a series resistor R507 is used to reduce transients. The buffered signal is also used on the GROM port.

Q3

Q3 is buffered by U510, R506 used to reduce transients.

MBE

MBE is buffered by U510.

DBIN

DBIN is buffered by the two inverters U508.

DATA BUS

Since data bus is buffered by U616 in the interfacing circuit, no additional buffering is necessary. However to meet loading requirements a special pull-up/pull down circuitry is added. When DBIN is low, Q500 is in the on state.

R515 is used to reduce the base current in Q500, C506 is added to improve the switching speed. When in the on state, resistor pack R500 is connected to ground, thus generating a pull-down. When DBIN is low, Q500 is disabled. CR501, R513, R514, CR502 and R516 compose a circuit which gives a voltage of 5...volt on point A. Thus a pull-up exists when DBIN is low.

OUTPUT BUS PIN CONNECTIONS

An overview of the I/O bus pin connections is given on p. 104

POWER SUPPLY BOARD

GENERAL DESCRIPTION

The US power supply consists of an exter
regulator board inside the Home Computer.
Connection between the console and wa
connector.
The regulator board supplies the 99/4 t
and -5 volt. The +12 and -5 volt suppli
regulator, the +5 volt supply uses a swi

SWITCHING REGULATOR

The switching regulator used is a ua
in fig[illegible]9.In essence the ua 723 is
it is connected in such a way that it be
From the block diagram it can be seen th
compensated voltage reference, an
limiting circuit.

HARDWARE DESCRIPTION

+12 VOLT SUPPLY

The +12 volt regulator circuit shares
volt regulator. Thi
consisting of L1, L2, C1, C2, C3 and C4.
interference on the mains.
D1, D2, D3 and D4 compose the bridge rec
C9 and C17 are used to reduce the ripple
The DC voltage is fed to the three
regulates the input voltage down to +1
voltage swing due to fast changing load

-5 VOLT SUPPLY

The -5 volt supply uses a separate
together with C5 and C6 compose a RF fil
by D5, C8 reduces the ripple on the outp
U2 is a 5 volt fixed regulator. C7 on t
due to fast changing load conditions.

+5 VOLT SUPPLY

REFERENCE VOLTAGE

The reference voltage for the regula
R1, D7 and zener diode D8 compose a 7
compensate for temperature variations.
The 7 volt reference is divided by R11,
through R19 are supplied with jumper w
that the voltage on the non inverting ir
Since this comparator has an open co
pull-up. R14 connected between the
(pin 2) sets the voltage gain to 1.
feedback. Since in this configuration t
gain amplifier, the voltage on the ir

that of the divider. This voltage is used as reference for the switching regulator U3. C16 is used to ensure a slow starting up of the +5 volt regulator, thus the starting condition that the -5 volt is applied first to the circuitry inside the 99/4 is met. C16 also determines the frequency at which the +5V regualtor switches.

SWITCHING REGULATOR

Switching regulator U3 (US 723 C) uses the following circuitry:

REFERENCE VOLTAGE

The reference voltage on pin 2 of U4 is connected to the non inverting input of U3 (pin 5).

FEEDBACK VOLTAGE

The +5 volt is directly connected to the inverting input of U3 (PIN 4).

POWER CONNECTION

Power is connected to pin 12 of U3 via R3. C13 is used to reduce voltage swings on the power line. Since the power comes from the +12 volt supply, the switching regulator only works when this voltage is present. Ground connection is to pin 7.

FREQUENCY COMPENSATION

Frequency compensation is performed by C11 on pin 13.

REGULATING CIRCUIT

The output of U3 on pin 11 is used to switch the current through L4 after amplification by Q1 and Q2. R5 reduces the input current of Q1. R4 and R6 are used to ensure that both Q1 and Q2 are in the non conducting state when not enabled by U3.

The flyback circuitry consists of L4 and D9. The output voltage ripple is reduced by C14 and C15.

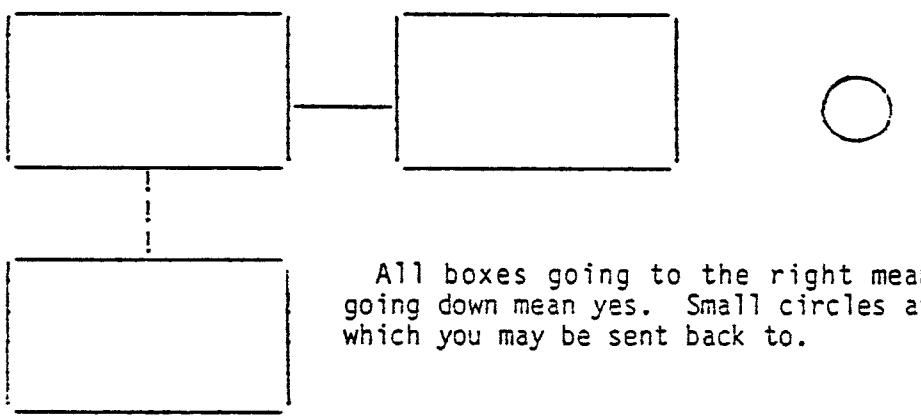
CURRENT LIMITING

Current limiting is done by using the voltage drop over R9/R10 and comparing this with the voltage on the cathode of the diode the divider circuit consisting of R7, R8 and D10.

D10 is used for temperature compensation.

TEXAS INSTRUMENTS HOME COMPUTER
TROUBLE SHOOTING GUIDE

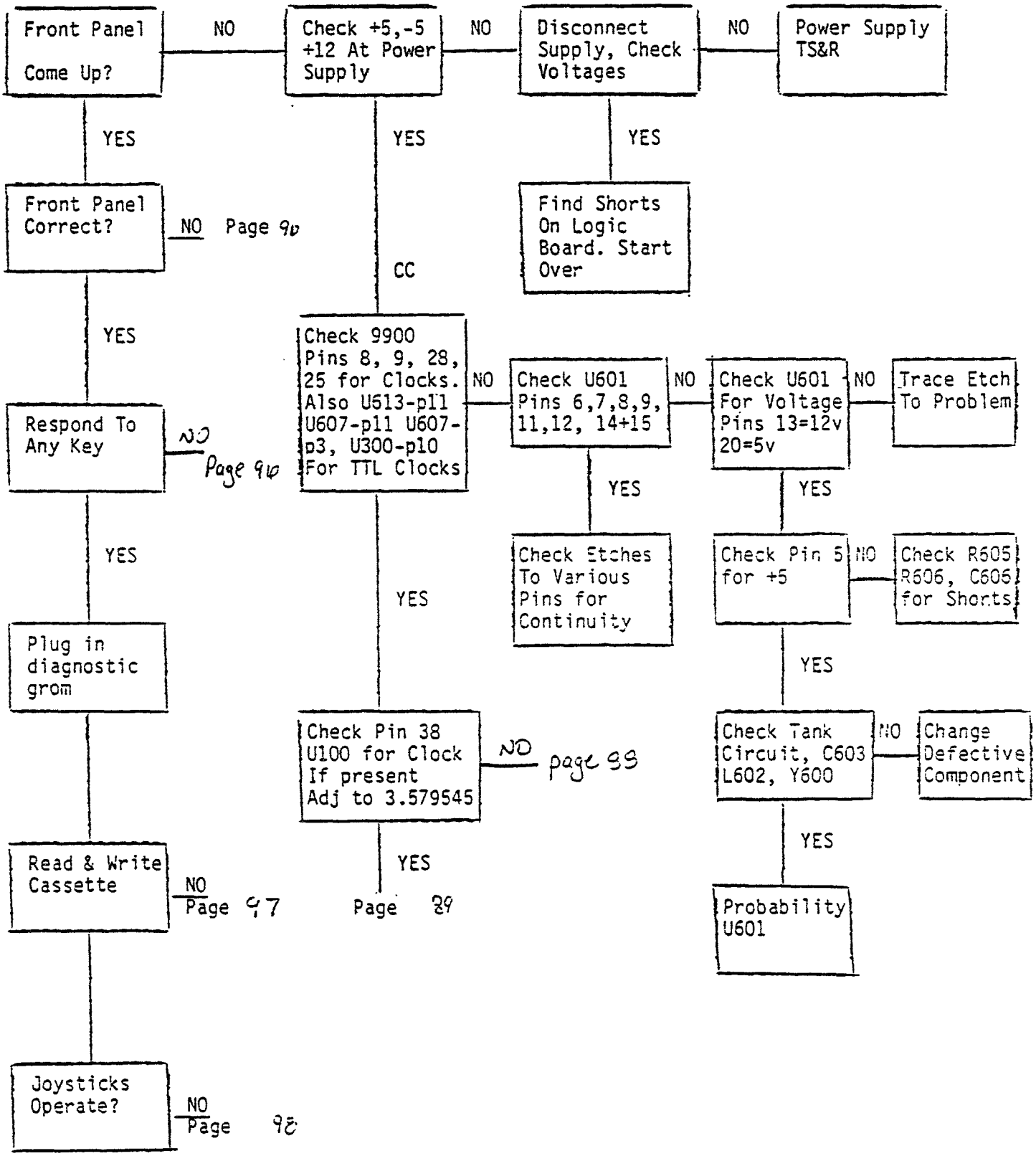
This guide will take you by the problem, not neccessarily to the problem. You still need your basic troubleshooting skills. This guide is aimed at the new technician but still can be referenced when in doubt.

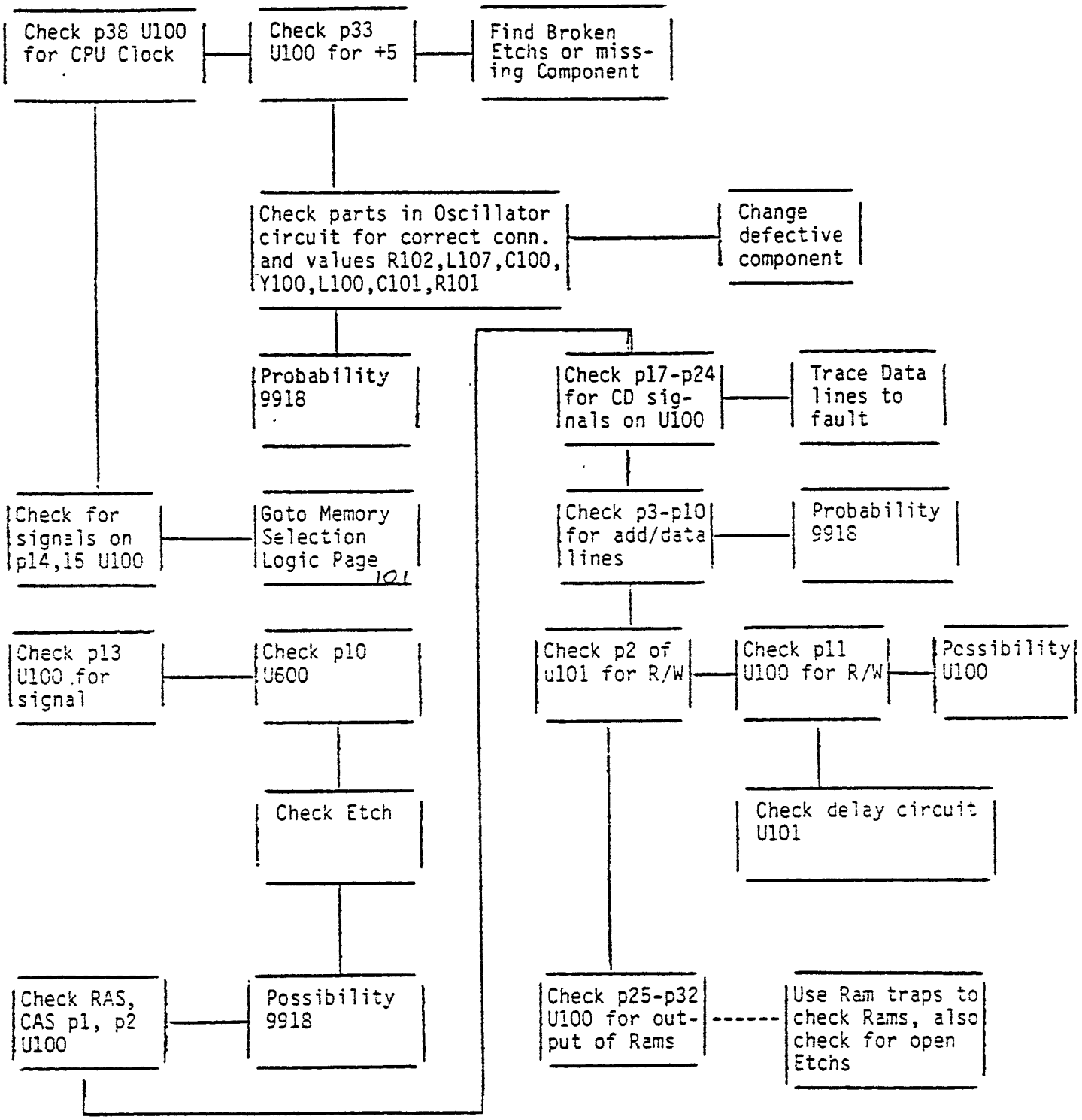


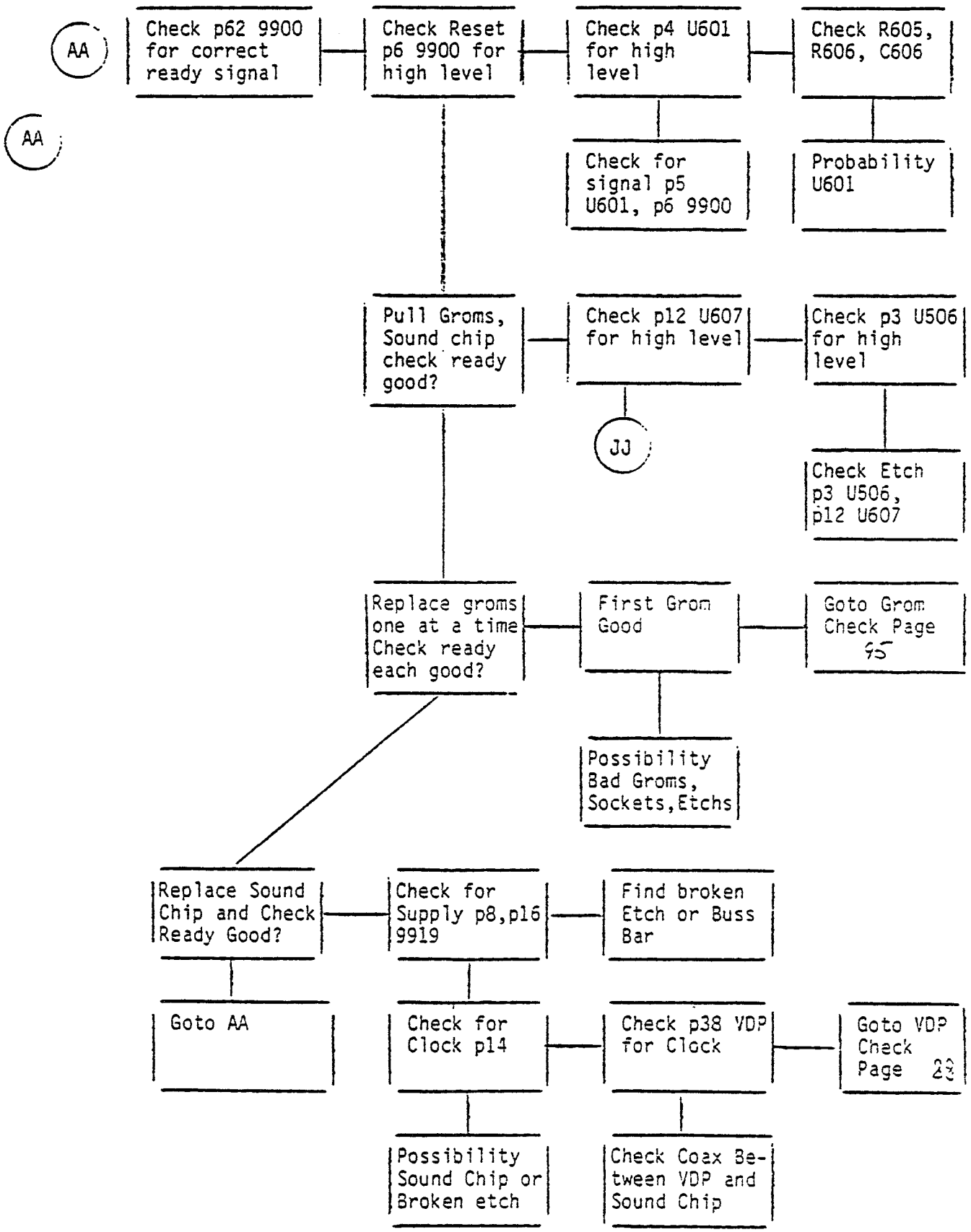
All boxes going to the right mean no, and all boxes going down mean yes. Small circles are reference points which you may be sent back to.

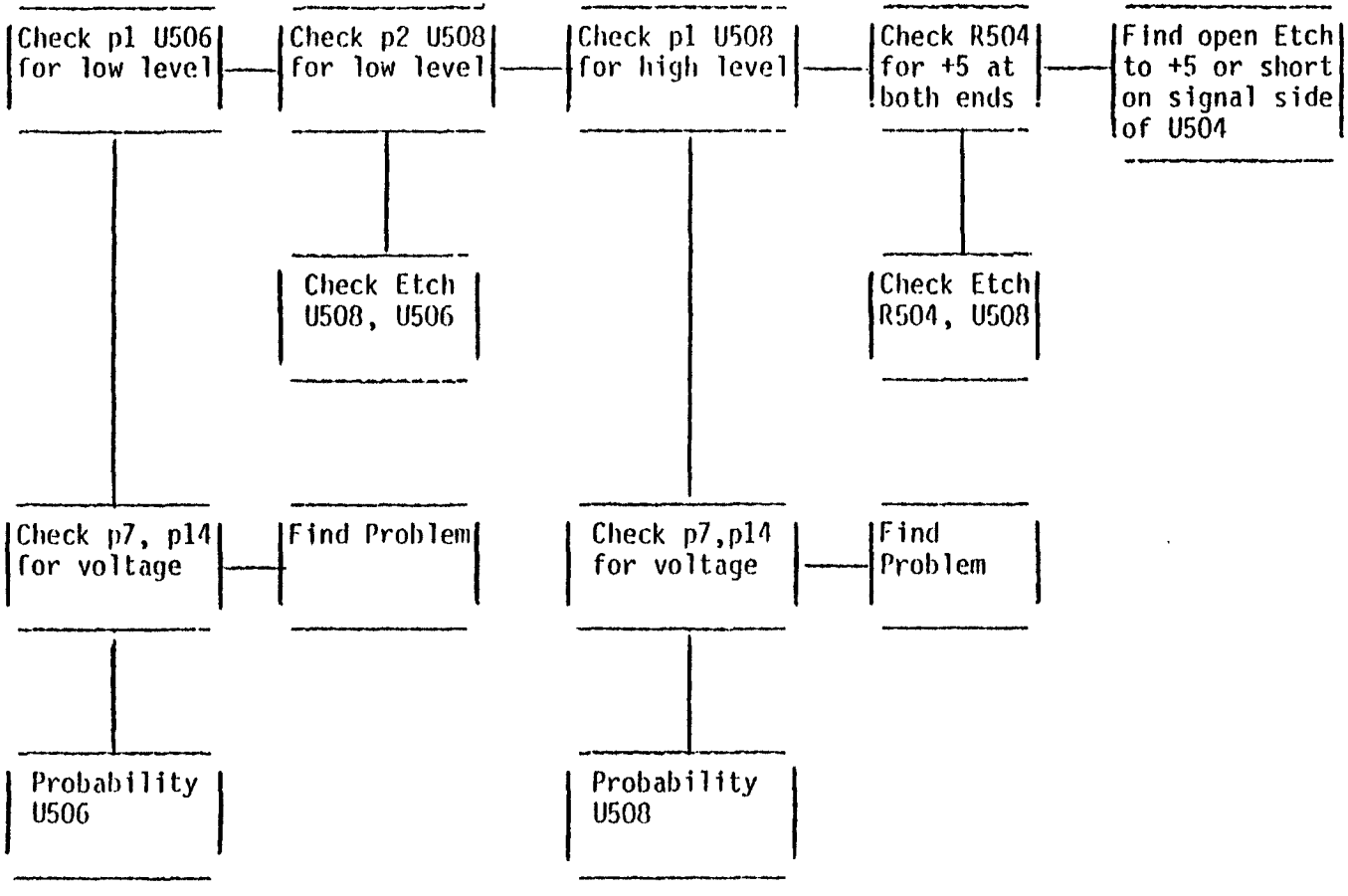
Page	87	Start
Page	88	VDP Check
Page	89	System Ready
Page	95	Grom Check
Page	96	Front Panel Incorrect and Keyboard
Page	97	Cassette
Page	98	Joysticks
Page	99	Multiplex
Page	101	Memory Selection Logic
Page	103	INTREQ

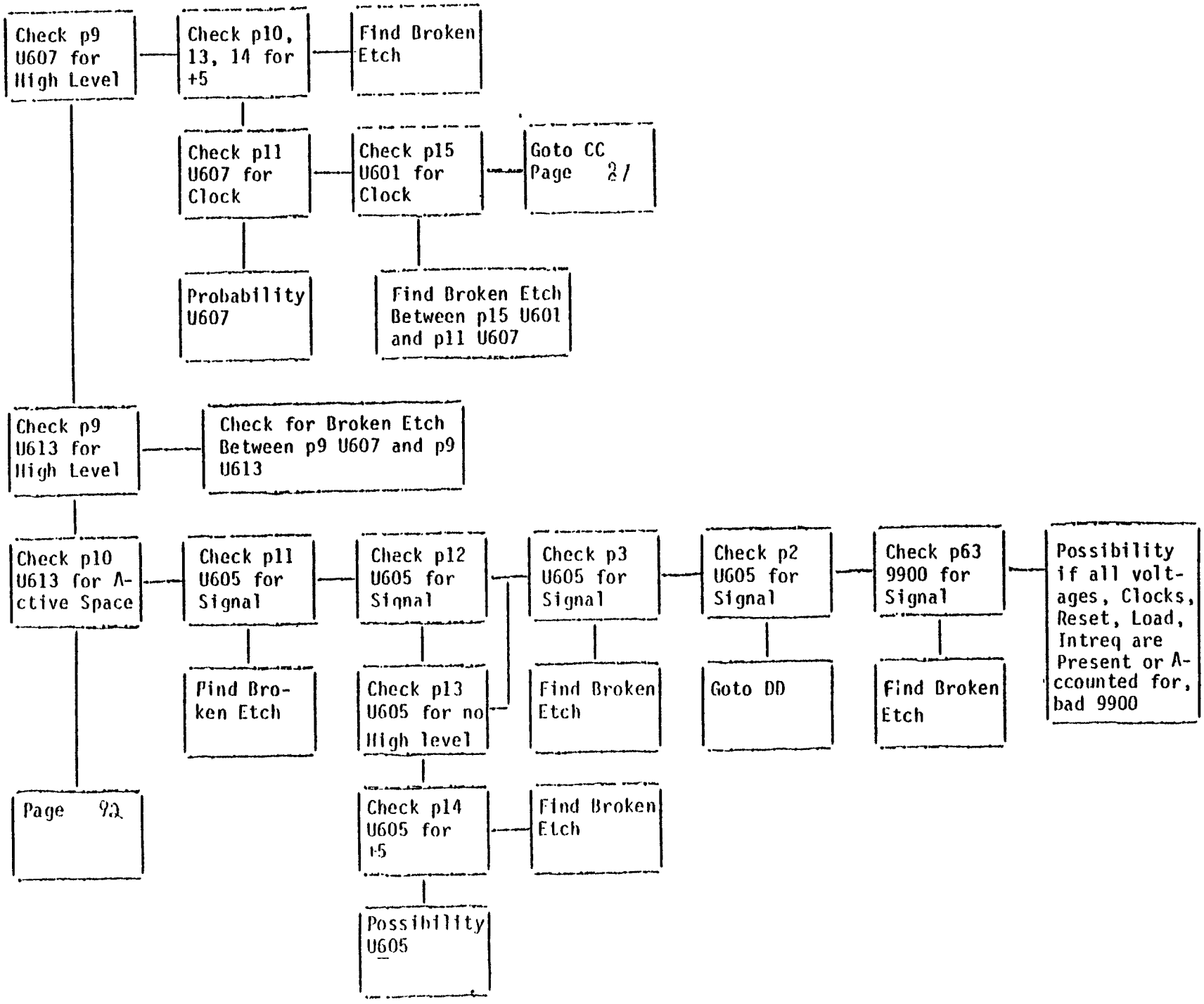
Compiled by Curt Larsen and Paul Greenwood

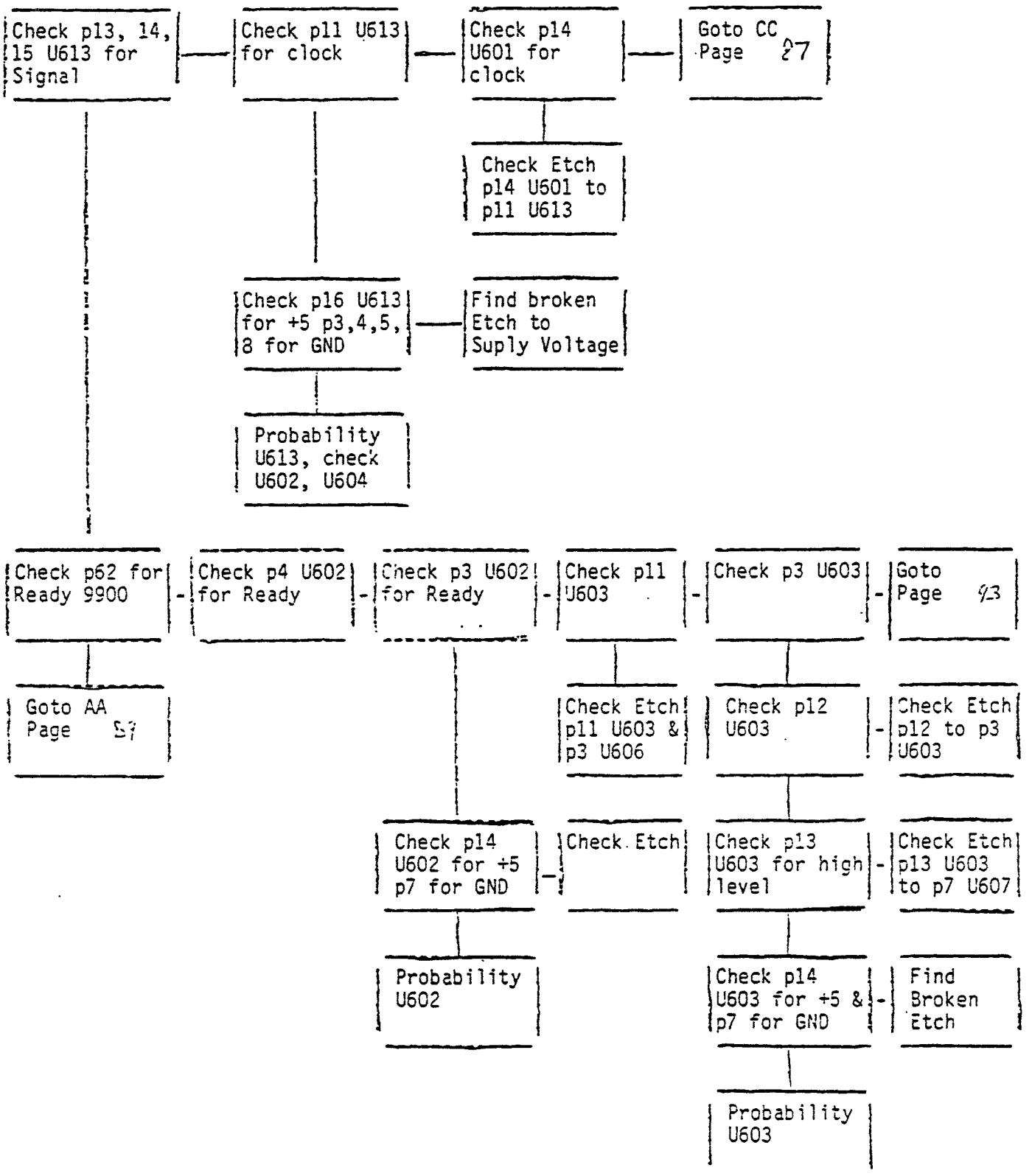

Front Panel Come Up?
NO
Check +5,-5 +12 At Power Supply
NO
Disconnect Supply, Check Voltages
NO
Power Supply TS&R
YES
YES
YES
Front Panel Correct?
NO Page 9b
Find Shorts On Logic Board. Start Over
CC
YES
Check 9900 Pins 8, 9, 28, 25 for Clocks. Also U613-p11 U607-p11 U607-p3, U300-p10 For TTL Clocks
NO
Check U601 Pins 6,7,8,9, 11,12, 14+15
NO
Check U601 For Voltage Pins 13=12v 20=5v
NO
Trace Etch To Problem
Respond To Any Key
NO Page 9b
YES
YES
YES
Check Etches To Various Pins for Continuity
Check Pin 5 for +5
NO
Check R605 R606, C606 for Shorts
YES
YES
YES
Plug in diagnostic grom
Check Pin 38 U100 for Clock If present Adj to 3.579545
NO page 99
Check Tank Circuit, C603 L602, Y600
NO
Change Defective Component
YES
YES
YES
Read & Write Cassette
NO Page 97
Page 89
Probability U601
Joysticks Operate?
NO Page 98

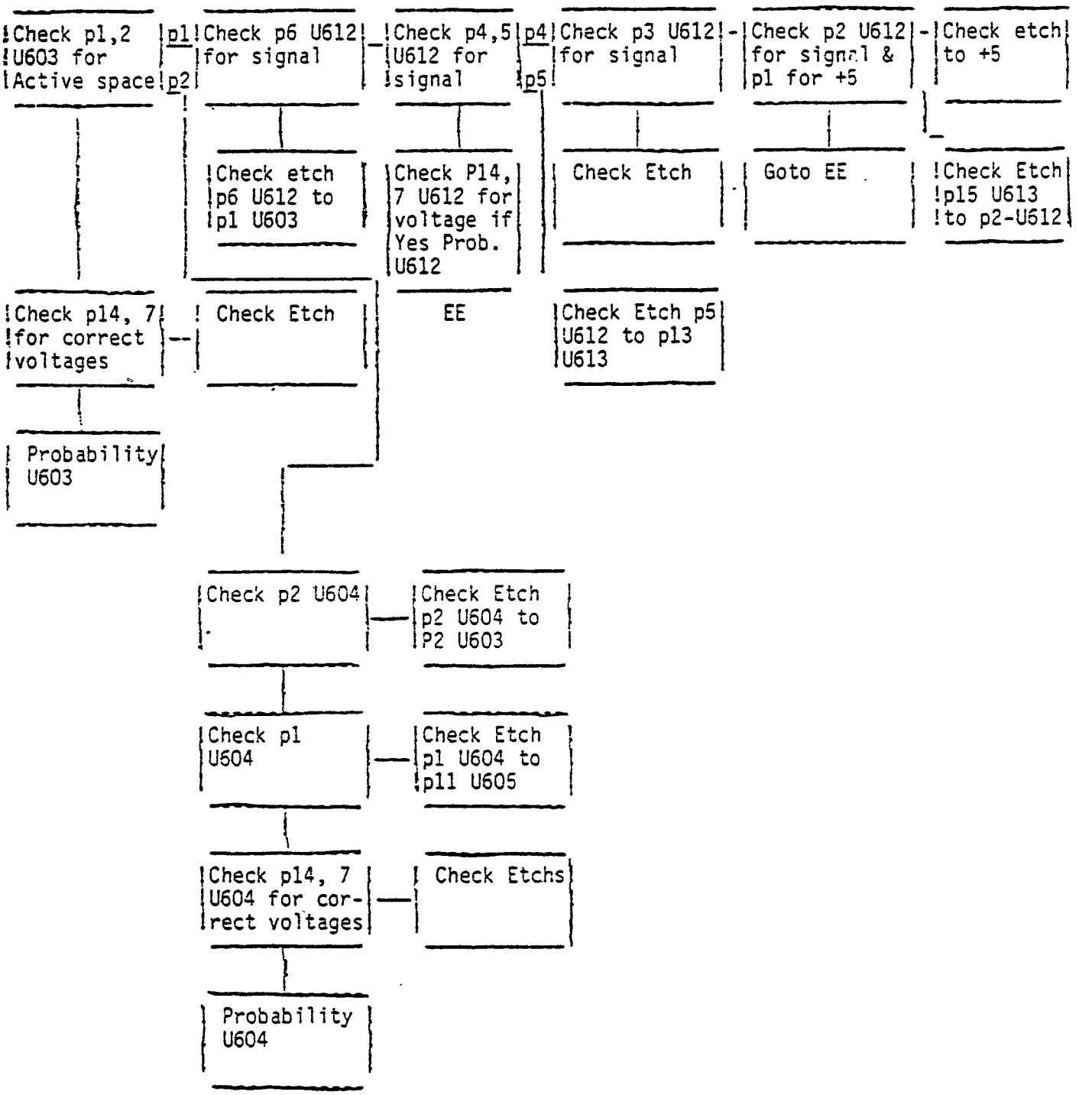

Check p38 U100 for CPU Clock
Check p33 U100 for +5
Find Broken Etchs or miss-ing Component
Check parts in Oscillator circuit for correct conn. and values R102,L107,C100, Y100,L100,C101,R101
Change defective component
Probability 9918
Check p17-p24 for CD sig-nals on U100
Trace Data lines to fault
Check for signals on p14,15 U100
Goto Memory Selection Logic Page 101
Check p3-p10 for add/data lines
Probability 9918
Check p13 U100 for signal
Check p10 U600
Check p2 of u101 for R/W
Check p11 U100 for R/W
Possibility U100
Check Etch
Check delay circuit U101
Check RAS, CAS p1, p2 U100
Possibility 9918
Check p25-p32 U100 for out-put of Rams
Use Ram traps to check Rams, also check for open Etchs

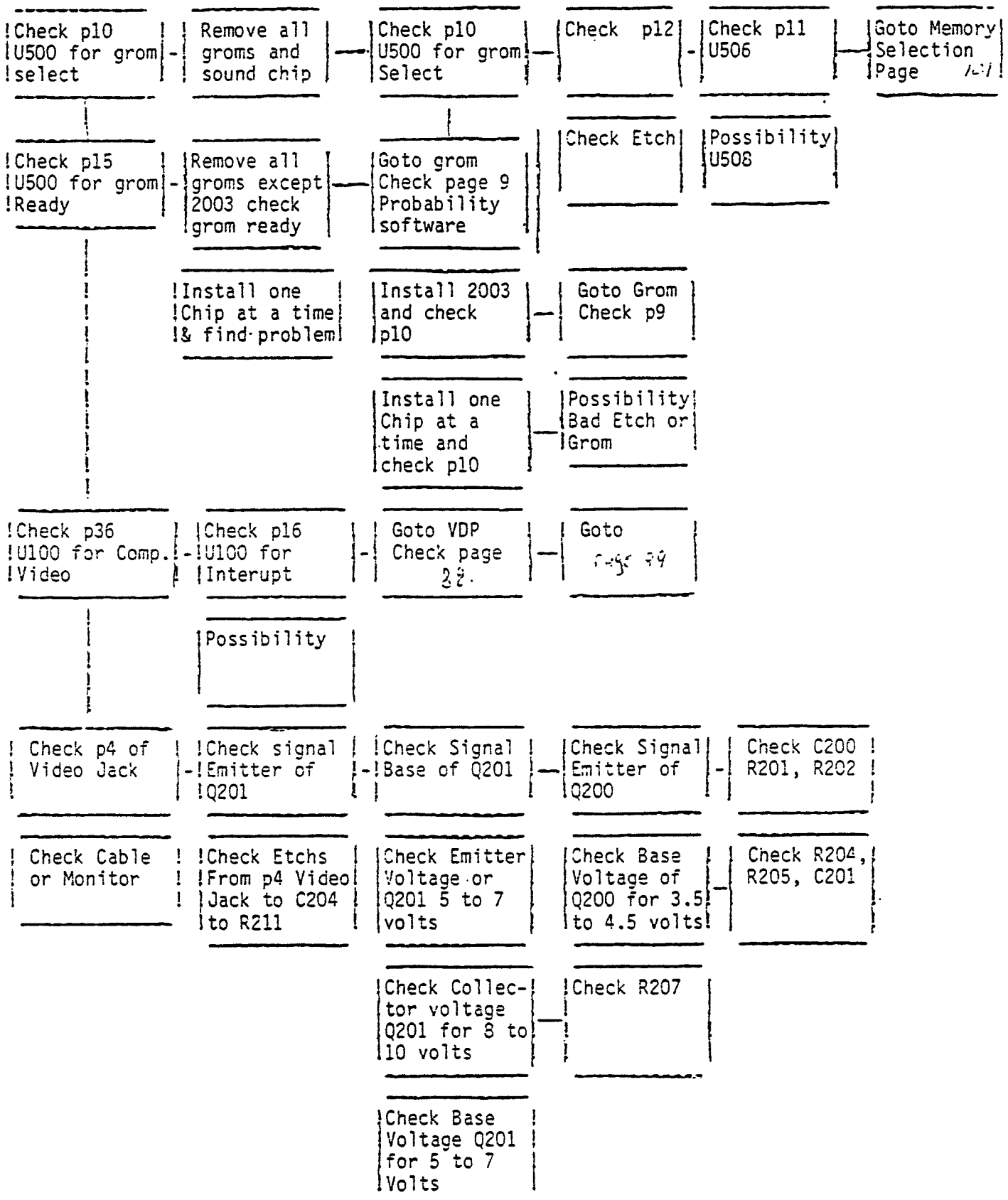

AA
Check p62 9900 for correct ready signal
Check Reset p6 9900 for high level
Check p4 U601 for high level
Check R605, R606, C606
AA
Check for signal p5 U601, p6 9900
Probability U601
Pull Groms, Sound chip check ready good?
Check p12 U607 for high level
Check p3 U506 for high level
JJ
Check Etch p3 U506, p12 U607
Replace groms one at a time Check ready each good?
First Grom Good
Goto Grom Check Page 15
Possibility Bad Groms, Sockets, Etchs
Replace Sound Chip and Check Ready Good?
Check for Supply p8,p16 9919
Find broken Etch or Buss Bar
Goto AA
Check for Clock p14
Check p38 VDP for Clock
Goto VDP Check Page 23
Possibility Sound Chip or Broken etch
Check Coax Between VDP and Sound Chip

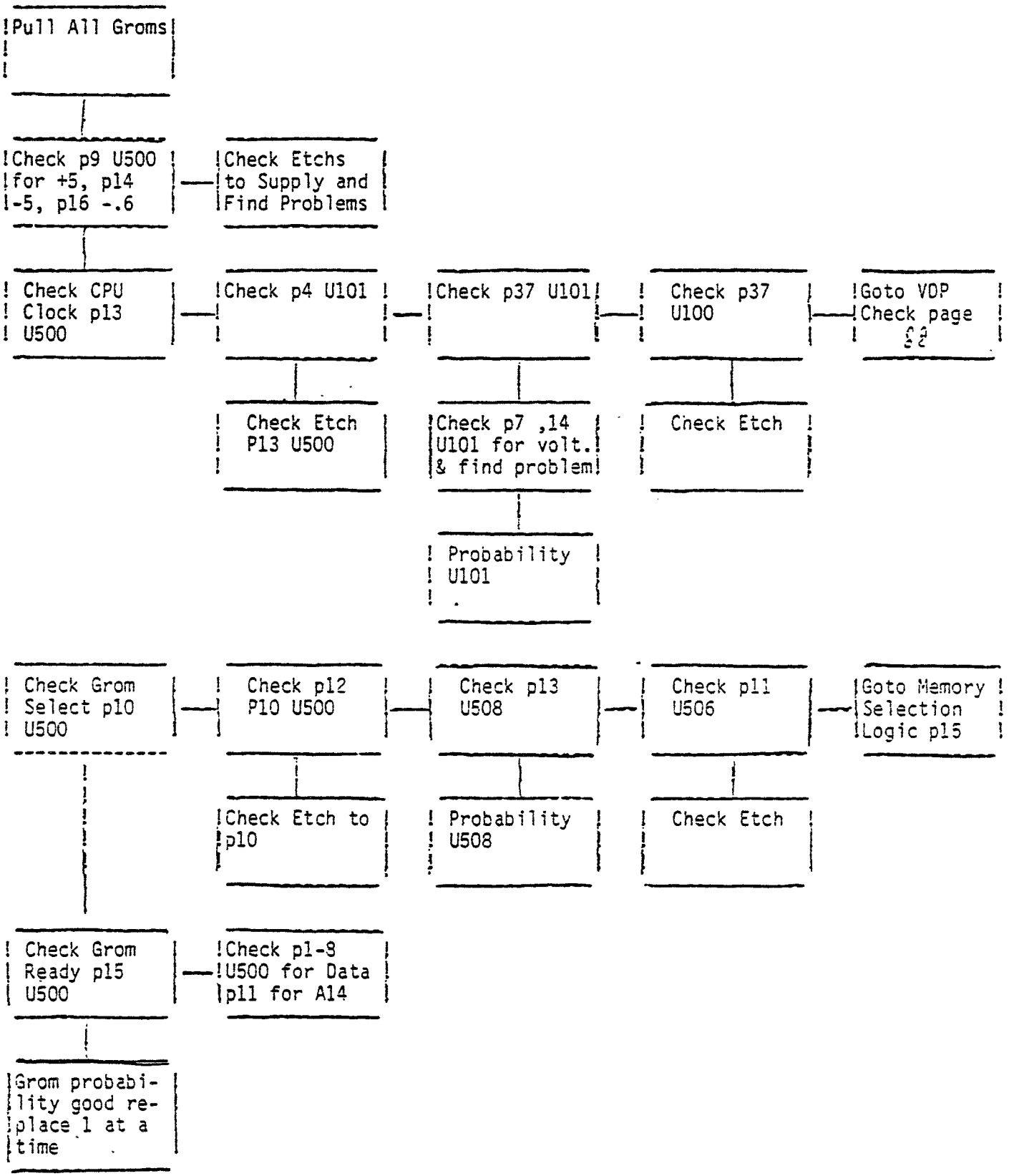

Check p1 U506 for low level
Check p2 U508 for low level
Check p1 U508 for high level
Check R504 for +5 at both ends
Find open Etch to +5 or short on signal side of U504
Check Etch U508, U506
Check Etch R504, U508
Check p7, p14 for voltage
Find Problem
Check p7,p14 for voltage
Find Problem
Probability U506
Probability U508

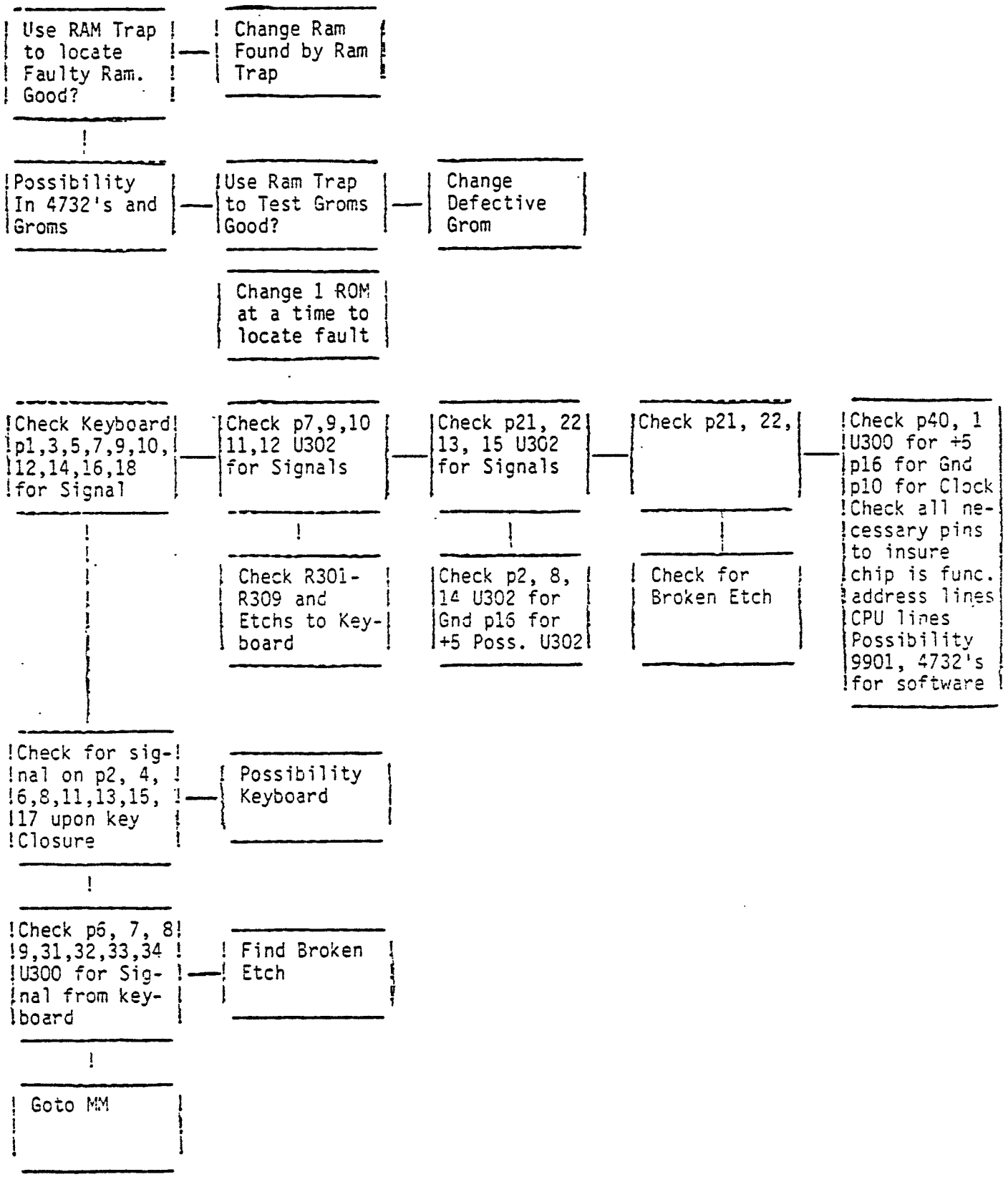

Check p9 U607 for High Level
Check p10, 13, 14 for +5
Find Broken Etch
Check p11 U607 for Clock
Check p15 U601 for Clock
Goto CC Page 21
Probability U607
Find Broken Etch Between p15 U601 and p11 U607
Check p9 U613 for High Level
Check for Broken Etch Between p9 U607 and p9 U613
Check p10 U613 for Active Space
Check p11 U605 for Signal
Check p12 U605 for Signal
Check p3 U605 for Signal
Check p2 U605 for Signal
Check p63 9900 for Signal
Possibility if all voltages, Clocks, Reset, Load, Intreq are Present or Accounted for, bad 9900
Find Broken Etch
Check p13 U605 for no High level
Find Broken Etch
Goto DD
Find Broken Etch
Page 92
Check p14 U605 for +5
Find Broken Etch
Possibility U605

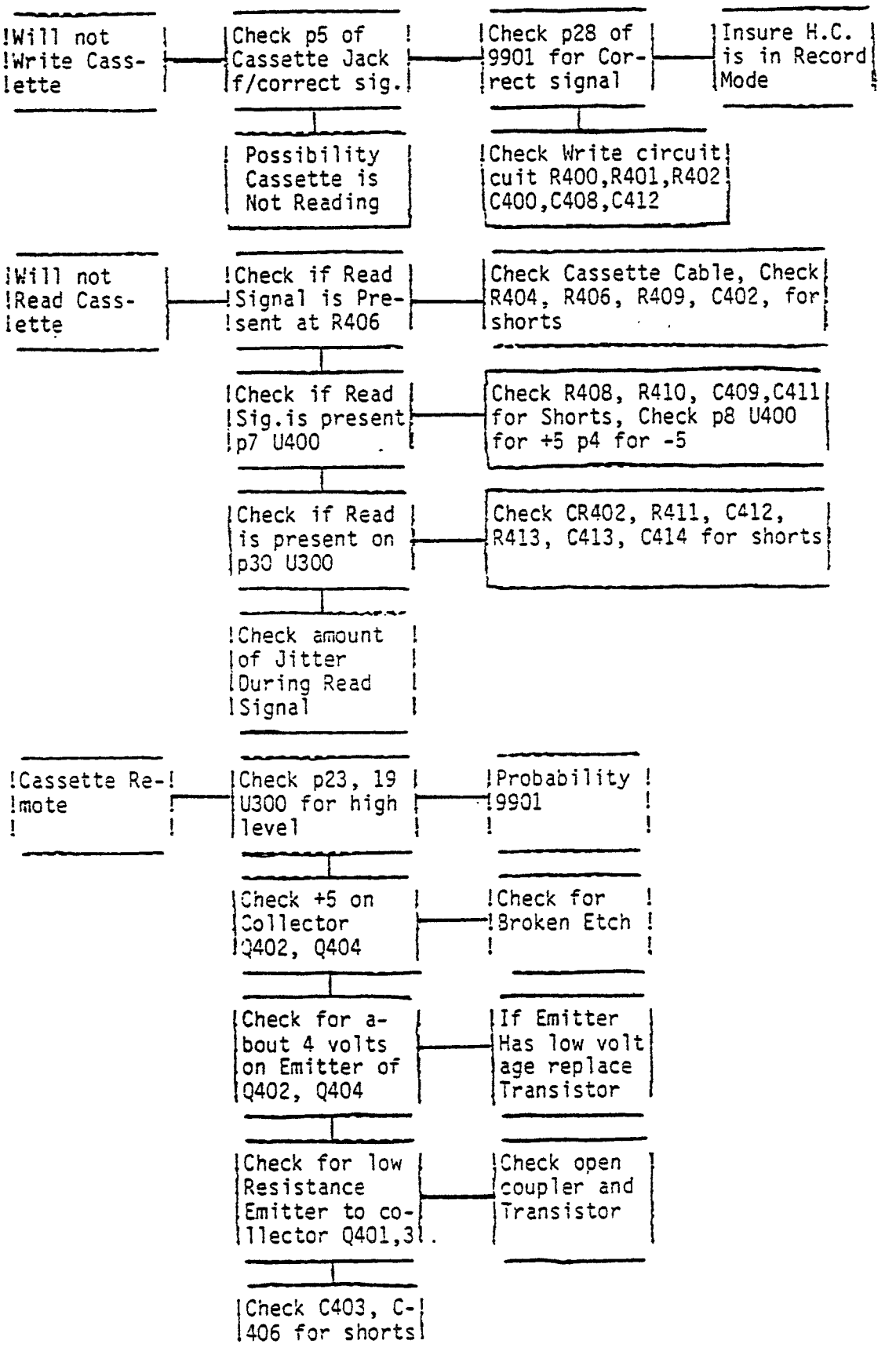

Check p13, 14, 15 U613 for Signal
Check p11 U613 for clock
Check p14 U601 for clock
Goto CC Page 27
Check Etch p14 U601 to p11 U613
Check p16 U613 for +5 p3,4,5, 8 for GND
Find broken Etch to Suply Voltage
Probability U613, check U602, U604
Check p62 for Ready 9900
Check p4 U602 for Ready
Check p3 U602 for Ready
Check p11 U603
Check p3 U603
Goto Page 93
Goto AA Page 57
Check Etch p11 U603 & p3 U606
Check p12 U603
Check Etch p12 to p3 U603
Check p14 U602 for +5 p7 for GND
Check Etch
Check p13 U603 for high level
Check Etch p13 U603 to p7 U607
Probability U602
Check p14 U603 for +5 & p7 for GND
Find Broken Etch
Probability U603

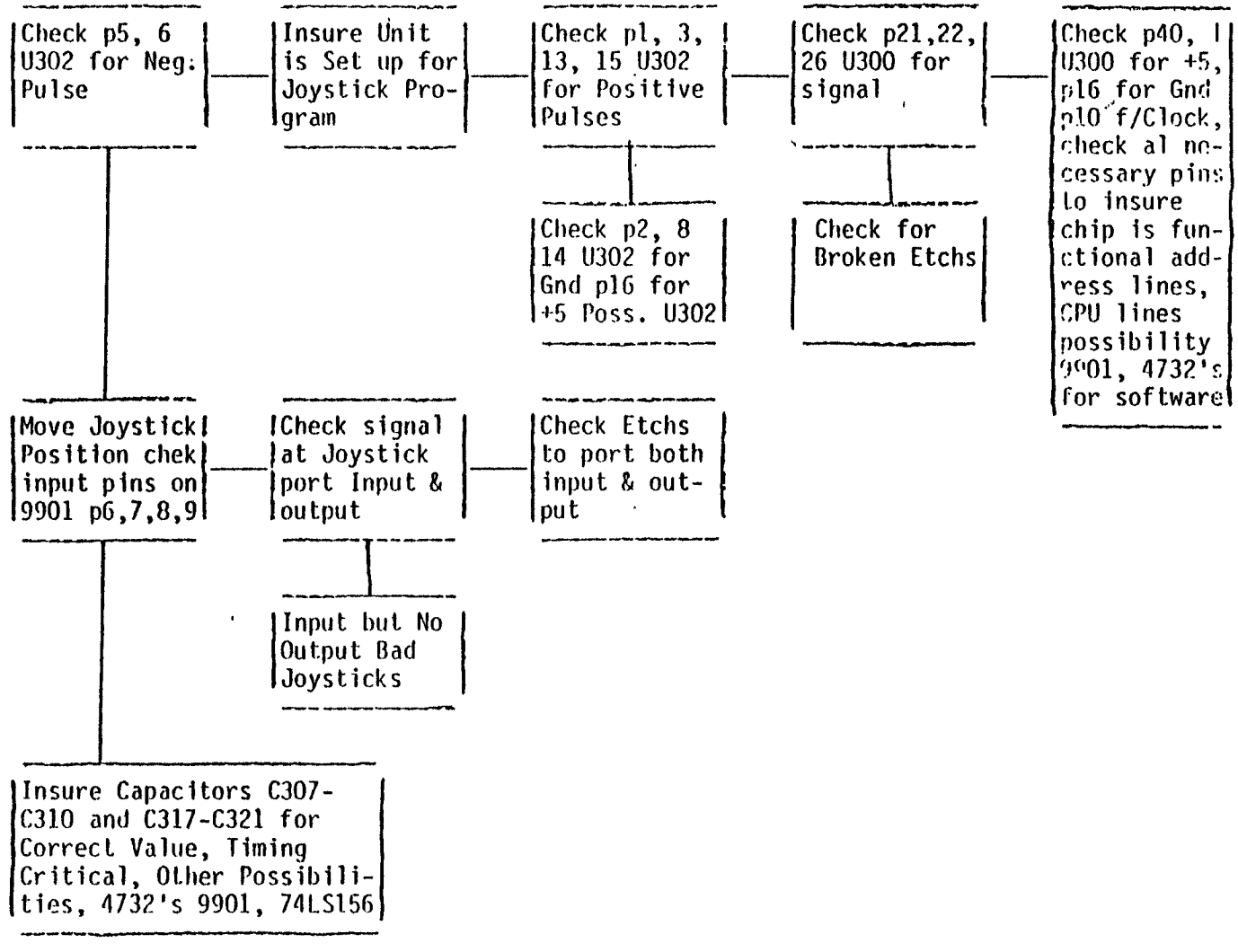

Check p1,2 U603 for Active space
p1
p2
Check p6 U612 for signal
Check p4,5 U612 for signal
p4
p5
Check p3 U612 for signal
Check p2 U612 for signal & p1 for +5
Check etch to +5
Check etch p6 U612 to p1 U603
Check P14, 7 U612 for voltage if Yes Prob. U612
Check Etch
Goto EE
Check Etch p15 U613 to p2-U612
Check p14, 7 for correct voltages
Check Etch
EE
Check Etch p5 U612 to p13 U613
Probability U603
Check p2 U604
Check Etch p2 U604 to P2 U603
Check p1 U604
Check Etch p1 U604 to p11 U605
Check p14, 7 U604 for correct voltages
Check Etchs
Probability U604

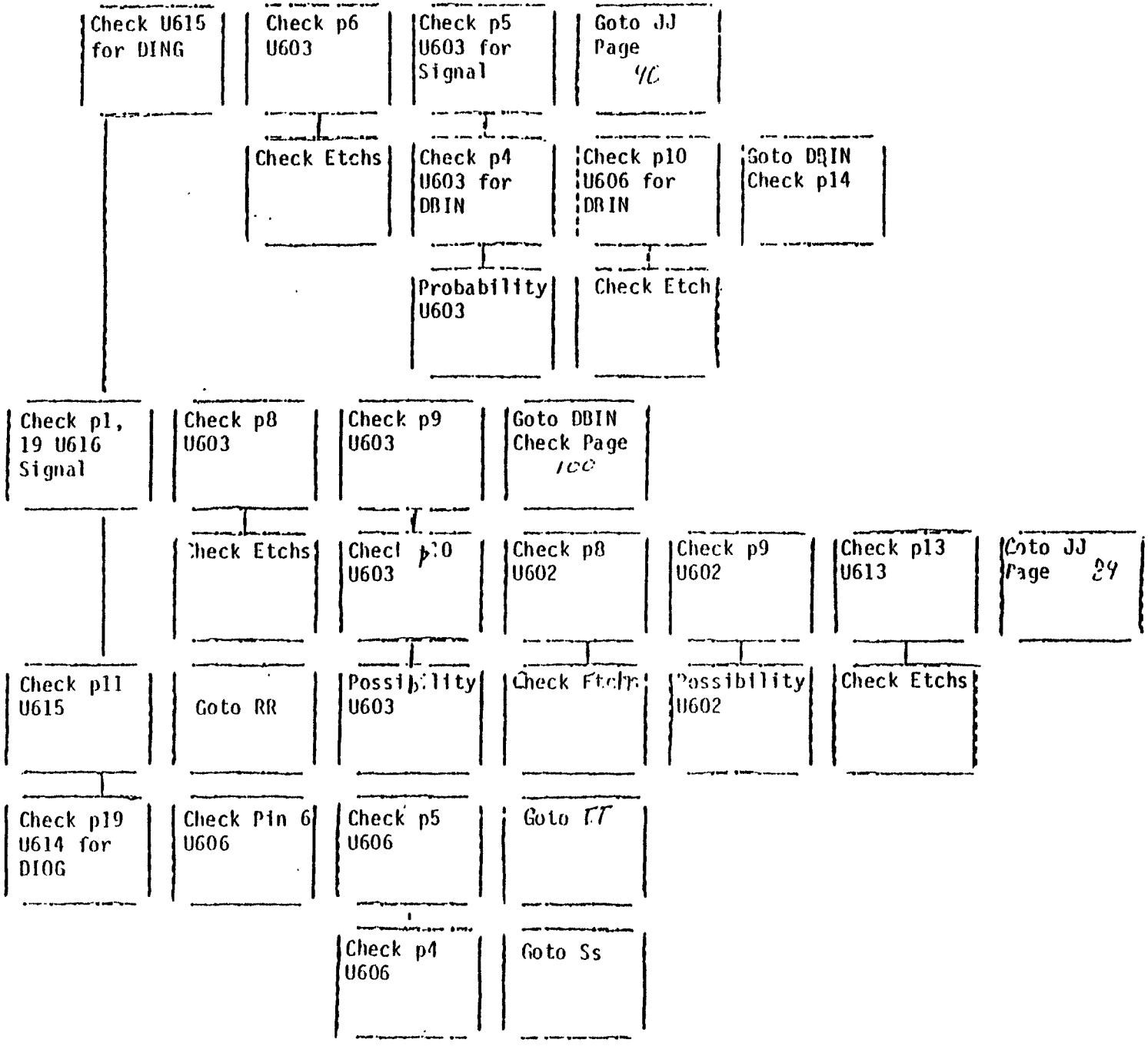

Check p10 U500 for grom select
Remove all groms and sound chip
Check p10 U500 for grom Select
Check p12
Check p11 U506
Goto Memory Selection Page
Check p15 U500 for grom Ready
Remove all groms except 2003 check grom ready
Goto grom Check page 9 Probability software
Check Etch
Possibility U508
Install one Chip at a time & find problem
Install 2003 and check p10
Goto Grom Check p9
Install one Chip at a time and check p10
Possibility Bad Etch or Grom
Check p36 U100 for Comp. Video
Check p16 U100 for Interupt
Goto VDP Check page 28.
Goto page 29
Possibility
Check p4 of Video Jack
Check signal Emitter of Q201
Check Signal Base of Q201
Check Signal Emitter of Q200
Check C200 R201, R202
Check Cable or Monitor
Check Etchs From p4 Video Jack to C204 to R211
Check Emitter Voltage or Q201 5 to 7 volts
Check Base Voltage of Q200 for 3.5 to 4.5 volts
Check R204, R205, C201
Check Collector voltage Q201 for 8 to 10 volts
Check R207
Check Base Voltage Q201 for 5 to 7 Volts

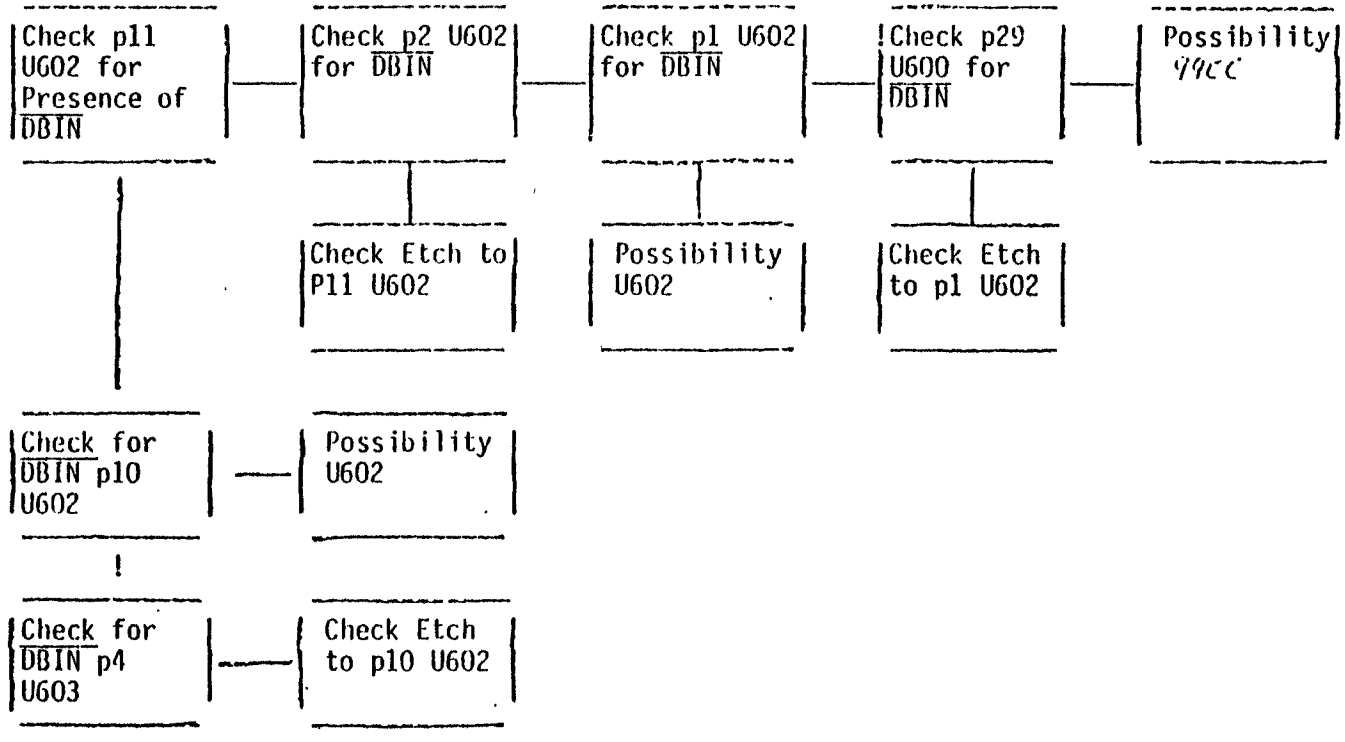

Pull All Groms
Check p9 U500 for +5, p14 -5, p16 -.6
Check Etchs to Supply and Find Problems
Check CPU Clock p13 U500
Check p4 U101
Check p37 U101
Check p37 U100
Goto VDP Check page 22
Check Etch P13 U500
Check p7 ,14 U101 for volt. & find problem
Check Etch
Probability U101
Check Grom Select p10 U500
Check p12 P10 U500
Check p13 U508
Check p11 U506
Goto Memory Selection Logic p15
Check Etch to p10
Probability U508
Check Etch
Check Grom Ready p15 U500
Check p1-8 U500 for Data p11 for A14
Grom probability good replace 1 at a time

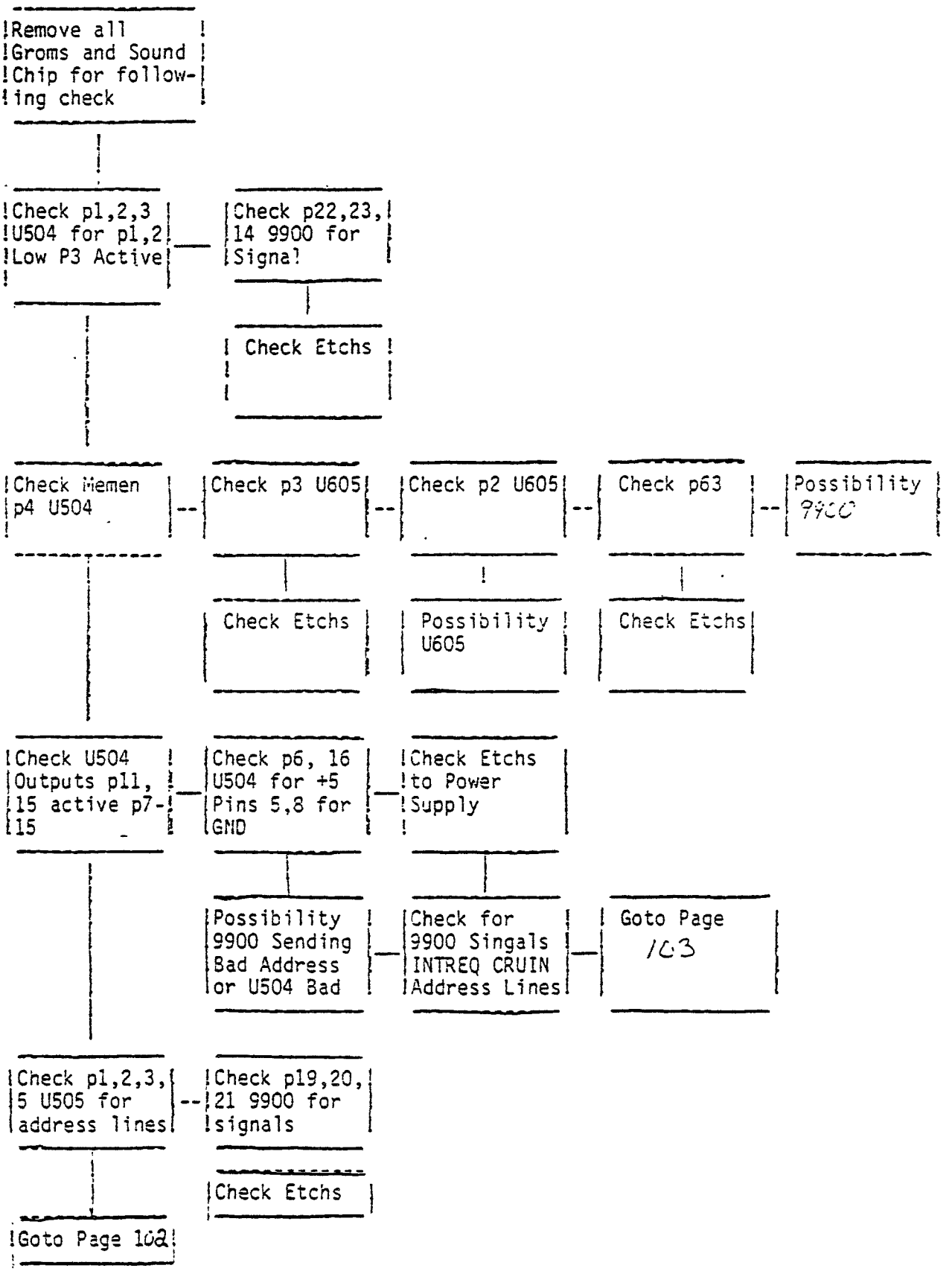

Use RAM Trap to locate Faulty Ram. Good?
Change Ram Found by Ram Trap
Possibility In 4732's and Groms
Use Ram Trap to Test Groms Good?
Change Defective Grom
Change 1 ROM at a time to locate fault
Check Keyboard p1,3,5,7,9,10, 12,14,16,18 for Signal
Check p7,9,10 11,12 U302 for Signals
Check p21, 22 13, 15 U302 for Signals
Check p21, 22,
Check p40, 1 U300 for +5 p16 for Gnd p10 for Clock Check all necessary pins to insure chip is func. address lines CPU lines Possibility 9901, 4732's for software
Check R301-R309 and Etchs to Keyboard
Check p2, 8, 14 U302 for Gnd p16 for +5 Poss. U302
Check for Broken Etch
Check for signal on p2, 4, 6,8,11,13,15, 17 upon key Closure
Possibility Keyboard
Check p6, 7, 8 9,31,32,33,34 U300 for Signal from keyboard
Find Broken Etch
Goto MM

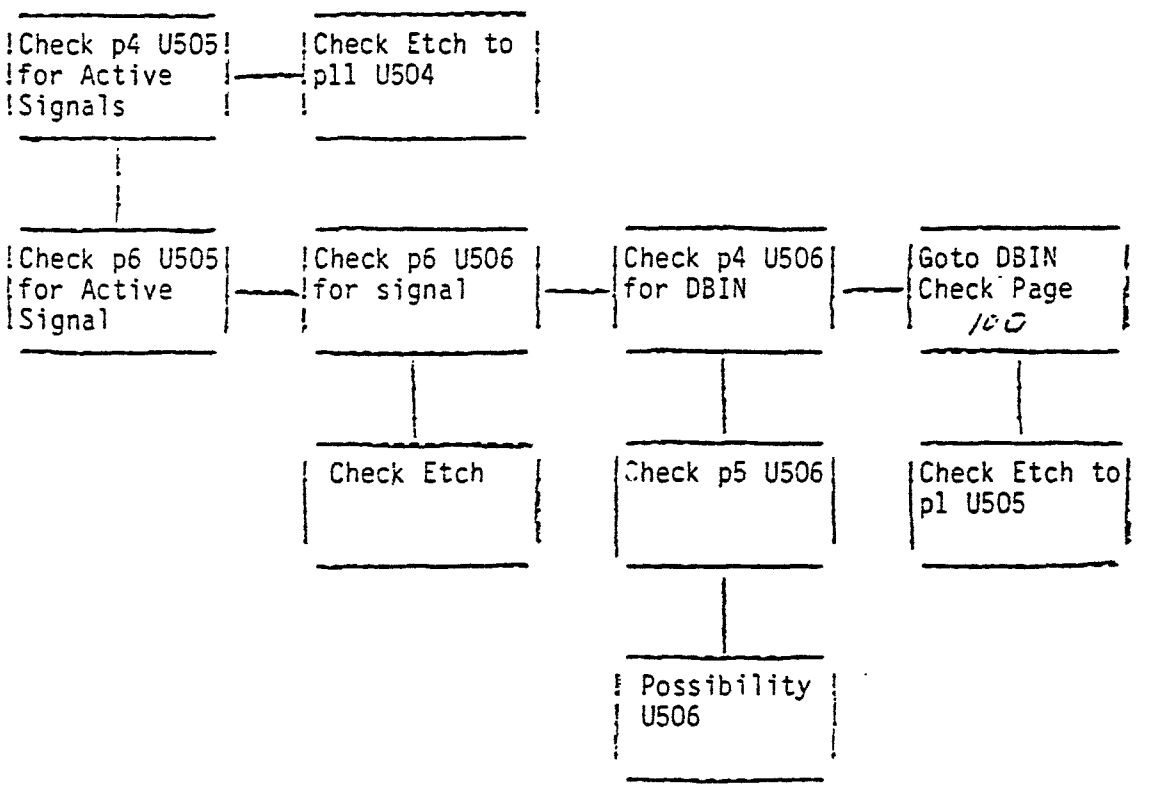

Will not Write Cassette
Check p5 of Cassette Jack f/correct sig.
Check p28 of 9901 for Correct signal
Insure H.C. is in Record Mode
Possibility Cassette is Not Reading
Check Write circuit cuit R400,R401,R402 C400,C408,C412
Will not Read Cassette
Check if Read Signal is Present at R406
Check Cassette Cable, Check R404, R406, R409, C402, for shorts
Check if Read Sig.is present p7 U400
Check R408, R410, C409,C411 for Shorts, Check p8 U400 for +5 p4 for -5
Check if Read is present on p30 U300
Check CR402, R411, C412, R413, C413, C414 for shorts
Check amount of Jitter During Read Signal
Cassette Remote
Check p23, 19 U300 for high level
Probability 9901
Check +5 on Collector Q402, Q404
Check for Broken Etch
Check for about 4 volts on Emitter of Q402, Q404
If Emitter Has low voltage replace Transistor
Check for low Resistance Emitter to collector Q401,3
Check open coupler and Transistor
Check C403, C406 for shorts

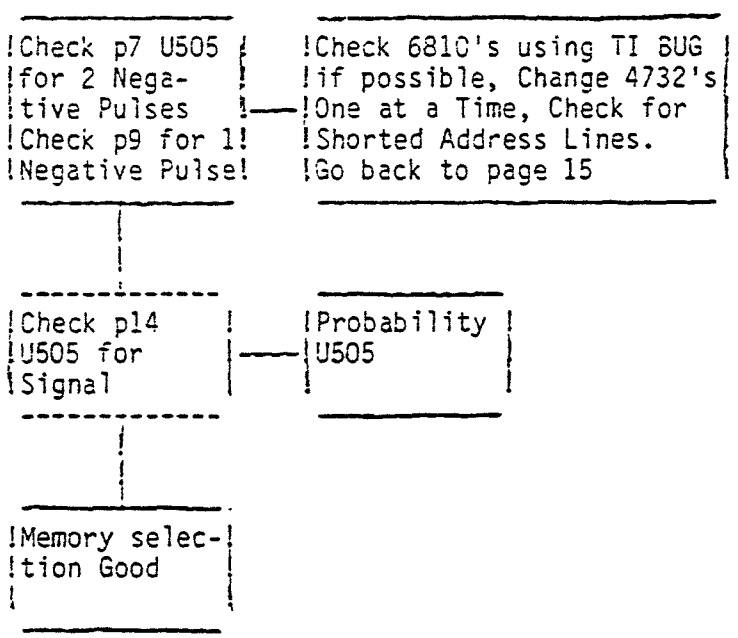

Check p5, 6 U302 for Neg: Pulse
Insure Unit is Set up for Joystick Program
Check p1, 3, 13, 15 U302 for Positive Pulses
Check p21,22, 26 U300 for signal
Check p40, 1 U300 for +5, p16 for Gnd p10 f/Clock, check al necessary pins to insure chip is functional address lines, CPU lines possibility 9901, 4732's for software
Check p2, 8 14 U302 for Gnd p16 for +5 Poss. U302
Check for Broken Etchs
Move Joystick Position chek input pins on 9901 p6,7,8,9
Check signal at Joystick port Input & output
Check Etchs to port both input & output
Input but No Output Bad Joysticks
Insure Capacitors C307-C310 and C317-C321 for Correct Value, Timing Critical, Other Possibilities, 4732's 9901, 74LS156

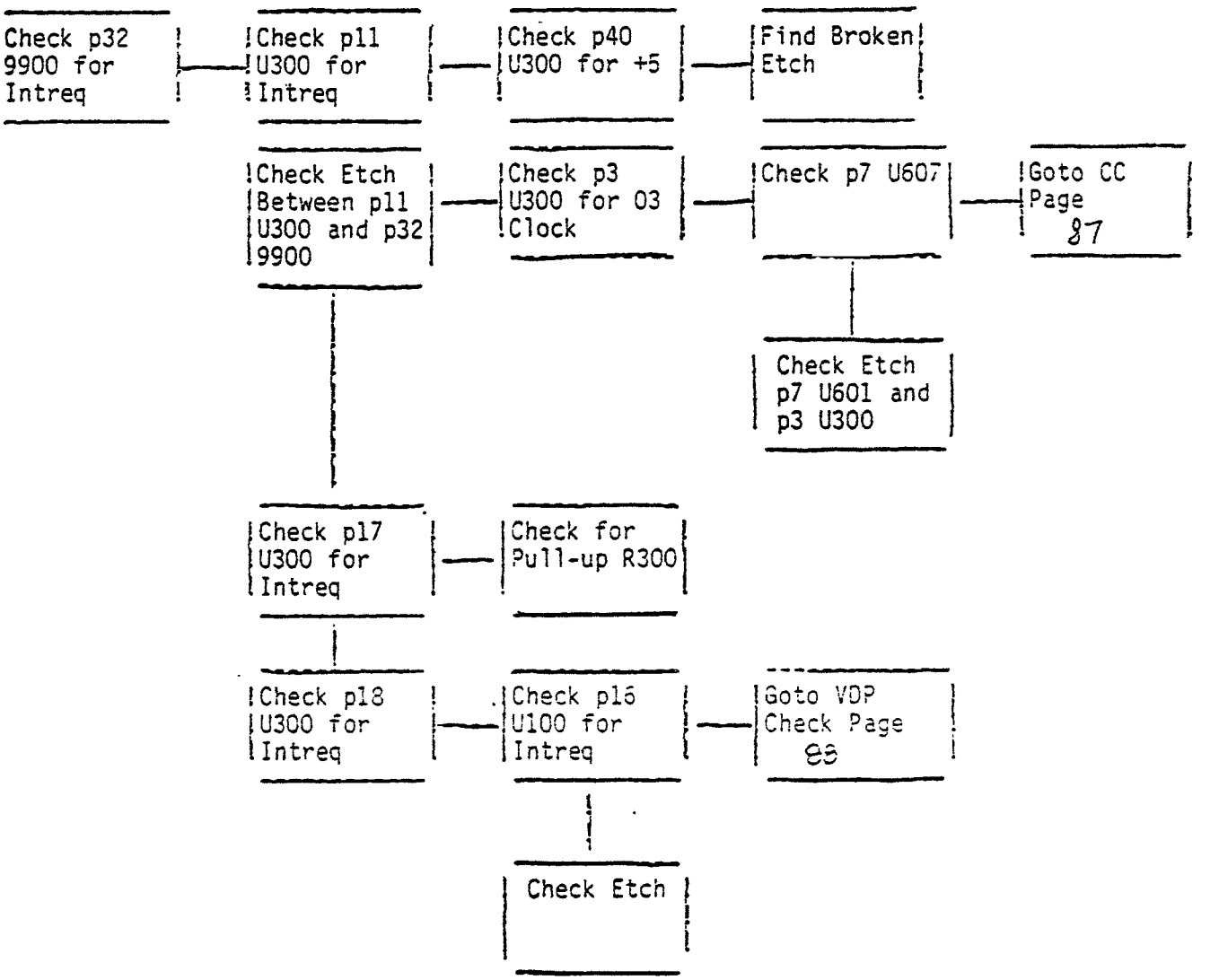

Check U615 for DING
Check p6 U603
Check p5 U603 for Signal
Goto JJ Page 4C
Check Etchs
Check p4 U603 for DBIN
Check p10 U606 for DBIN
Goto DBIN Check p14
Probability U603
Check Etch
Check p1, 19 U616 Signal
Check p8 U603
Check p9 U603
Goto DBIN Check Page 10C
Check Etchs
Check p10 U603
Check p8 U602
Check p9 U602
Check p13 U613
Goto JJ Page 29
Check p11 U615
Goto RR
Possibility U603
Check Etchs
Possibility U602
Check Etchs
Check p19 U614 for DIOG
Check Pin 6 U606
Check p5 U606
Goto TT
Check p4 U606
Goto Ss


Check p11 U602 for Presence of $\overline{DBIN}$
Check p2 U602 for $\overline{DBIN}$
Check p1 U602 for $\overline{DBIN}$
Check p29 U600 for $\overline{DBIN}$
Possibility
Check Etch to P11 U602
Possibility U602
Check Etch to p1 U602
Check for $\overline{DBIN}$ p10 U602
Possibility U602
Check for $\overline{DBIN}$ p4 U603
Check Etch to p10 U602

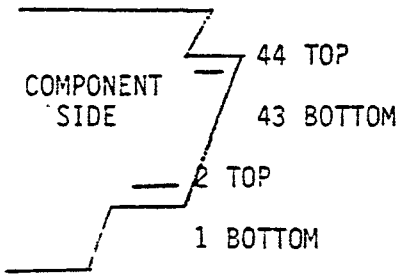

Remove all Groms and Sound Chip for following check
Check p1,2,3 U504 for p1,2 Low P3 Active
Check p22,23, 14 9900 for Signal
Check Etchs
Check Memen p4 U504
Check p3 U605
Check p2 U605
Check p63
Possibility 9900
Check Etchs
Possibility U605
Check Etchs
Check U504 Outputs p11, 15 active p7-15
Check p6, 16 U504 for +5 Pins 5,8 for GND
Check Etchs to Power Supply
Possibility 9900 Sending Bad Address or U504 Bad
Check for 9900 Singals INTREQ CRUIN Address Lines
Goto Page 103
Check p1,2,3, 5 U505 for address lines
Check p19,20, 21 9900 for signals
Check Etchs
Goto Page 102


Check p4 U505 for Active Signals
Check Etch to p11 U504
Check p6 U505 for Active Signal
Check p6 U506 for signal
Check p4 U506 for DBIN
Goto DBIN Check Page 100
Check Etch
Check p5 U506
Check Etch to p1 U505
Possibility U506


Check p7 U505 for 2 Negative Pulses Check p9 for 1 Negative Pulse
Check 6810's using TI BUG if possible, Change 4732's One at a Time, Check for Shorted Address Lines. Go back to page 15
Check p14 U505 for Signal
Probability U505
Memory selection Good


Check p32 9900 for Intreq
Check p11 U300 for Intreq
Check p40 U300 for +5
Find Broken Etch
Check Etch Between p11 U300 and p32 9900
Check p3 U300 for 03 Clock
Check p7 U607
Goto CC Page 87
Check Etch p7 U601 and p3 U300
Check p17 U300 for Intreq
Check for Pull-up R300
Check p18 U300 for Intreq
Check p16 U100 for Intreq
Goto VDP Check Page 88
Check Etch

I/O PORT CONNECTOR

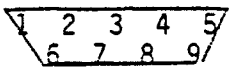


TOP		BOTTOM	
2	SBE	1	+5 V
4	-EXT INT	3	RESET
6	A10	5	A5
8	A11	7	A4
10	A3	9	DBIN *
12	READY	11	A12
14	A8	13	-LOAD
16	A14	15	A13
18	A9	17	A7
20	A2	19	A15
22	-CRU CLOCK	21	GROUND
24	-03 SYSTEM CLOCK	23	
26	-WE	25	
28	-MBE	27	GROUND
30	A1	29	A6
32	-MEMEN	31	A0
34	D7	33	CRU IN
36	D6	35	D4
38	D5	37	D0
40	D1	39	D2
42	D3	41	HOLD / IAQ
44	SOUND IN	43	-5 V

SBE - SPEECH BLOCK ENABLE
MBE - MEMORY BLOCK ENABLE
EXT INT - EXTERNAL INTERUPT
MEMEN - MEMORY ENABLE
DBIN - DATA BUS IN
IAQ - INSTRUCTION AQUISITION

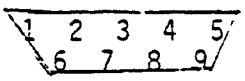
CASSETTE I/O PORT

1 - CASSETTE 1 MOTOR CONTROL
2 - CASSETTE 1 MOTOR CONTROL
3 - MAG OUT RETURN (GROUND)
4 - CASSETTE AUDIO INPUT
5 - MAG OUT
6 - CASSETTE 2 MOTOR CONTROL
7 - CASSETTE 2 MOTOR CONTROL
8 - MAG IN
9 - MAG IN RETURN (GROUND)



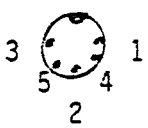
JOYSTICK I/O

1 -
2 - JOYSTICK B
3 - UP
4 - PUSH BUTTON
5 - LEFT
6 -
7 - JOYSTICK A
8 - DOWN
9 - RIGHT



VIDEO I/O

1 - +12 VOLTS
2 - GROUND
3 - AUDIO OUT
4 - COMPOSITE VIDEO OUT
5 - GROUND

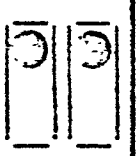
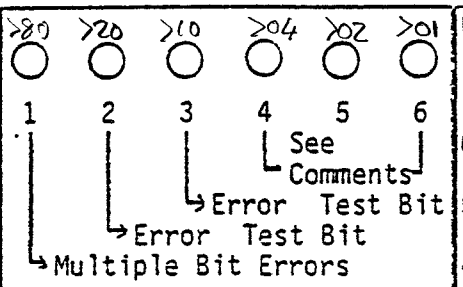
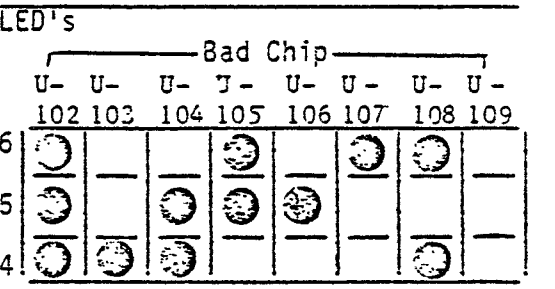
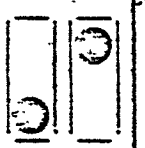
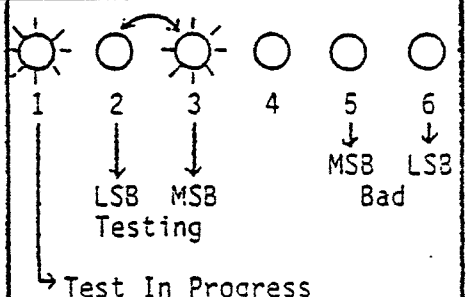
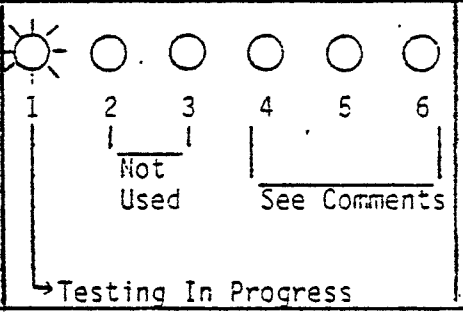
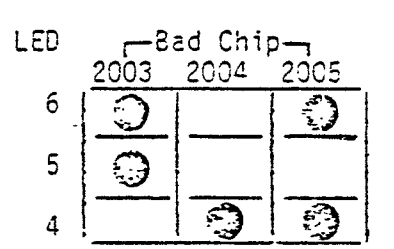


GROM PORT CONNECTOR

GROUND	35	36	GROUND (VPP)
GROM VSS	33	34	-ROM G
GROM READY	31	32	-WE
-5 V	29	30	A4
GROM CLOCK	27	28	A5
DBIN	25	26	A6
A14	23	24	A3
GROM SELECT	21	22	A7
+5 V	19	20	A8
D0	17	18	A9
D1	15	16	A10
D2	13	14	A11
D3	11	12	A12
D4	9	10	A13
D5	7	8	A15/CRU OUT
D6	5	6	CRU IN
D7	3	4	-CRU CLOCK
RESET	1	2	GROUND

—FRONT→

RAM TRAP OPERATING INSTRUCTIONS

TEST FUNCTION	Switch Position	INDICATORS	COMMENTS
4116's U102-U109			
6810's U608, U609			2nd & 3rd Indicators should alternate SLOWLY. 5th Indicator shows MSB ERROR. 6th Indicator shows LSB ERROR.
2003 2004 2005			

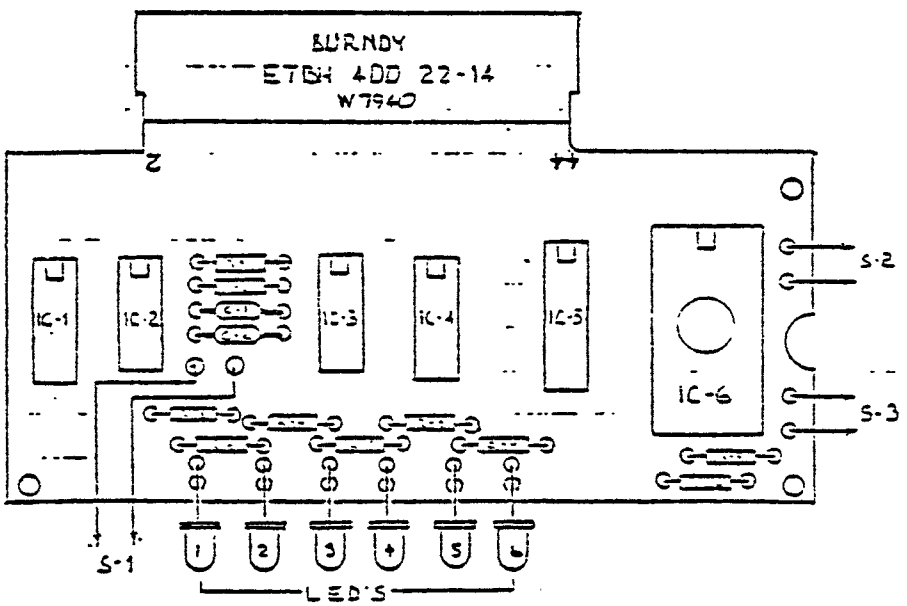
BEFORE EACH TEST MAKE SURE THE UNIT UNDER TEST IS SWITCHED "OFF".

START UP PROCEDURE:

1. Turn Unit To Be Tested "Off"
2. Insert RAM Trap
3. Select Test Mode On Ram Trap
4. Turn "On" Unit To Be Tested
5. Press LOAD Switch

MAINFRAME RAM-TRAP

COMPONENT LAYOUT :

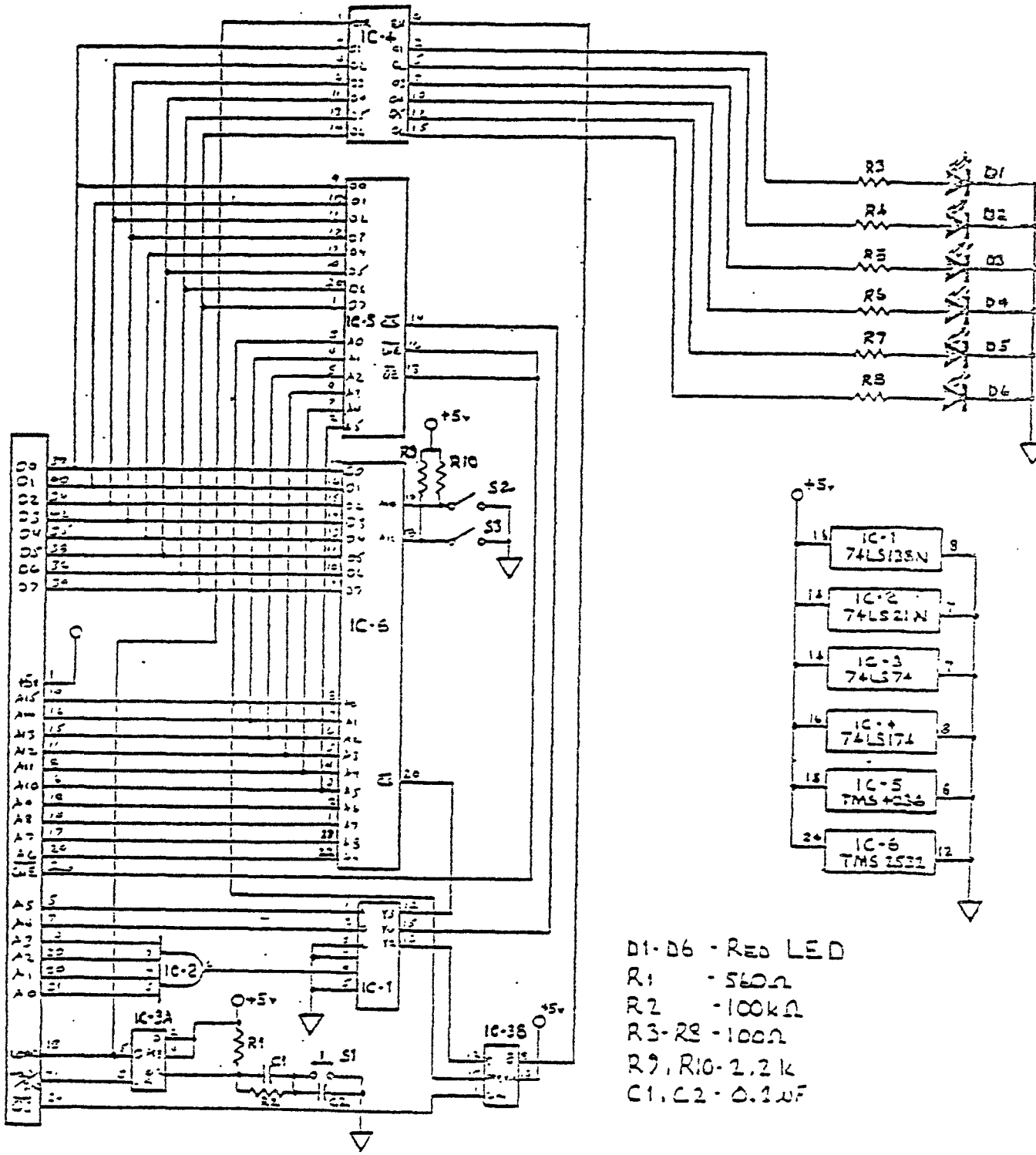


PARTS LIST :

C-1, C-2	0.1 µF CAPACITORS	R-1	560 Ω	ALL RESISTORS ARE ¼ WATT 5%
IC-1	74LS138N	R-2	100 kΩ	
IC-2	74LS21N	R-3 – R-8	100 Ω	
IC-3	74LS74AN	R-9, R-10	2.2 kΩ	
IC-4	74LS174N	S-1	SPST PUSHBUTTON SWITCH (MOMENTARY N.C.)	
IC-5	TMS 4036-2NL	S-2, S-3	SPST TOGGLE SWITCHES	
IC-6	2532 (EPROM)			

BY: [illegible] 3.4.80

RAM TRAP SCHEMATIC



D1-D6 - RED LED
R1 - 560Ω
R2 - 100kΩ
R3-R8 - 100Ω
R9, R10 - 2.2k
C1, C2 - 0.1uF

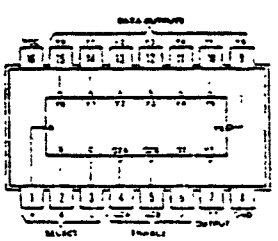
BY: [redacted] 3-26-80

LS138

- 3 TO 8 LINE DECODER/MULTIPLIER
- 2 STATE OUPUT: 1) HIGH
  2) LOW
- 3 ENABLES, $\overline{G2A}$ & $\overline{G2B}$ - ACTIVE LOW, G1 - ACTIVE HIGH
- ENABLES CAN BE USED AS INVERTING OR NON-INVERTING INPUT TO MULTIPLEX DATA

3-TO-8 LINE DECODERS/MULTIPLEXERS

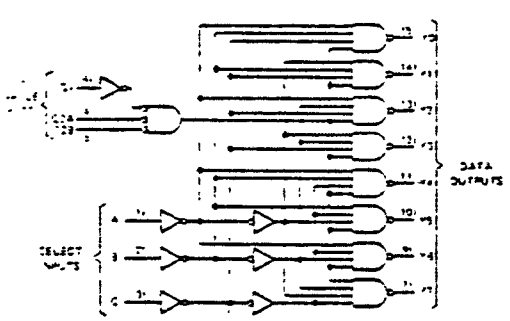
138



*See page 7-134

SN54LS138 (J, W) SN74LS138 (J, N)
SN54S138 (J, W) SN74S138 (J, N)

*LS138, *S138



*LS138, *S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = high level, L = low level, X = irrelevant

Fig. 31

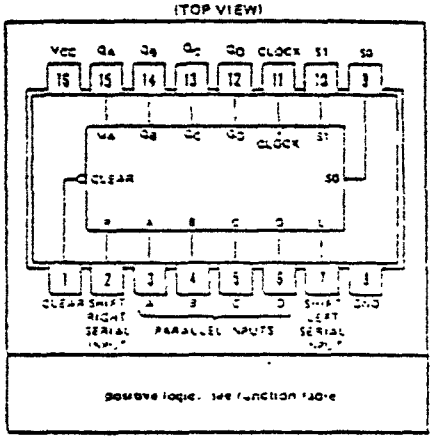
RAG 06-0 3-82

- 4 BIT BI-DIRECTIONAL SHIFT REGISTER
- POSITIVE EDGE TRIGGERING (↑)
- 4 MODES OF OPERATION: (A) PARALLEL LOAD
  (B) SHIFT RIGHT (QA TO QD)
  (C) SHIFT LEFT (QD TO QA)
  (D) INHIBIT CLOCK (DO NOTHING)

- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'194	36 MHz	195 mW
LS194A	36 MHz	75 mW
'S194	105 MHz	425 mW

SN74194, SN74LS194A, SN74S194 ... J OR N PACKAGE
(TOP VIEW)



description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the SN54194, SN74194 should be changed only while the clock input is high.

FUNCTION TABLE

INPUTS									OUTPUTS			
CLEAR	MODE S1	MODE S0	CLOCK	SERIAL LEFT	SERIAL RIGHT	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most recent ↑ transition of the clock

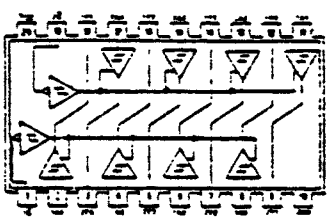
Fig. 32

PAG 06-05-82

- 'OCTAL (8) BUS DRIVER'
- 'NON-INVERTING'
- '1-WAY COMMUNICATION'
- '3 STATE OUTPUT': 1) HIGH
  2) LOW
  3) HIGH IMPEDANCE
- $\overline{G}$ IS ENABLE ACTIVE - LOW

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

244 NONINVERTED 3-STATE OUTPUTS



See page 6-43

SN54LS244 (J) SN74LS244 (J, N)

- INPUT/OUTPUT/ENABLE

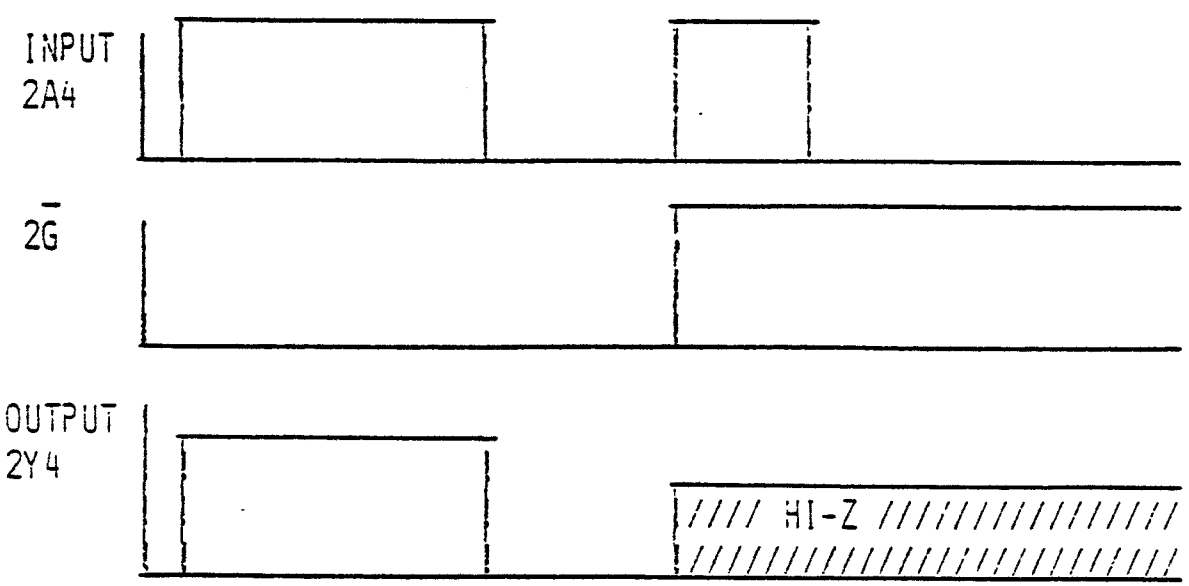
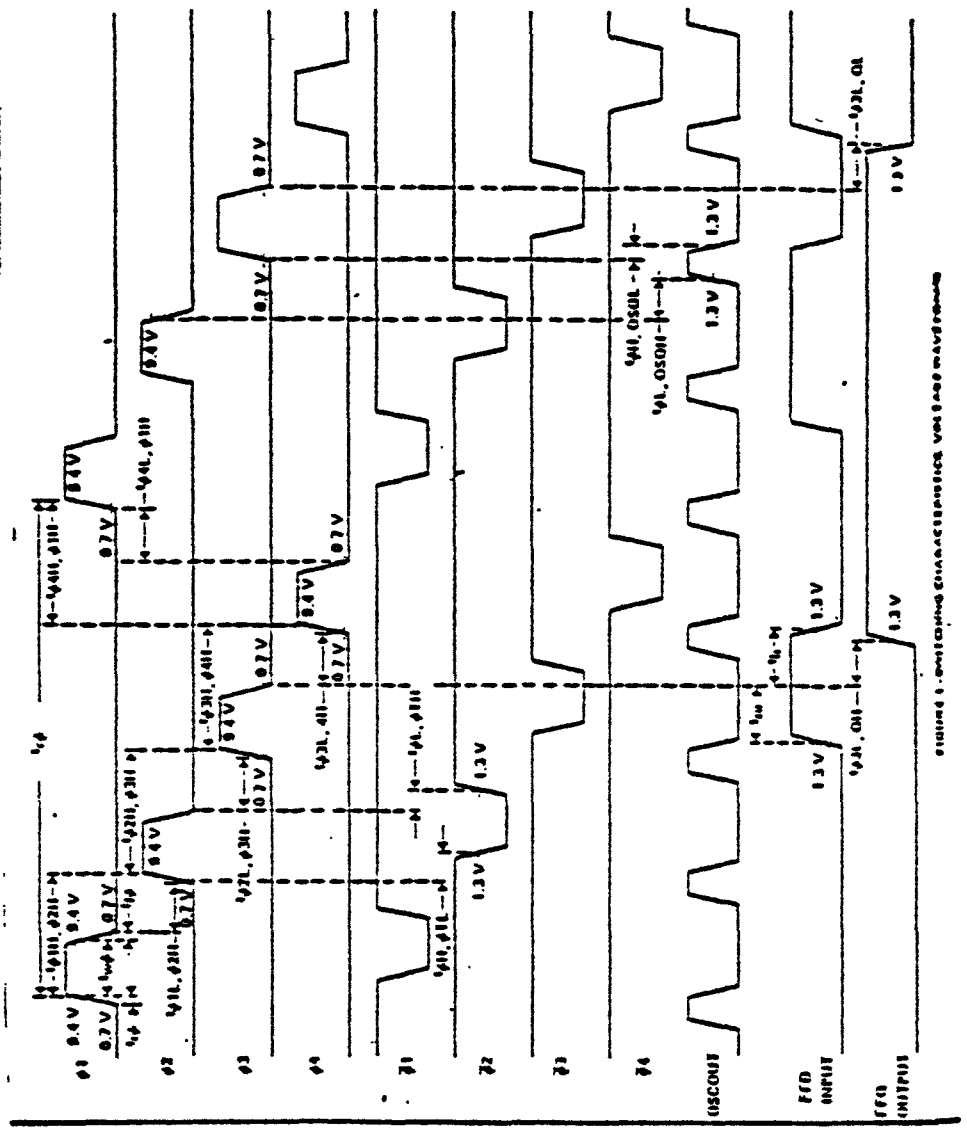


Fig. 33

PARAMETER MEASUREMENT INFORMATION



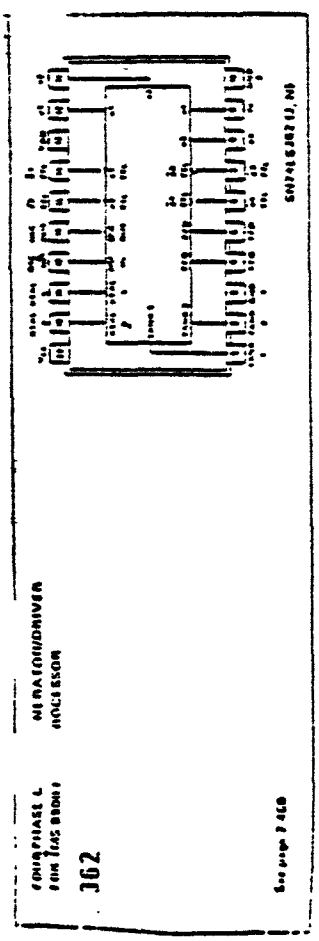
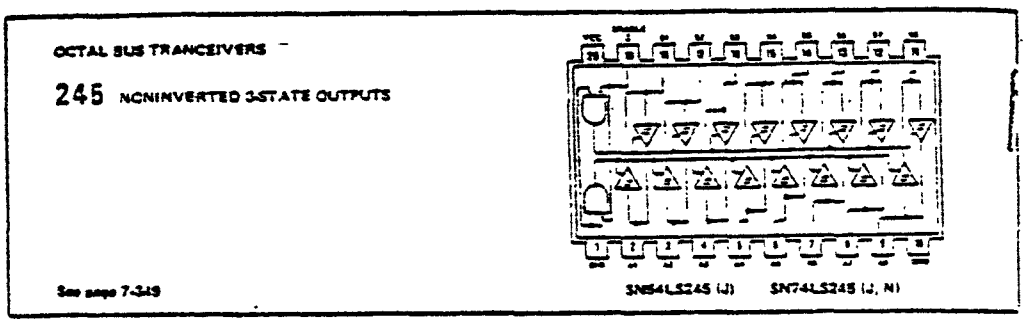
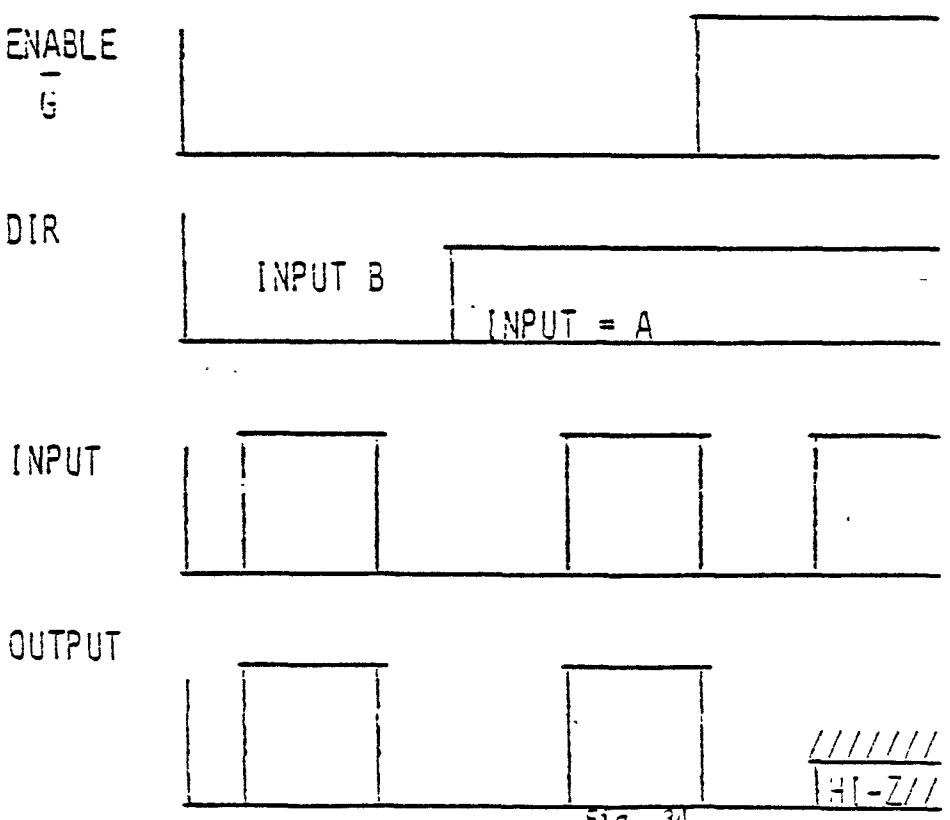


Fig. 35

LS245

- OCTAL (8) BUS DRIVER'
- 'NON-INVERTING '
- '2-WAY COMMUNICATION'
- '3-STATE OUTPUT' 1) HIGH
  2) LOW
  3) HIGH IMPEDANCE
- $\overline{G}$ IS ENABLE..ACTIVE LOW
- DIR IS DIRECTION CONTROL A→B...B→A





$\overline{G}$	DIR	OPERATION
0	0	B DATA TO
0	1	A DATA TO
1	X	ISOLATION (HI-Z)

X = DON'T CARE WHAT STA

Fig. 34

A=OUTPUT B=OUTPUT

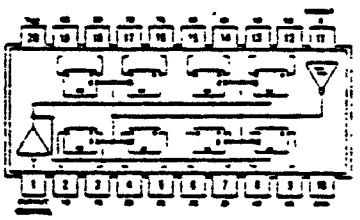
RAG JG-03-3

LS 373

- OCTAL (8) D-TYPE LATCHES
- 3 STATE OUPUT: 1) HIGH
  2) LOW
  3) HIGH IMPEDANCE
- WHEN G (ENABLE) IS HIGH, THEN Q (INPUT) WILL FOLLOW D (INPUT)
- WHEN G (ENABLE) IS LOW, THEN Q (OUTPUT) WILL LATCH D (INPUT)

OCTAL D-TYPE LATCHES

373 3-STATE OUTPUTS
COMMON OUTPUT CONTROL
COMMON ENABLE



SN54LS373 (J) SN74LS373 (J, N)
SN54S373 (J) SN74S373 (J, N)

See page 7-471

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	HI = Z

Q_0 = DATA PRESENT AT INPUT WHEN ENABLE WENT LOW

X = DON'T CARE

Fig. 37

4116 DYNAMIC RAM

- 16,384 X 1 ORGANIZATION

- 3 STATE OUTPUTS

A0 - A6 - ADDRESS INPUTS

$\overline{CAS}$ - COLUMN ADDRESS STROBE
D - DATA INPUT
Q - DATA OUTPUT
$\overline{RAS}$ - ROW ADDRESS STROBE
$\overline{W}$ - WRITE ENABLE

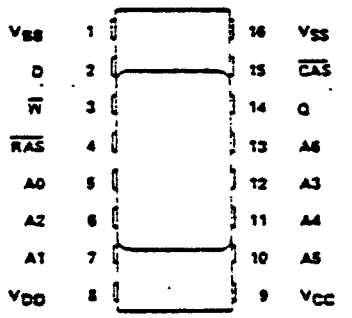
- REFRESH MUST BE PERFORMED EVERY 2 MILLISECONDS

- $\overline{RAS}$ LATCHES THE ROW ADDRESS (A0 - A6)

- $\overline{CAS}$ LATCHES THE COLUMN ADDRESS (A0 - A6)

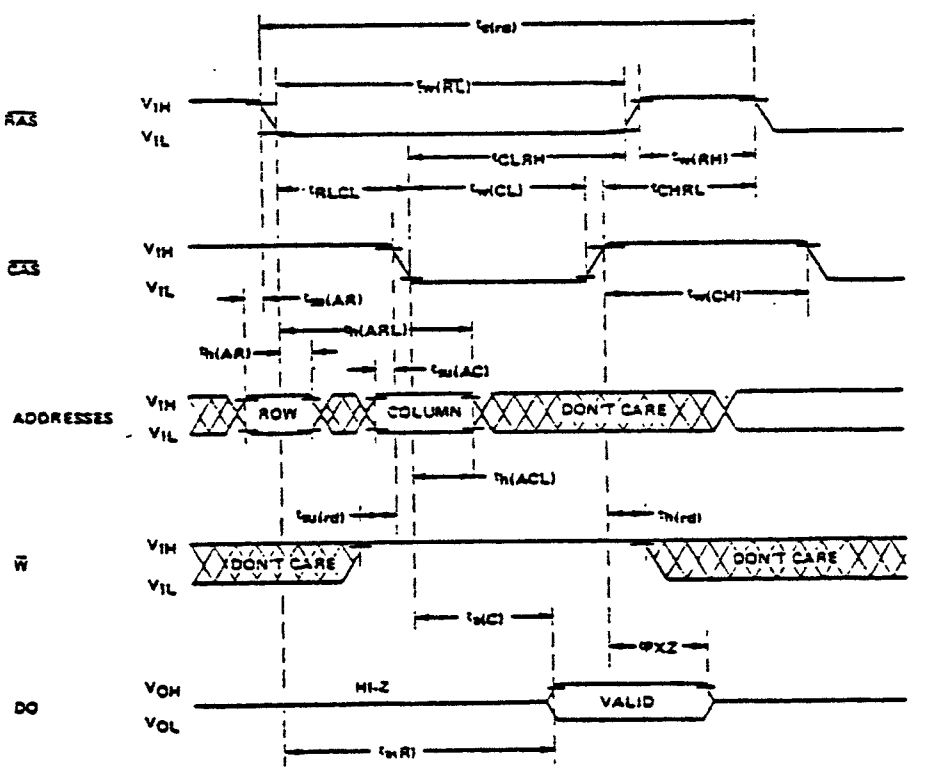
A0	A1	A2	A3	A4	A5	A6	A0	A1	A2	A3	A4	A5	A6
8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
			$\overline{CAS}$							$\overline{RAS}$			

16-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



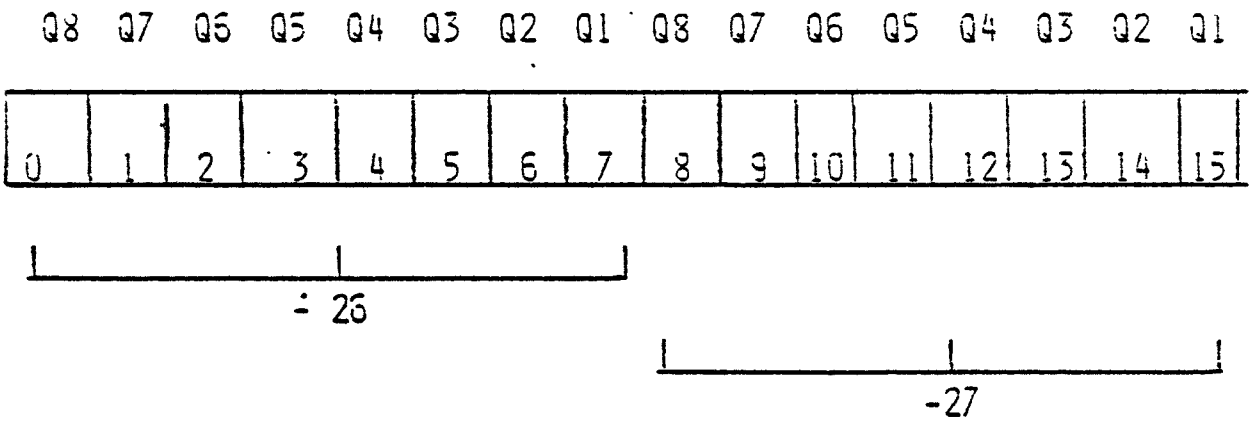
PIN NOMENCLATURE			
A0-A6	Address inputs	$\overline{W}$	Write Enable
$\overline{CAS}$	Column address strobe	V_{BB}	−5-V power supply
D	Data input	V_{CC}	+5-V power supply
Q	Data output	V_{DD}	+12-V power supply
$\overline{RAS}$	Row address strobe	V_{SS}	0 V ground

read cycle timing



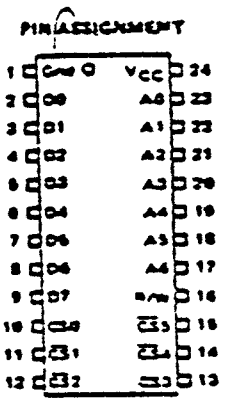
MF 4732 ROMS

- 4096 X 8 BIT MEMORY SIZE
- +5, GND ONLY
- 8 BIT TRI-STATE DATA OUTPUTS (Q1-Q8)
  Q8 = MSB
  Q1 = LSB
- 12 ADDRESS LINES (A0-A11)
  A11 = MSB
  A0 = LSB
- CHIP IS ENABLED WHEN $\overline{CS1}$ AND $\overline{CS2}$ ARE BOTH LOW
- ONLY DURING THE ENABLE ARE THE OUTPUTS ENABLED, ALL OTHER CASES THE OUTPUTS ARE TRI-STATED.



6810 RAM

- 128 X 8 STATIC RAM
- USED AS SCRATCH PAD (CPU RAM)
- TWO DEVICES ARE USED TO MAKE A 128 X 16 MEMORY AREA
- + 5, GND ONLY

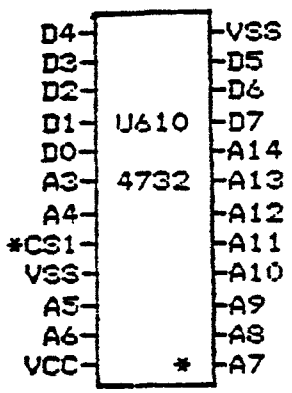


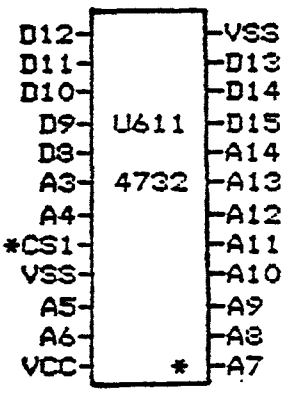
D0 - D7 = DATA I/O
A0 - A6 = ADDRESS LINES
R/W = HIGH IS READ, LOW IS $\overline{\text{WRITE}}$

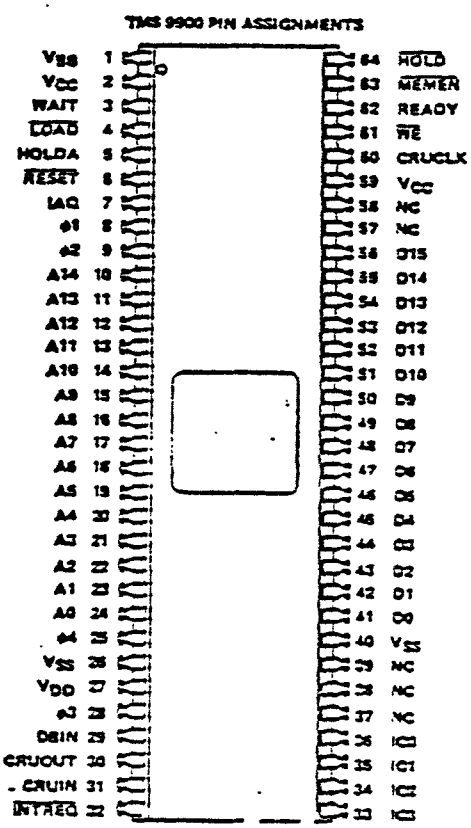
TO BE ENABLED: CS0 & CS3 MUST BE HIGH

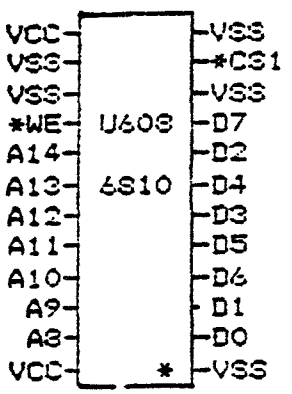
$\overline{\text{CS1}}, \overline{\text{CS2}}, \overline{\text{CS4}}$, & $\overline{\text{CS5}}$ MUST BE LOW

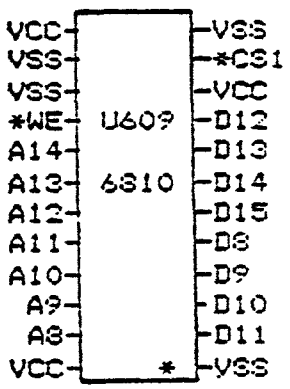
Fig. 39

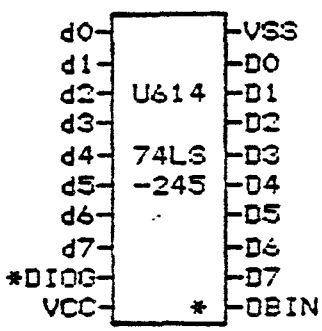


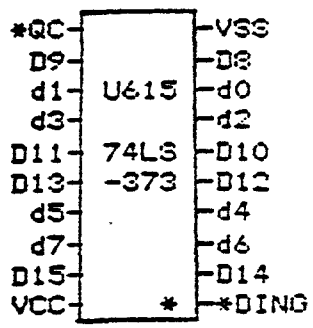


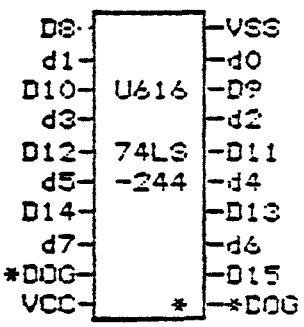






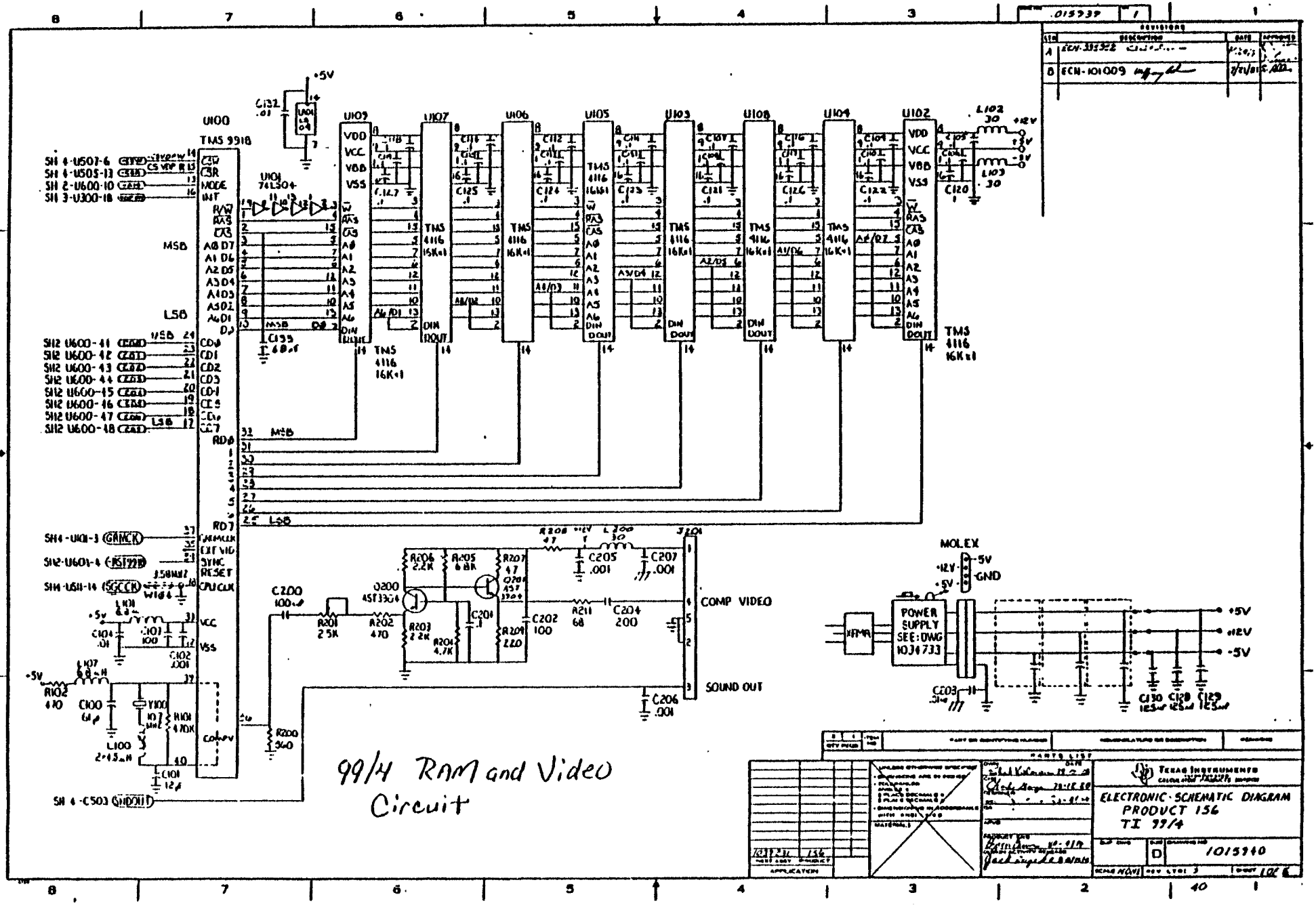




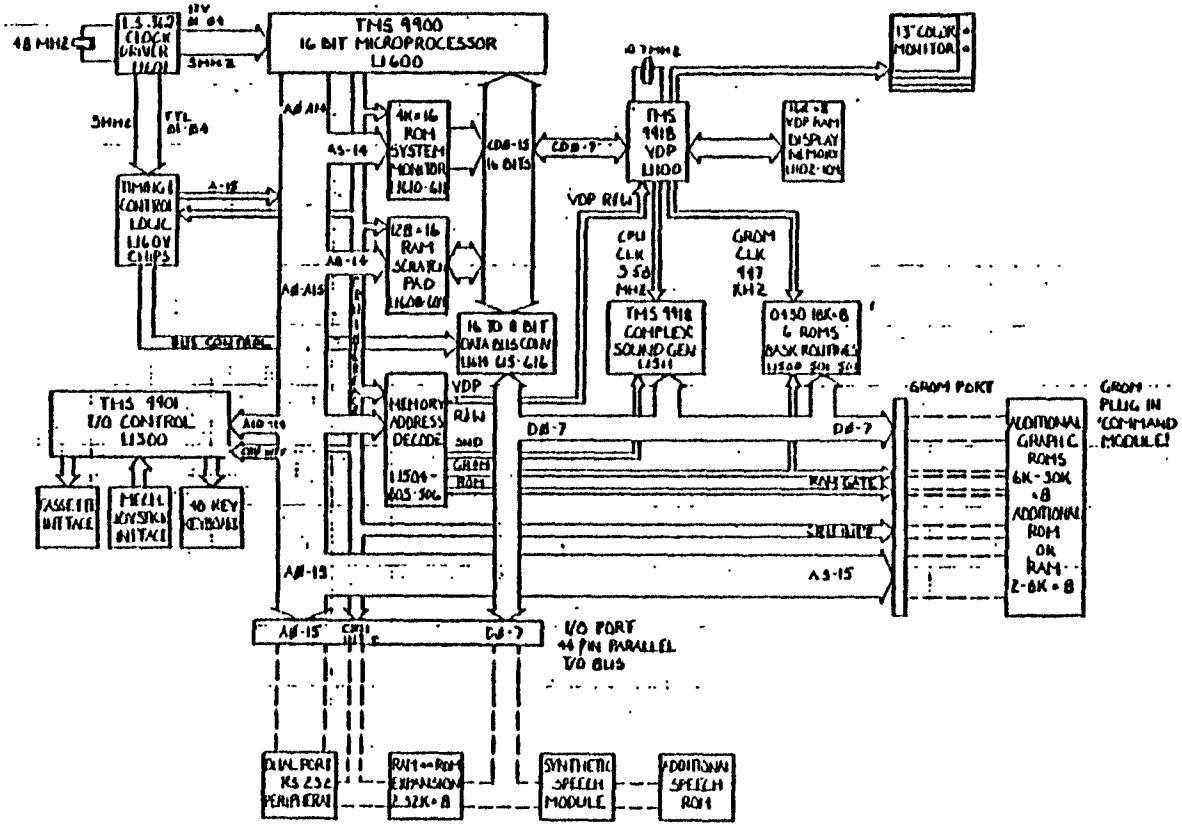


D denotes 16 bit data bus
d denotes 8 bit multiplexed data bus

Fig. 40 .



.015939
REVISIONS
A ECN-335952
B ECN-101009
U100
TMS 9918
U101
74LS04
U109
U107
U106
U105
U103
U108
U104
U102
TMS 4116 16K×1
MSB
LSB
SH 4-U507-6
SH 4-U505-13
SH 2-U600-10
SH 3-U300-18
SH2 U600-41
SH2 U600-42
SH2 U600-43
SH2 U600-44
SH2 U600-45
SH2 U600-46
SH2 U600-47
SH2 U600-48
SH4-U101-3 (GRMCK)
SH2-U601-4 (RST99B)
SH4-U511-14 (SGCCK)
SH 4-C503 (SHDOUT)
Q200 AST3904
COMP VIDEO
SOUND OUT
MOLEX
POWER SUPPLY SEE: DWG 1034733
XFMR
+5V
+12V
-5V
GND
99/4 RAM and Video Circuit
TEXAS INSTRUMENTS
ELECTRONIC SCHEMATIC DIAGRAM
PRODUCT 156
TI 99/4
D
1015940



99/4 SYSTEM BLOCK DIAGRAM

Fig. 43

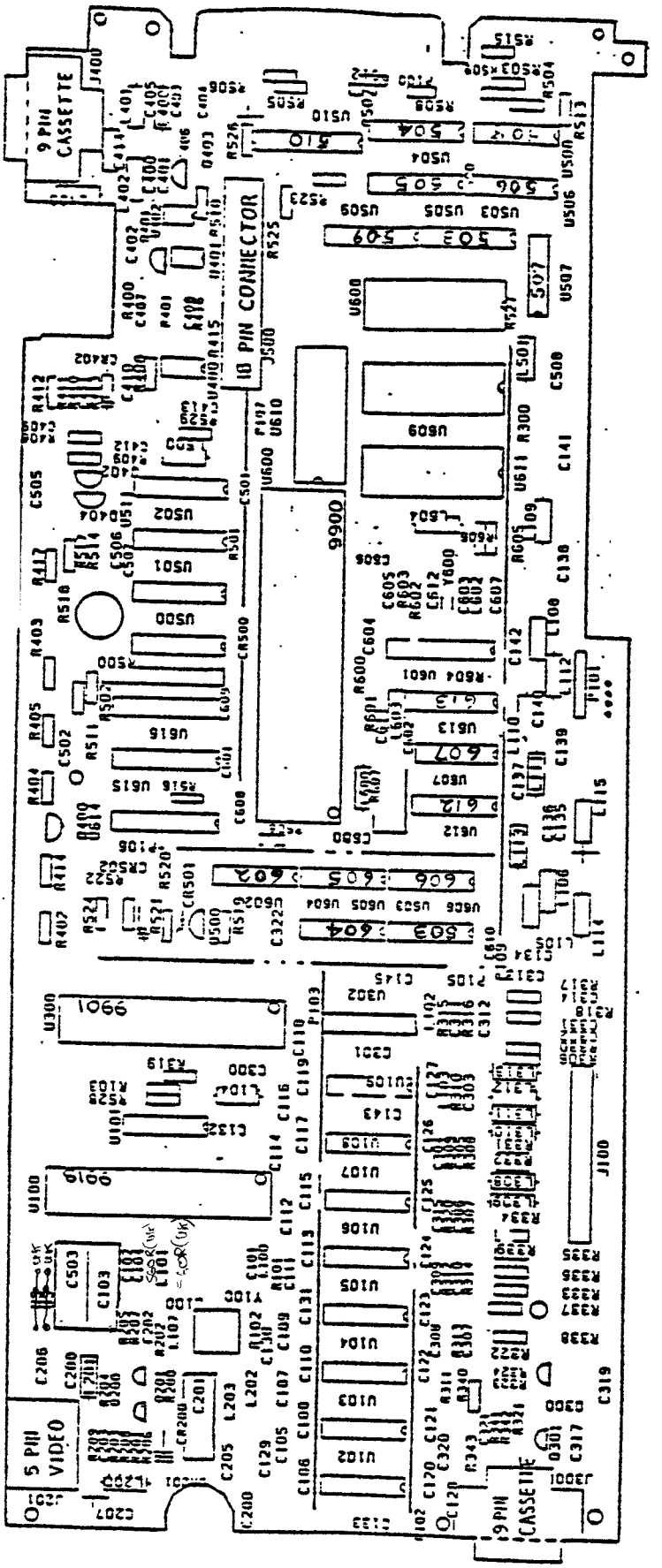

NP 1039026 REV A
MARKING
9 PIN CASSETTE
10 PIN CONNECTOR
5 PIN VIDEO
9 PIN CASSETTE

Fig. 41

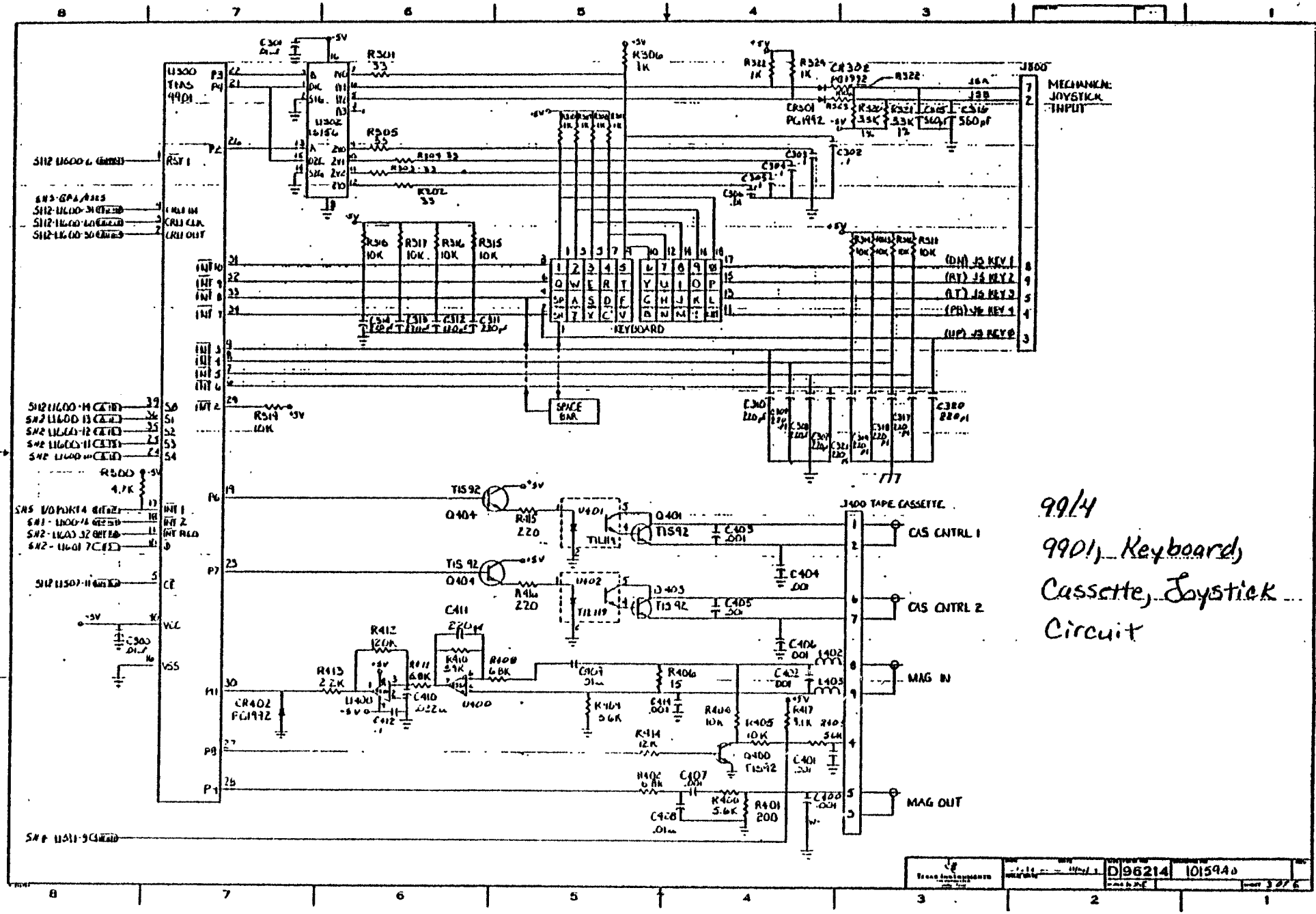
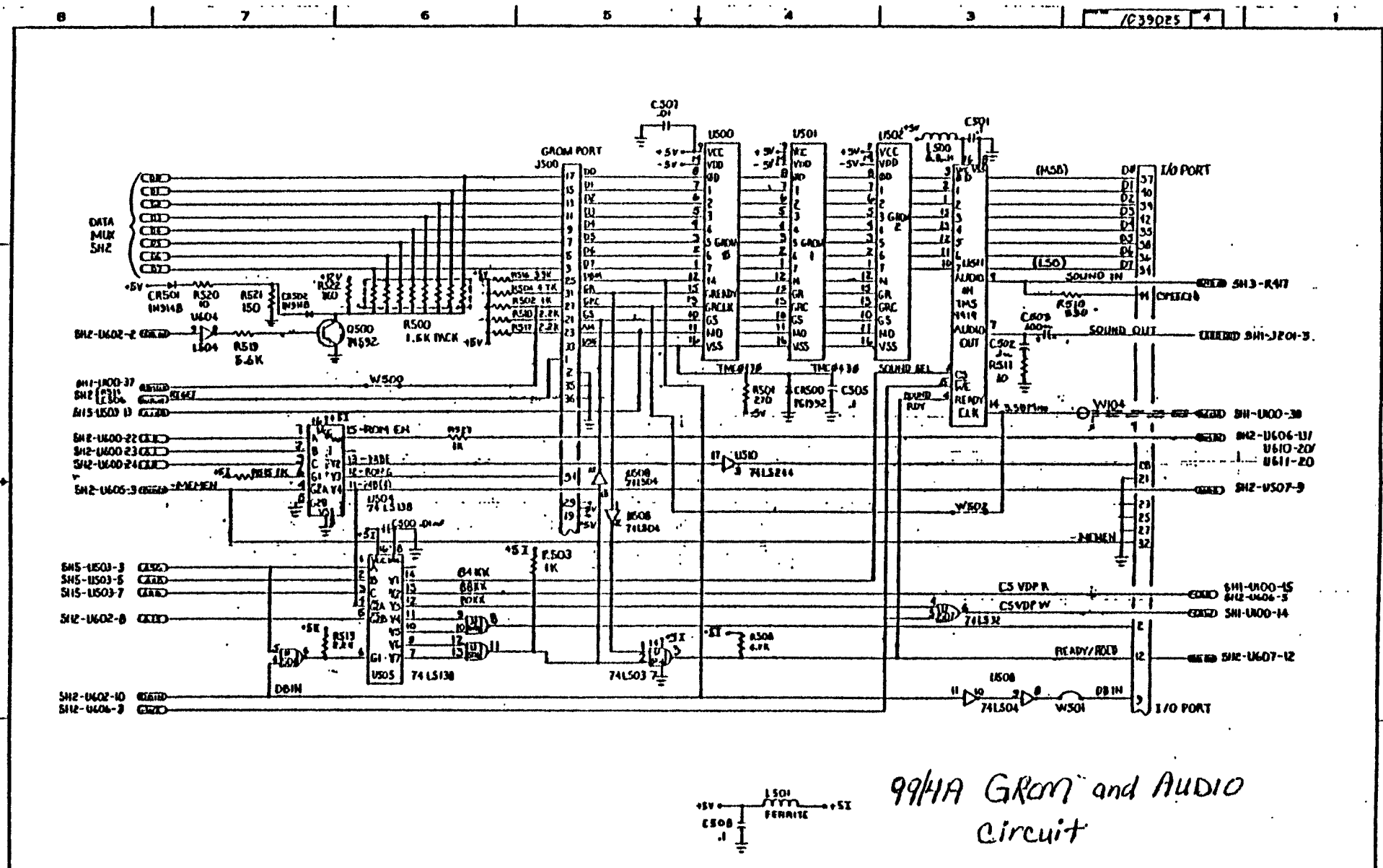

U300 TMS 9901
KEYBOARD
SPACE BAR
J800
MECHANICAL JOYSTICK INPUT
J400 TAPE CASSETTE
CAS CNTRL 1
CAS CNTRL 2
MAG IN
MAG OUT
99/4
9901, Keyboard, Cassette, Joystick ... Circuit

Fig. 47


1039025
GROM PORT
J500
DATA MUX SH2
I/O PORT
J501
SOUND IN
SOUND OUT
SH3-R4T
SH-J201-3
SH-U00-38
SH2-U606-13
U610-20
U611-20
SH2-U607-9
SH1-U00-15
SH2-U606-5
SH1-U00-14
SH2-U607-12
SH2-U602-2
SH2-U602-10
SH2-U606-9
SH5-U503-3
SH5-U503-5
SH5-U503-7
SH2-U602-8
SH1-J100-37
SH2
SH15-U501 D
SH2-U600-22
SH2-U600-23
SH2-U600-24
SH2-U606-3
W500
W501
W502
W503
W504
W505
W506
W507
W508
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U531
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U536
U537
U538
U539

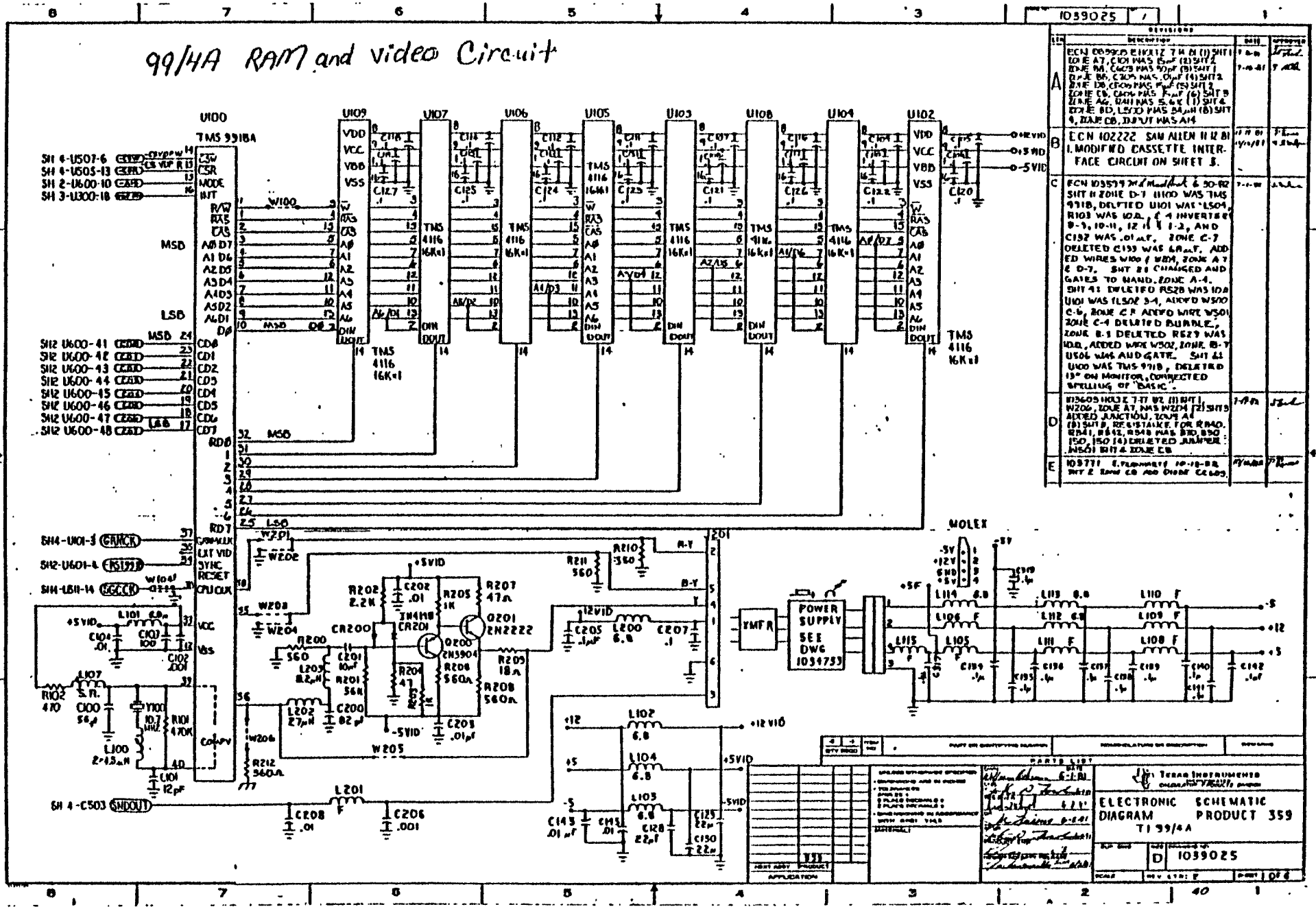
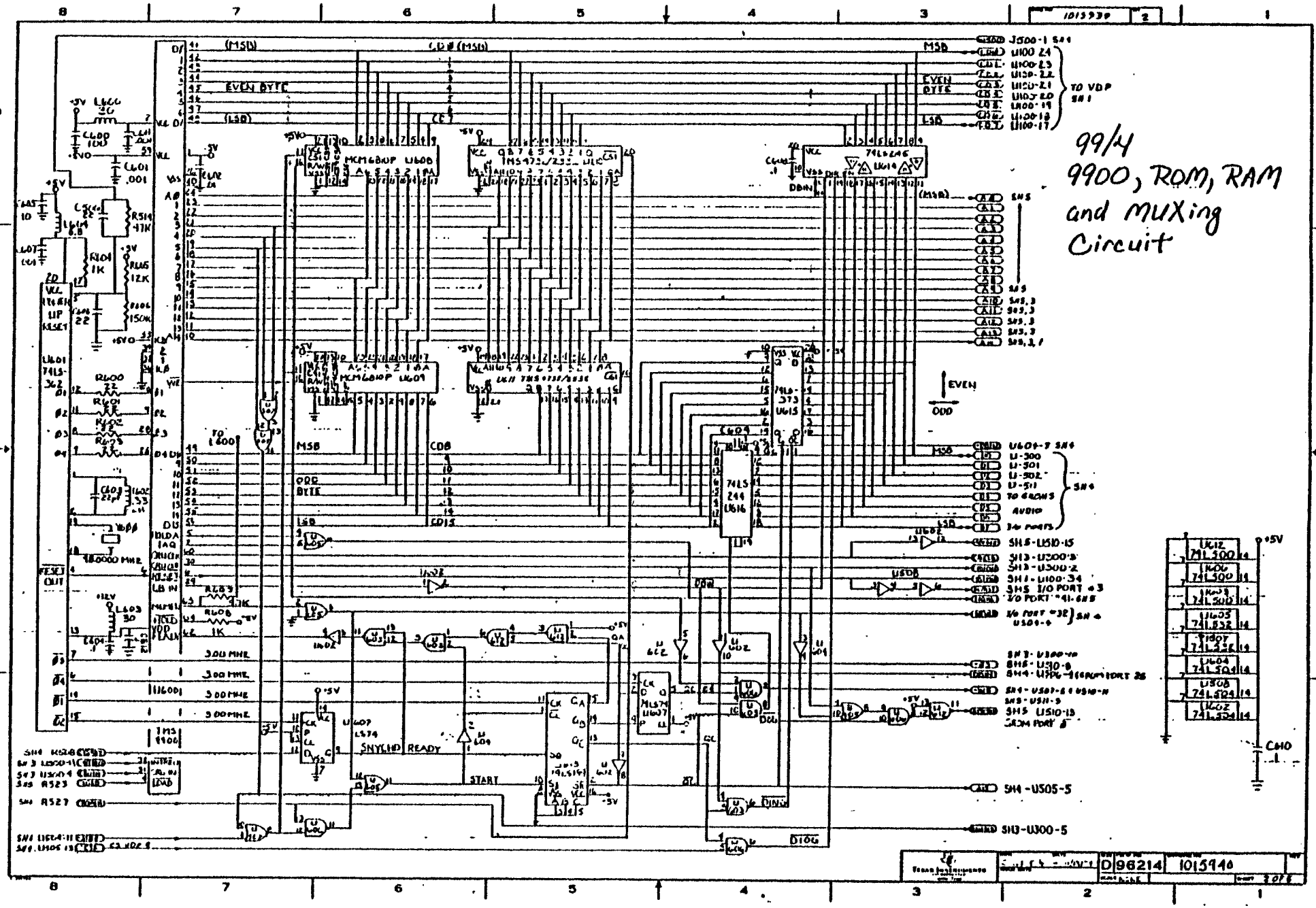
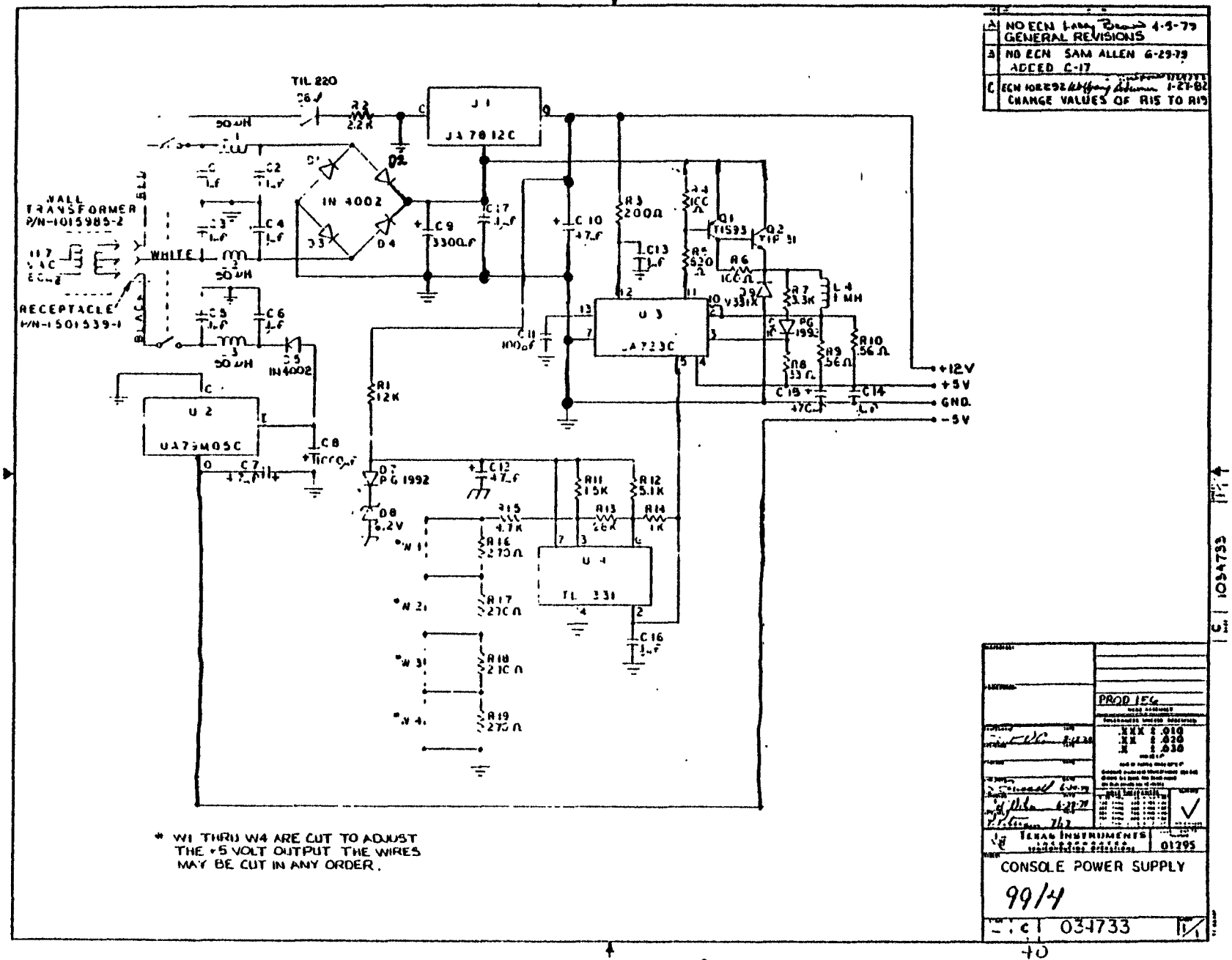

99/4A RAM and video Circuit
U100
TMS 9918A
U109
U107
U106
U105
U103
U108
U104
U102
TMS 4116 16K×1
MSB
LSB
W100
W201
W202
W203
W204
W205
W206
W207
W208
+5VID
+12VID
-5VID
+12 VID
-5 VID
POWER SUPPLY SEE DWG 1039753
YMTR
MOLEX
ECN 103599 SAN ANTONIO 7-11-82 (1) SHT 1 ZONE A7, C101 WAS 5pF (2) SHT 2 ZONE A4, C103 WAS 10pF (3) SHT 2 ZONE B8, C105 WAS .01μF (4) SHT 2 ZONE D8 (ECN MAC 8-6-82) (5) SHT 3 ZONE C6, C104 WAS 5pF (6) SHT 3 ZONE A6, R101 WAS 5.6K (7) SHT 4 ZONE B8, L200 WAS 56μH (8) SHT 4, ZONE C8, D3 PUT WAS A14
B ECN 102222 SAN ALLEN 11-12-81 MODIFIED CASSETTE INTERFACE CIRCUIT ON SHEET 3.
C ECN 103599 7-7-82 & 10-82 SHT 1 ZONE D-7 U100 WAS TMS 9918, DELETED U101 WAS LS04, R103 WAS 10Ω, 4 INVERTER B-9, 10-11, 12-13 & 1-2, AND C132 WAS .01μF, ZONE C-7 DELETED C133 WAS 68pF, ADDED WIRES W100 & W104, ZONE A-7 & D-7, SHT 2B CHANGED AND GATES TO NAND, ZONE A-4, SHT 4A DELETED R528 WAS 10Ω U101 WAS LS08 3-4, ADDED W500 C-6, ZONE C-8 ADDED WIRE W501 ZONE C-4 DELETED BUBBLE, ZONE B-1 DELETED R527 WAS 10Ω, ADDED WIRE W502, ZONE B-7 U506 WAS AND GATE. SHT 4A U100 WAS TMS 9918, DELETED 13" ON MONITOR, CORRECTED SPELLING OF "BASIC".
D 103605 HOUSTON 7-11-82 (1) SHT 1 W206, ZONE A7, WAS W204 (2) SHT 3 ADDED JUNCTION, ZONE A6 (3) SHT 3, RESISTANCE FOR R840, R841, R842, R843 WAS 330, 390, 150, 150 (4) DELETED JUMPER W501 SHT 4 ZONE C8
E 103771 (PRELIMINARY 10-18-82) SHT 2 ZONE C8 ADD DIODE CR209
PARTS LIST
Texas Instruments
ELECTRONIC SCHEMATIC DIAGRAM PRODUCT 359 TI 99/4A
D 1039025

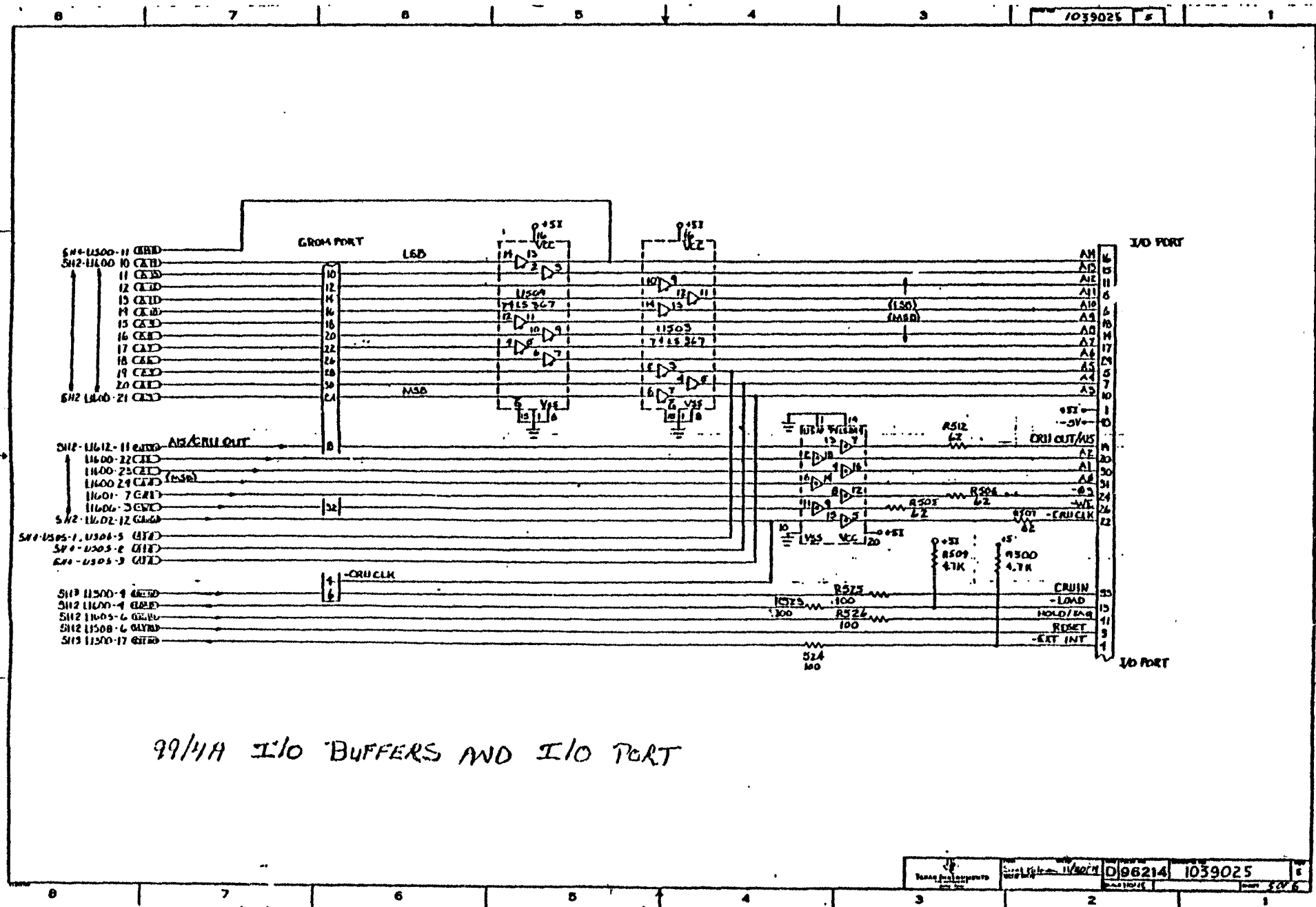
Fig. 5-3


99/4
9900, ROM, RAM
and MUXing
Circuit
EVEN BYTE
ODD BYTE
MSB
LSB
EVEN
ODD
TO VDP
SN1
SN3
SN4
SN5
SN6
SN7
SN8
SN9
SN10
SN11
SN12
SN13
SN14
SN15
SN16
SN17
SN18
SN19
SN20
SN21
SN22
SN23
SN24
SN25
SN26
SN27
SN28
SN29
SN30
SN31
SN32
SN33
SN34
SN35
SN36
SN37
SN38
SN39
SN40
SN41
SN42



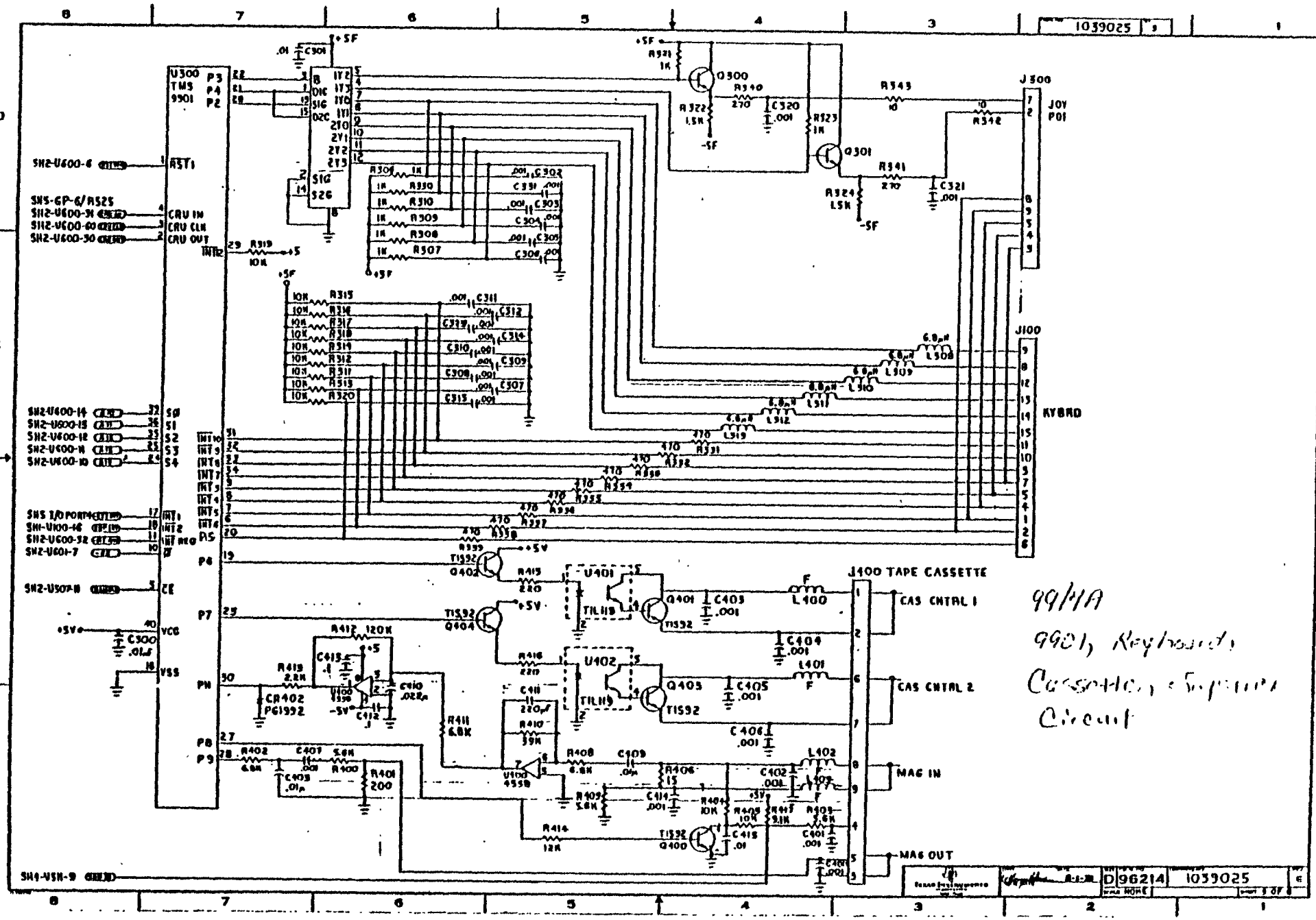
NO ECN 4-5-79
GENERAL REVISIONS
NO ECN SAM ALLEN 6-29-79
ADDED C-17
ECN 1-27-82
CHANGE VALUES OF R15 TO R19
TIL 220
J1
JA 7812C
IN 4002
WALL TRANSFORMER P/N-1015985-2
RECEPTACLE P/N-1501539-1
WHITE
BLACK
U2
UA79M05C
U3
UA723C
U4
TL 331
+12V
+5V
GND.
-5V
* W1 THRU W4 ARE CUT TO ADJUST THE +5 VOLT OUTPUT THE WIRES MAY BE CUT IN ANY ORDER.
PROD 156
TEXAS INSTRUMENTS
01295
CONSOLE POWER SUPPLY
99/4
034733

Fig. 49



99/4A I/O BUFFERS AND I/O PORT

Fig. 55



99/4A
9901, Keyboard,
Cassette, Supervisor
Circuit

Fig. 54

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