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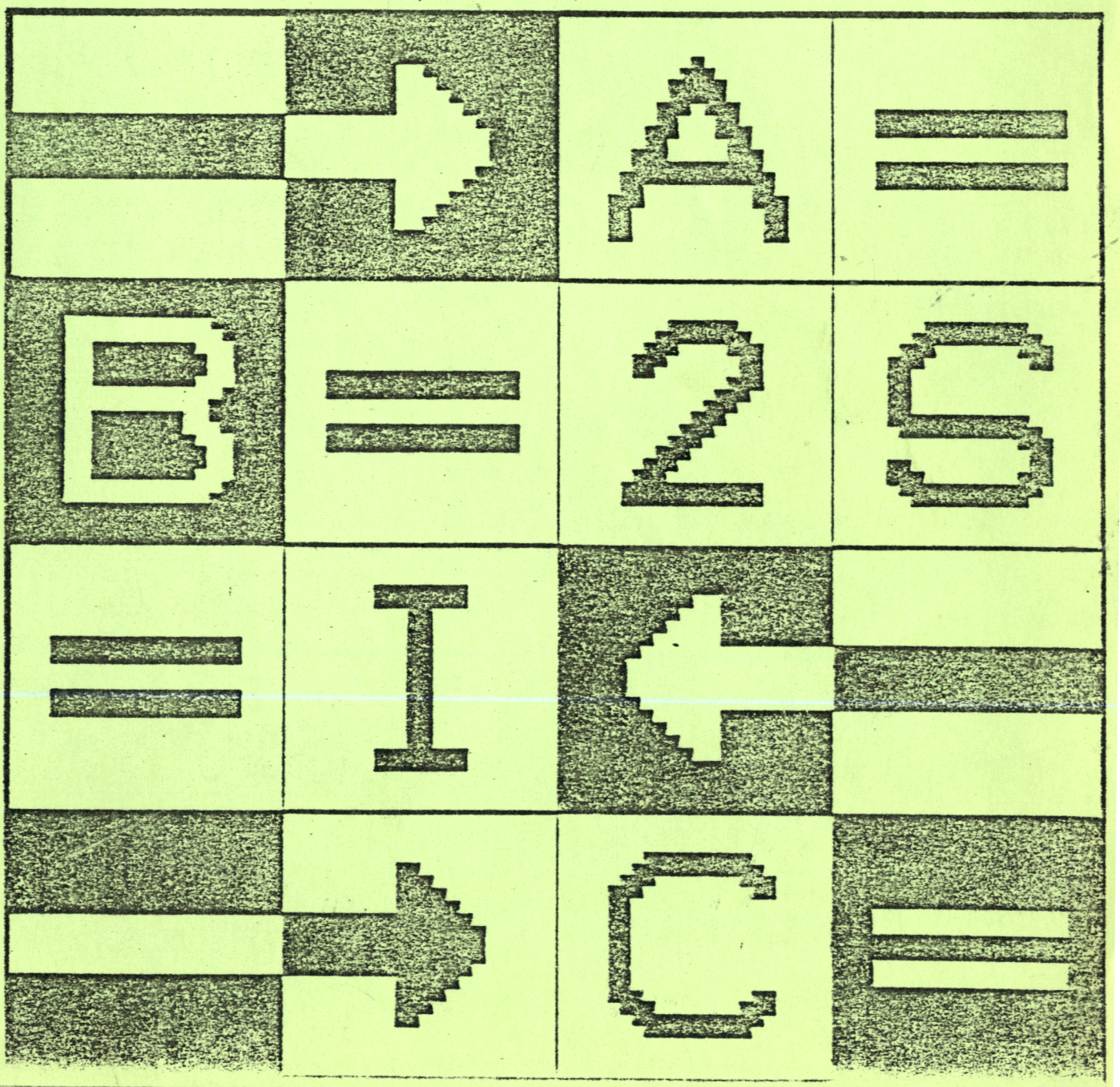
It is my hope that you find the file of use to you personally – I know that I would have liked to have found some of these files years ago – they would have saved me a lot of time !

Colin Hinson
In the village of Blunham, Bedfordshire.

TEXAS INSTRUMENTS HOME COMPUTER

Technical Data



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LIST OF ILLUSTRATIONS

GENERAL DESCRIPTION

The concept for the Texas Instruments Home Computer 99/4 or 99/4A I/O bus is to provide maximum flexibility and good performance with a constraint of low cost for both mainframe and computer system. This concept is achieved by providing both memory and CRU I/O buses to the 99/4 or 99/4A peripherals. This brief description will give key details of this interface. Detailed information regarding the 9900 CRU is assumed. A source for this information is the 9900 Family Systems Design and Data Book. This manual may be obtained from TI Semiconductor Distributors. The memory bus (with data bus converted to eight bits wide) is used for instruction fetch from ROM in external peripherals and for data transfer to/from memory mapped portions of these devices. The CRU bus is used for peripheral enable/disable and for device control and data transfer to/from CRU mapped peripherals.

A block diagram of the TI-99/4A electronics is shown in Figure A. The TMS 9900 microprocessor accesses each peripheral to obtain instructions from the device service routine (DSR) read only memory (ROM). Since each peripheral contains its own DSR, the 99/4A does not have to be designed to anticipate future peripheral requirements. The dual I/O bus capability, along with interrupt handling and external DSR's provide flexibility at low cost.

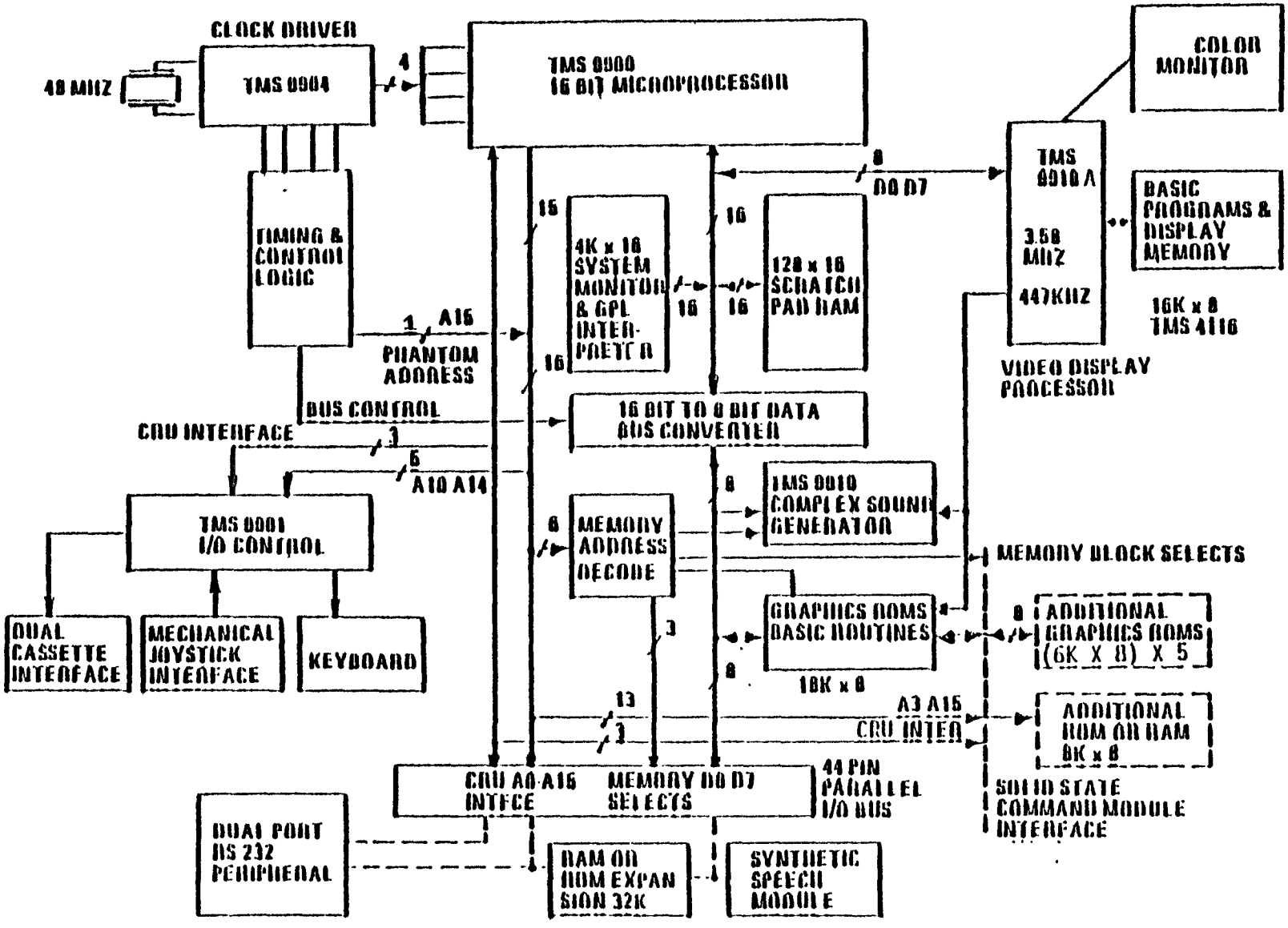


FIGURE A

SYSTEM BLOCK DIAGRAM

I. I/O DESCRIPTION

SIGNATURE	PIN	I/O	DESCRIPTION
A0 (MSB)	31	Out	
A1	30	Out	ADDRESS BUS
A2	20	Out	A0 through A15 comprise the
	10	Out	address bus. This bus provides
A4	7	Out	the 16 bit memory address vector
A5	5	Out	to the external memory system when
A6	29	Out	MEMEN is active. Address bit 15
A7	17	Out	is also used for CRU DATA OUT on
A8	14	Out	CRU output instructions.
A9	18	Out	
A10	6	Out	
A11	8	Out	
A12	11	Out	
A13	15	Out	
A14	16	Out	
A15/CRUOUT	19	Out	
D0 (MSB)	37	I/O	DATA BUS
D1	40	I/O	D0 through D7 comprise the bi-
D2	39	I/O	directional data bus. This bus
D3	42	I/O	transfers memory data to (when
D4	35	I/O	writing) and from (when reading)
D5	38	I/O	the external memory system when
D6	36	I/O	MEMEN is active.
D7	34	I/O	
			BUS CONTROL
MEMEN	32	Out	MEMory ENable. MEMEN indicates a memory access.
DBIN	9	Out	Data Bus IN. When active (high) the data buffers and 9900 are in the input mode.
WE	26	Out	Write Enable. WE indicates a memory write.
MBE	28	Out	Memory Block Enable. MBE indicates a memory access in memory block 4000-5FFF.
CRUCLK	22	Out	CRU CLOCK. Indicates data is available on the CRU OUT line.
CRUIN	33	In	CRU data IN. Input data line to the Home Computer.
READY/HOLD	12	In	READY (when MEMEN is active) Indicates external memory is ready for a memory access. HOLD (when MEMEN is inactive) indicates request to use data buss.

I/O DESCRIPTION (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
			MEMORY CONTROL
HOLD/IAQ	41	Out	HOLD Acknowledge goes true when MEMEN is inactive and indicates that the 9900 is in a HOLD state. Instruction AcQuisition indicates (when MEMEN is active) the CPU is acquiring an instruction during a memory cycle.
			TIMING AND CONTROL
LOAD	13	In	When active, LOAD causes the CPU to execute a nonmaskable interrupt; memory addresses FFFC and FFFE contain the new workspace and PC vectors respectively. vectors respectively.
RESET	3	Out	When active, RESET causes the Home Computer and the peripherals to be reset. RESET will be held active for a minimum of 5 clock cycles.
EXT INT	4	In	EXTernal INTerrupt. When active, EXT INT causes the CPU to execute an interrupt.
Ø3	24	Out	CPU clock. Phase 3 of the CPU clock.
			POWER
GND	21,23 25,27		Ground reference.
			SPEECH MODULE SIGNALS
SBE	2	Out	Speech Block Enable. SBE indicates a memory access in the speech memory.
AUDIO IN	44	In	Input for the audio from the speech module.
	+5	1	Supply voltage (+5V Nom) for speech module (50ma Max)
	-5	43	Supply voltage (-5 Nom) for speech module (50ma Max)

II. MEMORY ALLOCATION

The memory address space is broken into 8 blocks of 8K bytes of memory. The third block (addresses 4000 - 5FFF) is predecoded and made available at the I/O port for the peripherals. The second, sixth, seventh, and eighth blocks (address 2000-3FFF and A000-FFFF) are in the memory expansion peripheral. For the speech module, (addresses 9000-97FF), a predecoded line is available at the I/O port.

SYSTEM MEMORY MAP

HEX ADDRESS

0 - 1FFF	Console ROM Space
2000 - 3FFF	Memory Expansion
4000 - 5FFF	Peripheral Expansion (predecoded to I/O Connector).
6000 - 7FFF	Command Module ROM/RAM (predecoded to GROM Connector.
8000 - 9FFF	Microprocessor RAM, VDP, GROM, SOUND and SPEECH select.
A000 - BFFF	Memory Expansion
C000 - DFFF	" "
E000 - FFFF	" "

MEMORY MAPPED DEVICES

ADDRESSES	A0	A1	A2	A3	A4	A5	A14	USE
8000	1	0	0	0	0	0	0	Internal RAM (8300-83FF)
8400	1	0	0	0	0	1	0	Sound
8800	1	0	0	0	1	0	0	VDP Read Data
8802	1	0	0	0	1	0	1	VDP Read Status
8C00	1	0	0	0	1	1	0	VDP Write Data
8C02	1	0	0	0	1	1	1	VDP Write ADDR.
9000	1	0	0	1	0	0	0	Speech Read
9400	1	0	0	1	0	1	0	Speech Write
9800	1	0	0	1	1	0	0	GROM Read Data
9802	1	0	0	1	1	0	1	GROM Read ADDR.
9C00	1	0	0	1	1	1	0	GROM Write Data
9C02	1	0	0	1	1	1	1	GROM Write ADDR.

Banks 1-7 available at other addresses, with external decode logic.

III. CRU ALLOCATION

Of the available 4K of CRU bits, the first 1K (addresses 0000-07FE) are used internally in the console. The second 1K (addresses 0800-0FFE) are reserved for future use. The last 1.9K (addresses 1000-1FFE) are reserved for the peripherals to be plugged in the I/O port. A block of 128 CRU bits is assigned to each peripheral as listed below.

CRU ASSIGNMENTS

CRU ADDRESS	A3	A4	A5	A6	A7	USE
0000-0FFE	0	X	X	X	X	Internal Use
1000-10FE	1	0	0	0	0	Hard Disk Controller
1100-11FE	1	0	0	0	1	Disk Controller
1200-12FE	1	0	0	1	0	Modems
1300-13FE	1	0	0	1	1	RS232 (I)
1400-14FE	1	0	1	0	0	Reserved
1500-15FE	1	0	1	0	1	RS232 (II)
1600-16FE	1	0	1	1	0	Reserved
1700-17FE	1	0	1	1	1	Reserved
1800-18FE	1	1	0	0	0	Thermal Printer
1900-19FE	1	1	0	0	1	Unassigned
1A00-1AFE	1	1	0	1	0	Reserved
1B00-1BFE	1	1	0	1	1	Debugger
1C00-1CFE	1	1	1	0	0	VCR Controller
1D00-1DFE	1	1	1	0	1	IEEE 488 Bus Controller
1E00-1EFE	1	1	1	1	0	Reserved
1F00-1FFE	1	1	1	1	1	P-Code

IV. INTERRUPT HANDLING

The interrupt available on the I/O port is one of the maskable interrupts of the TMS 9901 Programmable System Interface.

9900 INTERRUPTS

INTERRUPT LEVEL	VECTOR LOC. (MEMORY ADDR. IN HEX)	CPU PIN	DEVICE ASSIGNMENT
(Highest Priority)	0000-WSP 0002-PC	RESET	RESET
0	FFFC-WSP FFFE-PC	LOAD	LOAD
1	0004-WSP 0006-PC	--	EX DEV (9901)

Lower priority CPU interrupts are not used. The additional interrupts are implemented on the 9901. Interrupt Level 1 is decoded by software to be either (1) VDP vertical sync. (2) 9901 internal timer or (3) I/O bus-generated.

9901 INTERRUPT MAPPING

ADDRESS	CRU BIT	9901	PIN	FUNCTION
0000	0	Control		Control
0002	1	INT1	17	External Interrupt
0004	2	INT2	18	Video Display Processor Vertical Sync
0006	3	INT3	9	9901 Internal Timer, Keyboard "=" line, Joystick "FIRE"
0008	4	INT4	8	Keyboard "Space" line, Joystick "LEFT"
000A	5	INT5	7	Keyboard "RETURN" line, Joystick "RIGHT"
000C	6	INT6	6	Keyboard "0" line, Joystick "DOWN"
000E	7	INT7 (P15)	34	Keyboard "FCTN" line, Joystick "UP"
0010	8	INT8 (P14)	33	Keyboard "SHIFT" line
0012	9	INT9 (P13)	32	Keyboard "CTRL" line
0014	10	INT10 (P12)	31	Keyboard "Z" line
0016	11	INT11 (P11)	30	Not Used As Interrupt
0018	12	INT12 (P10)	29	Reserved
001A-1E	13-15	INT13-INT15	28,27 & 23	Not Used As Interrupt

9901 I/O MAPPING

ADDRESS	CRU BIT	9901	PIN	FUNCTION
0020	16	P0	38	Reserved
0022	17	P1	37	Reserved
0024	18	P2	26	Bit2 of Keyboard Select
0026	19	P3	22	Bit1 of Keyboard Select
0028	20	P4	21	Bit0 (MSB) of Keyboard Select
002A	21	P5	20	Keyboard (ALPHA LOCK)
002C	22	P6	19	Cassette Control 1
002E	23	P7 (INT15)	23	Cassette Control 2
0030	24	P8 (INT14)	27	Audio Gate
0032	25	P9 (INT13)	28	Mag Tape Out
0034	26	P10 (INT12)	29	Reserved
0036	27	P11 (INT11)	30	Mag Tape Input
0038-003E	28-31	P12-15	31-34	Not Used In I/O Mapping

V. ELECTRICAL CHARACTERISTICS

DRIVE CAPABILITY OF I/O SIGNALS

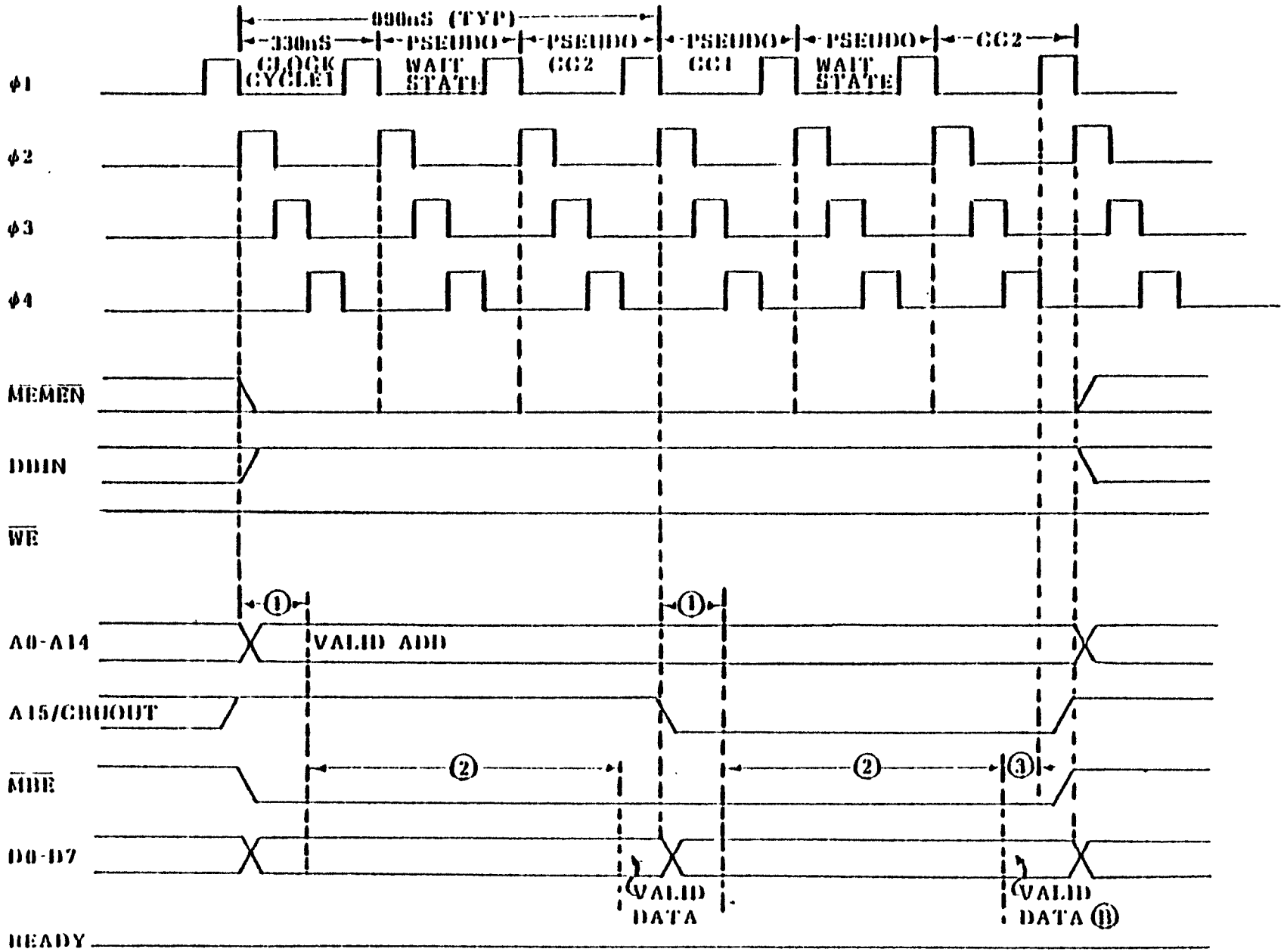
SIGNAL NAME	DRIVER
$\overline{\phi 3}$	74LS244
CRUCLK	74LS244
WE	74LS244
A0	74LS244
A1	74LS244
A2	74LS244
DBIN	74LS04
MBE	74LS244
MEMEN	74LS32
A3-A14	74LS367
D0-D7	74LS245
A15/CRUOUT	74LS244
SBE	74LS03
HOLD/IAQ	74LS32
RESET	74LS04

I/O READ

A CPU Read cycle for the external device consists of two 8-bit read cycles (Fig.B). The 2 bytes read are assembled as a 16 bit word before they are presented to the 9900. Shown in Fig. B are two 8 bit read cycles with one wait state inserted in each to work with slow memories. MEMEN goes low true at the beginning of clock cycle 1. At the same time DBIN goes high true. WE stays high false during the entire cycle. At the same time that MEMEN goes true, the address bus goes active. In order for the noise and the glitches (associated with crosstalk and simultaneous switching) to go away a minimum of 100nS should be allowed for the address lines to settle. MBE (predecoded from A0, A1, A2 and MEMEN) goes true during the leading edge of $\phi 2$ of clock cycle 1. Data read from the peripherals will be valid 750nS after the start of clock cycle 1. The CPU will look at the full 16 bit data bus during the leading edge of $\phi 1$, of clock cycle 2. Under worse-case conditions, data must be valid 100nS before that time.

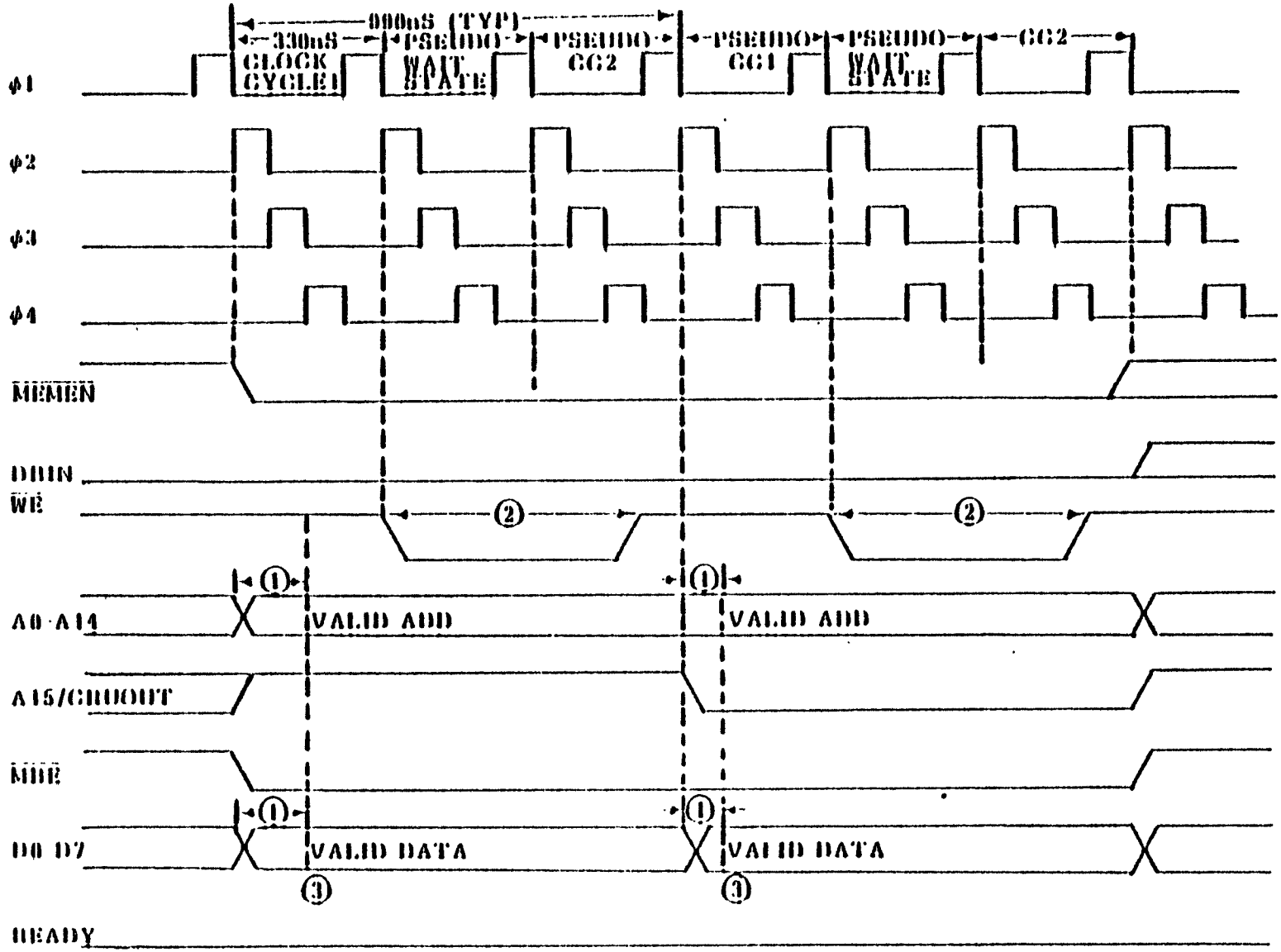
I/O WRITE

Figure C shows a 16 bit I/O write cycle. As described earlier it is composed of two 8-bit writes. A write cycle will always be preceeded by an ALU cycle. MEMEN and DBIN go true at the start of the cycle. A settling time of 100nS (min) is allowed for the address lines to settle. down. WE goes true (low) on the leading edge of $\phi 2$, during the wait states, and stays true for 660nS (TYP). Both during a Read or a Write the odd byte is accessed first, followed by the even byte. A15/CRU OUT changes its state 900nS (TYP) after the cycle is initiated. The second 8-bit write cycle is identical to the first 8-bit write. MBE stays true (low) during the entire (1.8us) cycle.



(1) - SETTLING TIME= 100nS (MIN)
(2) - ACCESS TIME FOR DSR ROM + DATA Ta + DATA BUFF DELAY (PERIPHERAL + MAINFRAME) =650nS (MAX)
(3) - SETUP TIME FOR 9900= 60nS (MIN)

FIGURE B
I/O READ TIMING



① SETTLING TIME- 100nS (MIN)
② WE PULSE WIDTH- 660nS (TYP)
③ VALID DATA

FIGURE C

I/O WRITE TIMING

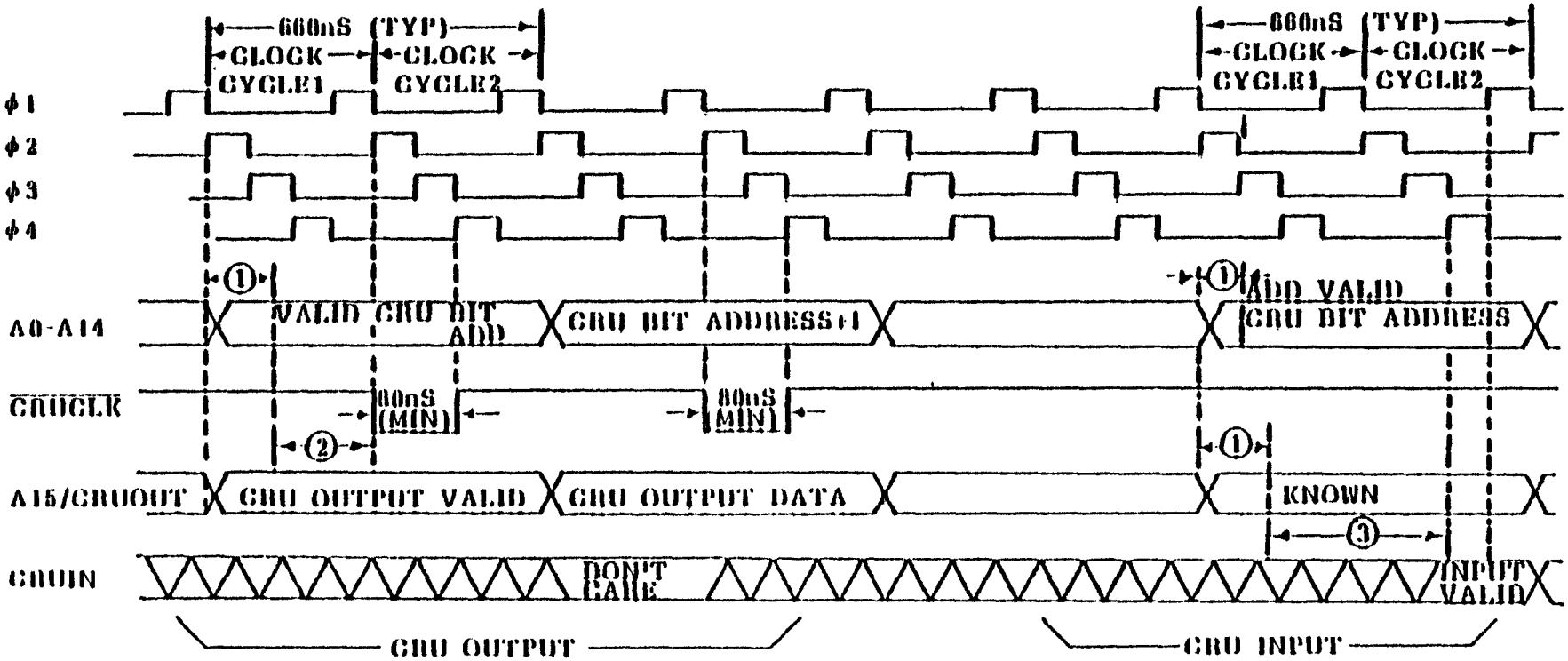
CRU TIMING

CRU interface timing is shown in figure D. The CRU OUT cycle is composed of 2 clock cycles. The CRU bit address when placed on the address bus A0 through A14 is allowed to settle for 100nS (min). CRUCLK is 63nS (max) low true signal which occurs on the trailing edge of 01 of clock cycle 2. CRUOUT data is valid at the state of clock cycle 1, and is latched by CRUCLK in the respective peripheral.

CRUIN also consists of 2 clock cycles 660nS (TYP). Again we allow 100nS for the address bus to settle down. The CPU samples the CRUIN line on the leading edge of 01 of clock cycle 2. Data must be valid 40nS (min) before that. This implies less than 500nS for CRUIN.

I/O BUS LOADING

SIGNAL	TOTAL SWITCHING LOAD (pf)	MAXIMUM PERIPHERAL LOAD (pf)
D0-D7	210	90
A0-A2	100	90
A3-A14	100	90
A15/CRUOUT	110	100
$\overline{03}$	110	100
$\overline{RESET}$	100	90
READY/HOLD	80	70
$\overline{CRUIN}$	125	90
$\overline{CRUCLK}$	100	90
$\overline{MBE}$	100	90
$\overline{WE}$	100	90
$\overline{SBE}$	35	25
$\overline{DBIN}$	100	90
$\overline{MEMEN}$	100	90
HOLD/IAQ	80	70



①-SETTLING TIME 100nS (MIN)
②-ADD VALID TO $\overline{\text{CRUCLK}}$ =220nS (TYP)
③-ADD VALID TO VALID CRUIN =400nS (MAX)

FIGURE D

CRU TIMING

VI. GLOSSARY

CPU	Central Processing Unit
CRU	Communication Register Unit (I/O technique for TMS 9900 Microprocessor)
DSR	Device Service Routine (TMS 9900 Machine language for Device Interface).
GROM	Graphics Read Only Memory (TMC 0430). This memory device is a 6144 byte read only memory with on board 13 bit program counter. The program counter can be written or read through an eight bit interface and will automatically increment.
I/O	Input/Output
VDP	Video Display Processor (TMS 9918A).
ROM	Read Only Memory.
RAM	Random Access Memory
MSB	Most Significant Bit
BIT	Smallest unit of memory, Binary digiT
BYTE	8 Bits of Memory
WORD	16 Bits/2 Bytes of Memory
ALU	Arithmetic Logic Unit

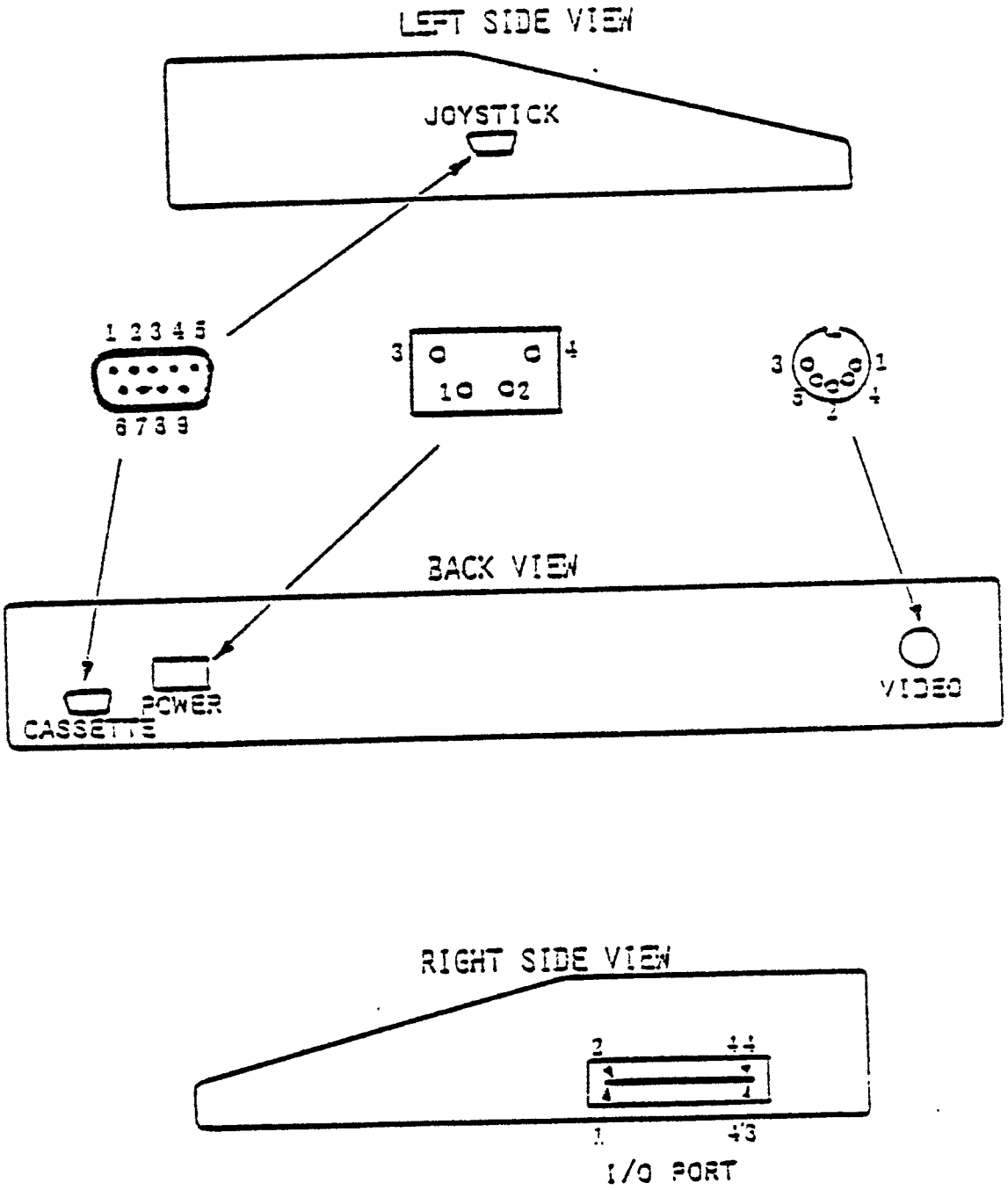


FIGURE E
CONNECTOR PIN IDENTIFICATION DIAGRAM

HP 1039026 REV A
MARKING

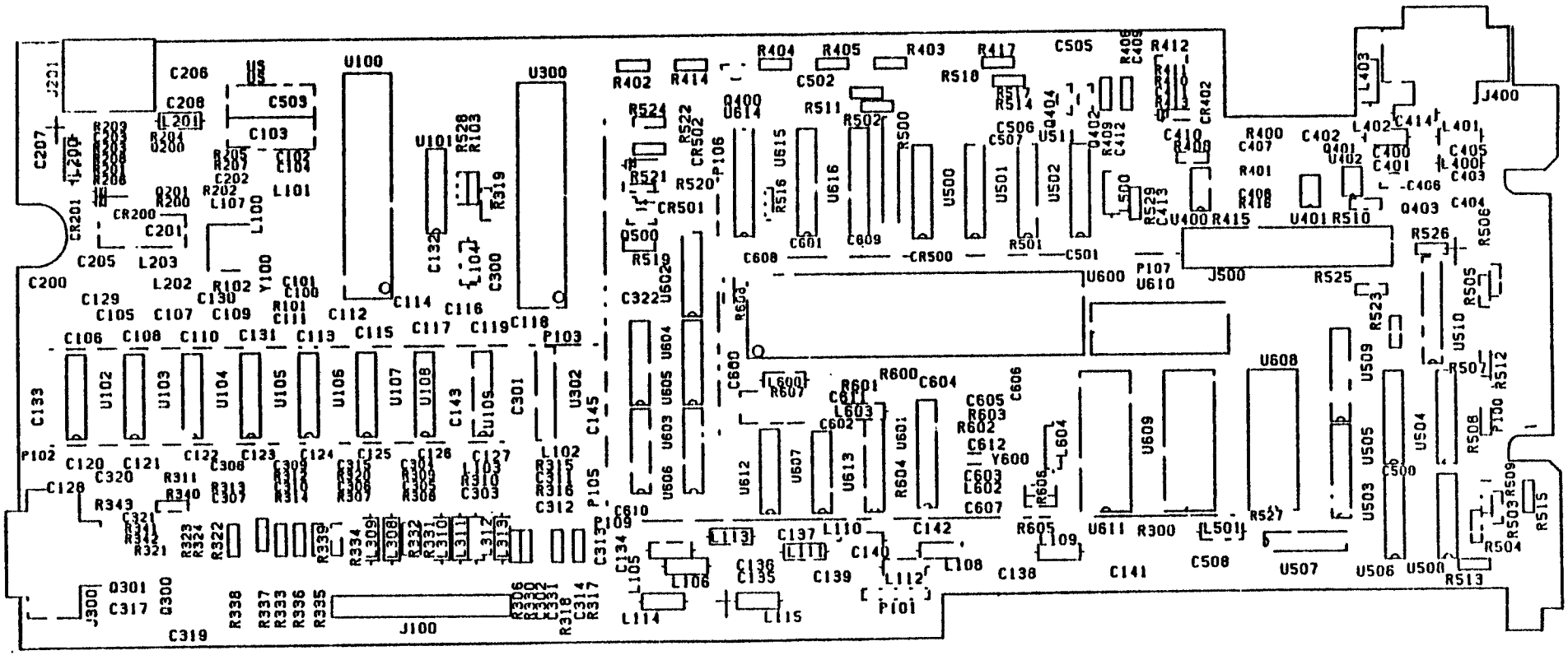


Figure F

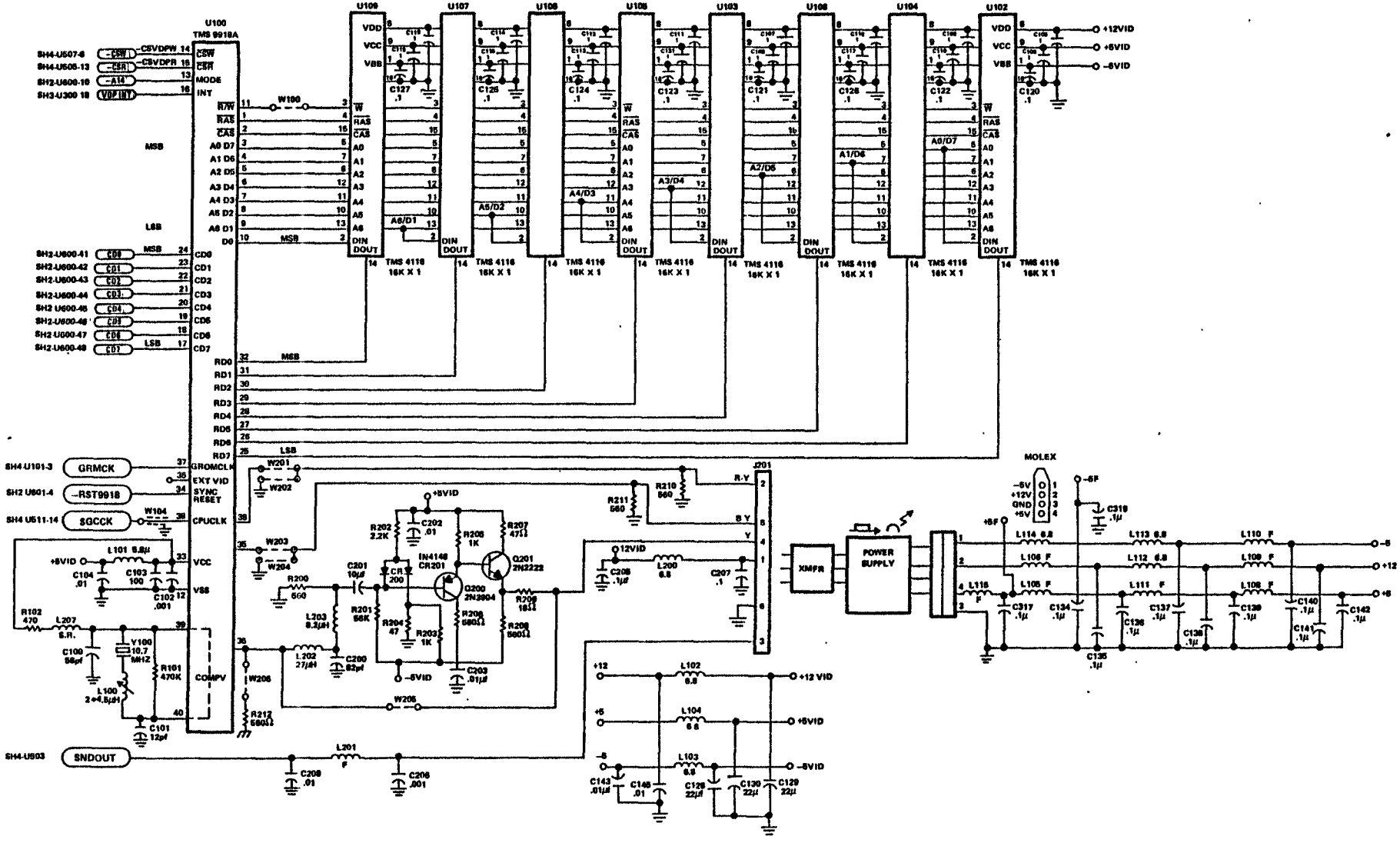


FIGURE G. TI-99/4A SCHEMATIC DIAGRAM (PAGE 1 OF 5)

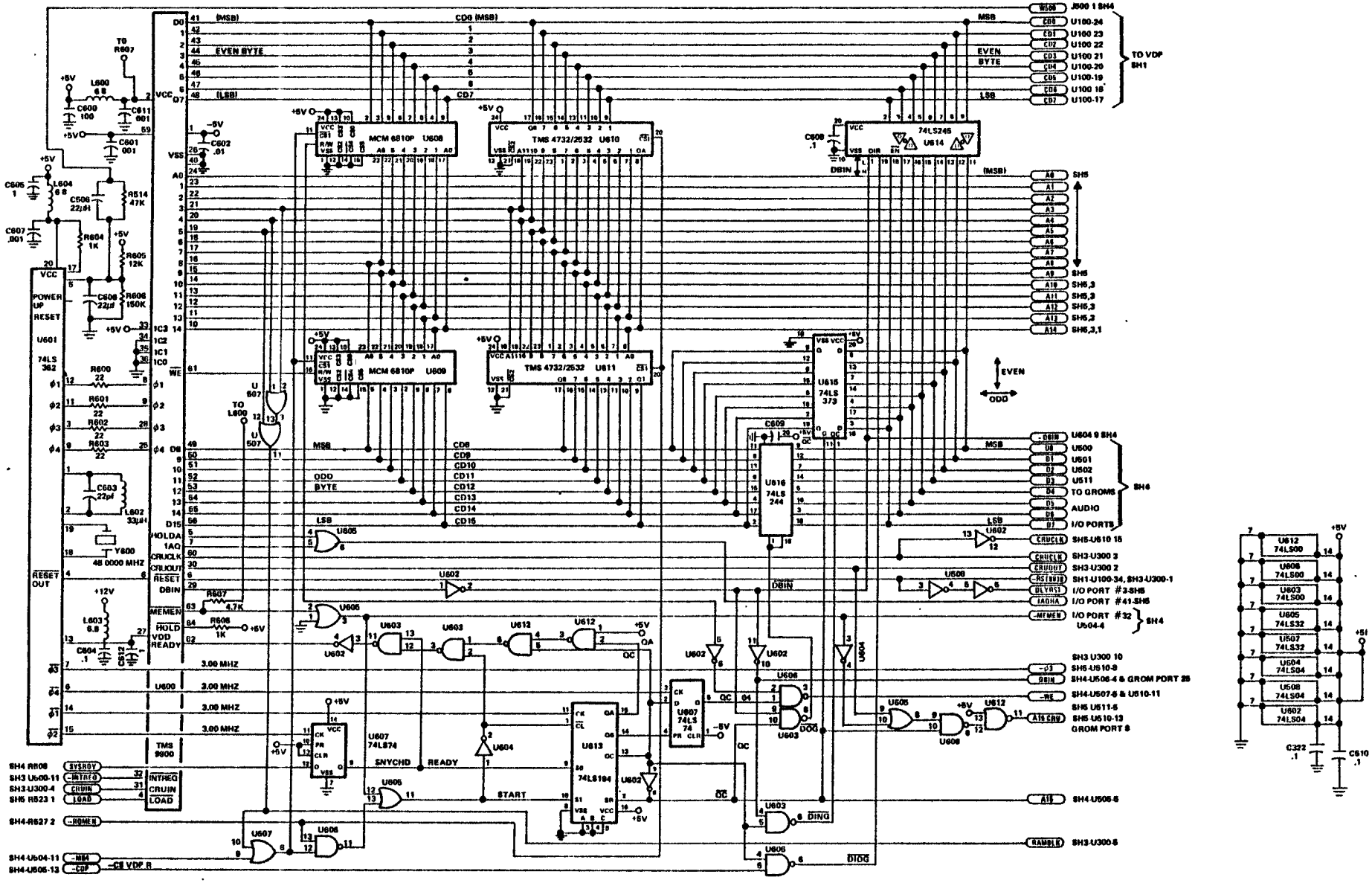


FIGURE G. TI-99/4A SCHEMATIC DIAGRAM (PAGE 2 OF 5)

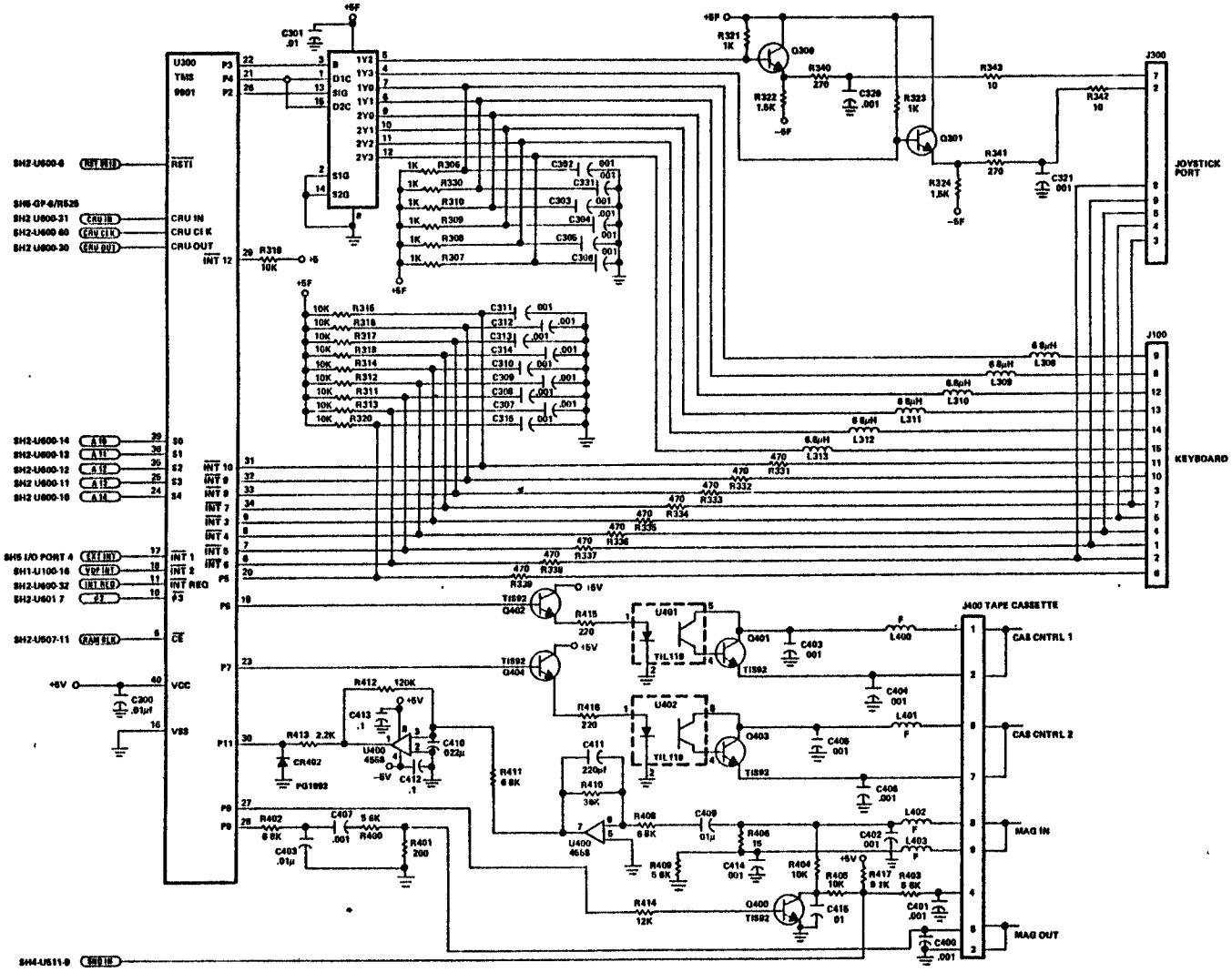


FIGURE G. TI-99/4A SCHEMATIC DIAGRAM (PAGE 3 OF 5)

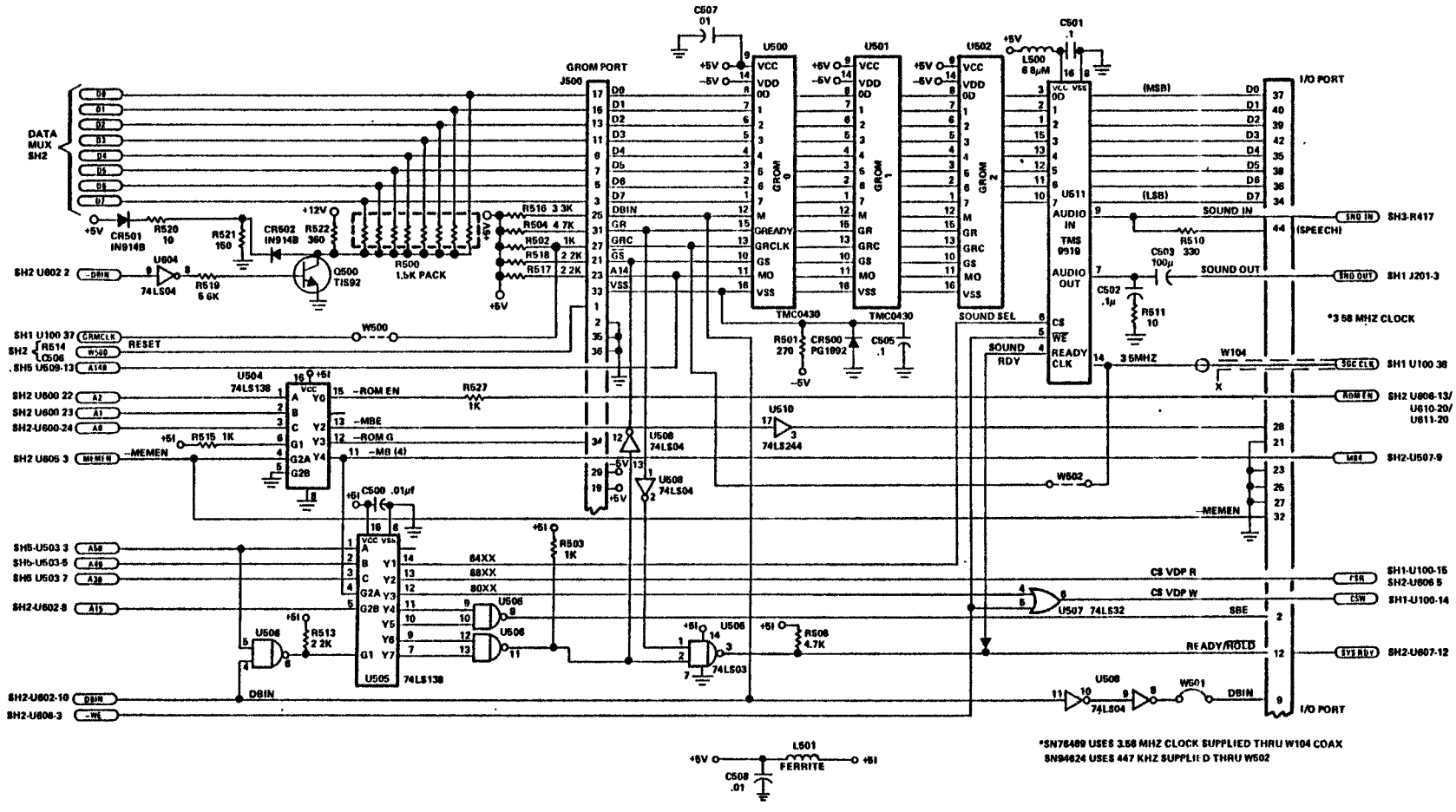
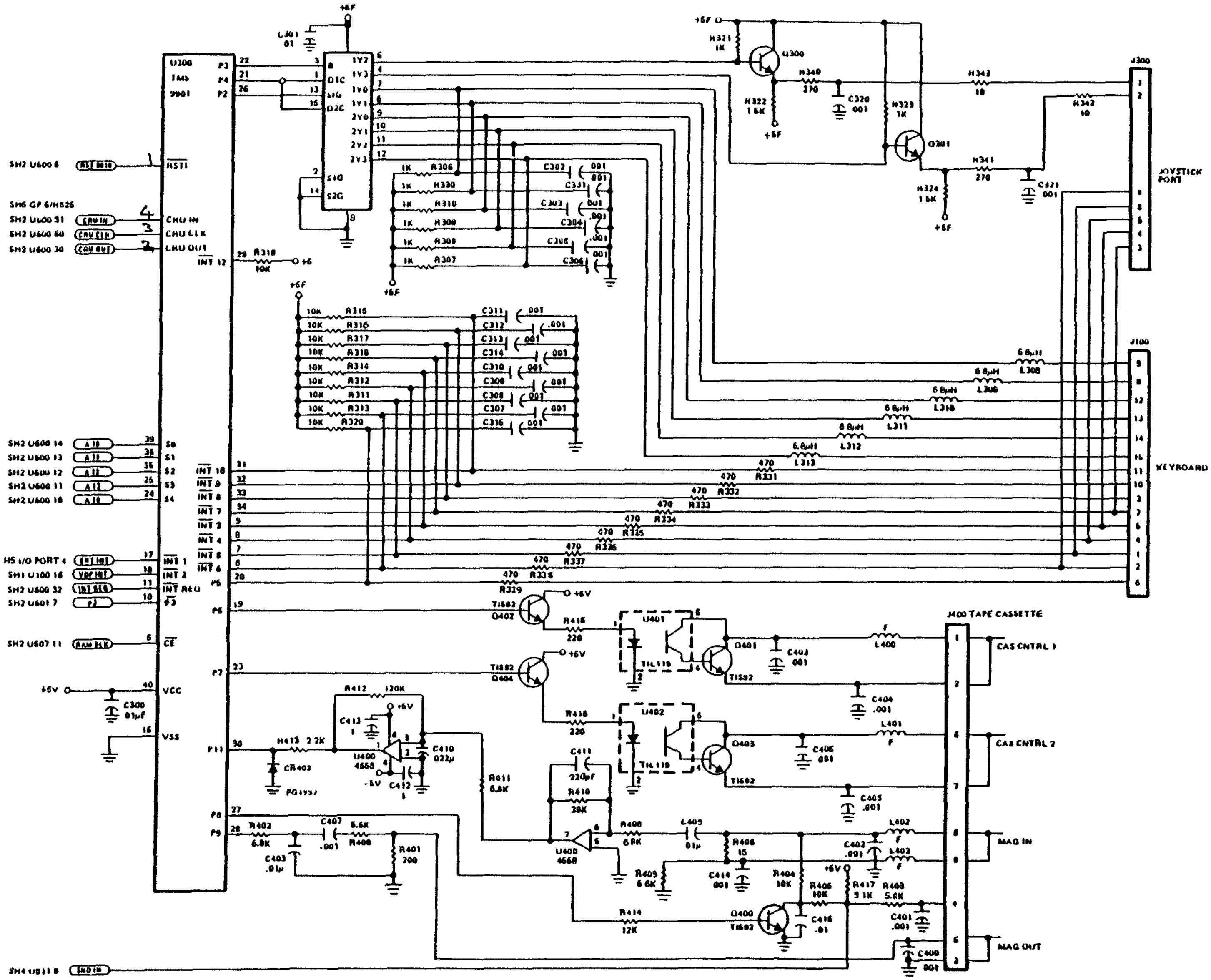


FIGURE G. TI-99/4A SCHEMATIC DIAGRAM (PAGE 4 OF 5)


U300
TMS
9901
HSTI
CHU IN
CHU CLK
CHU OUT
INT 12
JOYSTICK PORT
KEYBOARD
J400 TAPE CASSETTE
CAS CNTRL 1
CAS CNTRL 2
MAG IN
MAG OUT
VCC
VSS
+5V