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TEXAS INSTRUMENTS

TM 990

Microcomputer Handbook

MICROPROCESSOR SERIES

July 1979

LIST OF FIGURES

SECTION 1

INTRODUCTION

1.1 GENERAL

The Texas Instruments TM 990 Microcomputer Handbook describes the total capability of the product line. Taking the time to study this handbook will help insure that the optimum solution to a design is realized.

The CPU modules with on-board memory and I/O are highlighted in Section 2. These modules contain the Texas Instruments powerful 16-bit microprocessor featuring software compatibility ranging from the chip level up to and including the TM 990 minicomputer.

Memory modules are featured next and may be selected from a full line populated with dynamic RAM, EPROM and/or static RAM. A detailed description of these modules is given in section 3 to assist in selecting the right module or combination of modules.

Input/output modules answer your interface problems. Everything from optically isolated I/O for the AC/DC industrial environments; A/D and D/A modules; and TM 990/5MT modules for use on machine tools, process control systems, material handling equipment, and other industrial applications where operating conditions, both electrical and physical, may be severe.

In addition to a full line of hardware modules, Texas Instruments offers an extensive line of software products (see section 5). Solid state software includes line-by-line assemblers, monitors (for software debugging), and the easy to use English-like higher-level language, POWER BASIC. Software products on magnetic media to facilitate software development are also offered, including FORTRAN, POWER BASIC, and the higher level language that is quickly becoming an industry standard - Pascal. These products are for use on the FS (Floppy-based) and/or DS (Hard Disc) Development Systems from Texas Instruments.

The Development Systems, covered in section 7, are available in a number of cost effective products ranging from low cost board level to multi-user mini-computers with in-circuit emulation and higher-level languages. The TM 990/302 Module brings the cost of a development system within the range of virtually every designer and yet offers such powerful features as: symbolic assembler, PROM Programmer, nonvolatile storage through audio cassettes.

The AMPL (Advanced Microprocessor Prototyping Lab) allows powerful in-circuit emulation, while monitoring address and data buses simultaneously. Simple to use because of self-prompting procedures, it allows symbolic debug of hardware and software concurrently and utilized the Texas Instruments line of higher-level languages.

Some of the benefits of using the TM 990 line of off-the-shelf hardware and software products are:

- To shorten the development time (and therefore beat the competition to the market place).
- Simplify the design task and in-house design resources.

- In-house test equipment engineers can reuse the hardware to test a new product when an old product becomes obsolete.

- Test Marketing and Engineering runs of a new product can economically be introduced to the market place with a minimum amount of investment.

The TM 990 Module line will continue to take advantage of the latest semiconductor technology from Texas Instruments. Leadership products from Texas Instruments such as the first 4K by 8 EPROM, the first 64K dynamic RAM, bubble memories, I^2L Technology, Fiber Optics, etc. are all candidates for exciting additions to the TM 990 lines.

Texas Instruments welcomes you the family of TM 990 users and we hope that you will find the Systems Manual very helpful.

SECTION 2

CPU MODULES (100 SERIES MODULES)

2.1 GENERAL

A typical CPU module consists of the following: CPU, clock, RAM and ROM memory, serial and parallel I/O interfaces, and buffers for off-board expansion. These modules come preassembled, pretested, and ready to use. Simply plug the CPU module into a TM 990/510 or TM 990/520 card cage, connect a suitable terminal, connect a power supply to the barrier strip on the back plane and the system is ready to use. Some of the general features of the CPU modules are as follows:

- TMS 9901 Programmable Systems Interface (Parallel I/O Interface)
- TMS 9902 Asynchronous Communications Controller (Serial I/O Interface)
- TIBUG Operating Monitor
- Interface to TM990 System Bus

As the specific features vary from module to module, it is advisable to check the data sheets located in this section for the features of a given CPU module.

2.2 TIBUG OPERATING MONITOR

The CPU modules typically come equipped with the TM 990/401 TIBUG monitor. TIBUG includes 13 user commands plus six user accessible utilities and operates with 110, 300, 1200, 2400 and 9600 baud terminals.

TIBUG functions include the following:

- Inspect/change CPU, memory location, program counter, workspace pointer, status register, workspace elements
- Execute user programs under breakpoint in single/multiple steps
- Dump/load memory to, from paper tape or cassettes
- Find word/byte
- Hexadecimal arithmetic

User accessible utilities include the following:

- Read/Write character
- Hexadecimal numeric input/output
- ASCII message output

2.3 PROTOTYPING AREA

The TM 990/180 and TM 990/100M CPU modules provide a protoyping area that can be used for custom applications which require special interface circuitry. This area can also be used for adding additional devices such as TMS 9901's or TMS 9902's. Pads containing voltages and signals that may be needed are located on the periphery of the prototyping area.

2.4 SUMMARY OF KEY PARAMETERS

Table 2-1 provides a listing of the features of the CPU modules. This table provides information regarding the microprocessor, memory, power requirments and I/O interfaces that are used on the CPU modules.

2.5 CPU MODULE DATA SHEETS

Data sheets are provided in the following sections to familiarize the customer with characteristics of Texas Instruments CPU modules.

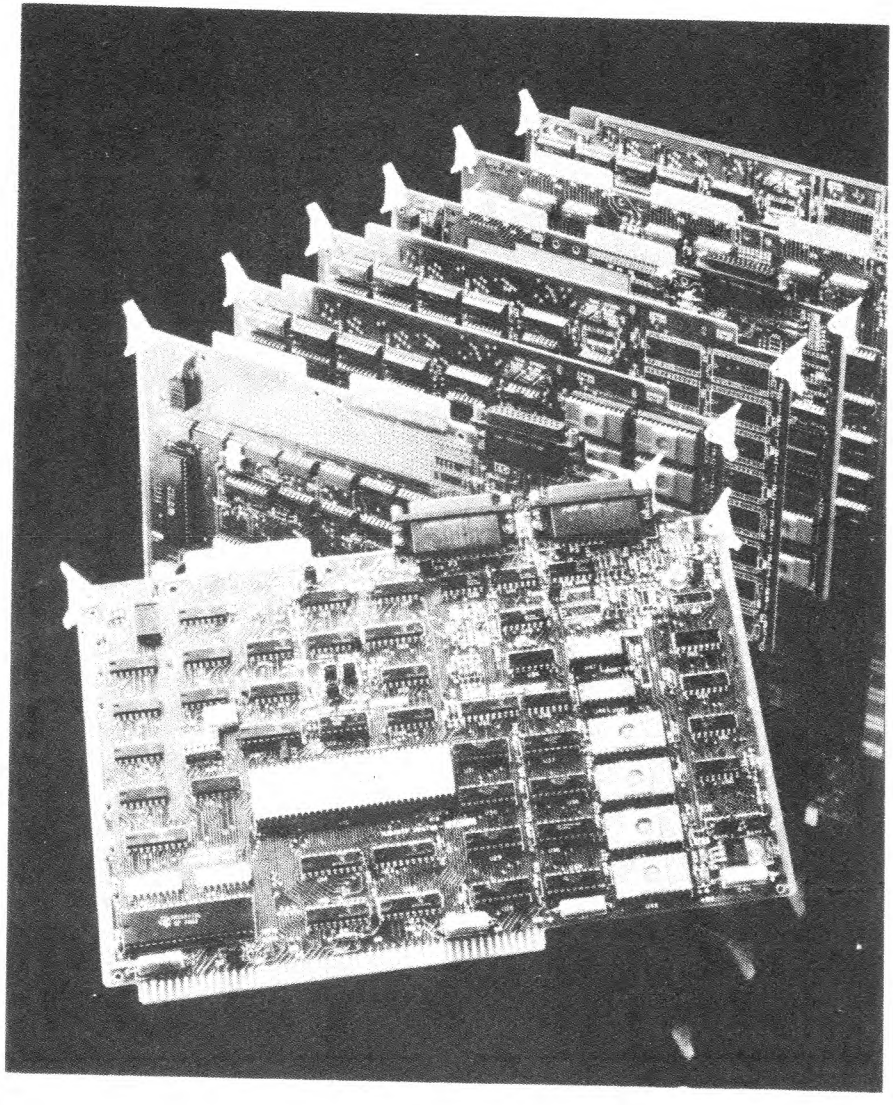
Table 2-1. SUMMARY OF KEY PARAMETERS

CPU MODULES

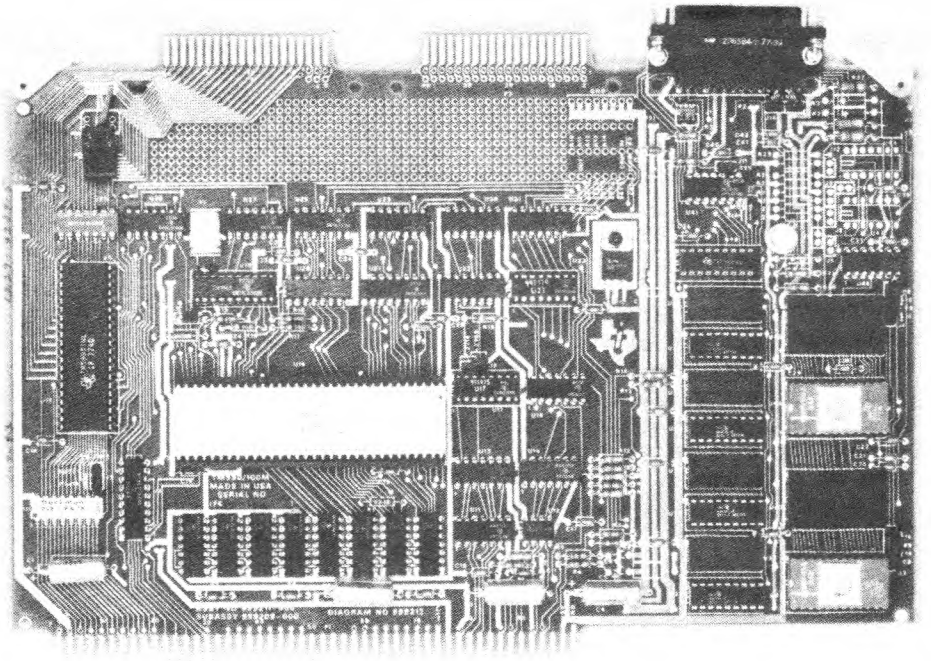
PRODUCT	CPU	EPROM (Bytes)	RAM (Bytes)	SERIAL I/O	Parallel I/O Lines	Prioritized Vectored Interrupts	Timers	Power Requirements +5V	+12V	-12V
TM990/100M-1	TMS9900	2K (2708) (Contains TIBUG Monitor) Expandable to 8K (2716)	512 Expandable to 1K	RS232C or TTY	16	16	2	1.3A	0.2A	0.1A
TM990/100M-2	TMS9900	2K (2708) (Blank Eprom's) Expandable to 8K (2716)	512 Expandable to 1K	RS232C or Differential line	16	16	2	1.4A	0.3A	0.1A
TM990/100M-3	TMS9900	8K (2716)	1K (4042-2)	RS232C or Differential line	16	16	2	1.6A	0.3A	0.2A
TM990/101M-1	TMS9900	2K (2708) (Contains TIBUG Monitor) Expandable to 8K (2716)	2K Expandable to 4K	Port A RS232C or TTY Port B RS232C or Modem	16	16	3	1.6A	0.3A	0.2A
TM990/101M-2	TMS9900	2K (2708) Blank Expandable to 8K (2716)	2K Expandable to 4K	Port A - RS232C or Multidrop Port B - RS232C or Modem	16	16	3	1.6A	0.3A	0.2A
TM990/101M-3	TMS9900	8K (2716) Blank	4K	Port A RS232C or TTY Port B RS232C or Modem	16	16	3	1.7A	0.4A	0.2A
TM990/101M-10	TMS9900	8K (2716) (Contains POWER BASIC)	2K Expandable to 4K	Port A RS232C or TTY Port B RS232C or Modem	16	16	3	1.7A	0.4A	0.2A
TM990/180M-1	TMS9980	2K (2708) (Contains TIBUG Monitor) Expandable to 4K	512 Expandable to 1K	RS232C or TTY	16	6	2	1.3A	0.2A	0.1A
TM990/189	TMS9980A/ MP9529	4K (4732) Expandable to 6K	1K Expandable to 2K	RS232C or TTY	16	6	3	1.8A	0.2A	0.2A

2.5 CPU MODULE

DATA SHEETS



2.5.1 TM 990/100M MICROCOMPUTER MODULE



The TM 990/100M is an assembled, tested microcomputer module utilizing the powerful, NMOS 16-bit, TMS 9900 microprocessor as its CPU. With RAM and ROM/EPROM included on board as well as programmable serial and parallel I/O, the TM 990/100M is a powerful single-board microcomputer. Since all address, data, and control lines are brought to the board connectors, the board can be expanded to use the entire capabilities of the TMS 9900 in larger systems.

FEATURES

- TMS 9900 16-bit CPU
- 512 bytes of 4042-2 (2111-1) static RAM, expandable to 1K byte
- 2K bytes of 2708 EPROM, expandable to 8K bytes using 2716 EPROM
- TMS 9901 programmable system interface
- TMS 9902 asynchronous communications controller
- EIA or TTY terminal interface option
- Prototyping area for custom applications
- Fully expandable bus structure
- Designed to fit the TM 990/510 or TM 990/520 card cage
- TIBUG operating monitor

OPERATION

The TM 990/100M microcomputer is a software compatible member of the TMS 9900/990 family. The TMS 9900 is used as a CPU to provide 16 bits of processing power with a minicomputer instruction set which includes multiply and divide. The TM 990/100M module is designed for 3 MHz operation, utilizing the full 16 levels of prioritized interrupts and the advanced memory-to-memory architecture of the TMS 9900. Additionally, the bus structures are set up to take advantage of the full 64K byte memory addressing capability of the 9900 and the nonmultiplexed memory, I/O and interrupt buses.

MEMORY

The on-board memory includes both an EPROM/ROM section and a static RAM section. Four sockets are available for TMS 2708, TMS 2716 EPROM or TMS 4700 ROM operation. The assembled price includes two TMS 2708's, or 2K bytes. Using the available jumper option, all four sockets can be populated with TMS 2716's, providing a maximum on-board EPROM capability of 8K bytes. The static RAM area consists of two 512-byte banks of memory. Four TMS 4042-2 (TMS 2111-1) sockets are populated and four additional sockets are provided. The cycle time of this memory section is 0.667 microseconds. The address map is shown in Figure 2-4 for the board as shipped. DMA Control lines are also accessible on the bus.

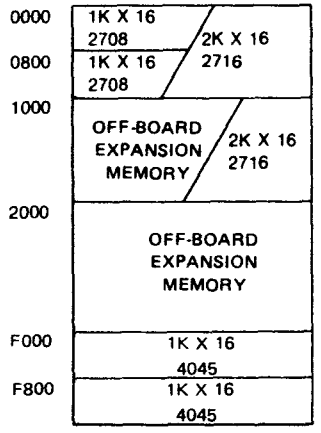


FIGURE 2-4. MEMORY ADDRESS MAP

INTERRUPTS AND TIMERS

Fifteen maskable interrupts plus the reset and load trap vectors are implemented. Table 2-2 shows the implementation. The TMS 9901 handles all 15 external interrrupts which can be generated from either the bus connector or the I/O bus. The TMS 9901 enables each level to be individually maskable under program control. Additionally, level 3 can be programmed to use the interval timer in the TMS 9901. Level 4 can be generated from the TMS 9902 as an interval timer or for three other serial interface conditions (see the TMS 9902 Data Manual). Two programmable timers, therfore, are available on board.

The serial I/O and the parallel I/O are handled over the dedicated I/O bus of the TMS 9900, the communications register unit (CRU). Table 2-3 lists the address assignments within the dedicated 4K CRU address space. The TMS 9902 acts as the controller for this asnychronous serial interface. The character length, baud rate (75 to 38,400), parity and stop bits are programmable. Three optional types of interface are supported:

- EIA
- 20 mA neutral current loop TTY
- Private wire differential line driver/receiver.

The TM 990/100M board is delivered complete with a 25-pin RS-232 type female connector, and is jumper selectable to support EIA, TTY, and differential line driver operation. Also, the TMS 9903 synchronous communications controller can be utilized since the TMS 9902/9903 are socket compatible.

TABLE 2-2. INTERRUPTS

INTERRUPT LEVEL	FUNCTION
0	Reset or PRES
1	External Device
2	External Device
3	Clock or External
4	Serial Int. or Ext.
5-15	External Devices
LOAD	Restart

TABLE 2-3. CRU ADDRESS MAP

SOFTWARE BASE ADDRESS	CRU BIT NUMBER		FUNCTION
0080_{16}	40_{16}	$5F_{16}$	On-Board Serial I/O Port (TMS 9902)
0100_{16}	80_{16}	$9F_{16}$	On-Board 16 I/O Parallel Interface, Interrupt Status Register, Interrupt Mask Register, and Interval Timer (TMS 9901)
0000_{16}	00_{16}	$3F_{16}$	
$00C0_{16}$	60_{16}	$7F_{16}$	Reserved for On-Board Expansion
0140_{16}	$A0_{16}$	FF_{16}	
0200_{16}	100_{16}	FFF_{16}	Off-Board CRU

The parallel I/O is handled by the TMS 9901; 16 parallel lines are all interfaced to the top edge connector which has 40 pins on 0.100 inch centers. Additionally, eight parallel lines are interfaced to the bus connectors. The programmable features of the TMS 9901 permit configuring these lines as I/O lines or interrupts (refer to the TMS 9901 Data Manual). All I/O lines are equipped with pullup resistors.

TIBUG

The TIBUG monitor TM 990/401-1 is normally supplied preprogrammed in the populated TMS 2708 EPROM's. Its operation is described in the user's manual or the TM 990 series literature.

PROTOTYPING AREA

The prototyping area is large enough to accommodate one 40-pin DIP (0.6 inch centers) plus four 16 pin DIP's (0.3 inch centers).

OPTIONS

The TM 990/100M board is equipped with two TMS 2708's preprogrammed with the TIBUG monitor, and the serial I/O is jumper selectable as an EIA port, TTY interface, or a private wire differential line driver. Other software or accessories, such as the Line-By-Line Assembler and the microterminal, may be ordered under separate part numbers.

SPECIFICATIONS

CPU: TMS 9900
- Instruction Set -- 69 instructions
- 8, 16, or 32 bit operation
- 3 MHz System Clock

Interrupts: 16 levels -- 15 may be external

Interval Timers: Two (in TMS 9901 and TMS 9902)

	Resolution	Maximum Interval
TMS 9901	21.3 usec	349 msec
TMS 9902	64 usec	16.32 msec

Memory: 16-bit word configuration
- On-board EPROM/ROM, 2K bytes, expandable to 8K bytes
- On-board RAM, 512 bytes, expandable to 1K bytes
- Off-board expansion to full 64K bytes

I/O: Parallel -- 16 bits expandable to 4096 bits
- Serial -- Asynchronous Controller TMS 9902,
  - 5-8 bit character,
  - Programmable data rate, stop bits, parity
  - Break characters generation,
  - Framing, parity, and overrun errors detected
  - 75 to 38400 baud, software programmable

Interfaces:

Bus -- Data and Address -- Three-state TTL compatible buffered output
Control -- TTL compatible
Parallel I/O and Interrupts -- TTL compatible
Serial I/O -- RS-232, 20 mA current loop or differential line driver

Expansion Prototyping Area:

May contain one 40-pin DIP plus up to four 16-pin DIPs.

Software:

TIBUG monitor self contained in EPROM

Mating Connectors:

Bus	100 pin, 0.125 in. cc	TI	H321150 (wire wrap)
		TI	H322150 (solder tail)
Parallel I/O	40 pin, 0.100 in. cc	TI	H312120 (solder tail)
		3M	3464-0001 (no ears)
		Viking	3VH20/1JN5 (pierced tail
Serial I/O	25 pin (male)	Cinch	DB-25

Power Requirements:

+5V ±3% @ 1.3A
+12V ± 3% @ 0.2A
-12V ± 3% @ 0.1A

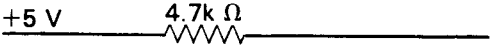
Operating Temperature Range:

0 deg C to 70 deg C

Physical Characteristics:

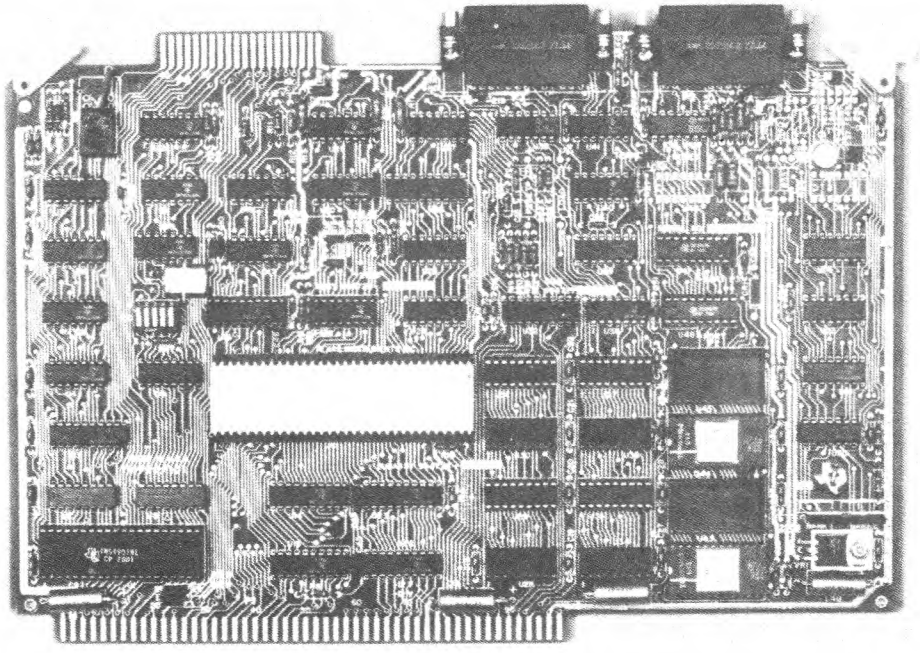
Width:	11 inches
Height:	7½ inches
Board Thickness:	0.062 inch

I/O and Interrupt Terminations:



Ordering Information:

TM 990/100M-1	TMS 9900 microcomputer board with TIBUG monitor in two TMS 2708 EPROM's and EIA or TTY serial I/O jumper option
TM 990/100M-2	TMS 9900 microcomputer board with unprogrammed TMS 2708 EPROM's and EIA or differential line driver jumper option
TM 990/100M-3	TMS 9900 microcomputer board with fully expanded memory (four TMS 2716 EPROM's and eight TMS 4042-2 RAM's) and EIA or differential line driver jumper option



The TM 990/101M is an assembled, tested microcomputer module utilizing the powerful, NMOS 16-bit, TMS 9900 microprocessor as its CPU. With RAM and ROM/EPROM included on board as well as programmable serial and parallel I/O, the TM 990/101M is a powerful single-board microcomputer. Since all address, data, and control lines are brought to the board connectors, the board can be expanded to use the entire capabilities of the TMS 9900 in larger systems. Figure 2-5 is a system block diagram of the TM 990/101M.

FEATURES

- TMS 9900 16- bit CPU
- 2K bytes of TMS 4045 (2114) Static RAM, expandable to 4K bytes
- 2K bytes of ROM, expandable to 8K bytes of ROM or EPROM
- TMS 9901 programmable system interface with up to 16 programmable I/O lines
- Two TMS 9902 asynchronous communications controllers
- EIA or TTY terminal interface option
- Supports communication with 103 and 202 series modems using optional cable
- Fully expandable bus structure & DMA to on-board memory
- Designed to fit the TM 990/510 and TM 990/520 card cage
- TIBUG operating monitor

- 3 MHz operation
- 3 Programmable interval timers
- 17 interrupts: 2 non-maskable and 15 prioritized and maskable
- Edge triggered interrupt, with software reset
- CRU addressable L.E.D. and DIP switch for custom applications

OPERATION

The TM 990/101M microcomputer is a software compatible member of the TMS 9900/990 family. The TMS 9900 is used as a CPU to provide 16 bits of processing power with a minicomputer instruction set which includes multiply and divide. The TM 990/101M module is designed for 3 MHz operation, utilizing the full 16 levels of prioritized interrupts and the advanced memory-to-memory architecture of the TMS 9900. Additionally, the bus structures are set up to take advantage of the full 64K byte memory addressing capability of the 9900 and the nonmultiplexed memory, I/O and interrupt busses. A total of eight addressing modes, including indirect and indexed addressing, provide powerful software capabilities while the TMS 9900's two-address architecture makes a memory-to-memory add possible without having to load register pairs with addresses or using dedicated accumulators.

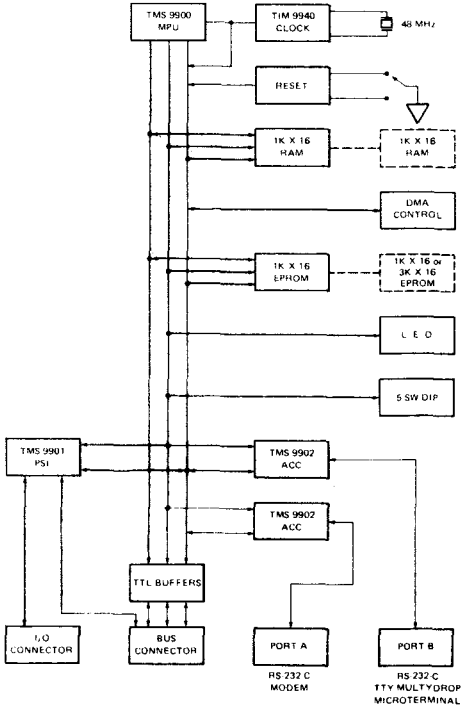


FIGURE 2-5. TM 990/101M BLOCK DIAGRAM

MEMORY

The on-board memory includes both an EPROM/ROM section and a static RAM section. Four sockets are available for TMS 2708, TMS 2716 EPROM or TMS 4700 ROM operation. Using the available jumper option, all four sockets can be populated with TMS 2716's, providing a maximum on-board EPROM capability of 8K bytes. The static RAM area contains sockets for 4K bytes of memory. Four TMS 4045 (2114) are populated and four additional sockets are included. The cycle time of this memory section is 0.667 microseconds. The address map is shown in Figure 2-6 for the board as shipped; an alternate memory map is jumper selectable (detailed in Table 2-4). DMA control lines are also accessible on the bus.

A PROM controls memory address decoding. The RAM is decoded as one bank but the two EPROM pairs are decoded as separate banks, allowing custom placement of EPROM. A custom decoding scheme can be implemented by obtaining a blank SN74S287 PROM, and programming it with the new memory address map.

- EPROM at low addresses, RAM at high
- Main EPROM is TMS 2708
- Main EPROM is TMS 2716
- Expansion EPROM is TMS 2708
- Expansion EPROM is TMS 2716

TABLE 2-4. MEMORY MAP

CONFIGURATION	MEMORY MAP	ALTERNATE MEMORY MAP
RAM, bank 2	$F000_{16}$-$F7FE_{16}$	0000_{16}-$07FE_{16}$
RAM, bank 1	$F800_{16}$-$FFFE_{16}$	0800_{16}-$0FFE_{16}$
EPROM, all TMS 2708*	0000_{16}-$0FFE_{16}$	$F000_{16}$-$FFFE_{16}$
EPROM, all TMS 2716*	0000_{16}-$1FFE_{16}$	$E000_{16}$-$FFFE_{16}$

INTERRUPTS AND TIMERS

Fifteen maskable interrupts plus the reset and load trap vectors are implemented. Table 2-5 shows the implementation. The TMS 9901 handles all 15 external interrupts which can be generated from either the bus connector of the I/O bus. The TMS 9901 enables each level to be individually maskable under program control. Additionally, level 3 can be programmed to use the interval timer in the TMS 9901. Interrupts at level 4 at the main TMS 9902 or level 5 at the auxiliary TMS 9902 can be generated by an interval timer or by three other serial interface conditions (see the TMS 9902

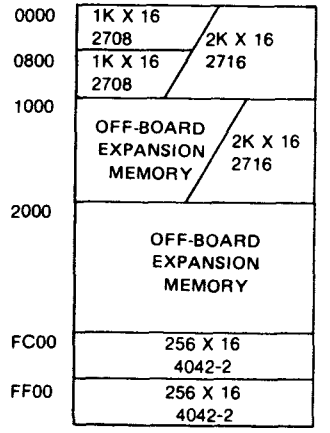


FIGURE 2-6. MEMORY ADDRESS MAP

Data Manual). Three programmable timers, therefore, are available on board. Interrupt 6 may be triggered on either a positive or negative transition, or level triggered (active low). All other interrupts are active low.

TABLE 2-5. INTERRUPTS

INTERRUPT	LEVEL	VECTOR	DESCRIPTION
PRES	0	0000_{16}-0002_{16}	Unmaskable, active low
RESTART	LOAD	$FFFC_{16}$-$FFFE_{16}$	Unmaskable, active low. May be activated by software (LREX)
INT1-INT5	1-5	0004_{16}-0016_{16}	Maskable, dedicated, active low.
INT6	6	0018_{16}-$001A_{16}$	Maskable, dedicated (+) or (-) edge detect or active low.
INT7-INT15	7-15	$001C_{16}$-$003E_{16}$	Maskable, active low. May be programmed as interrupt, input, or output.

I/O

The serial I/O and the parallel I/O are handled over the dedicated I/O bus of the TMS 9900, the communications register unit (CRU). Table 2-6 lists the address assignments within the dedicated 4K CRU address space. The CRU consists of 4096 output bits and 4096 input bits. Each bit is separately addressable. Five instructions enable the programmer to perform both single and multibit CRU operations.

The two TMS 9902's act as the controllers for the two asynchronous serial interfaces. The character length, baud rate (75 to 38,400), parity and stop bits are programmable. Port A is compatible with the serial I/O port on the TM 990/100M microcomputer; port A supports EIA compatible terminals as well as 20 mA neutral current loop teletypes. Port A also supports TI's TM 990/301 Microterminal. A version of the TM 990/101 supports a differential line driver-receiver communications interface in place of the TTY interface; this multidrop interface supports 9600 baud serial communications at distances of up to 10,000 ft. on shielded twisted pairs. Serial Port B supports communications with EIA compatible terminals as well as 103- and 202- series modems, using an optional modem cable. Between the two serial ports, then, a total of four interface types are supported:

- EIA (port A or port B)
- 20 mA neutral current loop TTY (port A only)
- Private wire differential line driver/receiver (port A only)
- Series 103 or 202 modems (port B only)

The TM 990/101M board is delivered complete with two 25-pin RS-232 type female connectors, and is jumper selectable to support EIA or TTY operation. The differential line driver (multidrop) is normally unpopulated (see Options). Also, the TMS 9903 synchronous communications controller can be utilized on port B since the TMS 9902/9903 are socket compatible.

The parallel I/O is handled by the TMS 9901; 16 parallel lines are all interfaced to the top edge connector which has 40 pins on 0.100 inch centers.

Additionally, nine parallel lines are interfaced to the bus connectors. The programmable features of the TMS 9901 permit configuring these lines as I/O lines or interrupts (refer to the TMS 9901 Data Manual). All I/O lines are equipped with pullup resistors.

TIBUG

The TIBUG monitor TM 990/401-3 is normally supplied preprogrammed in the populated TMS 2708 EPROM's (see OPTIONS). Its operation is described in the user's manual or the TM 990 series literature.

OPTIONS

There are four models of the TM 990/101M. Model characteristics are listed in Table 2-7. Other software or accessories, such as the Line-By-Line Assembler, microterminal, memory boards, etc., may be ordered under separate part numbers.

TABLE 2-6. CRU ADDRESS MAP

SOFTWARE BASE ADDRESS		FUNCTION
00_{16}		LED
20_{16}	24_{16}	ID Switch (DIP)
40_{16}	$5F_{16}$	Main Serial I/O Port (TMS 9902)
80_{16}	$9F_{16}$	On-Board 16 I/O Parallel Interface, Interrupt Status Register, Interrupt Mask Register, and Interval Timer (TMS 9901)
$A6_{16}$		INT6 Reset
$C0_{16}$	DF_{16}	Auxiliary Serial I/O Port (TMS 9902)
01_{16}	$1F_{16}$	
28_{16}	$3F_{16}$	
60_{16}	$7F_{16}$	Reserved for On-Card
$A0_{16}$	$A5_{16}$	Expansion
$A6_{16}$	BF_{16}	
$F0_{16}$	FF_{16}	
100_{16}	FFF_{16}	Off-Board CRU

TABLE 2-7. TM990/101M CONFIGURATIONS

TM 990/101M DASH NO	EPROM* POPULATED	EPROM* PROGRAM	RAM*	PORT A OPTION
-1	2 2708 (1K x 16)	TIBUG monitor	4 2114 (1K x 16)	TTY/EIA
-2	2 2716 (2K x 16)	Blank	4 2114 (1K x 16)	Multidrop
-3	4 2716 (4K x 16)	Blank	8 2114 (2K x 16)	TTY/EIA
-10	4 2716 (4K x 16)	POWER BASIC	4 2114 (1K x 16)	TTY/EIA

*TM 990/101M memory is fully socketed for easy expansion

SPECIFICATIONS

CPU: TMS 9900
Instruction Set -- 69 instructions
8, 16, or 32 bit operation
3 MHz System Clock, Crystal Stabilized

Interrupts: 17 levels -- 15 may be external

Interval Timers: Three (one in the TMS 9901 and two in the two TMS 9902's). Can be programmed to cause interrupts at countdown (interrupts 3, 4, and 5).

	Resolution	Maximum Interval
TMS 9901	21.3 usec	349 msec
TMS 9902	64 usec	16.32 msec

Memory: 16-bit word configuration. On-board configurations are shown in Table 2-8; off-board expansion to 64K bytes. Cycle time is 667 nsec (no wait), 1000 nsec (one wait state, EPROM only). TM 990/101M microcomputers are supplied with memory requiring no wait states.

I/O: Parallel -- 16 bits expandable to 4096
Serial -- Two Asynchronous Controllers, TMS 9902's
5-8 bit character,
Programmable data rate, stop bits, parity
Break characters generation,
Framing, parity, and overrun errors detected
75 to 38400 baud, software programmable

Software: TIBUG monitor self contained in EPROM

TABLE 2-8. MATING CONNECTORS

INTERFACE	NO OF PINS	CENTERS (INCH)	MATING CONNECTOR
Chassis	100	0.125	TI H321150 Viking 3VH50/1CN5
Parallel I/O	40	0.100	TI H311120 Viking 3VH20/1JN5 3M 3464-0000
Serial I/O	25	N/A	ITT DB-25P Cannon DB-25P

TABLE 2-9. POWER REQUIREMENTS

	1K EPROM (2708)	2K EPROM (2708)
Vdd +12V ±3%	0.3A	0.4A
Vcc +5V ±3%	1.6A	1.8A
Vaa -12V ±3%	0.2A	0.3A

Operating Temperature Range:

0 deg C to 70 deg C

Physical Characteristics:

Width:	11 inches (279.4 mm)
Height:	7½ inches (190.5 mm)
Depth:	½ inches (12.7 mm)
Shipping Weight	3 pounds (1136 Kg)

Interfaces:

Chassis: All TTL compatible

Parallel I/O: All TTL compatible (TMS 9901 driven)

High level input voltage	2V Min
Low level input voltage	0.8V Max
Absolute maximum input voltage	-0.3V to 10V
Input current	-1 mA @ 0.3V
High level output voltage	2.4V Min @ -100 uA
Low level output voltage	0.4V Min @ 3.2 mA

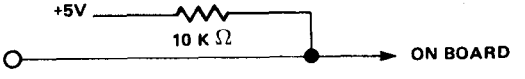
Serial I/O: Port A - RS-232-C/20 mA current loop or RS-232-C/Multidrop
Port B - RS-232-C terminal, or modem with optional cable

Interrupts: All TTL compatible

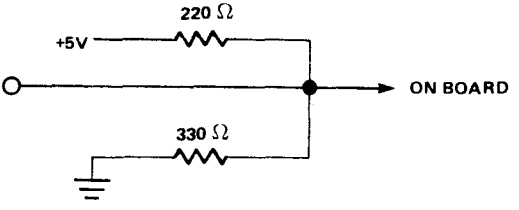
High level input voltage	2V Min
Low level input voltage	0.8V Max
Absolute maximum input voltage	-0.3V to 10V
Input current	-1mA @ 0.3V

Bus Drivers: All bus drivers sink 24 mA at 0.8 V maximum

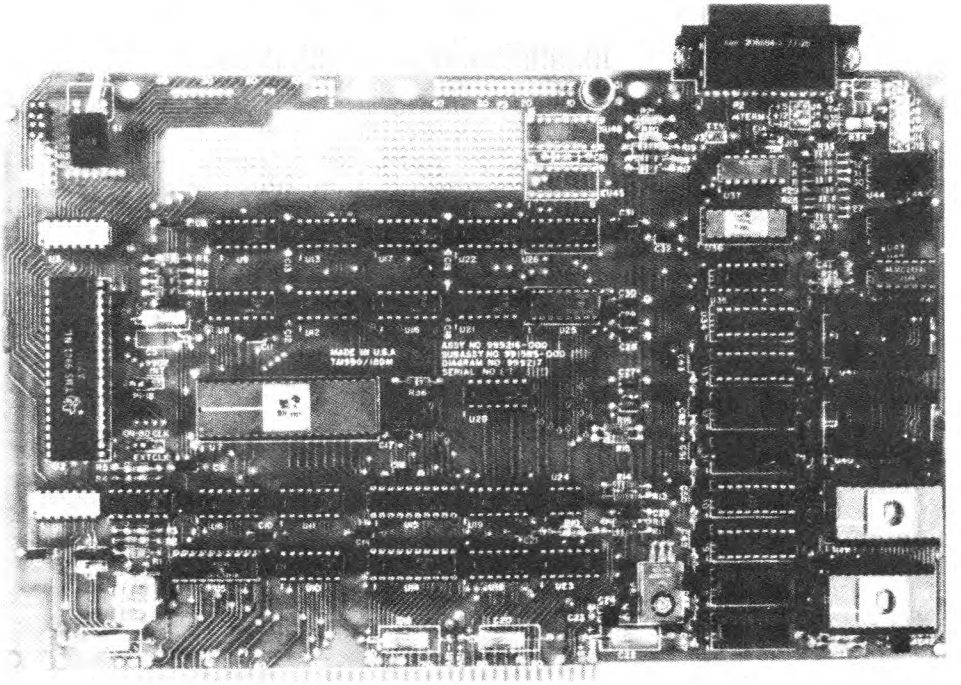
I/O and Interrupt Terminators:



Terminators on READY.B and HOLD.B inputs:



2.5.3 TM 990/180M MICROCOMPUTER MODULE



The TM 990/180M is an assembled, tested microcomputer module utilizing the NMOS 16-bit TMS 9980 microprocessor as its CPU. The TMS 9980 utilizes an eight bit data bus which may be the most cost effective solution for smaller byte-dedicated operations. With RAM and ROM/EPROM included on board as well as programmable serial and parallel I/O, the TM 990/180M is a powerful single-board microcomputer. Since all address, data, and control lines are brought to the board connectors, the board can be expanded to use the entire capabilities of the 9980.

FEATURES

- TMS 9980 16-bit CPU
- 512 bytes of 4042-2 (2111-1) Static RAM, expandable to 1K bytes
- 2K bytes of 2708 EPROM, expandable to 4K bytes
- TMS 9901 programmable system interface
- TMS 9902 asynchronous communications controller
- EIA or TTY terminal interface option
- Prototyping area for customer applications
- Designed to fit the TM 990/510 chassis
- Fully expandable bus structure
- TIBUG operating monitor

OPERATION

The TM 990/180M microcomputer module is a software compatible member of the TMS 9900/990 family. The 9980 is used as a CPU to provide 16 bits of processing power with a minicomputer instruction set which includes multiply and divide. The TM 990/180M module is designed for 2.5 MHz operation, utilizing the full six levels of prioritized interrupts and the advanced memory-to-memory architecture of the TMS 9980. Additionally, the bus structures are set up to take advantage of the full 16K byte memory addressing capability of the 9980 and the nonmultiplexed memory, I/O and interrupt busses. The bus structure is compatible with the TM 990/310 board.

MEMORY

The on-board memory includes both an EPROM/ROM section and a staic RAM section. Four sockets are available for TMS 2708 EPROM or TMS 4700 ROM operation. The assembled price includes two TMS 2708's or 2K bytes. The static RAM area consists of four 256 byte banks of memory. Four TMS 4042-2 (2111-1) are populated, and four more sockets are included. The cycle time of this memory section is 1.33 microseconds. The memory address map is shown in Figure 2-7.

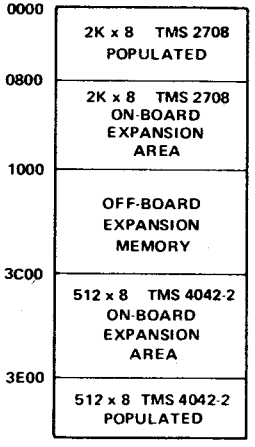


FIGURE 2-7. MEMORY ADDRESS MAP

INTERRUPTS AND TIMERS

Four maskable interrupts plus the reset and load trap vectors are implemented. Table 2-10 shows the implementation. The TMS 9901 handles all four external interrupts which can be generated from either the bus conector or the I/O bus. The TMS 9901 enables each level to be individually maskable under program control. Additionally, level 3 can be programmed to use the interval timer in the TMS 9901. Level 4 can be generated as an interrupt from the TMS 9902. One of the functions that will cause this interrupt is the interval timer. Two programmable timers, therefore, are available on board.

TABLE 2-10. TMS 9980 INTERRUPTS

LEVEL FROM TMS 9901	TRAP VECTOR LOCATION	FUNCTION
1	0000_{16}	Reset pushbutton or PRES from the chassis backplane connector
2	$3FFC_{16}$	Software (LREX) or RESTART from the chassis backplane connector
3	0004_{16}	Real Time Clock (TMS 9901) or external device
4	0008_{16}	Serial interface (TMS 9902) or external device
5	$000C_{16}$	External device
6	0010_{16}	External device

INPUT/OUTPUT

The serial I/O and the parallel I/O are handled over the dedicated I/O bus of the TMS 9980 or the communications register unit (CRU). Table 2-11 lists the address assignments within the dedicated 2048 bit CRU address space. The TMS 9902 acts as the controller for this asynchronous serial interface. The character length, baud rate (75 to 38,400) parity and stop bits are programmable. Three optional types of interface are supported:

- EIA
- 20 mA neutral current loop TTY
- Private wire differential line driver/receiver.

TABLE 2-11. CRU ADDRESS MAP

SOFTWARE BASE ADDRESS		FUNCTION
00_{16}	$3F_{16}$	Reserved for on-board CRU expansion
40_{16}	$5F_{16}$	On-board serial I/O (TMS 9902)
60_{16}	$7F_{16}$	Reserved for on-board CRU expansion
80_{16}	$9F_{16}$	On-board parallel I/O interface interrupt status register, interrupt mask register, interval timer (TMS 9901)
$A0_{16}$	FF_{16}	Reserved for on-board CRU expansion
100_{16}	$3FF_{16}$	Off-board CRU

The TM 990/180M board is delivered complete with a 25-pin RS-232 type female connector, and is jumper selectable to support EIA or TTY operation. Also, the TMS 9903 synchronous communications controller can be utilized, since the TMS 9902/9903 are socket compatible.

The parallel I/O is handled by the TMS 9901; 16 parallel lines are all interfaced to the top edge connector which has 40 pins on 0.100 inch centers. Additionally, eight parallel lines are interfaced to the bus connectors. The programmable features of the TMS 9901 permit these lines to be set up as I/O lines or interrupts (refer to the TMS 9901 Data Manual). All I/O lines are equipped with pullup resistors.

TIBUG

The TIBUG monitor is supplied preprogrammed in TMS 2708 EPROM's or mask ROM. Its operation is described in the TIBUG user's manual or the TM 990 series literature.

PROTOTYPING AREA

The prototyping area is large enough to accommodate one 40-pin DIP (0.6 inch centers) plus four 16-pin DIP's (0.3 inch centers).

SPECIFICATIONS

CPU: TMS 9980
Instruction Set--69 instructions
8, 16, or 32 bit operation
2.5 MHz System Clock

Interrupts: 6 levels--4 may be external

Interval Timers: Two

	Resolution	Maximum Interval
TMS 9901	25.6 usec	414 msec
TMS 9902	76.8 usec	19.7 msec

Memory: 8-bit byte configuration, on board EPROM/ROM, on board RAM, 256 bytes expandable to 1K bytes, off board expansion to full 16K bytes

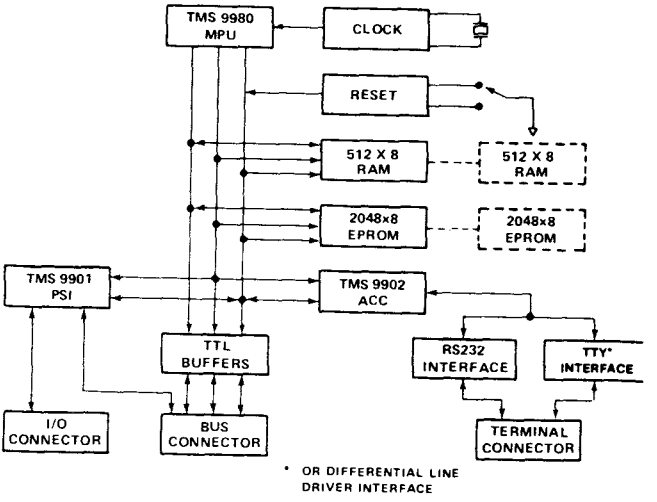


FIGURE 2-8. TM 990/180M BLOCK DIAGRAM

I/O: Parallel--16 bits expandable to 2048
Serial--Asynchronous (TMS 9902)
5-8 bit character,
Programmable data rate, stop bits, parity,
Break characters generation,
Framing, parity, and overrun errors detected,
75 to 38400 baud, software programmable.

Interfaces:
Data and Address--Three-state TTL compatible, buffered output
Control--TTL compatible
Parallel I/O and Interrupts--TTL compatible
Serial I/O--RS-232, 20 mA current loop TTY

Expansion Prototyping Area:
May contain one 40-pin DIP plus up to four 16-pin DIP's

Software:
TIBUG monitor self contained in EPROM (TM 990/401-2)

Mating Connectors:

Bus	100 pin, 0.125 in. cc	TI	H321150 (wire wrap)
		TI	H322150 (solder tail)
Parallel I/O	40 pin, 0.100 in. cc	TI	H312120 (wire wrap)
		3M	3463-0001 (no ears)
		Viking	3VH20/1JN5 (pierced tail)
Serial I/O	25 pin, male	Cinch	DB-25P

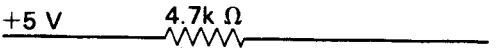
Power Requirements:
+5V $\pm$3% @ 1.3A
+12V $\pm$3% @ 0.2A
-12V $\pm$3% @ 0.1A

Operating Temperature Range:
0 deg C to 70 deg C

Physical Characteristics:

Width:	11 inches
Height:	7½ inches
Board Thickness	0.062 inch

I/O and Interrupt Terminations:

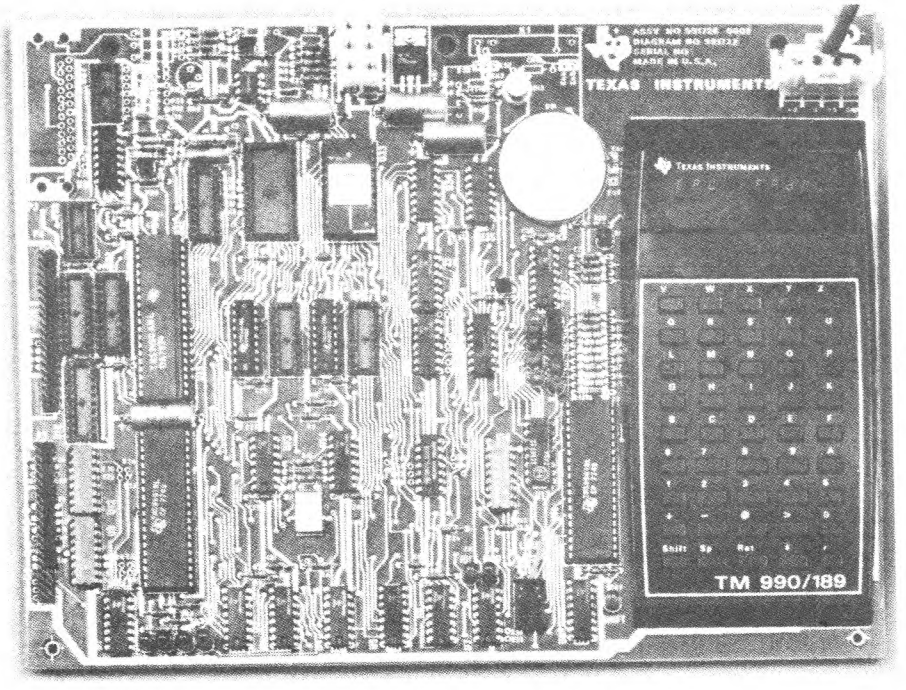


interrupt inputs
and parallel I/O lines

Ordering Information:

TM 990/180M-1	TMS 9980A CPU board with TIBUG monitor and EIA or TTY serial I/O jumper option

2.5.4 TM 990/189 UNIVERSITY BOARD



The TM 990/189 is a self-contained, single-board microcomputer system. It is intended for use as a learning aid in the instruction of microcomputer fundamentals, machine and assembly language programming, and microcomputer interfacing. It also demonstrates TMS 9900 family applications and advantages. Figure 2-9 is a system block diagram of the TM 990/189.

FEATURES

- TMS 9980A (MP9529) 16-bit CPU
- 1K bytes of TMS 4014 (4045) Static RAM, expandable to 2K bytes
- 4K bytes of TMS 4732 ROM, expandable to 6K bytes EPROM/ROM
- UNIBUG operating monitor and resident symbolic assembler
- Memory and I/O buses user expandable
- Audio cassette interface
- TMS 9901 programmable system interface
- TMS 9902 synchronous communications controller (user option)
- 45-key alphanumeric keyboard
- Ten-digit, seven-segment L.E.D. type, pseudo alphanumeric display
- Visual and acoustic indicators

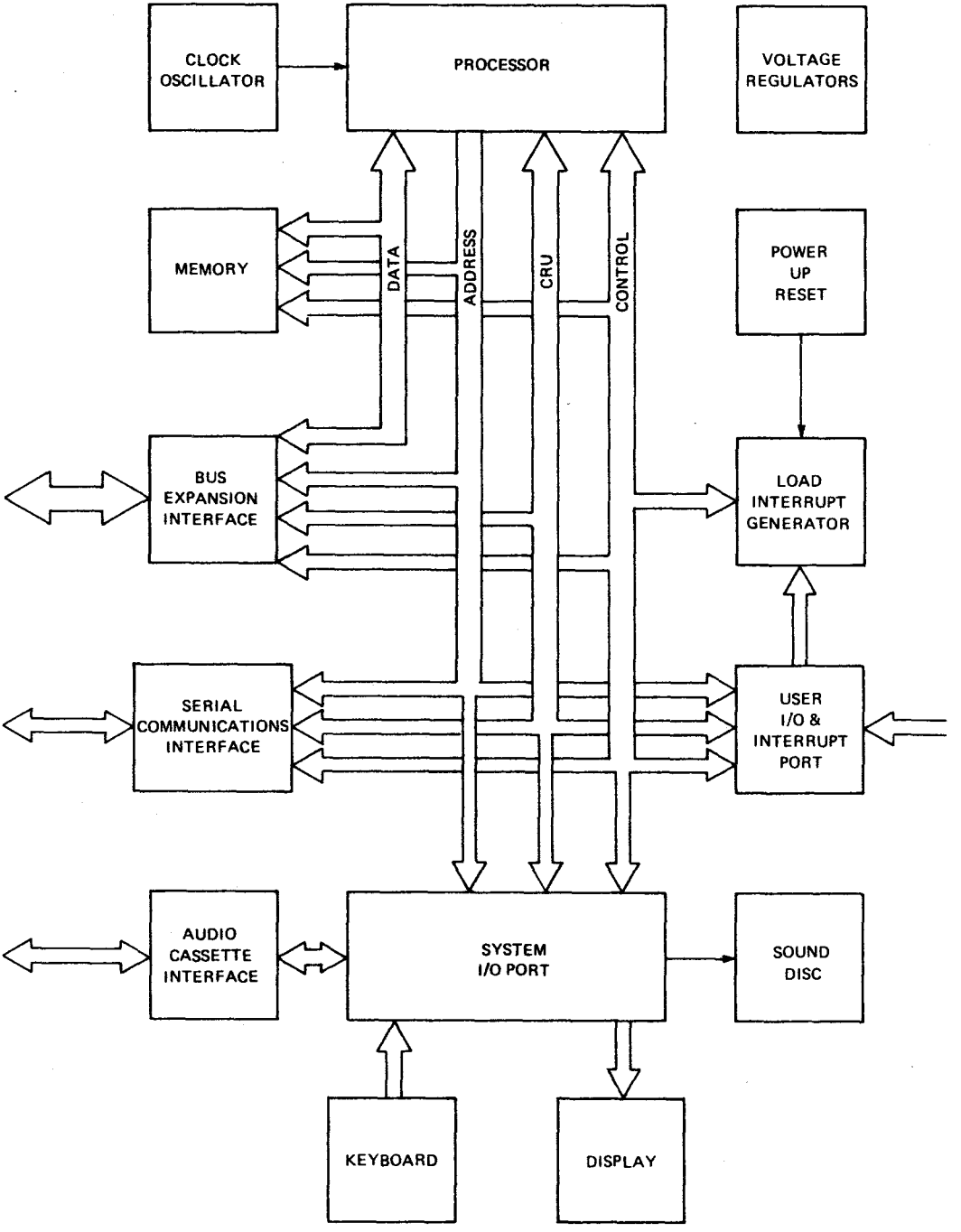


FIGURE 2-9. TM 990/189 BLOCK DIAGRAM

OPERATION

The TM 990/189 University Board is software compatible with the TMS 9900/990 family. A TMS 9980 is used as the CPU to provide 16 bits of processing power to an 8-bit data bus. An instruction set with the capabilities of full minicomputers and identical to that of the TMS 9900 is featured. The TM 990/189 is designed for 2 MHz operation, utilizing the full six levels of prioritized interrupts and the advanced memory-to-memory architecture of the TMS 9980. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility.

MEMORY

The on-board memory includes both an EPROM/ROM section and a static RAM section. Two sockets are avilable for TMS 2708, TMS 2716, TMS 2532 EPROM or TMS 4732 ROM operation. By performing a simple board modification, the on-board EPROM may be expanded to 6144 bytes via 1 TMS 2532 and 1 TMS 2716. The static RAM area is populated with 1K bytes of socketed static RAM and contains sockets for an additional 1K bytes of RAM. Memory is configured as shown in the address map in Figure 2-10. DMA control lines are also accessible on the bus.

The address space is divided into four 4K byte sections each of which is further subdivided into 1K byte blocks. Off-board memory expansion capability is provided through the bus expansion interface. As indicated in Figure 2-10, off-board memory expansion is from 1000_{16} to $2FFF_{16}$ which allows a full 16K byte memory space.

INTERRUPTS AND TIMERS

Four maskable prioritized interrupts plus the reset and load trap vectors are handled by the TMS 9901. The TMS 9901 enables each level except reset and load to be individually maskable under program control. Additionally two programmable timers are on board. Interrupt 1 and interrupt 4 can be programmed to use the interval timer in the TMS 9901. Interrupt 3 can be generated as a jumper selectable interrupt from the interval timer in the optional TMS 9902. Figure 2-12 shows the interrupt decoding and trap locations.

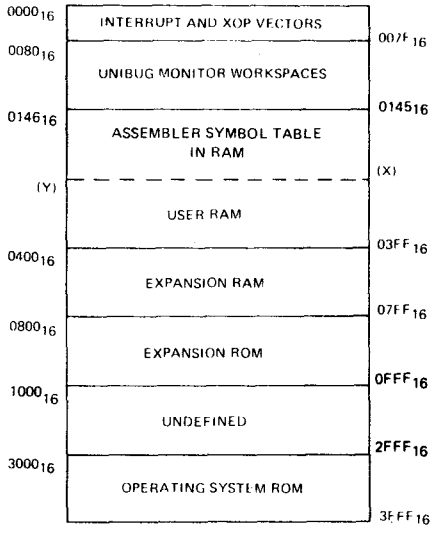


FIGURE 2-10. SYSTEM MEMORY MAP

TABLE 2-12. INTERRUPT DECODING

INTERRUPT CODE INTO - INT 2	FUNCTION	VECTOR ADDRESS
000_2	RESET	0000_{16}
001_2	RESET	0000_{16}
010_2	LOAD	$3FFC_{16}$
011_2	Interrupt 1	0004_{16}
100_2	Interrupt 2	$000B_{16}$
101_2	Interrupt 3	$000C_{16}$
110_2	Interrupt 4	0010_{16}

INPUT/OUTPUT

The serial I/O and the parallel I/O are handled over the dedicated I/O bus of the TMS 9980 or the Communications Register Unit (CRU). Table 2-13 lists the address assignments within the dedicated 2048 bit CRU address space. The user supplied TMS 9902 acts as the controller for this asynchronous serial interface. Character length, baud rate (75 to 38,400) parity and stop bits are programmable. Two jumper selectable types of interface are supported: EIA and 20 mA neutral current loop TTY.

TABLE 2-13. CRU ADDRESS MAP

SOFTWARE BASE ADDRESS	FUNCTION
000_{16} to $03E_{16}$	User I/O - P5 (TMS 9901 at U10)
040_{16} to $3FE_{16}$	Not Defined
400_{16} to $43E_{16}$	System I/O (TMS 9901 at U11)
440_{16} to $7FE_{16}$	Not Defined
800_{16} to $83E_{16}$	Communication I/O - P3 (TMS 9902)
840_{16} to BFE_{16}	Not Defined
$C00_{16}$ to $C3E_{16}$	External I/O - P4
$C40_{16}$ to FFE_{16}	External I/O Expansion

Parallel I/O handled by the TMS 9901 features 16 parallel lines brought out directly to P5. Additionally, the four low order lines are connected to LED drivers for CR1 through CR4 which illuminate in response to a logic one input.

UNIBUG

The UNIBUG monitor is supplied preprogrammed in TMS 4732 ROM. Fifteen commands and seven subroutines are provided by UNIBUG. Memory inspect/change and CRU inspect/change allow the user to effectively look at memory and CRU addresses. Load and dump commands allow the user to recall and store programs from audio cassette, or paper tape/digital cassette via user supplied data terminal. An execute command is provided to execute an entire program or execute to a breakpoint address where the program is halted. There is a status register inspect/change command along with individual program counter, workspace register and workspace pointer inspect/change commands. The New Line Request command causes a carriage return, line feed and new line request

if a terminal is used. When the keyboard is used, a "?" prompt is displayed. Seven utility subroutines allow the user to read and write ASCII or hexadecimal characters to and from a terminal. UNIBUG displays "ERR" on the board when an invalid command is entered or when an invalid termination character is detected.

The most powerful feature of the UNIBUG monitor is the symbolic assembler. By interpreting assembly language source statements into object code, the TM 990/189 symbolic assembler processes all 69 instructions of the TMS 9980. In addition, the pseudo instruction NOP assembles as "JMP $+2". Six assembler directives are also featured: AORG, BSS, DATA, END, EQU, TEXT. Comments as well as two character labels can be used with this assembler.

USER OPTIONS

Users wishing to expand the capability of their TM990/189 are encouraged to make use of the numerous user options already provided on the board. On-board RAM may be expanded to 2K bytes by installing 2 TMS 4014's. 1K bytes of EPROM may be added by installing a TMS 2708. 2K bytes of EPROM may be added by a simple board modification and by installing a TMS 2716. The UNIBUG monitor may be substituted by a 4K byte EPROM by removing the system ROM and replacing it with a TMS 2532. While sacrificing the use of the UNIBUG monitor and assembler, this substitution provides the capability for installing resident user programs of up to 4K bytes on the board. This capability may be expanded to 6K bytes if the TMS 2716 has been installed.

The capability to perform serial communications with devices meeting the requirements of EIA RS-232-C may be added to the board by installing 2 networks, 2 resistors and a connector as indicated in the user's manual. Devices having a 20 mA current loop interface, such as a TTY, may be featured by installing the serial communicaion interface as indicated in the user's manual.

Control of cassette deck motors may be performed by the TM 990/189 through the installation of an on-board relay and transient protection diode. Jumper options make available an open-collector drive signal so that the user may install an off-board cassette deck motor relay. Additional user options include expanding the CRU off-board, installing interrupt driven serial I/O and increasing the clock frequency. Detailed instructions are included in the user's manual.

SPECIFICATIONS

CPU: TMS 9980 - MP 9529
Instruction Set--69 instructions
8, 16, or 32 bit operation
2 MHz System Clock

Interrupts: 6 levels--4 maskable, 2 non-maskable

Interval Timers: TMS 9901, TMS 9902 (user installed option)

Memory: 8-bit byte configuration, on-board EPROM/ROM, on-board RAM, 1K bytes expandable to 2K bytes; total addressable memory with off-board expansion is 16K bytes

I/O: Parallel--16 bits expandable to 2048 bits
Serial--Asynchronous (TMS 9902)
5-8 bit character,
Programmable data rates, stop bits, parity,
Break characters generation,
Framing, parity, and overrun errors detected,
75 to 38400 baud, software programmable

Note: UNIBUG only supports 110 & 300 baud.

Interfaces:
Data and Address--Three-state TTL compatible, buffered output
Control--TTL compatible, buffered output
Parallel I/O and Interrupts--TTL compatible (TMS 9901 driven)
Serial I/O--EIA RS-232, 20 mA current loop TTY

Software: UNIBUG monitor self contained in ROM (TMS 4732)

Power Requirements (maximum):
+5V $\pm$ 5% @ 1.787 A
+12V $\pm$ 5% @ 214 mA
-12V $\pm$ 3% @ 155 mA

Operating Temperature Range:
10 deg C to 50 deg C

Physical Characteristics:

Width:	11 inches
Height:	8.15 inches
Board Thickness:	0.062 inch
Board Height:	1 inch

Ordering Information:

TM 990/189	University Board containing TMS 9980 (MP9529) CPU, UNIBUG monitor in TMS 4732 ROM
TM 990/519	Companion Power Supply for TM 990/189

2.6 CPU COMPATIBILITY

Table 2-14 indicates the compatibility of TM 990 modules with three of the CPU modules. This is intended to be a guide so that the user will not mistakenly order modules that are incompatible.

TABLE 2-14. CPU COMPATIBILITY

	100M	101M	180M		100M	101M	180M
TM 990/201	YES	YES	NO	TM 990/504	YES	YES	YES
TM 990/203	YES	YES	NO	TM 990/505	YES	YES	YES
TM 990/206	YES	YES	NO	TM 990/506	NO	YES	NO
TM 990/301	YES	YES	YES	TM 990/507	YES	YES	YES
TM 990/302	YES	YES	NO	TM 990/508[3]	NO	NO	NO
TM 990/305	YES	YES	YES[1]	TM 990/509[2]	NO	NO	NO
TM 990/310	YES	YES	YES	TM 990/510	YES	YES	YES
TM 990/401	YES	YES	NO	TM 990/520	YES	YES	YES
TM 990/402	YES	YES	YES[4]	TM 990/1240R	YES	YES	NO
TM 990/430	YES	YES	NO	TM 990/1241S	YES	YES	NO
TM 990/450	YES	YES	NO	TM 990/1241R	YES	YES	NO
TM 990/451	YES	YES	NO	TM 990/1243	YES	YES	NO
TM 990/452	YES	YES	NO	TM 990/1001	YES	YES	YES
TM 990/501	YES	YES	YES	TM 990/1002	YES	YES	NO
TM 990/502	YES	YES	YES	TM 990/2001	YES	YES	NO
TM 990/503	YES	YES	YES	TM 990/3001	YES	YES	NO

1. I/O only; memory will not function
2. 509 cable for 305
3. Audio Cassette Cable for 302
4. 402-2 version must be ordered

SECTION 3

MEMORY EXPANSION MODULES (200 SERIES)

3.1 GENERAL

A variety of memory expansion modules is available to support the TM 990/10X CPU modules. These assembled, tested modules are bus compatible, TTL-compatible, and designed to fit either the TM 990/510 or TM 990/520 card cage.

The TM 990/201 module contains both static RAM and EPROM memory, expandable to a maximum configuration of 16K bytes of RAM and 32K bytes of EPROM. The TM 990/206 contains static RAM memory devices up to a maximum configuration of 16K bytes. The TM 990/203 contains dynamic RAM memory devices: it is expandable to 64K bytes.

The memory map configuration is switch selectable on the TM 990/20X modules. This switch is used to map memory located on the memory expansion board into the available CPU module address space. The operational procedure for the memory expansion boards will be described in the following data sheets.

3.2 SUMMARY OF KEY PARAMETERS

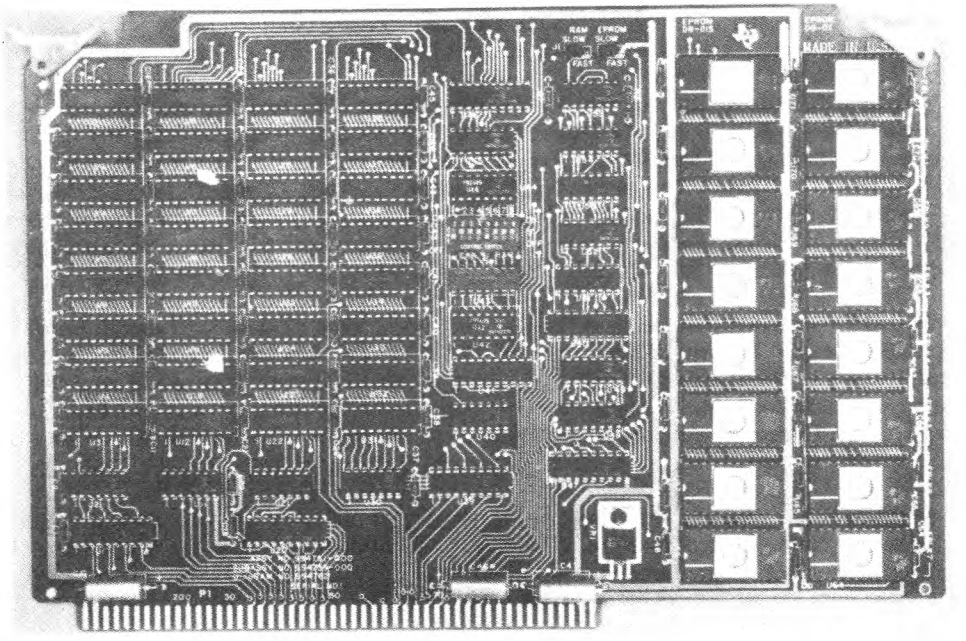
Table 3-1 provides a listing of the key parameters of the TM 990/20X memory expansion modules. Section 3.3 contains Data Sheets for these modules.

TABLE 3-1. SUMMARY OF KEY PARAMETERS

Product	Memory Type	Memory Size (Bytes)	Power Requirements +5V	+12V	-12V
TM 990/201-41	EPROM/Static RAM	8K EPROM, 4K RAM	1.0A	50mA	160mA
TM 990/201-42	EPROM/Static RAM	16K EPROM, 8K RAM	1.4A	125mA	225mA
TM 990/201-43	EPROM/Static RAM	32K EPROM, 16K RAM	2.2A	225mA	475mA
TM 990/206-41	Static RAM	8K RAM	1.3A	0	0
TM 990/206-42	Static RAM	16K RAM	2.2A	0	0
TM 990/203-41	Dynamic RAM	8K DRAM	3.0A	1.2A	20mA
TM 990/203-42	Dynamic RAM	16K DRAM	2.7A	65mA	15mA
TM 990/203-43	Dynamic RAM	32K DRAM	3.0A	1.2A	20mA

3.3 MEMORY EXPANSION MODULE

DATA SHEETS



The TM 990/201 is an assembled, tested memory expansion board designed for use with TMS 9900-based microcomputer modules such as the TM 990/100M. The TM 990/201 contains both static RAM and EPROM memory, expandable to a maximum configuration of 16K bytes of RAM and 32K bytes of EPROM. The TM 990/201 does not support the TMS 9980-based TM 990/180M microcomputer.

Features

- Bus-compatible with the TM 990/100M and TM 990/101M microcomputer modules
- 8K bytes TMS 2716 EPROM, expandable to 32K bytes
- 4K bytes TMS 4045 static RAM, expandable to 16K bytes
- 1 microsecond cycle time (3 MHz)
- TTL-compatible interface
- Designed to fit the TM 990/510 and TM 990/520 card cage

DESCRIPTION

The TM 990/201 memory expansion board is a member of Texas Instruments line of OEM computer products which takes advantage of Texas Instruments broad based semiconductor technology to provide economical, computer based solutions for OEM applications. The memory expansion board is contained on a 7½ x 11 inch printed circuit board which is fully compatible with the TM 990 board format.

The TM 990/201 features up to 16K bytes of static RAM and up to 32K bytes of EPROM. The static RAM array is composed of Texas Instruments TMS 4045, 1K x 4 static memory devices. The EPROM array comprises Texas Instruments TMS 2716, 2K x 8 EPROM devices. The static RAM array is arranged into four banks of memory, each 2K x 16. THe EPROM array is likewise arranged into eight banks, each 2K x 16. Both memory arrays are socketed for convenient memory expansion. (The TM 990/201-42 and TM 990/201-43 are fully socketed.)

The TM 990/201 memory controller logic provides the timing and memory mapping functions necessary to interface the TM 990/201 to 16-bit TM 990/10X series microcomputers. The memory map is switch selectable for both the RAM and EPROM arrays. Sixteen convenient memory map configurations are possible for each array, and the maps are configured on 4K byte address boundaries. The map logic also is designed to accommodate customized memory maps.

The TM 990/201-4X family of memory expansion boards is populated with TMS 4045-45 static RAM's and TMS 2716 EPROM's. Both devices offer 450 nsec access time; consequently, each memory cycle to the TM 990/201 is extended one clock cycle by the insertion of a WAIT state. If faster static RAM's are utilized in the RAM array, the WAIT state in RAM memory cycles can be conveniently removed using only a jumper.

OPERATION

This section explains the procedure for setting up the TM 990/201 module for operation with a TM 990/100M microcomputer. Essentially the user needs only to choose the correct memory configuration, insert the board into the chassis, and apply power to set up the system for operation.

The operation of the TM 990/201 memory module should be transparent to the user in that no special signals are required other than those supplied through the backplane of the card cage.

MEMORY ACCESS SPEED

Jumpers J1 and J2 must be set to FAST or SLOW to indicate respectively the access time of the RAM or EPROM memories used. Table 3-2 lists access time and J1/J2 settings.

TABLE 3-2. ACCESS TIME AND J1/J2 SETTINGS

MEMORY ACCESS TIME	J1 (RAM) AND J2 (EPROM) SETTING AT CLOCK RATE	
	3 MHz	4 MHz
450 ns	SLOW	SLOW
300 ns	FAST	SLOW
200 ns	FAST	FAST
150 ns	FAST	FAST

EXAMPLE

This example assumes the following configurations:

1. TM 990/100M microcomputer
   - 4K x 16 EPROM in memory address (M.A.) 0000_{16} to $1FFF_{16}$
   - 2K x 16 RAM in M.A. $FC00_{16}$ to $FFFF_{16}$.
2. TM 990/201-41 expansion board
   - 4K x 16 EPROM
   - 2K x 16 RAM

Figure 3-1 depicts the desired memory map. Note that expansion EPROM resides at address 2000_{16} to $3FFF_{16}$ while expansion RAM on the TM 990/201-41 is to reside in locations $E000_{16}$ to $EFFF_{16}$ of the TM 990/100M address map.

The user must do four things to the TM 990/201-41 prior to interfacing the unit to the microcomputer:

1. Configure the expansion RAM into the TM 990/100M memory map using switch S1 and memory placement on the board.
2. Configure the expansion EPROM into the TM 990/100M memory map using switch S1 and memory placement on the board.
3. Select the wait state for RAM using jumper J1.
4. Select the wait state for EPROM using jumper J2.

In order to configure expansion RAM and ROM into the TM 990/100M memory map, consult Figure 3-2 for switch positions for RAM and Figure 3-3 for switch positions for ROM. Switches 5-8 (RAM) on memory configuration switch S1 should be set to switch code D (OFF-ON-OFF-OFF) and switches 1-4 (ROM) to switch code C (ON-ON-OFF-OFF).

In order to configure the wait state jumpers for RAM and EPROM, the CPU speed and memory access times must be known. The TM 990/100M operates at 3 MHz. The TM 990/201-41 is shipped with TMS 4045-45 RAM's, 450 nsec access time. Thus, place the RAM FAST/SLOW jumper (J1) in the "SLOW" position. The TM 990/201-41 is shipped with TMS 2716 EPROM's which have a 450 nsec access time. Place the EPROM FAST/SLOW jumper (J2) in the "SLOW" position. The jumper positions were obtained from Table 3-2.

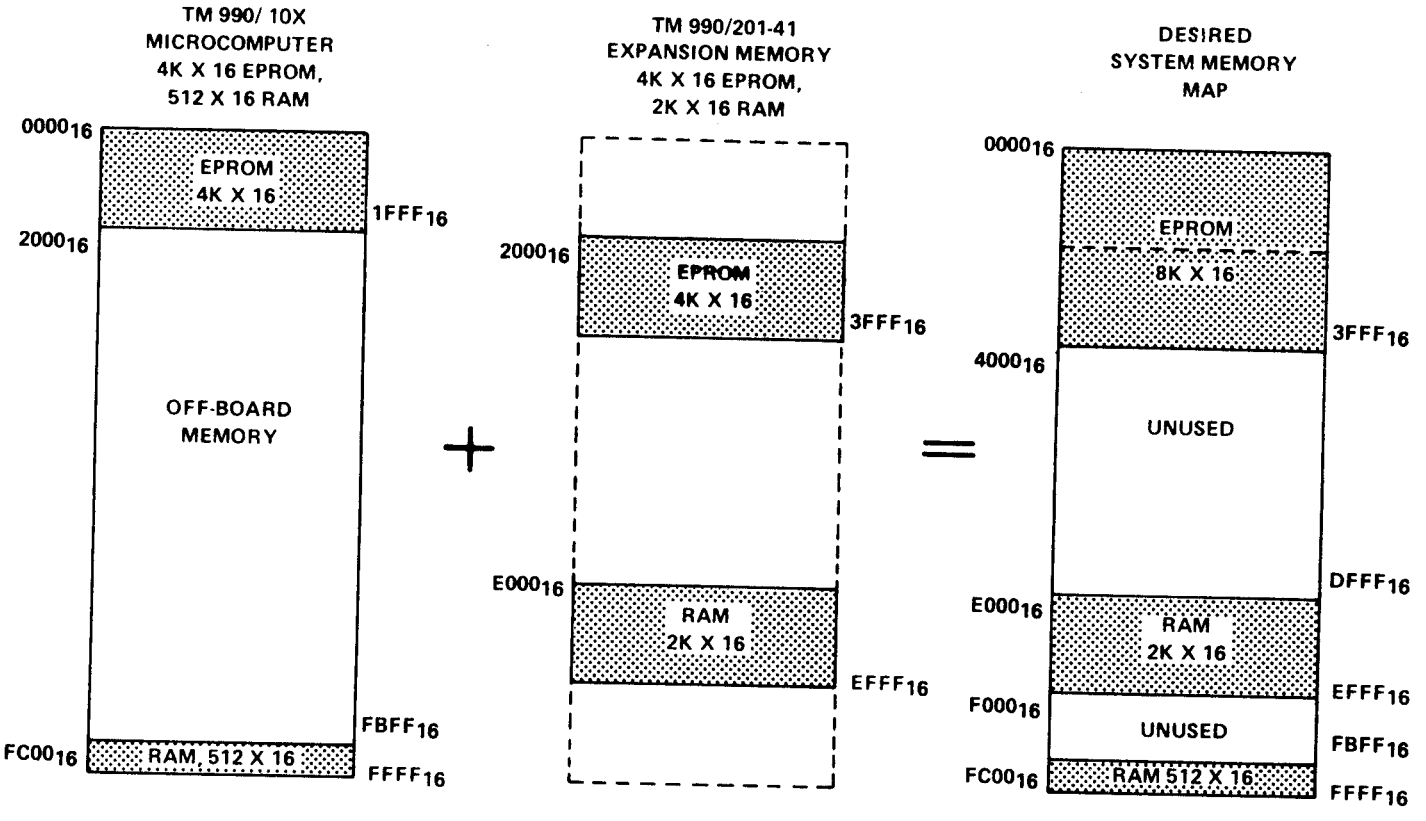


FIGURE 3-1. TM 990/201 MEMORY MAP EXAMPLE

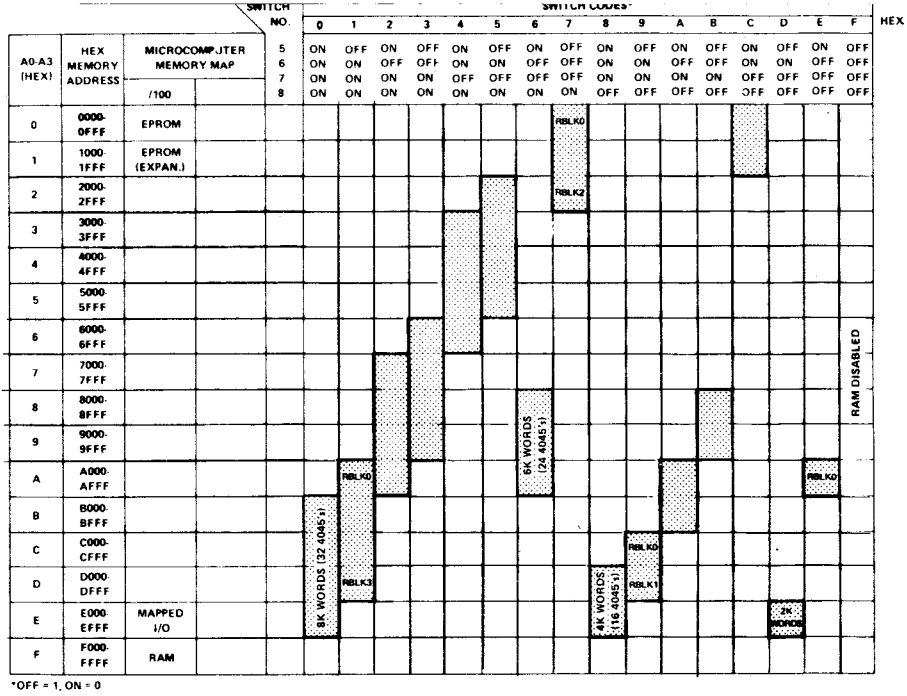


FIGURE 3-2. TM 990/201 RAM DECODE CONFIGURATIONS

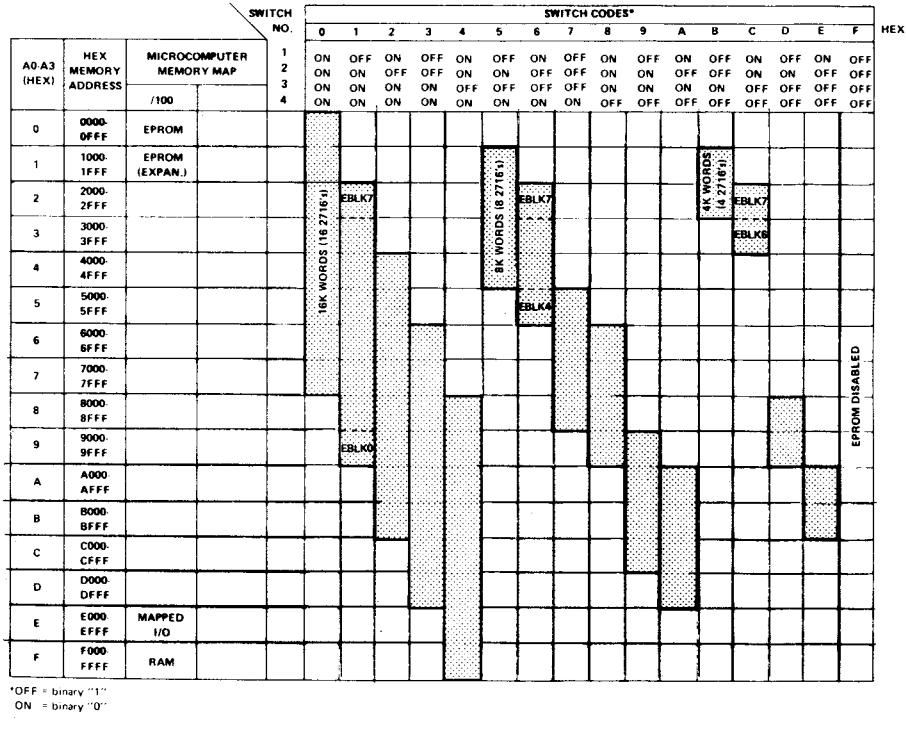


FIGURE 3-3. TM 990/201 EPROM DECODE CONFIGURATIONS

OPTIONS

The TM 990/201 is available in the following three versions:

TABLE 3-3. TM 990/201 OPTIONS

MODEL NO.	MEMORY POPULATED		MEMORY EXPANSION AREA EXTRA SOCKETS PROVIDED	
	EPROM	RAM	EPROM	RAM
TM 990/201-41	4K x 16	2K x 16	4K x 16	2K x 16
TM 990/201-42	8K x 16	4K x 16	8K x 16	4K x 16
TM 990/201-43	16K x 16	8K x 16	---	---

SPECIFICATIONS

Memory Configuration: TMS 4045-45 static RAM 1K x 4, 450 nsec Access Time
TMS 2716 EPROM 2K x 8, 450 nsec Access Time

Power Requirements (Typical):

Model	+5V ±3%	+12V ±3%	-12V ±3%
TM 990/201-41	1.0A	0.16A	0.05A
TM 990/201-42	1.4A	0.225A	0.125A
TM 990/201-43	2.15A	0.475A	0.225A

Cycle Time:

Memory Device Access Time (nsec)	Memory Cycle Time @ 3 MHz (usec)
450	1.0
300	0.667
200	0.667
150	0.667

Bus Interface: Data and Address--Three-State TTL-compatible
Control--TTL-compatible

Mating Connector: 100 Pin, 0.125 in. cc TI H321150 (wire wrap),
TI H322150 (solder tail), or
Viking 3VH50/1CN5 (Pierced tail)

Operating Temperature Range: 0 deg C to 70 deg C

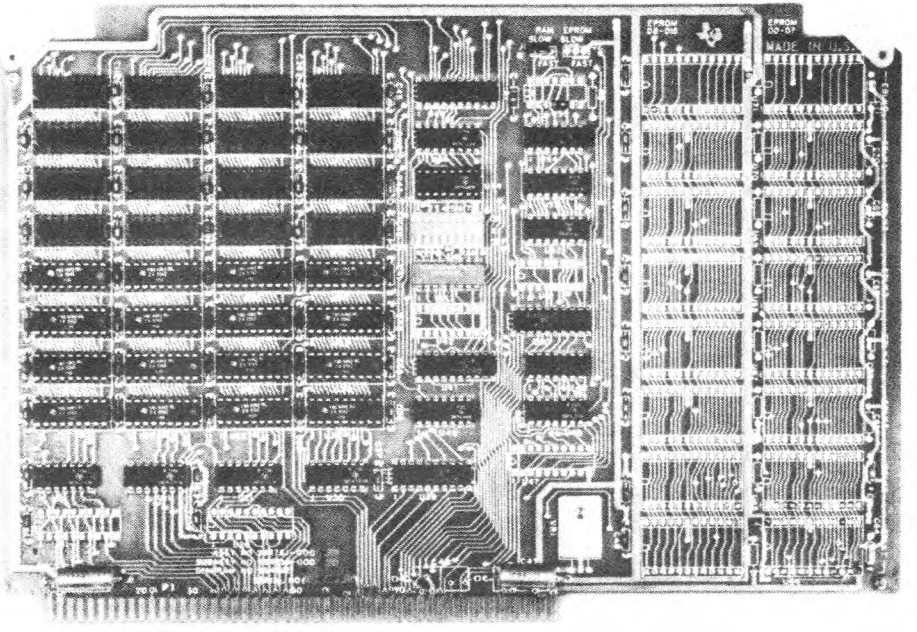
Physical Characteristics:

Width	11 inches
Height	7½ inches
Board Thickness	0.062 inch
Component Height	0.40 inch

ORDERING INFORMATION

TM 990/201-41 8K bytes EPROM, 4K bytes RAM, half socketed
TM 990/201-42 16K bytes EPROM, 8K bytes RAM, fully socketed
TM 990/201-43 32K bytes EPROM, 16K bytes RAM, fully socketed

3.3.2 TM 990/206 EXPANSION MEMORY BOARD



The TM 990/206 is an assembled, tested, RAM expansion memory board designed for use with TMS 9900-based microcomputer modules such as the TM 990/100M. The TM 990/206 contains static RAM memory devices up to a maximum configuration of 16K bytes. The TM 990/206 is similar to the popular TM 990/201 memory board, but only the RAM section is populated. The TM 990/206 does not support the TMS 9980-based TM 990/180M microcomputer.

FEATURES

- Bus compatible with the TM 990/100M microcomputer module
- 8K bytes of TMS 4045 static RAM, expandable to 16K bytes
- 1 usec cycle time (3 MHz)
- TTL-compatible interface
- Designed to fit the TM 990/510 and TM 990/520 card cages

DESCRIPTION

The TM 990/206 expansion memory board is a member of Texas Instruments' line of OEM computer products which take advantage of Texas Instruments' broad based semiconductor technology to provide economical, computer based solutions for OEM applications. The memory expansion board is contained on a 7½ x 11

inch printed circuit board which is fully compatible with the TM 990 board format. The TM 990/206 features up to 16K bytes static RAM. The RAM array is composed of Texas Instruments TMS 4045-45 1K x 4 static memory devices. The array is configured into four banks of memory, each bank consisting of 4K bytes. The RAM array is fully socketed for convenient memory expansion.

The memory controller logic provides the timing and memory mapping funcions necessary to interface the TM 990/206 to 16-bit TM 990/10X series microcomputers. Sixteen convenient, switch selectable, memory map configurations are possible. All maps are configured on 8K byte address boundaries.

The TM 990/206-4X family of memory expansion boards is populated with TMS 4045-45 static RAM's, featuring an access time of 450 nsec. For operation with a TM 990/100M microcomputer, each memory cycle to the TM 990/206 is extended one clock cycle by the insertions of a WAIT state. If faster static RAM's are utilized, the WAIT state can be conveniently removed with a jumper.

OPERATION

Essentially the user needs only to choose the correct memory configuration, insert the board into the chassis, and apply power to set up the system for operation.

The operation of the TM 990/206 memory module should be transparent to the user in that no special signals are required other than those supplied through the backplane of the card cage.

MEMORY ACCESS SPEED

Jumpers J1 and J2 must be set to FAST or SLOW to indicate respectively the access time of the RAM or EPROM memories used. Table 3-4 lists access time and J1/J2 settings.

TABLE 3-4. ACCESS TIME AND J1/J2 SETTINGS

MEMORY ACCESS TIME	J1 (RAM) AND J2 (EPROM) SETTING AT CLOCK RATE	
	3 MHz	4 MHz
450 ns	SLOW	SLOW
300 ns	FAST	SLOW
200 ns	FAST	FAST
150 ns	FAST	FAST

EXAMPLE

This example assumes the following configurations:

1. TM 990/100M CPU Module
   - 4K x 16 EPROM in memory address (M.A.) 0000_{16}
   - 2K x 16 RAM in M.A. $F000_{16}$ to $FFFE_{16}$

2. TM 990/206-41 memory expansion module

   - 4K x 16 RAM

Figure 3-5 depicts the desired memory map. Note that expansion RAM on the TM 990/206-41 is to reside in locations $D000_{16}$ to $EFFE_{16}$ of the TM 990/100M address map.

The user must do two things to the TM 990/206-41 prior to interfacing the unit to the microcomputer:

1. Configure the expansion RAM into the TM 990/100M memory map.

2. Configure the wait state for RAM.

In order to configure the expansion RAM into the TM 990/100M memory map, set switch array S1 to code ON-OFF-OFF-OFF (switch code E in Figure 3-4).

In order to configure the wait state for RAM, the CPU speed and the access time for the slowest memory devices used must be known. The TM 990/100M CPU module operates at 3 MHz. The TM 990/206-41 is shipped with TMS 4045-45 RAM's, these RAM's have 450 nanosecond access time. Table 3-4 indicates that the RAM FAST/SLOW jumper (J1) should be in the "SLOW" position.

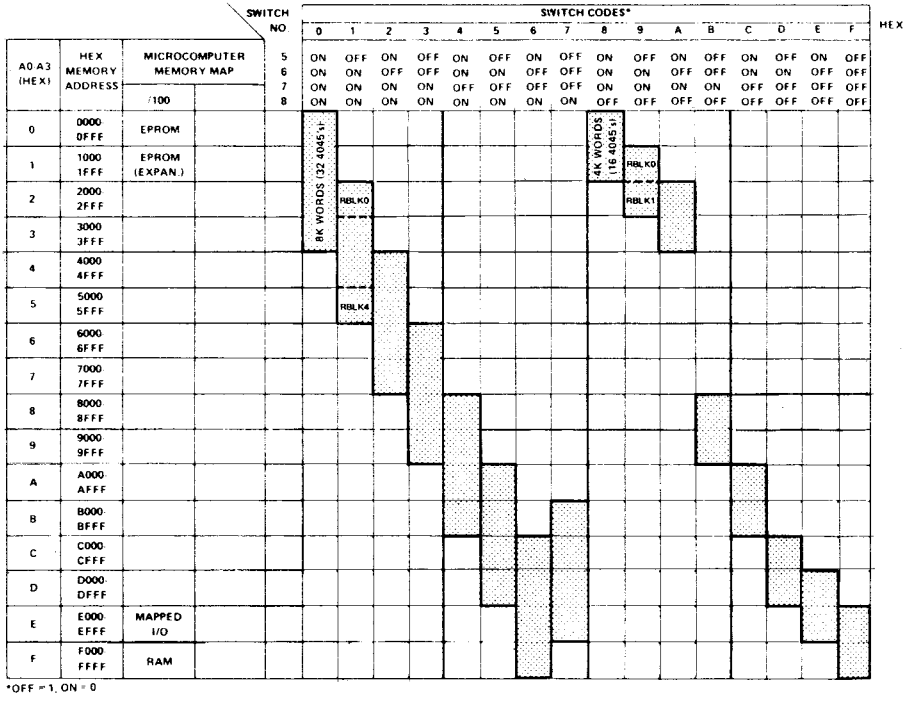


FIGURE 3-4. TM 990/206-4X RAM DECODE CONFIGURATION

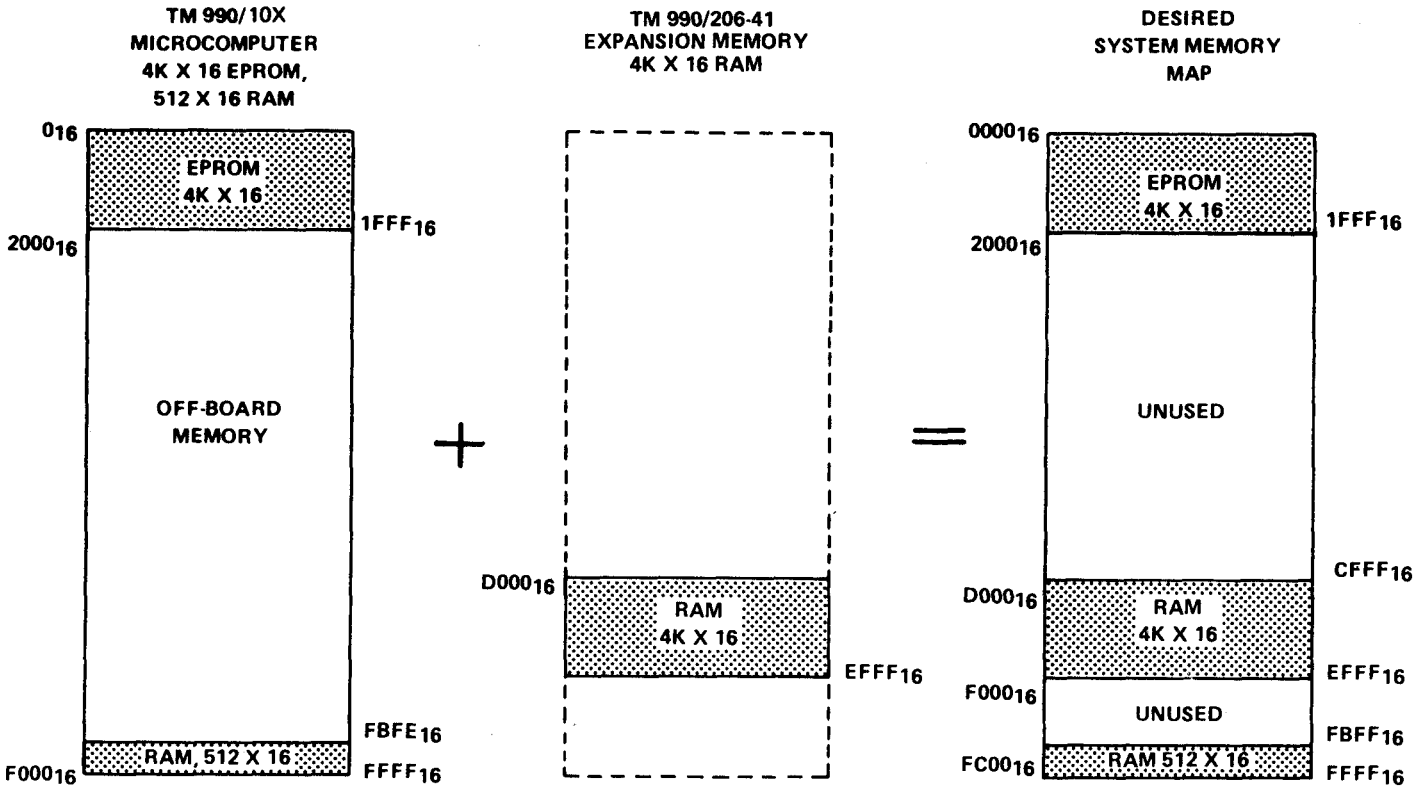


FIGURE 3-5. TM 990/206 MEMORY MAP EXAMPLE

OPTIONS

The TM 990/206 is available in two versions:

TABLE 3-5. TM 990/206 OPTIONS

MODEL NO.	RAM POPULATION	EXPANSION AREA ADDITIONAL SOCKETS
TM 990/206-41	4K x 16	4K x 16
TM 990/206-42	8K x 16	---

SPECIFICATIONS

Memory Configuration: TMS 4045-45, 1K x 4 static RAM

Power Requirements (Typical):

Model	+5V
TM 990/206-41	1.3A
TM 990/206-42	2.15A

Cycle Time:

Memory Device Access Time (nsec)	Memory Cycle Time (usec) @3 MHz
450	1.0
300	0.667
200	0.667
150	0.667

Bus Interface:

Data and Address	Three-State TTL-Compatible
Control	TTL-Compatible

Mating connector:
100 Pin, 0.125 in. cc

TI	H321150 (wire wrap)
TI	H322150 (solder tail),
Viking	3VH50/1CN5 (pierced tail)

Operating Temperature Range:
0 deg C to 70 deg C

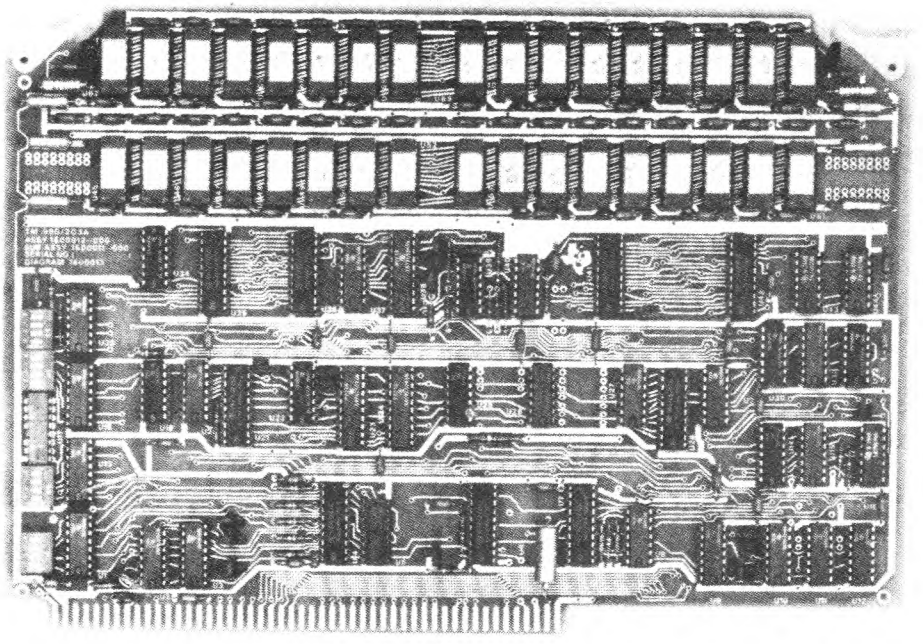
Physical Characteristics:

Width	11 inches
Height	7½ inches
Board Thickness	0.062 inch
Board Standoff	0.4 inch

ORDERING INFORMATION

TM 990/206-41 4K x 16 RAM, sockets for 8K x 16 memory
TM 990/206-42 8K x 16 RAM, fully socketed

3.3.3 TM 990/203 EXPANSION MEMORY BOARD



The TM 990/203 is an assembled, tested, memory expansion board designed for use with TMS 9900-based microcomputer modules such as the TM 990/100M or TM 990/101M. The TM 990/203 contains dynamic RAM memory, expandable to a maximum configuration of 64K bytes. The TM 990/203 does not support the TMS 9980-based TM 990/180M microcomputer.

FEATURES

- Bus compatible with the TM 990/10X microcomputer modules
- 64K bytes of TMS 4116 dynamic RAM (16,384 X 1 bits each) for TM 990/203-23
- 32K bytes of TMS 4116 dynamic RAM (16,384 X 1 bits each) for TM 990/203-22
- 16K bytes of TMS 4027 dynamic RAM (4,096 X 1 bits each) For TM 990/203-21
- Cycle steal or transparent refresh
- Runs with no wait states at 3 MHz
- Parity checking capability
- DMA capability
- Designed to fit either the TM 990/510 or TM 990/520 card cage.

DESCRIPTION

Address decoding circuitry on the TM 990/203 module automatically decodes both 16- and 20- bit addresses. Upper and lower boundaries are DIP switch selectable on 4K byte boundaries. Boundary selection is independent of the amount of memory actually populated on the module. This means the user can disable any 4K bytes of memory for other use such as a 4K EPROM loader. All of the TM 990/203 memory may be disabled without removing it from the card cage by selecting a starting address that is greater than the ending address.

PARITY OPTIONS

The TM 990/203 memory module will interrupt the processor in the event of a parity error if operation with parity is used. An interrupt handler (software routine) must be generated by the user to reset the parity interrupt and flag the memory location which is in error. The exact location in error may be found by the interrupt routine if a read operation is performed, with all additional interrupts masked, on the entire RAM memory while the software monitors the interrupt line to check for errors.

Three jumper selectable parity options are available: no parity interrupts, parity interrupts resetable by the CPU's TMS 9901, or parity interrupts resetable by a discrete CRU location (with user supplied PROM). Jumpers are also provided to configure the TM 990/203 parity interrupt to level 1 or level 2.

Parity interrupts may be reset by the TM 990 bus signal INT15.B-/P7 which is usually generated by setting bit P7 in the CPU TMS 9901 I/O port. A low on this line will clear and disable the parity interrupt. A high on this line will enable the parity interrupt.

Parity interrupts can also be reset by doing a CRUOUT operation. The particular location is programmed into an SN74S287N PROM supplied by the user. This allows the user to free INT15.B- for other purposes. It also allows the user to configure his reset in the CRU address map.

MEMORY OPTIONS

For processors operating at clock rates faster than 3.2 MHz and for TMS 4027 and TMS 4116 memory devices with access times other than 250 ns, consult Table 3-6 to determine the number of wait states that are needed.

TABLE 3-6. TM 990/203 WAIT STATES

	Memory Access Time			
Clock Rate	300ns	250ns	200ns	150ns
3-3.2 MHz	0WS	0WS	0WS	0WS
3.2-3.5 MHz	1WS	0WS	0WS	0WS
3.5-3.9 MHz	1WS	1WS	0WS	0WS
3.9-5.0 Mhz	1WS	1WS	1WS	0WS
5.0-6.0 Mhz	2WS	1WS	1WS	1WS

Two jumper selectable refresh modes are available. Transparent refresh automatically refreshes the dynamic memories when they are not being accessed. In transparent mode the processor indicates to the memory that the following few cycles are available to do a refresh cycle. This indication is the rising edge of MEMEN-. When this is sensed by the TM 990/203 the next 2 consecutive clock cycles following this edge are used for refresh.

The TM 990/203 is designed such that transparent mode defaults to cycle steal mode; this occurs every time there is a minimum refresh violation. That is, the number of refresh cycles performed during any fixed time is less than the minimum required to insure data integrity. For example, if the processor is placed in a hold state in order that another processor may take the line, MEMEN-, as well as the data and address lines of the processor, is placed in the three-state, high impedance condition. If the bus is not captured and MEMEN- stays in this state, the TM 990/203 cycle steal circuitry will time out and issue a refresh request. This is all done on board the TM 990/203 and is transparent to the user unless he tries to access the TM 990/203 during this time. In that case a not ready condition will be asserted until the end of the refresh cycle.

SPECIFICATONS

Clock Rate: 6 MHz maximum

Devices Utilized: TMS 4027 dynamic RAM (4K x 1 bit each) in TM 990/203-21
TMS 4116 dynamic RAM (16K x 1 bit each) in TM 990/203-22 and TM 990/203-23

Operating Temperature: 0 deg C to 70 deg C

Power Requirements:

	Currents (cycle steal)					
	16K (bytes)		32K		64K	
	TYP	MAX	TYP	MAX	TYP	MAX
Vdd +12V ±5%	77 mA	1.2 A	65 mA	0.6 A	90 mA	1.2 A
Vcc +5V ±5%	1.9 A	3.0 A	1.85 A	2.7 A	1.9 A	3.0 A
Vaa -12V ±5%	10 mA	20 mA	10 mA	15 mA	10 mA	20 mA
	Currents(transparent mode)					
	16K		32K		64K	
	TYP	MAX	TYP	MAX	TYP	MAX
Vdd +12V ±5%	150 mA	1.2 A	110 mA	0.6 A	190 mA	1.2 A
Vcc +5V ±5%	1.9 A	3.0 A	1.85 A	2.7 A	1.9 A	3.0 A
Vaa -12V ±5%	10 mA	20 mA	10 mA	15 mA	10 mA	20 mA

Ordering Information:

TM 990/203-21	16K Bytes Dynamic Memory
TM 990/203-22	32K Bytes Dynamic Memory
TM 990/203-23	64K Bytes Dynamic Memory

SECTION 4

PERIPHERALS AND INPUT/OUTPUT INTERFACE MODULES (300 SERIES)

4.1 GENERAL

The TM 990/3XX series of modules consists of peripherals and input/output interfaces. A peripheral device can be considered as a device or unit operating outside of the mainframe of a computer but connected to it. Terminals, tape recorders, and floppy disks are typical examples of peripheral devices. Input/output (I/O) interfaces allow communications between the CPU and the outside work. In industrial applications, the CPU reads sensors via input modules and provides the control via output modules. I/O interfaces generally fall into three broad classifications: digital I/O modules, industrial I/O modules, and analog I/O modules. This section provides an introduction to both peripherals and input/output interfaces.

4.2 PERIPHERALS

Texas Instruments provides a variety of terminals that satisfy a wide range of application needs. The CPU modules provide both teletype and EIA RS-232-C interfaces. Appendix A shows the wiring configuration required to connect a Teletype Model 3320/5JE in a 20 mA current loop with a TM 990/100M. Appendix B shows the wiring for RS-232-C cabling between a TM 990/100M and a KSR 743 data terminal. The TM 990/301 microterminal is a low-cost microterminal designed to interface with the TM 990 series of CPU modules. The microterminal allows the programmer to enter, examine, change (if necessary), and execute programs entered in hexadecimal.

The TM 990/303 is a floppy-disk controller that is expected to be available in mid-1979.

4.3 INPUT/OUTPUT EXPANSION MODULES

The TM 990/310 is a digital I/O module that is compatible with all TM 990 family CPU modules. This I/O module provides a maximum I/O capability of 48 I/O points, programmable as either inputs or outputs. The I/O ports are also compatible with those on the CPU.

The TM 990/305 is a combination memory and input/output expansion module. The TM 990/305 has a memory capacity of 32K bytes. This module has 16 parallel input lines (Port 1) and 16 parallel input/output lines (Port 0) that can be configured as either inputs or outputs. All I/O lines are optically isolated and interface through the Communications Register Unit (CRU).

Now that the TM 990/310 and TM 990/305 modules have been described, several applications will be given that illustrate their use.

4.3.1 TM 990/310 Applications

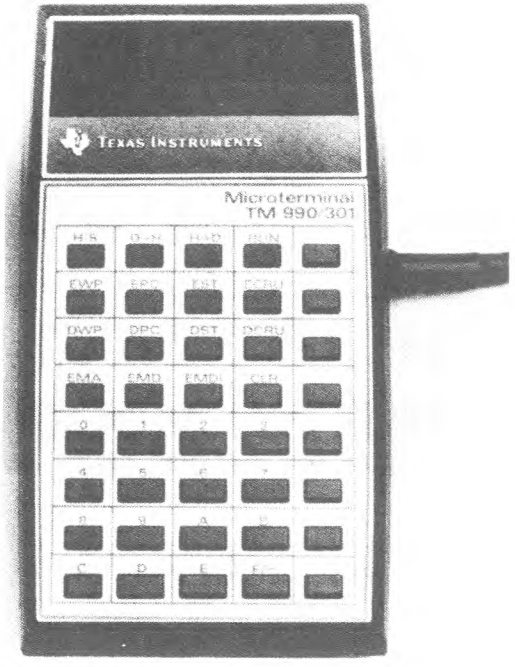
The TM 990/310 I/O module can be used to drive a variety of loads. The signal conditioning circuitry that will be needed between the I/O module and the load can be implemented on the prototyping area of CPU modules or on the TM 990/512 prototyping board in many cases. Several applications for the TM 990/310 I/O module are given below:

- LED Driver
- Relay Driver
- Optically Isolated Loads
- Logic Testing.

In addition, the TM 990/310 can be used in programmable control systems that use the TM 990/5MT industrial I/O system.

4.4 PERIPHERALS AND INPUT/OUTPUT MODULES

DATA SHEETS



The TM 990/301 is a microterminal designed to interface with the TM 990 series of microcomputer modules. The microterminal's communications link to the TM 990 CPU module is via the EIA type cable and the serial terminal interface. The TM 990/301 performs the front panel functions of the microcomputer system, giving the programmer the ability to display and change register and memory information. This low cost terminal offers the capability to enter short programs in hexadecimal or alter a section of a longer sequence.

FEATURES

- Hexadecimal pushbutton keyboard
- 4 digit hexadecimal display of address and data
- Register, memory, or CRU display and entry keys
- Execution, single instruction and conversion keys
- Operations under TIBUG monitor

OPERATION

The TM 990/301 operates under control of the TM 990/401 TIBUG monitor. The data rate utilized is 110 baud. Once the CPU board is initialized, depressing the clear (CLR) key transfers TIBUG monitor control to the microterminal. The TIBUG software will enter a wait routine unless performing a function defined by the microterminal. Depressing the run (RUN) key will cause the CPU module to begin program execution and it will ignore other key depressions

until the halt (HALT/SIE) key is depressed. If the CPU is halted, depression of the single instruction execution key (HALT/SIE) causes execution of the next instruction.

The display of the microterminal is divided into two 4 hexadecimal digit banks. The left bank displays address register information and the right bank displays data registers.

KEY	FUNCTION
CLR	Clear--blank all displays--initialize software
RUN	Run--TM 990 CPU begins program execution "RUN" is displayed in data digits
HALT/SIE	Halt/Single Instruction Execution--If in run mode, halts CPU execution--address of next instruction displayed in address digits. If CPU is halted, one single instruction will be executed. Address display indicates address of next instruction data display indicates contents of that location.
0-F	Hexadecimal digits (0-15)--data entry. F/- also indicates negative.
EPC	Enter Program Counter--Enter 4 digits, key depressions alters active program counter, data display indicates entered value.
DPC	Display Program Counter--Active PC register indicated in data display.
EST	Enter Status Register--Enter 4 digits--key depressions alters active status register data display indicates entered value.
DST	Display Status Register--Active status register indicated in data display.
EWP	Enter Workspace Pointer--Enter 4 digits--key depression alters active workspace pointer--data display indicates entered value.
DWP	Display Workspace Pointer--Active WP indicated in data displayed.
EMA	Enter Memory Address--Enter 4 digits--key depression will shift display of digit from data display to address display. Contents of the new memory address will then be indicated in the data display.
EMD	Enter Memory Data--After EMA function has been executed, enter 4 digits--the data display indicates the new data--key depression alters the data at the displayed memory address.
EMDI	Enter Memory Data/Increment--Functions the same as EMD--after key depression of EMDI and data update the address display will automatically increment by 2 and the new addresses contents will be indicated by the data display. To increment the address register without altering data contents, depress EMDI key without entering new digit information.

DCRU — Display CRU Data--Enter 4 digits--the first digit specifies the CRU bit count; the remaining 3 digits specify the CRU address. Key depression shifts the entered digits to the address display and indicates the contents of that address in the data display. All 16 bits will be displayed.

ECRU — Enter CRU Data--After DCRU function has been executed, enter 4 digits--the new data is now indicated by the data display--key depression alters the data at the spedivfied CRU address--only the number of bits specified will be altered.

H--→ D — Hexadecimal to Decimal Conversion--Enter 4 digits--key depression will indicate the decimal equivalent in rightmost display digits.

D--→ H — Decimal to Hexadecimal Conversion--Enter 6 digits--the first digit designates the sign F/ = negative, 0 = positive) the remaining 5 are decimal data--key depression displays hexadecimal equivalent in 4 right digits.

SPECIFICATIONS

Display:
- 8 digit hexadecimal display
- 4 left digits indicate address register
- 4 digits indicate data register

Keyboard
- 16 data keys
- 16 function keys
- 8 keys not connected

Interface: Serial Asynchronous Interface--Signals Include
- /HALT
- TERMINAL DATA IN
- TERMINAL DATA OUT
- +12V
- GND
- -12V
- +5V

Power requirements: Supplied through cable
- +12V @ 50 mA
- -12V @ 20 mA
- +5V @ 150 mA

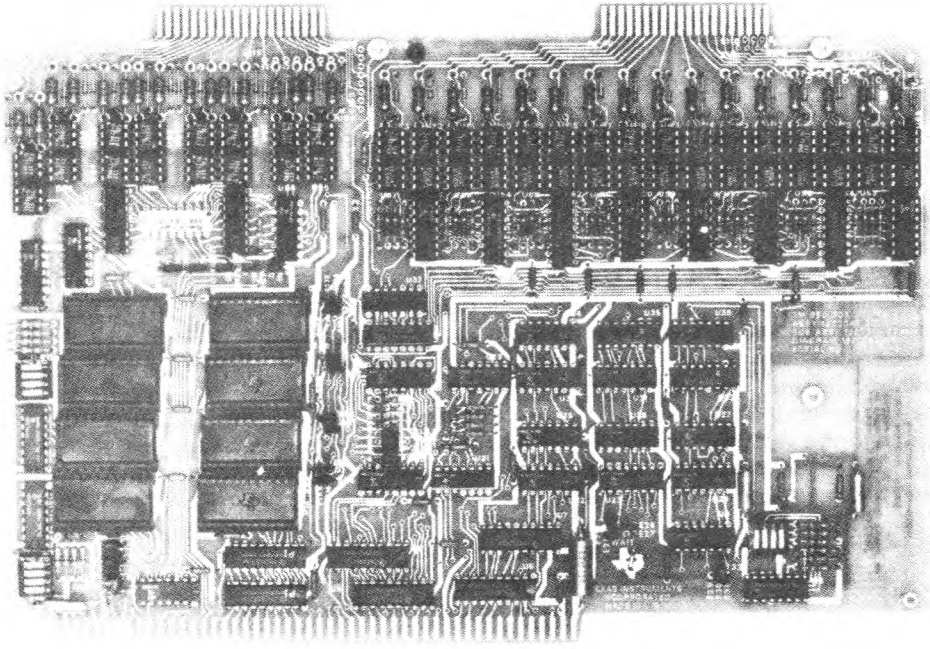
Operating Temperature Range:
- 0 deg C to 50 deg C

Physical Dimensions:
- Height: 5.8 inches
- Width: 3.2 inches
- Thickness: 1 38 inches
- Cable Length: 6 ft.

Ordering Information

TM 990/301	Microterminal compatible with all TM 990 series microcomputer modules.

4.4.2 TM 990/305 COMBINATION MEMORY AND I/O EXPANSION MODULE



The TM 990/305 is a combination memory and input/output expansion module. This module can comprehend a 16-bit address, as used in a TM 990/10X system, or a 20-bit address, as used in a system utilizing a memory-mapping CPU. The TM 990/305 has a memory capacity of 32K bytes. This module has 16 parallel input lines (Port 1) and 16 parallel input/output lines (Port 0) that can be configured as either inputs or outputs. All I/O lines are optically isolated and interface through the Communications Register Unit (CRU).

FEATURES:

- Provision for 5MT interface (via TM 990/509 cable) including resetting 5MT to logic "0" and 8V supply to power 5MT
- Designed to fit either the TM990/510 or TM 990/520 card cage
- Designed to interface with the TM 990/10X CPU modules
- All parallel input/output lines are optically isolated
- Memory capacity of 32K bytes
- 16 optically isolated parallel input lines
- 16 optically isolated parallel input/output lines
- 16 or 20-bit address handling capability.
- 2 positive and two negative edge triggered and latched interrupts

OPERATION

The TM 990/305 combination memory and optically coupled input/output expansion module is implemented using the TM 990 printed circuit format. This module can comprehend a 16-bit address, as used in a TM 990/10X system, or a 20-bit address as used in a system utilizing memory-mapping CPU. Not only does the TM 990/305 have a 32K byte memory capacity, but its memory configuration is significantly enhanced by allowing the use of either static RAM or EPROM in each of the memory sockets.

INPUT/OUTPUT

This module has 16 parallel input lines (port 1) and 16 parallel input/output lines (port 0) that can be individually configured as either inputs or outputs. All I/O lines are optically isolated and interface through the Communications Register Unit (CRU). Each input line of port 0 and port 1 has its own socketed resistor to allow the user to easily reconfigure the module for voltages up to 30 volts. Lines 0 through 3 and line 15 of port 1 can be configured as either inputs or interrupts by selecting the proper jumper option. Line 15 could be used to wire-or interrupts 0 through 3 if the user desires a board interrupt. Interrupts are edge-triggered and latched.

Port 0 functions in much the same manner as port 1 with the exception that the lines can be used as inputs or outputs. When a line is to be configured as a latched output, its individual line resistor must be removed from its socket. By using high current, open-collector devices in port 0, output currents of 30 mA are permitted. If a line is to be used as an input, the optical isolator in its output section should be removed from its socket. The typical port schematic is shown in Figure 4-6.

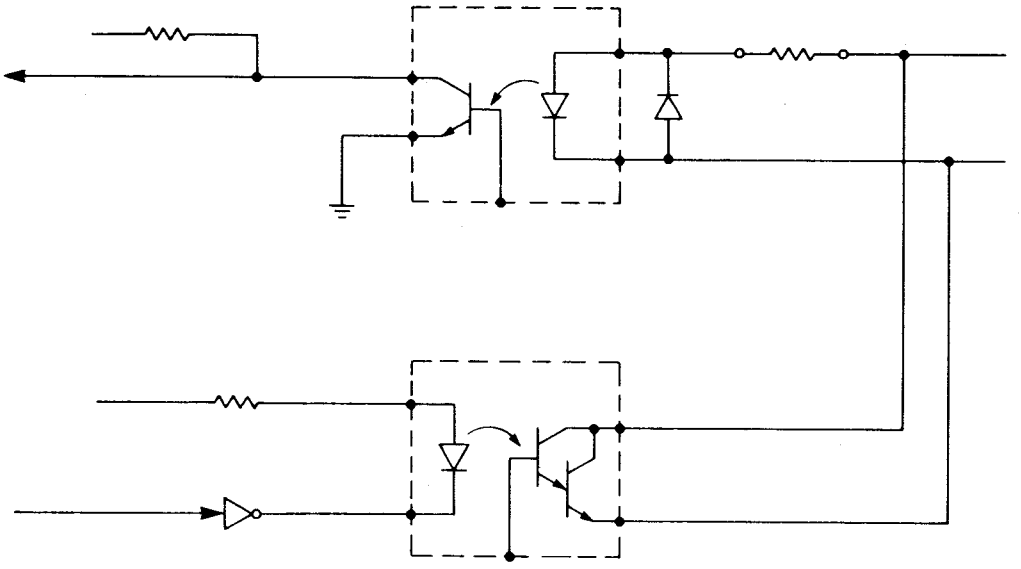


FIGURE 4-6. TM 990/305 TYPICAL PORT SCHEMATIC

MEMORY

The TM 990/305 module is shipped with 8 non-populated 24 pin sockets for memory placement in order to be the most flexible for the user. Memory expansion is provided using either TMS 2516 EPROM, TMS 2532 EPROM, or 2K x 8 static RAM memory devices under development. Selection of up to three wait states are jumper selectable to accommodate the use of slower memories. It should be noted that the wait state jumper controls all memory devices on the module. The number of wait states required is determined by the slowest device on the module.

Jumper options are available to disable the memory (I/O use only), enable the memory for use with the TM 990/100M or TM 990/101M, or enable the memory for use with 20-bit memory mapping CPU modules. For memory-mapped systems requiring more than 64K bytes, a four position switch is provided to decode the 4 high order address bits. In order for the user to get maximum use from his software, page boundaries are in 4K byte increments. Page lines are brought out to a jumper/wire-wrap area to be configured by the user as desired.

I/O ADDRESSING

The TM 990/305 module I/O is addressed via the dedicated CRU interface over the system bus connector. Each I/O bit can be addressed individually or in blocks of up to 16 bits at a time. Maximum flexibility is provided by allowing the user to switch the CRU base address in the range of 0000_{16} to $0FE0_{16}$. The relative CRU input and output functions are listed in Tables 4-1 and 4-2.

SOFTWARE BASE ADDRESS	
00_{16}	INPUT PORT 0
20_{16}	PORT 1 BITS 0-3/ INTERRUPTS 0-3
28_{16}	PORT 1 BITS 4-14
$3E_{16}$	PORT 1 BIT 15/ BOARD INTERRUPT

TABLE 4-1. INPUT CRU MAP

SOFTWARE BASE ADDRESS	
00_{16}	OUTPUT PORT 0
20_{16}	INTERRUPT RESETS
28_{16}	UNDEFINED
30_{16}	INTERRUPT MASKS
38_{16}	STATUS LEDS
$3C_{16}$	BOARD I/O RESET
$3E_{16}$	BOARD INTERRUPT RESET

TABLE 4-2. OUTPUT CRU MAP

OPTIONS

Port 0 is equipped with four socketed SN7406 inverting buffers which drive the output lines. When using 5MT I/O modules, it may be desirable to replace the buffers with SN7407 non-inverting buffers so the 5MT output lines will set to logic "0" upon power up and subsequent assertion of IORST-. The output lines are supplied with sockets so the user may install the required pull-up resistors for 5MT interface.

SPECIFICATIONS

Memory Options (user populated):
- 16K bytes of 2K x 8 static RAM (under development)
- 16K bytes of EPROM (TMS 2516)
- 32K bytes of EPROM (TMS 2532)

Input/Output:*
- Port 0 - 16 lines hardware configurable as inputs or latched outputs
- Port 1 - 16 dedicated input lines; 4 lines jumper selectable as interrupts; 1 line jumper selectable as board interrupt

Input Power Range (TIL 117):

Standard line resistor	3.8-8.5V, 12-34 mA
User-supplied line resistor	3.3-30V, 12-34 mA

Output Power Range:

TTL Option (TIL 117)	0.4V, 2mA; Iceo = 30V
Current Option (TIL 119)	1.0V, 30mA; Iceo = 30V

Interrupts:
- 2 positive edge-triggered, latched interrupts
- 2 negative edge-triggered, latched interrupts

Power Requirements (maximum):
- 5V $\pm$ 3% @ 1.5 A
- 12V $\pm$ 3% @ 600 mA if 5MT interface cable (TM 990/509) is used

Temperature Range:
- 0 deg C to 70 deg C

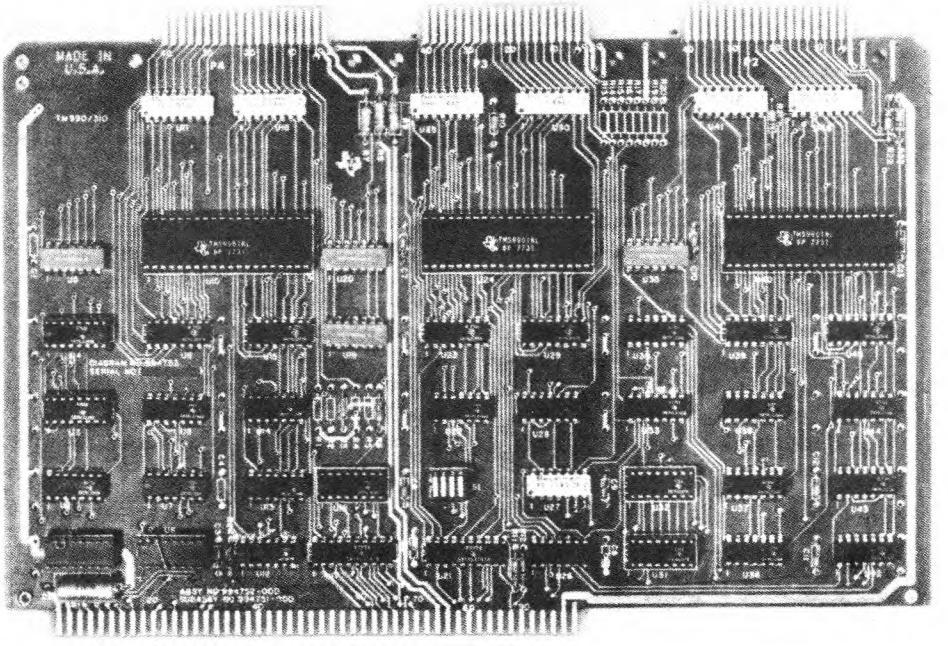
Physical Characteristics:

Width:	11 inches
Height:	7½ inches
Board Thickness:	0.062 inches

Ordering Information:

TM 990/305	combination memory and I/O module with eight 24 pin sockets for user supplied memory & sockets for OCI devices (board populated with 16 TIL 117 inputs at port 0 and 4 TIL 119 outputs at port 0)

* The TM 990/305 module is shipped with 16 input opto-couplers and 4 output opto-couplers in Port 0. No opto-couplers are shipped in Port 1.



The TM 990/310 is a fully assembled, fully tested, input/output expansion module compatible with all TM 990 family microcomputer modules. The TM 990/310 offers a maximum I/O expansion capability of 48 I/O points, programmable as either inputs or outputs.

FEATURES

- Compatible with the TM 990 microcomputer module CRU bus
- Designed to fit the TM 990/510 chassis
- Inputs/outputs are TTL-compatible
- May be used with solder, wire wrap, or ribbon cable edge connectors
- Up to 27 I/O lines may be programmed as prioritized, unlatched interrupts
- Three (+) and three (-) edge-triggered and latched, prioritized interrupt inputs are provided (in addition to 48 I/O lines)
- Contains three real-time clocks (or event timers)
- I/O lines are provided with echo-back feature.

OPERATION

The TM 990/310 input/output expansion module is implemented using the TM 990 printed circuit format. The TM 990/310 uses three TMS 9901 LSI programmable systems interface chips to control I/O. The extreme versatility and low cost of the TM 990/310 module makes it usable in a wide variety of I/O applications. Inputs and outputs may be mixed in any proportion, and any number of interrupts may be utilized, up to a maximum of 33. The interrupt priority encoding scheme also permits use of the module as an interrupt expander for the TM 990/100M microcomputer family.

The TM 990/310 expansion module contains three I/O logic groups, each of which interfaces to separate connectors with 16 I/O lines. (Signal and ground are routed for each I/O line, and each line is equipped with pullup resistors.) Each I/O group may be programmed as 16 inputs, 16 outputs, nine interrupts, or any combination thereof. Each of the output lines is equipped with an echo back feature which enables the user to read back each bit as it is written to a given output point. In addition, each connector contains a "rising edge" detect interrupt input and a "falling edge" detect interrupt input, along with +5 volts, +12 volts, and -12 volts power supply connections.

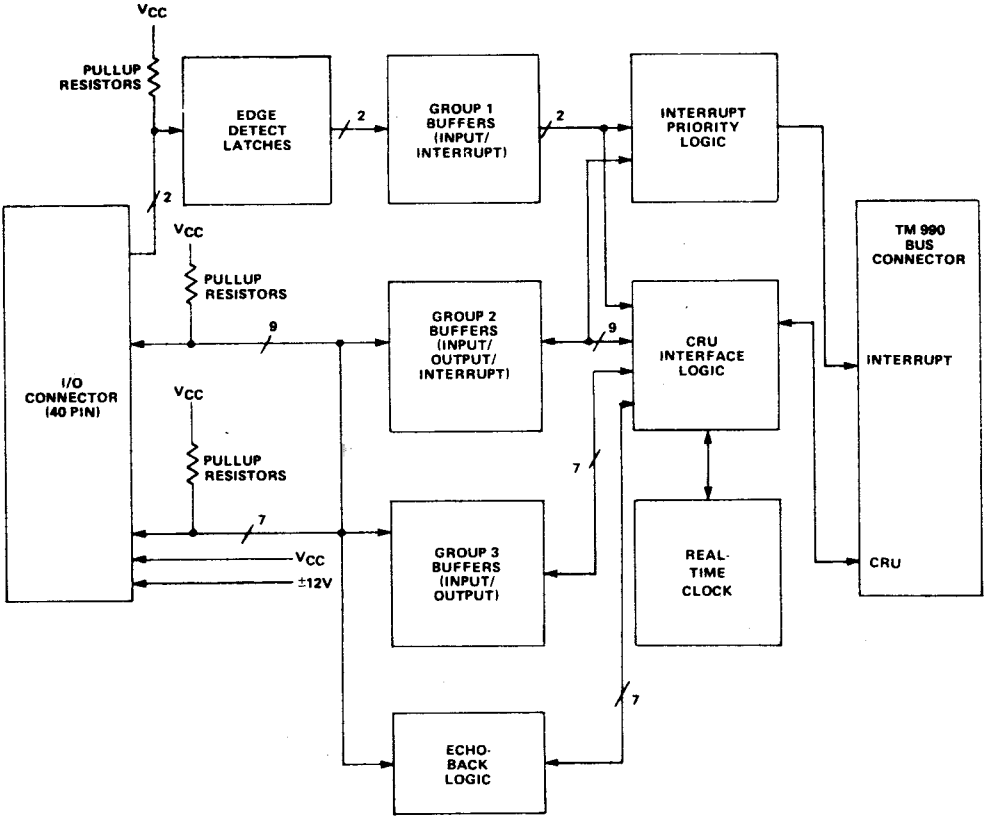


FIGURE 4-7. TM 990/310 EXPANSION MODULE, 16 I/O LINES, LOGIC GROUP BLOCK DIAGRAM (ONE OF THREE GROUPS)

ADDRESSING

The TM 990/310 I/O expansion module is addressed via the dedicated CRU interface over the system bus connector. Each I/O bit can be addressed individually; or up to 16-bit parallel ports can be addressed. Each 16-bit I/O line logic group has an addressing block of 64 bits, and each group can be stacked back to back. Each connector appears exactly the same; the functions and relative addresses for one TM 990/310 is shown below. The CRU address map permits addressing of 4K individual addresses. Any CRU bit beginning with 100_{16} can be addressed; the first FF_{16} bits are dedicated to the microcomputer module.

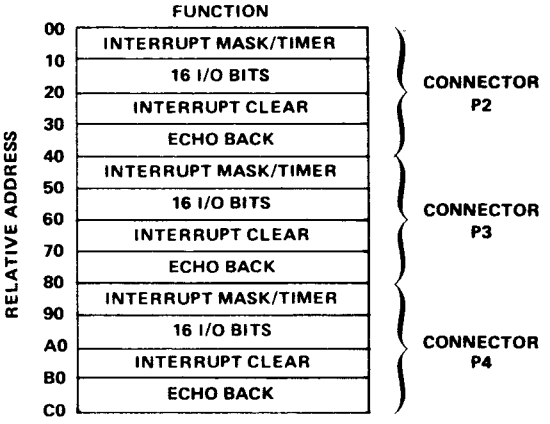


FIGURE 4-8. CRU ADDRESS MAP

SPECIFICATIONS

I/O: 48 bits programmed as inputs, outputs, or up to 27 unlatched interrupts.

Interrupts: 33 maximum, six are (+) or (-) edge-detect latches; output of priority encoders may be jumpered to three levels of the 15 external TM 990 interrupt levels.

Interval Timers: Three 14-bit timers with resolution of 21.3 microseconds and maximum interval of 349 microseconds (for 3 MHz CPU clock)

Level Inputs:
High level input voltage: 2.0 volts, Min.
Low level input voltage: 0.8 volt, Max.
Absolute maximum input voltage: -0.3 to Vcc
Input current: -1.01 mA Max. @ 0.4V

Edge Detect Interrupts

Positive-going threshold voltage: 1.9 volts, maximum
Negative-going threshold voltage: 0.5 volts, minimum
Hysteresis: 0.8 volt, typical
0.4 volt, minimum
Absolute maximum input voltage: -0.3 to +7.0 volts
High Level Input Current: -1.22 mA, maximum at 2.7 volts
Low Level Input Current: -2.72 mA, maximum at 0.4 volt

Outputs:

High Level Output Voltage
2.4 volts, minimum at -300 uA
2.0 volts, minimum at -460 uA
Low Level Output Voltage:
0.56 volt, maximum at 2.3 mA

I/O Connectors

40 Pin (3): TI H311120 (wire wrap),
Viking 3VH20/1JN5 (solder tail),
3M 3464-0001 (ribbon cable),
or equivalents

100 Pin: TI H321150 (wire wrap),
TI H322150 (solder tail),
Viking 3VH50/1CN5 (pierced tail),
or TM 990/510 chassis.

Power Requirements:

+5 volts ±3%
800 mA (typical)

Temperature Range

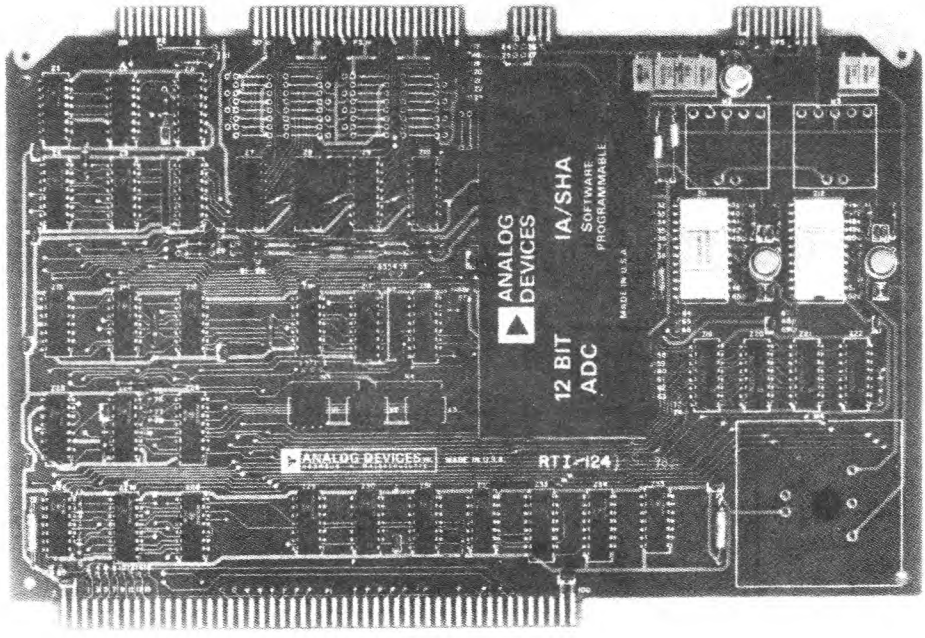
Operating: 0 deg C to 70 deg C
Storage: -65 deg C to 150 deg C

Physical Characteristics:

Width: 11 inches
Height: 7½ inches
Board thickness: 0.062
Component Height: 0.5

ORDERING INFORMATION

TM 990/310 48-bit, I/O Expansion Module



The TM 990/1240 series of analog I/O subsystems are compatible with the TM 990/100M and the TM 990/101M CPU modules. All data bus, control bus and address bus connections to the microcomputer are made by simply plugging the board into the computer card cage. The analog signals connect at the opposite board edge from the digital bus connector.

FEATURES

- 16 bit capability
- memory mapped I/O interface
- 12 bit resolution and accuracy
- optional single +5V power
- 256 input channel expansion capability
- input overvoltage protection
- software or resistor programmable input gain
- interrupt operation capability
- 8 latched, open collector, high current logic drivers
- 4 or 8 analog output channels

TM 990/1240 ANALOG INPUT SUBSYSTEM

The basic function of the TM 990/1240 is to convert analog signals to digital form. An input analog multiplexer (MUX) provides overvoltage protection with an option for either resistor or software programmable gain. The 12 bit A/D converter and associated digital interface logic is shown in Figure 4-9.

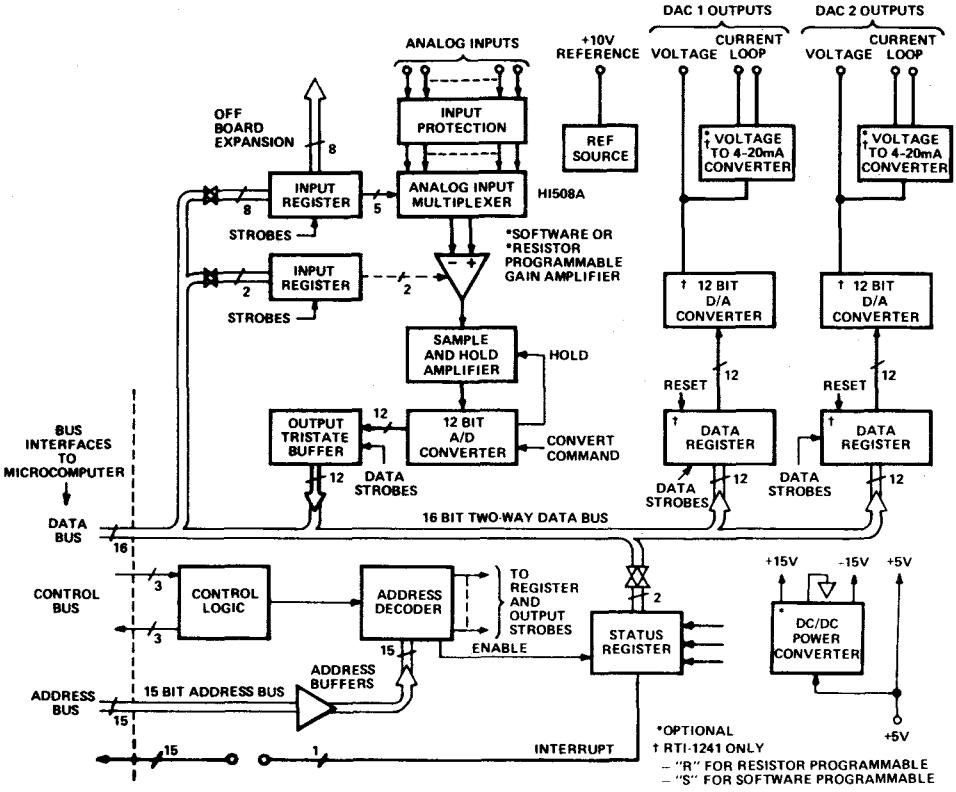


FIGURE 4-9. TM 990/1240, TM 990/1241 BLOCK DIAGRAM

INPUT MULTIPLEXER

The TM 990/1240 is available with up to 32 single-ended or 16 differential, overvoltage protected, input channels on-board and has the capacity of off-board expansion to 256 channels using on-board control logic. Channels can be randomly selected by the memory map control word. MUX channels can be automatically incremented upon receipt of the ADC convert command.

INSTRUMENTATION AMPLIFIER/SAMPLE AND HOLD AMPLIFIER

Input boards are provided with a single module incorporating an instrumentaion amplifier, sample and hold amplifier and analog-to-digital converter. Two types of instrumentation amplifiers (IA) meet 12 bit compatible CMRR & CMV specifications. One board provides software-programmable gain settings of 1, 2, 4, or 8 while the other is resistor programmable over the ranges from 10 mVFS to $\pm$ 10VFS. The sample and hold amplifier allows sampling of high slew rate signals and is automatically switched to the hold mode upon receipt of a convert command.

ANALOG/DIGITAL CONVERTER

The TM 990/1240 operates in either transparent mode where the ADC stops the CPU during conversion for software simplicity, or various modes of polled status programming for the highest data throughput rates. Six ADC input ranges and one of three output codes can be selected with wire-wrap jumpers.

MICROCOMPUTER INTERFACE

The interface to the TM 990 systems is memory mapped; each board has a base address that is jumper selectable from $000X_{16}$ to $FFFX_{16}$. Eight 16-bit words are reserved to transfer data, status and control as shown in the memory map in Figure 4-10. Jumper selectable, optional status words provide flexibility during polling to read either ADC data or gain and multiplexer data at the same time the status word is read. An under-range bit is available to indicate when the signal just converted is small enough to permit a higher gain and that a higher gain is still available.

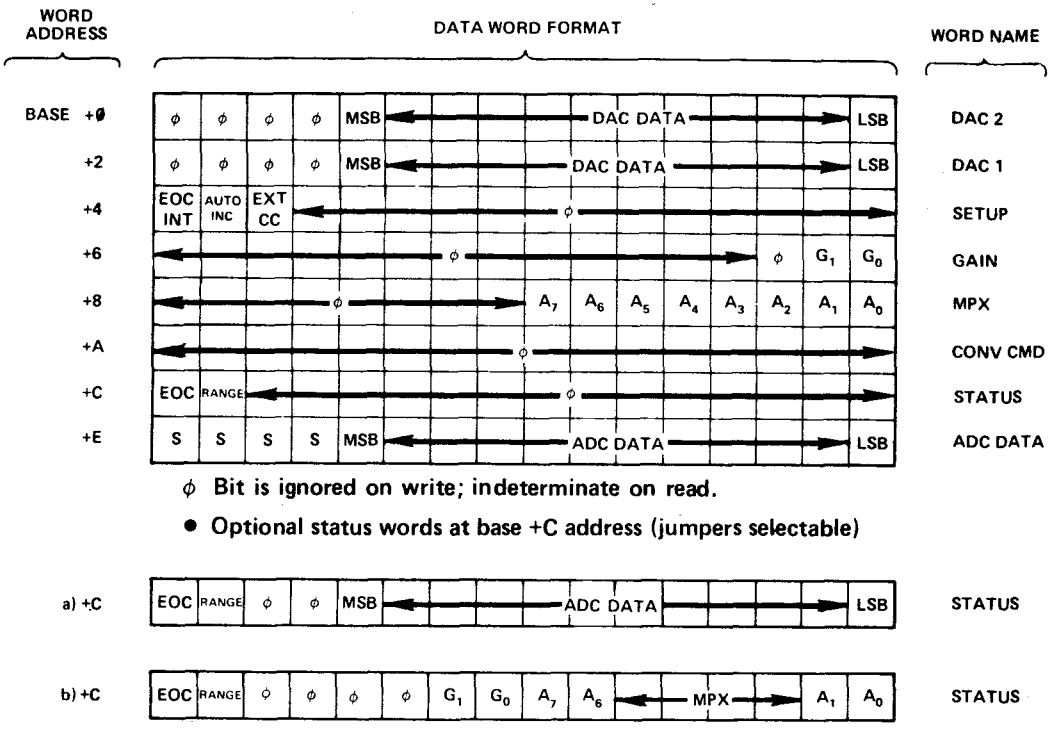


FIGURE 4-10. TM 990/1240, 1241 ADDRESS MAP

TM 990/1241 ANALOG COMBINATION I/O INTERFACE

Figure 4-9 also shows the block diagram of the TM 990/1241 combination I/O module, which is essentially the same as the TM 990/1240 input module with the addition of two channels of 12 bit analog output. D/A converters on the TM 990/1241 provide up to ± 10V analog output, wire-wrap jumper selectable in several ranges. A +10V reference for the DAC's is located on-board, but the option is provided for an external reference from +1V to +10V.

By installing jumpers, the DAC's will reset to zero volts upon receiving an IORST- from the CPU. This feature can be used to reduce output transients when system power is applied. The output channels include 4-20 mA current loops for use in process and industrial control (using the plug-in voltage to current modules).

TM 990/1243 ANALOG OUTPUT SUBSYSTEMS

The TM 990/1243 provides 8 channels of 12-bit analog output whose input code and output range is independantly jumper selectable. Each module also provides 8 high current, logic driver outputs. The digital outputs are software controlled, open collector drivers capable of 300 mA and up to +30V. Figure 4-9 shows the block diagram and optional features. A single on-board +10V reference provides excellent tracking between channels. External references of between +1V and +10V can also be used. The DAC's are equiped with external load sense to compensate for IR losses.

The output subsystem provides sockets for RAM's and buffers to allow DAC and driver data to be read back to the microcomputer. This feature offers additional software flexibility and convenience since it eliminates the need for scratch pad memory or software overhead to store data written to the TM 990/1243 DAC's and drivers. The DAC's and logic drivers can be reset by an IORST- from the CPU module. A standard address map for the TM 990/1243 is shown in Figure 4-11. If the logic drivers are not used, the user may select optional address maps as shown in Figure 4-12.

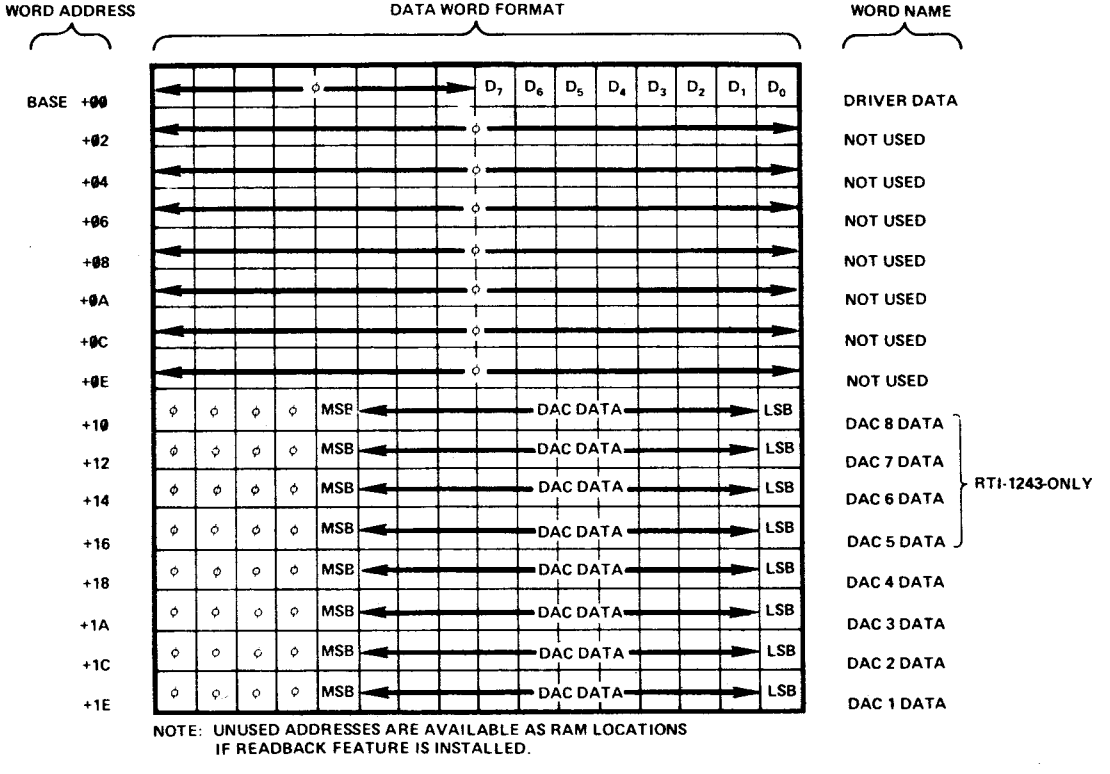


Figure 4-11. STANDARD TM 990/1243 ADDRESS MAP

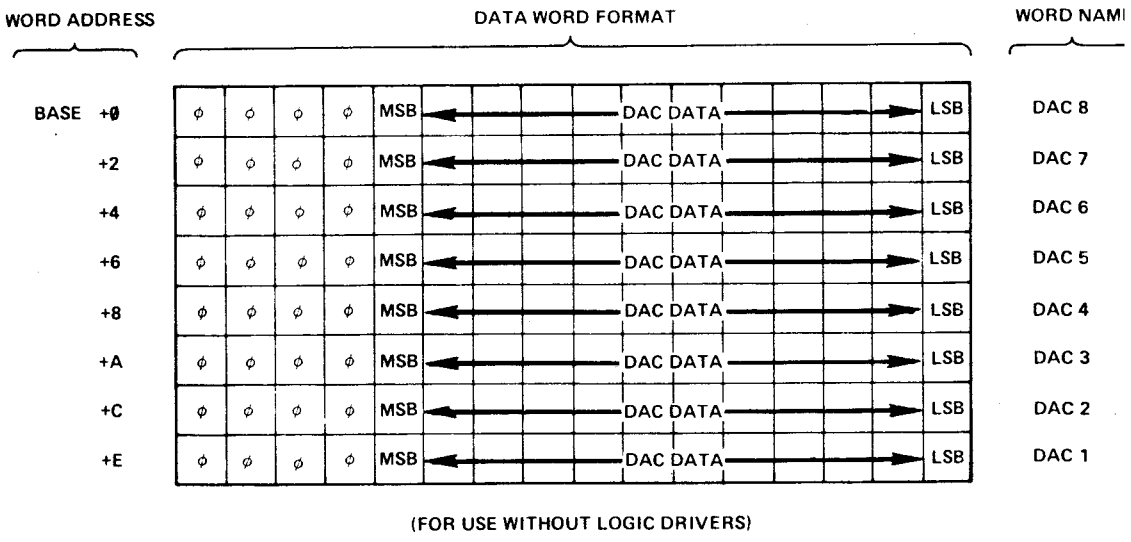


FIGURE 4-12. TM 990/1243 OPTIONAL ADDRESS MAP

SPECIFICATIONS

ANALOG INPUT (TM 990/1240R, 1241R, 1241S)

Input Channels:
32 single-ended, 16 differential
256 addressable channels with off-board expansion

Input Range:
resistor programmable - 10mVFS to ±10VFS
software programmable - 0.625 to ±10VFS

Current Loop Inputs: 0-50mA, 0-20mA

Input Protection: ±(Vcc + 20V)

Switching: Break-Before-Make

Input Impedance: greater than 10^8 ohms

Input Bias Current:
resistor programmable - ±50mA max
software programmable - ±5mA max

Gain Range:
resistor programmable - 1 to 1000 V/V
software programmable - 1, 2, 4, 8 V/V

Common Mode Voltage: ± 10V min

Common Mode Rejection Ratio (DC to 500 Hz): 76 dB min

Input Settling Time:
resistor programmable - 15us max (G = 1)
software programmable - 10us max (G= 1 to 8)

Input Ranges: ±5V, ±5.12V ±10V, ±10.24V, +10V, +10.24V

Resolution: 12 bits

Conversion Time: 25 us max

Throughput Rate: 40,000 Channels/sec

Output Codes: Binary, Offset Binary, Two's Complement

Nonlinearity Error: ±½LSB typ (±1 LSB max)

Offset & Gain Error: Adjustable to Zero

Offset Temperature Coefficient:
resistor programmable - ±(1 + 20)uV/deg C (RTI)
software programmable - ±30uV/deg C (RTI)

Gain Temperature Coefficient:
resistor programmable - ±20ppm of rdg/deg C (RTI)
software programmable - ±25ppm of rdg/deg C (RTI)
Noise Error: ±¼LSB max

Overall Error @ G = 1: ±1LSB max

SHA Aperature Delay: 90ns

SHA Aperature Width: 20ns

SHA Aperature Uncertainty: 5ns

ANALOG OUTPUT

Output Channels: 2 - 1241R, 1241S; 8 - 1243

Resolution: 12 bits

Output Ranges (with on board Ref): +5V, +10V, ±2.5V, +5V, +10V

Output Current: ±5mA min @ ±10V

Nonlinearity Error @ +10V Ref: ±0.01% max

Offset & Gain Error: Adjustable to Zero

Offset Temperature Coefficient: ±15uV/deg C

Gain Temperature Coefficient: ±15ppm

Settling Time (for 20V step to ± 0.01%): 10us

Input Codes: Binary, Two's Complement, or Offset Binary

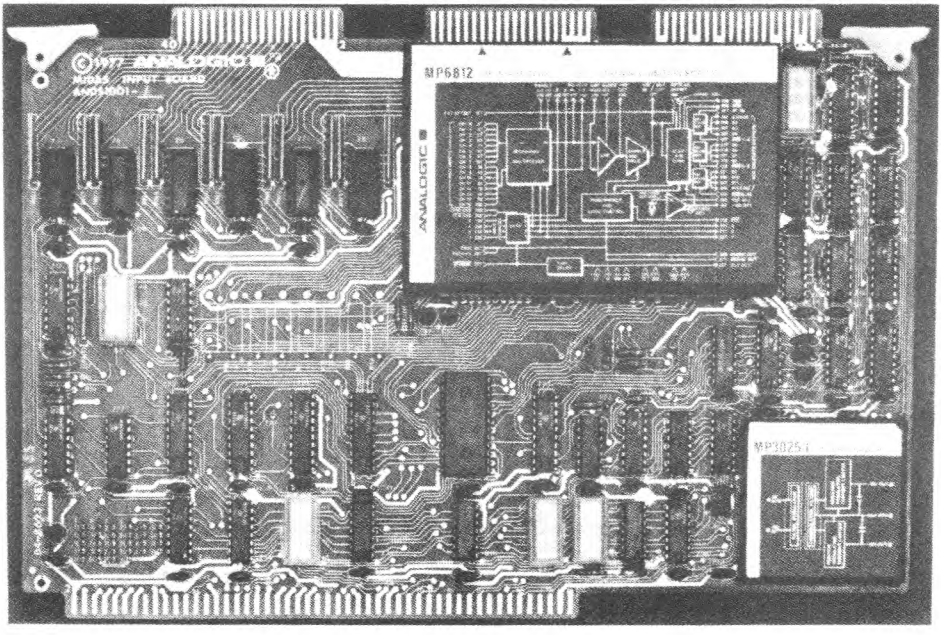
OTHER OUTPUTS

TM 990/1243: 8 Open-Collector Logic Drivers;
300mA sink @ 0.7V; +30V max

TM 990/1241R, 1241S: 2 Current Loops, 4-20mA
Supply Voltage Range: +15V to +30V
Input Voltage Range: 0V to +10V
Offset & Gain Error: Adjustable to Zero
Offset TC: ±0.4uA/deg C
Gain TC: ±30ppm/deg C
Nonlinearity Error: ±0.01% max
Settling Time: 50us max to 0.02%

Power Requirements (+5V max):
1240 - 1.4A
1241 - 1.5A
1243 - 1.6A

Physical Dimensions:
Width - 7½ inches
Depth - 11 inches
Card Spacing - 0.6 inch min



The TM 990/1001, 2001, 3001 series of I/O systems are compatible with the TM 990/100M and the 990/101M CPU modules. All data bus, control bus and address bus connections to the microcomputer are made by simply plugging the board into the computer card cage. The analog signals connect at the opposite board edge from the digital bus connector.

FEATURES

- 16 bit capability
- memory mapped I/O interface, CRU control (CRU I/O for TM 990/1001)
- 12 bit resolution and accuracy
- single +5V power is standard
- input overvoltage protection
- output open circuit protection to 120 VAC
- dual gain buffer amplifier
- interrupt operation capability
- 4 latched, voltage outputs
- 4-20mA current loop outputs

TM 990/1001 HIGH LEVEL INPUT SYSTEM

The high level input system is built around the Analogic MP6812 data acqusition module which incorporates a 16-channel multiplexer, instrumentation amplifier, sample and hold amplifier and analog-to-digital converter. There are 64 single ended and 32 differential inputs fully protected to ±30 volts. Eight 0-50mA current loop inputs are available. Specific current ranges are user-selectable by instalation of appropriate resistors. Input configuration, full-scale input range and digital output coding are all switch programmable. An on-board DC/DC converter eliminates the need for an external power supply.

A/D conversion can be initiated in three modes: 1) Communications Register Unit (CRU), 2) memory read in program transparent I/O, or 3) an external trigger. When initially powered up or after an IORST- signal, the TM 990/1001 will be in the CRU mode. Memory mapped mode is enabled by writing a one to CRU bit 12 and disabled by writing a zero to the same bit. Similarly, the external trigger input is enabled by writing a one to the CRU bit 13 and disabled by writing a zero to the same bit.

The TM 990/1001 has both CRU and memory mapped I/O interfaces. Dip switches select the CRU base address for 16 bits in the CRU address space. Figures 4-13 and 4-14 show the CRU input and output functions at their relative software base addresses.

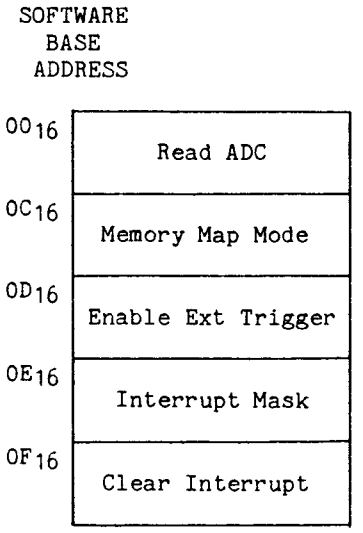


FIGURE 4-13. INPUT CRU MAP

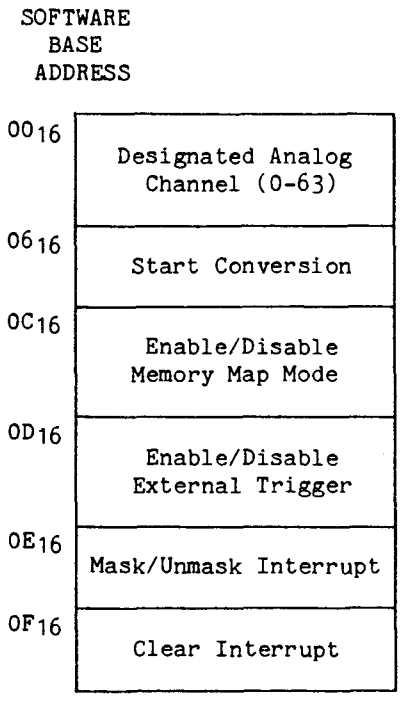


FIGURE 4-14. OUTPUT CRU MAP

Memory mapped I/O requires 64 consecutive addresses, switch selectable from $E000_{16}$ to $FFFE_{16}$. The addresses correspond to the 64 analog input channels. When a read instruction references any one of the 64 decoded addresses, conversion is initiated and the READY line is pulled low. This means that the CPU is halted and cannot respond to any external stimulus such as interrupts during this time. After conversion is complete, the READY line is released and the data is read.

TM 990/2001 HIGH LEVEL OUTPUT SYSTEM

This high level output module interfaces to the host CPU as four memory addresses. Data written to these addresses is latched into the selected digital-to-analog converter and transformed into the analog output. The 12-bit input word must be right justified in the 16-bit field of the data bus as the four most significant bits are ignored by the D/A converter.

Since the TM 990/2001 module responds only to memory write instructions and does not drive the data bus during read instructions, it is possible to locate the four memory write addresses coincident with RAM memory locations. This allows the data written to the analog output channel to be stored concurrently in RAM memory at the same address for later recall.

DIP switches select the base address which may be between $E000_{16}$ and $FFE0_{16}$. By connecting the appropriate wire-wrap jumper terminals on the TM 990/2001, the output channels may be addressed consecutively or 16 words apart. When overlayed on RAM memory, this allows the output channels to reside in one workspace or in four consecutive workspaces.

The TM 990/2001 has four output channels each of which may be independantly set for 4-20 mA current loop output or 5 or 10 volt unipolar or bipolar operation. Current loop operation utilizes the Analogic MP1480 module as a current valve and therefore an external loop supply is required.

TM 990/3001 COMBINATION INPUT/OUTPUT SYSTEM

This combination I/O module combines the features of the TM 990/1001 and the TM 990/2001. There are 32 single-ended or 16 differential input channels. Two DAC output channels are provided each of which is capable of providing a 4-20 mA current loop or 5/10 volt unipolar/bipolar operation. The remaining details are similar to the TM 990/1001 and TM 990/2001.

SPECIFICATIONS

TM 990/1001 - Analog Input

Number of Input Channels: 64 Single-ended, 32 Differential

Input Ranges: ±10.24V, +10.24V, ±5.12V, +5.12V

Maximum Input Voltage: -10.24V or +10.235V (signal plus common mode)

Current Input Range: 0-50mA, selected by user installed resistors

Input Protection: ±30V

Input Fault Current: Limited to 20mA

Input Current (per channel): 1nA @ 25 deg C typ.; 40nA @ 70 deg C

Input Resistance: greater than 100 Megohms

Input Capacitance: less than 10 pf for "off" channel;
less than 500 pf for "on" channel

Resolution: 12 bits

Absolute Accuracy: ±0.025% FSR @ 30 kHz thru-put rate

Inherent Quantizing Error: ±½LSB

3-sigma Noise: 0.01% FSR p-p referred to input

Monotonicity: Guaranteed, 0 deg C to 70 deg C

Linearity Temperature Coefficient: less than 3 ppm FSR/deg C

Gain Temperature Coefficient: less than 15 ppm FSR/deg C

Offset Temperature Coefficient: less than 10 ppm FSR/deg C

Power Supply Sensitivity: 0.003% FSR change in supply voltage

Recommended Recalibration Interval: 6 months

Maximum Throughput Rate: 30 kHz

Sample and Hold Uncertainty: 5 nsec

Crosstalk: 74 dB down at 1 kHz "off" channels to "on" channels

Common Mode Rejection Ratio: greater than 60 dB (DC to 1 kHz)

Sample and Hold Feedthrough: 80 dB down at 1 kHz

Maximum Error for -F.S. to +F.S. transition between successively addressed channes: 1 LSB

Output Code: Binary, offset binary or two's complement; switch-selectable

Power Consumption: Approx. 1.2A @ 5V

TM 990/2001 - ANALOG OUTPUT SYSTEM

Number of Output Channels: 4

Output Current Range: 4 to 20 mA

Compliance Voltage: 10 Volts (without external power supply)

Resolution: 12 bits

Linearity: ±0.012% FSR

Offset Drift: 0.6uA/deg C

Gain Drift: 1.0 uA/deg C

Noise 0-10 kHz: 2.0 uA RMS max.

Over-Voltage Protection: Up to 120 VAC

Output Voltage Range: ±5V, ±10V, +5V, +10V (adj. to 5.12 or 10.24V) @±5mA max

Output Impedance: less than 0.3 ohms @ DC

Offset Drift: 30ppm/deg C max.

Gain Drift: 50ppm/deg C max.

Noise on Voltage Output: 0.01%FSR RMS

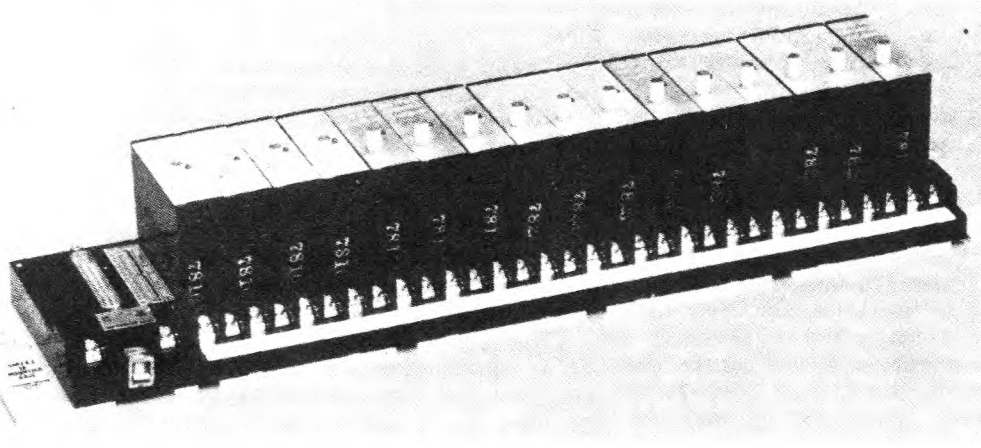
Power Consumption: Approx. 1.0A @ +5V

TM 990/3001 - COMBINATION I/O BOARD

32 Single-ended, 16 Differential inputs; 2 Outputs

Power Consumption: Approx. 1.4A @ +5V

Remaining I/O Specifications Identical to TM 990/1001 and TM 990/2001. Outputs satisfy Instrument Society of America Standard ISA-S50.1 "Compatability of Analog Signals for Industrial Process Control" type 4 transmitter type L and U operation.



The 5MT interface system is designed to handle ac or dc "input" functions and dc or ac "output" functions on industrial control applications. It is typically used to transfer 120 Vac signals from push buttons, limit switches and other sensing devices into dc logic and to operate 120 Vac pilot control loads from dc logic command signals. The system offers a convenient plug-in packaging concept which facilitates installation and maintenance and is suited for use on machine tools, process control systems, material handling equipment, and other industrial applications where operating conditions, both electrical and physical, may be severe. Both the input and output modules are solid state and optically isolated. Internal protection against harmful voltage transients and RFI noise is provided in the system to eliminate the need for external filters, clippers, or suppressors. The modules plug in to the TM 990/5MT43 mounting base and are secured tightly to it by a hold down screw on the modules. The mounting base will accomodate up to 16 modules.

FEATURES

- Designed for industrial applications
- Individual plug-in modules
- Prewired mounting base
- Optical coupled isolation
- One I/O point per module
- LED status indicator
- Input and output modules
- Compatible with TM 990/100M, 101M, 305, 310
- AC, DC modules
- 1500 V isolation between input and output

Practical features of the plug-in 5MT system include indicator lights on all modules, color-coded marking, integral output module heat sinks, input and output device interchangeability, and reduced installation costs over devices requiring four individually wired connections. No special training or equipment is needed for fast, efficient maintenance, thereby reducing down time and expense in the event of a malfunction.

INDUSTRIAL CAPABILITY

5MT series interface modules are designed to operate in rough industrial environments where RFI noise and voltage transient conditions may be severe. Output modules contain 400V triacs which were developed by Texas Instruments specifically for industrial use. They have excellent dv/dt capability and are conservatively rated to provide optimum long-term performance and require no dv/dt protection. Interference generated by the 5MT system is negligible making it ideally suited for use with numerical control, computers, programmable controllers, integrated circuits, and other types of dc logic. All units have highly reliable optical coupler isolation and circuitry which has been proven effective on many actual field installations. Packaging is rugged and practical and provides the interface accessibility preferred by most industrial end users.

APPLICATION FLEXIBILITY

The 5MT system is suitable for use in virtually all control applications which combine 110/120 Vac sensing and pilot control voltage with 5-28 Vdc logic. A general purpose ac/dc input module which sinks up to 200 mA is available. Output modules have full range 5-28 Vdc input voltage capability and may be controlled by logical "1" voltages from TTL logic. Individual dc ground connections to each module permit mixed dc voltages on a single-mounting base. Input and output modules may be mixed in a single mounting base. Interlock pins, supplied with the bases, may be used to prevent incorrect placement of modules.

EASY INSTALLATION

The plug-in mounting concept of the 5MT system facilitates installation and reduces cost over four-terminal, hard-wired devices. One screw-terminal connection is made to the mounting base for each individual model and all remaining connections are made via pin terminals. Each module has ac line and common supplied from lug terminal connections made once to the mounting base, and dc terminations are made by means of a plug connector. Standard connectors offered are suitable for crimp solder or wire-wrap connections.

Convenient to Use and Maintain When in use, 5MT series interface modules can be easily monitored and maintained by regular electrical maintenance personnel. Color-coded markings (blue for ac/dc inputs and red for dc/ac outputs) give visual identification of function and LED signal lights indicate dc circuit energization. Conventional test equipment can be used on ac terminals to provide complete operational checks on each installed device. Modules may be added or removed individually and replacement can be made quickly without requiring the removal and reconnection of terminal wires. The pins on each package are located so as to eliminate the possibility of improper field installation.

INTERFACING

The 5MT series of modules may be interfaced to any of the parallel data ports (TMS 9901) on the 100 series of CPU modules, or may be used with the TM 990/305 or TM 990/310 I/O expansion modules.

The TM 990/507 cable provides the interface between the TM 990/5MT43 mounting base and any of the following: TM 990/100M, 101M, 180M, 310. The user must supply an external voltage of 6-9 volts dc to the base (.6A max at 8 Vdc). Figure 4-18 shows a diagram of a typical system configuration using a TM 990/507 cable.

The user should note that a system I/O reset causes all TMS 9901 outputs to revert to the input state; this will cause 5MT output modules to turn on. If this is unacceptable the user may provide a software power up initialization routine, or use the TM 990/305, TM 990/509 interface.

The TM 990/509 cable provides an interface to the TM 990/5MT43 mounting base for the TM 990/305 I/O module. This cable may be used on port 1 only (the input/output port) for up to 16 5MT interface modules per I/O board. The TM 990/305 module provides 8V @ 0.6A to the TM 990/5MT43 mounting base through the TM990/509 cable. TM 990/305 options allow I/O reset to turn the outputs either on or off, depending on the application requirements. Note that the TM 990/305 generates the +8 volts by regulating from the +12V line and the TM 990/305 +12 V requirement will increase approximately 40 mA per TM 990/5MT I/O module connected.

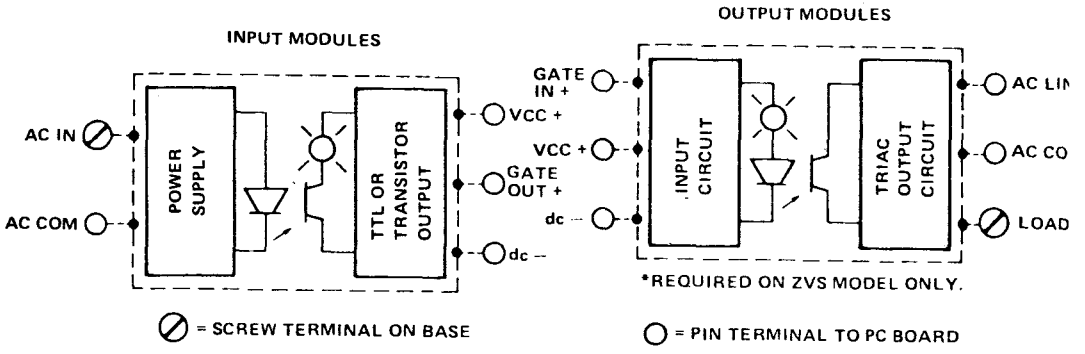


FIGURE 4-15. TM 990/5MT MODULE DIAGRAMS

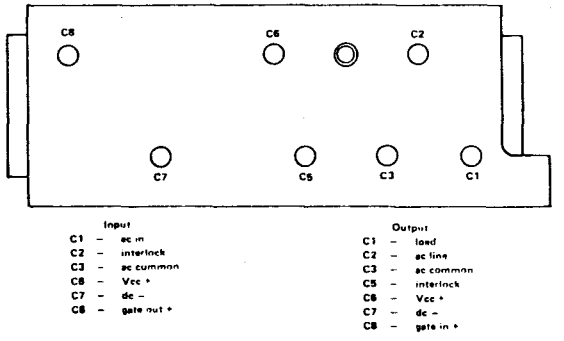


FIGURE 4-16. TM 990/5MT MODULE CONNECTIONS

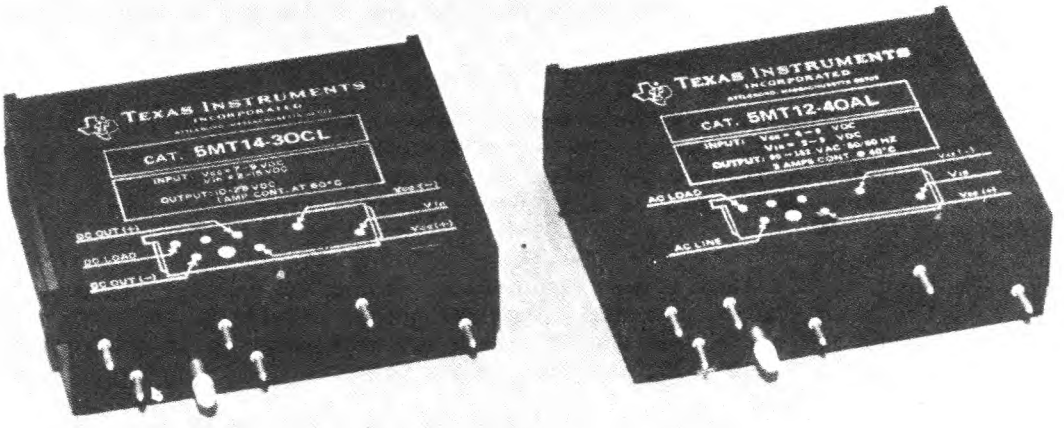


FIGURE 4-17. TM 990/5MT I/O MODULES

MODULE SELECTION TABLE

Catalog No.	Type of Device	Rating	
		Voltage	Current
TM 990/5MT1A05L	AC Input	90-132 VAC	35 mA Max
TM 990/5MT1E05L	AC Input	17-28 VAC	18 mA Max
TM 990/5MT240AL	AC Output	90-132 VAC	3 A Max
TM 990/5MT240EL	AC Output	17-28 VAC	3 A Max
TM 990/5MT3D03L	DC Input	3-28 VDC	30 mA Max
TM 990/5MT430CL	DC Output	10-28 VDC	1 A
TM 990/5MT43	Mounting Base	Holds up to 16 modules	

Note: TM 990/5MT modules are available in OEM prices from Texas Instruments Incorporated, Industrial Controls Marketing, Mail Station 12-13, Attleboro, Massachussetts 02703

GENERAL PERFORMANCE CHARACTERISTICS

- Power requirements: 6-9 Vdc
  (With 8 Vdc applied and 16 modules used, the maximum current is 0.6A)
- Operating temperature range: 0-60 C
- Dielectric isolation: 1500 V
- Clearance voltage: 600 V
- Design life: 100 X 10^6 operations
- Output triac rated 400 V
- TM 990/5MT43 mounting base dimensions (with modules): 19 x 3½ x 3-5/16

A summary of key features is provided in Table 4-3.

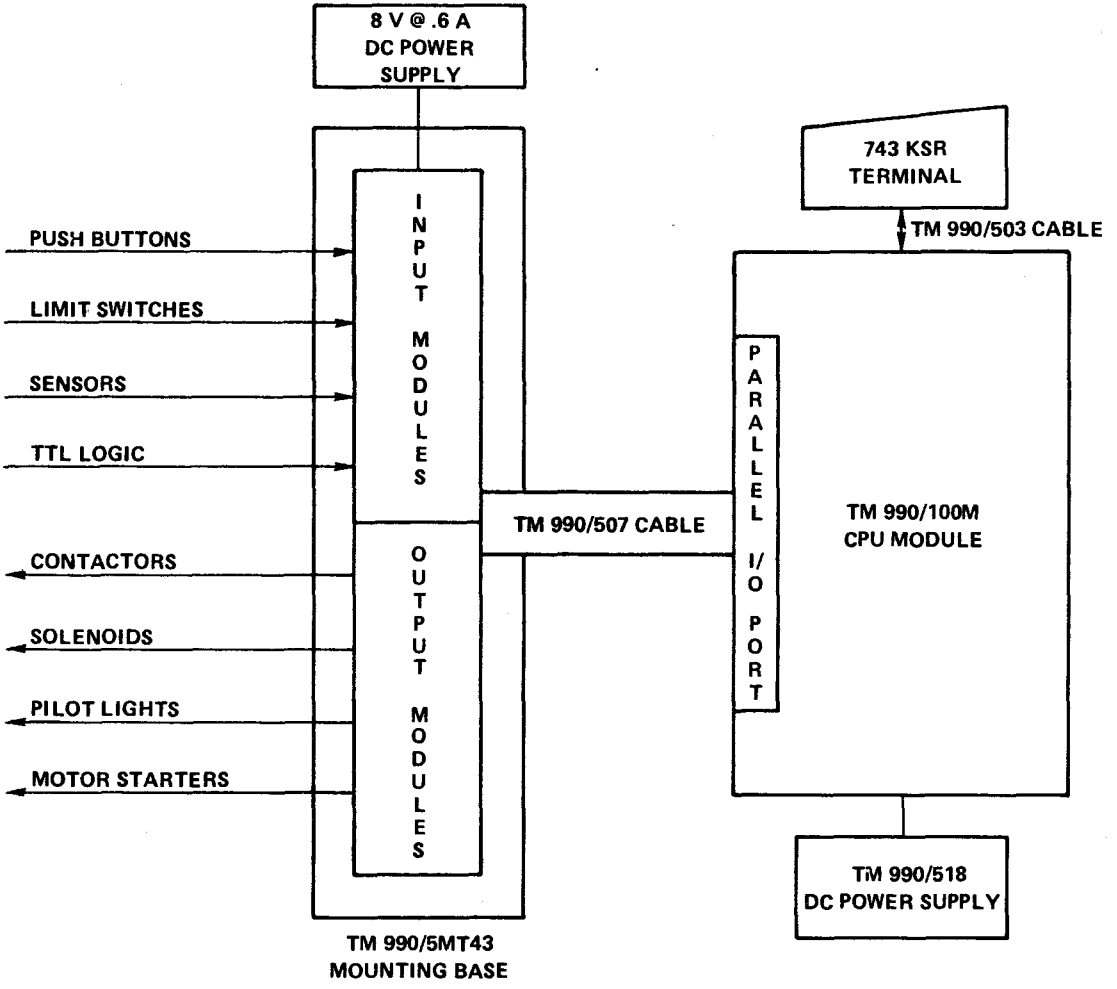


FIGURE 4-18. PROGRAMMABLE CONTROL SYSTEM

Power Application From TM 990/100M

The TM 990/100M microcomputer module can supply the +8Vdc to the TM 990/5MT43 mounting base with the installation of an 8 volt regulator in the prototyping area. Figure 4-19 shows the schematic and Table 4-4 shows the parts list. The pigtail wire on the TM 990/507 cable will need to be extended; it can then be attached to the TM 990/100M board with a machine screw and a fiber washer to keep the screw from contacting any circuit traces. Figure 4-20 illustrates a typical TM 990/5MT system with power being supplied by the CPU module.

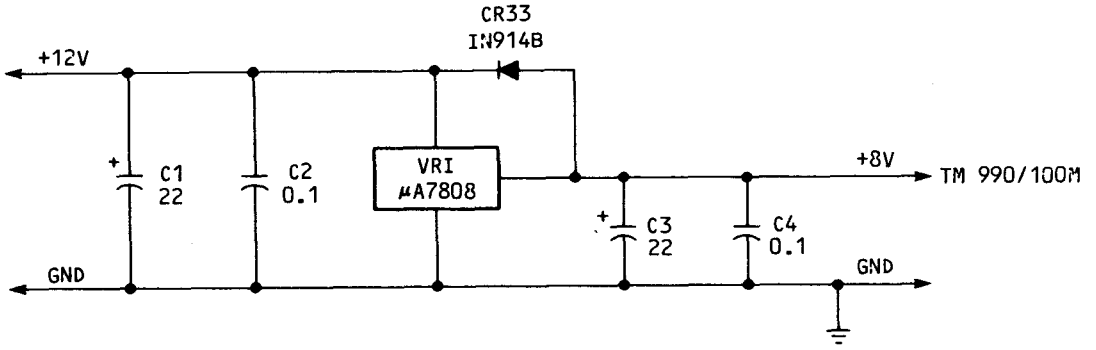


FIGURE 4-19. POWER SCHEMATIC

TABLE 4-4. PARTS LIST

C1,3	22 mfd, 10%, 35V	QPL-M39003/1-23
C2,4	0.1 mfd, 10%, 50V	QPL-M39014/01-1
CR33	1N914B	Texas Instruments
VR1	uA 7808	Texas Instruments

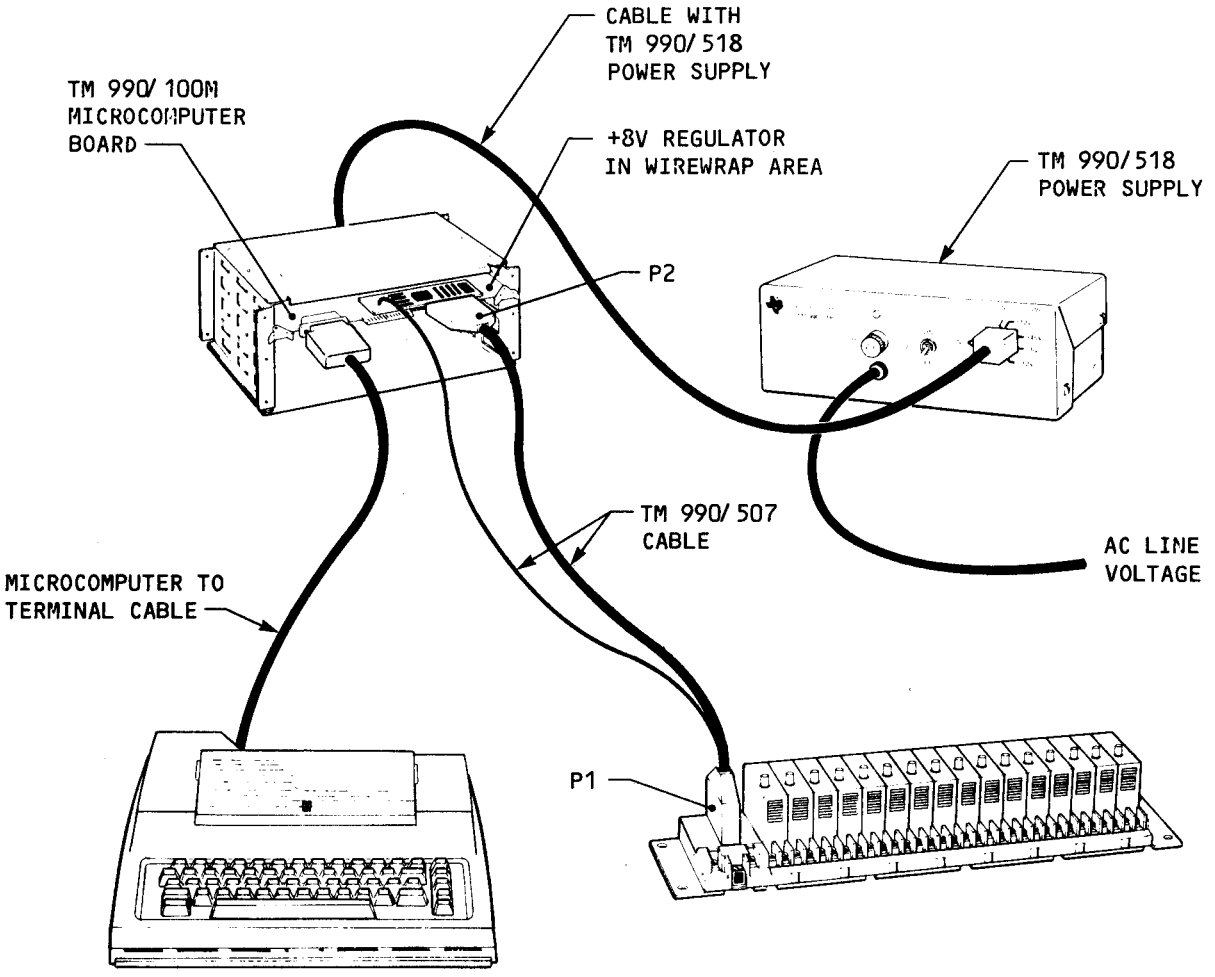


FIGURE 4-20. POWER SUPPLIED TO TM 990/5MT BY TM990/100M

TABLE 4-3. SUMMARY OF KEY PARAMETERS

Product	Mfgr. Part Number	Resolution	Input Channels	Input Voltage Range	Input Current Range	Throughput Rates	Programmable Gain	Output Channels	Voltage Output Range	Current Loop Outputs	Interrupts	+5V Power Requirements	Output Code
Analog Devices - Route 1 Industrial Park, Box 280, Norwood, Massachusetts 02062, 617-329-4700													
*	RTI-1240-S	12 Bits	16 SE, 8 Diff Expandable to 32 SE, 16 Diff	+5V, +10V ±5V, ±10V	0-50 mA	40K Chan/sec	1,2,4,8	0	---	---	15	1.4A	Binary, Offset Binary Two's Complement
TM990/1240R	RTI-1240-R 0A10 0A09	12 Bits	32 SE, 16 Diff **	+5V, +10V ±5V, ±10V	0-50 mA	40K Chan/sec	1-1000	0	---	---	15	1.4A	Binary, Offset Binary Two's Complement
TM990/1241S	RTI-1241-S 0A10, 0A09 0A08, 0A08	12 Bits	32 SE, 16 Diff **	+5V, +10V ±5V, ±10V	0-50 mA	40K Chan/sec	1,2,4,8	2	+5V, +10V ±2.5V, ±5V ±10V	4-20 mA	15	1.4A	Binary, Offset Binary Two's Complement
TM990/1241R	RTI-1241-R 0A10, 0A09 0A08, 0A08	12 Bits	32 SE, 16 Diff **	+5V, +10V ±5V, ±10V	0-50 mA	40K Chan/sec	1-1000	2	+5V, +10V ±2.5V, ±5V ±10V	4-20 mA	15	1.4A	Binary, Offset Binary Two's Complement
*	RTI-1242	12 Bits	0	---	---	---	---	4	"		15	1.4A	"
TM990/1243	RTI-1243 0A09	12 Bits	0	---	---	---	---	8	"		15	1.4A	"
Analogic - Audubon Road, Wakefield, Massachusetts 01880, 617-246-0300													
TM990/1001	ANDS 1001-1	12 Bits	16 SE, 8 Diff Expandable to 32 SE, 16 Diff	+5V, +10V ±5V, ±10V	0-50 mA	30K Chan/sec	---	0	---	---	15	700mA	Binary, Offset Binary Two's Complement
TM990/1002	ANDS 1002	15 Bits + Sign Bit	1 - 4	±20mV, ±40mV ±80mV Thermocouples	---	10 samples/sec	---	0	---	---	na	1500mA	Binary, Offset Binary Two's Complement
TM990/2001	ANDS 2001-4	12 Bits	0	---	---	---	---	4	+5V, +10V ±5V, ±10V	4-20 mA	na	500mA	Binary, Offset Binary Two's Complement
TM990/3001	ANDS 3001-22	12 Bits	32 SE, 16 Diff **	+5V, +10V ±5V, ±10V	0-50 mA	30K Chan/sec	---	2	+5V, +10V ±5V, ±10V	4-20 mA	15	1400mA	Binary, Offset Binary Two's Complement

COMBINATION MEMORY AND I/O EXPANSION

Product	RAM/EPROM Compatibility (Bytes)	Optically-Isolated Programmable I/O Input/Output	Optically-Isolated Programmable I/O Dedicated	Number of Interrupts	Edge Triggered and Latched	Levels	Power Requirements
TM990/305	16K (2K x 8 static RAM) 16K (TMS 2516 EPROM) 32K (TMS 2532 EPROM)	16	16 Inputs	2 2	(+) (-)	15 15	+5V @750mA typical

* Supplied by vendor only

** A depopulated version is available from vendor

SECTION 5
SOFTWARE (400 series)

5.1 GENERAL

Because software support is vital to the successful functioning of TM 990 systems, Texas Instruments provides broad-based support ranging from assembly-based monitors to BASIC interpreters and Pascal Compilers. Many of the popular packaging forms are available such as EPROM's, digital cassettes, floppy discs, hard discs and ½ inch magnetic tape depending on the size and complexibility of the software.

5.2 TIBUG MONITOR

TM 990/401 is a comprehensive, interactive debug monitor included in the basic price of most TM 990 CPU modules. TIBUG includes 13 user commands plus six user accessible utilities and operates with 110, 300, 1200, and 2400 baud terminals. Only TM 990/401-3 may be purchased separately. Section 2.2 mentions some TIBUG characteristics.

5.3 LINE-BY-LINE ASSEMBLER

TM 990/402 is a line-by-line assembler (no labels) supplied pre-programmed into a ROM kit for immediate system use. By allowing you to enter instructions in mnemonic form and performing simple address resolution calculations up to a displacement range of +254/-256 bytes, the assembler is an extremely powerful tool for assembly language input of short programs or easy patching of long programs.

5.4 BASIC

POWER BASIC is a language specifically designed for the industrial realtime I/O environment. POWER BASIC was designed to help solve five common industrial appication problems:

- Unfamiliarity with Microprocessors
  A manufacturer wishes to implement a microprocessor in his industrial process. Unfortunately, his design group is unfamiliar with assembly language or computer programming in general.

- Dividing a Task
  In an industrial development environment, a task is divided among two or more groups. The project leader is reluctant to divide the programming task in fear that the groups will not understand each other's work.

- Intergroup Design
  One group must design a development system for another group to use. Unfortunately, development is stifled because the target group has trouble understanding the operation of the system and is unable to make even minor modifications.

- High Level Language Phobia
  Many manufacturers are using assembly language because they feel it is their only choice. They claim that although high-level languages seem easier to use and easier to understand, they are too slow and require too much memory overhead.

- Equipment (and Software) Obsolescence
  A manufacturer is afraid to design a microprocessor into his equipment because he will then be locked into a particular microprocessor technology. He feels that the development and application programs he writes in assembly language will be obsolete for the microprocessor technology of 1981. His answer is to wait--unfortunately, he has been waiting for years now and sees no end in sight. In fact, the electronics industry seems to evolve faster each year.

Keeping all five of these problems in mind, Texas Instruments designed POWER BASIC, an offspring of the BASIC language created at Dartmouth University. BASIC is a language designed for individuals who have no previous experience with computers. BASIC has incorporated English-like statements (such as "READ" or "PRINT"), so that individuals can write simple BASIC programs after an hour's instruction.

Texas Instruments has added industrial capability to BASIC without sacrificing its simplicity. Now a manufacturer can interface a microprocessor to his industrial devices without a need to learn assembly language. POWER BASIC is available as ROM resident software of in floppy diskette. POWER BASIC is convenient to use and designed specifically for the TM 990 modules. The user only need press the reset switch and the TM 990 board is ready to accept his POWER BASIC instructions.

POWER BASIC programs are also very easy to understand. Since POWER BASIC statements are very similar to English, individuals can "read" a POWER BASIC program without the need for lengthy documentation. In addition, POWER BASIC has the "REMark" feature, which allows the user to add descriptive comments at strategic points in the program. POWER BASIC also allows variables up to three letters long, which allows the programmer to add much more flexibility and meaning to his program.

POWER BASIC was specifically designed to be fast and have the minimum amount of memory overhead. The user can also manipulate bit I/O directly from POWER BASIC, a feature usually found only in assembly languages. Programmers in the industrial control environment will feel comfortable with POWER BASIC because all the tools for their application are available in the language:

- 48 bit arithmetic accuracy (11 significant digits)
- 24 hour time of day clock
- elapsed time for 1/25th of a second or greater
- interrupt capabilities
- string manipulation capabilities
- EPROM programming
- 3 letter variables
- user oriented editor
- ability to call assembly language subroutines directly from Power BASIC

Equipment obsolescence is a problem that is relevant to all software written today. In contrast to assembly language, POWER BASIC is virtually independent of advances in microprocessor technology. Future advances in microprocessor technology will speed up POWER BASIC without demanding a reorganization of the language. Programs written in POWER BASIC for today's microprocessors will also run on tomorrow's microprocessors.

TI's POWER BASIC is available in three versions: Evaluation POWER BASIC, Development POWER BASIC and Configurable POWER BASIC.

5.4.1 Evaluation POWER BASIC

Evaluation POWER BASIC (TM 990/450) occupies 8K bytes of memory contained in four ROM's. In conjunction with either of the 100 series modules, Evaluation POWER BASIC allows the user to enter and execute various applications programs directly from a terminal or other input device. In addition, the user can store his programs directly on digital cassette via the EIA connector on the module. Evaluation POWER BASIC provides the user with the lowest cost capability for design, development and debugging of POWER BASIC programs.

5.4.2 Development POWER BASIC

Development POWER BASIC (TM 990/451) occupies 12K bytes of memory contained in six ROM's. Development POWER BASIC provides several advantages over Evaluation POWER BASIC. For example, one can call assembly language programs as subroutines directly from a POWER BASIC program. This feature is particularly useful for subroutines where high speed execution time is critical.

A typical Development POWER BASIC system would include the six ROM's (TM 990/451), a 100 series module (i.e. TM 990/101M), and a memory expansion board (i.e. TM 990/201). In addition to EPROM programming, the POWER BASIC Enhancement Package (TM 990/452) provides features not available in Evaluation or Development POWER BASIC, such as print formatting for decimal numbers, and an enhanced set of error messages.

If the user development cycle requires audio cassette storage and EPROM programming, an add-on package to the TM 990/451 is available. The POWER BASIC Enhancement Package (TM 990/452) works directly with the TM 990/451 to provide the user with complete POWER BASIC board level capability--from evaluation to EPROM programming. A typical EPROM programming system would include the TM 990/101M module, the TM 990/302 software development board, Development POWER BASIC (TM 990/451) and the Development POWER BASIC Enhancement Package (TM 990/452).

5.4.3 Configurable POWER BASIC

Configurable POWER BASIC (TMSW510F) is our third version of POWER BASIC. Configurable POWER BASIC is a set of floppy diskettes for the FS990 minicomputer. As our most sophisticated POWER BASIC package, Configurable POWER BASIC provides the user with all the statement and library routines available in the ROM resident version of Development POWER BASIC as well as the means to reduce application programs to their minimal memory requirements. The user can write a program in POWER BASIC, eliminate unnecessary library and statement routines through the Configurator, and then "burn" the application program and minimum runtime POWER BASIC interpreter into EPROM's.

5.4.4 POWER Basic Statements

Statements form the basis for all POWER BASIC programs. Typically, statements are entered into a program with line numbers and are executed when the RUN command is entered. All letters of POWER BASIC must be entered in upper case. Table 5-1 lists the set of POWER BASIC statements in alphabetical order.

TABLE 5-1. POWER BASIC STATEMENTS

C	D	E	Syntax	Example/Explanation
*	*		BAUD	Sets the baud rate of the serial I/O port(s). The BAUD rate is the rate of data flow through the ports.
*	*	*	BASE	BASE (256) sets CRU base for subsequent CRU operations. The CRU allows the user to access a line that can turn on a load.
#			BYE	BYE Terminates POWER BASIC and returns control to the TX990 operating system.
*	*		CALL	CALL "SUB1", 0D430H,A,(B) Calls assembly language subroutines. Variables may be passed optionally. "SUB2" would be a program in memory that has to execute often and/or very quickly.
*	*	*	DATA	DATA1,4*ATN(1),"HI" Define internal data for access by READ statement. Allows the user to easily change his input data without changing the program structure.
*	*		DEF	DEFFND(X,Y)=3*X/Y Defines user arithmetic function. Functions are especially useful for mathematical formulas that are used repeatedly.
#			DIGITS	DIGITS7 Specifies the number of digits to be output.
*	*	*	DIM	DIMA(10),DOG(5,10,10) The dimension statement allocates storage for each user variable.
*	*		ELSE	IF A=10 THEN GOTO 2000 ELSE_____ When the most recently executed IF condition is false, the ELSE statement is executed.
*	*	*	END	END terminates program execution.
#			EQUATE	EQUATENAM,A(9,5);B5,B(5) The specified simple variable is assigned the value of the second variable.

TABLE 5-1. POWER BASIC STATEMENTS

C	D	E	Syntax	Example/Explanation
*	*		ERROR	ERROR 1000 ERROR allows user to trap program errors. User can specify a subroutine that will be called via a GOSUB statement when an error occurs by calling a specific line in a program.
*	*	*	ESCAPE	ESCAPE enables the esc key to interrupt program execution.
*	*	*	FOR	FOR I=1TO20 STEP2; The FOR statement is used with the NEST statement to open and close a program loop. Both identify the same control variable. The FOR statement specifies the control variable and assigns the starting and ending value, as well as the increment between those values (STEP).
#			FRA	A=FRA(B) Return the fractional part of the expression.
*	*	*	GOSUB	GOSUB2000 Transfer program execution to an internal POWER BASIC subroutine beginning at the specified line number. See POP and RETURN for two methods to exit from the subroutine. Routines may be nested to 20 levels (Evaluation Power BASIC accepts 10 levels).
*	*	*	GOTO	GOTO300 Transfer program execution to the specified line number or label
*	*	*	IF...THEN	IF I=0 THENI=J::GOTO 200 Causes conditional execution of the statement(s) following THEN. Statments following THEN execute of TRUE condition.
*	*		IMASK	IMASK8 Set interrupt mask of TMS 9900 microprocessor to specified level.
*	*		IRTN	IRTN Return from interrupt subroutine.
*	*	*	INPUT	INPUT1,$B The input statements prompts the user from the terminal using a "?". The user can then enter numeric and string values from the keyboard.
*	*	*	LET	LETA=B*4 A=B*4 Evaluates and assigns values to variables or array elements The LET is optional.
*	*	*	NEXT	NEXT NEXT tests the end of a FOR loop. It delimits end of FOR loop. The sim-var must match the FOR control variable.

TABLE 5-1. POWER BASIC STATEMENTS

C	D	E	Syntax	Example/Explanation
*	*		NOESC	NOESC disables the escape key
*	*		ONTHEN	GOTO GOSUB ON I THEN GOTO 100,200,300 ON J THEN GOSUB 500,600,700 Multibranch statement that transfers control to a line number or subroutine depending on the value of the interval expression.
*	*		POP	POP Removes from the GOSUB stack the last pushed return address without an execution transfer. Useful for exiting nested subroutines.
*	*	*	PRINT	PRINTA,B,$NAM Print (without formatting) the evaluated expressions to the terminal device.
*	*		RANDOM	RANDOM4*MEM(OFDOOH) Set the seed of the random-number generation to the evaluated expression.
*	*	*	READ	READA,$B,C,(0),$D(0) Assigns values from the internal data list to variables or array elements
*	*	*	REM	REM comment lines for documentation. Inserts comment lines into program.
*	*	*	RESTOR	RESTOR RESTOR 40 RESTOR without a parameter resets pointer to the beginning of DATA sequence,while RESTOR with a parameter resets pointer to specified line number.
*	*	*	RETURN	RETURN Return from BASIC subroutine. RETURN also removes top address from GOSUB stack.
#			SGN	A=SGN(B) Returns: 1 if expression is positive 0 if expression is zero -1 if expression is negative
#			SPOOL	SPOOL2TOA Directs unit output specified by expression 1 to logical unit number (luno) specified by expression 2.

TABLE 5-1. POWER BASIC STATEMENTS

C	D	E	Syntax	Example/Explanation
*	*	*	STOP	STOP Terminate program execution and return to keyboard (edit) mode.
#			TAN	A=TAN(B) Tangent of expression (in radians).
*	*	*	TIME	TIME 11,18,30 Start the 24-hour time-of-day clock and set the time of the specified expressions values to hour minutes and seconds.
*	*	*	TIME	TIME Output the clock time as HR:MN:SD to the terminal device.
*	*	*	TIME	TIME$A(0) Stores current clock time into specified string variable.
*	*		UNIT	UNIT 3 Designate the device(s) to receive all printed output.

Note: C = Configurable POWER BASIC, E = Evaluation POWER BASIC
D = Development POWER BASIC, * = denotes availability of feature
# = Statement supported by interpreter but not available to target system.

5.4.5 POWER BASIC Commands

POWER BASIC commands direct and control system operations. Commands cause immediate computer interaction thereby allowing operator control. Commands may only be entered one per line and may not be entered into a BASIC program. POWER BASIC commands may be abbreviated to the first three letters of the command name, and all letters must be entered in upper case. Table 5-3 lists the set of POWER BASIC commands.

TABLE 5-2. POWER BASIC COMMANDS

C	D	E	Syntax	Example/Explanation
*	*		CONtinue	CONTINUE Resume execution starting from the last break in the program.
*	*	*	LIST	LIST List the user's POWER BASIC program from a specified line number or in its entirety.

TABLE 5-2. POWER BASIC COMMANDS

C D E	Syntax	Example/Explanation
*	LIST	LIST 10-100 Selectively lists the user's POWER BASIC program.
* * *	LOAD	LOAD Reads a previously recorded POWER BASIC program from 733 ASR digital cassette.
* *	LOAD	LOAD2 Reads a previously recorded POWER BASIC program from audio cassette drive number 1 or number 2.
* *	LOAD	LOAD 05000H Sets the lower RAM memory bound used by POWER BASIC after auto-sizing at power-up. Sets the higher RAM memory bound in Configurable POWER BASIC.
*	LOAD	LOAD"DSC2:PROCESS/CNT" Reads a previously recorded POWER BASIC program from specified pathname.
* * *	NEW	NEW NEW clears current user programs including variables, pointers, and stacks, and prepares for entry of new program.
* *	NEW	NEW0A000H Sets the lower RAM memory bound used by POWER BASIC after auto-sizing at power-up. Sets the higher RAM memory bound in Configurable POWER BASIC.
*	NUMber	NUMBER 200,20 Specify starting line number and increment value for auto-line numbering.
* * *	PROgram	Program current POWER BASIC application program into EPROM. Available only with Enhancement Package.
*	PURGE	PURGE 200 TO 400 Delete specified range of POWER BASIC statements from user program.
* * *	RUN	RUN Begin program execution at the lowest line number.
* * *	SAVE	SAVE Records a POWER BASIC program onto a 733 ASR digital cassette.

TABLE 5-2. POWER BASIC COMMANDS

C D E	Syntax	Example/Explanation
* * *	SAVE	SAVE1 Records a POWER BASIC program or audio cassette drive number 1 or number 2. Available only with Enhancement Package.
*	SAVE	SAVE"CS1" Records a POWER BASIC program to the specified pathname.
* * *	SIZE	SIZE Display current program size, allocated variable space, and available memory in bytes.
*	STAck	STACK Display the return line numbers which were pushed on the GOSUB stack.
*	SOUrce	SOURCE Display number of bytes that will be stored if the current program were saved.

5.4.6 Edit Mode Commands

An advanced editor is contained in POWER BASIC to aid in program writing, editing, and debugging. The editor uses the following special control characters. Note that the phrase "(ctrl)" indicates that the user holds down the control key while depressing the key corresponding to the character immediately following. The EDIT MODE commands for Configurable POWER BASIC use terminal dependent control keys and are listed in Table 5-3. Note that no editing functions are supported after a program is configured.

TABLE 5-3. EDIT MODE COMMANDS

C D E	Syntax	Example/Explanation
* * *	(CR)	(CR) Enter last line typed into program source
* *	(ctrl)In	(ctrl)I4 Insert n blanks
* * *	(ctrl)Dn	(ctrl)D4 Delete n characters
* *	(ctrl)H	(ctrl)H Backspace 1 character

TABLE 5-3. POWER BASIC EDIT MODE COMMANDS

C	D	E	Syntax	Example/Explanation
*	*		(ctrl)F	(ctrl)F Forward space 1 character
*	*		1n(ctrl)E	100(ctrl)E Display source line indicated by line number (1n) for editing.
	*		(ctrl)T	(ctrl)T Toggle from one partition to the other partition.
*	*	*	(esc)	Cancel input line or break program execution.
*	*	*	(Rubout) or (DEL)	Backspace and delete character.

5.4.7 POWER BASIC Functions

Table 5-4 lists operators that are valid in the POWER BASIC language.

TABLE 5-4. POWER BASIC FUNCTIONS

ABS (exp)	Absolute value of expression.
ASC (string value)	Returns decimal ASCII code for first character of string variable.
ATN (exp)	Arctangent of expression in radians.
BIT (var, exp) BIT (var,exp1)=exp2	Reads or modifies any bit within a variable. Returns a 1 if bit is set and 0 if not set. Selected bit is set to 1 if assigned value is non-zero and to zero if the assigned value is zero.
COS (exp)	Cosine of the expression in radians.
CRB (exp)	Reads CRU bit as selected by CRU base + exp. Exp is valid for -127 thru 128.
CRF (exp)	Reads v CRU bits as selected by CRU base where exp evaluates to n. Exp is valid for 0 thru 15. If exp=0, 16 bits will be read.
CRF (exp1)=(exp2)	Stores exp 1 bits of exp 2 to CRU lines as selected by CRU base. Exp 1 is valid for 0 thru 15. If exp 1=0, 16 bits will be stored.

TABLE 5-4. POWER BASIC FUNCTIONS

EXP (exp)	Raise the constant e to the power of the evaluated expression.
INP (exp)	INP returns the signed integer portion of the expression.
LOG (exp)	Returns natural logarithm of the expression.
MEM (exp)	Stores byte exp 2 into user memory specified by exp 1. Exp 1 and exp 2 must be in the integer range.
MEM (string1),(string2)	Returns the number of characters to which the two strings agree.
NYK (exp)	Conditionally samples the keyboard in run time mode. If exp=0, return decimal value of last key struck and clear key register. (0 if no key struck). IF exp=0, return a 1 if the last key struck has the same decimal value as the expression. Clear key register if TRUE, else return 0 if FALSE.
RND	Returns a random number between 0 and 1.
SIN (exp)	Sine of the expression in radians.
SQR (exp)	Square foot of expression.
SRH (sting1),(string2)	Return the position of string 1 in string 2, 0 if not found.
SYS (exp)	Obtains system parameters generated during program execution. Example: SYS(0)=INPUT control character, SYS(1)=Error code number, SYS(2)=error line number.
TIC (exp)	Returns the number of time tics less the expression value. One TIC is equal to 40 milliseconds (1/25 second).

POWER BASIC language interpreters to meet your requirements for evaluation, development, and application are available in economical and versatile packages (see Figure 5-1). Table 5-5 lists the POWER BASIC Family.

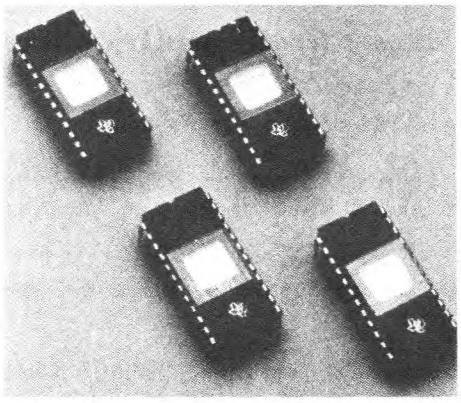


FIGURE 5-1. TYPICAL SOFTWARE PACKAGES

TABLE 5-5. POWER BASIC FAMILY

Part No.	Media	Name	Description
TM 990/450	ROM device	Evaluation	Reduced memory version (8K byte) designed to offer evaluation tools for exploring POWER BASIC applications. ROM kit executes stand-alone on TM 990/101M modules.
TM 990/451	ROM device	Development	Expanded memory version (12K byte) providing capability for design, development, debug, and EPROM programming of POWER BASIC programs. Executes on TM 990/302 module interfaced with TM 990/100M, 101M CPU modules.
TM 990/452	ROM device	Development	Extends the capability of TM 990/451. Included is decimal print formatting, error message printing, audio cassette storage and EPROM programming.
TMSW510F	Floppy Disc	Configurable	Fully expanded version including complete diskette file support and a configurator program which reduces the size of POWER BASIC programs for execution.

5.5 Pascal

The programming language TI Pascal (TIP) has been designed to facilitate the construction of reliable, transportable systems and scientific programs. It is a relatively easy language to learn and to use. A basic assumption in the design of the language is that readability is as important as writeability. Many programs undergo modifications during their lifetime and the ease of modification is dependent on the ability of a programmer (frequently not the author) to read and understand the program. Other considerations in the design of the language look forward to the development of more sophisticated techniques for verfying the correctness of programs.

TI Pascal has excellent bit-manipulation capabilities, and is ideally suited for a wide variety of applications. TIP is supported on Texas Instruments' hard disc-based minicomputer, the DS990.

5.6 EXECUTIVE SUPPORT

5.6.1 TIPMX

The Texas Instruments Microprocessor Executive Library (TIPMX) is a collection of operating system components available to users of the TMS 9900 family of microprocessors. The software is modularized for ease of understanding, and is provided in source, object, and listing format on a variety of storage media.

TIPMX is targeted for 9900 microprocessor users who have a requirement for multiprocessing executive support. Although both Pascal and assembler language are appropriate for use with TIPMX, other source language subroutines may be used with appropriate assembler language interface.

The minimum development tools required for use with TIPMX are a text editor, an assembler, and a link editor. Hence, the library may be used on either the floppy disc based FS990 development system, or on any of the several hard disc based development systems (DX10, etc.). TI Pascal and its extensive Run Time Support Library are available on the hard disc based systems and are highly recommended for use with TIPMX.

A fundamental benefit of TIPMX is that it eliminates the time consuming derivation of standards and conventions for system data structure organization, inter-module parameter passing, register usage, etc., for each user. By deriving these standards and conventions at the 9900 family level, a framework is established for the continued supply of consistent, vendor supported system and application software components from Texas Instruments. Further, providing detailed, comprehensive documentation and source for TIPMX, extablishes a framework which facilitates the generation and free interchange of consistent software between the total 9900 microprocessor community of users.

5.6.1.1 TIPMX Features/Benefits

Some of the system features available in the TIPMX library are presented below:

- Concurrent process execution with n-level pre-emptive priority scheduling

- Stack and heap management
- Interrupt processing and control
- Default power-up, power-fail, and error processing
- Inter-process communication
- Real-time clock servicing
- Semaphore creation/management
- Dynamic process creation and destruction

5.6.1.2 Packaging and Release Media

TIPMX is released on either floppy diskettes, DIABLO or HAWK disk cartridge, or a magnetic tape. The package contains multiple libraries with all the necessary code to construct the TIPMX environment. The libraries contain:

- TIPMX source
- TIPMX object
- TIPMX listings
- Maintenance files for compiling, assembling, and listing TIPMX
- Package description print file

5.6.2 TIMBER

Texas Instrument's Modular-Based Executive in ROM (TIMBER) is the latest innovation in ROM-resident support software. Before the advent of TIMBER, the microprocessor designer usually provided each application with too much "microprocessor power", unless he could design his software to share the microprocessor with a number of separate programs. The motive behind an executive is very simple: one microprocessor executes several separate programs at the same time. The task of designing such an executive is both time consuming and tedious. Now the user can take the TIMBER software, plug it into his TM 990/101M module, and then build his application around the library of executive components fully described in the TIMBER manual. The novice user can become acquainted with TIMBER by following the step-by-step application note included with the product (MPB 23). This application note is available from local TI sales offices and authorized TI distributors.

TIMBER is a software compatible subset of TIPMX. TI's innovative engineers have done most of the "dirty work" as far as setting up the basis for an operating system. They have provided the user with dozens of executive routines. For example:

- Memory Management
- Multiple Sites of Execution
- Real Time Clock Management (from 1 millisecond to 24 days)

- Coordination of multiple tasks

TIMBER is not only useful for reducing development time and stretching a microprocessor's capability; TIMBER also saves memory cost--by permitting the user to run several tasks at the same time from the same location in memory.

5.7 CROSS-SUPPORT

The TMS 9900 Family Transportable Cross Support package is composed of three distinct products: 9900 Cross Assembler, Simulator, and ROM Utility. The part number for the package is SYS9900/16F.X. Initially the package will be manufactured on ½ inch, 9 track PE encoded (IBM compatible) magnetic tape recorded at 1600 BPI. The tape will be unlabeled, unblocked, with 80 ASCII bytes per data record and will contain 131 files. The first file on the tape is a data file which contains:

a) A one-time descriptor for each file on the tape

b) A bill of materials (to verify that the complete package has been received), and

c) An errata list of problems and known solutions for the software version on that tape.

Each file on the tape is terminated by an EOF mark except for the last file which is terminated with a double EOF to indicate end-of-logical tape.

Included in the shipping package is a User Manual for each of the three programs and an Installation Manual covering each of the three programs (4 manuals, total).

5.7.1 9900 Family Cross Assembler Description

The TMS 9900 Assembly Language source is translated by the 9900 Cross Assembler into relocatable linkable TMS 9900 object module format. Both the source input and the object output are fully compatible with the FS 9900 Prototype Development System and TMS time-sharing services (GE TERMINET, NCSS, and TYMSHARE).

5.7.2 Operating Environment

The programs are written to conform to ANSI STANDARD X3.0 (1966) 16-BIT FORTRAN and are designed to execute on any minicomputer with the following minimum characteristics.

1) ANSI STANDARD X3.0 (1966) 16-BIT FORTRAN COMPILER

2) Two's complement arithmetic

3) Disk capacity for up to 7 simultaneously active sequential files

4) A 20K word user program memory partition

To date, the package has been extensively tested on the TI 990/10 under DX10V2.2, DEC PDP11/10 under RSX-11M (FIN IV PLUS), and System 370/168 under MVS.

5.7.3 TMS 9900 Family Simulator Description

The Simulator is patterned after and affords extensions to the TMS 9900 Simulator on GE TERMINET, NSCC and TYMSHARE. Object modules generated by the cross assembler along with "link-control" statements are input to the first stage of the simulator. The output from this stage is an absolute, non-relocatable load module, plus simulation/debug control statements to the second stage of simulation. This stage may be operated in "batchmode" or interactively (e.g., the simulation/debug control stream is entered to the simulator from a Keyboard/Display device). In this second phase of simulation the user's program logic is verified and the program's performance characteristics are ascertained. Performance parameterization is supported for considerations such as target system clock speed, memory characteristics, and I/O part descriptions. Debug features include multiple breakpoints, full instruction trace and snapshots, plus the normal inspect/modify for CPU registers. All program references may be made symbolically, using symbols defined in the user's source program.

5.7.4 ROM Utility Description

When the application program has been satisfactorily verified, the object module may be input to the ROM Utility Program for translation into a format acceptable for production of a gate placement program (preparatory to mass production). Alternatively, the utility may be used to generate a BNPF formatted file which may be input to a PROM programmer (DATA I/O, etc.) to produce a PROM version of the program. In all, there are 12 acceptable input formats and 12 output formats in support of the TMS 1000 and the TMS 9900 microprocessors.

SECTION 6

ACCESSORIES AND CARD CAGES (500 SERIES)

6.1 GENERAL

The accessories and card cage group consists of the following items:

- Card cages
- Special purpose boards
- Power supplies
- Connectors
- Cables
- Adapters.

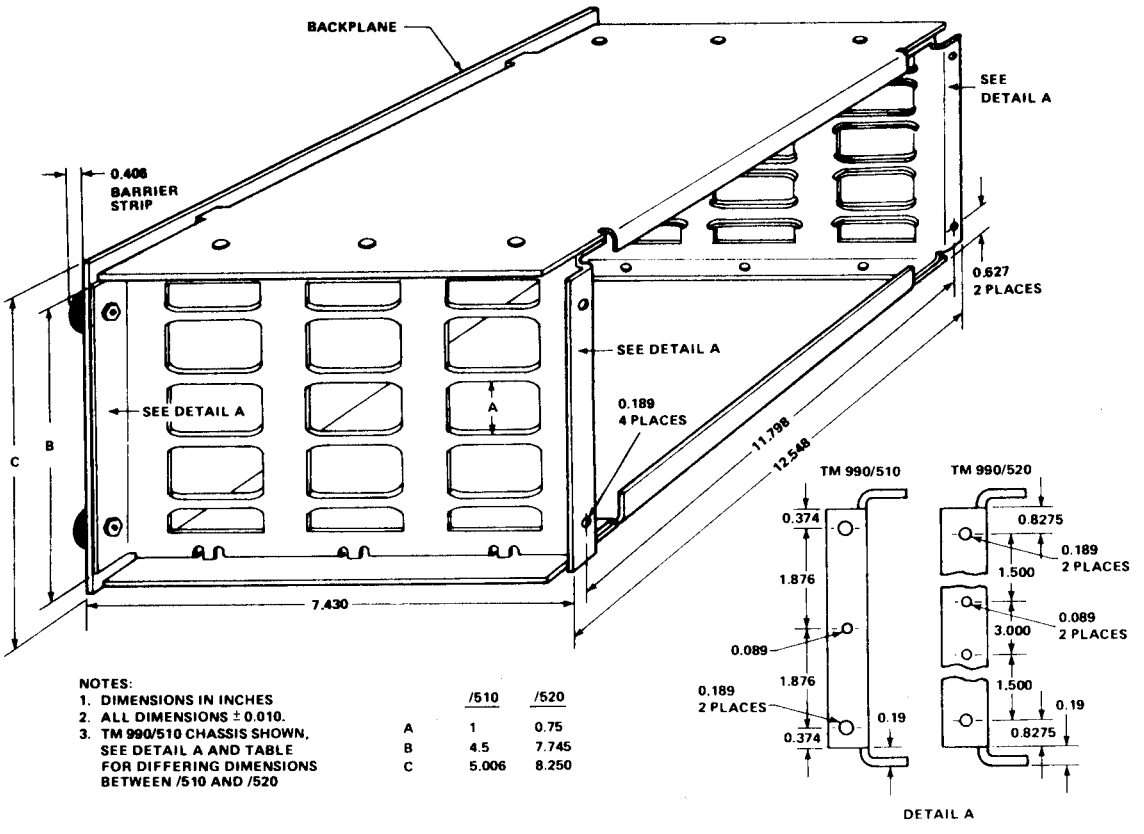
Each of these support items will be described in the paragraphs that follow.

6.2 CARD CAGES

Two card cages are provided to house and provide expansion capability for the TM 990 series modules: the TM 990/510 and the TM 990/520. The TM 990/510 has four-module capacity while the TM 990/520 can accommodate eight modules. The backplane contains the address bus, data bus, interrupt and control lines to permit memory, I/O and DMA expansion of CPU modules. Table 6-1 provides a comparison of the two card cages and Figure 6-1 is an illustration of the TM 990/510 card cage that provides the dimensions for both models. Figure 6-2 shows the TM 990/510 and TM 990/520 card cages.

TABLE 6-1. CARD CAGE MODEL COMPARISON

PARAMETER	TM 990/510	TM 990/520
No. of Slots	4	8
Dimensions	See Figure 6-1	See Figure 6-1
Termination Resistors At:		
Pin 22, ø1.B	N	Y
Pin 24, ø3.B	N	Y
Pin 26, CLK.B	N	Y
Pin 78, WE.B	Y	Y
Pin 80, MEMEN.B	Y	Y
Pin 86, HOLDA.B	Y	Y
Pin 87, CRUCLK.B	Y	Y
Pin 88, IORST.B	Y	Y
Space Between Board Slots	1 in.	0.75 in.



NOTES:
1. DIMENSIONS IN INCHES
2. ALL DIMENSIONS ± 0.010.
3. TM 990/510 CHASSIS SHOWN, SEE DETAIL A AND TABLE FOR DIFFERING DIMENSIONS BETWEEN /510 AND /520

	/510	/520
A	1	0.75
B	4.5	7.745
C	5.006	8.250

FIGURE 6-1. CARD CAGE DIMENSIONS FOR BOTH MODELS
(MODEL TM 990/510 ILLUSTRATED)

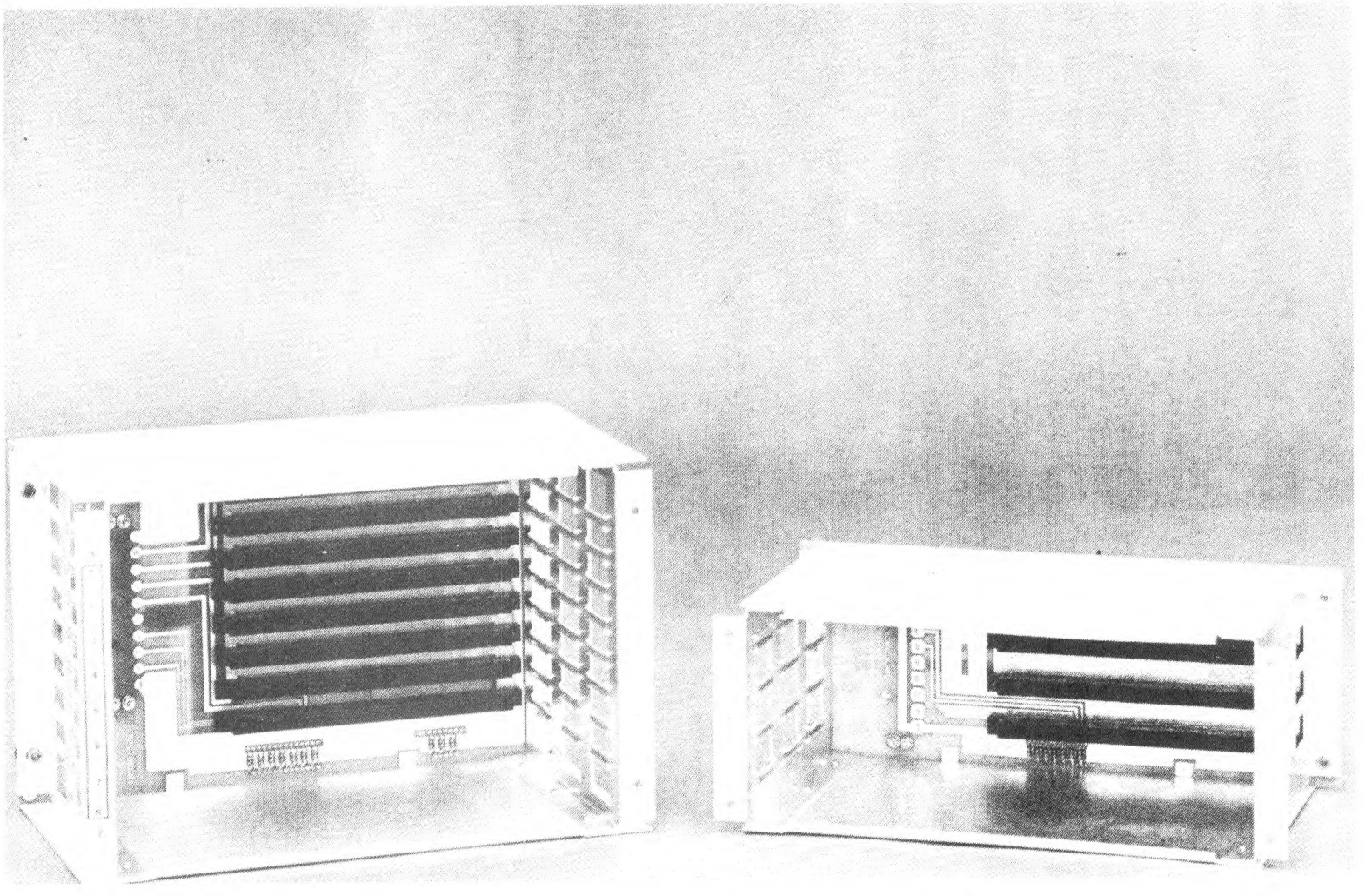


FIGURE 6-2. TM 990/510 and TM 990/520 CARD CAGES

6.3 SPECIAL PURPOSE BOARDS

Two categories of special purpose boards are provided for use with the TM 990 series modules: extender and prototyping boards. Figure 6-3 shows these special purpose boards.

The TM 990/511 extender board allows the user easy access to a printed circuit board such as a prototyping board which contains circuits under development.

The TM 990/512 and TM 990/513 are universal prototyping cards which allow breadboarding of developmental circuits. The printed circuit boards are designed to accomodate 0.3, 0.4, 0.6, and 0.9 inch wide, dual in line, IC packages or their equivalent soldertail or wirewrap sockets.

The TM 990/512 (unpopulated) and the TM 990/513 (wire-wrap pin populated) universal prototyping boards offer the following features:

- TM 990/513 board populated with gold-plated, plug-in type, wire-wrap pins; TM 990/512 board comes unpopulated. This is the only difference between board models.
- Rows of solder through-holes organized into two blocks, each with columns labelled column A to column Z, each block with 50 rows (labelled onboard 1 to 50) of solder-through holes.
- Holes in each row located on 0.10 inch (0.254 cm) centers.
- Both boards are glass epoxy.
- Gold-plated connectors include 100-pin connector directly compatible with TM 990 series motherboard, two 40-pin edge connectors, one edge-connector with solder through-holes for receiving 25-pin EIA connector.
- Ground/+5 V holes provided for filter capacitors which can be jumper wired if necessary.

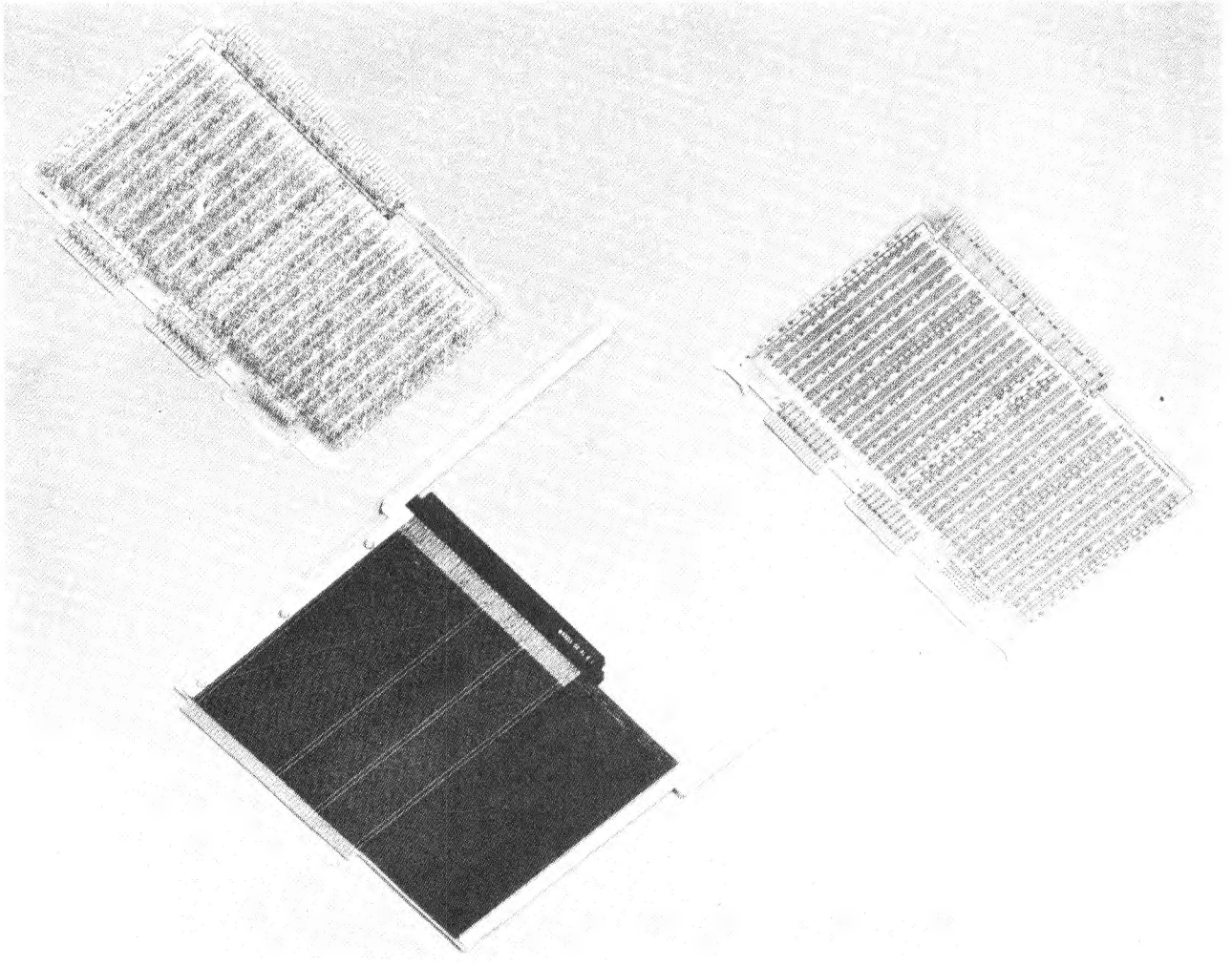


FIGURE 6-3. SPECIAL PURPOSE BOARDS

6.4 POWER SUPPLIES

Texas Instruments provides two power supplies to be used with the TM 990 Series Modules. The TM 990/519 is a low current version designed to be used with the TM 990/189 University Board. The TM 990/518A provides a higher current output and is especially suited for use with the TM 990/302 software development module; it provides all required voltages and includes all required cabling to the TM 990/510 O.E.M. chassis. The TM 990/518 is an O.E.M. open frame version of the TM 990/518A intended for the user who wishes to provide his own enclosure (the user must provide ac power cord, fusing, dc cabling and enclosure with fan). Table 6-2 gives the dc output ratings and maximum load currents for each supply (ratings shown are for +5°C to +50°C ambient temperature).

TABLE 6-2. DC POWER SUPPLY SPECIFICATIONS

MODEL	V_{cc} (5V±3%)	V_{dd} (+12V±3%)	V_{ee} (-12V±3%)	+45V±15%
TM 990/519	2.0A	.25A	.18A	----
TM 990/518A	4.0A	.60A	.40A	.10A
TM 990/518	6.0A	.90A	.90A	.10A

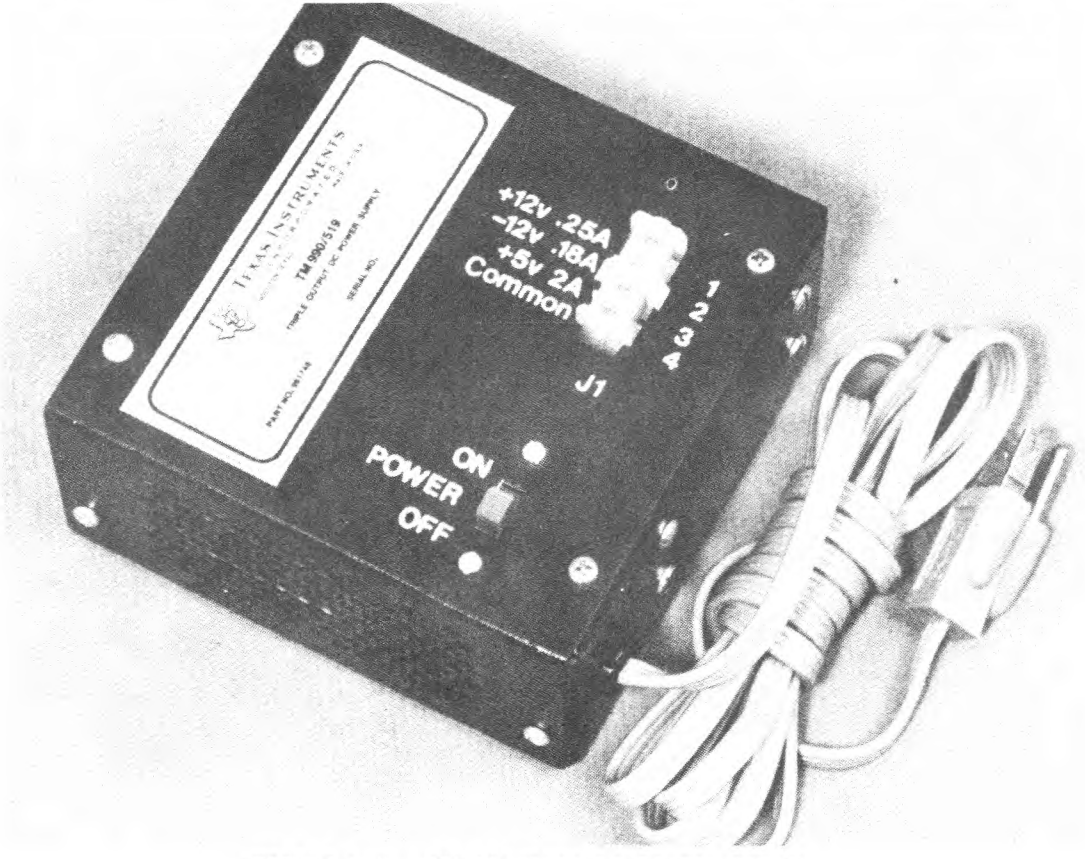


FIGURE 6-4. TM 990/518A DC POWER SUPPLY

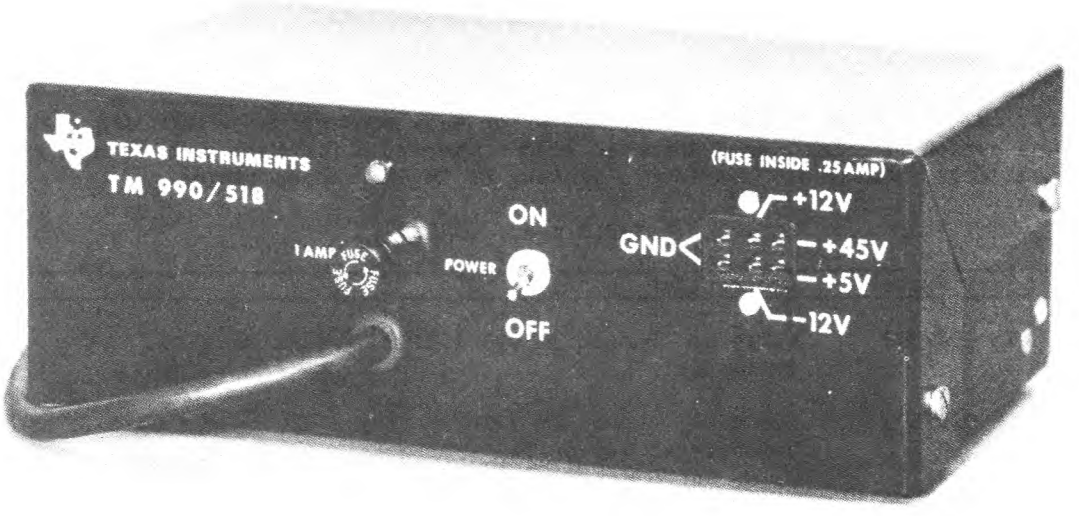


FIGURE 6-5. TM 990/519 DC POWER SUPPLY

All TM 990 series power supplies are shipped configured for 115 Vac, but may be reconfigured by the user for use with 230 Vac input. AC input power specifications are 102 to 132 Vac 47-63 Hz (or 204 to 264 Vac) for the TM 990/519 and 115 Vac ±10% 57-63 Hz (or 230 Vac ±10%) for the TM 990/518 and TM 990/518A.

The power requirements for TM 990 modules are specified in the sections which describe those products. The system configuration sheets in section 10 may be used as an aid in selecting an appropriately sized power supply. If "typical" power requirements are summed to obtain system power requirement the user should allow a safety margin to avoid overloading the power supply. When "maximum" values are specified they contain sufficient margin to avoid the need to add a safety factor.

6.5 CONNECTORS

A variety of connector kits are available for system development. The TM 990 bus requires 100 lines, the EIA connector requires 25 lines and 40 lines are required for I/O or interrupt. The bus connector is a 100-pin printed circuit tab on 0-125 inch centers. Two 40-pin, printed circuit tab connectors for I/O or interrupt are on 0.10 inch centers. Additionally, the CPU modules come mounted with a 25-pin EIA connector, and the universal prototyping boards have space for mounting the same. The TM 990/501 is a three piece connector kit. It includes one each of the 100, 40, and 25-pin connectors. Table 6-3 provides a list of the connector kits that are available.

TABLE 6-3. CONNECTOR KITS

TM 990/501	25 Pin EIA, 40 Pin, and 100 Pin Connectors
TM 990/523	100 Pin Connector Kit
TM 990/524	40 Pin Connector Kit
TM 990/525	25 Pin EIA Connector Kit

6.6 CABLES

Several cables are provided that allow for easy connection between CPU modules and peripheral devices. Several other special interface cables are also available. Table 6-4 provides a listing of TM 990 series cables.

TABLE 6-4. CABLES

Part Number	Description
TM 990/502	Cable to connect TM 990/100 CPU module to a RS-232-C terminal.
TM 990/503	Cable to connect TM 990/100 series CPU module to a Texas Instruments 743 or 745 terminal.
TM 990/504	Cable to connect a TM 990/100 to a Model 33 ASR teletype modified for 20 mA current loop operation
TM 990/505	Cable to connect a TM 990/10X CPU module with a Texas Instruments Model 733 ASR data terminal.
TM 990/506	Cable to connect port P3 of the TM 990/101 CPU module to a RS-232-C modem such as a 103 type data set.
TM 990/507	Cable to connect TM 990/100M or TM 990/310 I/O Module to TM 990/5MT industrial I/O interface.
TM 990/508	Audio cassette interface cable to be used with the TM 990/302 software development module.
TM 990/509	Cable to connect TM 990/305 I/O Module to TM 990/5MT industrial I/O interface.

6.7 ADAPTERS

The TM 990/514 and TM 990/515 EPROM Personality Programming Cards are adapters that are available for use with the TM 990/302 Software Development Module. These adapters allow the user to program different EPROM's with the TM 990/302. Figure 6-6 shows these adapters.

6.7.1 TM 990/514 EPROM Personality Programming Card

The TM 990/514 EPROM Personality Programming Card provides the necessary interface for TMS2708 and TMS2716 EPROM's and the TM 990/302. This card is required when programming these devices with the TM 990/302 Software Development Module.

6.7.2 TM 990/515 EPROM Personality Programming Card

The TM 990/515 EPROM Personality Programming Card provides the necessary interface for TMS2516 and TMS2532 EPROM's and the TM 990/302. This card is required when programming these devices with the TM 990/302 Software Development Module.

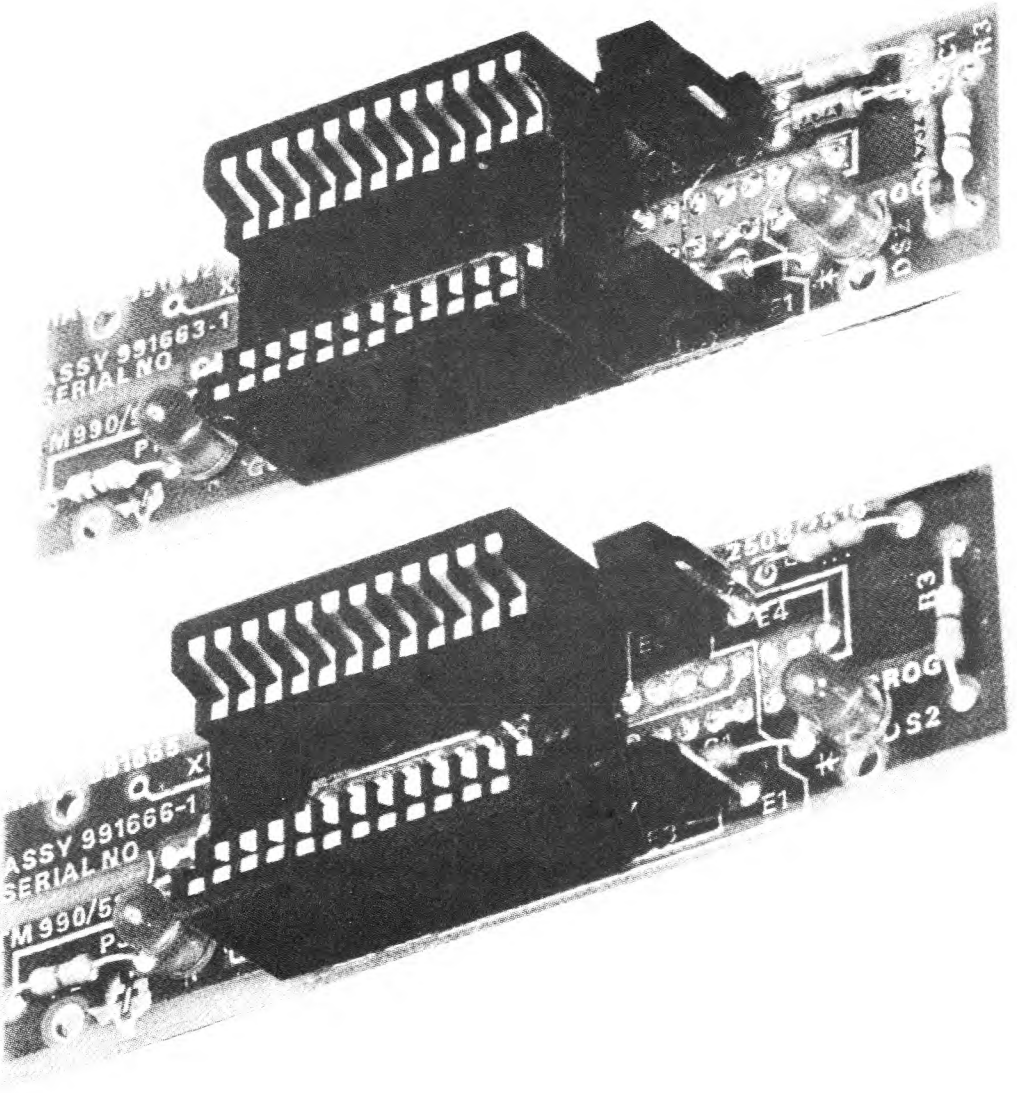


FIGURE 6-6. TM 990/514 AND TM 990/515 EPROM PERSONALITY PROGRAMMING CARDS

SECTION 7

SOFTWARE DEVELOPMENT

7.1 GENERAL

The TM 990 series is supported by a family of software development systems, ranging in capability from a standalone CPU board, the TM 990/189, to hard disc development systems with universal emulation for the 9900 family microprocessors. These systems include:

- TM 990/189 University Board
- TM 990/302 Software Development Board
- FS 990/4 Floppy Disc Development System
- FS 990/10 Floppy Disc Development System
- DS 990 Disc Based System
- AMPL Microprocessor Prototyping Laboratory

The TM 990/189 University Board provides a low cost standalone capability to generate TMS9900 code in assembly language. Its features are described in section 2.5.4. The features of the other development systems are described in following sections.

7.2 TM 990/302 SOFTWARE DEVELOPMENT MODULE

A software development system is shown in Figure 7-1. It consists of a CPU module, power supply, audio cassette/cassettes, software development board and EPROM programmer personality card. The end algorithm is generally related to industrial control with less than 500 lines of code and 10 to 20 target systems in production.

The heart of this low-cost software development system is the TM 990/302 Software Development Board; typical power requirement is +12V @ 132 mA, -12V @ 55 mA, +5V @ 830 mA and 35 to 55V @ 80 mA. This module is used for developing assembly language software to be used on 990/9900 family microprocessor based system. The TM 990/302, a bus-compatible memory of the TM 990 microcomputer module family, provides dual audio cassette interfaces, both static RAM and ROM memory, and hardware circuitry to aid in the programming of read-only memory devices. Used in conjunction with either the TM 990/100M or TM 990/101M CPU modules, the TM 990/302 provides a complete standalone software development system offering support for program generation, editing, assembly, debugging, and EPROM programming. The TM 990/302 provides the following features:

- Dual or Single audio-cassette interface
- EPROM programming options: TMS 2716, TMS 2708, TMS 2532, TMS 2516, TMS 2508
- Optional POWER BASIC development software residing in ROM (12K bytes)
- 2K x 16 RAM

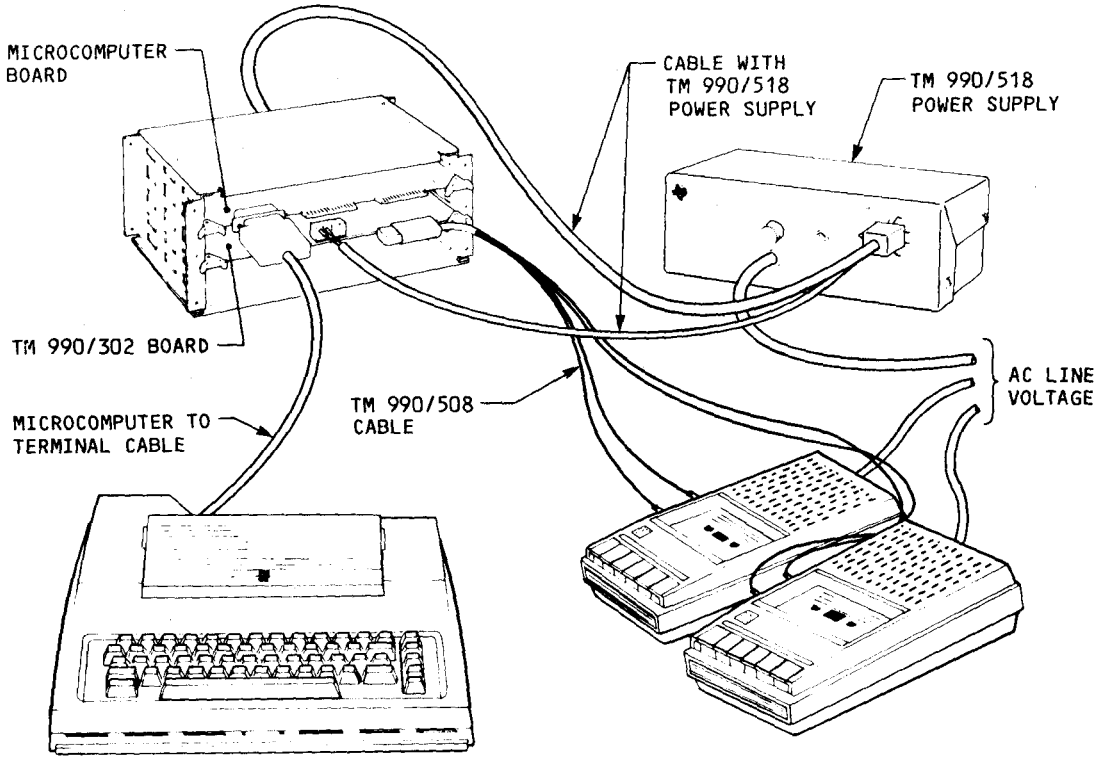


FIGURE 7-1. SOFTWARE DEVELOPMENT SYSTEM

- Software development aids residing in ROM
  - Symbolic Assembler
  - Text Editor
  - EPROM Programmer
  - Relocating loader
  - I/O Scheduler/Handler
  - Debugger

- Memory expandability for additional performance (TM 990/201, TM 990/206, TM 990/203 memory expansion boards)

- EIA communication with other computers

7.2.1 Software Development

Figure 7-2 is a typical software development cycle using the TM 990/302 Software Development board.

7.2.2 Source Text Editing

The text editor provides the means for initial source code entry or program update. Initial source inputs will be from the user's terminal. Source programs on audio cassette will be updated with changes made from the user's terminal. The size of the text editor buffer is determined at initialization as a function of the total RAM.

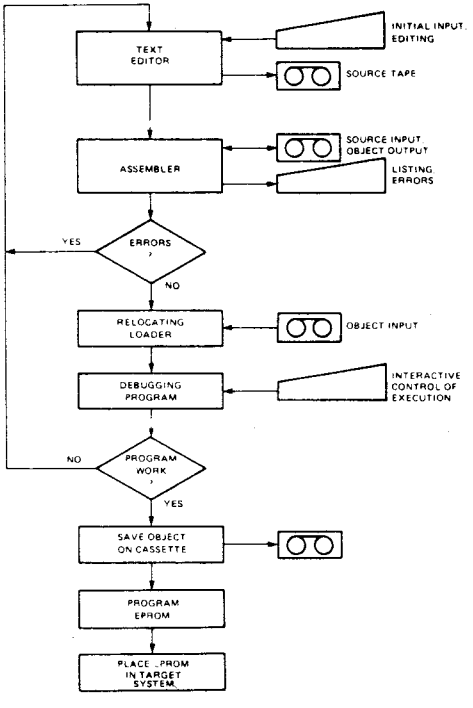


FIGURE 7-2. TYPICAL SOFTWARE DEVELOPMENT EXECUTION

The text editor operates on the source code text in a line mode. Text editor commands with their respective functions are:

D Delete lines n thru m

I Insert at line n with optional line-number autoincrement by m

K Keep (store) buffer and print new top line in the buffer

P Print lines n thru m

Q Flush the input file until end of input file and return to executive

R Resequence output line numbers, giving the initial line number and the increment

To create or update the source program, the text editor provides manipulation of individual lines of code. The designer may delete, insert, print and resequence text from his keyboard. The text editor handles programs of any length by segmenting the source code into "buffer" blocks. It controls buffer loading and storage into cassette-tape memory. The buffer is enlarged by plugging in memory-expansion cards, which also expand the amount of target system memory available for execution.

7.2.3 Assembling Source

The next step in program development is a two pass assembly of TMS 9900, SBP 9900, TMS 9940, TMS 9980, TMS 9985 instruction sets into absolute standard 9900 object code. This two pass assembler allows four-character symbolic addressing. The assembly listing output, including error messages, is routed to a user chosen device.

7.2.4 Debugging

Seven debug commands aid program development after the loader program puts the assembled object into memory. Multi-step trace, software breakpoints and data inspection/changes are featured.

Debug Commands:

SB Set software breakpoint and execute

IM Inspect/change memory

IC Inspect/change CRU

IR Inspect/change registers

RU Run program & trace conditional jumps

ST Single step for 1 or more instructions

DM Dump memory to specified cassette in object format

7.2.5 EPROM Programming

After debug, the EPROM programmer can be invoked to program EPROM's, read back EPROM's into memory, or compare EPROM contents to memory. Byte and word serial formats are available. The EPROM programmer is able to program the following EPROM's: TMS 2708, TMS 2716, TMS 2516, TMS 2532, TMS 2508.

7.3 ADVANCED MICROPROCESSOR PROTYPING LAB (AMPL)

AMPL uses TI's 990 computer and offers 10 MHz trace capability and universal emulation for the 9900 family microprocessors. The AMPL system includes a video display terminal, disk system, and software license.

The lab is available as a floppy disk system or as a hard-disk system that accomodates multiple users. Programs can be edited, assembled, linked, loaded and executed much faster than conventional paper or cassette based systems. Figure 7-3 shows an FS 990 Based AMPL System.

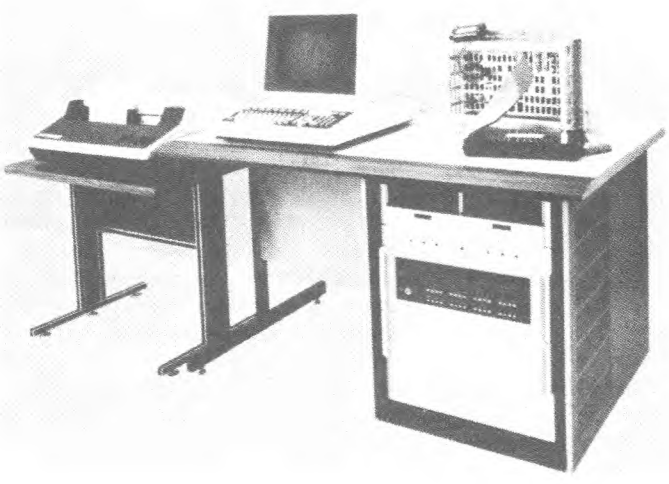


FIGURE 7-3. FS 990 BASED AMPL SYSTEM

The elements of an AMPL system include:

- In-Circuit Emulation Support
- Logic-State Trace
- AMPL Software
- PROM Programming.

In-circuit emulation support permits development and debugging directly on a TM 990 module while monitoring and controlling the operation from AMPL.

Logic-state trace features interactive on-line control and analysis to provide fast data reduction and programmable emulation control based on the results of this analysis.

AMPL software, a high level language, has design features that simplify orientation for the new user yet provide extensive flexibility and support for the experienced user.

PROM programming implements target system memory in PROM and EPROM.

AMPL's interactive process makes it easy to identify and implement design changes. Result: substantial savings in design time and cost.

7.3.1 In-Circuit Emulation Support

The TMS 9900 in-circuit emulation feature includes the TMS 9900 emulator, TMS 9900 buffer, and TMS 9900 target connector. This feature allows the TMS 9900 microprocessor-based system design engineer to simulate his target system by utilizing the dedicated 4096 words of emulator memory and the TMS 9900 microprocessor emulator. All functions of the proposed system can be simulated except input/output, and benchmark data can be tabulated.

TMS 9900 emulation is designed to aid the design engineer through each stage of his prototype implementation. Emulation control provided by the FS990 system allows the design engineer to step through the developed code, setting breakpoints and instruction traces to start/stop tests at desired points within his code.

Two significant advantages included in the emulation feature are the use of dedicated emulator memory and the ability under interactive software control to switch back and forth between target system memory and emulator memory. The dedicated 4096 16-bit words of emulator memory provides a significant speed advantage over systems which utilize host system memory on a cycle-stealing basis. The faster, dedicated emulator memory allows emulation to occur unimpeded at normal target system clock rates. The 9900 emulator is designed so that this dedicated memory can have precedence over target system memory so that even after target system memory is implemented, 9900 code changes can be quickly evaluated and tested before implementing this change in target system ROM/PROM.

7.3.2 Logic-State Trace

The logic-state trace feature adds a dramatic new dimension to the integration and checkout of the target system.

The FS990 system trace/emulation features interactive on-line control and analysis to provide fast data reduction and programmable emulation control based on the results of this analysis.

The trace feature can be interconnected with the emulator module or it can utilize the general-purpose Trace Data Probe. When interconnected to the emulator, the design engineer can trace 256 events of both address and 16-bit data. The Trace Data Probe provides 20 individual logic-line trace probes.

These probes can be used by the design engineer to trace any TTL logic lines desired in his target system. The sampling rate can be controlled by a 10-megahertz internal clock or by an external clock up to 10 megahertz.

Of the 20 trace probes, 4 have a special glitch latch feature and can detect noisy pulses down to 10 nanoseconds in width.

In addition to the 20 trace data probes, 4 general-purpose trace clock qualifier probes are provided to allow the user to prequalify trace conditions based on logic-state conditions within his target system. By using the interactive programming features within the host FS990 system, the design engineer can define procedures and functions to automatically process incoming trace data from these events, perform data reduction looking for defined conditions, display or print only the desired results, or branch into other emulation/trace procedures. Thus, for example, the design engineer can set qualifying conditions and start trace and emulation in a continuous cycle while looking for those random troublesome noise glitches. Upon detecting a glitch, the trace/emulation cycle can be programmed to pause momentarily, analyze and print conditions, and then continue the trace/emulation sequence looking for the next glitch. This feature can mean tremendous savings in manpower and design checkout time since the full speed and power of the 990 computer is processing the problem.

7.3.3 AMPL Software, An Interactive Control Language

The operator interface to the TMS 9900 emulation and the logic-state functions is provided by AMPL software, a higher level language executing within the FS990 system. This interactive microprocessor prototyping language unifies the diverse 9900 prototyping support capabilities into a user-oriented system. AMPL software has designed-in features to simplify orientation for the new user, yet provides extensive flexibility and support for the experienced user. AMPL software features include:

- Block-structured concepts and simple, concise syntax
- Straight forward interactive evaluation and display of expressions
- User- and system-defined procedures and functions
- Interactive display/modification of target memory with instruction level assembly and conversion from internal binary to assembly instruction mnemonics
- Symbolic target system debug
- Dynamic processing of traced data collected by the emulator and trace modules
- Batch-like execution through predefined disk resident sessions

The user-defined procedural and functional support provided by AMPL software allows the user to develop standard support tasks for emulation, debug, and trace data evaluation which can significantly ease the microprocessor application design efforts.

7.3.4 9900 Family Software Development

The TMS 9900 family software support includes a source editor, two-pass assembler, link editor, and debugger. The source editor is an interactive text editor that simplifies the creation and modification of TMS 9900 source code. The two-pass assembler supports the full 9900/990 assembly language and

resultant software can be implemented for the FS990 system and the TMS 9900-based target system. FS990 FORTRAN is a valuable aid to the design engineer for statistical, benchmark and other engineering scientific support. The FS990 FORTRAN meets the American Standard FORTRAN IV (X3.9-1966) requirements.

The FS990 FORTRAN is structured to provide the design engineer capability to utilize FORTRAN subroutines within his target system. Output of the FORTRAN compiler can be defined to produce 9900 object which can be linked into other TMS 9900 code for implementation into the target system.

7.3.5 PROM Programming

Part of every 9900 microprocessor-based target system memory will be implemented in nonvolatile read-only memory. This section may contain only the bootstrap loader program to control loading of the system program into RAM memory, or it may contain all of the target system code. The read-only memory support available with the FS990 system includes BNPF and HIGH/LOW formatted output, and PROM/EPROM implementation using the 990 PROM programming module.

The PROM programming module offers the TMS 9900 user the capability to implement his target system memory in PROM or EPROM. Bipolar PROM devices which can be implemented include SN74188A, SN72S188, SN72S288, SN72S287, SN72S387, SN72S470, SN74S471, SN72S472, and SN74S473. EPROM device includes the TMS 2708. By using the PROM programming module with the FS990 system, the TMS 9900 user can develop 9900 code, test it through in-circuit emulation, and implement it in PROM or EPROM.

7.3.6 Standard Kits And Options

The FS990/4 system includes 990/4 with 24K 16-bit words of memory, dual floppy-disk drives, Model 911 Video Display Terminal, TX990/TXDS system software license, one-year software subscription service, hardware installation* within the continental United States, and programming and user manuals. The system is mounted in a single-bay equipment desk (34 inches deep by 31 inches high by 54 inches wide).

7.3.6.1 FS990 FORTRAN IV Option

This option includes FS990 FORTRAN software object license and one-year software subscription service.

7.3.6.2 Printer Option

The Model 810 Printer is a 132-column, 150-cps, 9 X 7 matrix printer with controller and 30-foot cable.

7.3.6.3 TMS9900/9980 Emulator Options

The TMS 9900/9980 emulator options include the 9900/9980 emulator, either the 9900 buffer module or 9980 buffer module, AMPL software license, one-year software subscription service, and manuals.

* Single service call for hardware installation is included in FS990 system price for the basic system configuration plus any of above listed options, within a 26-mile radius of the nearest Texas Instruments DSG service office. Travel beyond this radius will be in accordance with TI's then-current rates.

7.3.6.4 Logic-State Trace Option

The trace option includes trace support for 16 channels of data or address plus 3 control bits when used with TMS 9900/9980 emulator or 20 channels of general-purpose TTL logic data when used with Trace Data Probe. This function requires one of the TMS 9900/9980 emulator options.

7.4 AMPL MICROPROCESSOR PROTOTYPING LAB (DS990 BASED)

DS990-AMPL systems are based on a TI DS990 Model 4, 6, or 8 computer system with one or more AMPL microprocessor prototyping lab stations.

7.4.1 DS990 Computer

DS990 Model 4, 6, and 8 systems are based on the 990/10 computer, with disk storage, Model 911 Video Display Terminals for operator interaction, and DX10 operation system software.

7.4.2 Standard System Hardware

System hardware includes the Model 990/10 computer with 128K bytes of error-correcting memory; one Model 911 Video Display Terminal with 1920-character display, full-ASCII keyboard, and dual controller to allow expansion; and disk drives appropriate to the model number, as shown in Figure 7-4.

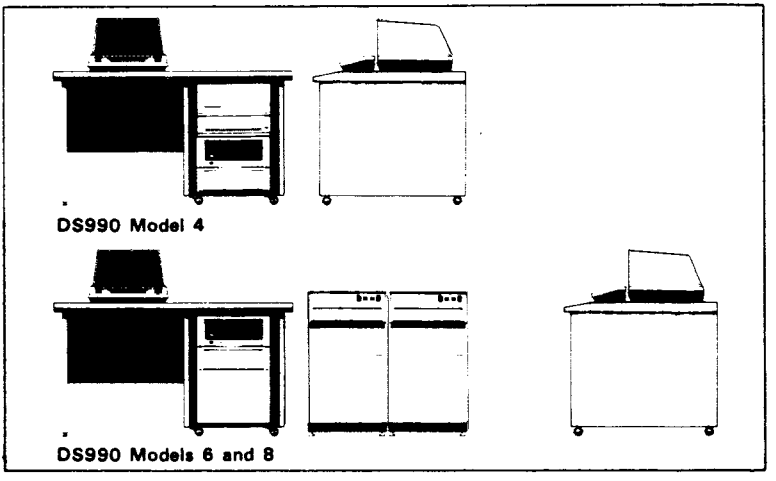


FIGURE 7-4. DS990 SYSTEM DRIVES AND STORAGE

Hardware also includes an equipment rack built into a 54 inch x 20 inch desk unit. Hardware installation includes the basic system, one 810 printer, one expansion 911 VDT, and one AMPL station.

Hard copy is provided by the Model 810 Printer, a 150-character-per-second impact printer with 9 x 7 dot matrix character structure and a 96-character full ACSII print set. It uses sprocket-type paper, 3 to 15 inches wide, and can print 132 columns in either normal (13.2 inches) or compressed (8 inch) format.

An additional Model 911 Video Display Terminal provides expansion of display and keyboard functions, through the second port of the dual controller provided with the standard system; or a dual controller, two displays, and keyboards with two terminals, by using an additional controller.

Disk expansion (Model 4 system only) is accomplished with the use of a secondary Model DS10 Disk Drive using the two-drive controller provided with the system.

An expansion chassis is required for two or more AMPL stations. Expansion requires a CRU expansion kit, which provides an interface and chassis to support a total of two AMPL stations; a TILINE interface kit to support 128K bytes of memory in the above chassis; and a single-bay pedestal cabinet or table top dust cover for the expansion chassis.

Other peripherals may include line printers, such as Models 2232/2260 with 300 and 600 lines per minute, respectively; disk drives, such as the Model FD800 Floppy Disk Drive, or Model DS31 (2315-type cartridge disk); Model 979A Magnetic Tape Drive (1600bpi); and up to 128K bytes of additional ECC memory expansion in each expansion chassis.

7.4.3 Standard System Software

A TI DX10 disk system software license, with installation and one-year update service, is included with the DS990 system. The software includes a disk-based operating system with comprehensive file management and software development support in batch and interactive modes. DX10 provides development tools including an interactive text editor, macro assembler, and link editor. Several optional programming languages are supported.

Interactive Text Editor. Edit operations allow modification, insertion, and deletion of entire records or of character strings within records. Edit operations are initiated via edit keys directly or by command. When operations are initiated by commands, parameters are prompted by DX10.

Macro Assembler. The DX10 system assembler is the most powerful of the 990 family assemblers. In addition to accepting standard 990 assembly-language instructions, the macro assembler is extended to include a macro facility, support for FORTRAN common segments, and conditional assembly. The macro facility provides character string manipulation, access to binary values in the symbol table, and support for macro definition libraries.

The relocatable object code produced by the assembler may be partitioned in segments. Common blocks, program segments, and data segments are assigned separate location counters. A sequence of assembly-language statements may be conditionally processed depending on the value of an assembler arithmetic or logical expression. Directives are provided to specify the amount of information in the assembly listing.

Link Editor. The DX10 system link editor accepts relocatable object code generated by the assembler, FORTRAN compiler, or COBOL compiler, and combines the individual modules into a linked-load module. References between the modules are resolved to their correct values. Common blocks, program segments, and data segments are colleted, and each segment type assigned to its own contiguous area of memory.

The Link Editor accepts control statements that may specify the use of shared procedures and the use of overlay structures. Available options include generation of a load map, search of a set of object libraries to automatically resolve unresolved values, and a partial link that leaves external references to be resolved at a later time. Output of the link editor may be an installable object file or may be written directly into memory image in a program file or DX10 image file.

Optional Languages. The FORTRAN compiler, available as a DX10 option, comforms to the American National Standsards Institute (ANSI) standard FORTRAN, or FORTRAN IV. The compiler also incorporates the extensions recommended by the Instrument Society of America in their document ISA-S-61.1, 1975, and in their document ISA-61.2, 1976.

Texas Instruments has incorporated other useful attributes into the FORTRAN compiler to provide for more effective coding and program development. These added features include direct disk I/O, overlapped I/O, free-format source input, internal data manipulation statements, and literal character strings represented in quotes. Also included are vaiable names of any length, double-word (32-bit) integer data type, implicit variable typing, general integer expressions in subscripts, data statements array names, mixed-mode expressions, Hollerith and hexadecimal constants and assignments, scaled binary data types, copy directives, and accept and display commands for interfacing with a VDT.

Optionally, the compiler can generate a cross-reference listing for each variable in the program, provide a debug module that references specific line numbers in the source program traversed during execution, provide conditional compilation, allow free format, and generate 990/9900 assembly language instead of object code.

A FORTRAN function library is provided that includes all intrinsic functions and basic external functions defined in the ANSI standard. This library contains all runtime support to interface with the DX10 operating system. In addition, several generally useful routines, such as random number generation, are also provided. Additional libraries are provided to allow execution of FORTRAN programs under TX990 operating system or in a limited stand-alone mode. FORTRAN compiler output can also be linked into other 9900 code for implentation in the target system.

Other Languages. Other languages, such as COBOL, BASIC, and Business BASIC, are available for users who want to extend the application of their DS990 systems beyond microprocessor development.

7.4.4 AMPL

A DS990-AMPL lab supports up to four lab stations, each consisting of a Model 911 video display terminal, AMPL emulator kit, and AMPL logic-state trace module. Although equipment will generally be grouped into convenient work areas with a terminal near each set of AMPL modules, a station is actually defined by an AMPL language command which assigns an emulator module and trace module to a terminal. The resulting flexibility is useful when several users need access to the same emulator (at different times) or when one user needs access from two locations (e.g., lab and office).

Model 4,6, and 8 AMPL emulator kits include emulator hardware and AMPL software on the corresponding system disk, with installation and one-year

update service. Only one kit with software is required. For additional stations, AMPL emulator hardware kits include emulator hardware only. AMPL modules are interchangeable between DS990-AMPL and FS990-AMPL, and the AMPL language syntax is the same for both systems.

7.4.4.1 AMPL Language.

AMPL software is a high-level prototyping language that controls debug functions, and executes under the DX10 operating system. AMPL unifies the prototyping capabilities into a user-oriented system by allowing the user to initiate and control each operation interactively from the terminal and to design and store procedures which execute without manual intervention. AMPL software has designed-in features to simplify orientation for the new user yet provides extensive flexibility for the experienced user. AMPL software features include:

- High-level language constructs such as IF-THEN-ELSE, WHILE-DO, REPEAT-UNTIL, which support structured programming techniques
- User-controlled display formats in binary, octal, decimal, hexadecimal, or 990 assembly language mnemonics (disassembly)
- Procedure and function declaration for design of user routines and subroutines
- Arithmetic and boolean expression evaluation
- Library procedures and functions for commonly used operations, such as initialization, dumps, searches, traces, breakpoints, and single instruction execution
- Dynamic processing of traced data collected by the emulator and trace modules
- Single-line assembly and disassembly during debug
- Batch execution of predefined disk-resident sessions
- Saving sessions on disk for later use

The user-defined procedure and function support provided by AMPL software allows the user to develop standard support tasks for emulation, debug, and trace data evaluation that can significantly ease microprocessor application design efforts. For example, an infrequent or random error condition can be debugged by writing an AMPL procedure to set up the error mode in the target, run the target system until the error occurs, and make a record of system operation before and after the error.

7.4.4.2 Emulator Kits.

An emulator kit includes three hardware items: the TMS9900 emulator, TMS9900 or 9980 buffer, and the target system connector. The connector plugs into the microprocessor socket of the target system. This extends all the microprocessor input and output lines through an 18-inch cable to the buffer module. Electrical characteristics of the connector and cable closely approximate the characteristics of the microprocessor to duplicate loading effects on the target system.

The buffer module contains a microprocessor with bidirectional three-state line drivers for communication with the emulator module and the target system. The buffer is unique for each microprocessor type to be emulated. Buffers are currently available for the TMS 9900 and TMS 9980. Any combination of buffers can operate on the same system.

A 6-foot flat ribbon cable connects the buffer module to the emulator module. The emulator contains two random access memories, an 8K-byte emulator user memory and a 512-byte emulator trace memory. An AMPL command allows the emulator user memory to take precedence over any target system memory in the same address space. Programs may be loaded into the emulator user memory and executed as though they were stored in the target system's RAM or ROM, using normal target system memory timing. Thus firmware changes can be fully and quickly evaluated before being implemented into PROM or EPROM.

The emulator trace memory can be used in the same manner. The primary use of the trace memory, however, is to trace activity on the address bus. An AMPL command allows the user to select whether all addresses or only instruction addresses are to be traced.

The trace operation does not introduce any "wait" states or affect the speed of execution in any way. The emulator trace may be activated for a discrete number of samples (1 to 256) or in a continuous mode. In continuous mode, the trace wraps around the 256-word memory unitl a selected breakpoint halts the microprocessor. When execution halts, the trace memory contains the last 256 qualified addresses.

7.4.4.3 Logic-state Trace Module.

Expanding the emulator module's trace function, which is dedicated to the microprocessor address bus, the logic-state trace module is a versatile, general-purpose logic analyzer on a single logic board. The dials and switches which usually appear on a logic analyzer are replaced by AMPL commands. The traced data is displayed on the terminal screen in formats which are selected by AMPL commands or procedures.

Input data to the trace module is supplied either by a short data cable from the emulator module or a general-purpose trace-data probe which connects to TTL-level signals in the target system hardware. The trace data probe consists of a 6-foot ribbon cable with a board edge connector on one end and a terminator box on the other end. The terminator box has twenty-six color-coded probe leads which mate with wire-wrap pins or spring-loaded clips. Isolation resistors in the terminator box minimize the loading effects of the probes. The test leads allow connection to twenty data channels, four trace qualifiers, external clock (up to 10 MHz), and a trace-event trigger.

The trace memory records up to 256 samples of 20-bit data. The data may be individual TTL signals from the trace data probes attached to the target system, or it may be microprocessor bus control signals and either address bus or data bus words from the emulator module. By using the qualifier lines, unnecessary or undesired samples may be ignored to make the best use of trace memory space.

The high-speed trace memory allows data to be sampled at rates up to 10 MHz. Four of the input lines may be programmed as "glitch catchers." The glitch catchers can capture pulses as narrow as ten nanoseconds and hold them for recording on the next sampling clock.

An internal crystal controlled clock circuit supplies a 10 MHz clock. Use of the internal clock allows the user to sample signals which are not synchronized with the microprocessor system clock. It also allows finer resolution than is possible with the 3 MHz system clock. An AMPL command allows selection of the trace module internal clock or an external clock signal up to 10MHz. The external clock signal is supplies from the emulator if the emulator data cable is installed. If the trace-data probes are used, the external clock is supplied by a lead attached to the target system hardware.

An event function preset by an AMPL command allows 1 to 65,536 occurrences of a programmed trace input before outputting a trace. A delay function determines where in the 256-word trace the event will be placed. For example, it is possible to select the 400th iteration of a loop and record the trace information with 100 samples before and 155 samples after the event.

SECTION 8

TM 990 SYSTEM BUS

8.1 INTRODUCTION

The TM 990 System Bus provides the standard electrical and mechanical interface for interconnection of the various processors, memories and I/O modules of the TM 990 family. Physically implemented on the system chassis back plane, the TM 990 system bus consists of a set of 100 signal lines. This bus has been specifically designed to offer a high degree of flexibility, thus enabling systems designers to define the optimum system configurations suited to their particular applications. This flexibility can also be of great benefit for established systems in easing the task of reconfiguration should system requirements change or when a system upgrade is required to add new capabilities. The structure of the bus, however, is such that the bus interface circuitry required on each module can be quite simple; this is a particular advantage when custom module design is required, and for ease of system check out and maintenance.

This section contains a general description of the TM 990 system bus, and its characteristics. A detailed description of the bus, including timing details, is contained in the "TM 990 System Specification".

8.2 TM 990 BUS DESCRIPTION

The TM 990 system bus has the following signal group assignments:

28 lines - power and ground
20 lines - address bus
16 lines - bidirectional data bus
18 lines - control bus
3 lines - communication register unit bus
15 lines - prioritized vectored interrupts

Figure 8-1 categorizes each pin in the TM 990 system bus into one of the above bus groups, and shows the signal assigned to each pin. Each signal is defined in the appropriate detailed bus group description.

8.2.1 Power Bus

This group of lines is intended to provide regulated DC voltages to all modules requiring them. Whenever possible, modules should operate only from the +5 volts supply lines. A VBATT power bus is included to allow inclusion of battery backup during power down (for memory retention), and an auxiliary line VAUX is available for special requirements. The power bus contains the following voltages:

Voltage	No. of Lines
+5V	4
+12V	2
-12V	2
VBATT	2
VAUX	2
GND	16

TABLE 8-1. TM 990 SYSTEM BUS PIN DEFINITION

Pin	Signal	Group	Pin	Signal	Group
1	GND	Power/Ground	2	GND	Power/ground
3	+5V		4	+5V	
5	INT8-		6	INT7-	
7	INT10-		8	INT9-	
9	INT12-		10	INT11-	
11	INT14-	Interrupt	12	INT13-	Interrupt
13	INT2-		14	INT15-	
15	INT3-		16	INT1-	
17	INT5-		18	INT4-	
19	IAQ	Control Bus	20	INT6-	
21	GND		22	BUSCLK-	
23	GND	Power/Ground	24	REFCLK-	
25	GND		26	RESERVED	
27	GND		28	RESERVED	
29	CRUIN	CRU Serial Bus	30	CRUOUT	CRU Serial Bus
31	GND	Power/Ground	32	BUSY	Control Bus
33	D0		34	D1	
35	D2		36	D3	
37	D4		38	D5	
39	D6	Data Bus	40	D7	Data Bus
41	D8		42	D9	
43	D10		44	D11	
45	D12		46	D13	
47	D14		48	D15	
49	VAUX	Power/Ground	50	VAUX	Power/Ground
51	VBATT		52	VBATT	
53	XA0		54	XA1	
55	XA2		56	XA3	
57	A0		58	A1	
59	A2		60	A3	
61	A4	Address Bus	62	A5	Address Bus
63	A6		64	A7	
65	A8		66	A9	
67	A10		68	A11	
69	A12		70	A13	
71	A14		72	A15	
73	-12V		74	-12V	Power/Ground
75	+12V		76	+12V	
77	GND		78	WE-	
79	GND	Power/Ground	80	MEMEN-	
81	GND		82	DBIN	
83	GND		84	MEMCYC-	
85	GND		86	HOLDA	Control Bus
87	CRUCLK-	CRU Serial Bus	88	IORST-	
89	GND	Power/Ground	90	READY	
91	GND		92	HOLD-	
93	RESTART	Control Bus	94	PRES-	
95	Grantout-		96	GRANTIN-	
97	+5V	Power/Ground	98	+5V	Power/Ground
99	GND		100	GND	

Although a -5 volt line is not included on the TM 990 bus, this voltage may be derived from on-board regulation of the -12 volts.

All voltages are specified to be ±3%. Individual systems requirements will dictate which set of the above are needed and thus guide the selection of appropriate power supplies.

8.2.2 Address Bus

The address bus consists of 20 three-state address lines. These 20 lines are comprised of a set of 16 basic address lines, A0 through A15, and a set of four extended address lines XA0 through XA3. The address bus is used to access memory locations, CRU bits and for memory mapped I/O.

For most applications, a 16-bit byte address is formed with A0 as the most significant bit (MSB) and A15 as the least significant bit (LSB). These 16 bits permit a processor to address up to 64K bytes. For word addresses, line A15 is held low and A14 becomes the LSB. A processor can address up to 32K words. The four extended address lines permit a processor to use memory mapping to address up to 1M bytes. Lines XA0 (MSB) and XA3 (LSB) form the most significant part of the 20-line address bus. Memory mapping is discussed in detail in section 8.3.

Memory-mapped I/O permits TM 990 I/O modules to be addressed (for data transfer) in the same manner as a memory location; data transfer takes place on the TM 990 data bus. All 20 address lines may be used to access memory mapped TM 990 I/O modules; normally these modules should not have the same addresses as memory locations. Most TM 990 I/O modules, however, because of cost, simplicity and flexibility will use the Communications Register Unit (CRU). Each bit in the CRU is addressed individually or in groups by the processor, using the 12-bit address field formed with address lines A3 through A14.

All 20 address lines are controlled by the master processor unless disabled by the activation of HOLD-. The address lines are not terminated on the system backplane.

8.2.3 Data Bus

The data bus consists of 16 bi-directional three-state data lines, D0 through D15. This bus is used by processors and Direct Memory Access (DMA) modules to make parallel memory data transfers and by memory mapped I/O modules to make parallel I/O data transfers. The data bus represents data words with D0 as the MSB and D15 as the LSB. The direction of the data transfer taking place on the bus is determined by the state of signal DBIN.

The data bus is controlled by the master processor unless disabled by activation of HOLD-. The data lines are not terminated on the system backplane.

8.2.4 Control Bus

The control bus is comprised of 15 signal lines which control all data transfer transactions on the TM 990 bus and permit module synchronization and set up. The control bus has several functional subsets as described below.

8.2.4.1 Memory Control Signals

MEMEN- Memory Enable: When active (low), it indicates that the address bus contains a memory address, and that a memory access is in progress. MEMEN- may remain active for several consecutive memory cycles. It is inactive (high) during CRU cycles. MEMEN- is a three-state signal controlled by the master processor unless disabled by activation of HOLD-. MEMEN is terminated on the system backplane.

MEMCYC- Memory Cycle: When active (low), it indicates that a memory cycle is in progress. MEMCYC- is activated one BUSCLK cycle after MEMEN- is made active, and remains so only for a single memory cycle. MEMCYC- is normally released on the second BUSCLK- following the receipt of the READY signal. A memory cycle can be extended, however, by holding MEMCYC- active. MEMCYC- is a three-state signal controlled by the master processor unless disabled by activation of HOLD-. MEMCYC- is terminated on the system backplane.

DBIN Data Bus In: When active (high), it indicates that the processor has disabled its output buffers to allow memory to place read data on the data bus during MEMEN-. DBIN remains low in all cases except during a memory read cycle. It can be used in conjunction with an active MEMEN- signal to indicate the data direction during a memory cycle. (When high, a read cycle is in progress, and when low, a write cycle is in progress.) DBIN is a three-state signal controlled by the master processor unless disabled by activation of HOLD-. DBIN is terminated on the system backplane.

WE- Write Enable: When active (low), it indicates that data to be written into memory is present on the data bus. WE- is a three-state signal controlled by the master processor unless disabled by activation of HOLD-. WE- is terminated on the system backplane.

READY Ready: When active (high), this indicates that memory will be ready to complete its read or write operation during the next BUSCLK- cycle. When a not-ready condition is indicated during a memory operation, the processor suspends operation and enters a wait state until the memory indicates that it is ready. READY is driven by an open collector device and is not terminated on the system backplane.

8.2.4.2 Timing and Synchronization Signals

BUSCLK- Bus Clock: Generated on the primary processor, BUSCLK- is distributed throughout the system for synchronization of memory and bus arbitration functions. Synchronization is to the low-to-high transition of BUSCLK-. BUSCLK- is terminated on the system backplane.

REFCLK- Reference Clock: Generated on the primary processor, REFCLK- is distributed throughout the system as a timing reference for I/O devices, timers and counters. REFCLK- is terminated on the system backplane.

8.2.4.3 Direct Memory Access Signals

HOLD- Hold: When active (low), it indicates that a DMA device is contending for priority and is requesting the master processor to relinquish the system bus. HOLD- is driven by an open collector device.

HOLDA Hold Acknowledge: When active (high) this signal indicates that the master processor has relinquished the system bus to a requesting DMA device.

8.2.4.4 Bus Arbitration Signals

The TM 990 system bus employs a serial arbitration scheme with positional priority. The signals are:

BUSY- Bus Busy: When active (low) this signal indicates that a processor or DMA device has established control of the system bus and is undergoing a memory data transfer. BUSY- is driven by an open collector device.

GRANTIN- Grant Input: When active (low) this signal indicates to a processor or DMA device that no higher device is using or requesting the system bus. Processors must monitor both GRANTIN- and BUSY- before asserting bus mastership.

GRANTOUT- Grant Output: When active (low) this signal indicates to the next lower priority processor or DMA device that it may assert bus mastership if required. When requesting the system bus, devices must deactivate this signal to prevent lower priority devices from asserting bus mastership.

8.2.4.5 Miscellaneous Signals

IORST- I/O Reset: This signal is generated by the primary processor. When active (low), it indicates a system reset and that all I/O modules should be reset to their initial or idle condition. This signal is active for two cycles of REFCLK-. IORST- is terminated on the system backplane.

PRES- Power On Reset: Normally generated by the system power supply during power up. When active low, PRES- resets the primary processor which, in turn, issues an IORST- to the system. PRES- must remain active for 100 nsec after all power voltages are stable. This is an asynchronous signal and is intended for system initialization or full system reset if activated after initialization. PRES- is driven by an open collector device.

RESTART- Restart: When active (low), this signal causes the primary processor to perform a load function. No resets are generated. RESTART- is an asynchronous system input signal and must remain active for a minimum of 100 nanoseconds. RESTART is driven by an open collector device.

IAQ Instruction Acquisition: When active (high) this optional signal indicates that the primary processor is performing an instruction fetch memory cycle. IAQ may be used as a diagnostic and to detect illegal instruction codes.

8.2.5 Communications Register Unit Bus

The Communications Register Unit (CRU) bus consists of three lines used to conduct bit oriented serial input or output operations under software control. During CRU operations, the memory control signal MEMEN- is high, indicating that the address bus lines A3 through A14 contain the address of the single CRU bit to be operated on. The three CRU bus lines are:

CRUIN: The serial data input line to the primary processor. During CRU input operations the processor samples the CRUIN line to read the data bit whose

source is identified by the 12-bit address field. This is a three-state line to which all CRU input modules are connected.

CRUOUT: The serial output data line from the primary processor. During CRU output operations the processor puts the data on this line which is to be placed into the destination address.

CRUCLK-: The CRU clock is output from the primary processor during CRU output operations. CRU output modules connected to the system bus should sample the data from the CRUOUT line on the low to high transition of CRUCLK-.

8.3 MEMORY

The TM 990 address bus contains 20 separate lines, a basic set of 16 (A0 through A15) and an extended set of four (XA0 through XA3). This 20-bit address field permits the TM 990 system bus to support a memory capacity of up to one megabyte (1,048,576 bytes) with memory mapping. This memory can be made up of masked ROM, field-programmable ROM (PROM), erasable PROM (EPROM), static RAM (SRAM), and dynamic RAM (DRAM). The systems designer has the flexibility to choose the combination which best meets his application. The TM 990 product family provides a series of processor and memory expansion modules which can be combined to form the required configuration. Since the address space is shared by processor on-board memory, expansion memory and memory mapped I/O, care must be exercised when configuring a system not to overlap addresses on the various functions, except in specific cases where bus conflicts are avoided (for example it might be desireable to write to a mapped I/O device and a RAM location simultaneously).

8.3.1 Paged Memory Mapping

For most systems applications, the 64K-byte memory capacity addressable by the basic set of address lines A0 through A15 will be more than adequate. For those systems requiring additional memory capacity, the total addressable memory can be increased to one megabyte by use of memory mapping. Memory mapping is a technique which enables the processor's basic 16-line address field to be expanded into a 20-line address field. This process is illustrated in Figure 8-1.

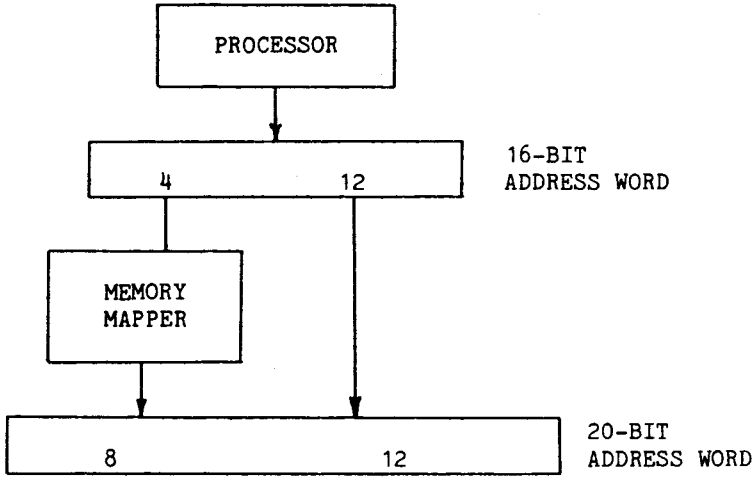


FIGURE 8-1. PAGED MEMORY MAPPING

The four most significant bits of the processor's basic address field are used by the memory mapper to access one of sixteen 8-bit codes stored within the mapper. This 8-bit code from the mapper is put onto the extended memory address bus to form the most significant part of the extended memory address. The least significant 12 bits of the extended memory address are the unaltered least significant 12 bits of the basic address from the processor. Figure 8-2 shows the structure of this extended memory address word.

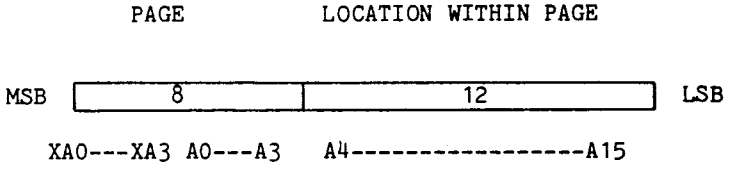


FIGURE 8-2. EXTENDED MEMORY ADDRESS WORD

For each of the 8-bit codes obtainable from the memory mapper, there are 2^{12} or 4096-byte addresses available to the processor. Each set of 4096 (4K) addresses is considered to be one page of memory. Changing the 8-bit code from the mapper is equivalent to changing the page of memory. The 8-bit field from the memory mapper allows up to 256 pages in the system. The four most significant address bits from the processor, however, can address only one out of 16 pages at a time. This is illustrated in Figure 8-3.

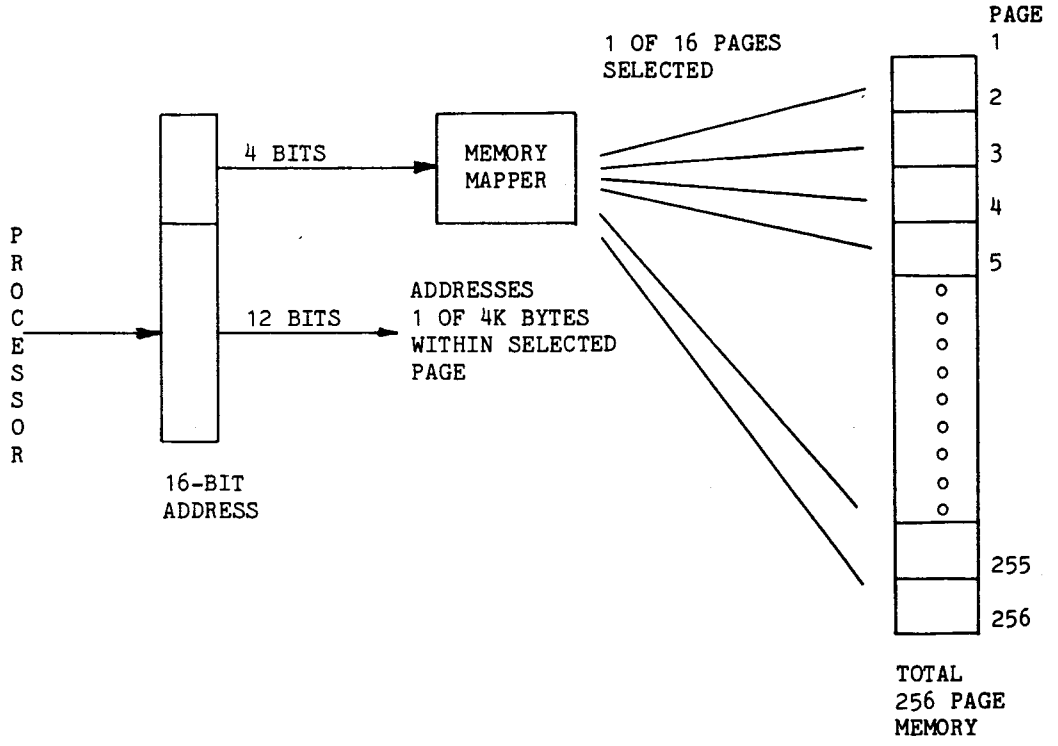


FIGURE 8-3. MEMORY ADDRESSING WITH PAGED MEMORY MAPPING

To utilize the entire 256 pages of memory the 16 8-bit codes of the memory mapper are dynamically altered by the processor under software control.

8.4 INPUT/OUTPUT

The TM 990 system bus provides three modes of I/O interfacing. Each mode has its own characteristic advantages and disadvantages which must be considered when designing a system. The systems designer has the flexibility to choose those modes best suited to his application, and may use any combination of modes as desired; these three modes are communications Register Unit (CRU), memory mapped I/O, and Direct Memory Access (DMA).

8.4.1 Communications Register Unit

The Communications Register Unit (CRU) is the simplest of the three I/O modes supported by the TM 990 system bus. CRU data transfers between the processor and the I/O device take place on serial data lines. (Input and output transfers take place on different lines under software control.) The CRU is a bit-oriented I/O system and the software can transfer from 1 to 16 bits into or out of the processor at a time (in a serial string). The condition of Lines A3 and A14 on the address bus define which bit is to be operated on (that is, input or output); this 12-bit address field allows a possible 4096 input bits and 4096 output bits to be utilized. For multiple bit operations, the address is automatically incremented as each data bit is transferred (Each CRU bit is always addressed individually). Although it would appear that the addresses of the CRU conflict with the memory addresses, MEMEN is always inactive (high) while CRU I/O is in progress; thus a memory cycle will never occur while CRU I/O addresses are present. The basic configuration of CRU modules are illustrated in Figure 8-4.

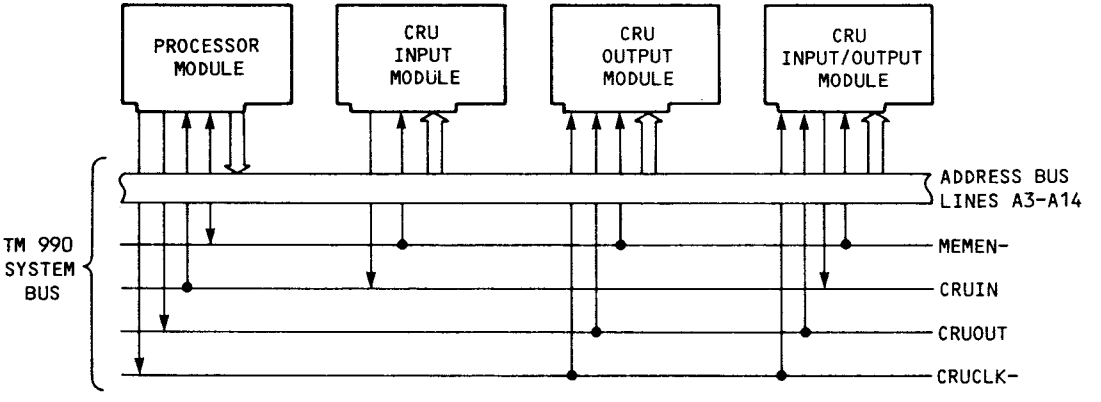


FIGURE 8-4. CRU CONFIGURATIONS

Three types of CRU modules can be implemented as shown above: CRU input only modules, CRU output only modules and CRU input/output modules. Additionally, CRU may be implemented with other I/O modes on the same module. For example, a peripheral device controller module may have a high data transfer rate, thus cycle stealing DMA is selected to implement the data transfers, but CRU is selected as a simple, convenient means for the processor to pass commands to the controller (number of words to transfer, starting location address, read or write and so forth). Although only three CRU modules are shown in the system above, any number of modules can be used and each module may be assigned any number of input and/or output bits required so long as the total system availability of 4096 input and 4096 output bits is not exceeded. In

the interests of simplicity, however, it is best to allocate 32 bits or multiples of 32 bits to each module. Doing this will ease both hardware setup and software generation.

8.4.1.1 CRU Input

When the processor executes a CRU input instruction the MEMEN- signal is deactivated (high) and the bit address appears on the address bus. The CRU module must place the addressed bit onto the CRUIN line, which the processor samples at the appropriate time. This is shown in Figure 8-5.

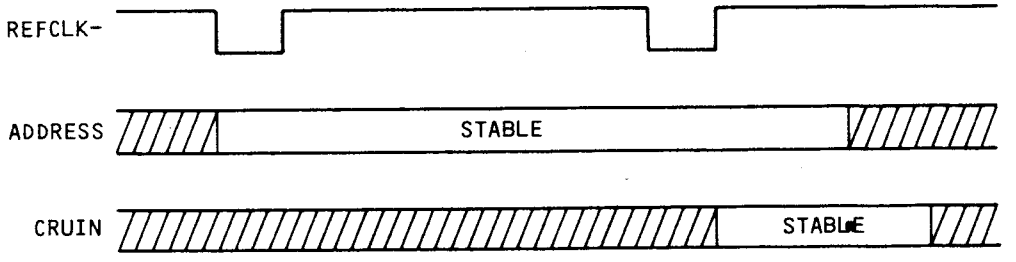


FIGURE 8-5. CRU INPUT TIMING

CRU input modules are required to continuously monitor the address lines and enable the addressed bit onto the CRUIN line. MEMEN may be used by the CRU input module to disable address decode during memory cycles, but this is not a system requirement. If a CRU input module responds to an address during a non CRU input operation, the processor simply ignores any data present on the CRUIN line. CRUCLK is inactive during CRU input operations.

8.4.1.2 CRU Output

When the processor executes a CRU output instruction, the MEMEN- signal is again deactivated and the bit address appears on the address bus. In this case, however, the processor places the data bit onto the CRUOUT line and generates a CRUCLK- pulse which the CRU output module uses to strobe the data bit into the correct destination address. This is shown in Figure 8-6.

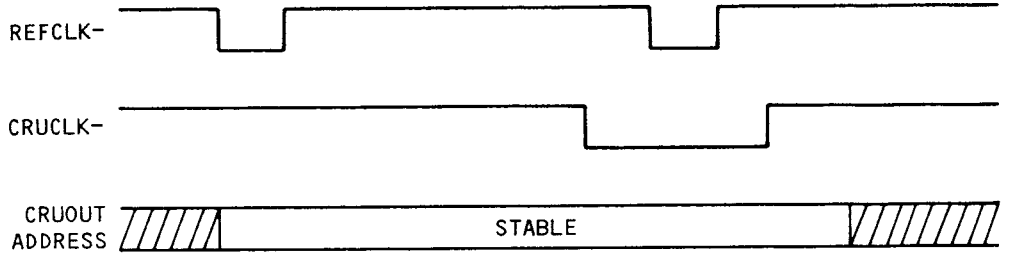


FIGURE 8-6. CRU OUTPUT TIMING

More than one CRU output module may share the same set of addresses permitting the processor to "broadcast" data to these modules simultaneously during execution of a single CRU output instruction. This feature, however, cannot

be used with CRU input modules, as the data from several responding modules would interfere with each other and be meaningless.

8.4.2 Memory Mapped I/O

Memory mapped I/O permits the processor to make I/O data transfers as though memory data transfers were taking place. This is shown in Figure 8-7.

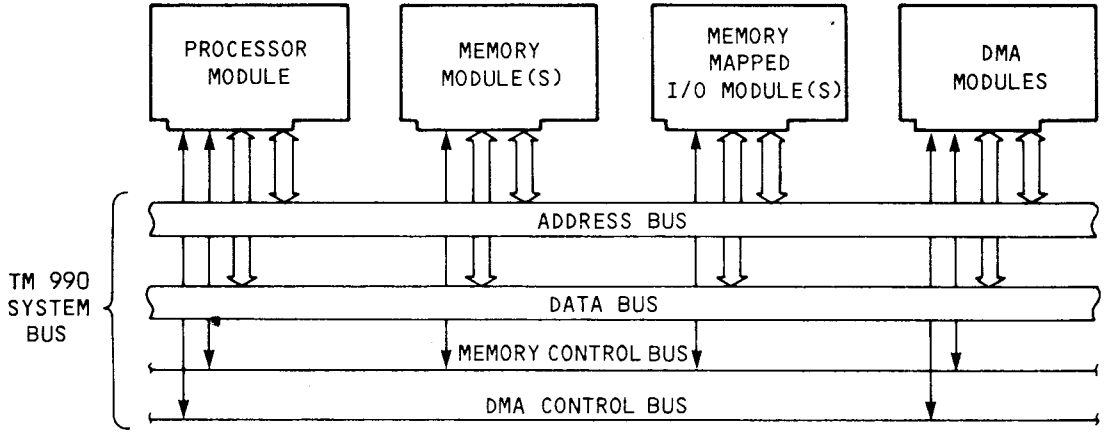


FIGURE 8-7. MEMORY MAPPED I/O

Memory mapped I/O modules connect to the TM 990 system bus in exactly the same manner as do external memory modules, and have an identical interface as do the memory modules. Memory mapped I/O modules share the available memory address space with the system memory and caution must be exercised when duplicating the same address fields on both, in order to prevent bus conflicts. This is discussed further in the memory section. Memory mapped I/O permits the rapid transfer of 16-bit parallel data words between the processor and the outside world under direct software control. This may offer a cost advantage over DMA control,if the data transfer rates are low enough to permit the use of memory mapped I/O.

8.4.3 Direct Memory Access

Direct Memory Access (DMA) is used primarily when there is a requirement for a device to transfer blocks of data to/from memory at high speed without interaction of the master processor. In a typical DMA transfer sequence, the processor initiates the transfer by "setting up" the DMA controller on the peripheral module as a result of executing a software sequence. The DMA controller then acquires the system memory independently of the processor and makes the required data transfers directly to the memory. Upon completion of the data transfers the DMA controller updates a status word and interrupts the processor to indicate that the data transfer operation is complete.

8.4.3.1 DMA Operation

DMA can occur in two modes, block transfer and cycle stealing. Both nodes use the processor HOLD- capability and either can be used for DMA module design. The DMA process can be divided into three distinct phases as shown in Figure 8-8.

1 Acquisition of memory control from the system

2 Memory control by the DMA module

3 Release of memory control to the system

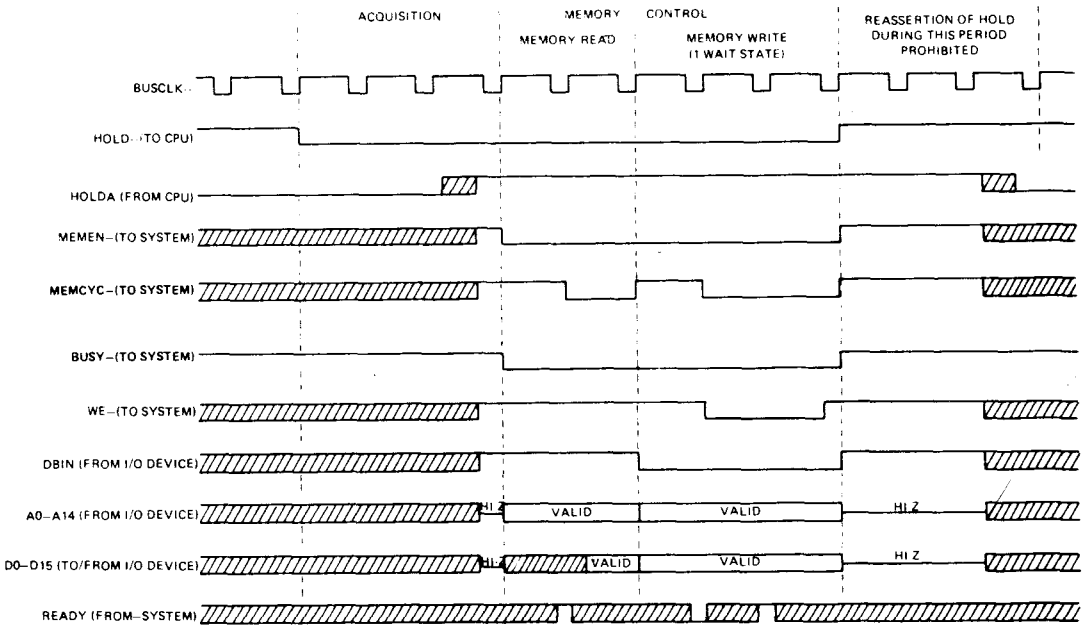


FIGURE 8-8. DIRECT MEMORY ACCESS

The acquisition of memory control from the system begins when the HOLD- signal is asserted by the DMA device. This is an open-collector signal and the DMA controller must synchronize it with the low-to-high transition of BUSCLK-. On receipt of HOLD- the processor enters the hold state at the beginning of the next available non-memory cycle, and activates HOLDA to acknowledge transfer of memory control to the DMA controller. While HOLDA is active, the processor address lines, data lines, DBIN, MEMEN-, MEMCYC- and WE- remain in the high impedance state, and control of these lines is by the DMA controller as shown in Figure 8-9. Note that BUSCLK- comes from the primary processor even when a DMA module has control of the bus. The acquisition phase ends at the first low-to-high transition of BUSCLK- following receipt of HOLDA by the DMA controller.

The control of memory by the DMA device begins at the completion of bus acquisition from the processor. With control of memory established, the DMA controller can make the required data transfers in either cycle-stealing or in block mode. In either mode, these data transfers must comply with the memory timing requirements for a memory data transfer. In cycle stealing mode, the DMA controller will make one data transfer to or from memory and then release memory control back to the system. The DMA controller must then reacquire control of the bus for every word of data to be transferred. In block mode,

the DMA controller retains control of memory for as long as is required to transfer an entire block of data. The system designer must weigh the implication of each mode carefully before choosing. The cycle stealing mode has the least impact on the processor but can take longer to make transfers. The block mode transfers large blocks of data rapidly but may require synchronization with dynamic RAM refresh or interfere with critical processor timing.

The release of memory control to the system begins when HOLD- is released by the DMA controller and is complete when the processor correspondingly releases HOLDA. The processor may require several clock cycles to release HOLDA, and re-assertion of HOLD- by the DMA is prohibited during this time. Loss or modification of memory data will result if the DMA device does reassert HOLD- before the processor removes HOLDA.

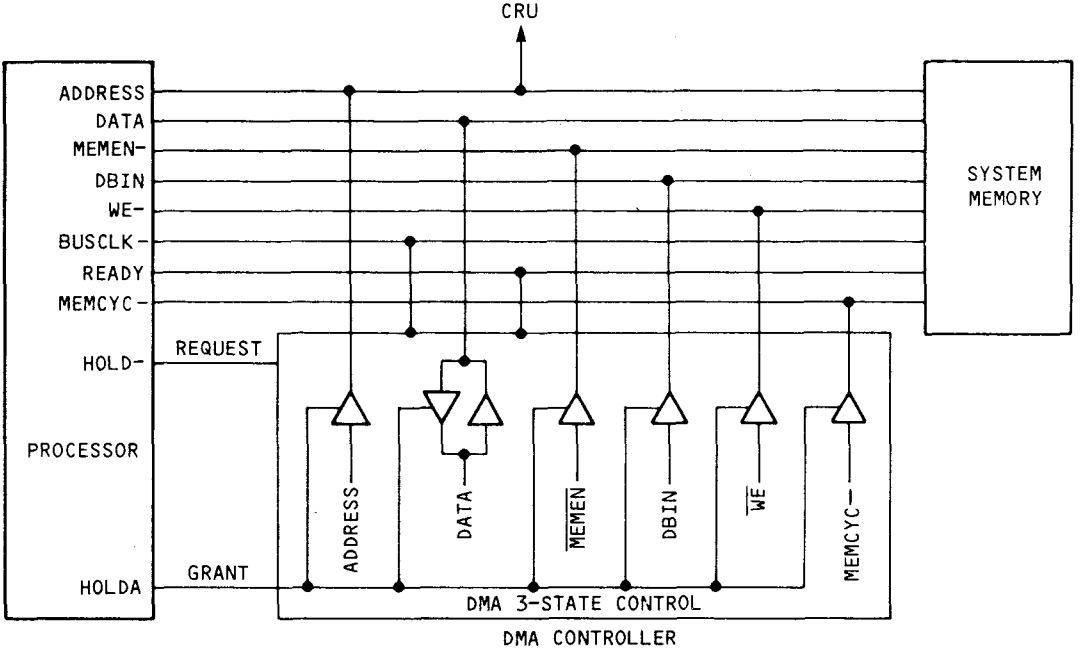


FIGURE 8-9. DMA BUS CONTROL

8.4.3.2 Multiple DMA Devices

The TM 990 system bus supports configurations in which multiple DMA devices may be employed. In this case, any DMA module requiring control of the bus must compete on a priority basis with any other DMA modules requiring control at the same time. Only one DMA module may control the bus at one time. All lower priority modules must wait for the higher priority devices to complete their tasks. The priority of a DMA module is established by that module's physical position in a serial priority chain. That is, the priority of a DMA module in a TM 990 system is determined by the slot in the chassis in which it is installed, slot 1 having the highest priority.

8.4.3.3 Bus Arbitration

Before initiating any data transfers with memory, a DMA module first must become bus master as a result of being the highest priority requesting device as described above. Three signals on the TM 990 system bus are dedicated to resolving simultaneous bus requests from multiple DMA modules. These signalsare BUSY-, GRANTIN- and GRANTOUT-. Each of these signals is synchronized to the low-to-high transition of BUSCLK-. The BUSY- signal is activated (low) by a DMA module when it has acquired control of the bus and is an indication to all other DMA modules that the bus is currently in use. The DMA module in control of the bus must not activate any memory control signals prior to activating BUSY- and, upon completion of the data transfer, must deactivate all memory control signals no later than the deactivation of BUSY-. GRANTIN- and GRANTOUT- form the serial priority network which is distributed among the DMA modules on the system backplane. All DMA modules monitor the condition of the GRANTIN- signal before acquiring bus control. If the GRANTIN- signal is active (low), this indicates to the DMA module that no higher priority DMA module requires the bus and bus control may be established as soon as the bus becomes not busy. A DMA module requiring control of of the bus will deactivate its GRANTOUT- signal (high) as soon as the requirement occurs. Even if the bus is presently busy from some other device, deactivating the GRANTOUT- signal will will lock out all lower priority DMA modules until the module completes its required data transfer and reactivates GRANTOUT-. GRANTOUT- of one DMA module becomes the GRANTIN- of the next lower priority DMA module.

8.5 INTERRUPTS

The TM 990 system bus accommodates two fixed and 15 general purpose interrupts. The two fixed interrupts are PRES- and RESTART-; these cannot be masked by the primary processor.

PRES- is the highest priority interrupt in the TM 990 system and is the system reset. When activated, PRES- causes the processor to terminate the instruction in progress and enter the RESET condition. The processor issues an IORST- to the rest of the system, masks all general purpose interrupts and, when PRES- is released, traps to and executes the "reset" subroutine. The PRES- interrupt is normally generated by the system power supply when all voltages are stable following power up, or by actuation of a switch by the system operator when return to the system initial conditions is required.

The RESTART- interrupt is also initiated by the actuation of a switch by the system operator. This interrupt, when activated, causes the primary processor to perform a load function following completion of the instruction in progress. Performing the load function causes the processor to trap to and execute the "load" subroutine. This feature may be used to implement bootstrap ROM loaders, front panel functions and so forth. If a RESTART- interrupt is activated while the PRES- interrupt line is still active, the processor will be reset, IORST- generated and all general purpose interrupts masked, but the processor will trap to the load subroutine. No resets occur with activation of the RESTART- interrupt.

The 15 general purpose interrupts are maskable by the primary processor under software control, and are prioritized with INT1- having the highest priority and INT15- the lowest. Use of these interrupts is unrestricted and the system designer may assign them in any way required with one exception. If the system is to have a power-fail feature INT1- should be reserved for the power-fail

interrupt. The power-fail indication from the power supply should activate this interrupt which, in turn, causes the primary processor to trap to the power-fail subroutine. Software for systems using the power-fail interrupt should not mask Interrupt 1. System modules generating general purpose interrupts must hold their respective interrupt line active until the processor acknowledges receipt of the interrupt by addressing the initiating system module.

8.6 MULTIPLE PROCESSING SYSTEMS

A multiple processing system may be defined as a system in which more than one program counter is running. This very broad definition permits many types of multiple processing systems to be defined.

8.6.1 Loosely Coupled Systems

This type of multiple processor system is characterized by physical separation of the processors and by relatively low data transfer rates. Many structures for this type of multiple processor system can be developed; Figure 8.10, illustrates a classical hierarchical structure using multichannal communications from a host system to subhost systems, and multidrop communications from the subhosts to individual control systems.

Multichannel communications utilize separate data lines for each communications path (to maximize data throughput). Multidrop communications utilize a shared communications line to minimize line costs (line access is controlled by the host or subhost on a polled basis); communication links may be either asynchronous or synchronous protocols).

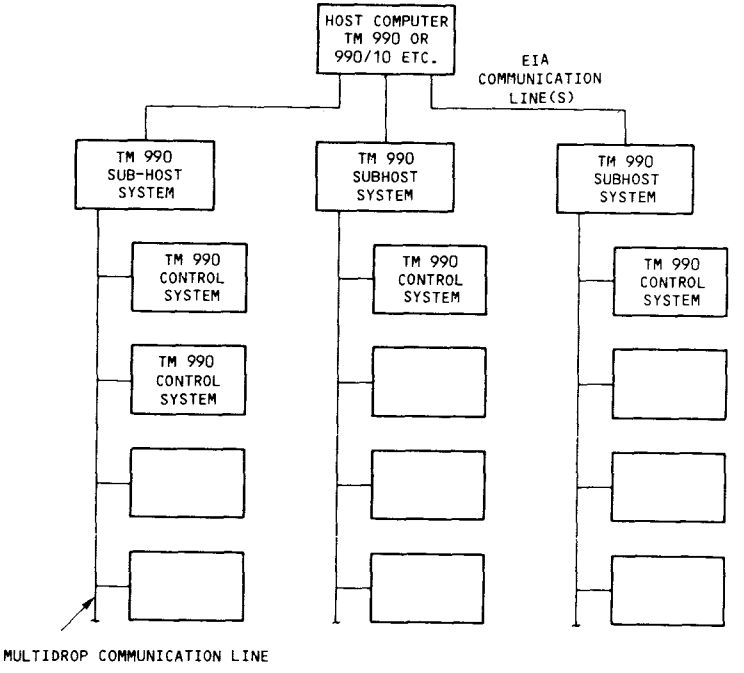


FIGURE 8-10. LOOSELY COUPLED SYSTEM.

Each processor in the system will be an individual TM 990 system consisting of a chassis with TM 990 System Bus, a processor module and some conbination of memory and I/O modules. Each processor may also have its own unique set of peripheral equipment. In other words, each processor is essentially a separate TM 990 system performing a specific function or functions. Communication between these processors will be commands and/or processed data rather than raw data.

8.6.2 Tightly Coupled Systems

For the purposes of this discussion, tightly coupled systems are those multiple processing systems in which each processor shares a common bus with the other processors.

8.6.2.1 Multiprocessing Architecture

In TM 990 systems all processors utilize subsets of a three bus architecture, illustrated in Figure 8-11.

In a multi-master system one or more processors has the capability to become the bus master; bus contention is arbitrated via the GRANTIN-, GRANTOUT- and BUSY- signals (previously defined). In addition to accessing system memory or I/O via the system bus, processors may contain local memory and or I/O which may be utilized without accessing the system bus. The three bus architecture also allows implementation of a communication memory which may be accessed by both on-board and off-board processors.

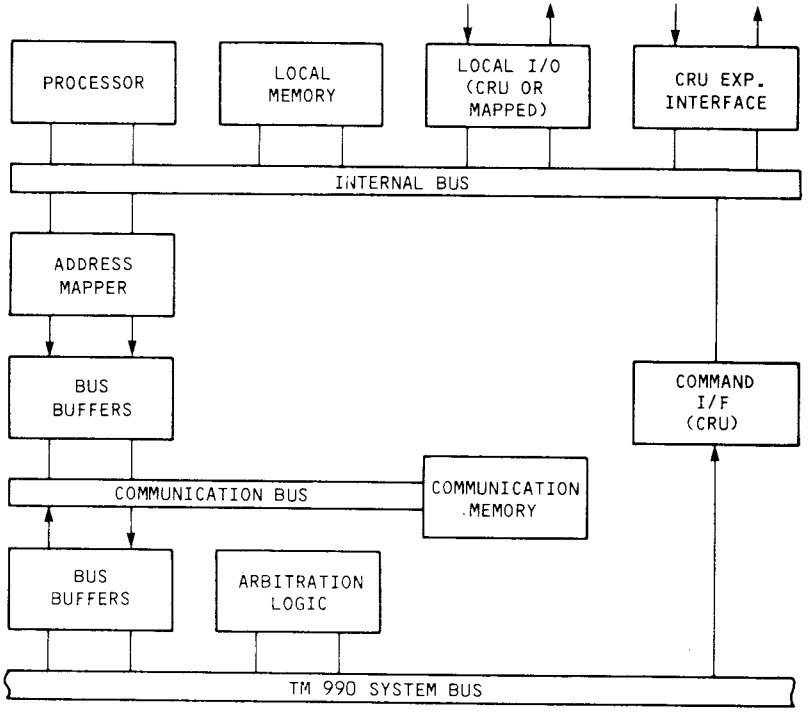


FIGURE 8-11. TM 990 MULTIPROCESSING ARCHITECTURE

In TM 990 systems, one processor may be designated as the master processor and all other processors designated as secondary (attached) processors. Each of the processors are individually programmed, but process execution in secondary processors is initiated and altered by commands from the primary processor. Attached processors may be programmed as required to perform any designated specific functions. Processors interface to the TM 990 system bus via either memory mapped of DMA interfaces. In this type of system the primary processor does not require arbitration logic, as it is always the primary processor; in addition, system software may be written as though it were a single processor system with all attached processors appearing as "intelligent" I/O devices to the primary processor. The following sections describe these subsets in more detail.

8.6.2.2 Single Processor Systems

The basic type of TM 990 system is one with a single CPU resident in a single 4 or 8 slot chassis. Most applications fall into this category. If a particular application has four boards identified, consideration should be given to using an 8 slot chassis to readily permit system expansion (the TM 990 bus is designed to support up to 12 boards on one bus).

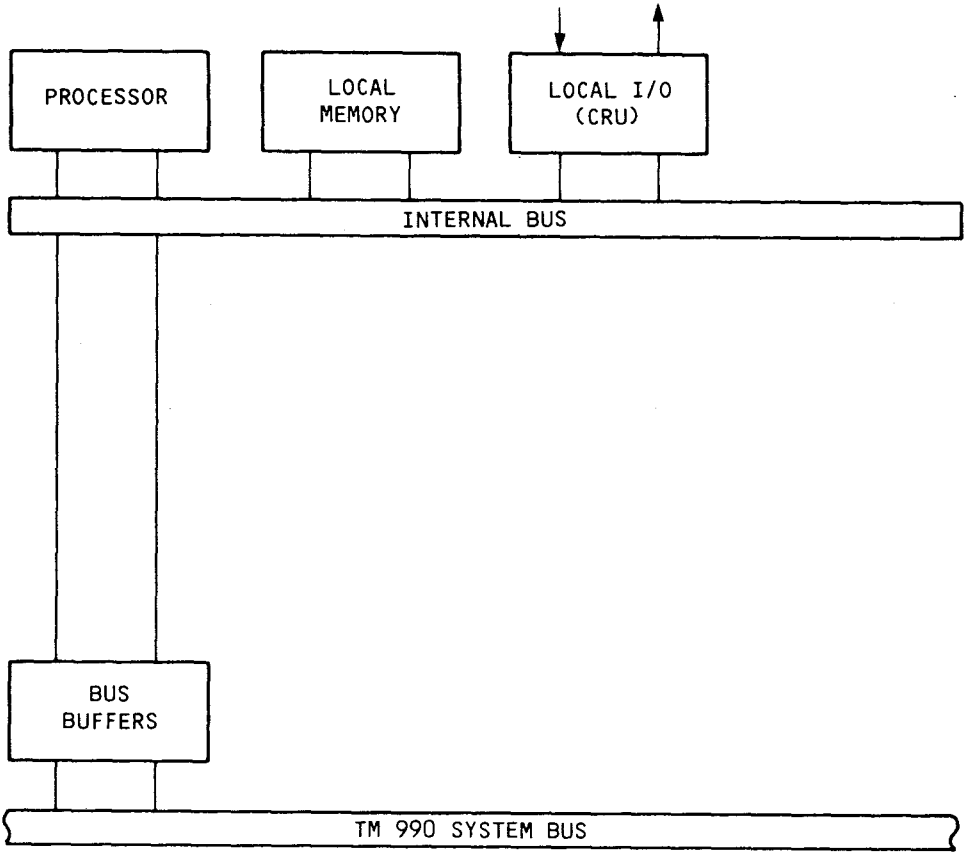


FIGURE 8-12. TM 990/100M MICROCOMPUTER

Figure 8-12 illustrates the TM 990/100M as a subset of the multiprocessing architecture. Note that on-board memory and I/O are accessible only to the on-board processor and cannot be accessed from the system bus. Figure 8-13 illustrates the TM 990/101M architecture. Note that the memory on the TM 990/101M is accessible both from the on-board processor and from the system bus; however, since the TM 990/101M does not have bus arbitration logic it cannot be used in multi-master system configurations. Both the TM 990/100M and TM 990/101M can be used with attached processors described below.

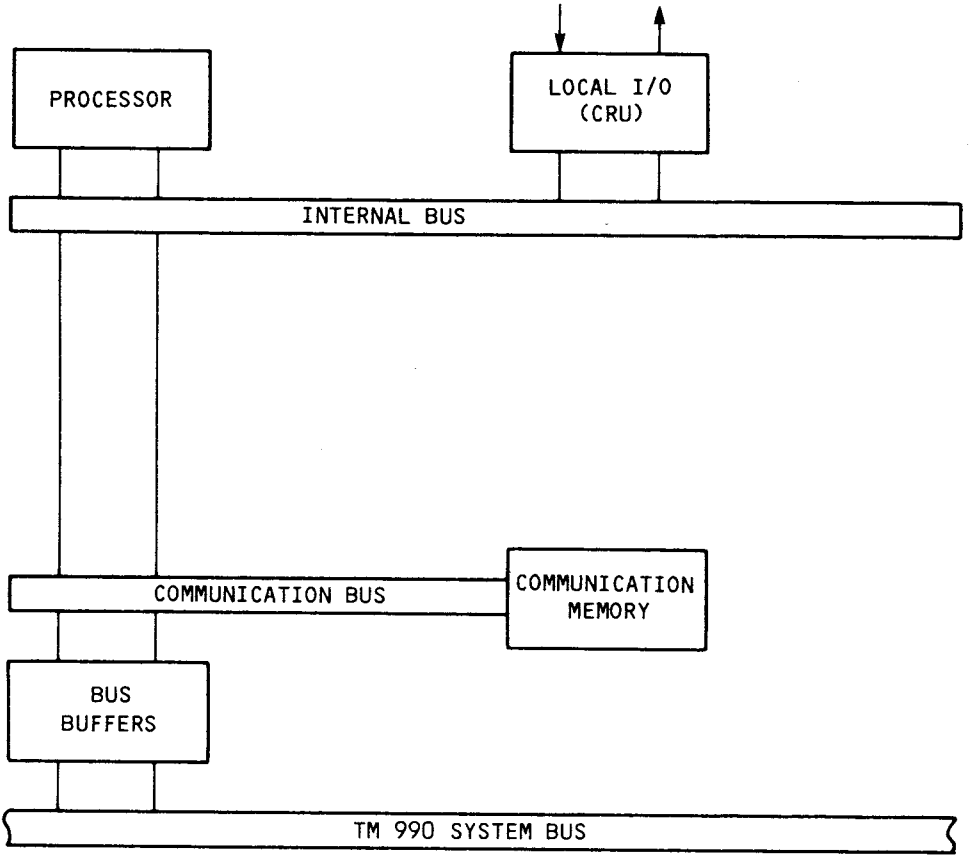


FIGURE 8-13. TM 990/101M MICROCOMPUTER

8.6.2.3 Expansion Chassis Configurations

If the total number of boards determined to be required for a system application exceeds the capacity of a single chassis, an expansion chassis can be used as shown in Figure 8-14.

Only CRU I/O modules should be placed in the expansion chassis. All memory, DMA and memory mapped I/O modules should remain in the main chassis to avoid system performance degradation caused by additional propagation delays in time critical memory control signals. CRU I/O modules may be located in both chassis, with the highest priority modules being in the main chassis.

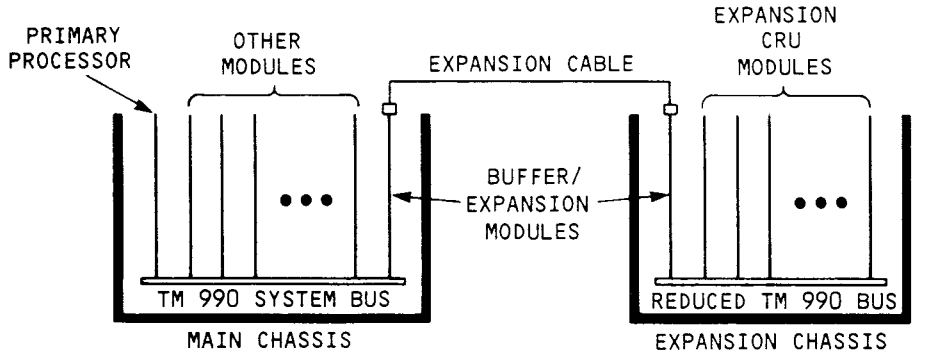


FIGURE 8-14. EXPANSION CHASSIS CONFIGURATIONS

8.6.2.4 Memory Mapped Attached Processors

This is a derivation of the classical "dual port memory" tightly coupled system and a processor of this type is illustrated in Figure 8-15 below.

The dual port memory can be implemented with either storage registers or with RAM depending on the capacity required. Although the memory is common to both the on-board processor and the primary processor, any one memory location may

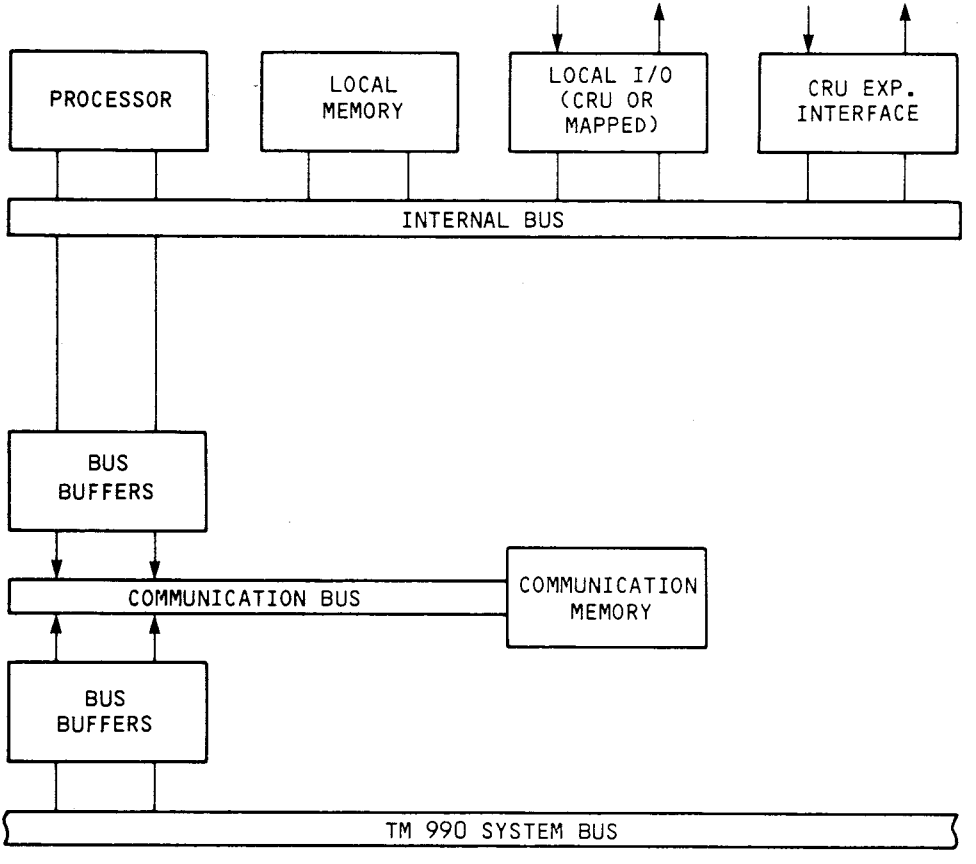


FIGURE 8-15. MEMORY MAPPED ATTACHED PROCESSOR

appear to have a different address to both processors. As far as the primary processor is concerned, the dual port memory is part of the overall system memory and local processor access to this memory is invisible to the system bus; the memory is used for command and data storage as required by the application. This type of secondary processor is very flexible and suited to a wide range of applications.

It should be noted that since mapped attached processors appear as system memory to the TM 990 Bus, bus arbitration logic is not required; furthermore, it is possible to implement communication memories such that system bus timing is not affected by local processor accesses to that memory.

8.6.2.5 Direct Memory Access Attached Processors

Direct memory access is utilized on secondary processors in conjunction with CRU I/O. A generalized processor of this type is illustrated in Figure 8-14 below.

In this type of secondary processor the CRU I/O is used to pass commands from the primary processor to the on-board processor. The DMA is used to transfer data to or from system memory. This type of secondary processor is particularly suited to applications such as magnetic tape transport controllers, floppy disc controllers and so forth where there is a requirement for large data throughput between system memory and the external storage device.

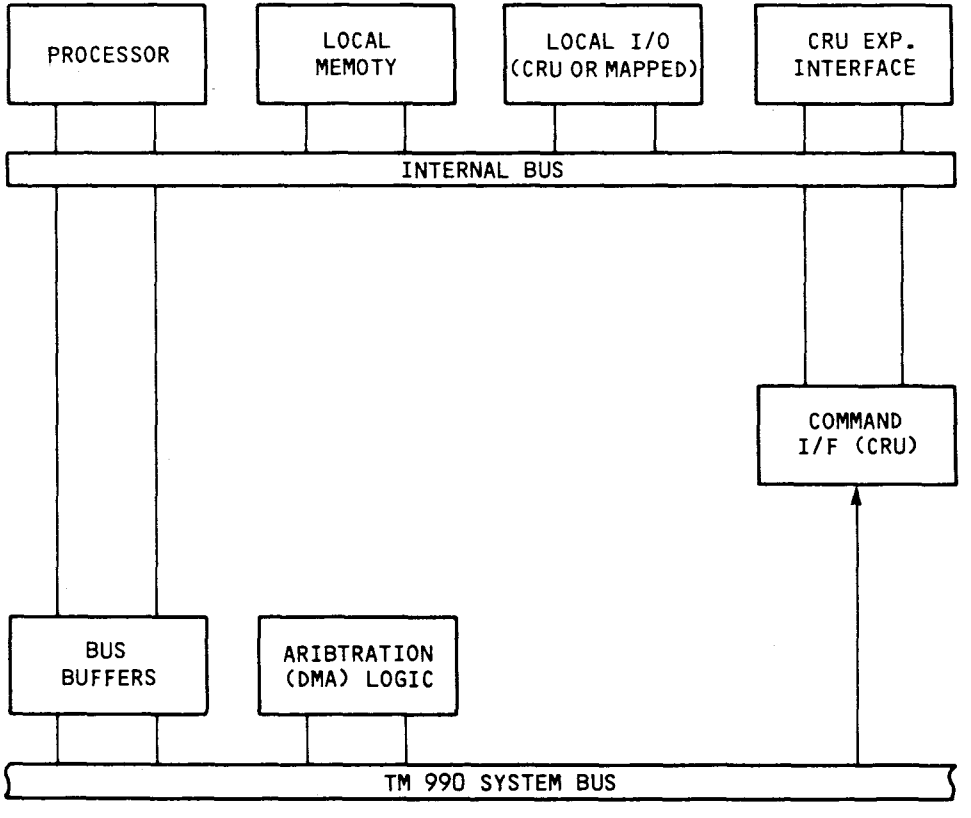


FIGURE 8-16. DMA ATTACHED PROCESSOR

SECTION 9

QUALITY ASSURANCE AND RELIABILITY

9.1 INTRODUCTION

All TM 990 products are thoroughly tested and inspected to rigorous manufacturing and quality control standards.

Quality Assurance participation throughout the product development, manufacturing and product test planning phases ensures the establishment and implementation of exacting controls and standards.

Inspection and testing begins at the component level, with exhaustive testing at incoming inspection and continues through subassembly and final assembly levels, concluding with a comprehensive final system test and inspection. Figure 9-1 illustrates the test and inspection sequences.

9.2 INCOMING INSPECTION AND TEST

Table 9-1 shows the degree and methods of incoming testing, employed by Quality Assurance, by which all components used in TM 990 products are subjected to TI's strict quality assurance criteria.

9.3 SUBASSEMBLY TEST

All subassembly modules (essentially finished product minus LSI MOS parts) are subjected to a pre-system test check out on the Spring Pin Integrated Test System (SPITS) which tests the modules for trace continuity, shorts, proper TTL logic response (static logic check), and missing or wrong parts.

This computer controlled test station permits rapid fault isolation to a high degree of accuracy while providing a level of testing that covers certain classes of faults that do not always cause a failure indication during the more sophisticated function, system level tests.

9.4 PRE BURN-IN SYSTEM TEST

Upon completion of the "SPITS" testing, the subassembly is populated with the LSI MOS memory and microprocessor devices, yielding a fully configured "deliverable end item." This ensures that the product to be shipped enters the system test and burn-in cycle early enough so that the fully populated "as shipped" configuration passes through the entire, critical system test and burn-in process.

The pre burn-in system test is a functiional test of the TM 990 board assembly at 25 degrees Celsius (the same thorouth system test used at the final test state) and is executed primarily to avoid loading burn-in with room temperature functional failures.

9.5 BURN-IN TESTING

All TM 990 board modules are dynamically exercised in burn-in chambers across a temperautre range of 25 degrees Celsius to 70 degrees Celsius with a cycle time of one hour. Typical Burn-in time varies from 8 hours minimum to 4 days. Automatic error monitoring, employing special burn-in test software is

exercised throughout the burn-in testing cycle, detecting failures as soon as they occur. Repaired modules are re=started at time zero, thus maintaining the requirement that modules complete the full burn-in cycle, error free.

9.6 FINAL SYSTEM TESTING

Upon completion of specified burn-in testing, the TM 990 board modules receive a comprehensive functional test at 25 degrees Celsius. Failures occurring at this "final system test" resulting in a part replacement, cause the module to be rerouted through burn-in. In addition to system testing for strict compliance to system specifications, all TM 990 outgoing product receives a final quality control inspection to ensure total compliance to rigorous workmanship standards and other applicable quality assurance criteria, prior to shipping.

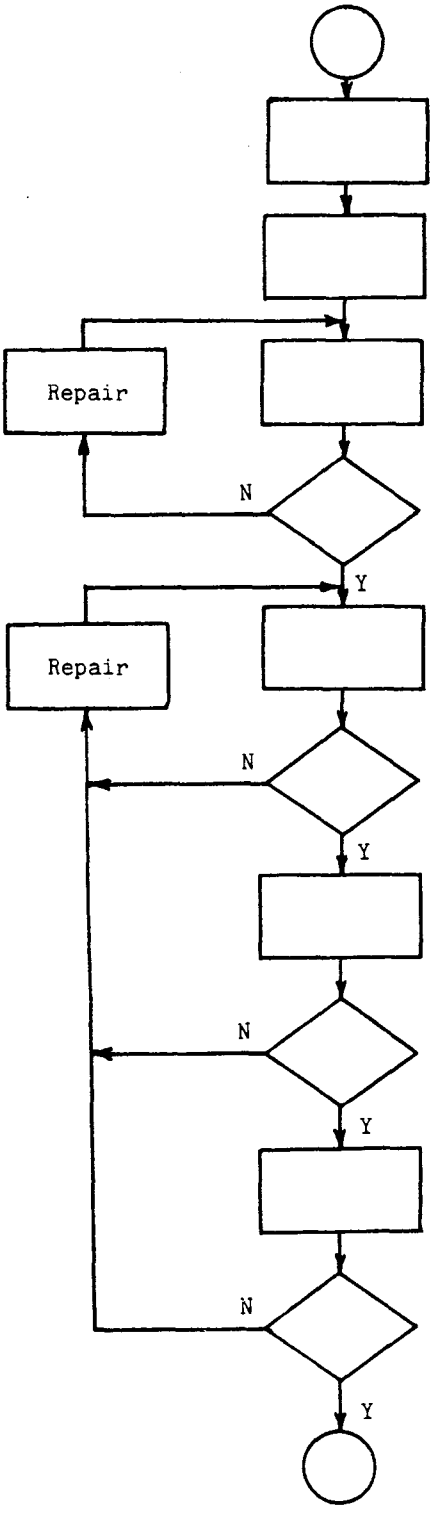
9.7 TM 990 MODULE RELIABILITY

On going reliability testing of major board modules, providing early identification and resolution of time related failures, ensures the TM 990 user/customer of lengthy, error free operation in a "commercial grade environment."

While exact "field operating conditions" can never be fully duplicated, the large samples of product subjected to the 70 degrees Celsius, 1000 hour minimum, continously monitored, dynamically exercised testing routines (identical to production burn-in test) provide a very good approximation to the "nominal commercial environment, and generates statistically accurate performance/test data, regarding long term operation.

Periodic room temperature testing (the same comprehensive testing, done in production system test) maintains direct coorelation with production test and provides a means of detecting "parameter" shifts due to time and temperature.

Major module functions, exercised during long term reliability testing include: RAM pattern testing; TMS 9901 I/O line exercise/register compare using various data patterns, rigorous timer tolerance testing of interrupt count in timing loop; TMS 9902 I/O testing at 110, 600, 1200, and 19,200 baud and timer test; and CPU arithmetic function and shift instructions testing.



Incoming QA and Test of Components

Subassembly Build Up

Subassembly QA

Run Subassembly without MOS Parts on Spring Pin Integrated Test System

Pass SPITS?

Populate Subassembly With MOS Parts. Run System Test

Pass System Test?

Burn-In For Specified Interval

Pass Burn-In?

Run System Test

Pass System Test?

QA, Pack, Ship

FIGURE 9-1. TEST AND INSPECTION SEQUENCE

TABLE 9-1. RECEIVING INSPECTION AND INCOMING TEST

Comodity Type	Inspection Level	Test Method
TTL Integrated Circuits	100% @ 70°C	Parametrics, dc and Dynamic
Linear Integrated Circuits	100% @ 25°C	Parametrics, dc and Dynamic
Diodes	Reel - 100% 25°C Loose - Sample	Parametrics
Transistors	Sample @ 25°C	Parametrics
Discrete Passive Devices	Sample @ 25°C	Auto Bridge, Parametrics
Crystals	Sample @ 25°C	Dedicated Test System, Frequency Only
Printed Circuit Boards	Sample	Microsection, Plated Holes Dimensions Betascope, Plating Thickness
MOS Memories	Sample	Parametrics, Functionality
MOS Microprocessors	Sample	Parametrics, Functionality
5MT Modules & Base	100%	Dedicated Test System, Functionality
Power Supplies	100%	Dedicated Test System, Functionality
Analog Boards	100%	Dedicated Test System, Functionality
Cables	100%	Dedicated Test System, Functionality
Bipolar PROMS/EPROMS	100% Sample	Programmability & Verification Parametrics

SECTION 10

CUSTOMER SERVICE AND SUPPORT

10.1 INTRODUCTION

Texas Instruments provides customer support for the TM 990 series of modules in the form of a customer support line, field specialists, field system centers, module repair, and publications. This support can be quite helpful in the planning and developmental stages of a project in addition to providing service support should the need arise.

10.2 CUSTOMER SERVICE

10.2.1 Customer Support Line (713-776-6632)

Texas Instruments provides a customer support line (713-776-6632) that is manned by experienced engineers who supply answers to technical questions from the field. These engineers can be consulted regarding maintenance or applications problems that may occur. The customer support line is manned during normal working hours, five days a week.

10.2.2 Systems Engineers

The systems engineers work with customers to partition systems to meet customer cost performance requirements. They provide applications assistance on TI products. This assures that state of the art semiconductor products are properly supported through the use of the engineer's skills in system design, circuit design and use of TI resources such as microprocessor development systems. They work with sales engineers to provide customer insight into TI product plans and to assure that TI product plans properly address needs of the market.

10.2.3 Field System Centers

There are approximately fifty field systems centers where the TM 990 Series Microcomputer Family can be found on display. These centers have a factory trained field application engineer to assist in system development and provide training on the use of the TM 990 Series Microcomputer Modules product line.

The AMPL Microprocessor Protyping Lab is also on display. The AMPL lab provides in-circuit emulation support, logic-state trace and analysis, read-only memory implementation aids, and TMS 9900 software development support. This lab provides the user with a dedicated design center where 9900-based systems can be developed in an integrated software-hardware design and debug sequence.

10.2.4 Module Repair

A module repair service is also available. To have an out of warranty module repaired by Texas Instruments, submit the module and a purchare order (current repair price is $100) to the seller. At its option, Texas Instruments will repair the returned module, replace the module with a reconditioned one, or return the original module as unrepairable.

10.2.5 Publications

Each TM 990 Series Microcomputer Module is supplied with the appropriate documentation. User's manuals cover specifications, operation, theory of operation, schematics and other pertinent data. These manuals provide complete and verified information in a consise format that guides the reader in the use and maintenance of his equipment. Table 10-1 provides a listing of the TM 990 Series Microcomputer Module Manuals that are available.

TABLE 10-1. TM 990 SERIES MICROCOMPUTER MODULE MANUALS

MANUAL TITLE	MANUAL NUMBER
CPU MODULES (100 Series)	
TM 990/100M Microcomputer User's Guide	MP321
TM 990/101M Microcomputer User's Guide	MP337
TM 990/180M Microcomputer User's Guide	MP322
TM 990/189 Microcomputer User's Guide	MPB06
Introduction to Microprocessors (TM 990/189 tutorial)	MPB30
MEMORY EXPANSION (200 Series)	
TM 990/201 and TM 990/206 Expansion Memory Boards	MP334
PERIPHERALS AND I/O INTERFACES (300 Series)	
TM 990/301 Microterminal	MP323
TM 990/310 48 Bit I/O Module User's Guide	MP336
SOFTWARE DEVELOPMENT (300 Series)	
TM 990/302 Software Development Board User's Guide	MP343
TM 990/302 Hardware User's Guide	MP344
SOFTWARE (400 Series)	
TM 990/401-1 TIBUG Monitor	MP324
TM 990/401-2 TIBUG Monitor	MP331
TM 990/401-3 TIBUG Monitor	MPB01
TM 990/402 Line-By-Line Assembler User's Guide and Listing	MPB07
TM 990/430 TI Modular-Based Executive in ROM (TIMBER)	MPB23
TM 990 POWER BASIC Reference Manual	MP308
PROGRAMMING	
Model 990 Computer Assembly Language Programmer's Guide (DSG)	943441-9701
ACCESSORIES AND CARD CAGES (500)	
TM 990/510 and TM 990/520 Card Cages	MP341
TM 990/511 Extender Board	MP333
TM 990/512 and TM 990/513 Universal Prototyping Boards	MP335

TABLE 10-1. MANUALS (cont.)

MANUAL TITLE	MANUAL NUMBER
TM 990/502 Cable Assembly	MP328
TM 990/503 Cable Assembly	MP329
TM 990/504 Cable Assembly	MP330
TM 990/505 Cable Assembly	MP338
TM 990/506 Cable Assembly	MP342
TM 990/407 Cable Assembly	MPB24
TM 990/508 Cable Assembly	MPB17
TM 990/514 and TM 990/515 EPROM Personality Cards	MPB12
TM 990/518 DC Power Supply	MPB08
TM 990/519 DC Power Supply	MPB11
TM 990 System Specification	MPB27

To obtain copies of the manuals in Table 10-1, mail your request to:

Literature Coordinator
TM990 Microcomputer Modules
P. O. Box 1443, MS 6404
Houston, Texas 77001

SECTION 11

ORDERING INFORMATION

11.1 GENERAL

This section presents a system configuration worksheet that will provide assistance in the planning of a system using TM 990 Modules. A listing of TI sales offices and distributors is also given.

11.2 SYSTEM CONFIGURATION

A system configuration worksheet is given in Table 11-1. The worksheet can be used for system development and cost projection. To use the system configuration worksheet:

A. Cut out both pages of Table 11-1 and place the pages so that the line numbers are aligned.

B. Determine system requirements and enter specifications on line 1.

C. Enter features of TI microcomputer board to be used on line 2.

D. Enter features of all expansion boards to be used on lines 3-10.

E. Combine the features on lines 2-10 and enter on line 11.

F. Compare line 11 to system requirements on line 1.

G. Select power supply to meet system requirements and enter on line 12.

H. Enter cost of any additional hardware (prototyping boards, cables, microterminal, etc.) on lines 13 and 14.

I. Enter total system cost on line 15.

Texas Instruments' TM 990/518A DC Power supply is capable of handling many applications. This supply provides the following dc outputs: +5 Vdc @ 6.0 A, +12 Vdc @ 0.9 A, -12 Vdc @ 0.9 A, and +48 Vdc (PROM Programming Voltage) @ 0.1 A.

11.3 TI SALES OFFICES AND DISTRIBUTORS

A listing of the TI sales offices is provided in Table 11-2 and a listing of TI distributors is given in Table 11-3.

Should there be any questions regarding the TM 990 Modules that cannot be answered in the field, direct your communication to:

Texas Instruments Incorporated
P. O. Box 1443
M/S 640
Houston, Texas 77001

TABLE 11-1. SYSTEM CONFIGURATION WORKSHEET

Instructions:

a) Determine system requirements and enter specifications on line 1.

b) Enter features of TI microcomputer board to be used on line 2.

c) Enter features of all expansion boards to be used on lines 3 – 10.

d) Combine the features on lines 2 – 10 and enter on line 11.

Equipment features:

Line Number	Description	Memory		Input/Output						No. of Interrupts	No. of Timers
		Bytes RAM	Bytes EPROM	Serial Ports TTY	Serial Ports RS232C	Parallel Lines In	Parallel Lines Out	Analog Channels In	Analog Channels Out		
1	SYSTEM REQUIREMENTS										
2	TM990/1 M–										
3											
4											
5											
6											
7											
8											
9											
10											
11 TOTAL											

*TI CONTACT:
Name _____
Phone _____

e) Compare line 11 to system requirements on line 1.

f) Select power supply to meet system requirements and enter on line 12.

g) Enter cost of any additional hardware (prototyping boards, cables, micro-terminal, etc.) on lines 13 and 14.

h) Enter total system cost on line 15.

Refer to Table 2-14 (CPU Compatibility).

	Peripheral Controller Type	Comments	Power Requirements				Price*			
			+5 V	-5 V	+12 V	-12 V	Unit Price	# Systems	# Systems	# Systems
POWER AVAILABLE										
12	POWER SUPPLY**									
13										
14										
15 TOTAL SYSTEM COST										

APPENDIX A

COMMUNICATIONS

A.1 TMS 9901 PROGRAMMABLE SYSTEMS INTERFACE (PSI)

The TMS 9901 Programmable Systems Interface is a multifunctional component designed to provide low cost interrupt and I/O ports and an interval timer for TMS 9900-family microprocessor systems. The TMS 9901 is fabricated using N-channel silicon-gate MOS technology and is TTL-compatible on all inputs and outputs, including the power supply (+5 V) and single-phase clock.

The architecture of the TMS 9901 PSI is designed to provide the user maximum flexibility when designating system I/O ports and interrupts. The TMS 9901 can be divided into four subsystems: CRU interface, interrupt interface, input/output interface, and interval timer. The CRU is addressed on a single-bit or 16-bit basis and can be thought of as occupying the first 4096 bits (in a 9900-based system) in an auxilliary memory space. RAM and EPROM memory is totally independant of the CRU. A very efficient method of addressing bits in an I/O port, for example, is provided by the CRU. This architecture can best be appreciated by considering a typical application.

Figure A-1 illustrates the use of a TMS 9901 PSI in a TMS 9900 system.. The CPU communicates with the TMS 9901 via the CRU. The CRU interface consists of five address select lines (S0-S4), chip enable (CE-), and the three CRU lines (CRUIN, CRUOUT,CRUCLK). The select lines (S0-S4) are connected to the five least significant bits of the address bus; for a TMS 9900 system S0-S4 are connected to A10-A14, respectively. Chip enable (CE-) is generated by decoding the most significant bits of the address bus on CPU cycles; for a 9900 based system address bits 0-9 would be decoded. In the case of a write operation, the TMS 9901 strobes data off the CRUOUT line with CRUCLK. For a read operation, the data is sent to the CPU on the CRUIN line.

A total of nine pins (INT7-/P15 to INT15-/P7) on the TMS 9901 are user programmable as either I/O ports or interrupts. Any pin which is not being used as an interrupt should have the appropriate interrupt mask disabled

(mask = 0) to avoid erronous interrupts to the CPU. To program one of the pins as an interrupt, its interrupt mask simply is enabled and the line may be used as if it were one of the dedicated interrupt lines. To program a pin as an I/O port, disable the interrupt mask and use that pin as if it were one of the dedicated I/O ports.

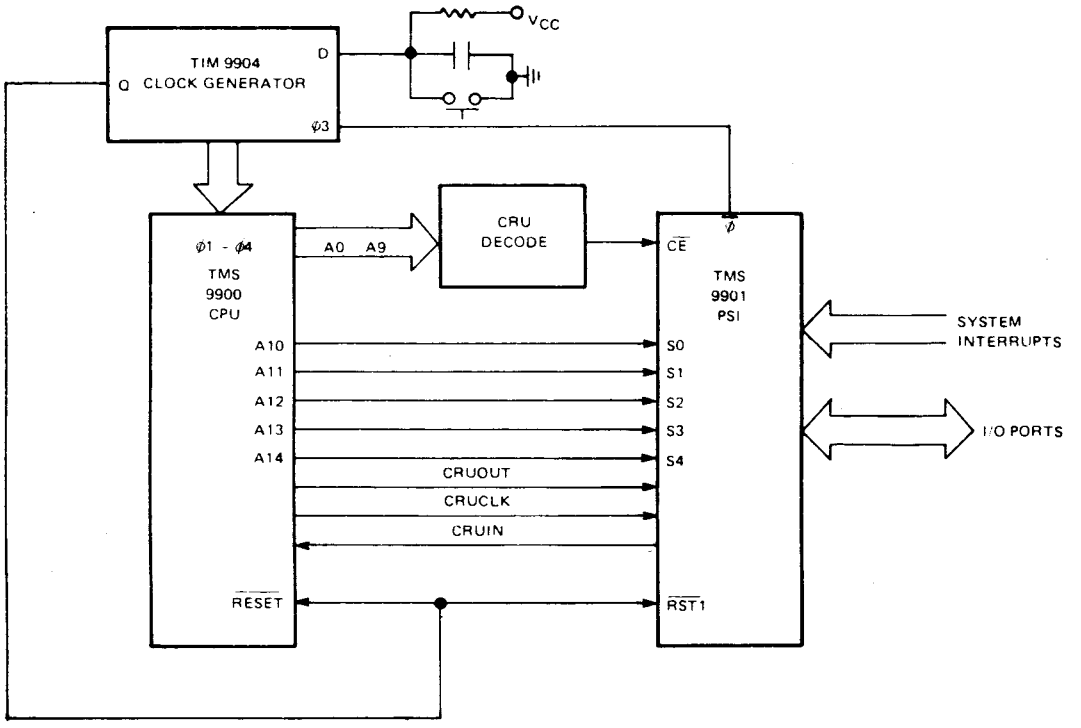


FIGURE A-1. TYPICAL TMS 9901 APPLICATION

Figure A-2 is a block diagram of the TMS 9901 interval timer section. The clock consists of a 14-bit counter that decrements at a rate of f(ø)/64 (at 3 MHz this results in a maximum interval of 349 milliseconds with a resolution of 21.3 microseconds). The clock can be used as either an interval timer or an event timer. To access the clock, select bit zero (control bit) must be set to a one. The clock is enabled to cause interrupts by writing a nonzero value to it and is then disabled from interrupting by writing zero to it or by a RST1-. The clock starts operating at no more than two ø times after it is loaded. When the clock decrementer is running, it will decrement down to zero and issue a level-3 interrupt. The decrementer, when it becomes zero, will also be reloaded from the clock register and decrementing will start again. (The zero state is counted as any other decrementer state.) The decrementer always runs, but it will not issue interrupts unless enabled; of course, the contents of the unenabled clock read register are meaningless.

The clock is accessed by writing a one into the control bit (TMS 9901 CRU bit zero) to force CRU bits 1-15 to clock mode. Writing a nonzero value into the clock register then enables the clock and sets its time period. When the clock is enabled, it interrupts on level 3 and external level-3 interrupts are disabled. The mask for level 3 in the PSI must be set to a one so that the processor will see the clock interrupt. When the clock interrupt is active, the clock mask (mask bit 3) must be written into with either a one or zero to clear the interrupt; writing a zero also disables further interrupts.
If a new clock value is required, a new 14-bit clock start value can be programmed by executing a CRU write operation to the clock register. During programming, the decrementer is restarted with the current start value after each start value bit is written. A timer restart is easily implemented by writing a single bit to any of the clock bits. The clock is disabled by RST1-

(power up reset) or by writing a zero value into the clock register; RST2- does not affect the clock.

The clock read register is updated every time the decrementer decrements when the TMS 9901 is not in clock mode. There are two methods to leave the clock mode: first, a zero is written to the control bit; or second, a TMS 9901 select bit greater than 15 is accessed. Note that when CE- is inactive (high), the PSI is not disabled from seeing the select lines. As the CPU is addressing memory, A10-A14 could very easily have a value of 15 or greater--A10-A14 are connected to the select lines; therefore, the TMS 9901 interval timer section can "think" it is out of clock mode and update the clock read register. Very simply, this means that a value cannot be locked into the clock read register by writing a one to CRU select bit zero (the control bit). The 9901 must be out of clock mode for at least one timer period to ensure that the contents of the clock read register has been updated. This means that to read the most recent contents of the decrementer, just before reading, the TMS 9901 must not be in the clock mode. The only sure way to manipulate clock mode is to use the control bit (select bit zero). When clock mode is reentered to access the clock read register, updating of the read register will cease. This is done so that the contents of the clock read register will not change while it is being accessed.

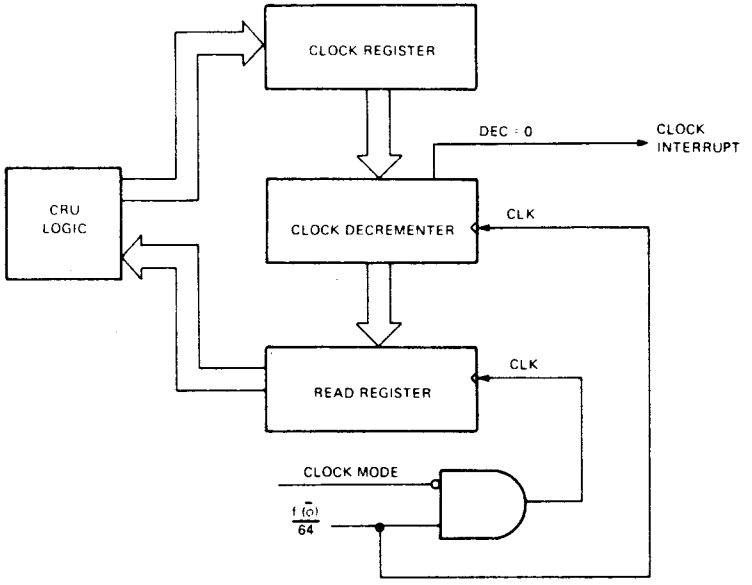


FIGURE A-2. TMS 9901 INTERVAL TIMER SECTION

A.2 TMS 9902 ASYNCHRONOUS COMMUNICATIONS CONTROLLER (ACC)

The TMS 9902 Asynchronous Communications Controller (ACC) is a peripheral device designed for use with the Texas Instruments 9900 family of microprocessors. The TMS 9902 is fabricated using N-channel, silicon gate, MOS technology. The TMS 9902 is TTL-compatible on all inputs and outputs, including the power supply (+5V) and single-phase clock. The TMS 9902 ACC provides an interface between a microprocessor and a serial, asynchronous,

communications channel. The ACC performs the timing and data serialization and deserialization functions, facilitating microprocessor control of the asynchronous channel. The TMS 9902 ACC accepts EIA Standard RS-232-C protocol.

The TMS 9902 is designed to provide a low cost, serial, asnychronous interface to the 9900 family of microprocessors. The ACC has five main subsections: CRU interface, transmitter section, receiver section, interval timer, and interrupt section.

Figure A-3 illustrates the use of a TMS 9902 ACC in a TMS 9900 system. The CPU communicates with the TMS 9902 via the CRU. The least significant bits of the address bus are connected to the select lines. In a TMS 9900 system, the five least significant bits (A10-A14) are connected to the select lines (S0-S4) respectively. CRU instructions can be used to set:

- Control criteria such as parity and character length
- Interval timer rate
- Receive data rate
- Transmit data rate.

Data is transmitted and received through the CRUOUT and CRUIN lines. The TMS 9902 can be used with an EIA or TTY terminal.

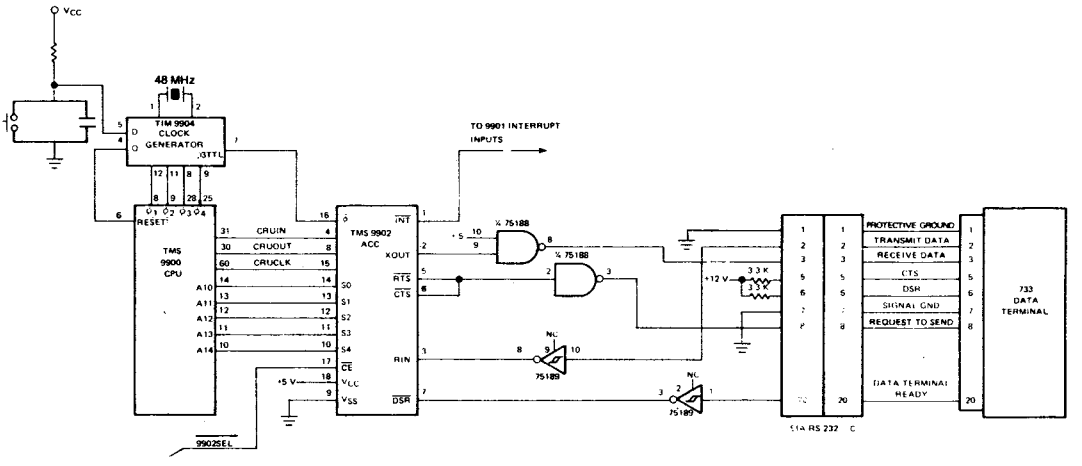


FIGURE A-3. TYPICAL TMS 9902 APPLICATION

Texas Instruments Northern European Semiconductor Division

UNITED KINGDOM PLANTS AND SALES OFFICES

HEAD OFFICE

Texas Instruments Limited
Northern European
Semiconductor Division,
Manton Lane,
Bedford MK41 7PA.
Telephone (0234) 67466
Telex 82178

TI SUPPLY REGIONAL SALES OFFICES

Bedford

Texas Instruments Limited
Manton Lane,
Bedford MK41 7PA.
Telephone (0234) 67466
Telex 82178

Slough

Texas Instruments Limited,
186 High Street,
Slough, Berks. SL1 1LD.
Telephone (0753) 33411
Telex 848363

Manchester

Texas Instruments Limited,
St. James House,
Wellington Road North,
Stockport SK4 3EL.
Telephone (061) 442 0645
Telex 667478

Edinburgh

Texas Instruments Limited,
24 Rutland Street,
Edinburgh EH1 2AN.
Telephone (031) 229-5573/1481
Telex 72637

INDEPENDENT DISTRIBUTORS

ENGLAND

Bristol

ITT Electronic Services,
30 Denmark Street,
Bristol.
Telephone (0272) 290125
Telex 449260

Derby

Quarndon Electronics (Semiconductors) Limited,
Slack Lane,
Derby DE3 3ED.
Telephone (0332) 32651
Telex 37163

Harlow

ITT Electronic Services,
Edinburgh Way,
Harlow,
Essex.
Telephone (0279) 26777
Telex 817379

Leicester

ITT Electronic Services,
56 Welford Road,
Leicester.
Telephone (0533) 548292
Telex 341237

Manchester

ITT Electronic Services,
110 Corn Exchange,
Manchester M4 3BN.
Telephone (061) 832-2681 and
(061) 834-7827/8
Telex 669177

Portsmouth

Celdis-SDS,
57 Kingston Road,
Portsmouth PO2 7DP.
Telephone (0705) 65311
Telex 86114

Reading

Celdis-SDS,
Loverock Road,
Reading RG3 1ED
Telephone (0734) 585171
Telex 848370

Sevenoaks

Jermyn-Mogul Electronics Limited,
Vestry Industrial Estate,
Sevenoaks, Kent.
Telephone (0732) 50144
Telex 95142

Slough

Macro-Marketing Limited,
396 Bath Road,
Slough, Berks SL1 6JA.
Telephone (06286) 4422
Telex 847945

Sunbury-on-Thames

Cramer Components Limited,
Hawke House,
Green Street,
Sunbury-on-Thames,
Middlesex.
Telephone (01) 979-7799
Telex 923592

Thame

Memec Component Systems Limited,
Thame Park Industrial Estate,
Thame,
Oxfordshire.
Telephone (084421) 3146
Telex 837508

SCOTLAND

East Kilbride

Celdis-SDS,
111 Alexandra House,
East Kilbride G74 1LX.
Telephone (03552) 35888/9
Telex 779044

Johnstone

ITT Electronic Services,
62 High Street,
Johnstone,
Renfrewshire.
Telephone (0505) 24357
Telex 778622

IRELAND

Dublin

Hawthorne Electronics Limited,
7 Ontario Terrace,
Dublin.
Telephone (0001) 962022/962308

ITT Electronic Services,
142 Phibsborough Road,
Phibsborough, Dublin.
Telephone (0001) 307522
Telex 8288

Larne

Hawthorne Electronics Limited,
18 Cross Street,
Larne,
County Antrim.
Telephone (0574) 5321
Telex 747286

BELGIAN T.I. SALES OFFICE

Belgium

S.A. Texas Instruments Belgium N.V.,
Raketstraat, 100, Rue De La Fusee,
1130 Brussels.
Telephone (02) 720 80 00
Telex 61 161

BELGIAN T.I. DISTRIBUTOR

Inelco S.A.
Avenue Val Duchesse 3,
1160 Brussels.
Telephone (02) 660 00 12
Telex 25 441

SCANDINAVIAN T.I. PLANTS AND SALES OFFICES

Sweden

Texas Instruments International Trade Corpn.,
(Sverige Filialen),
Fack S100-54,
Stockholm.
Telephone 08-23 54 80
Telex 10377

Norway

Texas Insruments Norway AS,
KR August GT.13,
Oslo 1.
Telephone (02) 689485
Telex 19628

Denmark

Texas Instruments A/S,
Marielundvej 46E,
2730 Herlev.
Telephone (02) 91 74 00
Telex 35123

Finland

Texas Instruments Finland OY,
Elimaenkatu 14-16
PL53 00511
Helsinki 51
Telephone 40 83 00
Telex 12 1457

SCANDINAVIAN T.I. DISTRIBUTORS

Sweden

AB Gosta Backstrom,
Box 12009,
Alstromergatan 22,
S-102 21 Stockholm 12.
Telephone (08) 541080
Telex 10135

Sweden

Multikomponent,
Fack,
Ankdammsgatan 32,
171 20 Solna.
Telephone (08) 835150
Telex 10516

Multikomponent,
Box 29047
Lundgatan 12,
400 62 Goteborg.
Telephone (031) 801980

Multikomponent,
Hålsjögatan 4,
217 66 Malmö.
Telephone (040) 130020

Interelko AB,
Sandborgsvägen 55,
S-122-33 Enskede,
Sweden.
08/49 26 60
Telex 10689

Norway

Ingeniorfirma Morgenstierne & Co. AS,
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