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TEXAS INSTRUMENTS

TM 990

TM 990/204 Memory Module With Battery Backup

MICROPROCESSOR SERIES™

User's Guide

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SECTION 1

INTRODUCTION

1.1 GENERAL

The TM 990/204 is a RAM memory expansion board compatible with the TM 990 bus and CPU modules such as the TM 990/100MA, TM 990/101MA, and the TM 990/1481. Figure 1-1 is a block diagram of the board. Its features include:

- Shipped with CMOS RAM. Memory is expandable in 4-K byte blocks to a maximum of 16 K bytes in four blocks. Dash-number configurations are shown in Table 1-1.

- CMOS or NMOS RAM compatible; can be mixed in individual 4 K by 8-bit blocks (blocks are shown in Figure 1-2).

- Memory organized into four 4-K-byte blocks; some features organized by blocks, a maximum of four blocks per board

- Built-in battery backup feature prevents loss of CMOS memory data in case of a power loss, as shown below for a new battery:

Model	Room Temperature, Typ	Worst Case, 0-70°C
TM 990/204-1	37 days	480 hours
TM 990/204-2	34 days	240 hours
TM 990/204-3	30 days	120 hours

NOTE

Because of the heavy current requirements for NMOS memory, this board's battery-backup feature is intended for CMOS only.

- CRU-controllable functions include:
  - Write protect selected memory blocks (if protected, memory will be deselected, and an interrupt, at board interrupt level, can be specified by user)
  - Execute protect selected memory blocks (memory is not deselected; but interrupt, at board interrupt level, can be specified by user)
  - Set and read four flag bits
  - Control functions such as delete board memory from system, write-protect violation indicators, execute-protect violation indicators, board-was-addressed bit

TABLE 1-1. PRODUCT INDEX AND POWER REQUIREMENTS

Model	Shipped* Memory Size (Bytes)	Amperage at 5V (±3%)			
		CMOS		NMOS	
		Typ	Max	Typ	Max
TM 990/204-1	4K CMOS	1.10	1.98	1.42	2.46
TM 990/204-2	8K CMOS	1.16	2.30	1.78	3.26
TM 990/204-3	16K CMOS	1.27	2.94	2.5	4.86

*Shipped with CMOS only; NMOS power shown for information only.

- Designed to fit in TM 990 card cages (TM 990/510 or equivalent)
- DMA capability
- Board LEDs designate:
  - Attempt to execute instruction from an execute-protected block of memory
  - Attempt to write to write-protected block of memory
  - User-designated purpose, software programmable
- All memory can be write protected by a switch accessable to the user while the board is installed.
- Memory can be memory mapped into system using jumper-selectable addresses; includes optional extended addressing (address 1 M bytes)
- Selectable memory wait states
- Selectable interrupt levels (interrupts, if enabled, are caused by attempts to violate write-protected or execute-protected memory)

1.2 MANUAL ORGANIZATION

- Section 1 gives general information on the TM 990/204 board including specifications, board outline, etc.
- Section 2 describes how to unpack the board, how the jumpers are used to configure the board to the user's system, and how to plug the board into the system and do an initial board checkout.
- Section 3 covers programming aspects of the board.
- Section 4 covers board theory of operation.
- Appendices contain auxiliary information such as schematics, parts list, etc.

1.3 SPECIFICATIONS

- Module dimensions: See Figure 1-3
- Operating temperature: 0 to 70 °C (32 to 158 °F)
- Memory device compatibility includes:
  - CMOS: 6514 or equivalent
  - NMOS: 2114 or equivalent
  - Chip organization: 1024 x 4
- Frequency: 5 MHz maximum, memory wait states jumper selectable
- Typical power requirements at +5 V (±3%): see Table 1-1.
- Battery

	Gould MS2501	Gould MS2503	GE 41B019AD00201	Unit
Voltage	1.2 (3 needed)	3.6	3.6	V
Capacity	250	250	250	mA-H
Temp (Max)	70	70	70	°C
Dimensions:				
Diameter	0.563	0.563	0.62	inch
Heighth	1.200	3.55	3.87	inches

Manufacturers:

Gould Inc.
Portable Battery Div.
931 N. Vandalia St.
St. Paul, Minn. 55114

General Electric
Battery Department
P.O. Box 861
Gainesville, Fla. 32602

1.4 APPLICABLE DOCUMENTS

- TM 990/100MA Microcomputer User's Guide
- TM 990/101MA Microcomputer User's Guide
- TM 990/1481 High Performance CPU Module User's Guide
- TM 990 System Specification

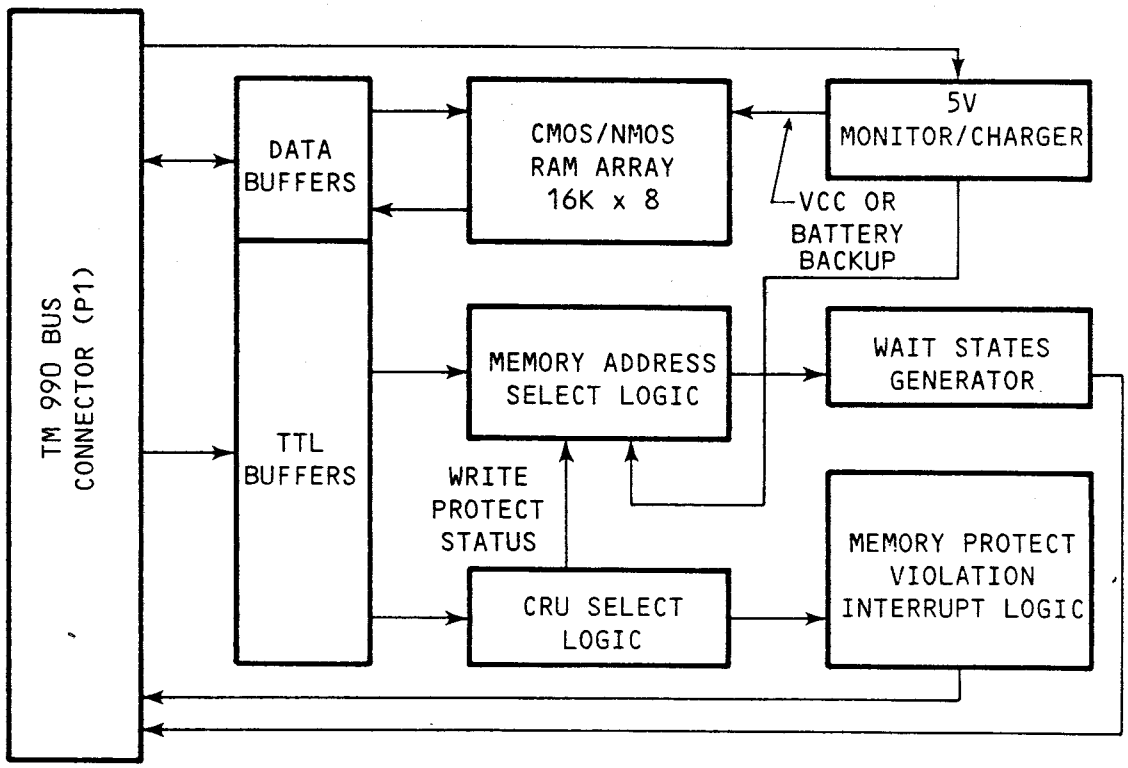


FIGURE 1-1. TM 990/204 BLOCK DIAGRAM

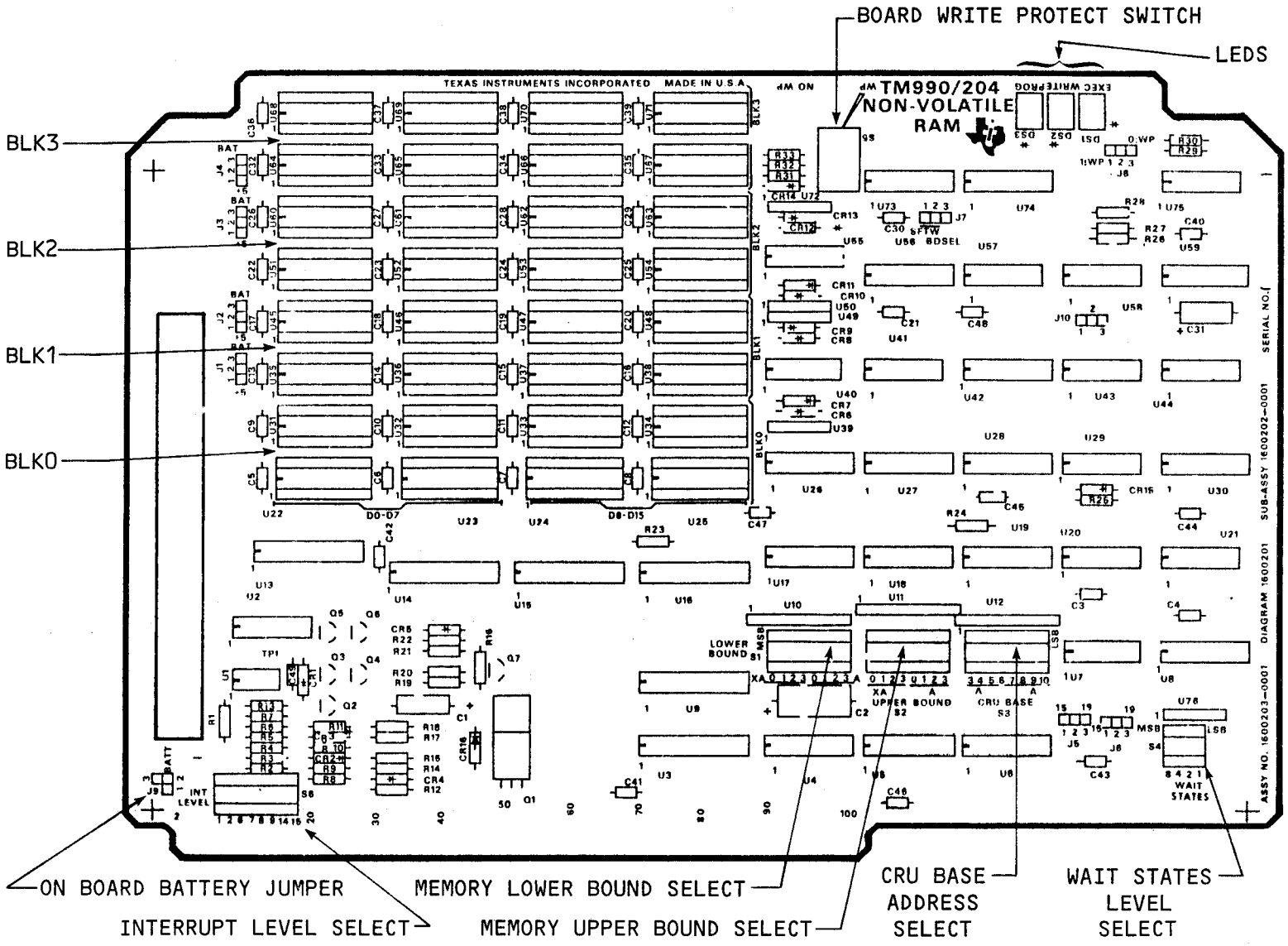
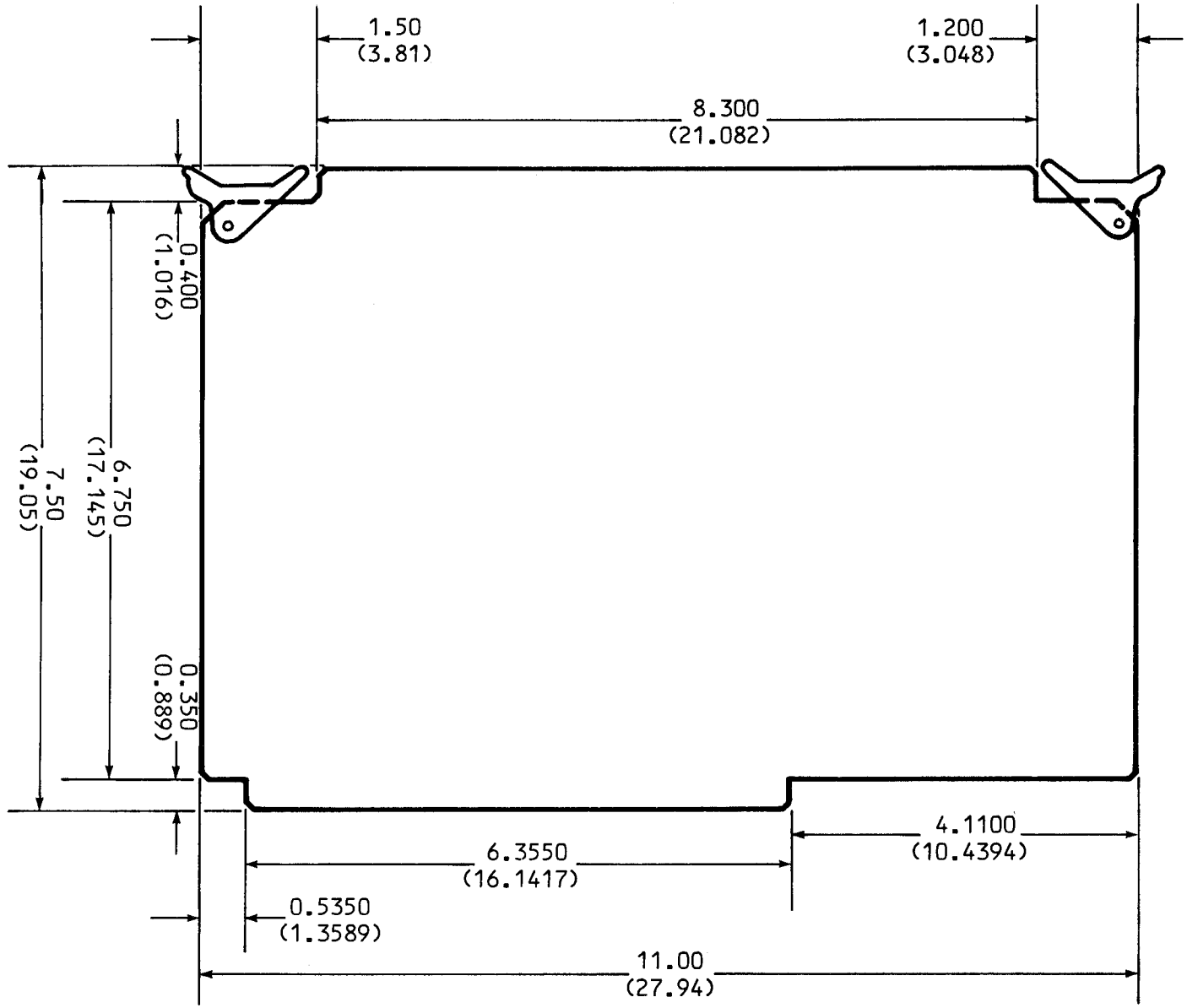


FIGURE 1-2. TM 990/204 MODULE PRINCIPAL COMPONENTS



NOTE: Top dimension is in inches and bottom dimension, in parenthesis, is in centimeters.

FIGURE 1-3. TM 990/204 MODULE DIMENSIONS

SECTION 2

INSTALLATION AND OPERATION

2.1 GENERAL

This section provides the procedure for unpacking and setting up the TM 990/204 module for operation with one of the TM 990 series of microcomputers compatible with the memory board's 16-bit data bus. A sample program is provided to demonstrate communication to a user-defined LED via the CRU (Communication Register Unit).

2.2 REQUIRED EQUIPMENT

The following equipment comprise the minimum system configuration required for the TM 990/204:

- Card cage such as TM 990/510 or equivalent
- Power supply such as the TM 990/518; selected supply must be large enough to provide required system voltages and current
- Compatible microcomputer board
- A suitable terminal is recommended to provide user communication to the system and also to perform the initial checkout routines in this section.

2.3 UNPACKING

Remove the TM 990/204 module from its carton. Check the module for any abnormalities that could have occurred in shipping. Report any discrepancies to your distributor immediately. Note that the battery is shipped disconnected from the board and must be connected via jumper J9 (paragraph 2.4.5). Sections 2.4 and 2.5 cover jumper and switch settings; section 2.6 describes steps for a typical installation.

2.4 JUMPER SETTINGS

This section defines the jumper configurations on the TM 990/204. As-shipped settings are shown in Table 2-1.

It is presumed that the user has a configured system including card cage, power supply, CPU board, and terminal. See the respective user's guides for installing these pieces of equipment.

CAUTION

Do not remove or install the TM 990/204 while power is applied to the card cage. Remove power to the card cage before installing or removing a module. Apply power only after installation or removal.

Table 2-1 is a summary of the board's jumpers which are further described in the following paragraphs. Note that the battery is shipped disconnected from the board and must be connected via jumper J9 (paragraph 2.4.5).

TABLE 2-1. JUMPER SETTINGS

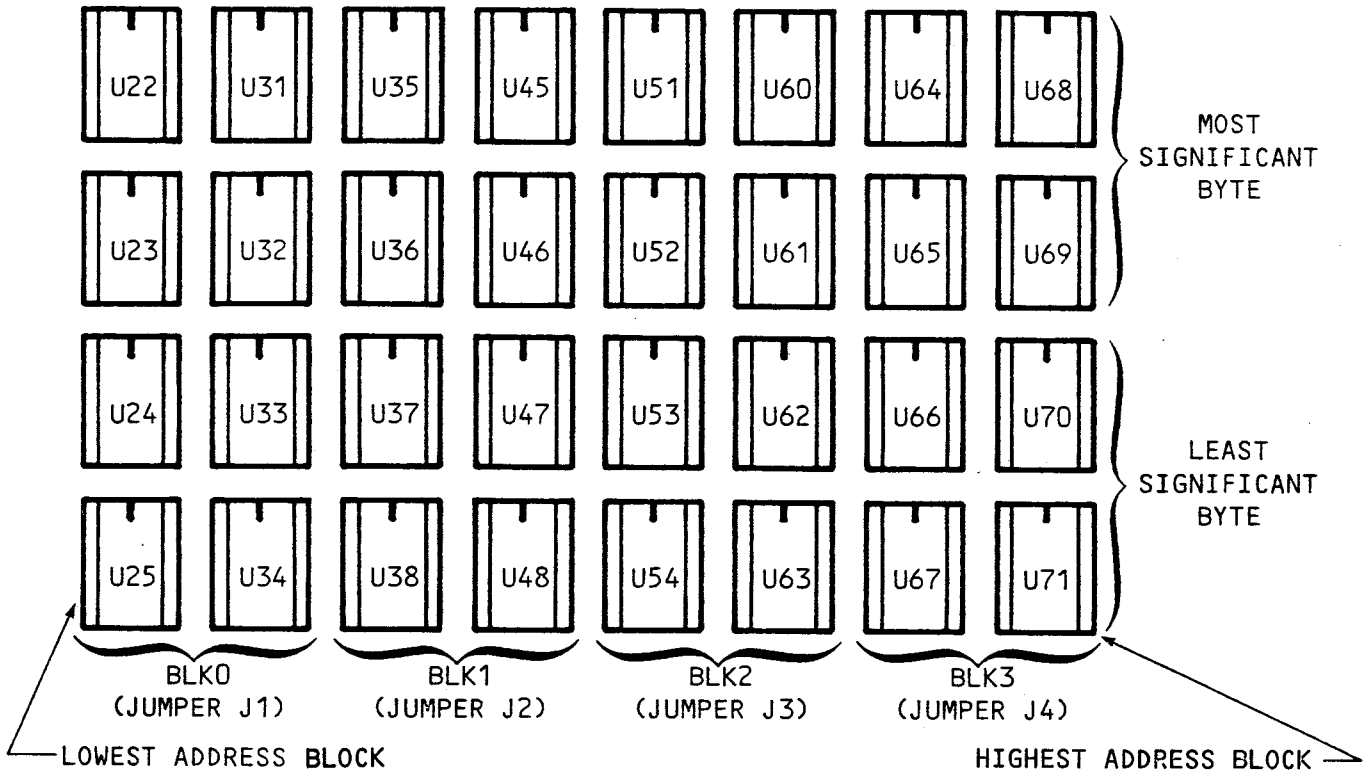
JUMPER & POSITION		PARA.	MEANING	AS SHIPPED (For each version)		
				-1	-2	-3
*J1	2-1	2.4.1	BLK0 not connected to battery backup			
	2-3		BLK0 connected to battery backup	2-3	2-3	2-3
*J2	2-1	2.4.1	BLK1 not connected to battery backup	2-1	2-3	2-3
	2-3		BLK1 connected to battery backup			
*J3	2-1	2.4.1	BLK2 not connected to battery backup	2-1	2-1	2-3
	2-3		BLK2 connected to battery backup			
*J4	2-1	2.4.1	BLK3 not connected to battery backup	2-1	2-1	2-3
	2-3		BLK3 connected to battery backup			
J5	2-1	2.4.2	Address lines A0-A3 decoded for lower memory bound	2-1	2-1	2-1
	2-3		**Address lines XA0-A3 decoded for lower memory bound			
J6	2-1	2.4.2	Address lines A0-A3 decoded for upper memory bound	2-1	2-1	2-1
	2-3		**Address lines XA0-A3 decoded for upper memory bound			
J7	2-1	2.4.3	Software setting of CRU bit 9 can either delete memory or allow memory access by the system	2-1	2-1	2-1
	2-3		Setting of CRU bit 9 doesn't affect memory access			
J8		2.4.4	Selects bit logic level to write to CRU bits 0 to 3 to cause Write Protect at BLK0 to BLK3			
	2-1		***One written to bits 0-3 causes WP of BLK0 to BLK3	2-1	2-1	2-1
	2-3		***Zero written to bits 0-3 causes WP of BLK0 to BLK3			
J9	2-1	2.4.5	Battery placed in circuit (connected to ground). User must install before battery can be used.	2-3	2-3	2-3
	2-3		Battery disconnected (board is shipped this way)			

NOTES

* Jumpers J1 to J4 select or deselect memory blocks BLK0 to BLK3 respectively from battery backup. These jumpers can be used to deselect NMOS memory, if used, because of NMOS memory's high current requirements.

** XA0 to XA3 are extended address lines (20 address lines)

*** Note that if J8 is set to the 2-3 position, then an I/O reset can cause a write protect of all memory blocks; if J8 is set to the 1-2 position, then an I/O reset will <u>not</u> cause memory write protect. (See WARNING in section 2.4.4.)



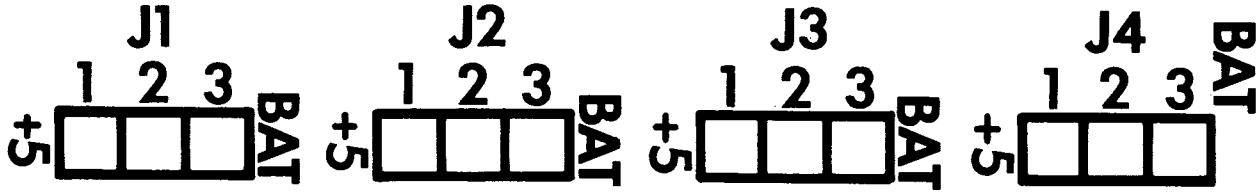
NOTE: Each block contains 4 K bytes as shown

FIGURE 2-1. MEMORY BLOCK ORGANIZATION

2.4.1 Connect/Disconnect Battery from Memory Blocks (Jumpers J1 to J4)

When a power failure occurs, the board's battery backup feature will provide power to battery blocks as selected at jumpers J1 to J4. These jumpers allow the user to connect or disconnect the battery backup from each of the four blocks of RAM (BLK0 to BLK3), shown organized in Figure 2-1. Since CMOS and NMOS RAM can be mixed onboard by individual blocks, these jumpers allow the user to disconnect battery backup to high power RAMS (i.e., NMOS). Prolonged heavy discharge can accidently shorten the life of a battery. The jumpers connect/disconnect the battery backup feature as shown below:

		Jumper Setting Battery Backup Feature	
RAM Block	Jumper	Connected	Disconnected
BLK0	J1	2-3	2-1
BLK1	J2	2-3	2-1
BLK2	J3	2-3	2-1
BLK3	J4	2-3	2-1

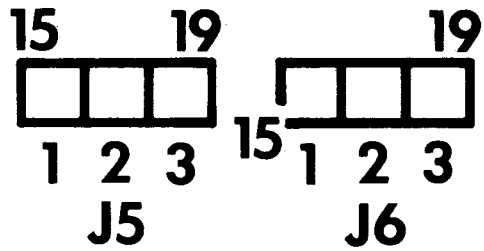


2.4.2 Decode/No-Decode of Extended Address Lines (Jumpers J5 and J6)

NOTE

The TM 990/204 memory board is designed to be addressed by TM 990 CPU boards capable of addressing 64 K bytes (32 K words) or 1 M bytes (500 K words) depending upon the microprocessor used. Because the TM 990/204 board can be populated with memory and addressed as 16-bit words, the addressing scheme for jumpers J5 and J6 utilizes 15 address lines (for 32 K words) or 19 address lines (for 500 K words).

Jumpers J5 and J6 designate the use of either extended addressing (19 address lines) or 15 address lines, depending upon the address structure of the microcomputer used. If extended addressing is used, extended address lines XA0, XA1, XA2, and XA3 are monitored along with lines A0 to A3; otherwise, only lines A0 to A3 are checked by the lower-bound comparator and upper-bound comparator as set at platforms S1 and S2 (see section 2.5.1). For TMS 9900 and S481 microprocessors, 15 address lines are decoded.

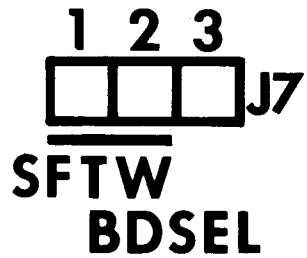


Two jumpers are provided, J5 and J6, one each for switches S1 and S2, which designate the lower bound and upper bound of memory respectively. Both jumpers should be set to decode the same address-line quantities. Jumper J5 designates address-line quantity for the memory lower bound (as set at platform S1), and jumper J6 designates address line quantity for the memory upper bound (as set at platform S2). Set the jumpers as shown below:

Jumpers J5/J6 Setting	Setting for 15 Address Lines	Setting for 19 Address Lines
J5 (Memory Lower Bound)	2-1	2-3
J6 (Memory Upper Bound)	2-1	2-3

2.4.3 Allow or Prevent Software to Delete/Map Board in System (Jumper J7)

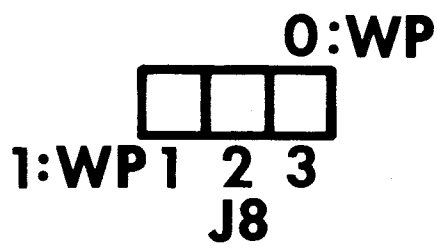
The board's memory can be deleted from the system or mapped into the system according to the software setting of bit 9 on the CRU (Communication Register Unit). This feature is allowed only if jumper J7 is set 2-1. Setting jumper J7 2-3 prevents using this software feature (setting of bit 9 will have no effect). Use of this CRU feature is further defined in section 3.6.



Jumper J7 Setting	
2-1	Allows software control to delete/enable memory
2-3	Disables software control to delete/enable memory

2.4.4 Select Logic Level to Enable/Disable Write Protect (Jumper J8)

Each of the four blocks of memory can be designated as write protected (cannot be written to, just read from) by software through CRU bits 0 to 3 as described in section 3.4.1. Jumper J8 allows selection of the logic level (a one or a zero) used by software to select this write protect feature. This option is one of convenience (i.e., write a one or a zero to a CRU bit); however, this jumper will be more effective for I/O reset purposes. If a one logic level is chosen (J8 set 2-1), then memory will not be write protected by an I/O reset (e.g., microcomputer RESET switch pressed); if a zero logic level is chosen, then memory will be write protected by an I/O reset. This latter position (2-3) will give optimum protection against the CPU altering RAM values should the CPU come up in an unknown state.



WARNING

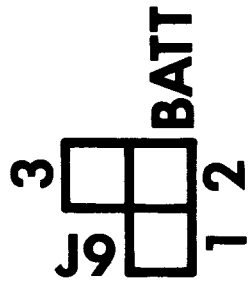
Note that a zero logic level (J8 set 2-3) is the default value when the jumper plug is totally removed, as this postion is in the etch of the board (default value if no jumper inserted). When using the J8 jumper in the 2-1 postion, the TM 990/204 requires a proper power-on reset (PRES.B-) to prevent erroneous data from being written into the board during powerup while the CPU is in an unknown state. In using the TM 990/204 with current CPU modules, including TM 990/100, TM 990/101, and TM 990/1481, the user must provide this reset capability offboard. Without such an offboard reset function, it is not recommended to use those CPU modules with the TM 990/204 with J8 in 2-1 position.

Jumper J8 Setting	Logic Level To Enable WP	Comment
2-1	One	No Write Protect on RESET
2-3	Zero	Write Protect on RESET

2.4.5 Connect Battery into Battery-Backup Circuit (Jumper J9)

The battery is shipped disconnected from the board circuitry by jumper J9. To connect the battery into the board circuitry, jumper as follows:

Jumper J11 Setting	
2-1	Battery connected into board backup circuitry
2-3	Battery disconnected from board circuitry



2.5 SWITCH SETTINGS

NOTE

Throughout this section, the terms "switch" and "jumper platform" are used interchangeably. The board is populated with five jumper platforms (S1 to S4 & S6). Selection of a position on the platform is made by inserting a jumper between two points on the platform. However, a standard DIP switch can be inserted on the platform to substitute for the jumper. Platform setting descriptions use the nomenclature silkscreened on the board.

Several options are available on the TM 990/204. In summary:

- S1: Selects lower address bound of RAM. If extended addressing (500 K words) is used, settings S1-XA0 to S1-A3 are used; if nonextended addressing (32 K words) is used, only S1-A0 to S1-A3 are used. This platform and platform S2 allow mapping the board into a system memory map scheme. Jumper J5 must be set to the number of address lines used (15 for 32 K words or 19 for 500 K words).

- S2: Selects upper address bound of RAM. If extended addressing (500 K words) is used, all switches S2-XA0 to S2-A3 are used; if nonextended addressing is used (32 K words), only S2-A0 to S2-A3 are used. Jumper J6 must be set to the number of address lines used (15 for 32 K words or 19 for 500 K words).

- S3: Selects the eight most-significant bits of the CRU address (values on address lines A3 to A10); this allows mapping the board's 16 CRU bits into the system CRU address scheme.

- S4: This four-position platform allows selection of 0 to 15 wait states depending upon access time of memory used and system clock.

- S5: Allows designating the entire board as write protected or not write protected. Designation can be made while board is installed in chassis. If write protect is selected (WP), this overrides any other jumper or software setting. If no write protection (NO WP) is selected, write protection is designated by other jumper settings and CRU bits.

- S6: Selects the interrupt level to the microcomputer board that would occur should a write- protect or execute-protect violation occurand the interrupt is selected by jumper and switch settings. If S6 is unpopulated, an interrupt level would not be sent to the system bus.

These platforms and switches are covered in the following paragraphs:

		Paragraph
• S1	Lower address bound	2.5.1
• S2	Upper address bound	2.5.1
• S3	CRU base address	2.5.2
• S4	Wait states	2.5.3
• S5	Write protect board	2.5.4
• S6	Interrupt Level Select	2.5.5

2.5.1 Select Memory Bounds (Platforms S1 and S2)

NOTES

1. Platform S1 specifies the 8 MSBs of the lower memory bound, and if BLK0 is populated, S1 specifies the beginning address of that block. S2 can be set to a value other than the actual 8 MSBs of the memory end address. These switches designate the addresses that will be interpreted by board hardware as the memory bounds.

2. If only 15 address lines are used (word addressing), failure to set jumpers J5 and J6 to 2-1 may inadvertently prohibit memory access.

Platforms S1 and S2 allow mapping the memory into a system memory map. Access to the board memory will be given only if the address is within the bounds specified by these switches. The most-significant bits (MSBs) of two addresses are specified by the user: the 4 or 8 MSBs of the lower address bound and the 4 or 8 MSBs of the upper address bound. Each is designated by an eight-position platform, divided into two four-bit segments:

(1) four extended address bits (XA0 to XA3), and
(2) four MSBs (A0 to A3) of address lines A0 to A14 (word addressing).

The use of extended and non-extended addressing must first be designated at jumpers J5 and J6 as explained in paragraph 2.4.2. The switches designate the following:

	Extended Addressing			Non-Extended Addressing		
	Platform	Setting	Jumper	Platform	Setting	Jumper
Memory lower bound	S1	XA0-A3	J5 2-3	S1	A0-A3	J5 2-1
Memory upper bound	S2	XA0-A3	J6 2-3	S2	A0-A3	J6 2-1

If extended addressing is not used, set jumpers J5 and J6 to 2-1, and platform settings XA0 to XA3 will be ignored. Table 2-2 lists various switch settings and corresponding address lines (in the table, an OFF indicates unjumpered or switch set to OFF, and an ON indicates jumpered or switch set to ON).

The "as shipped" switch S1 and S2 settings for all three versions of the TM 990/204 are shown below:

TM 990/204-1,2,3		TM 990/204-1		TM 990/204-2		TM 990/204-3	
SWITCH	LOCATION	SWITCH	LOCATION	SWITCH	LOCATION	SWITCH	LOCATION
S1-XA0	On	S2-XA0	On	S2-XA0	On	S2-XA0	On
S1-XA1	On	S2-XA1	On	S2-XA1	On	S2-XA1	On
S1-XA2	On	S2-XA2	On	S2-XA2	On	S2-XA2	On
S1-XA3	On	S2-XA3	On	S2-XA3	On	S2-XA3	On
S1-A0	On	S2-A0	On	S2-A0	On	S2-A0	On
S1-A1	On	S2-A1	On	S2-A1	Off	S2-A1	Off
S1-A2	Off	S2-A2	Off	S2-A2	On	S2-A2	Off
S1-A3	Off	S2-A3	Off	S2-A3	On	S2-A3	On

TABLE 2-2. LOWER AND UPPER ADDRESS BOUND SELECTION

[1]PLATFORM S1 OR S2 SETTING								LOWER BOUND (S1)	UPPER BOUND (S2)
XA0	XA1	XA2	XA3	A0	A1	A2	A3		
ON	ON	ON	ON	ON	ON	ON	ON	00000	00FFE
ON	ON	ON	ON	ON	ON	ON	OFF	01000	01FFE
ON	ON	ON	ON	ON	ON	OFF	ON	02000	02FFE
ON	ON	ON	ON	ON	ON	OFF	OFF	03000	03FFE
ON	ON	ON	ON	ON	OFF	ON	ON	04000	04FFE
ON	ON	ON	ON	ON	OFF	ON	OFF	05000	05FFE
ON	ON	ON	ON	ON	OFF	OFF	ON	06000	06FFE
ON	ON	ON	ON	ON	OFF	OFF	OFF	07000	07FFE
ON	ON	ON	ON	OFF	ON	ON	ON	08000	08FFE
ON	ON	ON	ON	OFF	ON	ON	OFF	09000	09FFE
ON	ON	ON	ON	OFF	ON	OFF	ON	0A000	0AFFE
ON	ON	ON	ON	OFF	ON	OFF	OFF	0B000	0BFFE
ON	ON	ON	ON	OFF	OFF	ON	ON	0C000	0CFFE
ON	ON	ON	ON	OFF	OFF	ON	OFF	0D000	0DFFE
ON	ON	ON	ON	OFF	OFF	OFF	ON	0E000	0EFFE
ON	ON	ON	ON	OFF	OFF	OFF	OFF	0F000	0FFFE
				.					
				.					
				.					
ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	7F000	7FFFE
OFF	ON	ON	ON	ON	ON	ON	ON	80000	80FFE
OFF	ON	ON	ON	ON	ON	ON	OFF	81000	81FFE
				.					
				.					
				.					
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	FF000	FFFFE

NOTES:

1. Address line is a 0 = ON switch setting (jumpered)
2. Address line is a 1 = OFF switch setting (unjumpered)

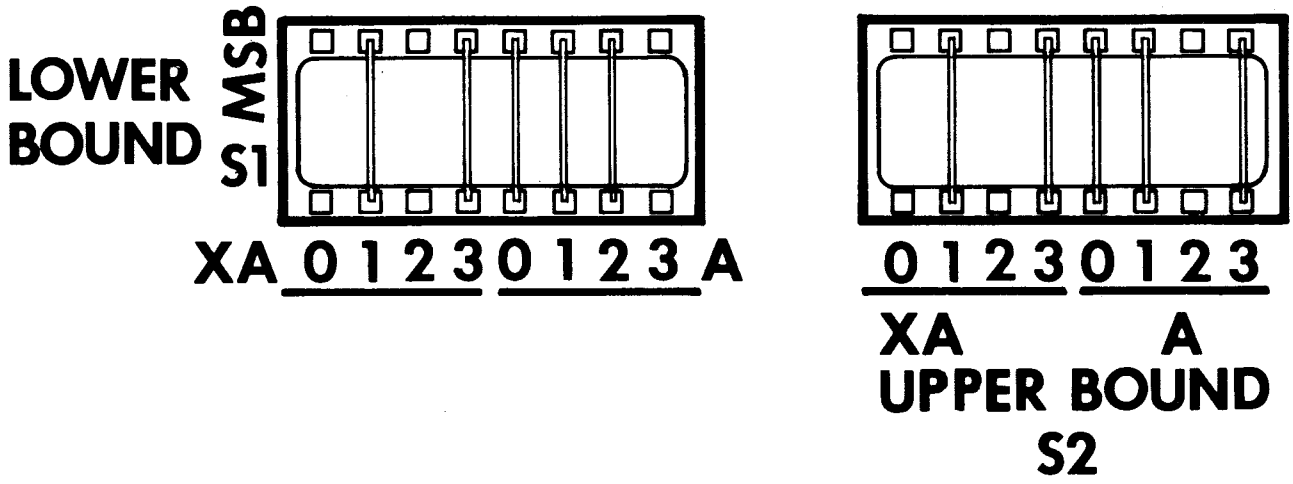


FIGURE 2-2. SWITCH S1 & S2 ADDRESS SELECTION (for examples)

NOTE

The memory in BLK0 will always start at the address bits selected in platform S1.

Address Example 1 (No Extended Addressing):

System does not have extended addressing, and BLK0 and BLK1 are populated with the eight K bytes of memory located between addresses 1000_{16} and $2FFE_{16}$:

- Set jumpers J5 and J6 to 2-1 (no extended addressing)
- Set platform S1-A0 to S1-A3 to ON ON ON OFF (1000_{16} lower bound)
- Set platform S2-A0 to S2-A3 to ON ON OFF ON ($2FFE_{16}$ upper bound)
- Platform S1-XA0 to S1-XA3 and S2-XA0 to S2-XA3 are ignored as jumpers J5 and J6 are set 2-1. The applicable halves of platforms S1 and S2 are shown properly jumpered in Figure 2-2.

Note that memory must exist in contiguous blocks, with each block taking up 4 K bytes of address space with BLK0 followed by BLK1, followed by BLK2, followed by BLK3.

Address Example 2 (Extended Addressing):

The example system uses extended addressing with BLK0 and BLK1 populated with the eight K bytes of memory located between addresses $A1000_{16}$ and $A2FFE_{16}$). The switch configuration is shown in Figure 2-2.

- Set jumpers J5 and J6 to 2-3 (extended addressing)
- Set platform S1-XA0 to S1-XA3 to OFF ON OFF ON ($A----_{16}$ extended address)
- Set platform S1-A0 to S1-A3 to ON ON ON OFF ($A1000_{16}$ remainder of address)
- Set platform S2-XA0 to S2-XA3 to OFF ON OFF ON ($A----_{16}$ extended address)
- Set platform S2-A0 to S2-A3 to ON ON OFF ON ($A2FFE_{16}$ remainder of address)

2.5.2 Select Start of CRU Address Space (Jumper Platform S3)

Through the Communications Register Unit (CRU), the microprocessor can serially communicate using single-bit and multiple-bit instructions to external hardware. The TMS 9900 and S481 microprocessors can address from 1 to 4096 CRU bits by using the value on address lines A3 to A14. This value is placed in register 12 before executing one of the five CRU instructions (see your microcomputer user's guide for further information on CRU instructions and adddressing). The four LSB's of this 12-bit address select one of the 16 CRU bits as further defined in Section 3. The eight MSB's of this address are selected at jumper platform S3, which allows the user to designate a beginning CRU address in order to map the TM 990/204 board into an overall system CRU address scheme. For example, if three TM 990/204 boards are in the same system, each must have a unique CRU address so that their CRU bits can be selected individually. The boards' switches can be set so that each board's address is contiguous with the other boards.

Two CRU terms:

- CRU hardware base address: The value on bits 3 to 14 of register 12 when a CRU instruction is executed. A displacement is added or subtracted from this value (as required by the instruction) to select the desired bit to address.

- CRU software base address: The entire contents of register 12 when a CRU instruction is executed.

Table 2-3 shows the settings on platform S3. The Software Base Address column lists the resulting values in bits 3 to 10 of register 12, (thus, also on address lines A3 to A10 that will be compared to the platform values). This is the same as the eight MSB's of the CRU hardware base address. The four LSB's on the address lines (A11 to A14) address one of the 16 CRU functions on the board. If the values at platform S3 and address lines A3 to A10 compare, the corresponding board CRU functions will be addressed. Note that an ON setting (jumper installed) corresponds to a zero address bus value, and an OFF setting (jumpered not installed) corresponds to a one address bus value.

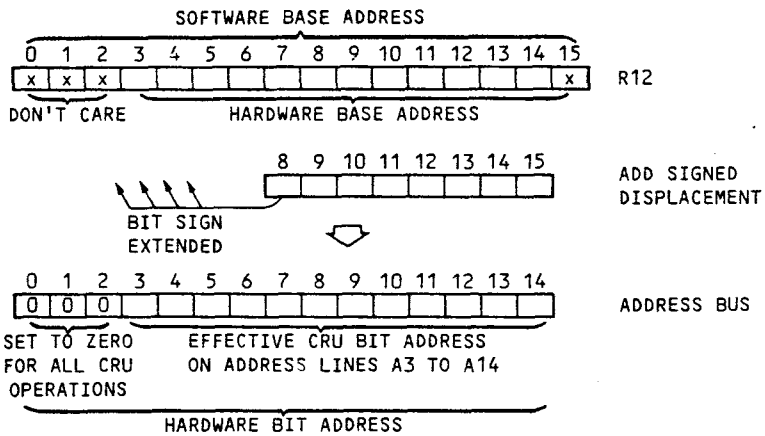
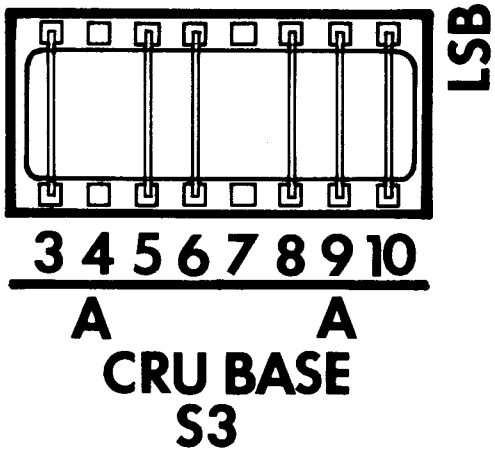


FIGURE 2-3. CRU ADDRESS NOMENCLATURE

TABLE 2-3. CRU BASE ADDRESS SELECTION

SWITCH S3 SETTING								SOFTWARE BASE ADDRESS	HARDWARE BASE ADDRESS
A3	A4	A5	A6	A7	A8	A9	A10		
ON	ON	ON	ON	ON	ON	ON	ON	0000	0000
ON	ON	ON	ON	ON	ON	ON	OFF	0020	0010
ON	ON	ON	ON	ON	ON	OFF	ON	0040	0020
ON	ON	ON	ON	ON	ON	OFF	OFF	0060	0030
ON	ON	ON	ON	ON	OFF	ON	ON	0080	0040
ON	ON	ON	ON	ON	OFF	ON	OFF	00A0	0050
				•					
				•					
				•					
ON	ON	ON	ON	OFF	ON	ON	ON	0100	0080
ON	ON	ON	ON	OFF	ON	ON	OFF	0120	0090
				•					
				•					
				•					
ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0FE0	07F0
OFF	ON	ON	ON	ON	ON	ON	ON	1000	0800
OFF	ON	ON	ON	ON	ON	ON	OFF	1020	0810
				•					
				•					
				•					
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	1FE0	0FF0

NOTE: 0 = ON switch setting or jumpered (tied low)
1 = OFF switch setting or not jumpered (tied high)



NOTES

1. Setting shown for hardware base addresses 0480_{16} - $048F_{16}$
2. Jumpered = zero address line
   Unjumpered = one address line
3. As shipped configuration for 204-1, -2, -3.

FIGURE 2-4. CRU SWITCH SETTINGS AT S3 (for example below)

Example:

Determine the CRU software base address (contents to load into register 12) and S3 settings when a hardware base address of 0480_{16} is used.

1. Write <u>hardware base address</u> in binary (corresponding to the eight MSBs of the address lines):

A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	
0	1	0	0	1	0	0	0	0	0	0	0	(binary)
	4				8				0			(hex)

2. Place another zero on the right and shift left one bit (multiply hardware base address by 2 to get <u>software base address</u>):

	0	1	0	0	1	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1	0	0	0	0	0
	0				9				0			0 (hex)

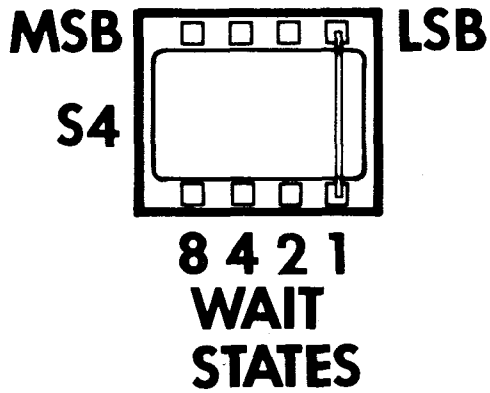
3. To determine switch settings, write the <u>hardware base address</u>. The eight MSB's on address lines A3 to A14 are the settings of switch S3 with a zero indicating an ON setting and a one indicating an OFF setting:

	0	1	0	0	1	0	0	0	
	↓	↓	↓	↓	↓	↓	↓	↓	(binary)
S3-	3	-4	-5	-6	-7	-8	-9	-10	
	ON	OFF	ON	ON	OFF	ON	ON	ON	(Platform S3 setting)

Thus, for a hardware base address of 0480_{16} (step 1 above), load register 12 with 0900_{16} (step 2 above) and set switches as in step 3 above. The range of CRU addresses are listed in Table 2-3.

2.5.3 Wait State Selection for Different Memories (Platform S4)

Because the TM 990/204 memory expansion board may be populated with different speed (access time) memories or used with different system bus clocks, wait states may be required to complete a memory read/write cycle. Platform S4 allows setting 0 to 15 wait states as shown by the settings in Tables 2-4 and 2-5.



For example, the TM 990/204 is shipped with 6514 CMOS RAMs (450 ns access time) requiring 1 wait state with a 3 MHz clock or 2 wait states with a 5 MHz clock.

TABLE 2-4. WAIT STATE SELECTION AT PLATFORM S4

SWITCH SETTING AT S4[1]				WAIT STATES[2]	MIN. WAIT PERIOD IN NS	
8	4	2	1		3 MHz CLOCK	5 MHz CLOCK
OFF	OFF	OFF	OFF	0	000 ns	000 ns
OFF	OFF	OFF	ON	1	330 ns	198 ns
OFF	OFF	ON	OFF	2	660 ns	396 ns
OFF	OFF	ON	ON	3	990 ns	585 ns
OFF	ON	OFF	OFF	4	1320 ns	792 ns
OFF	ON	OFF	ON	5	1650 ns	990 ns
OFF	ON	ON	OFF	6	1980 ns	1188 ns
OFF	ON	ON	ON	7	2310 ns	1386 ns
ON	OFF	OFF	OFF	8	2640 ns	1584 ns
ON	OFF	OFF	ON	9	2970 ns	1782 ns
ON	OFF	ON	OFF	10	3300 ns	1980 ns
ON	OFF	ON	ON	11	3630 ns	2178 ns
ON	ON	OFF	OFF	12	3960 ns	2376 ns
ON	ON	OFF	ON	13	4290 ns	2574 ns
ON	ON	ON	OFF	14	4620 ns	2772 ns
ON	ON	ON	ON	15	4950 ns	2970 ns

NOTE: 1. ON = jumpered; OFF = unjumpered

TABLE 2-5. WAIT STATES FOR EXAMPLE MEMORIES

MEMORY SPEED	WAIT STATES		MEMORY TYPE
	3 MHz	5 MHz	
150 ns	0	0	TMS 2114-15 (NMOS)
250 ns	0	1	TMS 2114-25 (NMOS), uPD444/6514-3 (CMOS)
450/500 ns	1	2	uPD444/6514 (CMOS)
650 ns	2	3	
800 ns	2	4	

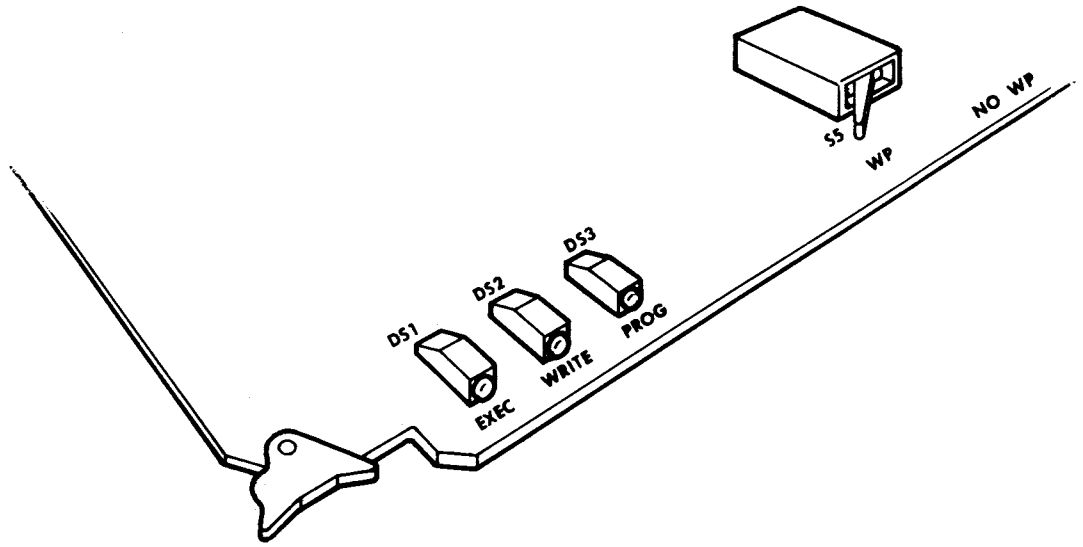


FIGURE 2-5. LEDs AND WRITE PROTECT SWITCH AT FRONT OF BOARD

2.5.4 Write Protect Entire Board (Switch S5)

Switch S5 allows a hardware setting of all the onboard memory to a write protect state (cannot be written to). Switch S5 is accessable from the front of the board when installed in a card cage as shown in Figure 2-5. Set the switch as follows:

Switch S5 Setting	
WP	Write protect all memory
NO WP	Write protect blocks only as set by software

When the switch is set to NO WP, write protect is CRU selectable (software selectable) on a block basis through CRU bits 0 to 3.

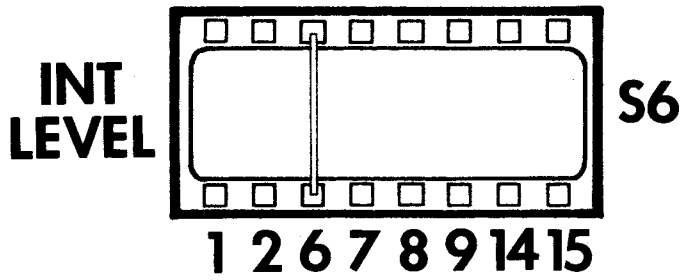
When switch S5 is set to WP, software cannot disable the write protect status of the entire memory as set by this switch. Also, when set to WP, a write-protect interrupt will not occur unless a write-protect interrupt was also enabled via CRU bits 0 to 3 and the interrupt level set at platform S6. Merely setting S5 to WP does not also cause a write-protect interrupt. The setting of this switch can be checked through software by reading CRU bit 10.

2.5.5 Select Level of Interrupt to CPU (Platform S6)

Several interrupt levels or a no-interrupt can be selected. This interrupt will go to the CPU board if a level is selected at platform S6 and either of the following two violations is attempted:

- Attempt to write into a memory block which has been designated as write protected through CRU bits 0-3
- Attempt to execute an instruction in a block of memory which has been designated as execute-protected through CRU bits 4-7.

If an attempt is made to violate these CRU-selectable protections, an interrupt, if jumpered at platform S6, is sent to the CPU. The interrupt service routine can then check for possible causes (CRU bits 8 and 9 indicate if a write- or execute-protect violation occurred) The following interrupts can be selected at S6: 1, 2, 6, 7, 8, 9, 14, 15 as shown on the silkscreen at the jumper platform. The adjacent platform drawing shows interrupt 6 jumpered, the level jumpered as shipped.



2.6 LED INDICATORS

Three LEDs are provided at the front of the board as shown in Figure 2-5. These indicate the following as seen from left to right:

- EXEC (DS1): Execute-protect violation attempted. Will remain lit until reset by writing first a zero and then a one to CRU bit 8.
- WRITE (DS2): Write-protect violation attempted. Will remain lit until reset by writing first a zero and then a one to CRU bit 8.
- PROG (DS3): Reserved for user definition. This can be lit or turned off by setting CRU bit 10 to a zero or one respectively.

Note that if enabled at CRU bits 0 to 7, a write-protect or execute-protect violation attempt will always illuminate an LED. However, actual sending of an interrupt depends upon jumpering platform S6.

2.7 INSTALLING A MINIMUM SYSTEM

After making the desired jumper and switch settings, the user can install a minimum system as described below. Also, sections 2.9 and 2.10 contain several general demonstration routines, complete with jumper and switch settings, that can be executed to demonstrate general board operation. Make the following attachments and installations:

1) Attach power supply connections to the card cage as shown in the card cage user manual.

CAUTION

Power should always be disconnected when attaching power cable to a chassis or when installing or removing a board from a card cage.

2) Make the proper jumper connections as listed in Table 2-1 and explained in section 2.4. If battery backup is desired, please jumper J9 in the 2-1 postion; this jumper is shipped 2-3 to deselect battery backup. The battery will come to a full charge within 16-20 hours.

3) Make the proper platform connections as described in section 2.5.

4) Install the microcomputer board and TM 990/204 board into the card cage. If DMA is to be used, make the appropriate modifications to the backplane as described in the card cage user manual.

5) Attach the terminal cable to the EIA port on the microcomputer.

6) Apply power. If the TIBUG monitor is installed, it should come up by actuating the RESET switch on the microcomputer board and pressing the RETURN key on the terminal.

2.8 CONSIDERATIONS

- Do not remove or install the TM 990/204 board while system Vcc power is applied.
- Upon an I/O reset (e.g., by toggling the RESET switch on the microcomputer board), all CRU bits are reset to the zero level. This means that the execute-protect feature is disabled after an I/O reset and must be set by software (the write-protect feature is conditional on jumper J8 set 2-3; see section 2.4.4).
- Battery backup merely retains RAM data during a power loss to the system; other board logic is not backed up. Battery data is provided in section 2.11.
- If more than one memory module is in a system, each must occupy unique (1) memory space and (2) CRU address space.

2.9 EXAMPLE PROGRAM

The following programs can be used to immediately demonstrate operation of the TM 990/204 expansion memory board.

The following program demonstrates communication to the board via the CRU (the CRU is further explained in Section 3). This program, if loaded at memory address 1000_{16} on the memory board will cause the user LED (marked DS3 as shown in Figure 2-5) to blink. Loading and executing this program requires that the monitor (e.g., TIBUG) be installed on the microcomputer board.

The following are program aspects:

1) CRU software base address is 0900_{16} (switch S3 set as in Figure 2-4).
2) Minimum memory required is a half block (more optional) inserted in BLK0.
3) Memory start address is 1000_{16} with platforms S1 and S2 set as shown in Figure 2-2. If extended addressing used, switches S1-XA0 to S1-XA3 and S2-XA0 to S2-XA3 are set to all ON.
4) Jumpers J5 and J6 set to 2-1 for non-extended addressing or 2-3 for extended addressing, as required.
5) Jumper J8 is set 2-1 for no write protect at RESET.

Do not use the CRU command of the monitor after powerup and before executing this program as bits can be mistakenly written to that would affect program execution.

Powerup the system. Toggle the RESET switch on the microcomputer board; the monitor heading should be printed on the terminal.

Load the following program at the memory address shown in the left column below beginning at 1000_{16} using the memory inspect/change command (M) of the monitor (TIBUG commands are used herein). Beginning at address 1000_{16}, change the location's contents to the object values as shown in the listing below (Objt column), then repeat at the next memory address using the space bar. When last value is entered, complete this final memory change with a carriage return, then use the monitor to change the Program Counter to 1000_{16}, and execute with the monitor execute (E) command.

```
Mem.
Addr Objt

1000 02E0        LWPI   > 1020          SET WORKSPACE POINTER
1002 1020
1004 020C        LI     R12, >900       LOAD SOFTWARE BASE ADDRESS INTO R12
1006 0900
1008 1D0A  LOOP  SBO    10              TURN ON USER LED
100A 0600        DEC    R0              DECREMENT COUNTER TO ZERO
100C 16FE        JNE    $-2             LOOP UNTIL ZERO
100E 1E0A        SBZ    10              TURN OFF USER LED
1010 0600        DEC    R0              DECREMENT COUNTER TO ZERO
1012 16FE        JNE    $-2             LOOP UNTIL ZERO
1014 10F9        JMP    LOOP            REPEAT BLINK SEQUENCE
```

Exit this loop by pressing the microcomputer RESET switch.

2.10 DEMONSTRATING WRITE PROTECT USING TIBUG COMMANDS

The programmable (through the CRU) write-protect bits can be demonstrated by using the system monitor (e.g., TIBUG, the commands used herein).

The following are program aspects (the first five steps are the same as for the program in 2.8; the sixth step has been added):

1) CRU software base address is 0900_{16} (hardware base address of 0480_{16}) used with switch S3 set as shown in Figure 2-4.

2) Minimum memory required is a half block (more optional) inserted in BLK0.

3) Memory start address is 1000_{16} with switches S1 and S2 set as shown in Figure 2-2.

4) Jumpers J5 and J6 set to 2-1 for non-extended addressing or 2-3 for extended addressing.

5) Jumper J8 set 2-1 for no write protect at RESET (also designates that a one sets write protect and a zero disables write protect when writing to CRU bits 0 to 3 (corresponding to blocks BLK0 to BLK3)).

6) Platform S6 unjumpered so that no interrupt will be issued when a write protect violation occurs.

By using the CRU (C) command of the monitor (e.g., TIBUG), a populated block of memory can be write protected or unprotected. This feature can be then demonstrated by using the memory inspect/change (M) monitor command to attempt changing memory (writing to it).

To address the board as mapped into the CRU at software base address 0900_{16}, use the CRU inspect/change command (C) running under the monitor. Then write to the CRU by designating a value to apply to the CRU address. See your microcomputer user's guide for detail information on this TIBUG command.

To demonstrate write protecting BLK0, do the following exercise at the terminal (note, CR = carriage return, SP = space, MS = minus key, and XXXX = unknown hex value).

Keyboard Interaction	Comment
?C 900 (CR)	View CRU values beginning at 0900_{16}
0900 = XXXX 0000 (CR)	CRU bits to zero (no write protect)[1]
?M 1000 (CR)	Inspect beginning of memory
1000 = XXXX AAAA (SP)	Change address contents to AAAA
1002 = XXXX BBBB (SP)	Change address contents to BBBB
1004 = XXXX CCCC (SP)	Change address contents to CCCC
1006 = XXXX (MS)	Minus key returns to previous address
1004 = CCCC (MS)	Value changed (address written to)
1002 = BBBB (MS)	Value changed
1000 = AAAA (CR)	Value changed
?C 900 (CR)	Return to CRU address 0900_{16}
0900 = 0000 0401 (CR)	Write protect BLK0, turn on user LED[1]
?M 1000 (CR)	Return to memory again
1000 = AAAA 1111 (SP)	Attempt to change (write to) address
1002 = BBBB 2222 (SP)	Attempt to change address contents
1004 = CCCC 3333 (SP)	Attempt to change address contents
1006 = XXXX (MS)	Minus key returns to previous address
1004 = CCCC (MS)	Contents unchanged, write protected
1002 = BBBB (MS)	Contents unchanged. write protected
1000 = AAAA (CR)	Contents unchanged, write protected
?	

NOTE: 1. All zeroes written to the CRU base address disables write protect and turns off the user LED. A hex pattern of 0401 to the CRU base address contains two one-value bits which enable write protect and turn on the user LED.

2.11 BATTERY BACKUP

The TM 990/204 module comes with a 3.6 V dc (nominal) battery which supplies Vcc to the memory chips in case of a power failure. Battery backup is provided for a 96-hour period on a fully populated board, with additional time on a partially populated board. Onboard circuitry determines a power failure to make the switch to battery backup.

The module is shipped with the battery disconnected from onboard circuitry. Jumper J9 must be set 2-1 for connecting the battery to the backup circuitry. Jumpers J1 to J4 select battery backup for RAM blocks BLK0 to BLK3 respectively; these must be installed 2-3 to be connected to battery backup. The user is able to specify battery backup for just part of the memory blocks; this permits a mix of CMOS RAM and NMOS RAM. Because NMOS RAM requires a high amount of current; jumpers J1 to J4 allow NMOS blocks to be deselected.

Two manufacturers that provide replacement batteries for the TM 990/204:

1) Part no.: MS2501 and MS2503

   Company: Gould, Inc.
   Portable Battery Division
   931 N. Vandalia Street
   St. Paul, Minnesota 55114

2) Part no.: 41B019AD00201

   Company: General Electric
   Battery Department
   P.O. Box 861
   Gainesville, Fla. 32602

Battery specifications are listed in section 1.3. Detail specifications are available from the manufacturer.

If the Gould model MS2501 is preferred, three batteries are used. In this case, inter-battery connection is made on the board by soldering the battery leads to the plated through holes positioned between the first and second batteries and between the second and third batteries on the board.

CAUTION

Do not place or lay the TM 990/204 Module on a conductive surface. You may seriously damage the battery and CMOS RAM if a metal surface touches the conductor side of the module.

SECTION 3

PROGRAMMING THE TM 990/204

3.1 GENERAL

The TM 990/204 has several programming features using the Communication Register Unit (CRU). Each board must have a unique CRU address, and the selection of the CRU addresses is defined in section 2.5.2 of this manual and in your microcomputer user's guide. Table 3-1 is a summary of the 16 programmable CRU addresses on the TM 990/204, showing the results of reading and applying various logic levels at the different displacements from the base address.

3.2 SELECT CRU BASE ADDRESS

The CRU base address is first selected in hardware as shown in section 2.5.2, which describes setting switch platform S3. If more than one TM 990/204 board is in a system, programming will be facilitated by making each board's 16-bit CRU address space contiguous (e.g., 0200_{16}, 0220_{16}, etc., for software base addresses). This allows multiboard access using different displacements without changing register 12 contents. Be aware of other CRU addresses in the system; use a software base address of 0200_{16} or greater to avoid conflicts with dedicated CRU features on the microcomputer board.

CAUTION

In constructing a CRU map for a system, be careful that CRU addresses for each board are unique in the system so that CRU addresses on one board do not conflict with addresses on other boards.

Example to load the software base address:

```
LI    R12,>200        SET SOFTWARE BASE ADDRESS OF  0200
```

This will be the CRU address used for some examples in this section. Once the software base address has been chosen at switch S3 and loaded into register 12, single-bit CRU instructions can be used to address any of the CRU bits:

```
SBZ   0               BLK0 NOT WRITE PROTECTED
SBO   1               BLK1 WRITE PROTECTED
```

Or the same effect can occur using multibit instructions:

```
LI    R1,>0200        LOAD BINARY VALUE 0000 0010 IN 1ST BYTE OF R1
LDCR  R1,2            BLK0 NOT WRITE PRTED; BLK1 WRITE PRTED
```

3.3 CRU BITS

Table 3-1 lists the different functions available through the CRU. These are covered in the following paragraphs.

NOTE

An I/O reset (e.g., caused by pressing the microcomputer RESET switch) will place all CRU bits in the zero state.

TABLE 3-1. TM 990/204 CRU MAP (Sheet 1 of 2)

DISPLACEMENT	READ BIT MEANING	[1]WRITE-TO-BIT EFFECT
0	Setting of BLK0 write protect bit as set according to WRITE-TO-BIT column on right	2^0 = BLK0 not write protected 2^1 = BLK0 write protected
1	Setting of BLK1 write protect bit as set according to WRITE-TO-BIT column on right	2^0 = BLK1 not write protected 2^1 = BLK1 write protected
2	Setting of BLK2 write protect bit as set according to WRITE-TO-BIT column on right	2^0 = BLK2 not write protected 2^1 = BLK2 write protected
3	Setting of BLK3 write protect bit as set according to WRITE-TO-BIT column on right	2^0 = BLK3 not write protected 2^1 = BLK3 write protected
4	Setting of BLK0 execute protect bit as set according to WRITE-TO-BIT column on right	0 = BLK0 not execute protected 1 = BLK0 execute protected
5	Setting of BLK1 execute protect bit as set according to WRITE-TO-BIT column on right	0 = BLK1 not execute protected 1 = BLK1 execute protected
6	Setting of BLK2 execute protect bit as set according to WRITE-TO-BIT column on right	0 = BLK2 not execute protected 1 = BLK2 execute protected
7	Setting of BLK3 execute protect bit as set according to WRITE-TO-BIT column on right	0 = BLK3 not execute protected 1 = BLK3 execute protected
8	0 = No write-protect violation (latch) 1 = Write-protect violation occurred (latched) NOTE The toggle procedure for bit 8 (set to one then set to zero) is opposite that for bit 11.	1/0=When a write protect or execute protect violation occurs, bit 8 or 9 (depending on the violation) is set to a one and it (they) remains in that state until write-bit 8 is reset. Bit 8 is reset by writing a one to it and then writing a zero to it (i.e., toggle bit 8). If bit 8 is not toggled, the value at that bit will remain at its present value. By toggling bit 8, LEDs DS1 and DS2 are extinguished and bit 8 is set to a zero state to allow sensing a state change should a write-protect or execute-protect violation occur.

TABLE 3-1. TM 990/204 CRU MAP (Sheet 2 of 2)

DIS-PLACE-MENT	READ BIT MEANING	WRITE-TO-BIT EFFECT
9	0 = No execute-protect violation 1 = Execute-protect violation occurred (latched)	0 = Memory available to system 1 = Memory cannot be accessed
10	0 = Wrt Prot Switch S5 to WP 1 = Wrt Prot Switch S5 to NO WP	0 = Turn off user LED DS3 1 = Turn on user LED DS3
11	0 = Board not addressed (latch); a change from this state to a one indicates the board had been addressed. 1 = Board had been addressed (latch) NOTE The toggle procedure for bit 11 (set to zero then one) is opposite that for bit 8.	1/0=When a board-addressed condition occurs, bit 11 is set to a one and remains in that state until reset.Bit 11 can be reset by first writing a zero to it and then writing a one to it (i.e., toggle bit 11). If the bit is not toggled, the bit will remain in its present state. If bit 11 is toggled, its read value will be set to a zero to allow sensing a state change (to a one) should a board-addressed condition occur.
12	Flag bit value as set	Set Flag bit to one or zero
13	Flag bit value as set	Set Flag bit to one or zero
14	Flag bit value as set	Set Flag bit to one or zero
15	Flag bit value as set	Set Flag bit to one or zero

NOTES:

1. An I/O reset (e.g., RESET switch pressed at the microcomputer board) will cause the execute protect bits as well as CRU bits (except as noted in note 2 below) to be set to zero. In other words, pressing the RESET switch on the microcomputer board sets no-execute-protect, turns off LEDs, sets flag bits to zero, allows memory access, etc.
2. The effect of writing a one or zero to CRU bits 0 to 3 is shown in this table only when jumper J8 is set 2-1. If J8 is set 2-3, then the effect of a one or zero as shown in this table is reversed. In effect, jumper J8 allows the programmer to select which logic level (one or zero) he desires to use in setting or resetting a CRU bit to cause write protect. When J8 is jumpered 2-1, an I/O reset (e.g., RESET pressed on the microcomputer) causes a zero to be output to these four CRU ports; thus, causing memory to be <u>not</u> write protected upon a reset. (See warning in section 2.4.4.) The board is shipped with jumper J8 set 2-1, the setting used in this table to show the effects of writing to bits 0 to 3.

3.4 WRITE- AND EXECUTE-PROTECT MEMORY

3.4.1 Software Write Protect of Memory (CRU Bits 0-3)

Blocks BLK0 to BLK3 can be set to a write-protect or a no-write-protect by addressing CRU bits 0 to 3. The effect of setting these bits is conditional on four other prerequisites:

- Setting of switch S5. If set to the WP (write protect) position, all memory will be write protected regardless of the setting of CRU bits 0 to 3. Set switch S5 to NO WP to use CRU bits 0 to 3.

- Setting of jumper J8 selects the logic level to cause a write-protect or no-write-protect condition as described in note 1 to Table 3-1 and in paragraph 2.4.4. As shipped, J8 is set 2-1 meaning a one sets write protect and thus no write protect occurs upon an I/O reset (e.g., RESET switch pressed on the microcomputer causes I/O reset).

- If a write-protect violation had occurred, CRU bit 8 must be toggled (to a one, then to a zero) before another write-protect violation can cause new violation-occurred conditions (LED DS2 lit, an interrupt issued if jumpered at S6, and a one value at CRU bit 8).

- Platform S6 must be jumpered to one of the interrupt levels if an interrupt is desired when an attempt is made to write to a write-protected block. The jumpering of platform S6 is explained in section 2.5.5.

Note that a block is the smallest area of memory that can be protected or unprotected. Blocks are shown in Figure 2-1.

The value read at CRU bits 0 to 3 will be the value set at those bits, reflecting the write-protect status of each block as set through the CRU.

The following example write protects all four blocks:

```
LI   R12,>0200      SOFTWARE BASE ADDRESS OF 1ST CRU BIT (0)
LI   R1,>0F00       BINARY 1111 IN FIRST BYTE
LDCR R1,4           APPLY ALL ONES TO CRU BITS 0-3
```

Checking for a write protect violation is made by testing CRU bit 8 as described in section 3.5.1.

These are latched interrupt requests; they set CRU bit 8 to a one and illuminate LED DS2. To clear the latched write-protect indicators, toggle CRU bit 8 by first writing a one to it to unlatch the indicators and then write a zero to it to allow the latching of future write-protect indications:

```
* TOGGLE CRU BIT 8 TO RESET AND RETRIGGER WRITE PROTECT LATCHES
     SBO  8              UNLATCH INTERRUPT AND LED INDICATORS
     SBZ  8              READY FOR NEXT WP VIOLATION
```

3.4.2 Execute Protect Memory (CRU Bits 4 to 7)

Memory blocks BLK0 to BLK3 can be execute protected. This will cause an interrupt condition when the memory area is accessed for an instruction. An interrupt is conditional on several prerequesites:

- If an execute-protect violation had occurred, CRU bit 8 must be toggled (to a one, then to a zero) before another execute-protect violation can cause new violation-occurred conditions (LED DS1 lit, an interrupt issued if jumpered at S6, and a one value at CRU bit 9).

- Platform S6 must be jumpered if an interrupt is desired when an attempt is made to violate an execute-protected block. The jumpering of platform S6 is explained in section 2.5.5.

- An interrupt is issued at the level specified at platform S6. If not jumpered, the only other execute protect indicators are illumination of LED DS1 and a one latched and read at CRU bit 9.

- Note that a context switch to an interrupt service routine will halt executing the code accessed in memory. Memory cannot be deselected by an execute-protect violation as can be specified for a write-protect violation.

A block is the smallest area of memory that can be protected or unprotected. Blocks are shown in Figure 2-1.

The value read at CRU bits 4 to 7 will be the value set at those bits, reflecting the execute-protect status of each block as set through the CRU.

The following execute protects all four blocks:

```
LI   R12,>0208      SOFTWARE BASE ADDR OF CRU BIT 4
LI   R1,>0F00       BINARY 1111 IN FIRST BYTE
LDCR R1,4           APPLY ALL ONES TO CRU BITS 4-8
```

The following execute protects blocks 0 and 3:

```
LI   R12,>0200      SOFTWARE BASE ADDR OF CRU BIT 0
SBO  4              EXECUTE PROTECT BLOCK 0
SBO  6              EXECUTE PROTECT BLOCK 3
```

To check for an execute-protect violation, test CRU bit 9 as shown below:

```
LI   R12,>200       SOFTWARE BASE ADDRESS OF CRU BIT 0
TB   9              EXECUTE PROTECT VIOLATION OCCUR?
JEQ  EXECPRT        YES, ONE FOUND, JUMP TO SUBROUTINE
```

To clear the latched execute-protect indicators (these are interrupt issuance and illumination of DS1), toggle CRU bit 8 by first writing a one to unlatch the indicators and then write a zero to it to allow the latching of future write-protect indications:

```
SBO  8              UNLATCH INTERRUPT AND LED INDICATORS
SBZ  8              READY FOR NEXT PC VIOLATION
```

3.5 INTERRUPT HANDLING

Power-fail interrupts are discussed in section 3.11.

Setting up for interrupts at the microcomputer includes the following:

- Write and install the interrupt service routine for the specified interrupt level.
- Set up the interrupt vectors for the interrupt level according to the microcomputer and monitor used.
- Enable the interrupt level at the TMS 9901 on the microcomputer board.
- Enable the interrupt level at the microprocessor through the status register.

Setting up of an interrupt at the TM 990/204 board includes the following:

- Enable interrupts for write protect at CRU bits 0 to 3 depending upon the block(s) to be protected
- Enable interrutpts for execute protect at CRU bits 4 to 7 depending upon the block(s) to be protected
- Insert the desired interrupt level at platform S6.

If several TM 990/204 boards are in a system, each can be given a separate interrupt level, or one level can be used to service all boards. In the former case, an interrupt service routine is dedicated to a single board; in the latter case, a single interrupt service routine would poll the CRU bits of each board to indentify the board in violation.

The following three CRU read bits can be used in the interrupt service routine:

- Bit 8: A write-protect violation did/did not occur on this board since the time this indicator was reset and triggered via the CRU.
- Bit 9: An execute-protect violation did/did not occur on this board since the time this indicator was reset and triggered via the CRU.
- Bit 10: The board was/was not addressed since the time this indicator was reset and triggered via the CRU.

Resetting and triggering CRU indicators is described in section 3.5.3.

3.5.1 Test for Write-Protect Violation (Read CRU Bit 8)

The value at CRU bit 8 tells whether a write protect (WP) violation occurred:

- A zero read at CRU bit 8 indicates no WP violation
- A one read at CRU bit 8 indicates a WP violation

This indication remains latched until reset by toggling bit 8 by writing to it a one and then a zero (section 3.5.3).

The following code checks write-protect violation on two boards located in the CRU map adjacent to each other. The CRU software base address points to CRU bit 0.

```
TB   8              DID A WRITE-PROTECT VIOLATION OCCUR?
JEQ  ERROR1         YES, CHECK FOR VIOLATION
TB   >18            NO, CHECK NEXT BOARD
JEQ  ERROR2         YES, CHECK FOR VIOLATION
 .                  NO, CONTINUE
 .
 .
```

3.5.2 Test for Execute-Protect Violation (Read CRU Bit 9)

The value at CRU bit 9 tells whether an execute protect (EP) violation occurred:

- A zero read at CRU bit 9 indicates no EP violation
- A one read at CRU bit 9 indicates a EP violation

This indication remains latched until reset by toggling bit 8 (writing to it a one and then a zero, see section 3.5.3).

The following code checks for an execute-protect violation on two boards located in the CRU map adjacent to each other. The CRU software base address points to CRU bit zero.

```
TB   9              DID AN EXECUTE-PROTECT VIOLATION OCCUR?
JEQ  ERROR1         YES, CHECK FOR VIOLATION
TB   >19            NO, CHECK NEXT BOARD
JEQ  ERROR2         YES, CHECK FOR VIOLATION
 .                  NO,
 .
 .
```

3.5.3 Reset and Trigger Indicators

Three indicators can be read via the CRU: write protect, execute protect, and board accessed. These indicators use J-K flip-flops to latch in the indication of the occurrance. To reset these, the latch's CLR pin must be toggled; this can be done by writing to CRU bit 8 (write and execute protect reset) and 11 (board addressed reset). Note that the toggling procedure for bit 8 (set to one, then to zero) is opposite that for bit 11 (set to zero, then one) as shown in the coding examples below.

CRU Bit	Triggers
8	Write-protect and Execute-protect violation occurrance
11	Board-had-been-addressed occurrance

For example:

```
SBO  8      RESET WRITE- AND EXECUTE-PROTECT INDICATOR
SBZ  8      TRIGGER WRITE- AND EXECUTE-PROTECT INDICATOR
SBZ  11     RESET BOARD-MEMORY-ACCESSED INDICATOR
SBO  11     TRIGGER BOARD-MEMORY-ACCESSED INDICATOR
```

3.6 DELETE ALL BOARD MEMORY FROM SYSTEM (Write to CRU Bit 9)

By writing to CRU bit 9, the entire board memory can be deleted or reinserted into the system memory map. Write to this bit as follows:

- zero causes memory to be in system
- one deletes memory from system.

In other words, writing a one to CRU bit 9 prevents accessing memory on the board.

An I/O reset (pressing RESET switch on mcirocomputer board) sets this bit to the zero state.

3.7 TEST POSITION OF WRITE PROTECT SWITCH S5 (Read CRU Bit 10)

If switch S5 is set to WP, the entire board's memory is write protected no matter the setting of CRU bits. If set to NO WP, write protection is according to CRU inputs. The position of switch S5 can be checked by testing CRU bit 10 as follows:

- A zero indicates switch S5 is in the WP (write protect) position
- A one indicates switch S5 is in the NO WP (no write protect) position

The following checks if the entire board is write protected by switch S5 set to WP:

```
TB    10          SWITCH S5 WRITE PROTECTING ENTIRE BOARD?
JEQ   PROTEC      YES, BOARD IS WRITE PROTECTED
  .               NO
  .
  .
```

3.8 USER LED DS3 (Write to CRU Bit 10)

The user LED at DS3 can be lit or turned off by writing to it as follows:

- a one turns on the LED
- a zero turns off the LED

The program in section 2.8 blinks the user LED.

3.9 BOARD-ADDRESSED INDICATION BIT (Read/Write CRU Bit 11)

CRU bit 11 can be used to check if a board's memory has been accessed. This bit will be enabled by a read or a write to the memory bounds specified in the memory address switches (S1 and S2). Reading this bit is as follows:

- a one indicates the board had been accessed since the bit was set to zero.
- a zero indicates the board had not been accessed since the bit was set to zero.

To reset the bit to zero to allow sensing a change, toggle CRU bit 11 by writing a zero to it to reset values, then write a one to it to enable future changes:

```
        SBZ  11          RESET VALUES
        SBO  11          ENABLE CHANGES TO BE READ
```

One use for this bit is to use software to determine the memory bounds at each of one or more boards in the system. First, initialize all board-addressed latches by toggling them as shown above, then begin reading memory at the lowest hex address. Next, check CRU bit 11 for evidence of a change from a zero to a one, indicating the memory read caused an access of a specific board. If a board's CRU bit 11 is a one, the memory address pertains to the board that corresponds to the CRU address being used. Next, reset (if a one) the bit 11, and add a hex 1000 to the memory address (e.g., go from 0000_{16} to 1000_{16}). Make another memory read and check again. In this manner, a system memory map can be determined via software. The following code checks for memory (no extended addressing) on a TM 990/204 board having a CRU software base addresses of 0200_{16} and populated with contiguous memories.

```
*****MAIN PROGRAM TO DETERMINE MEMORY BOUNDS
        LI   R12,>0200      CRU SOFTWARE BASE ADDRESS IN R12
        CLR  R1             R1 TO MEMORY ADDRESS 0000
LOOP2   SBZ  >B             TOGGLE BOARD-ADDRESS LATCH
        SBO  >B             TOGGLE BOARD-ADDRESS LATCH
        MOV  *R1,@TEMP      READ MEMORY
        TB   >B             BOARD ADDRESSED?
        JNE  NEXT           NO, GO CHECK NEXT PAGE
        MOV  R1,@LOWER      YES, STORE LOWER BOUND ADDRESS
LOOP1   SBZ  >B             TOGGLE BOARD-ADDRESS LATCH
        SBO  >B             TOGGLE BOARD-ADDRESS LATCH
        AI   R1,>1000       INCREMENT TO NEXT HEX 1000 BOUNDRY
        MOV  *R1,@TEMP      READ MEMORY
        TB   >B             BOARD ADDRESSED?
        JEQ  LOOP1          YES, CHECK NEXT HEX 1000 BOUNDRY
        DECT R1             NO, PAST UPPER BOUND, DECREMENT BY 2
        MOV  R1,@UPPER      STORE UPPER BOUND
        JMP  EXIT           QUIT
*SUBROUTINE TO INCREMENT TO NEXT HEX 1000, CHECK FOR RETURN TO HEX 0000
NEXT    AI   R1,>1000       R1 POINTS TO NEXT HEX 1000 BOUNDRY
        JNE  LOOP2          IF NOT HEX 0000, TEST NEXT BOUNDRY
        CLR  @UPPER         IF 0000, CLEAR BOTH BOUNDS TO SHOW--
        CLR  @LOWER             THAT NO MEMORIES FOUND
EXIT     .
         .
         .
```

3.10 FOUR FLAG BITS (Read/Write CRU Bits 12 to 15)

CRU bits 12 to 15 are user defined. The value written to these bits will be the value read. Note, that an I/O reset will set these bits to all zeroes.

3.11 POWER-FAIL INTERRUPT

When power is restored following a power failure, it is important that the system know the configuration when execution was interrupted. Interrupt one (signal INT1.B-) can be used for power-fail interrupts. This interrupt line is accessible via the backpanel terminal strip on the TM 990/510(A), TM 990/520(A), and TM 990/530 card cages. To activate the interrupt at a power fail, an external power-fail sensing circuitry, such as on the power supply, would bring INT1.B- low in relation to system ground. Execution of the interrupt would result in program return vectors (Workspace Pointer, Program Counter, and Status Register contents of interrupted program) to be in registers 13, 14, and 15 of the interrupt service routine workspace. Part of the interrupt service routine's tasks would be to store these values in a dedicated area of the battery-protected TM 990/204 memory; this could be facilitated by locating the workspace of the interrupt service routine in battery-protected memory.

The power-fail interrupt service routine would be executed via the interrupt one vectors (memory locations 0004_{16} and 0006_{16} as explained in your microcomputer user's guide). Prior to the interrupt, the user program must have enabled the interrupt at the microcomputer board's TMS 9901 interface (at the TMS 9901 CRU address, SBZ 0 to enter interrupt mode, SBO 1 to enable interrupt 1) and at the microprocessor Status Register interrupt mask (LIMI 1).

SECTION 4

THEORY OF OPERATION

4.1 GENERAL

This section describes the theory of operation for the TM 990/204 memory board. Figure 4-1 is a block diagram of the board. This section is divided into the following subjects:

- Connector P1 and Buffering (4.2)
- Board Address Decoding (4.3)
- Memory Organization and Enabling (4.4)
- CRU Programmable Devices (4.5)
- Interrupts (4.6)
- Battery Backup (4.7)
- Memory Timing Circuitry (4.8)

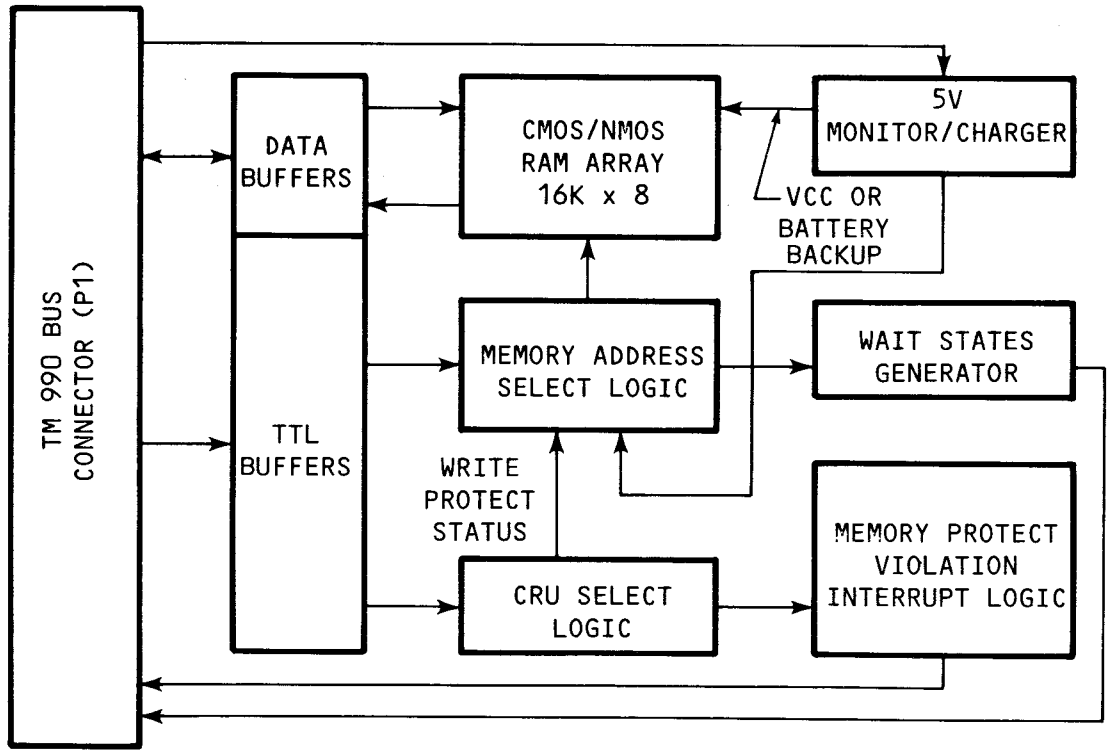


FIGURE 4-1. TM 990/204 MEMORY BOARD BLOCK DIAGRAM

4.2 CONNECTOR P1 AND BUFFERING

Connector P1 is a 100-pin connector which interfaces the TM 990/204 to the system backplane. Data lines are routed through two 74LS245 bi-directional buffers at U13 and U14 while address and control signals are routed through three 74LS241 uni-directional line drivers. These are shown in sheet 2 of the schematics (Appendix A).

The data-line buffers are enabled by the signal DATABUFFEN- from a D flip-flop at U7 as shown below in Figure 4-2. The flip-flop is clocked by MEMCYC- and cleared at each BUSCLK- during a memory cycle.

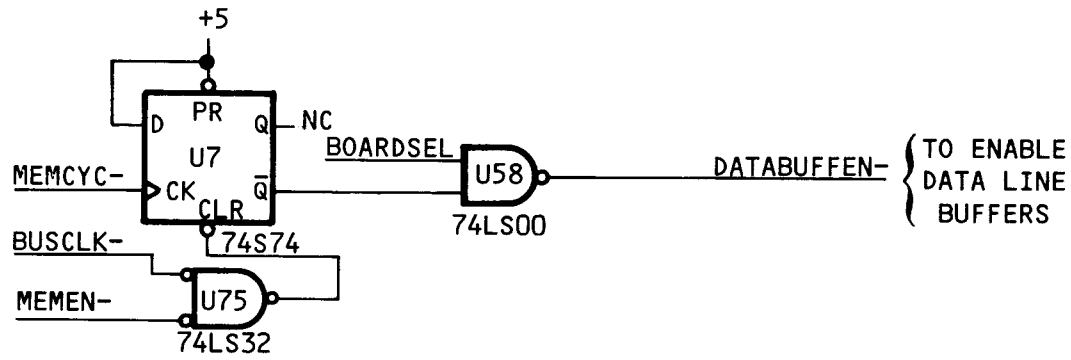


FIGURE 4-2. DATA BUFFER ENABLE CIRCUITRY

The address line and data line buffers at U13, U14, U9, U16, and U15 as shown in sheet 2 of the schematics have noninverted tri-state outputs. The 74LS240 control signal buffer at U3 inverts two control signals (CRUCLK.B- for CRU clock and IAQ.B for determining when an instruction is being accessed from memory); two other signals (CRUOUT.B and IORST.B-) are inverted at this inverter then re-inverted so that the end result is true.

Appendic C lists bus signals at P1 used by the TM 990/204.

4.3 BOARD MEMORY ADDRESS DECODING

Only incoming memory addresses within the address line bounds selected at switch platforms S1 and S2 will enable the onboard memory. The setting of these switch platforms are compared to address lines XA0 to A3 as explained in section 2.5.1 and Table 2-2. The comparison of these switches and address bus values is one of four inputs that enable the 74S260 positive

NOR gate at U20 (see center of Figure 4-3). An all-low input to this NOR gate brings high the gate output BOARDSEL which allows onboard memory selection. These four inputs to U20 are the following:

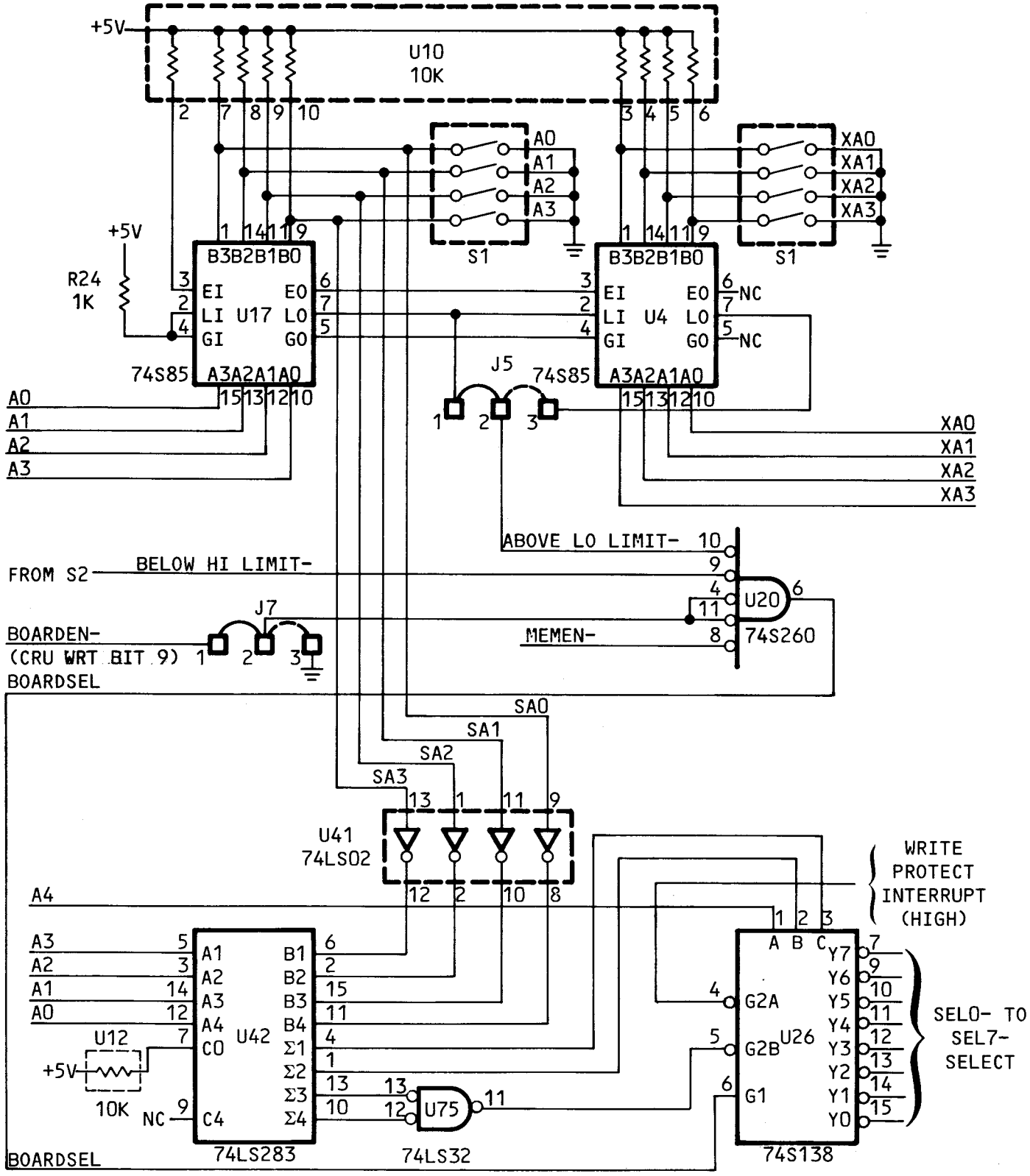
- Address line value is equal to or greater than the switch S1 setting (ABOVELOLIMIT- active).
- Address line value is equal to or less than the switch S2 setting (BELOWHILIMIT- active)
- Address lines contain a memory address (MEMEN- active)
- Jumper J7 set 2-3 (ground applied to U20); or set 2-1 with CRU bit 9 low so that BOARDEN- is active from CRU bit multiplexer at U73.

The lines of the address bus selected at S1 will be the four- (no extended addressing) or eight-MSBs (extended addressing) of the board's lower memory address bounds. Figure 4-3 shows the memory selection hardware for switch platform S1; switch platform S2 works in a similar manner. The 74S85 comparators at U4 and U17 are ganged together to compare switch-platform S1 values with address lines XA0 to XA3 (extended address lines) and A0 to A3. If only address lines A0 to A3 are to be compared (no extended addressing) then jumper J5 is set 2-1 to receive the negative (not-low) indicator from the LO output of comparator U17 to convey an enabling low to the NOR gate at U20; otherwise, the LO output of U4 is used with jumper J5 set 2-3 (extended addressing). In this latter case, the LO outputs of U17 and U4 are ganged together with a negative LO output from U4 indicating the address is not lower than the S1 settings.

The lines of the address bus selected at S2 will be the four- or eight-MSBs of the board's upper memory address bound. The 74S85 comparators at U5 and U18 are ganged together to compare switch values similar to U4 and U17 as specified in the paragraph above. In this case, a not-greater-than indicator from the 74S85 shows that the address line value is not above (but can be equal to) the S2 switch settings.

BOARDSEL enables the 74S138 3-to-8 line decoder at U26. The 74S138 selects one of the eight 2048-byte memory half-blocks. For battery backup purposes, memory is divided into four 4096 by 8 blocks (BLK0 to BLK3).

The lower memory address bound always begins on a multiple of 1000_{16} with each of the eight half blocks containing 0800_{16} bytes; thus a fully populated board could contain memory in four 1000_{16} boundaries (boundaries being a multiple of 1000_{16}). The lower memory address bound is designated at switches S1 and S2 by comparison to address lines A0, A1, A2, and A3 as well as the extended address lines. The S1 switch settings for A0 to A3 (SA0 to SA3) are subtracted from the actual values on A0 to A3 using the 74LS283 adder at U42. This will always allow the lower memory address bound to be pointed to the beginning of block BLK0.



NOTE: Only switch S1 shown; switch S2 schematic is similar

FIGURE 4-3. MEMORY ADDRESS SELECTION SCHEMATIC

4.4 MEMORY ORGANIZATION AND ENABLING

Memory is organized into four blocks of 4096 bytes each as shown in Figure 4-4. Battery backup can be selected for each block by jumpers J1 to J4, setting them to 2-3. Jumpering these 2-1 deselects battery backup for the block. These jumpers allow selecting only CMOS RAM for battery backup when CMOS and NMOS RAM are mixed on the board.

Jumper	Battery Backup Select	Battery Backup Deselect	Block
J1	2-3	2-1	BLK0
J2	2-3	2-1	BLK1
J3	2-3	2-1	BLK2
J4	2-3	2-1	BLK3

The smallest area of memory that can be populated is a block of 4096 bytes of RAM. These four-block areas are shown in Figure 4-4. Note that battery backup is selectable on a block basis.

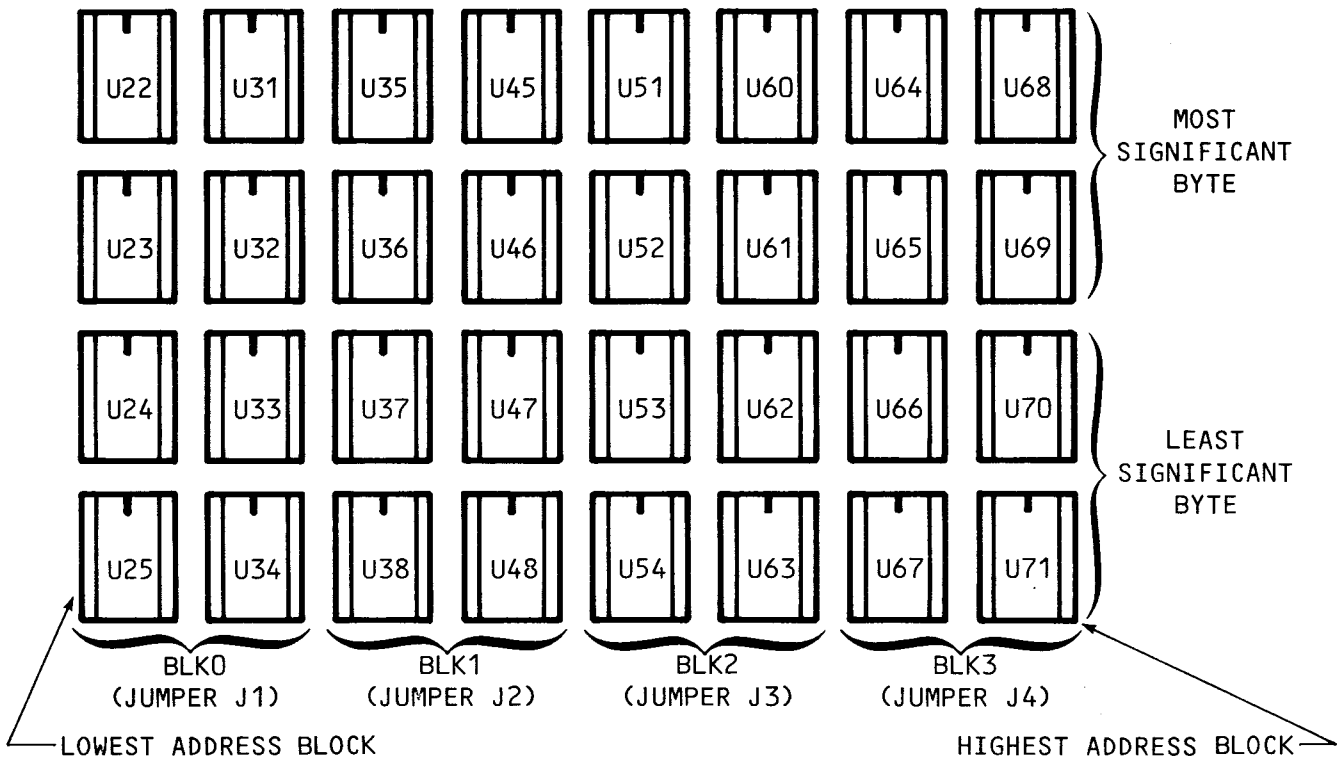


FIGURE 4-4. MEMORY PLACEMENT BY BLOCK

4.5 CRU PROGRAMMABLE DEVICES

The CRU address is selected at switch S3 as explained in section 2.5.2 and Table 2-3. Ganged 74LS85 comparators at U6 and U19 compare the eight MSBs (A3 to A10) of the CRU address (on the address bus) selected at S3. An equal comparison enables one of the four NAND gates at U43 and U58 as shown in Figure 4-5. In turn, these NAND gates (output active low) enable 74LS251 multiplexers for CRU read operations (explained in section 4.5.1) or enable 74LS259 latches for CRU write operations (explained in section 4.5.2).

Enablng the NAND gates are:

- For CRU read operations:
  - Equal indication from 74LS85 comparators at U6 and U19 of values on address bus and switch S3
  - Address-line A11 low for lower 8 CRU bits; address line A11 high for upper 8 CRU bits
- For CRU write operations:
  - Equal indication from 74LS85 comparators at U6 and U19 of values on address bus and switch S3
  - CRUCLK active
  - Address line A11 low for lower 8 CRU bits; address line A11 high for upper 8 CRU bits

4.5.1 CRU Read Operations

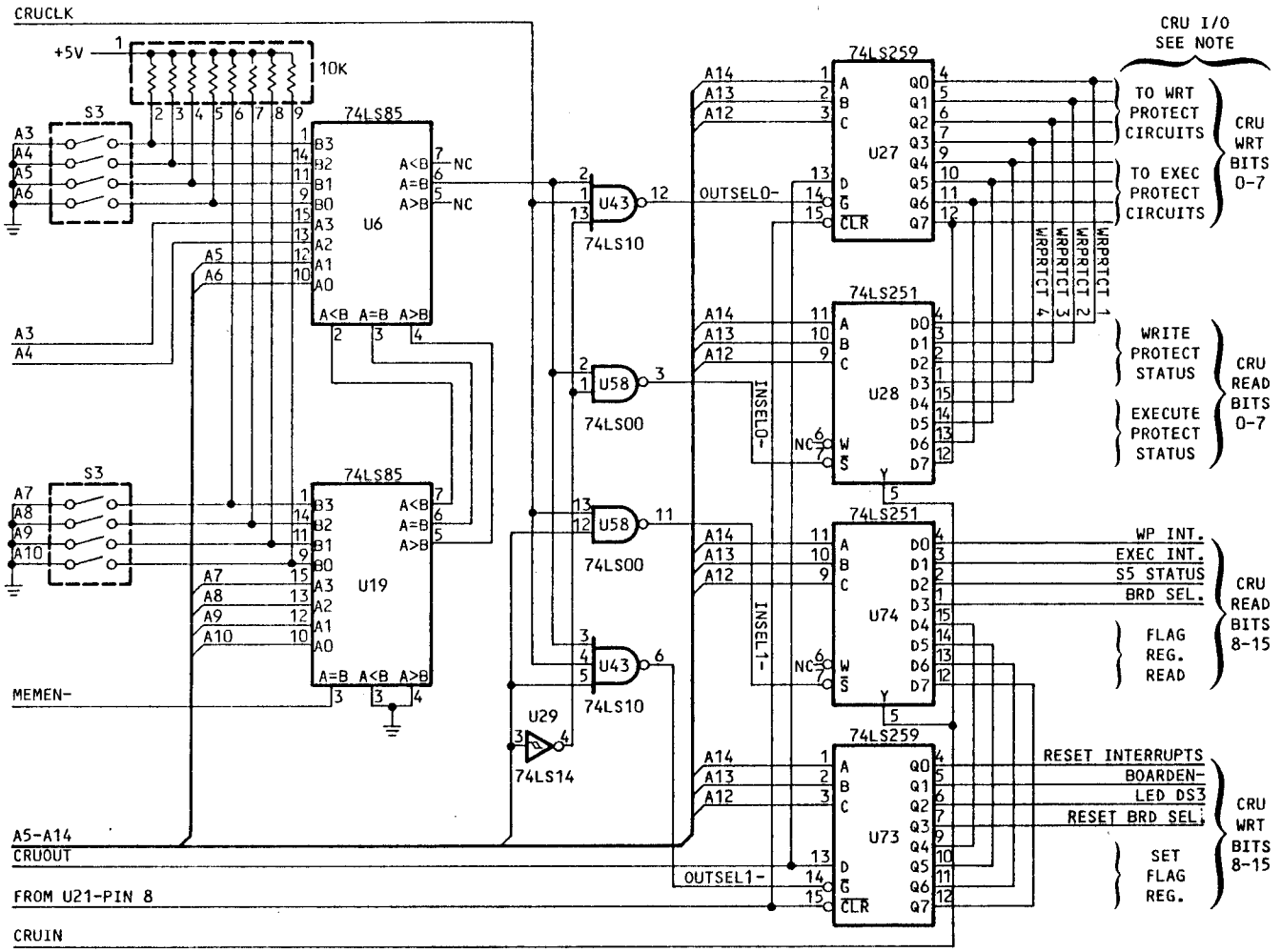
Two 74LS251 multiplexers at U28 and U74 are addressed by A12, A13, and A14 with the Y output going to the CRUIN line for reading the multiplexer's inputs D0-D7. See Figure 4-5. These inputs, as read through the CRU, are:

- CRU bits 0 to 7 as read at U28:
  - Bits 0 to 3 are the write protect status set through the CRU for BLK0 to BLK3 as read from the outputs of the CRU write latch at U27
  - Bits 4 to 7 are the execute protect status set through the CRU for BLK0 to BLK3 as read from the outputs of the CRU write latch at U27
- CRU bits 8 to 15 as read at U74:
  - Bits 8 to 11 show status (write and execute protect violations from the J-K flip-flop latches at U59, switch S5 setting, and board-addressed indicator value latched at the J-K flip-flop at U30).
  - Bits 12 to 15 are the values of the flag bits as read from the CRU write latch at U73.

4.5.2 CRU Write Operations

Two 74LS259 latches at U27 and U73 are addressed by address lines A12, A13, and A14 with the D input coming from the CRUOUT line. The outputs Q0 to Q7 of these latches write to CRU bits:

- U27 channels digital levels to CRU bits 0 to 7 (see Figure 4-6):
  - Bits 0 to 3 select/deselect write protect for BLK0 to BLK3. These bits drive the U57 EXCLUSIVE OR gates which drive the 1C0 to 1C3 inputs of the 74LS153 multiplexer at U56. The other input to U57 EXCLUSIVE OR gates decides whether a one or a zero from the U27 latch causes write protect; this input is a one or a zero selected by jumper J8.



NOTE: CRU bit functions are defined in detail in Section 3 and Table 3-1.

FIGURE 4-5. CRU SELECT CIRCUITRY

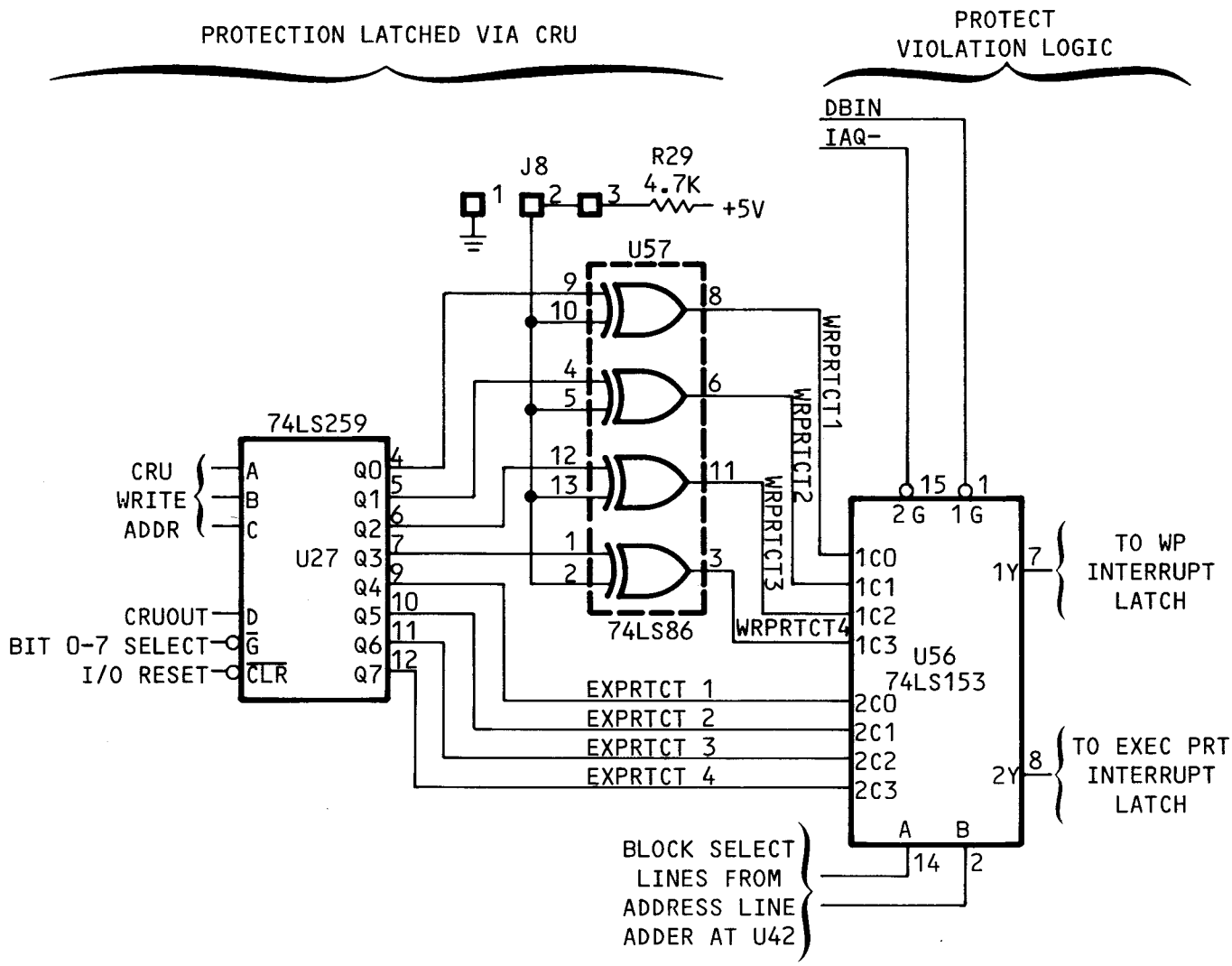


FIGURE 4-6. WRITE-PROTECT AND EXECUTE-PROTECT ENABLING

The inputs from these U57 gates go to the 1C0 to 1C3 inputs of the multiplexer at U56. These four inputs are the write protect status for BLK0 to BLK3 respectively. When the U56 multiplexer is enabled by DBIN low (write cycle), address inputs A and B select the block (1Cx input). If a one is at the 1Cx input, a one at the 1Y output goes to a J-K flip-flop where it is latched to drive the interrupt circuitry. See Figure 4-7.

- Bits 4 to 7 are similar to 0 to 3 above except they are for execute protect of BLK0 to BLK3 and can enable by a one only. The Q4 to Q7 outputs of U27 go directly to the 2C0 to 2C3 inputs of U56 which correspond to execute-protect status for BLK0 to BLK3 respectively. When the U56 multiplexer is strobed by IAQ- (indicating that an instruction is being retrieved from memory) from the multiprocessor, address inputs A and B indicate the memory block being accessed. See Figure 4-6. If a one is at the 2Cx input (enable execute protect for BLKx), a one goes to the J-K flop-flop at U59 which drives the interrupt circuitry. A zero to U59 would not cause an interrupt.

If jumper J10 is set 2-1 and a write-protect violation occurs, memory will be deselected by the writing of a one from the U56 multiplexer Y1 output to the G2A- chip enable (active low) of the memory-block select decoder at U26.

- U73 channels digital levels to CRU bits 8 to 15:

  - Bit 8, if a zero, clears the two 74LS109 J-K flip-flops (U59) whose latched Q outputs reflect a write-protect or execute-protect violation. This is shown at the top of Figure 4-7. These Q outputs can be read at CRU bits 8 and 9 to check for violations. Resetting these flip-flops will turn off the write- and execute-protect violation LEDs by bringing high the output of the inverters at U29-8 and -12 which go to the ground side of the LEDs. Clearing these flip-flops will also unlatch the interrupt request to OR gate U43. After being cleared, toggle this bit by writing a one to it; this will enable the flip-flop to make a later state change should a violation occur.

  - Bit 9, if a one, deselects all memory from the memory board by writing a one to the five-input NAND gate U20 (Figure 4-3) which then brings BOARDSEL low to disable the memory-block-select decoder at the 74S138 at U26. A zero level at bit 9 enables selecting board memory. Jumper J7 must be set 1-2 for this bit to work.

  - Bit 10, if a one, lights the user LED at DS3. The one is inverted by the 74LS04 inverter at U29 to complete the low side circuit from the LED. A zero level at bit 10 turns off the LED.

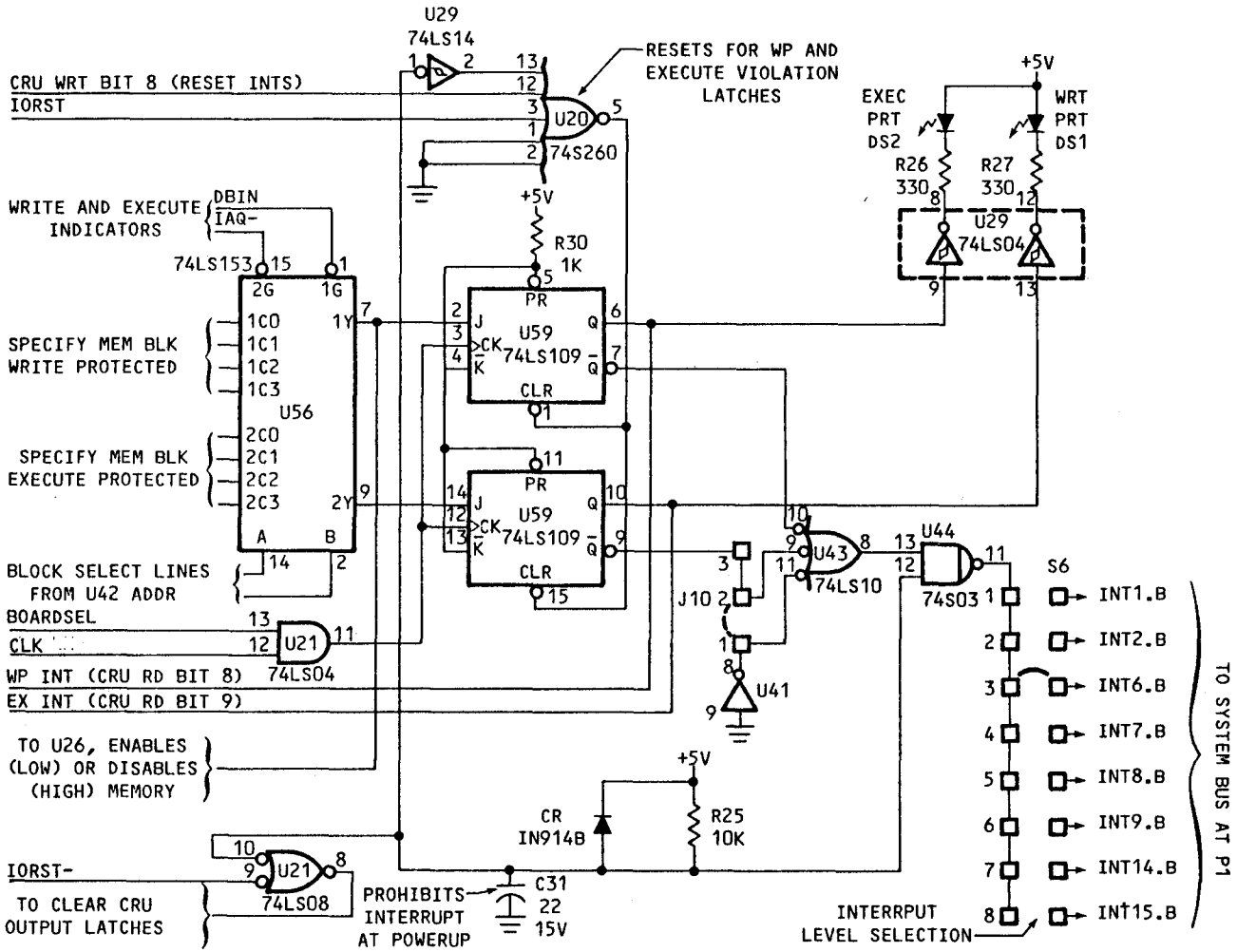


FIGURE 4-7. INTERRPUT LOGIC

- Bit 11, if a zero, clears the 74S109 J-K flip-flop at U30. The flip-flop's Q output is latched to a one if the board memory has been selected; clearing the flip-flop sets this output (which can be read at CRU bit 11) to a zero. Setting this bit back to a one allows the flip-flop to change state if another board access is made (and thus this change can be checked by reading CRU bit 11).

- Bits 12 to 15 serve as the flag registers. Data is latched at the 74LS259 addressable latch at U73. Data input can be read at the same CRU address.

4.6 INTERRUPTS

The interrupt circuitry is shown in Figure 4-7. Interrupts can be caused by an attempt to write to a part of memory that has been designated as write-protected or by trying to retrieve an instruction from a part of memory that has been designated as execute protected. Memory protection can be designated via the CRU as explained in sections 3.4.1 and 3.4.2.

Interrupt conditions are checked according to DBIN and IAQ-, both shown in the top left of Figure 4-7. When a memory write cycle is initiated by the CPU, DBIN activates the memory write protect area of the multiplexer at U56. The block select input lines A and B to the multiplexer select the write-protect CRU bit at 1C0 to 1C3 which reflects the write-protect status of each block as selected. The output at 1Y is latched at a J-K flip-flop on U59. If an interrupt is requested, the Q- output supplies the enabling low output to the three-input NAND gate at U43 (other NAND gate inputs are the execute-protect interrupt and a one from an inverter at U41). The high output from this NAND gate enables the two-input NAND gate at U44 (one side held high by Vcc) with its active-low output going to the active-low interrupt outputs; this is routed to the desired interrupt level via jumper platform S6.

Execute protection is handled in a similar manner. The second half of the multiplexer at U56 is enabled by IAQ- (when enabled, an instruction opcode is being accessed from memory). The block select lines A and B to the multiplexer select the execute-protect CRU input bits at 2C0 to 2C3 which reflects the execute protect status as selected. The output at 2Y selects or deselects an execute protect interrupt via a second J-K flip-flop at U59 with the Q- output supplying the enabling low output to the three-input NAND gate at U43. The output at U43 and the routing through NAND gate U44 and interrupt selection at switch platform S6 is the same as for write-protect interrupts as explained above.

Write protection is designated through the CRU and through switch and jumper settings as described in paragraph 3.3.1. Execute protection is designated through the CRU only. Both of these conditions can be checked by reading CRU bits, with the bits also indicating the memory block in which the violation was attemped or occurred. Switch platform S6 selects the interrupt level desired; if all platform settings are open, no interrupt will be issued even though jumpers and CRU bits are correctly set.

The four memory banks are designated as write protected and/or execute protected by the setting of CRU bits 0 to 3 and 4 to 7 respectively at the 74LS259 addressable latch at U27.

4.7 BATTERY BACKUP

Memory chip Vcc comes from either board Vcc only or from Vcc backed up by the board battery depending upon jumpers J1 to J4 (blocks BLK0 to BLK3 respectively) as shown below:

Source of Memory Vcc	J1 to J4 Setting
• Board Vcc only	2-1
• Board Vcc until powerfail, then from board battery	2-3

In the following paragraphs, it is assmumed that battery backup has been selected.

4.7.1 Memory Chip Select Circuitry

Figure 4-8 shows the circuitry that isolates the memory-block-select circuitry at U26 (shown at bottom of Figure 4-3) from the memory chips depending upon the status of Vcc. As long as Vcc is above the threshold at approximately 4.75 V, the block select signals from U26 (SEL0- to SEL7-) are routed to the select lines (CS-) of the memory chips. The NAND gate at U2 outputs a low (POWERGOOD-) signal, indicating Vcc is within tolerance, as long as high logic values are received from both the power-source switching circuitry (high = battery not being used) and the Vcc-level comparator cicuitry (high = board Vcc okay). The POWERGOOD- low value prevents the fast-switching VMOS power transistor from turning on and grounding the bases of the eight transistors at U40 and U55. Thus the bases are held high through pullup resistors at U39 and U50 and maintain a chip select circuitry between SEL0- to SEL7- (from U26 as shown in Figure 4-3) and the CS- inputs to the memory chips. Values to the chip select pins are held high by pullup resistors at U49 and U72 unless a block is enabled by a low from U26.

4.7.2 Power Fail Circuitry

The bottom (right side) of Figure 4-9 shows the circuitry to detect a power failure condition. The LM393 fine-tuned comparator at U1 compares divided-down voltages from Vcc and from the Zener diode IN4370A at CR1. Fine tuning is through the trim resistor at R5. The threshold is set such that the comparator will change state at or above the approximate minimum operating voltage for TTL logic, 4.75 V. While Vcc is within tolerance, the non-inverting input to the comparator is higher than the inverting input. This results in a high output to the NAND gate at U2; likewise, the other input to U2 is held high from the battery backup switch circuitry shown at the top of Figure 4-9 and described in section 4.7.3. The result is a low (POWERGOOD-) to the VMOS fast-switching power transistor at Q3 as explained in 4.7.1 above.

When Vcc drops below the threshold voltage (approximately 4.75 V), the inverting input to the U1 comparator becomes larger, and a zero is output. With a low comparator output, the POWERGOOD-signal goes high and becomes invalid, the Q3 transistor conducts causing the bases of the eight transistors at U40 and U55 to go low (shown in Figure 4-8). This turns off the SEL0- to SEL7- chip select values from U26.

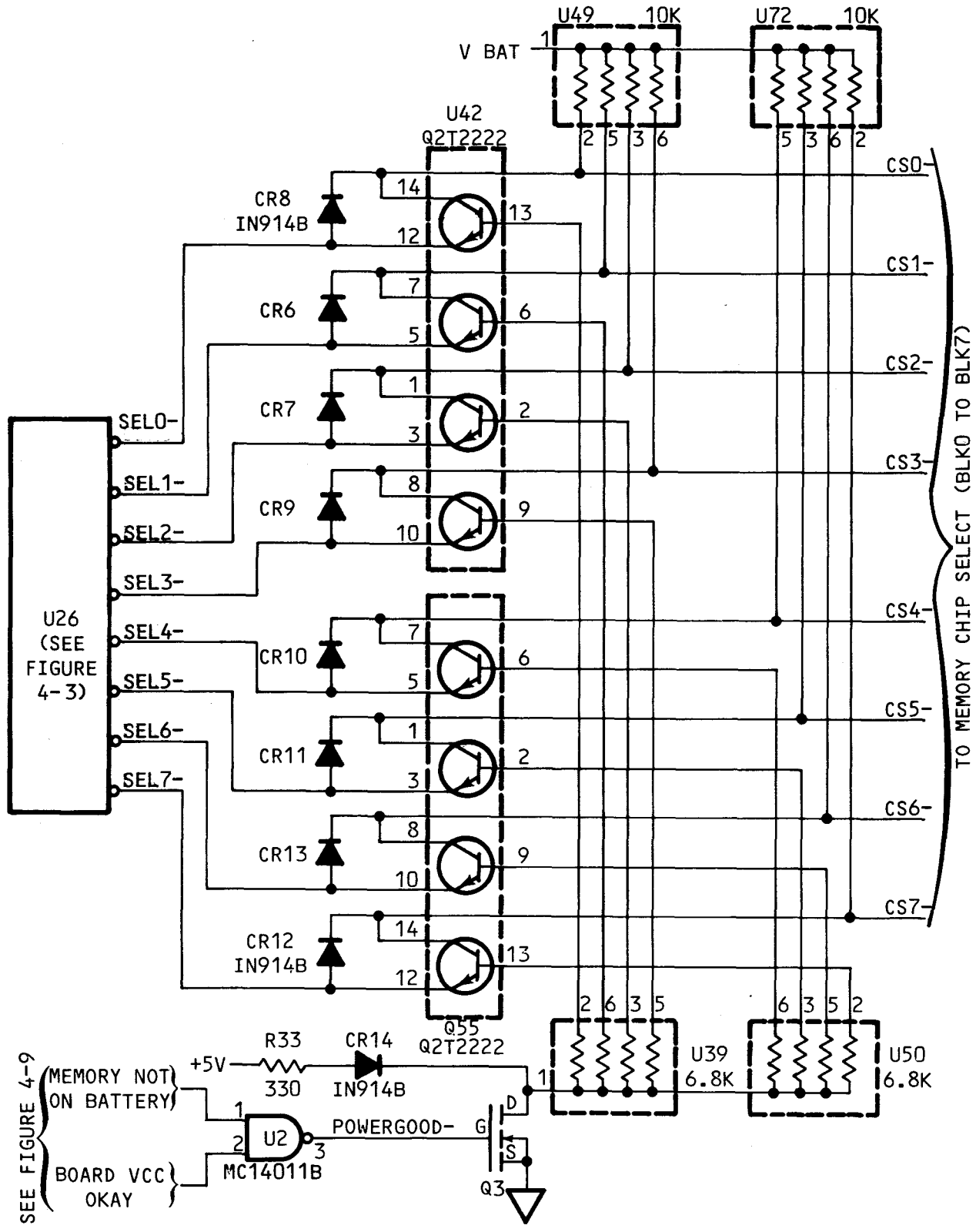


FIGURE 4-8. MEMORY CHIP ENABLE/DISABLE CIRCUITRY

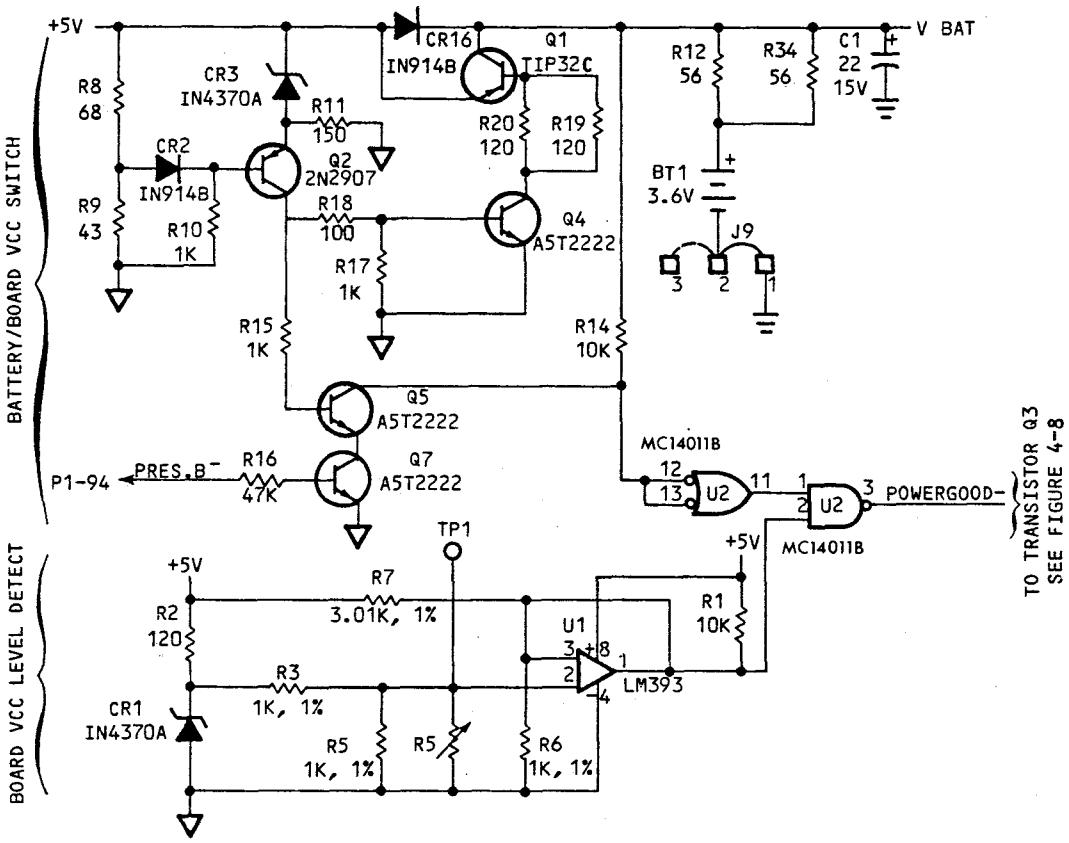


FIGURE 4-9. SWITCHING CIRCUITRY FOR MEMORY VCC SOURCE

4.7.3 Battery/Board Vcc Voltage Select

Memory chips receive memory Vcc from the battery backup circuitry only when the respective memory block is jumpered for battery backup at jumpers J1 to J4 as described in section 4.7. When so jumpered, voltage is normally provided by board Vcc through battery-backup line VBAT while the battery is kept on a trickle charge at the same time. When voltage becomes unstable, memory Vcc is switched from board Vcc to the battery backup voltage through VBAT.

The top (left side) of Figure 4-9 shows the circuitry to switch battery Vcc to either board Vcc or board battery. As long as board Vcc remains stable, the A5T2907 transistor at Q2 conducts, providing high base inputs to transistors Q4 and Q5 as shown at the top of Figure 4-9. Should board Vcc drop, transistor Q2 stops conducting and turns off transistors Q4 and Q5 to begin switching memory to battery backup.

When conducting, the A5T2222 transistor at Q5 provides a low level to NOR gate U2 which, in turn, provides a high to NAND gate U2 to maintain POWREGOOD- to transistor Q3. This allows normal memory chip select as explained in section 4.7.1. When turned off, Q5 causes POWERGOOD- to go high, turning on Q3 which causes the transistors at U40 and U55 to turn off and deselect all memory chips (Q3 is shown in Figure 4-6).

When the A5T2222 transistor at Q4 conducts, it turns on the TIB32C transistor at Q1; thus, providing a path for board Vcc to the VBAT source that goes to memory chip Vcc. Transistor Q1 conducting also provides a constant charge to the battery through resistor R12. As long as Q1 is conducting, board Vcc will go to the memory Vcc and battery. When Q1 is turned off, battery current goes to VBAT via diode IN4002 at CR4.

4.8 MEMORY TIMING CIRCUITRY

Wait states can be inserted into memory timing circuitry as explained in section 2.5.3 and in Table 2-4. This table lists the different wait states according to the setting of switch platform S4.

Figure 4-10 shows the wait state circuitry. A four-bit counter at U8 receives an initial binary count setting to input pins A to D from switch platform S4 (pin A being the LSB and D being the MSB) when the board is not being accessed. At the start of a memory cycle, the counter is placed in the count mode as soon as the board is accessed, indicated by BOARDSEL being active. The initial value is incremented by one at every leading edge of the BUSCLK-. When it reaches a total of 15, a one carry value will then be placed on pin RCO (ripple carry out). The RCO output goes to a J-K flip-flop at U30 which causes the binary value from S4 to be reloaded into the counter.

In addition to causing the counter to be reloaded, the output at RCO is ANDed to BOARDSEL (board selected) and output as READY.B, the bus signal specifying that memory is available for a read or write. In essence, the countup is the amount of delay before telling the microprocessor that memory is ready. Figure 4-11 shows timing for a read cycle and write cycle with one wait state.

The counter is clocked by BUSCLK-, the system clock. Thus the amount of the delay introduced will be a multiple of system clock speed used (e.g., with a 3 MHz clock, each delay will be 333 nanoseconds).

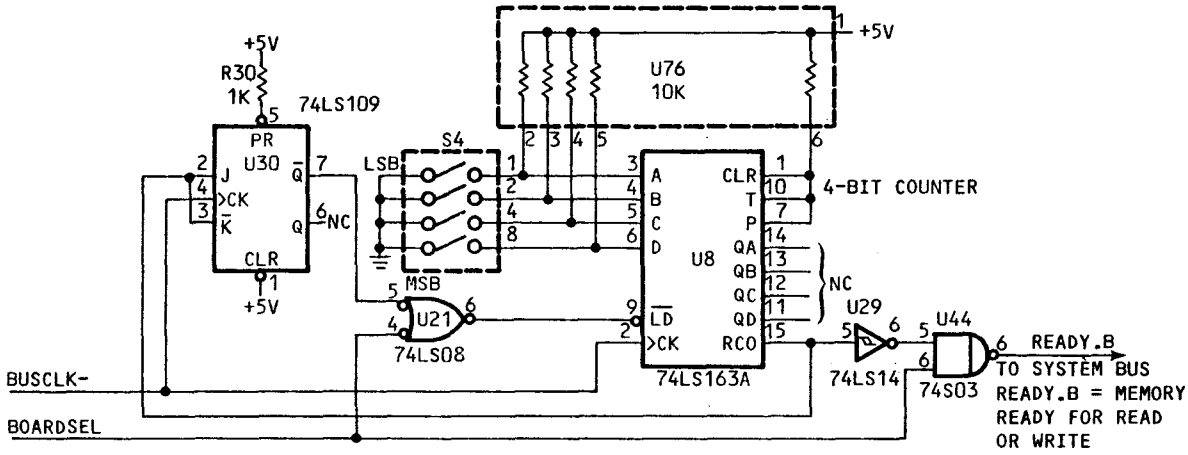
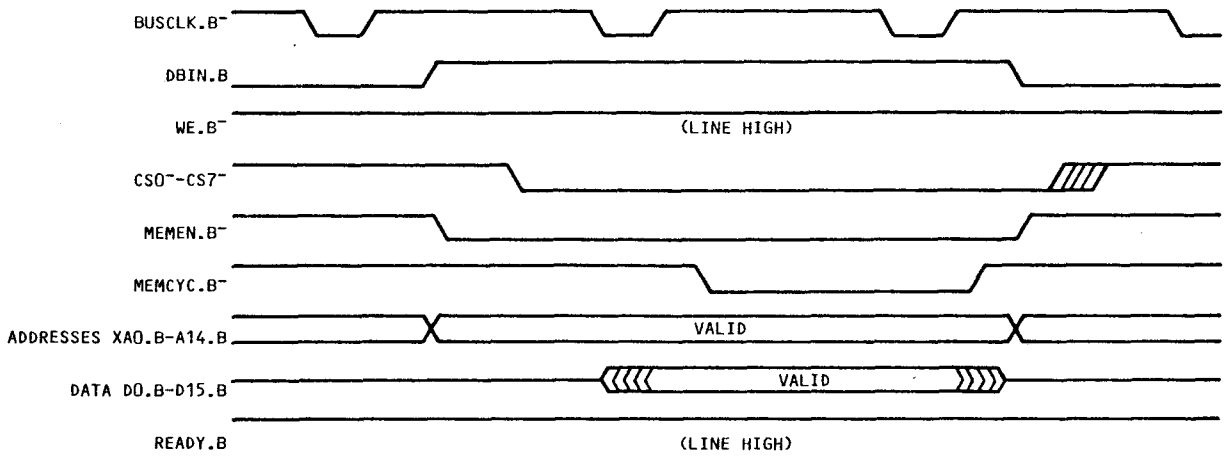
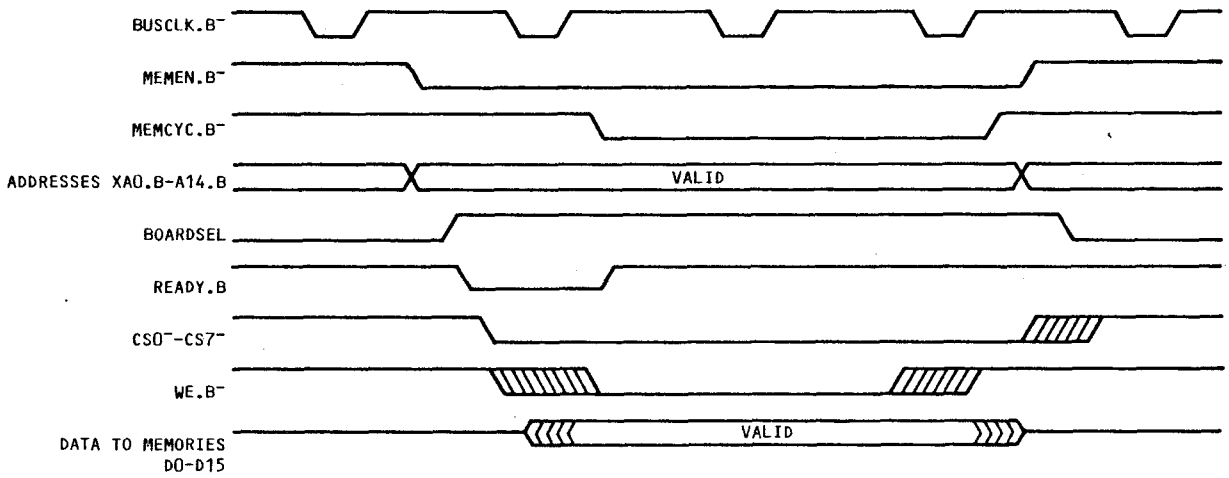


FIGURE 4-10. WAIT STATE INSERTION CIRCUITRY



(a) READ CYCLE (NO WAIT STATE)



(b) WRITE CYCLE (WITH ONE WAIT STATE)

FIGURE 4-11. TM 990/204 MEMORY TIMING

APPENDIX A

SCHEMATICS

NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE .25W, 5%
2. ALL RESISTANCE VALUES ARE IN OHMS
3. ALL CAPACITANCE VALUES ARE IN MICROFARADS
4. DEVICE U2 PIN 7 IS GND & PIN 14 IS VBAT
5. VALUE TO BE ADDED @ TEST
6. (UNITRODE) DEVICE UFT004N OR (SUPERTEX) VN1304N3 DEVICE ACCEPTABLE ALTERNATES
7. RESISTOR "R8" VALUE IS SELECTED AT UNIT TEST ; RESISTOR TO BE 1/4 W, 5 %
8. J10 IS A USER'S OPTION
9. CMOS RAMS ARE POPULATED AT:

   TM 990/204-1 ASSY (U22-U25, U31-U34)
   TM 990/204-2 ASSY (U22-U25, U31-U38, U45-U48)
   TM 990/204-3 ASSY (U22-U25, U31-U38, U45-U48, U51-U54, U60-U71)

10. SEE JUMPER CONFIGURATION CHART FOR JUMPER SETTING FOR J1 THRU J4

JUMPER	LOCATION		
	-0001	-0002	-0003
J1	2,3	2,3	2,3
J2	2,1	2,3	2,3
J3	2,1	2,1	2,3
J4	2,1	2,1	2,3
J5	2,1	2,1	2,1
J6	2,1	2,1	2,1
J7	2,1	2,1	2,1
J8	2,1	2,1	2,1
J9	2,3	2,3	2,3
J10	NOT USED	NOT USED	NOT USED

REFERENCE DESIGNATORS	
USED	NOT USED
C1 - C49	
DS1 - DS3	
J1 - J10	
R1 - R34	
S1 - S6	
U1 - U75	
Q1 - Q3	
CR1-CR3, CR5-CR16	CR4
P1	
BT1	

1600201 REV 1

REVISIONS

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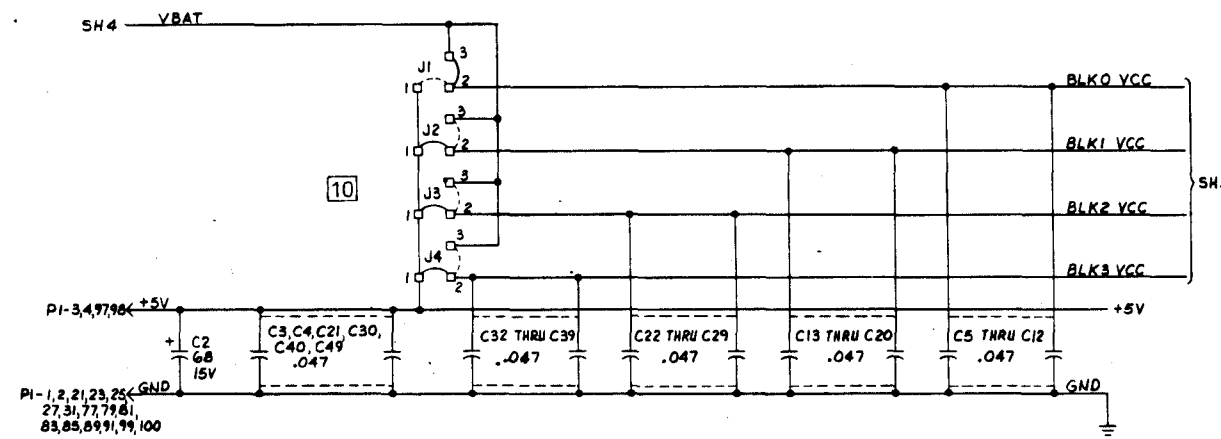
B	CN458995	5/27/81	



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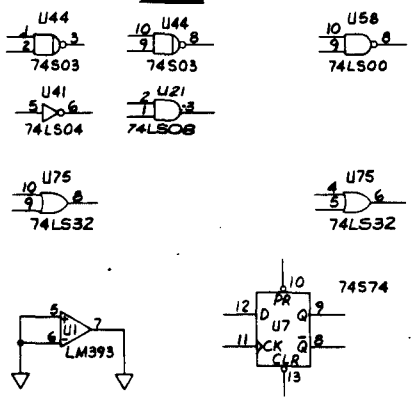

P1-96 GRANT OUT.B-

P1-95 GRANT IN.B-

SEQ NO	IDENT	F.SPEC	NO	ADDITIONAL
	PROCESS		CLASSIFICATION	NOTES

PROCESS — FOR CONFORMANCE TO QUALITY AND SPECIFICATIONS, SEE TI DRAWING 730467

ITEM NO	QTY	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED:
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±1°; 3 PLACE DECIMALS ± .010; 2 PLACE DECIMALS ± .02
- INTERPRET DRAWING PER MIL-D-1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONSISTENTLY MACHINED DIAMETERS ARE FOR DIMENSIONAL LIMITS ONLY BEFORE PROCESSING
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.XX ± .005	.XXX ± .003	.XXXX ± .0005
.XXX ± .003	.XXXX ± .0005	.XXXXX ± .0003
.XXXX ± .0005	.XXXXX ± .0003	.XXXXXX ± .0002

1600202 | 8117
NEXT ASSY | USED ON
APPLICATION

DRAWN 8-7-80
CHECKED 8/14/81
ENGR 8/14/81
PROJ ENGR 8/16/81

TEXAS INSTRUMENTS INCORPORATED Dallas, Texas

DIAGRAM, LOGIC
TM990/204

SIZE D | 96214 | 1600201
SCALE NONE | SHEET 1 OF 5

A-2

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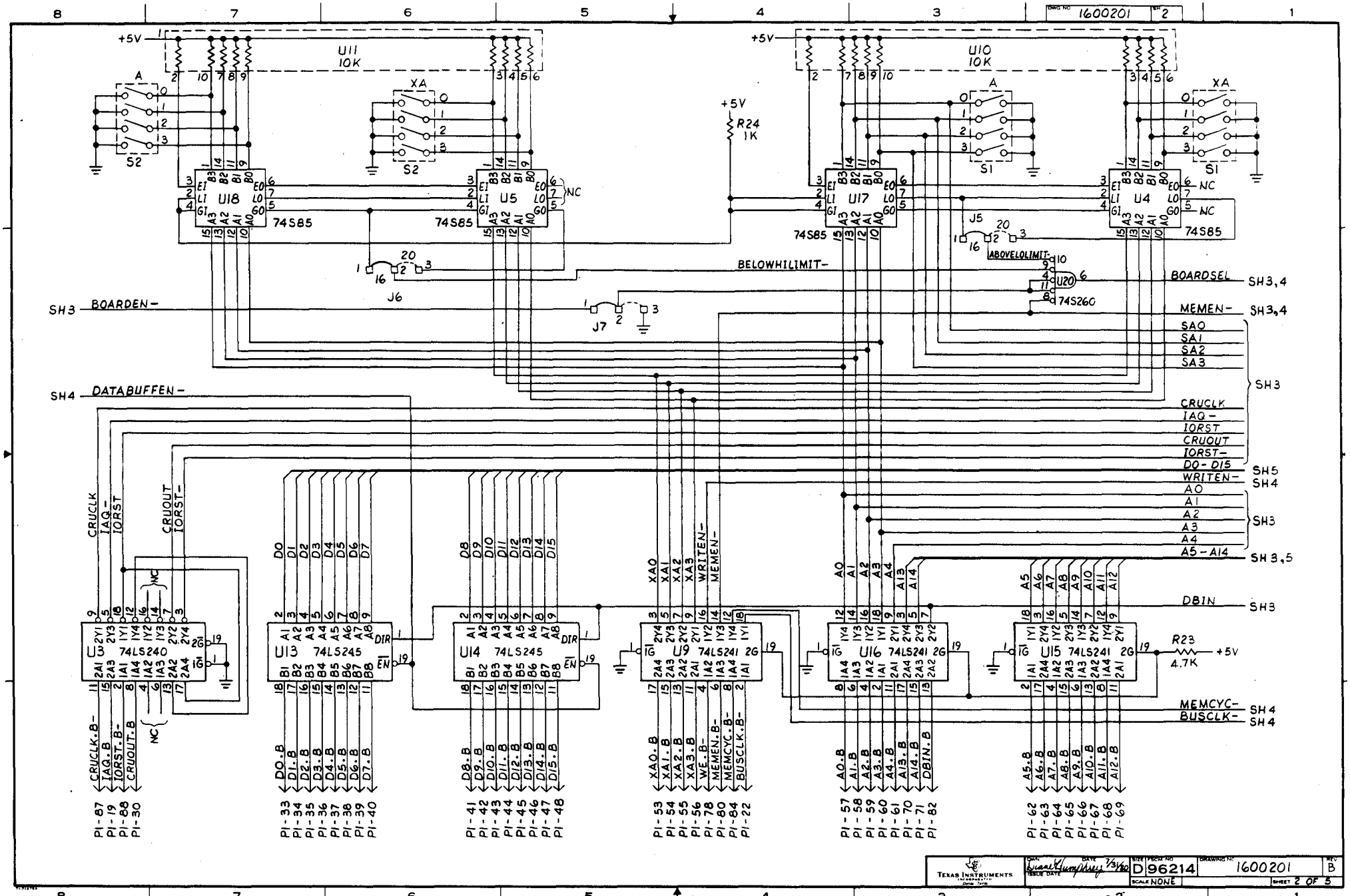
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S1
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U4 74S85
NC
J5
J6
J7
ABOVELOLIMIT-
BELOWHILIMIT-
U20 74S260
BOARDSEL SH3,4
SH3 BOARDEN-
MEMEN- SH3,4
SA0
SA1
SA2
SA3
SH3
SH4 DATABUFFEN-
CRUCLK
IAQ-
IORST
CRUOUT
IORST-
DO-D15 SH5
WRITEN- SH4
A0
A1
A2
A3
A4
SH3
A5-A14 SH3,5
DBIN SH3
U3 74LS240
U13 74LS245
U14 74LS245
U9 74LS241 2G
U16 74LS241 2G
U15 74LS241 2G
R23 4.7K
MEMCYC- SH4
BUSCLK- SH4
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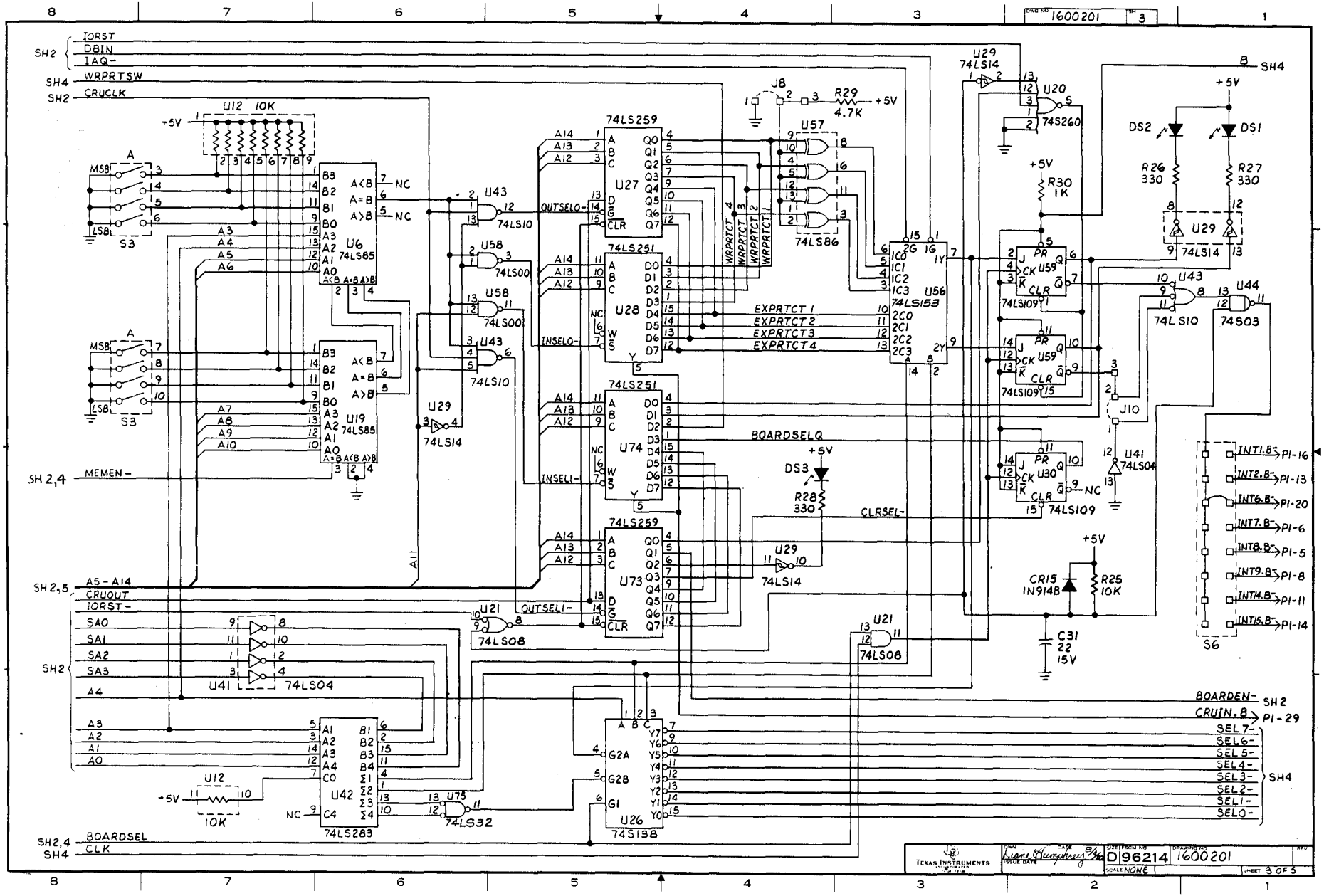
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MEMEN-
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CLRSEL-
INSELO-
INSEL1-
OUTSELO-
OUTSEL1-
EXPRTCT1
EXPRTCT2
EXPRTCT3
EXPRTCT4
BOARDEN-
CRUIN.8
SEL7-
SEL6-
SEL5-
SEL4-
SEL3-
SEL2-
SEL1-
SEL0-
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INT2.8-
INT6.8-
INT7.8-
INT8.8-
INT9.8-
INT4.8-
INT5.8-
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U19 74LS85
U42 74LS283
U26 74S138
U27 74LS259
U28 74LS251
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U56 74LS153
U57 74LS86
U59 74LS109
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U20 74S260
U41 74LS04
U21 74LS08
U75 74LS32
U43 74LS10
U58 74LS00
U44 74S03
U29 74LS14
U12 10K
J8
J10
S3
S6
R29 4.7K
R30 1K
R25 10K
R26 330
R27 330
R28 330
C31 22 15V
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DS2
DS3
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1600201
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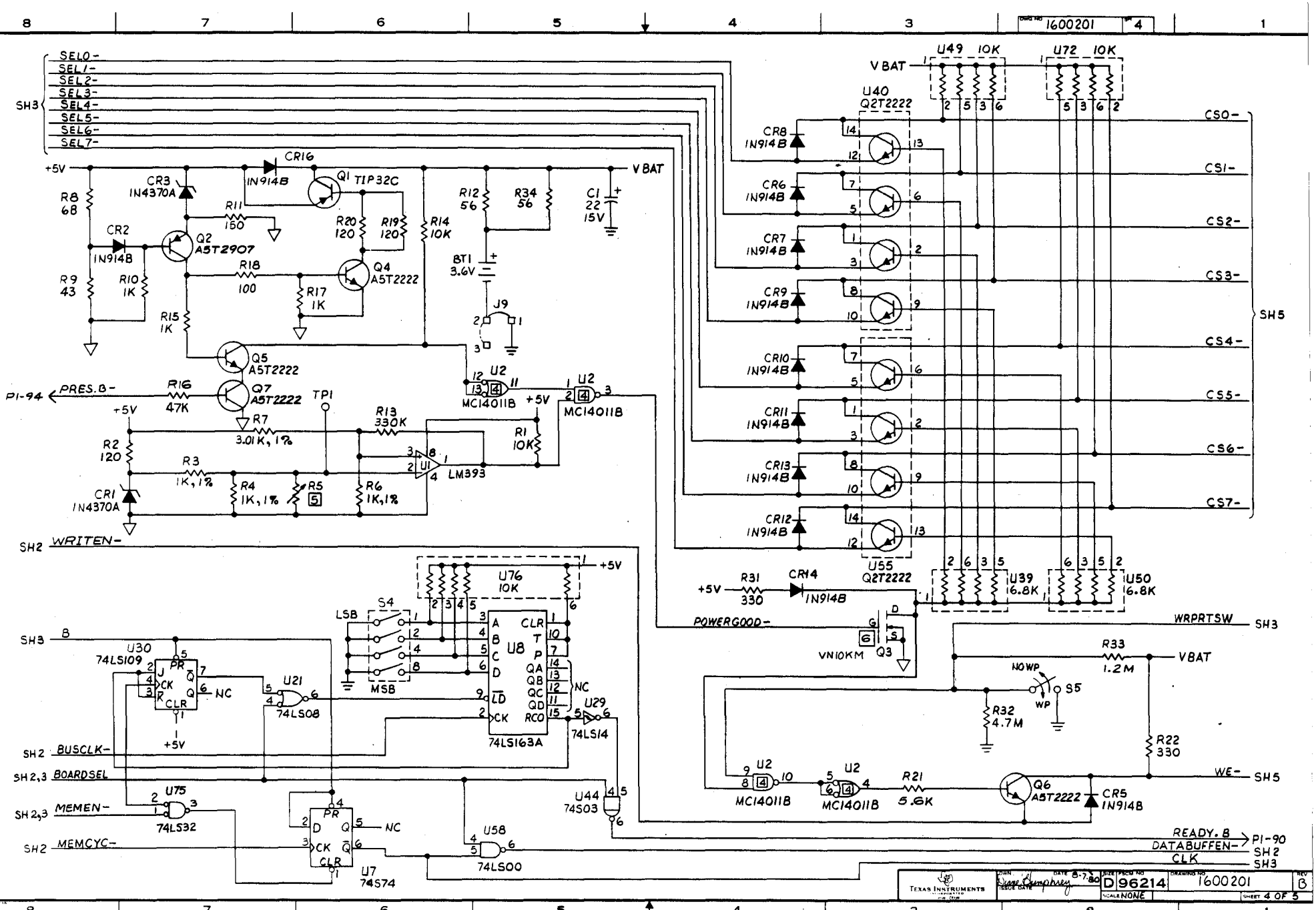
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SEL1-
SEL2-
SEL3-
SEL4-
SEL5-
SEL6-
SEL7-
+5V
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CR3
IN4370A
Q1
TIP32C
R8
68
R11
150
R20
120
R19
120
R14
10K
R12
56
R34
56
C1
22
15V
CR2
IN914B
Q2
A5T2907
R18
100
Q4
A5T2222
R9
43
R10
1K
R17
1K
BT1
3.6V
J9
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1K
Q5
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R13
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R1
10K
R2
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R5
R6
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CS5-
CS6-
CS7-
SH5
U55
Q2T2222
U39
6.8K
U50
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R32
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MSB
U8
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U30
74LS109
U21
74LS08
U29
74LS14
SH3
B
SH2
BUSCLK-
SH2,3
BOARDSEL
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74LS32
SH2,3
MEMEN-
SH2
MEMCYC-
U7
74S74
U58
74LS00
U44
74S03
MC14011B
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CR5
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SH3
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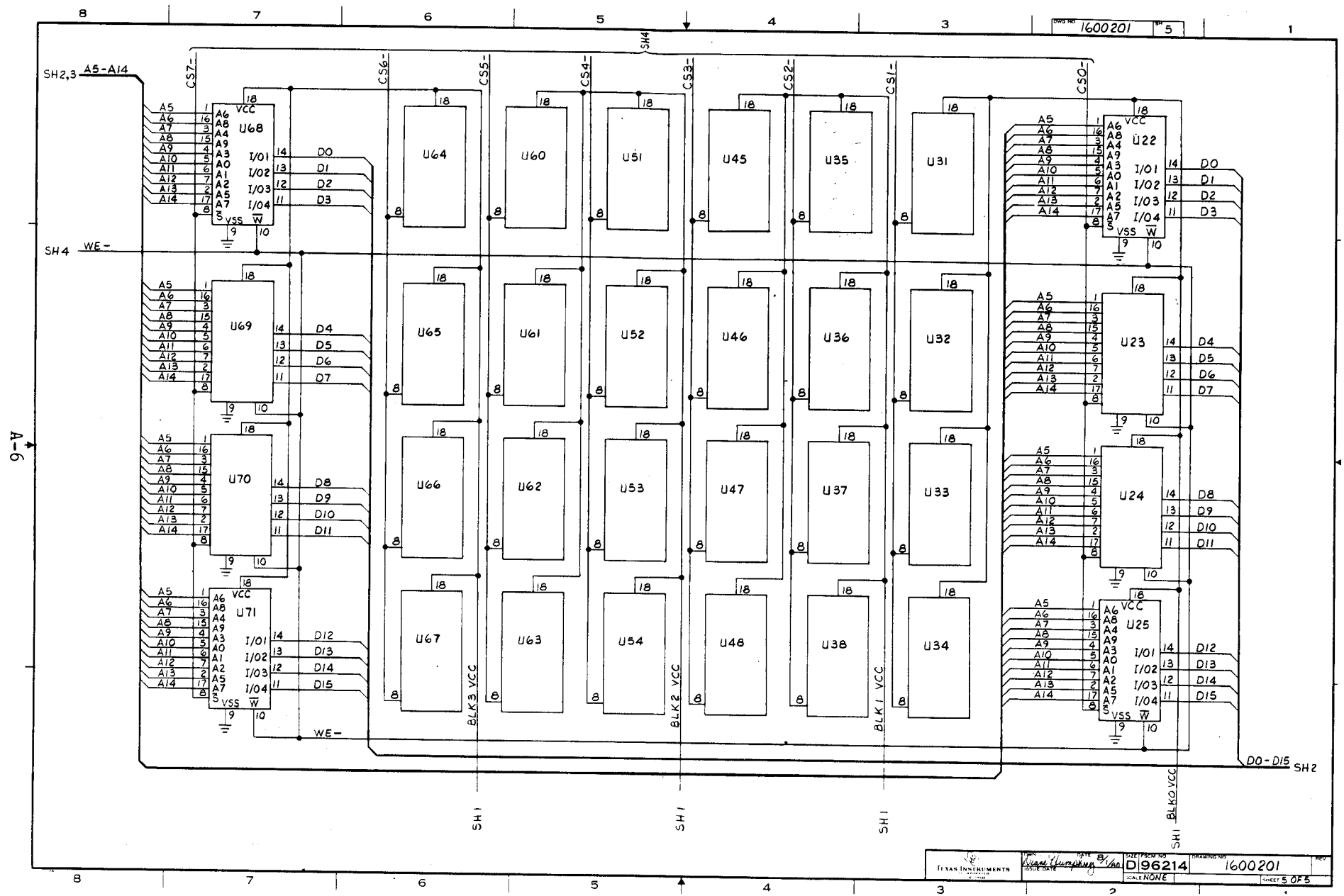
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U69
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U71
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U23
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D4
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D14
D15
BLK3 VCC
BLK2 VCC
BLK1 VCC
BLK0 VCC
D0-D15 SH2
SH1
A-6
TEXAS INSTRUMENTS
D96214
1600201
SCALE NONE
SHEET 5 OF 5

APPENDIX B

PARTS LIST

SYMBOL	DESCRIPTION	QTY
BT1	Battery, nickel cadium, 3.6 V	1
C1, C31	Capacitor, 22 uFd, 10%, 15 V	2
C2	Capacitor, 68 uFd, 10%, 15 V	1
C3-C30, C32-C49	Capacitor, 0,047 uFd, +80%, -20%	46
CR1, CR3	Diode, 1N4370A, 2.4 V, 5%, volt reg	2
CR2, CR5-CR16	Diode, 1N914B	13
DS1-DS3	LED, red, rt angle	3
J1-J9	Jumper plugs Available from: Berg Electronics, Inc. Rt. 3 New Cumberland, Pa. 17070 Part Number 65474-005	9
Q1	Transistor, TIP32C, PWR-AMP, HI-SPEED SWITCH, PNP	1
Q2	Transistor, A5T2907, PNP, silicon	1
Q3	Transistor, PWR, MOSFET	1
Q4, Q5, Q6, Q7	Transistor, A5T2222, NPN, silicon	4
R1, R14, R25	Resistor, 10K ohm, 5%, 0.25 W	3
R2, R19, R20	Resistor, 120 ohm, 5%, 0.25 W	3
R3, R4, R6	Resistor, 1.00 k ohm, 1%, 0.25 W	3
R7	Resistor, 3.01 k ohm, 1%, 0.25 W	1
R8	Resistor, 68 ohm, 5%, 0.25 W	1
R9	Resistor, 43 ohm, 5%, 0.25 W	1
R10, R15, R17, R24, R30	Resistor, 1.0 k ohm, 5%, 0.25 W	5
R11	Resistor, 150 ohm, 5%, 0.25 W	1
R12, R34	Resistor, 56.0 ohm, 5%, 0.25 W	2
R13	Resistor, 330 k ohm, 5%, 0.25 W	1
R16	Resistor, 47 k ohm, 5%, 0.25 W	1
R18	Resistor, 100 ohm, 5%, 0.25 W	1
R21	Resistor, 5.6K ohms, 0.25 W, 5%	1
R22, R26-R28, R31	Resistor, 330 ohm, 5%, 0.25 W	5
R23, R29	Resistor, 4.7K ohm, 5%, 0.25 W	2
R32	Resistor, Fixed, 4.7 M ohms, 5%, 0.25 W	1
R33	Resistor, 1.2 M ohm, 5%, 0.25 W	1
S5	Switch, toggle, 2 position	1

SYMBOL	DESCRIPTION	QTY
U1	Network, LM393	1
U2	IC, MC14011, CMOS NAND gate	1
U3	IC, SN74LS240N, Line drivers	1
U4, U5, U17, U18	Network, SN74S85N	4
U6, U19	Network, SN74LS85N	2
U7	Network, SN74S74N	1
U8	Network, SN74LS163A	1
U9, U15, U16	IC, SN74LS241N, Line drivers	3
U10-U12	Resistor, 10K ohms, 1.25W, 2%, 10 pins	3
U13, U14	IC, SN74LS245N, BUS XCVR Transition	2
U20	Network, SN74S260N	1
U21	Network, SN74LS08N	1
U22-U25, U31-U34	IC, CMOS, RAM, 6514, 1024 x 4	8
U26	Network, SN74S138N	1
U27, U73	IC, SN74LS259N	2
U28, U74	Network, SN74LS251N	2
U29	Network, SN74LS14N	1
U30, U59	Network, SN74LS109N	2
U39, U50	Resistor Network, 6800 ohms, 2%, 0.75W, 6 pins	2
U40, U55	Transistor, MPQ2222/SQ1062, QUAD	2
U57	Network, SN74LS86N	1
U41	Network, SN74LS04N	1
U42	Network, SN74LS283N	1
U43	Network, SN74LS10N	1
U44	Network, SN74S03N	1
U49, U72, U76	Resistor Network, 10K ohm, 2%, 6 pins	3
U56	Network, SN74LS153N	2
U57	Network, SN74LS86N	1
U58	Network, SN74LS00N	1
U75	Network, SN74LS32N	1

APPENDIX C

BUS SIGNALS TO TM 990/204 MODULE AT CONNECTOR P1

Pin at P1	Signal	Pin at P1	Signal	Pin at P1	Signal
-5	INT8.B-	-41	D8.B	-64	A7.B
-6	INT7.B-	-42	D9.B	-65	A8.B
-8	INT9.B-	-43	D10.B	-66	A9.B
-11	INT14.B-	-44	D11.B	-67	A10.B
-13	INT2.B-	-45	D12.B	-68	A11.B
-14	INT15.B-	-46	D13.B	-69	A12.B
-16	INT1.B-	-47	D14.B	-70	A13.B
-19	IAQ.B	-48	D15.B	-71	A14.B
-20	INT6.B-	-53	XA0.B	-80	MEMEN.B-
-22	BUSCLK.B-	-54	XA1.B	-82	DBIN.B
-29	CRUIN.B	-55	XA2.B	-84	MEMCYC.B-
-30	CRUOUT.B	-56	XA3.B	-87	CRUCLK.B-
-33	D0.B	-57	A0.B	-88	IORST.B-
-34	D1.B	-58	A1.B	-90	READY.B
-35	D2.B	-59	A2.B	-94	PRES.B-
-36	D3.B	-60	A3.B		
-37	D4.B	-61	A4.B		
-38	D5.B	-62	A5.B		
-39	D6.B	-63	A6.B		
-40	D7.B				

GROUND: -3, -4, -97, -98

+5 V: -1, -2, -21, -23, -25, -27, -31, -77, -79, -81, -83, -85, -89, -91, -99, -100

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