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TEXAS INSTRUMENTS

# TM 990

## TM 990/311
## Buffered I/O Module

MICROPROCESSOR SERIES™

User's Guide

PRINTING REVISION

This printing incorporates the following revision level:

| Date | Revision Change (From - to) | ECN Number |
|---|---|---|
| 06/03/81 | * to A | 456475 |

## IMPORTANT NOTICES

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

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# SECTION 1

# INTRODUCTION

## 1.1 GENERAL

The TM 990/311 is an input/output module designed for use with a TM 990 CPU module. The module has 48 I/O bits. These bits are organized into 8 bit blocks. Each block is programmable as input or output. Two blocks (of 8 bits each) make up a port. Each port has its own unique switch-selectable CRU base address. There are three ports, each port occupying one of the three edge connectors.

Other features of the TM 990/311 are as follows:

- Software compatible with I/O and reset features of the TM 990/310 I/O module.
- Blocks programmed as outputs can be read (echoed) with a CRU input instruction.
- Output drivers can be exchanged to provide non-inverting or inverting outputs.
- User option of series, pull-up or pull-down resistors on outputs.
- +12 V, -12 V, +8 V, and +5 V are available (at the user's option) at each port's edge connector.

Module dimensions are shown in Figure 1-1. Principal components of the TM 990/311 are shown in Figure 1-2. A block diagram is given in Figure 1-3.

## 1.2 SPECIFICATIONS

- Power Requirements:
  Without +8 V regulator: +5 V, ±3 %, .65 A (typical), 1.8 A (maximum)
  With 8 V Regulator driving 3 fully
  loaded 5 MT I/O module racks: +12 V, ± 5%, 1.2 A (typ.), 2.0 A (max.)
- Temperature Requirements:
  Operation Temperature:..0°C to 70°C
  Storage Temperature:....-65°C to 150°C
- Physical Characteristics:
  Width: 28 cm. (11 inches)
  Height: 19 cm. (7.5 inches)
  Thickness: 0.16 cm. (0.062 inch)
  Component height: 12.7 mm (0.50 inch) maximum
- Programmed Inputs:
  High-level input voltage: 2.0 V minimum
  Low-level input voltage: 0.8 V maximum
  Allowed voltage range: 0.0 V to 7.0 V
  Input current (with no pull-up resistors): 20 uA at 2.7 V

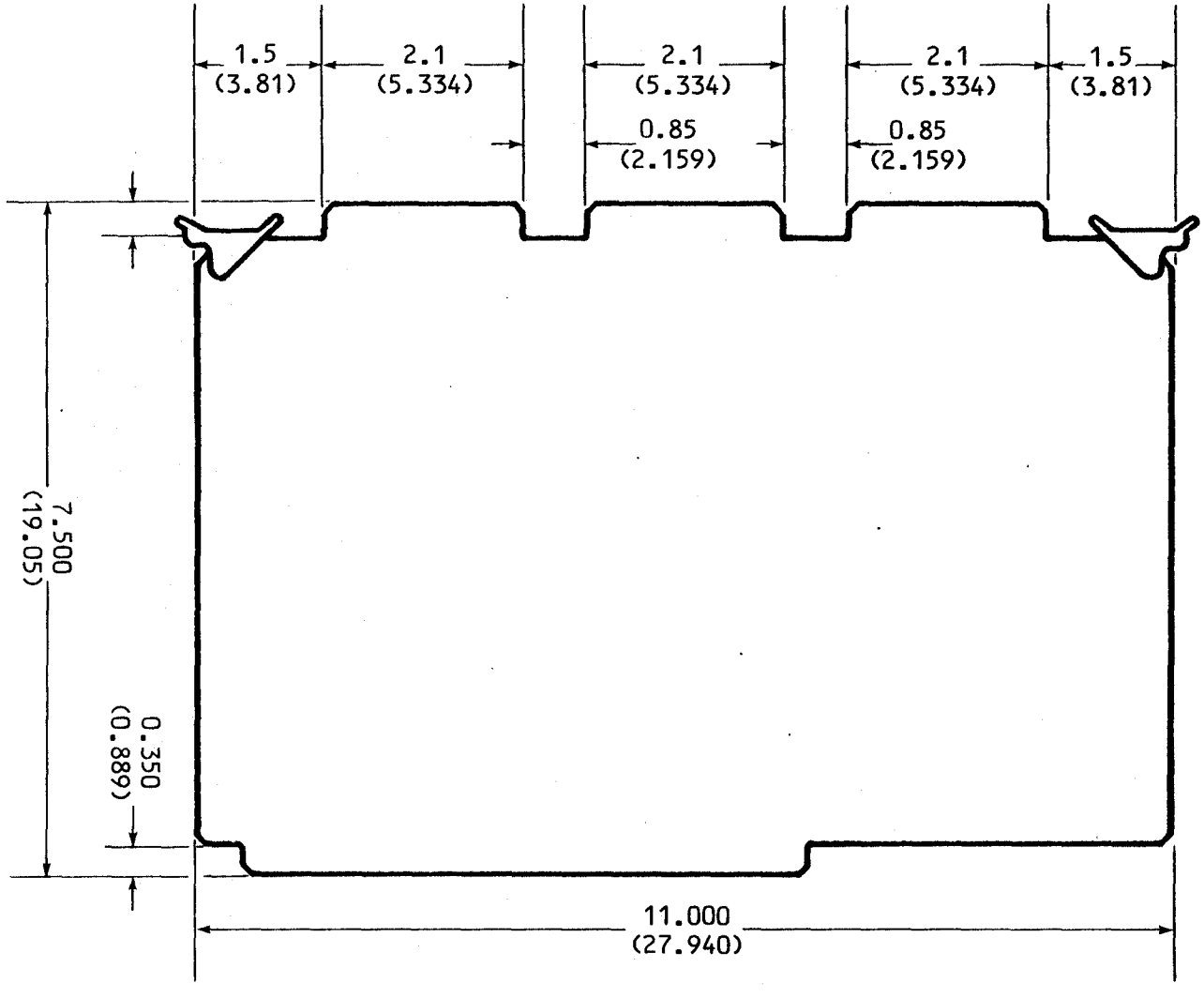
- Programmed Outputs:
  High-level output voltage: 2.4 V minimum @ 15 mA maximum

  Low-level output voltage : 0.50 V maximum @ 24 mA

  Maximum user current sink: 24 mA

## 1.3 Applicable Documents

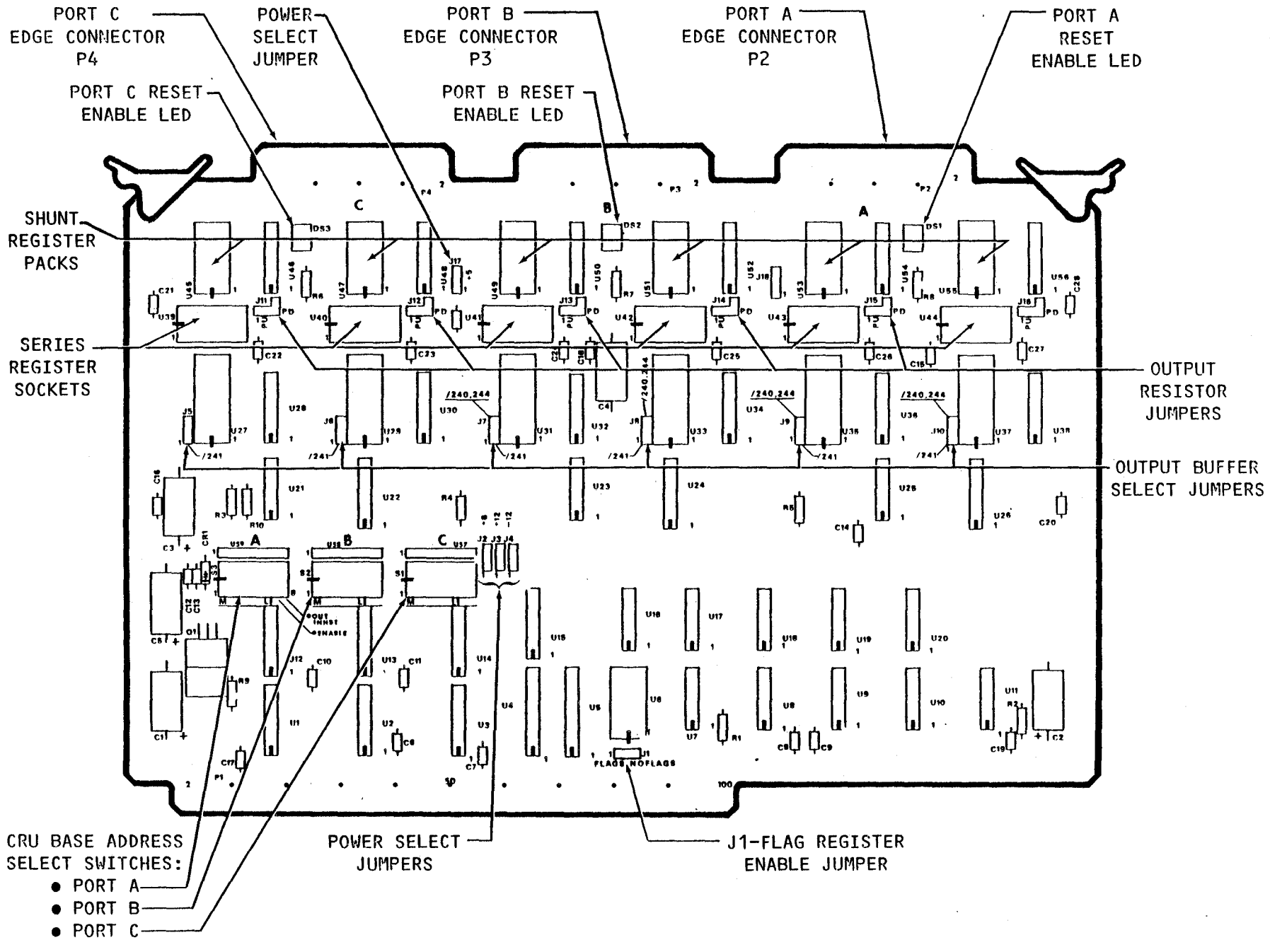
- TMS 9900 Microprocessor Data Manual
- TMS 990/401 TIBUG Monitor Listing
- TM 990 CPU User's Manual




NOTE:

Dimensions in inches (top numbers) and in centimeters (in parenthesis).

FIGURE 1-1. TM 990/311 MODULE DIMENSIONS


PORT C
EDGE CONNECTOR
P4
POWER
SELECT
JUMPER
PORT B
EDGE CONNECTOR
P3
PORT A
EDGE CONNECTOR
P2
PORT A
RESET
ENABLE LED
PORT C RESET
ENABLE LED
PORT B RESET
ENABLE LED
SHUNT
REGISTER
PACKS
SERIES
REGISTER
SOCKETS
OUTPUT
RESISTOR
JUMPERS
OUTPUT BUFFER
SELECT JUMPERS
CRU BASE ADDRESS
SELECT SWITCHES:
• PORT A
• PORT B
• PORT C
POWER SELECT
JUMPERS
J1-FLAG REGISTER
ENABLE JUMPER

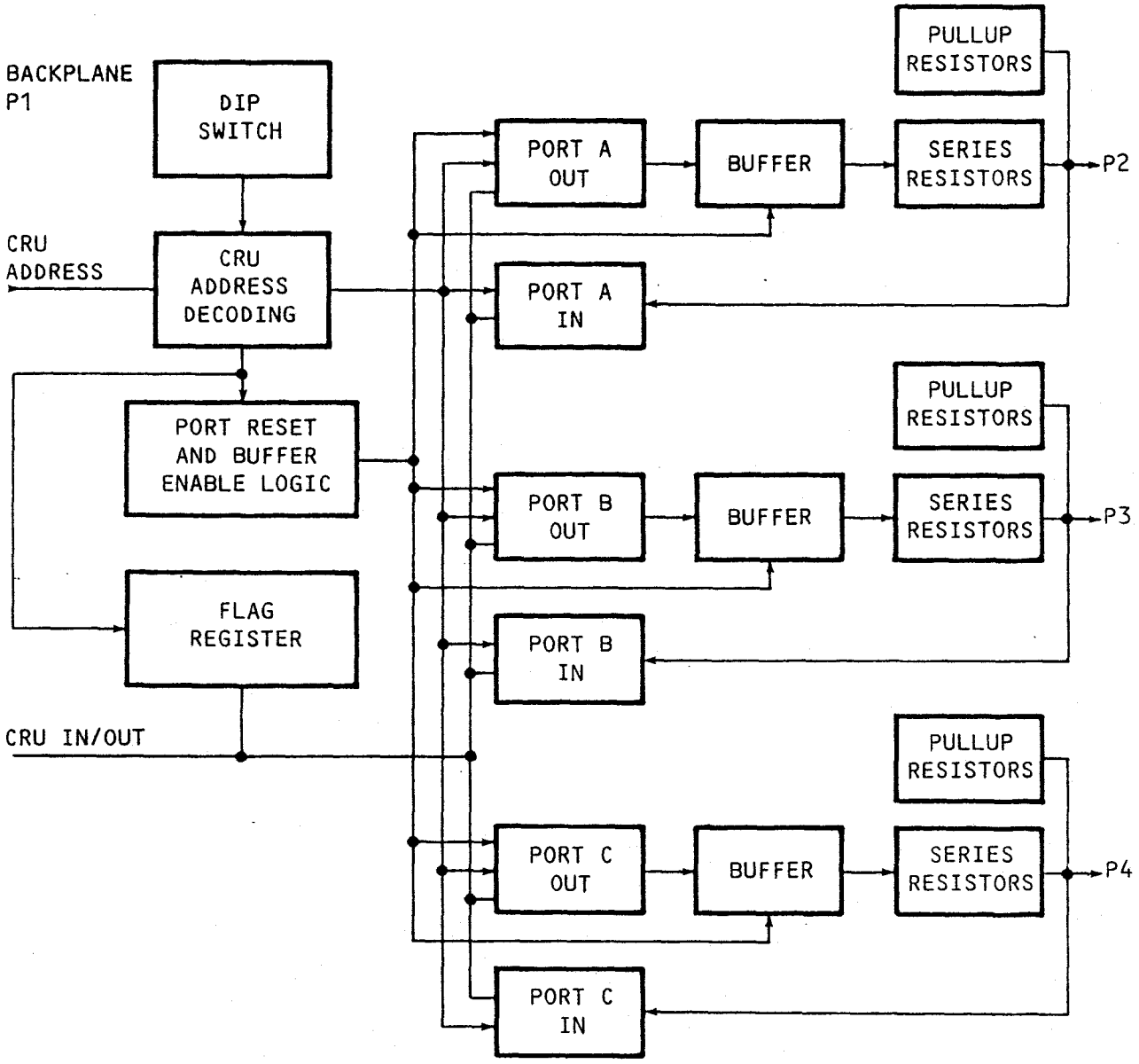



FIGURE 1-3. TM 990/311 BLOCK DIAGRAM

# SECTION 2

# INSTALLATION AND OPERATION

## 2.1 GENERAL

The procedures for unpacking and setting up the TM 990/311 module for operation are given in this section. The switch and jumper configurations as shipped are given in section 2.12.

## 2.2 UNPACKING AND INSPECTION

Remove the TM 990/311 from its carton and discard any protective wrapping. Inspect the module for any damage that might have occurred in shipping. Report any damage to your TI supplier.

## 2.3 PORT ADDRESS SELECTION

Each of the three TM 990/311 ports can be assigned a unique CRU base address (see your CPU Module User's Guide for a complete discussion of CRU hardware and CRU software addressing). Either an 8-position socket platform or an 8-position DIP switch (S1, S2, and S3) is provided for the CRU base address selection for each port. If S1, S2, and S3 are socket platforms, the user has the option of using jumpers or inserting a DIP switch in the socket.

If the socket platform is used, jumpers at S1-1 to S1-8 are inserted to indicate a logical one; sockets left unjumpered will be set to a logical zero. If a DIP switch is used, switch settings are ON = 1, OFF = 0. Comparator circuitry compares the jumper/switch values with values found on bus address lines A3 (Sx-1) to A8 (Sx-6).

The ports selected by each switch/jumper bank and the connector associated with each port are shown in Figure 2-1 and Figure 2-2. Figure 2-1 shows a DIP switch configuration. Figure 2-2 shows the socket platform and jumper method.

TABLE 2-1. CORRELATION BETWEEN SWITCH BANKS, PORTS AND CONNECTORS

| Port Designation | Switch/Jumper Number | Connector Designation |
|---|---|---|
| A | S3 | P2 |
| B | S2 | P3 |
| C | S1 | P4 |

Since each port occupies 64 CRU bits, and since there are only 12 bits of address (A3 - A14) which are used for CRU addressing, there are six positions in the address selection switch/jumper bank which determine the address of the port as shown in Figures 2-1 and 2-2.

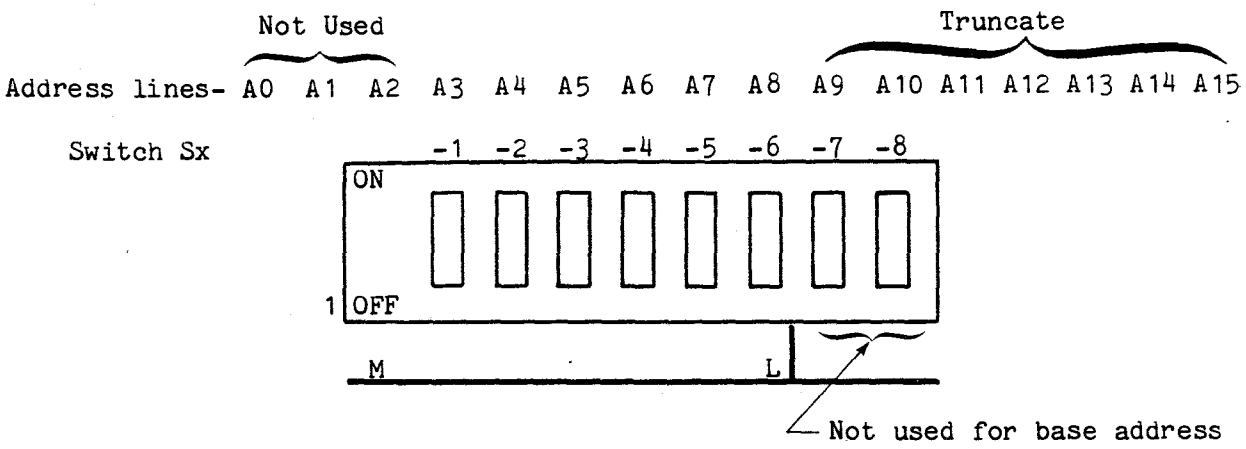



FIGURE 2-1. PORT ADDRESS SWITCH ASSIGNMENTS

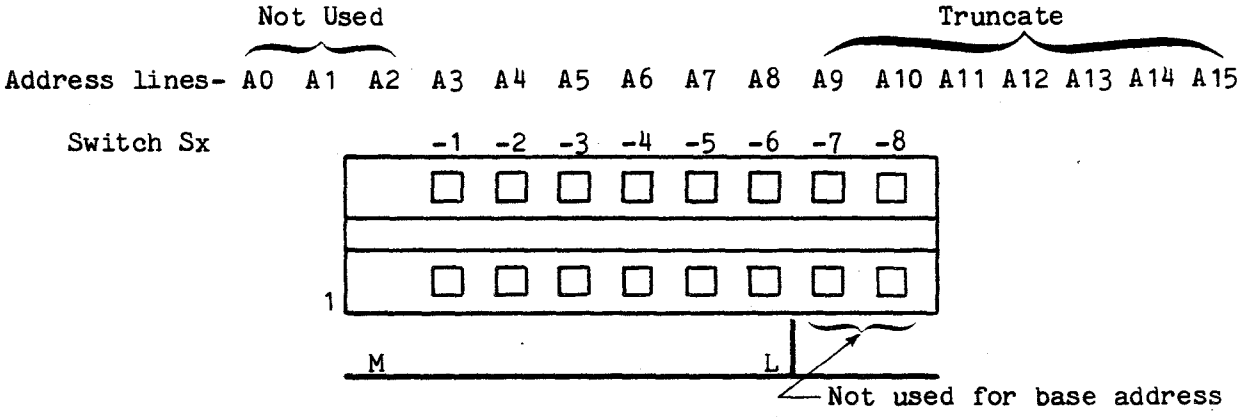



FIGURE 2-2. PORT ADDRESS JUMPER ASSIGNMENTS

NOTE

Switch/jumper numbers 7 and 8 of each switch/jumper bank are used for other purposes which are described in section 2.4.

Each port can be placed anywhere in the CRU address space with the following restrictions:

1) Do not select a CRU software base address (full R12 contents) between $0000_{16}$ and $0200_{16}$. This CRU space is reserved for CPU functions.

2) Do not select the same address for more than one port on the same TM 990/311 module. The TM 990/311 has protection circuitry which prevents accessing two ports with the same address. If the user accidently sets the same address on more than one switch/jumper bank, the ports with the duplicate addresses will be disabled.

Table 2-2 shows the switch/jumper settings for a few example CRU base addresses.

TABLE 2-2. CRU BASE ADDRESS SELECT SWITCHES/JUMPERS

| Switch Positions | | | | | | Hardware Base Addr. | | Software Base Addr. (Hex) |
|---|---|---|---|---|---|---|---|---|
| MSB A3 | A4 | A5 | A6 | A7 | LSB A8 | (Dec) | (Hex) | |
| Sx-1 | Sx-2 | Sx-3 | Sx-4 | Sx-5 | Sx-6 | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | | | |
| 0 | 0 | 0 | 0 | 1 | 0 | | Not Used | |
| 0 | 0 | 0 | 0 | 1 | 1 | | | |
| 0 | 0 | 0 | 1 | 0 | 0 | | | |
| 0 | 0 | 0 | 1 | 0 | 1 | 320 | 0140 | 0280 |
| 0 | 0 | 0 | 1 | 1 | 0 | 384 | 0180 | 0300 |
| 0 | 0 | 0 | 1 | 1 | 1 | 448 | 01C0 | 0380 |
| 0 | 0 | 1 | 0 | 0 | 0 | 512 | 0200 | 0400 |
| 0 | 0 | 1 | 0 | 0 | 1 | 576 | 0240 | 0480 |
| 0 | 0 | 1 | 0 | 1 | 0 | 640 | 0280 | 0500 |
| 0 | 0 | 1 | 0 | 1 | 1 | 704 | 02C0 | 0580 |
| 0 | 0 | 1 | 1 | 0 | 0 | 768 | 0300 | 0600 |
| | | | . | | | . | . | . |
| | | | . | | | . | . | . |
| | | | . | | | . | . | . |
| 1 | 1 | 1 | 1 | 1 | 1 | 4032 | 0FC0 | 1F80 |

Note: For DIP switches- 1 = ON; 0 = OFF
For Jumper Platform- 1 = Jumpered; 0 = Unjumpered

The port address switch/jumper settings for a CRU base address not shown in Table 2-2 may be determined by the following method:

1) Convert the CRU hardware base address into its binary equivalents.

2) Strip off the first four bits; the CRU hardware base address is a 12-bit value using only the 12 LSBs applied to address lines A3 to A14; since only address lines A3 to A8 are compared on the board, use the first six bits of these remaining 12 bits.

3) Convert the six MSBs of the remaining 12 bits (obtained in step 2) into ON/OFF equivalents to determine the switch settings. The following definitions apply: 1 = ON (or jumpered) ; 0 = OFF (or unjumpered).

Example: Determine the switch settings required to select CRU hardware base address $0140_{16}$ (software base address $0280_{16}$) for Port A.

1) 0 1 4 0 Hardware Base Address (Hex)

0000 0001 0100 0000 Binary equivalent of Hardware Base Address

2) 0001 01 Strip off first 4 bits; use next six MSBs which are compared to address lines A3 to A8

3)

| | A3 | A4 | A5 | A6 | A7 | A8 |
|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 1 | 0 | 1 |
| | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| | OFF | OFF | OFF | ON | OFF | ON |
| Port A Settings = S3 | -1 | -2 | -3 | -4 | -5 | -6 |

## 2.4 PORT AND OUTPUT DISABLE SWITCHES/JUMPERS

Switch/jumper number 7 of each switch bank (S1, S2 or S3) disables the corresponding port when left open (OFF or unjumpered). Switch/jumper 7 must be set ON/Jumpered for each port in use.

Switch/jumper number 8 of each switch bank (S1, S2, or S3) acts as a output disable when closed (ON/Jumpered). When switch/jumper 8 is ON/Jumpered, the corresponding port is set as an input-only port.

The settings of switch/jumper number 7 and 8 are summarized in Table 2-3.

TABLE 2-3. PORT AND OUTPUT DISABLE SWITCHES/JUMPERS (SX-7, SX-8)

| Switch No. | Setting | Function |
|---|---|---|
| -7 | ON/Jumpered | Enable Port |
| | OFF/Unjumpered | Disable Port |
| -8 | ON/Jumpered | Set Port as input only |
| | OFF/Unjumpered | Set Port as input and output |

## 2.5 JUMPER SELECTIONS

This subsection describes the jumper options on the TM 990/311.

### 2.5.1 Jumper J1

Jumper J1 enables or disables the Flag register on the TM 990/311. Section 2.10 describes the use of the Flag register. The connections for this jumper are as follows:

| J1 Pin No. | Function Selected |
|---|---|
| 2 to 1 | Flag Register enabled |
| 2 to 3 | Flag Register disabled |

### 2.5.2 Jumper J2

Jumper J2 couples + 8 volts to pin No. 4 on all three port connectors (P2-4, P3-4 and P4-4). The connections for this jumper are as follows:

| J2 Pin No. | Function Selected |
|---|---|
| 2 to 1 | +8 V to P2-4, P3-4, P4-4 |
| 2 to 3 | P2-4, P3-4, P4-4 are open circuit |

### 2.5.3 Jumper J3

Jumper J3 couples + 12 volts to pin No. 1 on all three port connectors (P2-1, P3-1 and P4-1). The connections for this jumper are as follows:

| J3 Pin No. | Function Selected |
|---|---|
| 2 to 1 | +12 V to P2-1, P3-1, P4-1 |
| 2 to 3 | P2-1, P3-1, P4-1 are open circuit |

### 2.5.4 Jumper J4

Jumper J4 couples - 12 volts to pin No. 2 on all three port connectors (P2-2, P3-2 and P4-2). The connections for this jumper are as follows:

| J4 Pin No. | Function Selected |
|---|---|
| 2 to 1 | -12 V to P2-2, P3-2, P4-2 |
| 2 to 3 | P2-2, P3-2, P4-2 are open circuit |

### 2.5.5 Jumper J5 Through J10

These jumpers allow the user to select one of three output buffers (74LS240, 74LS241 or 74LS244) for each output block (8 bits). The factors in the decision of which buffer to use is given in section 2.7. Table 2-4 gives the jumper pin connections for each jumper, which block is affected by that jumper the type of buffer selected, and the socket containing the chip. Section 2.6 describes the port connectors and their nomenclature.

TABLE 2-4. OUTPUT BUFFER JUMPERS (J5 - J10)

| Jumper No. | Block Affected | Pin Connections for 74LS241 | Pin Connections for 74LS240 or 74LS244 | Socket No. |
|---|---|---|---|---|
| | Port A | | | |
| J10 | 'L' Block | 1 to 2 | 2 to 3 | U37 |
| J 9 | 'H' Block | 1 to 2 | 2 to 3 | U35 |
| | Port B | | | |
| J 8 | 'L' Block | 1 to 2 | 2 to 3 | U33 |
| J 7 | 'H' Block | 1 to 2 | 2 to 3 | U31 |
| | Port C | | | |
| J 6 | 'L' Block | 1 to 2 | 2 to 3 | U29 |
| J 5 | 'H' Block | 1 to 2 | 2 to 3 | U27 |

2.5.6 Jumpers J11 through J16

Jumpers J11 through J16 allow the user to set the output shunt resistors of each block as pull-up or pull-down resistors. The factors involved in the use of these resistors is covered in section 2.8. Table 2-5 shows the connections of each jumper and the block affected. Figure 2-3 shows the layout of each jumper.

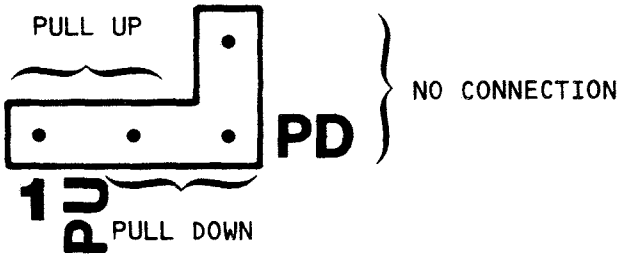



FIGURE 2-3. LAYOUT OF JUMPERS J11 THROUGH J16

TABLE 2-5. OUTPUT RESISTOR JUMPERS

| Jumper No. | Block Affected | Connection to Set Resistors as Pull-ups | Connection to set Resistors as Pull-downs |
|---|---|---|---|
| | Port A | | |
| J16 | 'L' Block | 1 to 2 | 2 to 3 |
| J15 | 'H' Block | 1 to 2 | 2 to 3 |
| | Port B | | |
| J14 | 'L' Block | 1 to 2 | 2 to 3 |
| J13 | 'H' Block | 1 to 2 | 2 to 3 |
| | Port C | | |
| J12 | 'L' Block | 1 to 2 | 2 to 3 |
| J11 | 'H' Block | 1 to 2 | 2 to 3 |

2.5.7 Jumper J17

Jumper J17 couples + 5 volts to pin No. 3 on all three port connectors (P2-3, P3-3 and P4-3). The connections for this jumper are as follows:

| J17 Pin No. | Function Selected |
|---|---|
| 2 to 1 | +5 V to P2-3, P3-3, P4-3 |
| 2 to 3 | P2-3, P3-3, P4-3 are open circuit |

2.6 EDGE CONNECTORS P2, P3, P4

The 48 I/O bits of the TM 990/311 are organized into 3 ports. Each port has its own edge connector (marked A, B and C on the component side of the board).

Each port is divided into 2 blocks. Each block contains 8 I/O bits. The assignments for each pin of the board edge connectors are shown in Figure 2-4. The assignments are the same for all three ports.

The top view in Figure 2-4 shows the board edge connector as seen from the component side. The number '2' is marked on the component side of the board to index the connector pin numbers.

**CAUTION**

The numbers marked on a given cable connector may not correspond to the numbers assigned to the board edge connector pins. The cable connector should be wired according the board edge connector numbers.

Figure 2-5 shows the connector assignments arranged by port and I/O bits for convenience in keeping track of the I/O bits.

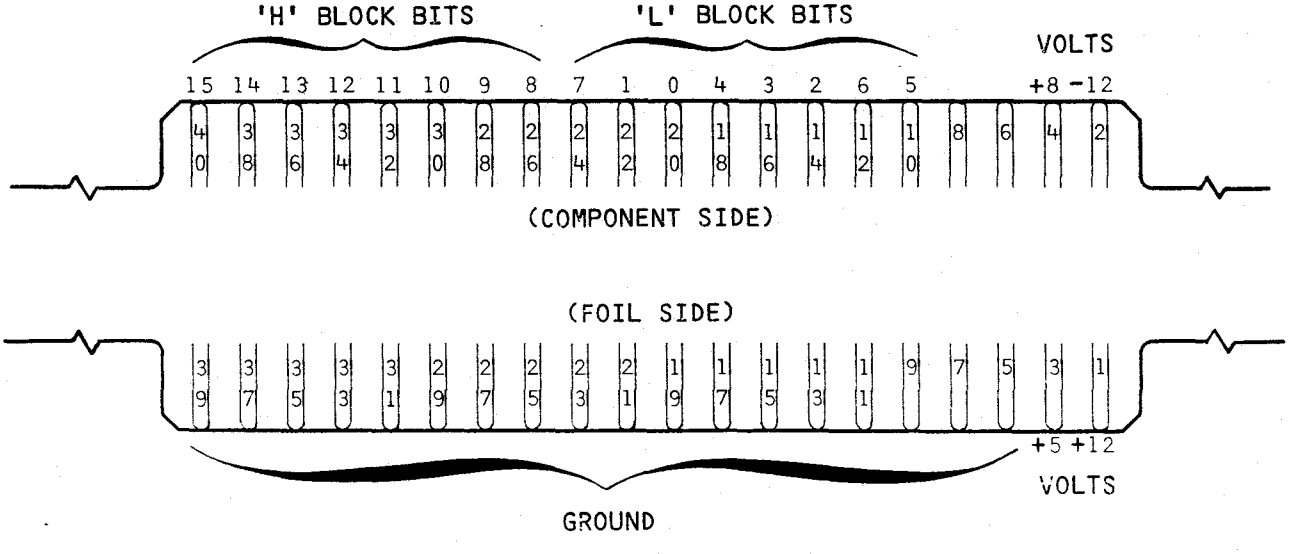



FIGURE 2-4. EDGE CONNECTOR ASSIGNMENTS

| PORT | BLOCK | I/O No. | CONNECTOR PIN No. | ASSIGNMENTS |
|---|---|---|---|---|
| Port A<br>Connector P2 | Low Block | 0 | 20 | |
| | | 1 | 22 | |
| | | 2 | 14 | |
| | | 3 | 16 | |
| | | 4 | 18 | |
| | | 5 | 10 | |
| | | 6 | 12 | |
| | | 7 | 24 | |
| | High Block | 8 | 26 | |
| | | 9 | 28 | |
| | | 10 | 30 | |
| | | 11 | 32 | |
| | | 12 | 34 | |
| | | 13 | 36 | |
| | | 14 | 38 | |
| | | 15 | 40 | |
| Port B<br>Connector P3 | Low Block | 0 | 20 | |
| | | 1 | 22 | |
| | | 2 | 14 | |
| | | 3 | 16 | |
| | | 4 | 18 | |
| | | 5 | 10 | |
| | | 6 | 12 | |
| | | 7 | 24 | |
| | High Block | 8 | 26 | |
| | | 9 | 28 | |
| | | 10 | 30 | |
| | | 11 | 32 | |
| | | 12 | 34 | |
| | | 13 | 36 | |
| | | 14 | 38 | |
| | | 15 | 40 | |
| Port C<br>Connector P4 | Low Block | 0 | 20 | |
| | | 1 | 22 | |
| | | 2 | 14 | |
| | | 3 | 16 | |
| | | 4 | 18 | |
| | | 5 | 10 | |
| | | 6 | 12 | |
| | | 7 | 24 | |
| | High Block | 8 | 26 | |
| | | 9 | 28 | |
| | | 10 | 30 | |
| | | 11 | 32 | |
| | | 12 | 34 | |
| | | 13 | 36 | |
| | | 14 | 38 | |
| | | 15 | 40 | |

FIGURE 2-4. PORT/CONNECTOR ASSIGNMENTS

## 2.7 OUTPUT BUFFERS

The TM 990/311 is shipped with 74LS244 non-inverting output socketed buffers on each block of 8 bits. This part may be replaced with either 74LS241 non-inverted buffers or 74LS240 inverting buffers if needed. When this replacement is made the appropriate jumper connections will have to made as described in section 2.5.5. Table 2-4 includes the socket number for each port buffer.

When the 74LS244 buffer is used for a given block, a reset operation sets all zeroes on the block outputs (if enabled). Writing a one to a bit results in a one on the corresponding edge connector.

When 74LS240 buffer is used for a given block, a reset operation sets all ones (if enabled). Writing a one to a bit results in a zero on the corresponding edge connector pin. This configuration might be useful if an external device under control also inverts the control signal (such as the TM 990/5MT I/O system).

Upon I/O reset, all block outputs on the TM 990/311 are disabled (i.e.,all blocks are reset as inputs). When the output buffers are disabled, the voltage and current levels at the edge connector pins are determined by the cable, receiving devices and the Pull-up/Pull-down output resistors.

Writing to any bit of a block sets that entire block (all eight bits) to the output enabled condition (output buffers enabled). In order to avoid confusion, the user should always output 8-bit or 16-bit wide fields when first initializing the output mode of a port (this sets all the bits of a block to a known state). After initialization, the value of individual bits may be changed with any single-bit or multi-bit CRU instruction. Once enabled, the block will remain in the output mode until reset via hardware (I/O reset; e.g., actuate RESET switch at microcomputer) or software (write a one first to CRU bit 0, then bit 15).

## 2.8 OUTPUT RESISTORS

The TM 990/311 user has several output resistor configurations available. The output resistors are included in DIP resistor packs. These resistor packs are shown on schematic sheet 4 (Appendix A-5) and schematic sheet 5 (Appendix A-6). Table 2-6 shows the resistor pack, sockets (U designations), and the associated port and block.

TABLE 2-6. OUTPUT RESISTOR PACKS AND ASSOCIATED PORTS

| Port | Block | Socket Locations | |
|---|---|---|---|
| | | Shunt Resistors | Series Resistors |
| Port A | 'L' Block | U55 | U44 |
| | 'H' Block | U53 | U43 |
| Port B | 'L' Block | U51 | U42 |
| | 'H' Block | U49 | U41 |
| Port C | 'L' Block | U47 | U40 |
| | 'H' Block | U45 | U39 |

### 2.8.1 Shunt Resistors

These resistors may be set by jumper (see section 2.5.6 and Table 2-5) as Pull-ups (to +5 V), Pull-downs (to ground) or disabled. In normal TTL operation, these resistors would be set as Pull-up resistors with a value between 1K ohms and 10K ohms. The TM 990/311 module is shipped with 4.7K ohm resistor packs installed. The user may substitute other values as required by the loading conditions of a specific application.

The use of the shunt resistors as Pull-downs is less common; this option should be adopted only after careful calculation of currents and voltages between the user's circuitry and the buffers of the TM 990/311.

### 2.8.2 Series Resistors

The TM 990/311 is shipped with a short-circuit jumper arrangement providing zero ohms of series resistance between the output buffer and the user circuitry. The pin arrangement of the jumper sockets is compatible with commonly available resistor packs, which may be substituted as the application requires. This substitution is made if special isolation requirements arise because of the nature of the circuitry attached to the TM 990/311 ports.

## 2.9 INPUT BUFFERS

The input buffers on the TM 990/311 are connected directly to the edge connector. This arrangement allows the user to do the following:

1) read values on the edge connector when in the input mode.

2) read the values on the edge connector when in the output mode as an echo-back check of proper output buffer operation.

## 2.10 FLAG REGISTER

The Flag register gives 32 bits of user-defined information for each port base address (96 bits in all). The register is accessed via the CRU as indicated in Figure 3-1 (see section 3.6). Each bit is unique, and can be set, reset, or tested individually or in a group by the CRU instructions.

## 2.11 RESET ENABLE LEDS

Each port on the TM 990/311 has one LED associated with it. The LED lights when the software RESET ENABLE is active for the appropriate port. When RESET ENABLE is inactive the LED is off (see section 3.2).

Flag bit 0 is at the same CRU address as the RESET ENABLE circuitry (see Table 3-1); thus the LED also reflects the state of Flag bit 0 (1 = ON, 0 = OFF). Flag bit 0 can be tested by software to determine whether the LED is ON or OFF.

## 2.12 CONFIGURATION AS SHIPPED

The TM 990/311 is shipped with switch/jumpers set as shown in Figure 2-6 and Figure 2-7. Table 2-7 shows the jumper configurations as shipped. The TM 990/311 is shipped with 4.7 Kilohms shunt resistors, 0 ohm (jumper shorted) series resistors and 74LS244 output buffers.

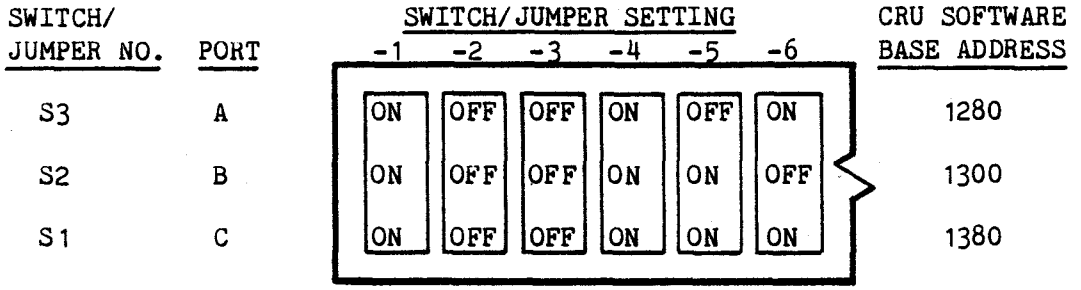



FIGURE 2-6. PORT ADDRESS SWITCH/JUMPER SETTINGS AS SHIPPED

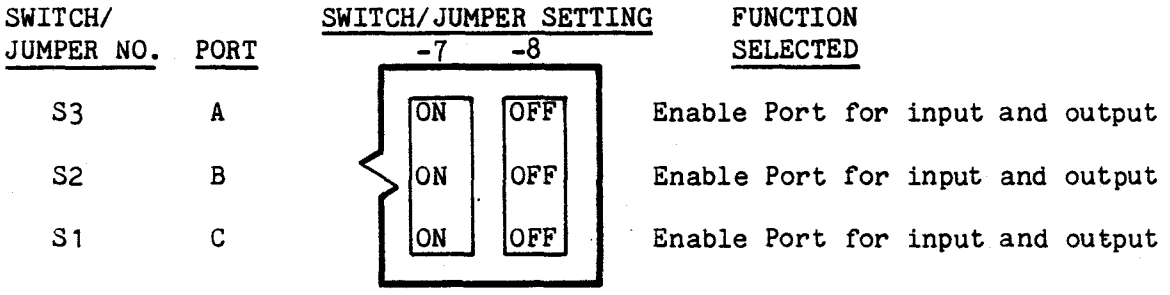



FIGURE 2-7. PORT AND OUTPUT DISABLE SWITCH/JUMPER SETTINGS AS SHIPPED

TABLE 2-7. JUMPER CONNECTIONS AS SHIPPED

| JUMPER | PIN CONNECTION | FUNCTION SELECTED |
|---|---|---|
| J1 | 2-1 | Flags enabled |
| J2 | 2-1 | Edge +8 volts deselected |
| J3 | 2-1 | Edge +12 volts deselected |
| J4 | 2-1 | Edge -12 volts deselected |
| J5-J10 | 2-3 | 74LS244 Buffers |
| J11-J16 | 2-1 | Pull-up resistors |
| J17 | 2-1 | Edge +5 volts deselected |

## 2.13 EXAMPLE PROGRAMS

The programs in section 3.8 can be loaded and executed as an initial board checkout. Use the TIBUG memory inspect/change command (M) to enter the object code beginning at memory address $FC00_{16}$. Then set the program counter to $FC20_{16}$ and execute using the E command.

# SECTION 3

# PROGRAMMING

## 3.1 GENERAL

This section describes how to use the CRU to access the TM 990/311 and do the following:

- Reset the ports with software
- Set and write to output ports
- Echo output data
- Read from input ports
- Write to and read from the flag register

### 3.1.1 Programming Considerations

The following points should be kept in mind while writing software for the TM 990/311 or studying the examples:

- The value written to an output port remains latched until reset or changed by the program.

- Once written to, an 8-bit block remains set as output, but it can be read (echoed) via the CRU.

- To read off-board data at a port, first RESET the port to the input mode by software. RESET can be tested because a software RESET also sets flag bit 15 to zero.

### 3.1.2 Example Program Assumptions

The following switch settings are assumed for all of the following examples:

| | Switch No. - | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|---|
| Switch S3 (Port A address - $0300_{16}$) = | | OFF | OFF | OFF | ON | ON | OFF | ON | OFF |
| Switch S2 (Port B address - $0400_{16}$) = | | OFF | OFF | ON | OFF | OFF | OFF | ON | OFF |
| Switch S1 (Port C address - $0500_{16}$) = | | OFF | OFF | ON | OFF | ON | OFF | ON | OFF |

Sx-7 (ON) = Enable Port
Sx-8 (OFF) = Output enabled

The following jumper settings are assumed for all of the following examples:

| Jumper # | Connection | Function Selected |
|---|---|---|
| J1 | Pin 1 to Pin 2 | Enable Flag Register |
| J2-J4 | Pin 2 to Pin 3 | No Power Out |
| J5-J10 | Pin 2 to Pin 3 | Output buffer = 74LS244 |
| J11-J16 | Pin 1 to Pin 2 | Output resistors set as pull-ups |
| J17 | Pin 2 to Pin 3 | No Power Out |

TABLE 3-1. CRU MAP OF EACH PORT (A, B OR C)

| Swftwr[1] Displ.16 | CRU[2] Bit | Bit Description | Conn.[3] Assign. | Swftwr Displ.16 | CRU Bit | Bit Description | Conn. Assign. |
|---|---|---|---|---|---|---|---|
| 0 | 0 | Reset Enable/ LED/Flag 0 | - | 40 | 33 | Flag 16 | - |
| 2 | 1 | Flag 1 | - | 42 | 34 | Flag 17 | - |
| 4 | 2 | Flag 2 | - | 44 | 35 | Flag 18 | - |
| 6 | 3 | Flag 3 | - | 46 | 36 | Flag 19 | - |
| 8 | 4 | Flag 4 | - | 48 | 37 | Flag 20 | - |
| A | 5 | Flag 5 | - | 4A | 38 | Flag 21 | - |
| C | 6 | Flag 6 | - | 4C | 39 | Flag 22 | - |
| E | 7 | Flag 7 | - | 4E | 40 | Flag 23 | - |
| 10 | 8 | Flag 8 | - | 50 | 41 | Flag 24 | - |
| 12 | 9 | Flag 9 | - | 52 | 42 | Flag 25 | - |
| 14 | 10 | Flag 10 | - | 54 | 43 | Flag 26 | - |
| 16 | 11 | Flag 11 | - | 56 | 44 | Flag 27 | - |
| 18 | 12 | Flag 12 | - | 58 | 45 | Flag 28 | - |
| 1A | 13 | Flag 13 | - | 5A | 46 | Flag 29 | - |
| 1C | 14 | Flag 14 | - | 5C | 47 | Flag 30 | - |
| 1E | 15 | Reset/Flag 15 | - | 5E | 48 | Flag 31 | - |
| 'L' Block | | | | | | | |
| 20 | 16 | I/O 0 | Px-20 | 60 | 49 | I/O 0 | Px-20 |
| 22 | 17 | I/O 1 | Px-22 | 62 | 50 | I/O 1 | Px-22 |
| 24 | 18 | I/O 2 | Px-14 | 64 | 51 | I/O 2 | Px-14 |
| 26 | 19 | I/O 3 | Px-16 | 66 | 52 | I/O 3 | Px-16 |
| 28 | 20 | I/O 4 | Px-18 | 68 | 53 | I/O 4 | Px-18 |
| 2A | 21 | I/O 5 | Px-10 | 6A | 54 | I/O 5 | Px-10 |
| 2C | 22 | I/O 6 | Px-12 | 6C | 55 | I/O 6 | Px-12 |
| 2E | 23 | I/O 7 | Px-24 | 6E | 56 | I/O 7 | Px-24 |
| 'H' Block | | | | | | | |
| 30 | 24 | I/O 8 | Px-26 | 70 | 57 | I/O 8 | Px-26 |
| 32 | 25 | I/O 9 | Px-28 | 72 | 58 | I/O 9 | Px-28 |
| 34 | 26 | I/O 10 | Px-30 | 74 | 59 | I/O 10 | Px-30 |
| 36 | 27 | I/O 11 | Px-32 | 76 | 60 | I/O 11 | Px-32 |
| 38 | 28 | I/O 12 | Px-34 | 78 | 61 | I/O 12 | Px-34 |
| 3A | 29 | I/O 13 | Px-36 | 7A | 62 | I/O 13 | Px-36 |
| 3C | 30 | I/O 14 | Px-38 | 7C | 63 | I/O 14 | Px-38 |
| 3E | 31 | I/O 15 | Px-40 | 7E | 64 | I/O 15 | Px-40 |

[1]This column represents the value to be added to the software base address to access a given bit or block.

[2]This column represents the displacement to be used with a CRU single bit instruction (e.g., SBO, SBZ, TB) with no displacement added to the base address.

[3]This column gives the pin assignments for the appropriate I/O bit for each CRU address.

### 3.1.3 CRU Map

Table 3-1 shows the CRU map for each of the three ports (A, B OR C) on the TM 990/311. The first and third block of 16 bits in the CRU map access the Flag register or reset functions. There are 32 unique bits in the Flag register for each port base address.

The second and fourth block of 16 bits access the I/O bits. Notice that each I/O bit (I/O 0 through I/O 15) have duplicate addresses. For example, if the CRU base address is $0300_{16}$, I/O 0 can be accessed with a CRU address of $0320_{16}$ or $0360_{16}$. This duplicate addressing provides software compatibility with the the addressing scheme of the TM 990/310. In the CRU map for the TM 990/310, the second address (i.e., $0360_{16}$) is the echo address of an output port with an address of $0320_{16}$.

## 3.2 RESETTING PORTS WITH SOFTWARE

The TM 990/311 was designed to be as software compatible as possible with the TM 990/310. Software Reset is accomplished via the CRU as if the user were writing to a TMS 9901 PSI. This example assumes that Port A had previously been set as an output port (e.g., had been written to via the CRU). Now, the user wishes to reset the port for some other use. Since switch S3 is set to a software base address of $0300_{16}$, register R12 is loaded with $0300_{16}$. CRU bits 0 and 15 are the 'RESET ENABLE' and 'RESET' signals respectively (see Table 3-1).

```
START LI   R12,>0300        LOAD BASE ADDRESS FOR PORT A
      SBO  0                ENABLE RESET FOR PORT A
      SBZ  15               RESET PORT A
      SBZ  0                DISABLE RESET FOR PORT A
```

NOTES

1. Writing a one to CRU bit 0 also lights the port LED, writing a zero to CRU bit 0 turns off the port LED.

2. Because writing to bit 15 also sets the flag bit accordingly, a port can be checked for having been reset by reading bit 15 for a known logic one condition.

## 3.3 SETTING AND WRITING TO OUTPUT PORTS

The first time a port (or block) is written to, it is set as an output until reset by hardware (e.g., RESET switch actuated on the microcomputer board) or software (see section 3.2). This example code sets all 16 bits of Port B as output; therefore, both blocks of Port B are set as output.

```
START LI   R12,>0420        LOAD BASE ADDRESS OF PORT B PLUS I/O DISPLACEMENT
      MOV  @DATA,R2         LOAD DATA TO BE OUTPUT INTO R2
      LDCR R2,0             OUTPUT 16 BITS
```

## 3.4 ECHOING OUTPUT DATA

The following code demonstrates two ways to echo. The first method uses the same address as the output ports after data has been written to the port (as in section 3.3).

```
START LI   R12,>0420        LOAD BASE ADDRESS OF PORT B PLUS I/O DISPLACEMENT
      MOV  @DATA,R2         LOAD DATA TO BE OUTPUT INTO R2
      LDCR R2,0             OUTPUT 16 BITS
      STCR R3,0             ECHO 16 OUTPUT BITS
      C    R2,R3            COMPARE DATA SENT, DATA RECEIVED
      JNE  ERROR            IF NOT THE SAME, CHECK
```

The second method uses the duplicate address for echoing.

```
START LI   R12,>0420        LOAD BASE ADDRESS OF PORT B PLUS I/O DISPLACEMENT
      MOV  @DATA,R2         LOAD DATA TO BE OUTPUT INTO R2
      LDCR R2,0             OUTPUT 16 BITS
      LI   R12,>0460        LOAD 'ECHO' ADDRESS FOR PORT B
      STCR R3,0             ECHO 16 OUTPUT BITS
      C    R2,R3            COMPARE DATA SENT, DATA RECEIVED
      JNE  ERROR            IF NOT THE SAME, CHECK
```

## 3.5 READING FROM INPUT PORTS

Any port not set as an output can be used as an input-only port. This code reads the 'H' block of Port C.

```
START  LI    R12,>0530       LOAD BASE ADDRESS OF PORT C PLUS I/O DISPLACEMENT
*                           FOR THE 'H' BLOCK
       STCR R2,8            READ 8 BITS OF THE 'H' BLOCK OF PORT C
```

## 3.6 WRITE TO AND READ FROM THE FLAG REGISTER

This code writes to Flag bit 3 of Port A and reads Flag bit 5 of Port B.

```
START LI   R12,>0300          LOAD BASE ADDRESS FOR PORT A
      SBO  3                  SET FLAG BIT 3 TO ONE
      LI   R12,>0400          LOAD BASE ADDRESS FOR PORT B
      TB   5
```

## 3.7 EXAMPLE PROGRAMS

The following example programs were tested with a TM 990/101M CPU module. All switches and jumpers on the TM 990/311 were set as described in section 3.1. These programs can be entered and run on a TM 990 CPU system with TIBUG as follows:

1) Use the memory inspect and change command (M) to enter the code in the corresponding memory addresses.

2) Use the hardware register inspect and change command (R) to set the program counter to $FC20_{16}$.

3) Use the execute command (E) to start the program.

### 3.7.1 Example Program to Flash LEDS 1, 2 and 3.

This program turns each RESET ENABLE LED on and off in sequence, 16 times.

```
Addr Code  Label Statement        Comment

FC00             AORG >FC00
                 *
                 *     DEFINTIONS:
                 *
     0300  PORTA EQU  >0300       CRU ADDRESS OF PORT A
     0400  PORTB EQU  >0400       CRU ADDRESS OF PORT B
     0500  PORTC EQU  >0500       CRU ADDRESS OF PORT C
FC00         WSP   BSS  32        RESERVE WORKSPACE
                 *
                 *     ENTRY POINT
                 *
FC20 02E0        LWPI WSP         LOAD WORKSPACE POINTER
FC22 FC00
FC24 0203        LI   R3,>10      LOAD COUNTER FOR NUMBER OF FLASH CYCLES
FC26 0010
                 *
                 *     FLASH PORT A LED
                 *
FC28 020C  START LI   R12,PORTA   LOAD CRU ADDRESS OF PORT A
FC2A 0300
FC2C 1D00        SBO  0           ENABLE PORT A RESET/LIGHT LED FOR PORT A
FC2E 06A0        BL   @DELAY      GO TO DELAY LOOP
FC30 FC60
FC32 1E00        SBZ  0           DISABLE RESET/TURN OFF LED FOR PORT B
FC34 06A0        BL   @DELAY
FC36 FC60
```

```
Addr Code  Label Statement       Comment

           *
           *     FLASH PORT B LED
           *
FC38 020C        LI   R12,PORTB  LOAD CRU ADDRESS OF PORT B
FC3A 0400
FC3C 1D00        SBO  0          LIGHT LED
FC3E 06A0        BL   @DELAY
FC40 FC60
FC42 1E00        SBZ  0          TURN OFF LED
FC44 06A0        BL   @DELAY
FC46 FC60
           *
           *     FLASH PORT C LED
           *
FC48 020C        LI   R12,PORTC  LOAD CRU ADDRESS OF PORT C
FC4A 0500
FC4C 1D00        SBO  0          LIGHT LED
FC4E 06A0        BL   @DELAY
FC50 FC60
FC52 1E00        SBZ  0          TURN OFF LED
FC54 06A0        BL   @DELAY
FC56 FC60
           *
           *     CYCLE COUNTER
           *
FC58 0603        DEC  R3         HAS THE CYCLE GONE 16 TIMES?
FC5A 16E6        JNE  START      IF NOT, DO IT AGAIN
FC5C 0460        B    @>80       GO TO MONITOR IF FINISHED
FC5E 0080
           *
           *     DELAY LOOP SUBROUTINE
           *
FC60 0202  DELAY LI   R2, 8000   SET DELAY COUNTER
FC62 8000
FC64 0602  LOOP  DEC  R2         IS THE COUNTER FINISHED
FC66 16FE        JNE  LOOP       IF NOT, DECREMENT COUNTER
FC68 045B        B    *R11       IF FINISHED, RETURN TO CALLING PROG. SEGMENT
```

### 3.7.2 Example Program to Write, Echo and Read to a Port

This example sets the 'L' block of Port A as output and the 'H' block of Port A as input. This example requires wiring a connector as shown in Figure 3-1. The wiring connects the 'L' block to the corresponding bits of the 'H' block.

The connector is attached to P2 (Port A) for this example. It could be attached to Ports B or C if the CRU base address is changed in the program to the appropriate value for the port used (i.e., $0400_{16}$ for Port B or $0500_{16}$ for Port C).

This example could serve as a simple test of a port. A test pattern ($AA_{16}$) is loaded into the 'L' block output. The 'L' block is echoed and compared with the test pattern. An error message is sent if the bits echoed do not match the bits output. Then, the 'H' block is read as input and compared to the original test pattern. If the inputs do not match the original test pattern an error message is generated.

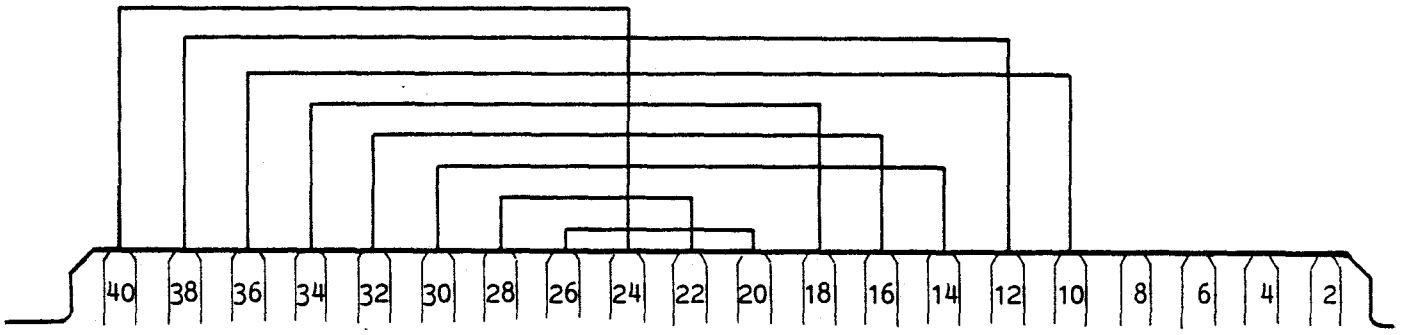



FIGURE 3-1. WIRING CONNECTIONS FOR EXAMPLE 3.7.2

```
Addr Code   Label Statement       Comment

FC00        *
            *     DEFINITIONS
            *
     0300   FLAGA EQU  >0300      CRU ADDRESS OF FLAG REGISTER/RESET OF PORT A
     0320   PORTA EQU  >0320      CRU ADDRESS OF I/O BITS OF PORT A
FC00        WSP   BSS  32        RESERVE WORKSPACE
            *
            *     ENTRY POINT - INITIALIZATION
            *
FC20 02E0           LWPI WSP     LOAD WORKSPACE POINTER
FC22 FC00
FC24 020C           LI   R12,FLAGA  LOAD CRU ADDRESS OF FLAG/RESET
FC26 0300
FC28 1D00           SBO  0       ENABLE RESET
FC2A 1E0F           SBZ  15      RESET PORT A
            *
            *     SET 'L' BLOCK OF PORT A AS OUTPUT - OUTPUT TEST PATTERN
            *
FC2C 020C           LI   R12,PORTA  LOAD CRU ADDRESS OF PORT A I/O BITS
FC2E 0320
FC30 0202           LI   R2,>AA00   LOAD BIT PATTERN '10101010'
FC32 AA00
FC34 3202           LDCR R2,8    SETS 'L' BLOCK=OUTPUT, OUTPUTS PATTERN
FC36 3603           STCR R3,8    ECHOS 'L' BLOCK OUTPUT BACK TO R3
FC38 90C2           CB   2,3     IS ECHO SAME AS OUTPUT?
FC3A 1606           JNE  ERR1    IF NOT, OUTPUT ERROR MESSAGE
FC3C 022C           AI   R12,>10    SET CRU BASE ADDRESS TO 'H' BLOCK
FC3E 0010
FC40 3604           STCR R4,8    READ 'H' BLOCK INPUTS
FC42 9102           CB   2,4     ARE 'H' INPUTS EQUAL TO 'L' OUTPUTS
FC44 160F           JNE  ERR2    IF NOT, OUTPUT ERROR MESSAGE
FC46 101D           JMP  FIN     TESTS PASSED, GO TO FINISH
            *
            *     ERROR MESSAGE ISSUED IF THE ECHO DOES NOT MATCH THE TEST
            *     PATTERN
            *
FC48 2FA0   ERR1    XOP  @MESS1,14  OUTPUT ERROR MESSAGE 1
FC4A FC50
FC4C 0460           B    @>80    BRANCH TO MONITOR
FC4E 0080
```

```
Addr Code  Label Statement        Comment

FC50 0D0A  MESS1 DATA >0D0A       CARRAGE RETURN/LINE FEED
FC52   45        TEXT 'ERROR- NO ECHO'
FC53   52
FC54   52
FC55   4F
FC56   52
FC57   2D
FC58   20
FC59   4E
FC5A   4F
FC5B   20
FC5C   45
FC5D   43
FC5E   48
FC5F   4F
FC60 0D0A        DATA >0D0A       CARRAGE RETURN/LINE FEED
FC62 0000        DATA >0000       END OF MESSAGE TAG
               *     ERROR MESSAGE ISSUED IF THE 'H' INPUTS DO NOT MATCH THE TEST
               *     PATTERN
               *
FC64 2FA0  ERR2  XOP  @MESS2,14   OUTPUT ERROR MESSAGE 2
FC66 FC6C
FC68 0460        B    @>80        BRANCH TO MONITOR
FC6A 0080
FC6C 0D0A  MESS2 DATA >0D0A       CARRAGE RETURN/LINE FEED
FC6E   45        TEXT 'ERROR- NO INPUTS'  ERROR MESSAGE
FC6F   52
FC70   52
FC71   4F
FC72   52
FC73   2D
FC74   20
FC75   4E
FC76   4F
FC77   20
FC78   49
FC79   4E
FC7A   50
FC7B   55
FC7C   54
FC7D   53
FC7E 0D0A        DATA >0D0A       CARRAGE RETURN/LINE FEED
FC80 0000        DATA >0000       END OF MESSAGE TAG
               *
               *     MESSAGE ISSUED IF ALL TESTS PASSED
               *
FC82 2FA0  FIN   XOP  @MESS3,14   OUTPUT TEST PASSED MESSAGE
FC84 FC8A
FC86 0460        B    @>80        BRANCH TO MONITOR
FC88 0080
```

```
Addr Code  Label Statement        Comment

FC8A 0D0A  MESS3 DATA >0D0A       CARRAGE RETURN/LINE FEED
FC8C   54        TEXT 'TESTS PASSED'
FC8D   45
FC8E   53
FC8F   54
FC90   53
FC91   20
FC92   50
FC93   41
FC94   53
FC95   53
FC96   45
FC97   44
FC98 0D0A        DATA >0D0A       CARRAGE RETURN/LINE FEED
FC9A 0000        DATA >0000       END OF MESSAGE TAG
```

SECTION 4

THEORY OF OPERATION

## 4.1 GENERAL

This section describes the theory of operation for the TM 990/311 I/O module. A simplified block diagram of the TM 990/311 is shown in Figure 4-1.

The module can be divided into the following functional elements;

- CRU Address Selection and Decode
- Port Reset and Buffer Enable Logic
- Input/Output Latches and Buffers
- Flag Register
- Voltage Regulator

Address lines shown on figures and schematics with a suffix of '.B' are TM 990 system address bus lines. Address lines with no suffix indicate TM 990/311 address lines.

The following expressions are used in Boolean expressions in the circuit descriptions:

X- = NOT X
+ = Logical OR
* = Logical AND

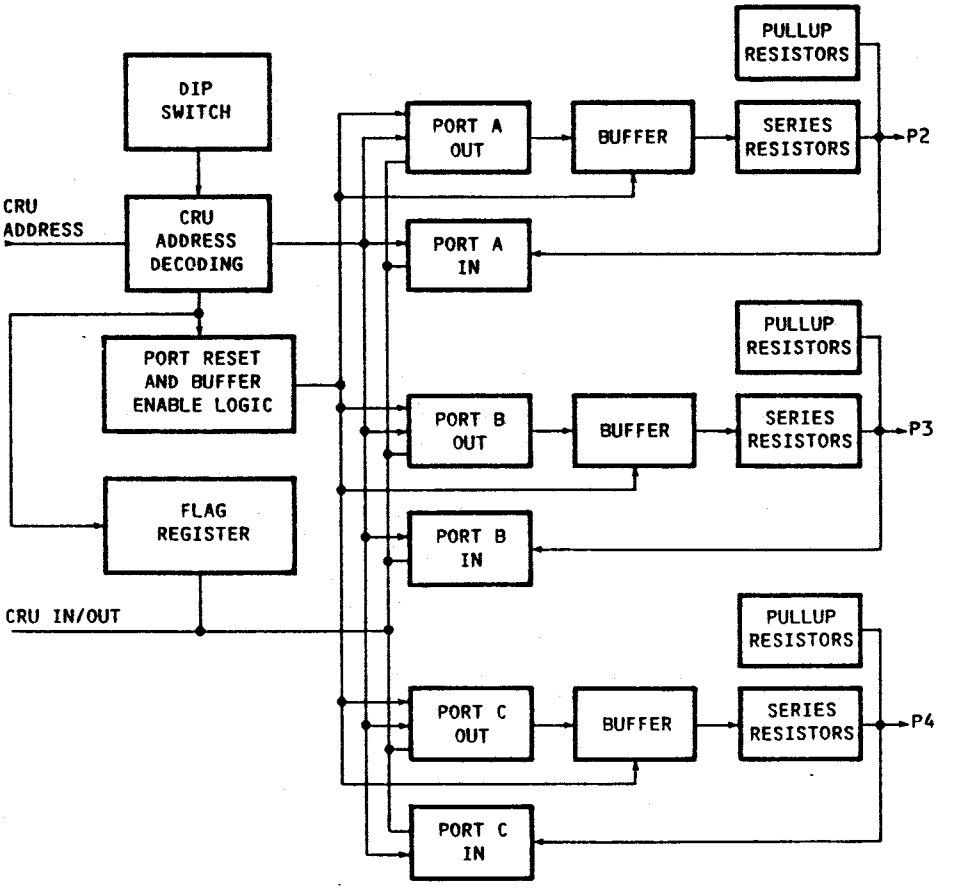



FIGURE 4-1. TM 990/311 BLOCK DIAGRAM

## 4.2 CRU ADDRESS SELECTION/DECODE

The circuits described in this subsection decode a CRU address and generate unique signals which enable one of the six output latches or one of the six input latches. Each latch represents one eight bit block of one of the ports. Each block is designated with a 'H' or 'L' suffix. For example, the line labled 'ASELIN.L-' (in Figure 4-2) carries the select signal for the input latch of the 'L' block of Port A.

The switch select and comparator circuit for Port A is shown in Figure 4-2. The CRU address selection and decode circuits of the other two ports are identical to Figure 4-2. This circuitry can also be found on sheets 2 and 3 of the schematic diagrams (page A-3 and A-4).

Address lines A3.B to A8.B (Figure 4-2) carry the CRU base address. They are inverted and buffered onto the module by a 74LS240 Octal Buffer. The six MSB's of the CRU address (A3- through A8-) are compared to switches S3-1 through S3-6 by the cascaded comparators U1 and U12.

Notice that switch S3-7 is compared to ground (logic 0) by U12; therefore, switch 7 must be closed (ON) in order to get a true comparison signal (A=B) out of U12 (labeled 'BAS' in Figure 4-2). Switch S3-7 acts as a port enable selector. When switch S3-7 is open, port A is disabled, and does not appear at all in the CRU map.

The base address select signals (BAS) from all three port address decoders are routed to U15, a 1-of-8 Data Selector. When any BAS signal is true, the Y output of U15 is high and the W output is low. If more than one BAS signal is true at once, the Y output of U15 will not go active high; therefore, if the same CRU address is set on more than one of the port select switch banks (S1, S2 or S3), none of the ports will be selected when the address appears on the address lines. The active low W output enables CRUIN onto the system bus through U7. The Y output forms the VALID signal in Figure 4-2 and Figure 4-5.

The BAS signal is ANDed with the VALID signal (by U16 in Figure 4-2) to produce a signal labeled 'ASEL'. ASEL is one input to U26, a 2-to-4-line Data Selector (U26 in Figure 4-2 is from schematic sheet 3, page A-4). The signals labeled 'ASELIN.L-' and 'ASELIN.H-' in Figure 4-2 are a Boolean function of ASEL, A11 and A10 as follows:

1) ASELIN.H- = ASEL * A11- * A10-

2) ASELIN.L- = ASEL * A11 * A10-

As can be seen from expressions 1 and 2, the status of A11 determines which 8 bit block (H or L) of each port is selected.

The Boolean expressions for the signals labeled ASELOUT.L- and ASELOUT.H- in Figure 4-2 are as follows:

3) ASELOUT.H- = ASELIN.H- * CRUCLK-

4) ASELIN.L- = ASELIN.L- * CRUCLK-

Expressions 3 and 4 indicate that an 'ASELOUT' signal will be active (low) when the corresponding 'ASELIN' signal is active (low) and CRUCLK- is active (low).

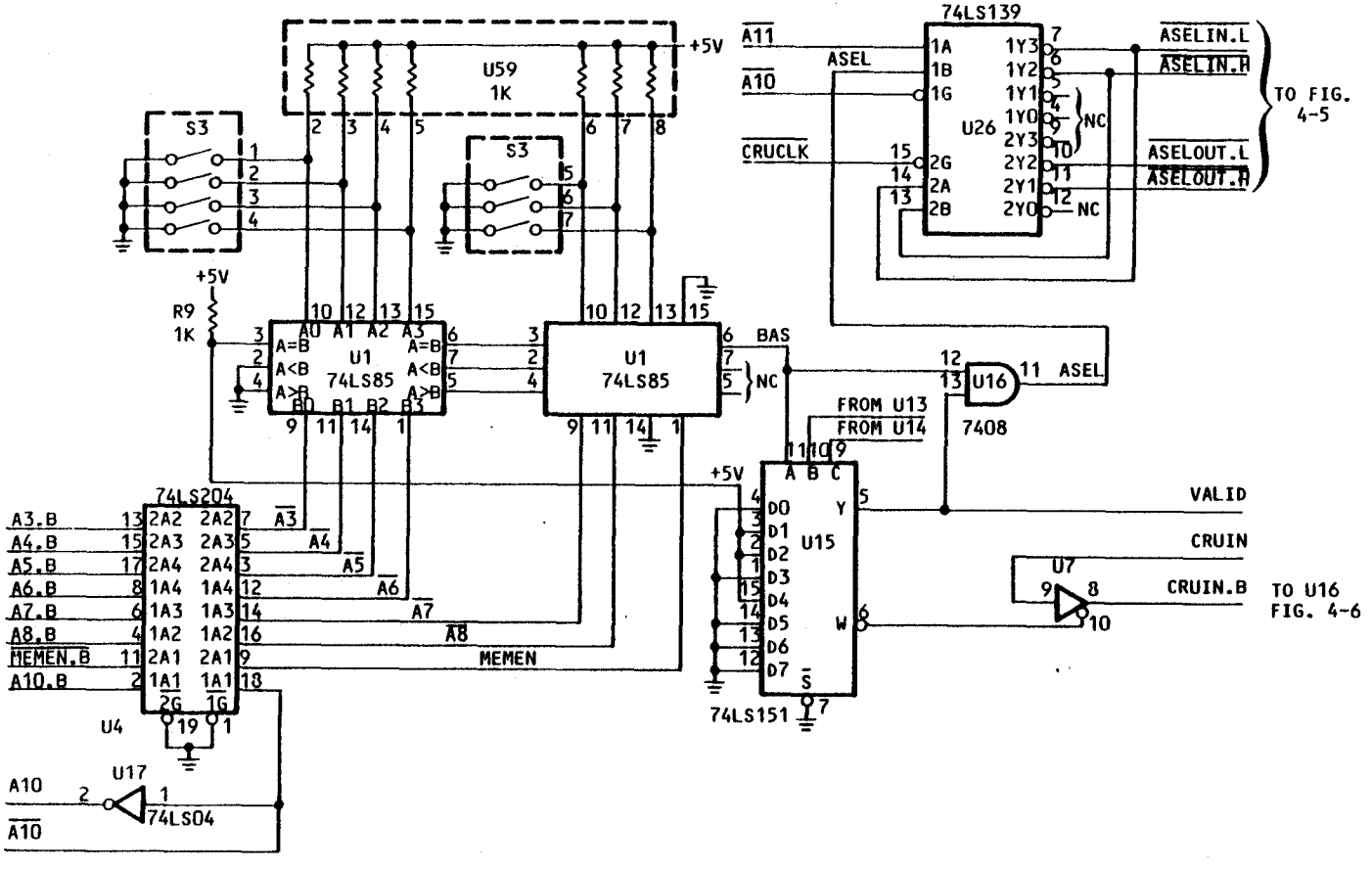



FIGURE 4-2. TM 990/311 CRU ADDRESS SELECTION/DECODE CIRCUITS

## 4.3 PORT RESET AND BUFFER ENABLE LOGIC

The reset logic circuitry is shown in Figure 4-3. This figure shows only the reset logic for Port A. The other two ports have identical counterparts of this circuit which can be found on schematic sheet 4 (page A-5).

The reset logic was designed to simulate the TMS 9901 reset logic so that the TM 990/311 would be software compatible with the TM 990/310.

Logic gates U18 (2) and U9 decode a CRU address equal to the base address for Port A plus a displacement of $00_{16}$. When this address occurs and CRUCLK- goes active low, the content of CRUOUT is clocked into U11 (in Figure 4-3). The Q output of U11 is a reset enable signal (active high). This reset enable signal acts as a gating signal at U19; if active, it allows the port clear signal ADIRCLR-.

Logic gate U8 decodes a CRU address equal to the base address for Port A plus a displacement of $1E_{16}$. When this address occurs (ASEL is high), CRUCLK- is active low and CRUOUT is low, a reset signal (active high) is fed to the inputs of U19; thus, if the reset enable signal is high, ADIRCLR- is generated.

ADIRCLR- is also generated if a RESET- (hardware reset) occurs. Note that RESET- also clears U11, thus clearing the reset enable.

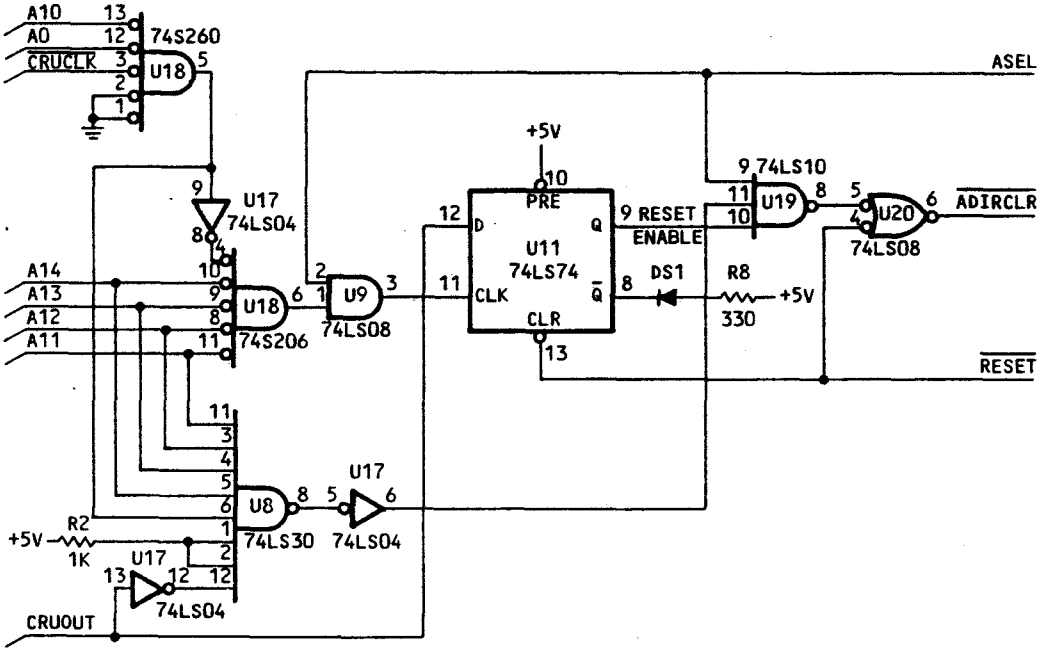



FIGURE 4-3. RESET LOGIC CIRCUIT

The output buffer enable circuitry is shown in Figure 4-4. This figure shows only the enable logic for Port A. The other two ports have identical counterparts of this circuit which can be found on schematic sheet 3 (page A-4).

The output buffer enable circuit was designed to simulate the programmable outputs of the TMS 9901. A port is an input until it has been written to. Once written to, the port becomes an output until reset.

When one of the 8 bit blocks of port A has been addressed, the output enable signal (ASELOUT) clocks a logic 1 into one of the flip-flops in Figure 4-4.

The outputs of the flip-flops make up the output buffer enable signals (ACTL). The value of these signals is determine by Jumper J9 and J10. When a jumper is connected from pin 1 to pin 2 of either jumper, ACTL.1 (or ACTL.3) will be active high. When a jumper is connected from pin 2 to pin 3 of either jumper, ACTL.1 (or ACTL.3) will be active low. Thus, the user may select the buffer enable signals required for different buffers (see Section 2.5.5).

When ADIRCLR- occurs from either a software or hardware reset, the flip-flops are cleared and the output buffers are disabled until written to again.

Switch S1-8, when closed, disables the output buffers of Port A, making Port A an input only.

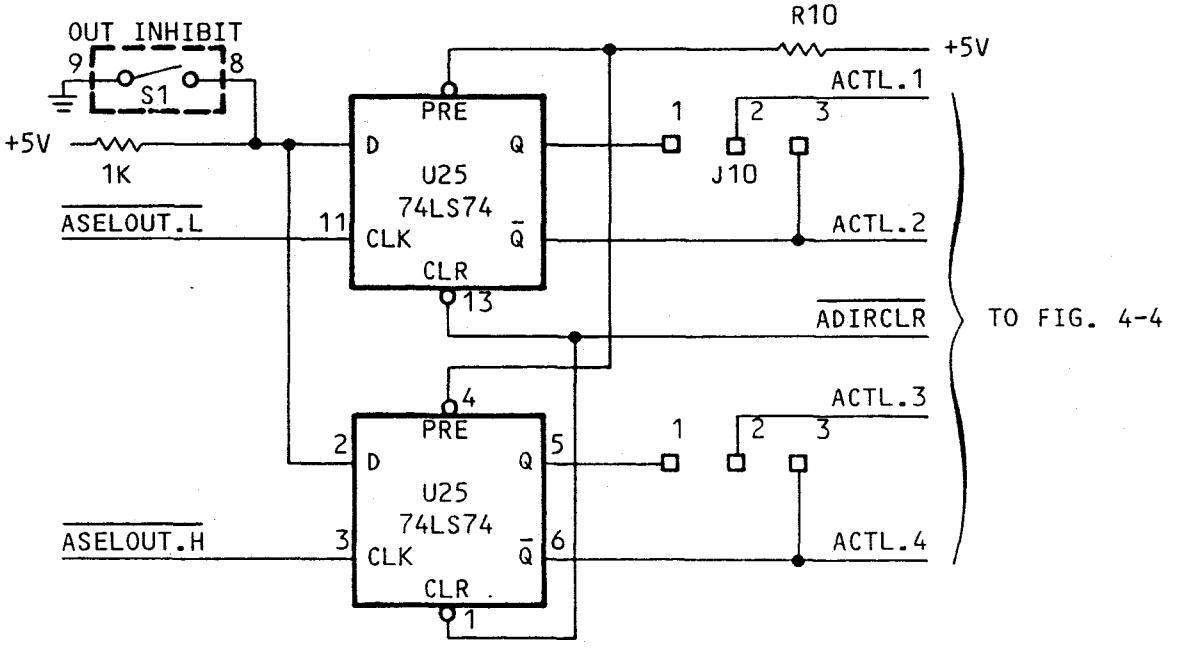



FIGURE 4-4. OUTPUT BUFFER ENABLE CIRCUIT

## 4.4 INPUT/OUTPUT LATCHES AND BUFFERS

The input and output buffers are shown in Figure 4-5. This figure shows only the circuit for Port A. The other two ports have identical counterparts of this circuit which can be found on schematic sheet 4 (page A-5).

The input selectors (U54 and U56 in Figure 4-5) have outputs (CRUIN) that are enabled by the appropriate ASELIN signal. The three least significant bits of the CRU address (A12, A13 and A14) select the input line that will be coupled to CRUIN.

The output latches (U36 and U38) are enabled by the appropriate ASELOUT signal. The three least significant bits of the CRU address select the output line (Q) that will be coupled to CRUOUT.

The output buffers (U35 and U37) are user selectable depending on the required output specifications (see Section 2.x). The buffers are enabled by the ACTL signals generated by the circuit in Figure 4-4.

The series resistors (U43 and U44) and the pull-up resistors (U53 and U55) are user selectable depending on the application (see section 2.8). Jumpers J15 and J16 are provided to set the resistors in U53 or U55 as pull-up or 'pull-down' resistors as needed.

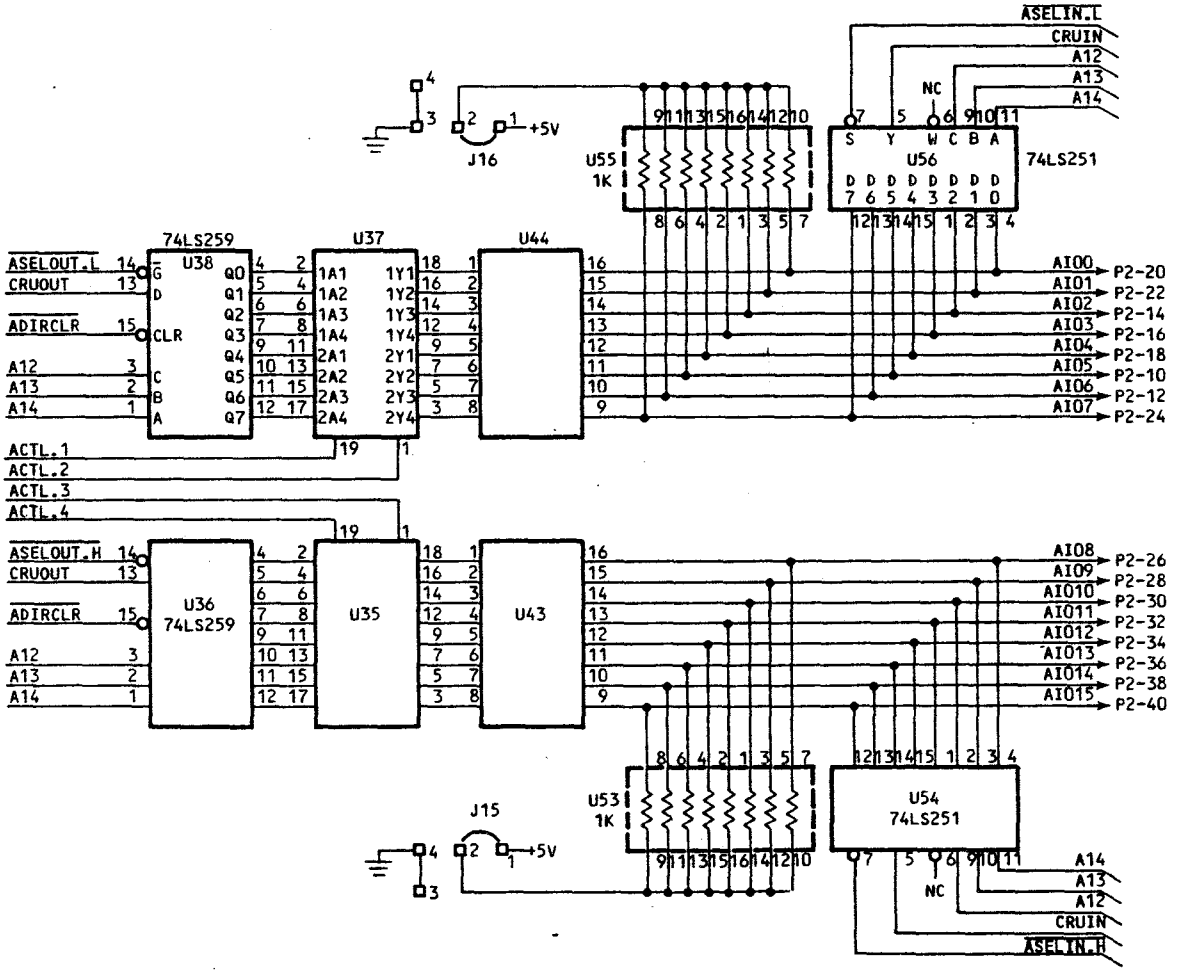



FIGURE 4-5. INPUT/OUTPUT LATCHES AND BUFFERS

## 4.5 FLAG REGISTER

The flag register (U6 in Figure 4-6) is a 1 bit wide RAM memory accessable by the user via the CRU. This circuit can be found on schematic sheet 3 (page A-4). The use of this register is determined by the user.

The least significant address lines and three control lines are buffered onto the module by U5.

Logic gates U16 and U17 (in Figure 4-6) generate the active low select signal for the flag register. When A10 is low and the CRU base address (A3 through A8) is true, U6 is selected.

The inputs to U6 labeled ASEL, BSEL and CSEL determine which one of three blocks of flags is addressed; thus, the same CRU base address for each of the ports select a unique block of flags. Each block of flags contain 32 bits. The values on address lines A9 and A11 through A14 determine which 1 of 32 bits in a block is addressed. The address map for the flag register is shown in Table 3-1.

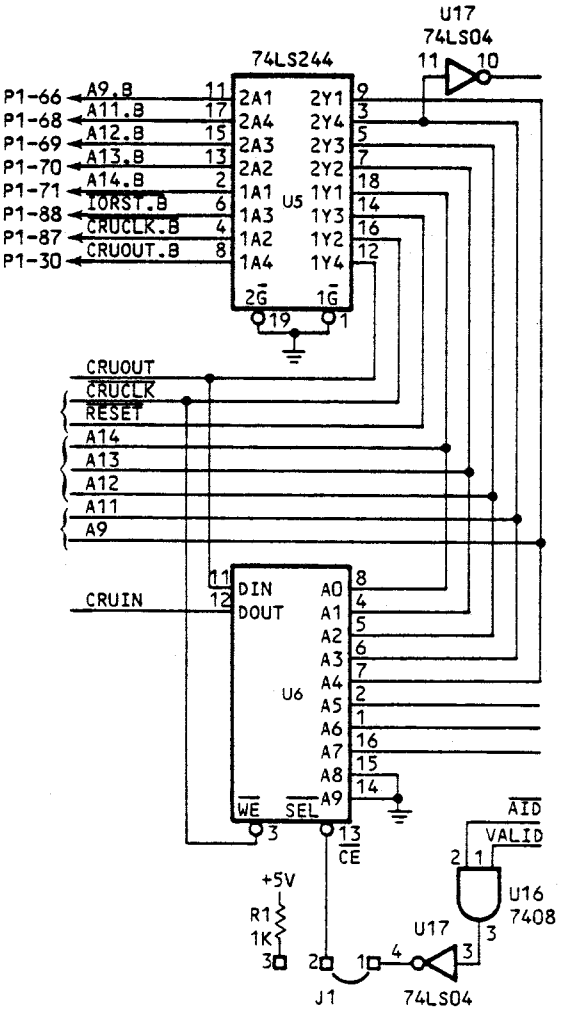



FIGURE 4-6. TM 990/311 FLAG REGISTER

## 4.6 VOLTAGE REGULATOR

The voltage regulator on the TM 990/311 is shown on schematic sheet 1 (page A-2). The primary purpose of the onboard regulator is to step the +12 V (derived from the backplane) down to + 8 V for compatibility with the 5MT series. This gives the user a choice of four voltages available at each port connector (+12 V, +8 V, +5 V and -12 V). The jumper settings required to select these voltages are described in section 2.5.

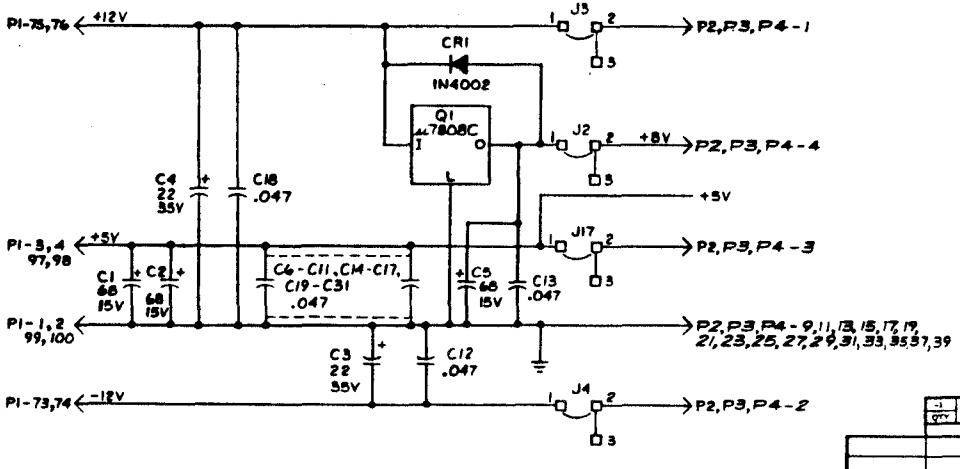
# APPENDIX A

# SCHEMATICS

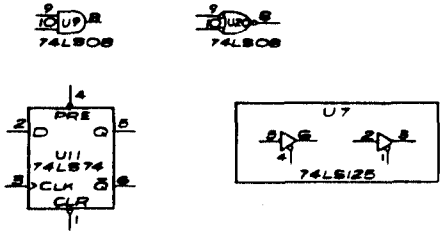
NOTES UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITANCE VALUES ARE IN MICROFARADS
2. ALL RESISTANCE VALUES ARE IN OHMS
3. ALL RESISTORS ARE .25W, 5%
4. FUTURE OPTION
5. RESISTOR VALUE MAY RANGE FROM 100 TO 10K OHMS FOR U57, U58 & U59

| REFERENCE DESIGNATORS | |
|---|---|
| USED | NOT USED |
| P1-P4 | |
| J1-J16 | |
| DS1-DS3 | |
| CR1 | |
| C1-C31 | |
| G | |
| S1-S3 | |
| R1-R10 | |
| U1-U59 | |




SPARES




| ITEM NO | QTY | PART OR IDENTIFYING NUMBER | NOMENCLATURE OR DESCRIPTION | PROCUREMENT SPECIFICATION | NOTES |
|---|---|---|---|---|---|
| | | | PARTS LIST | | |
| | | 1600181 | 8117 | | |
| | | 1600182 | 8117 | | |

UNLESS OTHERWISE SPECIFIED:
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±1°; 3 PLACE DECIMALS ± .010; 2 PLACE DECIMALS ± .02
- INTERPRET DRAWING PER MIL-D-1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY: MACHINED DIAMETERS .010 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSING
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

| .XXX ±.005 | .125 ±.005 | .250 ±.005 |
|---|---|---|
| YIELD: .139 | YIELD: .250 | YIELD: .500 |
| .XXX ±.001 | .XXX ±.001 | .XXX ±.001 |
| .501 ±.005 | .751 ±.010 | 1.251 ±.017 |
| YIELD: .750 | YIELD: 1.000 | YIELD: 2.000 |
| .XXX ±.001 | .XXX ±.001 | .XXX ±.001 |

| NEXT ASSY | USED ON |
|---|---|
| APPLICATION | |

| SEQ NO | IDENT | P SPEC | NO | ADDITIONAL | NOTES |
|---|---|---|---|---|---|
| | PROCESS | | CLASSIFICATION | | |

PROCESSES — FOR CORRELATION TO SOVT/IND SPECIFICATIONS SEE TI DRAWING 729447

| REV STATUS OF SHEETS | REV | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|
| | SH | | | | | |

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |

| | | | |
|---|---|---|---|
| Engr | J. Humphrey | 1-29-80 | |
| Mfg | Wm Hewett | 12-2-80 | |
| Prog | | | |
| QA | | 12/3/80 | |
| Mfg | | 12/3/80 | |
| Mfg | | 12/5/80 | |

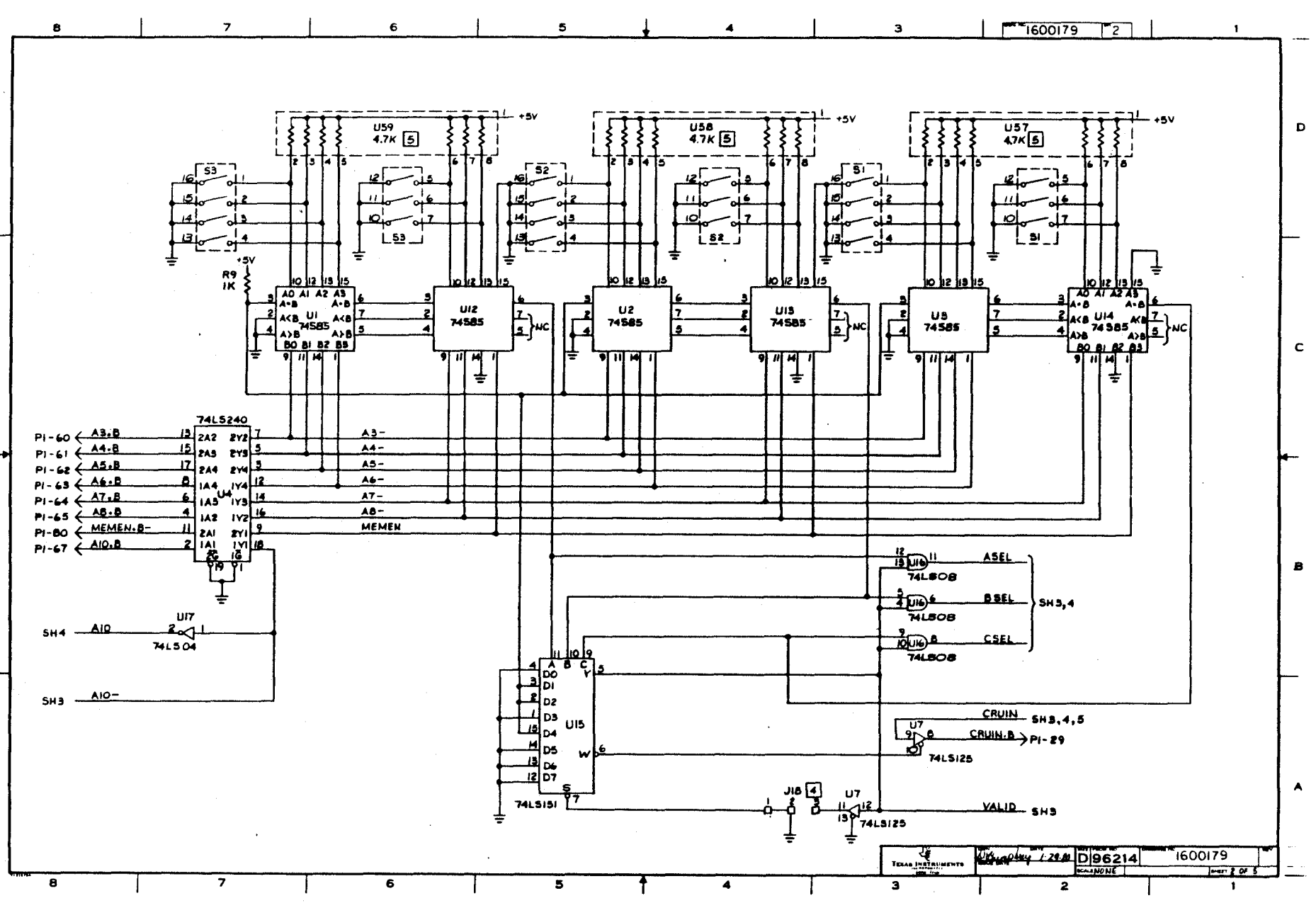
TEXAS INSTRUMENTS INCORPORATED, Dallas, Texas

DIAGRAM, LOGIC
TM990/311

| SIZE | FSCM NO | DRAWING NO |
|---|---|---|
| D | 96214 | 1600179 |

SCALE NONE SHEET 1 OF 5

A-2


1600179
2
U59 4.7K 5
U58 4.7K 5
U57 4.7K 5
+5V
S3
S2
S1
R9 1K
U1 74585
U12 74585
U2 74585
U13 74585
U8 74585
U14 74585
NC
74LS240
U4
PI-60 A3.B
PI-61 A4.B
PI-62 A5.B
PI-63 A6.B
PI-64 A7.B
PI-65 A8.B
PI-80 MEMEN.B-
PI-67 A10.B
A3-
A4-
A5-
A6-
A7-
A8-
MEMEN
U17
74LS04
SH4 A10
SH3 A10-
U16
74LS08
ASEL
BSEL
CSEL
SH3,4
U15
74LS151
U7
74LS125
CRUIN
SH3,4,5
CRUIN.B
PI-29
J18 4
VALID
SH3
TEXAS INSTRUMENTS
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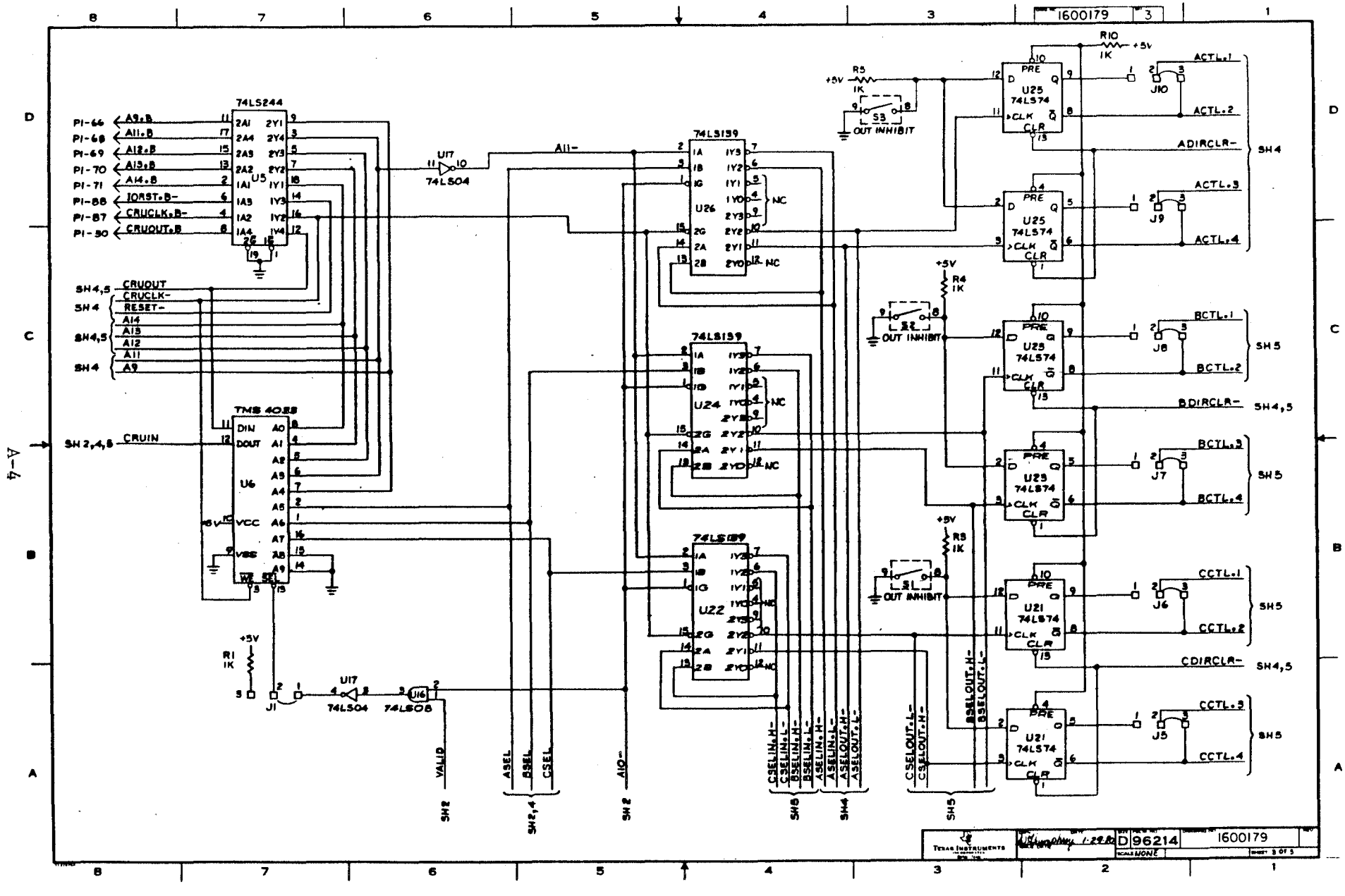
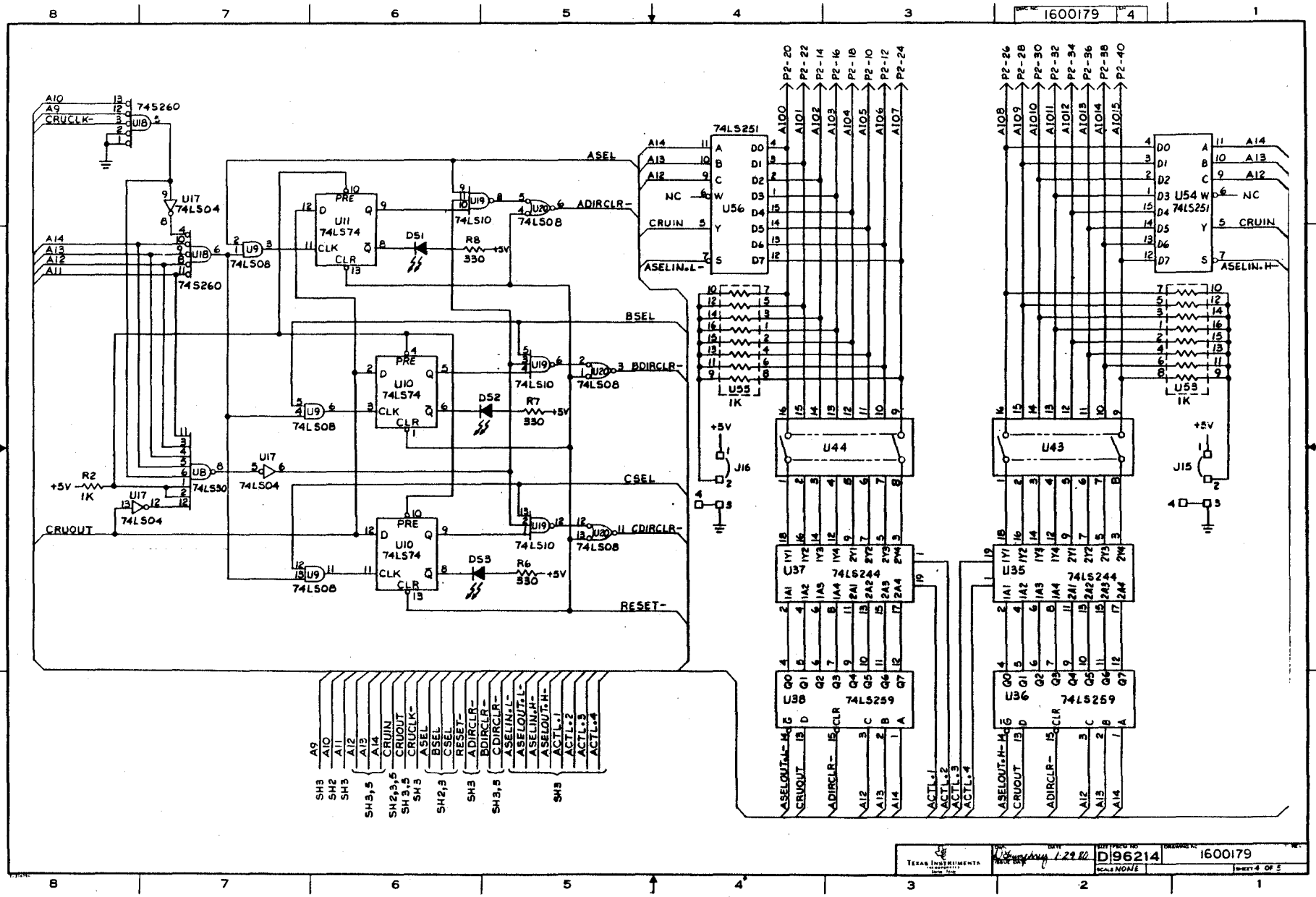
1600179
SCALE NONE
SHEET 2 OF 5

A-3


1600179
3
74LS244
U5
PI-66
PI-68
PI-69
PI-70
PI-71
PI-88
PI-87
PI-90
A9.B
A11.B
A12.B
A13.B
A14.B
IORST.B-
CRUCLK.B-
CRUOUT.B
SH4,5 CRUOUT
CRUCLK-
SH4 RESET-
A14
SH4,5 A15
A12
A11
SH4 A9
TMS 4044
U6
SH2,4,5 CRUIN
DIN
DOUT
VCC
VSS
WE
SEL
+5V
R1
1K
J1
U17
74LS04
U16
74LS08
VALID
SH2
ASEL
BSEL
CSEL
SH2,4
A11-
A10-
SH2
74LS139
U26
U24
U22
NC
CSELIN.H-
CSELIN.L-
BSELIN.H-
BSELIN.L-
ASELIN.H-
ASELIN.L-
ASELOUT.H-
ASELOUT.L-
SH5
SH4
CSELOUT.L-
CSELOUT.H-
BSELOUT.H-
BSELOUT.L-
SH5
R10
1K
+5V
R5
1K
S3
OUT INHIBIT
R4
1K
S2
OUT INHIBIT
R3
1K
S1
OUT INHIBIT
U25
74LS74
U21
74LS74
PRE
CLK
CLR
ACTL.1
ACTL.2
ADIRCLR-
ACTL.3
ACTL.4
SH4
BCTL.1
BCTL.2
BDIRCLR-
SH4,5
BCTL.3
BCTL.4
SH5
CCTL.1
CCTL.2
CDIRCLR-
SH4,5
CCTL.3
CCTL.4
SH5
J10
J9
J8
J7
J6
J5
A-4
Texas Instruments
D 96214
1600179
SHEET 3 OF 5


1600179 4
A10
A9
CRUCLK-
74S260
U18
U17
74LS04
A14
A13
A12
A11
74S260
U18
R2
+5V
1K
U17
74LS04
CRUOUT
U17
74LS04
U8
74LS30
U9
74LS08
U11
74LS74
PRE
D
CLK
CLR
Q
U19
74LS10
U20
74LS08
D51
R8
330
+5V
ASEL
ADIRCLR-
U10
74LS74
D52
R7
330
BSEL
BDIRCLR-
U10
74LS74
D53
R6
330
CSEL
CDIRCLR-
RESET-
74LS251
U56
A
B
C
W
Y
S
D0
D1
D2
D3
D4
D5
D6
D7
NC
CRUIN
ASELIN.L-
A100
A101
A102
A103
A104
A105
A106
A107
U55
1K
+5V
J16
U44
U37
74LS244
U38
74LS259
P2-20
P2-22
P2-14
P2-16
P2-18
P2-10
P2-12
P2-24
A108
A109
A1010
A1011
A1012
A1013
A1014
A1015
U54
74LS251
U59
1K
J15
U43
U35
74LS244
U36
74LS259
A14
A13
A12
NC
CRUIN
ASELIN.H-
SH3
SH2
SH3
SH3,5
SH2,3,5
SH3,5
SH3
SH2,3
SH3
SH3,5
SH3
A9
A10
A11
A12
A13
A14
CRUIN
CRUOUT
CRUCLK-
ASEL
BSEL
CSEL
RESET-
ADIRCLR-
BDIRCLR-
CDIRCLR-
ASELIN.L-
ASELOUT.L-
ASELIN.H-
ASELOUT.H-
ACT.1
ACT.2
ACT.3
ACT.4
ACT.5
ACT.6
ASELOUT.L-
CRUOUT
ADIRCLR-
A12
A13
A14
ACT.1
ACT.2
ACT.3
ACT.4
ASELOUT.H-
CRUOUT
ADIRCLR-
A12
A13
A14
TEXAS INSTRUMENTS
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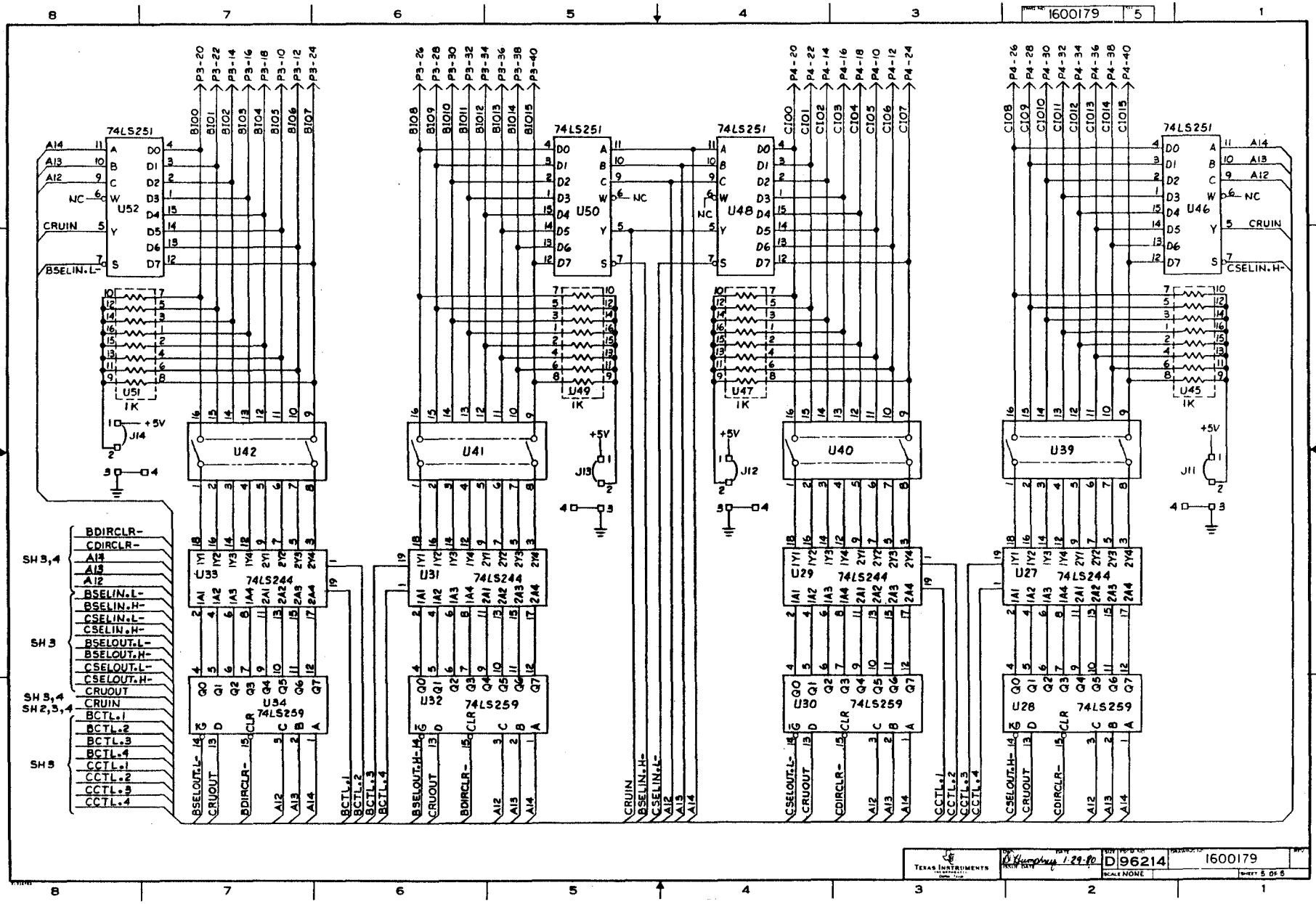
1600179
SHEET 4 OF 5
A-5


1600179
5
74LS251
U52
U50
U48
U46
74LS244
U33
U31
U29
U27
74LS259
U34
U32
U30
U28
U51
U49
U47
U45
1K
U42
U41
U40
U39
J14
J13
J12
J11
+5V
NC
CRUIN
BSELIN.L-
CSELIN.H-
BDIRCLR-
CDIRCLR-
SH 3,4
SH 3
SH 2,3,4
SH 3
BSELOUT.L-
BSELOUT.H-
CSELOUT.L-
CSELOUT.H-
CRUOUT
BCTL.1
BCTL.2
BCTL.3
BCTL.4
CCTL.1
CCTL.2
CCTL.3
CCTL.4
D96214
1600179
SCALE NONE
SHEET 5 OF 5

APPENDIX B

PARTS LIST

| Symbol | Description |
|---|---|
| C1 - C2 | Capacitor, Fixed, 68 MFD, 10 %, 15 V |
| C3 - C4 | Capacitor, Fixed, 22 MFD, 10 %, 35 V |
| C5 | Capacitor, Fixed, 68 MFD, 10 %, 15 V |
| C5 - C31 | Capacitor, Fixed, .047 uF, +80 %, -20% |
| CR1 | Diode, 1N4002, 1 Amp, 100 PIV Rectifier |
| DS1 - DS3 | Diode, LED |
| J1 - J17 | Jumper Plug, Connector |
| Q1 | IC, Pos Volt Reg, UA7808C |
| R1 - R5 | Resistor, Fixed, 1.0 kilohm, .25 W |
| R6 - R8 | Resistor, Fixed, 330 ohm, .25 W |
| R9 - R10 | Resistor, Fixed, 1.0 kilohm, .25 W |
| S1 - S3 | Jumper Plug, 8-section, DIP |
| U04 | IC, SN74LS240N, Line Drivers |
| U05 | IC, SN74LS244N Line Driver |
| U06 | IC, TMS 4033, Static Ram Memory |
| U07 | IC, SN74LS125N |
| U08 | Network, SN74LS30N |
| U9 | Network, SN74LS08N |
| U1 - U3 | Network, SN74S85N |
| U10 - U11 | Network, SN74LS74N |
| U12 - U14 | Network, SN74S85N |
| U15 | Network, SN74LS151N |
| U16 | Network, SN74LS08N |
| U17 | Network, SN74LS04N |
| U18 | Network, SN74S260N |
| U19 | Network, SN74LS10N |
| U20 | Network, SN74LS08N |
| U21 | Network, SN74LS74N |
| U22 | Network, SN74LS139N |
| U23 | Network, SN74LS74N |
| U24 | Network, SN74LS139N |
| U25 | Network, SN74LS74N |
| U26 | Network, SN74LS139N |
| U27 | IC, SN74LS244N Line Driver |
| U28 | IC, SN74LS259N |
| U29 | IC, SN74LS244N Line Driver |
| U30 | IC, SN74LS259N |
| U31 | IC, SN74LS244N Line Driver |
| U32 | IC, SN74LS259N |
| U33 | IC, SN74LS244N Line Driver |
| U34 | IC, SN74LS259N |
| U35 | IC, SN74LS244N Line Driver |
| U36 | IC, SN74LS259N |
| U37 | IC, SN74LS244N Line Driver |
| U38 | IC, SN74LS259N |
| U39 - U44 | Jumper Plug, 8-section, DIP |
| U45 | Resistor, Fixed-Array, 4.7 kilohm |
| U46 | Network, SN74LS251N |
| U47 | Resistor, Fixed-Array, 4.7 kilohm |

| Symbol | Description |
|---|---|
| U48 | Network, SN74LS251N |
| U49 | Resistor, Fixed-Array, 4.7 kilohm |
| U50 | Network, SN74LS251N |
| U51 | Resistor, Fixed-Array, 4.7 kilohm |
| U52 | Network, SN74LS251N |
| U53 | Resistor, Fixed-Array, 4.7 kilohm |
| U54 | Network, SN74LS251N |
| U55 | Resistor, Fixed-Array, 4.7 kilohm |
| U56 | Network, SN74LS251N |
| U57 - U59 | Network Resistor, 4700 ohms |

# INDEX