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TEXAS INSTRUMENTS

TM 990

TM 990/E351 Output Module

MICROPROCESSOR SERIES

August 1980

IMPORTANT NOTICES

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SECTION 1

INTRODUCTION

1.1 GENERAL

The TM 990/E351 is an opto-isolated dc power output module for use with the TM 990/E150 CPU module. The module uses the small, low-cost 100 X 160 mm board format (see Figure 1-1) and can provide direct drive for up to eight loads. The loads may be relays, lamps, motors, or other control elements that operate in systems using up to 30 Vdc. . Each port can sink up to 1.2 A. Each port can handle a peak current up to 5A with a pulse width of less than 10 milliseconds and a duty cycle of less than 10 percent. Other features include:

- Compatible with TM 990/E150 CPU module
- Dual watchdog timer for failsafe operation against improper program sequence
- Echo back feature at each port for software testability and output data verification during program execution
- Easy, low-cost, high reliability I/O connection through DIN41612, Form F, front connector
- DIN41612, Form C, backplane connector
- Small, low-cost 100 X 160 mm board format
- Eight-bit dip switch for data input of a data constant

Principal TM 990/E351 components are shown in Figure 1-2. A block diagram for the TM 990/E351 is given in Figure 1-3.

1.2 MANUAL ORGANIZATION

This manual is organized as follows:

- Section 1 covers module characteristics and specifications
- Section 2 shows how to install, power-up, and operate the TM 990/E351
- Section 3 covers the programming aspects of the module
- Section 4 covers the theory of operation with circuit descriptions keyed to schematic diagrams.

1.3 GENERAL SPECIFICATIONS

- Power Requirements:

Voltage	Regulation	Current TYP	Current MAX
+5V	±3%	0.4 A	0.55 A

- Operating Temperature: 0° C to 70° C
- Storage Temperature: -40° C to 80° C

- Humidity: 0 - 95% non-condensing
- Module Dimensions: See Figure 1-1.

1.4 PRODUCT INDEX

The TM 990/E351 is available in two different configurations. These configurations are listed in Table 1-1.

TABLE 1-1. TM 990/E351 CONFIGURATIONS

*MODEL	DESCRIPTION
TM 990/E351-1	TM 990/E351 shipped with on-board DIP switch, watchdog timer, and user's manual.
TM 990/E351-2	TM 990/E351 shipped without on-board DIP switch, watchdog timer, and user's manual.

1.5 APPLICABLE DOCUMENTS

The following is a list of documents that provide supplementary information for the TM 990/E351 user.

- TMS 9901 Programmable Systems Interface
- The Optoelectronics Data Book (Texas Instuments)
- The TTL Data Book (Texas Instruments)

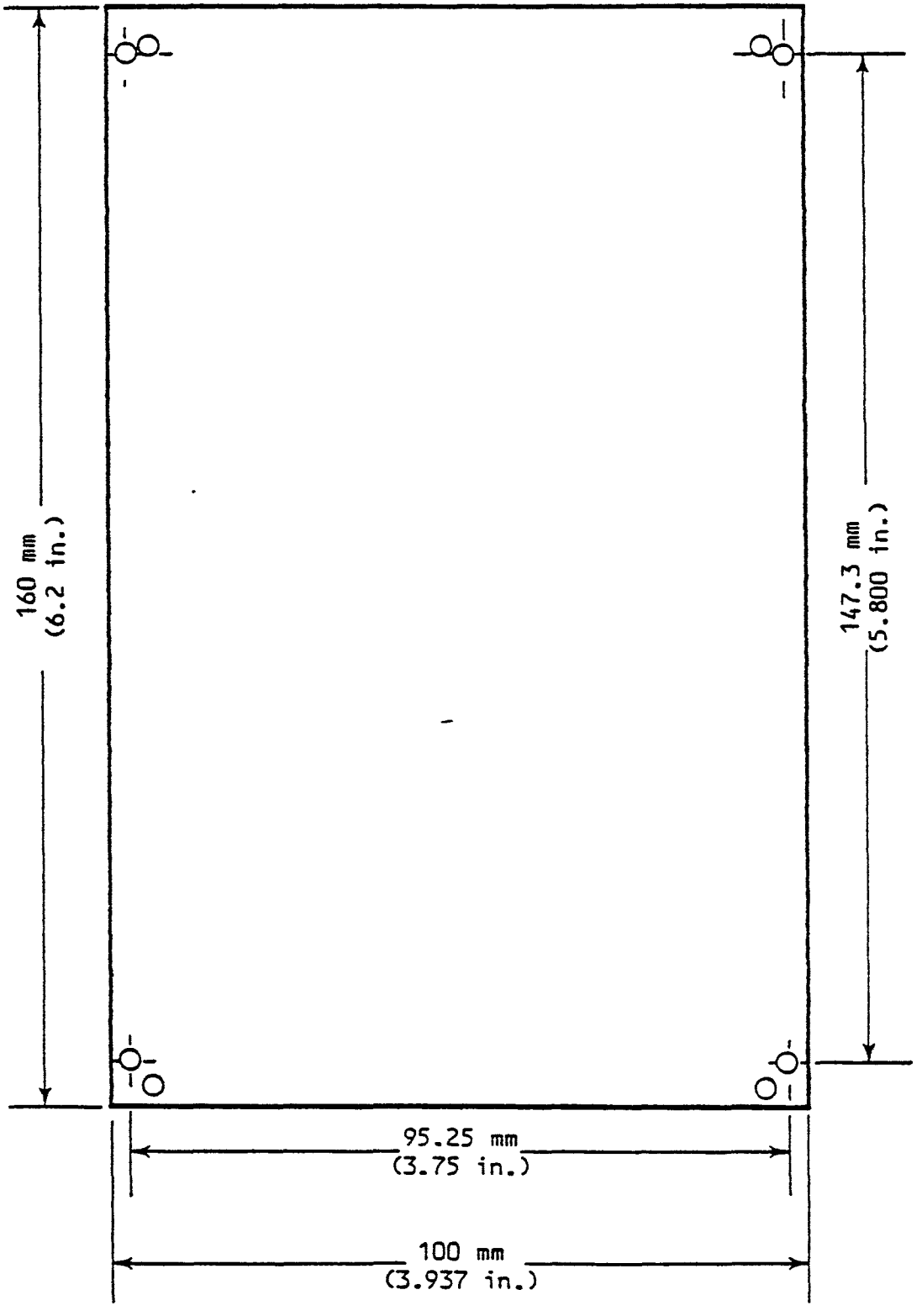


FIGURE 1-1. TM 990/E351 MODULE DIMENSIONS

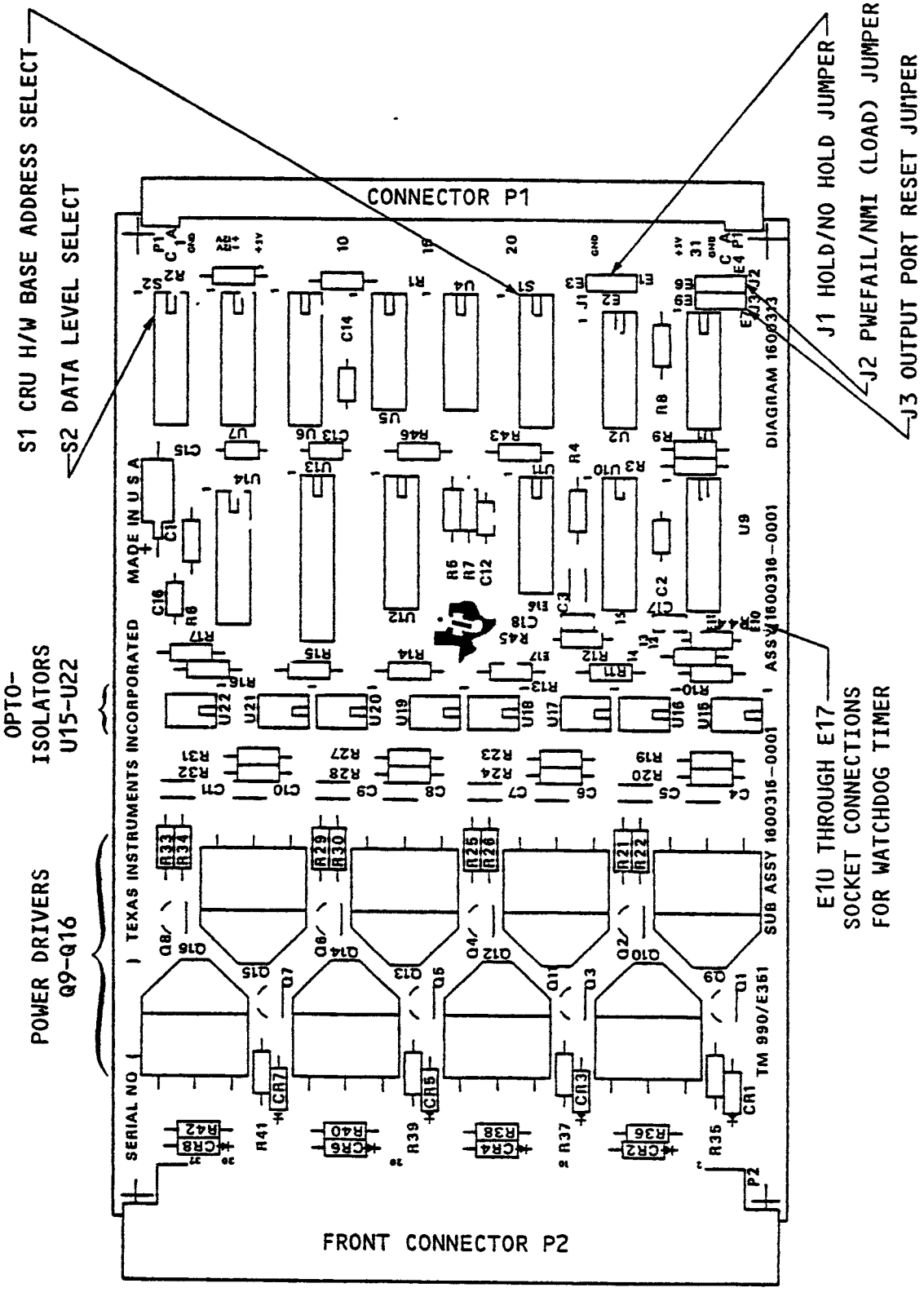


FIGURE 1-2. TM 990/E351 PRINCIPAL COMPONENTS

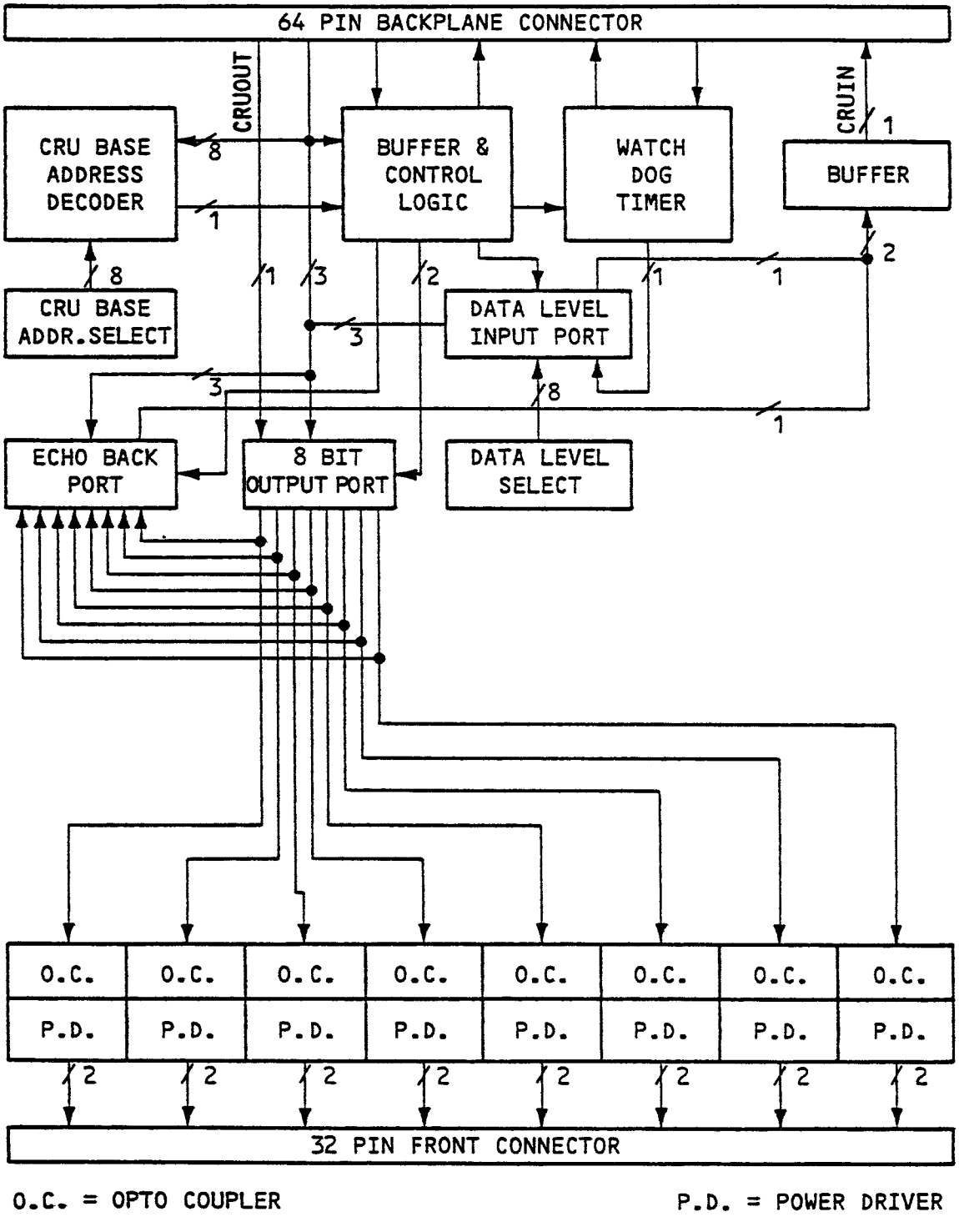


FIGURE 1-3. TM 990/E351 BLOCK DIAGRAM

SECTION 2

INSTALLATION AND OPERATION

2.1 GENERAL

The procedures for unpacking and setting up the TM 990/E351 module for operation are given in this section along with a test routine that can be used to check out the module.

2.2 UNPACKING AND INSPECTION

Remove the TM 990/E351 from its carton and discard any protective wrapping. Inspect the module for any damage that might have occurred in shipping. Report any damage to your TI supplier.

2.3 JUMPER/SWITCH POSITIONS

2.3.1 CRU Base Address Selection

The TM 990/E351 output ports can be assigned a unique CRU base address. Either an 8-position socket platform or an 8-position DIP switch (S1) is provided for this CRU base address selection. If S1 is a socket platform, the user has the option of using jumpers or inserting a DIP switch in the socket.

If the socket platform is used, jumpers at S1-8 to S1-1 are inserted to indicate a zero; sockets left unjumpered will be high. If a DIP switch is used, switch settings are ON = zero, OFF = one. Comparator circuitry compares the jumper/switch values with values found on bus address lines A3 (S1-8) to A10 (S1-1). The first address that is available is 0000_{16}. Addresses that are available follow in steps of 16_{10} (10_{16}). The jumper/switch positions for selecting a specific CRU hardware base address are given in Table 2-1.

TABLE 2-1. CRU BASE ADDRESS SELECTED

S1-8 A3	S1-7 A4	S1-6 A5	S1-5 A6	S1-4 A7	S1-3 A8	S1-2 A9	S1-1 A10	CRU HARDWARE BASE ADDRESS		SOFTWARE BASE ADDR
								(DEC)	(HEX)	(HEX)
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	16	10	20
0	0	0	0	0	0	1	0	32	20	40
0	0	0	0	0	0	1	1	48	30	60
0	0	0	0	0	1	0	0	64	40	80
0	0	0	0	0	1	0	1	80	50	A0
0	0	0	0	0	1	1	0	96	60	C0
0	0	0	0	0	1	1	1	112	70	E0
					•					
					•					
					•					
0	1	1	1	1	1	1	1	2032	7F0	FE0
					•					
					•					
					•					
1	1	1	1	1	1	1	1	4080	FF0	1FE0

0 = Jumpered or ON, 1 = Unjumpered or OFF

The following procedure can be used to determine the jumper/switch positions for a CRU base address that is not given in Table 2-1.

1) Convert the 3 most significant hex digits of the CRU hardware base address into their binary equivalents.

2) Convert the 8 least significant bits of the binary equivalents into ON/OFF equivalents to determine the jumper/switch positions for S1-1 through S1-8. The following jumper/switch definitions apply: 0 = Jumpered or ON, 1 = Unjumpered or OFF.

EXAMPLE: Determine the jumper/switch (S1) positions that are required to select CRU hardware base address 2032_{10} ($07F0_{16}$).

SOLUTION:

1) 0 7 F 0
    0000 0111 1111

2)

	0	1	1	1	1	1	1	1
	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
	S1-8 ←			Through				→ S1-1

2.3.2 Constant Data Input

An 8-position jumper platform is provided for inputting constants such as parameters or station numbers during program execution. A 74LS251 data selector/multiplexer decodes address lines A12-A14 and provides an output that is determined by the positions of S2-1 (LSB) through S2-8 (MSB). The user may insert an 8-position DIP switch in this platform. The values are as follows;

0 = Jumpered or ON, 1 = Unjumpered or OFF

2.3.3 Watchdog Timer Options (Jumpers J1, J2, and J3)

The TM 990/E351 is protected by a watchdog timer. This timer starts counting down at system reset (IORST- active) or when reset via the CRU (this is covered in detail in Section 3, Programming). Its length of countdown time is dependent upon the impedance circuitry connected to the two 74LS123 retriggerable monostable multivibrators that provide the countdown. This impedance is hardware programmable by the size of the capacitance and resistance inserted at pins E10 through E17. A data sheet and application sheet on the 74LS123 is provided in Appendix C. It includes formulae on customizing countdown time. As shipped at the factory, there are two countdown periods, one followed by another:

- First time period: 20 milliseconds
- Second time period: 10 milliseconds

A countdown can be avoided by resetting the watchdog timer via the Commuication Register Unit (CRU) by writing to a displacement of 8 from the hardware base address as covered in Section 3.

The effect of countdown on the system is determined by jumpers as explained in the following paragraphs.

2.3.3.1 First Timeout Jumpers (J2 and J3). The first timeout period occurs approximately 20 milliseconds after the timer is set. This countdown causes the following actions depending upon the jumpers set by the user:

- Output ports can be set to the open state (RESET, jumper J3):

  . E8-E7: Reset output ports to open state

  . E8-E9: Do not reset output ports to open state

NOTE

Jumper J3 should not be left unconnected. Choose one of the two options above.

- Optionally and at the same timeout, a context switch can be caused to handle the timeout (NMI*, PWRFAIL, jumper J2):

  . E5-E6: Powerfail indicated on connector pin P1-A24 (causes interrupt INT1 at TM 990/E150 microcomputer, vectors at 0004_{16} for WP and . 0006_{16} for PC)

  . E5-E4: Causes context switch to NMI* (non-maskable interrupt) vectors in upper memory via pin P1-C04 (vectors at $3FFC_{16}$ for WP and $3FFE_{16}$ for PC at TM 990/E150)

  . E4/E5/E6 without jumper: No signal sent to CPU

*NOTE

NMI is the same as the LOAD interrupt (vectors in upper memory).

2.3.3.2 Second Timeout Jumper (J1). The second timeout occurs approximately 10 milliseconds after the first timeout. The following occur depending upon the jumper settings:

- E2-E1: System placed in hold mode by GRANTOUT line on system bus being pulled low (it is necssary that the GRANTIN/GRANTOUT jumper on the backplane be removed).

- E2-E3: No hold state issued.

NOTE

Do not leave jumper J1 unjumpered. Pick one of the two options shown above. If unjumpered, bus arbitration circuitry using GRANTIN and GRANTOUT can be impaired.

2.3.3.3 Polling CRU for Second Timeout. The CRU can be used to poll for issuance of the second timeout. To do this, poll jumper/switch S2-1 as described in Section 3. It is mandatory that jumper/switch S2-1 be in the OFF position for this feature. A one sensed at S2-1 indicates no timeout; a zero indicates a timeout.

2.4 FRONT CONNECTOR P2

See section 3.2 for a description of the front connector (P2) and pin assignments. There are eight possible ports on the TM 990/E351. Each port is divided into a + side and a - side. The purpose of each port is to complete or break the circuit connected to the + side and the -side under software control.

Each port can used to control a circuit operating up to 30 V. The circuit must not exceed 1.2 A continuous current and 5 A peak current.

Two or more ports may be connected together to carry higher currents. If two ports are coupled to the same controlled circuit, then only the LDCR instruction should be used to access the coupled ports. If two SBO instructions are used to access the coupled ports and an interrupt occurs after the execution of the first SBO instruction, then an overload of one of the coupled ports could occur.

Each side of each port (i.e. P0+) is assigned two pins (see Section 3.2). Thus there are 4 pins for each port, two for the negative side and two for the positive side. Both pins of the same polarity on the same port must be connected in parallel to the line being controlled. This decreases the effective resistance of the connection.

For example, Figure 2-1 shows Port 0 controlling a 24 V relay.

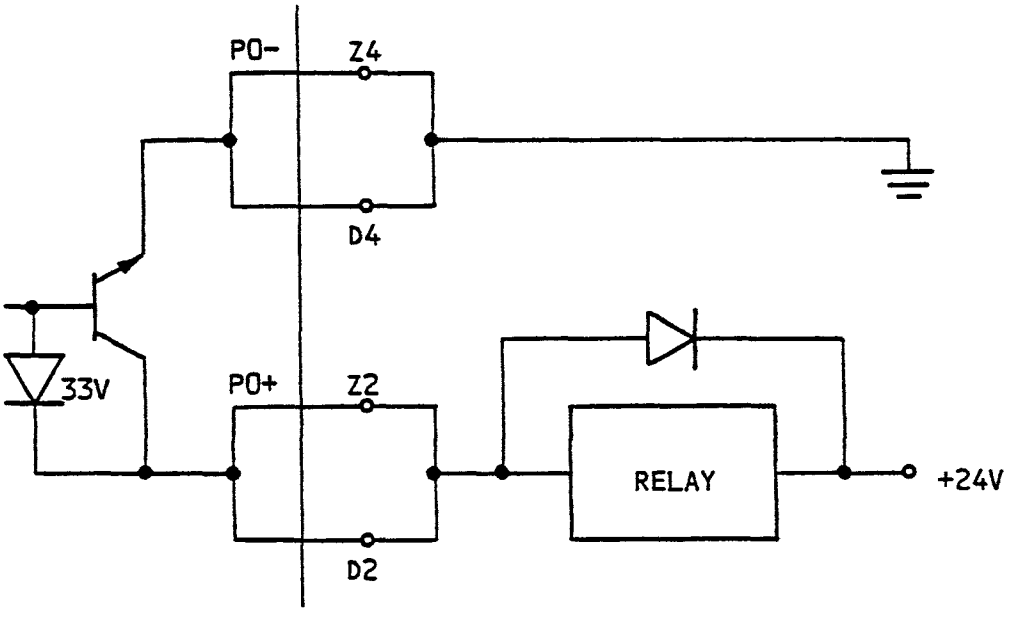


FIGURE 2-1. EXAMPLE OF PORT 0 CONTROLLING A 24 V RELAY

SECTION 3

PROGRAMMING

3.1 GENERAL

This section describes how to use the Communications Register Unit (CRU) to do the following:

- Write to one of eight output ports
- Set the watchdog timer
- Read Data Level
- Clear the output latches
- Read Echo Back

The reader should be familiar with the various jumper options as explained in Section 2.

3.2 OUTPUT PORTS AT FRONT CONNECTOR P2

The 32 pins at front connector P2 are grouped as shown in Table 3-1. Pins on the Z row and D row of the same pin number (i.e. Z2 and D2) are connected in parallel to the same line. This decreases the effective impedence of the connector pins.

The pin pairs are also designated as either the + side or the -side of a given port number (i.e. Z2/D2 = + side of P0, Z4/D4 = - side of P0). When a logical 1 is written to Port 0 (P0) using a CRU instruction, pins Z2/D2 are effectively coupled to Z4/D4, closing the circuit. The same is true for the other ports and the circuits connected to them. When a logical 0 is written to a port, the circuit connected to that port is effectively opened.

Figure 3-1 shows the front connector and the port designations for the appropriate pins.

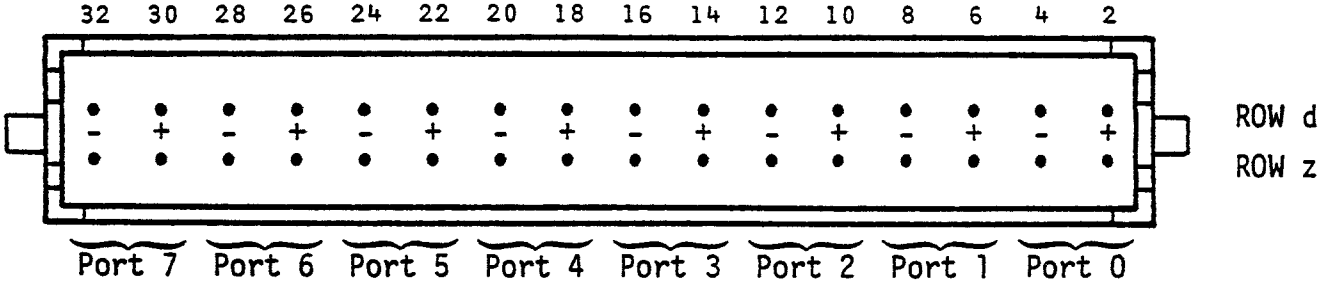


FIGURE 3-1. OUTPUT PORTS AT FRONT CONNECTOR P2

TABLE 3-1. FRONT CONNECTOR P2 PIN ASSIGNMENTS

Pins	Output Port	Pins	Output Port
Z2/D2	P0+	Z4/D4	P0-
Z6/D6	P1+	Z8/D8	P1-
Z10/D10	P2+	Z12/D12	P2-
Z14/D14	P3+	Z16/D16	P3-
Z18/D18	P4+	Z20/D20	P4-
Z22/D22	P5+	Z24/D24	P5-
Z26/D26	P6+	Z28/D28	P6-
Z30/D30	P7+	Z32/D32	P7-

3.3 CRU BASE ADDRESS NOMENCLATURE

The following are definitions of CRU address nomenclature. These are shown in Figure 3-2.

- CRU Hardware Base Address: Bits 3 through 14 of register 12 with bits 0 through 2 and 15 being zeros. Bits 3 through 14 of R12 are applied to bus address bits A3 to A14 (plus signed displacement -- see Hardware Bit Address below).

- CRU Hardware Bit Address: Final address bus value (with A14 as LSB, A3 as MSB) at execution of the CRU instruction. This includes the CRU Hardware Base Address (see below) and the signed 8-bit displacement of the single-bit CRU instruction (SBO, SBZ, and TB), or the resulting CRU bit addressed by a CRU mulitibit instruction (LDCR or STCR).

- CRU Software Base Address: Entire contents of register 12.

For a complete discussion of CRU addressing, see Section 5 of "TM 990/E150 Microcomputer User's Guide".

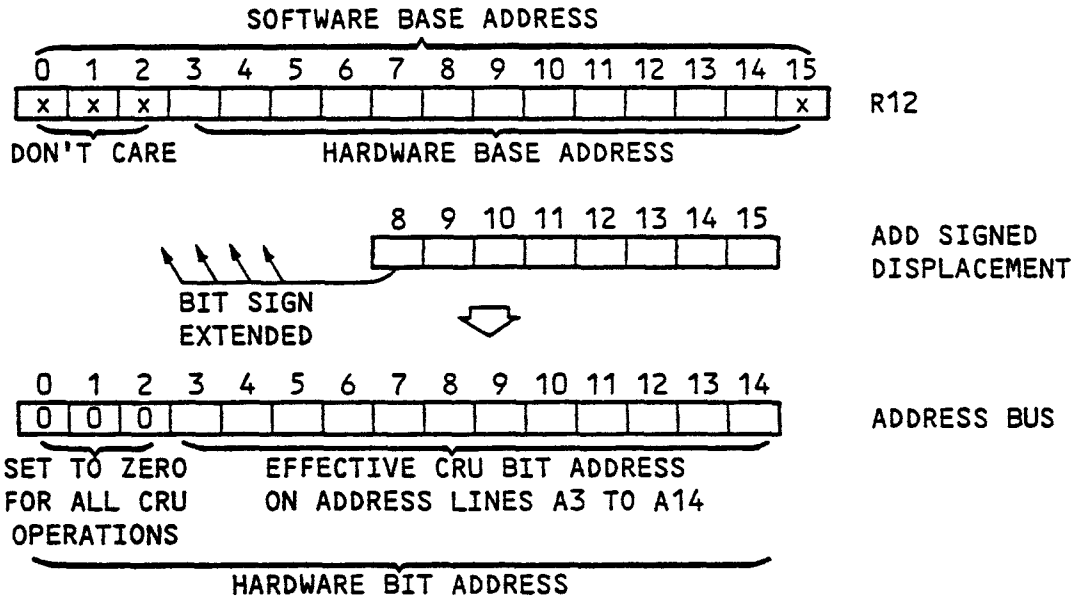


FIGURE 3-2. CRU ADDRESSING NOMENCLATURE

3.4 SELECTING MOST SIGNIFICANT BITS OF CRU HARDWARE BASE ADDRESS

Bus address lines A3 through A10 contain the module select address. These lines are compared to jumper/switch S1. Only CRU instructions with a CRU hardware address corresponding to S1 settings will be executed on this particular module. This allows several TM 990/E351 modules to be used in a system; each addressable through unique switch-selectable CRU addresses.

3.5 SELECTING CRU FUNCTIONS

Table 3-2 lists the CRU functions on the TM 990/E351 module. A software base address of 0100_{16} is used as an example. The column in Table 3-2 labeled EXAMPLE SFTWR ADDRESS represents the example software base address plus the displacement necessary to select the desired function.

The column in Table 3-2 labeled HARDWARE DISPLACEMENT represents the displacement from the hardware base address to select the desired output port or function. This can be used as the displacement in single-bit CRU instructions (SBO, SBZ, TB).

There are eight CRU addressable output ports on the TM 990/E351 module. These ports are selected via address lines A12 through A14 (three LSBs of the hardware base address).

A11 is used as a function select control line . When A11 is low during a CRU output instruction (i.e. LDCR, SBO, SBZ), the programmer can write to one of the eight output ports. When A11 is high, one of the auxillary functions is selected. Notice that when A11 is high during an output function, A13 and A14 are ignored.

For an example of CRU addressing on the TM 990/E351 refer to Figure 3-3. Assume that S1 is set for a hardware address of 0080_{16}. Then R12 is loaded with a software address of two times 0080_{16} or 0100_{16}.

TABLE 3-2. CRU FUNCTION ADDRESSING

INPUT FUNCTION (STCR,TB)	OUTPUT FUNCTION (LDCR,SBO,SBZ)	HARDWARE DISPLACEMENT	EXAMPLE SFTWR ADDRESS*	CRU HARDWARE BIT ADDRESS (R12) 11	12	13	14
Read Echo Back	Close Switch AT						
Port 0	Port 0	00	0100	0	0	0	0
Port 1	Port 1	01	0102	0	0	0	1
Port 2	Port 2	02	0104	0	0	1	0
Port 3	Port 3	03	0106	0	0	1	1
Port 4	Port 4	04	0108	0	1	0	0
Port 5	Port 5	05	010A	0	1	0	1
Port 6	Port 6	06	010C	0	1	1	0
Port 7	Port 7	07	010E	0	1	1	1
Read Data Level							
S2-1/2nd Timeout	Set Timer	08	0110	1	0	0	0
Jumper/Switch S2-2	Set Timer	09	0112	1	0	0	1
Jumper/Switch S2-3	Set Timer	0A	0114	1	0	1	0
Jumper/Switch S2-4	Set Timer	0B	0116	1	0	1	1
Jumper/Switch S2-5	Clear Latches	0C	0118	1	1	0	0
Jumper/Switch S2-6	Clear Latches	0D	011A	1	1	0	1
Jumper/Switch S2-7	Clear Latches	0E	011C	1	1	1	0
Jumper/Switch S2-8	Clear Latches	0F	011E	1	1	1	1

*In this example, register 12 contains 0100_{16} and jumper/switch S1 (CRU base address select) is set S1-8 to S1-1 as follows; 0 0 0 0 1 0 0 0, where 0 = Jumpered or ON, 1 = Unjumpered or OFF.

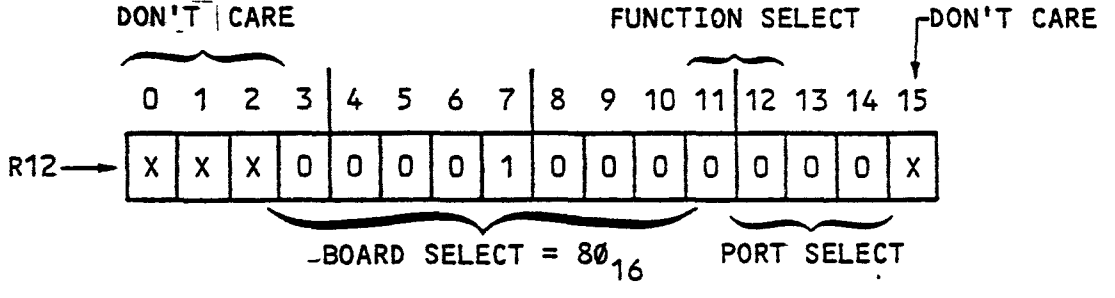


FIGURE 3-3. EXAMPLE OF CRU ADDRESSING

Assume that a SBO 0 instruction is executed (as in Figure 3-3). The following points would apply to our example;

1) Bits 3 through 10 carry the information to select the board which has it's S1 switch set to 08_{16}.

2) Since A11 is low in this case, a Write to Output function is selected.

3) Bits 12,13 and 14 are all low, selecting Port 0.

4) Bits 0,1,2 and 15 are ignored for CRU functions.

5) Thus Port 0 would be turned on.

3.6 PROGRAMMING EXAMPLES

It will be assumed for the following examples that:

- The user is familiar with the TM 990 Assembly language
- The CRU Hardware Base address is 0080_{16} and the CRU software base address is 0100_{16}.
- Jumper/switch S1 is set to decode the hardware base address, 0080_{16} as follows;

S1-8							S1-1	
ON	ON	ON	ON	ON	ON	ON	ON	
0	0	0	0	1	0	0	0	= 08_{16}

3.6.1 Write a logical 1 to Port 0 (Close circuit at Port 0)

```
LI   R12,>0100     LOAD R12 WITH THE CRU SOFTWARE BASE ADDRESS
SBO  0             CLOSE CIRCUIT AT PORT ONE
 •
 •
 •
```

This closes the circuit connected to P0+ and P0-.

3.6.2 Write a logical 1 to Port 5 and Read Echo Back

```
LI   R12,>0100     LOAD R12 WITH THE CRU SOFTWARE BASE ADDRESS
SBO  5             SET PORT 5 TO 1
TB   5             HAS PORT 5 CIRCUIT CLOSED?
JNE  ERROR         NO, JUMP TO ERROR ROUTINE
 •                 YES, CONTINUE
 •
 •
```

This example writes a 1 to port 5, tests port 5 and jumps to an error routine if Port 5 was not sensed as being a closed circuit.

3.6.3 Read Jumper/switch S2-3 for Data Level

```
LI   R12,>0100     LOAD R12 WITH THE CRU SOFTWARE BASE ADDRESS
TB   >A            >A IS FROM TABLE 2-3, HARDWARE DISPLACEMENT TO
 •                 SELECT READ DATA LEVEL JUMPER/SWITCH S2-3
 •
 •
```

This reads one of the DATA LEVEL jumper/switches. These jumper/switches are set when the TM 990/E351 board is installed. The value of the jumper/switches can represent anything the user wants. Some of the possibilities are;

1) a code identifing the location of the board in the system

2) the type of device that the board is controlling

3) constant data input

3.6.4 Set and Poll Watchdog Timer

```
LI   R12,>0100     LOAD R12 WITH THE CRU SOFTWARE BASE ADDRESS
SBO  8             TRIGGERS THE TIMER
 •
 •
 •
TB   8             HAS A TIMEOUT OCCURRED?
JNE  TIMEOUT       YES, GO TO TIMEOUT ROUTINE
 •                 NO, CONTINUE
 •
 •
```

Remember that the Watchdog Timer must be set every 20 ms or the options set at jumpers J2 and J3 will occur as specified in paragraph 2.3.3. It is the programmers responsibility to see that the timer is kept set. A routine to set the timer should be included in any loop or subroutine that waits for an input or interrupt.

To poll the Watchdog Timer for the second timeout, test the CRU address of data level jumper/switch S2-1. The jumper/switch must be jumpered or set to OFF for this test to be valid. A zero indicates a timeout occured, a one indicates a timeout did not occur.

3.6.5 Clear All Output Ports

```
LI   R12,>0100     LOAD R12 WITH THE CRU SOFTWARE BASE ADDRESS
SBO  >C            RESETS ALL PORTS TO LOGICAL 0'S (OPENS CIRCUITS)
 •
 •
 •
```

This is a short-cut method to shut down all circuits controlled by the same board at the same time.

3.6.6 Write a Logical 1 to Port 3, Turn Off All Other Ports, and Set the Watchdog Timer

```
LI   R12,>0100     LOAD R12 WITH THE CRU SOFTWARE BASE ADDRESS
LI   R2,>108       SEE EXPLANATION BELOW
LDCR R2,9          WRITES A LOGICAL 1 TO PORT 3 AND SETS THE TIMER
 •
 •
 •
```

The value 108_{16} loaded into R2 is derived in Figure 3-3. This value represents the two bits necessary to write to port 3 and set the timer. The zeros written to the other ports will open any closed circuits at these ports. R2 is loaded into the CRU as shown in the figure.

Bit 7 is set to 1 in R2. When the LDCR instruction is executed, this bit sets the timer.

Bit 12 is set to 1 in R2. When the LDCR instruction is executed, this bit causes Port 3 to be set to a logical 1.

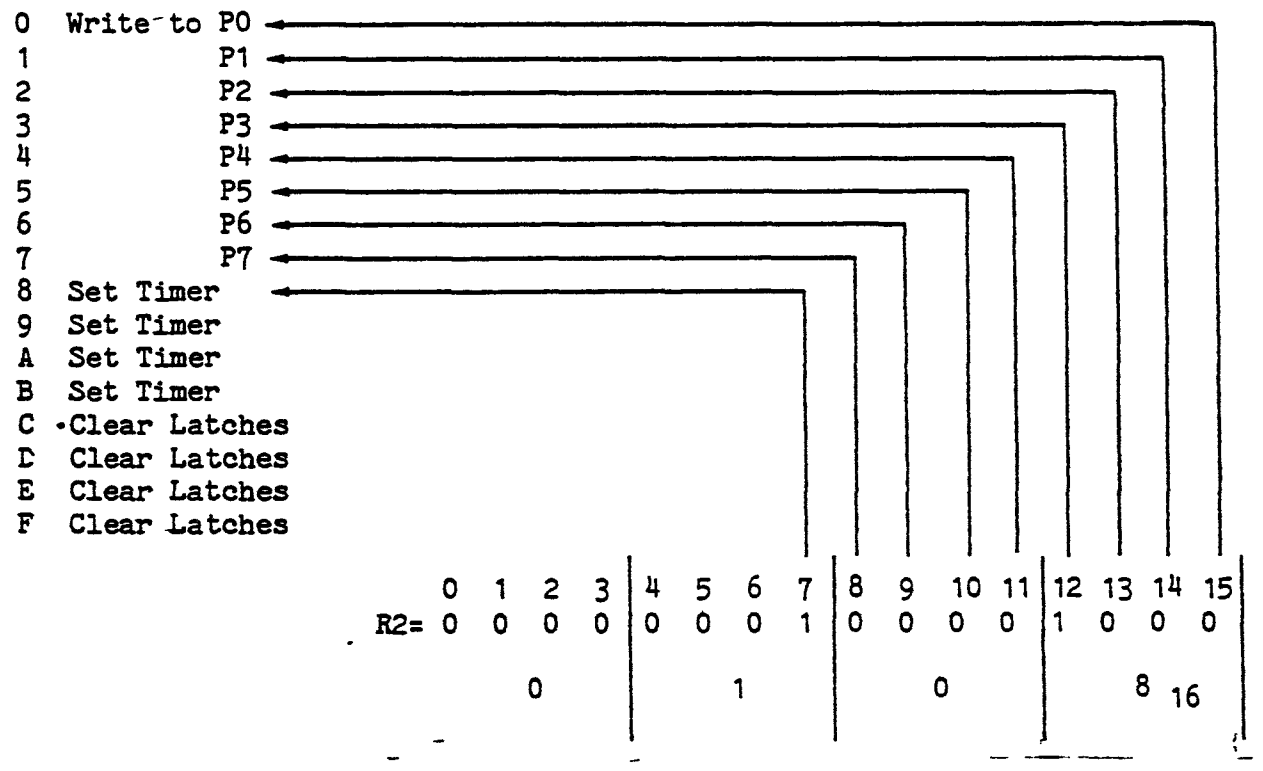


FIGURE 3-4. DERIVATION OF R2'S VALUE IN EXAMPLE 3.6.6

3.6.7 Sample Program

The following assumptions are made for the sample program in Figure 3-5;

1) Jumper/switch S1 is set to select a hardware base address of 0080_{16} as in the previous examples.

2) Jumper J1 is set for NO HOLD, E2 to E3.

3) Jumper J2 is set for a PWRFAIL- interrupt, E5 to E6.

4) Jumper J3 is set to INACTIVE, E8 to E9.

5) A demonstration display similar to the one shown in Figure 3-6 is connected to P2.

6) A TM 990/E150 CPU board with TIBUG TM 990/E4001 and the TM 990/E351 board are installed in a suitable chassis with suitable power supply.

7) A terminal is connected to the TM 990/E150 board.

If entered as it is listed, this program will light the display LED's in sequence.

After the demonstration, substitute a NOP (1000_{16}) for the SBO 8 instruction at memory location $3C3C_{16}$. With the SBO 0 instructon removed, the Watchdog Timer will not be set in time. A PWRFAIL- interrupt will be issued and the 'TIMEOUT' message will be displayed. Control is returned to the monitor.

```
MEM  OP
ADDR CODE
          *
          *INITIALIZATION
          *
3C00              AORG >3C00          SET STARTING ADDRESS
3C00      WSP     BSS  32            RESERVE WORKSPACE AREA
     0100 OUTPRT  EQU  >100           DEFINE CPU SOFTWARE BASE ADDRESS
3C20 020C         LI   R12,OUTPRT     LOAD THE CPU SOFTWARE BASE ADDRESS
3C22 0100
3C24 02E0         LWPI WSP            LOAD THE WORK SPACE POINTER
3C26 3C00
          *
          *
          *WHEN THE MONITOR IS RESET PRIOR TO RUNNING THIS PROGRAM,
          *THE WATCHDOG TIMER WILL BE TRIGGERED BY IORST- AND THE
          *INTERRUPT MASK WILL BE SET TO ZERO. THE PWRFAIL- INTERRUPT
          *WILL BE ACTIVE BUT MASKED OFF BEFORE THIS PROGRAM CAN BE STARTED.
          *THEREFORE, IT IS NECESSARY TO TRIGGER THE TIMER TO ELIMINATE THE
          *PWRFAIL- INTERRUPT AND THEN UNMASK IT SO THAT IT WILL BE
          *RECOGNIZED SHOULD IT OCCUR LATER.
          *
          *
3C28 1D08         SBO  8              SET THE WATCHDOG TIMER
3C2A 0300         LIMI 3              UNMASK THE PWRFAIL- INTERRUPT
3C2C 0003
          *
          *R1 RECEIVES THE INITIAL BIT PATTERN - 0000 0000 1000 0000
          *
3C2E 0201 RESET   LI   R1,>80         INITIAL BIT PATTERN INTO R1
3C30 0080
          *
          *EACH TIME R1 IS SHIFTED LEFT, A DIFFERENT LED WILL BE SELECTED
          *UNTIL THE '1' BIT IS SHIFTED OUT TO SET CARRY
          *
3C32 0A11 START   SLA  1,1            HAS THE '1' BIT BEEN SHIFTED TO CARRY?
3C34 18FC         JOC  RESET          YES, RESET R1
          *
          *USE THE CONTENTS OF R1 TO LOAD THE CRU. THIS TURNS ON ONE
          *LED AND TURNS OFF THE PREVIOUS LED
          *
3C36 3201         LDCR R1,8           NO, TURN ON/OFF SELECTED PORTS
          *
          *THIS SECTION IS THE DELAY TIMER. NOTE THAT THE WATCHDOG
          *TIMER IS SET ON EACH INTERATION OF THE LOOP. WHEN THE DELAY
          *IS FINISHED, GO BACK AND GET A NEW VALUE FOR R1
          *
3C38 0202         LI   R2,>4000       SET DELAY-TIMER VARIABLE
3C3A 4000
3C3C 1D08 LOOP    SBO  8              SET WATCHDOG TIMER
3C3E 0602         DEC  R2             IS THE DELAY LOOP FINISHED?
3C40 16FD         JNE  LOOP           NO, REPEAT THE LOOP
3C42 10F7         JMP  START          YES, GO DO THE NEXT DISPLAY
```

FIGURE 3-5. SAMPLE PROGRAM, SHEET 1 OF 2

```
                *
                *THIS SECTION IS THE MESSAGE TO BE DISPLAYED IF A TIMEOUT
                *OCCURS FROM THE WATCHDOG TIMER. AFTER 'TIMEOUT' HAS BEEN
                *DISPLAYED, CONTROL IS RETURNED TO THE MONITOR
                *
3C70                    AORG >3C70          SET ADDRESS FOR ERROR MESSAGE
3C70 2FA0               XOP  @MESS,14       OUTPUT ERROR MESSAGE
3C72 3C78
3C74 0460               B    @>80           BRANCH TO MONITOR
3C76 0080
3C78 0D0A       MESS    DATA >0D0A          CARRAGE RETURN, LINE FEED
3C7A 5449               DATA >5449          MESSAGE -'T','I'
3C7C 4D45               DATA >4D45                   'M','E'
3C7E 4F55               DATA >4F55                   'O','U'
3C80.5400               DATA >5400                   'T',END OF MESSAGE TAG
                *
                *THE PWRFAIL- INTERRUPT VECTORS TO >3F88. THIS INSTRUCTION
                *BRANCHES TO THE MESSAGE ROUTINE
                *
3F88                    AORG >3F88          SET ADDRESS FOR PWRFAIL- INTERRUPT
3F88 0460               B    >3C70             TO POINT TO ERROR MESSAGE ROUTINE
3F8A 3C70
```

FIGURE 3-5 SAMPLE PROGRAM, SHEET 2 OF 2

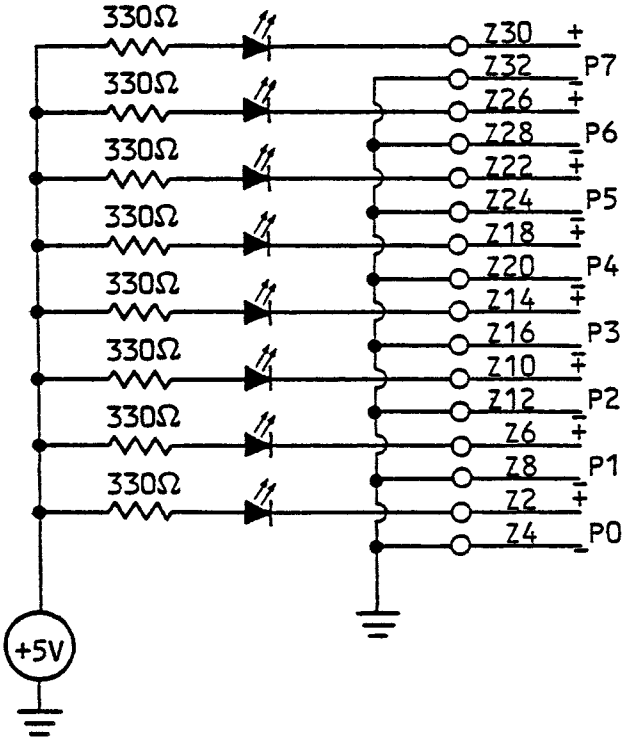


FIGURE 3-6. DEMONSTRATION DISPLAY FOR THE SAMPLE PROGRAM

SECTION 4

THEORY OF OPERATION

4.1 GENERAL

This section covers the theory of operation of the TM 990/E351. Information in the following manuals can be used to supplement the material in this section:

- The TTL Data Book
- The Optoelectronics Data Book
- The Transistor and Diode Data Book.

4.2 TM 990/E351 ARCHITECTURE

The block diagram for the TM 990/E351 is given in Figure 4-1. The major sections are the CRU base address selector and decoder, the data level selector and data level input port, the control logic, the watch dog timer, and the output ports. Each of these sections will be described in the sections that follow.

4.2.1 CRU Base Address Selector and Decoder

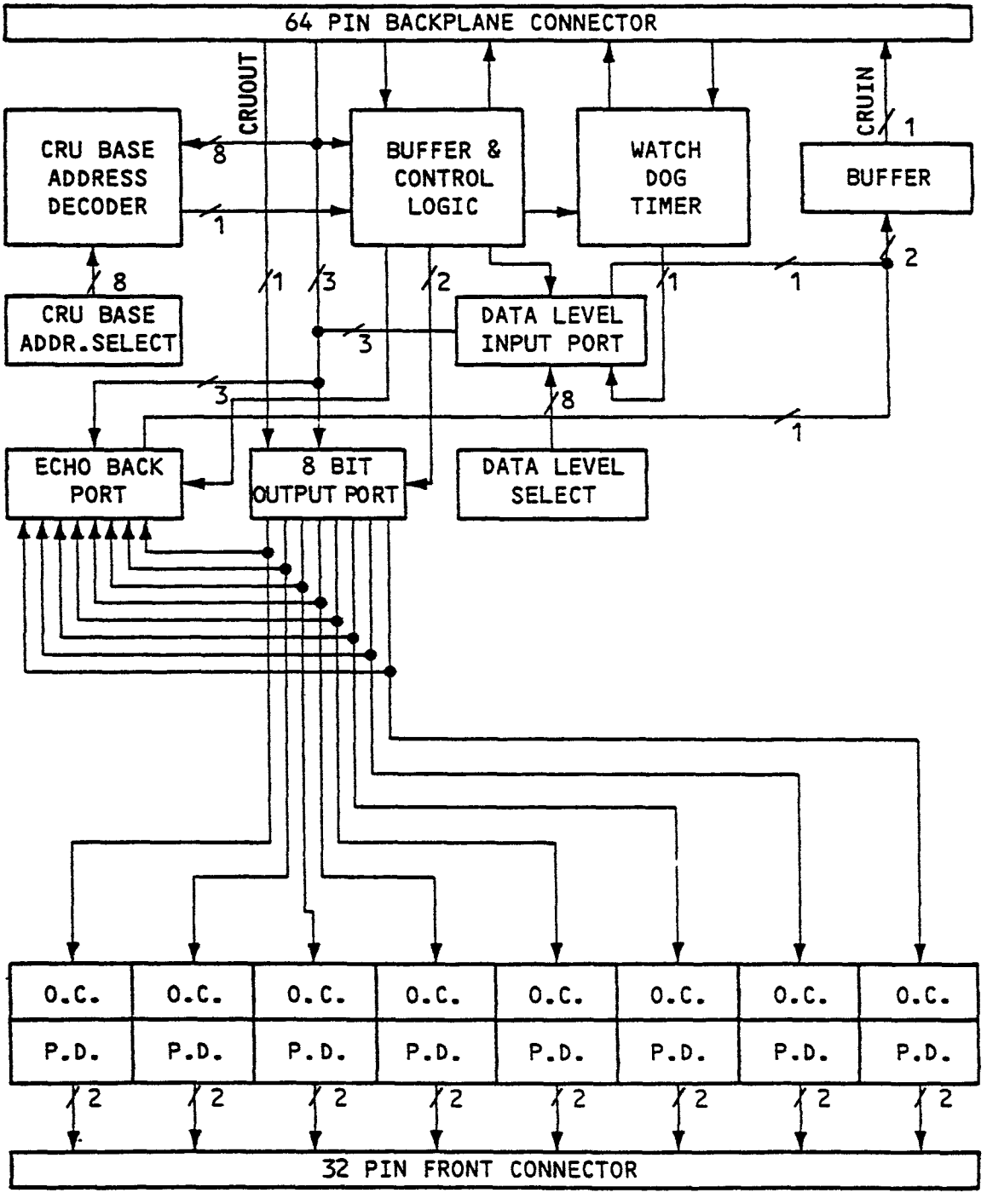
The CRU base address selector and decoder circuitry is given in Figure 4-2. The TM 990/E351 can be assigned a unique CRU base address as explained in Section 2.3.1. This address is determined by the setting on jumper/switches S1-1 through S1-8. The incoming value on address lines A3 through A10 is compared to the value determined by the jumper/switch settings of S1-8 to S1-1 respectively. When they are equal the 74LS266 comparators produce an active (high) signal; this signal is inverted by U11 which in turn produces an active (low) signal for the control logic. This signal is essentially a board select signal.

4.2.2 Data Level Select and Data Level Input Port

The data level input port circuitry is shown in Figure 4-3. An 8-position socket platform (S2) is provided for inputting constants such as parameters or station numbers. These data levels can also be used for testing/evaluating the performance of certain circuits on the TM 990/E351. The data levels that are set on S2-1 through S2-8 can be read when the 74LS251 data selector at U7 is addressed and selected. This chip reads address lines A12-A14 and is selected by an active 1Y2 or 1Y3 output from control logic decoder SN74LS156 at U9. S2-1 is wire-ORed with the Watchdog Timer output 2Q-, allowing software monitoring of the second timeout (see paragraph 2.3.3.3).

4.2.3 Control Logic

The control logic selects the input port, the output port, the echo back port, the watch dog timer and also can be used to clear the output ports. In order to produce these five control signals, a SN74LS156 reads address lines A11 and A12-, plus CRUCLK- and is gated on by a board select signal from the CRU base address decoder after it is inverted by U11. The control logic circuitry is given in Figure 4-4.



O.C. = OPTO COUPLER

P.D. = POWER DRIVER

FIGURE 4-1. TM 990/E351 BLOCK DIAGRAM

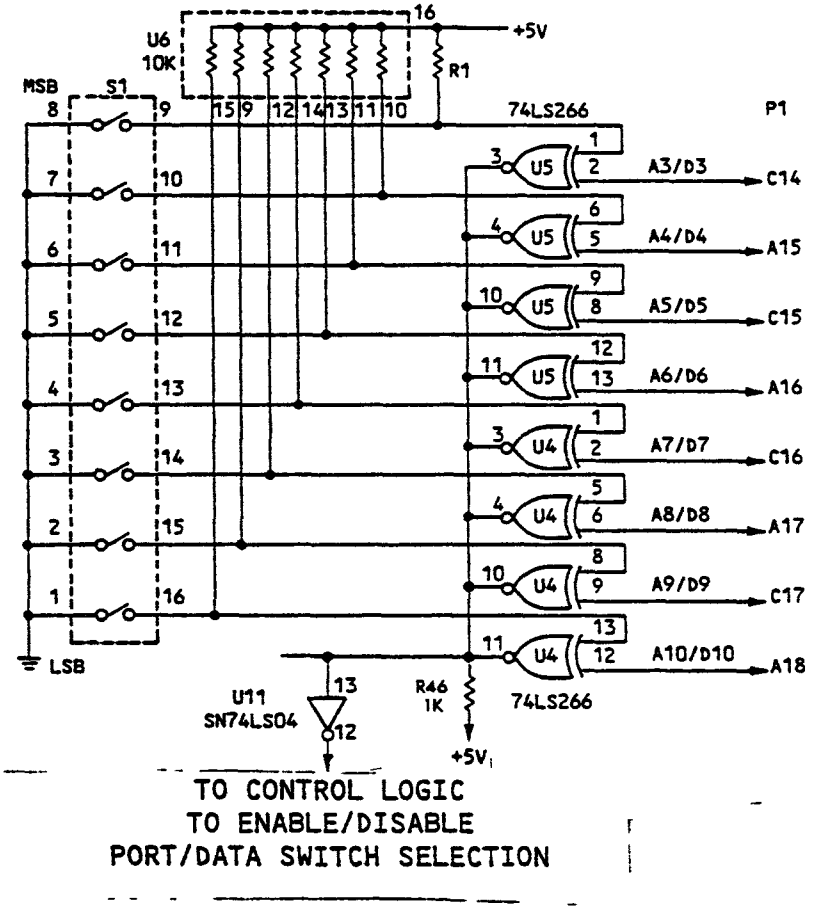


FIGURE 4-2. CRU BASE ADDRESS SELECTOR/DECODER

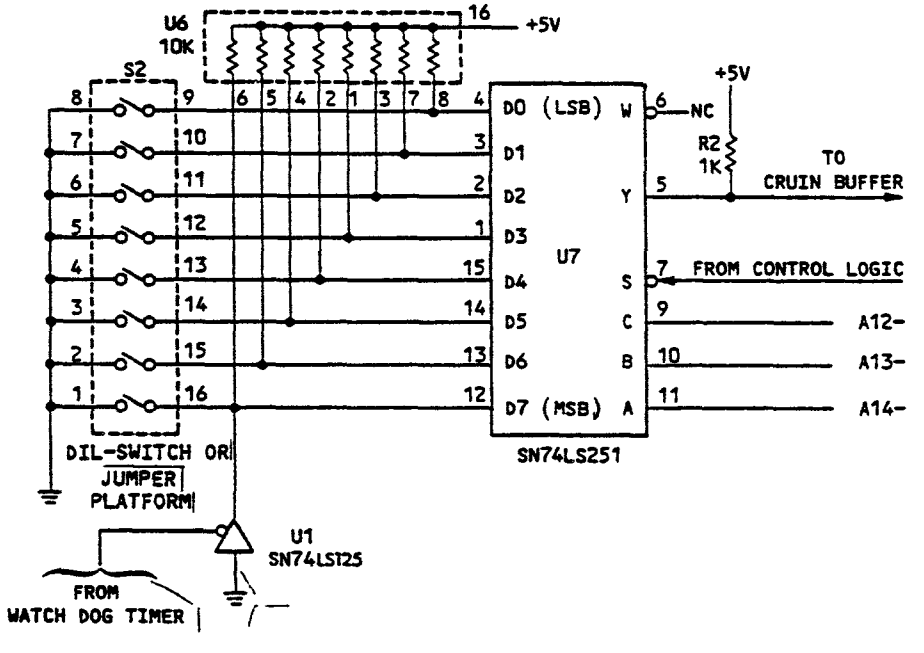


FIGURE 4-3. DATA LEVEL SELECT/DATA LEVEL INPUT PORT

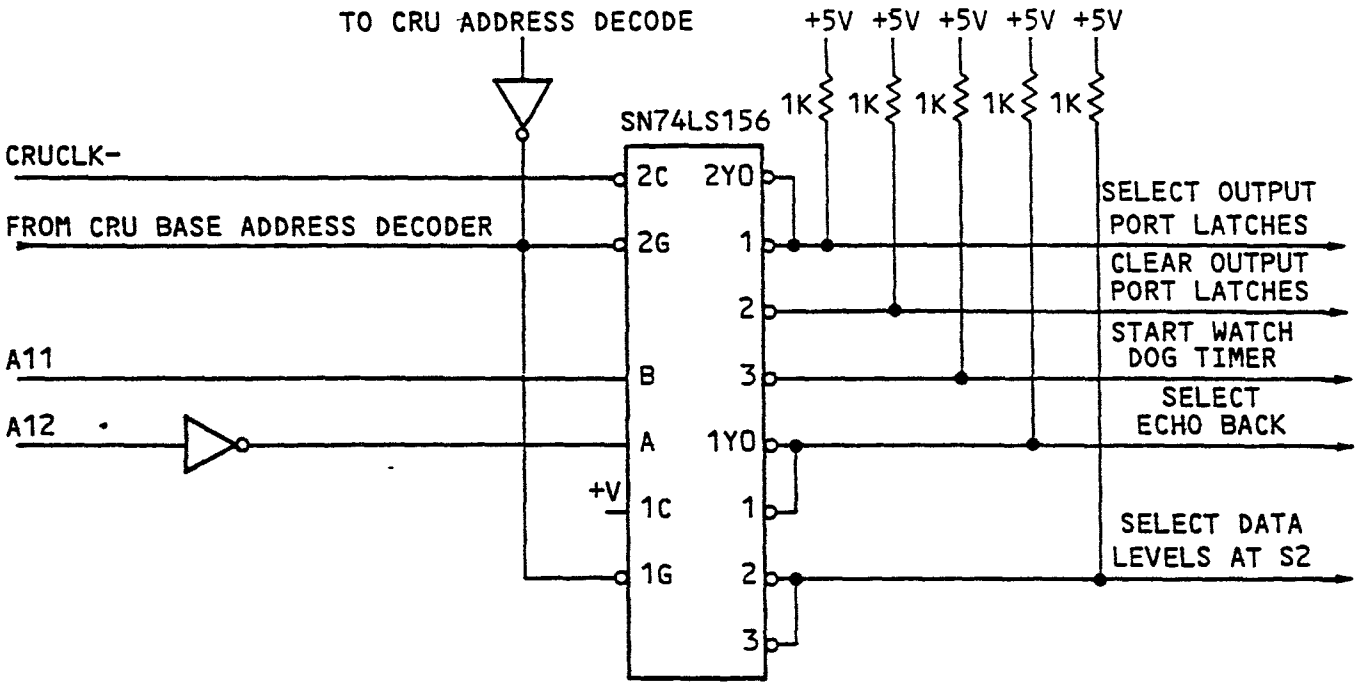


FIGURE 4-4. CONTROL LOGIC

4.2.4 Watchdog Timers

The watchdog timer circuitry is given in Figure 4-5. The timer provides the user of the TM 990/E351 with an excellent tool to identify erroneous program sequences and protect the system interfaces and attached peripherals (motors, relays, and controlled machines) against damage.

The TM 990/E351 has two time outs; timeout 1 equals 20 ms and timeout 2 equals 10 ms. If a program is running correctly, the timer will be reset by software before a timeout occurs. If not, the first timeout will generate either a PWRFAIL- or NMI- interrupt depending on the position of jumper J2 and then try a new system startup. If jumper J2 is not used, neither PWRFAIL- nor NMI- interrupt will occur.

The position of jumper J3 determines whether the output ports are reset or not reset after the first timeout. After timeout 1 is completed, timeout 2 will start. If the system recovers through the NMI- or PWRFAIL- interrupt, then the program will reset the timer and start timeout 1 again.

If the NMI- or PWRFAIL- interrupts fail to bring about a system recovery, then timeout 2 will cause a system hold by pulling the GRANTOUT line low if jumper J1 is connected E1 to E2. This type of system stop is possible when the GRANTIN-/GRANTOUT jumper on the backplane is removed from the slot occupied by the TM 990/E351 module. Once the system enters the hold mode, it can only be restarted by a system-RESET.

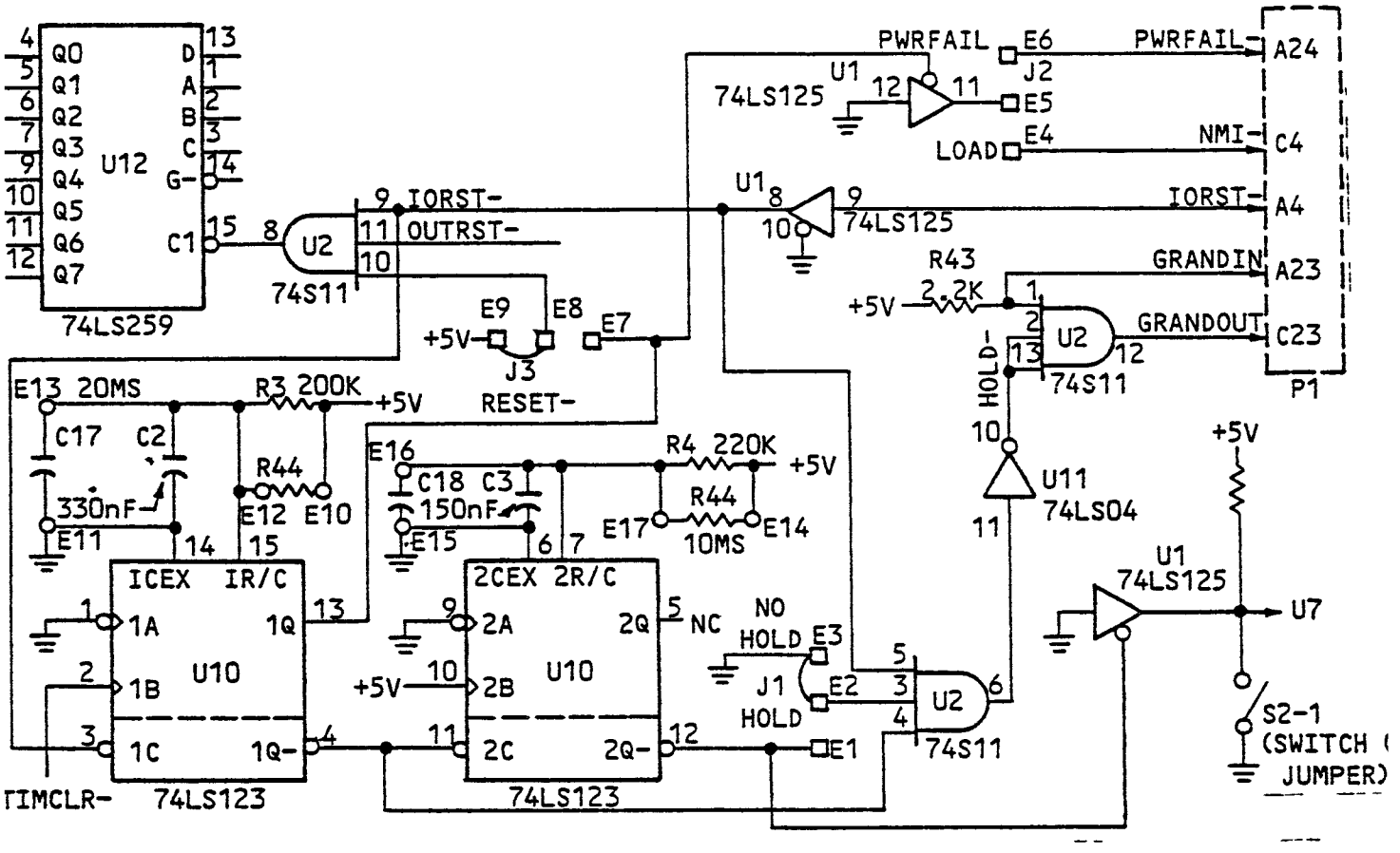


FIGURE 4-5. WATCHDOG TIMER

4.2.5 Output Ports

A partial diagram of the 8-bit output port with echo back circuitry, opto-couplers and power drivers is shown in Figure 4-6. Port 7 (P7) of the output ports is shown driving a relay so that certain theoretical aspects of this circuitry can be explained.

The output port consists of an 8-bit addressable latch (74LS259) which receives its data input from the processor via the CRUOUT line. This latch is addressed via address lines A12- through A14- and is selected by an active (low) signal from the control logic circuitry.

The 74LS259 latch provides outputs that are then inverted by the 74LS240 prior to being used to turn the photodiode on or off in the opto-couplers. When the photodiode conducts, the phototransistor in the opto-coupler conducts current through R33. This current produces the necessary voltage drop so that Q8 is now forward biased.

Q8's current flows through R42 thus providing the necessary forward bias for Q16. Q16 can be considered as a closed switch at this time thus activating the relay. The diode across Q16 is for transient suppression. The zener diode's function is to protect the opto-coupler against inductive transients.

When the current through an inductive load is rapidly cut-off, an inductive kick occurs. If this inductive kick produces approximately 33 volts, the zener diode will conduct current through R42 and turn on Q16. Q16 will shunt the inductive kick thus protecting the opto-coupler.

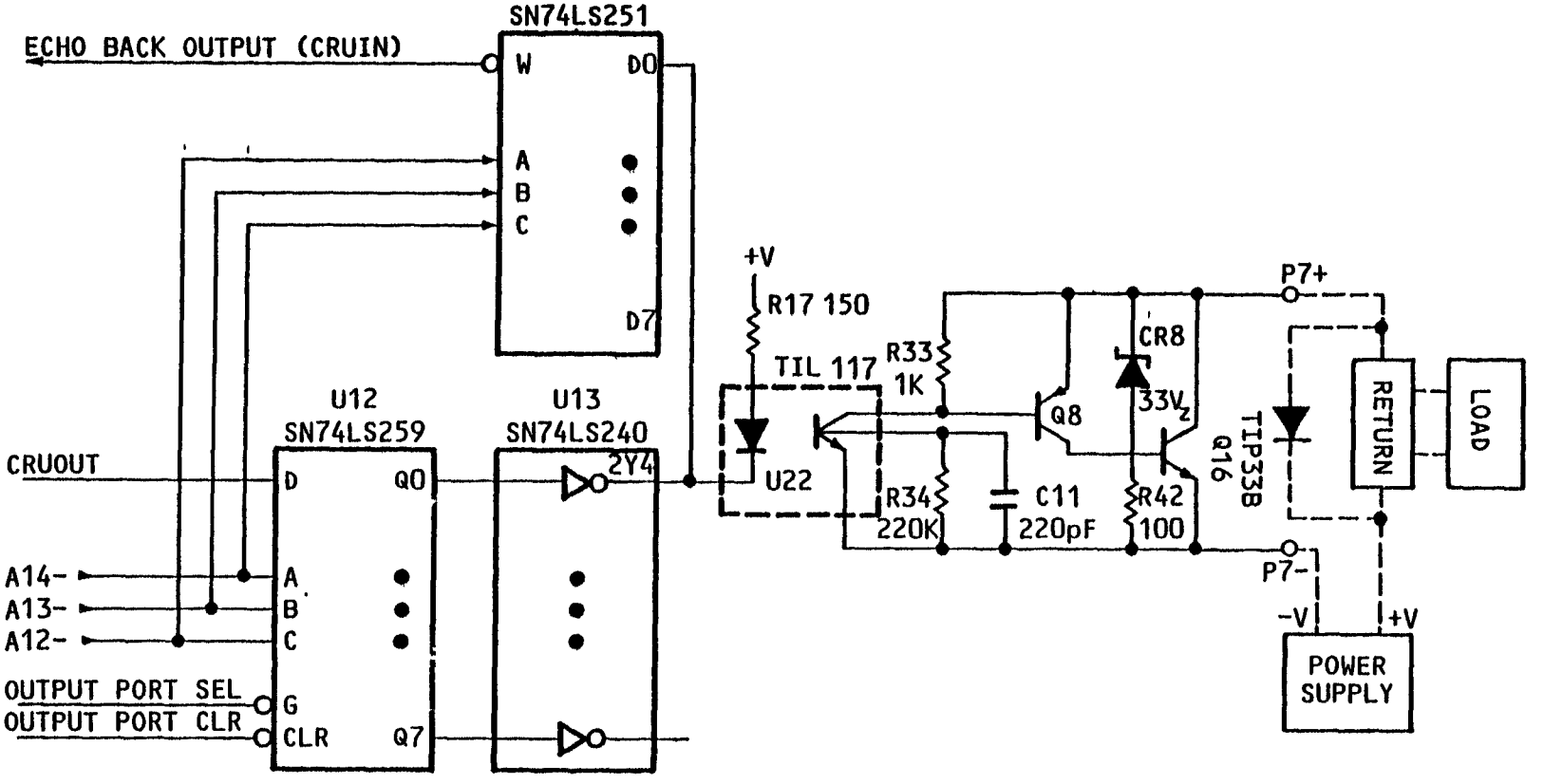
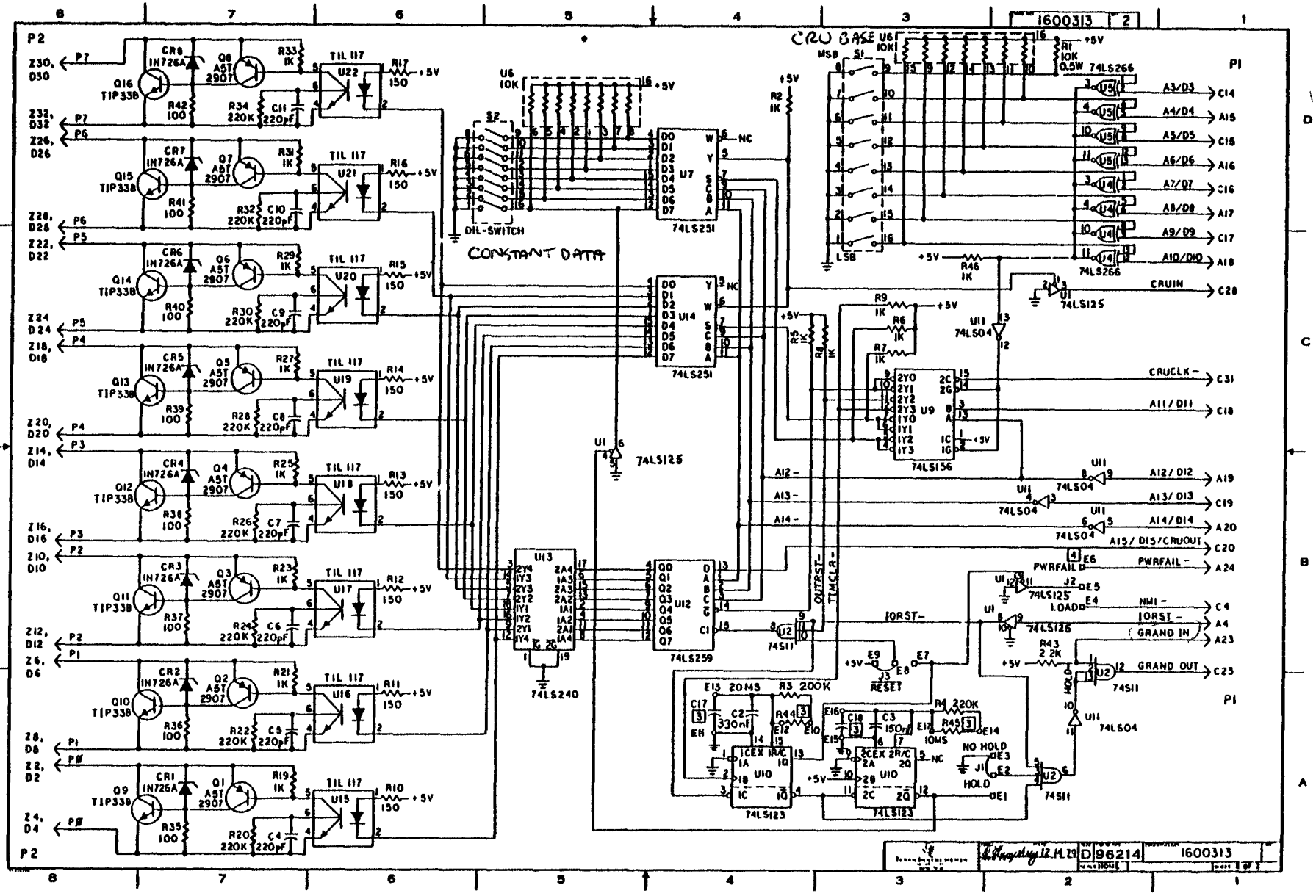


FIGURE 4-6. OUTPUT PORTS

APPENDIX A

SCHEMATICS


1600313 2
CRU BASE
CONSTANT DATA
DIL-SWITCH
74LS251
74LS125
74LS240
74LS259
74LS156
74LS266
74LS123
74LS04
74LS11
74LS126
RESET
HOLD
NO HOLD
CRUIN
CRUCLK-
PWRFAIL-
LOAD-
NMI-
IORST-
GRAND IN
GRAND OUT
A3/D3
A4/D4
A5/D5
A6/D6
A7/D7
A8/D8
A9/D9
A10/D10
A11/D11
A12/D12
A13/D13
A14/D14
A15/D15/CRUOUT
D 96214
1600313

1600313 SH 1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

NOTES UNLESS OTHERWISE SPECIFIED

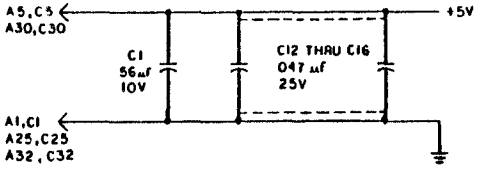
1 ALL RESISTANCE VALUES IN OHMS
2 ALL RESISTORS ARE 1/4 W, 5%
5 E10 THRU E17 ARE TERMINALS FOR INSTALLATION OF R44, R45; C17, C18 VALUES @ CUSTOMER OPTION

REFERENCE DESIGNATORS	
USED	NOT USED
C1 - C18	
CR1 - CR8	
E1 - E17	
J1 - J3	
P1, P2	
Q1 - Q16	
R1 - R46	R18
S1, S2	
U1 - U22	U3, U8

JUMPER CONFIGURATION	
JUMPER	POSITION
J1	E2, E3
J2	E5, E6
J3	E8, E9

4

SPARES



ITEM NO	QTY	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	MFR'S PART NUMBER OR SPECIFICATION	MFR CODE

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±1°; 3 PLACE DECIMALS ±.010; 2 PLACE DECIMALS ±.03
- REMOVE ALL BURRS AND SHARP EDGES
- FINISH METRICAL PARTS FOR REFERENCE ONLY

REQ NO	IDENT	T SPEC	NO	ADDITIONAL CLASSIFICATION	NOTES
	PROCESS				

PROCESSES — FOR CORRELATION TO GOVERNING SPECIFICATIONS, SEE TI DRAWING 7269187

1600315	8117
NEXT ASSY APPLICATION	USED ON

Texas Instruments
Dallas, Texas

DIAGRAM, LOGIC
TM 990/E 351

CAGE NO	DRAWING NO
D96214	1600313

NEXT ASSY NONE | SHT 1 OF 2

43

APPENDIX B

PARTS LIST

SYMBOL	DESCRIPTION
C1	Capacitor, tant., 39 MFD, 10%, 10 V
C2	Capacitor, .33 uF, 2%, 25 Vdc
C3	Capacitor, ceramic, .15 uF, 2%, 25 V
C4-C11	Capacitor, ceramic, 220 pF, 10%, 200 V
C12-C16	Capacitor, .047 uF, +80%,-20%
CR1-CR8	Diode, IN726A
E1-E9	Pin, .025 square
J1-J3	Connector, jumper plug
P1	Connector, IEC/DIN, PCB, 64-pin male
P2	Connector, IEC/DIN, male, 32-pin, right angle
Q1-Q8	Transistor A5T2907, PNP
Q9-Q16	Transistor TIP 33B
R1	Resistor, 10 K ohm, 5%, ½ W
R2	Resistor, 1.0 K ohm, 5%, ¼ W
R3-R4	Resistor, 220 K ohm, 5%, ¼ W
R5-R9	Resistor, 1.0 K ohm, 5%, ¼ W
R10-R17	Resistor, 150 ohm, 5%, ¼ W
R19	Resistor, 1.0 K ohm, 5%, ¼ W
R20	Resistor, 220 K ohm, 5%, ¼ W
R21	Resistor, 1.0 K ohm, 5%, ¼ W
R22	Resistor, 220 K ohm, 5%, ¼ W
R23	Resistor, 1.0 K ohm, 5%, ¼ W
R24	Resistor, 220 K ohm, 5%, ¼ W
R25	Resistor, 1.0 K ohm, 5%, ¼ W
R26	Resistor, 220 K ohm, 5%, ¼ W
R27	Resistor, 1.0 K ohm, 5%, ¼ W
R28	Resistor, 220 K ohm, 5%, ¼ W
R29	Resistor, 1.0 K ohm, 5%, ¼ W
R30	Resistor, 220 K ohm, 5%, ¼ W
R31	Resistor, 1.0 K ohm, 5%, ¼ W
R32	Resistor, 220 K ohm, 5%, ¼ W
R33	Resistor, 1.0 K ohm, 5%, ¼ W
R34	Resistor, 220 K ohm, 5%, ¼ W
R35-R42	Resistor, 100 ohm, 5%, ¼ W
R43	Resistor, 2.2 K ohm, 5%, ¼ W
R46	Resistor, 1.0 K ohm, 5%, ¼ W
S1-S2	Switch, dual in line, 8 position
U1	Network, SN74LS125N
U2	Network, SN74S11N
U4-U5	IC, SN74LS266N
U6	Network, resistor, 10.0 K ohm, DIL
U7	Network, SN74LS251N
U9	IC, dual 2-line-to-4-line decoder
U10	Network, SN74LS123N
U11	Network, SN74LS04N
U12	IC, SN74LS259N
U13	IC, SN74LS240N
U14	Network, SN74LS251N
U15-U22	IC, TIL-33B Optically Coupled Isolator

APPENDIX C

DATA SHEET ON 74LS123 MONOSTABLE MULTIVIBRATOR

NOTE

Countdown time for the watchdog timer can be varied according to the impedance inserted at sockets E10 to E17 as shown on page 2 of the schematics. Formulae and charts for customizing this timeout period are provided in this data sheet.

Designing with Low Power Schottky SN54/74LS123 Dual Retriggerable Monostable Multivibrators

From Bulletin CA-196

by
W. T. Greer, Jr.
Low-Power Schottky Engineering

INTRODUCTION

Texas Instruments SN54/74LS123 Dual Retriggerable Monostable Multivibrator, direct replacement for the SN54/74L123 and SN54/74123 is a one-shot capable of very long output pulses and up to 100% duty cycle. The SN54/74LS123 also features dc triggering from gated low-level active ("A") and high-level active ("B") inputs and provides a "Clear" input which terminates the output pulse at any predetermined time independent of timing components, R_{ext} and C_{ext}. The output pulse width can also be extended by retriggering the input prior to the termination of an existing output pulse.

The "B" input on a SN54/74LS123 is designed to handle pulses with a transition rate as slow as 1 volt per 10 μs (Schmitt trigger input) with jitter-free one-shot action. This capability allows the SN54/74LS123 to be used as an interface element between circuits with very slow rising output pulses and circuits which require fast rising input pulses.

DEVICE DESCRIPTION

- 100% maximum duty cycle
- DC triggered from active-high or active-low logic inputs
- Input clamp diodes
- Low power dissipation
- Compensated for V_{CC} and temperature variations
- Compatible with TTL and DTL circuits

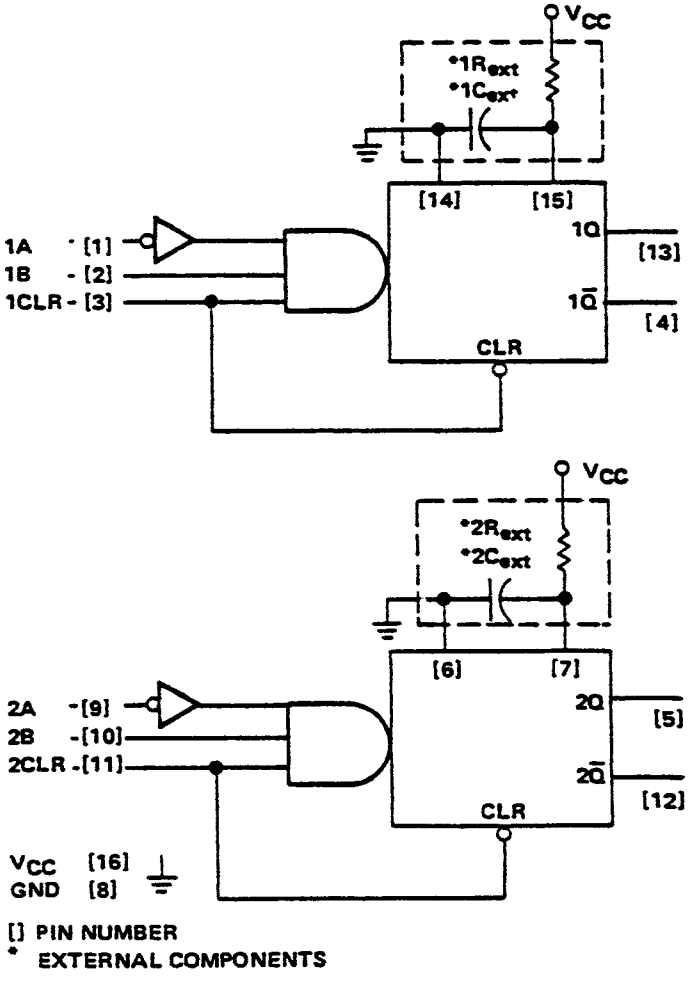


FIGURE 1. LS123 Logic Diagram

A functional block diagram is shown in Figure 1. Each one-shot has two inputs, one active low and one active high, which allow both leading or trailing edge triggering. Once triggered, the basic pulse width may be extended by retriggering the gated low-level active (A) or high-level active (B) inputs, or the pulse width may be reduced by use of the overriding clear. Therefore an input cycle time shorter than the output cycle time will retrigger the LS123 and result in a continuously high Q output.

FUNCTIONAL TABLE

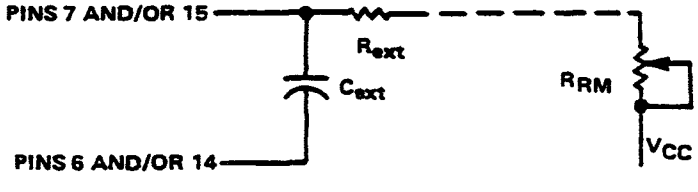
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		
↑	L	H		

RULES FOR OPERATION

1. An external resistor (R_{ext}) and an external capacitor (C_{ext}) are required as shown in Figure 1 for proper circuit operation.
   NOTE: For best results, system ground should be applied to the C_{ext} terminals.
2. This value of R_{ext} may vary from 5 kΩ to 160 kΩ from −55°C to 125°C.
3. C_{ext} may vary from 0 pF to any necessary value.
4. The input may have a minimum amplitude of −0.5 volt and a maximum of 5.5 volts.
5. The output pulse width (T_w) is defined as follows:

   $$T_w = K^* \cdot R_{ext} \cdot C_{ext}$$

   NOTE: K is independent of R_{ext}.
   If,
   R_{ext} is in kΩ
   C_{ext} is in pF
   T_w is in ns
6. When an electrolytic capacitor is used as C_{ext}, the switching diode required by most one-shots *is not needed* for LS123 operation.
7. For remote trimming, the circuit shown in Figure 2 is recommended:

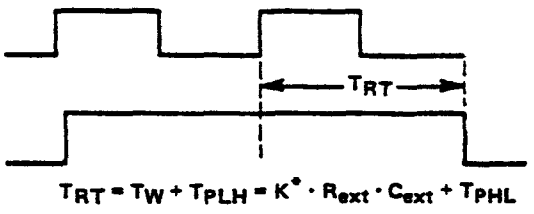


R_{RM} SHOULD BE AS CLOSE AS POSSIBLE TO THE LS123.

FIGURE 2. Remote Trimming Circuit

8. The retrigger pulse width is calculated as shown in Figure 3.

*See Figure 4 for values of K.



*SEE FIGURE 4 FOR K.

FIGURE 3. Retrigger Pulse Width Calculation

9. A 0.001 to 0.01 μF by-pass capacitor between V_{CC} and ground as close as possible to the LS123 is recommended.

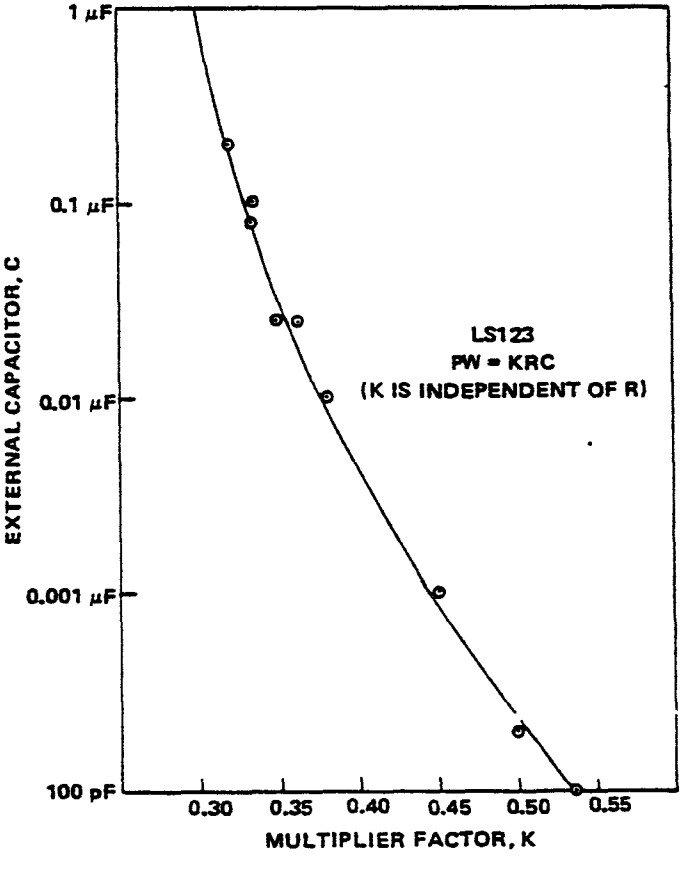


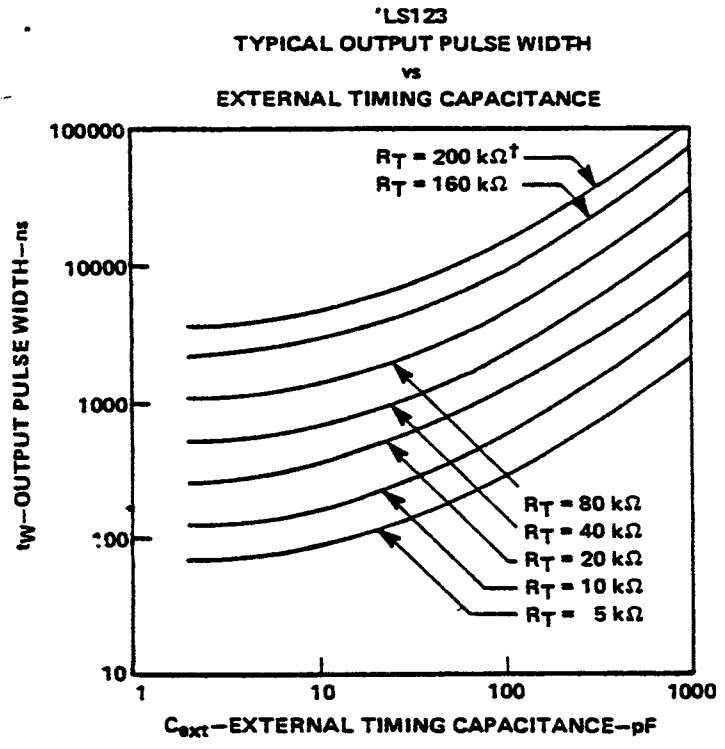
FIGURE 4. Multiplier Factor (K) Versus External Capacitor (C_{ext})

Output Pulse Width

As shown in operating Rule 5, the output pulse width (T_w) is defined as

$$T_w = K \cdot R_{ext} \cdot C_{ext}$$

However, for capacitor values less than 1000 pF, the typical curves in Figure 5 can be used.



†THIS VALUE OF RESISTANCE EXCEEDS THE MAXIMUM RECOMMENDED FOR USE OVER THE FULL TEMPERATURE RANGE OF THE SN54LS CIRCUITS.

FIGURE 5. Output Pulse Versus External Timing

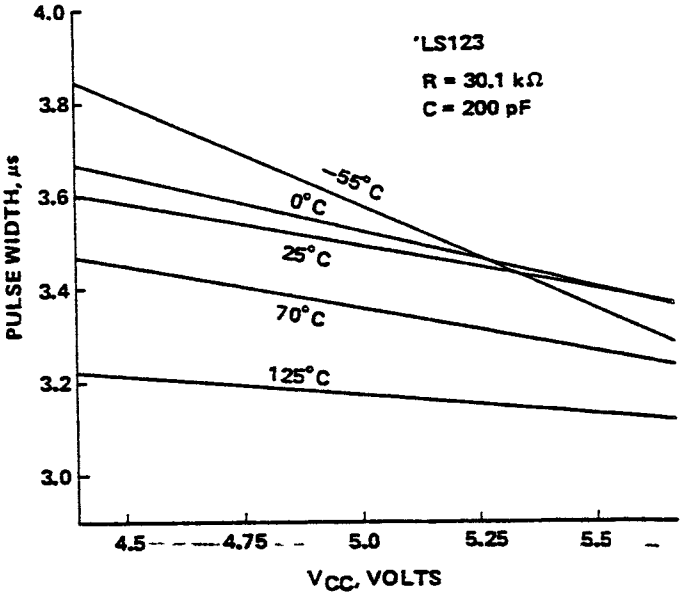


FIGURE 6. Output Pulse Width Versus Temperature

Output Width vs V_{CC} Temperature

Figure 6 shows the relationship between the pulse width, V_{CC}, and temperature.

APPLICATIONS

Delayed Pulse Generator With Override

The first one-shot, (OS_1), determines the delay time by preselected values of $R_{ext\,1}$ and $C_{ext\,1}$, whereas the second one-shot, OS_2, determines the output pulse width, by preselected values of R_{ext} and C_{ext}. (See Figure 7.)

The output pulse can be terminated at any time by a positive rising pulse into the override input.

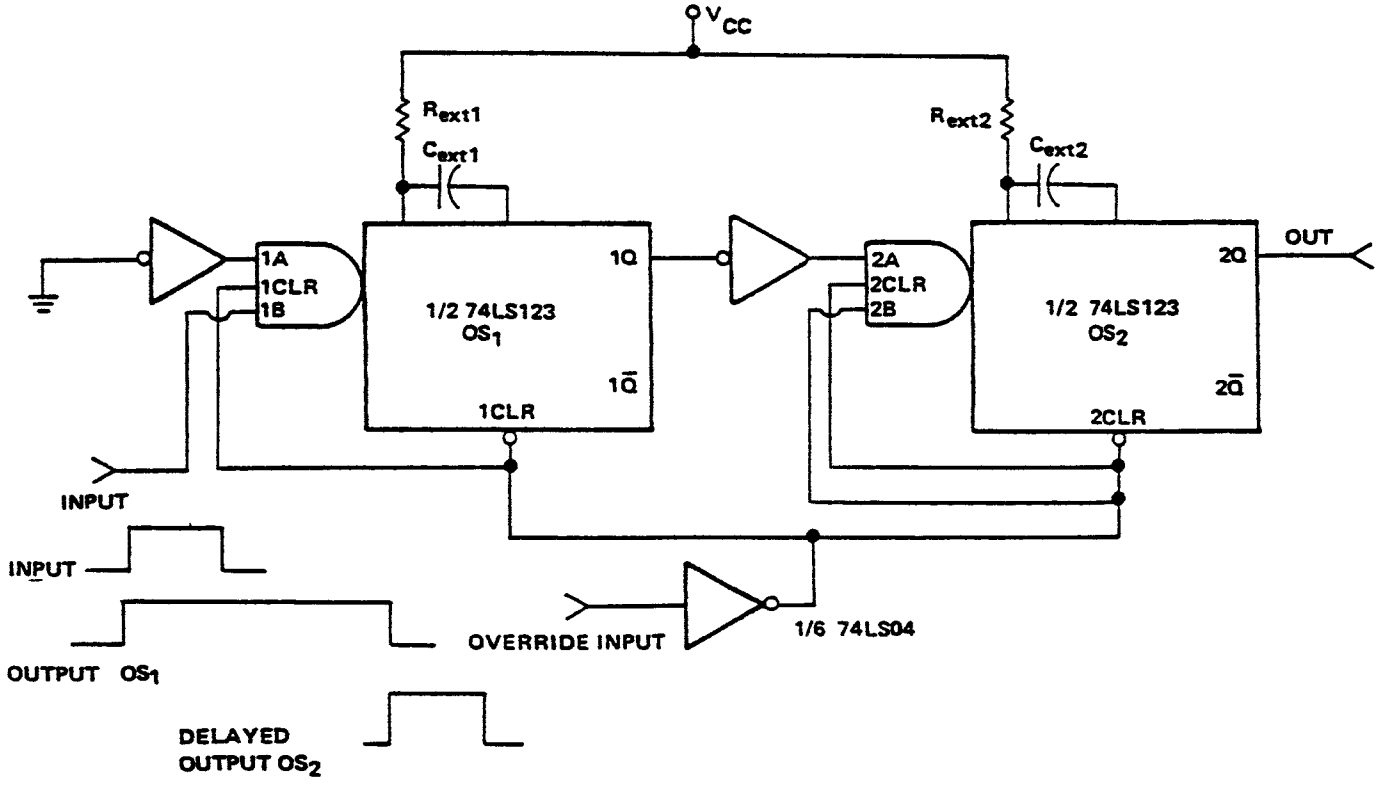
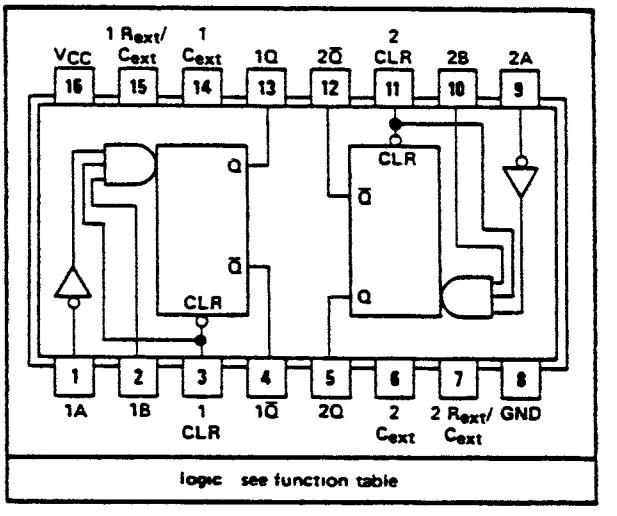


FIGURE 7. Delayed Pulse Generator with Override

TYPE SN54LS123, SN74LS123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Compensated for V_{CC} and Temperature Variations

SN54LS123 . . . J OR W
SN74LS123 . . . J OR N
(TOP VIEW) (SEE NOTES 1 AND 2)



description

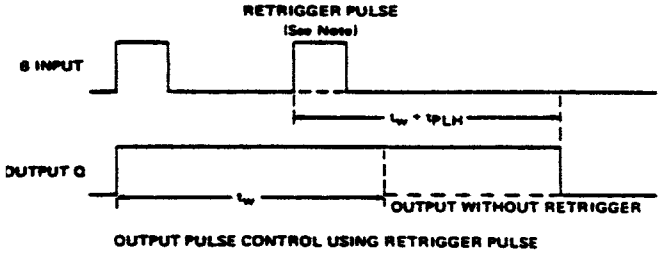
These d-c triggered multivibrators feature output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data).

Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

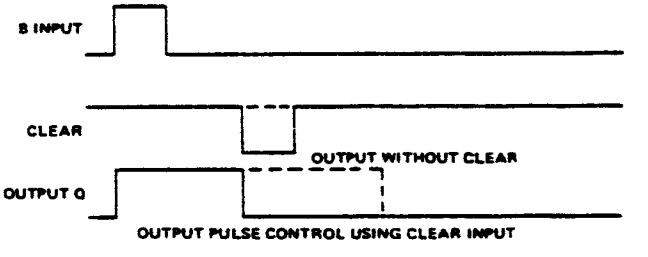
The LS123 is provided enough Schmitt hysterisis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

NOTES. 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To obtain variable pulse widths, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC}.

description (continued)



OUTPUT PULSE CONTROL USING RETRIGGER PULSE

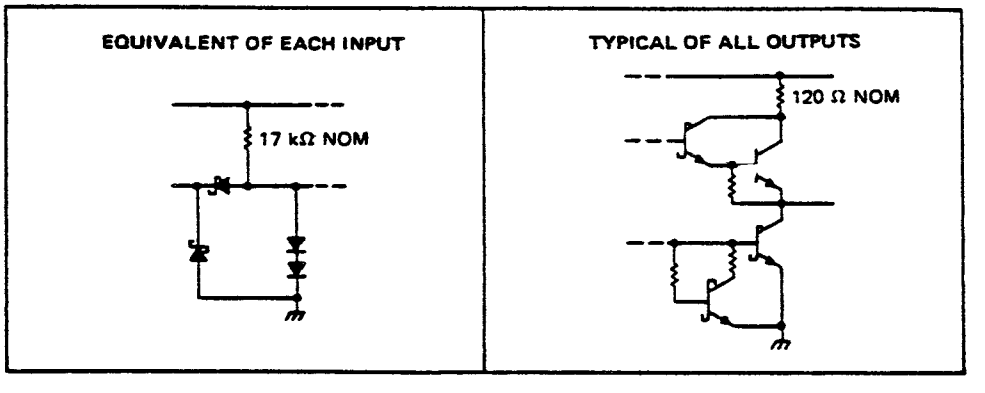


OUTPUT PULSE CONTROL USING CLEAR INPUT

NOTE Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse

FIGURE 1–TYPICAL INPUT/OUTPUT PULSES

schematics of inputs and outputs



recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Pulse width, t_w	40			40			ns
External timing resistance, R_{ext}	5		180	5		260	kΩ
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current♦	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current (quiescent or triggered)	V_{CC} = MAX,	See Note 13			12	20		12	20	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTES: 12. To measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q, ground R_{ext}/C_{ext}, apply 2 V to B and clear, and pulse A from 2 V to 0 V
13. With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 14

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_{ext} = 0, C_L = 15 pF,	R_{ext} = 5 kΩ, R_L = 2 kΩ		23	33	ns
	B					23	44	
t_{PHL}	A	$\overline{Q}$				32	45	ns
	B					34	56	
t_{PHL}	Clear	Q				20	27	ns
t_{PLH}		$\overline{Q}$				28	45	
t_{wQ} (min)	A or B	Q				116	200	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, C_L = 15 pF,	R_{ext} = 10 kΩ, R_L = 2 kΩ	4	4.5	5	μs

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{wQ} ≡ width of pulse at output Q
NOTE 14 Load circuit and voltage waveforms are shown on page 3-11

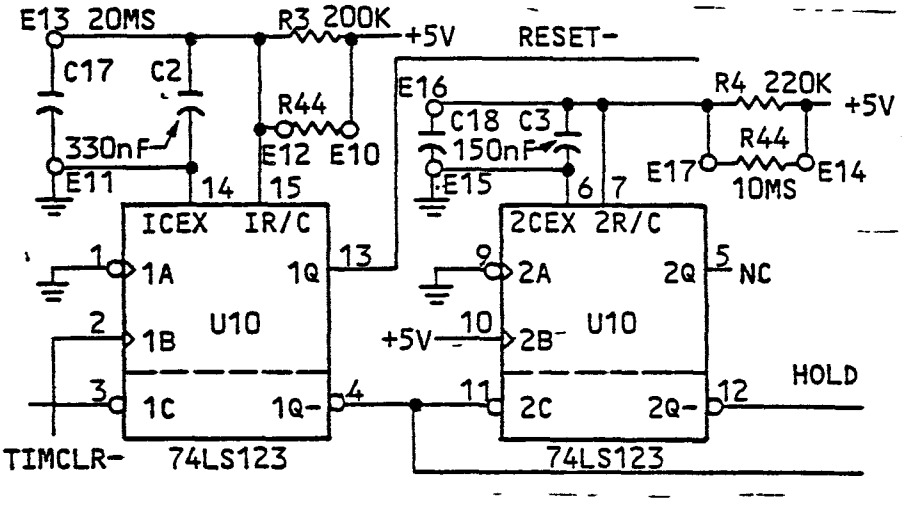


FIGURE C-1. WATCHDOG TIMER

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