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Colin Hinson

In the village of Blunham, Bedfordshire.



AP 116E-1212-1B

January 1988

UK/FRT 651
30KW HF AUTO-TUNED
LINEAR AMPLIFIER

GENERAL AND TECHNICAL INFORMATION

(Section D)

Ministry of Defence

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Prepared by: Marconi Communication Systems Ltd, Chelmsford

Publications authority ATP/MOD (PE)

Service users should send their comments through
the channel prescribed for the purpose in:

AP 100N-0140 Article 5203 (RN)

AP 100B-01, Order 0504 (RAF)

25 Two additional capacitors are switched into the output valve output circuit by the capacitor assembly (tune fixed). These capacitors, 18C1 and 18C2, are switched into circuit for the lower frequency ranges by switching solenoids 18RLA and 18RLB. For range 1 both of these relays are energized and for ranges 2 and 3, 18RLA alone is energized. Both of these capacitors are connected in series with parasitic suppressor circuits formed by two pairs of shorted parallel resistors 18R1 to 18R4.

26 The coil assembly (tuning) and the coil assembly (loading 1) contain inductors 19L1 and 21L1 respectively. Each of these inductors has eight taps which may be connected to the output of the coil by the range selection switching solenoids. These solenoids are controlled by the range selection module and are energized, to select the required tuning and loading inductance, in accordance with the sequence shown in Table 1. For range 3 and above, the next contact immediately below the first used contact is de-energized.

TABLE 1 TUNING AND LOADING 1 – SOLENOID CONTROL

RANGE NUMBER	FREQUENCY MHz	SOLENOIDS ENERGISED							
		RLA	RLB	RLC	RLD	RLE	RLF	RLG	RLH
1	2 – 2.3								
2	2.3 – 3	*							
3	3 – 4.5		*						
4	4.5 – 6.7	*		*					
5	6.7 – 10	*	*		*				
6	10 – 15	*	*	*		*			
7	15 – 20	*	*	*	*		*		
8	20 – 25	*	*	*	*	*		*	
9	25 – 30	*	*	*	*	*	*		*

* solenoid energised

27 The capacitor assembly (centre) contains the central tuning capacitor for the rf output pi circuits. In addition to this capacitor this assembly contains a stepping motor together with position sensing and zero detector circuits.

28 Tune data for the centre capacitor is provided by the servo module (07ML14). This module generates a four-phase, stepping waveform to drive the tuning motor 20M1. The tuning capacitor 20C1 is driven by this motor to a preset position dependent on range and frequency. This position is detected by a comparator in the servo module. Since this capacitor is a vacuum operated device it returns to maximum capacitance when the power supply is switched off. At the start of the tune sequence this capacitor is driven to minimum capacitance, as sensed by the zero detector circuit 20X1; the motor then reverses its direction of rotation to drive the capacitor to its tune position. The position sensing circuit 20RV1 provides an analogue indication of the capacitor setting for display on the front panel meter of the auto-tune control module.

39 Blocking diodes 07D1 to 07D27 prevent the +48V switching voltage, provided by range selection module, interacting with the +10V holding voltage, provided by the power supply. Diodes 07D28 to 07D31 ensure that the solenoids in the coil assembly (ht feed) are only activated on the higher frequency ranges.

40 The start interlock chain is shown on Fig D1-6. This chain must be complete before a 0V (ET22 earth) input is presented to $\pm 12V$ power supply, on TS1.5. The $\pm 12V$ control supplies are enabled by this input. Should this chain be broken then the equipment is disabled until interlock path is restored. The $\pm 12V$ control supplies are then automatically restored following a short delay generated by the $\pm 12V$ power supply unit.

41 The $\pm 12V$ distribution is shown on Fig D1-8. This diagram shows the distribution of these supplies from the $\pm 12V$ supply to the units and modules. Also shown are the external $\pm 12V$ supply connections, these supplies are taken via fuses 06FS1 and 06FS2 in the control frame. Speed control resistors 07R2 to 07R5 set the speed of the servo motors controlled by the four servo modules ML12 to ML15.

42 The interconnections for the control modules in the control assemblies (units 06 and 07) are shown in Fig D1-9 to D1-13. These diagrams show all of these interconnections, with the exception of the start interlock chain and $\pm 12V$ distribution, including the interface between the two control assemblies and the connectors for the cabinet wiring.

43 Details of the point-to-point wiring between the connectors of the control frame assemblies and the amplifier cabinets are shown in Fig D1-14 to D1-22. These diagrams show the source or destination in the amplifier cabinets for these connections. Details of the wiring between these connections and the modules of the control frame are duplicated on these diagrams for clarity. Tables 2 to 4 show the connections for the two control frame assemblies and their functions.

> TABLE 2 CONTROL FRAME ASSEMBLY (UNIT 06) CONNECTORS <

Connector	Destination	Function	Pins
SKA	1SKA	External control	34
SKB	1SKB	External control	34
SKC	1SKC	External control	34
SKD	1SKC	External control	34
SKE	10SKA	Metering	50
PLF	-	Interframe wiring	75
SKG	-	Various	75
SKAC	04SKJ	Contactors control	26
TS1	05TS1	$\pm 12V$ supply	12
> SKAD	01SKF	RF input from Drive to 06ML02	
SKAE	07SKW	RF input path, 06ML02 to 07ML17	

47 The switch is operated by a key-controlled lever mounted at the top, front of the rf cabinet, and connected to the switch by an articulated shaft.

48 The key required is one of the 'A' keys from the earth switch/isolator panel of the amplifier. The key must be inserted for the feeder earth switch to be turned to its OFF position, when it is then trapped.

EARTHING WAND

49 The earthing wand is provided as an adjunct to the amplifier safety equipment. It is mounted on the top of the power supply cabinet and connected by a flexible cable to an earth terminal thereon. When gaining access to the amplifier following a period of operation, this wand should be used to ensure that all the high voltage capacitors are fully discharged before commencing any maintenance work.

SMOKE DETECTOR W10-4745-01)

50 In addition to the smoke detector assembly described in Para 30, a second assembly (W10-4745-01) is fitted to the top of Cabinet 02 to monitor the air exhausted from the Cabinet. When the detector senses the presence of smoke an alarm circuit is triggered, and both the Xenon beacon and the red Tx Trip indicator light. The equipment is isolated from the 3-phase mains supply. External alarms may be activated depending on individual site connections, refer to local documentation.

MAINTENANCE

51 Alignment and setting up instructions for the rf, supply and control functions of the amplifier will be found in Sub-sect B3 of this manual. In common with all high power amplifiers general cleanliness is an important consideration of maintenance. A further aspect is the 'good housekeeping' approach in which, whenever there is access to the cabinet assembly for a particular task a general inspection is also performed paying attention the following aspects:

The correct mechanical fit and condition of sub-units, components, connectors and wiring interconnections.

The absence of accumulations of dust, remove any which may become the source of a fault condition.

Finally, the correct replacement of all panels, guards, high voltage screens and protective covers before the amplifier is returned to service.

Earth switch/isolator

52 Before re-applying the mains supply to the amplifier following maintenance which involves the high voltage circuits, check the mechanical and electrical operation of the earth switch/isolator. Pay attention to the following aspects:

Cable terminations, both at the earth switch and at the component(s) being earthed.
The condition of the earth switch contacts.

The mechanical interlock i.e. with one or more panel keys removed, the earth switch/isolator is locked in the EARTHED position and with one or both of the external isolator/feeder switch keys removed the EARTHED position cannot be selected.

The electrical operation to prove that all the relevant components are earthed, see Fig D1-2 and Fig D1-4.

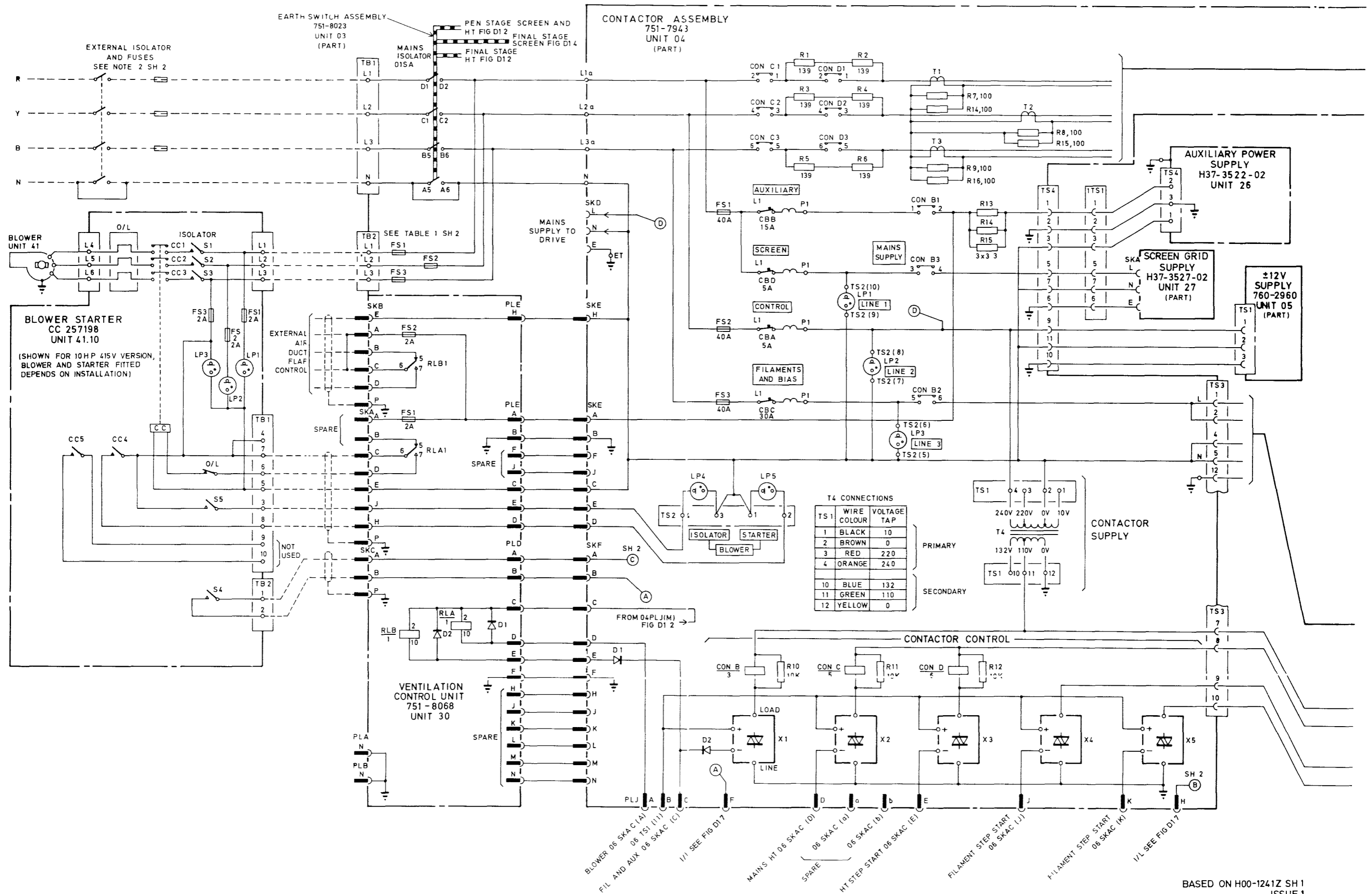


Fig D1-1

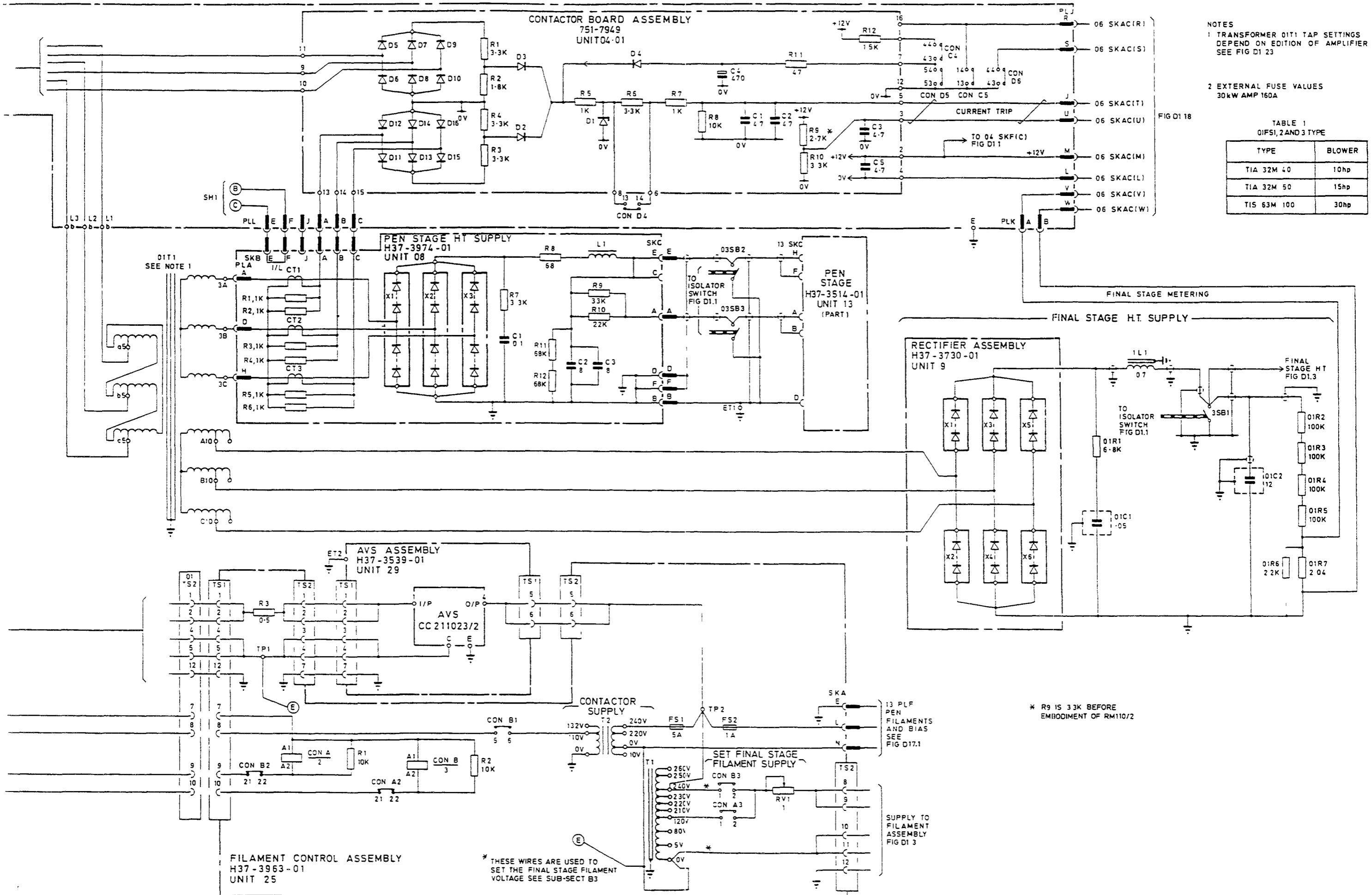
Sub-sect D1

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UK/FRT 651 amplifier : mains distribution circuit diagram

Fig D1-1

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NOTES
 1 TRANSFORMER 01T1 TAP SETTINGS DEPEND ON EDITION OF AMPLIFIER SEE FIG D1 23
 2 EXTERNAL FUSE VALUES 30kW AMP 160A

TABLE 1
 O1FS1, 2 AND 3 TYPE

TYPE	BLOWER
T1A 32M 40	10hp
T1A 32M 50	15hp
T1S 63M 100	30hp

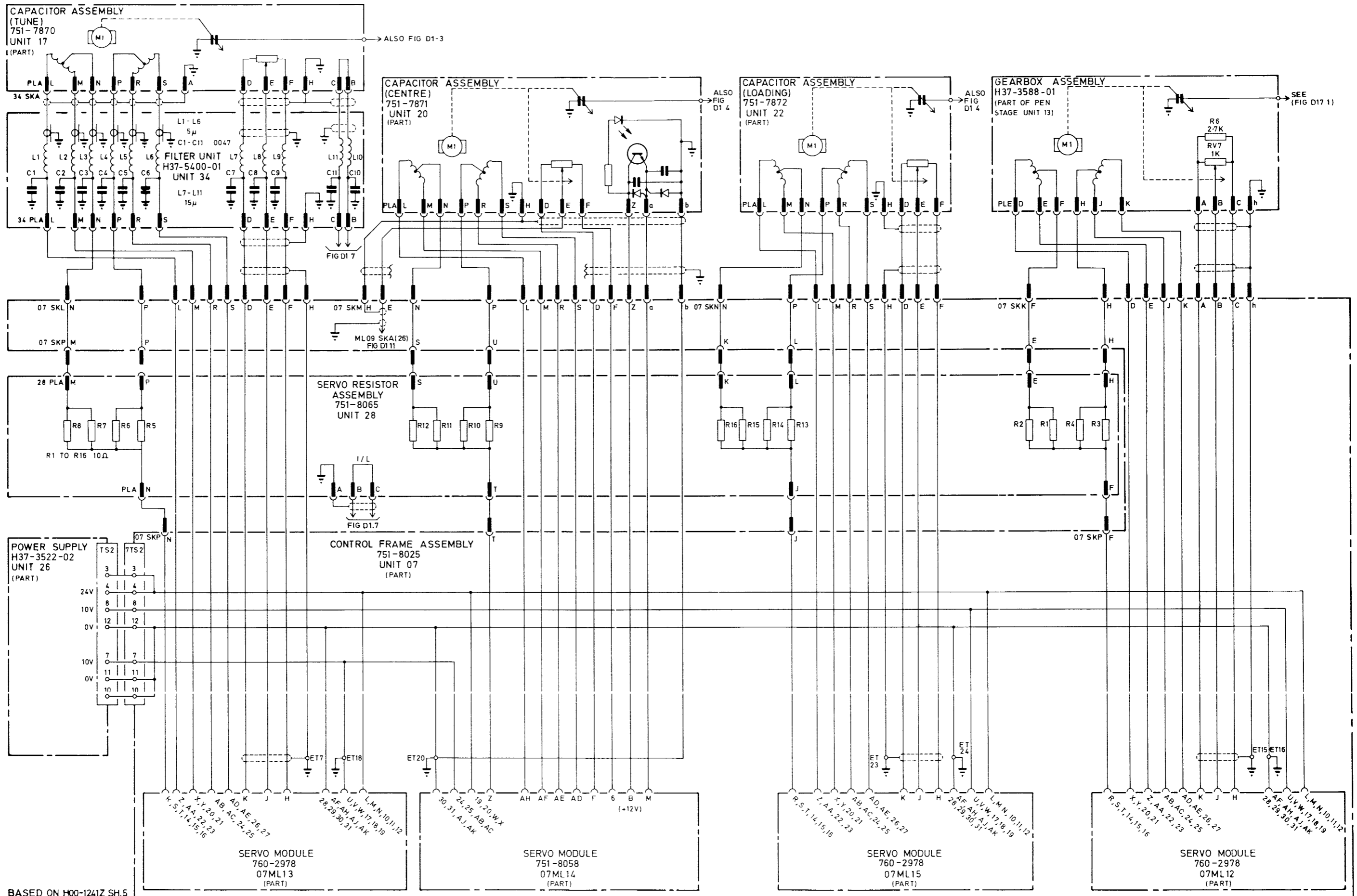
BASED ON H00-1241Z SH 2 ISSUE 1

Fig D1-2

UK/FRT 651 amplifier : mains distribution : circuit diagram

Fig D1-2

Sub-sect D1



BASED ON H00-1241Z SH.5
ISSUE 1

Fig D1-5

UK/FRT 651 amplifier : servo .circuit diagram

Fig D1-5

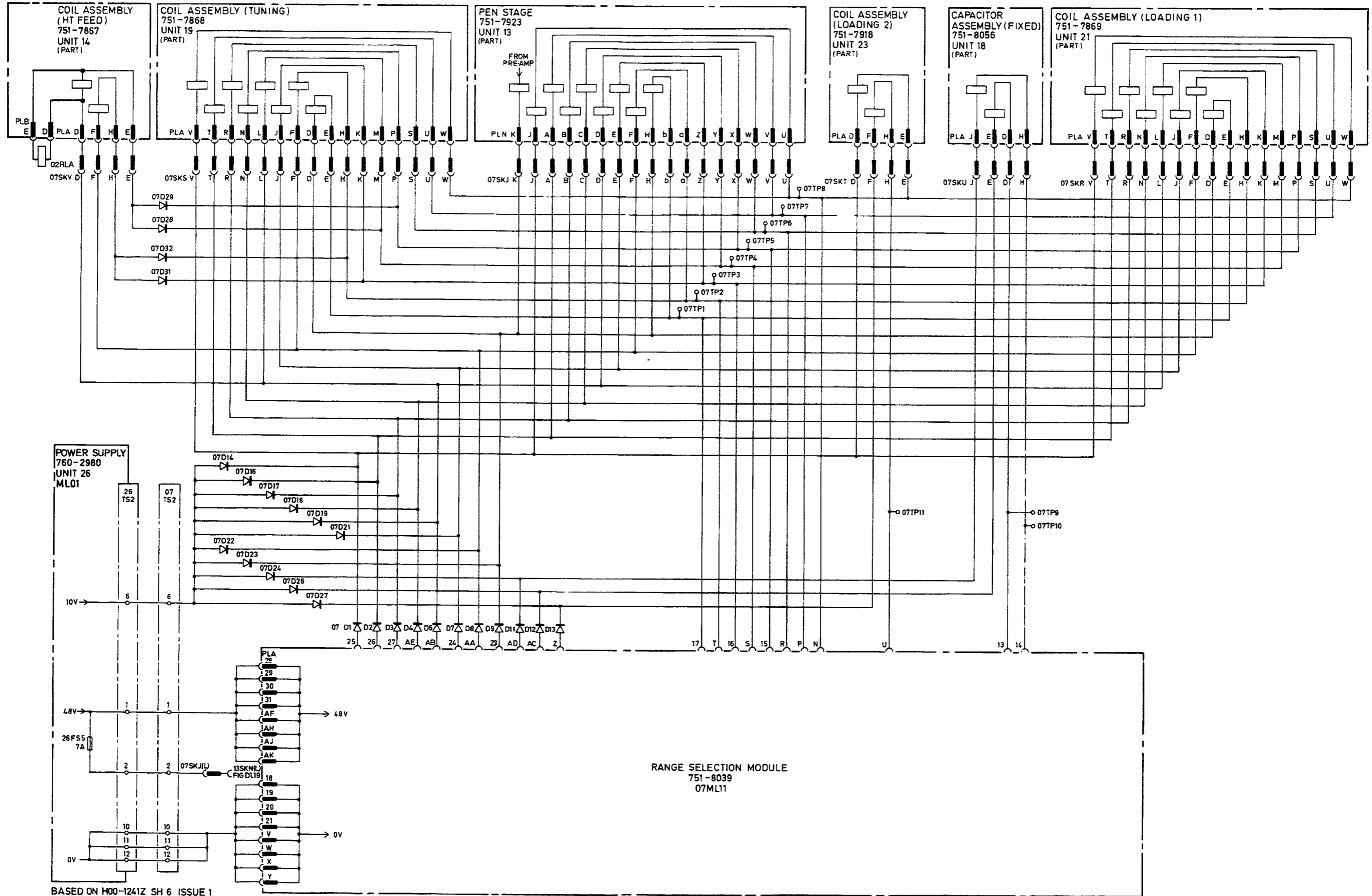
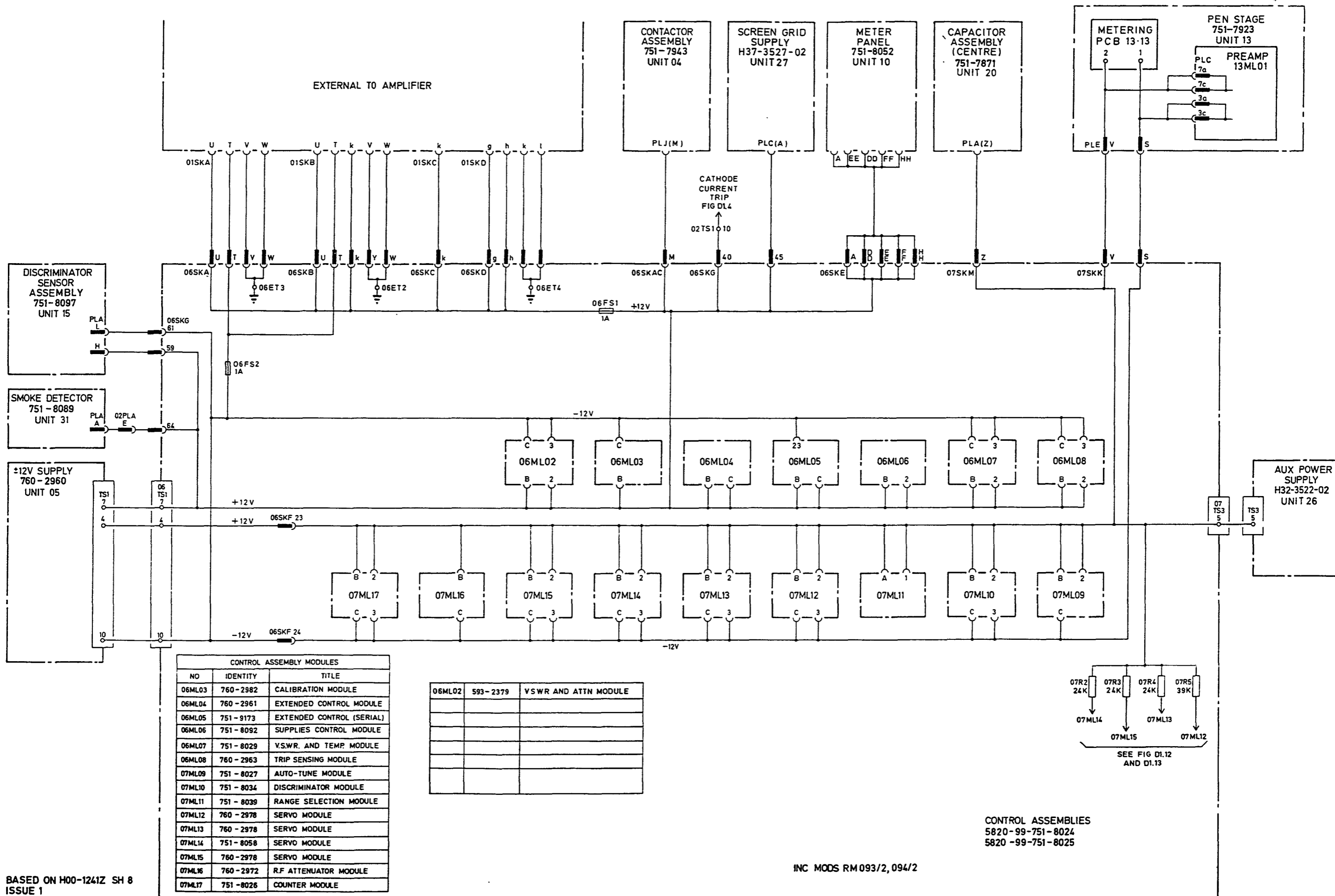


Fig D1-6

UK/FRT 651 amplifier : range selection : circuit diagram

Dec 93 (Amdt 14)

Fig D1-6
Sub-sect D1
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CONTROL ASSEMBLY MODULES		
NO	IDENTITY	TITLE
06ML03	760-2982	CALIBRATION MODULE
06ML04	760-2961	EXTENDED CONTROL MODULE
06ML05	751-9173	EXTENDED CONTROL (SERIAL)
06ML06	751-8092	SUPPLIES CONTROL MODULE
06ML07	751-8029	V.S.W.R. AND TEMP MODULE
06ML08	760-2963	TRIP SENSING MODULE
07ML09	751-8027	AUTO-TUNE MODULE
07ML10	751-8034	DISCRIMINATOR MODULE
07ML11	751-8039	RANGE SELECTION MODULE
07ML12	760-2978	SERVO MODULE
07ML13	760-2978	SERVO MODULE
07ML14	751-8058	SERVO MODULE
07ML15	760-2978	SERVO MODULE
07ML16	760-2972	R.F. ATTENUATOR MODULE
07ML17	751-8026	COUNTER MODULE

06ML02	593-2379	VSWR AND ATTN MODULE

CONTROL ASSEMBLIES
5820-99-751-8024
5820-99-751-8025

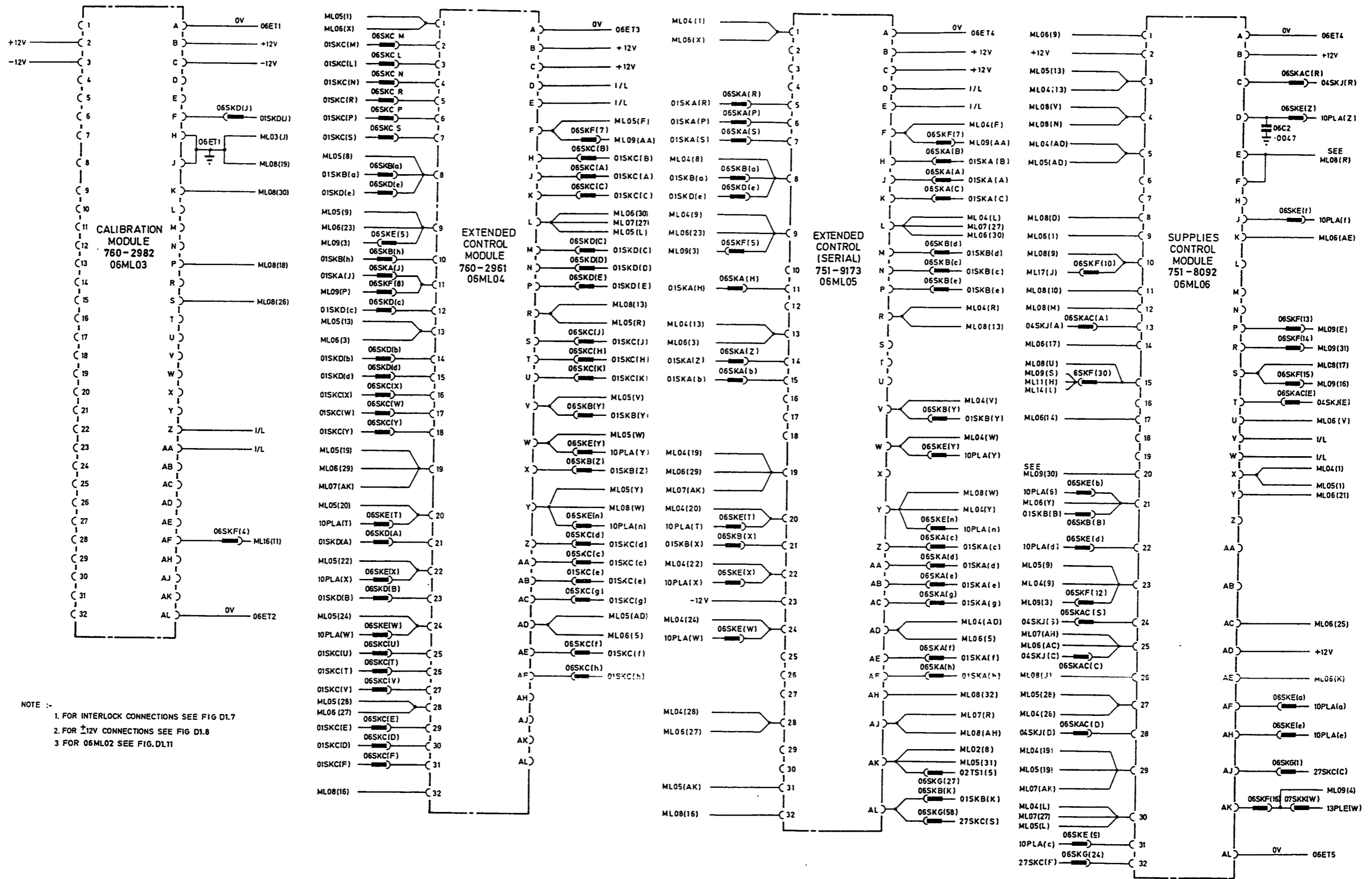
INC MODS RM 093/2, 094/2

BASED ON H00-1241Z SH 8
ISSUE 1

Fig D1-8

UK/FRT 651 amplifier: ±12V distribution

Fig D1-8

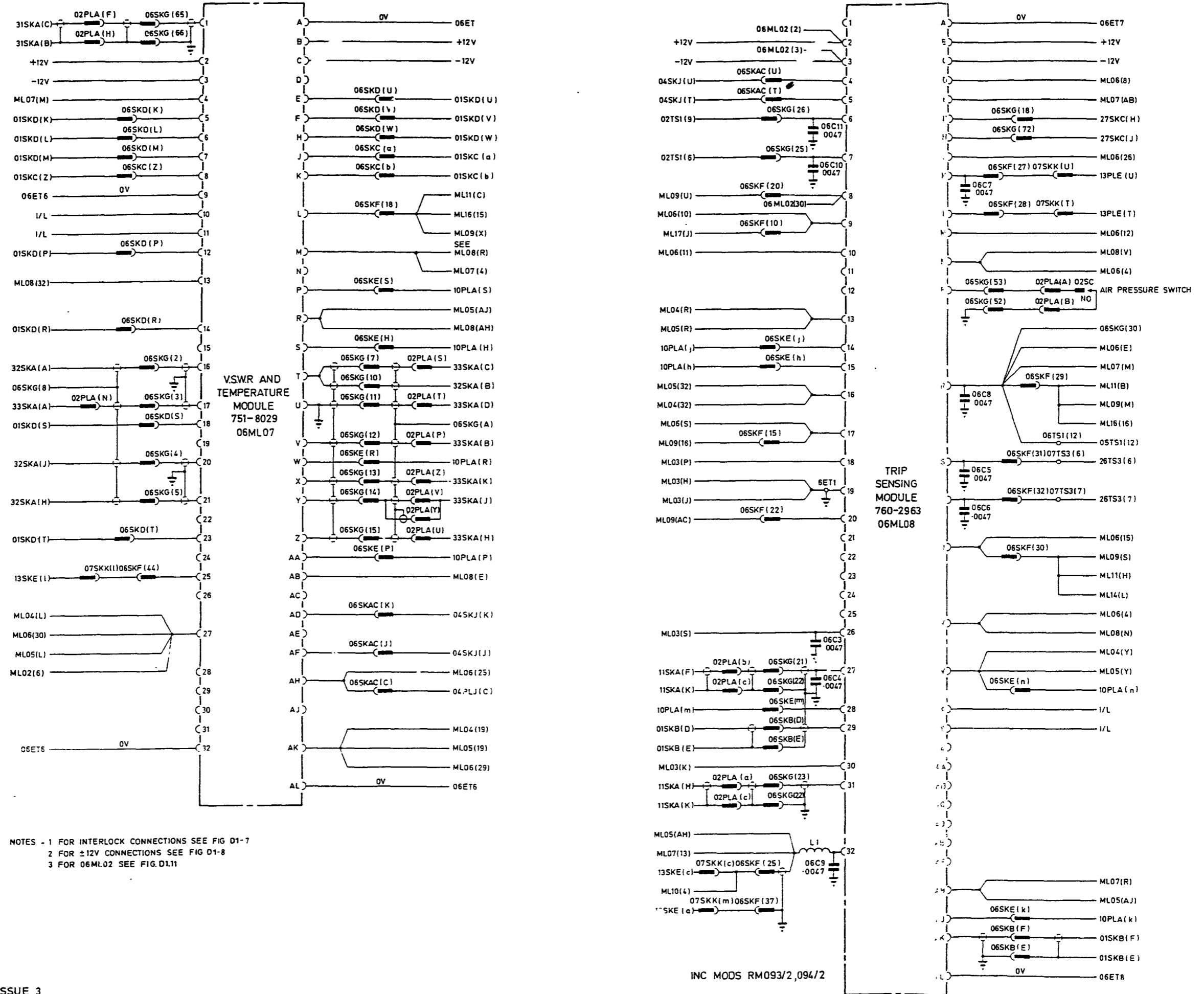


NOTE :-
 1. FOR INTERLOCK CONNECTIONS SEE FIG D1.7
 2. FOR ±12V CONNECTIONS SEE FIG D1.8
 3. FOR 06ML02 SEE FIG.D1.11

BASED ON H00-1241Z SH 9 ISSUE 1
 Fig D1-9

UK/FRT 651 amplifier : interconnection diagram

INC MODS RM 093/2, 094/2



BASED ON H00-1241Z SH 10 ISSUE 3

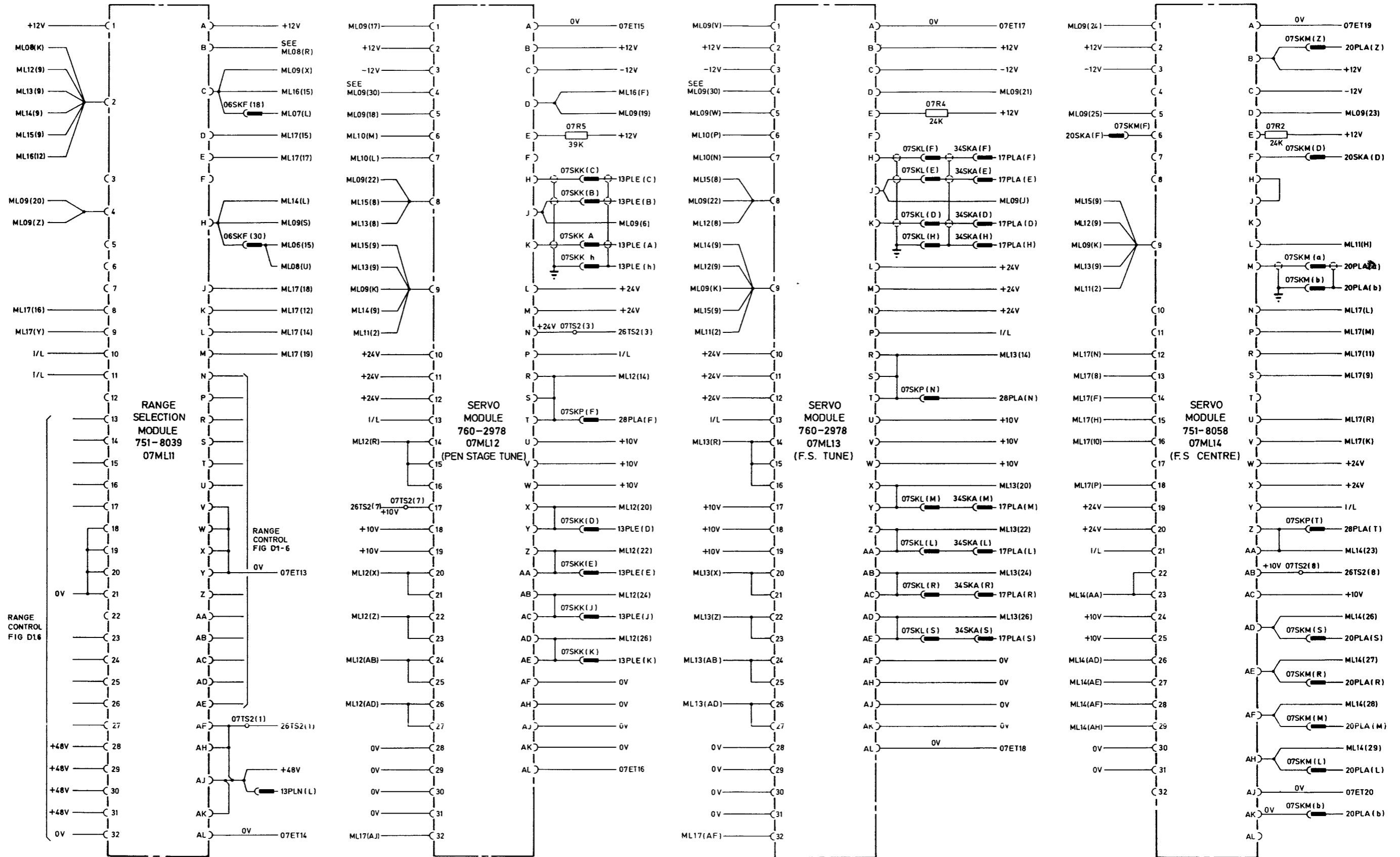
Fig D1-10

UK/FRT 651 amplifier : interconnection diagram

Fig D1-10

Sub-sect D1

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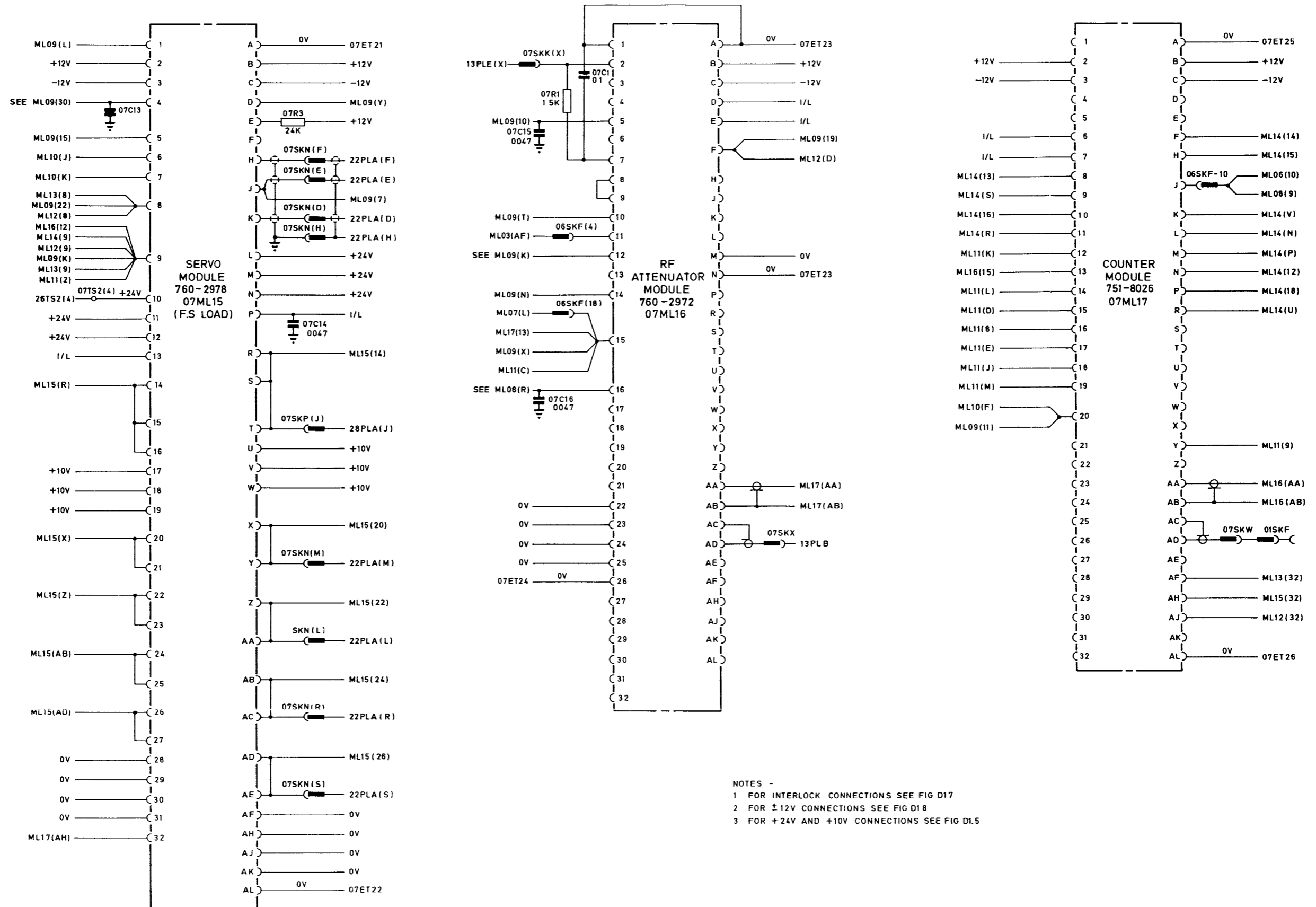


NOTES - 1 FOR INTERLOCK CONNECTIONS
 SEE FIG D1 7
 2 FOR ±12V CONNECTIONS SEE
 FIG D1 8
 3 FOR +24V AND +10V CONNECTIONS
 SEE FIG D1.5

BASED ON H00-1241Z SH 12 ISSUE 1

Fig D1-12

UK/FRT 651 amplifier : interconnection diagram

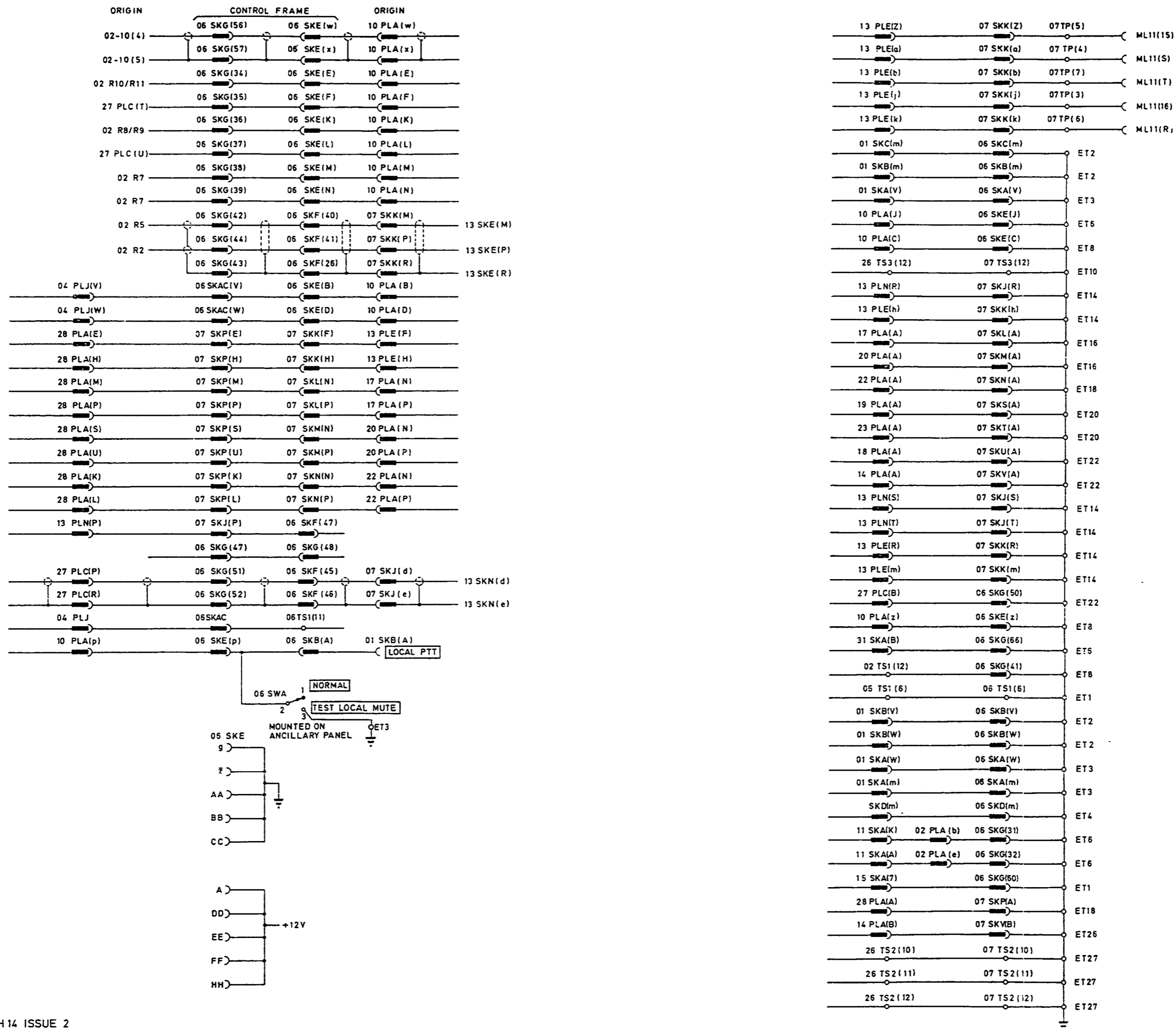


NOTES -
 1 FOR INTERLOCK CONNECTIONS SEE FIG D17
 2 FOR ±12V CONNECTIONS SEE FIG D18
 3 FOR +24V AND +10V CONNECTIONS SEE FIG D1.5

BASED ON H00-1241G SH 13 ISSUE 1

Fig D1-13

UK/FRT 651 amplifier : interconnection diagram



INC. MOD RM074/1

BASED ON H00-1241Z SH 14 ISSUE 2

Fig D1-14

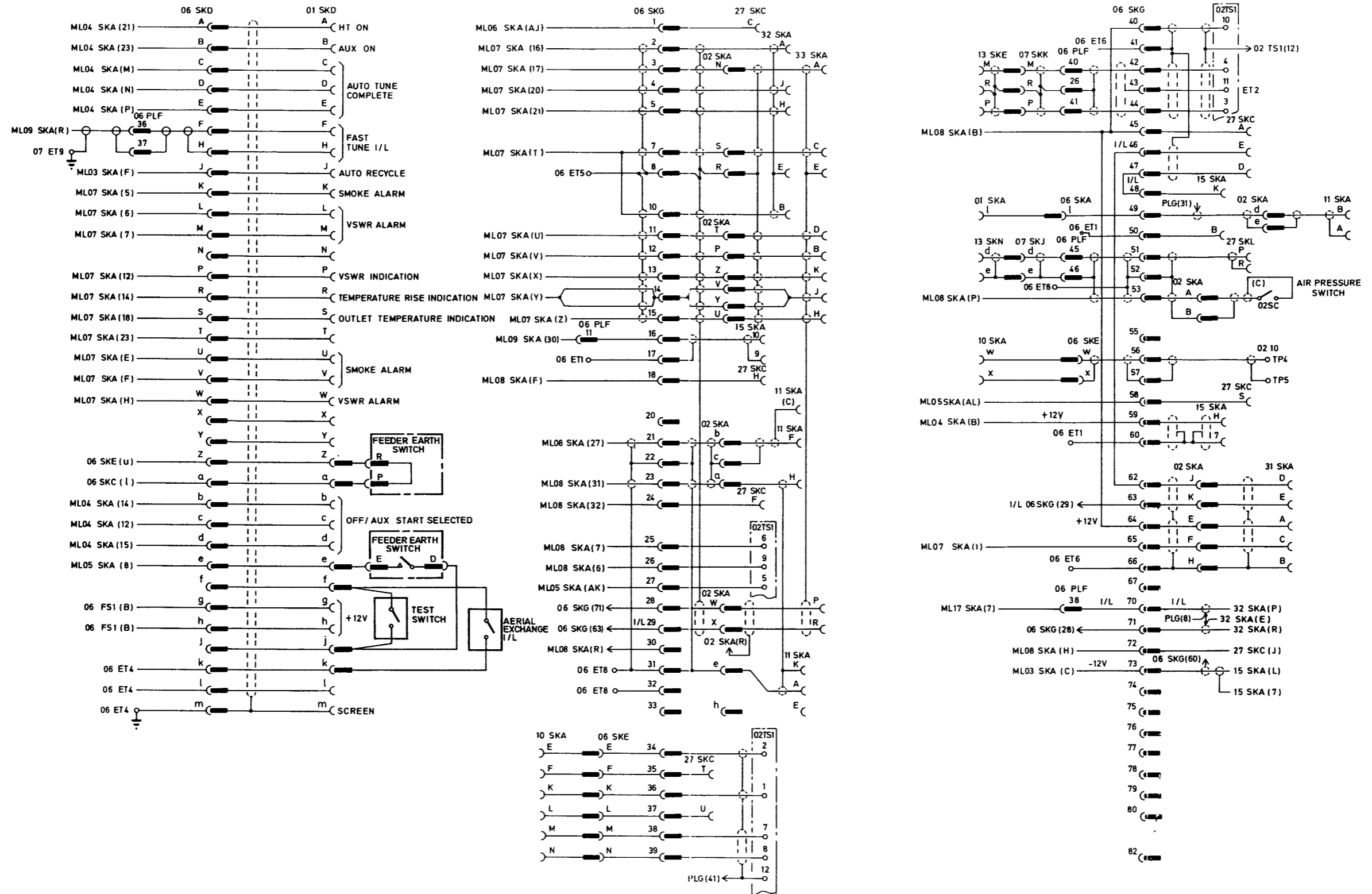
UK/FRT 651 amplifier : interconnection diagram

Nov 92 (Amdt 9)

Fig D1-14

Sub-sect D1

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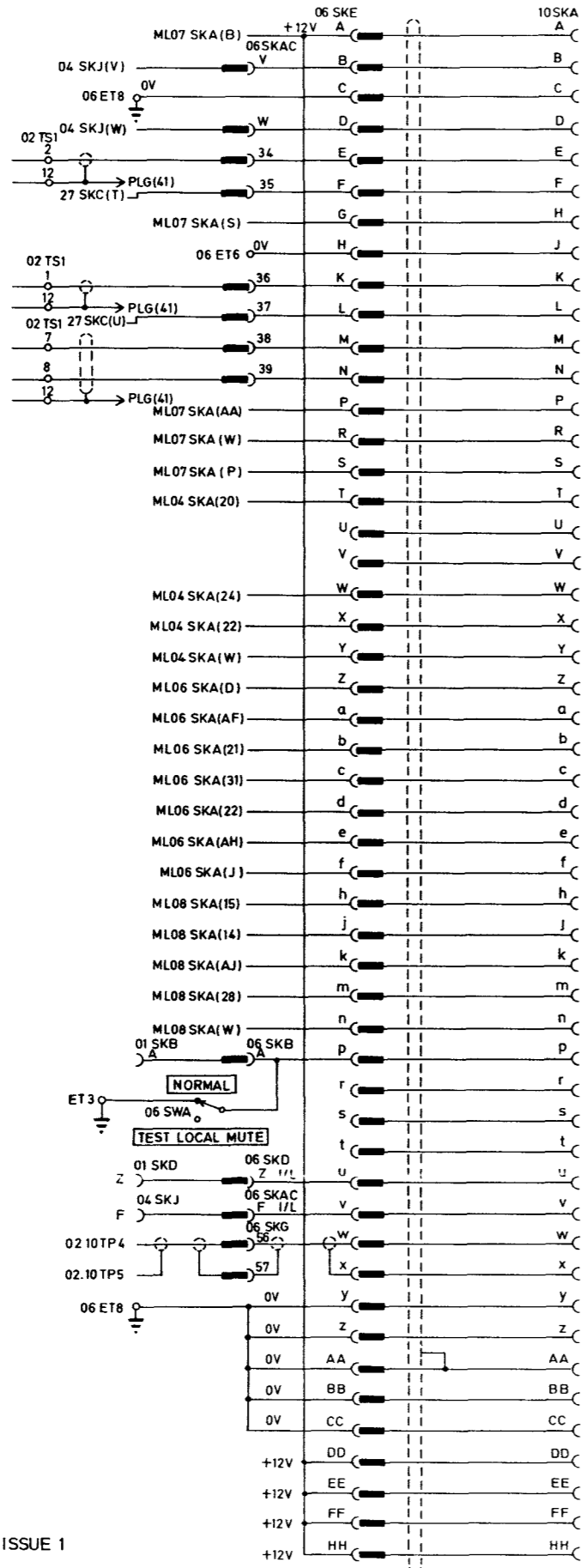
BASED ON H00-1241Z SH 16 ISSUE 2

Fig D1-16

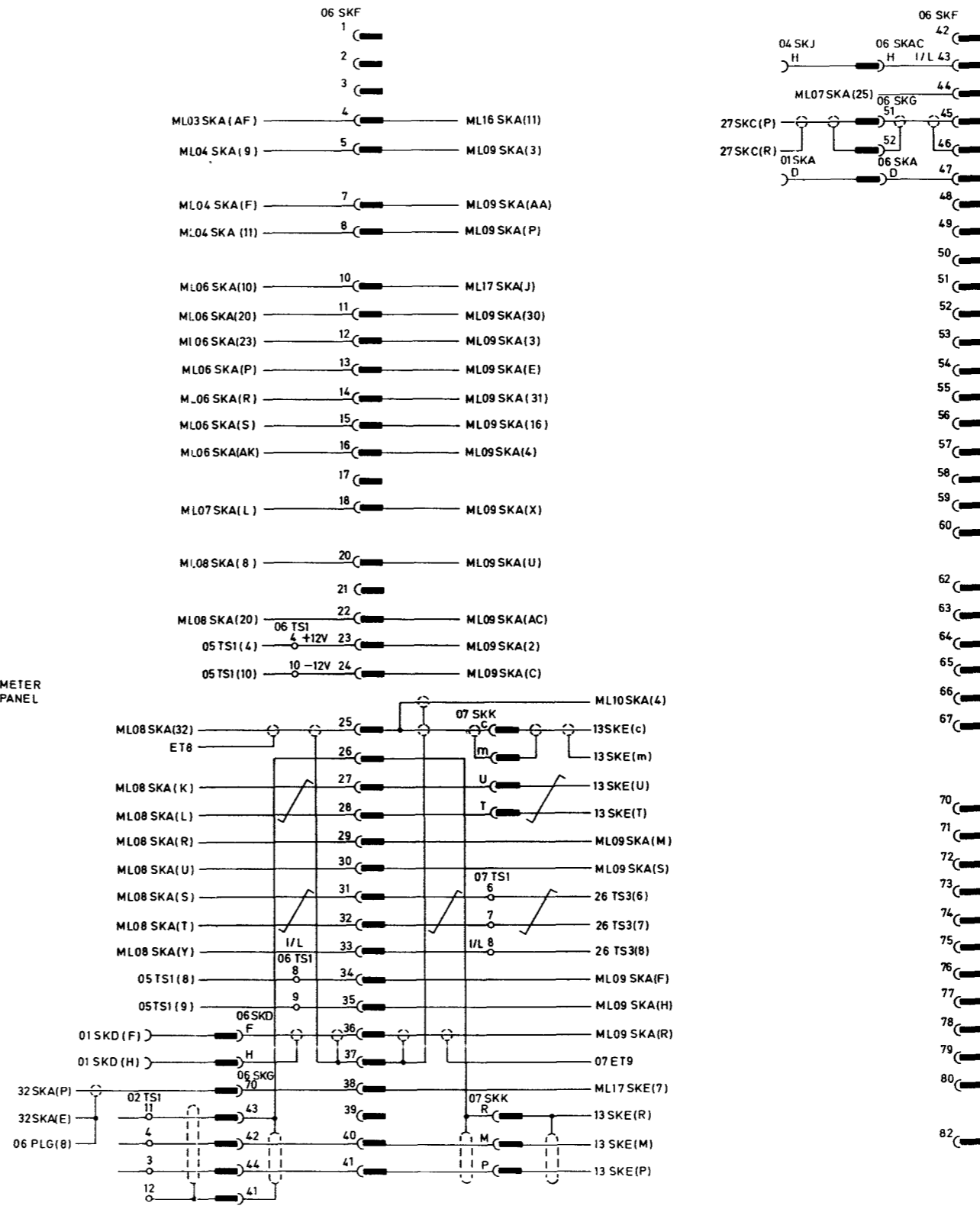
UK/FRT 651 amplifier interconnection diagram

Jan 88

Fig D1-16



METER PANEL



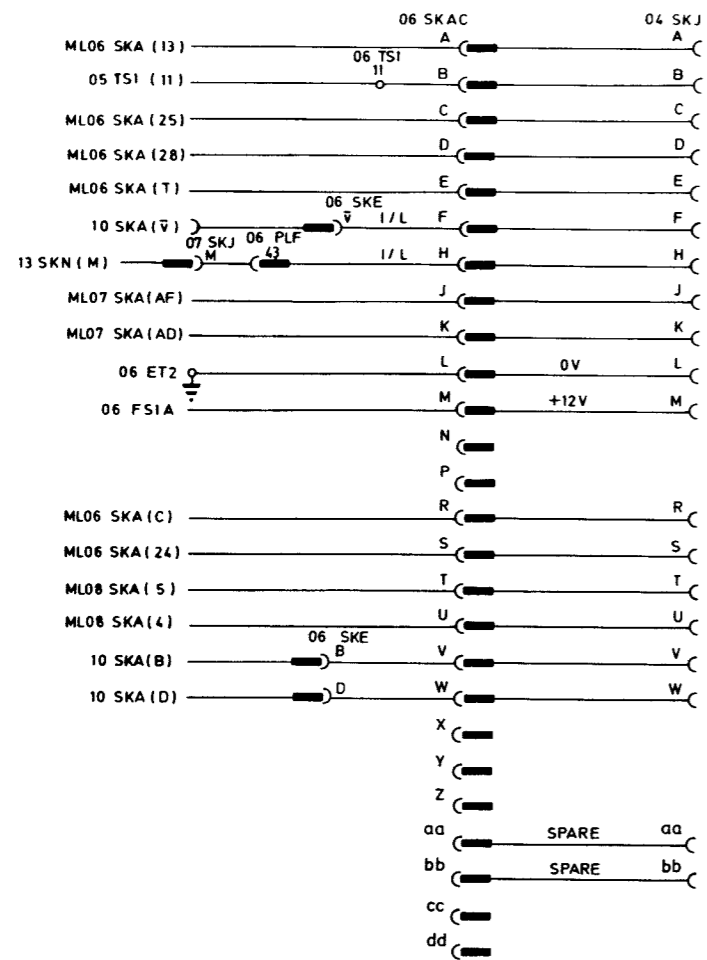
BASED ON H00-1241Z SH 17 ISSUE 1

Fig D1-17

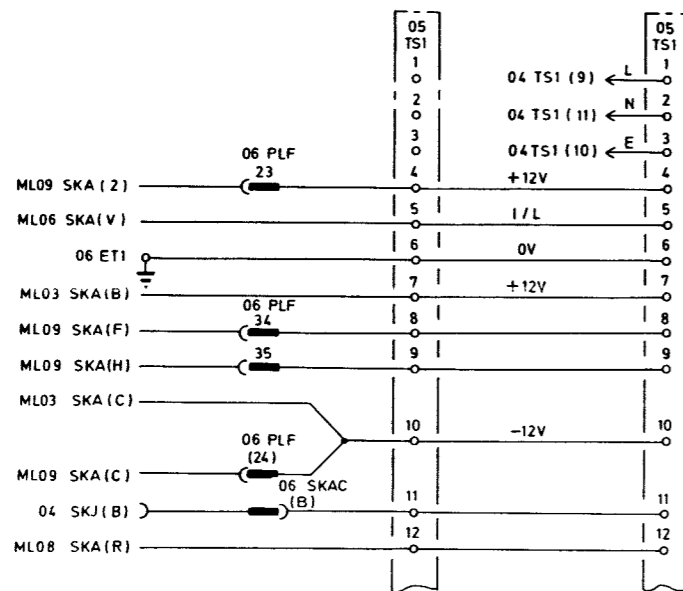
Jan 88

UK/FRT 651 amplifier : interconnection diagram

Fig D1- 17



CONTACTOR CONTROL
FIG D1.2



BASED ON H00-1241Z SH18 ISSUE 1

Fig D1-18

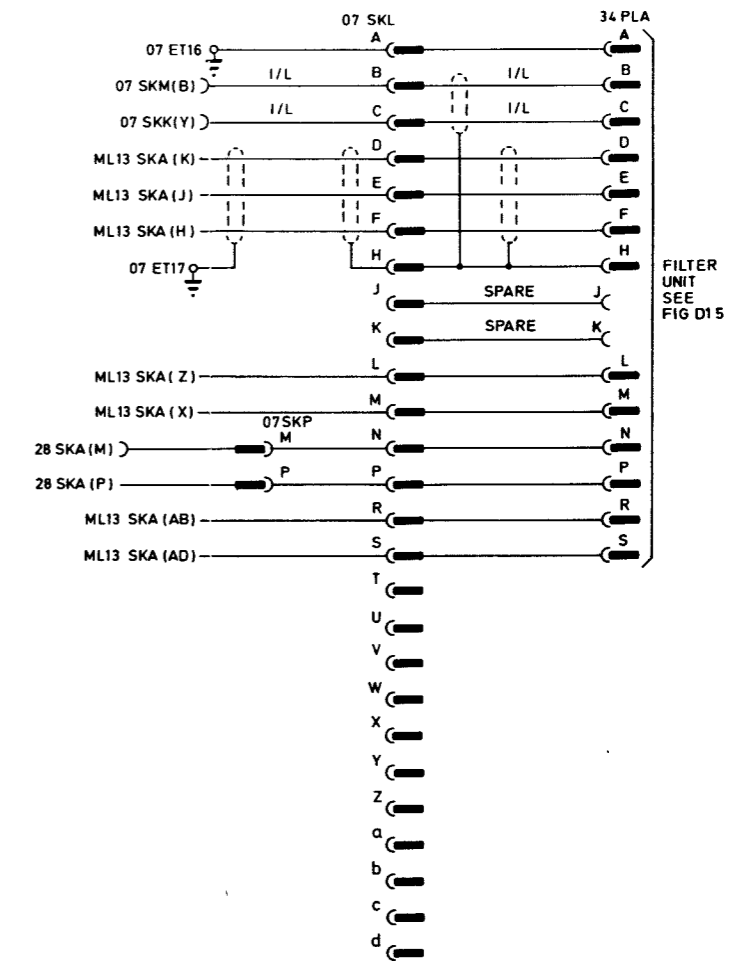
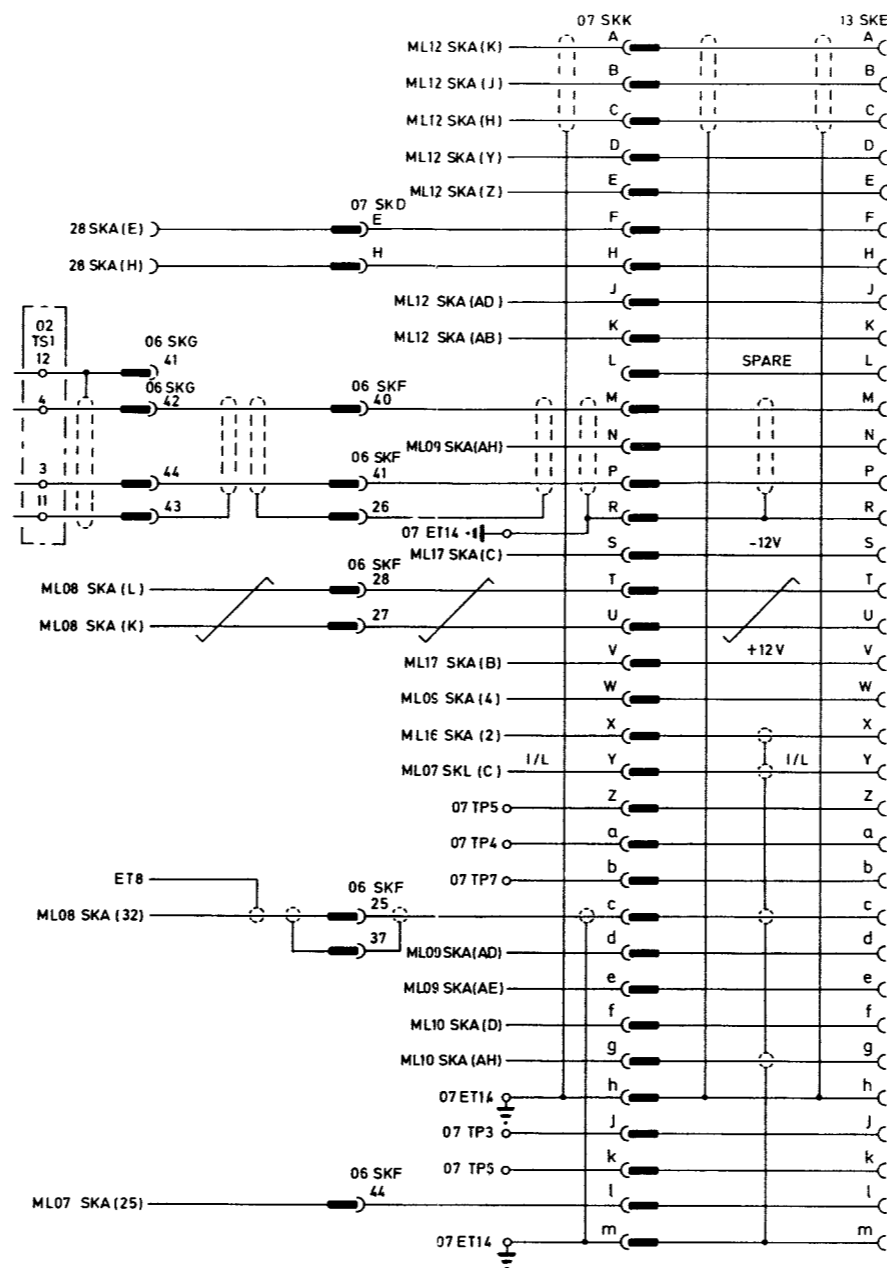
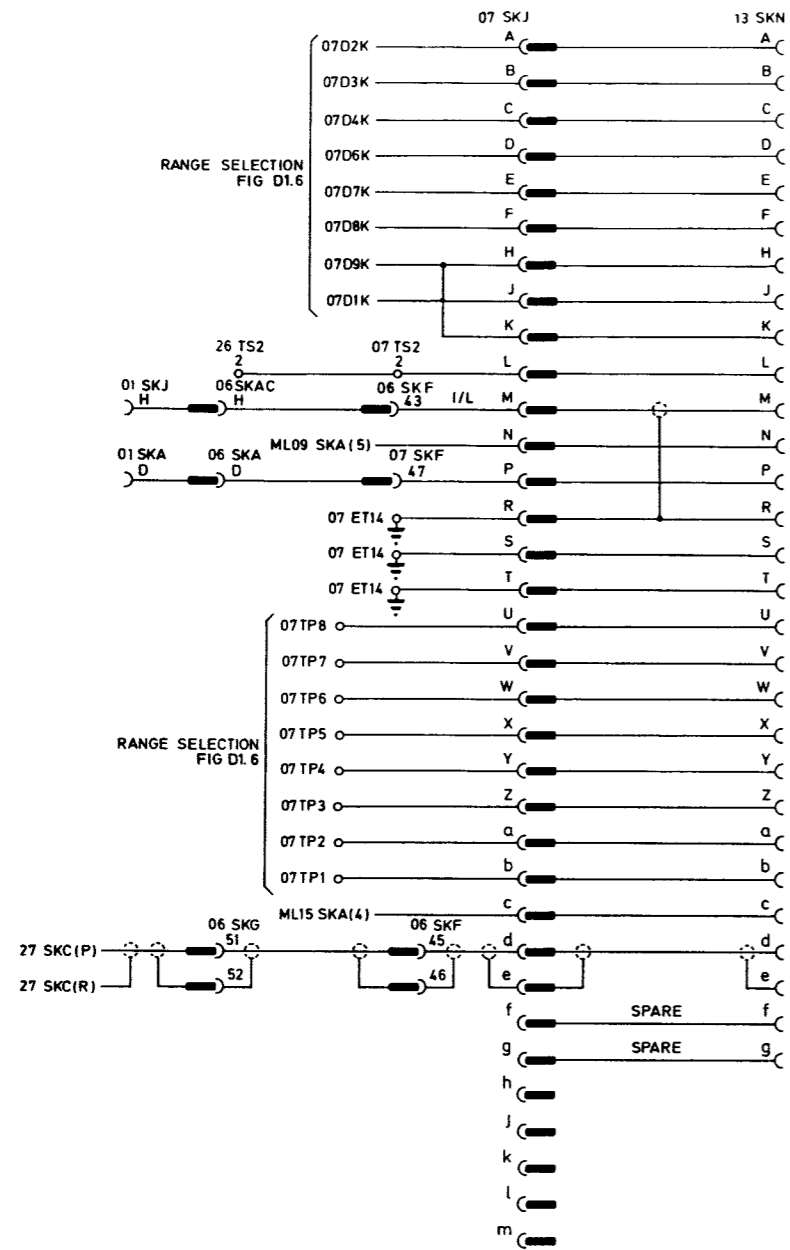
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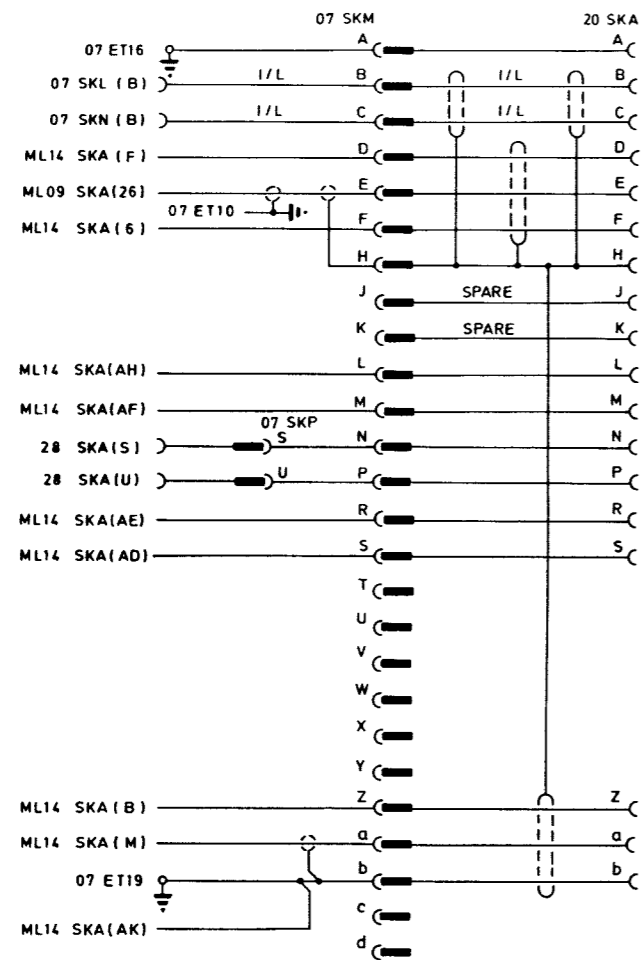
UK/FRT 651 amplifier : interconnections diagram

Fig D1 .18

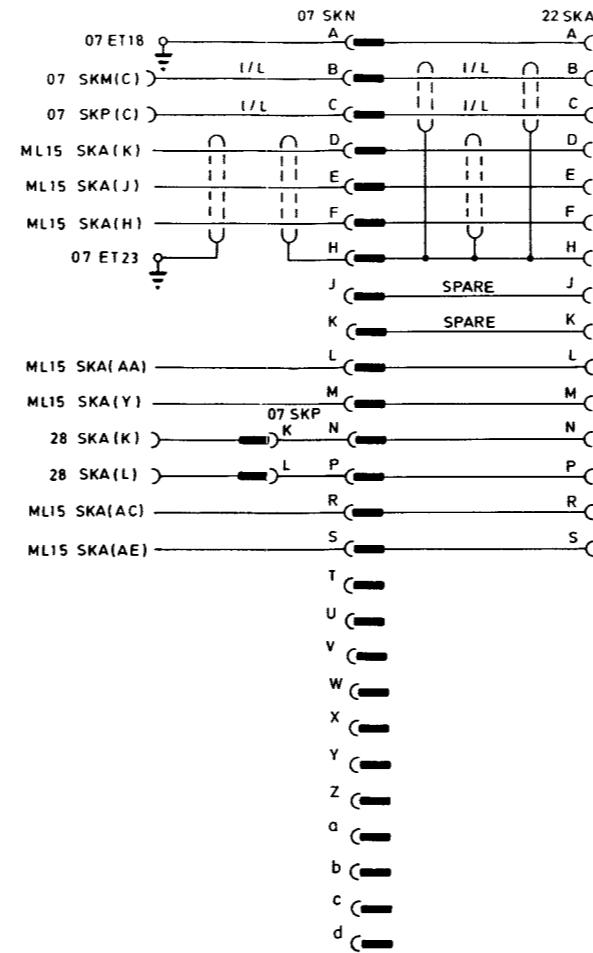
Sub-sect D1

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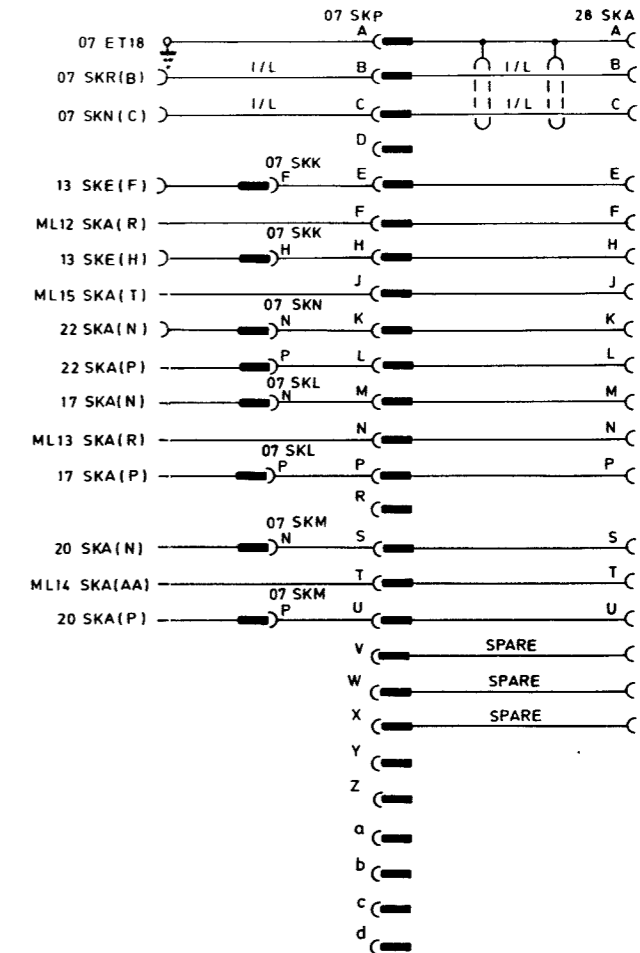




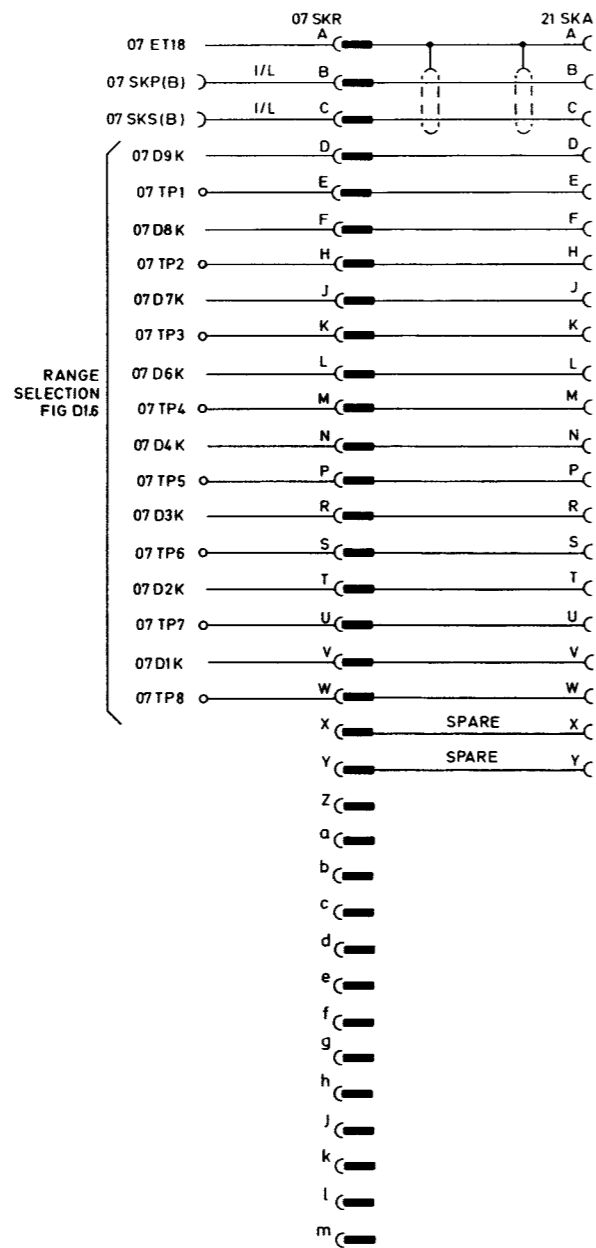
CAPACITOR ASSEMBLY (CENTRE) FIG D15



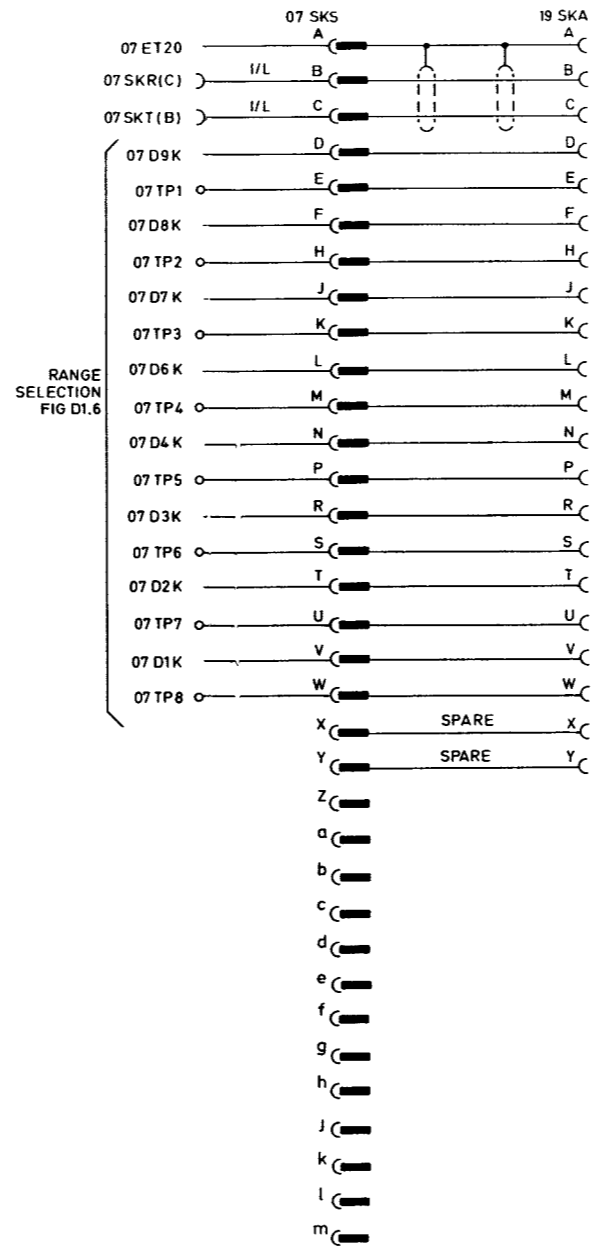
CAPACITOR ASSEMBLY (LOADING) FIG D15



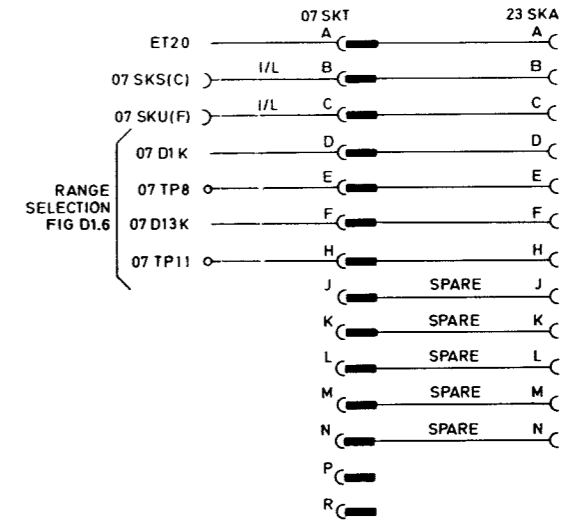
SERVO-RESISTOR ASSEMBLY FIG D15



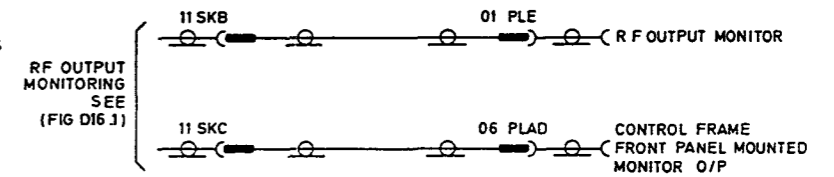
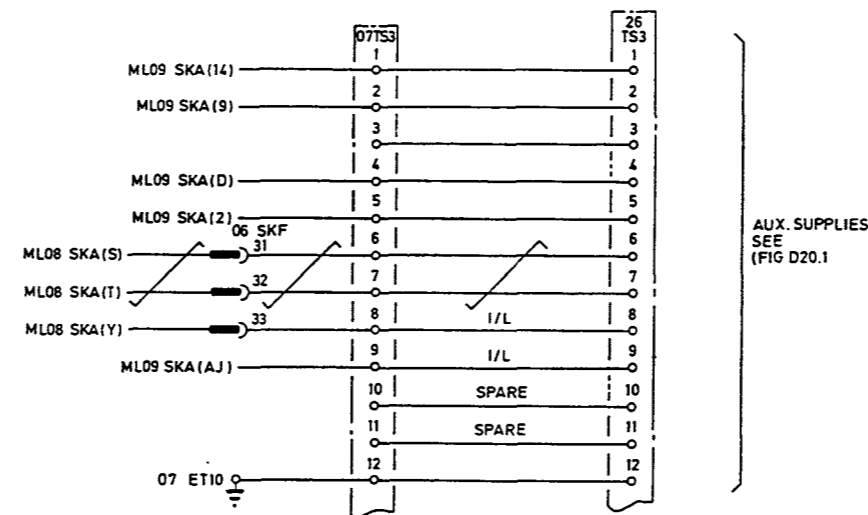
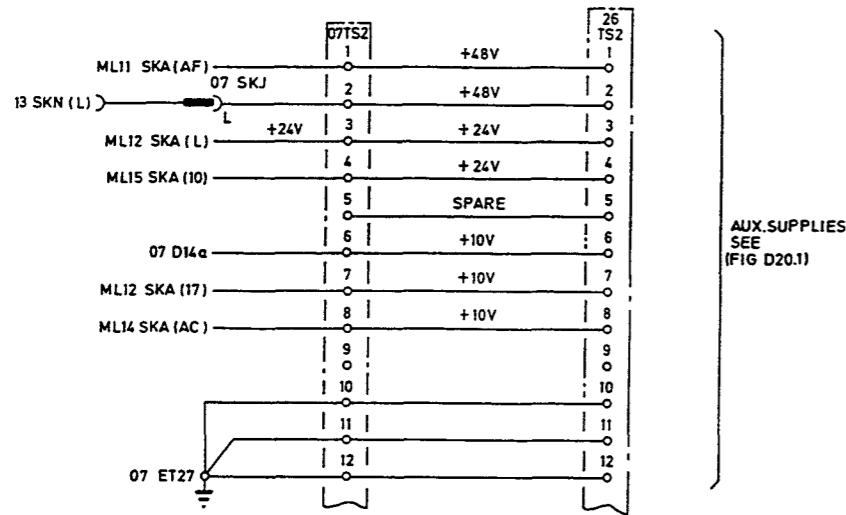
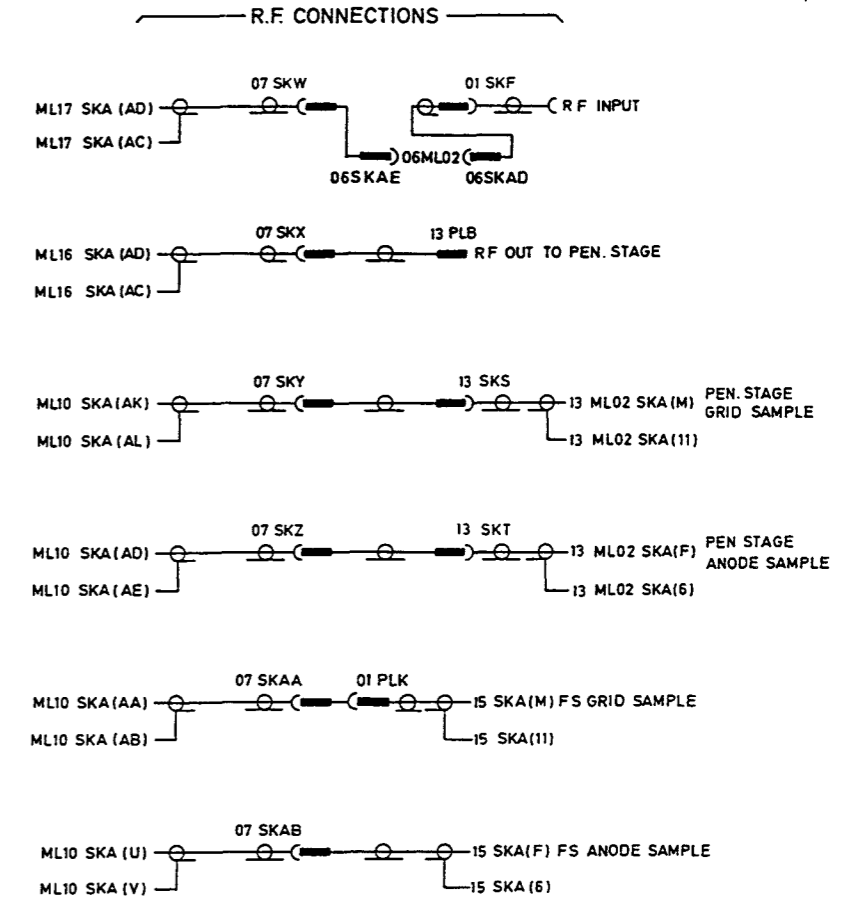
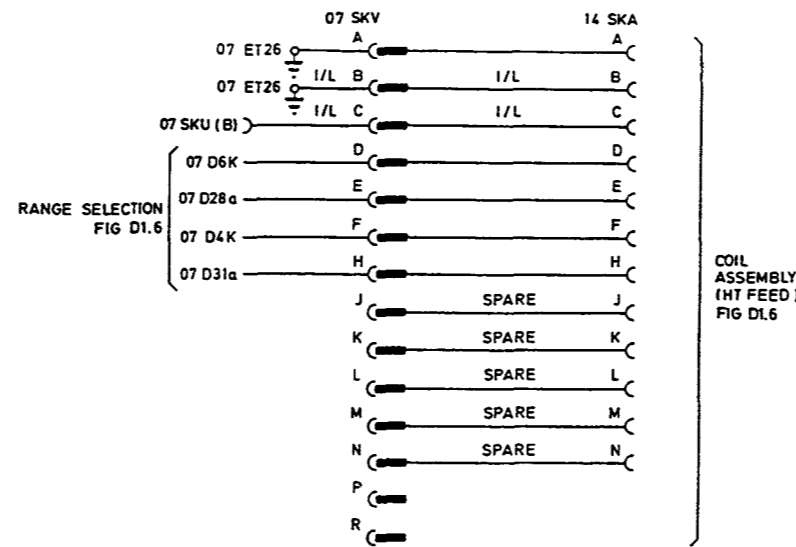
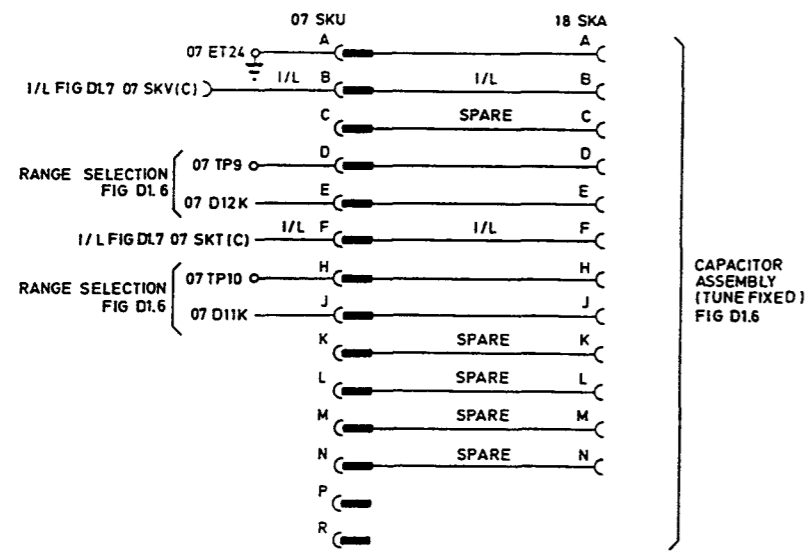
COIL ASSEMBLY (LOADING 1)



COIL ASSEMBLY (TUNING)

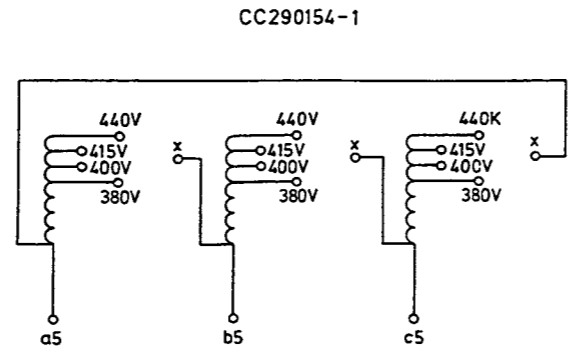


COIL ASSEMBLY (LOADING 2)

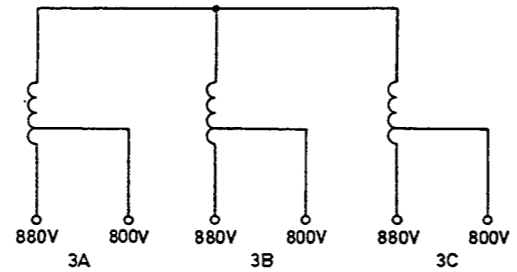


INC MODS RM093/2,094/2

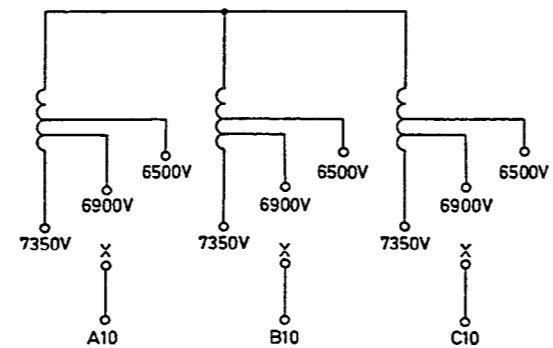
30 kW
 LV
 SUPPLY ACROSS a5, b5, c5
 FOR 440V INPUT LINK x TO 440V
 FOR 415V INPUT LINK x TO 415V
 FOR 400V INPUT LINK x TO 400V
 FOR 380V INPUT LINK x TO 380V



TERTIARY
 FOR 800V - TERMINAL 3A 800V ETC
 FOR 880V - TERMINAL 3A 880V ETC



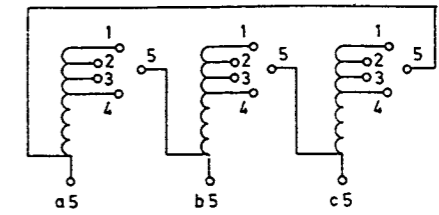
HV
 OUTPUT ACROSS A10, B10, C10
 FOR 6500V OUTPUT LINK x-6500V ETC
 FOR 6900V OUTPUT LINK x-6900V ETC
 FOR 7350V OUTPUT LINK x-7350V ETC



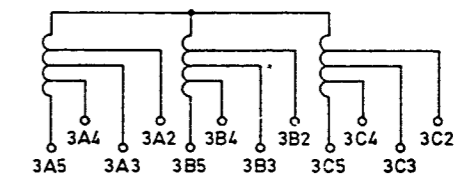
PRE MOD RM077/3

30kW/50kW
 LV
 SUPPLY ACROSS a5, b5, c5
 FOR 440V INPUT LINK 5-1
 FOR 415V INPUT LINK 5-2
 FOR 400V INPUT LINK 5-3
 FOR 380V INPUT LINK 5-4
 IN THREE POSITIONS

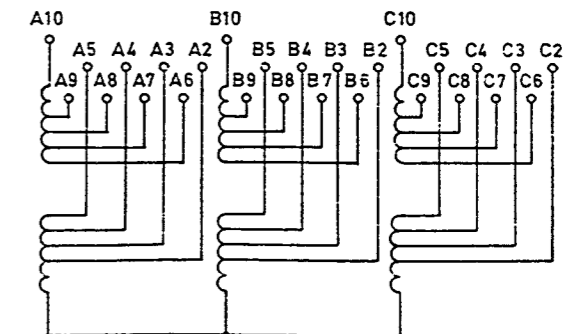
CC290182-1



TERTIARY
 800V ACROSS 3A2, 3B2, 3C2
 880V ACROSS 3A3, 3B3, 3C3
 1050V ACROSS 3A4, 3B4, 3C4
 1150V ACROSS 3A5, 3B5, 3C5



HV
 OUTPUT ACROSS A10, B10, C10
 FOR 6500V OUTPUT LINK A2-A9 ETC
 FOR 6900V OUTPUT LINK A2-A8 ETC
 FOR 7350V OUTPUT LINK A3-A8 ETC
 FOR 8000V OUTPUT LINK A4-A7 ETC
 FOR 8400V OUTPUT LINK A5-A7 ETC
 FOR 8800V OUTPUT LINK A5-A6 ETC

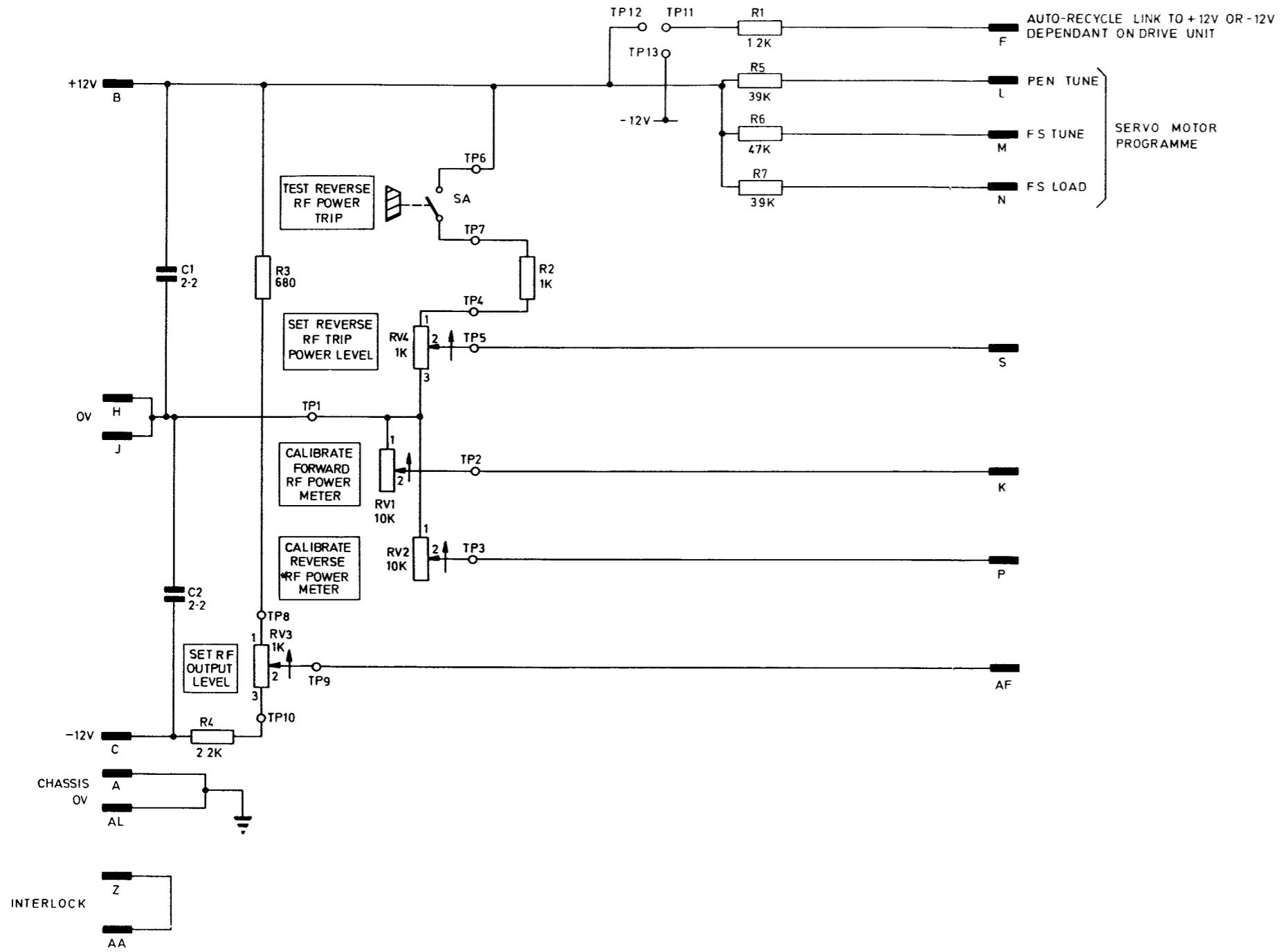


POST MOD RM077/3

BASED ON H00-1241Z SH 23
 ISSUE 1

BASED ON H-00-1241Z SH50
 ISSUE 1

Fig D1-23 : UK/FRT 651 amplifier : HT transformer taps

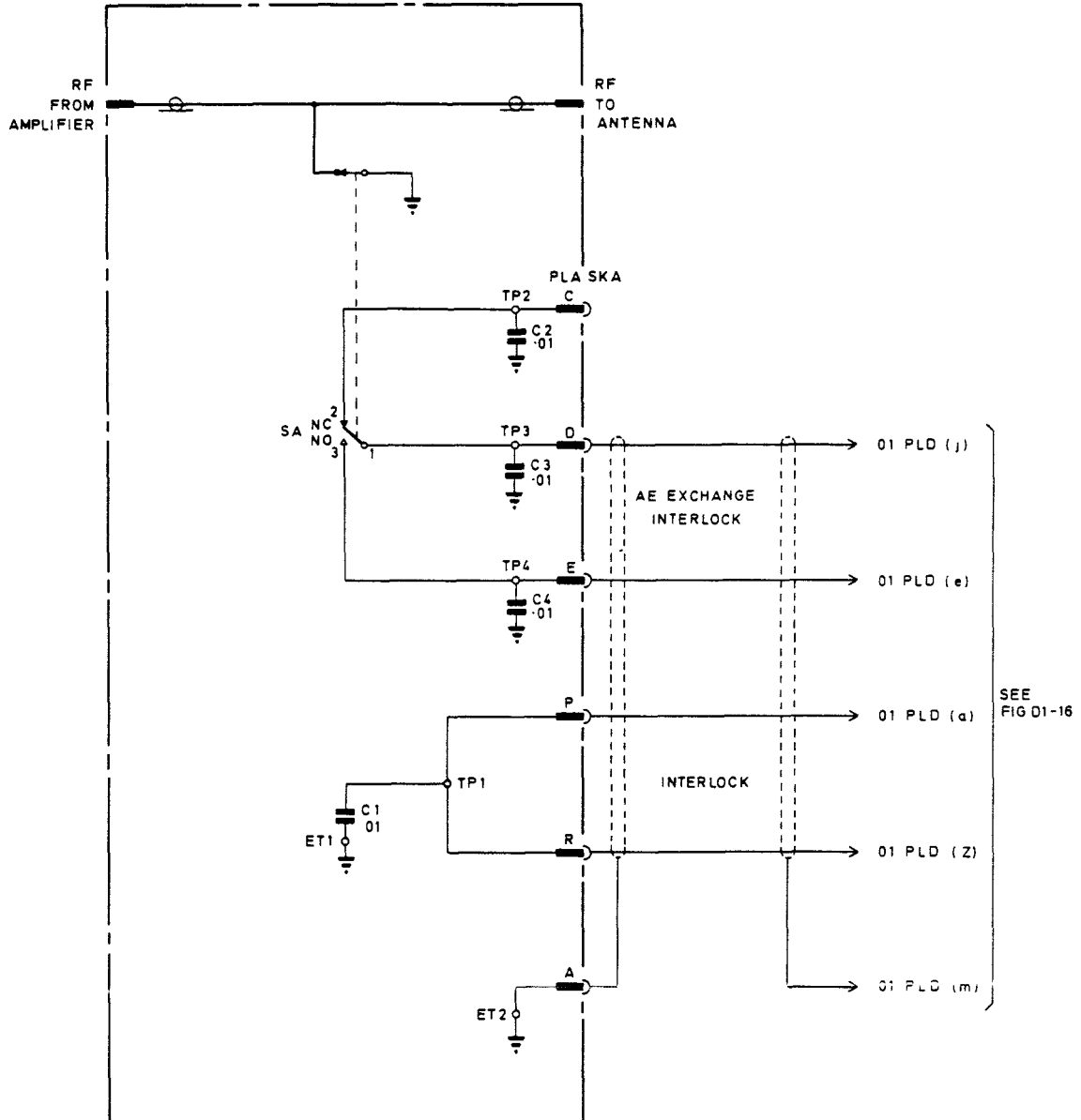


BASED ON H00-9922Z SH1 ISSUE 6
Fig D1-24

Module, calibration 5820-99-760-2982: circuit diagram

Jan 88

Fig D1-24
Sub-sect D1
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BASED ON H37-5800 Z SH 1 ISSUE 1

FigD1-25 Feeder Earth Switch : Circuit diagram

Sub-section D2MODULE EXTENDED CONTROL (ML04)5820-99-760-2961

CONTENTS

Para

- 1 Introduction
- 2 Circuit Description
- 4 Interlocks
- 5 Revertive checks

Fig

Page

- | | | |
|------|---|---|
| D2-1 | Module extended control 5820-99-760-2961: circuit diagram | 3 |
|------|---|---|

INTRODUCTION

1 The module provides an interface between the solid-state logic control circuitry of the amplifier and an external extended control system by means of printed board mounted relays.

CIRCUIT DESCRIPTION

2 When EXTENDED is selected at the amplifier sequencing switch, RLH in the module is energized enabling commands from an extended control system to control the amplifier.

3 The following extended control commands are made available to the amplifier via the module (associated relays are in brackets):

- 3.1 AUX ON (RLA)
- 3.2 HT ON (RLB)
- 3.3 PUSH-TO-TALK (RLC)
- 3.4 LOCKOUT RESET (RLD)

Interlocks

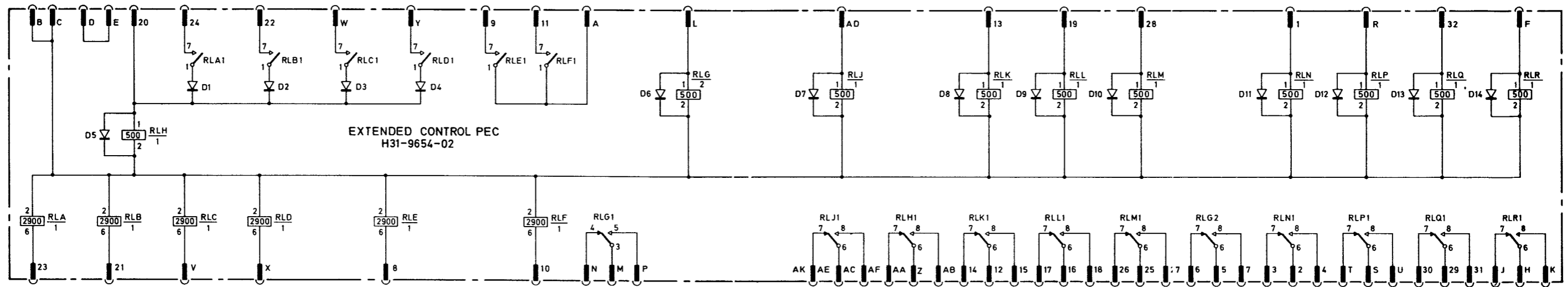
4 The following external interlock signals are made available to the amplifier via the module in either local or extended control conditions (associated relays are in brackets):

- 4.1 AERIAL INTERLOCK (RLE)
- 4.2 'SLOW' DRIVE INTERLOCK (RLF)

Revertive checks

5 The following revertive checks from the amplifier are made available to the extended control system via the module (associated relays are in brackets):

- 5.1 TUNE COMPLETE (RLG)
RLG1 gives a DRIVE TO GO TO TUNE command to the associated drive unit. RLG2 gives TUNE COMPLETE revertive check.
- 5.2 EXTENDED CONTROL SELECTED (RLH)
Refer to para 2
- 5.3 AMPLIFIER AVAILABLE (RLJ)
- 5.4 AUX START (RLK)
- 5.5 AUX COMPLETE (RLL)
- 5.6 HT ON (RLM)
- 5.7 NORMAL/STANDBY (RLN)
- 5.8 TRIP (RLP)
- 5.9 LOCKOUT (RLQ)
- 5.10 AUTO-TUNE FAIL (RLR)



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Fig D2-1

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Module, extended control, 5820-99-760-2961 : circuit diagram

Fig D2-1

Sub-sect D2

Sub-section D3MODULE EXTENDED CONTROL (SERIAL) (ML05)5820-99-795-9173

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INTRODUCTION

1 The extended control, serial module, 751-9173, provides an interface between the solid state logic control circuitry of the amplifier and an external control system by means of a serial data channel, controlled by a microprocessor system. The module provides two such data channels each providing full duplex working at CCITT V28 line data levels. The module consists of two printed circuit boards of which the top board (H37-3016-01) is the MFT2 common area. The layout of this board is repeated in the printed circuit board designs of all equipments in the MFT2 range. The bottom board (H37-3015-01) contains circuits specific to the amplifier application.

2 The function of recognising and translating both forward and revertive data along the serial channel is performed by a microprocessor system. This consists of a central processing unit (CPU) working under the control of a fixed program. This program is stored in Programmable Read Only Memory (PROM) during manufacture of the module.

3 The CPU operates from a clock of 2.5 MHz, some functions however require separate timing facilities which are derived from the clock generator by the counter timer circuit (CTC).

4 A Random Access Memory (RAM) provides the facility for the CPU to temporarily store information within the system.

5 Interface devices in the form of a variety of parallel input and output ports allow the microprocessor to communicate with the transmitter control logic. A serial input/output device (SIO) provides communication with the remote system.

6 Communication within the extended control, serial, module is achieved using the control, address and data buses. The address bus is a 16 line bus which selects a particular memory location (RAM or PROM) or an input/output (IO) device. The eight line data bus is bidirectional and allows the transfer of data from PROM memory locations and both to and from RAM memory locations and IO devices.

FUNCTIONAL DESCRIPTION

General

7 A block diagram of the extended control, serial module, is shown on Fig D3-2

8 The extended control, serial module, consists of the following discrete functional areas:

- 8.1 Central processing unit (CPU)
- 8.2 Watchdog timer (WDT)
- 8.3 Clock circuit
- 8.4 Memory selector (memory address decoder)
- 8.5 Reset circuit
- 8.6 Wait state circuit
- 8.7 1 kbyte RAM
- 8.8 12 kbyte PROM
- 8.9 Counter timer circuit (CTC)
- 8.10 Serial input/output (SIO)
- 8.11 Port selector (input/output address decoder)
- 8.12 Input/output ports
- 8.13 Test selection switch
- 8.14 Program function selection switches

Central processing unit (CPU)

9 The microprocessor used in the serial module is the Z80 CPU, which is an eight-bit, parallel, n-channel MOS, single chip device mounted in a 40 pin dual-in-line (dil) package.

10 Functionally under the control of the system program which is stored in PROM, the CPU can perform the following operations:

- 10.1 Read data from memory (RAM or PROM)
- 10.2 Write data into memory (RAM only)
- 10.3 Accept data from input ports
- 10.4 Send data to output ports

11 All data entering and leaving the CPU does so on an eight-bit bidirectional data bus (D_0 to D_7). The device associated with the data on the data bus is identified by a combination of the 16-bit address bus (A_0 to A_{15}) and a memory request (\overline{MREQ}) or an input/output request (\overline{IORQ}) signal generated by the CPU. When a memory or IO device is addressed, a signal is generated indicating whether the CPU wishes to read or write (\overline{RD} or \overline{WR}) data from or to that location.

Note...

The bar above the signal type indicates that the signal is active low, e.g. when the CPU requests memory, \overline{MREQ} goes to logic 0. This convention is used for all CPU signals.

12 It is necessary at times to interrupt the normal program flow of the CPU to give priority to specific functions. This facility is available on two devices on the serial module, the SIO and CTC. When a specific function is required the device concerned will generate an interrupt signal (\overline{INT}). This is recognised by the CPU, which will temporarily cease its normal operation, attend to the specific requirement and then return to its normal operation.

13 Since access to the memories is slower than the normal memory access cycle of the CPU it is necessary to extend the cycle for one clock period when reading or writing data from the memory. This is achieved by applying a signal to the WAIT input of the CPU.

14 A RESET facility exists on the CPU which removes all signal levels from the data and address buses and sets the CPU to the beginning of the program. This reset state is generated during initialization or by manual operation of the reset button.

15 Of the remaining CPU facilities, two are used for test purposes (\overline{BUSAK} and \overline{BUSRQ}) and one is pulled up to +5V via a resistor (\overline{NMI}). None of these facilities is relevant to the operation of the serial interface module and are not described further.

Watchdog timer (WDT)

16 The primary function of the watchdog timer is to monitor the correct running of the application program. If the program is not running correctly due to a device or circuit malfunction, the WDT causes a reset signal to be generated and applied to the CPU. Under normal operating conditions the port selector output pulses at IC11(2), are applied to the first (IC19(5)) of two retriggerable monostables which form the WDT (IC19). The chip select pulse, normally occurs every 25 ms, but, if for any reason it does not occur, the first monostable period matures and its \overline{Q} output (IC19(7)) goes high, which causes the led on the bottom board to light. At the same time the Q output (IC19(6)) goes low, causing the second monostable to trigger its Q output high and IC22(10) to give a logic 0 on the \overline{RESET} output of the CPU.

Note...

During signature analysis test modes it is necessary to prevent the WDT from resetting the CPU in the absence of port select pulses, this is achieved by placing link LK1 in position A.

Clock circuit

17 The clock rate for the CPU is 2.5 MHz, which is provided by the clock circuit. A high stability crystal oscillator provides a 10 MHz signal which two D-type flip-flops divide by four to produce the required system clock, which is fed to the CPU, SIO and CTC.

Reset circuit

18 The reset circuit comprises a comparator (IC28) and associated components which provide a reset pulse to the CPU, CTC and SIO as part of the power switch on sequence or if the reset switch (SA) on the control board, is operated. The circuit will also maintain the reset condition (logic 0) if a power failure is detected in the -12V or +5V supplies. When power is first applied to the board C32 is discharged and the comparator output is at logic 0 as is the reset signal at IC22(10) thus holding the CPU, CTC and SIO in the reset condition.

19 As the voltage rises C32 is charged via R12. When it is sufficiently charged the comparator (IC28) output switches to logic 1, setting the reset signal to logic 1 and allowing the CPU to operate. TR13 discharges C32 when the WDT operates to provide a full-length reset pulse.

Wait state circuit

20 Due to the nature of the memories and address decoding circuit used on the serial board, the operation of the CPU during a memory read or write operation must be delayed for one clock period. This is performed by the wait circuit.

21 At various times during a memory input/output cycle the CPU samples the $\overline{\text{WAIT}}$ input. If logic 1 is sampled the cycle is not extended and if logic 0 is sampled the cycle is extended by one system clock period. The wait state circuit (IC21 and IC9) gates together the $\overline{\text{MREQ}}$ and the system clock to produce a logic 0 on the $\overline{\text{WAIT}}$ input the first time it is sampled during a memory cycle and logic 1 on the next sample. This produces a memory cycle that is extended by one clock period.

Memory selector

22 Three lines of the address bus (A12, A13 and A14) are not used directly to address the memory; but, are decoded by a 3 to 8 line decoder which forms the memory selector. The selector is enabled during the memory request ($\overline{\text{MREQ}}$) period and the address on the appropriate three lines of the address bus, at that time, result in the enabling of the appropriate memory device. Other address lines are connected directly to the memory and select the location within that memory.

23 The outputs from the memory selector (PROM 0 to 2 and RAM) are connected to the chip enable (CE) pin of each memory device. The CE pins of the RAM devices are connected together and hence both RAMs are enabled together.

1k byte RAM

24 Two random access memory (RAM) devices each with a capacity of 1024 4-bit words, provide the CPU with the facility to temporarily store information. The RAMs are enabled by the memory selector and the individual locations are addressed by lines A0 to A9 of the address bus. The \overline{WR} input is used by the CPU to cause a data read or write operation, as required at that location. The RAMs used in the serial module are static in operation and so do not need refreshing by the CPU. As they are volatile devices, however, they require a constant power supply, failure of which results in all stored information within the RAMs being lost.

12k byte PROM

25 Programmable read only memory (PROM) capability on the module is provided by three 4k byte PROM devices which collectively contain the system program and test routine. Each PROM is programmed during manufacture.

26 Timing functions which are required to be carried out independently of the program instructions sequence are performed by the CTC. This is a four-channel device, each channel of which can provide either counter or timing functions. Only two channels are used in this application.

26.1 Channel 0 provides the 'real time' clock. The CTC interrupts the CPU every 2.5 ms and all the system timing is based on this period.

26.2 Channel 1 provides the X16 baud rate clock for the SIO. This clock appears at pin 8 of the CTC (IC8) as a series of 400 ns positive pulses.

Counter timer circuits (CTC)

27 The CTC is programmed by the CPU to provide the desired mode of operation and is also controlled by the CPU. Address lines A6 and A7 are gated to provide the chip enable (\overline{CE}) signal whilst address lines A0 and A1 are used to determine which channel is being accessed. The CPU control signals \overline{IORQ} , \overline{RD} and \overline{MI} are used to control the timing of data transfer between the CPU and CTC on the data bus. The CTC uses the same reset signal as the CPU and after being initiated by the CPU it will automatically interrupt the CPU every 2.5 ms using the \overline{INT} line.

Serial input/output (SIO)

28 The serial input and output of control and revertive information for the serial module is achieved using a single serial input/output device (SIO) IC17. The SIO is a dual channel device which can transmit data either synchronously or asynchronously. In the application for the amplifier only the asynchronous mode is used. Although two serial communication channels (CC1, CC2) are provided only one (CC2) is usually used as a pairing link to the drive through which commands and revertives are sent.

29 The SIO is programmed for the desired mode of operation and is controlled by the CPU. Address lines A6 and A7 are gated to provide the chip enable (CE) signal. Address line A0 is used to determine which of the two channels is being accessed, and address line A1 determines whether the control or data registers are being accessed. The CPU control signals \overline{IORQ} , \overline{RD} and \overline{MI} are used to control the timing of data transfer between the CPU and SIO on the data bus. The SIO uses the same reset signal as the CPU and CTC.

30 The baud rate clock generated by the CTC is applied to the transmit and receive clock input of the SIO. This clock runs at 16 times the required baud rate. Four baud rates are available, as determined by the setting of the Program Function Selection Switches (Para 159). When serial data is transmitted or received the SIO interrupts the normal program flow of the CPU by setting an interrupt signal on the $\overline{\text{INT}}$ line. This enables special transmit and receive data interrupt routines to be accessed.

Port selector

31 A 4 to 16 line decoder provides the enabling signals for seven parallel input/output ports. Four lines of the address bus (A2 to A5) are fed to the decoder together with the control signals $\overline{\text{TORQ}}$ and $\overline{\text{MI}}$ which ensure that a port select signal is only produced during an input/output cycle. An eighth output from the decoder is fed to the WDT to maintain its output and prevent it from producing a reset pulse (Para 27). The remaining eight outputs of the decoder are not used.

Input/output ports

32 The input/output (IO) ports, one of which is an output port, provide the parallel communication capability between the serial interface module and the remainder of the transmitter logic control system.

33 Data is fed between the CPU and the IO ports via the data bus and each port is enabled by a combination of the port selector output and the read (RD) pulse (for input ports) or the write (WR) pulse (for the output port). Port 6 is an analogue to digital (A/D) converter which is a four channel device that requires a clock at $\frac{1}{4}$ of the system clock speed. A divide by four circuit is therefore included to provide this clock rate.

Test selection switch

34 The test selection switch (SPB) is a 6-section dil switch mounted on the top board, H37-3016. It is used to select either the application (normal operational) program or one of the signature analysis or self-test programs. To run the application program all six switches of SPB are set to the closed position. For details of the switch settings for signature analysis and self-test routines refer to Para 37.

Program function selection switches

35 The program function selection switches No 1 and 2 (SPB and SPA) are 8-section dil switches mounted on the bottom board. They are accessed via the data lines and the appropriate signal from its port selector.

36 The options available for selection by SPA are:

- 36.1 The selection of four baud rates
- 36.2 Whether the press-to-talk (PTT) command comes via the serial remote control channel or as a hard-wired connection at the amplifier PTT input.
- 36.3 Whether or not there is a special block check formed on serial data. Refer to Table 6 for option switch settings.

SELF TEST AND SIGNATURE ANALYSIS

37 This equipment contains bus-structured printed boards using LSI devices. Two methods of transferring data to and from the CPU are used, unidirectional and bidirectional, by way of these buses.

38 By controlling the communication and algorithmic interaction between the bus devices, much of the dedicated hardware logic previously associated with performing complex signal and data processing tasks can be replaced by software data.

39 Within a microprocessor system, however, logic signals are replaced by data bit streams. This often means that the operating characteristics of a board are not directly associated with specific hardware components. Also certain functional characteristics are much more difficult to characterize and define because of the long complex data streams necessary. Both these aspects are further complicated by the fact that devices attached to the bidirectional bus can input or output data on the same bus pin connection.

40 When fault analysis, using conventional fault diagnostic techniques, is attempted on micro-processor systems several major requirements have to be met. Among these are:

- 40.1 Extensive circuit isolation techniques are required which increase complexity and size of printed boards.
- 40.2 Extensive and detailed documentation including many pages of logic waveforms and tables of logic levels.
- 40.3 Multichannel, storage and programmable logic analysers and other specialized service and design test equipment.
- 40.4 The servicing personnel need not only a knowledge and understanding of the logic circuits but also of the internal architecture and operation of the LSI devices and of the software used to control the system.

41 Even with the above requirements fully satisfied fault analysis and rectification can be a complex process and consume a considerable amount of time. To simplify fault analysis and reduce the down-time of the equipment, provision has been made in the design for built-in test routines and Signature Analysis.

42 Built-in test routines provide facilities for the equipment to self-test various functions and operational areas using specifically-designed software contained in the PROM. Each function or operational area can be separately selected by means of a test switch on the control board. Indicators on the test extension unit are used to show a pass or fail condition for each test. A specific LSI device may be shown as faulty, or an area will be indicated which can then be subjected to further investigation.

43 Signature Analysis (SA) provides the means by which detailed checking of a circuit may be carried out. Used in conjunction with algorithmic flow charts, SA is intended to provide assistance to servicing personnel by indicating in a logical sequence the state of dependencies associated with a particular function or operational area.

The concept of signature analysis

44 The two basic principles of Signature Analysis are 'data compression' and 'circuit generated stimulus'.

45 Data compression within a Signature Analyser reduces any long, complex data bit stream pattern on a logic node to a four-digit display on hexadecimal indicators. The four-digit display is the 'Signature' of the logic node. Data compression is achieved by probing the logic test node from which data is input for each and every circuit clock cycle that occurs within a specified circuit controlled measurement time interval (window).

46 Within the Signature Analyser is a 16-bit feedback shift register into which the data at the logic node is entered in either its true or complement logic state, according to previous data dependent register feedback conditions. There are 2^{16} states to which the shift register can be set during a measurement window. These states are then encoded to four hexadecimal states and displayed as the 'signature'. Thus this signature is a characteristic number representing the time dependent logic activity at the logic node during the measurement window. Any change in the logic activity at the node (e.g. a transition that is shifted one clock cycle or skewed with respect to the clock) will produce a different signature, indicating a probable circuit malfunction.

47 By probing various nodes and comparing the signatures obtained to known correct signatures a comparison can be made with the circuit running at full operating speed, to determine good or bad circuit operation.

48 The measurement window is determined by initiate and terminate signals from the circuit applied to the analyser 'Start' and 'Stop' connections. A 'clock' input synchronizes and controls the data sample rate of the probe input so that the data is input to the analyser and processed every clock cycle within a Start/Stop interval. The Start and Stop inputs to the analyser are individually selectable for logic '1' or '0' levels, the Clock input is edge-triggered and can be selected for rising or falling edges. Alternatively the probe can be connected to a permanent logic 1 (e.g. +5V supply) and the clock connection to a node which will change state in a specified manner during the window. The probe can also be used to detect the presence of logic 0, logic 1 or pulses, for these states the probe gate led will cease to glow, will glow more brightly than normal or flash at the pulse rate.

49 The signal that causes the node to produce a signature is the 'stimulus' and in SA is supplied by the circuit itself. By doing this, a controlled environment can be created in which selected portions of the circuit can be independently tested. The stimulus is a series of programs held in PROM which can be used to exercise selected areas of the circuit systems as required.

50 For further information relating to Signature Analysis and Analysers refer to Hewlett Packard publication:-

AN 222, A Designers Guide to Signature Analysis

BUILT-IN TEST SOFTWARE

INTRODUCTION

51 The Built-in Test Software (BITS) includes tests which will check the microprocessor control selection. The tests cover most components on the Common Area Board (H37-3016) and the Extended Control Serial Board (H37-3015).

52 The BITS facilities in this equipment consist of self-test routines and Signature Analysis tests.

Self-test

53 These tests are controlled by programs which check circuit areas and report certain types of fault condition, or give a pass indication. In some tests there is no user intervention required except to set up and start the test. Other tests require the user to perform simple operations and observe the response of the equipment.

54 For the self-test routines the module is fitted onto the extension unit (ECS), 5820-99-795-9175. This unit extends the $\pm 12V$ supplies and the amplifier start interlock from the control frame assembly, and provides the required interface conditions for the parallel input and output ports of the module. Refer to Para 166 onwards and Fig D3-7.

55 The user selects the required test on the dual-in-line Test Selection switch and may be required to make various links on the board or its connectors. The Reset switch is then pressed and the test runs. If the test is of the type which requires no further user intervention it will give an indication on the extension unit when complete. The test number is displayed as shown in the overall fault-finding flow-chart. Should the test require user intervention the display will light in the manner described in the individual test descriptions, which also lists the operations required to complete the test.

56 On reset all self-test programs perform a lamp test before the actual test begins. During the lamp test the test extension led(s) are illuminated for 2s, then extinguished for 2s. If the display is not obtained the display is faulty or the processor is not able to run the program. In this situation the user should perform the NO-OP test (Refer to Para 98), and then the PROM. Signature Analysis test (Refer to Para 105).

57 A self-test program which displays a test and fault indication runs once after reset and is not repeated unless the reset switch is pressed again. These tests end on the first detected fault, or when all items tested have been passed. It should be noted that the test terminates early if a fault is found and items which would normally be tested subsequently are not checked. The indicated fault should be cleared first and the test re-run to determine other faults if any.

58 Self-tests that require user intervention run continuously once entered and provide a display which responds to operations performed by the user.

Signature analysis tests

59 These tests are of two types. The first is similar to a self-test program, in that it checks a specific circuit area and is able to determine whether or not it is functioning correctly. In this case the gating and clock signals generated produce signatures for the Signature Analysis which are equivalent to the fault number displays given by the self-tests.

60 The second type of SA test provides a stimulus for a circuit area and the user is required to probe the circuit with the signature analyser and check the set of signatures obtained.

61 All SA tests run continuously until stopped by selecting a different test and pressing the Reset switch. The SA tests do not perform a lamp test and do not display a test or fault indication on the extension unit on the equipment being tested.

BITS Test description

62 The Built-in test Software in this equipment contains self-test and signature analysis programs for the following circuit areas:

- 62.1 PROM
- 62.2 RAM
- 62.3 CTC Timer operation with interrupts
- 62.4 SIO Asynchronous operation with interrupts
- 62.5 Dual-in-line switches
- 62.6 Output ports
- 62.7 Input ports
- 62.8 A/D converter

63 Some tests have both self-test and S.A. versions, whilst other tests exist only in one form. A brief description of each test is given below, including a description of the Basic Functions Test and the NO-OP test which check more than one specific area.

NO-OP Test

64 This is the lowest level of test used in the BITS fault-finding package and is used when the Basic Functions Test cannot successfully be run.

65 Being the lowest level of test certain checks should be made before the NO-OP test is run. These include checks of the power supplies, reset circuit, clock signals, the position of links and for correctly inserted components.

66 During this test all the CPU data lines are disconnected from the CPU by the removal of a link pack. A dual-in-line resistor module is then used to pull all the CPU data lines to 0V, which is interpreted as a NO-OP instruction by the CPU which will increment throughout the whole address range, from 0000 to FFFF (Hexadecimal). The cycle will repeat until the data bus lines are reconnected by the link pack.

67 The NO-OP test enables several CPU functions to be tested even if a test program cannot be run.

Basic functions test

68 This test is the starting point for fault finding using Signature Analysis and the self-test package. The Basic Functions Test combines the PROM, RAM and CTC Tests with no reconfiguration of the equipment required, i.e. no special linking is necessary. The PROM, RAM and CTC Tests are performed in sequence and the first detected failure is reported.

69 If the basic functions test is satisfactory, the four left-hand yellow led's (DLP3 to DLP7) will indicate the basic functions test number (1) in binary, and the four right-hand led's will indicate a pass, (binary 0).

PROM Test

70 Each PROM is checked as a separate unit. All bytes in the PROM under test are added together to form a three byte checksum. This value is then compared with a checksum stored in the BITS PROM and if the calculated checksum is correct the next PROM is checked. Should there be a disparity between the stored and the calculated values this fault is indicated by the led on the extension unit display as a binary fault number (for the self-test) or as an incorrect signature on the Signature Analyser (for the SA test).

71 The BITS PROM ICI is also checked but does not include the three bytes containing its own checksum when adding up the bytes.

RAM Test

72 The RAMs are tested as a complete memory area. The test involves writing in a block of ten bytes. The contents of the RAM are then read back and compared with the data previously written in. If all comparisons are correct the sequence of bytes is written again but with the block advanced within the RAM by one byte. If, on readout, the values differ, the test ends and a fault indication is given.

73 The comparison is then repeated. The write-read and compare operations are repeated until each sequence element has occupied every RAM location, or until a fault is found. A no-fault indication is given on completion of an error-free run of the test.

74 An error-free test takes about 2s to run.

CTC Test

75 The CTC is tested, channel by channel, in the timer mode with interrupts enabled. A check is made that each channel counts, interrupts and reloads the time constant correctly. This function is checked by comparing the timer delay for three count-down periods against a program loop counter. The correct operation of the vectored interrupt system is also checked, with any detected malfunction giving a fault indication.

76 The fault indication shows which channel causes a wrong interrupt or does not produce the correct timer period.

SIO Test

77 The SIO is tested by connecting the transmit and receive data of each channel together, and then sending a string of characters through both channels under interrupt control. This is accomplished by using the transmit buffer empty interrupt and the character received interrupt. The following fault conditions can be detected:

- 77.1 An interrupt fault is indicated if an expected interrupt does not occur, or if the wrong interrupt routine is accessed.
- 77.2 A character corrupted fault is indicated if an incorrect character is received.

Output port test

78 A sequence of eight bytes is used to stimulate all the lines of every output port. The first byte of the sequence is fed to all the ports and subsequent bytes of the sequence are then fed to all the ports with a clock pulse after the ports have received each sequential byte. Thus a set of eight different signatures is produced, each signature corresponding to a particular line of the output ports but with the same set of signatures applying to each port. The operator can then check any suspect lines using the signature analyser.

79 The test sequence is repeated until the Reset switch is operated. There is no extension unit indication for this test.

Input port test

80 The two input ports are tested by the operator manually setting up logic states at the port inputs and observing the read-in state of the port on the test display.

Analogue-to-digital converter test

81 The A/D converter test checks the operation of the four operational channels of the converter. The test extension unit has been designed to provide different preset voltages for the four A/D converter channels.

82 When the A/D converter test is running, the test selection switch is used to determine which of the four A/D channel readings is displayed on the test extension unit leds.

Dual-in-line switch tests

83 A different test is run for each of the dual-in-line switches but with each test operating in a similar manner as shown below.

84 The test reads in the state of the dual-in-line switch and displays the read-in value on the extension unit. The setting of the switch can then be changed and the new reading will then be displayed. The test will continue to operate until the Reset switch is pressed.

85 Signals are produced during this test which enable the Signature Analyser to produce a signature which indicates the most significant switch that is closed, or that all switches are open.

86 The test selection switch test is entered if the value of the read-in test selection switch setting is invalid, that is the setting does not correspond to one of the self-test, SA, or application settings. The test-switch test is also entered if it is correctly selected by the test switch.

BITS OPERATIONGeneral

87 To ensure that tests are performed in the correct sequence the BITS overall fault-finding flowchart (See Fig D3-8) should be followed.

88 The fault finding procedure often requires replacing a suspect IC. It should be noted that an IC should normally only be replaced once. In order to prevent flow charts from becoming too complicated a group of IC's may sometimes be indicated as being the possible cause of the fault. In this case the IC's should be replaced one at a time to isolate the faulty components.

89 The Watchdog Timer should be disabled by placing link LK1 in the B position before running any tests. This is done to prevent the Watchdog Timer from resetting the CPU. Any equipment which is normally connected to the equipment under test should be disconnected before any tests are run. Links and test connections made during the signature analysis and self-test routines should be replaced before normal operation is resumed.

90 If an inconsistent display is produced when a test is run this may be a result of a fault in the test selection switch or associated components, such that the test which runs is not the intended test. For test switch settings, as read by the CPU, which do not correspond to a valid test the test-selection-switch test is entered. It should be possible therefore, to run the test-switch test to check its operation even if there is a fault which causes the normal settings not to select this test.

91 All SA tests generate Start and Stop gating signals for the Signature Analyser. As these signals are fundamental to the correct operation of the test and fault-finding procedure, a check should be made when doing an SA test that the Gate led on the Signature Analyser flashes, indicating the presence of the gating signals and either a pass or one of the listed fail signatures is produced. Should an unlisted or unstable signature be produced then the test is not running correctly and an unstable signature will cause the 'Unstable Signature' led to flash.

92 See Table 4 for a complete list of self-test and Signature Analysis tests with the corresponding test selection switch settings.

Signature analysis gating failure

93 If no gating is produced, or the signatures obtained are unstable, the SA test should be abandoned, except in the case of the NO-OP and PROM SA Test. The appropriate check list below should be carried out.

CPU \overline{RD}

94 If there is no activity on the CPU \overline{RD} test point, TP13, the NO-OP test should be performed. See Para 98.

Test switch chip select

95 If there is no activity on the test switch chip select, IC9 pin 3, or an unstable signature is obtained, the NO-OP test (Para 98) and then the PROM SA test (Para 105) should be run.

SIO \overline{DTRA}

96 If there is no activity on the SIO \overline{DTRA} pin (IC17 pin 16) or an incorrect or unstable signature is obtained, then IC17 (SIO) or IC9 should be replaced. If the fault persists the NO-OP test (Para 98) should be performed, probing for signatures or activity on the SIO pins where applicable, e.g. address lines, data bus lines etc.

97 To return to the normal, operational program, the test selection switch (SPB on common area board) should be set as follows and the reset switch pressed.

1	2	3	4	5	6
ON	ON	ON	ON	ON	ON

NO-OP Test

- 98 The following preliminary checks should be made before this test is run.
- 98.1 Power supplies.
Check that the following voltage readings are obtained with respect to the common area 0V, TP24.
- | | | |
|------------------|---|---------------|
| +12V IC27 pin 14 |) | |
| -12V IC27 pin 1 |) | SIO O/P gates |
| +5V IC16 pin 11 | | CPU |
- A more extensive check of the power supplies and their connections should be made if a fault is suspected in this area.
- 98.2 System clock
Check that a 2.5 MHz clock signal appears on the following pins:
- | |
|-------------|
| IC16 pin 6 |
| IC17 pin 20 |
| IC8 pin 15 |
- 98.3 Reset circuit
Ensure that the reset circuit produces the correct power-on reset pulse, and that the correct reset pulse is produced when switch SA in the common area is pressed.
- 98.4 Link position
Ensure that all the links on the common area board are in the correct position (Refer to Table 7).
- 98.5 Component insertion
Ensure that all components are inserted correctly and are correctly orientated.

99 After performing the basic checks listed above remove LKP1 on the common area board and connect the clips of the Signature Analyser pod as follows:

Start and Stop	TP9	CPU $\overline{A15}$
Clock	TP13	CPU \overline{RD}
Ground	TP24	0V

100 Set the switches on the Signature Analyser as follows:

Start	Falling edge, switch in
Stop	Falling edge, switch in
Clock	Falling edge, switch in
Hold, self-test	Off, switches out

101 Follow the procedure detailed in the NO-OP Flowcharts see Figs D3-9 and D3-10 and when the NO-OP test has been completed any components which were removed during the test should be refitted.

PROM Self-test

102 Set the Test Selection switch (SPB on common area board) as follows:

Switch	1	2	3	4	5	6
Position	ON	OFF	ON	ON	ON	ON

103 Press the Reset switch SA on the common area board. Check that the test extender led indicators are lit for 2s and then extinguished for 2s. The led display should then indicate the PROM test number (2) in binary on the four left-hand led's and a binary fault number on the four right-hand led's.

104 Proceed as detailed in the PROM Self-Test Flowchart, see Fig D3-11.

PROM Signature analysis test

105 Set the Test Selection Switch, (SPB on common area board) as follows:

Switch	1	2	3	4	5	6
Position	ON	OFF	ON	ON	ON	OFF

106 Connect the clips of the Signature Analyser pod as follows:

Start and Stop	IC9 pin 3	Test switch port chip select TP25
Clock	TP13	(RD)
Ground	TP24	0V

107 Set the switches on the signature analyser as follows:

Start	Rising edge, switch out
Stop	Falling edge, switch in
Clock	Rising edge, switch out
Hold, Self-test	OFF, switches out.

108 Place the probe on the +5V supply at the common area board, and proceed as detailed in the PROM Signature Analysis Flowchart, see Fig D3-12.

RAM Self-test

109 Set the Test Selection Switch (SPB on the common area board) as follows:

Switch	1	2	3	4	5	6
Position	OFF	OFF	ON	ON	ON	ON

110 Press the reset switch, SA, on the common area board. Check that all the test extender led indicators are lit for 2s and then extinguished for 2s. The led display should then indicate the RAM test number (3) in binary on the four left-hand led's and a binary fault number on the four right-hand led's.

111 Proceed as detailed in the RAM test flow chart see Fig D3-13.

RAM Signature analysis test

112 Set the Test Selection Switch (SPB, on the common area board) as follows:

Switch	1	2	3	4	5	6
Position	OFF	OFF	ON	ON	ON	OFF

113 Connect the clips of the Signature Analyser pod as follows:

Start and Stop	IC9 pin 3	Test switch port chip select TP25
Clock	TP13	RD
Ground	TP24	0V

114 Set the switches on the signature analyser as follows:

Start	Rising edge, switch out
Stop	Falling edge, switch in
Clock	Rising edge, switch out
Hold,	
Self-test	OFF switches out

115 Place the probe on the +5V supply of the common area board. Press the reset switch on the probe and the reset switch on the control board.

116 Check that the Signature Analyser gate led flashes, and proceed as detailed in its RAM Test Flowchart. If the led does not flash or an unstable signature is obtained refer to the Signature Analyser Gating Failure Para 93.

CTC Self-test

117 Set the Test Selection Switch (SPB, on the common area board) as follows:

Switch	1	2	3	4	5	6
Position	ON	ON	OFF	ON	ON	ON

118 Press the Reset Switch, SA on the common area board. Check that the test extender led indicators are lit for 2s and then extinguished for 2s. The led display should then indicate the CTC test number (4) in binary on the four left-hand led's and a binary fault number on the four right-hand led's.

119 Proceed as detailed in the CTC Test Flowchart, see Fig D3-14.

CTC Signature analysis test

120 Set the Test Selection Switch (SPB on the common area board) as follows:

Switch	1	2	3	4	5	6
Position	ON	ON	OFF	ON	ON	OFF

121 Connect the clips of the Signature Analysis pod as follows:

Start and Stop	IC17 pin 16	SIO $\overline{\text{DTRA}}$ TP26
Clock	TP13	RD
Ground	TP24	0V

122 Set the switches on the Signature Analyser as follows:

Start	Falling edge, switch in
Stop	Rising edge, switch out
Clock	Rising edge, switch out
Hold, Self-test	Off, switches out

123 Place the probe on the +5V supply of the common area board. Press the reset switch on the probe and the reset switch (SA) on the board.

124 Check that the Signature Analyser gate led flashes and proceed as detailed in the CTC Test Flowchart. If the gate led does not flash or an unstable signature is obtained refer to Signature Analyser Gating Failure, see Para 93.

SIO Self-test

125 Set the Test Selection Switch (SPB, on the common area board) as follows:

Switch	1	2	3	4	5	6
Position	OFF	ON	OFF	ON	ON	ON

126 Place links 3 and 4 on the common area board in the 'A' position. Make a note of the position of link 6 and then make sure that it is in the 'B' position.

127 Disconnect any serial control connections from the equipment.

128 Press the reset switch SA on the common area board. Check that all the test extender led indicators are lit for 2s and then extinguished for 2s. The led display should then indicate the SIO test number (5) in binary on the four left-hand led's and a binary fault number on the four right-hand led's.

129 Proceed as detailed in the SIO Self-test Flowchart, see Fig D3-15, ensuring that links 3 and 4 are replaced in the 'B' position and that link 6 is restored to its original position when the test has been completed. Reconnect any serial control connections.

SIO Signature analysis test

130 Set the Test Selection Switch (SPB, on the common area board) as follows:

Switch Position	1 OFF	2 ON	3 OFF	4 ON	5 ON	6 OFF
--------------------	----------	---------	----------	---------	---------	----------

131 Connect the clips of the Signature Analyser pad as follows:

Start and Stop	IC17 pin 16	SIO <u>DTRA</u> , TP26
Clock	TP13	RD
Ground	TP24	0V

132 Set the switches on the Signature Analyser as follows:

Start	Falling edge, switch in
Stop	Rising edge, switch out
Clock	Rising edge, switch out
Hold, Self-test	Off, switches out

133 Place links 3 and 4 on the common area board in the A position. Note the position of link 6 and then ensure it is in the B position. Disconnect any serial control connections from the equipment.

134 Place the Signature Analyser probe on the +5V supply. Press the reset switch on the probe and the reset switch (SA) on the Common Area Board. Check that the Signature Analyser gate led flashes and proceed as detailed in the SIO Signature Analysis Flowchart, see Fig D3-16 and D3-17.

135 If the gate led does not flash or an unstable signature is obtained refer to Signature Analyser Gating Failure Para 93.

136 On completion of the test replace links 3 and 4 to the B position and replace link 6 to its original position. Reconnect any serial control connections.

Output port test

137 Set the Test Selection Switch (SPB on common area board) as follows:

Switch Position	1 ON	2 OFF	3 OFF	4 ON	5 ON	6 OFF
--------------------	---------	----------	----------	---------	---------	----------

138 Connect the clips of the Signature Analyser pod as follows:

Start and Stop	IC17 pin 16	SIO $\overline{\text{DTRA}}$ TP26
Clock	IC9 pin 3	Test Selection Switch port chip select (TP25)
Ground	TP24	(0V)

139 Set the switches on the Signature Analyser pod as follows:

Start	Falling edge, switch in
Stop	Rising edge, switch out
Clock	Rising edge, switch out
Hold, Self-test	Off, switches out

140 Place the Signature Analyser probe on the +5V supply of the common area board. Press the reset switch on the probe and the reset switch (SA) on the common area board.

141 Check that the Signature Analyser gate led is flashing and a signature of Ooup is displayed. This is an indication that the test program is running correctly, but gives no information about the functioning of the output ports.

142 If the gate led does flash and the correct signature is obtained, proceed as detailed in the Output Port Test Flowchart see Fig D3-18.

143. Should an incorrect signature be produced or the gate led does not flash refer to Signature Analyser Gating Failure, Para 93.

Input port tests No.2 and 3

144 Input port test No 2 tests input port IN0 (address decode 9) which consists of IC6 and part of IC9. Input port test No 3 tests input port IN1 (address decode A), which consists of part of IC9 and IC13. Both ports are on the extended control, serial, board H37-3015.

145. Set the Test Selector Switch (SPB on the common area board), as follows:

Switch	1	2	3	4	5	6
Test 2 (IN0)	ON	ON	ON	OFF	ON	OFF
Test 3 (IN1)	OFF	ON	ON	OFF	ON	OFF

146 Press the reset switch, SA on the common area board. Check that the led's on the extension unit are illuminated for 2s and then extinguished for 2s. The eight led's (DLP3-DLP12) should then indicate the state of the input lines of the port under test. Switch packs SPA and SPB on the test extender can be used to put a logic 0 or 1 on the inputs of the port under test. If a logic 0 is read into the input port under test the corresponding led will be off, if a logic 1 is read in the corresponding led will be on.

147 For input port test No 2 a logic 0 is applied to the inputs of port IN0 when the upper end of the appropriate switch toggles of SPA and SPB on the test extension unit are pressed in. When the lower end is pressed in a logic 1 is enabled at the corresponding input. The latter condition is shown in Fig D3-7.

148 For input port test No 3 the opposite condition applies, pressing in the upper end of the switch toggles applies a logic 1 to the corresponding inputs of port IN1.

149 If a fault is suspected during the test the Signature Analyser probe should be used to check that the correct stimulus is being applied to the input of the input port under test. Tables 3 and 4 show the test extender switches and indicators corresponding to each input of a port and also the components connected to that input. These tables should be used as an aid to fault finding.

150 If SPA or SPB (on the test extender) is set so that the input port should read a value of 0 on a specific line that input should be pulsing. If the switches are set so that the input port should read a value of 1 on a specific line that input should be a permanent logic 1.

151 If the correct signals are being applied to the inputs, and the wrong indication is obtained, the input port IC (either IC6, IC9 or IC13) should be replaced and if the fault persists IC8 should be replaced. If the correct signals are not being applied the output port test should be performed see Para 137.

Analogue-to-digital converter test

152 Set the Test Selection Switch, SPB on the common area board, as follows:

Switch	1	2	3	4	5	6
Position	ON	ON	OFF	OFF	ON	ON

153 Press the reset switch SA on the common area board. Check that the indicators on the test extender are illuminated for 2s and are then extinguished for 2s.

154 Once the test has been entered the Test Selection switch should be set to display the value of each of the A/D channels as shown below.

Channel to be displayed	Switch Settings					
	1	2	3	4	5	6
0	ON	ON	ON	ON	ON	ON
1	OFF	ON	ON	ON	ON	ON
2	ON	OFF	ON	ON	ON	ON
3	OFF	OFF	ON	ON	ON	ON

155 The value read in by the A/D converter is displayed on the test extender led's DLP3-DLP12 in binary which can be interpreted as two hexadecimal digits. The four left-hand led's represent the most significant hexadecimal digit, and the four right-hand led display the least significant digit. Each hexadecimal digit can have one of 16 values which is equivalent to the binary state of the led's. The state of the led's and the hexadecimal value they represent are shown below.

LED (Binary representation)	Hexadecimal value
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	A
1 0 1 1	B
1 1 0 0	C
1 1 0 1	D
1 1 1 0	E
1 1 1 1	F

Note...

A led is lit to indicate a logic 1.

156 The values displayed for each channel should be in the hexadecimal range shown below:

Channel No. displayed	Hexadecimal range (Hex.)	Voltage range at input of A/D (Volts)	A/D input
0	35 to 44	1.13 to 1.27	IC2 pin 38
1	6B to 84	2.22 to 2.47	IC2 pin 39
2	AE to D9	3.58 to 4.07	IC2 pin 40
3	C6 to FF	4.07 to 4.90	IC2 pin 1

157 If a hexadecimal value outside the range shown is obtained ensure that the correct voltage is being applied to the A/D converter inputs. If an incorrect voltage is being applied use conventional fault-finding techniques to cure the fault, or replace the A/D converter (IC2 on the extended control serial board).

158 If only one channel is faulty, with the correct voltage being applied, replace IC2, IC4 (on extended control serial board) or IC11 (on common area board), or check for a faulty ribbon cable connecting the two boards.

Dual-in-line switch tests

159 Set the Test Selection Switch (SPB on common area board) for the required test as shown below:

Test	1	2	3	4	5	6
Test Switch Test (SPB on H37-3016)	OFF	OFF	OFF	ON	ON	ON
Program Function Selection Switch 2 (SPA on H37-3015)	ON	ON	ON	OFF	ON	ON
Program Function Selection Switch 1 (SPB on H37-3015)	OFF	ON	ON	OFF	ON	ON

160 Press the reset switch SA on common area board. Check that the led indicators on the test extender are illuminated for 2s and then extinguished for 2s. The eight led's should then indicate the state of the switch under test as shown below. A switch contact that is open causes the corresponding led to be lit.

LED Indicator	DLP3	DLP4	DLP6	DLP7	DLP8	DLP9	DLP11	DLP12
Test Selection Switch SPB (on H37-3016)	6	5	4	3	2	1	x	x
Program Function Selection Switch 2 SPA (on H37-3015)	1	2	3	4	5	6	7	8
Program Function Selection Switch 1 SPB (on H37-3015)	1	2	3	4	5	6	7	8

Note...

x Indicates led's that are always off.

161 When the test is running the displays will follow any changes made in the state of the switch under test, thus each section of the switch can be checked. If there is any discrepancy between the switch settings and the display the corresponding fault-finding flowchart should be followed, either the test switch test flowchart, see Fig D3-19 or the program function selection switch flowchart, see Fig D3-20.

162 As an alternative to using the led display for checking the dil switches a signature analyser may be used to obtain a signature which will indicate the most significant switch which is closed.

163 Connect the signature analyser clips as follows, depending on the switch under test.

163.1 Test Selection Test switch

Start	IC9 pin 3		
Stop			on H37-3016 board
Clock	TP13	$\overline{(RD)}$	
Ground	TP24	(0V)	

163.2 Program Function Selection switch 2 (SPA)

Start and Stop	IC8 pin 3		on H37-3015 board
Clock	TP13	$\overline{(RD)}$	on H37-3016 board
Ground	TP24	(0V)	

163.3 Program Function Selection switch 1 (SPB)

Start and Stop	IC8 pin 4		on H37-3015 board
Clock	TP13	$\overline{(RD)}$	on H37-3016 board
Ground	TP24	(0V)	

164 Set the switches on the signature analyser as follows:

Start	Falling edge, switch in
Stop	Rising edge, switch out
Clock	Rising edge, switch out
Hold, self-test	OFF, switches out

Place the Signature Analyser probe on the +5V supply of the common area board. Press the reset switch on the probe and the reset switch (SA) on the common area board. Do not press the reset switch, SA, during the running of the Test Selection Switch test if the setting of the Test Selection Switch has changed as another test would then be run.

165 The signatures produced for various switch settings are shown below.

TEST SELECTION SWITCH TEST (SPB on H-37-3016)

1	2	3	4	5	6	Signature
OFF	OFF	OFF	OFF	OFF	OFF	6H2H
ON	OFF	OFF	OFF	OFF	OFF	F369
X	ON	OFF	OFF	OFF	OFF	6P1C
X	X	ON	OFF	OFF	OFF	FC70
X	X	X	ON	OFF	OFF	865C
X	X	X	X	ON	OFF	9F32
X	X	X	X	X	ON	94P1

X setting not important

PROGRAM FUNCTION SELECTION SWITCH 2 (SPA)

1	2	3	4	5	6	7	8	Signature
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	32HF
OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	3865
OFF	OFF	OFF	OFF	OFF	OFF	ON	X	4A70
OFF	OFF	OFF	OFF	OFF	ON	X	X	3494
OFF	OFF	OFF	OFF	ON	X	X	X	5669
OFF	OFF	OFF	ON	X	X	X	X	A8AF
OFF	OFF	ON	X	X	X	X	X	3951
OFF	ON	X	X	X	X	X	X	P672
ON	X	X	X	X	X	X	X	U9FF

PROGRAM FUNCTION SELECTION SWITCH 1 (SPB)

1	2	3	4	5	6	7	8	Signature
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	4P19
OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	2538
OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	3494
OFF	OFF	OFF	OFF	OFF	ON	X	X	AFH2
OFF	OFF	OFF	OFF	ON	X	X	X	A2C3
OFF	OFF	OFF	ON	X	X	X	X	FA8A
OFF	OFF	ON	X	X	X	X	X	672A
OFF	ON	X	X	X	X	X	X	399F
ON	X	X	X	X	X	X	X	UFP6

EXTENSION UNIT (ECS)

166 This unit consists of a pec mounted on a frame onto which the module under test can also be mounted. When in use the assembly is plugged into the connector on the control frame assembly normally occupied by the module. The circuit diagram is shown in Fig D3-7.

167 The extension unit interfaces with the extended control, serial, pec of the module to provide the following facilities:

- 167.1 $\pm 12V$ dc supply.
- 167.2 extension of the start interlock chain.
- 167.3 fixed voltages to simulate the A-D inputs to the module.
- 167.4 switched logic 0 and logic 1 inputs to the parallel input ports of the module.
- 167.5 LED indicators driven by the output port.
- 167.6 Three switched relay drives.

168 For the basic functions test and the PROM, RAM, CTC and SIO self-tests, para 68, 102, 109, 117 and 125 respectively, DLP3 to DLP7 (the left-hand four yellow led's) indicate the test number in binary format, and DLP8 to DLP12 indicate the fault number, also in binary format.

TABLE 1: TEST NUMBERS

No	Test
1	Basic functions test
2	PROM self test
3	RAM self test
4	CTC self test
5	SIO self test

TABLE 2: FAULT NUMBERS

No	Basic functions	PROM	RAM	CTC	SIO
0	No fault	No fault	No fault	No fault	No fault
1	*	PROM 1 fail	Either RAM fail	Channel 0 fail	SIO fail
2	*	PROM 2 fail	-	Channel 1 fail	-
3	*	PROM 3 fail	-	Channel 2 fail	-
4	*	-	-	Channel 3 fail	-

* Any fail indication as appropriate to failed section as shown by test indication

169 For the input port tests, para 144, the led's on the extension unit, DLP3 to DLP12 indicate the logic level of each input of the port under test, with the led lit for logic 1 and off for logic 0.

170 The input logic levels are selected by the switch packs SPA and SPB. Fig D3-7 shows SPA and SPB set to give logic 1 to the inputs of port IN0 (see Table 3). This is achieved by pressing the lower end of the switch levers.

171 When the extension unit is used on the analogue-to-digital (A-D) tests, the led's DLP3 to DLP12 give an indication of the voltage present on the channel under test, see para 152 to 158.

172 In a similar manner, the led's are used to indicate the status of the dual-in-line switches on the module under test, see para 159-161.

173 SA, SB and SC are momentary action press switches, which, when pressed, energise the relays RLA, RLC and RLB respectively on the module under test. The operation of RLA causes DLP1 on the extension unit to light, and similarly the operation of RLB and RLC cause DLP12 and DLP2, respectively, to light. These switches are not used in the series of tests described.

TABLE 3 INPUT AND OUTPUT PORTS

Port	Bits (Data bus D0-D7)	Remark
Input (IN0)	0	Auto-tune fail
	1	Trip
	2	Lockout
	3	Press-to-talk (PTT) selected
	4-7	Control mode status word (cmsw)
Input (IN1)	0	Extended
	1	Available
	2	Auxiliaries selected
	3	Auxiliaries complete
	4	H.T ON
Output *	5	Auto-tune complete
	0	PTT
	1	Aux. ON
	2	H.T. ON
	3	Lockout reset
	6	Initiate re-tune

Note*...

The logic outputs shown in the remarks column refer to the polarities written to the output port from the CPU. The electrical outputs from the board are inverted from these.

TABLE 4 SELF-TEST AND SA TEST SELECTION

Test	Test Selection Switch (SPB)					
	1	2	3	4	5	6
Basic function test	OFF	ON	ON	ON	ON	ON
PROM self-test	ON	OFF	ON	ON	ON	ON
RAM self-test	OFF	OFF	ON	ON	ON	ON
CTC self-test	ON	ON	OFF	ON	ON	ON
SIO self-test	OFF	ON	OFF	ON	ON	ON
Test selection switch test	OFF	OFF	OFF	ON	ON	ON
Program function selection switch 2 test	ON	ON	ON	OFF	ON	ON
Program function selection switch 1 test	OFF	ON	ON	OFF	ON	ON
A-D converter test	ON	ON	OFF	OFF	ON	ON
PROM SA test	ON	OFF	ON	ON	ON	OFF
RAM SA test	OFF	OFF	ON	ON	ON	OFF
CTC SA test	ON	ON	OFF	ON	ON	OFF
SIO SA test	OFF	ON	OFF	ON	ON	OFF
Output port SA test	ON	OFF	OFF	ON	ON	OFF
Input port 2 test	ON	ON	ON	OFF	ON	OFF
Input port 3 test	OFF	ON	ON	OFF	ON	OFF

TABLE 5 INPUT PORT TEST 2

Indicator on test extender	DLP3	DLP4	DLP6	DLP7	DLP8	DLP9	DLP11	DLP12
Control switch on test extender	SPA1	SPA2	SPA3	SPA4	SPB1	SBP2	SPB3	SPB4
Input port IC pin	6 2	6 4	6 6	6 10	9 2	9 4	9 6	9 10
Input port connections	RP4.16 RP4.1	RP4.15 RP4.2	RP4.14 RP4.3	RP4.13 RP4.4	IC12 Pins 2 and 3 RP4.12 RP4.5 RP2.5	IC12 Pins 4 and 5 RP4.11 RP4.6 RP2.6	IC12 Pins 6 and 7 RP4.10 RP4.7 RP2.7	IC12 Pins 11 and 12 RP4.9 RP4.8 RP2.8
Edge connector	K	H	J	21	1	32	R	F
Function	cmsw3	cmsw2	cmsw1	cmsw0	PTT Sel	Lockout	Trip	Auto-tune fail

TABLE 6 INPUT PORT TEST 3

Indicator on test extender	DLP3	DLP4	DLP6	DLP7	DLP8	DLP9	DLP11	DLP12
Control switch on test extender	SPA1	SPA2	SPA3	SPA4	SPB1	SPB2	SPB3	SPB4
Input port ICpin	9 14	9 12	13 2	13 4	13 6	13 10	13 14	13 16
Input port connections	0V	0V	IC17 pins 6 and 7 RP6.12	IC17 pins 4 and 5 RP6.11	IC17 pins 2 and 3	IC17 pins 14 and 15 RP6.10	IC17 pins 9 and 10 RP6.13	IC17 pins 11 and 12 RP6.15
RP6.14								
Edge connector			RP6.5 RP1.6 L	RP6.6 RP1.7 28	RP6.7 RP1.8 19	RP6.4 RP1.5 13	RP6.2 RP1.3 AD	RP6.3 RP1.1 20
Function	-	-	Auto-tune Complete	H.T. ON	Aux Complete	Aux Selected	Available	Extended

TABLE 7 LINK SETTINGS

Link No.	Setting	Remarks
Common Area Board H37-3016-01		
1	A	Enables the watchdog timer to reset the CPU
	B	Disables the watchdog timer for test purposes
2	B	SIO's RTSA connected to DCDA
3	B	SIO channel B Tx data connected to output
	A	SIO channel B Tx data linked to channel B Rx data for test purposes
4	B	SIO channel A Tx data connected to output
	A	SIO channel A Tx data linked to channel A Rx data for test purposes
6	B	SIO channel A Rx data connected to line for V28 level input
	A	SIO channel A Rx data connected to modem port for logic level input
7	A	SIO RTSB connected to DCDB
8	A	SIO CTSB connected to 0V
	B	SIO CTSB connected to DTRB for test purposes
9	A	SIO CTSA connected to 0V
	B	SIO CTSA connected to DTRA for test purposes
21		These links connected when 4 kbyte
22	B	PROMs are used in IC4, IC6 and IC7
23		positions
24	Fitted	System clock connected
25	Fitted	WAIT input to CPU connected
26	Fitted	CTC INT output connected to CPU INT input
27	Fitted	SIO INT output connected to CPU INT input

TABLE 7 (cont.)

28	Fitted	X16 baud rate clock output from CTC connected to SIO
LKP1	Fitted	CPU connected to data bus. LKP1 removed for test purposes
LKP2	Fitted	2 kbyte PROMs in IC1, IC2 and IC3 positions
LKP3	Fitted	Input lines connected to input ports
LKP9	Fitted	Input and output ports connected to data bus

LKP1	Extended serial board Fitted	I/O ports connected to data BUS
------	---------------------------------	---------------------------------

LKP = Link Pack containing up to 8 links

TABLE 8 CONTROL SYSTEM CONFIGURATION SWITCHING

Two program function selection switches SPB (No.1) and SPA (No.2), are fitted to the extended control serial board

Switch positions: Closed = ON

Switch	Remarks
SPA 1	This is used to select whether metering information from the amplifier to remote control is supplied on a regular timing or on request. ON = regular timing
SPA 2	This switch enables or disables a block check on the serial control data. The remote control command and revertive data is composed of data blocks. Each block can contain from one to 17 data bytes. If the block check is enabled a sum of the data bytes in a block to be transmitted is formed and this 'check-sum' byte is added to the block for transmission. When the block is received at the distant terminal a check-sum is formed of the original data and compared to the transmitted check-sum. If the comparison shows an invalid state the data block is not acted upon. This option can be used in high integrity systems. ON = block check disabled
SPA 3	This switch determines whether the MUTE signal to the drive unit comes via the serial remote control channel or as a hard-wired input to the microprocessor control board. (The second case eliminates the need for a separate mute line in remote control applications). ON - Serial channel mute OFF - Hard-wired mute
SPA 4	Not used
SPA 5	Not used
SPA 6	Not used

TABLE 8 (Cont.)

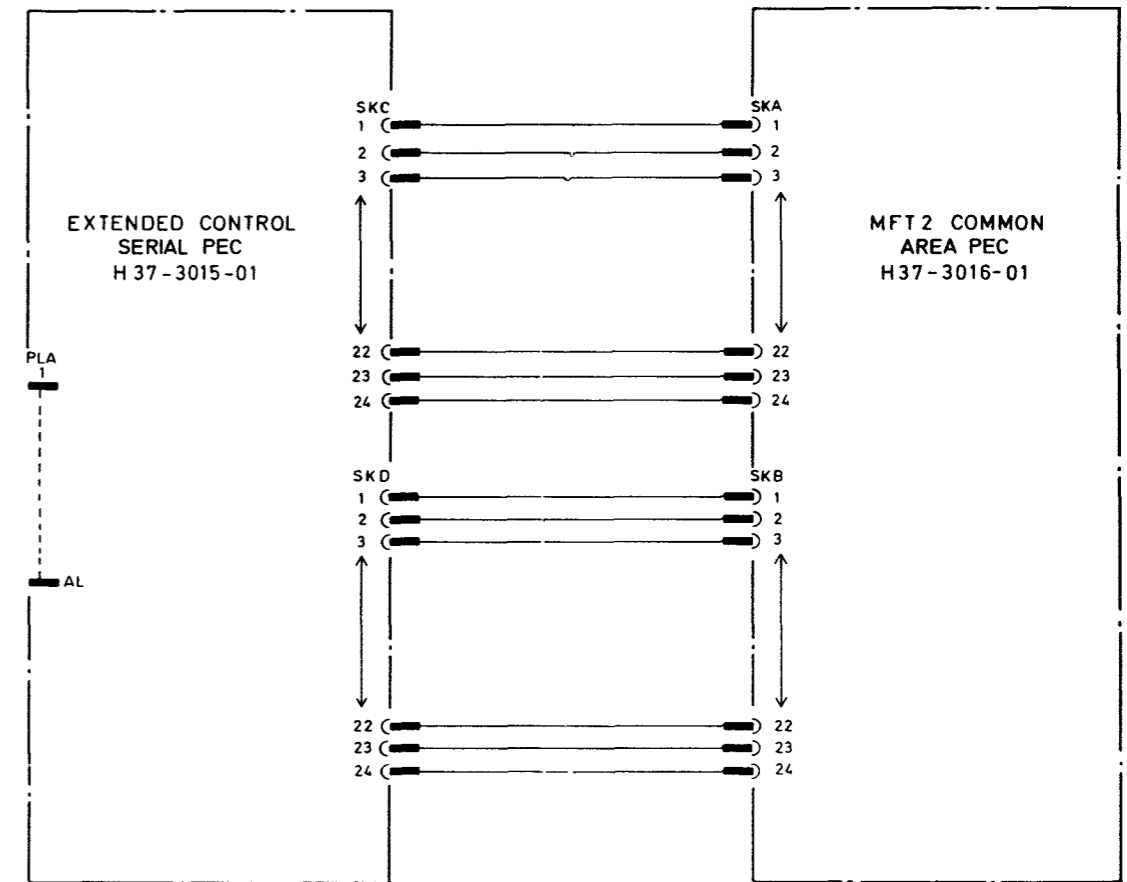
SPA 7 and 8

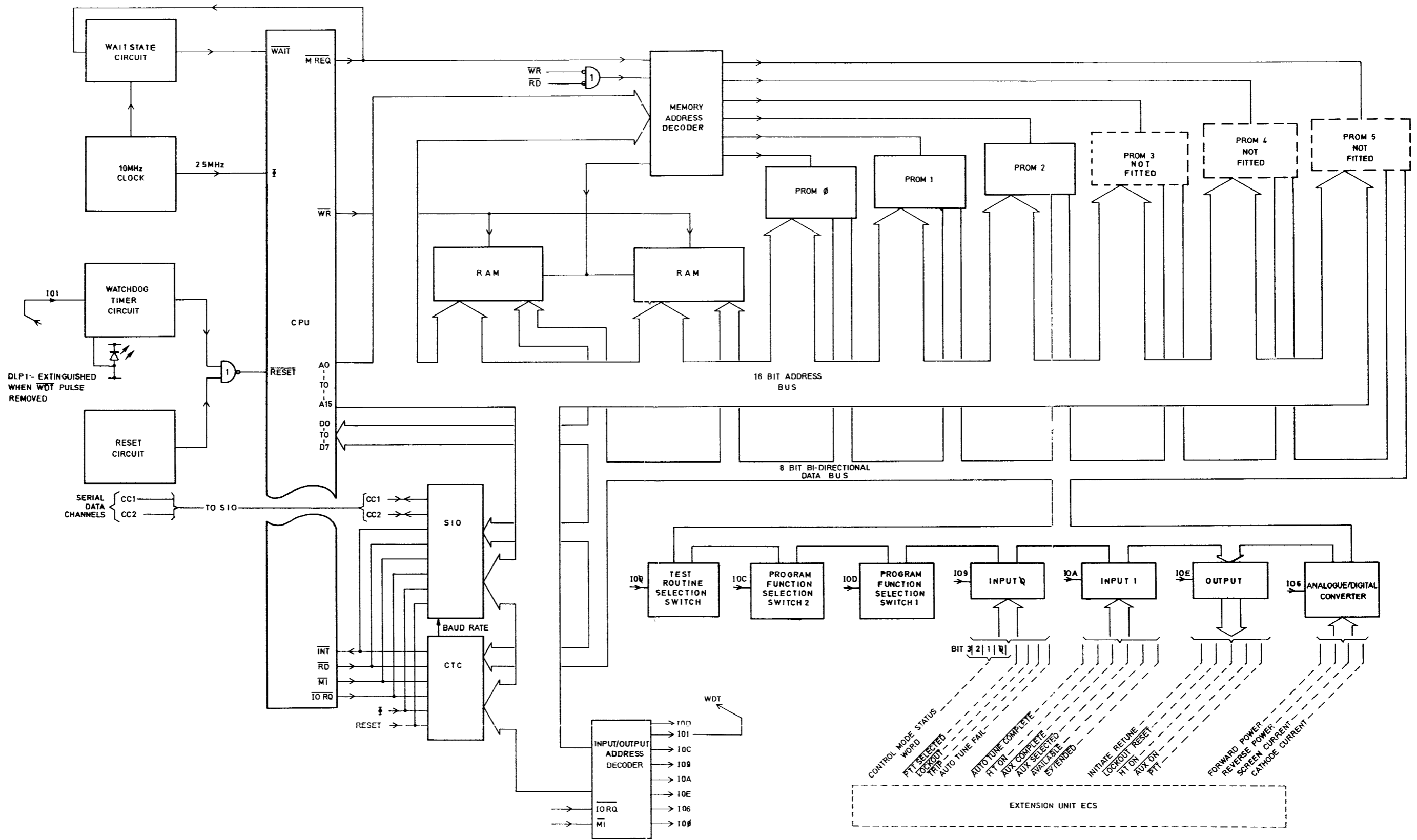
These two switches determine the baud rate for the remote control serial channels. The switch settings for the four possible baud rates are shown:

Baud rate	Switch setting	
	8	7
50	ON	ON
110	OFF	ON
300	ON	OFF
600	OFF	OFF

SPB

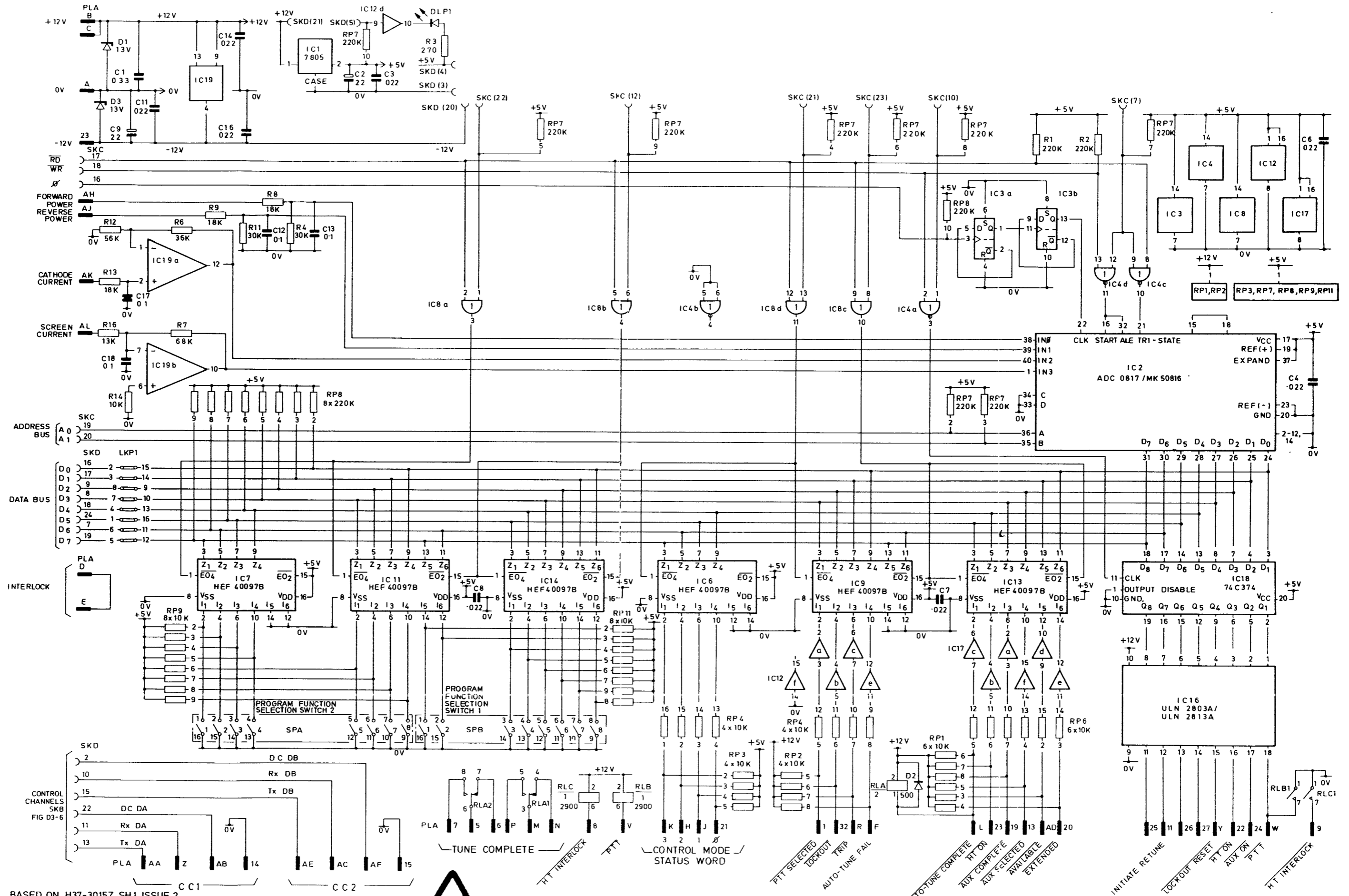
Not used in amplifier configuration





BASED ON H37-2892G SH 1 ISSUE 1
Fig D3-2

Module, extended control, serial, 5820-99-795-9173: block diagram



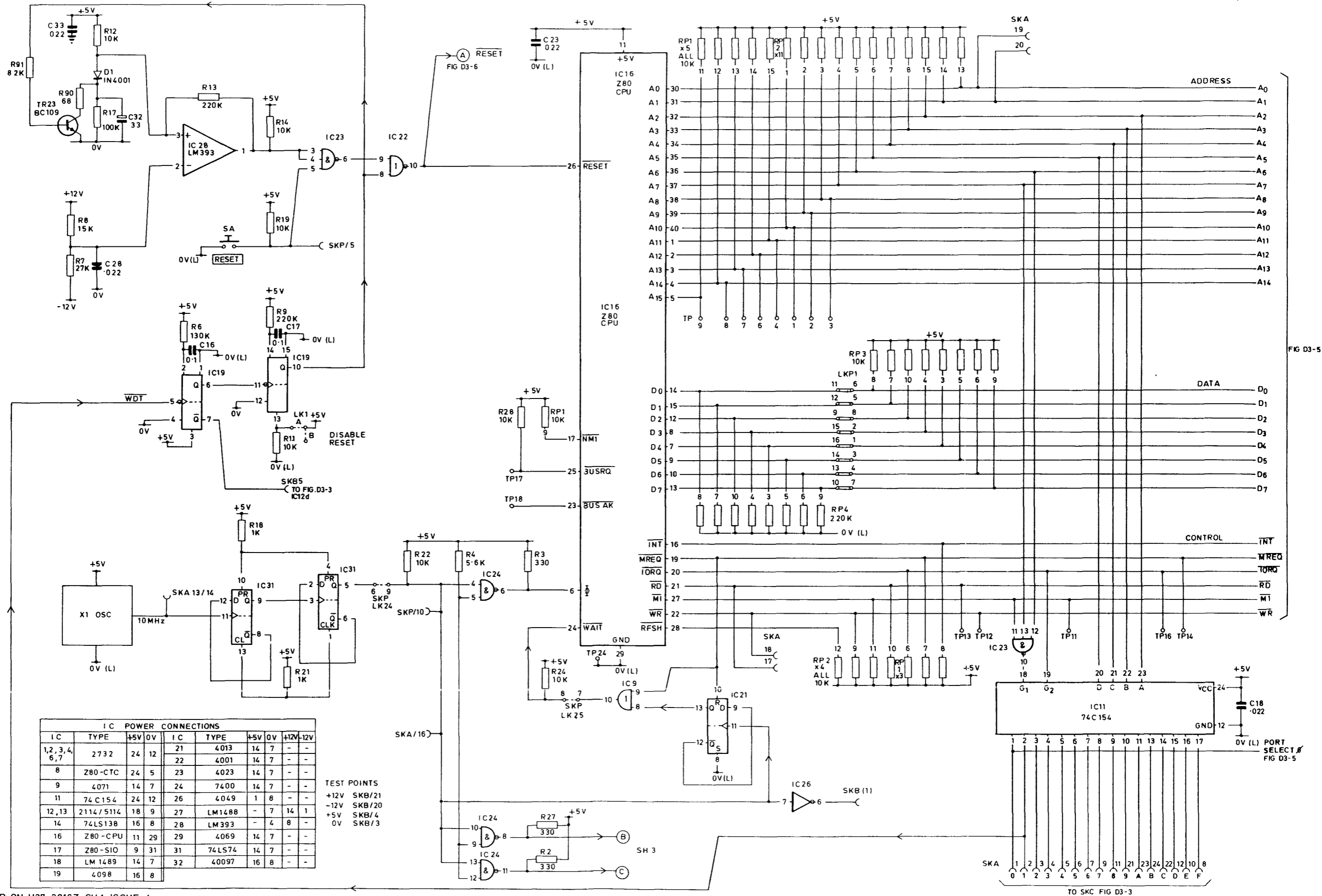
BASED ON H37-3015Z SH1 ISSUE 2

Fig D3-3



Extended control, serial, PEC, H37-3015-01 : circuit diagram

Fig D3-3



I C POWER CONNECTIONS									
I C	TYPE	+5V	0V	I C	TYPE	+5V	0V	+12V	-12V
1,2,3,4,6,7	2732	24	12	21	4013	14	7	-	-
8	Z80-CTC	24	5	22	4001	14	7	-	-
9	4071	14	7	23	4023	14	7	-	-
11	74C154	24	12	24	7400	14	7	-	-
12,13	2114/5114	18	9	26	4049	1	8	-	-
14	74LS138	16	8	27	LM1488	-	7	14	1
16	Z80-CPU	11	29	28	LM393	-	4	8	-
17	Z80-SIO	9	31	29	4069	14	7	-	-
18	LM1489	14	7	31	74LS74	14	7	-	-
19	4098	16	8	32	40097	16	8	-	-

TEST POINTS
 +12V SKB/21
 -12V SKB/20
 +5V SKB/4
 0V SKB/3

BASED ON H37-3016Z SH1 ISSUE 4

Fig D3-4

CAUTION
 THIS BOARD/UNIT CONTAINS
 STATIC SENSITIVE DEVICES.



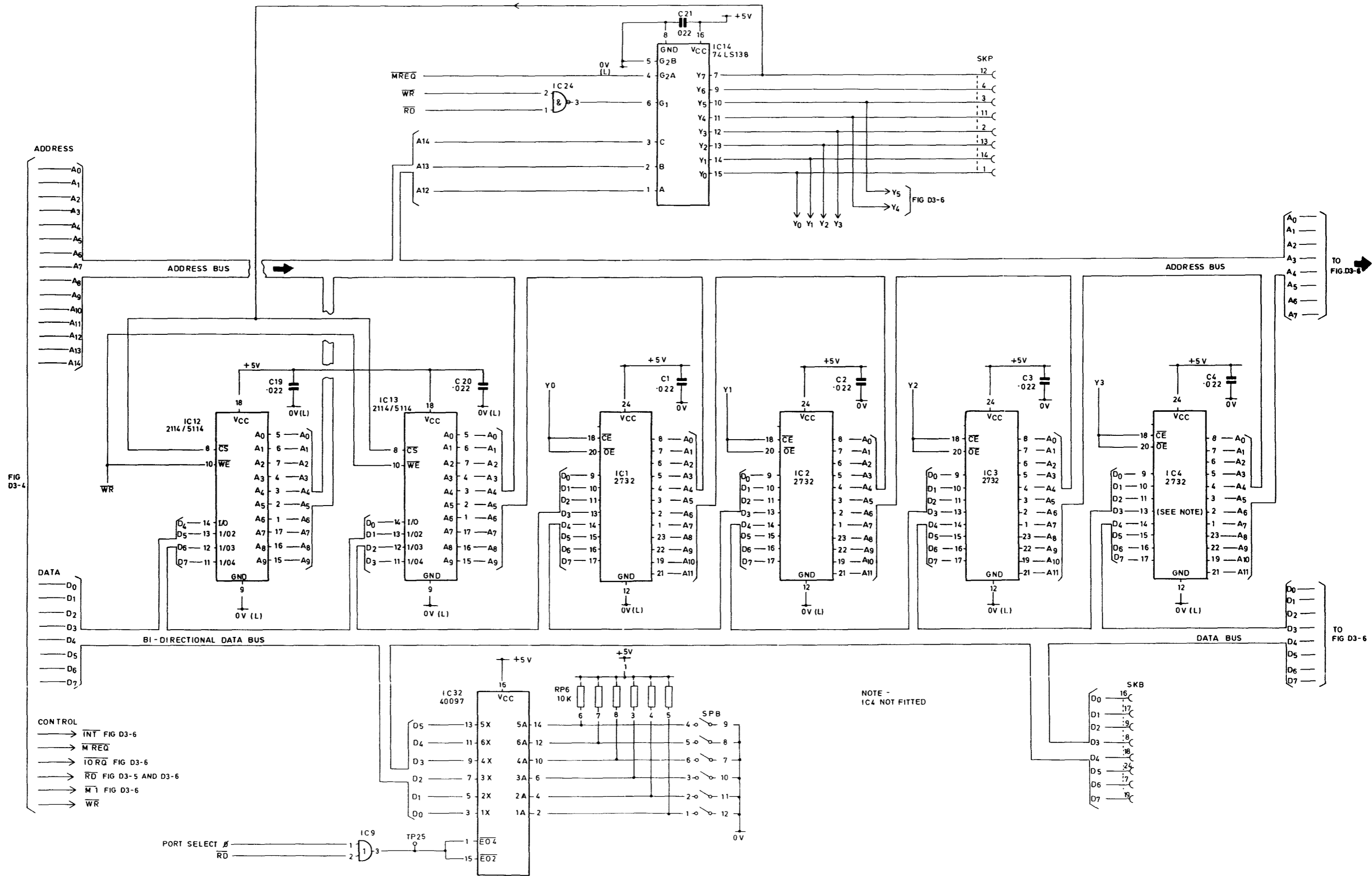
MFT2 common area, H37-3016-01: circuit diagram

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Fig D3-4

Sub-sect D3

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BASED ON H37 3016Z SH 2 ISSUE 4

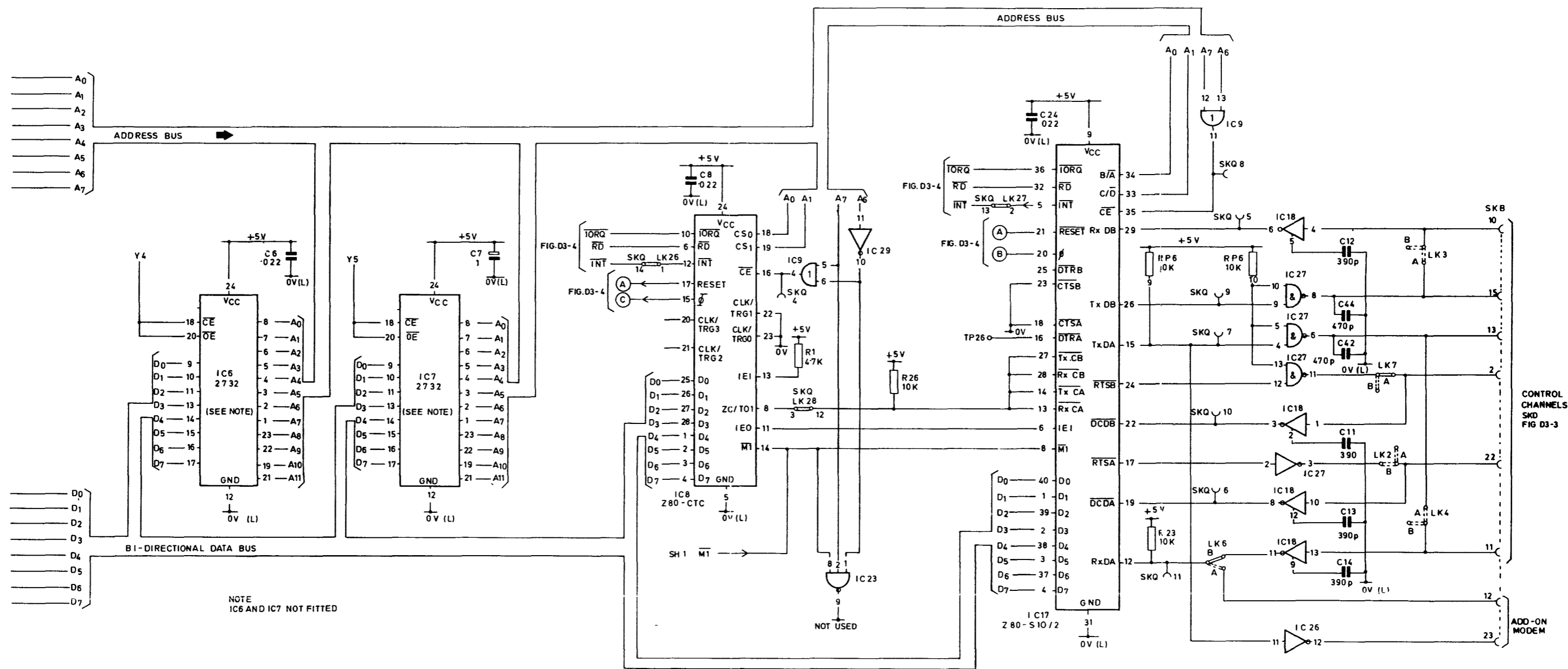
Fig D3-5

CAUTION
 THIS BOARD/UNIT CONTAINS
 STATIC SENSITIVE DEVICES



MFT2 common area, H37-3016-01: circuit diagram

Fig D3-5



BASED ON H37-3016Z SH 3 ISSUE 5

Fig D3-6

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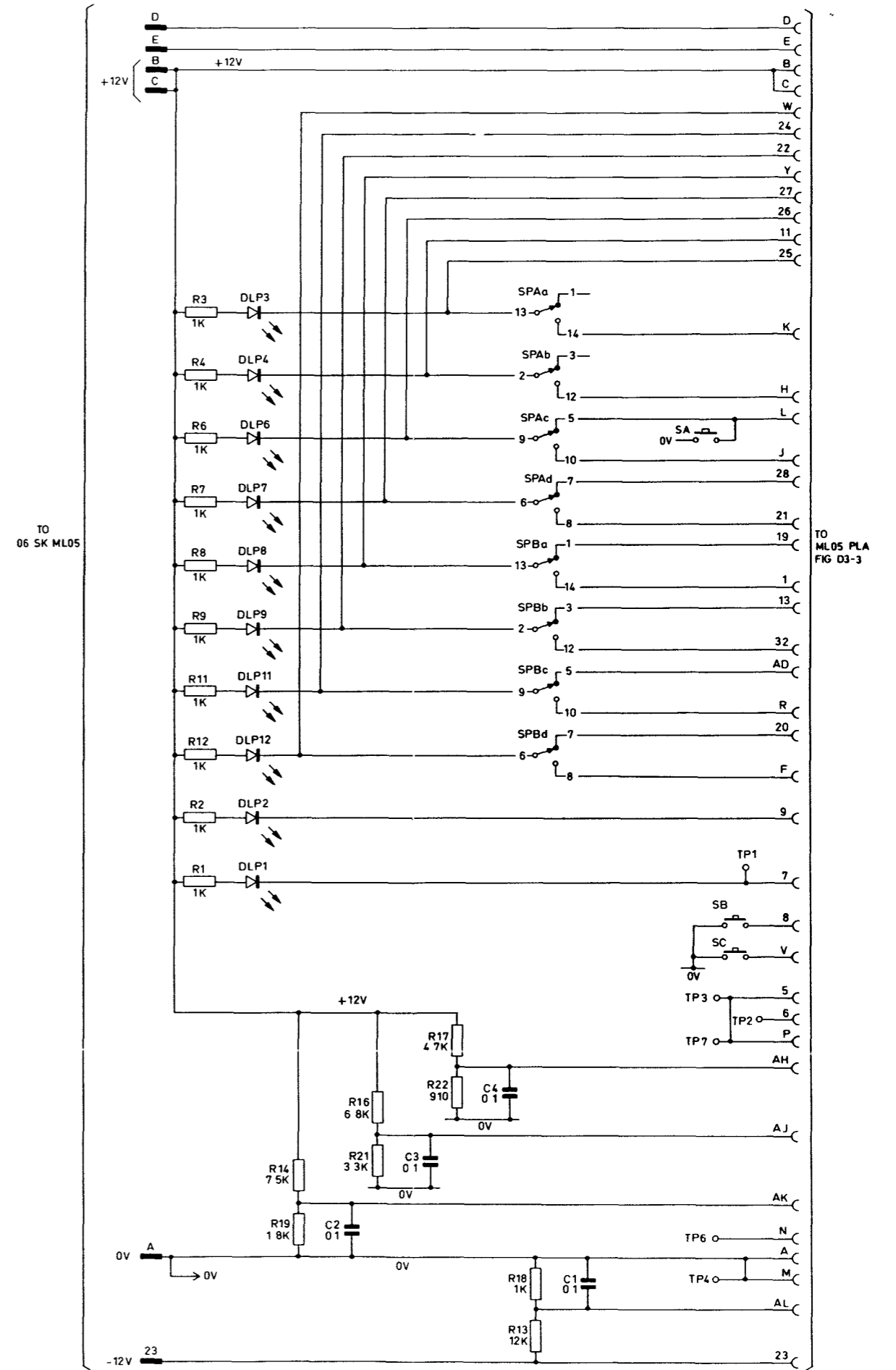
CAUTION
THIS BOARD/UNIT CONTAINS
STATIC SENSITIVE DEVICES.



MFT2 common area, H37-3016-01 : circuit diagram

Fig D3-6

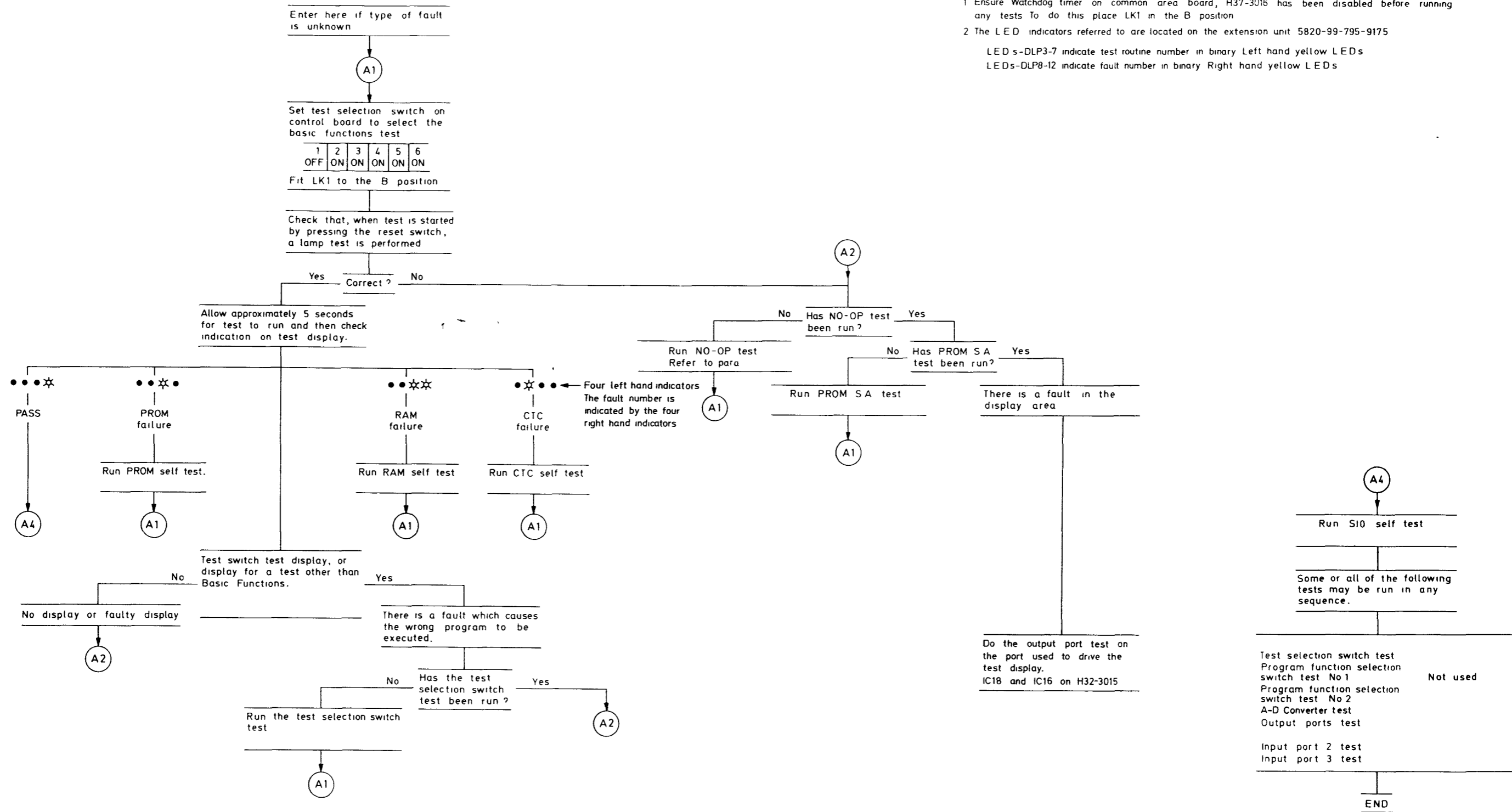
Sub-sect D3
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BASED ON H37-3203Z SH 1 ISSUE 1
Fig D3-7

Extension unit (ECS) 5820-99-795-9175 : circuit diagram

Fig D3-7



1 Ensure Watchdog timer on common area board, H37-3016 has been disabled before running any tests To do this place LK1 in the B position

2 The LED indicators referred to are located on the extension unit 5820-99-795-9175

LEDs-DLP3-7 indicate test routine number in binary Left hand yellow LEDs
LEDs-DLP8-12 indicate fault number in binary Right hand yellow LEDs

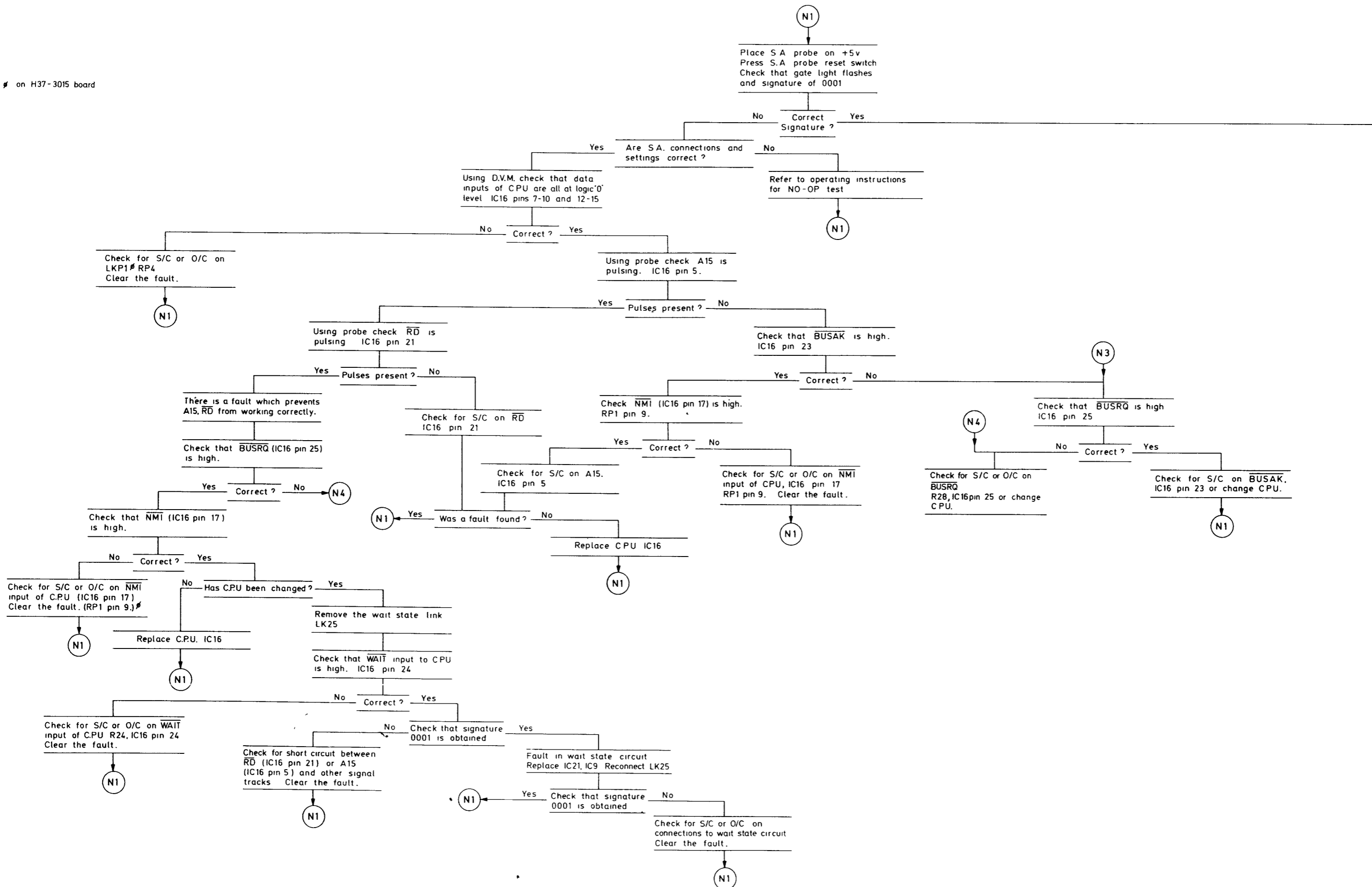
BASED ON H37-2892Z SH 2 ISSUE 1
Fig D3-8

BITS:overall fault finding flowchart

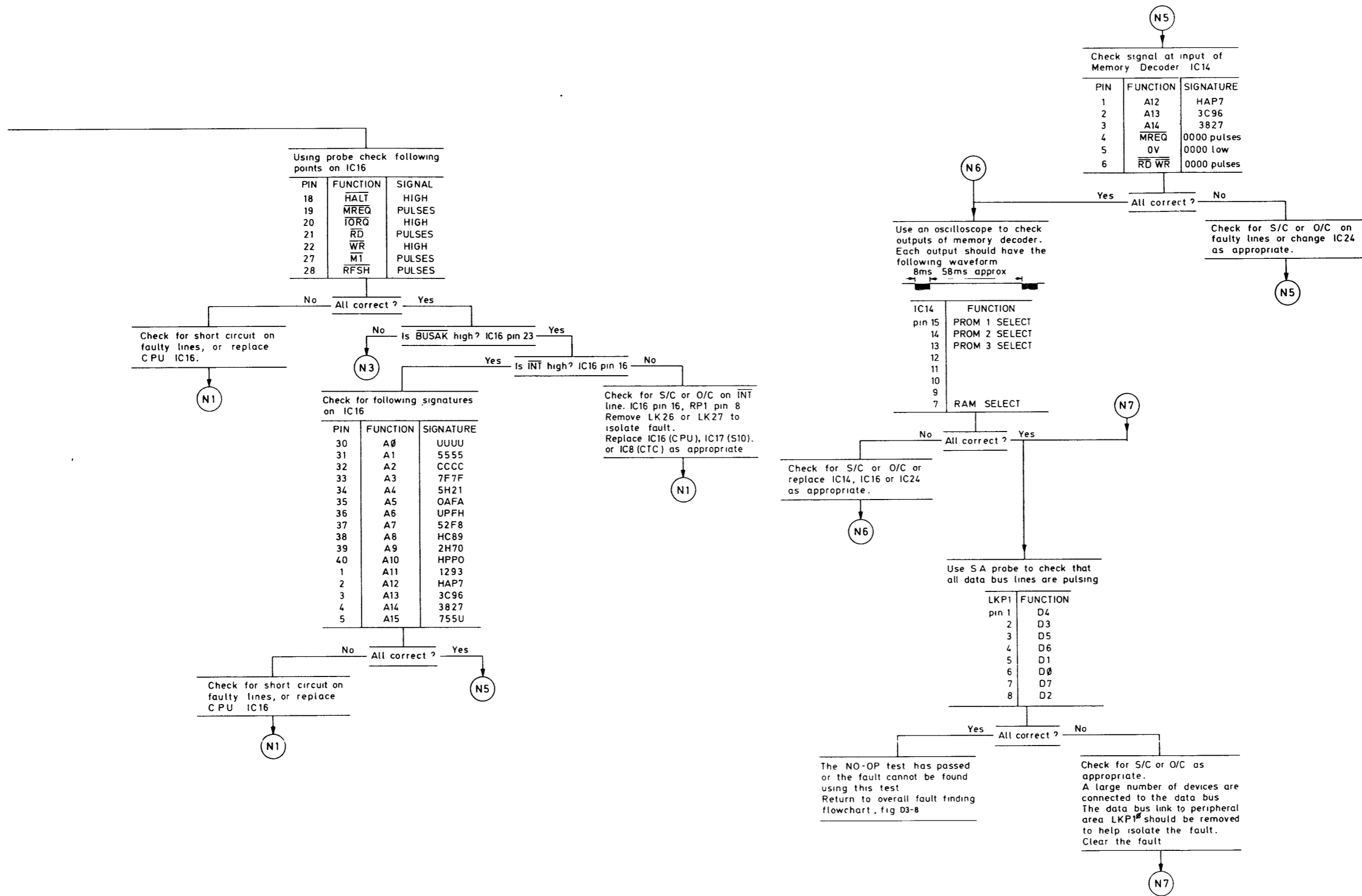
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Fig D3-8
Sub-sect D3
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on H37-3015 board



No-op flowchart



BASED ON H37-2892Z SH 4 ISSUE 2

Fig D3-10

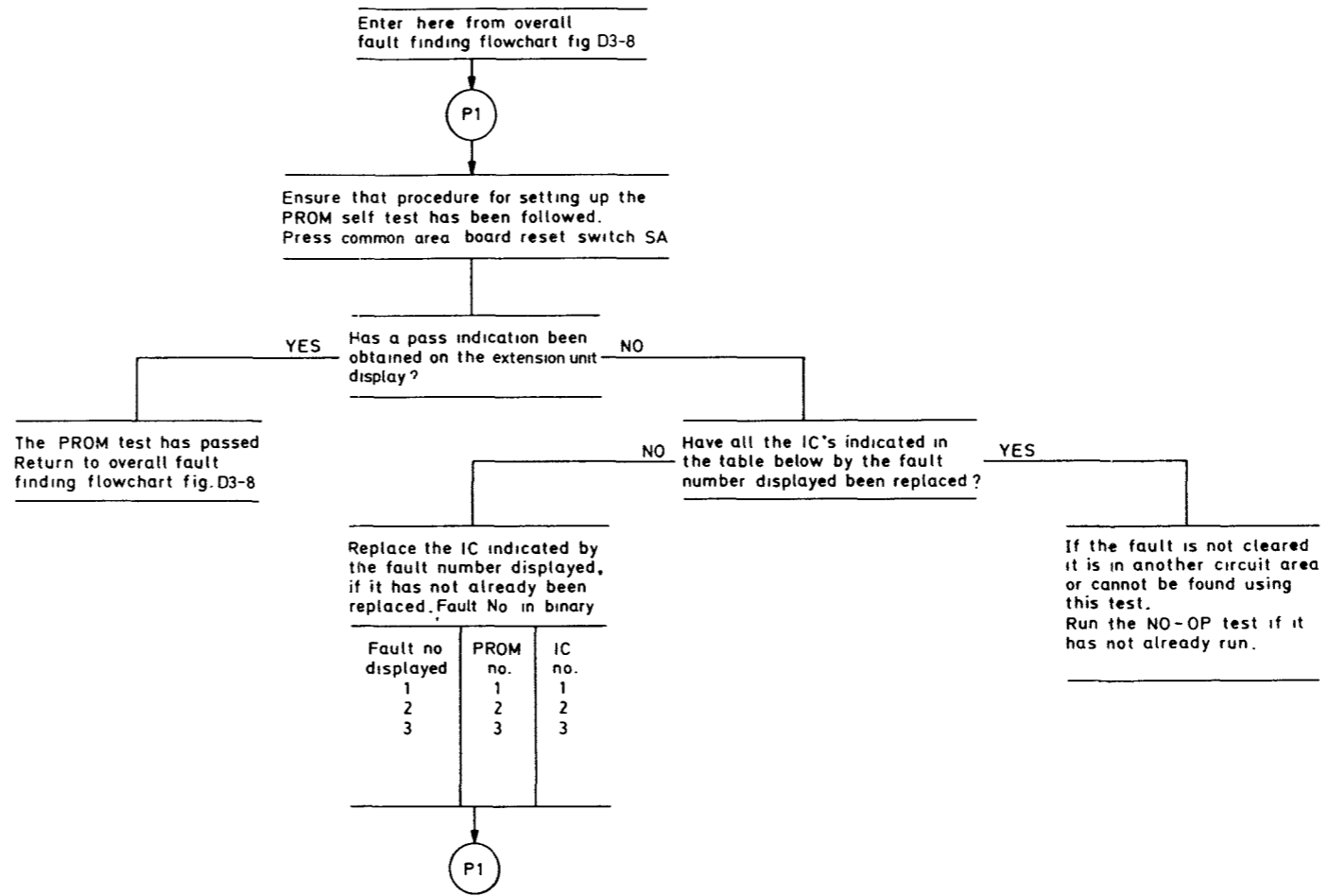
Jan 88

No-op flowchart

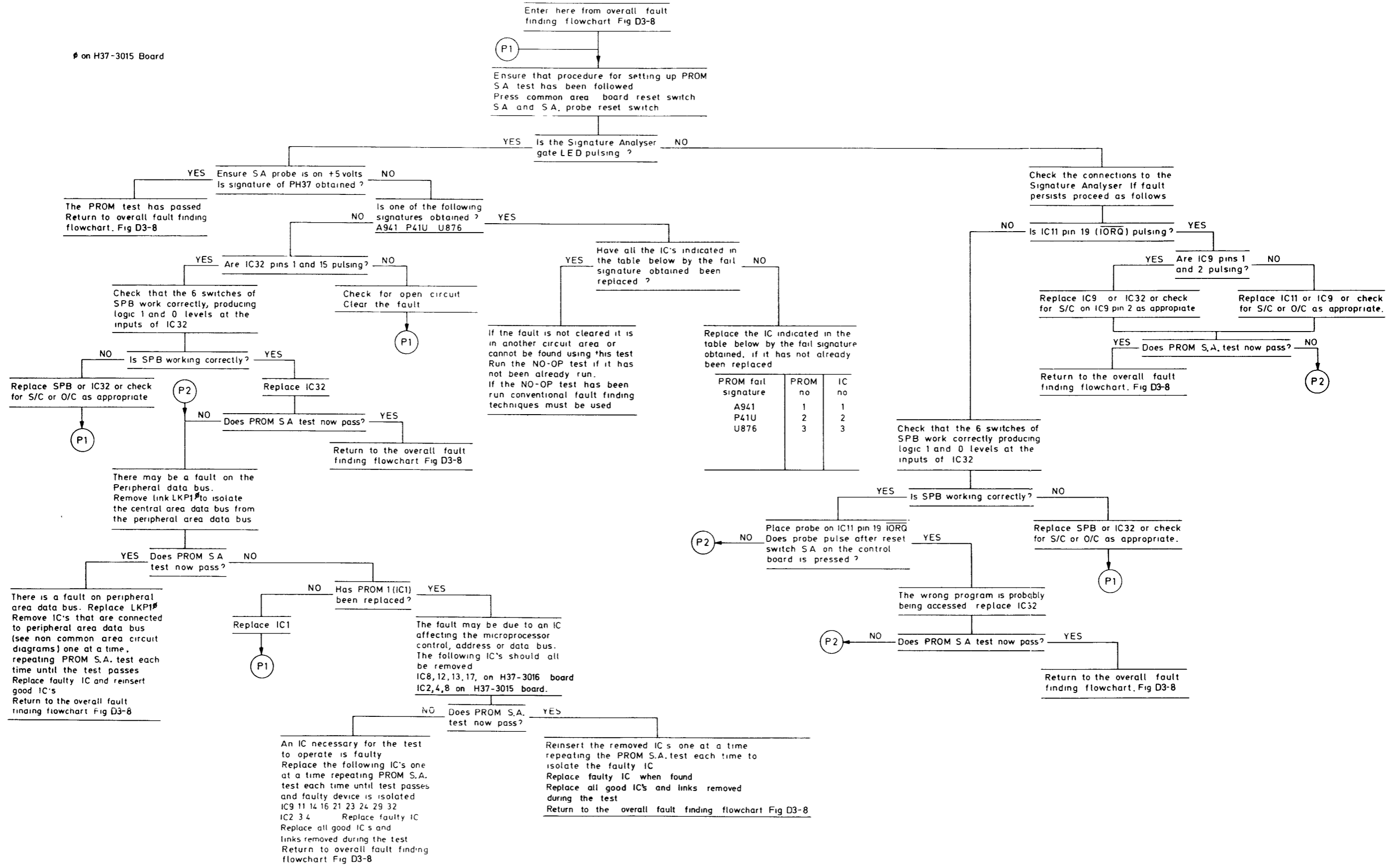
Fig D3-10

Sub-sect D3

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⌀ on H37-3015 Board

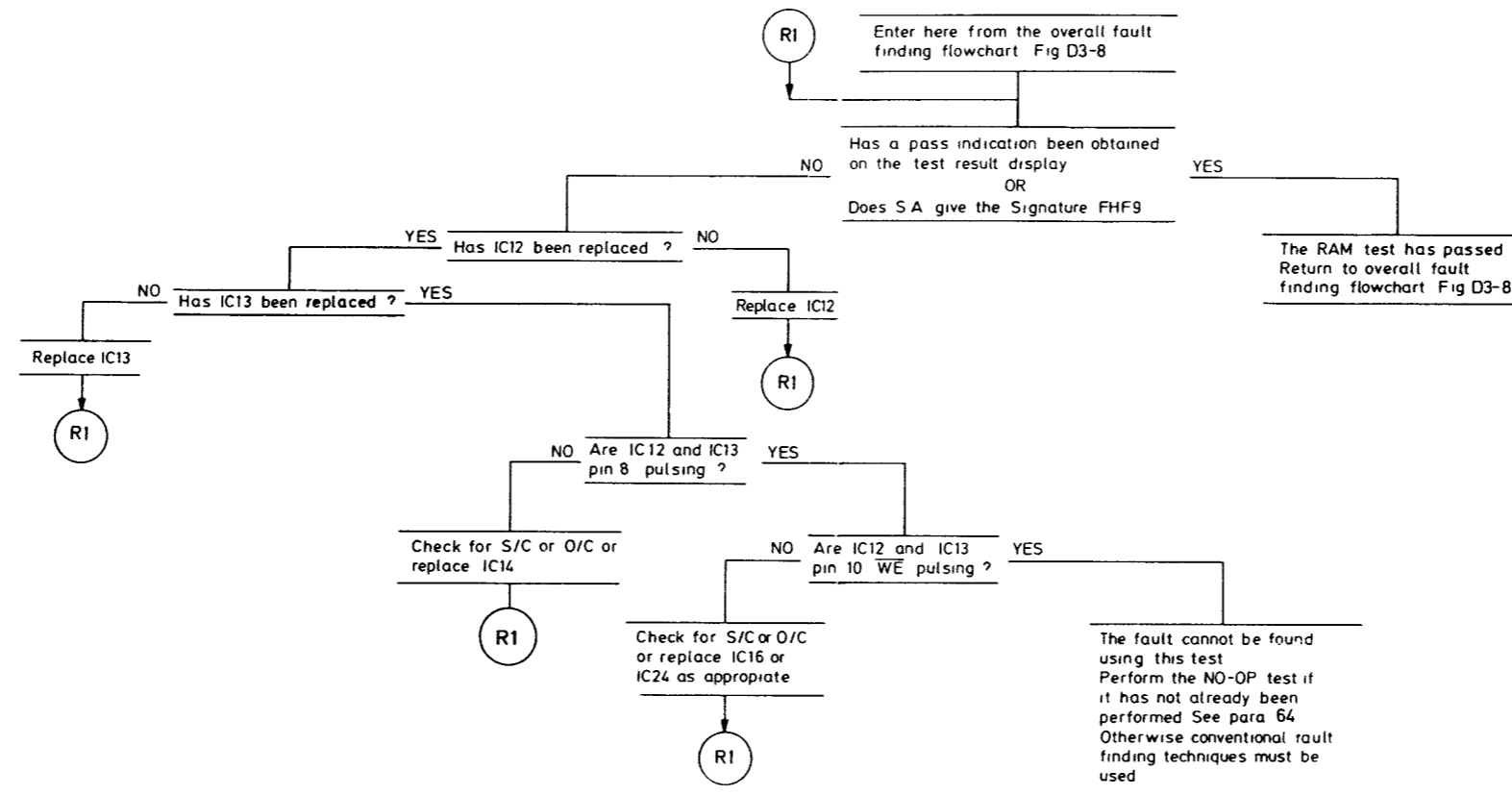


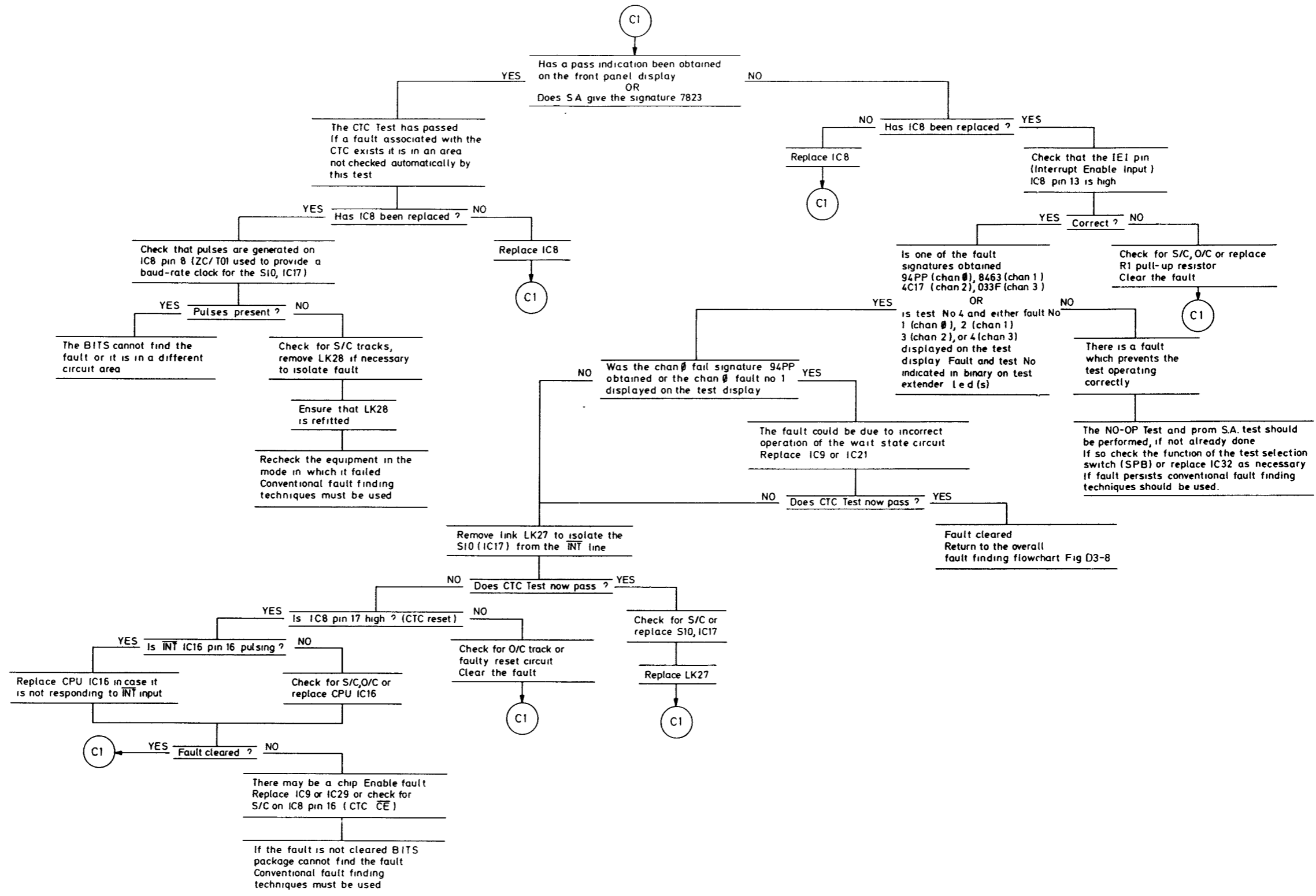
BASED ON H37-2892Z SH 6 ISSUE 2

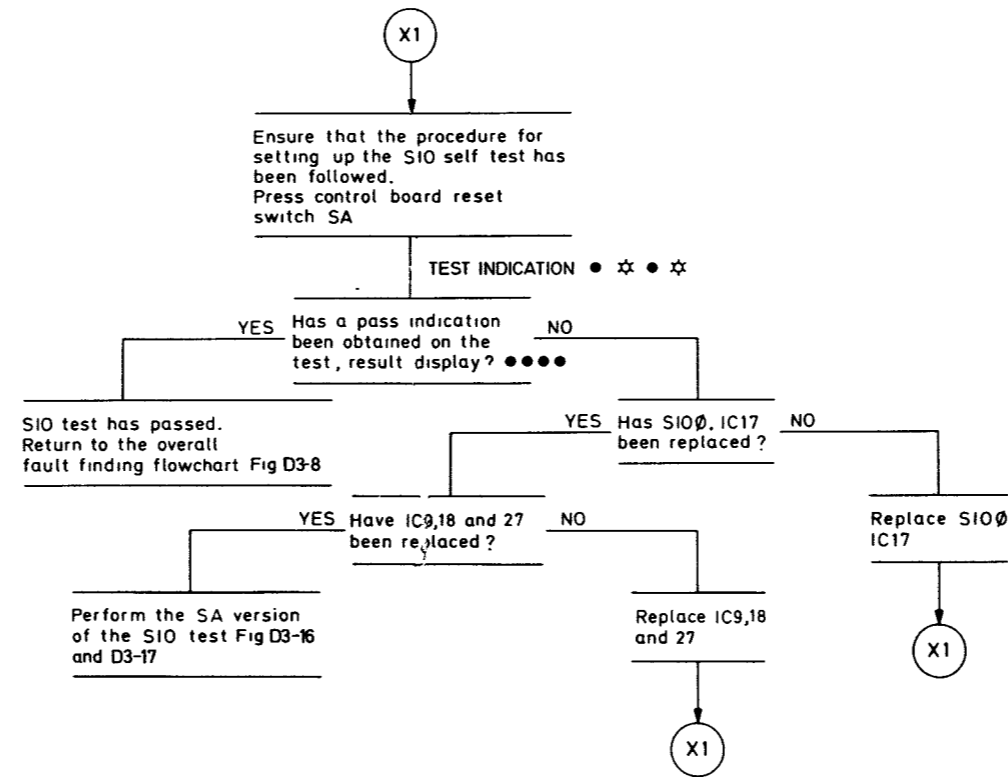
Fig D3-12

PROM: signature analysis flowchart

Fig D3-12







SIO: self-test flowchart

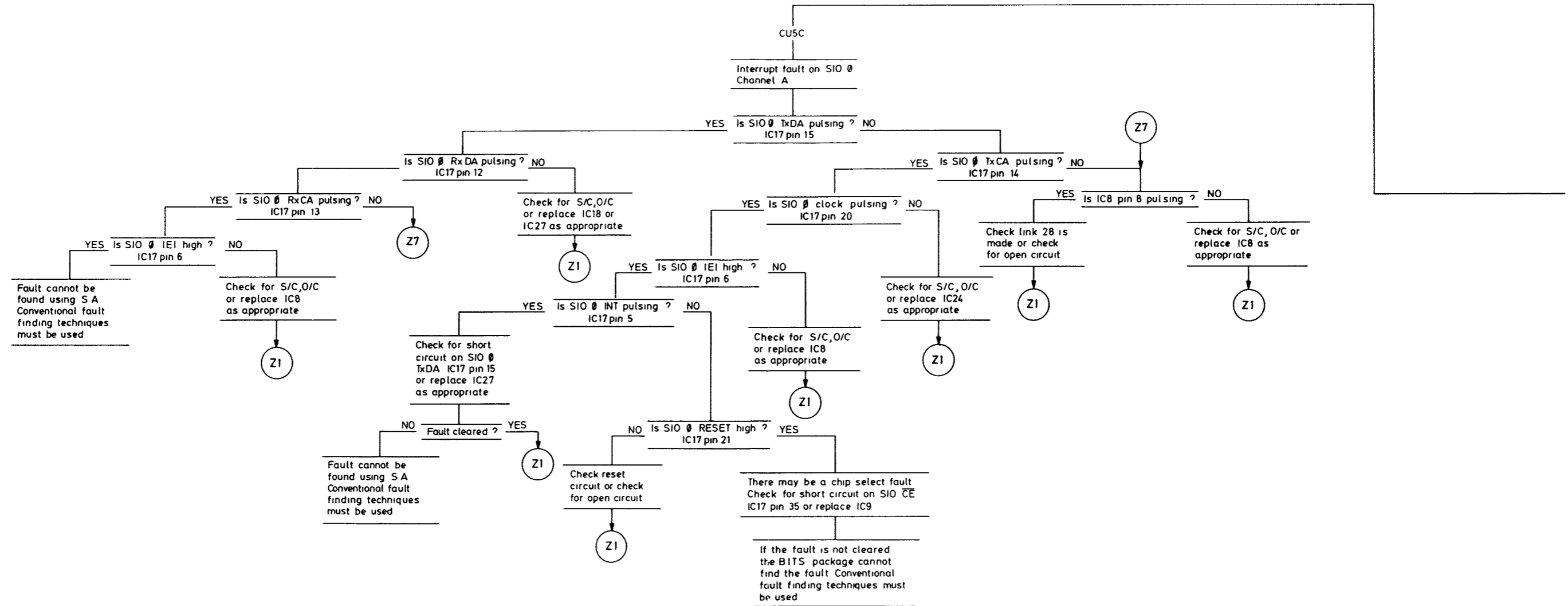
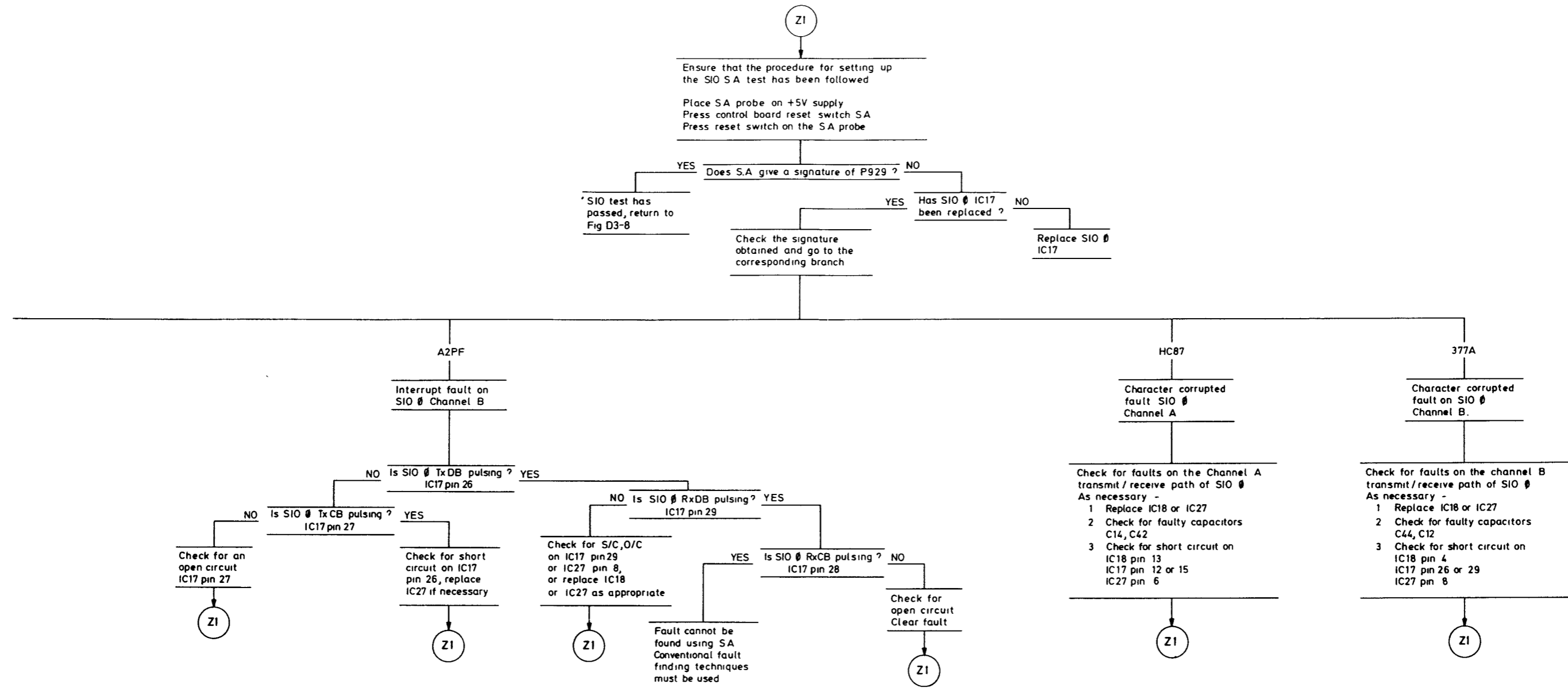


Fig D3-16

SIO: signature analysis test flowchart



1 All components on H37-3016 board unless otherwise stated

Table I

Port	IC on H37-3015	Function	Decoder Output
14	18	Amplifier Control	IC11 pin 16

The signatures on the output lines should be as follows

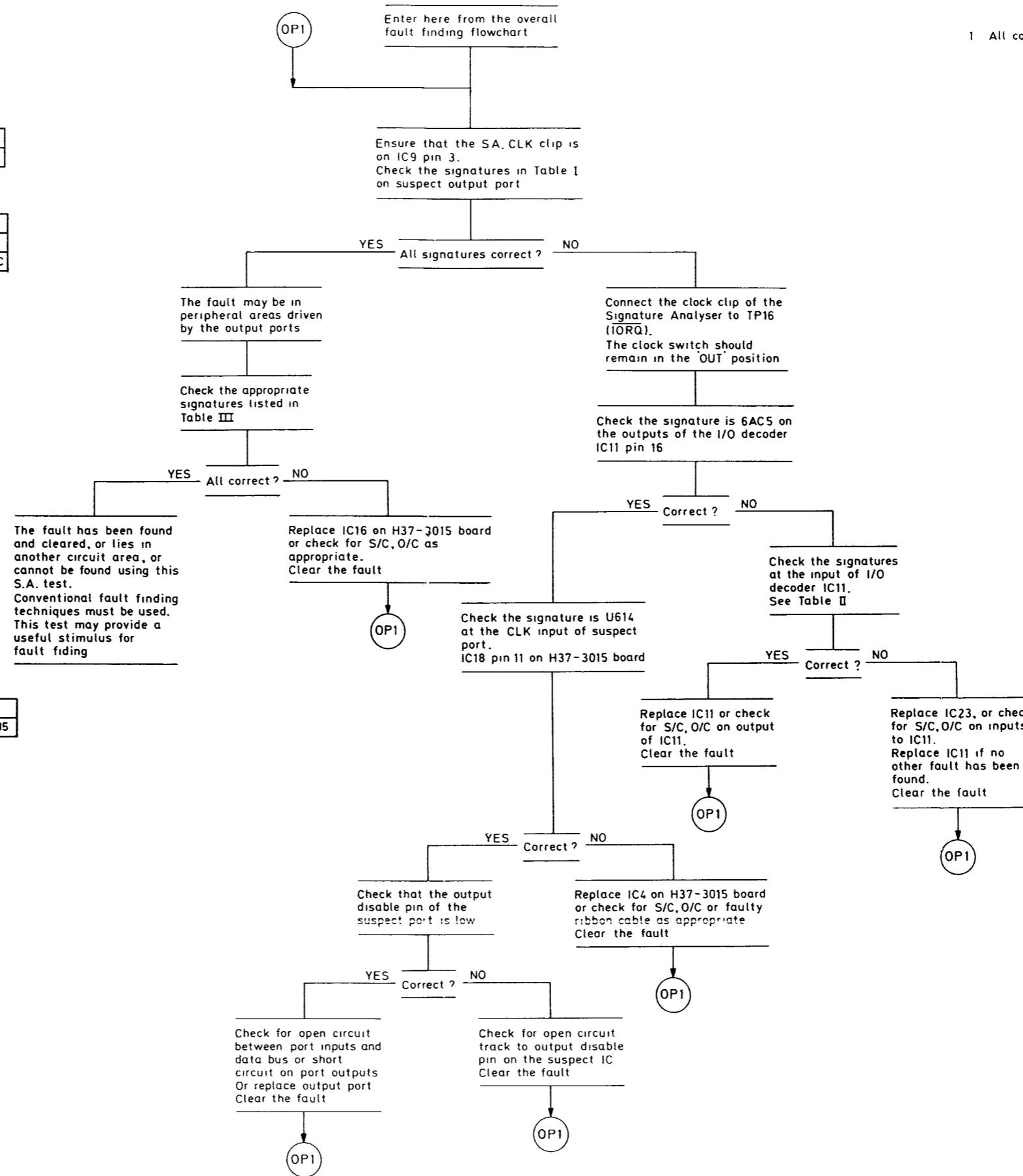
	D0	D1	D2	D3	D4	D5	D6	D7
IC 18 pin	2	5	6	9	12	15	16	19
Signature	0065	00C3	0059	00AH	0056	002C	0094	00FC

Table II

IC11	Signature
pin 23	0000 pulsing
22	U61H
21	U61H
20	U61H
18	868A
19	pulsing

Table III

IC16 pin	18	17	16	15	14	13	12	11
Signature	009C	004H	00A7	0053	00A8	00H5	006A	0035



BASED ON H37-2892Z SH12 ISSUE 1

Fig D3-18

Jan 88

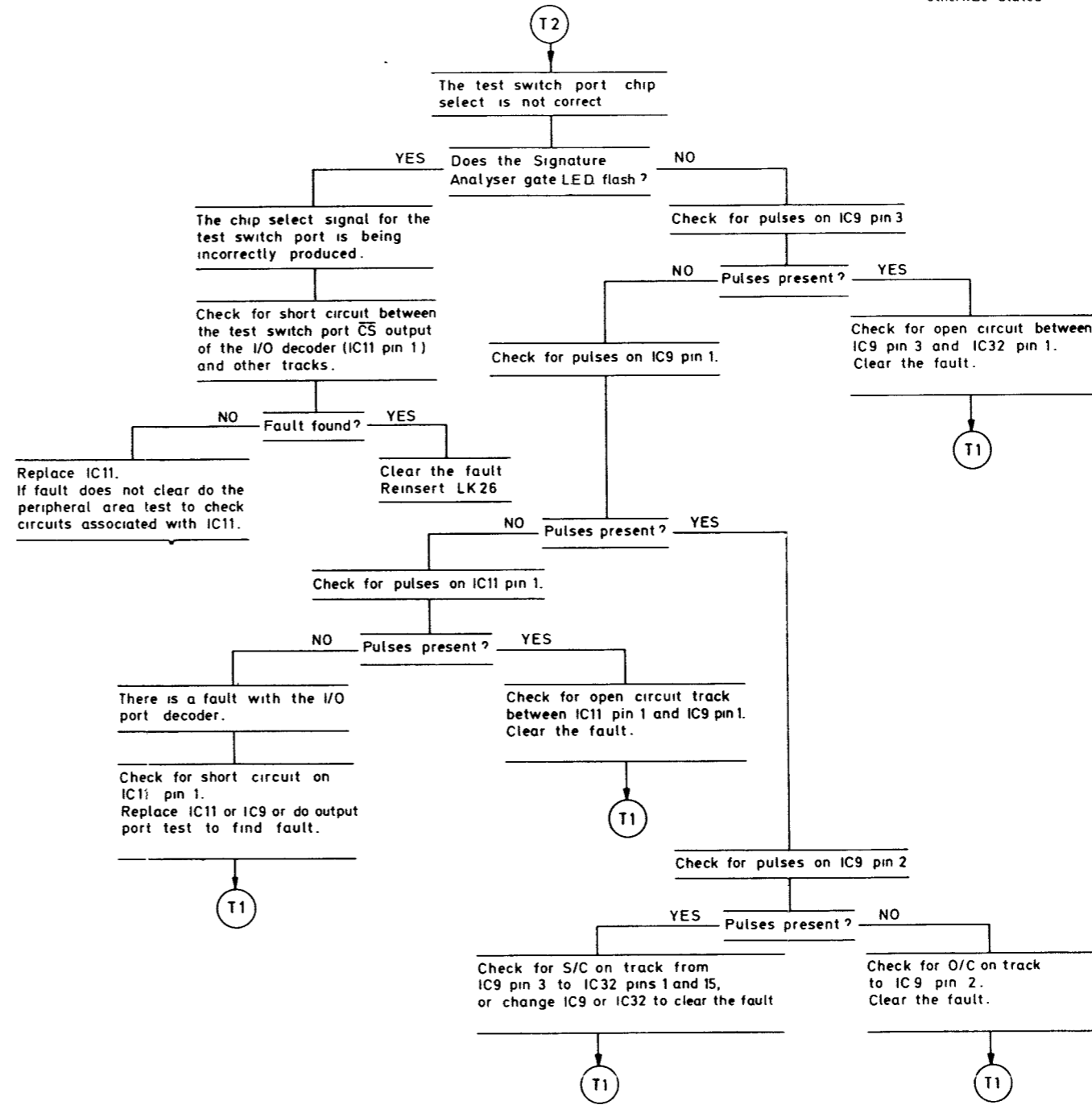
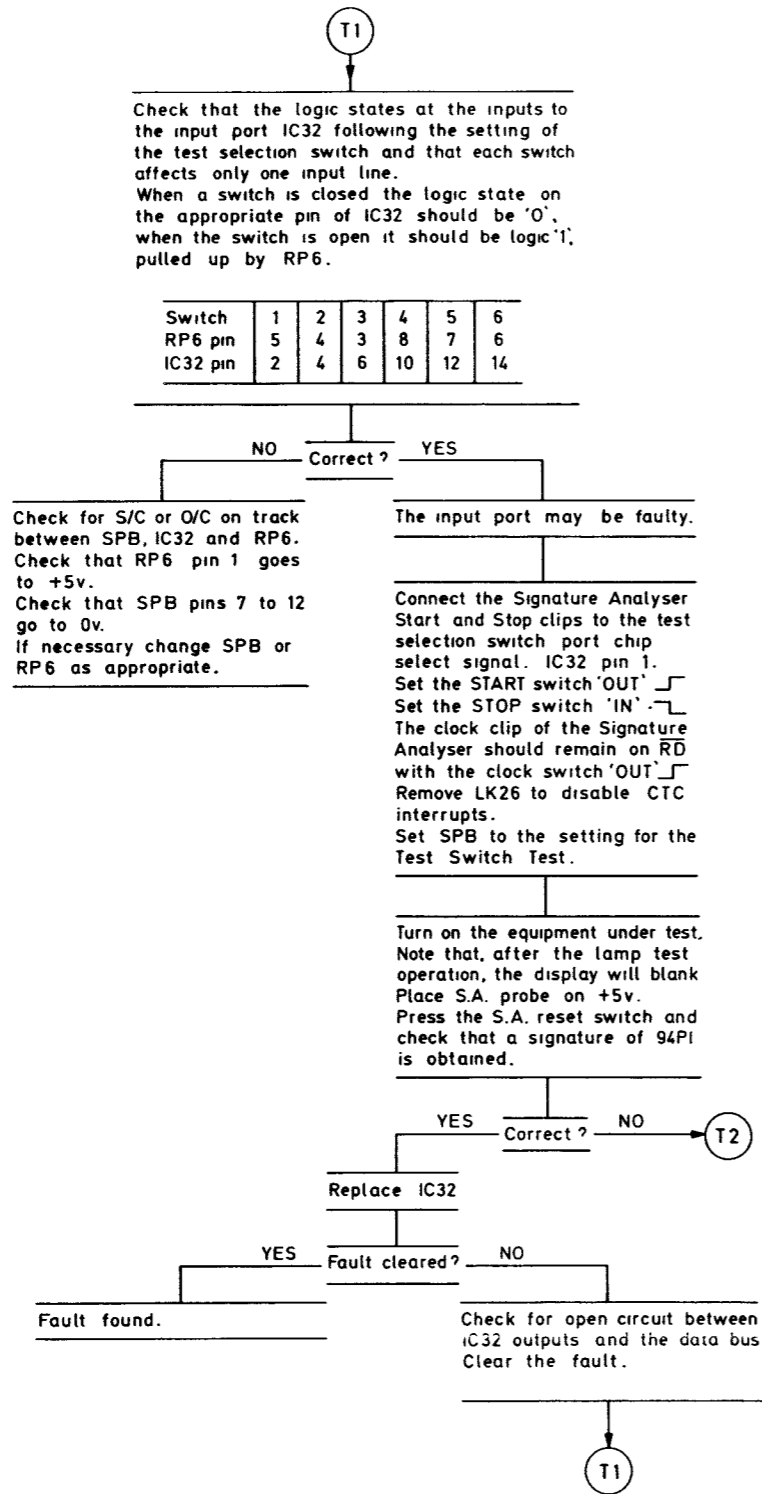
Output port : test flowchart

Fig D3-18

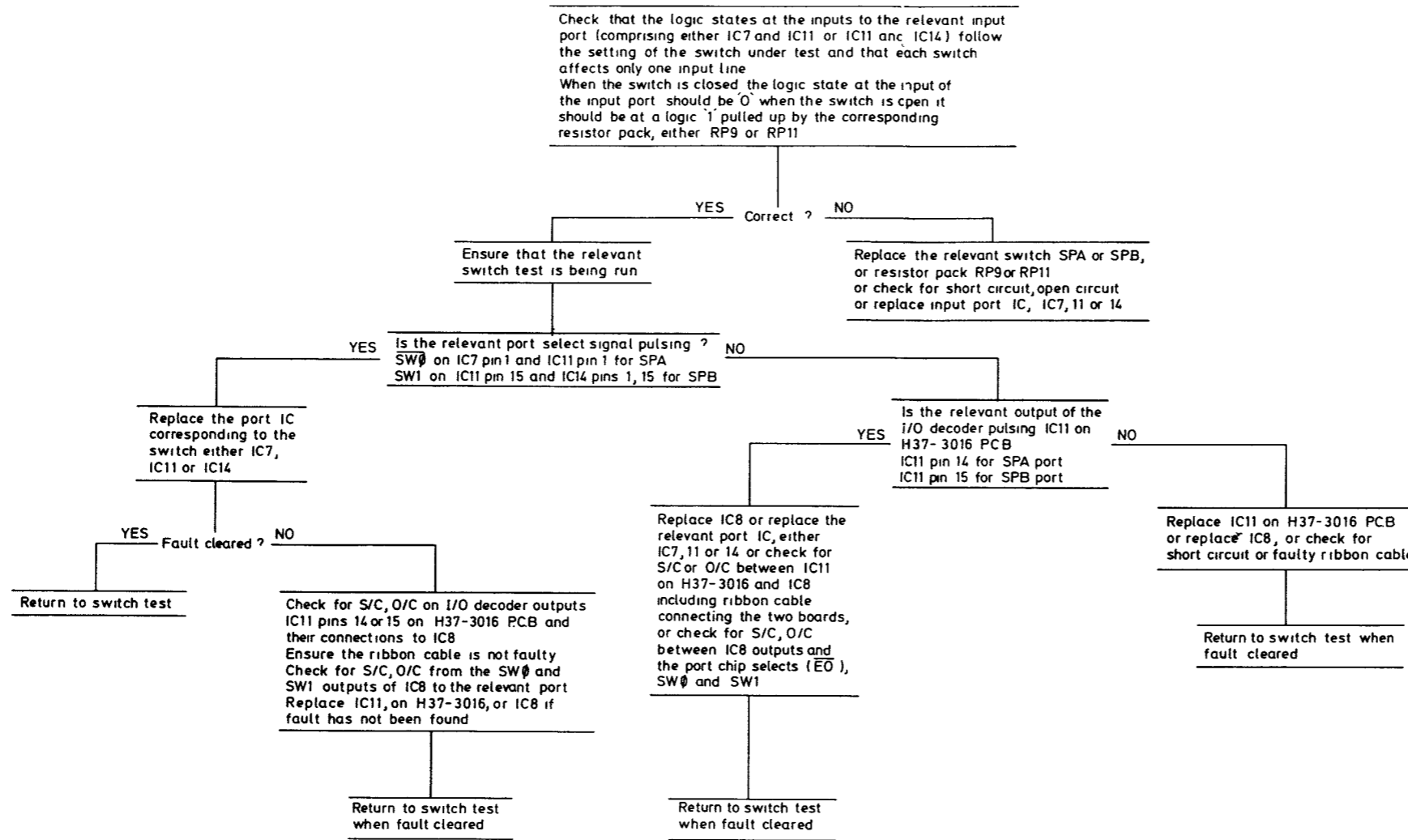
Sub-sect D3

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NOTE All components are on H37-3016 board unless otherwise stated



1 All IC's named are on H37-3015 PCB unless stated otherwise



Sub-section D4MODULE SUPPLIES CONTROL (ML06)5820-99-751-8092

CONTENTS

Para

1	Introduction
	Circuit Description
4	Logic flow
7	Control supplies normal input
8	The filament delay and mains fail override
19	HT step-start delay
23	Blower off override

Fig

Page

D4-1	Module, supplies control 5820-99-751-8092: circuit diagram	5
D4-2	Module, supplies control 5820-99-751-8092: circuit diagram	7

INTRODUCTION

1 The module provides logic control of the sequential switch on and switch off of all power supplies and the forced air cooling blower.

2 In order to obtain high-noise immunity, c-mos digital integrated circuits operating from a +12 V supply are used for signal processing. Status indications are provided by light-emitting diodes.

3 To protect the integrated circuits against damage that may be caused by withdrawing or replacing the module whilst the +12 V supply is on, the inputs from the edge-connector are fed into a 'pull-up' resistor of typically 220 k Ω and a series resistor of typically 10 k Ω . Where very noisy inputs are expected, a 0.1 μ F capacitor is fitted to form an RC network in conjunction with the 10 k Ω resistor. In some cases, additional transient protection is provided by a pair of reverse-biased diodes.

CIRCUIT DESCRIPTIONLogic flow

4 To switch on the amplifier supplies it is necessary to satisfy a series of gates which sequence the amplifier through the 'MAINS ON', 'AVAILABLE', 'AUXILIARIES ON' and 'HT ON' states. These states are controlled by the sequencing switch on the amplifier metering panel. If a failure occurs the associated lamps on the metering panel will light up to the point of failure.

5 The logic gates required to satisfy each step of the sequencing are listed below and also annotated on the circuit diagram. These gates are activated in the order as follows:

- 5.1 Available gate.
- 5.2 Auxiliary start gate.
- 5.3 Filaments, bias and auxiliary supplies start gate.
- 5.4 Auxiliaries complete gate.
- 5.5 HT start gate.
- 5.6 Final stage screen supply start gate.
- 5.7 Auto-tune complete and normal standby gate.

6 The logic levels required to satisfy each gate are annotated on the circuit diagram. Delays are applied in the module. These are described below.

Control supplies normal input

7 On initial switch-on the control supplies normal input to PLA(E) is momentarily applied as a logic 0 to reset other modules for the run-up sequence, and reverts to logic 1 to satisfy the AVAILABLE gate.

The filament delay and mains fail override

8 One of the four inputs required to satisfy the auxiliaries complete gate is delayed to enable the valve filaments to preheat before application of ht. To prevent the delay operating on a short-term mains failure (one-second or less) the filament delay is overridden. Details of the filament delay and mains fail override are given in para 9 to 14 and 15 to 18 respectively. TP3 and TP4 are used for factory tests.

9 Until the filament supply in the amplifier is switched on, PLA(9) is held at logic level 0. The COUNT bistable is set such that IC16c(10) is at logic level 0 and with IC4(11) at logic level 0, all IC4 outputs are also at logic level 0. The FIL. DELAY COMPLETE bistable is set such that PLA(14) is at logic level 1.

10 TR18 is non-conducting and IC2(9) is at logic level 1. IC3 is a free-running clock oscillator with a pulse repetition frequency of 16 Hz.

11 When the filament supply is switched on, PLA(9) goes to logic level 1, activating IC4 which then divides the input from the free-running oscillator IC3. The bistables are unaffected until both inputs of IC16a are at logic level 1. This happens 48 seconds after initiating the count. IC16b and IC16d change state resetting the COUNT bistable such that IC16c(10) switches to logic 1 and IC1b(4) to logic level 0.

12 Approximately two seconds after the COUNT bistable change state IC4(2) switches to logic level 1 causing IC17a to change state. This resets the FIL. DELAY COMPLETE bistable such that PLA(14) switches to logic level 0 lighting DLP7 and providing an input to the AUX. COMPLETE gate.

13 With IC17b(4) at logic level 0, IC14f and IC7f change state to turn on TR18, rapidly charging C7 via R73. IC2(9) changes state to apply logic level 0 to IC16b(6).

14 Unless PLA(9) is reset to logic level 0 the two bistables retain their new states due to logic level 0 at IC14e(12).

15 If a mains failure occurs within the amplifier, C7 will start to discharge via R73 and R72. When the supplies are restored, PLA(9) is momentarily held at logic level 0 and then switched to logic level 1. Therefore the two bistables are set to their original states.

16 If the failure is for less than one second then C7 discharges insufficiently to change IC2(9) from logic level 0. Therefore the COUNT bistable is reset without a count from IC4. Due to the output from IC4(2), two seconds later PLA(14) will switch to logic level 0 creating the conditions as described in para 12. The two second delay is incorporated to allow the amplifier output stage valve to reheat.

17 If the mains failure is for more than one second then C7 will discharge sufficiently for IC2(a) to revert to logic level 1 thus permitting the full filament delay.

18 At switch-off, PLA(9) is switched to logic level 0, resetting the bistables, IC17c(10) changes state to logic level 0 and TR18 turns off discharging C7. Approximately one second later IC2(9) changes state and all circuit elements revert to their original condition.

HT step-start delay

19 The ht step-start delay is incorporated to prevent a current surge in the main ht supply at initial switch-on. A description of the nominal 100 ms delay is given in paras 20 to 22.

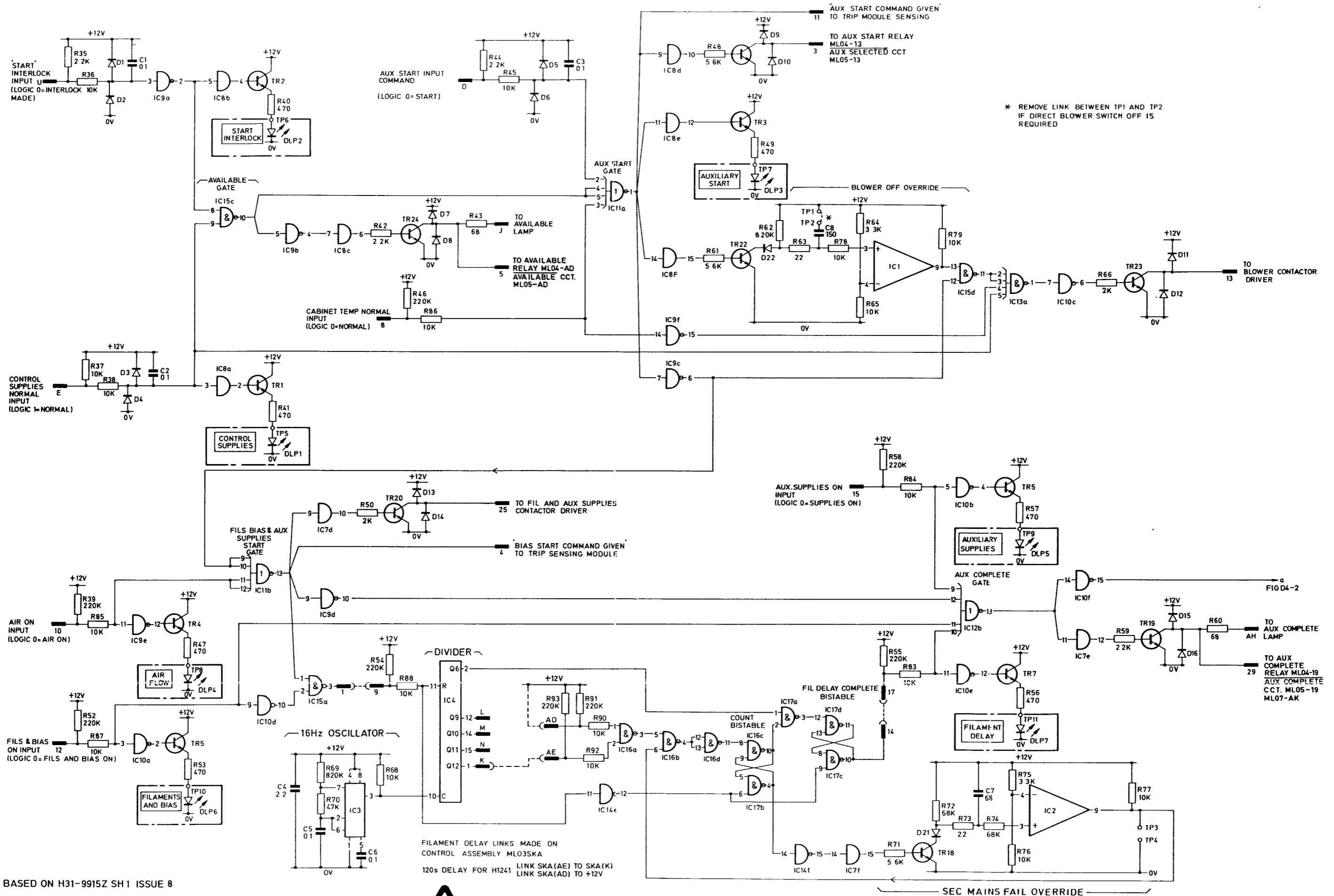
20 When the amplifier main ht contactor is de-energized, PLA(C) is open circuit biasing TR12 on, discharging C15. IC7(7) is at logic level 0, therefore TR25 is turned off.

21 When the amplifier main ht contactor is energized, PLA(c) is at logic level 0, turning TR12 off. C15 charges via R31 and R32. When the voltage across C15 is approximately 6 V, the output of IC7c switches to logic level 1. TR25 turns on, forwarding a logic level 0 to PLA(T). This is used to energize the HT Step-start Contactor. The time taken for C15 to charge to 6 V is nominally 100 ms.

22 At switch off, the amplifier main contactor is de-energized TR12 turns on, rapidly discharging C15 via R32. The output of IC7c reverts to logic level 0 turning off TR25 and de-energizing the amplifier ht step-start contactor.

Blower off override

23 The blower is required to run for 150 seconds after switch-off in order to reduce the temperature within the cabinet, particularly the final stage valve and its filament ring connections. For this TP1 and TP2 are linked, and a 150 μ F capacitor is fitted as C8. The delay will maintain the blower-on command for 150 seconds, the action being similar to the one-second override described in Para 15 to 18. If immediate switch-off is required, TP1 and TP2 are not linked.



BASED ON H31-9915Z SH 1 ISSUE 8

Fig D4-1

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CAUTION:
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Module, supplies control, 5820-99-751-8092 : circuit diagram

Fig D4-1

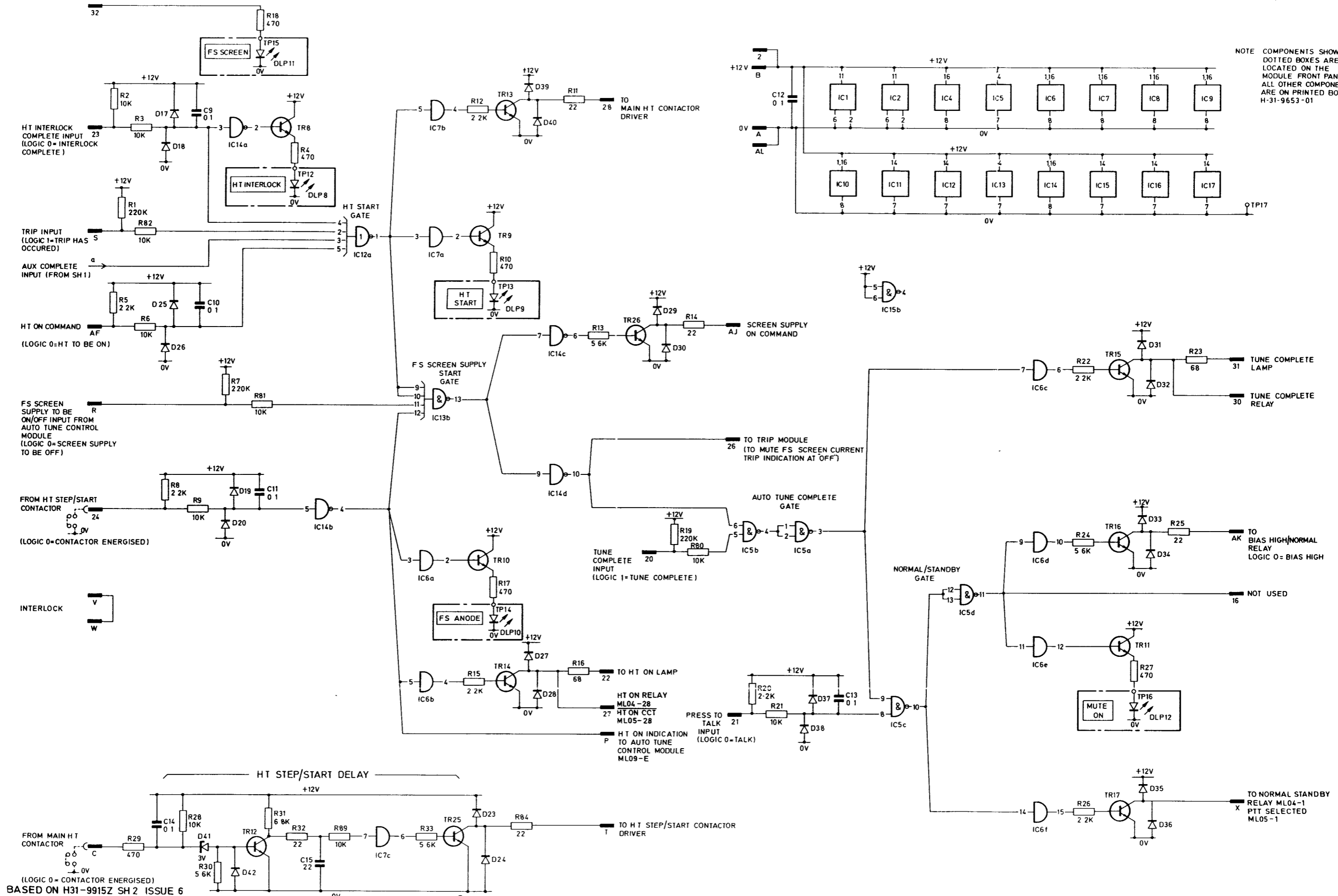


Fig D4-2

CAUTION:
THIS BOARD /UNIT CONTAINS
STATIC SENSITIVE DEVICES



Module, supplies control 5820-99-751-8092: circuit diagram

Sub-sect D5MODULE VSWR AND TEMPERATURE (ML07)5820-99-751-8029

CONTENTS

Para.		
1	Introduction	
3	Description	
4	Smoke detector	
5	VSWR monitoring and trip circuit	
10	Outlet temperature monitoring circuit	
13	Temperature rise monitoring circuit	
18	Contactator control circuit	
Table		Page
1	VSWR voltage and current levels	2
2	Outlet temperature voltage and current levels	4
3	Temperature rise voltage and current levels	4
Fig		Page
D5-1	Module VSWR and temperature: circuit	7
D5-2	Module VSWR and temperature: circuit	9

INTRODUCTION

1 The module forms part of the control circuits for the amplifier. It responds to various monitoring inputs to provide indications and monitor circuits for these inputs. When certain defined parameters are exceeded this module causes trip circuits to operate. A smoke detector alarm circuit is also included together with a contactor control circuit.

2 Control signal processing is by means of c-mos digital integrated circuits. For the supply voltage used logic levels are defined as:

2.1 Logic level 0 = 0 to 3.5V

2.2 Logic level 1 = 8.5 to 12V

DESCRIPTION: Refer to Fig D5-1 and Fig D5-2.

3 For purposes of this description this module can be divided into five separate areas. These areas are:

3.1 Smoke detector circuit

3.2 VSWR monitoring and trip circuit

3.3 Outlet temperature metering circuit

3.4 Temperature difference metering circuit

3.5 Contactor control circuit

Smoke detector

WARNING...

DEPENDENT ON THE LOCAL INSTALLATION OPERATING THE TEST SMOKE ALARM PUSH BUTTON COULD CAUSE THE STATION AUTOMATIC FIRE EXTINGUISHERS TO OPERATE RESULTING IN DRY POWDER OR TOXIC GAS EXTINGUISHERS BEING ACTIVATED.

4 This is a trip circuit based on an F600 probe smoke detector mounted in the amplifier exhaust air duct. In the event of smoke being detected a conducting path is presented across PLA.B and I. This in turn causes TR3 to conduct energizing RLA and lighting the SMOKE ALARM indicator DLP3. Relay contact RLA.1 initiates the external extinguisher circuits, via PLA.5 and E, while RLA.2 is used to initiate an immediate amplifier shutdown via PLA.4 and D and the supplies normal circuit. The TEST SMOKE ALARM push-button SA is protected against accidental operation by a cover. Operating this push-button simulates a smoke alarm, breaking the interlock chain and initiating the external fire alarm circuits.

VSWR monitoring and trip circuit

5 Mathematically dividing integrated circuit IC13 responds to the forward and reverse power analogue inputs supplied to the module on PLA.13 and R respectively. The reverse power input is inverted and applied to a further input to IC7. The output of IC13 is defined as being:

$$10 \frac{(\text{Pin 10 voltage} - \text{Pin 11 voltage})}{(\text{Pin 1 voltage} - \text{Pin 2 voltage})} \text{ Volts}$$

since the input to PLA.13 is proportional to the forward voltage and the input to PLA.R is proportional to the reverse voltage it can be seen that the output on IC13 is equivalent to:

$$10 \frac{(V_f - V_r)}{(V_f + V_r)} \text{ Volts or } \frac{(10)}{(\text{vswr})} \text{ Volts}$$

6 This output is subtracted from a voltage derived from the potential divider R73, R83 by means of IC9b and fed to various vswr circuits, including, two voltage reducing circuits R68, R69 and R71, R72, for the local and remote vswr meter displays. These outputs are taken via filters and fed out on PLA.P, for the local meter panel display, and PLA.12, for the external display. They are suitable for providing a display on 100Ω, 1mA fsd meters. Some typical values of vswr and their associated meter voltage and current levels are shown in Table 1.

TABLE 1 VSWR VOLTAGE AND CURRENT LEVELS

VSWR	Voltage	Current
1.5	.033 Volts	0.33 mA
2.0	.05 Volts	0.5 mA
2.5	.06 Volts	0.6 mA
3.0	.067 Volts	0.67 mA

Note...

Indications of vswr of better than 1.2:1 should be regarded as approximate and for guidance only.

7 The vswr output on IC9.7 is also applied to the vswr alarm control circuits on IC5.3 and IC8.3. Comparator IC5 compares this vswr level with output of potential divider R48, R49 and the front panel VSWR ALARM control RV1. In the event of the vswr level on IC5.3 exceeding the threshold level, set by the potential divider, IC5.7 changes to logic 0. This results in the front panel VSWR ALARM indicator DLP5 being lit and RLB energizing. Relay contacts RLB1 and RLB2 provide an external vswr alarm indication. When the vswr fault is cleared and the voltage on IC5.3 is less than that on IC5.2 the output of IC5.7 reverts to logic 1 extinguishing VSWR ALARM indicator and removing remote vswr alarm indication.

8 Comparator IC8 compares the vswr level on IC9.7 with the output of potential divider R62, R64 and RV6. If the vswr level exceeds this preset level IC8.7 changes to logic 0, resetting the bistable formed by IC12a and b. This results in TR4 conducting, lighting the VSWR REDUCED POWER indicator DLP4, and a logic 1 being fed to the pre-amplifier via PLA.25.

9 When the amplifier is switched off and the vswr fault cleared the bistable is set by the control supplies normal input to PLA.M. This input is held at logic 0 for approximately 50 ms, when the amplifier supplies are restored, resulting in IC11.4 being held at logic 0 for this period. This sets the bistable so that the VSWR REDUCED POWER indication remains extinguished and PLA.25 is held at logic 0. A logic 0 auto-recycle input on PLA.L, from the counter module, will also set this bistable.

Outlet temperature monitoring circuit

10 This circuit uses the voltage sensed by an AD590 temperature sensing device mounted in the outlet air duct of the amplifier. The output of this device is a voltage which varies with temperature. Operational amplifier IC6a adds this voltage level to a reference level of nominally -2.73V set by R34 and RV2. The reference level may be varied by set trip control RV1. Test link LK6 should normally be set to position A. When set to position B it allows the monitor circuit to be tested using the monitor control RV4. Test link LK4 when broken isolates the input to this monitor circuit.

11 The resulting voltage from this summing amplifier on IC6.1 is applied to an inverting amplifier IC6d. Gain control for this stage is provided by RV3. A distribution network connected to the output of this amplifier provides three outlet temperature monitor outputs. Two of these are used to provide a drive for the outlet temperature meters. These meter outputs are taken via limiting resistors R24, R26, R28 and R31 to PLA.18, to provide a remote outlet temperature indication, and PLA.W, for the meter panel outlet temperature indication. The remaining output provides a drive for the outlet temperature trip circuit.

12 The outlet temperature trip circuit IC7 compares the output on IC6.14 with a reference level provided by potential divider R46 and R47. If the outlet temperature rises sufficiently to cause the voltage level on IC6.14 to exceed this reference level then the output on IC7.7 changes to logic 0, resetting the bistable formed by IC3a and b. This results in TR1 conducting, lighting the OUTLET TEMPERATURE indicator DLP1.

13 This bistable is set by the control supplies normal or auto-recycle inputs to IC3.1, see Para 9, when the outlet air temperature has cooled sufficiently to allow IC7.7 to return to logic 1. This results in the OUTLET TEMPERATURE trip being extinguished. Some typical outlet temperature indications and their associated meter voltage and current levels are shown in Table 2.

TABLE 2 OUTLET TEMPERATURE VOLTAGE AND CURRENT LEVELS

Temperature	Voltage	Current
100°C	0.05V	0.5 mA
133°C	0.067V	0.67 mA
166°C	0.083V	0.83 mA
200°C	0.1V	1 mA

14 The logic 0 temperature trip output on IC7.7 is also fed to PLA.AB via IC12c. This output is connected to the trip sensing module providing a logic 1 trip signal when the output air temperature exceeds 95°C, nominal.

Temperature rise monitoring circuit

15 This circuit monitors the difference between the sensed input and output air temperatures to give an indication of the rise in cooling air temperature within the amplifier. A voltage proportional to the temperature rise is applied to operational amplifier IC1 via PLA.T. This amplifier is used in its adder mode producing an output voltage at IC1.8 of 10 mV/°C temperature difference. The resulting voltage is applied to local and remote temperature monitoring outputs via limiting resistors R1 and R2. These outputs are taken via PLA 5, to provide a temperature rise indication on the meter panel, and PLA 14, to provide a remote temperature rise indication. Some typical temperature rise indications and their associated meter voltage and current levels are shown in Table 3.

TABLE 3 TEMPERATURE RISE VOLTAGE AND CURRENT LEVELS

Temperature rise	Voltage	Current
25°C	0.025V	0.25 mA
50°C	0.05V	0.5 mA
70°C	0.075V	0.75 mA
100°C	0.1V	1 mA

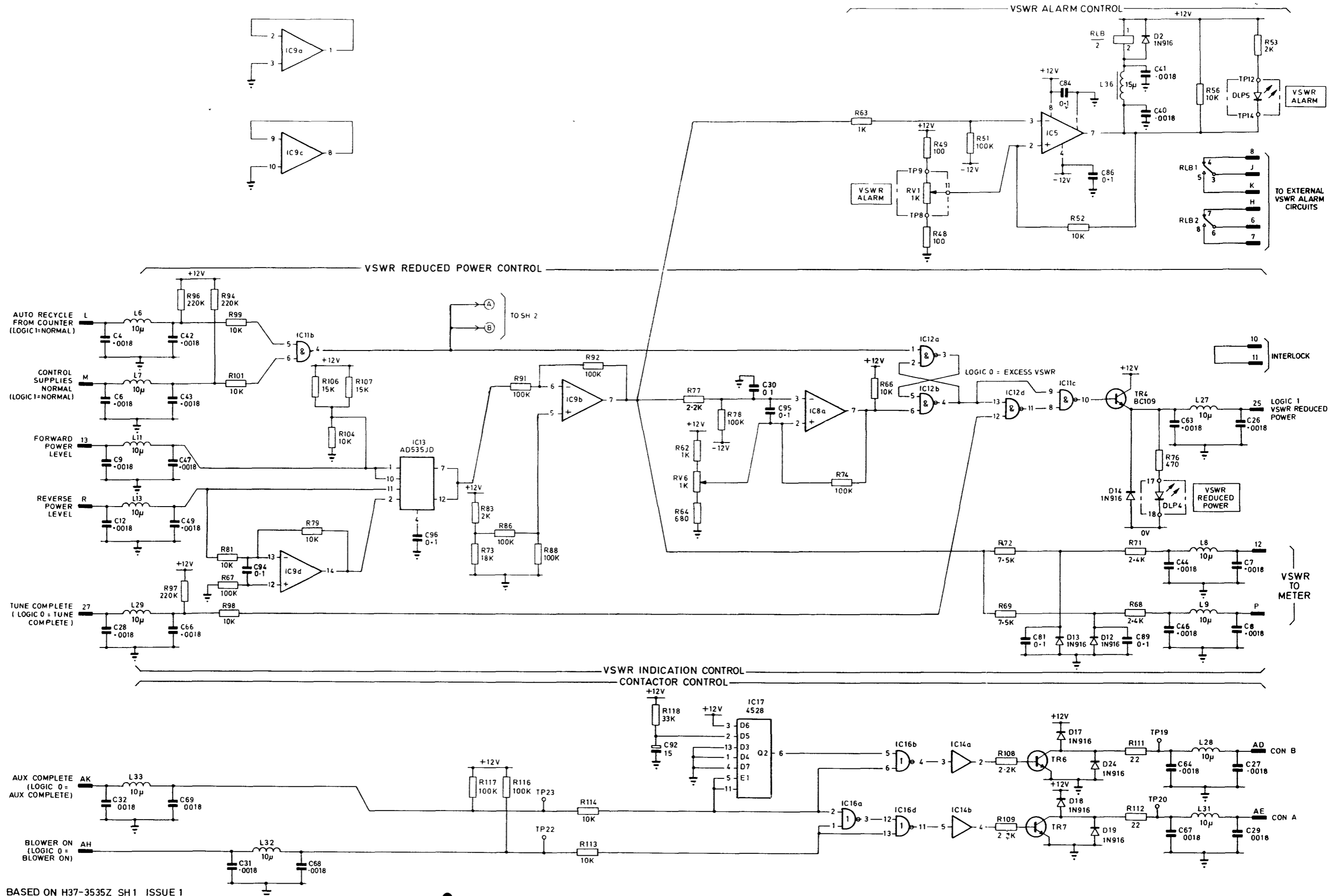
16 The temperature rise output level on IC1.1 is also fed to a comparator IC2, via a potential divider R3 and R4. This comparator compares this temperature rise level with a reference level provided by potential divider R6 and R7. In the event of the temperature rise exceeding 45°C nominal the comparator output on IC2.7 changes to logic 0 resetting the bistable formed by IC3c and d. This results in TR2 conducting, lighting the TEMPERATURE RISE indicator DLP2 and feeding a logic 0 to PLA 15.

17 This bistable is set by the control supplies normal or auto-recycle inputs to IC3.8, see Para 9, providing the temperature rise has returned to less than 45°C. This results in the TEMPERATURE RISE indicator being extinguished and a logic 1 being fed out on PLA 15.

Contactor control circuit

18 This circuit controls two contactors situated in the filament control assembly. These contactors, CON.B and CON.A are switched into circuit by way of two inputs from the supplies control module. Both of these inputs are initially held at logic 1 when the amplifier is switched on. When the cooling air supply and controls supplies are established PLA.AH changes to logic 0 causing IC16.3 to change to logic 0 and IC16.11 to change to logic 1. This results in CON A being energized via TR17 and PLA AF.

19 When the auxiliaries are complete and the AUX COMPLETE lamp lit PLA AK changes to logic 0. This logic 0 is fed to IC17.5 and 11 initiating a nominal 0.5s delay generated by IC7. After this delay IC17.6 changes to logic 1 energizing CON B via TR6 and PLA AD. The logic 0 on PLA.AK is also applied to IC16.2 causing IC16.11 to change to logic 0 resulting in CON.A de-energizing via TR7 and PLA AE.



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Fig D5-1

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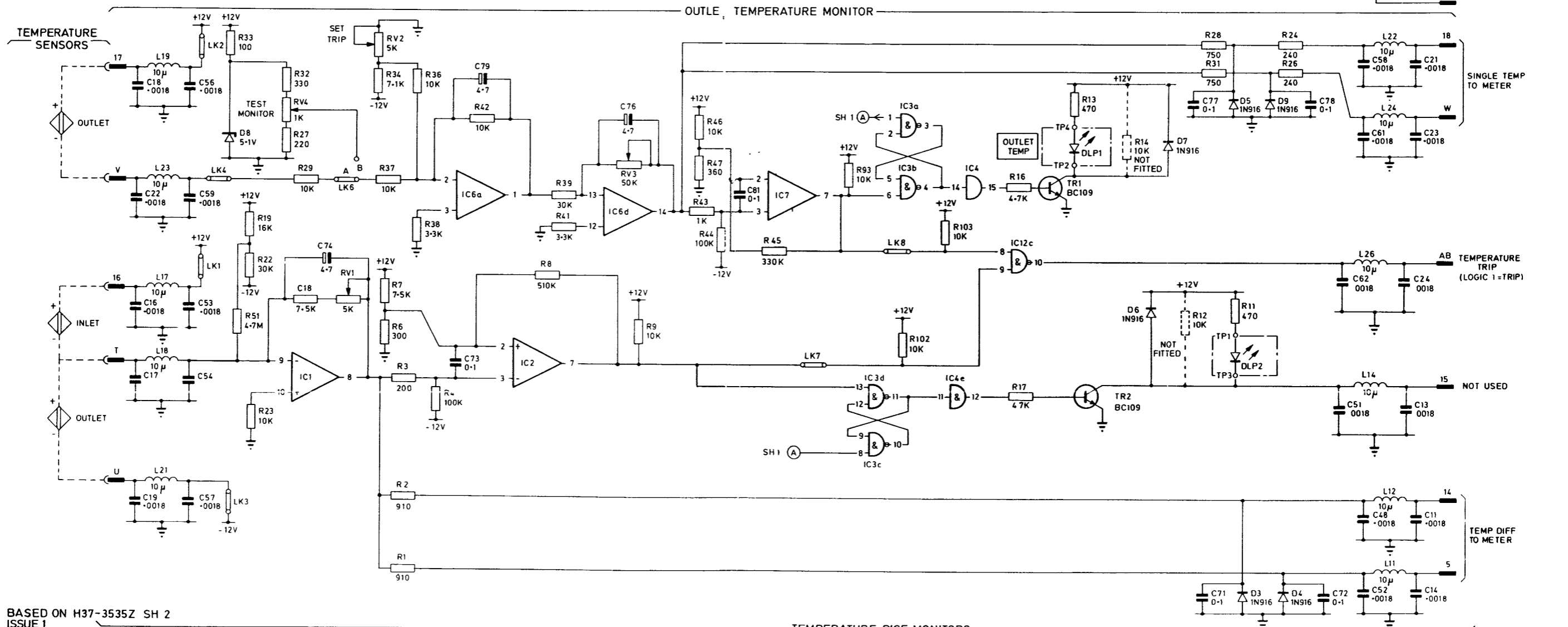
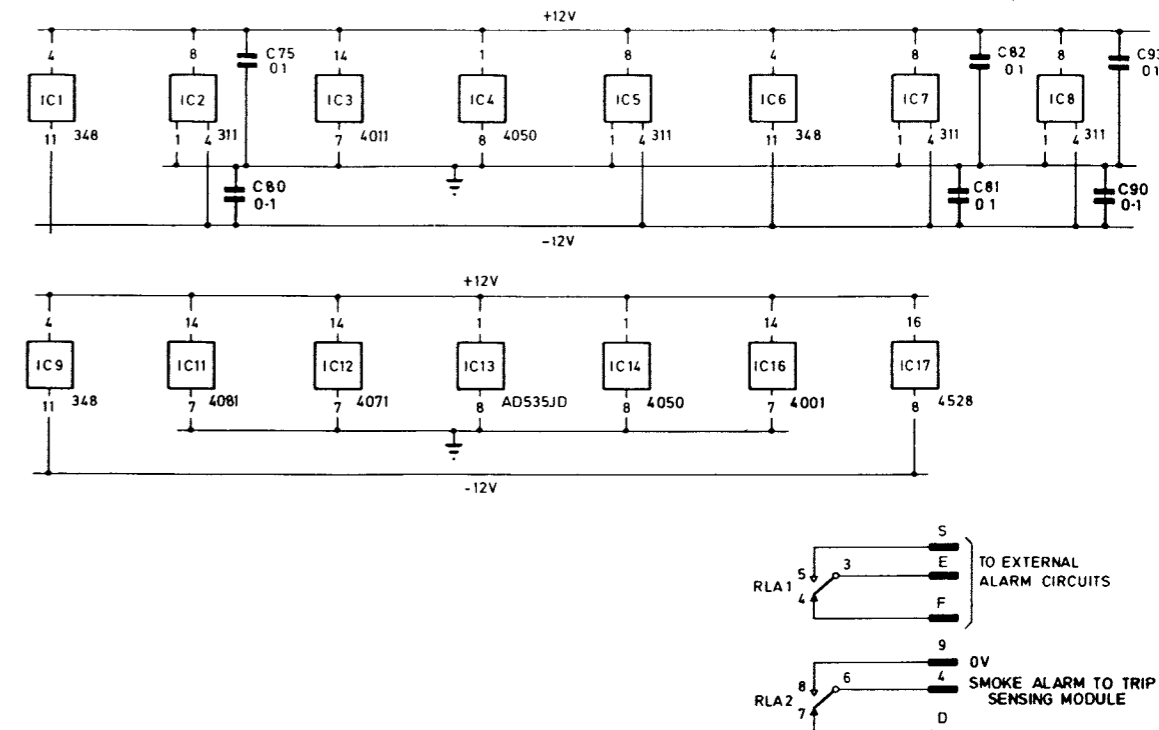
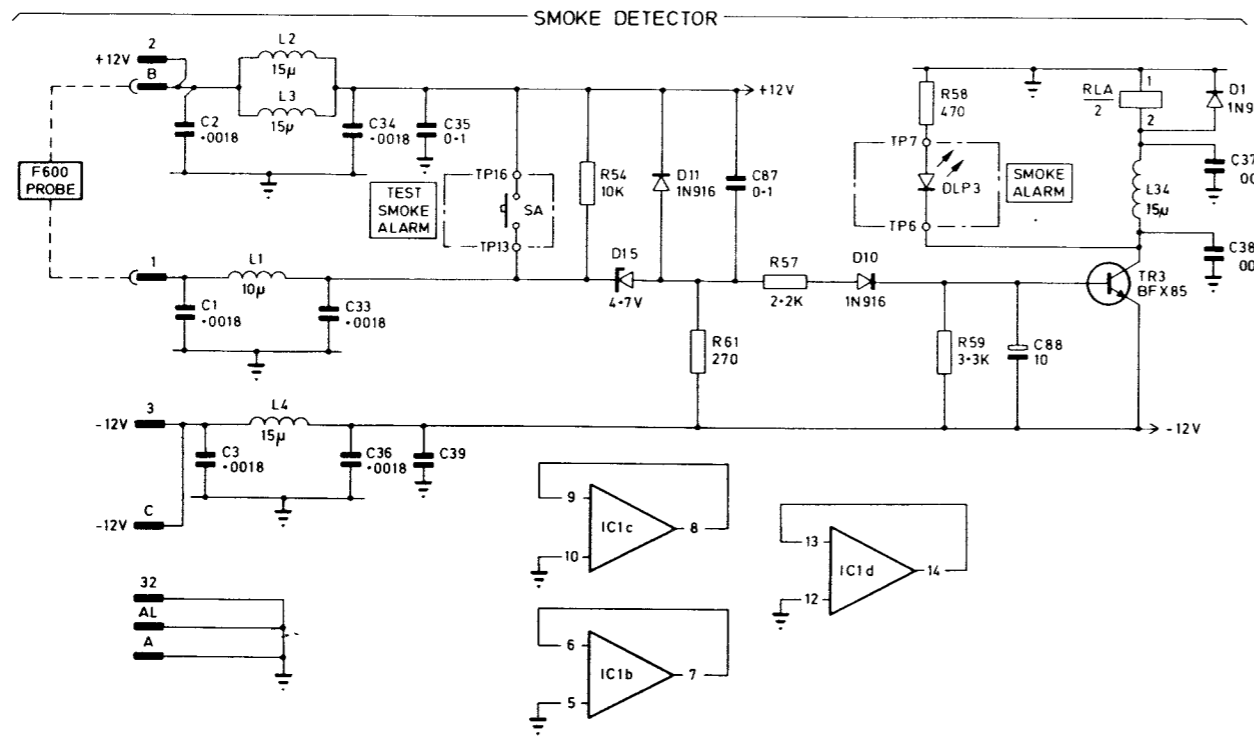


Module, vswr and temperature 5820-99-751-8029 : circuit diagram

Fig D5-1

Sub-sect D5

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ISSUE 1

Fig D5-2

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Module, vswr and temperature, 5820-99-751-8029 : circuit diagram

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Fig D5-2

Sub-sect D5
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Sub-section D6MODULE TRIP SENSING (MLO8)5820-99-760-2963

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INTRODUCTION

1 The trip sensing module monitors eight trip parameters within the amplifier which are as follows:

- 1.1 Cabinet temperature
- 1.2 Air flow
- 1.3 Bias on
- 1.4 Auxiliary supplies on
- 1.5 HT current
- 1.6 Final stage screen current
- 1.7 Final stage cathode current
- 1.8 Reverse power.

2 In the event of a trip condition being sensed the module generates a command to turn off the ht power supply. A three-shot restoration and lockout circuit is incorporated to attempt to restore the supplies to normal two seconds after the trip is sensed. Three such attempts are made before a lockout condition is met whereby the ht supply remains off until the condition is reset manually. In the event of a high cabinet temperature trip being sensed the module generates a command to turn off all aux. and ht and blower supplies and a lockout condition is created directly by bypassing the three-shot circuit. Red light-emitting diodes on the module front panel indicate the sensed trip and remain lit until extinguished manually.

3 An option is provided where, by fitting the appropriate link, as shown on fig D6-2, the ht supplies trip can be used to operate the lockout circuit with only a single shot.

4 In addition to the trip sensing and lockout circuitry the module contains meter amplifiers which are incorporated to monitor the forward and reverse rf power levels in the output feeder of the amplifier. These are switched to read p.e.p. upon completion of the amplifier tuning sequence.

5 In order to obtain high-noise immunity, c-mos digital integrated circuits operating from a +12 V supply are used for signal processing. To protect the integrated circuits against damage that may be caused by withdrawing or replacing the module whilst the +12 V supply is on, the inputs from the edge-connector are fed into a 'pull-up' resistor of typically 220 k Ω and a series resistor of typically 10 k Ω . Where very noisy inputs are expected, a 0.1 μ F capacitor is fitted to form a RC network in conjunction with the 10 k Ω resistor. In some cases, additional transient protection is provided by a pair of reverse biased diodes.

CIRCUIT DESCRIPTION

Control supplies normal input

6 When the amplifier isolator switch is first closed to connect the mains supply, PLA(R) on the trip sensing module is momentarily held at logic level 0. The purpose of this is to reset the various bistables within the module to clear any previous trip indications or lockout condition. After the delay, PLA(R) switches to logic level 1 indicating that the control supplies are normal. This delayed input is also used in other modules to ensure that the control circuits are correctly sequenced at switch-on.

Cabinet temperature trip

7 A thermostat in the amplifier exhaust chimney normally connects PLA(E) to 0V. IC1a(11) and IC12a(3) are therefore at logic level 0. If the chimney temperature exceeds 130 °C then the thermostat will open changing the state of the CAB. TEMP. TRIP SENSED bistable, IC1d and b. PLA(d) switches to logic level 1. This is used as a HIGH CAB. TEMP. command to the supplies control module, turning off the ht aux supplies and blower.

8 IC1c(10) switches to logic level 0 giving the following conditions:

- 8.1 An input at 'a' to the TRIP SENSED gate IC27 (described in para 24).
- 8.2 An input to direct lockout gate at IC17d(12) which, together with logic level 1 from the TRIP SENSED bistable, causes the LOCKOUT ACHIEVED bistable to change state, initiating a LOCKOUT condition (refer to para 28).

- 8.3 Resetting the bistable formed by IC12a and b. IC12a(3) changes to logic level 1 lighting the CABINET TEMP. led.

9 The circuits will remain in this condition until the thermostat recloses and a LOCKOUT RESET command is given at PLA(W) resetting the bistable formed by IC1d and b. The trip indicator remains lit until the INDICATOR RESET switch SA is operated, resetting the bistable formed by IC12a and b.

Air fail trip

10 When the amplifier sequencing switch is set to AVAILABLE logic level 0 is present at PLA(10). This sets the bistable formed by IC9a and b such that IC9b(4) is at logic level 1. A switch located in the exhaust duct of the amplifier is connected to PLA(P) and remains open until sufficient air flow is detected. Thus, initially, PLA(9) is at logic level 1 indicating to the supplies control module that no air is flowing and supplies should be off. IC9d(12) is at logic level 0 therefore IC9d(11) is at logic level 1. The bistable formed by IC12d and c is set such that IC12d(11) is at logic level 0.

11 When the amplifier sequencing switch is set to AUX.ON then PLA(10) changes to logic level 1 but the circuit elements do not change state. When the air flow has built up sufficiently the air switch will close connecting logic level 0 to PLA(P). Logic level 0 at PLA(9) indicates to the supplies control module that the power supplies can be switched on and at IC9a(1), sets the bistable such that IC9b(4) is at logic level 0. IC9d(12) is a logic level 1 and IC9d(13) is at logic level 0 therefore IC9d(11) must remain at logic level 1.

12 If there is no subsequent fail in airflow then the circuit remains in this condition until the AVAILABLE condition is selected at the amplifier sequencing switch. PLA(10) changes back to logic level 0 causing IC9d(12) to change to logic level 1. IC9b(4) is forced to logic level 1 despite IC9a not being reset. As the blower speed falls so the switch opens, the circuits then reverting to conditions described in para 10. As IC9d(11) has remained at logic level 1 throughout, no 'Air Fail' indication is given.

13 Now consider the condition as described in para 11 but where the air flow fails subsequent to the air flow switch closing. PLA(P) and PLA(9) change to logic level 1 commanding the supplies control module to turn off the power supplies. Both inputs of IC9d are at logic level 1 so that the output changes to logic level 0, giving an input at 'b' to the TRIP SENSED gate, IC27 (described in para 24) and setting the bistable by IC12d and c. IC12d(11) changes to logic level 1 lighting the AIR FAIL l.e.d. If the air flow remains low, the circuits will remain in this state eventually achieving a LOCKOUT condition (described in para 28). If the air flow recovers then PLA(P) and PLA(9) switch to logic level 0, removing the input to the trip sensed gate. However, the bistable formed by IC12d and c does not change state and so the trip indicator remains lit until reset by operating the INDICATOR RESET switch SA.

Bias fail trip

14 IC3 is a differential level detector whereby IC3(9) is at logic level 1 until such time as the amplifier bias supply voltage exceeds a proven level preset in the amplifier pen. stage. The action of the remainder of the circuit is similar to the 'Air Fail' trip described in paras 10 to 13.

HT supplies trip

15 PLA(4) and (5) are fed from the HT trip PEC in the amplifier cabinet which senses the primary and tertiary currents of the main ht transformer and detects whether the ht step-start circuit has functioned correctly.

16 IC4 is a differential level detector whereby IC4(9) is at logic level 1 in a non-trip condition. If a trip condition is sensed. IC4(9) switches to logic level 0 giving the following conditions:

- 16.1 An input at 'd' to the TRIP SENSED gate IC27 (described in para 24)
- 16.2 An input to the direct lockout gate at IC17d(13) if the appropriate link is made on the printed circuit board. This is an optional facility enabling a lockout condition to be met directly by bypassing the three-shot circuit (refer to para 23).
- 16.3 Resetting the bistable formed by IC13d and c. IC13d(11) changes to logic level 1 lighting the HT SUPPLIES l.e.d.

17 With the ht supplies off, IC4(9) reverts to logic level 1. The trip indicator remains lit until the associated bistable is reset by operating the INDICATOR RESET switch SA.

FS screen current trip

18 IC5 is a differential level detector whereby IC5(9) is at logic level 1 if the amplifier final-stage screen current exceeds a proven level preset in the amplifier final stage. The action of this circuit is similar to that of the 'ht supplies' trip circuit except for the inhibit input at PLA(J).

19 When the ht supplies are switched off, the main ht voltage can sometimes decay faster than the screen supply voltage causing a rise in screen current to a point where a trip could occur. To prevent spurious trip indications an input at PLA(J) from the supplies control module, indicating that a screen supply on command has been given, ensures that IC10d(11) remains at logic level 1.

FS cathode current trip

20 The action of this circuit is similar to that of the 'ht supplies' trip circuit.

Aux. supplies trip

21 The action of this circuit is similar to that of the 'Bias Fail' trip circuit.

Reverse rf power trip

22 The action of this circuit is similar to that of the 'ht supplies' trip circuit. The differential level detector, IC32, receives its input from the reverse power meter amplifier circuit (described in para 33).

Three shot and lockout circuit

23 In the condition where no trips are sensed and where any previous lockout condition or trip indications have been reset, the TRIP SENSED and LOCKOUT ACHIEVED bistables are set such that IC18a(3) and IC16f(10) are at logic level 0. Also, the trip-sensed lockout output to the supplies control module at PLA(17) is at logic level 0.

24 All eight trip circuits are fed to the TRIP SENSED gate, the output of which, at IC27(14), switches to logic level 0 when any one or more trips occur.

25 When a trip occurs the TRIP SENSED bistable is set such that IC18a(3) switches to logic level 1, resulting in PLA(17) switching to logic level 1, inhibiting the ht start gate in the supplies control module.

26 With IC18a(3) at logic level 1, IC18d(11) changes to logic level 0, removing the reset input from divider IC20. IC19b is programmed by IC20 such that approximately two seconds later IC19b(4) switches momentarily to logic level 0. This gives the counter formed by IC23 and IC17 one count pulse and also attempts to reset the TRIP SENSED bistable via IC19a and IC18c. If, in the time delay, the TRIP SENSED gate is in a non-trip condition, then the bistable resets and PLA(17) reverts to logic level 0 permitting the ht supply to come on again.

27 An additional function of the output of IC19a is to reset counter IC21. IC19d is programmed by IC21 such that IC19d(11) momentarily switches to logic level 0 every 62 seconds, resetting the three-shot counter via IC19c.

28 If a further trip is sensed before IC21 completes the 62 second count, then the TRIP SENSED bistable set again such that IC18a(3) is at logic level 1. IC20 produces a pulse after two seconds to reset the bistable, reset counter IC21 and to give a second count pulse to the three-shot counter IC23. The action continues until the three-shot counter IC23 has received three count pulses, causing IC17a(2) to switch to logic level 1. Thus when the next trip is sensed, IC17a(3) switches to logic level 0 setting the LOCKOUT ACHIEVED such that the IC16c(10) changes to logic level 1. Thus PLA(17) will remain at logic level 1, indicating a lockout condition.

29 To reset the lockout condition after the trip has been cleared, PLA(W) is switched momentarily to logic level 1 by an external reset switch. This resets the bistables and restores the circuits to their original states.

30 If one or two shots have taken place without lockout being actioned, then 62 seconds after the last reset pulse from IC19a(3), IC21 produces a reset pulse via IC19d and c, resetting the three-shot counter IC23.

External trip indication

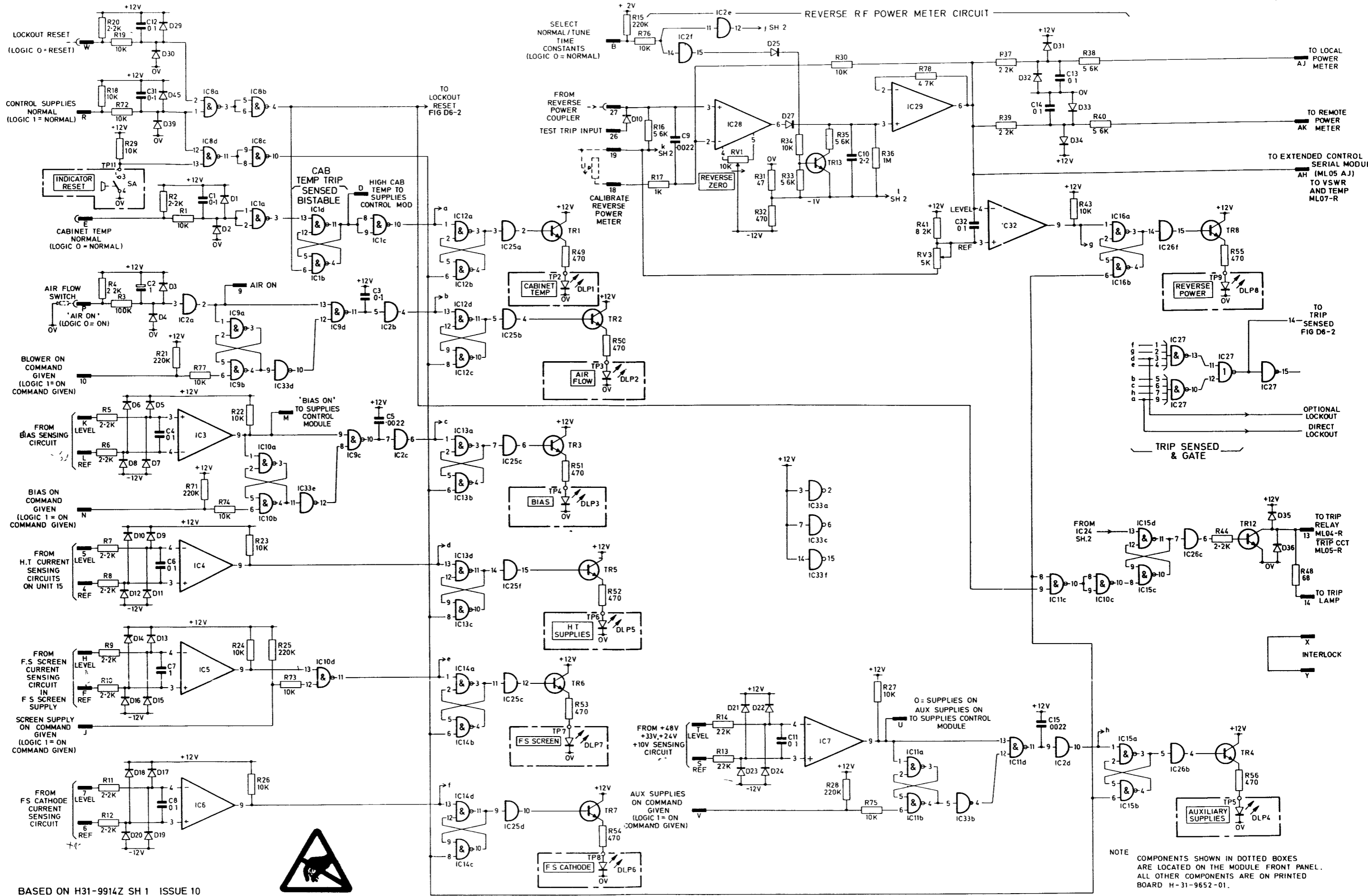
31 The output of the TRIP SENSED gate is also routed to the bistable formed by IC15d and IC15c. When a trip occurs the bistable is set such that IC15d(11) is at logic level 1, turning on TR12. PLA(13) and (14) switch to logic level 0, enabling external indications of a trip condition to be made. The indications may be cleared by operating either the INDICATOR RESET switch SA or the external lockout reset switch.

Forward RF power meter amplifier

32 When the amplifier is in the 'Tune Complete' condition PLA(B) is taken to logic level 0. This causes TR11 to be non-conducting. A directional coupler in the amplifier rf output assembly monitors forward rf power and feeds a low level dc signal to PLA(31) proportional to the power. The dc signal is amplified by IC30 such that C20 charges rapidly via D28. If the input level falls then D28 becomes reverse biased resulting in C20 slowly discharging via R66. IC31 is a voltage follower and drives the local and remote rf power meters. Feedback via R62 is taken from the outputs of IC31 and applied to the inverting input of IC30. The gain is determined by a variable resistor situated in the calibration unit and is connected to PLA(30).

Reverse RF power meter amplifier

33 This circuit is similar to that of the forward rf power meter amplifier. An additional output is fed to a differential level detector, IC32, in order to provide a reverse power trip sensor (refer to para 22). RV3 allows the reverse power trip level to be set up.



NOTE
COMPONENTS SHOWN IN DOTTED BOXES
ARE LOCATED ON THE MODULE FRONT PANEL.
ALL OTHER COMPONENTS ARE ON PRINTED
BOARD H-31-9652-01.

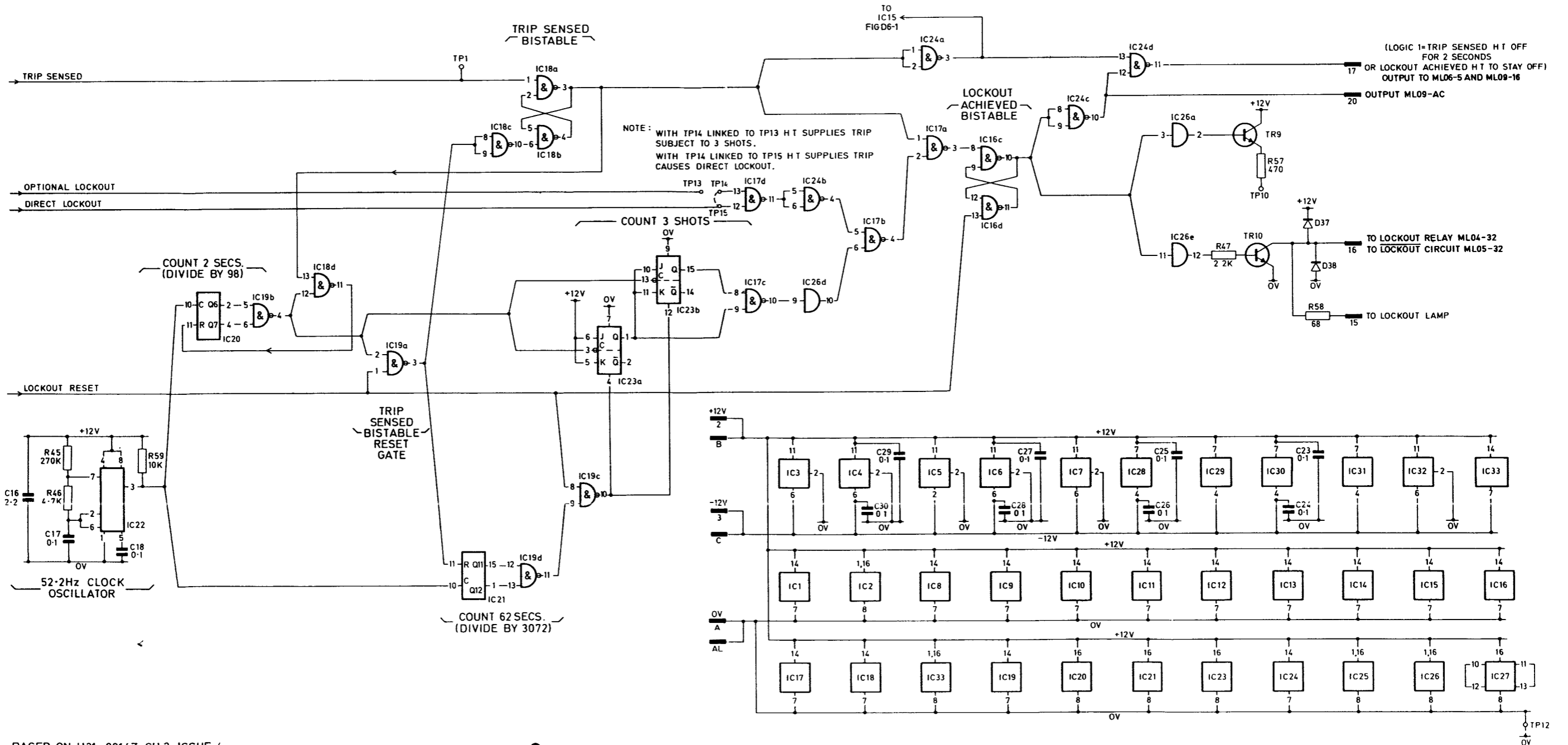
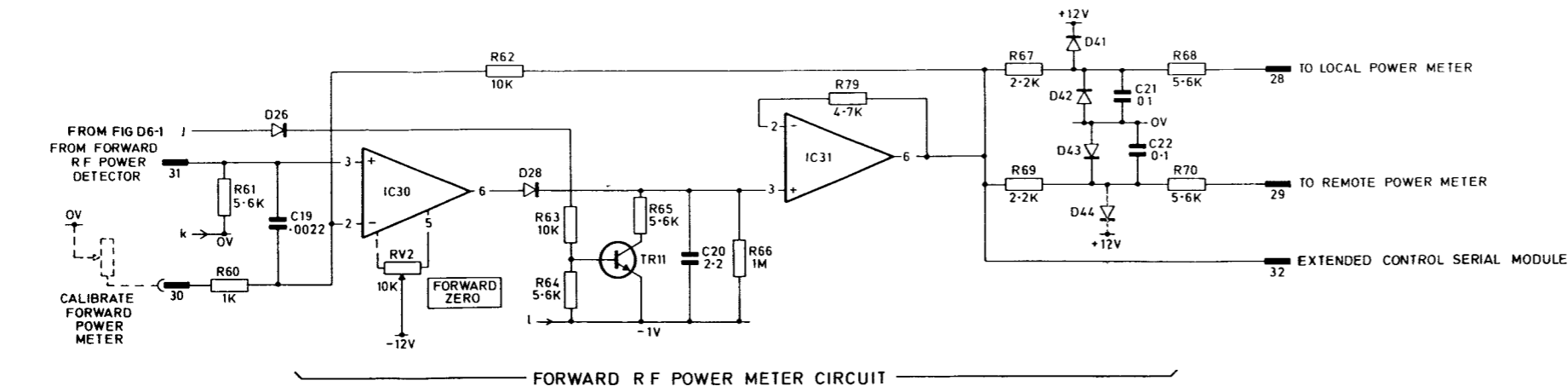
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Fig D6-1

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Module, trip sensing, 5820-99-760-2963 : circuit diagram

Fig D6-1



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Fig D6-2

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Module, trip sensing, 5820-99-760-2963 : circuit diagram

Fig D6-2

Sub-sect D6

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Sub-sect D7MODULE AUTO-TUNE CONTROL (ML09)5820-99-751-8027

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8	Pen. tune
9	F.S. tune
11	Set output level
12	Tune complete
16	HT on/off switching
18	HT trip before auto-tune complete
20	HT trip after auto-tune complete
22	Function switch SA
25	Metering the auxiliary supplies

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INTRODUCTION

1 The module provides for control of the automatic tuning sequence and interlocks the supplies to ensure that a safe condition is always present. Status indications of the tuning sequence are provided by light-emitting diodes. The supplies associated with the servo-motors and range solenoids are monitored by a switched meter on the front of the module.

2 In order to obtain high noise immunity, c-mos digital integrated circuits operating from a +12V supply are used for signal processing. To protect the integrated circuits against damage that may be caused by withdrawing or replacing the module whilst the +12V supply is on, the inputs from the edge-connector are fed into a 'pull-up' resistor of typically 100 k Ω and a series resistor of typically 10 k Ω .

CIRCUIT DESCRIPTIONGeneral

3 Refer to Fig D7-1 and D7-2. The auto-tune sequence progresses through coarse tune, penultimate stage tune (pen. tune), final stage tune (fs tune), set output level and tune complete. To enable the amplifier to progress through the auto-tune sequence, switch SA on the front of the auto-tune control module is set to 'NORMAL'. Any one of the conditions listed in Para 4 will initiate the selection of coarse tune, the first step in the auto-tune sequence.

Coarse tune

4 The selection of the coarse tune condition is initiated by any of the inputs applied to the 'select coarse tune' gate as follows:

- 4.1 HT/Aerial Interlock (open circuit) at PLA.3
- 4.2 'Slow' drive interlock (open circuit) at PLA.P.
- 4.3 'HT on' (absent) at PLA.E.
- 4.4 'Fast drive' interlock (open circuit) at PLA.R.
- 4.5 Lockout (achieved) at PLA.AC.
- 4.6 Switching from a manual condition to an automatic condition on SA.
- 4.7 Initiate retune by switch SC.
- 4.8 Setting SA to 'COARSE TUNE'.

Note...

The input at 4.2 or 4.4 is dependent on type of drive in service. Refer to note on circuit diagram (Fig D7-1) for linking arrangements.

5 If any one of the inputs to the 'select coarse tune' gate is activated IC6.13 changes to logic 0 causing the coarse tune bistable IC34c and d to change to logic 1 at IC34.11. This in turn generates a set of conditions as follows:

- 5.1 PLA.22 to assume logic level 0 to tell the other auto tune modules that coarse tune has been selected.
- 5.2 The rf attenuator module will switch such that the binary coded ladder attenuator takes up the 'pre-entry' set value of 6 dB.
- 5.3 The signal at PLA.N ensures that the 10 dB tune attenuator is activated if the drive has a 0 dB tune level.

Note...

The attenuator stays in this state until the counter module has measured the selected frequency. Thereafter it is controlled by a dc signal derived from the pre-amplifier until the 'set output level' condition is reached. After this stage it is controlled by the rf coupler dc output.

- 5.4 The servo modules will switch such that the motors are controlled by an error signal derived from comparing a voltage from a shaft encoder potentiometer to a voltage from the counter module. As, at this time, the counter module has not measured the selected frequency, the servo motors are prevented from moving by an inhibiting signal from PLA 19, 21, 23 and Y on the auto-tune module. This signal is derived by sensing the state of the 'frequency count complete' bistable.
- 5.5 The COARSE TUNE light emitting diode to light.
- 5.6 The final stage screen supply to be switched off during COARSE TUNE by a signal fed from PLA.31. This supply is then switched on after the 'coarse tune' sequence has been completed, in order to prevent "auto tune fail" at FS TUNE.
- 5.7 The final stage bias to be set to maximum, and the pre-amplifier to be muted by a signal from PLA 4. The bias and pre-amplifier stay in this condition until coarse tune is complete.

- 5.8 The forward and reverse power meters to be switched to a fast time constant by the signal fed from PLA.U. This signal also causes the 'tune complete' lamp on the meter panel to extinguish and the tune complete relay in the extended control module to change state. PLA.U remains at logic level 1 until 'tune complete' is achieved.
- 5.9 The 'pen. tune' bistable, and subsequent bistables to be set.
- 5.10 The 'frequency count complete' bistable to be set by the action of IC8 and C9 such that IC4.11 changes to logic level 0. The output from IC4.11 is routed to the 'coarse tune complete' gate IC26 via IC23b to indicate that one of the conditions for completion has not been satisfied. It is also fed to IC8a which in turn ensures the servo motors are not free to run.
- 5.11 IC4b to be fed a pulse from C9 to ensure TR4 stays on long enough to fully discharge C4.
- 5.12 Relay RLG in the extended control module is energized to hold the drive in the tune condition.
- 5.13 With IC6.13 at logic level 0. TR4 is turned on to rapidly discharge C4 via R21. IC21.2 changes to logic level 1 causing C3 to rapidly discharge via R14 and D3. This primes the integrator and pulse generator circuits which command the frequency counter to measure the frequency again. The 'auto tune fail' timer is also primed via IC8a to produce a logic level input to IC26.5 via IC23b. This prevents the 'coarse tune complete gate' becoming satisfied until a logic 1 frequency count signal is fed out on PLA.11.
- 5.14 When all interlocks are complete to the select coarse tune gate IC6b, IC6.13 will change to logic 1. TR4 switches off and C4 charges through a long time constant R24 and R26. If all interlocks remain intact, then 200 ms later IC21.7 changes to logic level 0. Capacitor C3 charges via R14 such that PLA.11 changes to logic level 1 for 1 ms then reverts to logic level 0. The signal from PLA.11 tells the frequency counter module to measure the incoming frequency. The integrator circuit is included to ensure that 'switch bounce' and the frequency synthesizer setting times do not result in an incorrect count.
- 5.15 Once the frequency counter starts to measure the drive frequency a logic level 0 is fed to PLA.A. This presents an input to IC26 to indicate that one of the conditions for 'coarse tune complete' has not been satisfied. The 'frequency count complete' bistable is reset, but IC4.3 remains at logic 1 due to the input being fed to IC4.1.
- 5.16 When the frequency count is complete, PLA.X is switched to logic level. The inhibiting input to IC26 is removed. IC4.3 changes to logic 0 and the servo motors are now free to run and the range selection circuit able to comply with the ranging information available from the counter module. PLA.18 will change to logic level 0 as soon as the pen. servo motor has set up the pen. stage capacitors to their coarse tune position. Provided no end stop condition is reached PLA.17 will remain at logic 0, IC14.11 will change to logic level 1 and remove one of the inhibiting inputs to IC26. Similar action takes place for both of the final stage tune and load capacitor servo systems. Diode D22 cathode is at logic level 1 until such time an 'auto tune fail' condition is detected and thus presents no inhibiting action to IC26. The penultimate stage range selection is by means of a motorized switch (Ledex). Whilst this is turning PLA.Z is held at logic level 0 to present an inhibiting input to IC26. The final stage range selection is by means of solenoid-operated shorting bars on the coil assemblies. Until the appropriate solenoids have been energized or de-energized as required. PLA.20 is held at logic level 0 to present an inhibiting input to IC26.

6 Thus, for the 'coarse tune complete' gate to be satisfied, the following events must have been achieved within the amplifier.

- 6.1 Frequency count complete.
- 6.2 Penultimate stage capacitors in coarse tune position and no end stop reached.
- 6.3 Final stage tune capacitors in coarse tune position and no end stop reached.
- 6.4 Final stage load 1 and 2 capacitors in coarse tune position and no end stop reached.
- 6.5 Penultimate stage range selection complete.
- 6.6 Final stage range selection complete.

7 When the 'coarse tune complete' gate is satisfied IC26.15 changes to logic level 0 and the 'coarse tune' bistable is reset such that IC16.11 changes to logic 0. A delay circuit C23, R81 and D41 provides a 70 ms delay between IC31.8 changing to logic 1 and IC31.12 changing to logic 0. This delay is to overcome any transient conditions brought about by circuit switching and the overshoot of the servo system. PLA.22 changes to logic 1 to indicate completion of the coarse tune sequence and the COARSE TUNE light-emitting diode will extinguish.

Pen. tune

8 The PEN TUNE light-emitting diode lights to indicate the start of the pen. tune sequence. The final stage tune and load capacitor servo motors are still prevented from running by PLA.21 and Y being held at logic 1. The pen. stage motor is free to run by PLA.19 changing to logic 0. With PLA.22 now at logic 1, the pen. servo module switches such that the motor is now controlled by the pen. stage discriminator. The final stage motors also switch to the final stage discriminator but at this point in the sequence remain inactive. PLA.4 changes to logic 1, removing the mute from the preamplifier and switching the final stage bias back to normal. The pen. stage motor runs until no tune error is sensed. PLA.18 changes to logic 0, provided no end stop has been reached. PLA.17 remains at logic 0. Thus there are no inhibiting inputs fed to IC23c and the pen. tune is complete. The 'pen. tune' bistable is reset such that IC16.3 changes to logic 0. The PEN TUNE light emitting diode will extinguish.

FS tune

9 The FS TUNE light-emitting diode lights to indicate the start of the final stage tune sequence. The final stage screen supply is switched on by PLA.31 changing to logic 1. The fs tune servo motor is freed to run by PLA.21 changing to logic 0. The fs load servo motors are freed to run by PLA.23 and 4 changing to logic 0 provided no large error is sensed as indicated by the logic state of PLA.AB.

10 The final stage tune and load motors run until no errors are present as seen by the tune and load discriminators. The penultimate stage tune motor remains free to run. Once all four motors have ceased running, and provided no end stop conditions have been reached both inputs to the 'fs tune complete' gate IC31a are satisfied and the 'fs tune' bistable is reset such that IC28.11 changes to logic 0. The FS TUNE light emitting diode will extinguish.

Set output level

11 The SET OUTPUT LEVEL light emitting diode lights to indicate the start of the set output level sequence. The three servo circuits remain active. PLA.19 changes to logic 0 and the attenuator module operates to set the required output level. When this has been achieved PLA.T changes to logic 1 to remove an inhibiting input to the 'set output level complete gate' IC17b. When both inputs to IC17b are satisfied the 'set output level' bistable is reset such that IC28.3 changes to logic 0. The SET OUTPUT LEVEL light-emitting diode will extinguish.

Tune complete

12 The 'TUNE COMPLETE' light-emitting diode and the TUNE COMPLETE lamp on the meter panel will light. The attenuator and servo motors are prevented from further operation by PLA.19, 21, 23 and Y changing to logic 1.

13 PLA.U changes to logic 0 to switch the rf power monitoring circuits to indicate peak-envelope-power (pep).

14 PLA.30 changes to logic 1 to extinguish the discriminator indicators on the servo modules and to permit the use of 'push-to-talk' if required. PLA.N changes to logic 1 to switch out the 10 dB attenuator (if used). PLA.30 also switches the drive back to traffic by de-energizing RLG in the extended control module. The 'auto-tune fail' timer output bistable is held set by a signal routed via IC92 and IC8b.

15 If at any stage of the auto tune sequence one of the conditions for completing the sequence is not achieved, then after a preset period the 'auto tune fail' timer operates such that its output bistable changes state and IC5.11 changes to logic 0. A signal routed via D22 is fed to each 'stage complete' gate. This ensures that the stage which has 'held' is indicated by its associated led, also the 'auto tune fail' indicator will light. The servo motors are switched off. The final stage screen supply is switched off. The final stage bias is switched to maximum and the preamplifier is muted. PLA.AA changes to logic 1 to de-energize RLR in the extended control module to indicate there is an 'auto tune fail'. The circuits are reset when coarse tune is again selected.

HT on/off switching

16 The circuit that decides whether or not to initiate a return to coarse tune with the ht switching on and off functions in the following manner.

17 When the amplifier is first switched on, PLA.M is held at logic 0 for a few milliseconds, before it changes to logic 1. This sets the bistable formed by IC12c and d, such that IC12.10 changes to logic 1. With no trip present PLA.16 is at logic 1. With the auxiliary supplies off PLA.S is at logic 1 and IC12.3 is at logic 0 holding IC12.8 at logic 0 via D7. IC12.3 is at logic 0 since auto tune complete has not been achieved, and holds IC12.8 at logic 0 via D8. With the ht supply off, PLA.E is at logic 0. Thus both inputs to IC13c are at logic 1 and consequently IC6.11 is at logic 1 to enforce a 'select coarse tune'. As the amplifier run up sequence starts, so PLA.S changes to logic 0 when the auxiliary supplies switch on. When the ht supply switches on, PLA.E changes to logic 1. IC21c, IC13c and IC21a change state to remove the select coarse tune input to IC6.11. Additionally IC21b changes state resulting in a pulse being fed to IC13.13 via C13, also affecting the bistable formed by IC12c and d, causing a logic 1 to remain at IC13.8.

H.T. trip before 'auto tune complete'

18 Consider the case where a trip occurs before 'auto tune complete' is achieved.

19 As soon as a trip is sensed PLA.16 changes to logic 1. A few milliseconds later PLA.E changes to logic 0. This results in IC21c, IC13c and IC21a changing state to present a logic 1 at IC6.11 initiating a retune. Thus until 'tune complete' is achieved, whereby the bistable formed by IC12c and d is reset, whenever the ht trips off a retune is initiated. Once 'auto tune complete' is achieved then IC12.3 changes to logic 1. PLA.16 is still at logic 0, therefore the state of the bistable does not change. Thus whenever the ht is switched on or off a retune is initiated.

HT trip after 'auto tune complete'

20 Consider the case where a trip occurs after 'auto tune complete' is achieved.

21 When a trip occurs PLA.16 changes to logic 1. Provided the trip is not a failure of the auxiliary supply, then IC12.8 changes to logic 1 and resets the bistable to present a logic 0 at IC13.8. Approximately 50 ms later PLA.E changes to logic 0 as the ht step-start contactor opens. This has no affect now on IC13c and no retune command is fed to IC6.11. When the ht is switched on again, a pulse is fed via C13 to reset the bistable and restore the circuits to their original conditions.

Function switch SA

22 The function switch SA enables the tune sequence to be held at any stage for setting up or fault diagnosis.

23 If the 0 dB PILOT or TRAFFIC MANUAL position is selected, the auto tune circuitry is disabled and manual control of range selection, capacitor servo motors and the attenuators is available by PLA.K changing to logic 0. Additionally PLA.19, 21, 23 and Y change to logic 0 enabling the servo motors to be permanently active. PLA.30 changes to logic 0, to ensure the drive is switched to its tune tone. Consequently the 'TUNE COMPLETE' lamp on the meter panel will extinguish. PLA.U changes to logic 1, switching the forward and reverse power monitor circuits to a fast time constant to facilitate tuning. PLA.N changes to logic 1, switching out the 10 dB tune attenuator, permitting tuning and loading with the drive up to full output level.

24 The final stage screen supply is switched on, the final stage bias is normal and the preamplifier is not muted. If the amplifier is tuned in the 0 dB PILOT position when switch SA is set to MANUAL TRAFFIC the conditions remain as for 0 dB PILOT except that the power meters are switched to read pep and the drive is switched from the tune condition to traffic. The TUNE COMPLETE lamp will light, the discriminator condition indicators and the auto tune status indicators are muted. When SA is set from manual to auto NORMAL, the auto-tune sequence is automatically initiated.

Metering the auxiliary supplies

25 The supplies associated with the servo motors and range solenoids are monitored on meter ME1. To enable the positions of the tune capacitors, or the amount of attenuation switched in to be known, a positioning analogue voltage from the appropriate unit is fed to a voltage follower IC22 which presents a high input impedance to avoid loading the external circuits.

26 The supplies voltages are fed directly to the meter via external multiplier resistors. The voltage scale of the +12V, -12V, +10V, +24V, +33V is 50V full scale deflection, for the +48V it is 100V full scale deflection. When IC22 is switched into circuit the fsd is 8.3V.

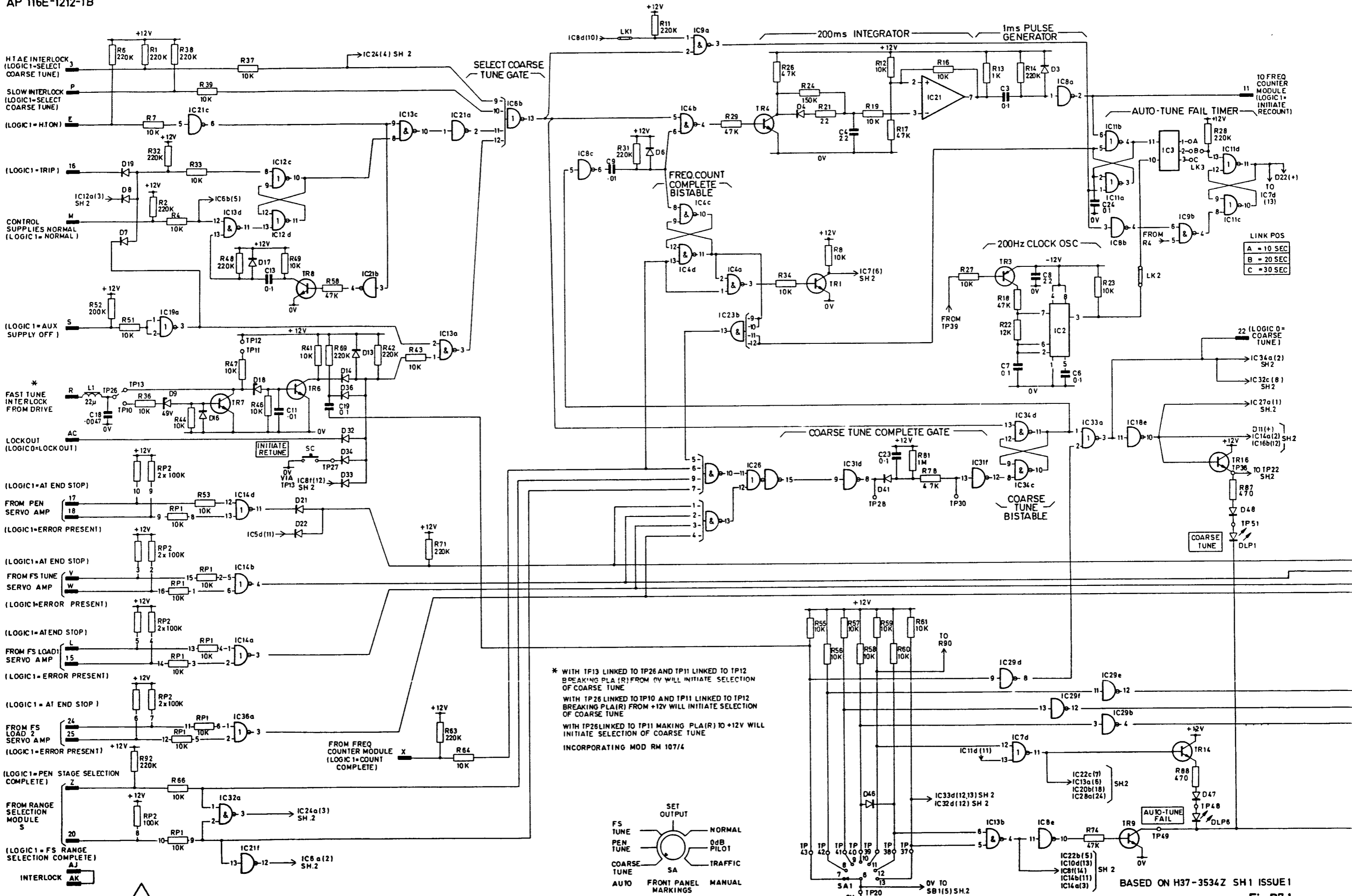
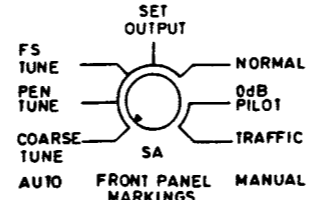


Fig D7-1
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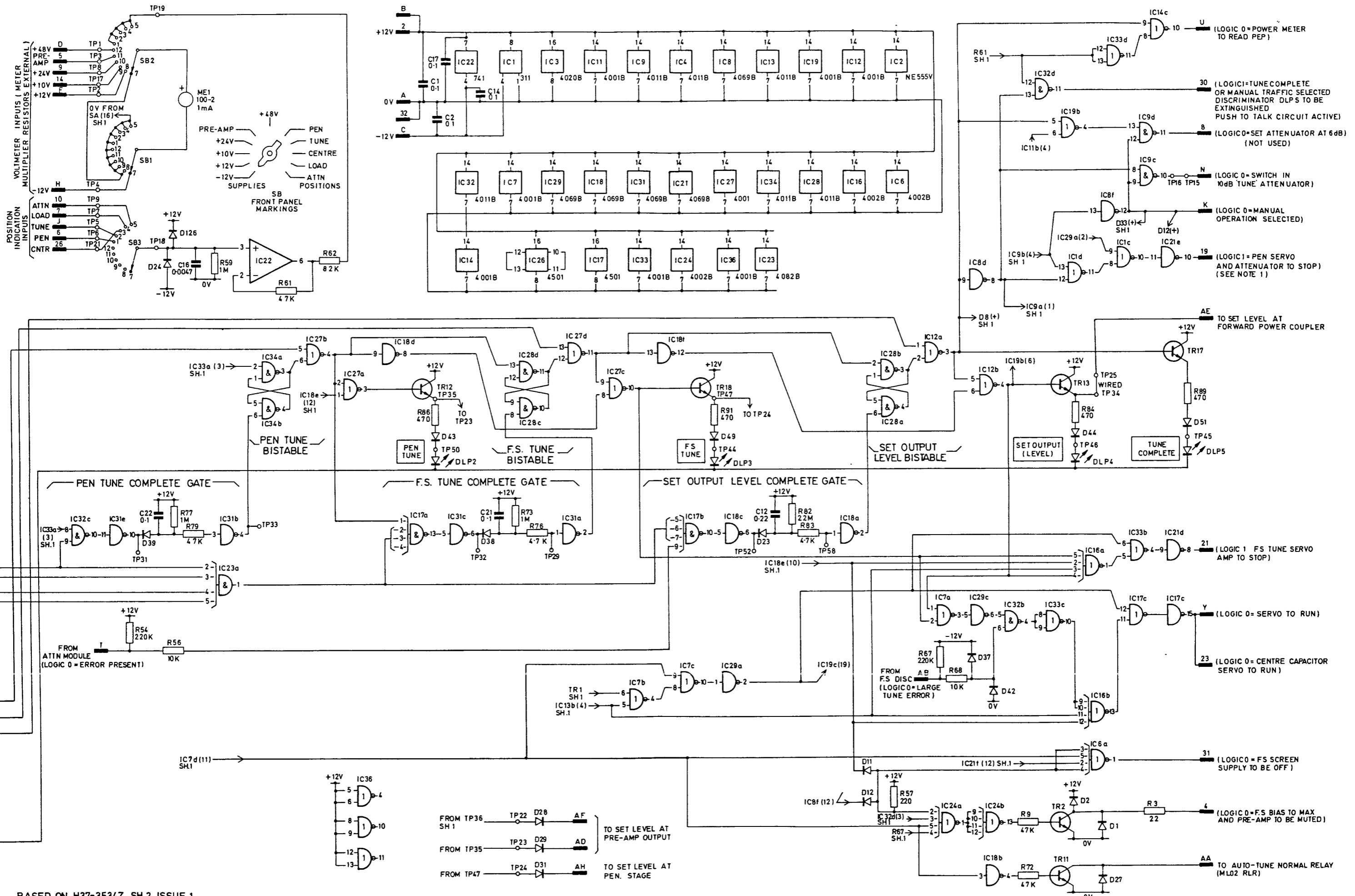
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Module, auto-tune control, 5820-99-751-8027 : circuit diagram



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Fig D7-1



BASED ON H37-3534Z SH 2 ISSUE 1

Fig D7-2

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Module, auto-tune control 5820-99-751-8027: circuit diagram

NOTE: EMBODYING
MOD. RM 051/3

Sub-sect D8MODULE DISCRIMINATOR (ML10)5820-99-751-8034

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INTRODUCTION

1 This module accepts samples of the grid and anode rf signals at both the pen. stage valves and the final stage valve. From these samples it provides direction information, in a digital form, to enable the pen. stage and final stage tuning capacitors to be fine tuned for a 180° phase difference between the valve grid and anode signals. The grid and anode samples are fed to this module via the discriminator sensor assemblies.

2 Digital direction information is also provided for the final stage loading capacitor by comparing the anode and grid voltage levels on the final stage valve.

3 To protect the c-mos integrated circuits against damage that may be caused by withdrawing or replacing the module whilst the supply is on, inputs from PLA are into 'pull up' resistor of typically $220\text{ k}\Omega$ and a series resistor of typically $10\text{ k}\Omega$.

FINAL STAGE TUNINGInput circuits

4 Refer to Fig D8-1. The rf sample from the final stage valve anode, at a level of approximately 1V rms, is applied to the primary winding of T1. A sample, at a similar level, from the final stage valve grid is applied to the primary winding of T2. These transformers have a turns ratio of 1:1 so that unchanged signals are induced in their secondaries. However, the phases of the two secondary windings are reversed, relative to each other, so that the anode and grid samples are given a 180° phase shift, in addition to any which may already exist.

5 Following these phase shifting circuits the remaining signal paths for the two final stage rf samples are identical so that only that of the anode sample is described.

6 The signal is terminated by a 50Ω load, R41, and taken via an emitter follower buffer TR1 to a level matching potential divider R48 and R49. A diode limiter D6 and D9 follows this circuit to prevent the subsequent circuit being overdriven when the signal level increases, at the end of the tuning sequence. Emitter coupled logic line receivers IC14 and IC16 form a cascade amplifier which squares the incoming sine wave, fed from the limiter. The final amplifier IC16a is wired as a Schmitt trigger.

Phase detector

7 Both the square wave rf signal derived from the anode sample and that derived from the grid sample are fed to the phase detector IC7. This is an emitter coupled logic phase detector the output of which is a series of pulses with a width proportional to the phase difference between the inputs. These pulses appear at either IC17.3 or IC17.12, dependent on whether the input at IC17.6 or IC17.9 leads.

8 Differential integration of the two phase detector outputs by IC18 produces a voltage at TP6 with a polarity dependent on the phase of the input signals and a magnitude directly proportional to the phase difference. A positive voltage is produced when the anode sample leads the grid sample with an amplitude of approximately 30 mV/degree of phase difference.

Digital direction indication

9 The analogue phase indication at TP6 is applied to two comparators, IC19 and IC21, connected as Schmitt triggers, one inverting and the other non-inverting. If the magnitude of the phase error exceeds approximately 5° one of these comparator outputs will be 0V. When the anode sample is leading then the output of IC21 will be 0V, the output of IC19 changing to 0V when the grid sample leads. A non-conducting output, approaching +12V, is generated by the remaining comparator. These outputs are inverted by IC1e and IC1f.

10 This provides the direction information for the servo module to drive the final stage tuning capacitor. The capacitor is driven in the required direction to decrease the phase error until this error has been reduced to just beyond zero. At this point, as a result of the Schmitt trigger action, the output of this comparator changes to 0V.

11 Once the adjustment has been made, to give a logic 0 output from both inverters, they will remain in this state until the phase error exceeds 5° in either direction. In this event the appropriate inverter output changes to logic 1 resulting in the tuning capacitor being adjusted once again.

Large tune error

12 A large tune error is detected by comparators IC12 and IC13. These comparators are connected as a window detector to give a logic 0 output on PLA.H, if a large tune error exists. The threshold of this detector is set at $\pm 15^\circ$. Its purpose is to inhibit the adjustment of the final stage loading capacitor until the tuning capacitor is reasonably close to the correct tune setting.

13 It is possible for the phase error voltage at TP6 to be the equivalent of a reciprocal phase difference indication of greater than 180° . In this event a false reverse polarity will occur at TP6 to the alternative true smaller phase error indication. Comparators IC9 and IC11 detect if a false large phase indication has occurred and if so drive TR3 and TR4 to shunt the r.f. samples at the input to the line receivers.

14 This has the effect of driving the output on TP6 to the opposite polarity and thus removing the drive from the shunt transistors. The phase error output will then hold this polarity to indicate the desired smaller phase angle. Delay circuit R26 and C17 prevents this circuit oscillating.

Loading comparator

15 The final stage anode and grid samples at the output of emitter followers TR1 and TR2 are also taken to the loading comparator circuit.

16 The detector circuit centred on D3 provides a positive voltage equal to the magnitude of the anode sample, while the circuit based on D4 produces a similar negative voltage from the grid sample. These two voltages are taken to either end of the front panel LOAD BALANCE potentiometer RV2.

17 When the final stage valve is loaded correctly the grid and anode voltages will always have the same magnitude ratio. The LOAD BALANCE potentiometer RV2 is adjusted, when the discriminator module is installed in the amplifier, so that a null is obtained on the sliding contact when the correct loading is achieved.

18 The slider voltage is amplified by IC4, to increase the sensitivity of the null, and taken to another complementary pair of Schmitt trigger circuits, IC7 and IC8. These provide directional adjustment information for the final stage loading capacitor servo in the same way as those of the tuning capacitor servo, IC19 and IC21.

PEN STAGE TUNING

19 Refer to Fig D8-2. The anode and grid samples from the pen. stage valves are applied to T3 and T4 respectively. This input circuit together with the remaining circuits are identical to those for the final stage valve samples, with the exception of the following changes. A large tune error circuit and a loading comparator are not required for the pen. stage, since the tuning and loading capacitors are driven together in this stage.

20 An additional facility is provided, an analogue indication of the pen. stage anode level for use by the level setting circuits in the amplifier during the tune sequence. This is derived by rectifying the anode sample of the output of the emitter follower TR6. The rectified sample is amplified and buffered by IC32 before being fed out on PLA.AH. Potential divider R128 and R139 together with diode D21 ensure that a small residual output is present for the level setting circuits when no r.f. signal is present.

OVERDRIVE CIRCUIT

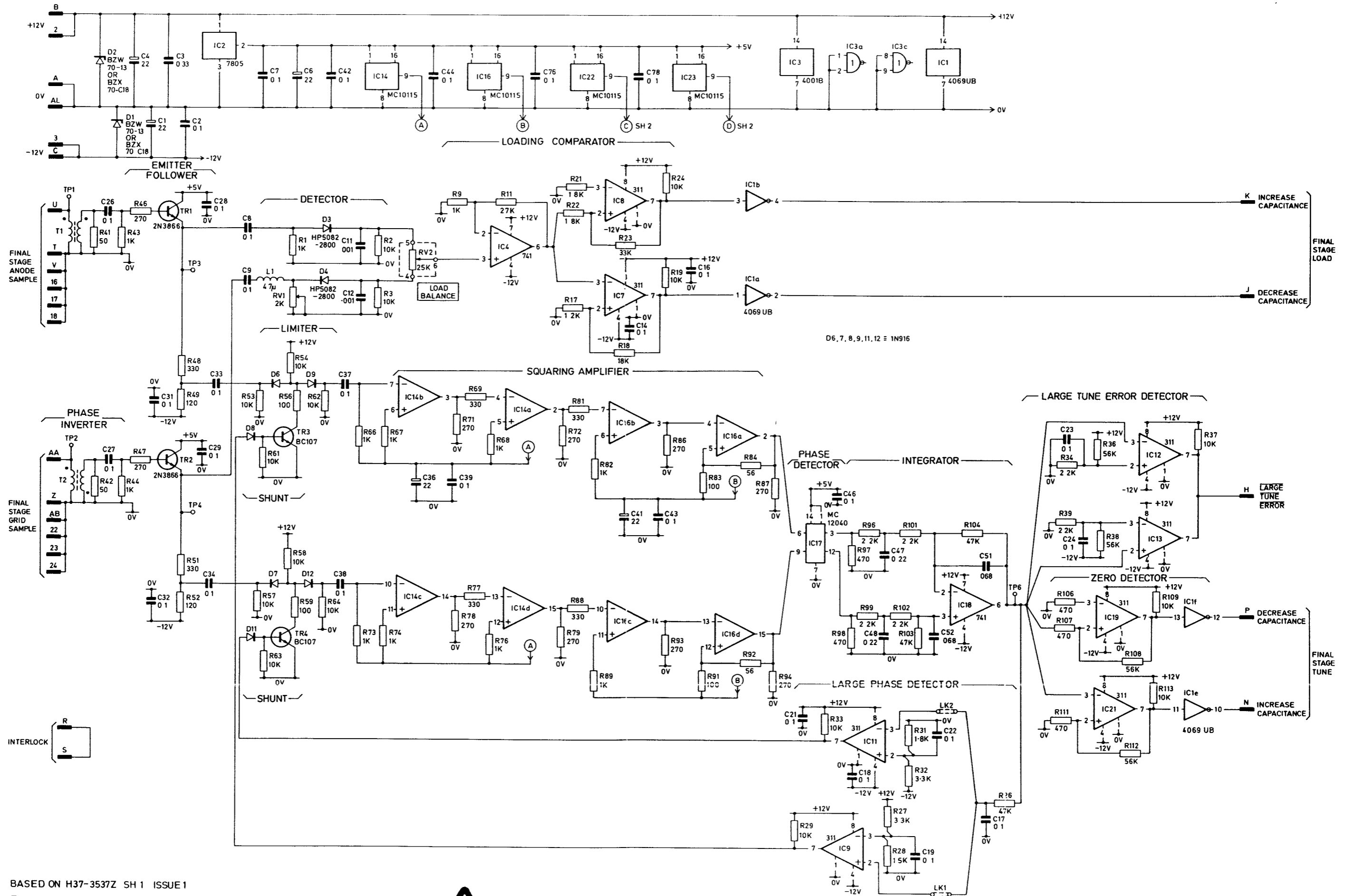
21 Refer to Fig D8-1. The overdrive circuit is a comparator, IC6, which accepts an analogue voltage representing the forward power level and compares it with the OVERDRIVE THRESHOLD level pre-set by the front panel potentiometer RV1. A logic 1 from IC6 is generated if the threshold is exceeded. Latch IC3b and IC3d allows the overdrive condition to be latched and provide an alternative logic 0 latched output to PLA.E. This latched output is cleared by a logic 1 recount command to PLA.F, from the auto-tune module.

5V REGULATOR

22 The +5V power supply for the emitter coupled logic integrated circuits is provided by the integrated regulator IC2.

TEST LINKS

23 Links LK1 to LK4 allow the inputs to the large phase detector circuits to be broken for test purposes and should normally be closed.



BASED ON H37-3537Z SH 1 ISSUE 1
Fig D8-1

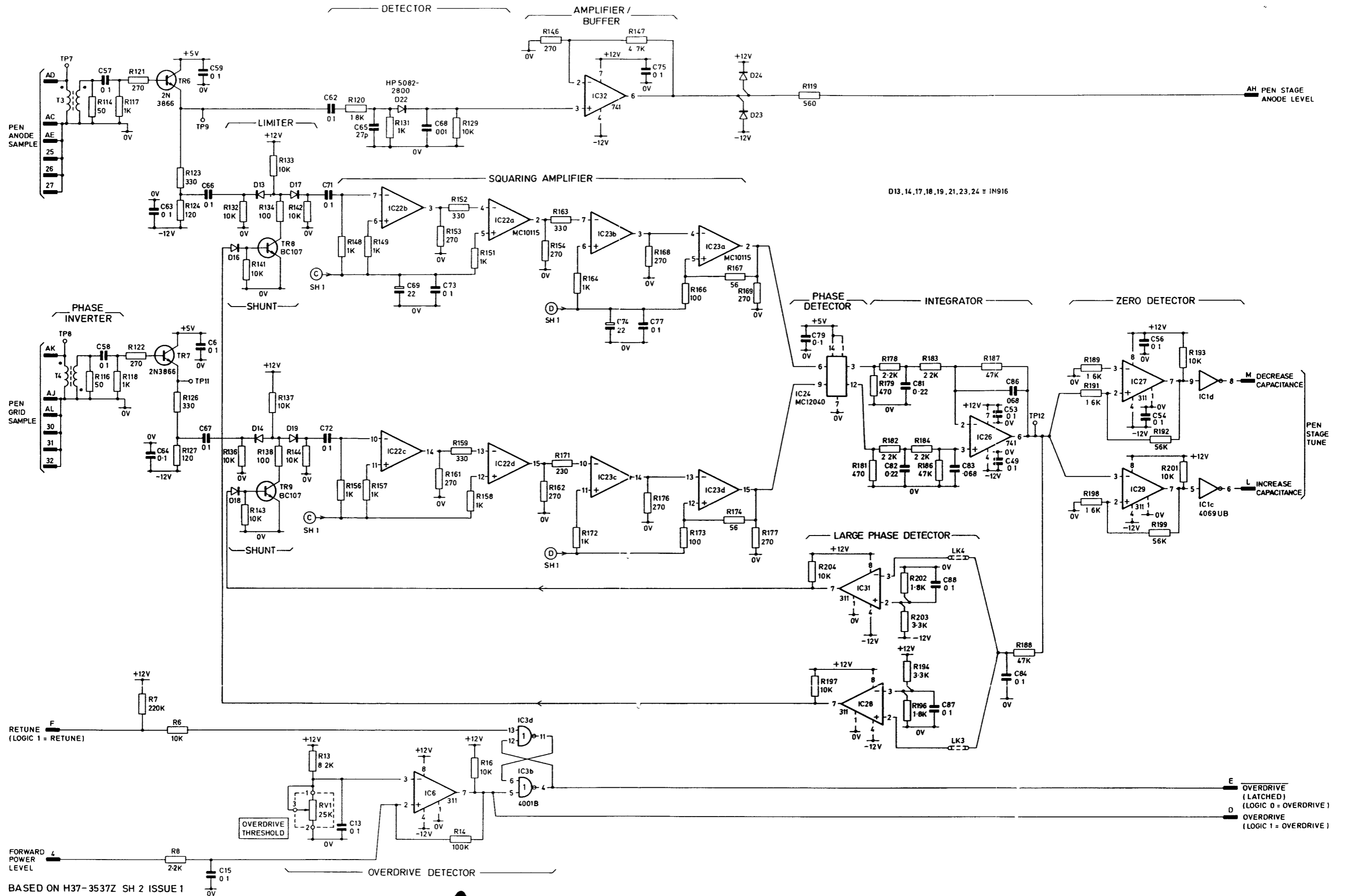
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Module, discriminator, 5820-99-751-8034 : circuit diagram

Fig D8-1



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Fig D8-2

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Module, discriminator, 5820-99-751-8034 : circuit diagram

Fig D8-2

Sub-sect D8

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Sub-sect D9MODULE RANGE SELECTION (ML11)5820-99-751-8039

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INTRODUCTION

1 This module actuates the range selection for the penultimate and final stages of the amplifier, as part of the overall auto-tune or manual tuning sequences.

2 Range selection for the pen. stage and final stage is provided by shorting out sections of the inductors in the coil assemblies and selecting additional capacitors. This is achieved by way of power solenoids which are controlled by the module. These solenoids are energized using the +48V supply and held on by the +10V supply in sequences of several ranges at a time, in order to limit the current demand from the +48V supply.

3 Automatic or manual range control is determined by the auto-tune module. A frequency range can be selected, either by using the front panel RANGE SELECTION switch, or, automatically in response to data received from the counter module. The appropriate range selection solenoids are then selected to be energized.

4 Signal processing is by means of c-mos digital integrated circuits. For the supply voltage used the logic levels are defined as:

- 4.1 Logic level 0 = 0 to 3.5V and
- 4.2 Logic level 1 = 8.5V to 12V.

5 To protect the integrated circuits against damage that may be caused by withdrawing or replacing the module while the +12V supply is on, the inputs from the edge connector are fed into a 'pull-up' resistor of typically 100 k ohms and a series resistor of typically 10 k ohms.

DESCRIPTION

Manual/automatic range control

6 When manual range selection is required PLA.2 is held at logic 0 causing the outputs from the NAND gates normally controlled by the automatic range select input to be held at logic 1. Diodes D13 to D23 are now reverse biased and the automatic range select input is inhibited. The front panel mounted RANGE SELECTION switch SA connects the cathode of one of these diodes to logic 0, via D6 and RP12, to select the required range.

7 As a result of SA having a break-before-make action a momentary logic 1 is fed to IC34.9 each time a different range is selected manually. Also, IC34.11 is held at logic 1 by the logic 0 on PLA.2, inhibiting the auto recycle input from the counter module on PLA.C. Hence when a new range is selected by SA, IC33.10 momentarily changes to logic 0, to initiate the new range selection cycle.

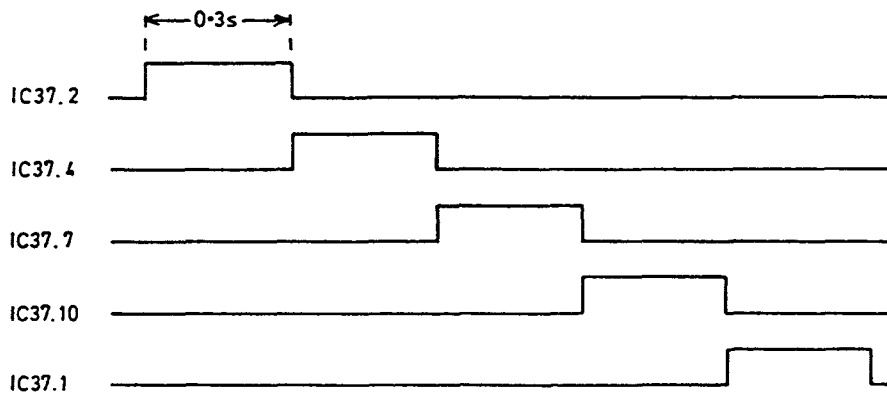
8 When automatic range control is selected PLA.2 is held at logic 1. This results in IC24.6 being held at logic 0, preventing IC34.10 responding to the manual range select input. A logic 0 auto-recycle input to PLA.C, from the counter module, will also result in IC33.10 changing to logic 0 initiating a new range selection cycle. The module will now respond to the automatic range select input from the counter module. This input is shown in Table 1.

TABLE 1 AUTOMATIC RANGE SELECT INPUT

Range	Input to PLA							
	9	K	D	C	J	8	L	M
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	1
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	1	1
5	0	0	0	0	1	1	1	1
6	0	0	0	1	1	1	1	1
7	0	0	1	1	1	1	1	1
8	0	1	1	1	1	1	1	1
9	1	1	1	1	1	1	1	1

9 The logic 0 on IC33.10 sets the bistable formed by IC1.1 to 6, via IC33.6 and 4, such that IC1.4 changes to logic 0. This results in reset signals being fed to IC38.15, via IC39.9 and 10, and the final stage valve grid 2 control circuit via PLA.4, thus ensuring that the counter is cleared to zero count and the final stage screen supply is switched off while range selection is in progress. This bistable is also controlled by the auxillary supplies on and control supplies normal inputs, from the supplies control module, to PLA.H and B respectively.

10 When IC33.4 reverts to logic 1, IC38 is enabled to count the output of the clock pulse generator IC42. This clock pulse has a nominal time period of 0.3s so that the counter generator timing waveforms are as shown in Fig D9-1.



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Fig D9-1 Range selection timing

Range selected indication

11 For both auto and manual range selection the output of the range selection circuit is as shown in Table 2.

TABLE 2 RANGE SELECT OUTPUT

Range	Output								
	IC13.11	IC13.10	IC13.4	IC13.3	IC23.10	IC23.11	IC23.3	IC32.6	IC22.10
1	0	1	1	1	1	1	1	1	1
2	1	0	1	1	1	1	1	1	1
3	1	1	0	1	1	1	1	1	1
4	1	1	1	0	1	1	1	1	1
5	1	1	1	1	0	1	1	1	1
6	1	1	1	1	1	0	1	1	1
7	1	1	1	1	1	1	0	1	1
8	1	1	1	1	1	1	1	0	1
9	1	1	1	1	1	1	1	1	0

12 So, dependant upon the range selected, one of the transistors in transistor packs IC2 and IC3 will conduct, resulting in the appropriate RANGE SELECTED indicator being lit.

Range selection

13 Initially assume range 1 to be selected. Here range select solenoid circuits S1A and S1B only are required to be energized, as follows. For range 1 the range select output, see Table 2, will cause IC27.2 and IC36.12 to be switched to logic 1. Hence, when IC37.10, followed 0.3s later by IC37.6, change, logic 1, as a result of the counter being enabled, the S1A followed by the S1B solenoid driver groups conduct. TR18 and TR51 together with TR2 and TR62, form the S1A group while TR23, TR53, TR4 and TR64, form the S1B group. This results in the S1A and S1B range select solenoids becoming energized from the +48V supply.

14 When IC37.6 changes to logic 1, IC37.10 reverts to logic 0. The S1A solenoid energizing transistors TR18 and TR51 will now switch off, but the solenoid will be held in from the +10V supply, via TR2 and TR62. After a further period of 0.5 seconds the S1B solenoid energizing path will switch off, when IC37.6 reverts to logic 0, as described for the S1A solenoid.

15 These external +48V and +10V supplies are isolated from each other by blocking diodes fitted to the control frame.

16 If, for example, range 4 is now selected, range select solenoid circuits S2A, S3B and S4A are required to be energized. For this range the output of the range select circuit, see Table 2, will apply a logic 0 to IC16.9. This in turn causes IC34.2, IC6.5 and IC6.13 to change to logic level 1, enabling these NAND gates. As a result of this the bistable latches formed by IC8.3, 4, 13, IC8.6, 7, 9 and IC8.10, 11, 12 will be reset in sequence when the counter outputs on IC37.6 and IC37.10 change to logic 1.

17 This results in IC8.13, 9 and 10 changing to logic 0 causing the S2A and S4A transistor driver groups to be energized and held in, via the +48V and +10V supplies respectively, in a similar manner to the range 1 solenoids selection, described in Paras 13 and 14. The S3A transistor driver group is prevented from becoming energized from the logic 1 on IC8.9 by the logic 1 on IC31.1. The remaining transistor driver group required to be energized for range 4 is S3B. These transistors are energized as a result of IC14.12 and 15 being held at logic 1 resulting in IC37.12 changing to logic 1 energizing the S3B solenoid as before.

18 Since the solenoids required to be energized for range 4 are different to those for range 1 the range 1 solenoids will be de-energized when IC27.2 and IC36.12 revert to logic 0.

19 Further changes in the frequency range selected will result in any additional solenoids that are required to be energized being selected in sequence, as the pulse sequence progress. If the new frequency range selected does not require all of the solenoids previously energized, then those solenoids not required are de-energized at the start of the selection sequence, when IC38.2 changes to logic 1. This logic 1 causes any bistable latches of IC8 and IC9 not selected by the new range select output data to be set such that Q is a logic 1. The range selection solenoids associated with these bistable latches will then be de-energized.

20 The time taken for any range change is determined by the range selection timing outputs from the counter, a range selection taking 1.5 seconds to complete.

21 Details of the solenoids energized for each of the nine available frequency ranges are shown in Table 3.

TABLE 3 RANGE CONTROL

Range	Solenoid circuits energized
1	S1A, S1B
2	S1A, S2A
3	S1A, S2A, S3A, S3B
4	S2A, S3B, S4A
5	S2A, S3A, S3B, S5A
6	S2A, S3A, S3B, S4A, S6A
7	S2A, S3A, S3B, S4A, S5A, S7A
8	S2A, S3A, S3B, S4A, S5A, S6A, S8A
9	S2A, S3A, S3B, S4A, S5A, S6A, S7A, S9A

Note...

Applies only when links LK1 to LK7 are set to position A.

Links

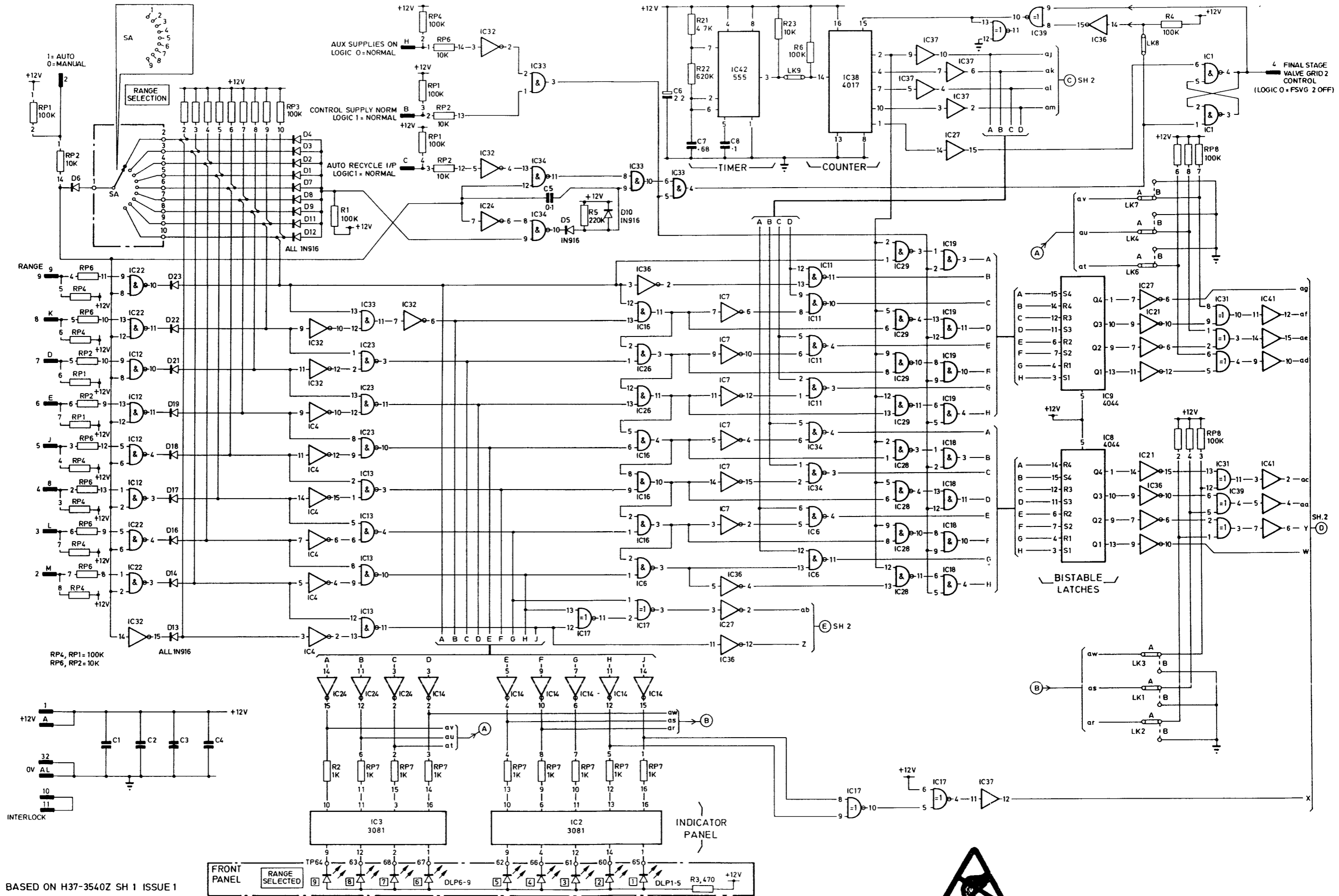
22 Links LK1 to LK7, when set to position A, provide an optional range selection sequence where the previous solenoid circuit to the finally energized solenoid circuit is de-energized. If, for example, range 9 is selected and these links are set to position B, all the bistable latches IC8 and IC9 are set and all the solenoid circuits are energized. Setting these links to position A would result in the output on IC31.10 being held at logic 0, for this range, as a result of both of its inputs being held at logic 1. This causes the S8A solenoid circuit to be de-energized.

Power fail recycle

23. The power supplies monitoring inputs to PLA.B and PLA.H, from the $\pm 12V$ power supply unit and the trip sensing module respectively, detect the presence of the +48V, +33V, +24V, +10V auxillary supplies and $\pm 12V$ control supplies. In the event of one of these supplies failing either PLA.B changes to logic 0 or, PLA.H changes to logic 1. This results in a logic 0 recycle output on IC33.3 causing all of the solenoid circuits to be de-energized. When these supplies return to normal the range selection sequence will be recycled from the start.

IC types

24 Details of the integrated circuit types and their power connections are shown on Fig D9-4.

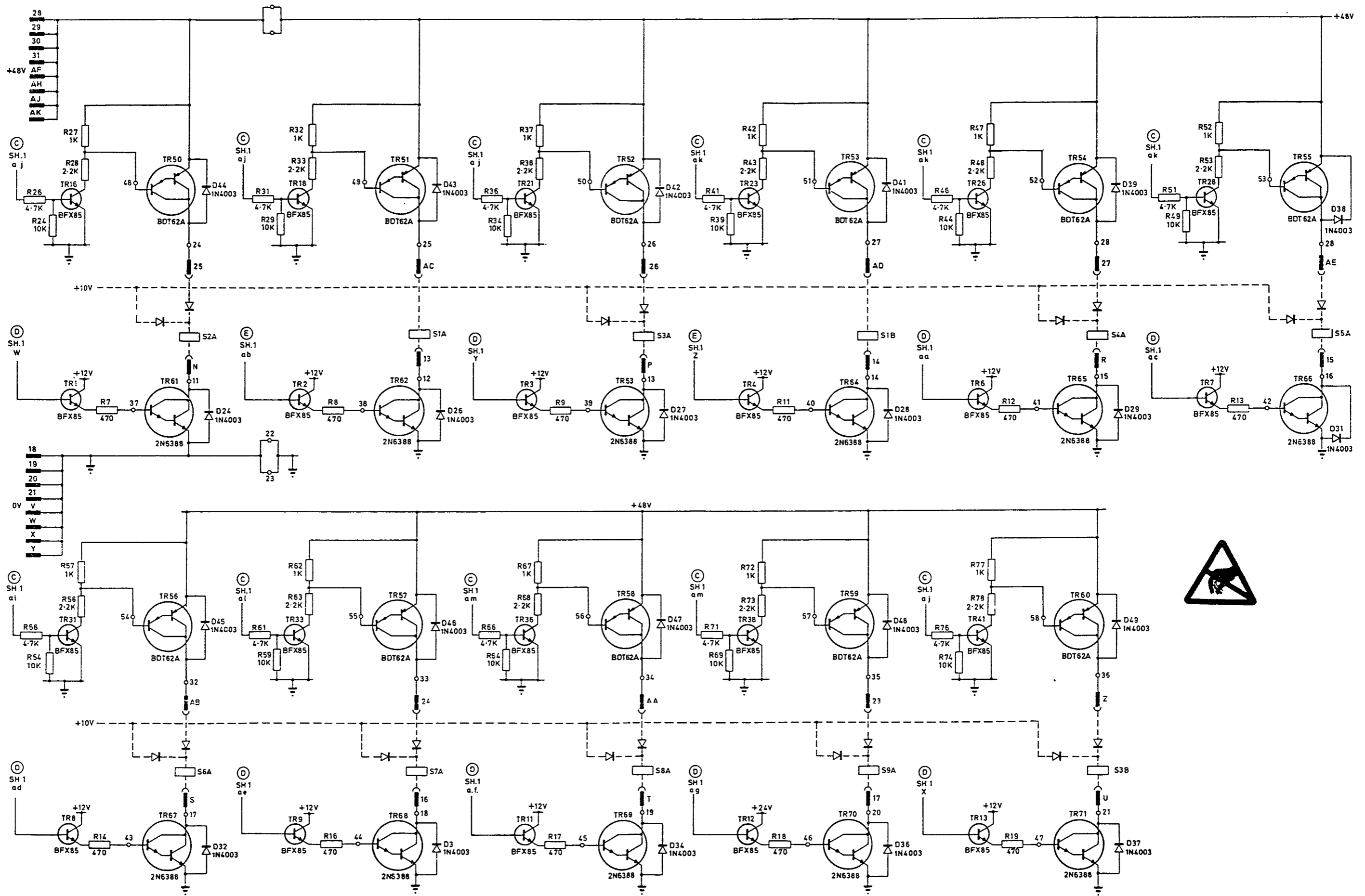


BASED ON H37-3540Z SH 1 ISSUE 1

Fig D9-2

Module, range selection, 5820-99-751-8039: circuit diagram



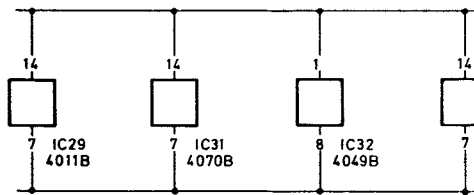
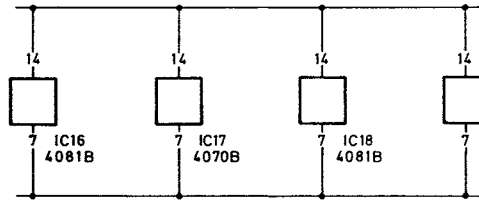
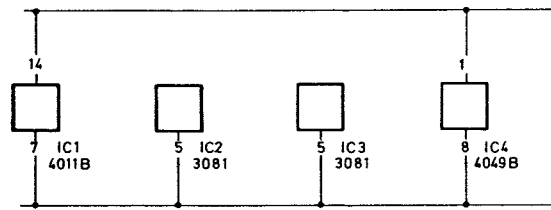


BASED ON H37-3540Z SH 2 ISSUE 1 MOD RM072/1 INCORPORATED

Fig D9-3

Module, range selection, 5820-99-751-8039: circuit diagram

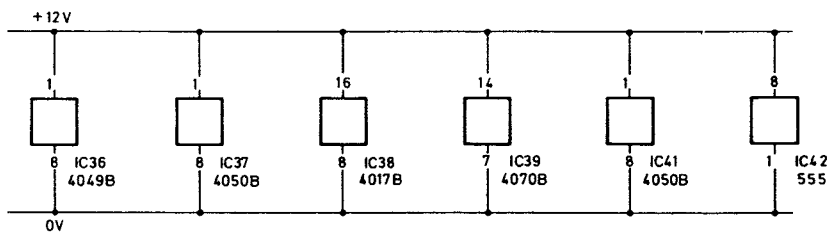
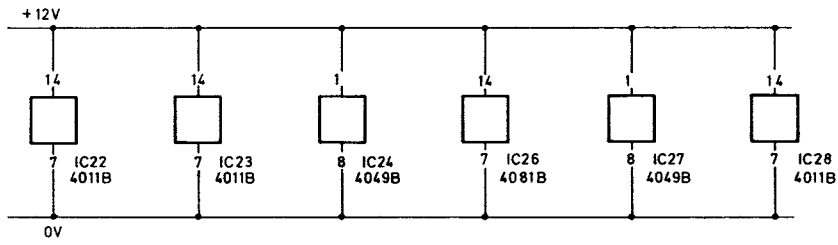
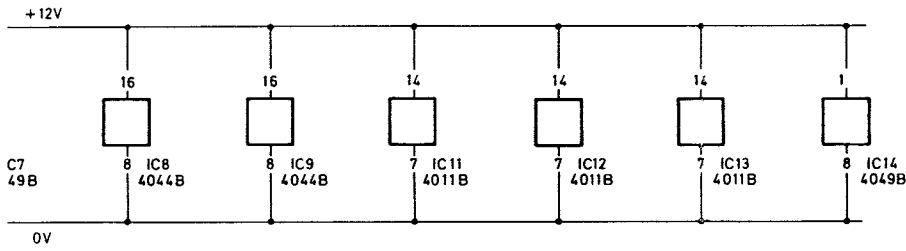
Fig D9-3



BASED ON H37-3540Z SH 3 ISSUE 1
Fig D9-4

Module, rat

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99-751-8039:circuit diagram



Fig D9-4

Sub-sect D9

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Sub-section D10MODULE CONTROL SERVO (ML 12,13,15)5820-99-760-2978

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INTRODUCTION

1 The module provides for control of the stepper motor which positions the appropriate capacitor assembly in response to commands from the amplifier control system. A servo module (ML12) is required to drive the pen. stage ganged capacitors module (ML13) to drive the final stage tuning capacitor and module (ML15) to drive the final stage loading capacitor.

2 Signal processing is by means of c-mos digital integrated circuits. The supply used is +12 V and logic levels are defined as:

2.1 Logic level 0 = 0 to 3.5 V and

2.2 Logic level 1 = 8.5 to 12 V.

3 When the motor is being driven the motor supply is 24 V, but when the motor is stopped an economizer circuit is brought into operation and the power dissipation is reduced by applying the 10 V supply to the motor.

4 To protect the integrated circuits against damage that may be caused by withdrawing or replacing the module whilst the supply is on, inputs from PLA are into a 'pull-up' resistor of typically 220 k Ω and a series resistor of typically 10 k Ω .

CIRCUIT DESCRIPTIONGeneral

5 The UK/FRT 651 amplifier can be operated either in an auto-tune mode or manually. When the auto-tune sequence is selected the front panel control on each servo module is rendered inoperative.

6 During the auto-tune sequence the module receives analogue information from the counter module which represents coarse tune information to position the associated capacitor appropriate to the amplifier radiated frequency. The analogue voltage from the counter is compared with the analogue voltage produced by the shaft encoder potentiometer. This will drive the capacitor assembly until zero error is produced, which completes the coarse tune sequence.

7 Once the coarse tune sequence is complete, the servo module is enabled into the fine tune mode, which will drive the associated capacitor assembly under control of the relevant discriminator or comparator. An indication of rotation direction is shown by led's (light emitting diodes) on the servo module front panel.

8 The analogue voltage from the shaft encoder is utilized to prevent the capacitor assembly travelling beyond minimum or maximum capacitance. When this condition is detected the motor is stopped and this is indicated by the end stop led on the servo front panel.

9 When the manual mode is selected each capacitor assembly is capable of being operated independently by the manual control on the associated servo module front panel.

Auto-tune operation

10 When the automatic mode of operation is selected a logic 1 will be fed to PLA(9). This energizes RLA and de-energizes RLB. During the coarse tune sequence PLA(8) is at logic 0, therefore the motor will respond to the analogue voltage fed to PLA32 from the counter module (ML17). This voltage will vary between 0 V and + 8 V, where 0 V represents minimum capacitance and + 8 V represents maximum capacitance.

11 When in the automatic mode and when coarse tune is not selected, the servo is under the control of the associated discriminator inputs at PLA(6) and (7). Logic 0 will appear at IC5c(10), preventing the operation of the comparators IC9 and IC10. Logic 1 at PLA(6) or PLA(7) will drive the motor to decrease or increase the capacitance. This will be indicated on the front panel by led's DLP2 and DLP3 during the tune sequence, and will be inhibited by the tune complete logic 1 at PLA(4).

Manual operation

12 When manual control is selected a logic 0 is present at PLA9. This will energize RLB and de-energize RLA, IC5c(10) will change to logic 1, IC14f(15) will change to logic 0, hence the discriminator inputs will be inhibited, but DLP2 or DLP3 will light while PLA4 is at logic 0 (tune not complete).

13 Under manual control IC6(1), (6) (8) and (12) are at logic 1, providing the capacitor assembly is within the limits of travel. The voltage from the manual control wiper RV1, via RLB1, and the voltage from the shaft encoder wiper are fed to the differential amplifier IC8(2) and (3) respectively. The output of IC8 is fed to comparators IC9 (increase capacitance) and IC10 (decrease capacitance).

14 The trigger voltage of IC9 is 2.5 V. When the input voltage on IC9(2) exceeds this value then IC9(7) will change to logic 1. The output at IC13(4) will change to logic 0, thus triggering IC6 to operate IC4 and trigger the direction bistable IC3a to give an 'increase' signal.

15 The trigger voltage of IC10 is -2.1 V. When the input voltage at IC10(3) is more negative than 2.1 V, then IC10(7) will change to logic 1. The output at IC13a(3) will change to logic 0, thus triggering IC6 to operate IC4 and trigger the directional bistable IC3a to give a 'decrease' signal.

Motor stationary conditions

16 When the motor is required to be stationary, the logic level at IC6a(3) and (4) will be at logic 1. As the clock is free running at IC4(3) and (11) then IC4(1) and (13) will also be at logic 1, thus IC5a(3) will be at logic 0. This will clock through to IC3b(13) causing the gate IC5b to cut off the clock to the stepping J-K bistables. The output at IC7c(15) will be at logic 0 to operate the power supply economizer circuit and IC3b(12) will be at logic 1, switching TR25 on and TR26 off.

The ramp clock oscillator

17 The ramp clock oscillator comprises a timer connected as a free running oscillator, the basic frequency of operation is determined by C2, R35 and the resistor in the calibration module ML03. This resistor is situated in the calibration module to ensure interchangeability of the servo modules, where the stepping motors are operated at different speeds.

18 Transistors TR25 and 26 are connected to form a Miller integrator. TR25 is switched off, the voltage at TR26 collector will fall in a linear manner producing a negative ramp between 9.3 and 6.2 V at IC1(5). This ramp has a duration of approximately 220 ms. When TR25 is switched on, IC1(5) restores to 9.3 V in approximately 20 ms. Therefore when no error is present the frequency at IC1(3) will be low. When an error is present, the frequency at IC3b(12) is low and the ramp clock oscillator frequency will increase linearly to twice the original frequency in a period of 220 ms. This starts the motor at low speed, hence giving greater motor torque.

19 Since the voltage at IC1(5) takes approximately 20 ms to reset to 9.3 V the comparator IC18 and associated gates prevents the motor restarting until the lower frequency is produced. This is achieved by resetting the direction bistable which opens the clock gate to the step producing circuit. A logic 1 on PLA(D) will also prevent the motor from running.

Direction bistable IC3a

20 The direction bistable IC3a is 'set' or 'reset' according to the direction-of-travel dictated by the logic levels at IC4(5) and (9). The true and complement outputs at IC3a(1) and (2) are fed to IC16 and control the direction of the step sequence related to the outputs at IC3a(12) and (13). The outputs at IC16(10) and (11) are used to inhibit the 'direction' signal not if the motor is commanded to increase capacitance, then IC4a(5) will be at logic 0 and IC4b(9) will be at logic 1. On the front positive edge of the clock pulse at IC1(3), after the appearance of the error logic 0 at IC4a(5), the logic levels at IC3a(1) and (2) will be logic 0 and 1 respectively. After the next negative edge of the clock pulse at IC1b(3), IC3b(13) will be at logic 1, hence the 'set' input at IC4b(8) will be at logic 1. This prevents any 'decrease' capacitance signals from being accepted until the 'increase' capacitance sequence has been completed.

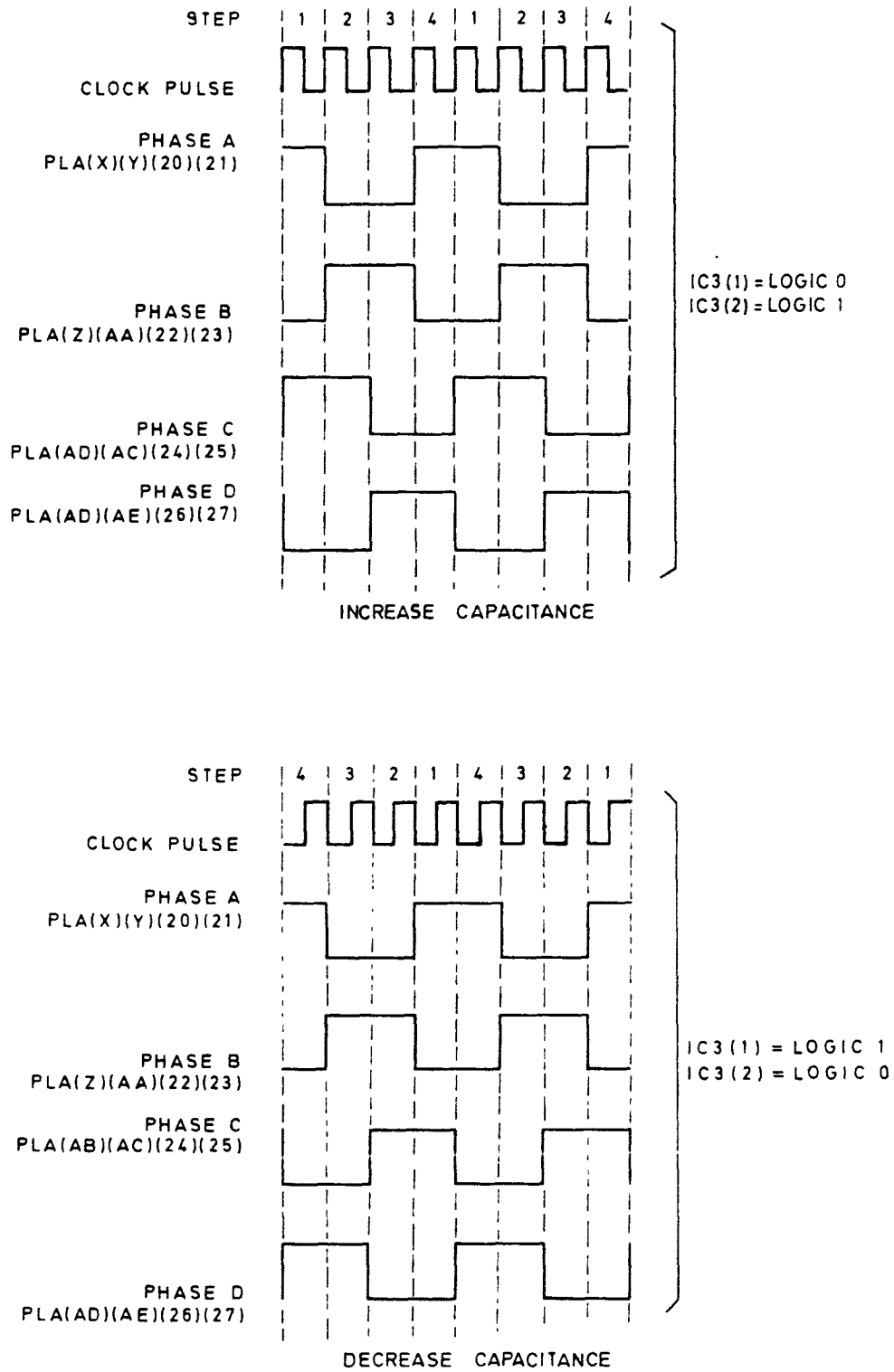
Control step sequence

21 The control step sequence, as shown in fig D10-1, is created by the J-K bistables IC2(a) and (b). When the outputs at IC3a(1) and (2) are set as shown, then the corresponding four-step sequence will be obtained. The transition from one state to another will occur at positive-going transitions of the clock at IC2(3) and (13). Changes at IC3a(1) and (2) will occur only when the clock inputs to the J-K bistables IC2a and b are low.

Stepping motor drive circuits

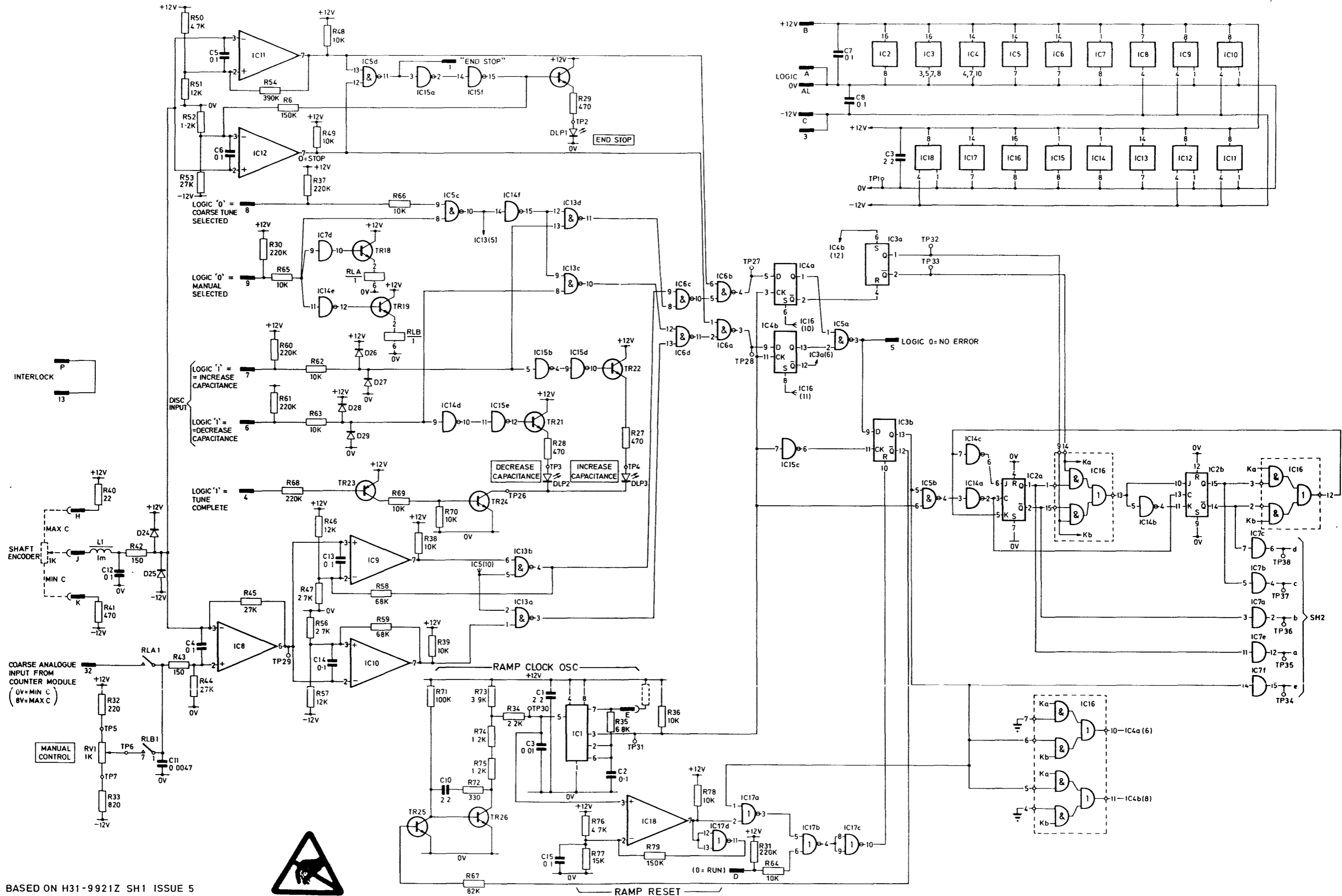
22 The positive voltage occurring at PLA(R) (S) (T) (14) (15) and (16) is derived from either +24 V or +10 V, dependant on the logic level at e. When e is at logic 1, the driver transistors TR12, TR11 and TR10 are switched on. This will switch on the Darlington pair TR3 and TR13. applying the +24 V supply to the motor via diode D1. When e is at logic 0, transistors TR10, 11, 12, 13 and 3 will be switched off, applying the +10 V supply to the motor via diode D2.

23 The four motor phases, A, B, C and D are driven by four identical transistor driver stages. Considering phase A, when at logic level 1, the driver transistor TR14 is switched on to activate the Darlington pair TR9 and TR5. Diode D19 prevents the maximum collector voltage from being exceeded. Diode D16 prevents the output collector voltage from reaching more than 0.7 V negative with respect to earth.



H-00-1140G SH.33 (3)

Fig D10-1 Motor drive step sequence



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Fig D10-2

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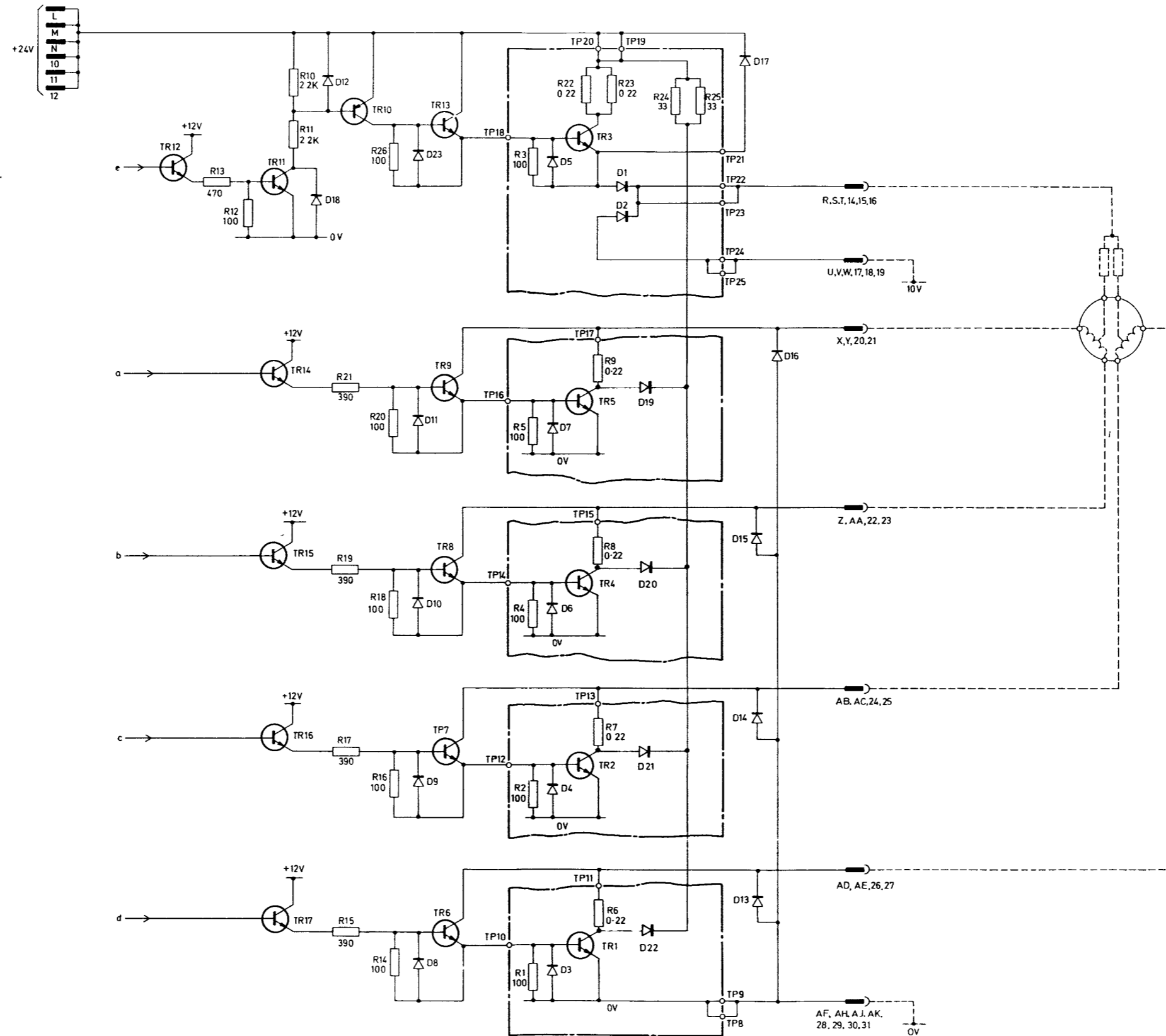


Module control servo 5820-99-760-2978 : circuit diagram

Fig D10-2

Sub-sect D10

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BASED H31-9921Z SH 2 ISSUE 6

Fig D10-3

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Module, control servo, 5820-99-760-2978 : circuit diagram

Fig D10-3

Sub-sect D10

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Sub-sect D11MODULE SERVO (ML14)5820-99-751-8058

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10	Circuit Description
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16	Motor control
27	Counter
28	Decoder
29	Auto/manual control
31	End stop detectors
35	Motor waveform generator
37	Motor drive
38	Economizer
39	Ramp clock oscillator
42	Shaft encoder potentiometer
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D11-3	Module servo: circuit	10
D11-4	Module servo: circuit	11

INTRODUCTION

1 This servo module provides clocking waveforms for the stepping motor which drives the rf output centre variable capacitor to its tune position. Tune data for this module is provided by either the counter module, when auto-tune is selected, or, the module front panel push-button switches, when manual is selected. The centre capacitor and its motor are situated in the capacitor assembly (centre) which forms part of the output stage of the amplifier.

2 Signal processing is by means of c-mos digital integrated circuits. The supply used is +12V and logic levels are defined as:

Logic level 0 = 0 to 3.5V and

Logic level 1 = 8.5 to 12V.

3 When the motor is being driven the motor supply is 24V, but when the motor is stopped an economizer circuit is brought into operation and the power dissipation is reduced by applying the 10V supply to the motor.

4 To protect the integrated circuits against damage that may be caused by withdrawing or replacing the module whilst the supply is on, inputs from PLA are into a 'pull up' resistor of typically 220 k Ω and a series resistor of typically 10 k Ω .

GENERAL DESCRIPTION

5 A block diagram of the servo module is shown in Fig D11-2.

6 The amplifier can be operated either in an auto-tune mode or manually. When the auto-tune mode is selected the front panel controls on the servo module are rendered inoperative.

7 For both methods of tuning the capacitor is driven from a four-phase stepping waveform generated by this module. This output is generated until a comparator senses that the tune position has been achieved. When the motor is stopped the economizer circuit is enabled to reduce the motor supply voltage. Since the capacitor is a vacuum type it tends to return to maximum capacitance when the power is switched off. After the amplifier is switched on, and the auxiliary supplies are established, the capacitor is driven to minimum capacitance, as detected by the position detector, and back to the required tune position.

8 The data selector is controlled by the auto-manual input, selecting tune data from either the frequency counter module or the decoded output of the front panel manual position switches. The selected data is compared with the output of the counter, which counts the clock pulses to the four-phase waveform generator until a count equal to the selected data is detected. At this point the clock is inhibited stopping the motor.

9 The ramp generator is reset each time the motor stops. This circuit provides a lower frequency clock pulse, to improve the starting torque of the motor, when a tune sequence is initiated gradually increasing to full frequency.

CIRCUIT DESCRIPTION

10 A circuit diagram of the module is shown in Fig D11-3 and Fig D11-4 and details of the motor drive stepping waveforms are shown in Fig D11-1.

Initiate

11 When the overall equipment is first switched on the capacitor will be at maximum capacity and the counter will have a random value. Therefore, regardless of the output of the comparator, the motor must initially be driven to reduce the capacitance until the optical position sensor indicates the zero position has been achieved and the counter can be zeroed.

12 This is initiated by the aux. supplies on input to PLA.L. Before the auxiliary supplies in the amplifier are established this input is a logic 1. After inversion by IC6c it sets the latch IC9c and d to give logic 0 at IC9.10. This forces the IC9.3 output to logic 1 to set the direction to down regardless of the output of the comparator.

13 When the auxiliary supplies are switched on, the aux. on input changes to logic 0 but the state of the latch IC9c and d remains unchanged. While the run input to PLA.D is also at logic 0 there will be a logic 0 at IC7.1. The ramp generator will be reset causing a logic 0 to be fed to IC7.2 resulting in IC17.8 changing to logic 1 and, providing IC17.9 is also logic 1, the motor running. This is ensured by the output at IC9.10 which causes IC9.4 to be held at logic 1, overriding other conditions which can normally stop the motor.

14 The motor will run to reduce the capacitance until the optical position sensor detects that the zero position for the capacitor has been reached. At this point PLAM will change to logic 1 causing latch IC9c and d to be reset to give a logic 1 at IC9.10. This results in IC9.3 no longer being forced to indicate the down direction and IC9.4 no longer forced to logic 1 to override the conditions to stop the motor.

15 In addition to resetting the latch the position sensor input also causes a logic 1 to appear at IC4.6. which, because the motor speed ramp generator is not reset, results in the motor stopping.

Motor control

16 Following the initiate sequence and detection of the capacitor zero position, the motor direction is determined by comparing the selected capacitor position with the current position held by the counter. The selected capacitor position is set by the front panel MANUAL POSITION switch SA, when manual is selected, or the binary input, when auto is selected. When the selected position is greater than the current position IC18.5 is held at logic 1. This produces a logic 0 at IC9.3 to select count up. A logic 0 at IC18.5 sets IC9.3 to logic 1 and count down.

17 When the selected and current positions are coincident IC18.6 changes to logic 1. This results in a logic 0 being fed to IC8.3 and IC8.6 changing to logic 1. If the zero position has been detected during the initiation sequence IC17.9 changes to logic 0. This has the effect, if the motor is not already stopped by a logic 0 at IC17.8, of stopping the motor since the selected position has been reached. The logic 0 at IC6.12 causes the ERROR indication (DLP 2) to be extinguished.

18 A logic 0 on IC8.5 will also stop the motor, providing it is already running. This is generated as described in Para.33 when an end-step is detected, providing the motor direction is not away from the end stop.

19 In addition to the two inputs to IC8a already described, IC8.4 must also be at logic 1 if the motor is to run once the initiate sequence has been completed. This requires at least one of the four inputs to IC4b to be at logic 1.

20 The first of these inputs is the zero position signal to IC4.9. This ensures that the motor will run again even through this signal causes the motor to stop, once the motor speed has been reset to its low starting value, as described in Para 15. This input causes the motor to run until the selected position is achieved without further intervention. A motor stop at the zero position for the ramp to reset is necessary to allow the motor to reverse direction.

21 If the capacitor positioning is not the first to be performed after switch-on and MANUAL operation is selected, the motor will run only when the START push-button, SA, on the front panel is pressed. This allows the new position to be selected and checked using the front panel controls before the motor is driven. Operating the START button applies a logic 1 to IC4.10.

22 If AUTO is selected a logic 1 will be applied to IC4.11 and the motor will run as soon as a new selection is made.

23 The fourth input to IC4.12 is held at logic 1 when the motor is running. This ensures that once the motor is allowed to start by virtue of a logic 1 to any of the other three inputs, it remains running regardless of the state of these inputs until stopped by a input to IC8a.

24 In addition to the conditions described, which allow the motor to run and ultimately produce a logic 1 run signal to IC17.9 and an error signal output on PLA.5, there are further conditions which will prevent the motor running by applying a logic 0 to IC17.8. These are, a logic 1 to the run input at PLA.D or a logic 1 to the aux. supplies on input at PLA.L. Either of these logic 1 inputs will produce a logic 1 at IC7.1 which results in motor running being inhibited.

25 When IC7.1 is at logic 0, a logic 1 at IC7.2 will inhibit running of the motor. If the motor is already stopped IC7.2 will not change to logic 0 until the oscillator speed control ramp is reset generating a logic 1 at IC1.7. When the motor starts IC1.7 will soon change to logic 0 again, but the motor will keep running because the logic 0 at IC4.5 keeps IC7.2 at logic 0. If the zero position is reached, the logic 1 at IC4.6 will override this and force IC7.2 to logic 1 until the ramp is reset once more.

26 Ultimately the motor is controlled by the logic level on IC17.10. When this input is at logic 0 it allows the clock pulses to appear at IC4.11. This output also drives TR7 to apply +24V to the motor windings.

Counter

27 Three four-bit presettable up/down counters, IC13, IC14 and IC16 connected in cascade are used to provide a 12-bit up/down count of the clock output. These counters increment one step up or down for each logic 1 transition of the clock signal applied to IC16.5 or IC16.4 respectively. Count up or down is determined by the A>B output of the comparator at IC18.5. A logic 1 at this point indicates that the data output from the data selector is greater than the data output of the counter so that the counter is required to count up. A logic 0 on IC18.5 results in a down count.

Decoder

28 The decoder provides a 12-bit binary output from the 3 1/2 digit BCD output generated by the front panel push-button MANUAL POSITION switch assembly SA. This 12-bit output corresponds to the manual position selected and is decoded from the BCD output by ten 4-bit full adders. The decoded output is fed to the data selector.

Auto/manual control

29 Auto or manual control is determined by the auto-tune control module. A logic 0 is fed to PLA.9 from this module to select manual control. When this input changes to logic 0 the output of the decoder is selected by the data selector IC28, IC29 and IC31 and IC4.11 changes to logic 0, see Para 21.

30 Auto is selected by the auto-tune control module when this module sends a logic 1 to PLA.9. This results in the data selector accepting the 12-bit frequency count provided by the frequency counter module. A logic 0 run input to PLA.D, from the auto-tune control module initiates the auto-tune sequence, via IC7.1.

End stop detectors

31 The maximum and minimum limits of travel for the tuning capacitor are detected by the end stop detector circuits. These detectors are connected to the output of the counter and recognise the counts corresponding to the position limits for the capacitor. When an end stop is detected the output of the clock generator is inhibited, the front panel END STOP indicator is lit and an end stop indication is fed out from the module on PLA.1.

32 The lower end-stop corresponds to a decimal count of zero and is detected by IC3a, IC3b and IC4a. If all of the inputs to these gates are logic 0 this will produce a logic 1 at each of their outputs which will in turn produce a logic 0 at IC8.10. This results in a logic 1 at IC17.11 which provides an external end stop signal for the auto-tune control module, via PLA.1, and drives TR18 to light the END STOP indicator DLP1.

33 If the motor direction selected is down the input to IC41.1 will be logic 0. This together with the logic 0 at IC41.2 will result in a logic 0 at IC7.10. Since this is one of the inputs to IC8a used to stop the clock driving the waveform generator circuit, see Para 18, the motor will stop once the lower end-stop is reached. Thus, once the lower end-stop has been reached, the motor will only run if the up direction is selected.

34 The upper end-stop corresponds to a decimal count of 3277 and is detected by IC2 and the logic 0 end-stop output from this also produces a logic 1 at IC17.11 to provide both the external signal and cause the END STOP indicator to light. If the motor direction selected is up, a logic 0 at IC7.5 will cause a logic 1 to be at IC7.4 and a logic 0 at the input to IC8.5. So, in a similar manner to the lower end-stop the motor can only be driven in the down direction once the upper end-stop has been reached.

Motor waveform generator

35 The motor requires the two four-phase stepping waveforms shown in Fig D11-1 to drive the capacitor motor in either direction to the required position. These waveforms are derived from the output of a free-running oscillator IC12 using digital switching techniques. The basic frequency of operation of the oscillator is determined by the time constant of R1 and C1 together with an external resistor connected to PLA.E. The operating frequency of this oscillator is also controlled by the action of the ramp generator, see Para 39, when the motor is started.

36 The stepping waveforms are generated from the clock signal using a dual D-Type flip-flop IC42 together with AND-OR-INVERT gate IC39. Direction of travel for the tune capacitor is dictated by the up or down control inputs to IC39. These inputs are complementary and are applied to IC39.1, 5 and IC39.9, 13 respectively. The logic level present at IC42.5 and 9 is transferred to the Q outputs of IC42 when a positive transition of the clock is received on IC42.3 and 11.

Motor drive

37 The four phase stepping waveforms A to D shown in Fig D11-1 are driven by four identical driver stages. Considering phase A when IC43.6 is a logic level 1 driver transistor TR9 is switched on to activate Darlington pair TR18 and TR27. Diode D19 prevents the maximum collector voltage from being exceeded and diode D8 prevents the collector voltage exceeding -0.7V with respect to earth.

Economizer

38 The economizer circuit selects the 10V supply for the motor when it is stationary. This is achieved by the logic 0 on IC43.12 switching off transistors TR7, TR8, and TR4, resulting in Darlington pair TR3 and TR25, mounted on the heat sink, also being switched off so that the 10V supply is applied to the motor via diode D18.

The ramp clock oscillator

39 The ramp clock oscillator comprises a timer IC12 connected as a free running oscillator, the basic frequency of operation is determined by C1, R1 and an external resistor connected to PLA.E.

40 Transistors TR1 and 2 are connected to form a Miller integrator. When TR1 is switched off, the voltage at TR2 collector will fall in a linear manner producing a negative ramp between 9.3 and 6.2V at IC12.5. This ramp has a duration of approximately 220 ms. When TR1 is switched on, IC1.5 restores to 9.3V in approximately 20 ms. Therefore when no error is present the frequency at IC1.3 will be low. When an error is detected the ramp clock the ramp clock oscillator frequency will increase linearly to twice the original frequency in a period of 220 ms. This starts the motor at low speed, hence giving greater motor starting torque.

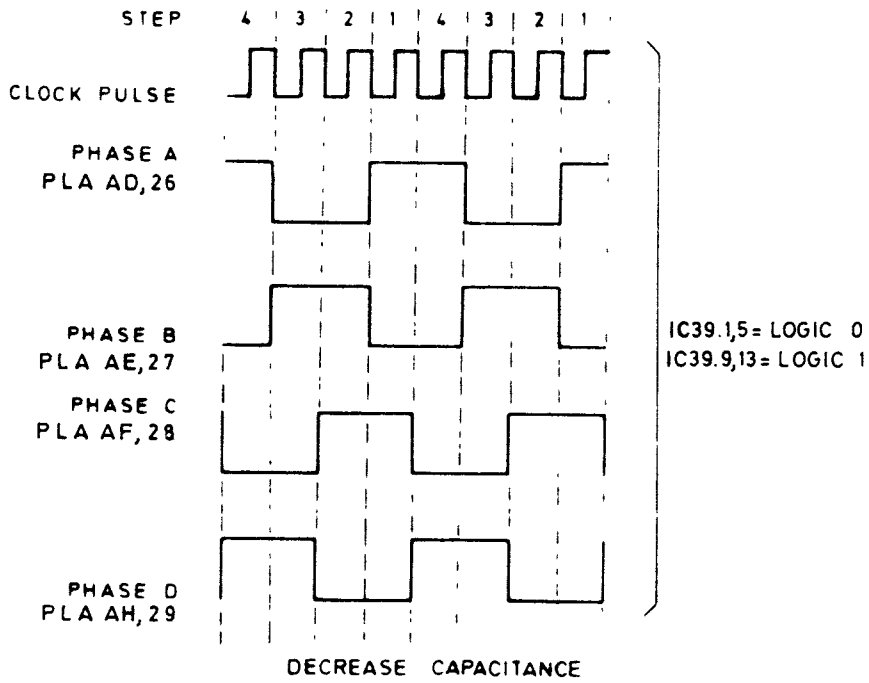
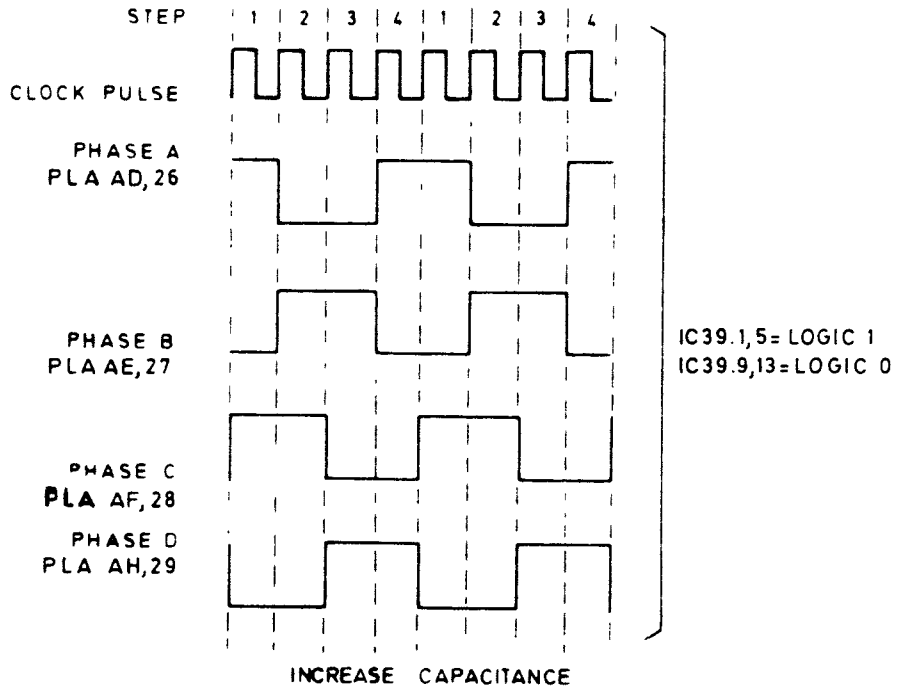
41 Since it takes approximately 20 ms to reset the ramp, a comparator IC1 is used to determine when the ramp voltage has exceeded approximately +9.2V, to prevent the motor restarting before the reset is completed. The comparator output an IC7.3 is used to inhibit starting of the motor circuit until a logic 1 is obtained at this point. This is achieved by IC7d, IC7a and finally IC17c which controls the clock signal to the motor waveform generator.

Shaft encoder potentiometer

42 This potentiometer is driven from the shaft of the stepping motor gearbox and provides an analogue indication of the capacitor setting. A +12V and 0V supply for this potentiometer is provided by this module and fed out, via resistors R5 and R10, to PLA.6 and F respectively. The resulting variable voltage produced by the potentiometer is fed to the auto-tune control module to provide a front panel display of the capacitor setting when selected.

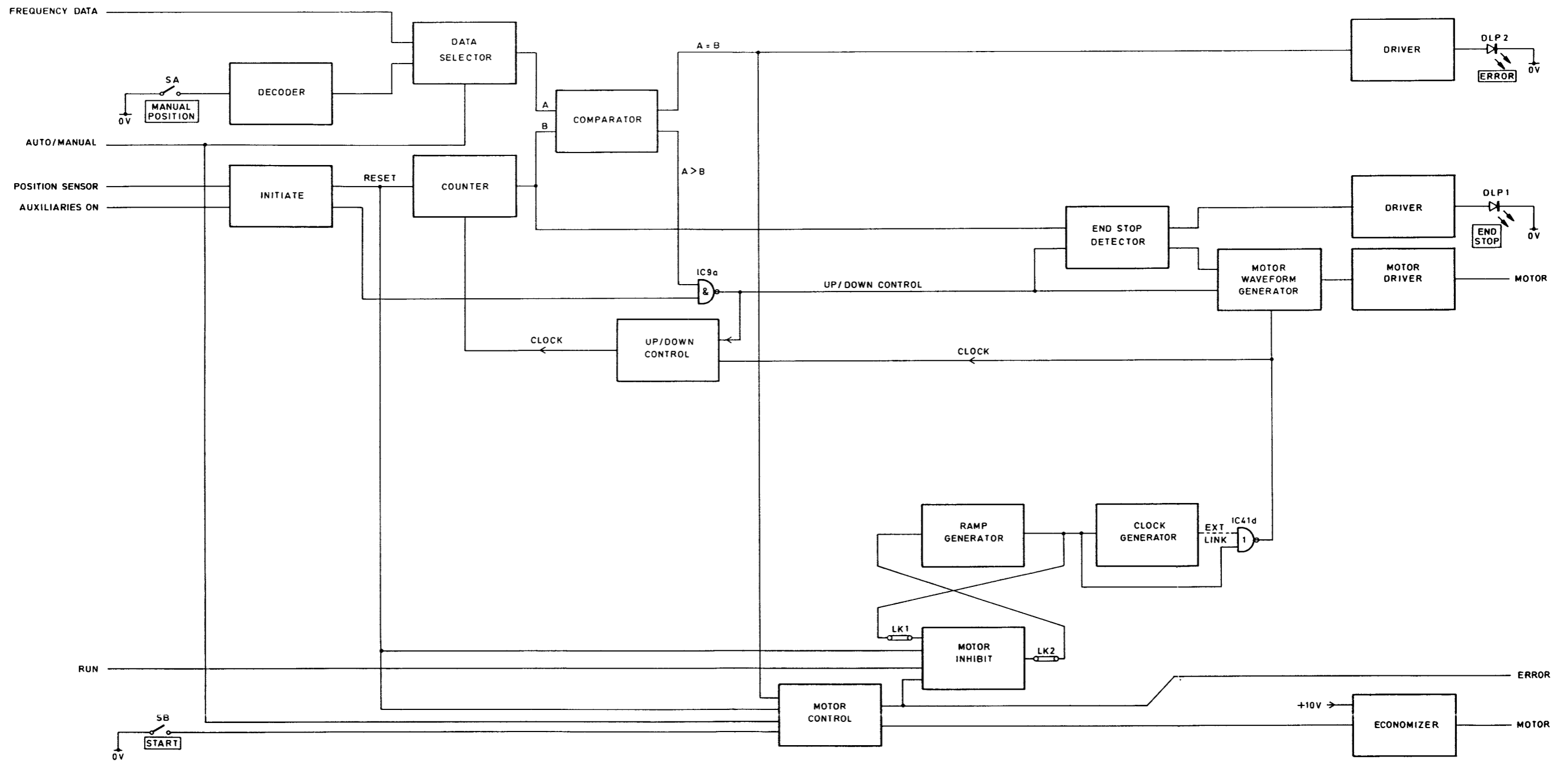
TEST LINKS

43 Various test links are fitted to this board. These links are required for test purposes only and under normal operating conditions all these links should be fitted.



H37-3544G SH 2 (1)

Fig D11-1 Stepping motor waveforms



BASED ON H37-3544G SH1 ISSUE 1
Fig D11-2

Module, servo, 5820-99-751-8058 : block diagram

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Fig D11-2
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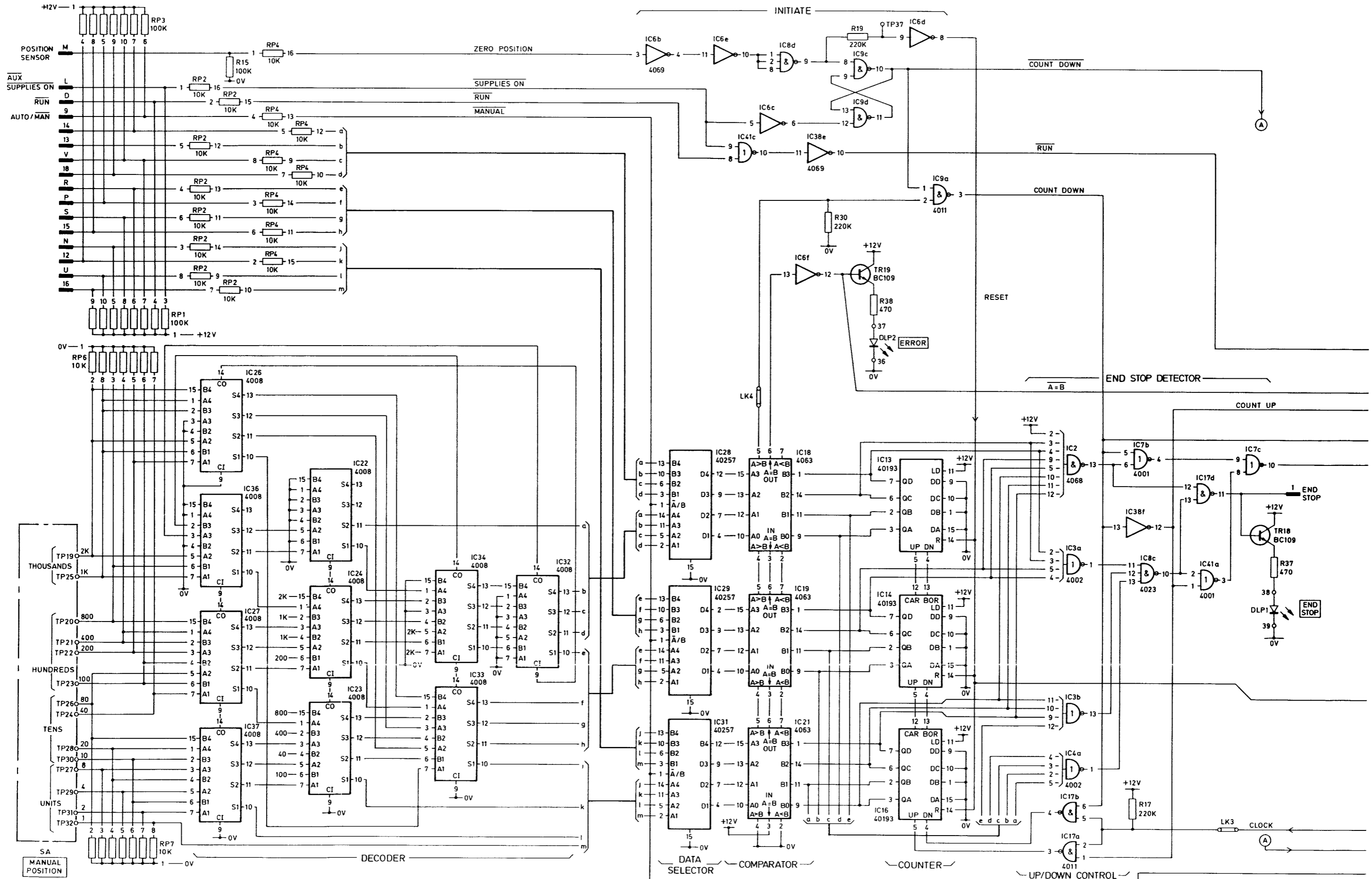


Fig D11-3

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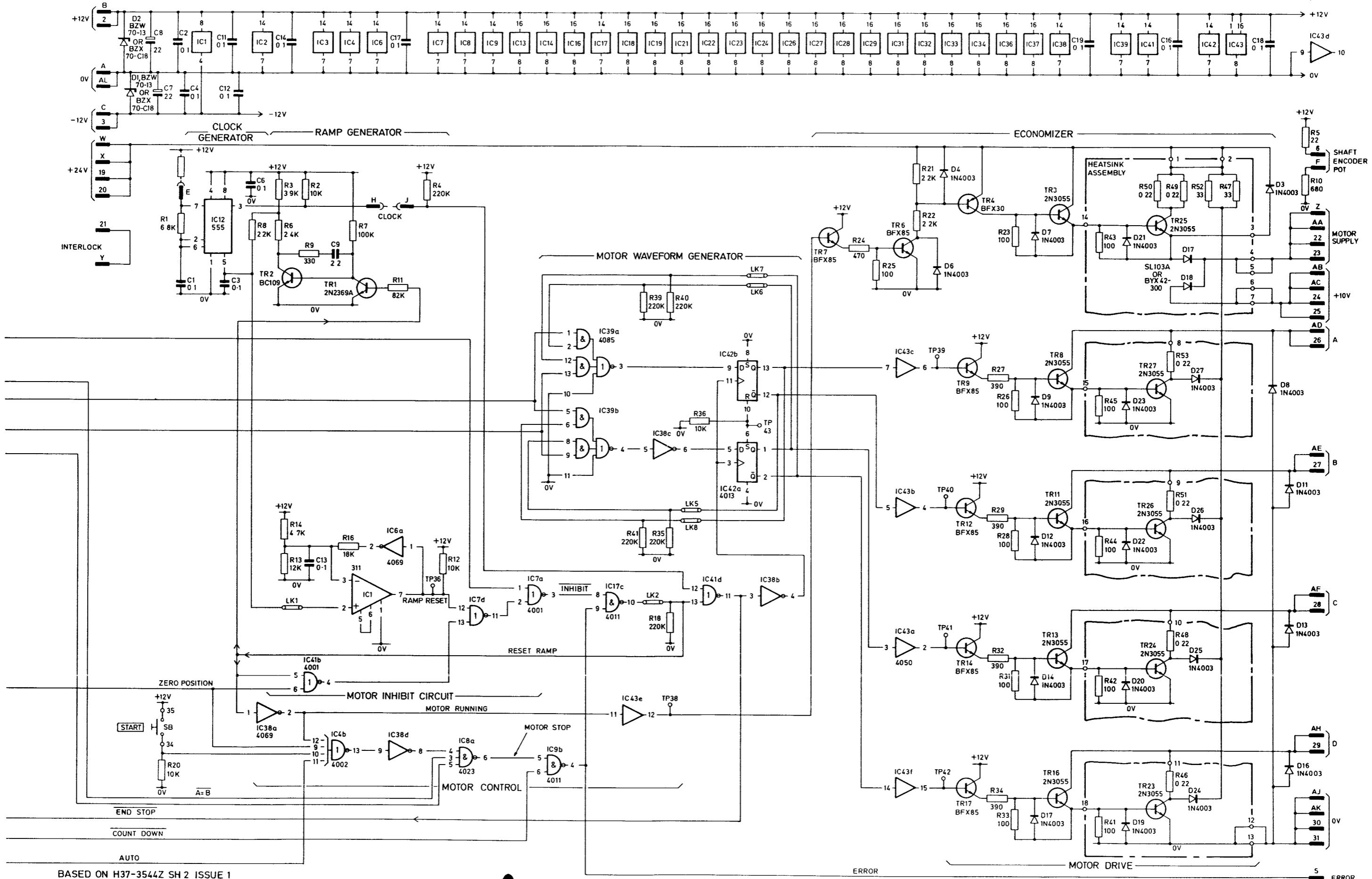
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Module, servo, 5820-99-751-8058 : circuit diagram

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Fig D11-3



BASED ON H37-3544Z SH 2 ISSUE 1

Fig D11-4

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Module, servo, 5820-99-751-8058 : circuit diagram

Fig D11-4

Sub-sect D11

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Sub-section D12MODULE ATTENUATOR (ML16)5820-99-760-2972

CONTENTS

Para

1	Introduction
	Circuit Description
4	Binary coded ladder attenuator
7	Digital to analogue converter
8	Auto control
13	Manual control
14	End stops
> 16	Output level

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INTRODUCTION

1 The module attenuator provides for control of the three rf attenuators which are also mounted on the module. These are:

- 1.1 A 0 to 15.875 dB binary coded ladder attenuator used during tuning and for setting the output level of the amplifier.
- 1.2 A 13 dB power attenuator for use with drives giving an output level of 2 W. This attenuator is wired in circuit by links if required, and
- 1.3 A 10 dB attenuator to reduce the tune tone input level of certain drives.

2 Control signal processing is by means of c-mos digital integrated circuits. For the supply voltage used logic levels are defined as:

- 2.1 Logic level 0 = 0 V to 3.5 V and
- 2.2 Logic level 1 = 8.5 V to 12 V.

3 To protect the integrated circuits against damage that may be caused by withdrawing or replacing the module whilst the supply is on, inputs from PLA are into a 'pull-up' resistor of typically 220 k Ω and a series resistor of typically 10 k Ω .

CIRCUIT DESCRIPTIONBinary coded ladder attenuator

4 Switched attenuators with values of 1/8 dB; $\frac{1}{4}$ dB; $\frac{1}{2}$ dB; 1 dB; 2 dB; 4 dB and 8 dB are connected in series, therefore by programmed selection of these attenuators it is possible to obtain 0 dB to 15.875 dB in 1/8 dB steps.

5 To gain a smooth progression from minimum to maximum values it is necessary to switch in and out the attenuators in a binary progression. This is achieved by clocking the binary coded up-down counters IC1 and IC2. The attenuators are switched by reed relays which have a finite operating time of approximately 1 ms.

6 To avoid a condition where one attenuator section switches out before another switches in, bistables are introduced. Thus, when switching one step, the bistables remember the previous address until a new address has been assumed. The bistables of the unused sections are unlatched to give the final value required. This means that for a short period, total attenuation may increase before the new value is assumed, but can never decrease by more than the nominal step of 1/8 dB.

Digital to analogue converter

7 To give an indication of the amount of attenuation in circuit, and to form part of the manual control circuits, a digital to analogue converter IC3 and IC4 is required, which acts as a conventional adder circuit driver from the outputs of IC1 and IC2.

Auto-control

8 When control of the attenuator is to be determined by the amplifier auto-tune sequence, RLA(12) is held at logic 1. Relays RLS and RLT are energized, RLU and RLV de-energized. During the coarse tune sequence the attenuator is set to a nominal 6 dB until the counter module has measured the selected frequency. This is achieved by changing PLA(15) to logic 0. This input accesses the pre-entry inputs of IC1 and IC2, which have been programmed to give this value of attenuation. When the frequency COUNT COMPLETE command is received, PLA(15) changes to logic 1. The up-down counters are then clocked until the value of attenuation required is reached.

9 The input to the unity gain voltage follower IC22 is fed from a preset potentiometer on the calibration module ML01. This potentiometer provides a reference voltage which determines the amplifier output level when at the tune point. An amplifier IC20, with a gain of two times, receives its input from the pre-amplifier output stage during tuning and from the forward power monitoring amplifier circuit during set output level. The outputs of IC20 and IC22 are fed to an error amplifier IC19 with a gain of 37 times. The output of IC19 is fed to a window detector IC17 and IC18.

10 If the output proportional to rf power is high, then IC19 output will swing positive. This will cause IC17 output to switch from logic 1 to logic 0. The output of IC18 will be unaffected and remain at logic 1. With IC1(9) at logic 0, the inhibiting signal at IC21b(6) is removed and the clock pulses are then free to reach IC1 and IC2 and commence the clocking process.

11 As the attenuation increases, the amplifier rf output will decrease, until a point is reached where IC17 output reverts to logic 1. A logic 1 is presented to IC21b(6) and the up-down counter is no longer clocked. If the output of the amplifier is low then IC18 output changes to logic 0, with IC17 output remaining at logic 1. The output of IC18 is also fed to the up-down input of IC1 and 2. When IC18(9) is at logic 0, IC1 and 2 are programmed to count down and thus remove attenuation.

12 While IC17 or IC18 is detecting an error, PLA(10) changes to logic 0 and the auto-tune control circuits remain in the set output level condition. When tune complete is achieved PLA(F) changes to logic 1, stopping the clock circuits and the attenuator at the value selected.

Manual selected

13 When manual control is selected PLA(12) is held at logic 0, energizing RLU and RLV, de-energizing RLS and RLT. The circuit action is as described for auto control except that the inputs to IC19 are taken from the up-down converter and the wiper of the front panel control RV1.

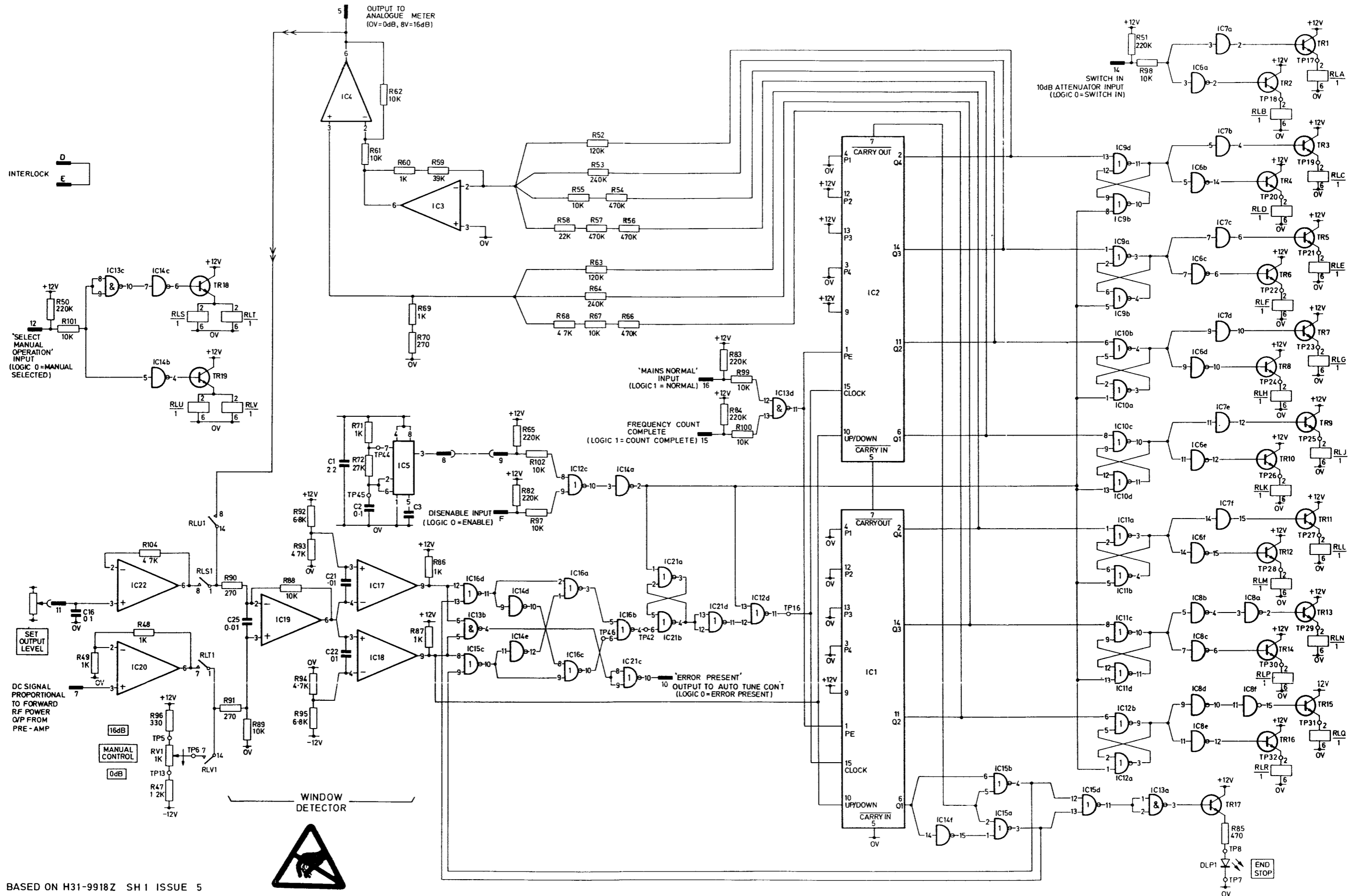
End stops

14 When the attenuator has counted down to 0 dB an inhibiting signal is fed to IC15c(9) to stop further clocking of the up-down counters. IC17 remains active so that the counters are still free to count up if the error amplifiers input conditions change.

15 Similarly when the attenuator has counted up to 15.875 dB an inhibiting signal is fed to IC16d(13) to stop further clocking of the up-down counters. IC18 remains active so that the counters are free to count down if the error amplifier input conditions change. An 'END STOP' light emitting diode DLPI is activated to indicate when this condition has been reached.

> Output level

16 When amplifier power output level at high frequencies (above 25 MHz) becomes too high under auto-tuned conditions, trimmer C20 in the TUNE 10 dB attenuator circuit is adjusted to meet the operational requirements. <



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Fig D12-1

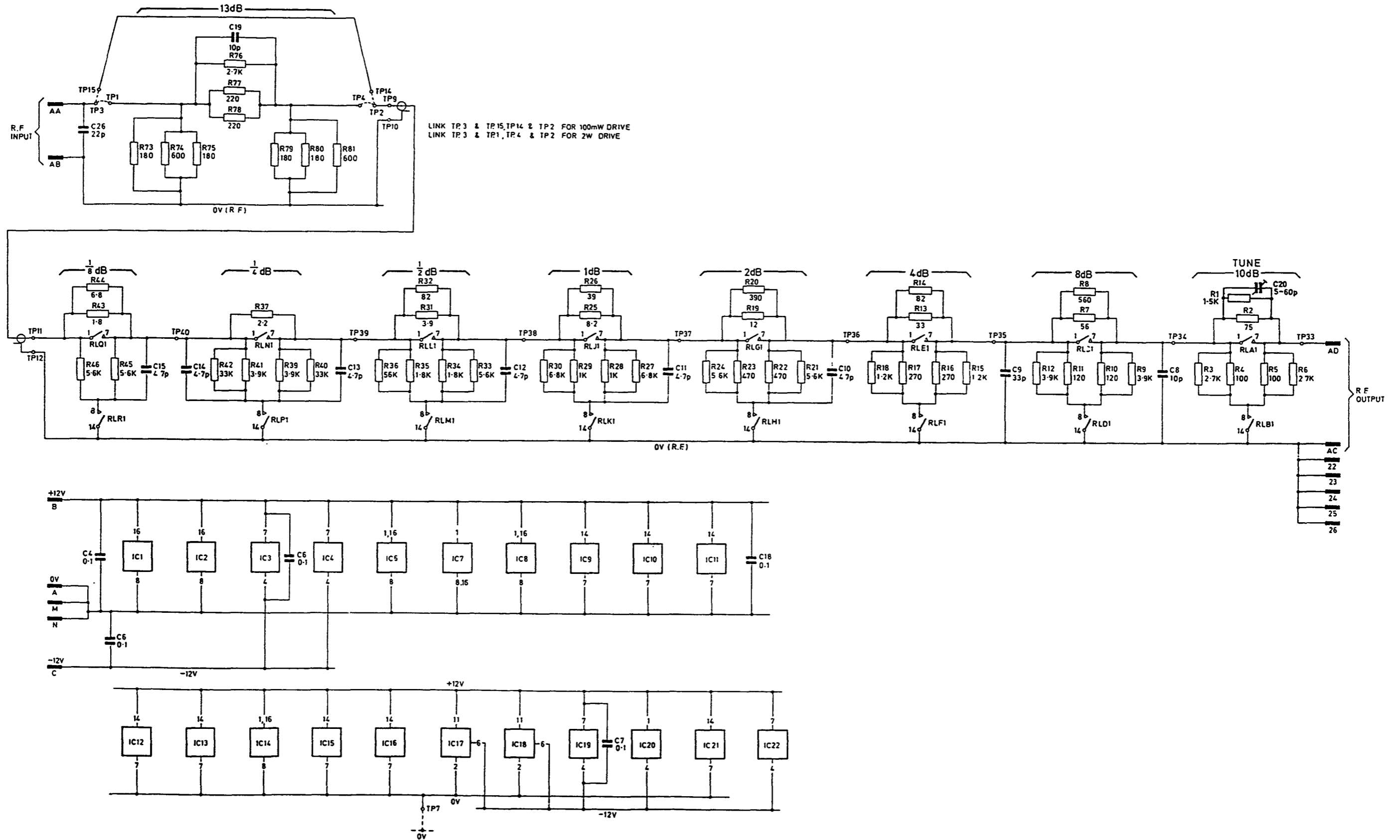
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Module, attenuator, 5820-99-760-2972 : circuit diagram

Fig D12-1

Sub-sect D12



INC MOD RM108/2

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 Fig D12-2

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Module, attenuator, 5820-99-760-2972: circuit diagram

Dec 92 (Amdt 10)

Fig D12-2
 Sub-sect D12
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Subsect D13MODULE FREQUENCY COUNTER (ML17)5820-99-751-8026

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INTRODUCTION

1 The counter module takes a sample of the incoming rf drive signal and from this input determines range and capacitor positioning information for use during the coarse tune stage of the amplifier tuning sequence. This is achieved by counting the incoming frequency, the resulting count being decoded by programmable memories on the board to provide a representation of the range and sub-range required. This output is further decoded to provide positioning information for the tuning and loading capacitors.

2. The following components are controlled from information provided by this module:

- 2.1 Penultimate stage coil.
- 2.2 Final stage tuning coil.
- 2.3 Final stage loading (1) coil.
- 2.4 Final stage loading (2) coil.

- 2.5 Penultimate stage capacitors.
- 2.6 Final stage tuning capacitor.
- 2.7 Final stage centre capacitor.
- 2.8 Final stage loading capacitor.

3 All coils are set by having their taps selected according to the frequency range determined by this module and the range is the only output required. This range, once determined by the frequency counter, will not alter until the frequency is changed and the circuit commanded to perform a recount.

4 Each of the capacitors require different positioning information dependent on their location in the circuit. Also, this module must determine the frequency within a range to provide the correct positioning information. Capacitor positioning information is provided in the form of an analogue voltage with the exception of that for the centre capacitor which is positioned from a digital output. The capacitors are set during the coarse tune stage of the amplifier tuning sequence. These settings may be subsequently modified during later stages of the tune sequence.

5 Control signal processing is by means of both c-mos and TTL digital intergrated circuits. For the c-mos to c-mos circuits the logic levels are defined as:

- 5.1 Logic level 0= 0 to 3.5V and
- 5.2 Logic level 1= 8.5 to 12V.

DESCRIPTION

6 This description must be used in conjunction with the functional diagram shown in Fig D13-1, the circuit diagram shown in Figs D13-2 and D13-3 and the timing and debounce waveforms shown in Figs D13-4 and D13-5.

RF input circuit

7 The rf input is applied to this module on PLA.AA and AC (earth). In order to prevent any unnecessary loading of the input signal the circuit is isolated from the input signal by relay contact RLA1 except when a frequency count is actually taking place. Attenuator R23 is used in conjunction with a nominal 2W r.f. input and is short-circuited by link LK3 when a nominal 100 mW input is used.

8 Non-saturating amplifier and limiter TR7 and TR8 produces a square wave output at the same frequency as the rf input and T29 acts, as a level shifter to provide the required TTL levels.

9 Divide-by-two circuit IC32d is only active during the frequency count period; this is achieved by driving its reset input to IC32.1 from TR11 which is controlled in turn by the count complete signal, see Para 19.

10 The input signal is divided by an additional 25 and 2 by IC33 and IC32b respectively so that the output on IC32.9 represents the rf input frequency divided by 100. This signal is converted to 0 and +12V c-mos levels by IC14a.

11 Providing that the rf input signal is of sufficient amplitude to cause these divider circuits to switch a square-wave output will be produced at IC9.15. If this output exceeds 16 kHz nominal then the charge on C12 is reduced sufficiently, via D3 and D4, to ensure that the input to IC9e is a logic 0. Conversely, if no transitions occur at IC9.15, C12 is charged via R13 to give a logic 1. This level on C12 is used to control the front panel COUNT SAMPLE PRESENT indicator, DLP1, via IC9d and TR3, and the debounce circuit.

Debounce

12 This circuit provides debounce for the count sample present signal on TP3. Typical waveforms and the sequence of operation for this circuit are shown in Fig D13-5. The waveforms for various points in the circuit, annotated by letters, and the sequence of events, numbered, associated with a decrease in level to below the operating range of the equipment with a subsequent return to the operating frequency are shown.

13 When the rf input is applied to the circuit it may be subject to switch bounce and the output of this circuit may alternate between logic 0 and 1, waveform A event 1. The first logic 0 output from this circuit causes the output of the debounce circuit to change to logic 1, waveform J event 6. This output is maintained for a minimum of four positive transitions of the 125 Hz clock, waveform C event 7.

14 With the return of the input signal to within the operating range of the equipment further changes in logic level on TP3 could occur, waveform A event 10. The first logic 0 transition causes IC11.2 to change to logic 0, waveform G event 13. This results in IC44.2 reverting to logic 0 on the fourth positive transition of the 125 Hz clock, waveform C event 15. The resulting 24-32 ms delay prevents the output of the debounce circuit changing to logic 0 before this time has lapsed, allowing the level on TP3 to settle, waveform J event 12.

Count initiation

15 To enable associated drive equipments to be compatible with the amplifier auto-tune system, switch SPA in the counter module allows the appropriate delays to be set. The types of drive able to work with the amplifier are as follows:

- 15.1 Retune by action switch-output muted during retune. Action arising from a tune command pulse having to be delayed until the drive input is restored and also delayed for a further 24 to 32 ms to allow counter bounce disturbances to cease.
- 15.2 Retune by action switch-output not muted during retune. Action arising from a tune command pulse having to be delayed by up to 1.5 seconds (selectable) to allow the drive to retune.
- 15.3 Retune by decade switches-output muted during retune. Action arising from a tune command pulse having to be delayed up to 1.5 seconds (selectable) to allow further decade switches to be operated without the amplifier retuning after each decade switch operation. Each switch operation will cause a tune command pulse which will retrigger the delay. At the end of the delay, after the last switch is operated, the timing sequence will start if the drive is no longer muted, i.e. the 24 to 32 ms antibounce delay elapsed. If at the end of the delay the drive is still muted then the tuning sequence will only start when the rf appears plus the 24 to 32 ms delay.

15.4 Retune by decade switches-output not muted during retune. Each tune command pulse will not be acted upon for a period of up to 1.5 seconds (selectable) and will retrigger the delay.

16 When a type of drive is used as specified in Para 15, switch SPA is set to position 1. Any other type of drive will require SPA to be set to give an appropriate delay as shown in Table 1.

17 The system assumes that with no action switch fitted, during a retune operation the decade switches will change in rapid succession, less than 1.536 ms interval between switch operations. This makes a delay period mandatory to ensure that each switch operated will not cause the amplifier to retune. Only when the delay period has elapsed, after operation of the last decade switch, will the tune sequence be initiated.

18 With an action switch fitted, when a retune is necessary, the decade switches will be set to the required frequency and the action switch operated.

19 The count is initiated upon receipt of a logic 1 pulse to the count command input on PLA.20. This initially sets the latches IC11b and IC11c and resets the shift register IC38/IC44d and D-type bistable IC6a. The resulting logic 1 on IC11.10 drives the following circuits:

- 19.1 Provides a logic 0 output on PLA.13 via IC22e for the rf attenuator module.
- 19.2 Extinguishes the front panel COUNT COMPLETE indicator DLP.2 via IC22d and TR4.
- 19.3 Removes the logic 1 reset input to D-type bistable IC32a via TR11.
- 19.4 Energizes RLA via TR6 to allow relay contact RLA1 to apply the rf input.

20 The logic 1 on IC11.9 is applied to the inputs of IC38 which together with IC44a forms a 12-bit shift register with 8-taps. This logic 1 input is shifted through the register by the 7.8125 Hz clock from IC6.13. Switch SPA allows the shift register output tap to be selected to provide a time delay of between 128 and 1536 ms, see Para 15. The output of the shift register is inverted by IC22d and, providing the count sample present has been detected, causes IC8.11 to change to logic 1. On the next rising edge of the 2 kHz clock, fed to IC6.3, the output on IC6.1 changes to logic 1. This output is fed back to IC3d where, together with the logic 1 produced when IC11b was set, causes IC3.11 to change to logic 0. After inversion by IC22c this resets IC11b and thus, as a result of the action of IC3d, causes its own reset signal to be removed. A new count sequence can now be initiated upon receipt of a second logic 1 count command. The logic 0 output on IC11.9 is also fed to the counting circuits to indicate that the count initiation delay is completed and that these circuit are activated.

Waveform generation

21 Crystal controlled oscillator X1 provides a 1.024 MHz TTL compatible output which is used to derive all of the clock and sequencing waveforms for the module.

22 The oscillator output is taken via a test link LK7 to a divide-by-four circuit provided by IC33. After conversion to c-mos logic levels by IC14f the resulting 256 kHz output is fed to a 14-stage binary counter IC2. This counter provides the following control and timing waveforms:

- 22.1 2 kHz from Q7.
- 22.2 500 Hz from Q9.
- 22.3 250 Hz from Q10.
- 22.4 125 Hz from Q11
- 22.5 15.625 Hz from Q14

The 15.625 Hz output is taken to a divide-by-four circuit, IC4. This circuit is inhibited until a logic 0 is received on IC4.4. From the count initiation delay.

Sequence control

23 Decade counter IC7 acts as a sequence controller generating five 0.25 ms pulses at 0.25 ms intervals from alternate outputs. These pulses are used in the output circuit of this module to set the output latches, see Para 37. Details of the timing waveforms and sequence controller output are shown on the timing diagram, see Fig D13-4.

24 The sequence controller IC7 is reset by the logic 0 count command output on IC11.9 so that the output on IC7.11 is also logic 0. This output is fed to the reset input of the first bistable of the divide-by-four circuit on IC4.10. The first rising edge output from IC2.15, after the count indication delay, will produce a logic 1 at IC4.1. This logic 1 is fed to IC3.5 and allows the input rf divide-by-one-hundred signal on IC3.6 to be applied to IC19.1 via IC18c.

25 The logic 1 on IC4.1 also sets IC11d so that a logic 1 is fed to IC3.2, since IC3.1 is now at logic 0 the input to IC7.13 will remain at logic 1. Both the sequence controller IC7 and the EPROM memory devices IC28, IC29 and IC31 are therefore not enabled at this stage.

26 After 16 ms the second subsequent rising from IC2.15 will have occurred and caused IC4.1 to return to logic 0. This will result in IC3.4 returning to logic 1 so that a 16 ms burst of the input rf divided-by-one-hundred will have been fed to IC18c.

27 The 14-bit binary counter formed by IC19 together with IC21 is operated at 5V to allow easy interfacing with the EPROM devices. This conversion is provided by IC18c. The counter is clocked by this 16 ms burst of rf divide-by-one-hundred pulses. Once IC4.1 returns to logic 0 the output of the counter will be a binary representation of the r.f. input frequency produced by counting the waveform over a measured 16 ms interval.

28 When IC4.1 returns to logic 0 the resulting logic 1 input to IC3.1 causes IC3.3 to change to logic 0, since latch IC11d will still have a logic 1 at IC11.1. Sequence controller IC7 together with the EPROM devices will now be enabled.

29 Four alternate outputs of the sequence controller IC7 are used to sequentially latch data into the output stage circuits. The fifth alternate output is used to signify count complete. This output, on IC7.11, resets IC11c to light the COUNT COMPLETE indicator DLP1 and prevents the sequence controller recycling by resetting IC11d. This applies a logic 1 to IC7.13, IC28, 18 and 20, IC29.18 and 20 and IC31.18 and 20 via IC3a. The output on IC7.11 also prevents a second 16 ms gating pulse being generated by resetting IC4b.

Decoding

30 The EPROM memory devices IC28, IC29 and IC31 act as decoders for the output of the counter. These circuits are enabled by the output on IC3d. Each memory address of IC29 and IC31 contains pre-programmed range and sub-range information. The receipt of a 12-bit address code, from the counter, together with a logic 0 at the enable input causes this stored information to be fed to the output pins.

31 Two stages of decoding are employed. The first state is formed by two of the EPROM memory devices IC29 and IC31 and provides 14-bits of positioning information as follows; 8-bits from IC29 and 6-bits from IC32. The 8-bits from IC29 contain 4-bits of range information and 4-bits of sub-range information for the second level decoder IC28 to form part of the 12-bit address code for this circuit. In addition to this function the 4-bits of range information from this output (D4 to D7) are also fed to the 8-bit register IC27, see Para 33. The 6-bit output of IC31 contain 4-bits of centre capacitor position information, fed to IC27 and a further 2-bits of sub-range information, for the second level decoder IC28.

32 Second level decoder IC28 provides 8-bits of capacitor position data, from a 12-bit address input, made up from the 10-bit output of the first decoder together with two timing outputs (Q9 and Q10) from the divider IC2. This output is fed to four 8-bit registers IC16, IC34, IC36 and IC37 which together with IC27 drive the output circuits of the module. The two timing inputs to IC28 select four passive outputs from the memory which are then latched into the appropriate 8-bit register.

33 The 8-bit register IC27 latches two 4-bit inputs from the first level decoder. From this input it provides a 4-bit range select output (1Q to 4Q) together with a 4-bit capacitor position output (5Q to 8Q) fed via inverters to the servo module for the centre capacitor. A further eight-bits of capacitor position information for this module are latched into IC16 when the appropriate output appears at the second level decoder IC28.

34 The range select output from IC27 is fed to a BCD to decimal decoder IC26. This decoder provides nine range select outputs for the range selection module which in turn controls the pen. stage and final stage selection circuits.

Output circuits

35 The output circuits are divided into four discrete areas each selected in turn by the four 0.25 ms pulses from the sequence controller, see Para 23. These areas provide position data for the following capacitors; final stage centre capacitor, final stage tuning capacitor, final stage loading capacitor and pen-stage capacitor. The selections are made to coincide with the appropriate data being available at IC28 output. This is controlled by two inputs to IC28.19 and IC28.21.

36 The four timing pulses are applied to the clock inputs of 8-input registers IC16, IC27, IC34, IC36 and IC37. Upon receipt of a positive transition of a clock pulse at any of these latches the data applied to the input is transferred to the output.

37 The centre capacitor servo requires 12-bits of position data, 8 of these bits are provided by 8-bit register IC16, the remaining 4-bits being provided by IC27, see Para 33.

38 The outputs of the remaining three output latches IC34, IC36 and IC37 are fed to digital-to-analogue converters IC41, IC42 and IC43 respectively. The analogue levels provided by these converters is determined by the output of the second level decoder IC28 and used to set the rf tuning capacitors. These outputs are taken via three current-to-voltage converters IC39.

Power supplies

39 A +12V and -12V power supply is fed to the module. The +12V input is used to supply the +5V regulator, most of the c-mos integrated circuits, the output amplifiers (IC39) and the rf input amplifier. The -12V supply is used by the digital-to-analogue converters and the output amplifiers.

40 The 5V stabilizer comprises a voltage regulator IC1 together with bypass transistor TR2 and is enabled by a logic 0 AIR ON input to PLA.J. The resulting 5V supply is used to power the TTL integrated circuits, the EPROM devices and some of the c-mos integrated circuits.

TABLE 1 COUNT COMMAND DELAYS

SA Position	Delay (ms)
1	128 to 256
2	256 to 384
3	384 to 512
4	512 to 640
5	640 to 768
6	896 to 1024
7	1162 to 1280
8	1408 to 1530

TABLE 2 FREQUENCY RANGE DIVISIONS

Range	Frequency
1	2-2.3 MHz
2	2.3-3.0 MHz
3	3.0-4.5 MHz
4	4.5-6.7 MHz
5	6.7-10.0 MHz
6	10.0-15.0 MHz
7	15.0-20.0 MHz
8	20.0-25.0 MHz
9	25.0-30.0 MHz

OPERATION CHECK

- 41 The correct operation of this module can be checked in situ as follows:
- 41.1 Connect the module to the extension unit and insert the extension unit in the frequency counter position in the control frame.
- 41.2 Set the auto-tune sequence switch on the auto-tune module to COARSE TUNE.
- 41.3 Set the drive frequency to 2.000 MHz.
- 41.4 Retune the amplifier to this frequency using the auto-tune sequence as detailed in Sub-sect B2. Ensure that during this retune sequence the COUNT COMPLETE indication extinguishes briefly before lighting again.
- 41.5 Using a digital voltmeter check the logic and signal levels of the following edge connector pins.

Edge connector	Output	Edge connector	Output
19	Logic 0	L	Logic 0
14	Logic 0	H	Logic 1
16	Logic 0	9	Logic 1
18	Logic 0	M	Logic 0
17	Logic 0	11	Logic 1
15	Logic 0	P	Logic 0
12	Logic 0	K	Logic 1
Y	Logic 0	8	Logic 0
X	Logic 0	F	Logic 1
10	Logic 1	AF	6.645V \pm 80 mV
R	Logic 0	AN	7.032V \pm 80 mV
N	Logic 0	AJ	5.780V \pm 80 mV

- 41.6 Set the drive frequency to 25.005 MHz.
- 41.7 Retune the amplifier to this frequency as detailed in 41.4 above.
- 41.8 Using a digital voltmeter recheck the logic and signal levels of the following edge connector pins:

Edge connector	Output	Edge connector	Output
19	Logic 1	L	Logic 1
14	Logic 1	H	Logic 1
16	Logic 1	9	Logic 0
18	Logic 1	M	Logic 0
17	Logic 1	11	Logic 1
15	Logic 1	P	Logic 1
12	Logic 1	K	Logic 0
Y	Logic 1	8	Logic 0
X	Logic 0	F	Logic 0
10	Logic 0	AF	1.980V \pm 80 mV
R	Logic 0	AH	1.830V \pm 80 mV
N	Logic 0	AJ	1.670V \pm 80 mV

42 If the digital output levels are all correct but the analogue voltage levels at edge connectors AF, AH and AJ are outside the indicated limits, they should be reset as follows:

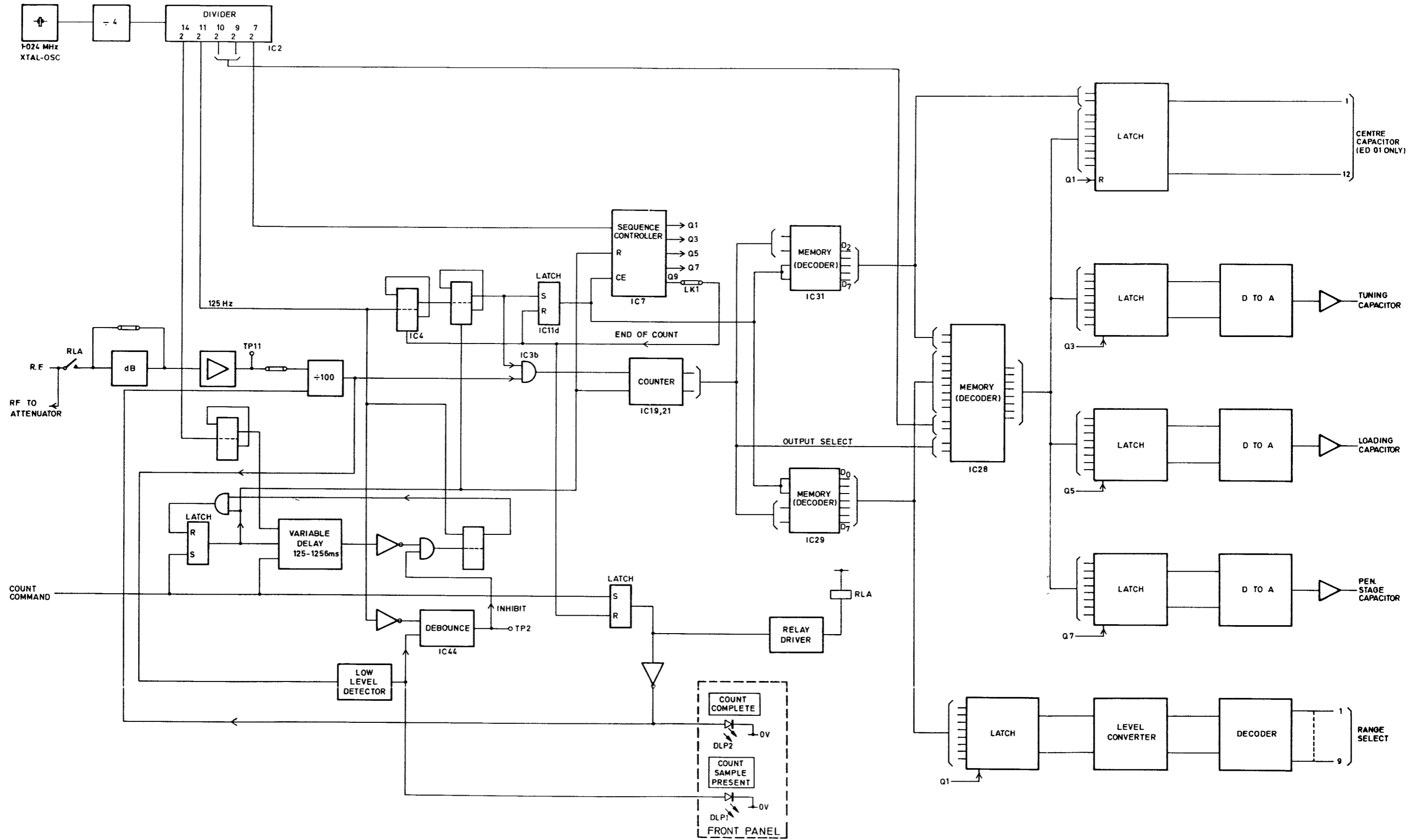
Set the drive frequency to 2.000 MHz.

Retune the amplifier to this frequency as detailed in Para 41.4.

Using a digital voltmeter measure the voltage levels at the following edge connectors and adjust the appropriate potentiometer to achieve the indicated voltage levels:

Edge corrector	Potentiometer	Voltage
AF	RV2	6.645V \pm 5 mV
AH	RV3	7.032V \pm 5 mV
AJ	RV4	5.780V \pm 5 mV

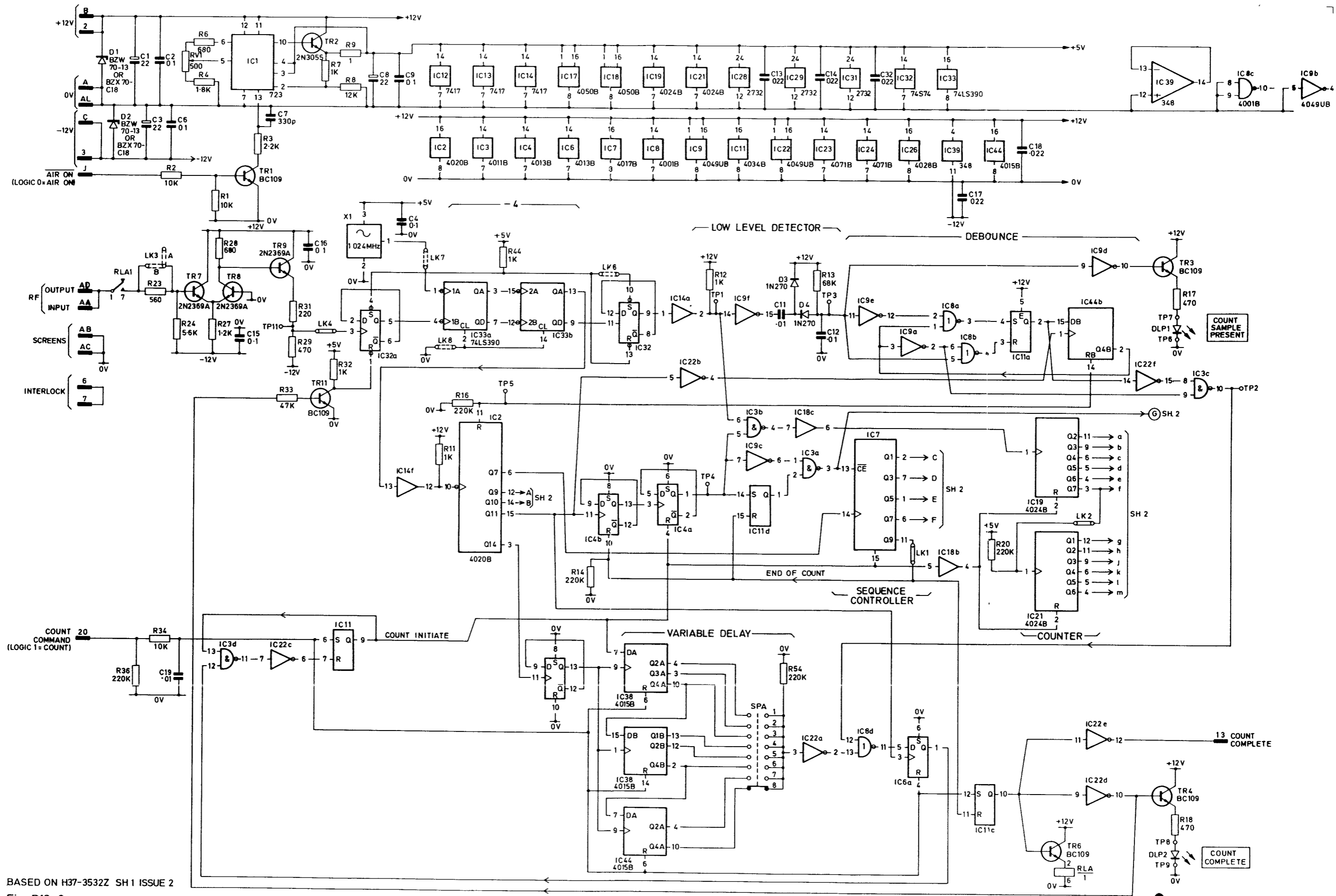
43 Remove the module from the extension unit. Replace the module in the control frame and refit the cover over the control frame.



BASED ON H37-3532G SH1 ISSUE 1

Fig D13-1

Module, frequency counter, 5820-99-751-8026: functional diagram



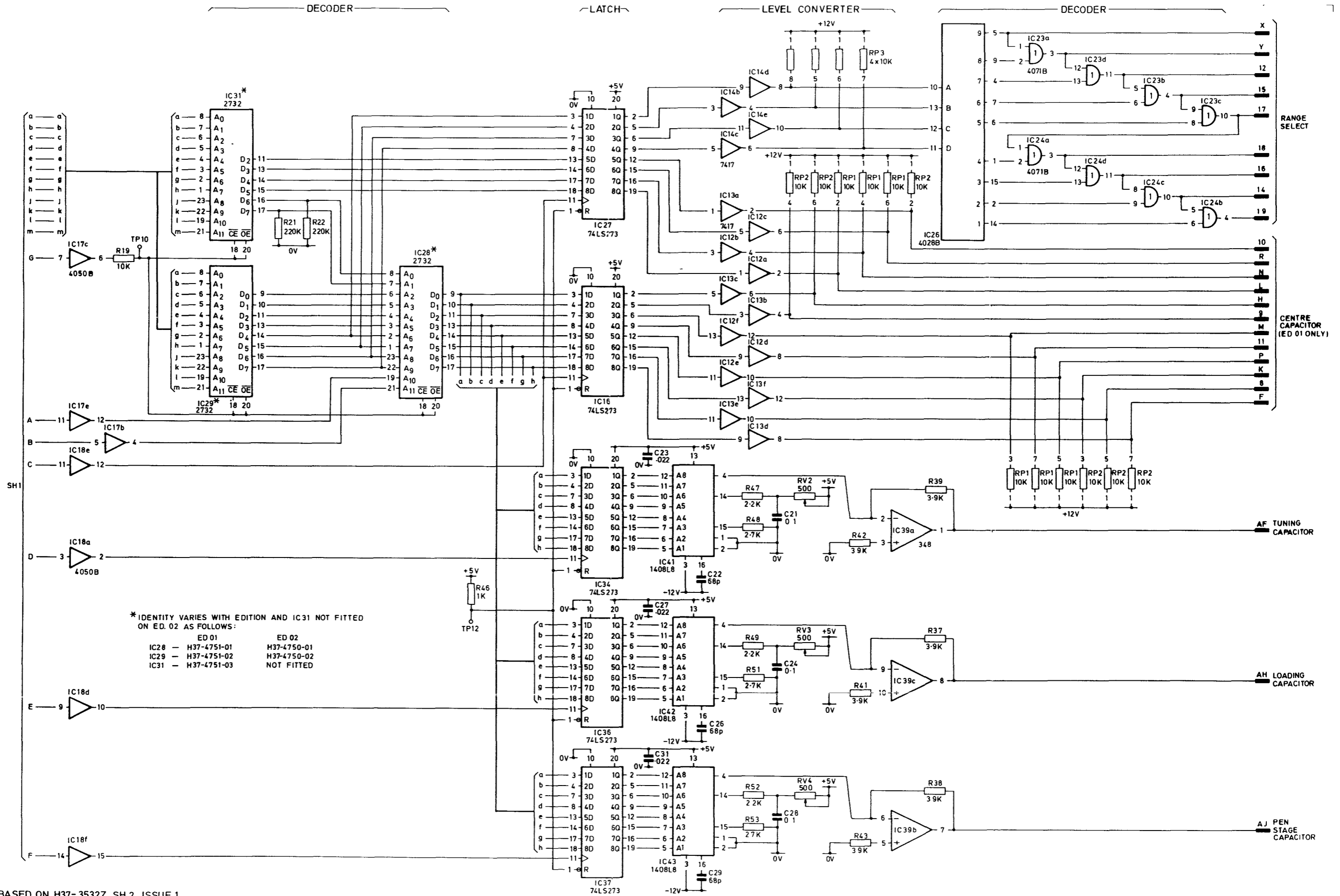
BASED ON H37-3532Z SH1 ISSUE 2
Fig D13-2

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Module, frequency counter, 5820-99-751-8026 : circuit diagram





* IDENTITY VARIES WITH EDITION AND IC31 NOT FITTED ON ED. 02 AS FOLLOWS:

	ED 01	ED 02
IC28	H37-4751-01	H37-4750-01
IC29	H37-4751-02	H37-4750-02
IC31	H37-4751-03	NOT FITTED

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Fig D13-3

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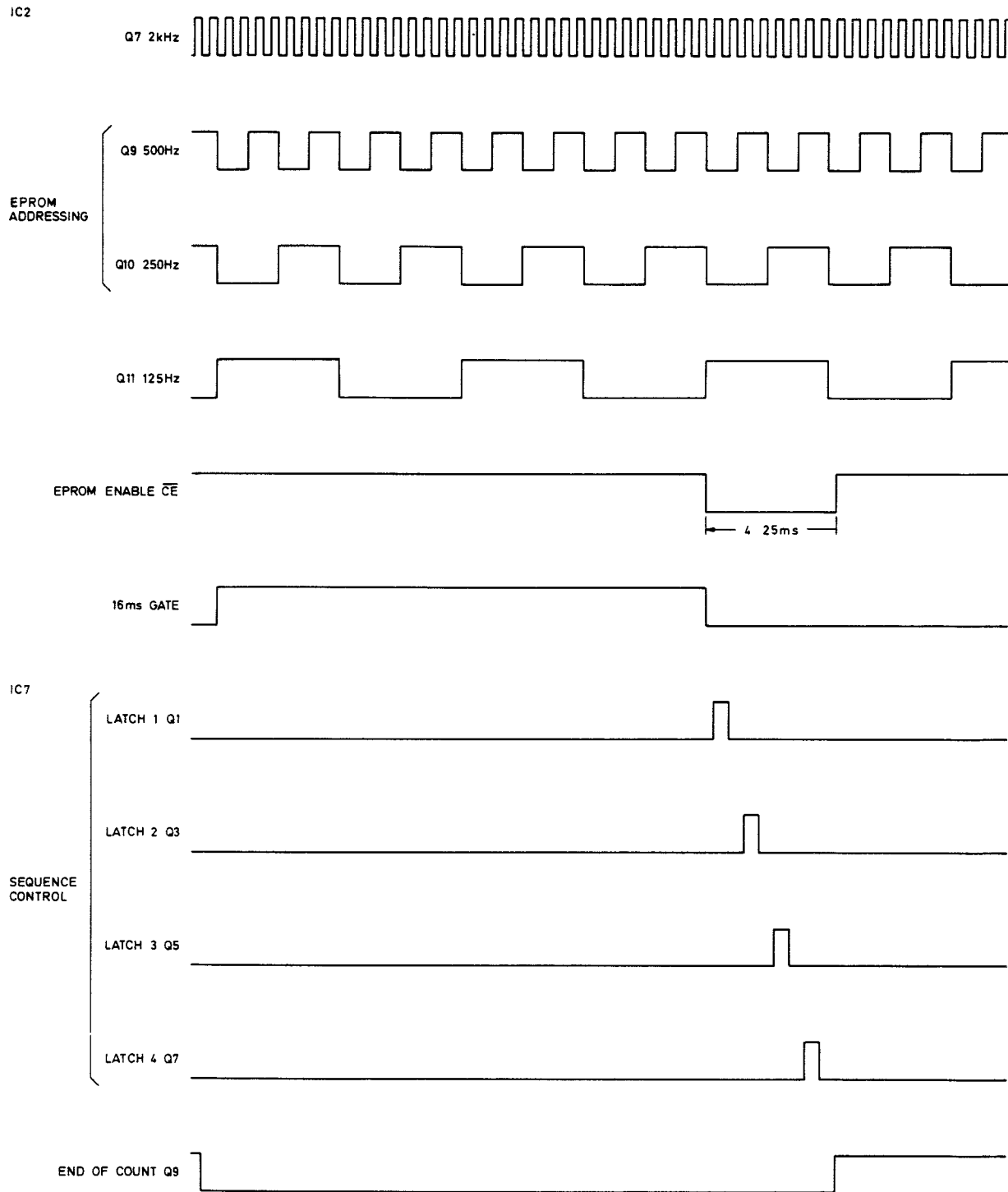
DIGITAL TO ANALOGUE CONVERTER
Module, frequency counter, 5820-99-751-8026: circuit diagram



Fig D13-3

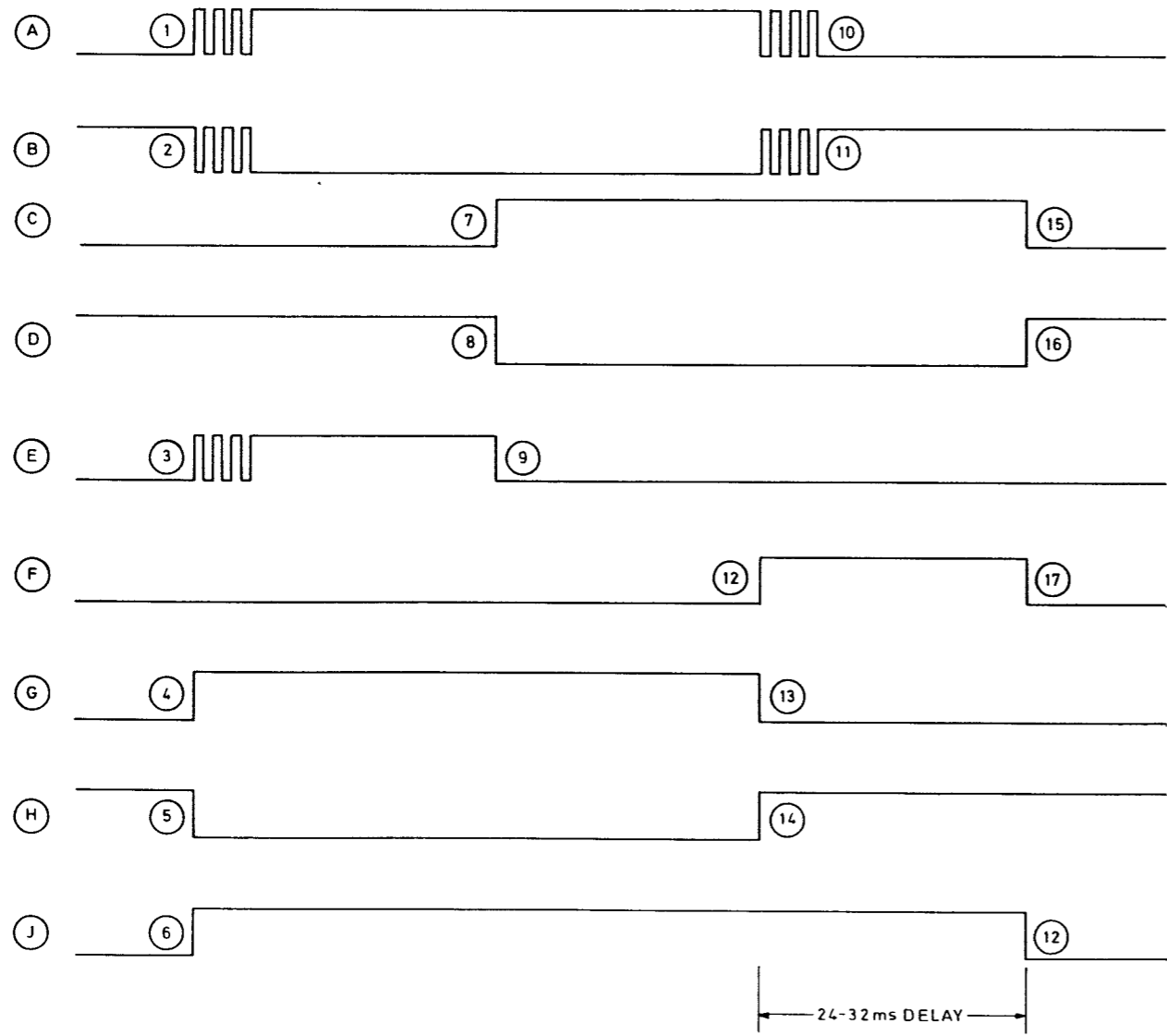
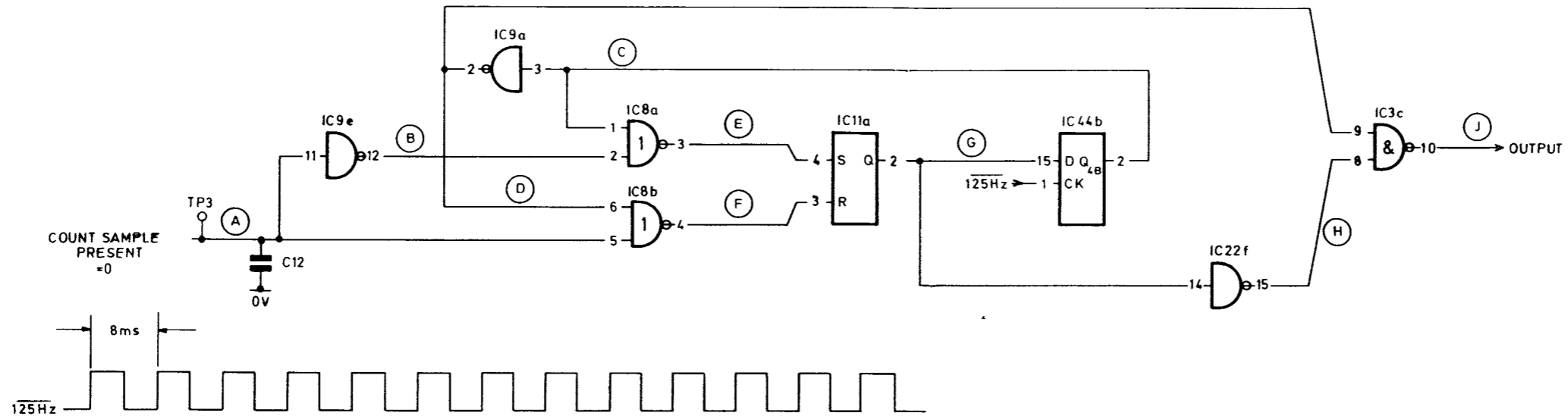
Sub-sect D13

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BASED ON H37-3532G SH 2
ISSUE 1

Fig D13-4 Module, frequency counter, 5820-99-751-8026: timing diagram



BASED ON H37-3532G SH 3 ISSUE 1
Fig D13-5

Module, frequency counter, 5820-99-751-8026 : de-bounce circuit diagram and waveforms

Sub-section D14POWER SUPPLY (UNIT 05)5820-99-760-2960

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3	General
5	+12 V supply
8	+15 V crowbar
9	-12 V supply and -15 V crowbar
10	'Control supplies normal' circuit
12	+12 V prove circuit
13	-12 V prove circuit
14	Mains prove circuit
15	Board interlock

Fig

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D14-2	Panel, electronic circuit (± 12 V supply) 5820-99-760-2959: circuit diagram	7

INTRODUCTION

1 The unit provides dual outputs of +12 V and -12 V each protected by current limiting and overvoltage crowbar circuits. In addition logic prove circuits are provided for interfacing with the associated amplifier control system.

2 The unit comprises chassis mounted components and a plug-in printed board assembly (05 ML01), identity 5820-99-760-2959. All external connections to the unit are made via a single tagstrip TS1.

DESCRIPTIONGeneral

3 Both 12 V outputs are derived from a single mains transformer. Integrated circuit regulators mounted on the printed circuit board are used to regulate the supplies in association with power transistors mounted externally. The crowbar and logic prove circuits are also on the printed board. The logic prove circuits are as follows:

- 3.1 +12 V supply is in excess of +10 V.
- 3.2 -12 V supply is in excess of -10 V.

3.3 The mains supply is in excess of -10 % of nominal.

3.4 The external interlock circuit is complete.

4 Two control outputs are provided, both indicating that the control supplies are 'normal', ie all logic prove circuits proven. One of the control outputs provides an energizing source for the contactor drivers and the other a signal to the associated amplifier control circuits.

+12 V supply

5 An unregulated dc supply is fed from bridge X1 to PLA(4) of the printed board and to the collectors of power transistors TR1 to TR3.

6 A reference voltage of 7.15 V is derived within IC1 and is made available at IC1(4). This is fed to the non-inverting input of an error amplifier at IC1(3). The +12 V output voltage is fed to PLA(21) and a proportion of this, available at the wiper of RV1, is fed to the inverting input of the error amplifier at IC1(2). This potentiometer enables the output voltage to be varied between +10 V and +22 V.

7 Current limiting is achieved by developing a voltage, proportional to the current demand, across resistors connected to the emitters of the series power transistors. This voltage is fed between the current sense input at IC1(1) and the current limit input at IC1(10) via potential divider R3/R4. The current limit is set to operate just in excess of 4 A.

+15 V crowbar

8 The output of the +12 V supply is fed to a potential divider chain R9, RV2, R10. The voltage at the wiper of RV2 is fed to the base of TR1. The emitter is at a reference voltage of +6.2 V set by zener diode D3. When the +12 V is below the 'crowbar' voltage TR1 is cut-off. Therefore TR2, TR3 and TR4 are off. If the +12 V rail rises sufficiently, a point is reached where TR1 is switched on. Thus TR2, TR3 and TR4 switch on. As TR1 turns on, positive feedback is applied via D4/R14 to ensure a 'snap-action'. The emitter of TR4 feeds the gate of a thyristor CSR1, external to the board. The thyristor 'fires' on creating a low resistance path across the +12 V supply and causing the fuse to blow. RV2 enables the crowbar voltage to be set between approximately +12 V and +19 V and is normally set at +15 V.

-12 V supply and -15 V crowbar

9 The circuits for the -12 V supply and -15 V crowbar are similar in operation to those described in paras 6 to 9. The current limit of the -12 V supply is set to operate at 2.5 A.

'Control supplies normal' circuit

10 For the control circuits of the associated amplifier to operate normally TR11 must be biased on, causing TR12 and TR13 to be on and TR14 to be off. TR12 provides the +12 V energizing supply for contactor drivers via PLA(29). With TR14 off, PLA(24) is at logic level 1, providing the 'control supplies normal' signal to the associated control circuits, ie with TR14 on, the associated amplifier run-up sequence is inhibited.

11 To turn TR11 on, clamp transistors TR19, TR10, TR15 and TR16 must all be off. As soon as all of these are off, C7 is free to charge via R36 and R35. When the zener voltage of D9 has been overcome then TR11 switches on. The nominal time delay before TR11 conducts is 35 ms. If one of the clamp transistors should subsequently turn on, C7 discharges rapidly via R36.

+12 V Prove circuit

12 The positive supply is proved to be in excess of +10 V by the circuit associated with TR9 and TR10. When the supply first establishes, TR9 is off as the zener voltage of D7 has not been overcome and therefore TR10 is on. When the supply voltage has risen sufficiently TR9 turns on and TR10 turns off, removing the clamp on C7.

-12 V Prove circuit

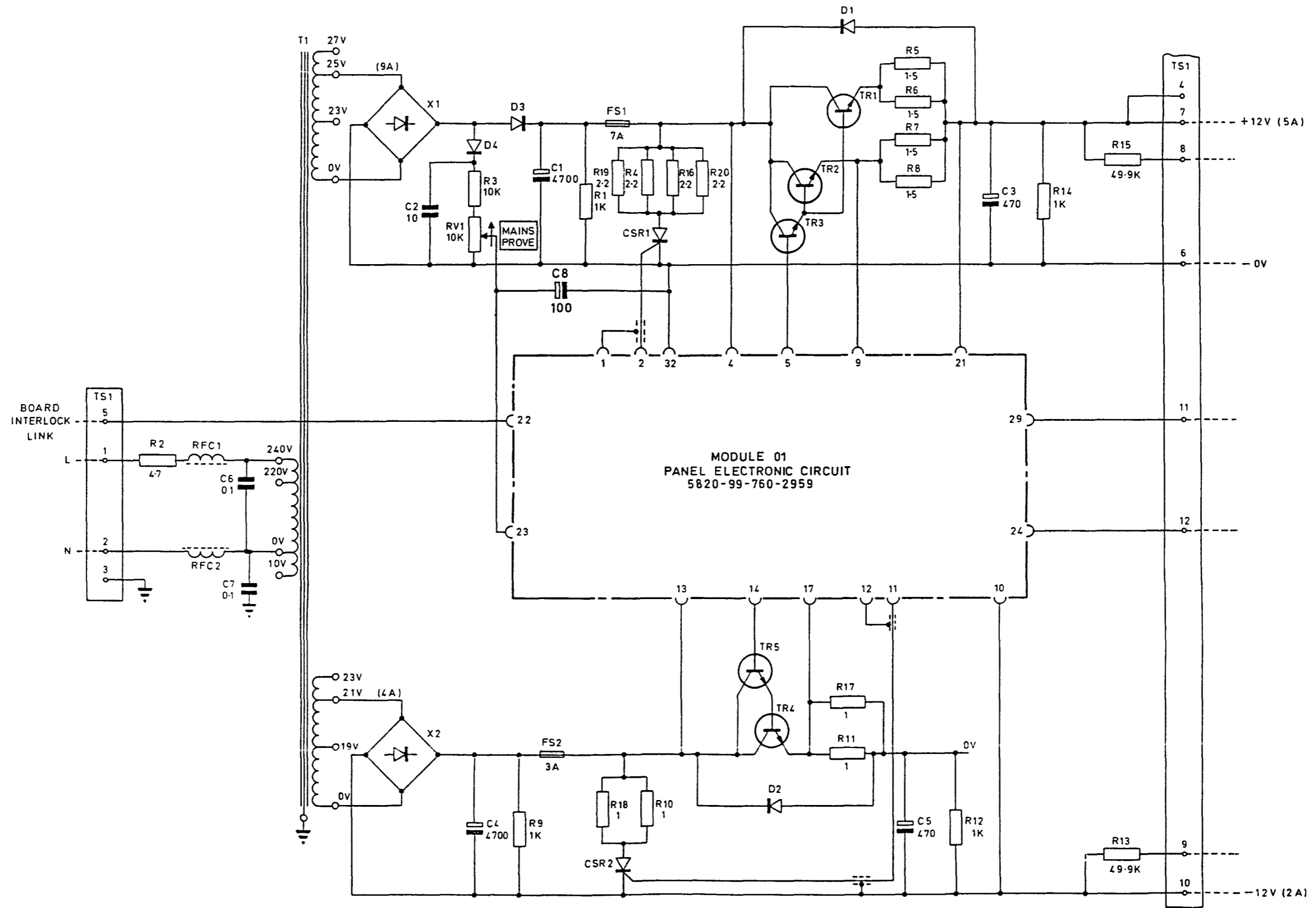
13 The negative supply is proved to be in excess of -10 V by the circuit associated with TR15. Initially TR15 is turned on via R47. When the zener voltage of D12 is overcome the negative supply pulls down the base of TR15, turning it off and removing the clamp on C7.

Mains prove circuit

14 The mains supply is proved to be in excess of -10 % of its nominal value by the circuit associated by IC3 and TR16. A reference voltage of approximately +6 V is fed to IC3(3) and a voltage proportional to the mains voltage is fed to IC3(4). If the mains voltage is low then IC3(9) is off and TR16 is switched on via R53. When the mains voltage exceeds the prove level set by RV1 (external to the board), IC3(9) switches on, switching off TR16 and removing the clamp on C7. The design of the power supplies is such that the ± 12 V supplies are at the nominal values just before the mains voltage can reach its prove level.

Board interlock

15 When all board interlocks are complete, PLA(22) is at 0 V. Therefore TR17 is on and TR18, TR19 and TR20 are off. If the interlock is subsequently broken, TR17 switches off and C8 charges rapidly via R57, turning on TR18. TR20 also switches on and ensures TR19 remains off. When the interlock is remade, TR17 switches on and TR20 switches off. TR18 remains on while C8 discharges via R58. Thus TR19 switches on for approximately 400 ms applying a clamp to C7, and then reverts to the off state.



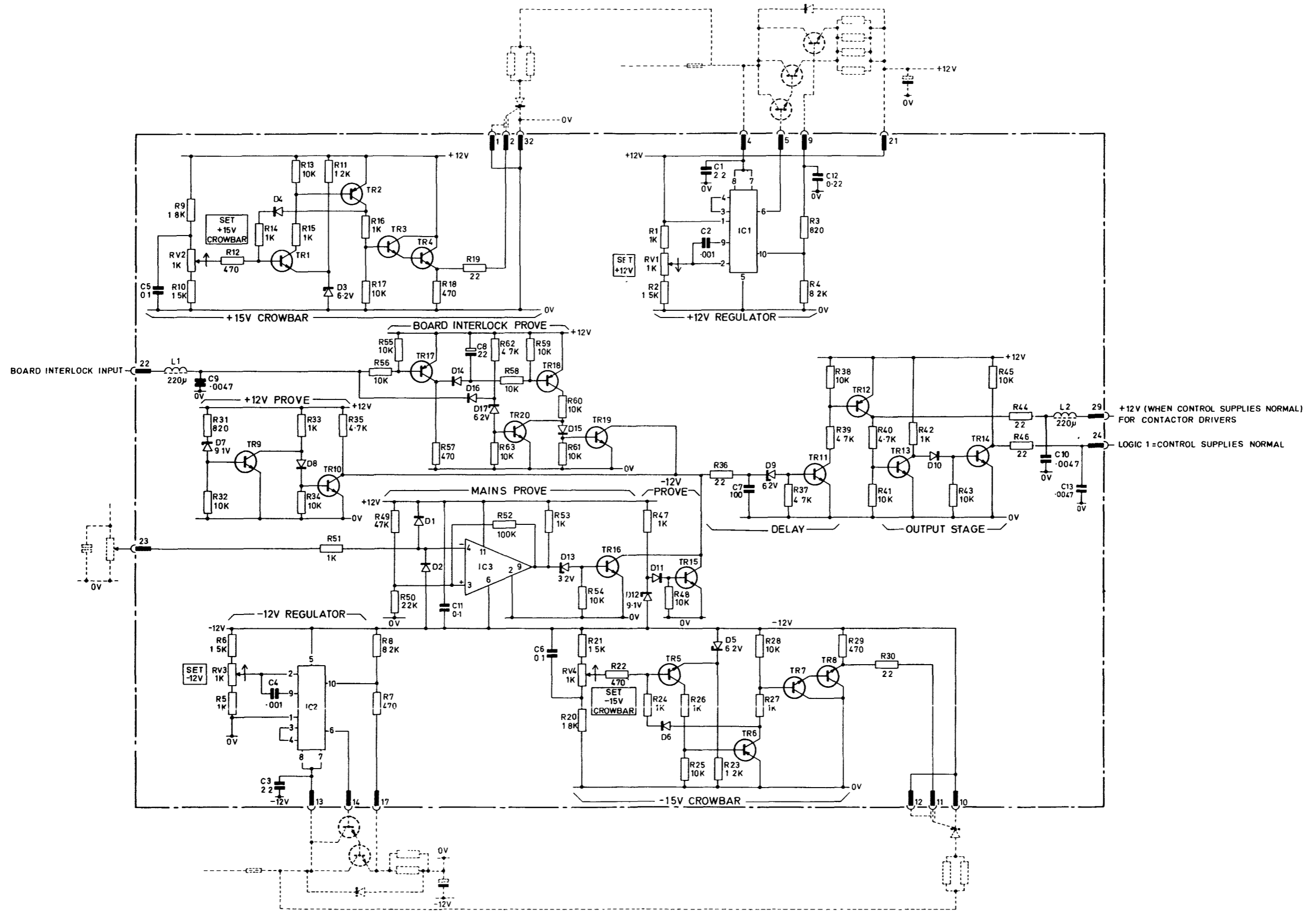
INCORPORATING MOD RM042
 BASED ON H31-9707Z SH 2 ISSUE 1
 Fig D14 - 1

Power supply unit 5820-99-760-2960 : circuit diagram

May 90 (Amdt 4)

MDM 23455 8146279 JUL 90 2648

Fig D14 - 1
 Sub-sect D14
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BASED ON H31-9708Z SH 1 ISSUE 8
Fig D14-2

±12V supply pec,5820-99-760-2959 : circuit diagram

Sub-sect D15METER PANEL (UNIT 10)5820-99-751-8052

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- 1 Introduction
- 3 Description

Fig

Page

D15-1 Meter Panel: circuit

3

INTRODUCTION

1 The meter panel provides monitoring indications for the pen. stage and final stage amplifiers together with forward and reverse power monitoring. Also provided by this panel are trip and lockout controls and indicators and a sequencing switch which provides limited testing facilities for the amplifier.

2 The unit is fitted to the top left-hand side of the rf cabinet. Its controls and indications are readily accessible to provide the normal day-to-day monitoring facilities for the equipment.

DESCRIPTION

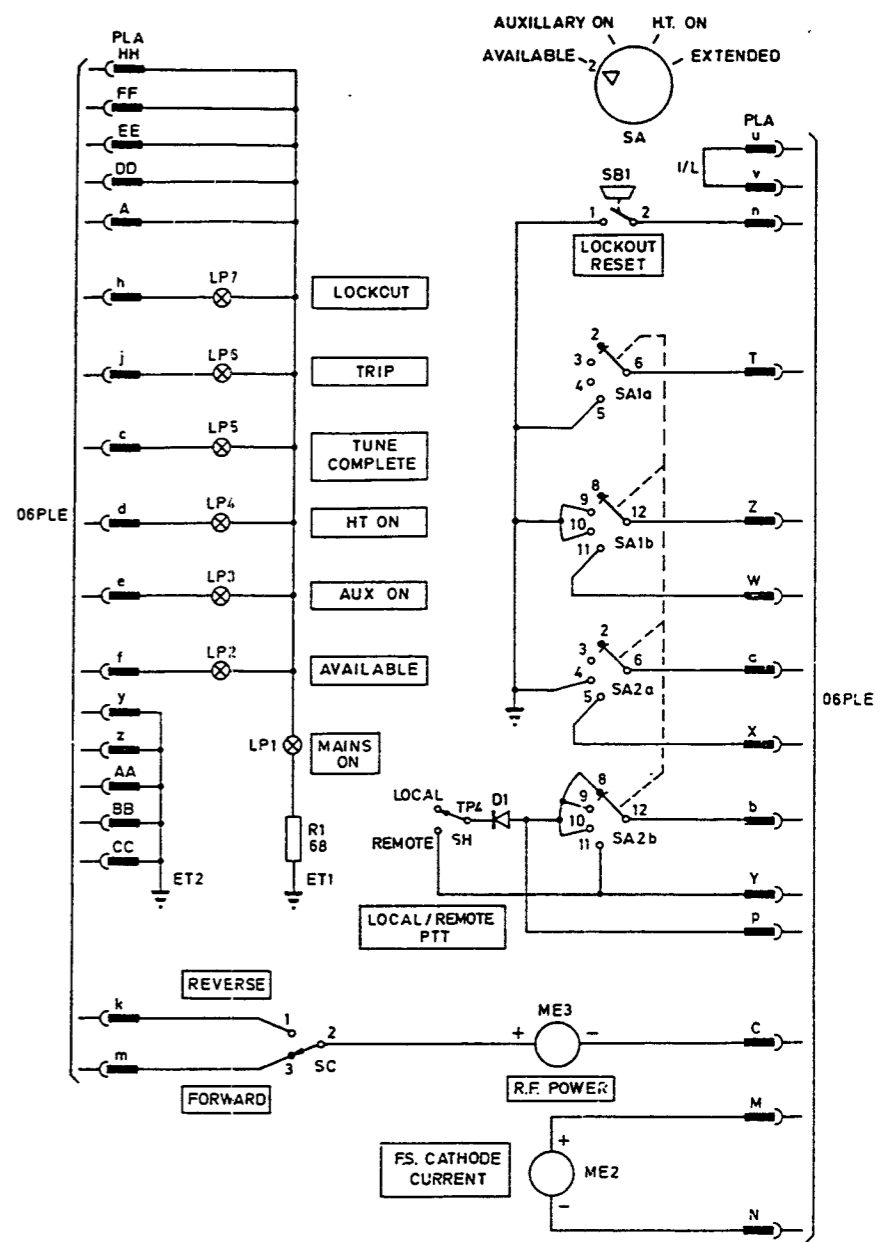
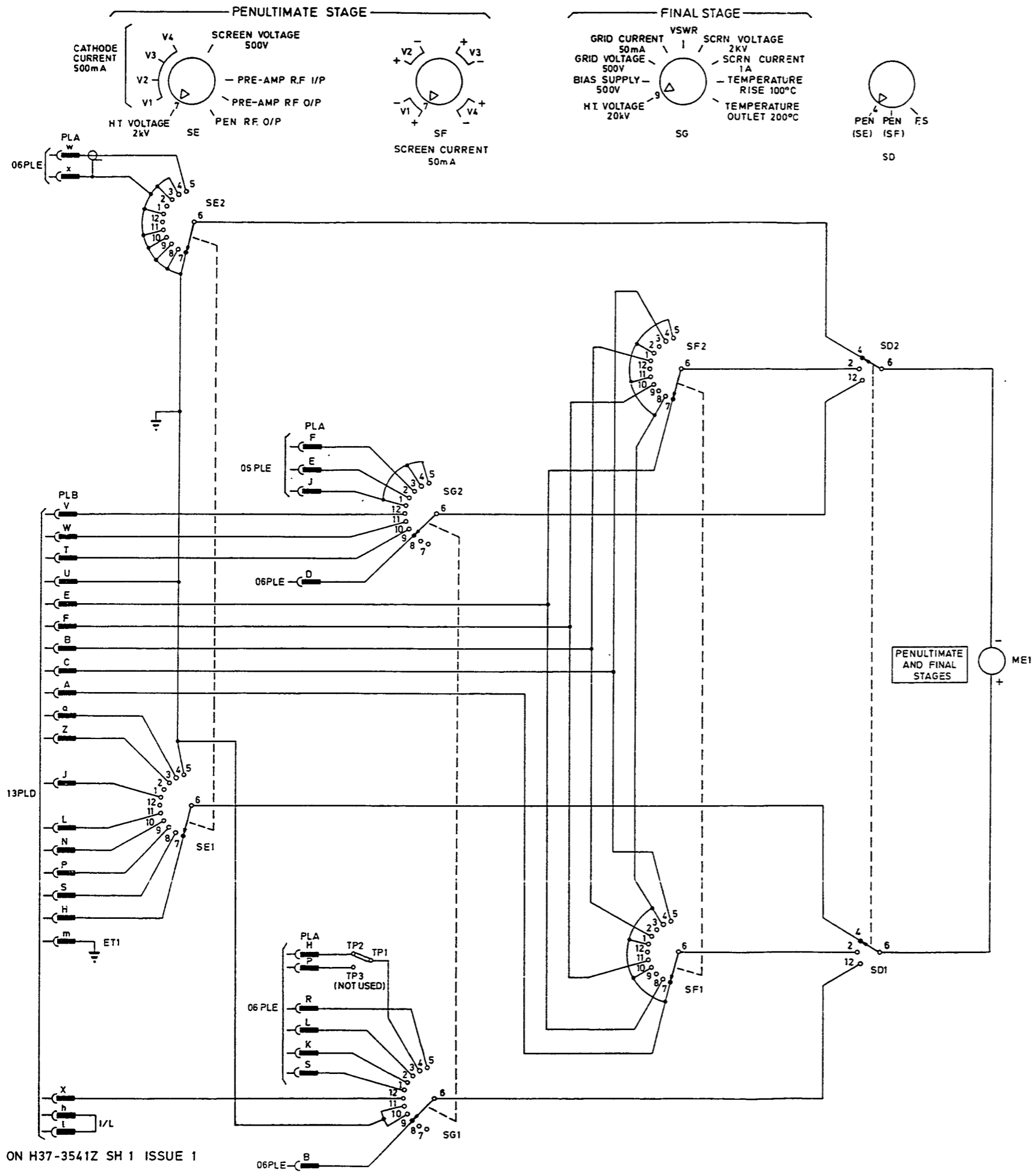
3 Refer to Fig D15-1. The pen. stage and final stage monitor levels are brought to PLA and PLB on the meter panel and, with the exception of the final stage cathode current level, routed by way of the selection switches SD to SG for display on the pen. stage and final stage meter ME1. Switches SE and SF are associated with the pen. stage, SF providing monitoring for the screen grid current and SE for general parameter monitoring. Two switch positions for each valve are provided by SF, these positions marked + and - allow screen grid current monitoring when the grid is supplying or drawing current. Final stage parameter indications are selected by SG and SD selects one of the three switch outputs for display on the pen. and final stage meter ME1.

4 Forward and reverse power indication levels are fed to this panel on PLA, m and k respectively. One of these inputs is selected by SC for display on the rf power meter ME3.

5 The final stage current is measured from the voltage level sensed by a meter divider 02R7 situated on the final stage. This current level is displayed by ME2, the final stage cathode current meter.

6 Trip indicator LP6 when lit indicates that a trip has occurred, as sensed by the trip sensing module, and been automatically reset by the amplifier 3-shot system. This indication will remain lit until manually reset on the trip sensing module.

- 7 A failure of the 3-shot restoration system to clear a trip will result in a lockout and its associated indicator LP7 being lit. This indication is cleared, after the cause of the lockout has been established, by operating reset switch SB.
- 8 Power supply sequencing for the amplifier is controlled by SA. Each switch position is supported by an indicator when each sequencing step is satisfied the associated indicator will light. The sequence may be held at any position for test purposes.
- ▶ 9 Wafer SA2B circuitry includes lever switch SH which provides selection of LOCAL/REMOTE PRESS TO TALK. Refer to AP116E-1212-1A Sect C Fig C9 for external circuits. This switch, in series with diode D1, is to restore LOCAL PRESS TO TALK and TEST LOCAL MUTE facilities, to overcome Drive Unit H1541 overriding certain functions of the amplifier. The switch prevents the effect of relay RLB of Extended Control Serial Module 06ML05 when the switch is put to LOCAL.
- 10 Test points TP1 and TP2 are permanently linked. ◀



FOR DETAILS OF INTERLOCK WIRING REFER TO FIG D1-7

INC. MOD RM074/1

BASED ON H37-3541Z SH 1 ISSUE 1
Fig D15-1

Meter panel 5820-99-751-8052 : circuit diagram

Nov 92 (Amdt 9)

Fig D15-1

Sub-sect D15

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Sub-sect D16FILTER/COUPLER ASSEMBLY (UNITS 11 & 12)H-37-4810-02

CONTENTS

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- 1 Introduction
- 4 External connections
- 5 Cooling
- Description
- 6 Harmonic filter
- 7 Directional coupler and output monitor
- 17 Setting up

Fig

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| D16-1 | Directional coupler: simplified circuit | 2 |
| D16-2 | Filter/coupler assembly: circuit diagram | 5 |

INTRODUCTION

1 The assembly forms part of the output feeder of the amplifier. It comprises two sub-units; one containing a directional coupler and a monitor point, the other being a harmonic filter.

2 The assembly operates up to an rf output power of 25 kW (cw) or 50 kW (pep) in the frequency range 2 to 30 MHz. It is mounted inside the rf cabinet in series with the rf output feeder. The two sub-units contained in this assembly are a line type Harmonic Filter 751-7873 (Unit 12) and a Directional Coupler and Output Monitor 751-7874 (Unit 11). The assembly contains three distinct functional areas as follows:

- 2.1 An harmonic filter
- 2.2 A monitor point, allowing accurate measurement of harmonics up to 100 MHz.
- 2.3 A directional coupler, providing two voltages proportional to the forward and reverse power. These voltages are amplified on the trip sensing module (ML08) and displayed on the front panel power meter.

3 The directional coupler and output monitor contains two compartments on either side of a dividing plate. The larger of the two is a continuation of the transmission line and contains two toroidal current transformers, for the directional coupler and monitor point, a voltage monitoring capacitor C2, for the directional coupler and two line matching capacitors C1 and C3. The remaining compartment contains the directional coupler detector circuits mounted on the Directional Coupler Board, H-37-4806-01 and the monitor point resistor load assembly. Access can be gained to this compartment by removing the cover for making adjustments to the variable capacitors.

External Connections

- 4 The external connections for the assembly are:
- 4.1 High power rf connectors for the hf input and output
 - 4.2 Two BNC connectors for monitor point outputs
 - 4.3 A multiway connectors for the dc outputs of the directional coupler.

Cooling

5 Cooling is by forced air fed to the assembly via an air hose to the hose input.

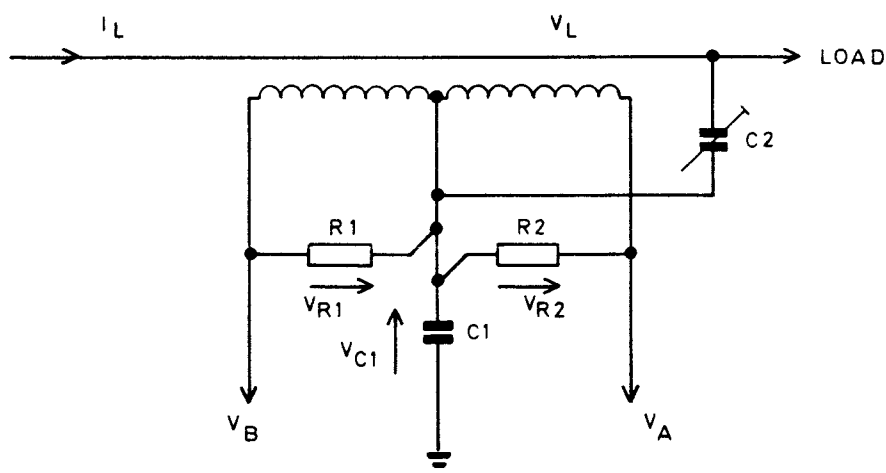
DESCRIPTIONHarmonic filter

6 The harmonic filter is a three section low-pass filter constructed in the form of a coaxial line. The capacitive filter elements are lumped components, while the inductive filter elements are formed by sections of a coaxial line.

Directional coupler and output monitor

7 The directional coupler consists of a section of transmission line with a matching capacitor at each end. The coupler provides information on the forward and reverse power in the output feeder by monitoring the current and voltage in the line. The voltage information is provided by a capacitive potential divider and the current information by a single toroidal current transformer. This transformer has a centre tapped winding to provide antiphase signals with respect to the centre tap.

8 The operation of this circuit is explained using the following simplified circuit diagram shown in Fig D16-1.



H37-4810G SH 1 ①

Fig D16-1 Directional coupler, simplified circuit

9 Voltage and current in the transmission line are designated V_L and I_L respectively. For a matched condition they will be in phase and related by the equation; $V_L = Z_0 \cdot I_L$ where Z_0 is the characteristic impedance.

10 A current flowing in the line will induce a current in the secondary of the current transformer T1 which will in turn produce antiphase voltages across R1 and R2, the load resistors. C2 is adjusted so that the voltage across C1 (V_{C1}) is equal to that across R1 (and R2). Then, for the matched condition, V_{C1} will add to V_{R2} to give V_A , the forward power information, and V_{C1} will subtract from V_{R1} , resulting in a zero voltage at V_B , the reverse power information.

11 Any mismatch condition arising will result in either a phase difference between the line voltage and current and/or a different ratio of line voltage to current. Either condition will result in a non-zero voltage at V_B . The voltage information relating to the forward and reverse power at V_A and V_B is proportional to $\sqrt{\text{forward power}}$ and $\sqrt{\text{reverse power}}$ respectively.

12 On the full circuit; the two banks of resistors R1 to R12 and R16 to R27 are the equivalent of R1 and R2, on the simplified circuit, and C13 to C15 represents C1.

13 The antiphase voltages V_A and V_B are applied to frequency compensating circuits, C29, C48, R28 and C32, C49, R33 which prevent the response falling at higher frequencies. These are followed by voltage doubler and low pass filter circuits formed by C43, D36, D42, C41, R31, R35 and C47 in the forward power section, and by C38, D35, D39, C40, R30, R44 and R46 in the reverse power section.

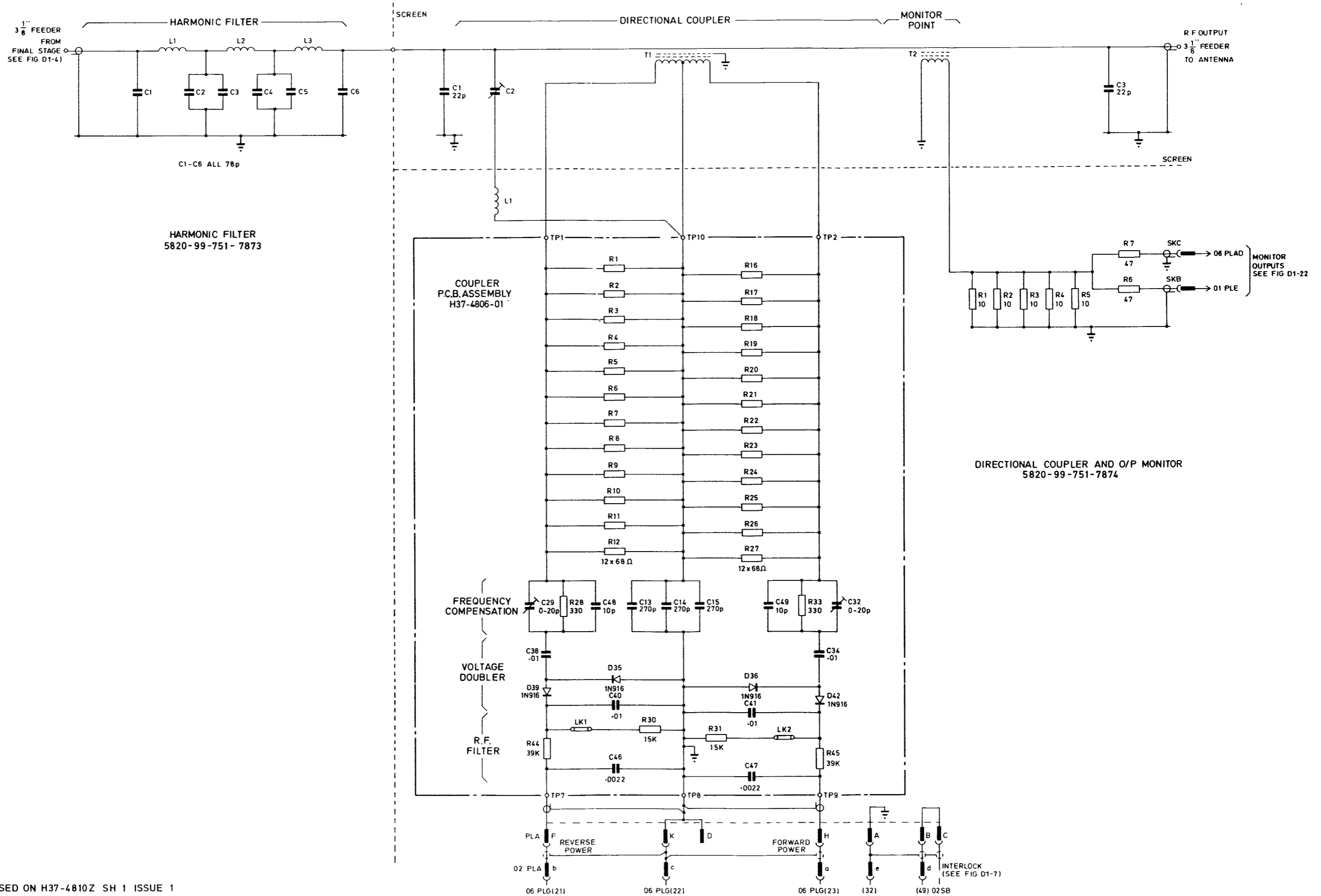
14 Inductance L1 provides frequency compensation for stray inductance in the bottom section of the capacitive divider.

15 The resulting dc output levels on PLA.F and PLA.G are fed to the meter panel, via dc amplifiers in the trip sensing module, to drive the forward and reverse power meter display.

16 The output monitor comprises a toroidal current transformer T2 and a resistive load R1 to R5. A sample of the rf output signal is provided by T2 with a flat output response up to 100 MHz for measuring harmonics. Matching for the rf monitor outputs is provided by R6 and R7.

SETTING UP

17 Links LK1 and LK2 are used for setting up the coupler and should be made. Setting up the coupler is a compromise between the capacitive divider setting for the lower frequencies, using C2, and the compensating capacitors C29 and C32, for the higher frequencies. These capacitors are set to give the best response over the operating frequency range.



BASED ON H37-4810Z SH 1 ISSUE 1
Fig D16-2

Filter/coupler assembly H37-4810-02 : circuit diagram

Fig D16-2

Sub-sect D17PENULTIMATE STAGE ASSEMBLY (UNIT 13)5820-99-751-7923

CONTENTS

Para

- 1 Introduction
- 7 Circuit Description

Fig

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| D17-1 Pen. stage assembly: circuit | 5 |
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INTRODUCTION

1 The penultimate stage unit consists of a wideband solid state amplifier driving a penultimate stage comprising four ceramic beam tetrode valves in parallel. These valves are coupled via a pi coupling network to the final stage valve (mounted in the main cabinet, unit 02).

2 The capacitors of the pi coupling circuit are motor driven and tuned automatically. The coarse tuning information is derived from the frequency counter module (ML17) and the range selection module (ML11), located in the main amplifier cabinet. The fine tuning information is derived from the discriminator module (ML10) located in the main amplifier cabinet, via the discriminator sensor (13ML02) mounted in the penultimate stage assembly.

3 The unit also contains the heater supplies for the penultimate stage, the final stage and penultimate stage bias supplies and the screen stabilizers for the penultimate stage.

4 The penultimate stage assembly is a runner-mounted unit located on the left-hand side of the rf cabinet assembly. Ball contacts on the top of the unit make connections to the final stage valve base (grid and earth) when the unit is pushed into position.

5 The assembly is divided into three screened compartments which are accessible through separate removable covers. The partition dividing the upper and lower compartments provides good r.f. isolation between the input and output circuits of the penultimate amplifier.

6 Cooling air is forced into the unit from a pressurized area in the main amplifier, via an aperture and holes in the base of the penultimate stage unit. The air flows over the pre-amplifier heat sink and then through the valve bases and is exhausted through a hole on the side of the unit. Air also passes through the terminating resistor compartment and is exhausted through a hole on the side of the unit.

CIRCUIT DESCRIPTION

7 Refer to Fig D17-1. The 50Ω , 2 to 30 MHz rf input to the unit, at a level of approximately 50 mW, from the rf attenuator module enters the assembly at SKB, which connects to a wideband solid state pre-amplifier (13ML01) providing up to 5W output into 50Ω . The output of the pre-amplifier is connected to pin 8 on the PCB H-37-3518-01 which has mounted on it all the components associated with the wideband coupling network matching the 50Ω output of the pre-amplifier to the grids of the valves V1 to V4. Wideband matching for the output of the pre-amplifier is provided by C1 to C4 together with L1 and C2. Impedance terminating resistors R1 to R8 provide a 75Ω termination for the 50Ω to 75Ω impedance matching transformer T1.

8 The four valves V1 to V4 are radial beam tetrodes, 4CX 350A connected in parallel, and operating in class AB. The ht supply is 1150V. The screen supply is 350V which is stabilized by a chain of zener diodes D2 to D10. Sockets SKG/H/J/K2 and plug PLP provide a means of setting the screen voltage to the required value. The screen stabilized voltage is derived from the 1150V supply by dropper resistors located in the penultimate stage power supply unit 08. R12 and R13 provide screen volts metering. Each valve has a cathode feedback resistor R6 or R7 to improve the linearity of the stage. L1 and L2 provide high rf impedance so that R2 and R3 can be used to measure the cathode currents of the valves. These components are mounted on each of two cathode PCBs H-37-3515 together with decoupling capacitors C1 to C4 and screen current measuring resistors R1 and R4. Valve grid bias is derived via R2 to R5 with C8, C10, C12 and C14 acting as dc blocking capacitors. The 1150V ht supply for the valves is fed through PLC.H choke L1 and L2 with C26 and C27 providing decoupling. Resistors R17 to R19, R21 and R22 provide a metering divider for the 1150V supply.

9 The pi network inductance L3 is switched in ranges corresponding to the ranges of the final stage as follows:

Range	Frequency
1	2 to 2.3 MHz
2	2.3 to 3 MHz
3	3 to 4.5 MHz
4	4.5 to 6.7 MHz
5	6.7 to 10 MHz
6	10 to 15 MHz
7	15 to 20 MHz
8	20 to 25 MHz
9	25 to 30 MHz

10 The tapping points of L3 are selected by means of contact bars which are operated by a solenoid mechanism. Sections of L3 are progressively shorted out as the frequency range increases.

11 The pi network variable capacitors C18 to C20 are ganged together and their ratio is such that the anode impedance of V1 to V4 is matched to the low impedance terminating resistors R7 to R10.

12 Fixed capacitor C17 is switched out of circuit by the solenoid operated contact RLJ1 on ranges 7 to 9. This solenoid is controlled by the range selection module, the control inputs being processed by the preamplifier and fed out on 13 ML01 SKA. 32a and 32c.

13 When a particular range between range 2 and 9 is selected the appropriate solenoids are energized by control signals the range selection module. The contacts of these solenoids RLA to RLH progressively short out sections of the tuning inductor L3 as the range and frequency increase. Two solenoids are operated at a time as follows: the solenoid for the range selected plus the next lower frequency range solenoid.

14 Grid and anode sample r.f. voltage levels are fed to discriminator sensor assembly 13ML02 via blocking capacitors C21 and C22. This module contains two separate emitter follower circuits which match these signals to the input of the discriminator module. In order to prevent these circuits having an adverse effect they are only switched into circuit during the amplifier tune sequence. This switching is controlled by the tune complete input from the auto-tune control module to PLN.c. A description of the discriminator sensor assembly is given in Sub-sect D19.

15 The discriminator module contains a phase comparator for the anode and grid sample levels and provides fine tuning information for the control circuits of the penultimate stage tuning motor M1, see Sub-sect D10.

16 A sample of the penultimate stage rf output is fed back via SKR to provide a front panel monitor output on SKA. This sample is derived from the final stage grid PCB located near the grid of the final stage valve.

17 Transformer T1 provides the 6V ac supply for the heaters of the valves. RV1 enables this voltage to be set up using TP1 and TP2 as monitoring points. Meter ME1 is a filament hours meter mounted on the front panel.

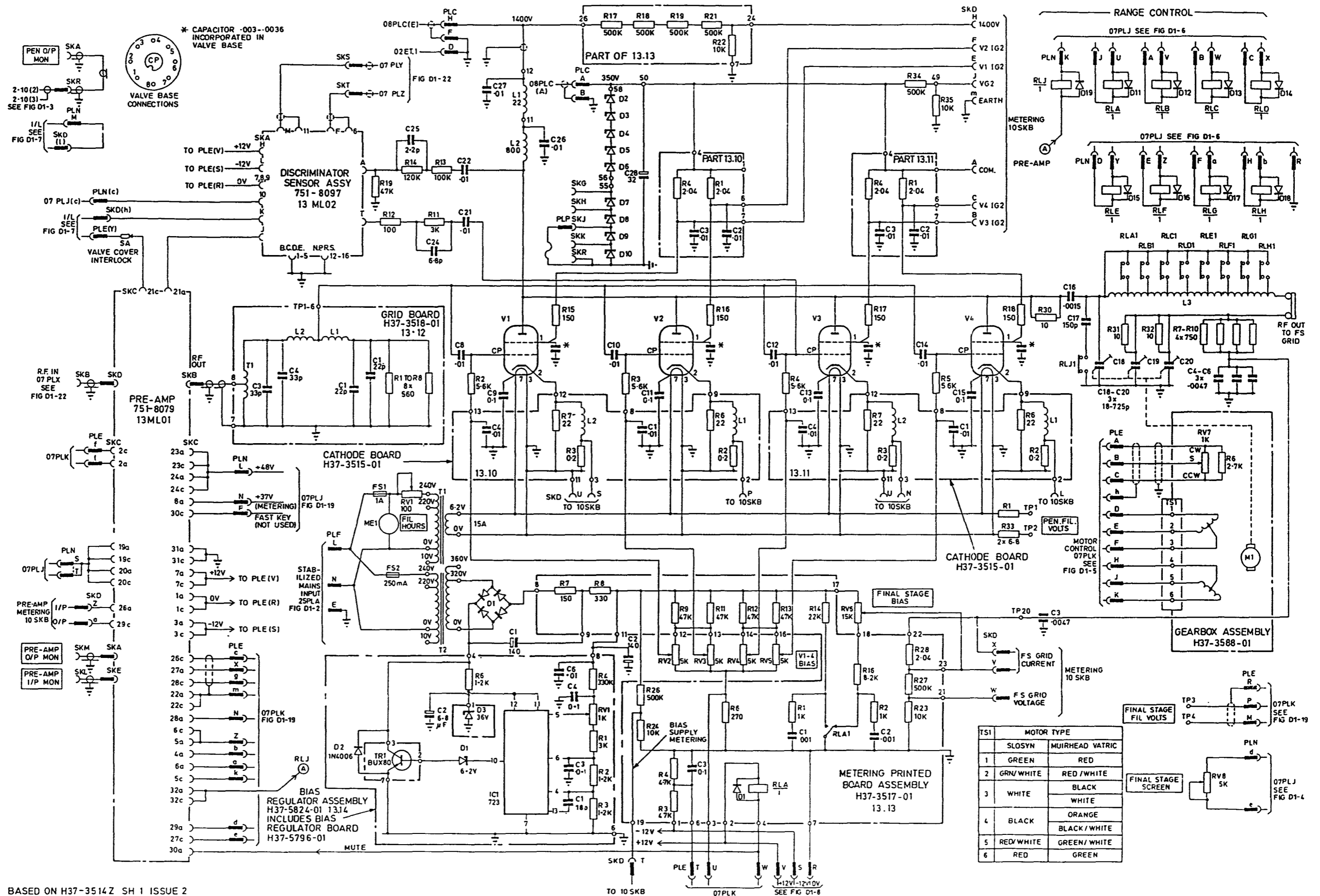
18 Transformer T2 is the bias supply transformer for both the pen. stage and final stage valves. Bridge rectifier and smoothing circuit D1, R7, R8, C1 and C2 provide a smoothed d.c. for the series regulator circuit. This regulator is mounted on the Bias Regulator Assembly H37-5824-01 and fitted in the earth return line. It comprises IC1 together with series pass transistor TR1. Protection for the regulator, when switching off, is provided by D2, while zener diode D3 ensures that the voltage drop across the regulator IC1 is limited to 36V. A potential divider chain consisting of R4, RV1, R1, R2 and R3 provides a reference voltage proportional to the output voltage for the regulator IC1 and RV1 is used to set this output voltage to -340V.

19 The bias for the penultimate valves is derived via R9, RV2 and R6 for V1, R11, RV3 and R6 for V2, R12, RV4 and R6 for V3, and R13, RV5 and R6 for V4, RV2 to RV5 being front panel preset controls enabling the valve static feeds to be set up.

20 The final stage bias is derived via RV6 which is also a front panel control enabling the final valve static feed to be set up. Connection of the bias to the final stage is via R28 (grid current metering) and terminating resistors R7 to R10. Capacitors C4, C5 and C6 provide an r.f. earth connection for the terminating resistors.

21 The metering PCB H-37-3517-01 has mounted on it the keying relay, RLA, R34 and R26 for bias supply metering, R23 and R27 for final stage bias metering. R6 provides a bias prove voltage together with a reference voltage from the -12V supply via R3 and R4 to the amplifier control circuits.

- 22 When coarse tuning is in progress logic level 0 is applied to PLE.W causing:
- 22.1 The keying relay RLA to operate and switching the final stage bias from normal to full bias (cutting off the final stage valve). Resistor R14 keeps the load constant on the bias supply line when RLA1 changes over.
 - 22.2 The rf output of the pre-amplifier to be muted. Logic level 0 is also applied when it is required to mute the transmitter during PTT (Press to Talk) operation.
- 23 The +12V interlock line enters the unit at PLE.Y and passes through SA when the valve cover is correctly fitted, then through links on the discriminator sensor and pre-amplifier PCBs and out through SKD.h. The interlock line re-enters the unit on SKD.l and is finally fed out on PLN.N.
- 24 This unit also houses the final stage filament monitoring and screen voltage controls. These facilities are mounted on the front panel.



BASED ON H37-3514Z SH 1 ISSUE 2
Fig D17-1

Penultimate stage assembly, 5820-99-751-7923 circuit diagram
MDM 22477 8146279 FEB 90 2648

NOTE:- EMBODYING
MOD RM 026/3

Fig D17-1
Sub-sect D17
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Sub-sect D18PRE-AMPLIFIER ASSEMBLY (UNIT 13 ML01)5820-99-751-8079

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6	Description
7	Amplifier
11	Bias
13	ALC Detector
16	Monitoring and Metering
18	Mute
21	Voltage Regulator
23	Solenoid Control
25	Variable Attenuator
28	Performance checks
29	Regulator output
30	Bias level checks
31	Variable attenuator operation
32	Pre-amplifier performance check
33	Fast key mute
34	ALC Detector

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D18-2	Pre-amplifier: circuit diagram	11

INTRODUCTIONWARNING...

THIS EQUIPMENT CONTAINS COMPONENTS IN WHICH BERYLLIA (BERYLLIUM OXIDE) IS USED. THIS MATERIAL IS HAZARDOUS IF ITS DUST IS INHALED OR TOUCHES CUT, ABRADED OR DISEASED SKIN. THE COMPONENTS ARE THE RF POWER TRANSISTORS, TR7, TR8, TR9, TR14, TR16 AND TR17. REFER TO DEF STAN 59-61 (PART 1) ISSUE 2, WHICH DETAILS THE NECESSARY SAFETY PRECAUTIONS.

1 The pre-amplifier provides a maximum drive output of 5W into the pen. stage. This output level is controlled by the attenuator module using the detected rf output level of the pre-amplifier. For 30 kW working an attenuator is connected into the rf input circuit by links.

2 In addition to this amplifier circuit the pre-amplifier also houses detector, monitoring, mute and solenoid control circuits together with a variable self resetting attenuator. A +37V regulator is fitted to provide the power supply for the amplifier circuit.

3 The assembly forms part of the pen stage and comprises a printed board and heat sink both mounted on a base plate. Cooling is by the forced air being drawn through the pen. stage. This air is arranged to pass over the pre-amplifier heatsink.

4 Control signal processing is by means of c-mos digital intergrated circuits. For the supply voltage used logic levels are defined as:

4.1 Logic level 0 = 0 to 3.5V and

4.2 Logic level 1 = 8.5 to 12V.

5 To protect the integrated circuits against damage that may be caused by withdrawing or replacing the module whilst the supply is on, inputs from PLA are into a 'pull-up' resistor of typically 10 k Ω and a series resistor of typically 10 k Ω .

DESCRIPTION

6 Refer to Fig D18-1 and Fig D18-2. This module contains seven discrete functional areas each of which is described separately in this section. These areas are:

6.1 Amplifier circuit

6.2 ALC detector

6.3 Input and output monitoring and meter circuits

6.4 Mute circuits

6.5 Voltage regulator

6.6 Solenoid control circuit

6.7 Variable self resetting attenuator circuit

Amplifier

7 The amplifier provides sufficient signal gain for the incoming rf drive to provide a 5W output to drive the pen. stage. This incoming rf drive signal is taken via a fixed matching attenuator R88, R89 and R91 to links LK9 and LK11 used to select a 2.2 dB attenuator R53, R54 and R56 for 30 kW working. When the tune sequence is complete a further 1.5 dB attenuator, R57 to R59, is switched into circuit by RLB if the vswr exceeds 2.2. This relay is controlled by the vswr and temperature sensing module. A variable overdrive attenuator is connected across the input to the amplifier.

8 A three stage amplifier is used to provide the required output level each of these stages employing a push-pull circuit. The first stage is formed by transistors TR7 and TR14 together with their associated components and is driven by unbalanced-balanced matching transformer T4. Current feedback is provided by transformers T1 and T7 which, in conjunction with the emitter resistors R37 and R64, set the input impedance of the amplifier.

9 The intermediate stage is transformer coupled to the first stage by T8. This stage is similar to the first stage, using TR8, TR16, T2 and T9, and is transformer coupled to the final stage by T11. A push-pull drive is provided by this transformer which also controls the input impedance for the final stage by means of a voltage feedback winding.

10 Final stage amplifier TR9 and TR17 has current feedback provided by T3 and T12. This stage is transformer coupled to the output circuits by balanced to unbalanced transformer T13.

Bias

11 Bias for the first two stages is provided by transistors TR23 and TR24 which sample the emitter voltages of the rf transistors and maintain these levels constant. The bias levels are set by potentiometers RV1 and RV2.

12 Final stage bias is provided by constant current source TR18 and TR25. These transistors sample the voltage fed to the centre top of the output transformer T13 and keep it constant. Bias level for the final stage is set by RV6.

ALC Detector

13 The alc detector provides a dc output signal proportional to the level of the rf output from the pre-amplifier. This signal varies between 1V and 0.2V, the lower level corresponding to an rf output signal of 1V, and is used to control the attenuators in the rf attenuator module.

14 A sample of the rf output signal from T13 is fed to the potential divider R114 and R115. The resulting signal is then fed to a voltage doubling detector D27 and D28. This detector circuit is forward biased from the +12V supply via D26 and RV7. Forward bias level is set by RV7, and D26 provides temperature compensation for the detector. Additional temperature compensation is provided by D29 and D33, these diodes are forward biased from the -12V supply via D34 and RV8. This allows linear operation of the detector down to very low signal levels.

15 The output of the detector is applied to a dc amplifier IC12. Limiting for the alc input level to this amplifier is provided by D31. Under normal operating conditions the resulting dc signal is fed to the rf attenuator module, via RLE.1, to provide a reference level. During the set output part of the auto-tune sequence RLC is energized and RLE de-energized so that rf output level at the coupler is used to provide this reference level. A further reference level is provided by the discriminator module. This is fed to the rf attenuator module via RLD.1 during the final stage tune sequence.

Monitoring and Metering

16 Resistive potential dividers are connected to the input (R92 and R93) and output (R42 and R46) of the amplifier. These potential dividers provide rf monitoring outputs for these input and output rf signals which are fed to the front panel of the pen. stage.

17 Meter outputs for both the input and output rf signals are provided by detector circuits connected to these points. These detector circuits allow the meter panel to display the input and output rf levels. An amplifier TR21 and TR22 increases the level of the rf input signal to a level suitable for this meter.

Mute

18 Two methods of muting the amplifier are employed; normal muting, using RLA and high speed muting, using the fast keying circuit based on TR19.

19 Relay contact RLA.1 is connected in the rf output path of the amplifier and is controlled from the auto-tune control module. Receipt of a logic 0 mute command from this module causes the rf output to be switched into the 50 Ω load formed by R41 to R44.

20 High speed muting is achieved by switching the +37V supply to the amplifier stages by way of TR19 and TR27. Receipt of a logic 0 key input on PLA.30a causes TR19 to cease conducting which causes TR27 to cease conducting, inhibiting the +37V supply to the amplifier circuit. Current bias for the mute circuit is provided by TR13.

Voltage Regulator

21 A +37V regulated supply is provided by the voltage regulator circuit for the three stage amplifier. This regulated supply is derived from the +48V supply to the module. Transistors TR1 and TR2 provide a constant current source for the main series regulator TR6 and TR28. The current available from the collector of TR2 is shared between the base of TR6 and the collectors of TR4 and TR3, this last transistor being normally non-conducting. The current source for the main series power regulator transistor TR28 is provided by TR6. A proportion of the output voltage is sensed by potential divider chain R9, R12 and RV3 and fed to the base of TR4 where it is compared to a 6.2V reference level set by D7. If, for example, the output voltage is high then this results in TR4 conducting more heavily causing a reduction in the current available at the base of TR6. This in turn causes an increase in the potential dropped across TR28 emitter and collector reducing the output voltage.

22 The operating range of the regulator is 35V to 40V and is set by RV3. The current drawn through TR28 is equalized by R9 and R12, the voltage across R9 being proportional to the load current. TR3 provides current limiting for the regulator. If the current demand is excessive then this voltage level is sufficient to cause TR3 to conduct, diverting current from TR2 collector. This in turn reduces the current available for TR6 base, resulting in a fall in output voltage from the regulator.

Solenoid Control

23 The solenoid control circuit is driven from the range selection module and normally energizes a solenoid in the pen. stage on ranges 7 to 9. This solenoid switches an additional capacitor into the rf output circuits. The operating range may be altered by breaking links on the pre-amplifier.

24. With links LK1, 2, and 3 made IC4.4 changes to logic 1 when ranges 7 to 9 are selected. This results in TR12 conducting causing Darlington pair TR26 to conduct and provide an earth path for PLA.32a and 32c, energizing RLJ on the pen. stage. Links LK1 to 3 allow the operating range for this solenoid to be varied, see Table 1.

TABLE 1 SOLENOID CONTROL RANGES

Links Made	Range
LK1	7
LK2	8
LK3	9

Variable Attenuator

25 The variable attenuator reduces the rf output level when a logic 0 is present on PLA.2a. This input generated by the discriminator module in response to a surge in drive level. When PLA.2a returns to logic 1 the rf output power is gradually returned to full power following a linear sawtooth pattern.

26 Seven stage binary ripple counter IC7 is used to provide a sawtooth input to IC11.2. Receipt of a logic 0 on PLA.2a causes the output of IC11, measured at TP36, to change from logic 0 to a preset level. This level is determined by RV4 and RV5. When the input to PLA.2a returns to logic 1 the voltage on TP6 will slowly fall to 0V. All the inputs to NAND gate IC8 will now be at logic 1 resulting in IC7.1 changing to logic 0 to inhibit the counter. This holds the output of IC11 at 0V until receipt of a further logic 0 on PLA.2a re-activates the counter.

27 Variable attenuation for the rf signal is provided by VMOS FET TR10. When IC11.6 changes to the preset level TR10 attenuates the rf signal by 3dB, gradually decreasing this attenuation to zero as the voltage on IC11.6 falls.

PERFORMANCE CHECKS

28 The following procedures provide setting and checking information for the various circuits in the pre-amplifier. Proceed as follows:

28.1 Remove the pre-amplifier from the pen. stage and arrange in a suitable position so that air from a fan can be directed through the heat sink. Any type of fan delivering approximately 1400 litres/min. (50 cfm) would be suitable, to ensure that the temperature of the module heat sink does not exceed 70°C.

28.2 Connect three stabilized power supplies to a 64 way female connector, Marconi identity CC-180422-2, as follows:

28.2.1 +48V, 3A: positive - pins 32a, 23c, 24d and 24c
negative (earth) - pins 19a, 19c, 20a and 20c.

28.2.2 +12V, 0.1A: positive - pins 7a and 7c
negative (earth) - pins 1a and 1c.

28.2.3 -12V, 0.1A: negative - pins 3a and 3c
positive (earth) - pins

28.3 Set the three power supplies to the following voltages:

28.3.1 +48V $\pm 0.5V$

28.3.2 +12V $\pm 0.1V$

28.3.3 -12V $\pm 0.1V$

28.4 Switch off the power supplies and connect the test socket to PLC on the pre-amplifier. Switch on the three power supplies.

Regulator output

29 Using a digital voltmeter check that the voltage between TP30 (positive) and earth (heat sink) is 36V $\pm 0.1V$. If this voltage is outside this tolerance adjust RV3 to achieve this reading.

Bias level checks

- 30 Check the bias for the pre-amplifier stages as follows:
- 30.1 Check the bias levels of TR7, TR14, TR8 and TR16 by connecting the digital voltmeter between each of the following test points (positive) and earth (negative) in turn and noting the readings:
 - 30.1.1 TP5 - 2.5V \pm 0.5V, set by RV1
 - 30.1.2 TP31 - 2.5V \pm 0.5V
 - 30.1.3 TP9 - 3.5V \pm 0.5, set by RV2
 - 30.1.4 TP32 - 3.4V \pm 0.5V
 - 30.2 If necessary adjust these potentiometers to achieve the indicated readings.
 - 30.3 Check the bias levels of TR9 and TR17 by connecting the digital voltmeter between TP20 (negative) and TR33 (positive). The indication should be 1.4V \pm 0.1V. If necessary adjust RV6 to achieve this reading.

Variable attenuator operation

- 31 Check the correct operation of the variable attenuator as follows:
- 31.1 Connect the oscilloscope between TR36 and earth. Check that the voltage level indicated is 3V \pm 0.2V. If necessary adjust RV4 to achieve this level.
 - 31.2 Connect PLC2c to earth and check that the oscilloscope display traces a linear ramp from 3V to 0V in approximately 2.5 seconds.
 - 31.3 If necessary adjust RV5 to set the 0V level and RV4 to set the timing. These controls interact so that several adjustments may be required.

Pre-amplifier performance check

- 32 Check the performance of the pre-amplifier as follows:
- 32.1 Switch off the power supplies.
 - 32.2 Connect the output of the drive to SKD on the pre-amplifier, via the variable attenuator.
 - 32.3 Set the variable attenuator to 20 dB.
 - 32.4 Connect SKB on the pre-amplifier to the 10W rf wattmeter.
 - 32.5 Fit links 9 and 11 to position B.
 - 32.6 Connect PLC.2c to earth.
 - 32.7 Select CW on the drive at a frequency of 2.000 MHz.
 - 32.8 Switch on the power supplies and adjust the variable attenuator to achieve a power output of 2.5W. The gain of the amplifier should be 23.5 dB \pm 0.5 dB.

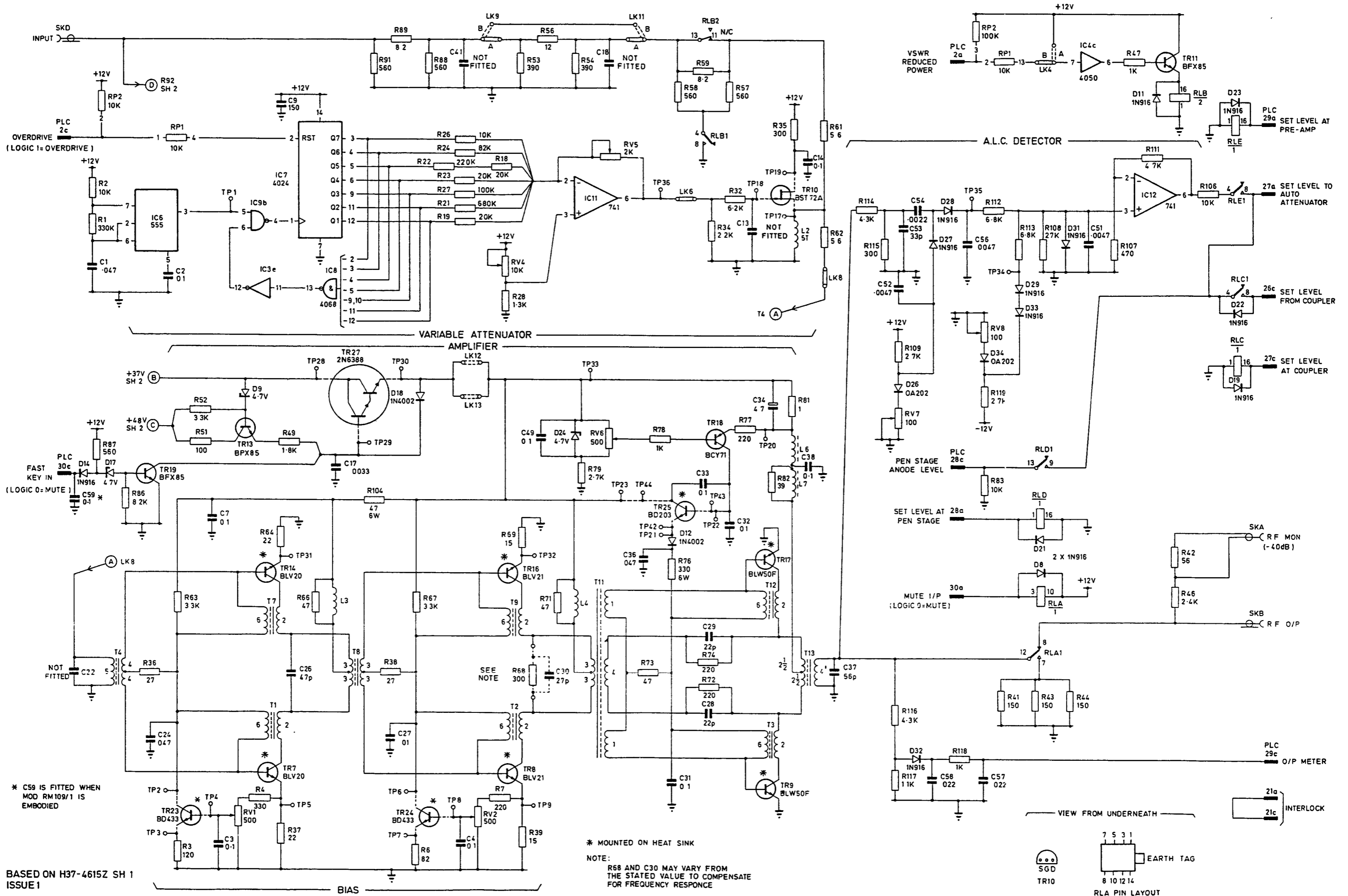
- 32.9 Check the gain of the pre-amplifier at various frequencies up to 30.000 MHz as detailed in 32.8 above. The gain should gradually increase through the frequency range to 26.5 dB \pm 0.5 dB at 30.000 MHz.
- 32.10 Reset the drive frequency to 2.000 MHz and the variable attenuator to achieve a power output of 2.5W.
- 32.11 Connect links LK9 and LK11 to position A and check that the output power decreases by 2.2 dB \pm 0.2 dB.
- 32.12 Remove the earth connection from PLC.2a and check that the output power decreases by a further 1.5 dB \pm 0.2 dB.
- 32.13 Connect the spectrum analyser to SKA and adjust the variable attenuator to achieve an output of 5W p.e.p. (2.5W mean).
- 32.14 Select 2-TONE TEST on the drive and check that all the intermodulation products are lower than -50 dB.
- 32.15 Select CW on the drive and check that none of the harmonic outputs exceed -45 dB.

Fast key mute

33 Check the operation of the fast key mute circuit by connecting PLC.30c to earth. Application of this earth connection should cause the rf output level to fall by a minimum of 40 dBs.

A.L.C. Detector

- 34 Check the alc detector circuit as follows:
 - 34.1 Disconnect the rf input signal.
 - 34.2 Using the digital voltmeter measure the voltage at TP35, this voltage should be within the range 78 to 82 mV.
 - 34.3 Check that the voltage at IC12.6 is 0V.
 - 34.4 Check that the voltage at TP34 is within the range 70 to 90 mV.
 - 34.5 If necessary adjust the settings of RV7 and RV8 to achieve the conditions in 34.3 and 34.4 above.
- 35 Remove all of the temporary connections and test equipment and reset the links to the settings shown in Sub-sect B3 Table 2 before refitting the pre-amplifier to the pen. stage.



BASED ON H37-4615Z SH 1 ISSUE 1

Fig D18-1

Mar 93 (Amdt 11)

CAUTION:
THIS BOARD / UNIT CONTAINS
STATIC SENSITIVE DEVICES.

WARNING:
THIS BOARD / UNIT CONTAINS
TOXIC BERYLLIUM OXIDE.

Pre-amplifier, 5820-99-751-8079: circuit diagram

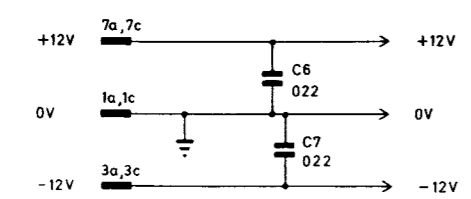
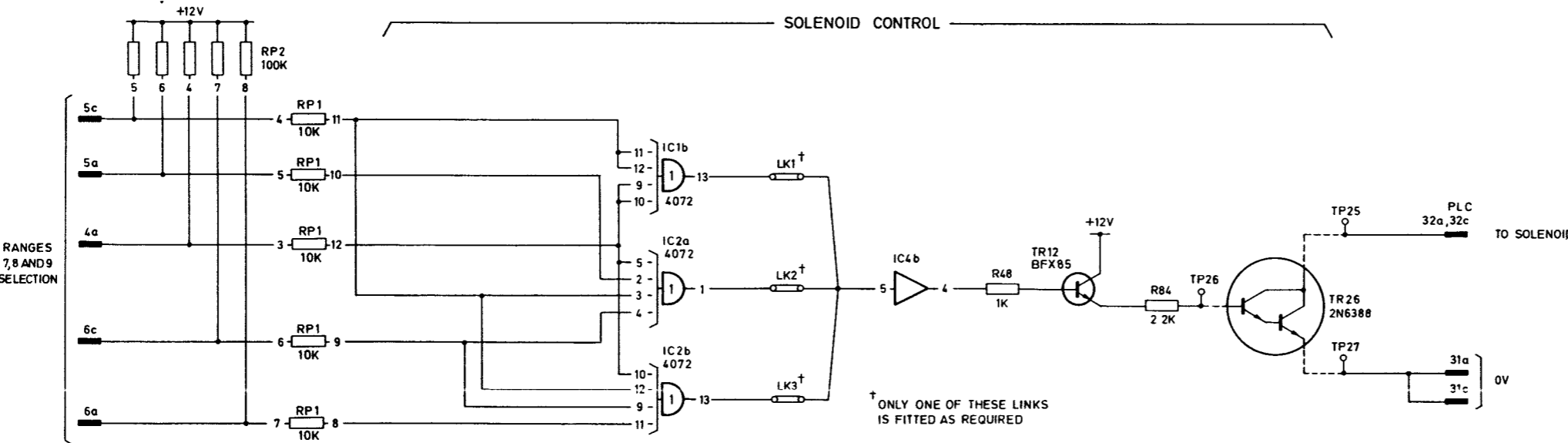
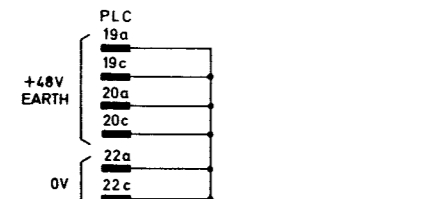
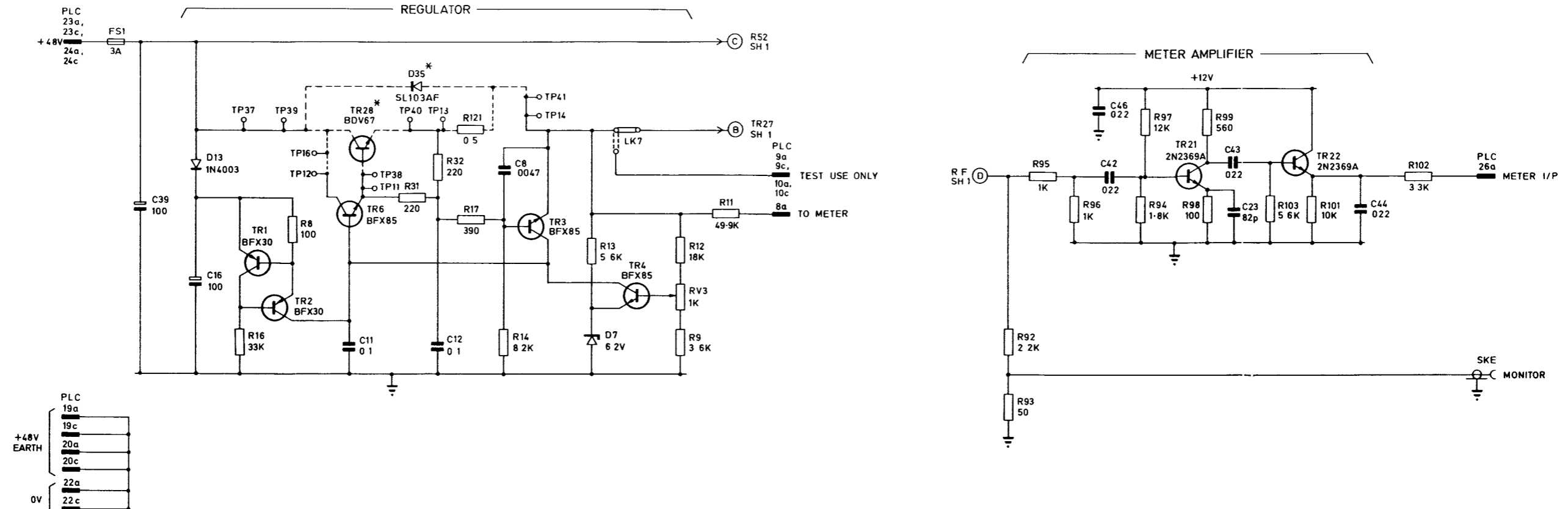
* MOUNTED ON HEAT SINK

NOTE:
R68 AND C30 MAY VARY FROM
THE STATED VALUE TO COMPENSATE
FOR FREQUENCY RESPONSE

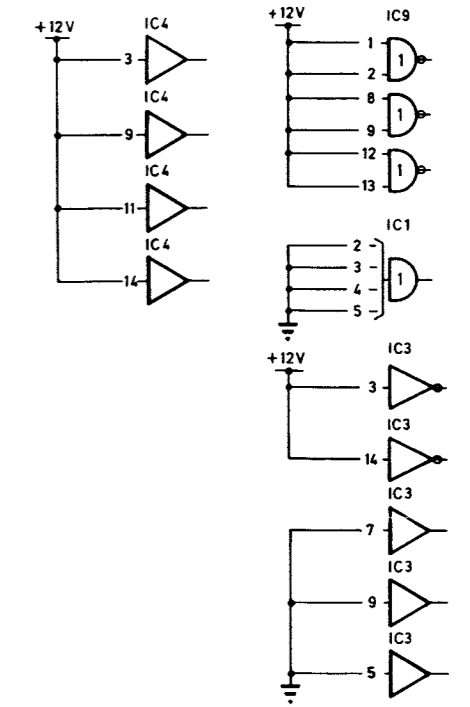
Fig D18-1

Sub-sect D18

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POWER CONNECTIONS				
IC	TYPE	+12V	0V	-12V
1	4072	14	7	-
2	4072	14	7	-
3	4049	1	8	-
4	4050	1	8	-
6	555	4, 8	1	-
7	4024	14	7	-
11	741	7	-	4
12	741	7	-	4
8	4068	14	7	-
9	4001	14	7	-



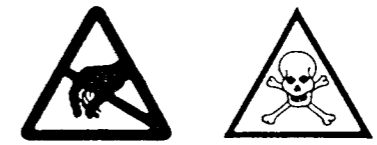
BASED ON H37-4615Z SH2 ISSUE 1

Fig D18-2

CAUTION: THIS BOARD / UNIT CONTAINS STATIC SENSITIVE DEVICES

WARNING: THIS BOARD / UNIT CONTAINS TOXIC BERYLLIUM OXIDE.

Pre-amplifier, 5820-99-751-8079 : circuit diagram



Jan 88

Sub-sect D19DISCRIMINATOR SENSOR ASSEMBLY (UNITS 15 AND 13 ML02)5820-99-751-8097

CONTENTS

Para

- 1 Introduction
- 2 Description

Fig

Page

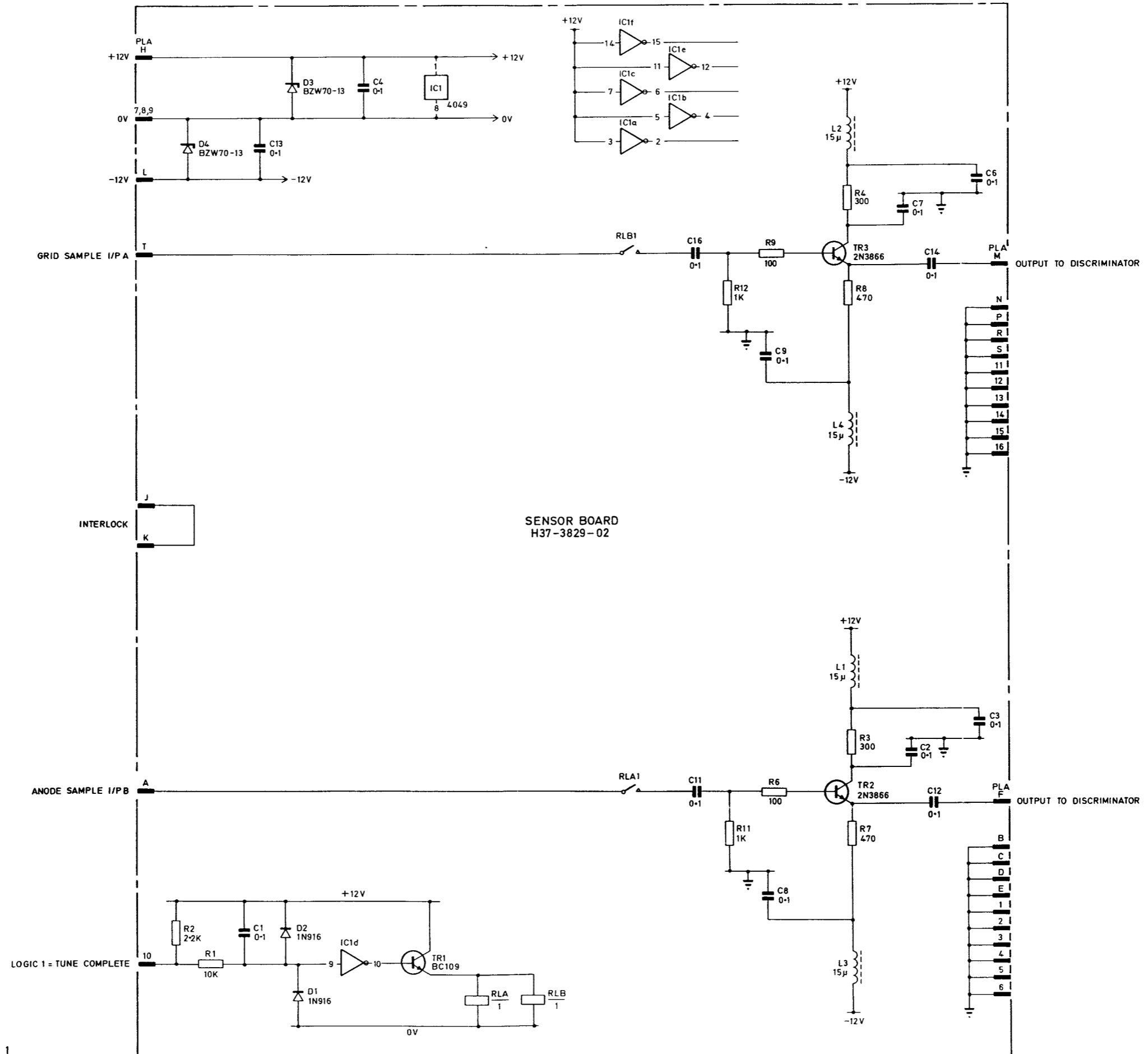
D19-1 Discriminator sensor assembly: circuit 3

INTRODUCTION

1 This unit provides a matching stage between the sampled grid and anode rf signals and the discriminator module, for both the penultimate stage and final stage of the amplifier. Two separate identical units are fitted, one as part of the penultimate stage with the remaining unit mounted near the final stage valve. Both units house a Sensor Board H-37-3829-02 which contains two emitter follower circuits to provide this matching for the sampled rf signal. These levels are monitored during the tune sequence only.

DESCRIPTION

2 The tune complete input to PLA.10 is held at logic 0 during the amplifier tune sequence resulting in both RLA and RLB energizing via IC1 and TR1 for this period. Relay contacts RLA1 and RLB1 connect the sampled rf signals to the base of transistors TR2 and TR3, via series resistors R6 and R9 with R11 and R12 which form terminating resistances. The outputs of these emitter follower circuits are connected to the discriminator module via PLA.M and F. When tuning the tune complete signal on PLA.10 changes to logic 1 causing the inputs to be disconnected.



Discriminator sensor assembly 5820-99-751-8097: circuit diagram

BASED ON H37-3543Z SH 1 ISSUE 1

Fig D19-1

Jan 88

Fig D19-1

Sub-sect D19

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Sub-section D20AUXILIARY POWER SUPPLY (UNIT 26)H37-3522-02

CONTENTS

Para

- 1 Introduction
- Circuit Description
- 2 General
- 4 +33 V regulator
- 7 +35 V crowbar
- 8 Auxiliary 'supplies prove' sensing

Fig

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|-------|---|---|
| D20-1 | Auxiliary power supply H37-3522-02: circuit diagram | 3 |
| D20-2 | Power supply 5820-99-760-2980: circuit diagram | 5 |

INTRODUCTION

1 This unit provides unregulated +48 V, +24 V and +10 V for the pre-amplifier, range selection solenoids and servo motor circuits. A regulated +33V supply is also provided but is not used in this application of the circuit. A sensing circuit, which feeds the trip sensing module, ensures that all these supplies are present before any attempt is made at range selection or servo motor operation. The unit houses a mains transformer and the power supply unit 5820-99-760-2980 which in turn contains the regulator pec 5820-99-762-1677.

CIRCUIT DESCRIPTIONGeneral

- 2 This power supply unit is capable of providing four outputs as follows:
 - 2.1 +48 V unstabilized.
 - 2.2 +24 V unstabilized.
 - 2.3 +10 V unstabilized.
 - 2.4 +33 V stabilized.

The unstabilized supplies are monitored on the auto-tune control module ML09.

3 The unit comprises a chassis on which are mounted the rectifiers and associated smoothing components, the power transistors and heatsinks and the plug-in regulator board. The mains input transformer associated with the unit is situated at the rear of the constant voltage regulator. The printed circuit board provides a stabilized +33 V supply derived from the +48 V supply.

+33 V regulator

4 Transistors TR3 and TR4 form a constant current source of approximately 1 mA. The current available from TR4 collector is shared between TR1 base, TR2 and TR5 collectors. TR2 is normally off, TR1 forms the current source for the power transistors TR1, 2 and 3 which are mounted external to the board. The +33 V output voltage is sensed and a proportion fed to TR5 base where it is compared to a reference voltage provided by zener diode D2.

5 If the output voltage is high then TR5 will conduct more heavily and reduces the current fed to TR1 base. The potential dropped across the power transistors increases and the output voltage falls. Thus a feedback loop is established to provide regulating action.

6 The range control of RV1 is between 32 V and 36.5 V approximately. Current through the power transistors TR2 and TR3 is equalized by R6 and R7. The voltage developed across R7 is proportional to the load current. When the load current exceeds 2.5 A, sufficient voltage is developed to turn on TR2, which takes current from TR4 collector and reduces that fed to TR1 base. Thus the output falls.

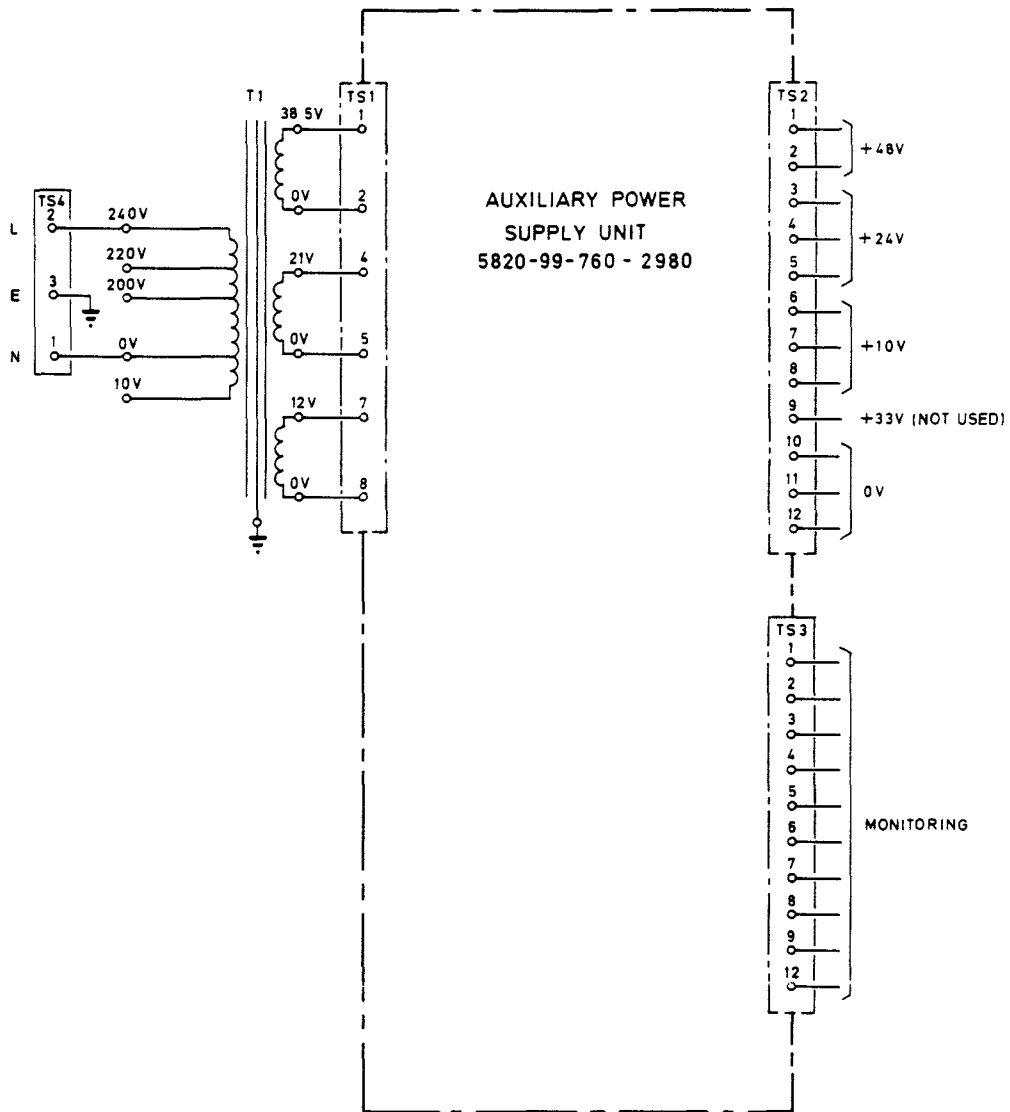
+35 V crowbar

7 Diode D11 provides a reference voltage for the crowbar circuit. The output of the +33 V supply is sensed and a proportion fed to TR6 base, which is normally non-conducting. If the +33 V supply output rises to +35 V, TR6 will then turn on. This causes TR7 to turn on and provide positive feedback via D12 and R28 to turn TR6 hard on. With TR7 on, TR8 and TR9 turn on to drive thyristor CSR1 and cause FS4 to blow. Current flowing through CSR1 is limited by the resistance in its anode circuit. Power diode D1 ensures that C8 is discharged and that the components of the regulator are not reversed biased.

Auxiliary 'supplies prove' sensing

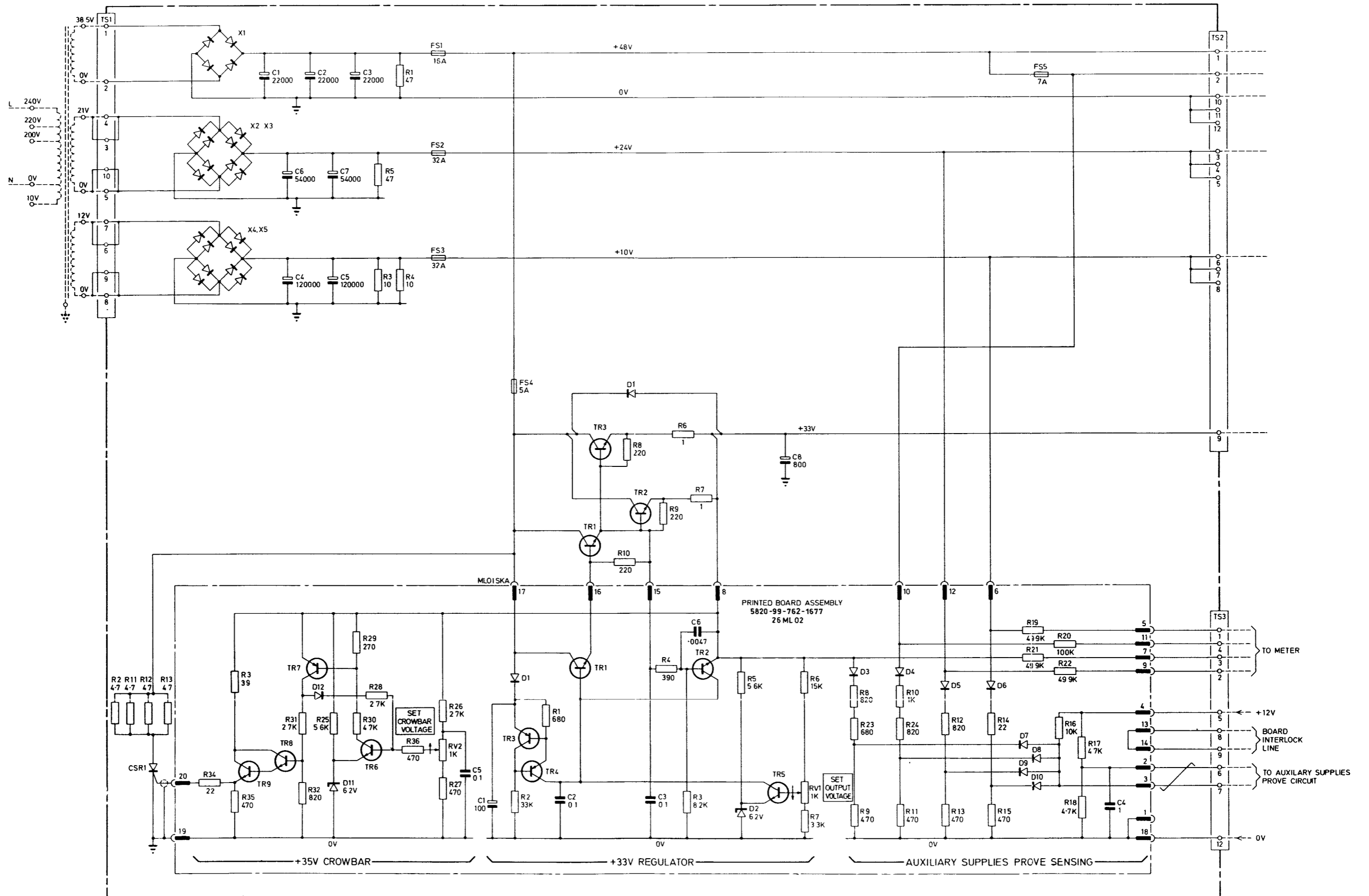
8 The external 'supplies prove' comparator is fed with a reference voltage of +6 V derived by R17 and R18. If the voltage at PLA(3) is less than the reference voltage, then the auxiliary supplies are said to be 'not proven'. The actions of the four sensing circuits (+48 V, +24 V, +10 V and +12 V) are identical.

9 Each of the supplies, when at normal level, develops a voltage of approximately 8 V to 10 V across one of the resistors R9, R11, R13 and R15, and will hold the voltage at PLA-3 at the lowest of these voltages. If any of the supplies falls sufficiently to pull PLA-3 below 6 V, the external comparator will produce a 'not proven' output.



BASED ON H37-3522Z SH 1
ISSUE 1

Fig D20-1 Auxiliary power supply H37-3522-02 : circuit diagram



BASED ON H31-9706Z SH1 ISSUE 9

Fig D20-2

Power supply 5820-99-760-2980 : circuit diagram

Fig D20-2

Sub-sect D21SCREEN GRID SUPPLY (UNIT 27)H37-3527-02

CONTENTS

Para

1	Introduction
	Description
5	Voltage regulation
9	Voltage control
13	Protection circuits
15	Output control
17	Supply on indication
18	Trip sensing

Fig

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D21-1	Screen grid supply: circuit diagram	5
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INTRODUCTION

1 This unit provides the +1400V regulated screen grid supply for the final stage valve of the amplifier. A single phase 240V mains supply is used to generate this regulated output. The mains input is rectified, smoothed and applied to the output circuit in the form of variable width pulses in order to achieve the required regulated output. The output from this chopping circuit is rectified and smoothed to provide the required dc output.

2 Sensing and monitoring circuits are connected to the output of this power supply. These circuits provide a feedback voltage which is used to control the output voltage together with control voltages, for external current and voltage indications.

3 The unit is mounted in the bottom left-hand corner of the rf cabinet. It contains two plug-in printed boards and a monitor board. These plug-in boards are the Control Board 751-8022 (27 ML01) and the Converter Board 751-8076 (27ML02). The converter board is mounted on a heat sink. Most of the components for this power supply are mounted on these boards. Some components, mostly those associated with the mains supply and high voltage output, are mounted directly on the chassis. Cooling is by air convection.

4 Since the operation of the printed boards and the chassis mounted components are interdependant they are treated as one complete unit for purposes of this description.

DESCRIPTIONVoltage regulation

5 The single phase supply is fed to the unit on PLA and full wave rectified by X4. The dc output is taken via a pi filter; C5, C6, and L1 to provide an unregulated high voltage supply for the regulator circuit. This supply is fed to the primary of T1 via switching FET's TR1 and TR2. These transistors are switched on simultaneously at 18 kHz by the pulsed output from the control circuit, the pulse duration determining the regulated voltage.

6 A 100:1 current transformer T2 provides current monitoring for T1 primary. The output from this transformer is fed to an overcurrent protection circuit, see Para 13. Two groups of five 75V zener diodes connected across the source and drain of TR1 and TR2 prevent an excess voltage occurring across these transistors. Diodes D12 and D13 limit the flyback voltage induced in the transformer primary to that of the unregulated dc supply.

7 The overall turns ratio of T1 is 7:1, with the transformer secondary winding divided into four separate windings. Each of these secondary windings has its own rectifier and smoothing circuit. The outputs of these smoothing circuits are connected in series to provide the high voltage output of the unit.

8 Two potential divider chains R16 to R19 and R23 to R29 are connected across the regulated output. These potential dividers provide monitoring levels for the regulation feedback and trip sample circuits. Also wired to the output circuit are meter shunt resistors R31 and R32, for the screen grid monitoring output and a meter protection 2.7V Zener diode D9.

Voltage control

9 The operation of the voltage control circuit is based on a pulse width modulation (PWM) supplies controller device IC1. This integrated circuit controls all of the basic functions of a PWM switched mode power supply (SMPS).

10 A logic 0 screen grid supply on input, from the supplies control module, to PLC.C is required to switch-on this supply. This logic 0 causes IC1.10 to change from 0V to +5V nominal, via filter L1, C8 and TR2 enabling IC1. Potential divider R12 and R13 limits the maximum mark/space ratio of the control waveform generated by IC1. Timing components R16 and C2 determine the fundamental frequency of operation. The switching waveform output produced at IC1.15 is used to drive TR1. Any noise on this output is attenuated by C1.

11 The squarewave switching waveform on C1 controls TR3 on the converter board, switching the 12V supply through the primary of T1. This results in +12V pulses in the two secondary windings of T1. These pulsed outputs control the drive FET's TR1 and TR2 switching the rectified and smoothed high voltage dc supply through the primary of T1.

12 When TR3 is switched off a large negative voltage is induced in the secondary windings of T1. Blocking diodes D12 and D13 prevent this voltage being applied to the gates of TR1 and TR2. Fast turn off of TR1 and TR2 is provided by TR4 and TR6. These transistors conduct when a negative voltage is detected, effectively connecting TR1 and TR2 gates to earth.

Protection circuits

13 The output current demanded from this power supply is sensed by current transformer T2. Positive voltages in this secondary are fed to the control board on PLA.Z and rectified by D3. Negative voltages are limited to 11V by D6 and blocked by D3. This rectified output is applied to the current limiting input of IC1. In the event of the current drawn from the power supply exceeding the threshold level of current limiting this input to IC1.11 causes the switching output of IC1 to be inhibited resulting in a fall in output voltage. This circuit provides immediate current limiting for the power supply output.

14 The voltage being delivered by this power supply is sampled by the potential divider R23, R24 and R26 to R29 and fed to the control board on PLA.U. This sample is used to provide a trip sample output for the trip sensing module and is fed out on PLC.H.

Output control

15 A potentiometer, situated in the penultimate stage, is used to set the output voltage under normal operating conditions. The level set by this potentiometer also controls the final stage screen supply indication. This potentiometer is part of potential divider R16 to R19 across the power supply output. The voltage level set by this potentiometer is fed to the screen grid supply board, on PLA.W, where it is applied to the feedback input of IC1 via LKA and frequency compensation circuit R14, R17, C6 and C7. An error amplifier in IC1 acts on this feedback level to control the output waveform.

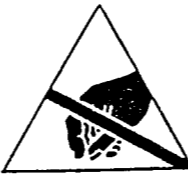
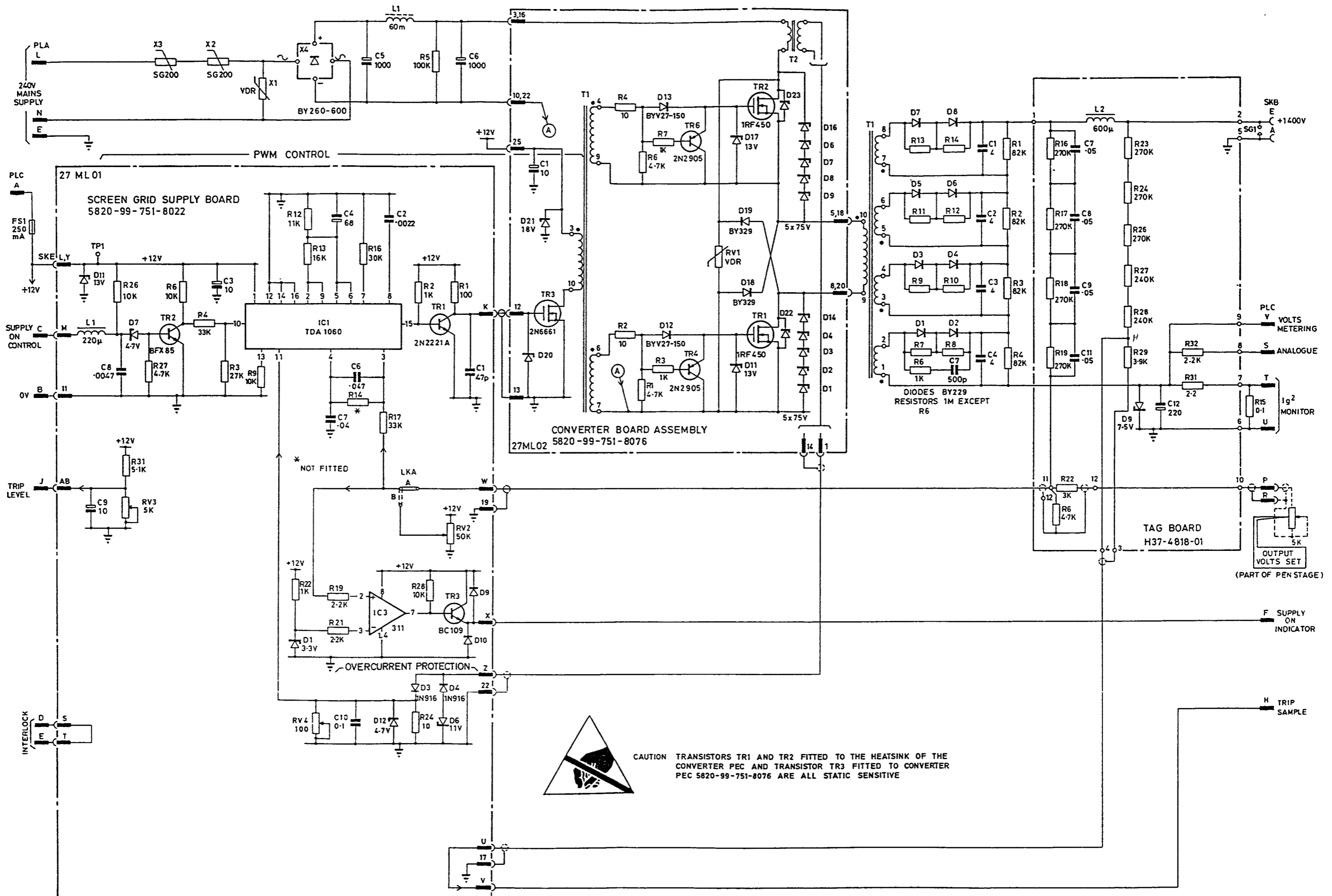
16 Provision is also made for control of the output voltage level at this unit for test purposes. This is achieved by setting link LKA to position B, the feedback level for IC1 is then set by RV2.

Supply on indication

17 The feedback level fed to R19 is compared to a 3.3V reference level set by D1 by comparator IC3. A logic 1 supply ON indication is fed out on PLC.F, via PLA.X, to provide an indication that the regulator is operating regardless of the output demanded. This screen grid indication is displayed on the supplies control module.

Trip sensing

18 A reference output of approximately 4.2 V on PLC-J is provided by R31, RV3 and C9 from the 12 V supply. This output is compared, in the trip sensing module, with the sample of the output voltage fed out on PLC-H, to actuate a trip condition in the event of the screen grid supply voltage exceeding the valve's safe screen level.



CAUTION TRANSISTORS TR1 AND TR2 FITTED TO THE HEATSINK OF THE CONVERTER PCB AND TRANSISTOR TR3 FITTED TO CONVERTER PCB 5820-99-751-8076 ARE ALL STATIC SENSITIVE

BASED ON H37-3527 Z SH.1 ISSUE 1

6130-99-751-8020 Screen Grid Supply Unit H37-3527-02: circuit diagram

Incorporating Mods RM052/1, RM053/1, RM062/1
June 92 (Amdt 6)

Sub-sect D22MODULE VSWR AND ATTENUATOR (06ML02)H37-6840-02

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1	Introduction
6	Description
7	CW/pep attenuator control circuits
20	50 kW/30 kW operation indicator circuits
21	Mean or pep indication

Fig.

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D22-2	Module VSWR and attenuator: circuit	7/8

INTRODUCTION

1 The MCVF equipment, when used in conjunction with the UK/FRT 651, adjusts its output to maintain a constant value, irrespective of the number of channels in operation. Between 2 - 8 channels, the mean power will be within the UK/FRT 651 specifications of 20 kW mean and 30 kW PEP.

2 When, however, single channel working is required. The mean and PEP power are equal, resulting in an overload situation, unless the drive level is reduced manually.

3 A modification (RM093/2, 094/2) fits a cathode current detector that causes an attenuator to be inserted before a trip occurs. In the case of 30 kW pep/20 kW CW operation a 1.76 dB attenuator is required, a 3 dB attenuator is required for 50 kW/25 kW CW operation. The attenuator is automatically deselected when two or more channels are in use and during a tune sequence. This MCVF attenuator has been incorporated into VSWR AND ATTENUATOR MODULE H37-6840-02.

4 Indicators on the front panel of the module show the configuration selected by the internal link settings, and in which mode the logic circuits are operating.

Note . . .

For the UK/FRT 651 Amplifier H1241 Edn.05, the vswr function of this module is not used.

5 Control signal processing is by means of c-mos digital integrated circuits. For the supply voltage used, logic levels are defined as:

5.1 Logic level 0 = 0 to 3.5V

5.2 Logic level 1 = 8.5 to 12V

DESCRIPTION: Refer to Fig D22-1 and Fig D22-2.

6 For the purpose of this description the module can be divided into three separate areas. These areas are:

- 6.1 CW/pep attenuator control circuits
- 6.2 50 kW/30 kW operation indicator circuits
- 6.3 Mean or pep power indication.

CW/pep attenuator control circuits

7 The attenuators are necessary because of the different cw and pep rating of the amplifier, when used with Multi-Channel Voice Frequency (MCVF) equipment.

8 The MCVF equipment adjusts its pep output to a constant value irrespective of the number of channels in operation, from 1 up to 8. Between 2 and 8 channels the mean power will not exceed one half of the pep value and is therefore within the rating of this amplifier, ie 50 kW pep and 25 kW cw, or 30 kW pep and 20 kW cw.

9 However, when single channel operation is required, the mean and pep values are equal, resulting in an overload situation if the drive level is not reduced.

10 The operation of the attenuator and the associated control relies on the detection of the cathode current of the final stage valve. The characteristics of the cathode trip circuit are such that a cathode current of up to 7 amps will not produce a trip; between 7 and 10 amps a trip will occur after approximately 1.5 seconds, and above 10 amps an immediate trip will occur. Operation with the mean power equal to pep rating results in the cathode current being in the delayed trip region. The circuits in this module are designed to operate in the delayed trip region such that it will cause an attenuator to be inserted in the drive output line before a trip occurs (ie reducing the drive level decreases the final stage cathode current).

11 The voltage which is proportional to the final stage cathode current is applied to PLA11 on this module.

12 LK1 can be used to isolate this voltage of the CW/PEP attenuator facility if not required.

13 This voltage drives the level detector IC8a whose reference voltage is set by RV3. When the level at IC8a pin 4 reaches the reference level at IC8a pin 5, then the output of IC8a changes state to drive the inverter IC8b, which in turn triggers the 0.5 second monostable IC9a and the D-type flip flops IC10a and IC10b. The 0.5 second timing components are R89 and C39.

14 The output of IC10a at pin 1 changes state after a period of 0.5 seconds (from the initial level detection at IC8a) to cause relays RLC or RLD to energise via drive IC7a.

15 Link LK3 is used to preset the selection of RLC or RLD whose contacts drive Pi network attenuators.

16 RLC is used for 50 kW operation to provide a drive attenuator of 3 dB by insertion of Pi attenuator R13 to R18. RLD is used for 30 kW operation to provide drive attenuation of 1.7 dB by insertion of Pi attenuator R19 to R24. RLC (or RLD if preset by LK3) will remain energised until the level at PLA11 falls to a predetermined level which is sensed by a second level detector IC8c whose level is preset by RV4.

17 IC8c drives a 5 second monostable IC9b (with timing components R95 and C40) and the D-type flip flops IC10a and b.

18 When the lower level reference voltage at IC8c pin 11 is reached, there is a delay of approximately 5 seconds before RLC (or RLD) is de-energised.

19 When a logic 1 tune command appears at PLA6 then IC10a and IC10b are instantly reset to ensure that RLC (or RLD) is de-energised to provide no attenuation in the drive input line during the transmitter tuning sequence.

50 kW/30 kW operation indicator circuits

20 The amplifier can be set up for either 50 kW or 30 kW operation. In order to achieve operation at the required output power it is necessary to set the taps on the main ht transformer together with various other adjustments. A switch located internally in the amplifier is manually set when these adjustments have been carried out which applies 0V to the appropriate indicator (DLP3 for 50 kW or DLP4 for 30 kW) on the front panel of this module.

Mean or pep indication

21 The OR gates IC14a, d and c are connected to enable the forward and reverse power indications of the transmitter to be switched to mean or peak reading via the remote control system, when tuning is complete.

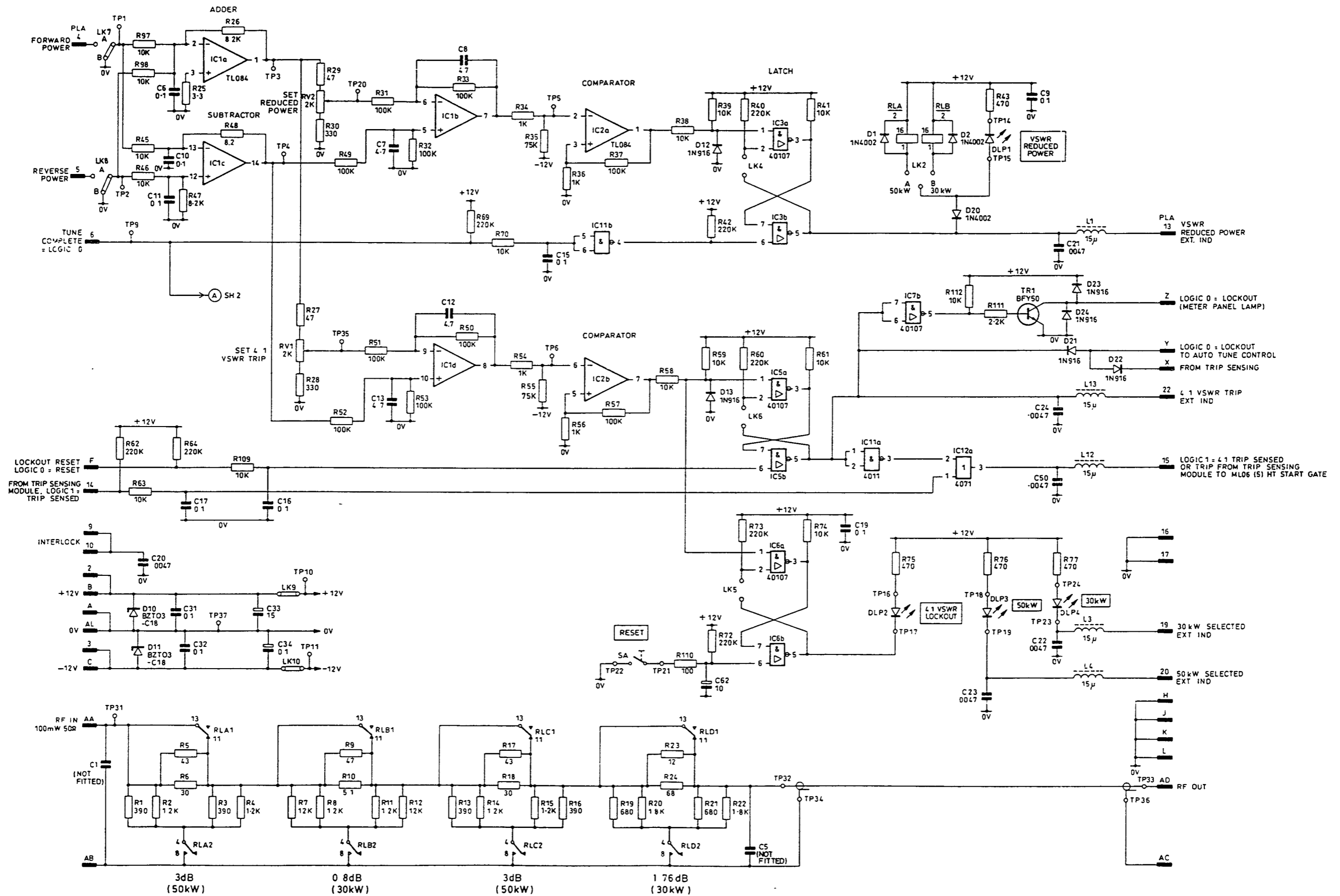
22 When working under local control, the transmitter forward and reverse power meters will read peak power when tuning is complete, and mean power when the transmitter is turning. The mean or peak reading is achieved by switching the time constants of the meter amplifiers in the trip sensing module.

23 The controlling voltage for the mean/peak power reading is derived from the auto tune control module of the transmitter and is connected to PLA30 on this module. When the transmitter has reached "tune complete", the logic level at PLA30 is 0. When the transmitter is connected for extended (remote) operation, a logic 0 appears at PLA31. The mean or pep selection from the remote control unit is applied to PLA32 where a logic 0, (corresponding to mean power) causes a logic 1 to appear at PLAD, and hence selects the mean power time constant in the trip sensing module, and lights the MEAN POWER led, DLP5 on the front panel of this module, via IC13a.

24 Similarly, a logic 1 at PLA32 causes a logic 0 at PLAD to select the peak power time constant and light the PEAK POWER led DLP7 via IC13b.

25 When local control is selected, the logic level 1 is applied to PLA31 and control of the mean or peak power is not possible via PLA32.

26 When the transmitter is tuning in local or remote, the logic level at PLA30 is 1, and mean power is selected by a logic 1 at PLAD. <



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Fig D22-1

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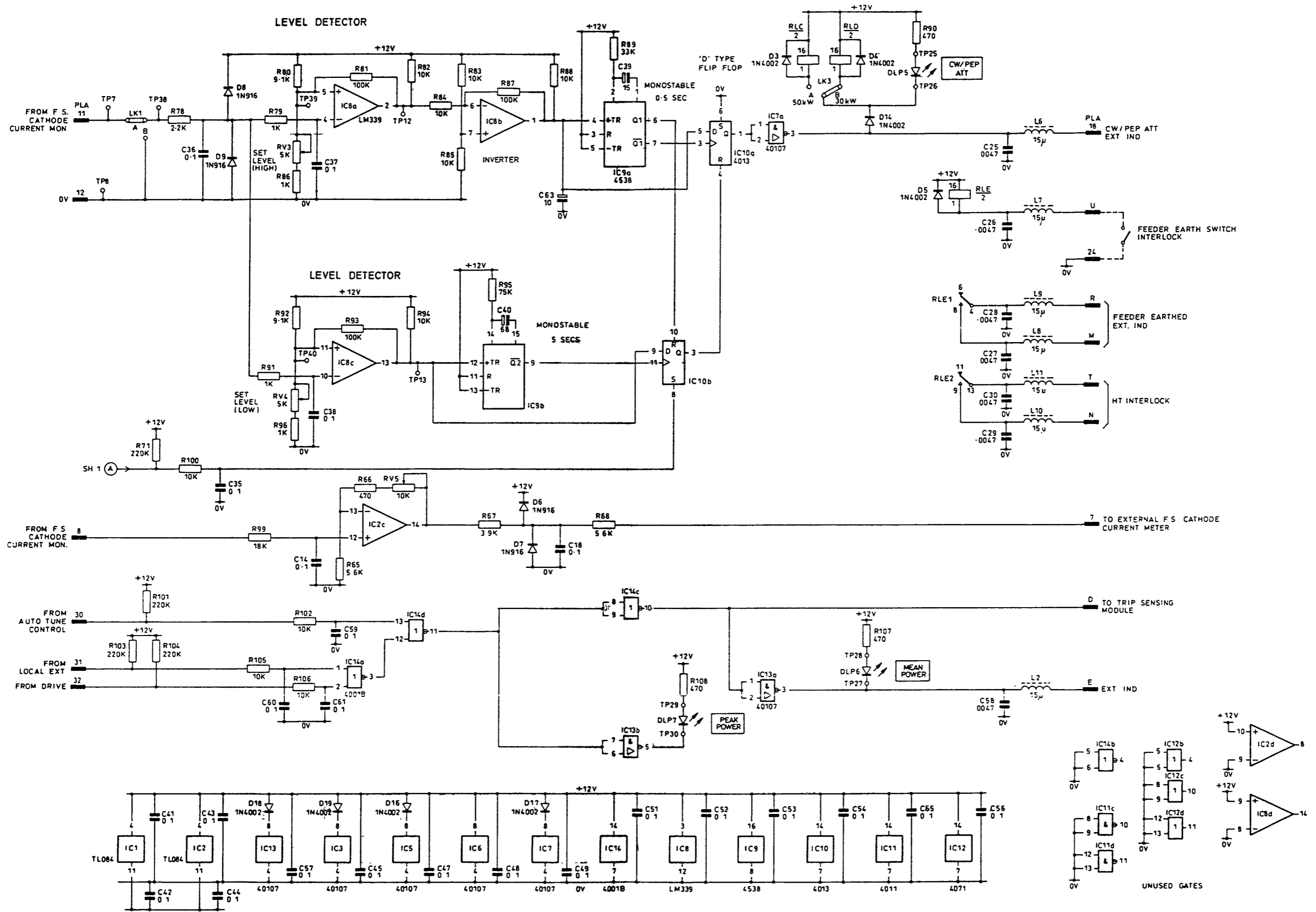
Module, vswr and attenuator 5820-99-593-2379: circuit diagram

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INC MODS RM093/2, RM094/2

Fig D22-1

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INC MODS RM093/2,094/2

Fig D22-2

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Module, vswr and attenuator 5820-99-593-2379: circuit diagram

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Fig D22-2

Sub sect D22

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