AIR PUBLICATION

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and Vol. 6, Sect. 1.

I.F.F. MK. 10 (GROUND)

GENERAL AND TECHNICAL DESCRIPTION AND DATA FOR THIRD LINE SERVICING

BY COMMAND OF THE DEFENCE COUNCIL

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Ministry of Defence

FOR USE IN THE
ROYAL AIR FORCE

(Prepared by the Ministry of Technology)

A.L.48, Mar. 69

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LIST OF ASSOCIATED PUBLICATIONS

(BRITISH)

	Air Publication
Inter Services radar manual	A.P.1093E

(AMERICAN)

	Technical Order
Radar recognition set AN/UPX-6	
Operation and service instructions ...	T.O.31P4-2UPX6-1 (formerly CO.16-30UPX6-2)
Maintenance instructions	T.O.31P4-2UPX6-2 (formerly CO.16-30UPX6-3)
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GENERAL INFORMATION

Chapter 1

INTRODUCTION

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General

1. IFF Mk. 10 is a secondary radar system designed to identify as friendly or enemy objects those targets detected by the search radar with which it is associated. The system employs the same basic principles as earlier marks of IFF equipment, i.e., a pulse transmitter interrogates the target. If the target is fitted with the appropriate transponder, a reply is sent back to the interrogator receiver. The U.K. system is an adaptation of the one which has been in service in the U.S.A. for a number of years.

2. As in the case of the Mk. 3 equipment, IFF Mk. 10 employs special IFF frequencies and operates in the band 950 to 1,150 Mc/s. The new system is, however, designed to provide greater efficiency and operational flexibility than hitherto. This is achieved by using the basic interrogator in conjunction with a variety of control equipment to give the desired facilities.

Facilities of the Mk. 10 system

3. The most important features of the Mk. 10 system are as follows:—

(1) Spot frequency operation on two separate channels within the 950 to 1,150 Mc/s band for interrogators and transponders. One channel is employed for interrogation and the other for reception of the reply signal. Transponders continue to reply as long as interrogations are received from the ground station, whereas in Mk. 3 IFF the whole frequency band is continuously swept.

(2) The use of selective coded interrogation. Transponders decode the interrogations received and reply only to those interrogators transmitting the appropriate code.

4. The selective coding feature is afforded by the provision of three modes of interrogation of the transponder, to meet different operational requirements. In effect, these modes are equivalent to three interrogation codes. By their use, specific friendly targets may be identified individually. All three modes have corresponding reply signals and these are illustrated in fig. 1 as they appear on the radar display. In addition, facilities exist for emergency or distress replies.

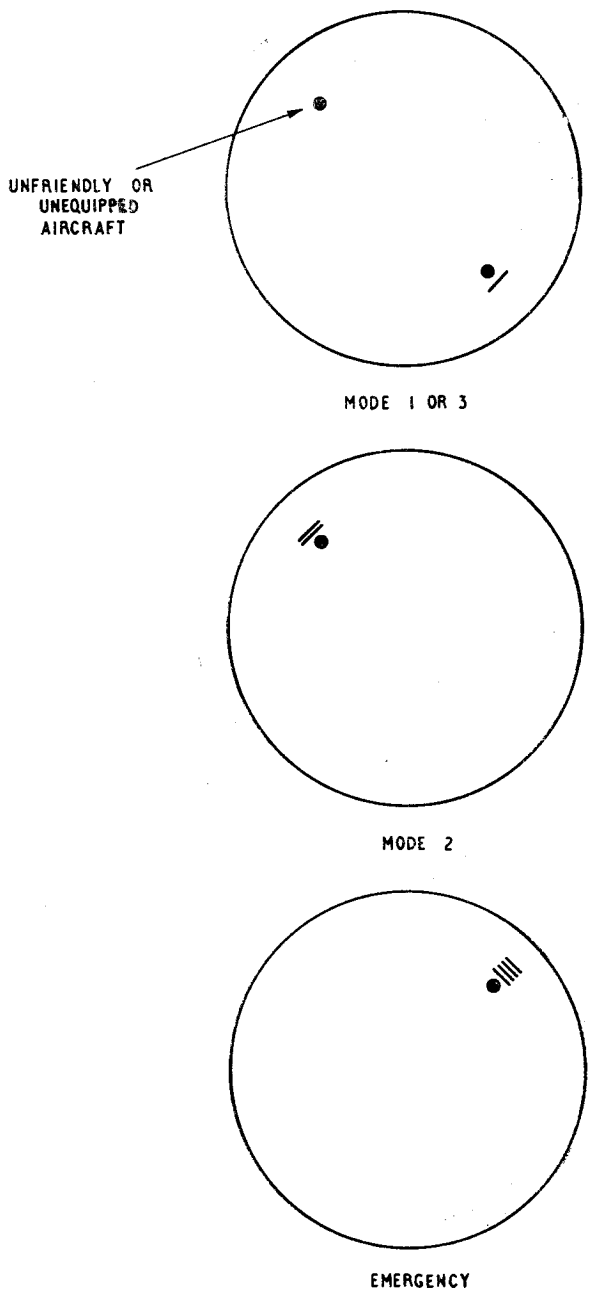

Fig. 1. PPI display with radar target and IFF response

5. Transponders can be switched to reply to the following combinations of interrogation modes: 1; 1 and 2; 1 and 3; 1, 2 and 3. It will be observed that operational transponders always reply to mode 1 interrogation.

Mode 1

6. This mode is intended for general use. The interrogating signal consists of a pair of one microsecond pulses with three microseconds spacing between the leading edges. Interrogators operating in mode 1 receive a single pulse reply from all transponders within range and this applies even though the transponders are replying to interrogators using other modes.

Mode 2

7. Mode 2 is intended for detailed recognition. Here again, the interrogating signal consists of a pair of one microsecond pulses but with five microseconds spacing between the leading edges. Airborne transponders return a two-pulse reply with 16 microseconds spacing between leading edges while shipborne transponders return a one-pulse reply. Interrogators operating in mode 2 receive replies from transponders switched to reply to mode 2 interrogation.

Mode 3

8. This mode is also intended for detailed identification such as the functional class of an aircraft. The interrogating signal is a pair of pulses with eight microseconds spacing between leading edges and the reply is the same single pulse used in mode 1. Confusion through duplication cannot arise however, since interrogators operating in mode 3 will receive replies only from those transponders switched to reply to mode 3 interrogation and locked or synchronized mode 1 signals will not appear on the display.

Emergency signal

9. By the operation of a special switch provided in the aircraft, the transponder can be set to radiate a characteristic four-pulse code irrespective of the mode of interrogation. These pulses are spaced at 16 microseconds intervals.

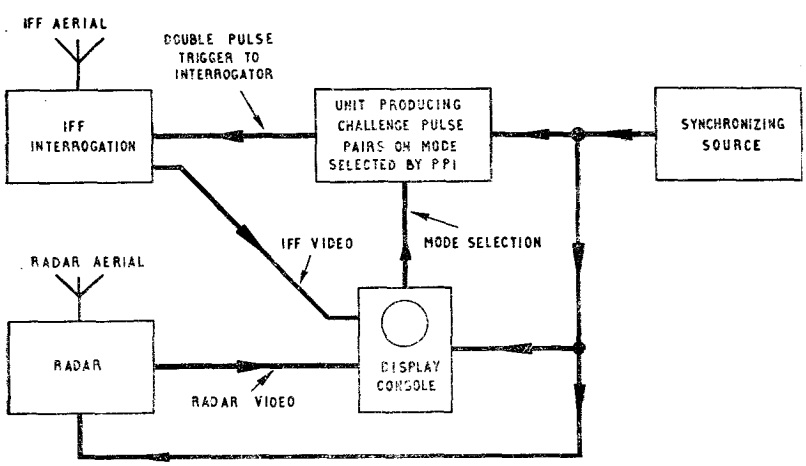

Fig. 2. Mk. 10 installation with one display: block diagram

10. The foregoing paragraphs describe the basic coding facilities provided in all Mk. 10 installations. By the inclusion of additional units it is possible to extend these facilities so that a large number of reply codes is available in response to each of the interrogation modes.

Reply pulse characteristics

11. At present the standard duration for IFF Mk. 10 reply pulses is one microsecond but it is probable that all future transponders will radiate half-microsecond pulses. No decision has yet been reached whether existing equipment will be modified.

12. When a transponder is interrogated, it will give a synchronized response at the appropriate range on the display as described in para. 6 to 8. Where the transponder is not switched to the particular mode of interrogation (mode 2 or 3), no synchronized reply is given. If however, the transponder is simultaneously interrogated by a number of ground stations operating on different modes, it will return synchronized responses to those interrogators transmitting the modes to which the transponder is switched. On all other displays within range such responses will appear as unsynchronized signals. The unsynchronized signals will normally be confined to the sector over which the synchronized reply would appear and will be seen as chains of dots, the exact pattern depending upon the p.r.f. relationship involved.

Equipment

13. The Mk. 10 system of interrogation may be employed with a variety of aerial and interrogator equipment but the purpose of this publication is to describe the use of the American UPX6 interrogators and aerial system AS295 in conjunction with U.K. control equipment. The function of the control gear is to

(1) Generate interrogation pulse pairs with the appropriate spacing, synchronized to the radar repetition frequency.

(2) Provide a combined display of IFF and radar signals.

14. Depending upon the facilities desired, the complexity of the control system can vary between wide limits. The simplest installation, using only one radar head and one display, is illustrated in the block diagram of fig. 2. In this case, only one mode would be called for at any time.

15. Where numerous displays are involved, requiring different modes of interrogation, provision must be made for the selection and transmission of the desired mode. This may be achieved in one of several ways.

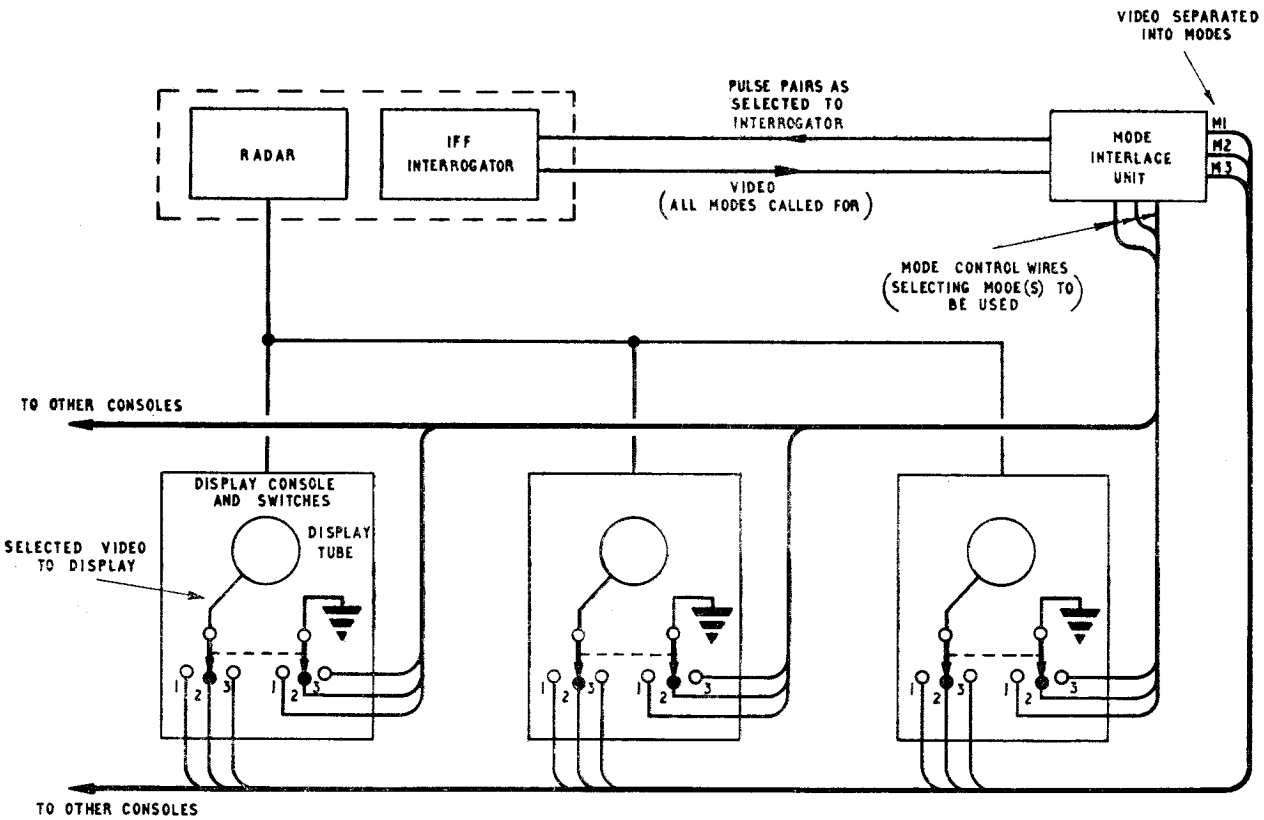

Fig. 3. Mk. 10 installation with multiple displays: block diagram

16. A priority system may be used where mode 1 is transmitted at all times except when either mode 2 or 3 is called for, in which case one or other of these modes is transmitted at all times instead of mode 1. This method has the disadvantage that the full range of facilities is not available to each operator, but it has been used in certain American installations and has an application to Army tactical control radar.

17. Alternatively, an interlacing system may be adopted in which modes 1, 2 and 3 are transmitted cyclically so that the operator can select the desired response. Such an arrangement involves wastage of time since interrogations are made in all three modes even when only one mode is required. The facility is however, incorporated in the UPX1 interrogator which is employed in Naval installations.

18. Another method of interlacing can be used in which only those modes selected by operators are transmitted. This method utilizes the available time to the best advantage and is the one which has been adopted by the R.A.F.

19. The unit which provides the interlacing facility is known as waveform generator 6010. Its purpose is to produce the necessary pulses for the interrogation mode selected by the PPI operator and to route the correct video response to each PPI via relay switches on the associated relay rack.

20. In practice, the foregoing is but a small advance on the simplest installation mentioned in para. 14 and represents only a portion of the whole range of facilities which are available, since the system is designed to operate with more than one radar head and interrogator to provide information for a large number of PPI displays.

21. Where it is desired to display IFF responses on several consoles as in the block diagram of fig. 3, the scale of basic equipment required in addition to the UPX6 interrogator is as follows:—

(1) One or more interrogator control units for remote control of the interrogator(s) from the radar office.

(2) One or more waveform generators to produce the necessary triggering pulses for the interrogator(s).

(3) One or more relay units to provide the necessary switching facilities between the display consoles and the radar heads.

22. The use of IFF Mk. 10 is not confined to static installations and it can be adapted to mobile equipments. A typical convoy might consist, for example, of a group of vehicles with two radar heads and two operations vehicles each containing two PPI display consoles. If IFF information is required to be fed from each head to all the consoles, the appropriate control equipment will be necessary and for this purpose a separate vehicle,

radio vehicle Type 511, has been designed. RVT 511 contains approximately the same control equipment as is normally located in the radar office but it is differently mounted owing to the restricted space available.

23. To obtain full flexibility, irrespective of the number of operations vehicles in a convoy, it is necessary to provide one RVT 511 for each operations vehicle Type 510. Each RVT 511 contains the relay unit and junction boxes for its associated RVT 510 and the IFF vehicles are themselves interconnected by video and control cables. The RVT 511 at one end of the chain of vehicles would provide mode interlacing facilities for one interrogator and, via the relay units in all the Type 511 vehicles in the convoy, would distribute IFF video to all the PPI consoles.

24. If the convoy is equipped with two interrogators, another waveform generator is necessary. This may be either the second unit in the RVT 511 already mentioned or it may be one of the two located in the corresponding vehicle at the other end of the chain. Since every RVT 511 carries a full complement of equipment, it is clear that, in large convoys, much of it would be spare but it is unlikely that a combination exceeding three each of RVT 510 and RVT 511 will ever be required.

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Chapter 2

RADAR HEAD ASSEMBLY

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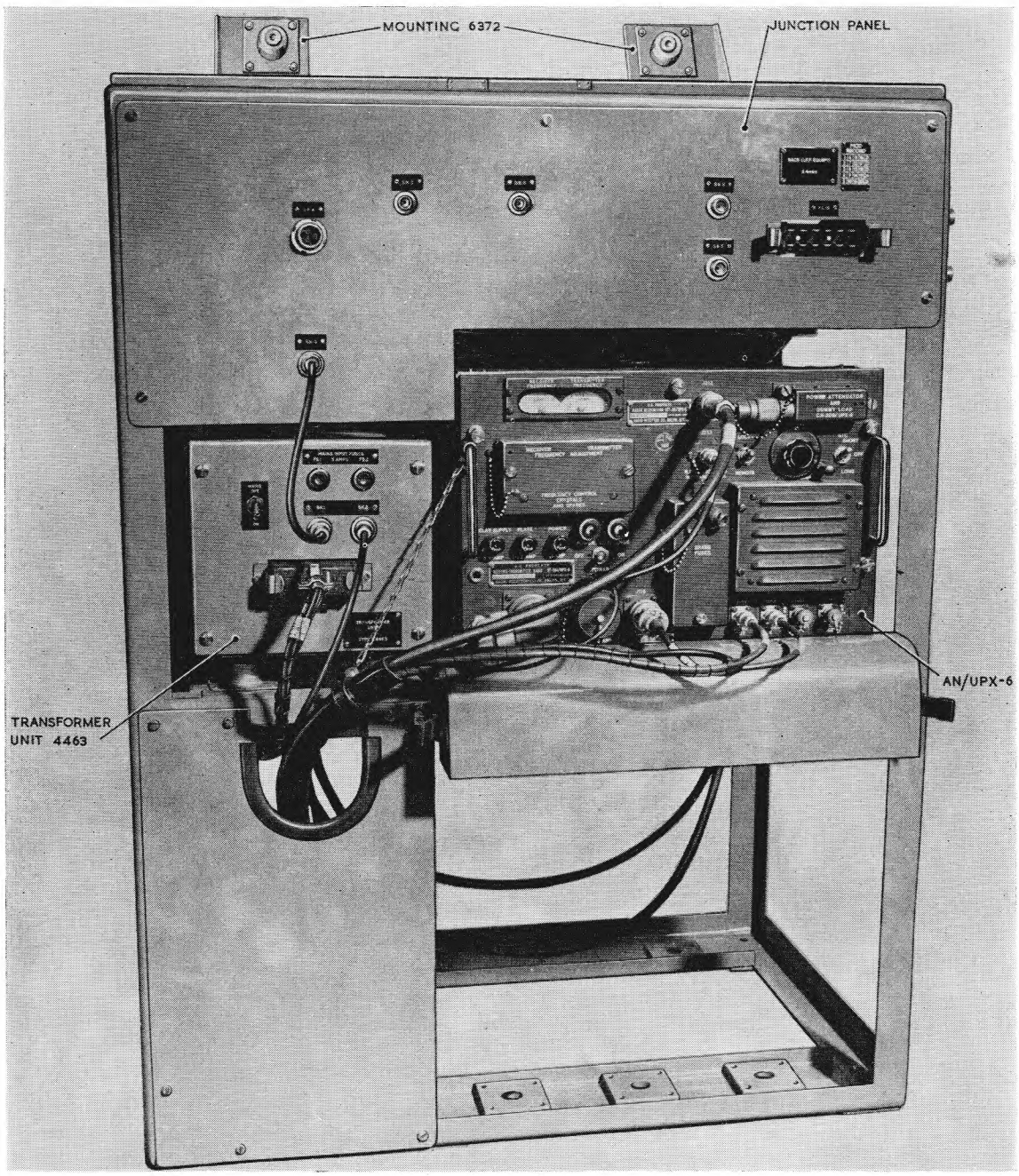

Fig. 1. Rack (IFF equipment) 4464: front view

General

1. The basis of any IFF ground installation is a unit containing a transmitter and receiver, known as an interrogator/responsor. As stated in Chapter 1, the British IFF Mk. 10 system employs the American-designed radar recognition set AN/UPX-6 which consists of transmitter-receiver RT-264/UPX-6 and transmitter-receiver cover CW-286/UPX-6.

2. The following is a brief summary of the characteristics of the interrogator:—

Transmitter

Type	Direct crystal control
Frequency range	990 to 1040 Mc/s
Normal operating frequency	1030 Mc/s
Nominal power output	1·5 kW peak
Pulse duration	1 microsecond
Output impedance	52 ohms

Receiver

Type	Superheterodyne with direct crystal control
Frequency range	1080 to 1130 Mc/s
Normal operating frequency	1090 Mc/s
Intermediate frequency	60 Mc/s
Overall bandwidth	8 to 11 Mc/s at 6dB below maximum
Input impedance	52 ohms
Video output level	4V minimum across 75 ohms, nominally limited at 8V
Dimensions of complete unit	Height 19 in. Width $15\frac{1}{4}$ in. Depth $9\frac{3}{4}$ in.
Weight	77 lb.

3. A full description of and servicing information for this unit will be found in the American handbooks 31P4-2UPX6-1 and 2.

RACK (IFF EQUIPMENT) 4464

General

4. The method of mounting the AN/UPX-6 interrogator in any ground station depends upon the particular search radar with which it is associated but one possible arrangement is shown in fig. 1 and 2. These illustrate rack (IFF equipment) 4464 employed in radar Type 14 Mk. 7, 8 and 9 and in radar Type 79 installations.

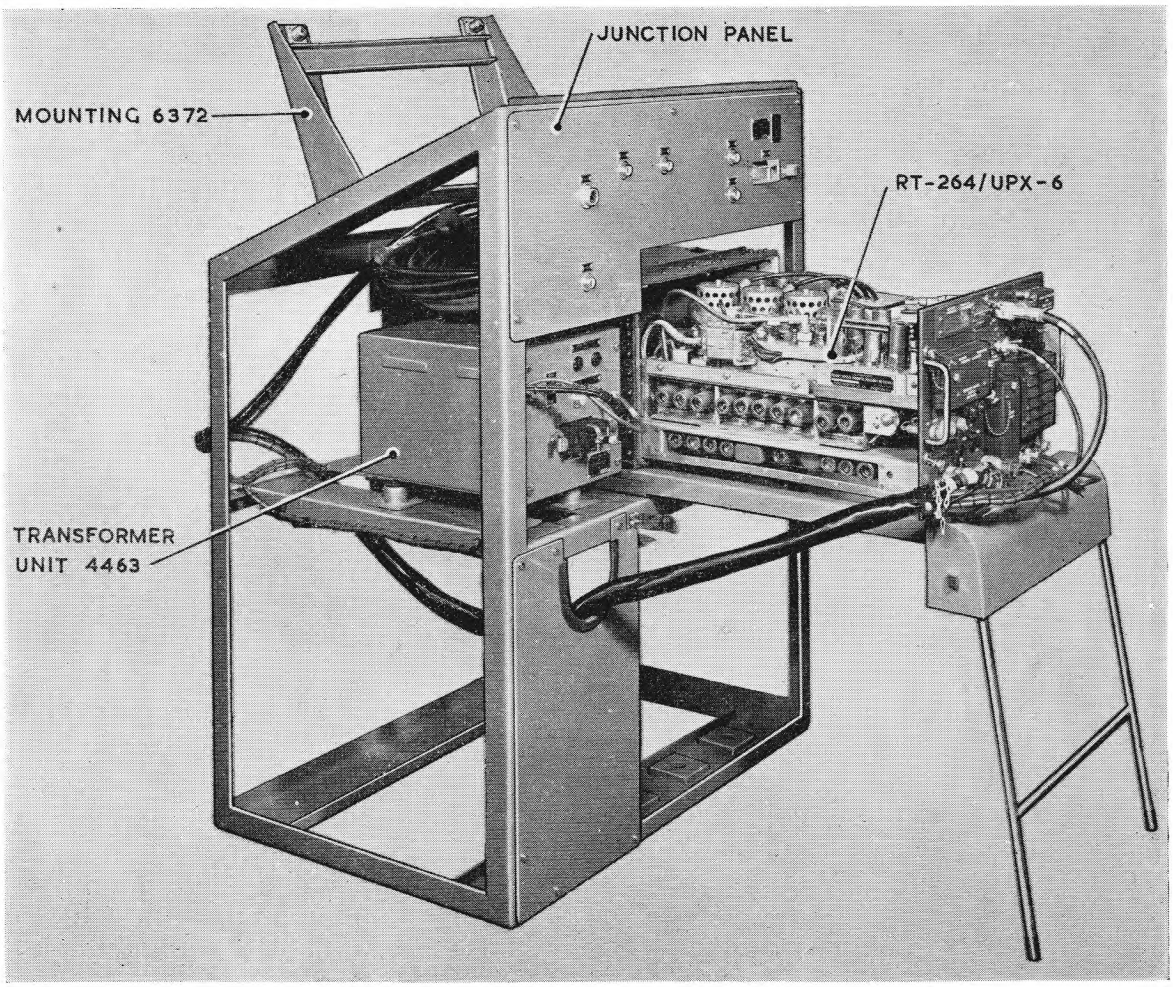

Fig. 2. Rack (IFF equipment) 4464: view showing interrogator withdrawn for servicing

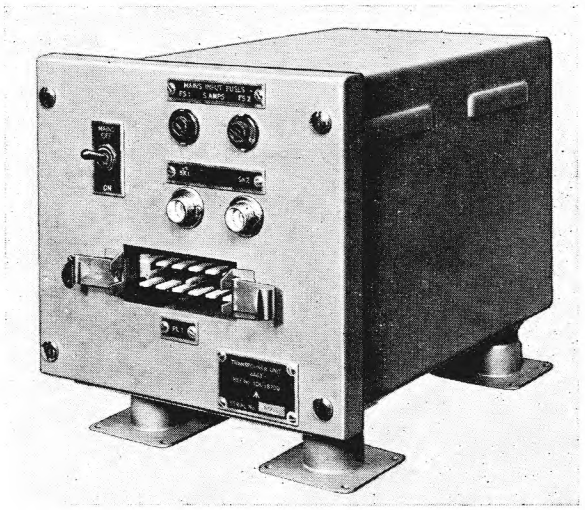

Fig. 3. Transformer unit 4463: general view

5. The rack consists of a pressed steel angle-section framework with a horizontal centre frame of similar construction to carry the units. The interrogator is mounted at the right-hand side of the centre frame and below it is a separate angle frame which is arranged to slide forward. In this position it is supported by a tubular steel frame pivoted at the front corners. The transmitter-receiver can thus be withdrawn from its cover for servicing without the necessity of removing the entire unit from the rack.

6. To the left of the interrogator is mounted transformer unit 4463 while at the top front of the framework is a junction panel for the incoming and outgoing services. The top of the rack slopes to the rear and carries a mounting 6372 for test set 4339. Ample space is available at the bottom of the rack for additional equipment and, in the Type 14 and 79 installations, it houses a unit not associated with IFF Mk. 10.

7. Rack (IFF equipment) 4464 is located in the cabin which contains the search radar head, input and output connections to the IFF equipment being made via the main slipring unit. Operation of the interrogator is remotely controlled from the radar office.

Transformer unit 4463

8. The American interrogator is designed to operate from sources of 105V, 117V or 125V, 60-400 c/s, single-phase a.c. and the normal U.K. supply of 230V requires to be stepped down before application to the unit. For this purpose transformer unit 4463, illustrated in fig. 3 and 4, is provided.

9. It should be noted that although the American UPX-6 is designed to operate from a.c. sources at all frequencies between 60 and 400 c/s it is not intended for use at frequencies below 60 c/s. When it is used with the U.K. 50 c/s supply some reduction in the permissible ambient temperature rating is inevitable. Provided the ambient temperature within the cabin housing the UPX-6 is not greater than 57 deg. C, satisfactory operation is possible but where the temperature is liable consistently to approach or exceed this value the alternative use of the British version of the interrogator, RT264/UPX-6 (MSA) is advised. The British unit is rated for use at ambient temperatures up to 60 deg. C at 50 c/s.

10. The transformer unit contains a step-down transformer from 230V to 117V designed for operation at frequencies between 45 and 65 c/s (*fig.* 5). The 230V input is brought in on pins 11 and 12 of the 12-pole plug and fed, through fuses FS1 and FS2 and a thermal cut-out XI, to the transformer primary and on pins 7 and 8 for connection to PL19/7 and PL19/8. The 117V output is brought out on pins 5 and 6 of PL1 for connection to the interrogator.

11. Across the secondary of TR1 is connected a rectifier/filter circuit consisting of the metal rectifier MR1, resistor R1 and capacitor C1. The resultant d.c. output is applied to the coil of a relay RLA. Relay A has two changeover springsets, one of which is connected in the trigger pulse input circuit. When the equipment is switched on, contacts 22/23 make and the trigger pulse is fed to the interrogator. Immediately the 230V source is switched off, relay A is de-energized and contacts 22/23 break. The trigger pulse is thus removed before the interrogator cools down thereby preventing possible damage to the modulator and RF amplifier valves. In the de-energized condition of RLA the trigger pulse input cable is terminated by R2 through contacts 22/21 so that the pulse may be monitored at the radar head without the necessity of switching on the interrogator. The other changeover springset on RLA is not used but the contacts are connected to pins on PL1 in case the facility should be required.

12. Transformer TR1 is rated at 320W which is in excess of the power required by the UPX-6 (250 W). The transformer unit may thus also be used to supply the 135 W required by the American test set AN/UPM-6 for periods of up to $1\frac{1}{2}$ hours' continuous operation.

Interconnections

13. An interconnection diagram for rack (IFF equipment) 4464 is given in fig. 6. Transformer unit 6428 shown on this diagram is an aerial heater unit for use in conjunction with aerial array 4992. Both aerial and heater have a very limited

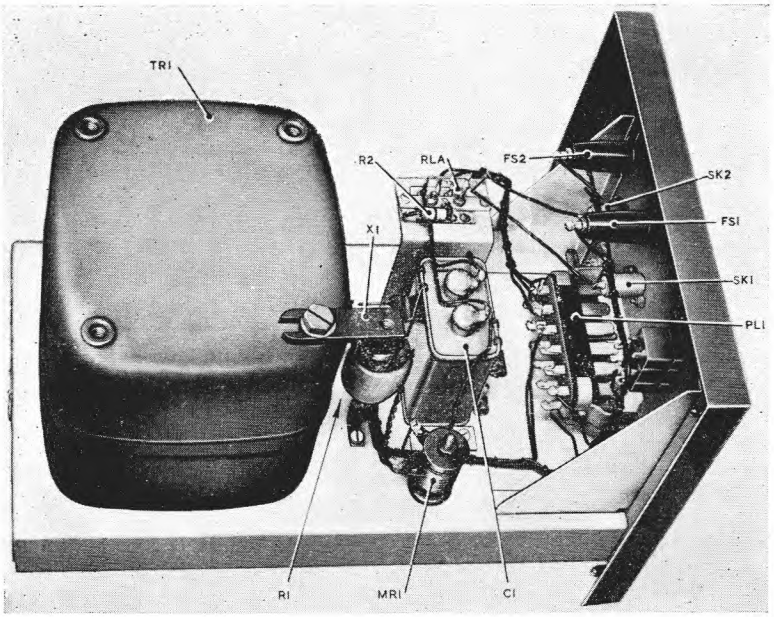

Fig. 4. Transformer unit 4463: interior view

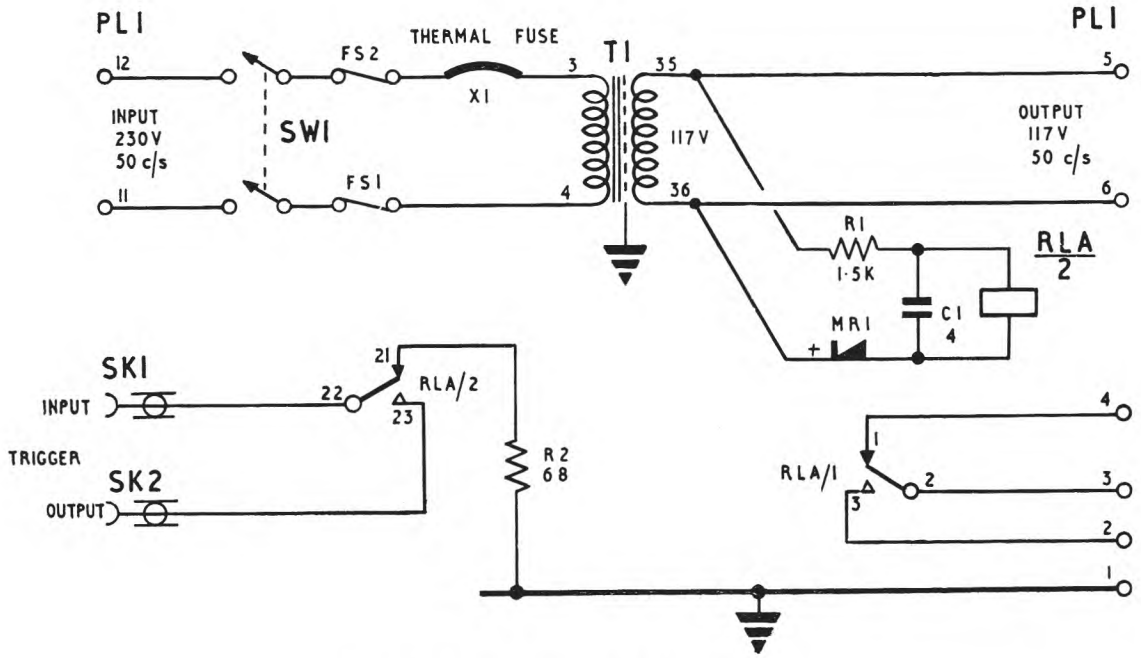

Fig. 5. Transformer unit 4463: circuit

application so that the transformer is not normally fitted in the rack. Since accommodation and the necessary connections for it are provided, however, it is included in the interconnection diagram. Details of transformer unit 6428 will be found in Sect. 2, Chap. 7.

AERIAL SYSTEM

14. The radar head assembly necessarily includes the IFF aerial which initially, in most installations, will be the American aerial AS-295A/UP. This aerial is designed for the transmission and reception of vertically polarized waves in the 950 to 1150 Mc/s band and consists of a broadside array with 24 slot radiators, each slot being excited by a vertical probe connected to the feeder system. The vertical beam width is approximately 40 deg. and the horizontal beam width $4\frac{1}{2}$ deg., both measured between the half-power points.

15. The feeder system, which forms part of the aerial array, includes a filter for the suppression of S and X-band interference and a coaxial aerial

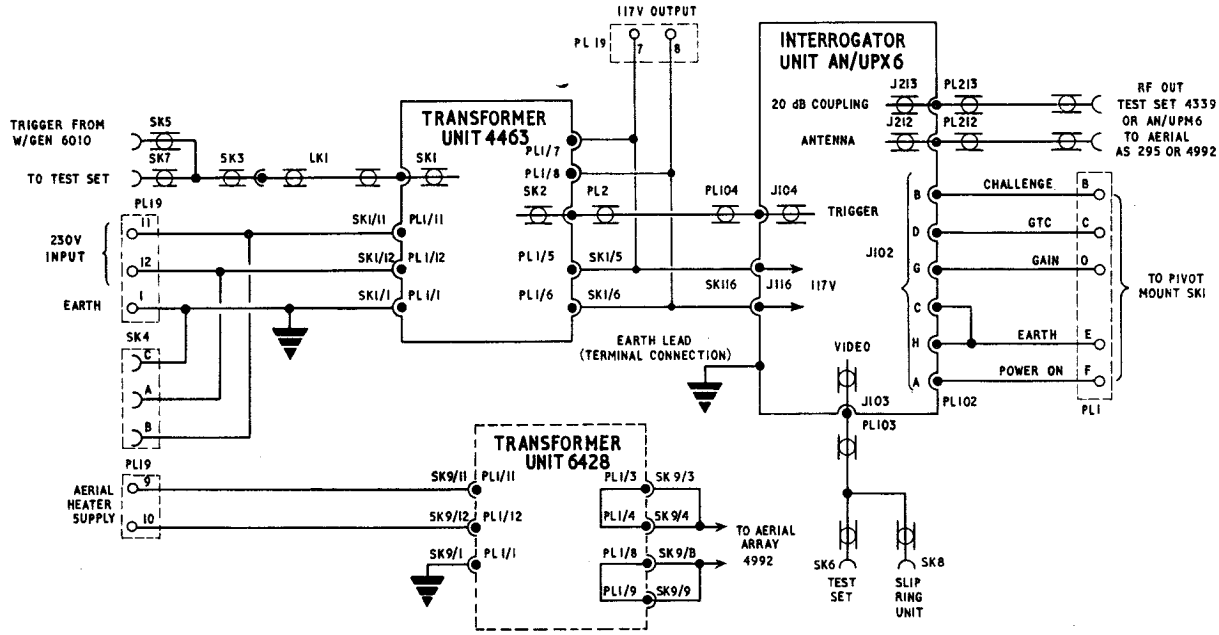

Fig. 6. Rack (IFF equipment) 4464: interconnection diagram

coupler to permit the use of standard coaxial cable between the interrogator and the aerial. Aerial assembly AS-295A/UP measures approximately 18 ft 16 in long × 13½ in high × 9½ in deep and weighs 101 lb. It is fully described in the American handbook 31P4-2GPX-121.

16. The mounting position for the aerial will depend on the particular search radar with which it is associated but, in general, it will replace the IFF Mk. 3 aerial on top of the reflector frameworks of the various radars. Typical mounting positions are shown in the illustrations in Sect. 2, Chap. 9.

17. A British equivalent of the AS295, aerial array 4992, is also available. Mechanically and electrically this is a direct replacement for the American aerial. Initially, however, aerial 4992 will be fitted only to mobile radars Type 14 and 15 deployed outside the N.A.T.O. area although provision has been made for its possible eventual use on all radar heads (other than Type 80) within the N.A.T.O. area.

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Chapter 3. — MOBILE INSTALLATIONS

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LIST OF ILLUSTRATIONS

General

1. When a convoy with IFF Mk. 10 facilities is assembled, the RVT 511 operates in conjunction with the RVT 510 which contains the display consoles. Each RVT 511 is provided with a single relay unit 6009 and thus provides switching facilities and video information for two consoles only. In consequence, every RVT 510 in a convoy requires its complementary RVT 511.

2. The number of vehicles Type 511 in a convoy is determined by the operational requirements and the extent of the IFF facilities desired. One RVT 511 is required for each RVT 510 in the convoy, the maximum number being three as, in practice, capacitance and waveform distortion limitations due to the shunting effect of the video lines to the various display vehicles (which have partial terminations only on the consoles) make it impracticable to employ more than three IFF vehicles. The termination pads, through which the lines to the relay unit 6009 are fed, are included to assist in reducing the distortion of pulses (particularly SIF pulses) caused by the shunted video lines. Inevitably however, they introduce loading of the main 70-ohm coaxial cables at each vehicle.

3. Fig. 1 shows the situation when three vehicles are connected. There is, effectively, a 300-ohm shunt across each video line in each vehicle with an additional 100-ohm shunt in the end vehicle. The combined value of the 300 and 100-ohm shunts in this end vehicle provides a 75-ohm termination to the interconnecting cable. When one or two spur lines are connected, by a relay unit 6009, to the associated RVT 510, the lower half of the 300-ohm pad concerned is shunted by the complex impedance of the line or lines. These have a characteristic impedance of 70 ohms but

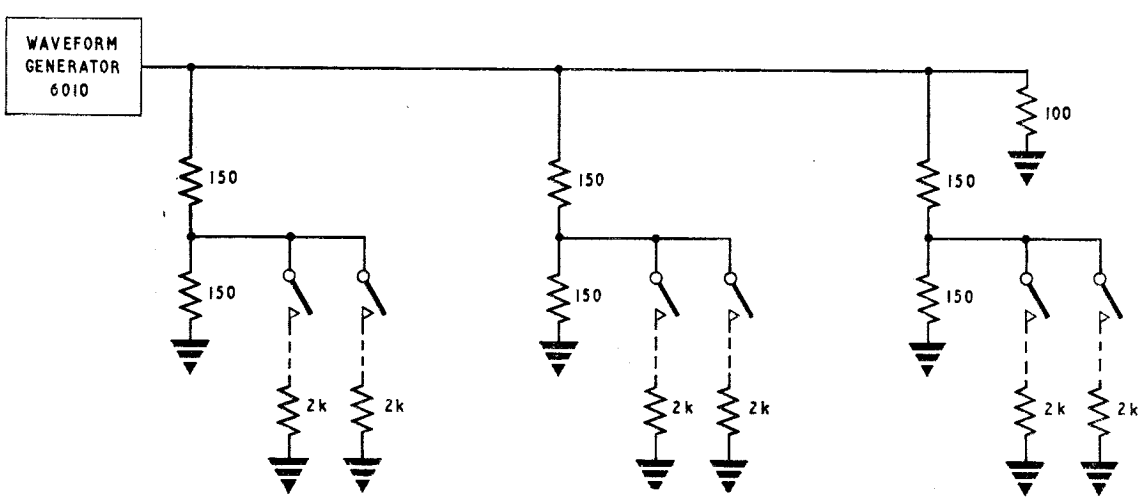


Fig. 1. Video cable loading by spurs to Type 510 vehicles

are electrically short and each is terminated by 2000 ohms.

4. Irrespective of the number of vehicles Type 511 in a convoy, only two IFF channels are provided, one for each of two interrogators installed in radar heads facing in opposite directions and associated with radar channels 1 or 2 and 3. In consequence, only two waveform generators 6010 are used and these are selected from the end vehicles in the chain. Fig. 2 shows, in block diagram form, some of the possible combinations. It should be noted that the waveform generators in a centrally connected RVT 511 are never used since this would require video signals to be fed in two directions simultaneously. The operational waveform generators may both be in one vehicle or, if for any reason it is more convenient, one unit in each of the end vehicles can be employed. When the operational waveform generators are in separate vehicles it is important to remember that corresponding units cannot be used. The arrangement must always be as shown in fig. 2, *i.e.* unit 2 in one vehicle and unit 5 in the other.

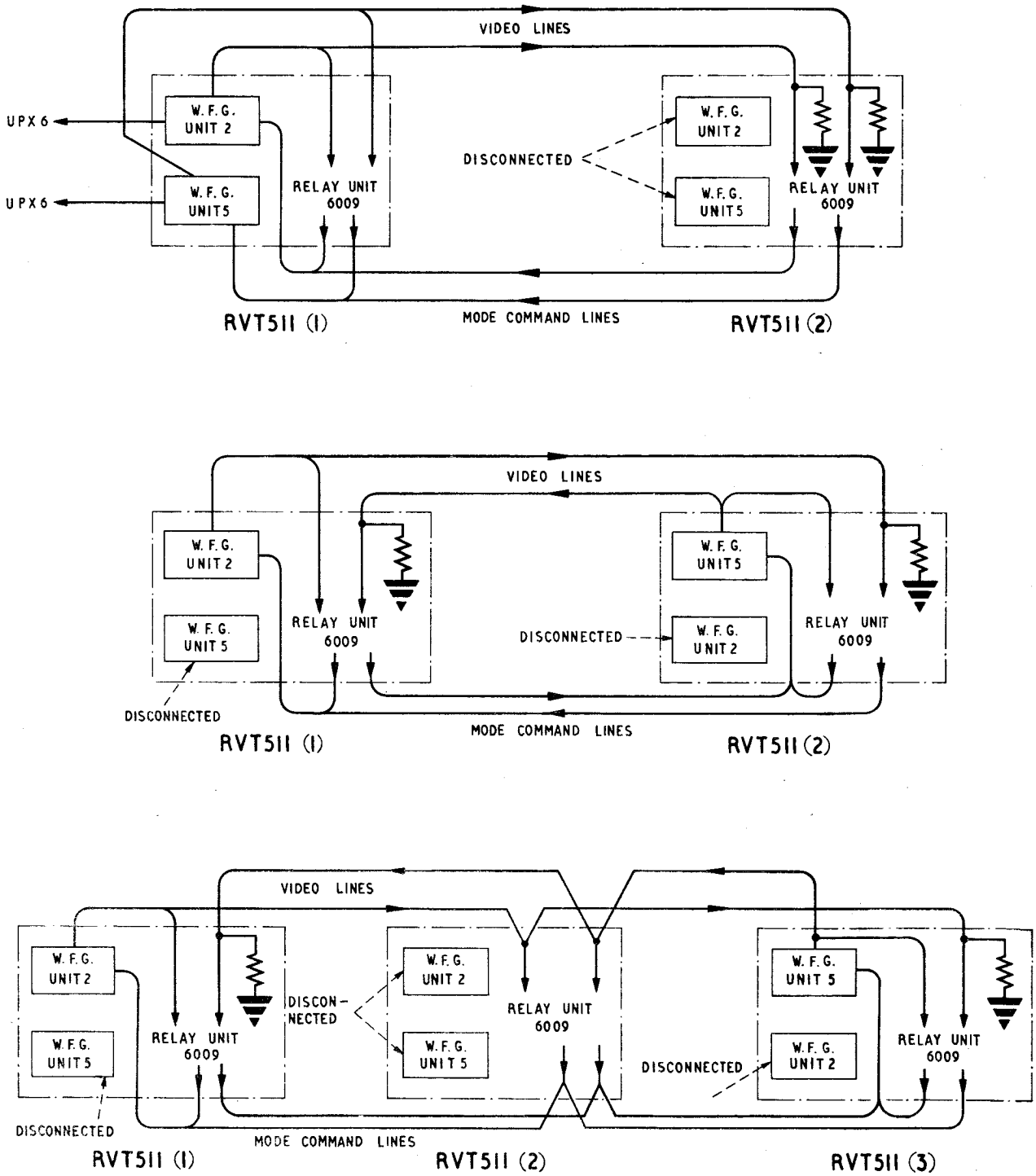


Fig. 2. Possible RVT 511 combinations

Mode and video switching

5. When the two waveform generators to be used have been selected, the video and mode command control switches for these units are set to IN. The switches are designated CHANNEL 1 or 2 WAVEFORM GENERATOR 6010 and CHANNEL 3 WAVEFORM GENERATOR 6010 and are located on the central control panel on rack (IFF control) 4470. All the other video and mode command switches must be set to OUT.

6. The IFF video circuits in the vehicles Type 511 are coupled by a series-connected 7-way video cable for which a termination is required at one end or the other; this is achieved through the LINE TERMINATIONS switches mounted immediately above the video and mode command control switches. If both waveform generators are in the one vehicle, then the LINE TERMINATIONS switches in the vehicle at the opposite end of the convoy are set to IN. All other termination switches must be set to OUT.

7. Where the waveform generators are in different vehicles, *i.e.* unit 2 in one vehicle and unit 5 in the other, then the LINE TERMINATIONS switch for unit 2 in the vehicle containing the operational unit 5 must be set to IN and the corresponding switch for unit 5 in the vehicle containing the operational unit 2 also set to IN. All other termination switches must be set to OUT. In a convoy which has only one RVT 511 both LINE TERMINATIONS and video and mode command control switches are set to IN.

Interlace synchronization

8. The necessity for synchronizing interrogators on a fixed site is explained in Sect. 2, Chap. 2, para. 49 and 50 and the same considerations apply with equal force to a mobile installation. Thus, the interlaced outputs of the waveform generators in the Type 511 vehicles must be synchronized.

9. On a fixed site, all the IFF control equipment is housed in the radar office and the master waveform generator is connected directly to the slave units through the rack cables. Since no great length of cable is required, there is no appreciable loading of the synchronizing circuits. Also, on a site associated with a remote Type 7, the synchronizing pulse is fed into a mixer amplifier at the remote site and, on arrival at the main site, is fed into a separator amplifier so that, here again, no loading problem arises.

10. In a mobile installation with more than one RVT 511 however, the long cable runs required introduce considerable capacitive loading with consequent attenuation of the synchronizing waveform. To overcome this, the transformer assembly described in the preceding chapter is provided. Each unit in the assembly is an auto-transformer with a ratio of 3 : 1 and is connected to give a step-up or step-down depending upon whether the associated waveform generator is the slave or master. The arrangement helps to reduce the source loading as well as the impedance mismatch due to the cable and ensures that the synchronizing pulse into the slave waveform generator is of sufficient amplitude. Where both waveform generators are in the same vehicle the transformers are not required and the units are interconnected directly via two coupled sockets on the cover of the transformer box.

11. The transformer connected between the cable and the slave waveform generator (*Chap.* 2, *fig.* 6) has a crystal diode in parallel with the windings and a second diode in series with the output. These diodes are included to prevent feedback between the waveform generators. The negative synchronizing waveform cuts off the shunt diode and is passed by the series diode to the slave unit. Any positive excursion, produced either by the regenerative action of the counter circuit in the slave waveform generator or by reflection in the cable, causes both diodes to conduct and thus cannot affect the synchronization. The connections are the same as those in a static installation, *i.e.* the output transformer is coupled to SK8 on the master unit and the input transformer to SK9 on the slave waveform generator.

Channel selection

12. Provision is made for each of the two consoles in an RVT 510 to select the desired channel. This is achieved through relay unit 6009 in the normal manner (*Sect.* 2, *Chap.* 4, *para.* 9) but there is no head selector unit in the mobile installation. The control switches in the RVT 510 are consequently connected in series with the 50 V supply to two relays RL 1 and RL 2 in rack 4470 (*Chap.* 2, *fig.* 8). Normally both consoles receive channel 1 or 2 information. When the appropriate switch in the RVT 510 is closed, RL 1 or RL 2 is energized so that the contacts make and apply 50 V to terminal A/B or H/J on the relay unit. That particular console then receives channel 3 information.

Convoy dispersal

13. A block diagram of a single RVT 511 convoy is given in fig. 3. Fig. 4 and 5 are video and mode switching interconnection diagrams for a three-vehicle convoy.

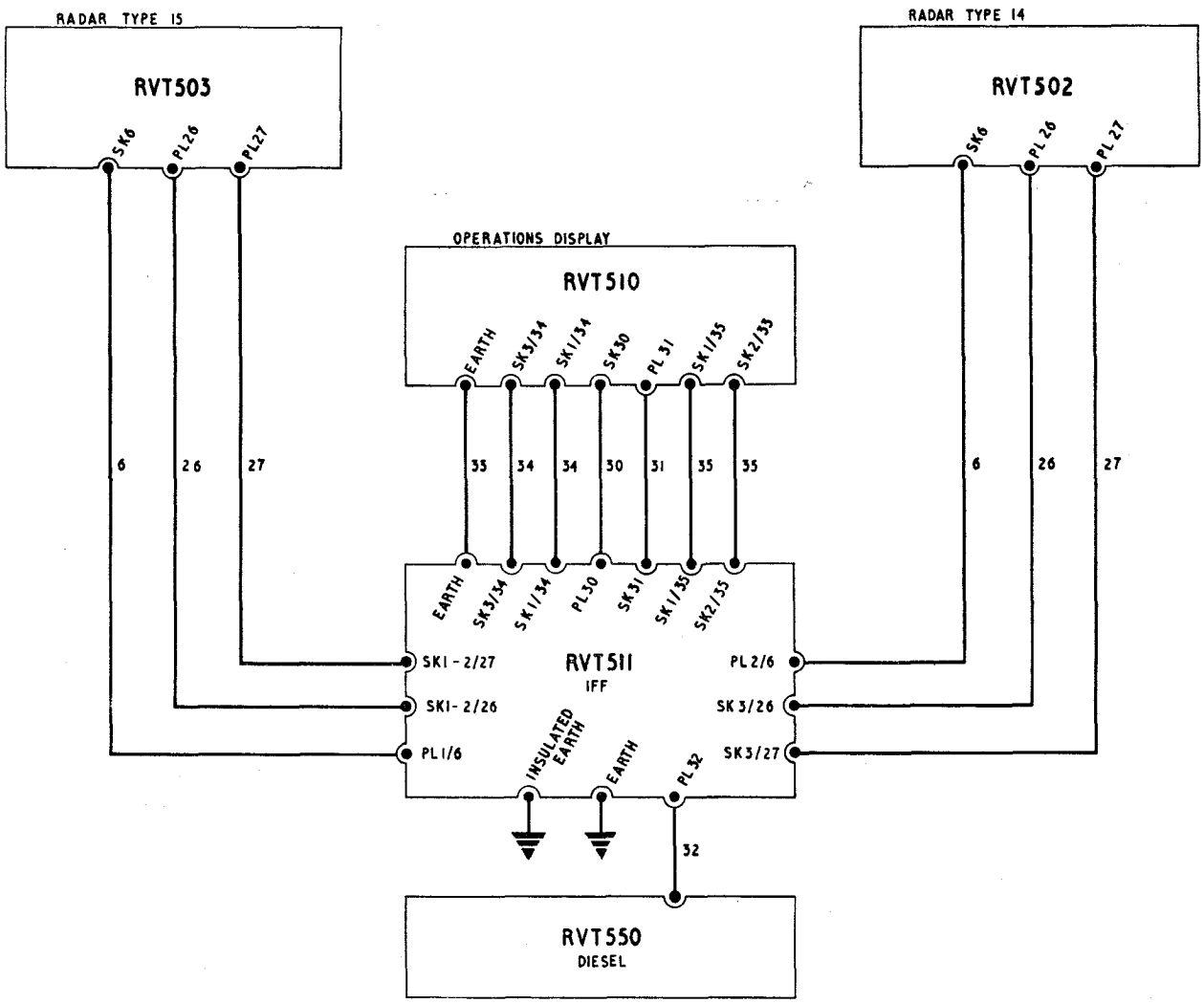
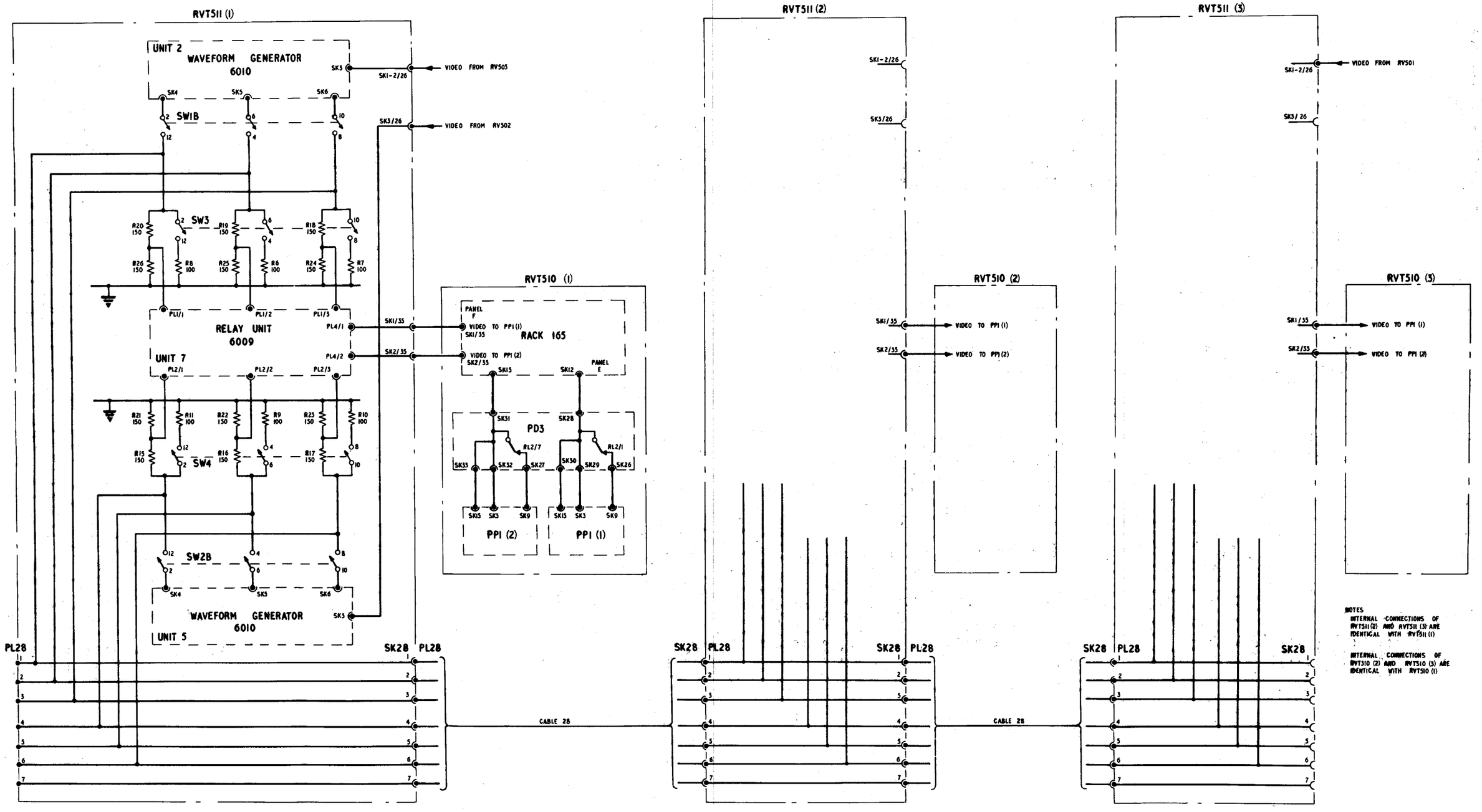
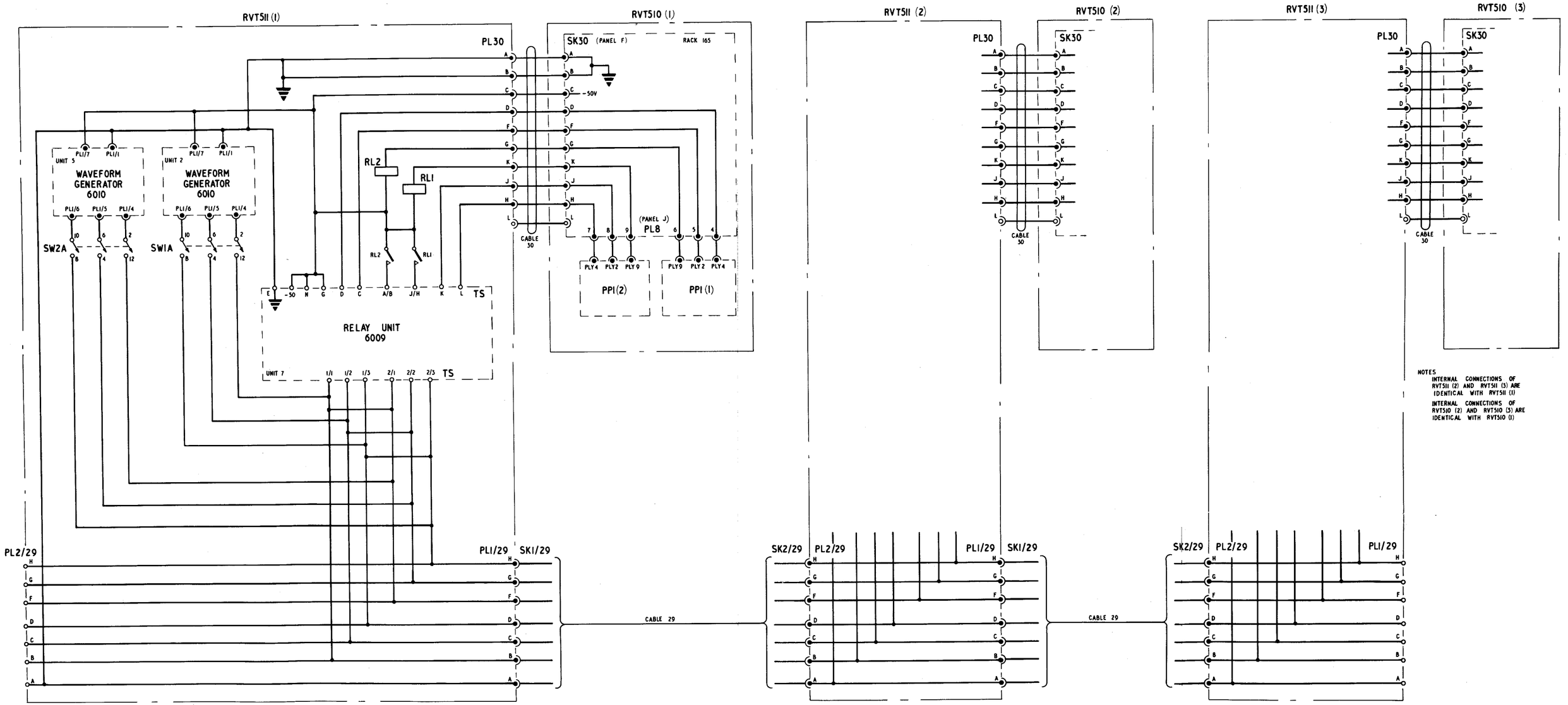


Fig. 3. Single RVT 511 convoy: block diagram



RVT511 convoy: video circuits

Fig. 4



RVT511 convoy: mode switching circuits

Fig. 5

Fig. 5

SECTION 2

STATIC APPLICATION

Chapter 1

RACK (IFF CONTROL) 4467

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LIST OF ILLUSTRATIONS

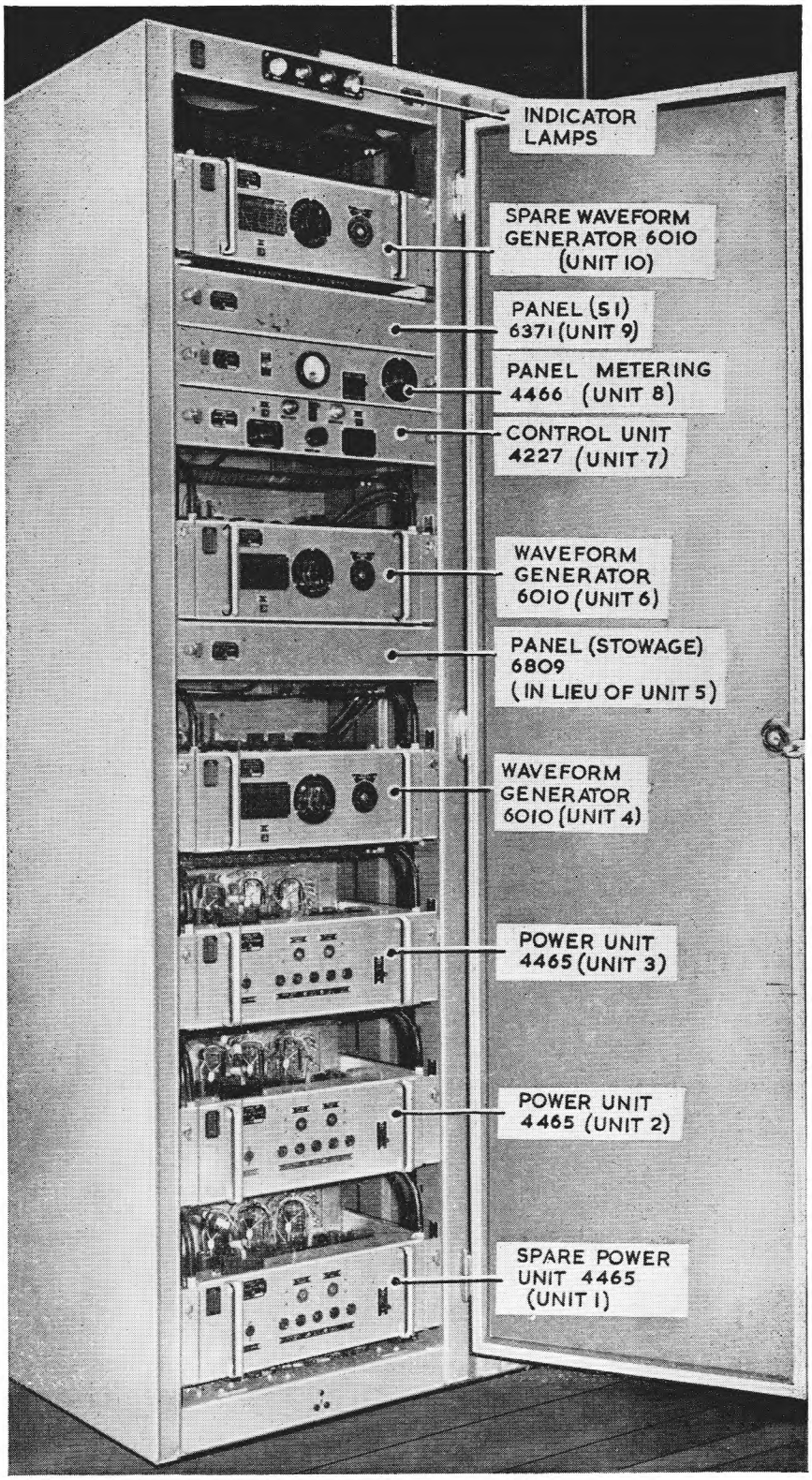


Fig. 1. Rack (IFF control) 4467: front view

General

1. Rack (IFF control) 4467 forms part of the radar office equipment and houses those units of the IFF Mk. 10 installation associated with the production of the mode trigger pulses, i.e. waveform generators 6010 and their power supplies. Control and metering panels are also included. The inter-unit cabling forms part of the rack assembly.

2. Each rack is designed to contain a maximum of ten units and can serve two interrogators. Starting at the top of the rack the units are numbered as follows:

Unit No.

10 Waveform generator 6010 (spare, not connected)
9 Panel (standby interconnection) 6371
or
Panel (stowage) 6809
8 Panel (metering) 4466
7 Control unit 4227 (for unit 6)
or
Panel (stowage) 6809
6 Waveform generator 6010
or
Panel (stowage) 6810
5 Control unit 4227 (for unit 4)
or
Panel (stowage) 6809
4 Waveform generator 6010
or
Panel (stowage) 6810
3 Power unit 4465 (supplies unit 6)
2 Power unit 4465 (supplies unit 4)
1 Power unit 4465 (spare)

3. The actual number of units fitted depends upon the station layout and the number of interrogators employed. For example, where only one head and one interrogator are in use, units 2, 4, 5 and 9 or 3, 6, 7 and 9 are unnecessary and may be omitted from the installation. It is preferable to omit the upper units 3, 6 and 7 for convenience in servicing. In multi-channel installations one completely fitted rack is required for every two interrogators.

Description

4. Rack (IFF control) 4467, illustrated in fig. 1, is a steel cabinet 7 ft. high, 23½ in. wide overall and 21 in. deep with doors at the front and rear. The three power units and the spare waveform generator are supported on angle-section runners while the smaller panels are secured, by captive screws, directly to mounting plates on the sides of the cabinet. The two operational waveform generators are so mounted that they slide in and out on extending arms, the principle adopted being similar to that used in filing cabinets. Each unit may thus be withdrawn for servicing without removing it completely from the rack, and can be tilted when withdrawn for increased accessibility. The larger units are retained in position by Oddie type fasteners.

5. Four indicator lamps are mounted at the top of the cabinet in such a position that they are clearly visible when the doors are closed. Three of the lamps are supplied from the power units and indicate that these are functioning correctly. The fourth lamp is connected across the 50V DC input to show that the supply is present at the rack.

6. Load resistors for the spare power unit 4465 are also housed in the top section of the cabinet. Since this unit normally operates in the standby condition and must be ready at all times to supply either waveform generator in the event of failure of one of the other two power units, the HT output must always be correctly stabilized and adjusted due to the automatic switching system employed. For this reason the positive supply is connected via relay contacts to a dummy load. The relay is mounted in the top of the cabinet and forms part of the automatic change-over circuit (*para.* 22).

Rack units

General

7. Waveform generator 6010 and power unit 4465 are described in Chapters 2 and 3 of this section. The remaining units housed in rack (IFF control) 4467 are described in the following paragraphs.

Control unit 4227

8. This unit is illustrated in fig. 2 and the circuit is included in the main wiring diagram of the rack (*fig.* 5). The panel carries the following controls

GAIN potentiometer
INTERROGATOR SELECTION switch
GTC LONG/SHORT switch

One control unit is provided for each waveform generator and its main purpose is to afford remote control facilities for the associated interrogator. The video and mode trigger lines from and to the interrogator are routed through the unit, monitoring sockets being provided at X1 and X2 for setting up and checking purposes.

9. Potentiometer RV1 may be used to control the gain of the interrogator receiver while the switch SW2 mounted above it controls the GTC (swept gain) characteristic. The two lamps LP1 and LP2 derive their supplies from the interrogator and give a remote repetition of similar indications in the interrogator. LP1 (POWER ON) shows that the thermal relays in the interrogator have operated and that HT is being supplied to the transmitter. LP2 (CHALLENGE) indicates that RF power in excess of a predetermined level is being radiated.

10. The remaining control on the unit (SW3) enables the video output from another interrogator to be selected when required. Such a condition might arise where the interrogator associated with a particular waveform generator becomes unserviceable and interruption of the IFF facilities is undesirable. Provided the links on panel (standby interconnection) 6371 are appropriately adjusted, another video channel can be selected immediately by setting SW3 to SPARE. This video may be

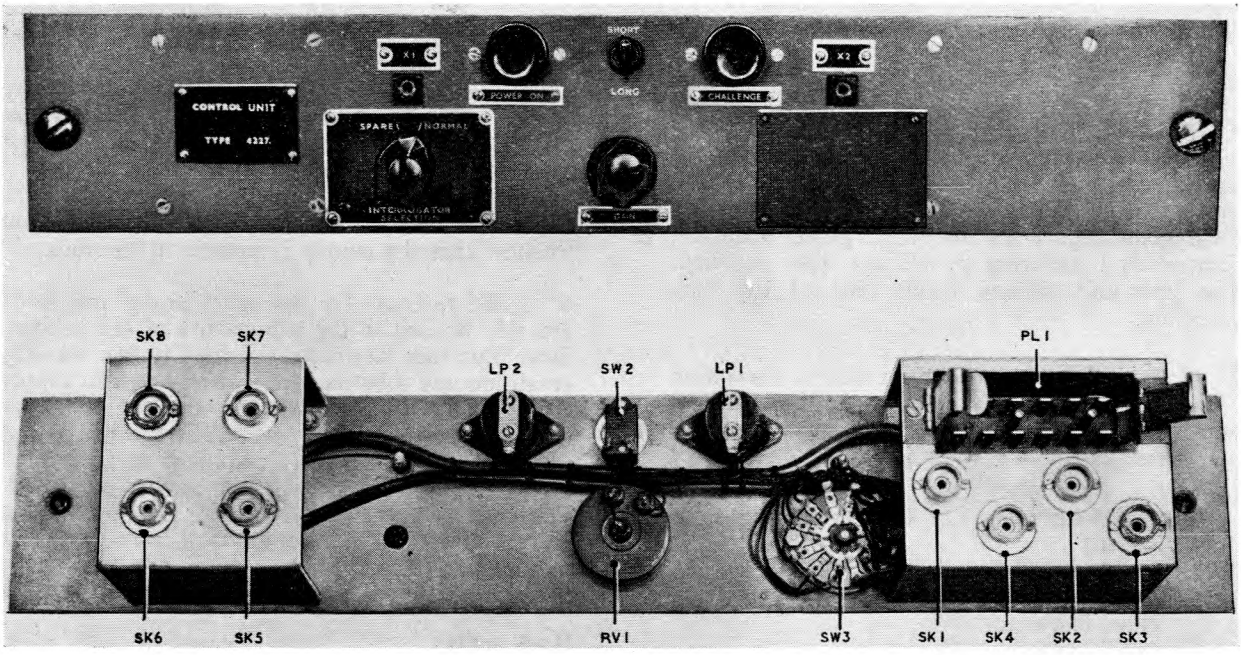


Fig. 2. Control unit 4227: front and rear views

derived from any other head on the same site, synchronized in trigger and rotation with the unserviceable one, and associated with a waveform generator in the same rack or in another rack 4467. The mode trigger circuit is not switched since continuity of this line enables servicing to proceed under operational conditions.

Panel (*standby interconnection*) 6371

11. This unit consists of a blank panel carrying at the rear sub-panels on which are mounted six coaxial sockets and eight single-pole sockets. The single-pole sockets may be connected together in any desired manner by means of short links terminated with plugs. The panel is illustrated in fig. 3 and a circuit diagram is included in fig. 5.

12. The function of the standby interconnection panel is to provide video connections between any interrogator and any waveform generator in either of two racks. For normal operation, i.e. when units 4 and 6 are operated in conjunction with their associated interrogators, the links are stowed as shown in fig. 5. By referring to this diagram the link positions for any combination of units can be determined.

13. At the rear of the panel, however, is a white tablet on which the various link combinations are partially engraved, space being left for the insertion (with a chinagraph pencil) of the additional information required at the particular site. Then, if the link settings are changed at any time the original connections can be rapidly re-established. Details of the tablet, annotated for a hypothetical case, are clearly shown in fig. 3.

Panels (*stowage*) 6809 *and* 6810

14. When a complete set of equipment for two channels is not required, the units omitted from the rack are replaced by either or both of these two blanking panels. Panel (stowage) 6809 is a direct replacement for control unit 4227 or panel (standby interconnection) 6371, while panel (stowage) 6810 is intended to replace a waveform generator. The main function of the stowage panels is to provide stowage for the unconnected cables and for this purpose spring clips are mounted at the rear, each panel affording stowage accommodation for all the connectors to the unit which it replaces.

15. At a site with only one interrogator the standby interconnection panel is replaced by a panel (stowage) 6809 and in place of one waveform generator and its control unit a panel (stowage) 6810 is fitted. Where, however, a remote radar Type 7 is used in conjunction with such a station, the second waveform generator 6010 is required for use with the remote Type 7 installation although the control unit 4227 is unnecessary. In this case the control unit is replaced by a panel

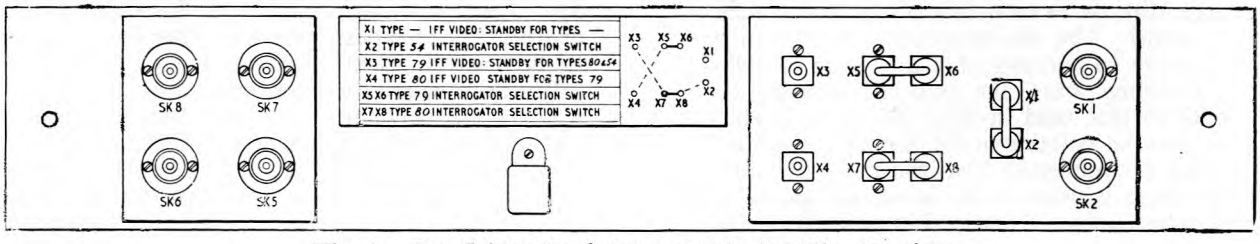


Fig. 3. Panel (standby interconnection) 6371: rear view

(stowage) 6809. In addition to the stowage clips, a double-ended coaxial socket is provided at the rear of panel (stowage) 6809. When used under the conditions mentioned, connectors 5PL1 and 5PL5 (for unit 5) or 7PL1 and 7PL5 (for unit 7) are coupled to the socket to complete the video input circuit to the waveform generator.

16. No stowage panels are used to replace any of the power units since stowage sockets for the power unit connectors are provided at the side of the rack.

Panel (metering) 4466

17. The metering panel, which is illustrated in fig. 4, has two main functions:

1. Measurement of the power unit voltages and the waveform generator valve currents.
2. The automatic switching into circuit of a spare power unit in the event of failure of either of the two operational units.

A circuit diagram is included in fig. 5.

18. The main 230V 50 c/s input to the rack is fed in on pins 3 and 4 of PL2 on the metering panel and thence, via the main on/off switch SW1, to pins 11 and 12 of PL2. It should be noted that SW1 controls the mains supply to all the rack units although each power unit is provided with a separate on/off switch for use when servicing the unit or to remove the HT supply from one or both waveform generators if required. The mains supply to the heater transformers in waveform generators 6010 is controlled only by SW1 on the metering panel.

19. The meter M1, in conjunction with the series resistors R1, R2, R3 and switch SW4, provides facilities for measuring the output voltages of the power units and the valve currents in the waveform generators. R1 is permanently in circuit while R2 and R3 are switched as required to give full-scale deflections of 250 V and 500 V. With SW4 in positions 3, 4 and 5 the meter reads directly, on the 500 V range, the +300 V output from each power unit in turn. In positions 9, 10 and 11 it measures, on the 250 V range, the −75V outputs from the power units.

20. When SW4 is set to positions 6 or 8 the meter is connected directly to the moving contact of the metering switch in the appropriate waveform generator and reads current, the particular current measured being selected by the waveform generator switch. Details of the meter readings which should be obtained are given in Part 2.

21. The remaining components on the panel, relays RL1, RL2 and switches SW2, SW3 are associated with the automatic switching circuit.

Automatic switching circuit

22. To ensure continuity of operation should one of the two power units in use fail, arrangements are made to switch the spare unit automatically into circuit. This is achieved by the relays in the power units themselves, RL1 and RL2 on the metering panel and RLA on the rack.

23. With normal operation relays RL1 and RL2 in the power units are energized (*Chap.* 3, *para.* 15 *and* 16) and their contacts are in the opposite positions to those shown in fig. 5. Assume that the negative supply in unit 2 fails. It should be noted that it is immaterial whether the positive or negative voltage disappears first since the circuit is arranged to ensure the minimum delay in the change-over operation.

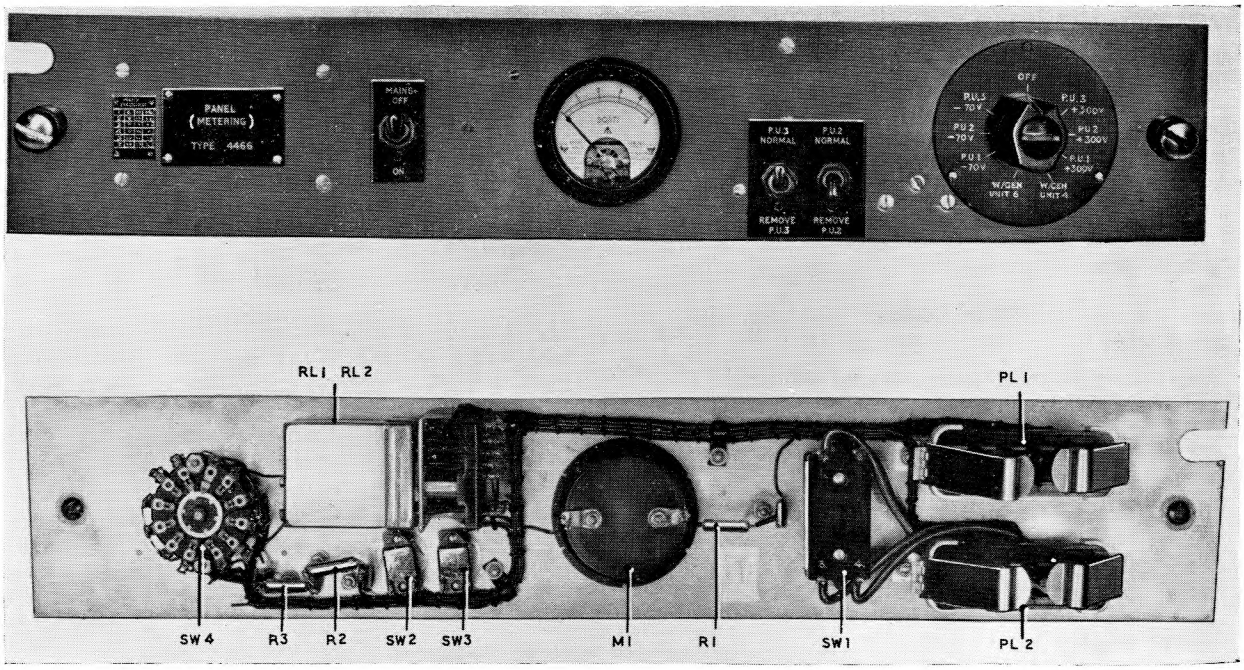


Fig. 4. Panel (metering) 4466: front and rear views

24. With the failure of the negative supply in unit 2, relay RL2 in that unit is de-energized. Contacts 25/26 break and remove the supply to the failure lamp LP2 which is extinguished thus indicating the unserviceable unit. Contacts 2/3 and 22/23 break to disconnect the +300V output from PL1/8 while 4/5 make and earth PL1/6.

25. When PL1/6 is earthed, an earth is also placed on one side of the coil of relay RL1 on panel (metering) 4466 and the relay is energized since the other side of the coil is connected to −50V through contacts 21/22 of RL2. Contacts 21/22 of RL1 break and 22/23 make connecting −50V to the coil of relay RLA on the rack. This relay is then energized and its contacts break to disconnect the dummy load from the spare power unit. The breaking of contacts 21/22 of RL1 removes the −50V supply to the coil of RL2 thus ensuring that if a fault subsequently develops in unit 3 the change-over system will not operate a second time and cause both waveform generators to be connected in parallel across the standby power unit.

26. The remaining contacts of RL1 on the metering panel select the new input supplies to the waveform generator. Contacts 2/3 switch PL1/3 to the negative input at PL2/6 in lieu of that at PL1/4 while contacts 5/6 and 25/26 in parallel switch PL1/1 to the new positive input at PL2/5 in place of PL1/2.

27. The sequence of operation is similar if a failure occurs in unit 3 with the difference that the switching is performed by relay RL2 on panel (metering) 4466 and LP3 is extinguished.

28. For correct operation of the change-over system it is essential that SW2 and SW3 on the metering panel are set to the NORMAL position when units 2 and 3 are both serviceable. If it is desired to remove a faulty power unit from the rack for servicing the appropriate switch (SW2 or SW3) must be set to REMOVE to ensure that the change-over relay on the metering panel remains energized.

Rack connections

29. Input and output connections for the complete rack are made through coaxial sockets and multi-pole plugs mounted in the base of the rack. Details of the connections are given in the following schedules.

Coaxial sockets

Termination	*Service*
SK1	Trigger pulse-pairs output from unit 6 via unit 7 to interrogator No. 1
SK2	IFF video input from interrogator No. 1
SK3	Trigger pulse-pairs output from unit 4 via unit 5 to interrogator No. 2
SK4	IFF video input from interrogator No. 2
SK5, SK6	IFF video connections to a second rack (IFF control) 4467
SK7	Sync input to unit 6 from master trigger unit in rack assembly 180-183
SK8	Mode 1
SK9	Mode 2
SK10	Mode 3
	IFF video from unit 6
SK11	Sync input to unit 4 from master trigger unit in rack assembly 180-183
SK12	Mode 1
SK13	Mode 2
SK14	Mode 3
	IFF video from unit 4
SK15	Video suppression trigger input to unit 6
SK16	Video suppression trigger input to unit 4
SK17, SK18	Interlace sync output from unit 6
SK19, SK20	Interlace sync output from unit 4
SK21	Spare

Multi-pole plugs

Termination	*Service*	
PL1/1	Gain control	Remote control facilities for interrogator No. 1
2	Challenge lamp	
3	Power on lamp	
4	GTC long/short switch	
5	Gain control	Remote control facilities for interrogator No. 2
6	Challenge lamp	
7	Power on lamp	
8	GTC long/short switch	
9, 10, 11, 12	Spare connections not used	
PL2/1	Earth	
2	−50V DC	
3	+50V DC	
4	Mode 1	command lines to unit 6
5	Mode 2	
6	Mode 3	
7	Mode 1	command line to unit 4
8	Mode 2	
9	Mode 3	
10	Spare	
11, 12	230V 50 c/s input	
PL3/1	Spare	
2	Gain control earth line from interrogator No. 1	
3	Spare	
4	Gain control earth line from interrogator No. 2	
5	−50V DC to unit 6	
6	−50V DC to unit 4	
7 to 12	Spare	

30. In addition to the plugs and sockets listed an unswitched 230V 50 c/s servicing outlet consisting of a 3-pin 5A socket (SK22) is provided on the rack.

31. The inter-synchronization leads terminated with 4PL8 and 6PL8 are normally connected to SK8 on each waveform generator as shown in fig. 5 but are left free at the bottom of the rack. A link connector, terminated with PL19 and PL20, is stowed between SK19 and SK20. When inter-synchronization is required, PL8 remains connected to SK8 on the waveform generator selected as the master but, on the slave unit the corresponding lead is transferred to SK9. SK18 and SK19 at the bottom of the rack are then coupled by the link connector provided. At the same time the mode command lines are interconnected as follows: PL2/4 to PL2/7: PL2/5 to PL2/8: PL2/6 to PL2/9.

◀**Trigger inputs**

32. To meet different operational requirements, various trigger input arrangements are necessary and these affect the disposition of the cable terminations. The three conditions required are illustrated in fig. 5 and may be summarized as follows:

(1) Two independent trigger channels to the waveform generators. Two separate inputs to the rack are required and each is terminated at the associated waveform generator. The rack terminations are unused.

(2) One MTU trigger source supplying two waveform generators. Both trigger inputs on the rack are linked and terminated. The waveform generator terminations are unused.

(3) One trigger source from frequency divider and power unit M2. Both trigger inputs on the rack are linked. The rack and waveform generator terminations are unused.

33. To avoid modifications to the equipment which would affect interchangeability, the existing terminations in the waveform generators are retained and a 68-ohm termination is added to each trigger input in rack (IFF control) 4467. All the terminating resistors are connected into circuit by soldered links so that any combination can be easily obtained.▶

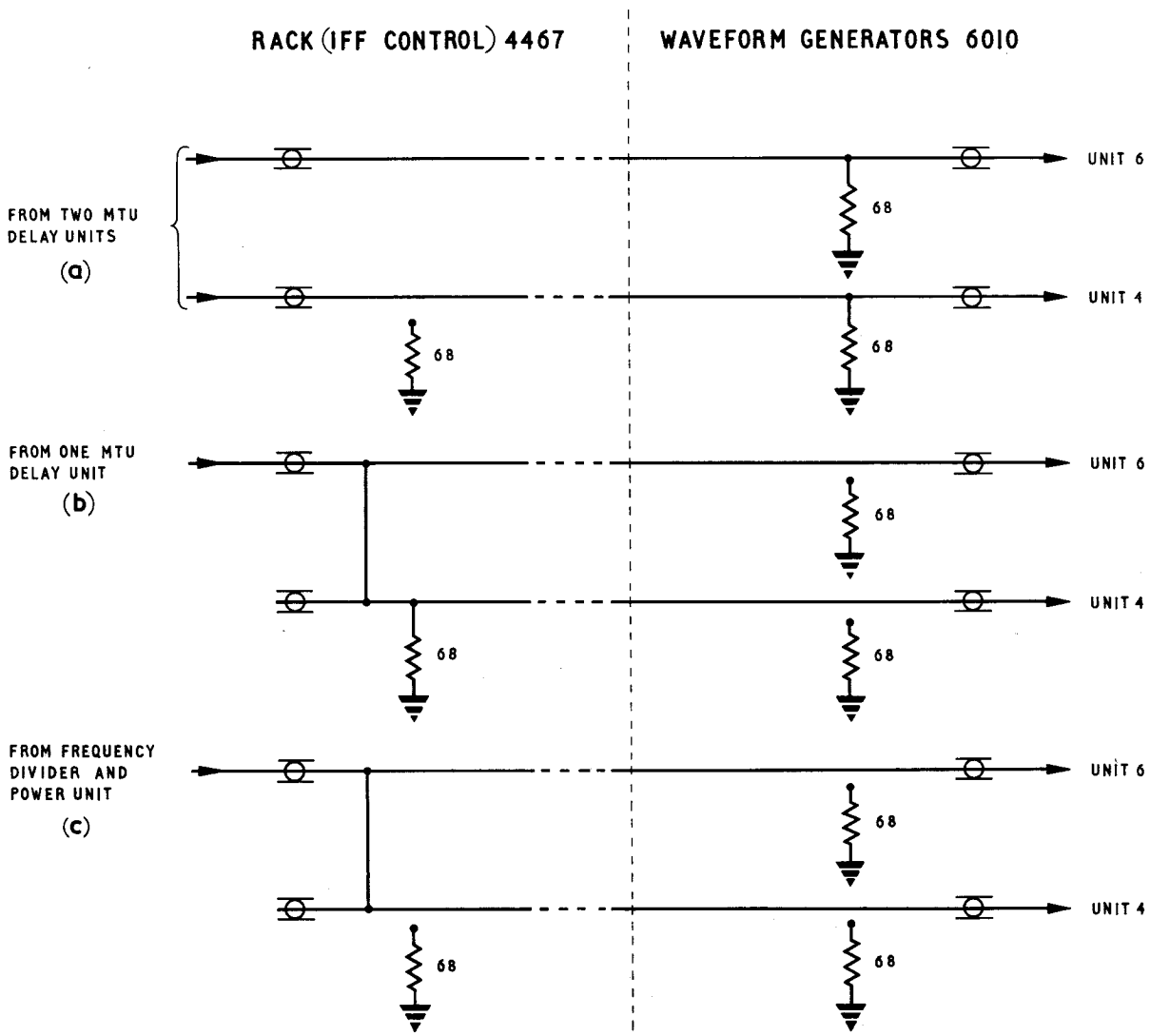
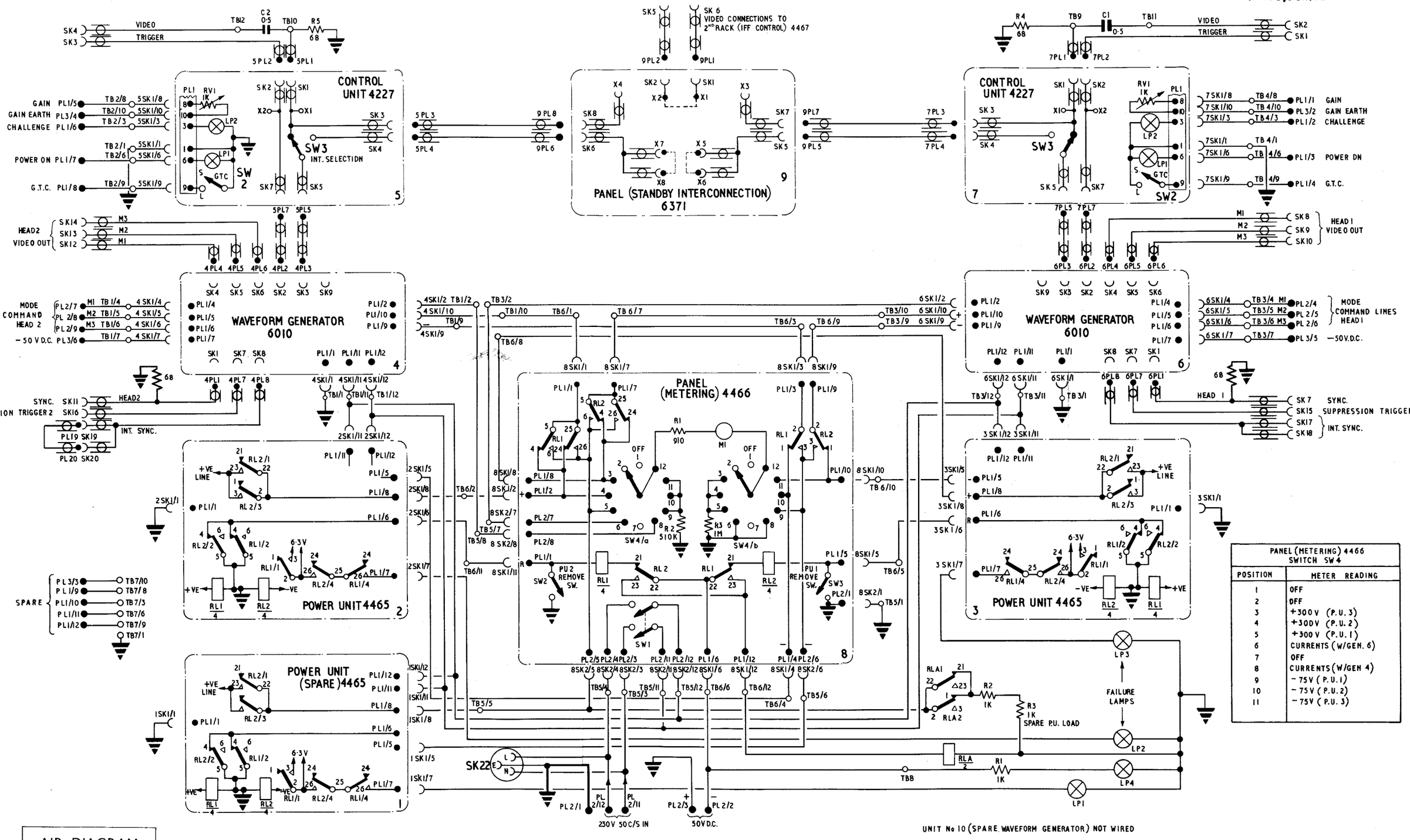


Fig. 5. Variations in trigger input terminations



PANEL (METERING) 4466 SWITCH SW4	
POSITION	METER READING
1	OFF
2	OFF
3	+300V (P.U.3)
4	+300V (P.U.2)
5	+300V (P.U.1)
6	CURRENTS (W/GEN. 6)
7	OFF
8	CURRENTS (W/GEN 4)
9	-75V (P.U.1)
10	-75V (P.U.2)
11	-75V (P.U.3)

Rack (IFF control) 4467: wiring diagram

Fig.6

AIR DIAGRAM
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Chapter 2

WAVEFORM GENERATOR 6010

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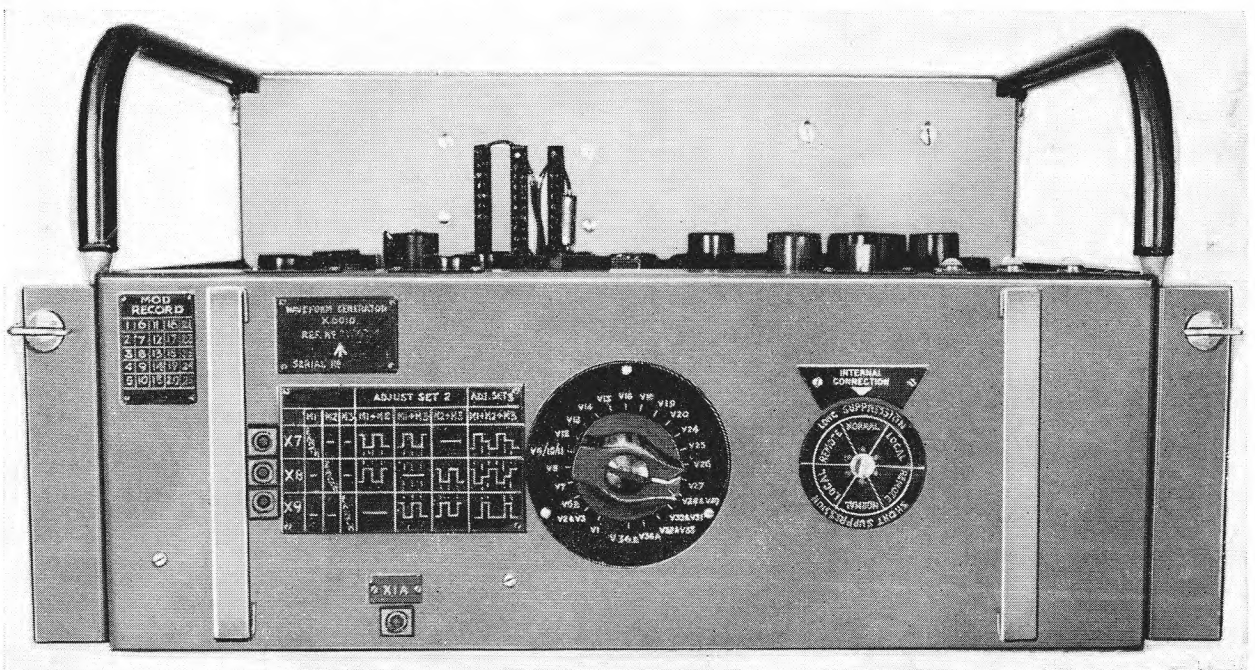

Fig. 1. Waveform generator 6010: front view

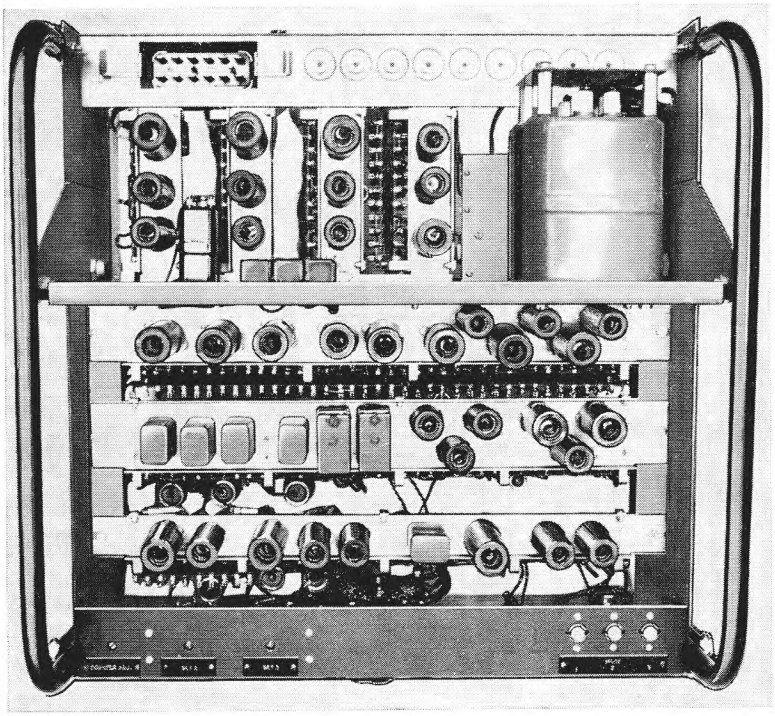

Fig. 2. Waveform generator 6010; top view

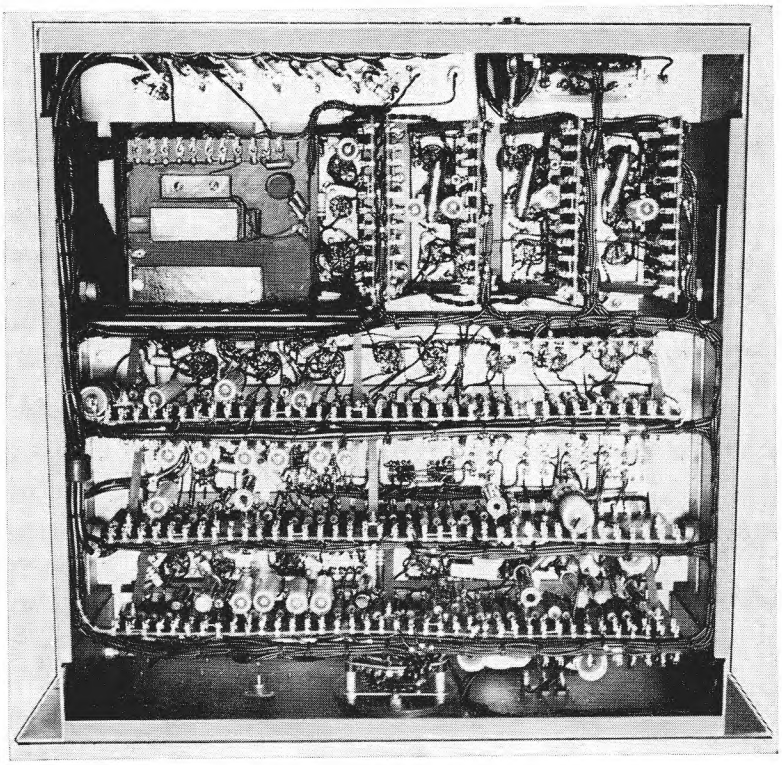

Fig. 3. Waveform generator 6010: underside view

INTRODUCTION

1. The function of waveform generator 6010 is to produce the pairs of pulses required for triggering the interrogator/responsor RT-264/UPX 6 and to accept the interrogator video output for transmission along the appropriate video channels. The unit also provides the facility known as interlacing whereby one interrogator may transmit all three modes.

2. When one mode only is required, the waveform generator produces interrogations in that mode at every cycle of the repetition frequency of the system. If two modes are called for, the unit generates the appropriate pairs of pulses at alternate cycles of the repetition frequency and correctly routes the corresponding video responses. With all three modes demanded, the waveform generator divides by three so that modes 1, 2 and 3 are interlaced at each cycle of the repetition frequency. In this way only the desired modes are transmitted and there is no waste of time or unnecessary interrogation. Provision is made in the associated equipment for the selection and display of any one mode on one console, simultaneously with the display of the same or different modes on other consoles.

3. A suppression circuit, which enables the video output to be cut off for periods of approximately 20 or 40 microseconds, is included in the video channel. This is done to reduce interference from unsynchronized local radar equipments and the circuit is operated by a trigger pulse at the repetition frequency of the interference.

4. Provision is made for the synchronization of a number of waveform generators in multi-channel installations. Visual indication of the modes selected is provided by lamps mounted on the unit.

GENERAL DESCRIPTION

5. General views of the waveform generator are given in fig. 1, 2, 3 and 4. It is housed in rack (IFF control) 4467 and consists of a box-section sheet steel framework to which are secured vertical and horizontal sub-chassis carrying the various components. Handling is facilitated by the provision of tubular steel frames at the top of each side member. For ease of access in servicing, the unit is arranged to tilt when withdrawn from the rack.

6. A block diagram showing the operation of the waveform generator in simplified form is given in fig. 5. The unit is designed to accept a positive-going synchronizing pulse of 4 microseconds in duration and 15V in amplitude. This pulse is applied to an amplifier and thence to a tapped delay line which, in conjunction with the associated valve circuits, determines the spacing between the pulses in each pair. The three trigger outputs, corresponding to modes 1, 2 and 3, are then passed through gating valves to a common mixer and, via a cathode follower, to the interrogator.

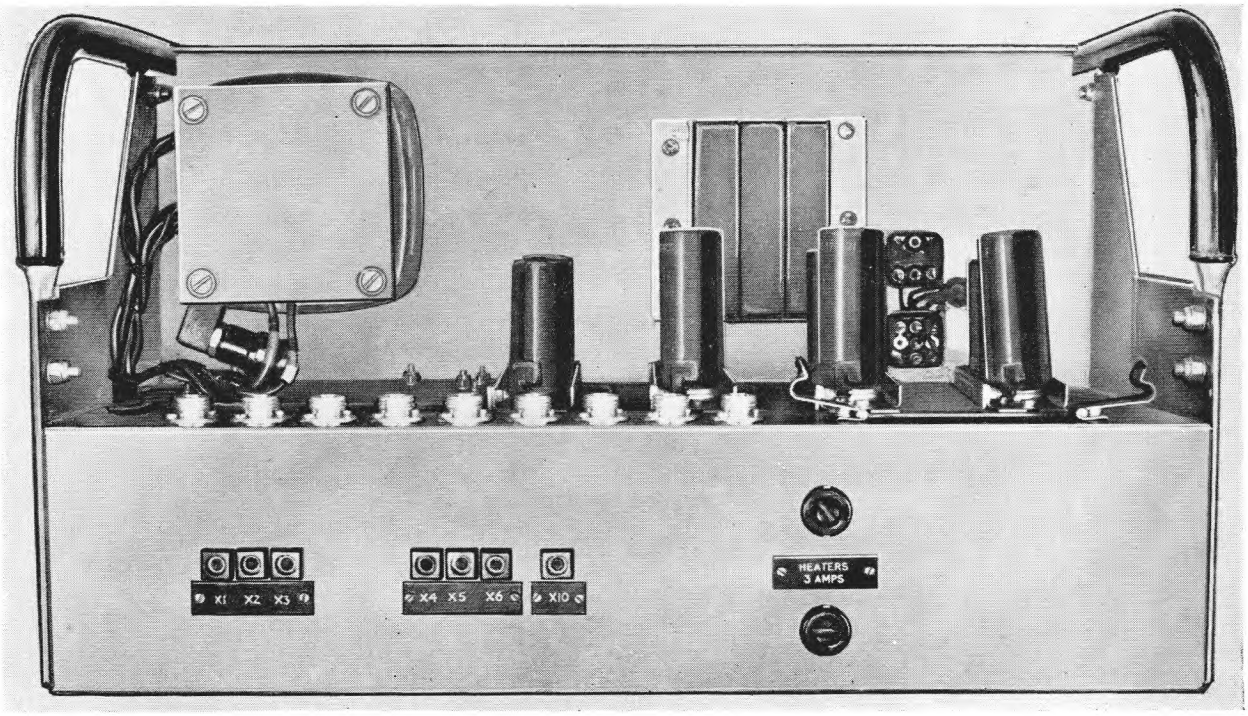

Fig. 4. Waveform generator 6010: rear view

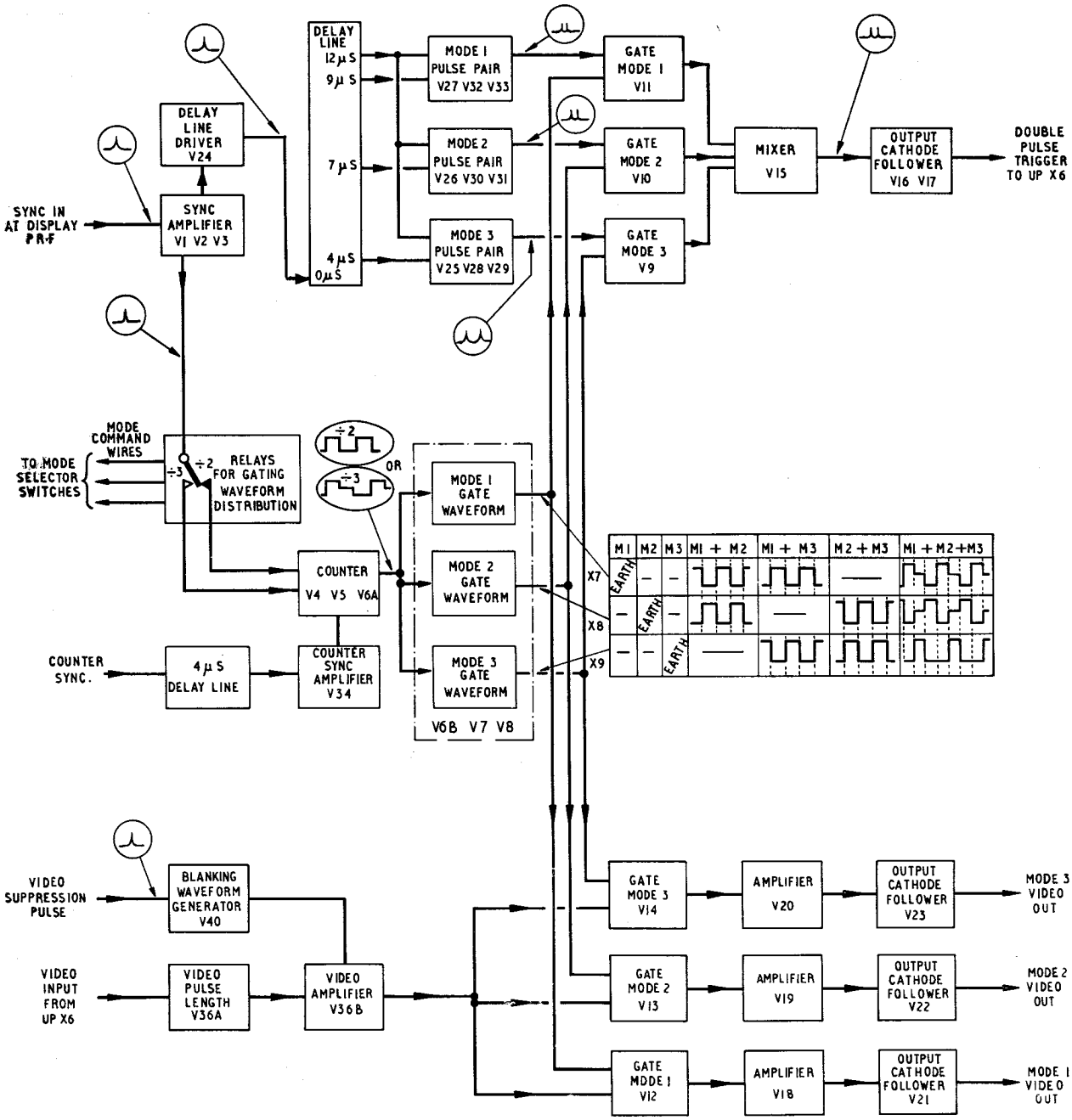

Fig. 5. Block diagram

7. Interlacing is achieved by the use of a stepping counter stage whose division ratios are controlled by relays actuated by the mode selector switches on the display consoles. The counter generates three gating waveforms which are fed to a relay switching circuit. The relays select the appropriate gating waveform for application to each trigger pulse generator gate valve and also to the corresponding video gate valve. Thus, at any given cycle of the repetition frequency, only one gate is open and only the mode trigger pulses passed by that gate are fed to the interrogator. Similarly, only video responses corresponding to the mode being transmitted will appear at the video output of the waveform generator.

8. The circuits associated with the 4 microseconds delay line and counter sync amplifier provide the interlace synchronization facility for several waveform generators 6010 in multi-channel installations.

CIRCUIT DESCRIPTION

Sync amplifier

9. A circuit diagram of the complete waveform generator is given in fig. 17. The trigger waveform is fed in at SK1 and, after differentiation by C1, R3, is applied to the grid of V1 which operates as a normal pulse amplifier. Due to the bias developed across the large value of cathode load, V1 normally passes very little current. The positive excursion of the differentiated waveform raises the potential at V1 grid and a negative-going pulse appears at the anode. This pulse is applied to V2, the grid input being again differentiated by C2, R8.

◀**Note . . .**
The input termination resistor R96 is connected to SK1 via a soldered link to facilitate disconnection in certain applications (Chap. 1).▶

10. V2 and V3 form a cathode-coupled flip-flop the purpose of which is to provide a trigger pulse of constant amplitude and duration for the counter circuit. The grid of V2 is at cathode potential while V3 grid is returned through R11 to a potential of −30V at the junction of R13 and R14 connected across the −75V supply. In the quiescent condition V3 is cut off and all the current through the stage is taken by V2.

11. With the onset of the negative excursion of the differentiated pulse from V1, V2 grid is driven beyond cut-off and the anode rises, taking with it the grid of V3. As V3 grid passes through the cut-off point, the valve conducts and a negative-going edge is produced at the anode. V2 grid recovers to cathode potential with a time-constant C2, C3, R8 so that a negative-going pulse 1 microsecond in duration is developed across R12. Since V3 passes considerable current, a positive-going pulse of approximately 25V in amplitude appears across the common cathode load R9.

12. Two outputs are taken from the flip-flop. The positive-going pulse at the cathode is used to trigger the counter circuit; the negative-going pulse from the anode of V3 is fed, via a pulse transformer TR2, to the grid of V24. Waveforms for this part of the circuit are illustrated in fig. 6.

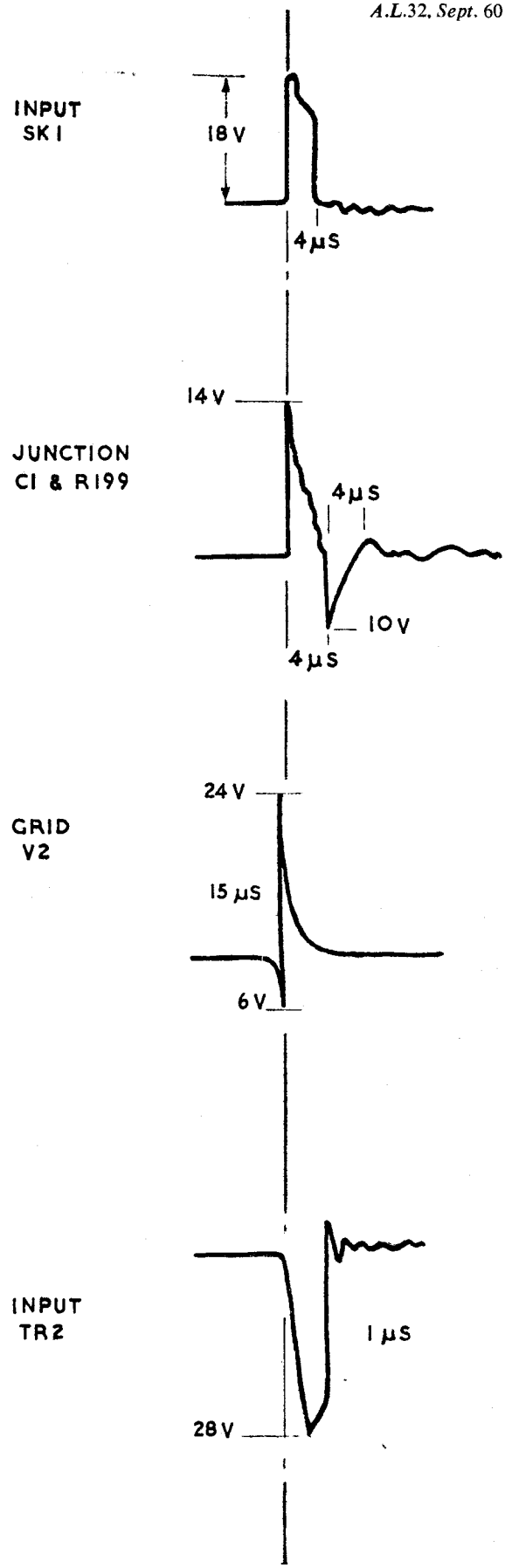

Fig. 6. Sync amplifier waveforms

Mode pulse generator

13. The pulse-pairs required to trigger the interrogator are generated by the circuits consisting of valves V24 to V33 inclusive and the delay line DL1. Each group of valves, V25, V28, V29; V26, V30, V31 and V27, V32, V33 may be regarded as an independent circuit but since all three are similar it is necessary to consider the operation in one case only.

14. The negative-going pulse from the anode of V3 is developed across the primary winding of transformer TR2. TR2 is connected as an auto-transformer with the earthy ends of the windings returned to approximately −27V at the junction of R112, R113; the high potential end of the secondary winding is connected directly to the grid of V24. V24 is therefore cut off. The pulse from V3 is reversed in polarity through the transformer so that the waveform at V24 grid is positive-going. V24 anode load consists of the primary winding of another pulse transformer TR3; the three-section delay line DL1A, B and C is connected across part of the secondary. Transformer input and output couplings are employed to provide low impedance driving sources and thus preserve the steepness of the pulse edges.

15. When the positive-going input pulse is applied to V24 grid, the valve is driven into grid current and the anode falls sharply, causing a negative-going pulse to be developed across TR3 primary. Phase reversal occurs in this transformer and a positive-going wavefront travels along the delay line. The line is terminated in its characteristic impedance by R170 so that no reflection occurs.

16. The end of the delay line is coupled through C37 to one grid of the double-triode mixer stage V25 and the 9 microseconds tapping on the line is connected to the other grid of V25 via C34. Both grids are returned to −25V and in the absence of any input waveform the two sections of the valve are cut off. 9 microseconds after the initial trigger pulse is applied to V24 grid, a positive-going pulse appears at one grid of V25 and switches on that section of the valve. 3 microseconds later a similar pulse is fed to the other grid and causes that section to conduct. The waveform developed across the common anode load of V25 thus consists of two negative-going 1 microsecond pulses with 3 microseconds spacing between the leading edges (*fig.* 7).

17. V28 and V29 form a cathode-coupled flip-flop in which V28 is conducting since its grid is at cathode potential; V29 grid is returned to −10V at the junction of R109, R110 and the valve is cut off. The circuit is triggered twice by the negative excursions of the pulse-pairs from V25, differentiated through C19, and the stage operates in a similar manner to that described in para. 11 for V2 and V3. The resultant waveform across the common cathode load R81 is a pair of positive-going pulses, 3 microseconds apart. V28 grid recovers to cathode potential with a time-constant C19, R80 and the duration of each pulse is still approximately 1 microsecond. The output from the cathode is then passed to the gate valve V9.

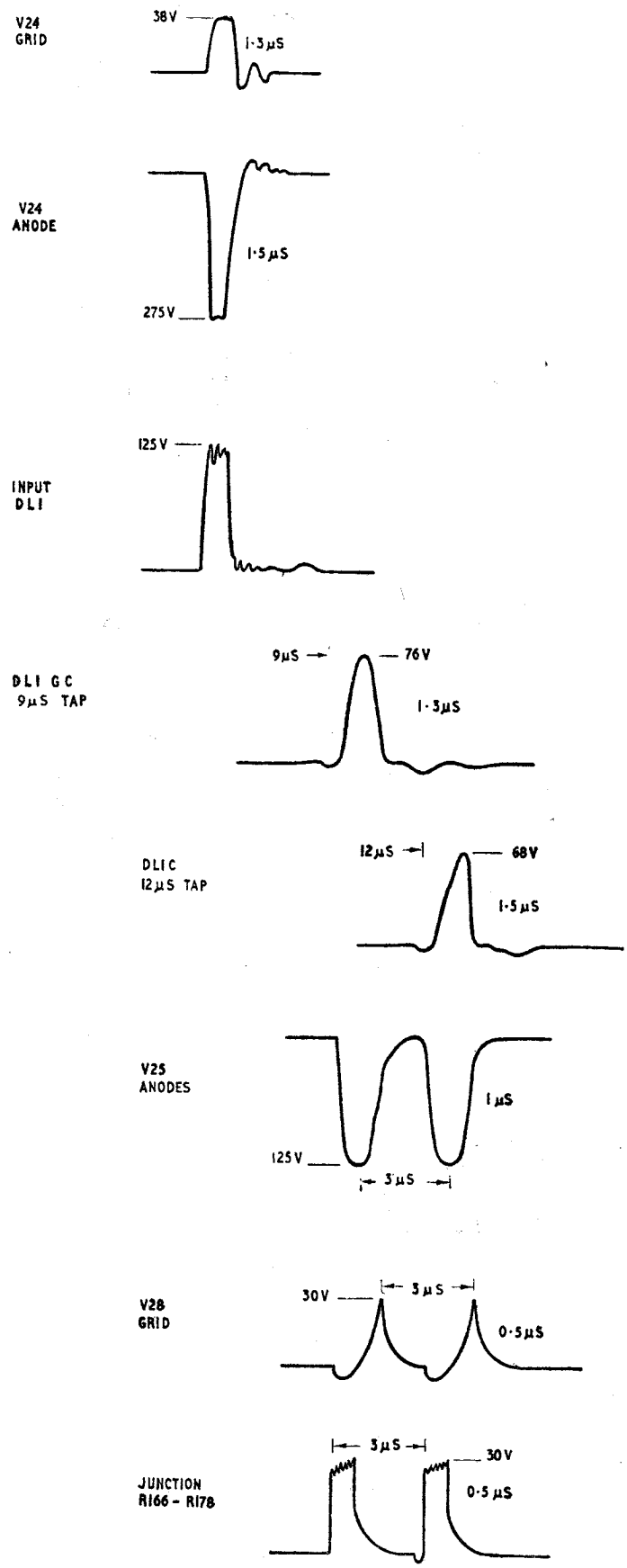

Fig. 7. Mode pulse generator waveforms

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18. The other two circuits formed by V26, V30, V31 and V27, V32, V33 operate in precisely the same manner, the only difference being in the pulse spacings. V26 is fed from the 7 microseconds point and the end of the line while V27 derives its inputs from the 4 microseconds tapping and the end of the line. These pulse-pairs are consequently spaced by 5 and 8 microseconds respectively but the second pulse in every pair is fixed in time since it is always delayed 12 microseconds behind the initial trigger pulse. A timing diagram of the pulse-pairs is given in fig. 8.

Gate circuits

19. The mode pulse gating valves are V9, V10 and V11. All three grids are returned to approximately −15V at the junction of R63, R64 and the anodes are connected in parallel. The suppressors are taken through R118, R119 and R120 to −34V at the junction of R117, R118 and are also connected to normally open contacts on relays A, B and C. All three valves are cut off and remain inoperative, even with grid input waveforms applied, if all the mode switches are open.

20. When one of the three modes is selected, operation of the mode switch on a display console energizes one of the relays A, B or C, closing the normally open contacts connected in series between the suppressor of the appropriate gate valve and earth. Under these conditions the gate is open and the pulse-pairs applied to the control grid switch on the valve so that negative-going pulse-pairs appear in the common anode circuit. The pulses are then fed to the grid of V15 via C15.

Output stages

21. V15 functions as a pulse amplifier. The negative-going pulse-pairs fed to the grid drive the valve towards cut-off and positive-going pulse-pairs are developed at the anode. This waveform is then applied to the output cathode followers.

22. In order to develop an output pulse of large amplitude across an 82-ohm load with positive grid drive, two cathode followers are used. V16 is almost cut off due to the large value of cathode load and forms a low impedence generator for V17.

23. V17 is biased beyond cut-off through the bias applied to the grid by returning R41 to approximately −30V at the junction of R68, R69. Considerable grid drive for V17 is provided by the cathode current of V16, enabling V17 to turn on sufficient current to produce a 35V positive-going pulse across an 82-ohm load. The output at SK2 thus consists of pairs of pulses correctly spaced according to the mode selected. These pulses have a duration of 1 microsecond and a very rapid rise of the leading edge (*fig.* 9).

Counter

24. The foregoing description deals with the sequence of events when only one mode is transmitted at any time. It is now necessary to consider the operation of the circuit when two or three modes are selected. Interlacing of the pulse-pairs is achieved by the use of a stepping counter which divides by two or three depending upon the condition of the mode control relays.

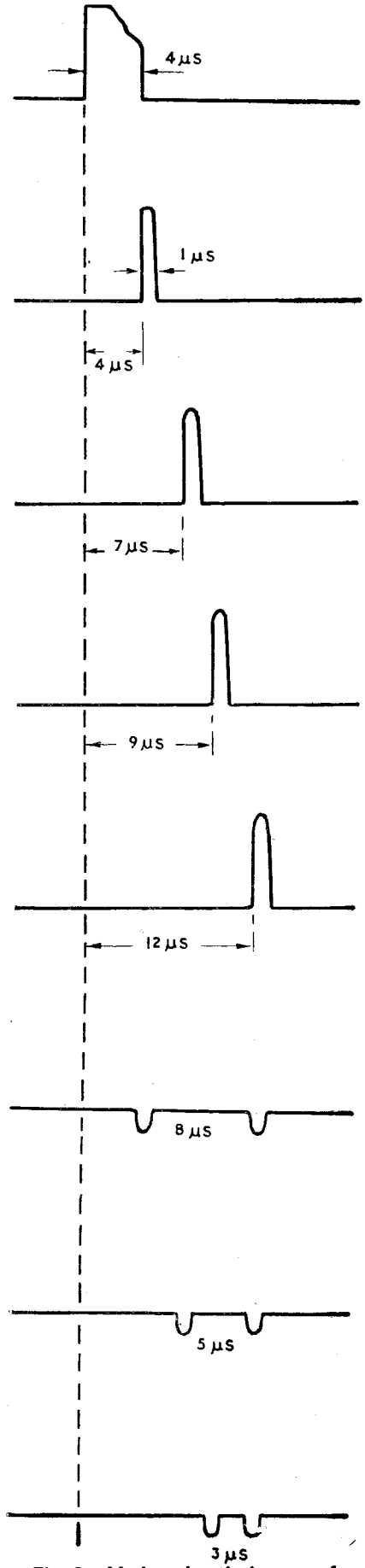

Fig. 8. Mode pulse timing waveforms

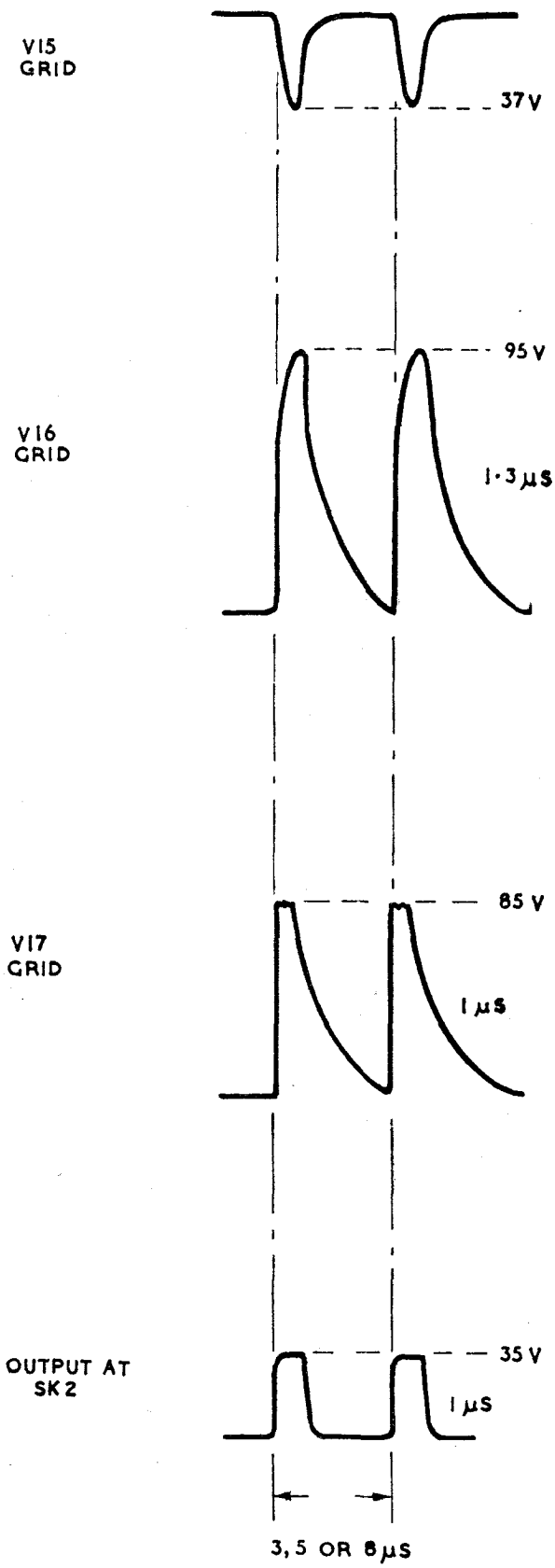

Fig. 9. Output waveforms

25. The circuit consists of the valves V4, V5 and V6A. The positive-going pulse from the cathode of the flip-flop, with its peak limited to earth potential by the action of the crystal diode V44, is applied via the changeover contacts of relay D to one of the preset resistors RV1 or RV2 and then through RV3 to the anode of the diode V4B. The baseline of the waveform at this point is clamped at approximately −20V by the action of the diode V4A.

26. V4B cathode is coupled to the grid of V5 which is a Miller integrator valve with feedback from anode to grid provided through C8 via the cathode follower V6A. In the quiescent condition, the anode of V5 is at almost HT potential and most of the current through the valve is taken by the screen. The positive-going pulse applied to V5 grid charges the input capacitance of the valve by a finite amount so that a step is produced in the grid waveform and a corresponding step in anode current. Between pulses V4B is cut off and the grid voltage remains constant with the result that the anode voltage falls in steps.

27. Since there is no grid resistor, the charge on V5 grid cannot leak away and, after two or three steps, a point is reached where V5 anode potential has fallen sufficiently to cause an increase in the proportion of cathode current flowing to the screen so that the next pulse produces a negative-going screen waveform of such an amplitude that the suppressor is partially cut off due to the coupling through C9. A regenerative action similar to that of the transitron follows, aided by the rising anode voltage which, through V6A and C8, drives V5 grid into grid current. The falling suppressor voltage completely cuts off anode current and all the cathode current is diverted to the screen. The speed of flyback of the anode voltage towards HT depends upon the time-constant of the charging circuit of C8 and this is reduced to a minimum by feeding C8 from a low impedance source, i.e. the cathode follower V6A. C9 now discharges on a time-constant of C9 and the resistive network R21, R22, R23 until anode current re-commences to flow. The resultant fall in anode voltage is transmitted through V6A and C8 to V5 grid and is arrested when the grid has fallen to a sufficiently negative potential. The circuit is now in the initial condition ready to re-commence the counting cycle on the receipt of further pulses.

28. The amplitude of the pulse applied to the grid of V5 governs the size of the step and hence the rate of counting. This amplitude is determined by the settings of RV3 and RV1 or RV2. RV1 and RV2 are selected by the contacts of relay D the operation of which is controlled by the mode control lines from the display consoles. If two modes are chosen, the counter divides by two and if the third mode is selected by another display relay D is energized and the counter divides by three. Fig. 10 illustrates the waveforms of V5 as observed on both fast and slow speed timebases.

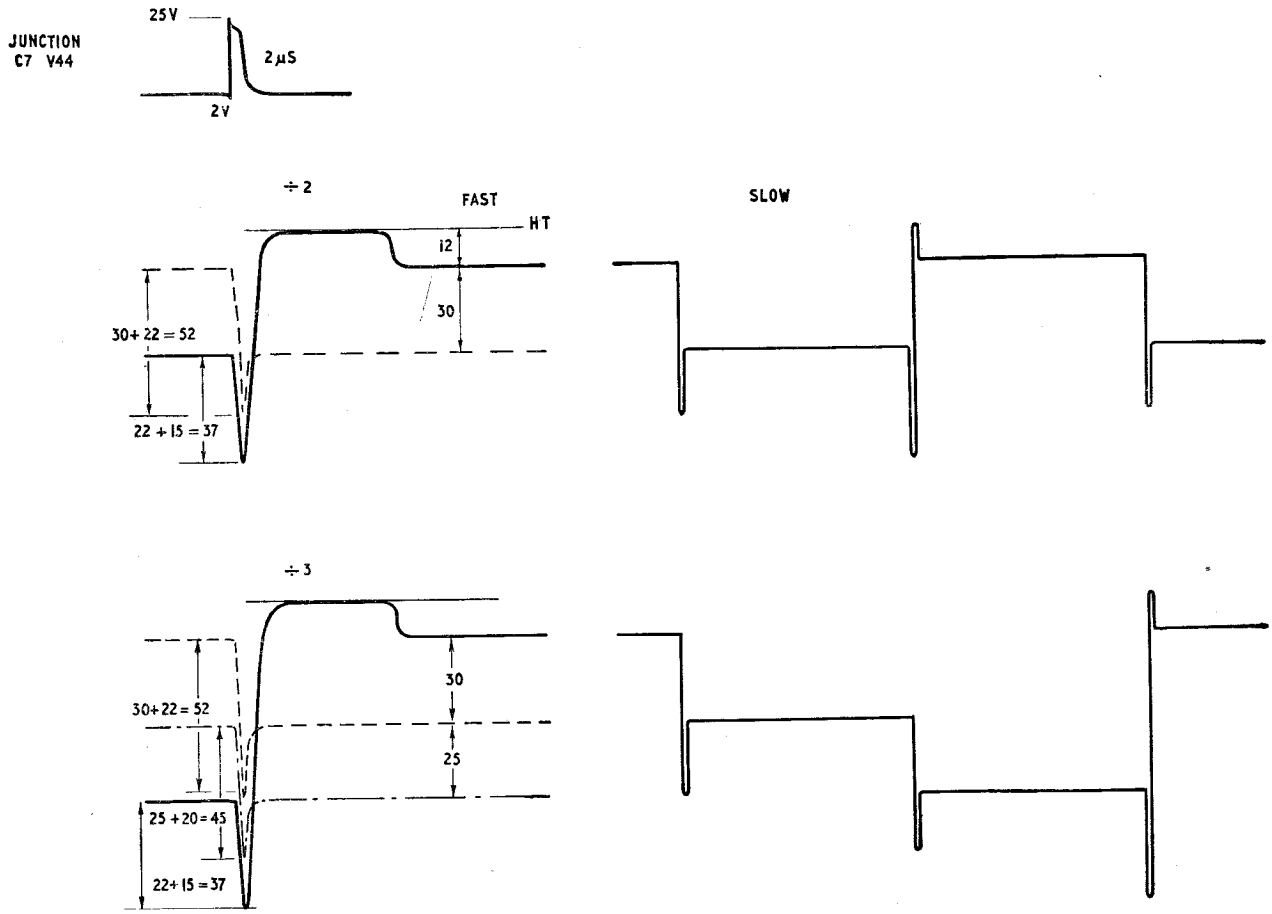

Fig. 10. V5 waveforms on fast and slow speed timebases

29. It should be noted that if no trigger pulses are applied to V5 grid the anode voltage falls gradually until it reaches a point at which the regenerative action occurs, causing the flyback sweep. In this condition the stage is free-running at a very low repetition frequency.

Counter gate

30. Two outputs are taken from the counter valve via the cathode follower V6A. One is fed to the grid of V7 which is a paraphase amplifier producing at its anode an inverted version of the input step waveform. The other output is applied through R26 and C11 to one grid of V8.

31. V8 is a double-triode mixer stage which develops a gating pulse to operate the gating valve V11 when all three modes are selected. Both grids are returned to a positive potential at the junction of R43, R44 but are DC restored to earth by the action of the internal suppressor diodes of V9 and V12, V10 and V13 or V11 and V14 (depending upon which pair of valves is connected through the relay contacts). The anodes are connected in parallel and coupled through C13 to the grid of a cathode follower V6B.

32. To one grid is applied the step waveform from V6A while the input to the other grid is the inverted step waveform from V7. Thus, on the divide-by-two function of the counter, one grid is at earth potential and the other negative, resulting in high anode current and continually low anode voltage. However, when the counter divides by three, both grids are at the same potential and are below cut-off so that the common anode voltage rises until it is limited by the effect of grid current flowing in V6B grid circuit. A positive-going gating pulse is consequently developed during the middle step of the counter waveform.

33. Waveforms of the counter circuit are given in fig. 11. It will be noted that no gating waveform is produced by V8 and V6B for the divide-by-two operation.

34. Three gating waveforms are thus produced by the counter circuit; these are the step waveform at the cathode of V6A, the inverted step waveform at the anode of V7 and the square pulse appearing at the cathode of V6B. All three are applied to a relay switching circuit formed by relays E, F and G. The operation of these relays is, in turn, controlled by the mode switching relays A, B and C together with relay D.

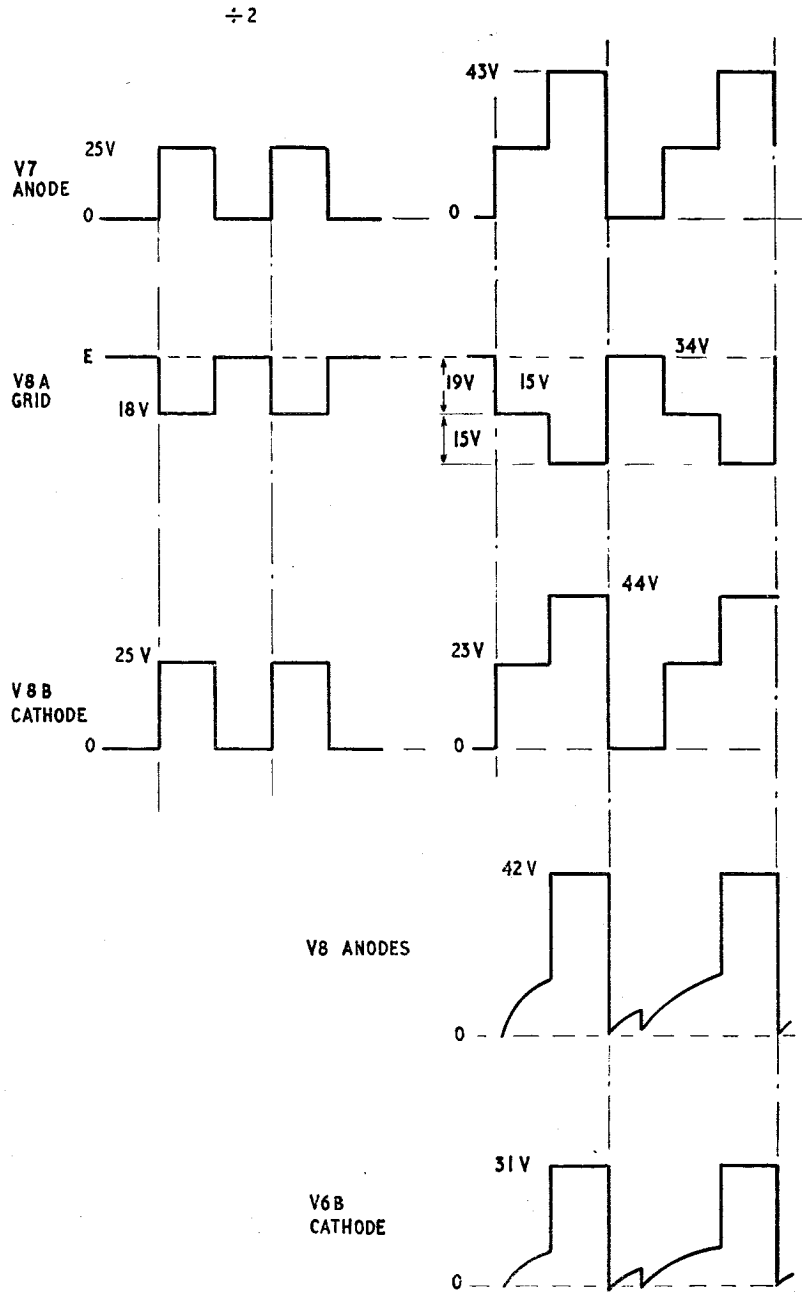

Fig. 11. Counter circuit waveforms

35. The suppressor grid of the appropriate mode pulse gate valve V9, V10 or V11 is connected, via the relay contacts, to earth for single mode operation or to the appropriate point in the circuit for injection of the counter gate pulse in multiple mode operation. Although the counter operates continuously, the gating pulses developed are ineffective until more than one mode is selected since they are isolated from the gate valves by the normally open relay contacts. The operation of the circuit may be more clearly understood by studying the following example.

36. Assume that modes 1 and 2 are selected. Relays A and B are energized, causing contacts A1, B1 and B3 to make so connecting the coil of relay E to earth with the result that this relay is also energized. Contacts A2 and B4 make and connect the suppressor grids of V9 and V10 to the change-over contacts E2 and E1. Since relay E is energized, the suppressor of V9 is coupled to the cathode of V6A through C11 and R26 while that of V10 is connected to the anode of V7 via C12.

37. On one cycle of the repetition frequency, the negative-going step waveform from V6A holds the suppressor of V9 beyond cut-off but the positive-going step from V7 switches on V10. In consesequence, V10 passes mode 2 trigger pulses to the output. On the next cycle, the step waveforms have changed polarity and the conditions are reversed, V9 now passing mode 1 trigger pulses and V10 being cut off. Thus, modes 1 and 2 are transmitted at alternate cycles of the repetition frequency.

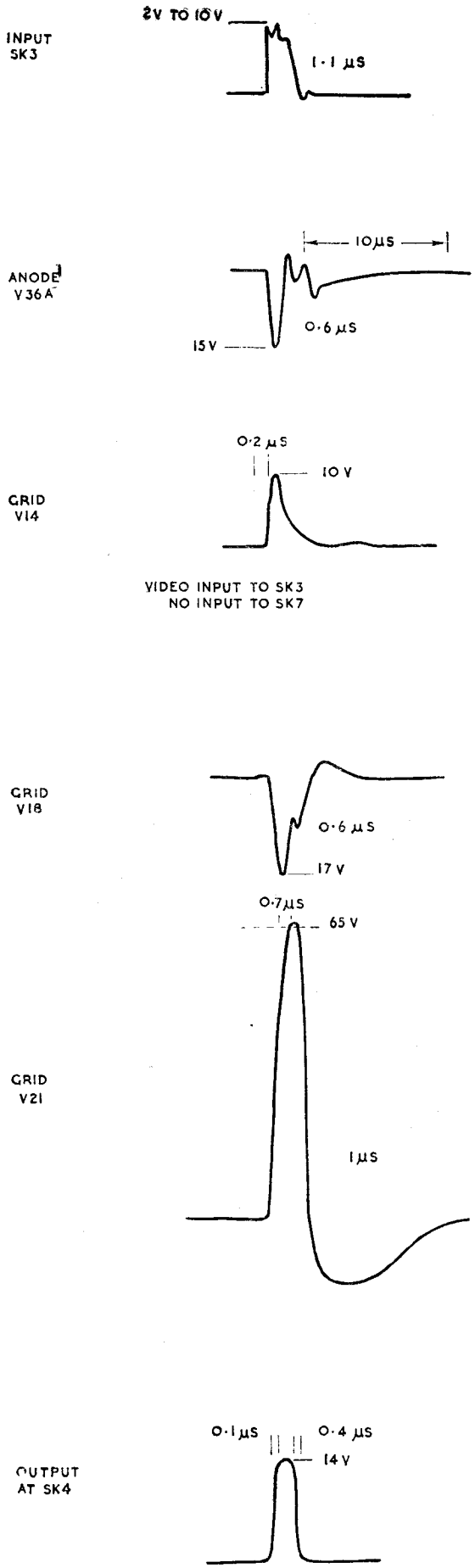

Fig. 12. Video circuit waveforms

38. Similar conditions apply if modes 1 and 3 or 2 and 3 are selected with the difference that relays F and G are energized in mode 3 operation. Depending upon the modes selected and the positions of the relay contacts, the positive and negative-going step waveforms are applied to the suppressors of the appropriate gate valves.

39. Assume now that all three modes are required. Relays A, B and C are all energized with the result that D, E, F and G are also energized. The step waveforms are applied to the suppressors of V9 and V10 as described in para. 36 but V11 suppressor is now connected, via contacts C4, D2 and capacitor C14, to the cathode of V6B. Since relay D is energized, the counter divides by three. On the first cycle of the repetition frequency, the negative-going step waveform from V6A holds the suppressor of V9 below cut-off while the positive step switches on V10. During the second cycle, both suppressors are held below cut-off and the positive-going pulse from V6B switches on V11, permitting mode 3 trigger pulses to pass to the output. On the third cycle the polarity of the step waveforms is reversed so that V9 is switched on and both V10 and V11 are cut off. In this way each mode is transmitted at one-third of the repetition frequency.

40. The indicator lamps which show the modes selected are connected in parallel with the supply to relays A, B and C and are automatically illuminated when the appropriate relays are energized.

Video circuits

41. Video signals from the interrogator are fed in at SK3 and are then applied to a circuit formed by the double-triode valve V36, the short-circuited delay line DL3 and the crystal diodes V37 and V38. This circuit provides part of the limiting action and also determines the video pulse duration, the purpose of the delay line being to reduce the effect of pulse stretching caused by echoes from local reflecting objects. The positive-going video pulse is fed to the grid of V36A where it is DC restored to earth potential by the action of the crystal diode V41. In consequence, a negative wavefront travels along the delay line until it reaches the short-circuit termination where it is reflected with change of sign. The delayed reflected wave cancels the remaining part of the negative pulse at V36A anode; the remainder of the reflected pulse causes a positive overshoot. Further reflections are negligible since the anode load R165 is an approximate match to the characteristic impedence of the delay line.

42. As any positive excursion of the anode of V37 is prevented by the action of the clamping diode V38, V37 is cut off by the positive portion of the waveform and so passes only the negative pulses. The output at V36B anode consists of positive video pulses 1 microsecond in duration and approximately 10V in amplitude for 2V input at SK3. The overall gain of V36 is so arranged that only signals with an amplitude of 2V or more at SK3 produce sufficient output at V36B anode to switch on the

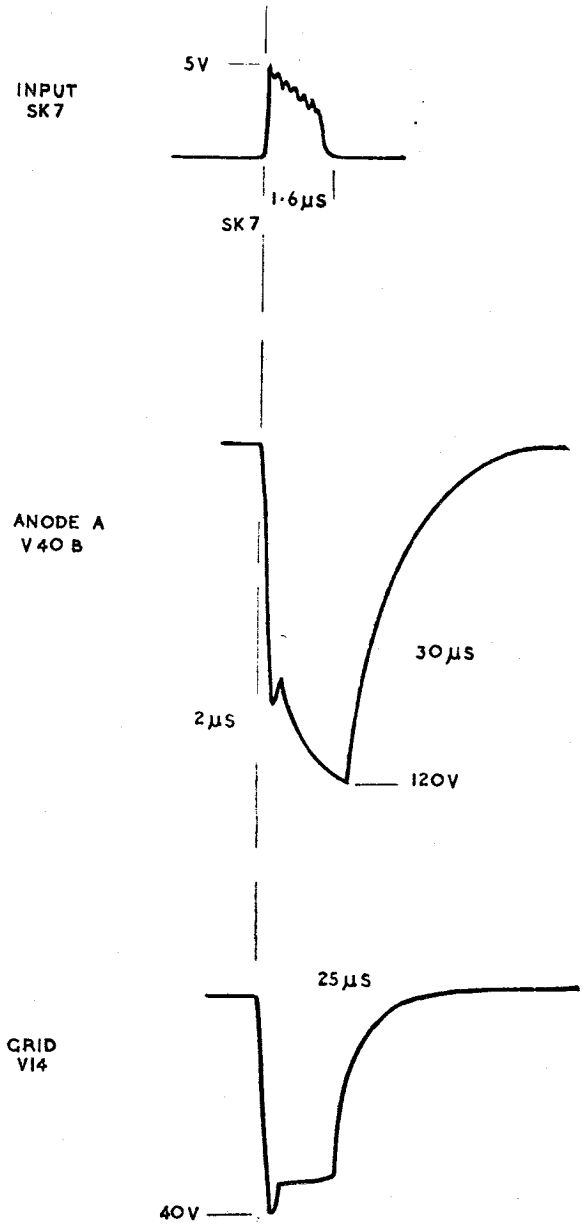

Fig. 13. Video suppression circuit waveforms

gate valves. Signals with an amplitude of 1V or less at SK3 are not amplified to a high enough level to overcome the fixed bias applied to the gate valve control grids.

43. The output at V36B anode, which may contain video signals in all three modes, is fed to three gating valves V12, V13 and V14 whose control grids are connected in parallel and returned to approximately −10V at the junction of R111, R115. Limiting on the positive video peaks is effected by the action of the crystal diode V39 which clamps the positive excursion of the gate input at earth potential.

44. The suppressor grids of the video gating valves are connected in parallel with those of the mode trigger gate valves. Thus, the appropriate video gate is opened at the same time as the corresponding mode trigger gate with the result that the video responses are routed along the correct channel.

45. Each gating valve is followed by a single stage of video-frequency amplification, V18, V19 or V20 and a cathode follower, V21, V22 or V23. The outputs at SK4, SK5 and SK6 consist of mode 1, 2 or 3 video pulses with an amplitude of approximately 14V when fed into a circuit of 68 ohms impedence (*fig.* 12). However, in large IFF installations, this voltage may fall to 3V if the same mode is selected at all the consoles.

46. The video suppression circuit consists of the double-triode valve V40 connected as a cathode-coupled flip-flop. In the quiescent state V40A is conducting and develops sufficient bias across the common cathode load R187 to cut off V40B. The circuit requires a positive-going input trigger pulse of not less than 10V in amplitude and not less than 1 microsecond in duration which must be so phased that the interference occurs during the period of the suppression pulse.

47. The suppression trigger pulse, at the p.r.f. of the interference, is fed through C66 to the cathode of the flip-flop and raises the cathode potential so that the current through V40A is reduced. V40A anode thereupon rises, taking with it the grid of V40B until that section of the valve starts to conduct. V40B anode falls and this fall, fed back through C67, reduces the grid potential of V40A. Eventually, all the current through the valve is taken by V40B and V40A is cut off. At V40B anode is developed a negative-going waveform whose duration is dependent upon the recovery time of the flip-flop, i.e., the time-constant of C67 and R185, R186. This is approximately 20 microseconds but, since conditions may exist where the period is inadequate, two resistors in parallel are provided in place of a single component. By breaking one of the connections between R185 and R186 the suppression period may be increased to 40 microseconds.

48. The output from V40B anode is applied through C69 and R192 to the grids of all three video gating valves. In the absence of a trigger pulse at SK7, the anode of V40B is at almost HT potential and video signals fed to the grids of V12, V13 and V14 are passed by the gate valves in the normal manner. When a suppression pulse is fed in at SK7 however, the gate valve grids are held at approximately −40V for the duration of the suppression waveform and the valves are then inoperative (*fig.* 13).

Interlace synchronizing circuit

49. To avoid difficulties which might arise due to mutual interaction at sites with two or more interrogators, it may be essential for all the IFF interrogators at a site to be synchronized so that all radiate the same modes simultaneously. Such conditions will exist where the heads radiate in the same direction and also where the radar heads are not rotating in phase. At ranges of the order of 40 miles or less, it is possible for back or side lobes to trigger transponders and such a lobe of one aerial may be pointing in the same direction as the main beam of another aerial.

50. To illustrate the effect of simultaneous interrogation of a transponder by two interrogators operating on different modes, consider the case where modes 2 and 3 pulse-pairs are radiated. The transponder receives the first pulse of the mode 3 pair and 3 microseconds later the first pulse of the mode 2 pair. Five microseconds afterwards the second pulses of both pairs arrive in unison. The transponder however, does not wait for the second pulses but provides a mode 1 reply as soon as it has received the two first pulses spaced by 3 microseconds. Thus a combined mode 2 and 3 interrogation will elicit a mode 1 reply. Similarly, a combined mode 1 and 3 interrogation will produce a mode 2 response from transponders with their mode 2 switches set to ON.

51. Although all the waveform generators at any one site would probably be synchronized in p.r.f. since the trigger source would be common, it does not follow that the interlaced outputs would be synchronized. Different factors, such as component tolerances and variations in the operating times of the mode switching relays, can affect the timing of the counter step waveforms. By locking all the counter circuits together, the gating waveforms must occur at the same time. In addition, when the IFF interrogators at a site are to be synchronized, the corresponding mode command input wires are connected together, thus ensuring that all the interrogators operate with the same combination of modes.

52. The interlace synchronizing circuit provided in the waveform generator is required to give the following facilities

(1) Normal use of the waveform generator, providing three separate video outputs of IFF responses from a local interrogator, but not synchronized in p.r.f. or interlacing with any other waveform generator.
(2) Normal use as in (1) but providing an interlace synchronizing waveform to one or more nearby waveform generators synchronized in p.r.f.
(3) Normal use as in (1) but receiving an interlace synchronizing waveform from a nearby waveform generator synchronized in p.r.f.
(4) Remote use, in which it supplies interlaced trigger pulses to an interrogator and interlaced video waveforms together with a synchronizing pulse to a radio or cable link.
(5) Local use, receiving interlaced video waveforms from a radio or cable link and distributing them into three separate video channels corresponding to the three interrogation modes of the associated remote waveform generator.

53. These varied requirements demand flexibility in the synchronizing system and this is achieved by the use of internal links which may be arranged to give the desired facility. An indicator plate on the front panel shows which function the waveform generator is performing. The

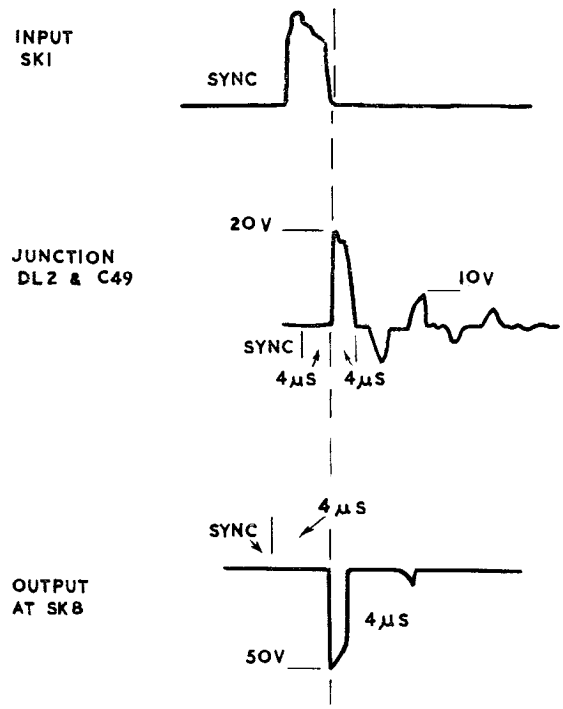

Fig. 14. Interlace synchronizing circuit waveforms

circuit diagram shows the links in the normal position and a table is provided giving details of the appropriate connections for remote and local use.

54. The interlace synchronizing pulse generator consists of the circuit formed by the delay line DL2 and the pulse amplifier V34. V34 grid is returned to a potential of approximately —15V at the junction of R156, R157 so that the valve is normally cut off. The positive-going input trigger pulse is applied to the input of the delay line. In order to compensate for the attenuation of the delay line it is not terminated with the result that the amplitude of the delayed output pulse is doubled. It is then approximately equal to the amplitude of the input pulse. The reflections caused by the mismatch existing at both ends of the line are rapidly attenuated and do not affect the operation of the circuit. The initial input to V34 grid is thus a positive-going pulse 4 microseconds in duration and delayed 4 microseconds behind the trigger pulse (*fig.*14). At V34 anode an amplified negative-going version of the grid waveform appears.

55. The suppressor of V34 is returned to the cathode of V6A. V34 is consequently gated by the counter step waveform and the synchronizing pulse at the anode does not appear at every cycle of the p.r.f. but at alternate cycles if the counter divides by two and every third cycle if the counter divides by three. From V34 anode the interlace synchronizing pulse is fed out to SK8 via C47.

56. For normal use as in para 52(1), no connection is made to SK9, and SK8 on each waveform generator serves as a stowage point

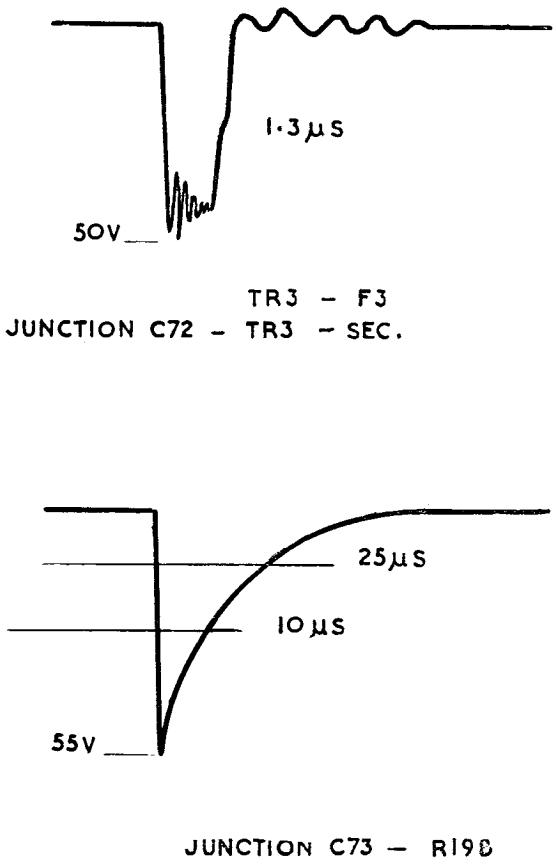

Fig. 15. Interlace suppression circuit waveforms

for the appropriate rack cable terminated with 4PL8 or 6PL8, the lower end of each cable being free. When synchronization is required, the cables are coupled together at the bottom of the rack. One waveform generator is selected as the master, the synchronizing pulse is talen from SK8 and fed in at SK9 on the other unit(s). From SK9 it is applied to the suppressors of the counter valves V5 in the slave waveform generators and initiates the regenerative recovery of the counter circuits in those units if they are not already interlacing in step. In this way the counter circuits are locked together and the step waveforms must coincide in time; as long as this state of affairs persists the synchronizing pulse plays no further part in the circuit operation.

57. When a waveform generator is to be used at a remote head, changes in the internal connections become necessary. The video link between the remote installation and the operations centre consists of a single cable carrying radar IF signals, IFF video for all three modes and the interlace synchronizing pulse. ◀This facility as in para.52(4) is available on all or any one of the modes 1, 2 and 3 video channels by changing the connections on the appropriate links (fig. 17; internal connections table). The circuit action is the same for each mode and for purposes of explanation consider mode 1 channel only to be carrying the common video output in the remote waveform generator. With the internal link connected between 8 and 9 the gating waveform is removed from V12 suppressor which is now held at earth potential by the action of the internal diode and the leak through R198 to HT. Points 5 and 6 are linked together to feed the interlace synchronizing pulse into the video channel.▶

58. With no gating waveform applied to the suppressor, V12 operates as a normal pulse amplifier and feeds negative-going video signals to the grid of V18. The interlace synchronizing pulse is injected at the same point through the crystal diode V42. In the absence of the synchronizing waveform, V42 is cut off by the negative-going pulses at V18 grid so that the video circuit is effectively isolated from the synchronizing pulse generator. With the onset of the synchronizing pulse V42 conducts and the pulse is passed to the grid of V18. At the end of the pulse the diode is again cut off and V18 grid potential recovers exponentially. In consequence of this stretching, the duration of the synchronizing pulse delivered from SK4 is of the order of 10 microseconds.

59. The circuit associated with the lower portion of the secondary winding of the pulse transformer TR3 and the crystal diode V43 provides a suppression pulse to prevent pulses caused by interrogator transmitter break-through from interfering with the interlace synchronizing waveform. Due to the common T and R system employed, a certain amount of transmitter break-through occurs in the interrogator, resulting in spurious pulses appearing on the video channel. These pulses coincide in time and spacing with the trigger pulse-pairs and, for certain mode combinations, may affect the operation of the synchronizing circuits. To overcome this, V12 is switched off for a period of approximately 20 microseconds after the repetition pulse.

60. The waveform appearing across the lower portion of TR3 secondary winding is a 1 microsecond negative-going pulse at the repetition frequency and this waveform is applied through capacitor C72 to the diode V43 and resistor R197. Due to the characteristics of the diode, pulse stretching occurs and the resultant waveform appearing at the junction of C73, R198 is a negative-going pulse with an exponential tail on the back edge (*fig.* 15). With 8 and 9 linked together, this waveform is applied to the suppressor of V12 and the valve is cut off for about 20 microseconds after the repetition pulse, thus ensuring that no video output appears during the period of the interlace synchronizing pulse.

Warning . . .

It should be noted that, when 8 and 9 are not connected together, the potential of the circuit between C72 and C73 (including tag 9) rises to +300V due to the connection through R198 to the HT line. With 8 and 9 joined, this circuit is clamped at earth potential by the action of the internal suppressor diode of V12.

61. The waveform generator located at the operations centre receives the composite information from the remote head via the single cable at SK3. In this unit 7 and 8 are connected so that V12 is gated in the normal manner. The video signals pass through the video circuits and are separated into the appropriate channels.

62. The interlace synchronizing pulse is extracted at SK3 and applied to the primary winding of a pulse transformer TR4. Some attenuation is inevitable in the cable link but it is not anticipated that the longest cable likely to be used will result in a pulse amplitude at SK3 of less than 3V. Accordingly, TR4 has a step-up ratio of 1 : 3 giving a pulse amplitude of approximately 9V across the secondary for 3V input.

63. The duration of the pulse developed across TR4 primary is some 10–12 microseconds (*para.* 58) but, due to differentiation through the transformer, the duration of the secondary waveform is of the order of 5–6 microseconds (*fig.* 16). By connecting 1 and 2 together the pulse from TR4 is applied to the suppressor of V34. During the period of this suppressor gating waveform V34 generates a 4 microseconds pulse as described in para. 54 and, since 4 and 5 are connected, the synchronizing pulse from V34 is fed to V5.

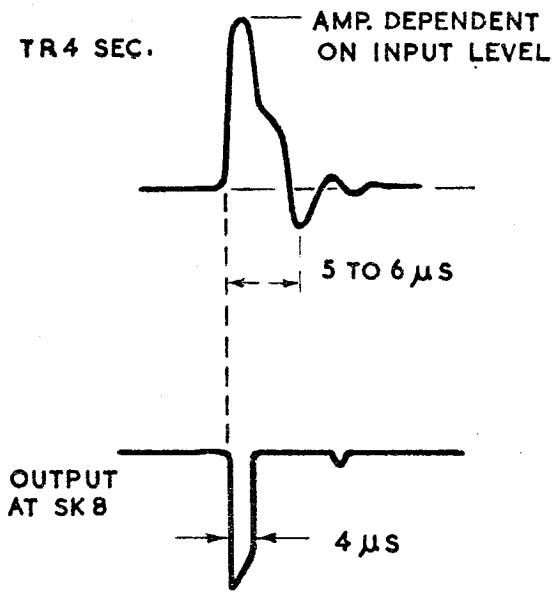

Fig. 16. Interlace sync from remote waveform generator

64. It should be noted that it is normal practice to synchronize all the radar heads on one site so that they radiate simultaneously and to trigger a remotely sited radar Type 7 sufficiently early for its responses to arrive by cable at the main site in the correct time relationship with those from the local radars. This allows a PPI display to be switched from one video source to the other without changing its timebase trigger timing. The same timing arrangements apply to the IFF trigger waveforms for waveform generators 6010 at remote and local sites. Thus, the waveform generator at the remote site, when triggered with the correct time relationship to the remote radar, supplies an interlace synchronizing pulse which arrives at the suppressor of V34 in the local waveform generator simultaneously with the 4 microseconds pulse produced at the grid by the local trigger waveform. To check this coincidence monitoring sockets are provided at X3 and X10 respectively.

Monitoring

65. To facilitate checking the waveform generator under operating conditions, other waveforms in addition to those mentioned in the preceding paragraph are brought out to monitoring points to which an oscilloscope may be connected. The counter waveforms appear at sockets on the front panel and the input trigger pulse is available at another socket for synchronization of the oscilloscope. The remaining monitoring sockets are at the rear of the unit and afford examination of the video input and output waveforms as well as the trigger pulse-pairs.

Power supplies

66. Positive and negative supplies from power unit 4465 are brought in on the 12-pole plug PL1. The negative supply is stabilized at −75V by the gas-filled stabilizer valve V35 as described in Chapter 3, para. 12. Heater supplies for the valves in the waveform generator are derived from a separate transformer TR1 housed within the unit. The transformer is protected by fuses FS1 and FS2 in the primary circuit together with the thermal cut-out FS3.

Metering

67. Provision is made for measuring the cathode currents of most of the valves in the waveform generator on panel (metering) 4466. The appropriate shunt resistor for the meter is included in each cathode circuit where necessary and the particular current being measured is shown by the switch indicator plate on the front panel of the waveform generator.

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Appendix 2

S.I.F. FACILITY

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Purpose

1. When S.I.F. is fitted, the video signal passing through the waveform generators 6010 and 6010A consists of lengthy pulse trains. Valve V40 causes undesirable back-biasing of these trains, and is removed, thus rendering all its associated components inoperative. A blanking plate (E/RAD/A68168-1) is fitted to the valve holder to make the modification permanent.

2. When waveform generators 6010 and 6010A have been modified as above, the description and information given in Chapter 2, paras. 46 to 48, and fig. 13 of that same chapter become inapplicable.

Appendix 1

WAVEFORM GENERATOR 6010A

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Purpose

1. The video output of waveform generator 6010, A.M. Ref. 10V/16274, consists of a series of pulses approximately 0·5 μs wide. At certain stations, the display equipment is designed to accept 2 μs wide pulses and the circuit of the waveform generator has, therefore, to be modified to provide output pulses of this length. After modification, the unit becomes waveform generator 6010A, A.M. Ref. 10V/16501.

2. The effect of the modification on the circuit is to change the values of resistors as detailed in Table 1. No changes are required to circuit connections.

TABLE 1

Resistor values

Circuit Reference	Value	
	6010	6010A
R121	6·8k ± 10% $\frac{3}{4}$W	33k ± 10% $\frac{1}{2}$W (J.S. 5905-99-022-2195)
R132	6·8k ± 10% $\frac{3}{4}$W	33k ± 10% $\frac{1}{2}$W (J.S. 5905-99-022-2195)
R143	6·8k ± 10% $\frac{3}{4}$W	33k ± 10% $\frac{1}{2}$W (J.S. 5905-99-022-2195)
R123	15k ± 10% $\frac{1}{4}$W	68k ± 10% $\frac{1}{2}$W (J.S. 5905-99-022-3018)
R134	15k ± 10% $\frac{1}{4}$W	68k ± 10% $\frac{1}{2}$W (J.S. 5905-99-022-3018)
R145	15k ± 10% $\frac{1}{4}$W	68k ± 10% $\frac{1}{2}$W (J.S. 5905-99-022-3018)

Chapter 3

POWER UNIT 4465

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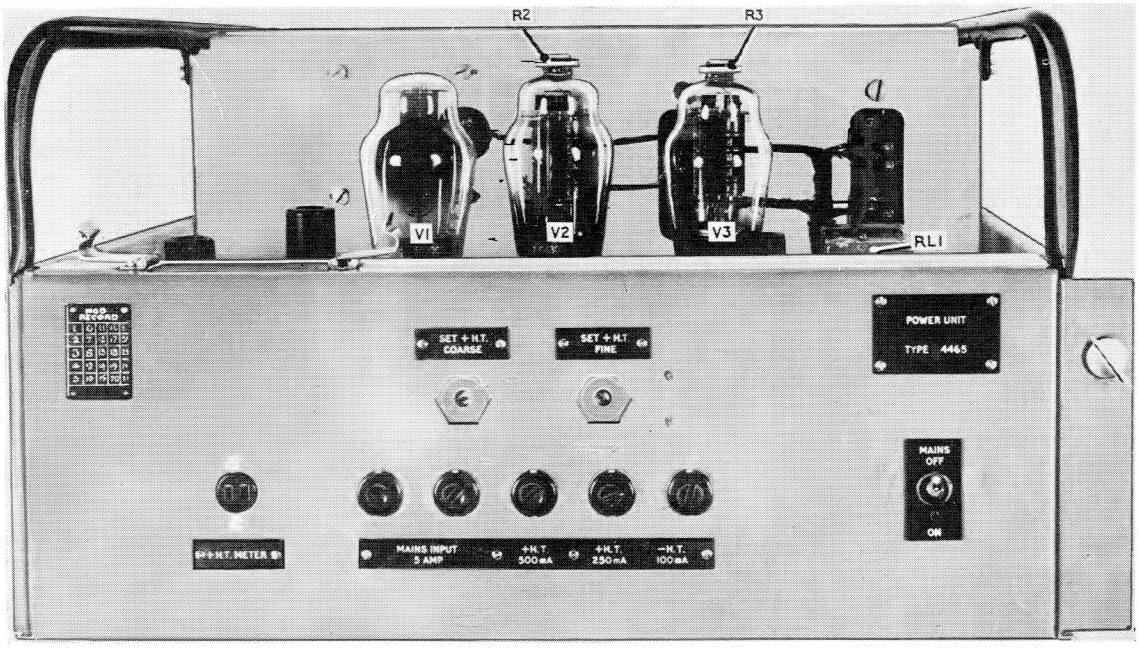

Fig. 1. Power unit 4465: front view

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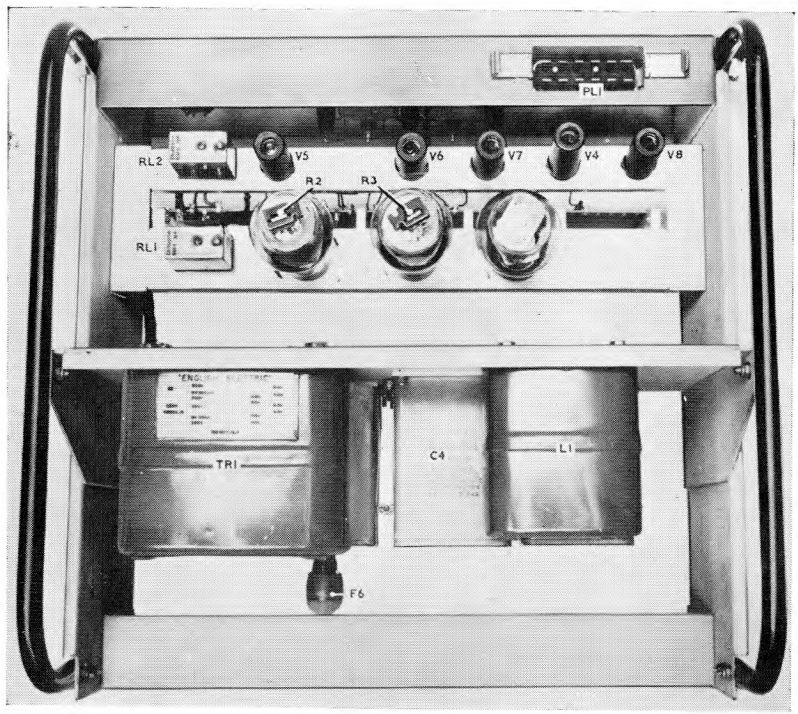

Fig. 2. Power unit 4465 : Top View

General

1. Power unit 4465 provides the positive and negative HT supplies required by waveform generator 6010. The unit operates from the 230V 50 c/s single-phase supply and delivers a stabilized output of 300V at 200mA together with an unregulated supply which is stabilized at –75V by a gas-filled stabilizer in the waveform generator.

2, General views of the power unit are given in fig. 1, 2 and 3. It is normally housed in rack (IFF control) 4467 and consists of a box-section sheet steel framework to which are secured vertical and horizontal sub-chassis carrying the various components. Handling is facilitated by the provision of tubular steel frames at the top of each side member.

Circuit description (*fig. 4*)

+300V. and –75V. supplies

3. The 230V 50 c/s single-phase supply is brought in on pins 11 and 12 of the 12-pole plug PL1 and is fed via the main on/off switch SW1 and fuses FS1 and FS2 to the primary winding of transformer TR1. A thermal fuse is included in the primary circuit to disconnect the mains supply in the event of the transformer becoming overheated.

4. TR1 has two high-voltage secondary windings delivering 500V–0–500V and 350V–0350V together with four heater windings for the valves in the unit. The output from the 500V–0–500V winding is applied to the anodes of a full-wave rectifier valve V1 and the DC output is smoothed by the capacitance-input filter consisting of C4, L1, C5 and C6. R23, connected in parallel with C4, is included to discharge the capacitor in the event of L1 becoming open-circuited.

5. From the filter circuit the DC output is fed to a stabilizer circuit formed by the series regulator valves V2, V3 and the associated control valve V6. The reference level for V6 is established by the gas-filled stabilizer valve V7 which maintains V6 cathode at a constant potential irrespective of the current through the valve.

6. The unregulated DC is applied to the anodes of V2, V3. Due to the impedance of these valves a voltage drop occurs across them, its magnitude being dependent upon their grid voltage. The grids of V2, V3 are returned to the anode of V6 whose grid is taken to the sliders of two potentiometers RV1 and RV2. Each potentiometer forms part of a resistor network connected between the +300V output and earth.

7. Any tendency of the HT output to vary from the nominal value of +300V causes a change of current through the networks and a resultant change in potential at V6 grid. These changes in grid potential are amplified by V6 and applied to the grides of V2, V3 to counteract the original variation in output level.

8. Since the anode of V6 is connected to the grids of V2, V3 and these valves operate at a low value of grid/cathode bias, the anode potential of V6 would be only slightly below +300V if R10 were returned to the stabilized line. However, in order to realise sufficient gain from V6 and ensure an adequate range of control,it is necessary to provide an HT source of considerably higher potential than 300V. This is achieved by the auxiliary stablilizing circuit consisting of R4, R11 and the gas-filled stabilizer valve V5, thus obtaining an effective HT supply of 375V for V6.

9. Two resistor networks with different values are included to afford coarse and fine adjustment of the stabilized output level. RV1 enables the output to be varied between the limits of 270V to 315V while RV2 varies the output by 5V about the mean set by the coarse control. This facility is of particular importance in multi-channel installations where one waveform generator may be supplied from either of two power units both of which must maintain the same HT output within close limits.

10. The normal load current of the power unit is within the rating of a single CV345, and if this were the only consideration, one series regulator valve would be adequate. However, when the waveform generator is first switched on, current surges up to 330mA occur, the current being reduced to approximately 180mA in the first second providing the unit is being triggered. For this reason the source impedance must be low, necessitating the use of two series regulator valves in parallel.

11. In addition to the primary fuses, further protection is afforded by FS3, connected between the secondary centre tap and earth, and FS4 in the stabilized output line. FS4 is a special magnesium nickel fuse designed to withstand the initial surges when the waveform generator is switched on.

12. The output from the 350V–0–350V secondary winding is fed to the anodes of a full-wave rectifier valve V4 and the resultant DC output is smoothed by C1 and C2 in conjunction with the inductance of the coil of relay R12. Since the full load current from this supply is only about 10mA, adequate stabilization is obtained with a gas-filled stabilizer valve. To ensure constancy of bias voltage when the power unit is changed, the stabilizer is incorporated in the waveform generator and not in the power unit. The gas-filled stabilizer V8 shown in the circuit diagram is included solely to prevent an excessive rise in the negative line when the waveform generator is not connected. It holds the output level at approximately –150V and is extinguished when the stabilizer in the waveform generator takes control and limits the voltage to –75V.

13. Protection for the negative supply is afforded by a fuse FS5 connected in series with the negative line.

14. The efficiency of the stabilizing circuits is such that for a change in the AC input voltage of $\pm$ 6 per cent, the varation in the positive H.T. line is less than $\pm$ 0.04 per cent, i.e. + 0.125V in 300V. The corresponding variation in the negative supply is + 0.7 per cent or $\pm$ 0.5V in 75V.

Control circuits

15. The outputs from the power unit are controlled by the action of two relays RL1 and RL2. The coil of RL1 is connected in series with RL6 across the +300V stabilized supply while that of RL2 is connected between the positive side of the negative supply and earth. In the de-energized condition, contacts RL1/1 break the 6.3V supply to the heater of V4, contacts

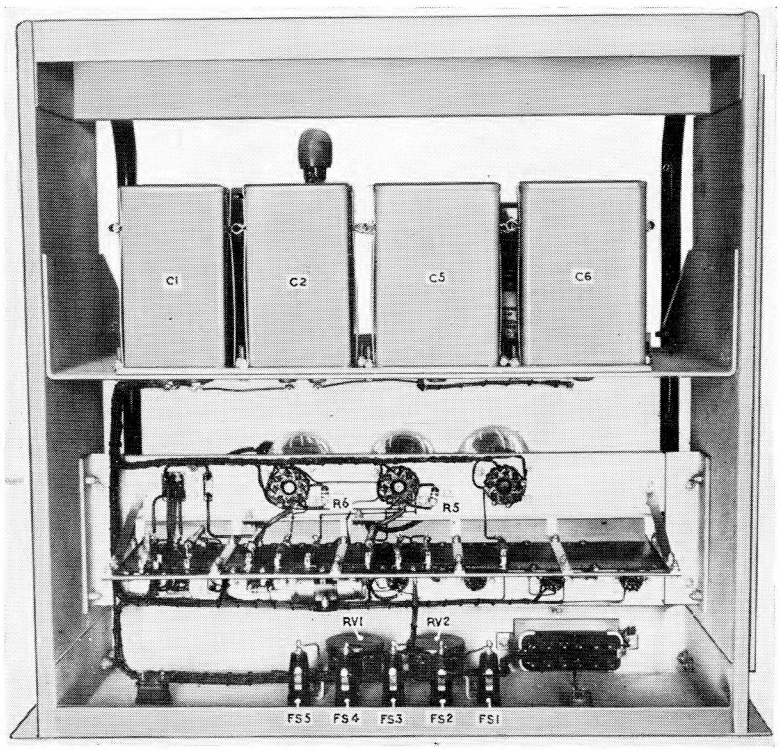

Fig. 3. Power unit 4465: Under side View.

(A.L. 2, Sep. 56)

RL1/2 in parallel with RL2/2 earth PL1/6 and contacts RL1/4 in series with RL2/4 break the circuit to the HT indicator lamp at the top of rack (IFF control) 4467. Contacts RL2/1 and RL2/3 in parallel break the +300V connection to PL1/8.

16. When the power unit is switched on the positive HT supply becomes available first so that RL1 is energized and contacts RL1/1 make to complete the heater circuit of V4. At the same time contacts RL1/2 break while contacts RL1/4 make. After a delay equal to the time taken by the heater of V4 to attain its operating temperature, the negative supply appears and RL2 is energized. Contacts RL2/1 and RL2/3 make so that the +300V supply is connected to PL1/8 and thence to the waveform generator. Simultaneously, contacts RL2/2 break and remove the earth from PL1/6 while contacts RL2/4 make and apply 6.3V to the HT indicator lamp.

17. The introduction of a delay period by switching the heater of V4 ensures that the +300V supply has time to settle down and regulate before the load is applied. The remainder of the switching sequence is protective. If the negative supply fails, RL2 is de-energized and the positive supply is immediately disconnected from the waveform generator.

18. Should either supply fail, causing RL1 or RL2 to be de-energized, the HT indicator lamp is extinguished and PL1/6 is earthed. By earthing PL1/6 the automatic changeover system is brought into operation so that the faulty power unit is replaced by a spare unit. A full description of the system is given in Chapter 1 of this section.

Metering

19. To facilitate measurement of the +300V line when checking and adjusting the stabilized output, a socket SK1 is provided on the front panel for the connection of an external meter.

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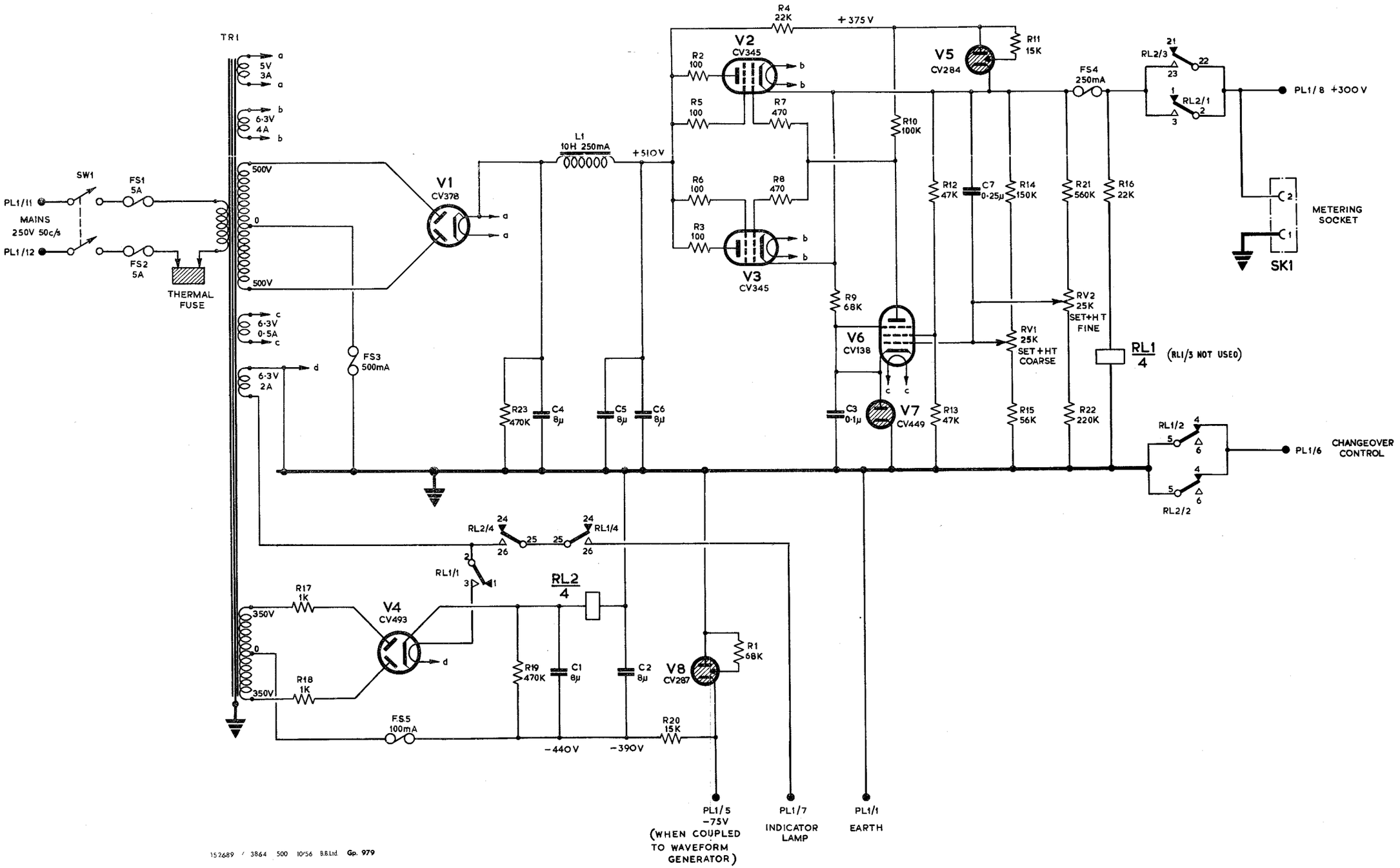

Fig.4 Power unit 4465 - circuit (A.L.2 Sep.56) Fig.4

Chapter 4

RELAY UNIT 6009

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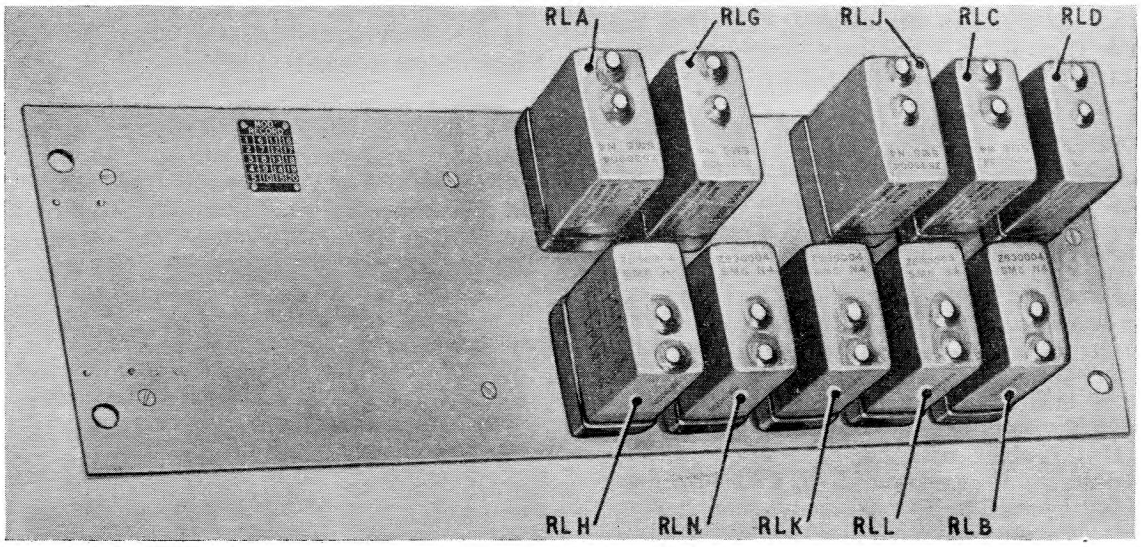

Fig. 1. Relay Unit 6009: general view

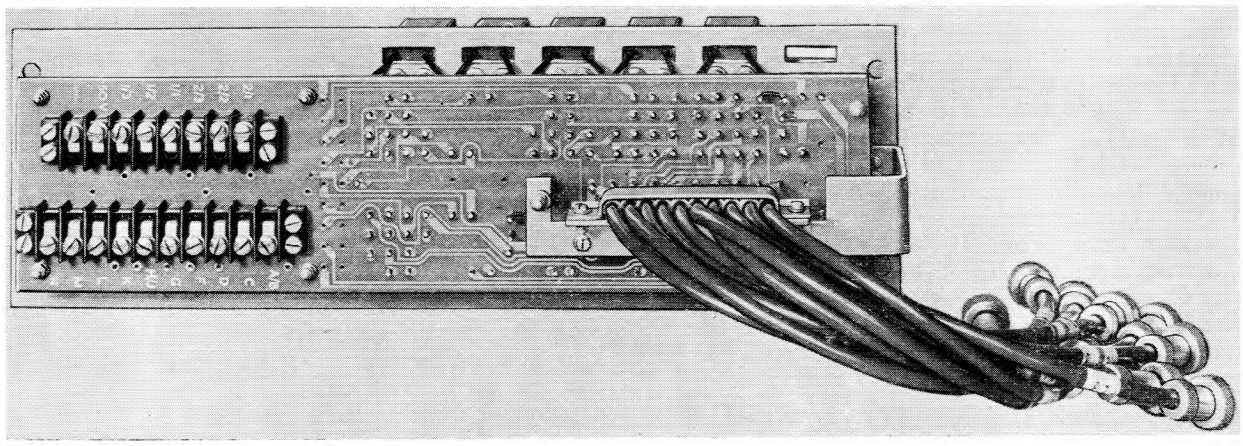

Fig. 2. Relay Unit 6009: interconnection panel

General

1. Relay unit 6009 provides the means by which the operator of each display console can call for and select his specific requirement from the general IFF Mk. 10 system. Each Mk. 10 installation normally includes a number of these units housed in a rack (*Chapter* 5) but in this chapter the operation of the basic unit only is considered since this is not affected by the number of units employed.

2. The relay unit is illustrated in fig. 1 and 2 and consists of a panel with ten relays mounted on one side. On the other side of the main panel and spaced from it by stand-off pillars, is a sub-panel carrying a printed circuit for the relay interconnections. Video input and output connections are made through flying leads of coaxial cable terminated in plugs. Two terminal blocks are provided for the switching connections.

3. Relay unit 6009 is designed to provide switching facilities and to carry video information for two consoles from either of two interrogators. It thus has two entirely separate channels on a single panel, the inputs being derived from the two common sources. In installations with three or four interrogators it is necessary to connect relay units in pairs to provide equivalent facilities.

Circuit description

4. A circuit diagram on which all the relay contacts are shown in the de-energized positions is given in fig. 3.

5. Channel 1 consists of relays A, B, C and D. Relays A and B control the selection of waveform generators 6010 in multi-channel installations and, where only one head is employed, are not used. Relays C and D perform the function of mode switching for console 1. Channel 2 consists of relays H, J, K and L operating in a similar manner for console 2. The purpose of relays G and N is to prevent interaction between the mode switching circuits when the relay units are coupled in pairs in installations with three or four interrogators (*para.* 11).

6. Consider a simple installation with one interrogator and two displays. When −50V is applied to terminal G, relay G is energized so that contacts G5/6 and G25/26 make, connecting −50V to the coils of relays C and D. If mode 1 is required by console 1, operation of the mode selection switch on that console connects terminal C to earth. Relay C is then energized so that contacts C2/3 make and terminal 1/1 is earthed through A4/5, C3/2 and D21/22. By thus earthing terminal 1/1 an earth is placed on the appropriate point of the circuit in waveform generator 6010 (*Chapter* 2). Also, with relay C energized, mode 1 video from the waveform generator is fed to PL4/1 from PL1/1 through B1/2, C6/5 and D24/25.

7. When console 1 calls for mode 2, terminal D is earthed, causing relay D to be energized. Terminal 1/2 is then earthed via A24/25, C21/22 and D23/22. If mode 3 is required, relays C and D are both energized by earthing terminals C and D through the mode selection switch. Terminal 1/3 is then earthed via A21/22, C23/22 and D23/22. In each case the correct video input is fed to PL4/1 through either B4/5, C24/25 and D26/25 or B24/25, C26/25 and D26/25.

8. Since parallel paths are provided between input and output, console 2 can make its own demands on the system without affecting the console 1 display. With −50V supplied to terminal N, relay N is energized, causing contacts N5/6 and N25/26 to make so that −50V is connected to the coils of relays K and L. By earthing terminals K or L or both together, mode switching is obtained as follows:—

Mode 1. Terminal 1/1 earthed through H24/25, K3/2 and L21/22

Mode 2. Terminal 1/2 earthed through H4/5, K4/5 and L23/22

Mode 3. Terminal 1/3 earthed through H1/2, K6/5 and L23/22.

The corresponding video inputs are routed to PL4/2 via J24/25, K23/22 and L24/25 for mode 1; J21/22, K24/25 and L26/25 for mode 2; J4/5, K26/25 and L26/25 for mode 3.

9. Where the installation has more than one radar head and interrogator, relays A, B, H and J come into operation. Through the head selector unit in the radar office, when the second head is selected by the head selector switch on console 1, the −50V supply to terminal G is removed and connected to terminal A/B so that relays A and B are energized. The change-over contacts of relay A transfer the mode switching control lines to terminals 2/1, 2/2 and 2/3 while those of relay B switch the video lines to PL2/1, PL2/2 and PL2/3. Relays H and J perform the same function for console 2 when the head selector switch on that console is operated.

10. Since the −50V supply is removed from terminals G and N by the operation of the head selector switches, relays G and/or N are energized through contacts A2/3 and H22/23. This ensures that the unused relay unit in a coupled pair is completely inoperative.

11. The reason for the inclusion of relays G and N is made clear by the simplified diagram of fig. 4 which shows some of the interconnections between two relay units 6009 when mounted in a rack (relay unit) 4495. This arrangement only occurs in installations with three or four interrogators. In the drawing the contacts of relay G in the left-hand unit are shown in the energized position. It will be noted that the earthy ends of both relays C and both relays D are connected together and that from these common connections control wires are taken to the console. With the normal connections shown in fig. 4(a), only the appropriate relay is energized when the mode switch is closed. However, if the −50V supply were fed directly to the relays, then the circuit would appear as in fig. 4(b).

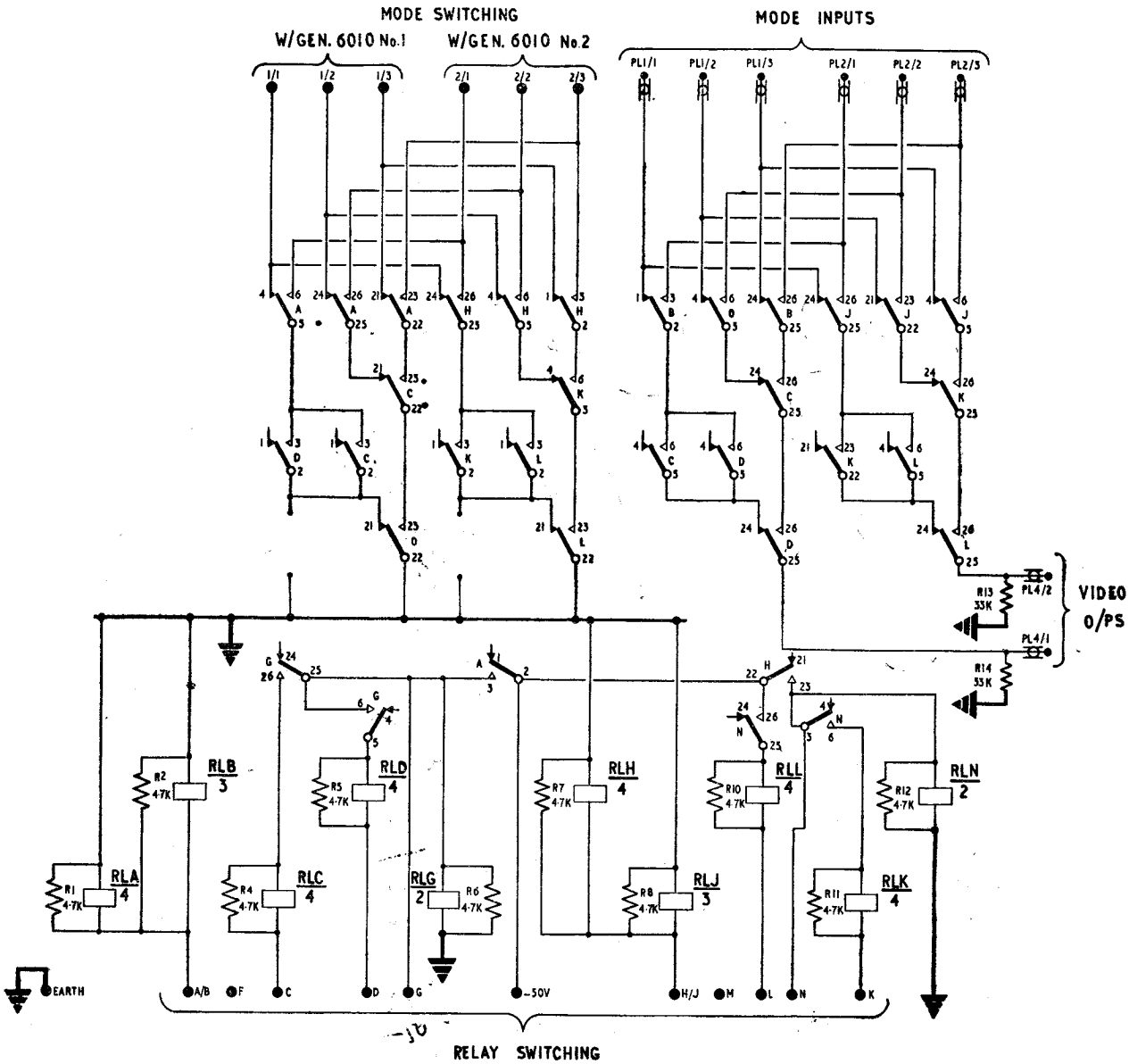

Fig. 3. Relay unit 6009: circuit

In that case, whilst the required relay would be energized by current i_1, a current i_2 could flow through the other relays and, although the three coils are in series across the 50V supply, this current could be sufficient for energizing purposes. The same considerations apply to channel 2 where relay N functions in a similar manner.

12. A resistor is connected across each relay coil. This is included to limit the voltage transient produced by the sudden interruption of the energizing supply when the control switches are operated, thus preventing possible interference on the displays.

13. It is clear that a single relay unit can handle the switching for two interrogators and two consoles. In multi-channel installations therefore, relay units 6009 have to be provided on the scale of one for every two interrogators per pair of consoles.

14. Input and output connections are clearly marked on the unit and are designated as follows:—

PL1/1—mode 1 } video signal coaxial inputs
PL1/2—mode 2 } from channel 1 waveform
PL1/3—mode 3 } generator

PL2/1—mode 1 } video signal coaxial inputs
PL2/2—mode 2 } from channel 2 waveform
PL2/3—mode 3 } generator

Terminals 1/1—mode 1 } mode command lines
1/2—mode 2 } to channel 1 wave-
1/3—mode 3 } form generator

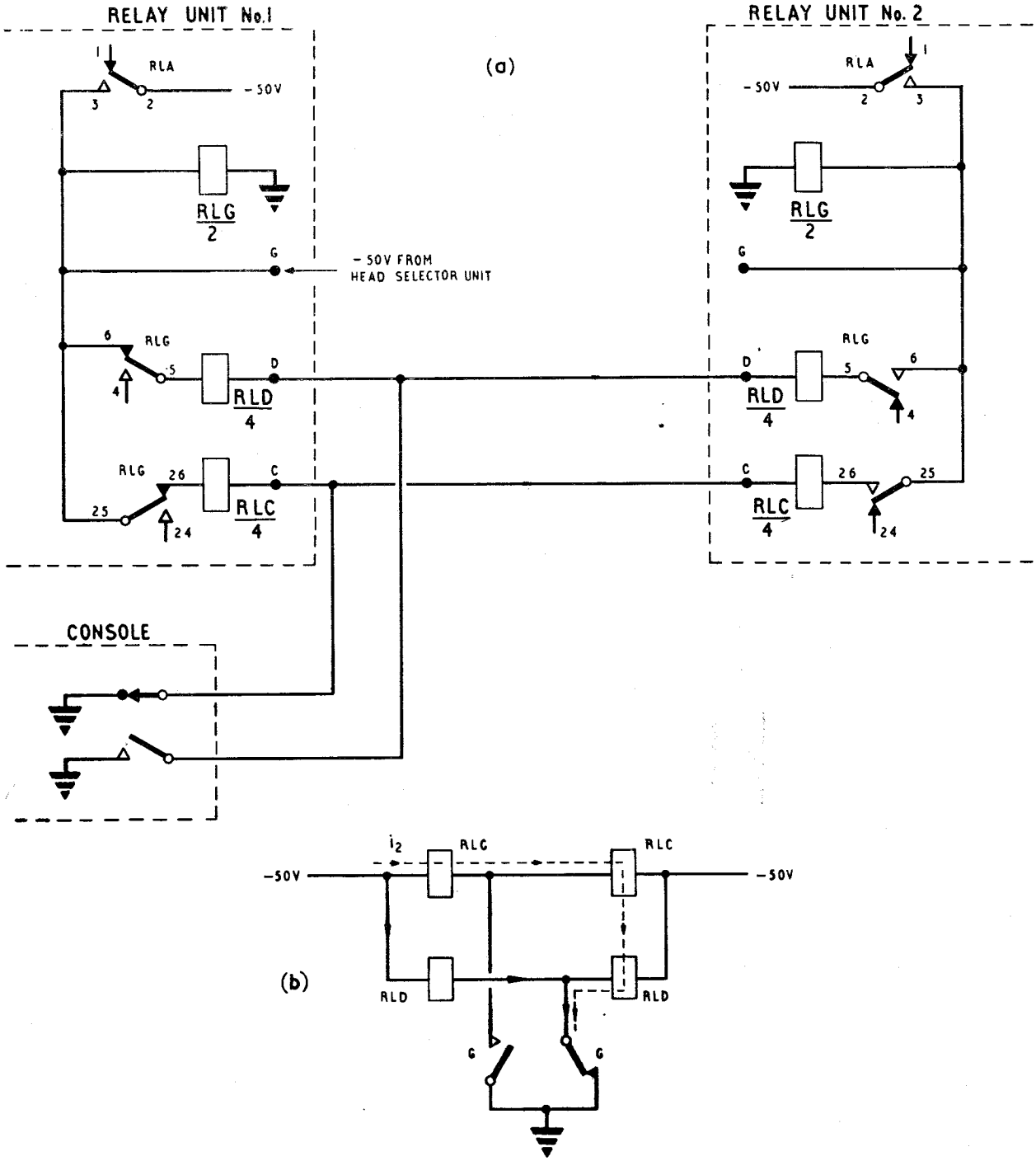

Fig. 4. Simplified diagram showing function of relays G and N

Terminals 2/1—mode 1, 2/2—mode 2, 2/3—mode 3 } mode command lines to channel 2 waveform generator

Terminals —50V—negative side of 50V supply
Earth—positive side of 50V supply and station common earth

Terminals C, D } control lines from display console 1

Terminals K, L } control lines from display console 2

Terminals G, A/B, N, H/J } —50V from head selector unit

PL4/1—video signal coaxial output to display console 1

PL4/2—video signal coaxial output to display console 2

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Chapter 5

RACKS (RELAY UNIT) 4468, 4494 and 4495

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LIST OF ILLUSTRATIONS

General

1. When installed in the radar office, the relay units described in Chapter 4 are housed in a rack. Three sizes of rack are available to meet different requirements. The relay rack is normally located adjacent to the rack (IFF control) 4467 with which it is associated (*fig.* 1), the interconnecting cables passing through a duct below the racks.

Construction

2. Each rack consists of a steel cabinet, 23½ in. wide overall and 21 in. deep with doors at the front and rear, and contains a sub-frame on which the relay units are mounted. This frame can be rotated through 90 deg. to permit easy and immediate access to all the wiring. During normal use, rotation is prevented by a locking pin in the bottom section of the frame.

3. Video information from the interrogator(s) is brought in on coaxial cables which terminate at a group of sockets mounted on one internal face of the sub-frame. Similarly, outgoing video signals are conveyed to the consoles from other coaxial sockets situated on the same face. The adjacent external side of the frame carries groups of coaxial sockets, the corresponding sockets in each group conveying incoming video signals being wired in parallel to the input sockets at the bottom of the rack. Thus, when a relay unit is mounted in any one of the rack positions and the flying leads are connected to the appropriate adjacent coaxial sockets, the correct video connections are established.

4. All the DC connections, consisting of the mode command lines to the waveform generators, the mode control leads from the display consoles and the radar head selection control leads from rack assembly 184, are brought in through 12-pole plugs and sockets mounted on the opposite side of the sub-frame. The DC wiring is carried up the side of the frame and, at each relay unit position, flying leads terminated in fanning strips (*fig.* 5) are provided for connection to the terminal strips on the relay unit. Since some of the connections are live during operating conditions, insulated stowage points are fitted on the inner side of the sub-frame to afford stowage for the fanning strips when they are not connected to relay units. These stowage points are provided in the upper half of the rack only due to space limitations in the lower half. Hence, in a partly fitted rack it is advisable to mount the relay units in the lowest positions to leave the stowage points available for the unused fanning strips in the upper half and also to facilitate servicing of the installed relay units.

Rack (relay unit) 4468

5. This is the smallest of the three racks and is a 3 ft. 6 in. high cabinet with accommodation for up to 7 relay units on one side of the sub-frame only. It can thus accept video information from two interrogators and provide switching facilities for, and video responses to, any number of display consoles up to a maximum of 14. The application of this rack is likely to be limited and it is probable that it will be used only in training installations.

6. No separate wiring diagram is provided since the cabling is similar to that of rack 4494 with a correspondingly smaller number of video channels. Reference should be made to fig. 6 for the rack connections.

Rack (relay unit) 4494

7. This is a 7 ft. high cabinet, again with provision for mounting the relay units on one side of the sub-frame only. It has a total capacity of 16 relay units so that it can serve up to 32 consoles from two interrogators. A wiring diagram is given in fig. 6.

8. Rack 4494 is intended as the standard radar office fitment on all sites where the number of interrogators does not exceed two. On those sites with 32 displays or less a single rack fitted with the appropriate number of relay units will meet the switching requirements but when there are more than 32 displays a second rack 4494 must be

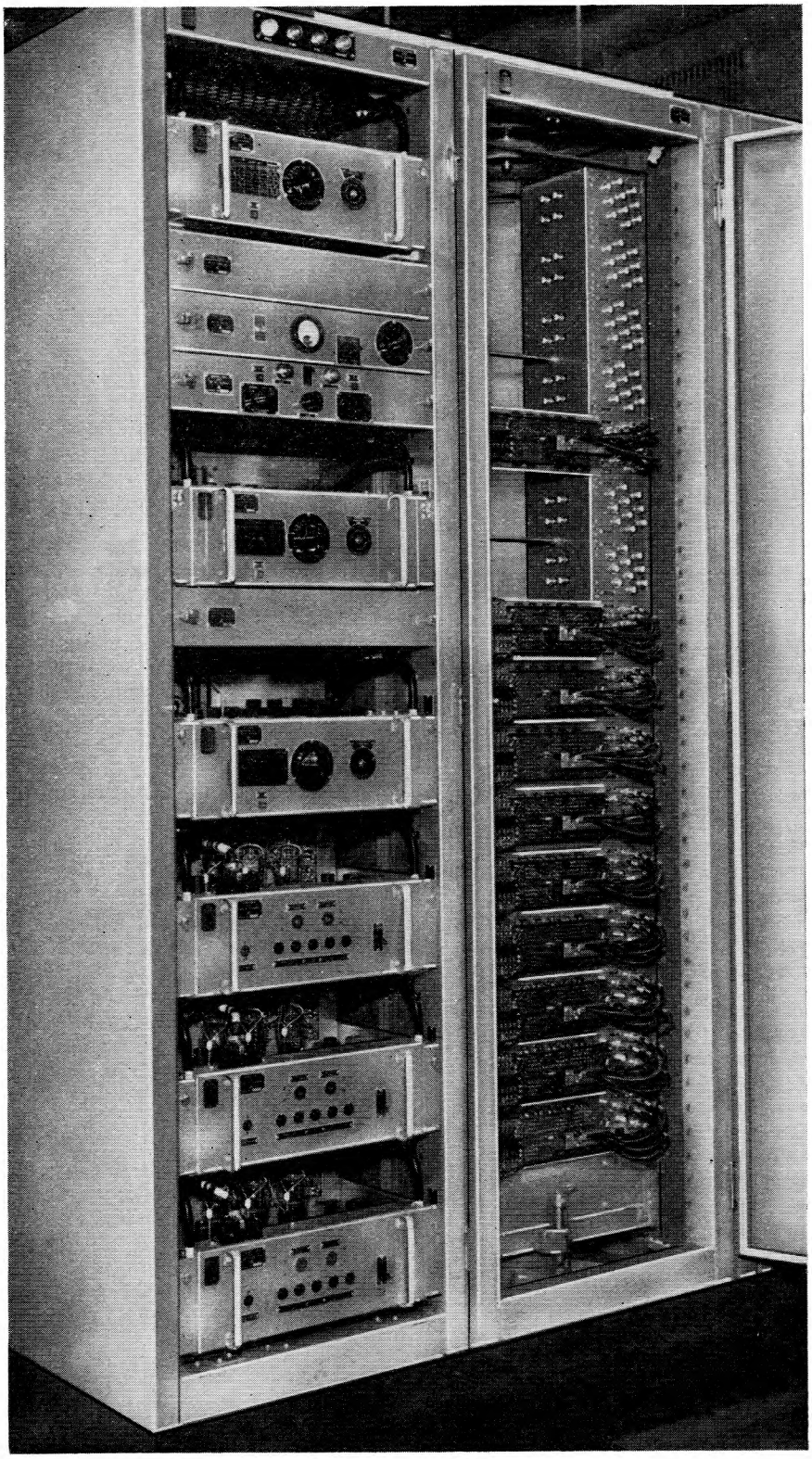


Fig. 1. Relay rack and control rack in situ

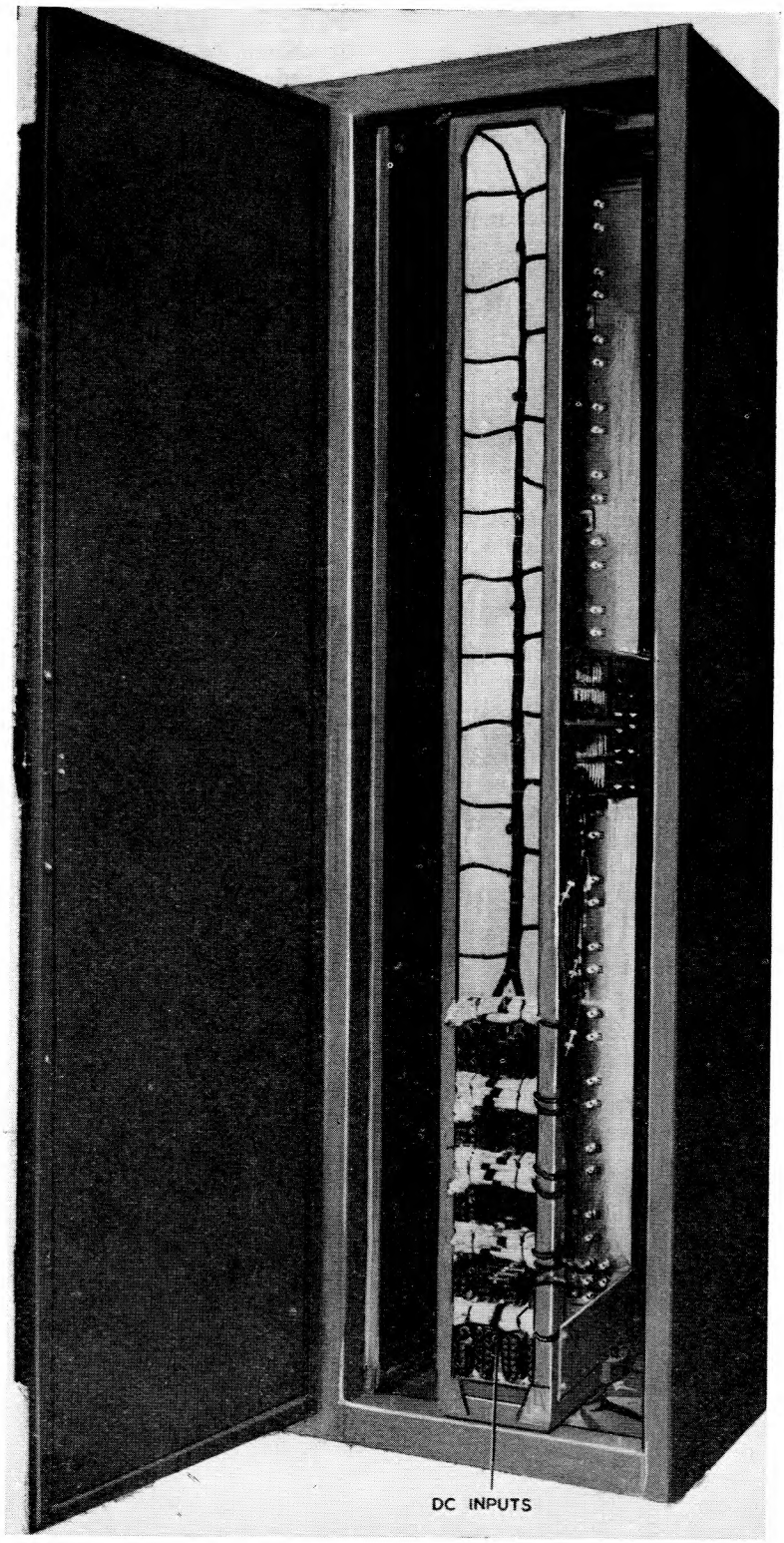


Fig. 4. Rack (relay unit) 4495: rear view with sub-frame rotated

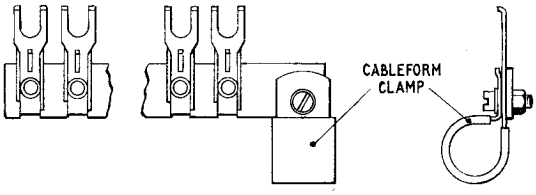


Fig. 5. Fanning strip

provided. It should be noted that, when an installation has two relay racks 4494, an impedance matching unit 12114 must be mounted in the base of rack (IFF control) 4467 to afford an adequately low video output impedance and that the six 68 ohm video input terminating resistors in one of the two racks 4494 must be removed.

Rack (relay unit) 4495

9. Views of this rack, which is the only one illustrated, are given in fig. 2, 3 and 4. These illustrations show the general construction of the cabinet and sub-frame, the only difference between rack 4495 and those previously described being in the provision of mounting facilities for relay units on both sides of the sub-frame.

10. Rack 4495 is designed for use at sites with more than two interrogators and, with a full complement of relay units, can serve four interrogators and 32 displays. It is not intended as an alternative to rack 4494 although it can be used at a site with only one or two interrogators. However, the converse does not apply and rack 4494 cannot be used where there are more than two interrogators.

11. A wiring diagram of rack 4495 is given in fig. 7. In this rack the relay units are coupled in pairs, i.e. that section of the top relay unit on one side of the sub-frame feeding video to PL4/1 is used in conjunction with the corresponding half of the relay unit on the other side of the frame. Similarly, the two halves of the top relay units feeding PL4/2 are used together and so on down the rack. It should be noted however, that there are not 64 independent channels but 32 pairs. Channels 1 and 33, 2 and 34, 3 and 35 and so on are common. Thus, each pair of relay units can select video information from four sources and pass it to two consoles.

12. Each pair of relay units has its mode relays connected in parallel but only in the unit which is supplied with a switching voltage from the head selector unit in rack assembly 184 will the mode relays operate (*Chap.* 4).

13. On very large sites with more than 32 displays similar requirements to those for rack 4494 exist (*para.* 8) and a second rack 4495 is necessary. In this case impedance matching units 12114 must be mounted in the bases of both of the associated racks (IFF control) 4467 and the twelve line terminating resistors in one rack 4495 disconnected.

◀Relay unit connections

14. Since difficulty may be experienced in relating fig. 3 of Chap. 4 to the rack wiring diagrams in fig. 7 and 8, a co-ordinating diagram is provided in fig. 6. This identifies the connections between the relay unit terminal board and the rack fanning strip.▶

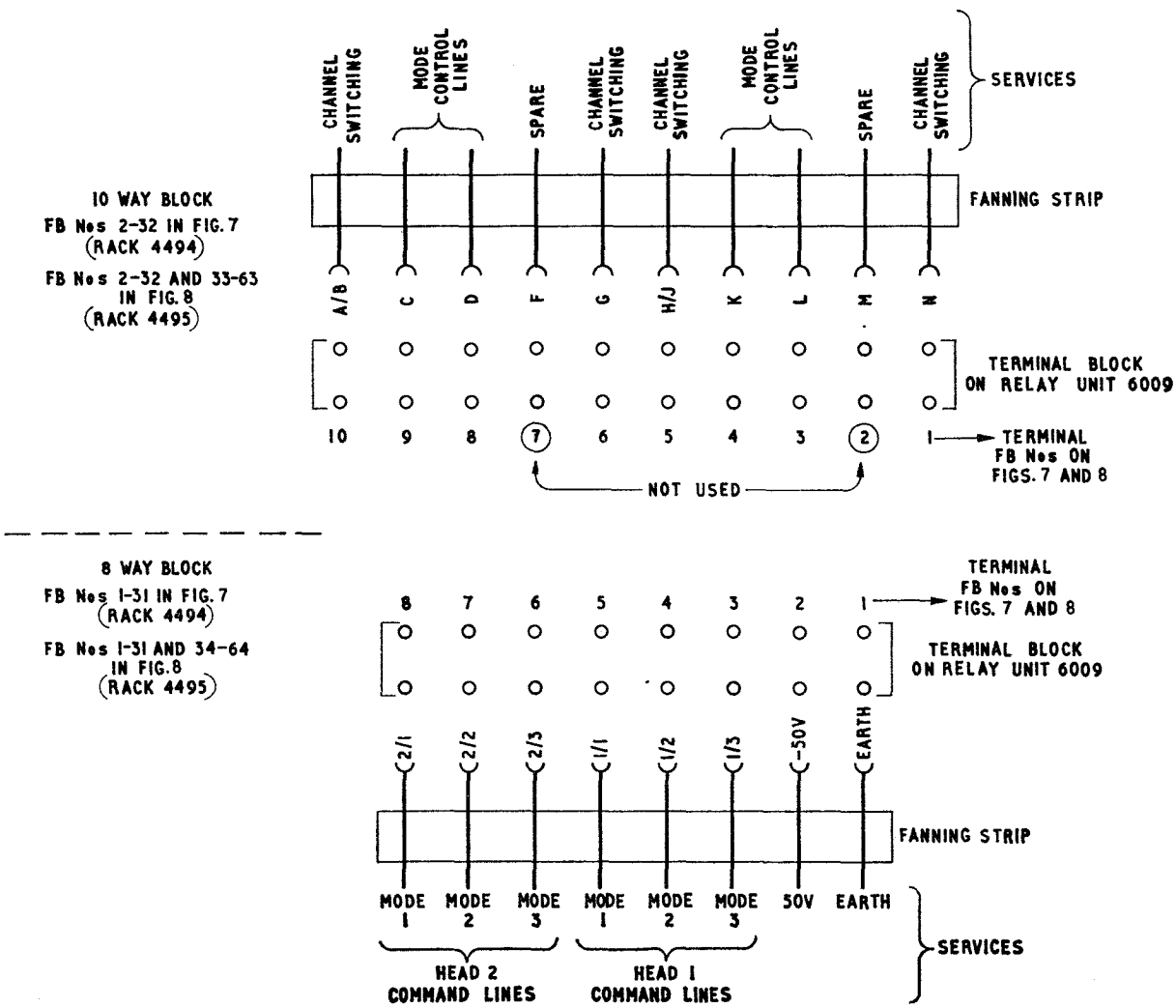
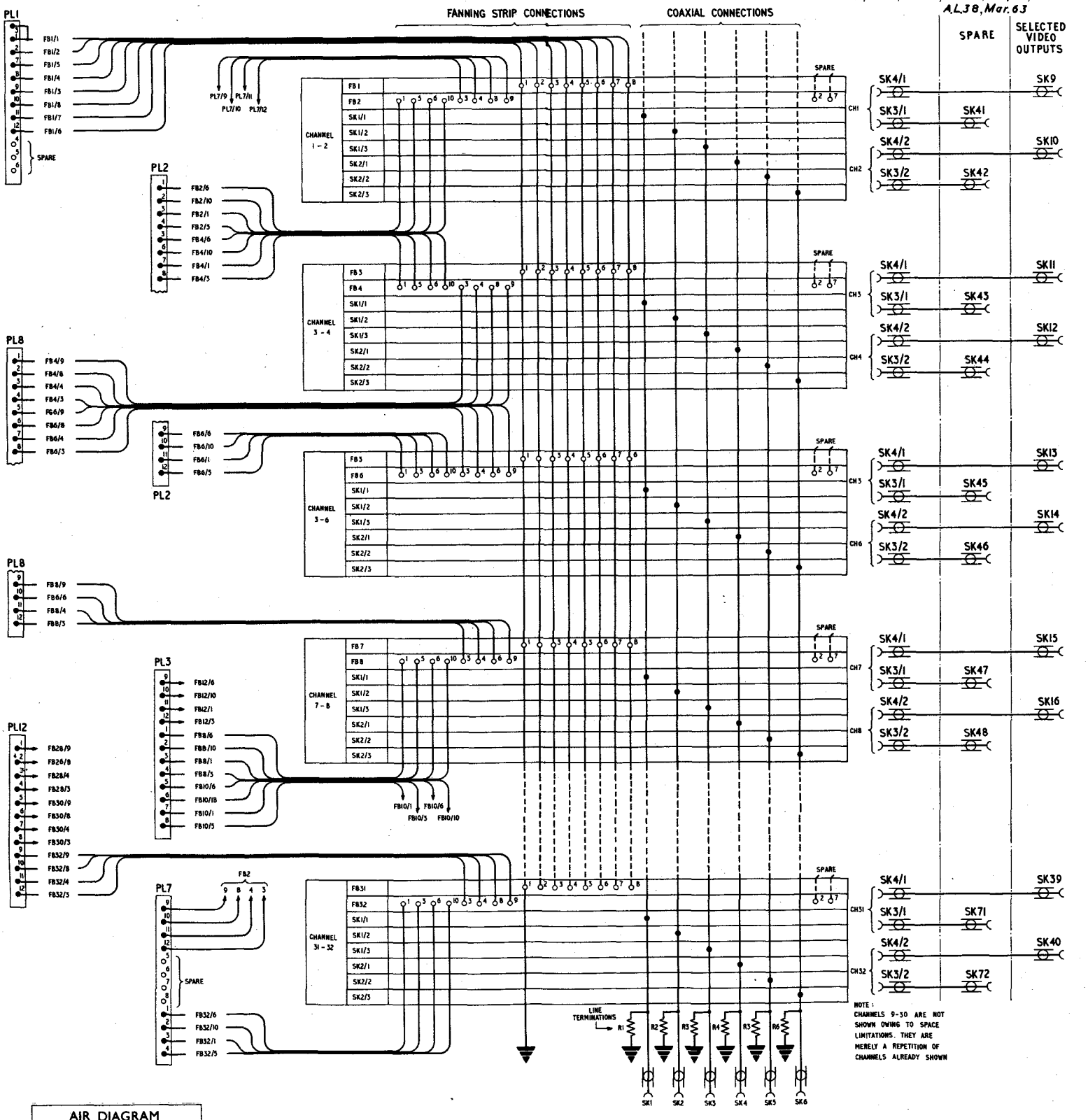


Fig. 6. Relay unit connections



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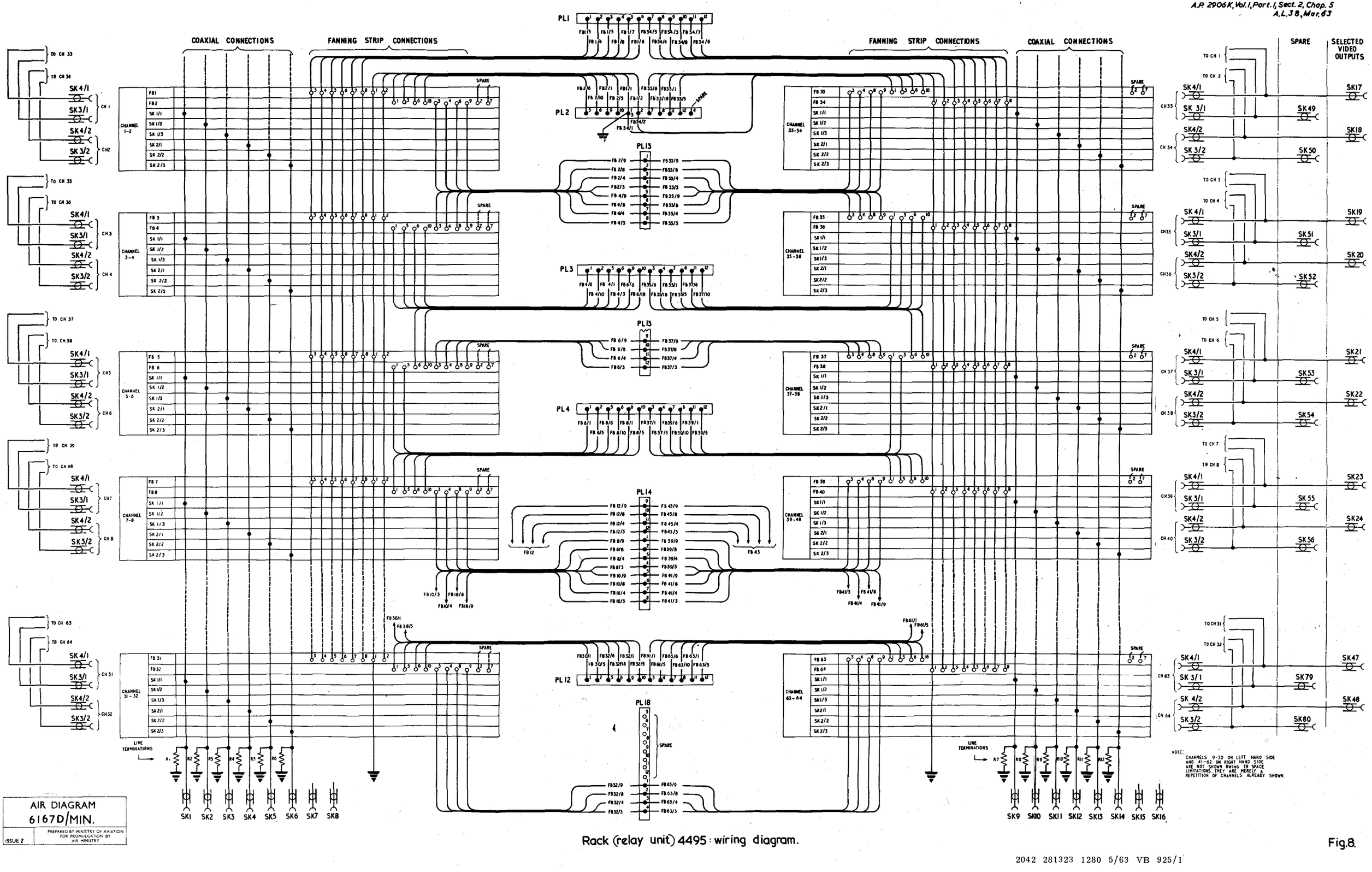
Rack relay unit 4494: wiring diagram.

Fig. 7



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Rack (relay unit) 4495: wiring diagram.

Fig.8.

Chapter 7

MISCELLANEOUS UNITS FOR SPECIFIC APPLICATION

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General

1. In certain installations, additional units are required when IFF Mk. 10 facilities are provided. These units do not form part of the basic IFF Mk. 10 equipment but, on the other hand, neither are they part of the primary installation since in the absence of IFF Mk. 10, they are not normally fitted. Because the units are more closely associated with IFF it is convenient to describe them and their application in this publication.

2. In all, three units are involved. They are selector unit 4535 used in conjunction with a remote Type 7 radar head and control units 6014 and 6022 which are fitted when IFF Mk. 10 facilities are required in the radar photographic display system.

Selector unit 4535

3. When an installation incorporates a remotely sited head such as the Type 7, it may be necessary

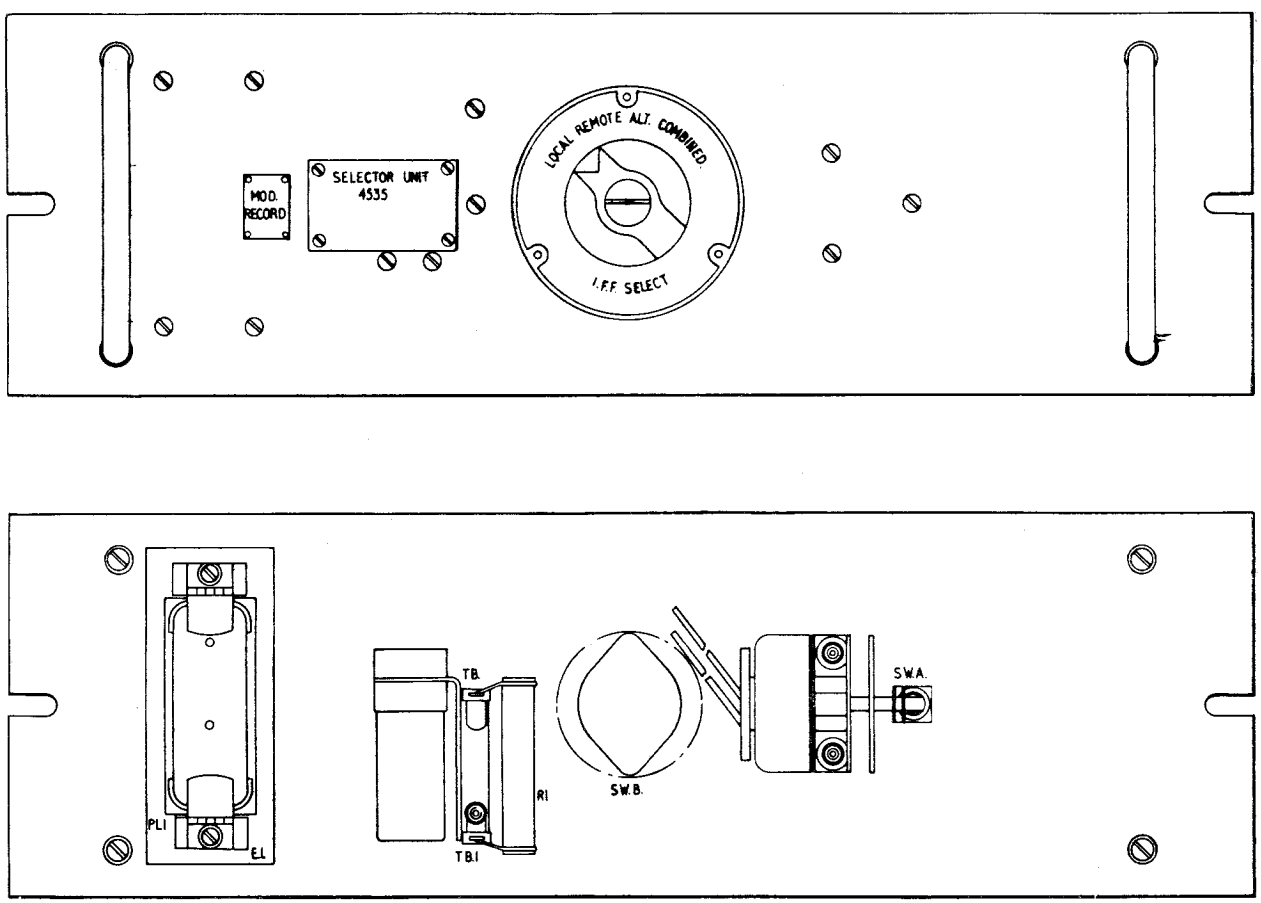

Fig. 1 Selector unit 4535 *(A.L.10, Nov. 57)*

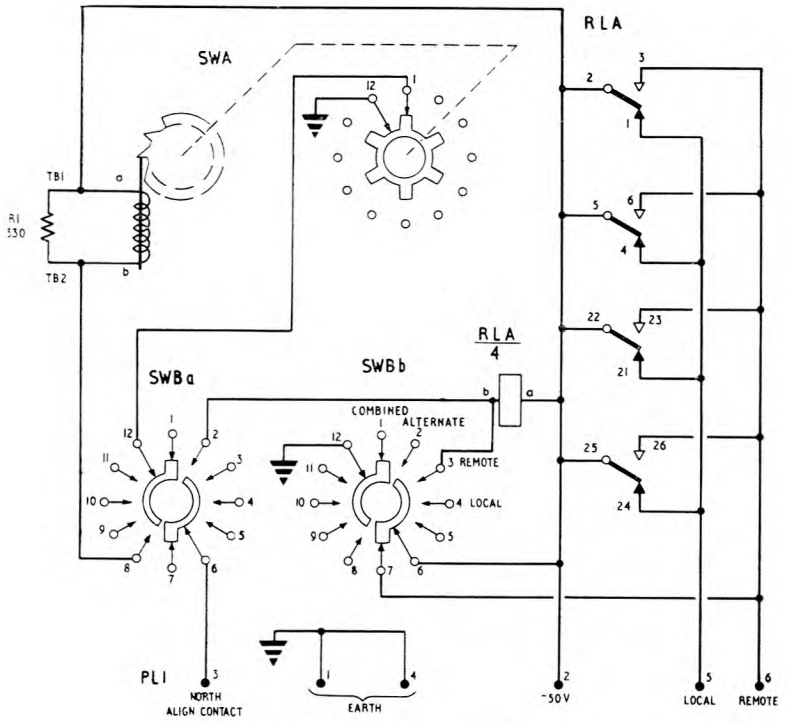

Fig. 2 Selector unit 4535 : circuit

to switch the interrogators at the two sites so that, on alternate rotations of the main site radar head IFF interrogations can be made from each site in turn (*Chap.* 9). This is achieved by switching the 50V DC supply to the IFF control racks through a selector unit 4535 at the main site.

4. Selector unit 4535 (*fig.* 1) consists of a panel on which are mounted a Ledex switch, a wafer switch, a relay and a 12-pole plug for the input and output connections. A circuit diagram is given in fig. 2. Operation of the Ledex switch causes relay RLA to be alternately energized and de-energized so that the 50V supply, fed via the relay contacts, is routed to the required points. The manual control SW B is included to extend the range of facilities afforded by the unit.

5. The coil of the Ledex switch is connected between —50V fed in at PL1/2 and a contact on one wafer of SW B. In fig. 2, SW B is shown in the COMBINED position, i.e. IFF interrogations are made from both main and remote sites simultaneously and the Ledex switch is inoperative.

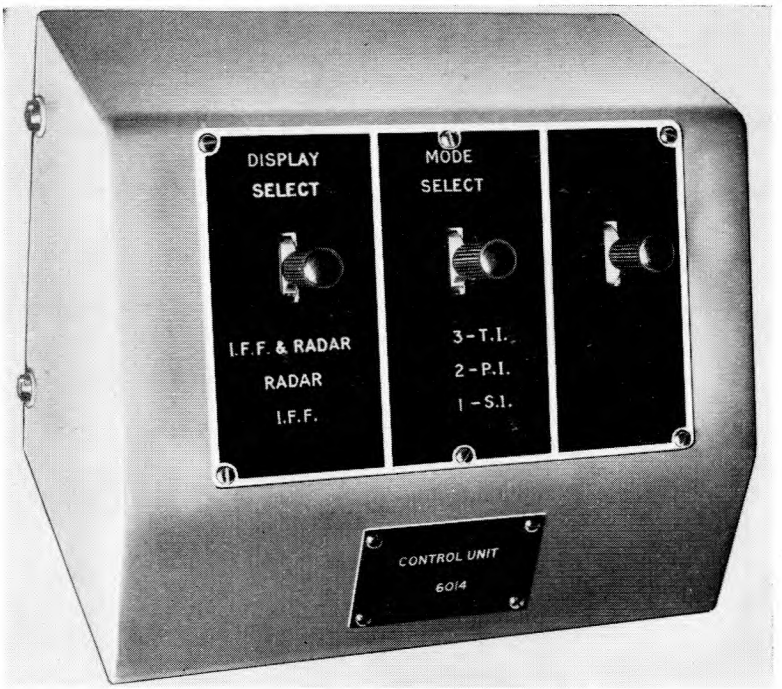

Fig. 3 Control unit 6014 : exterior view

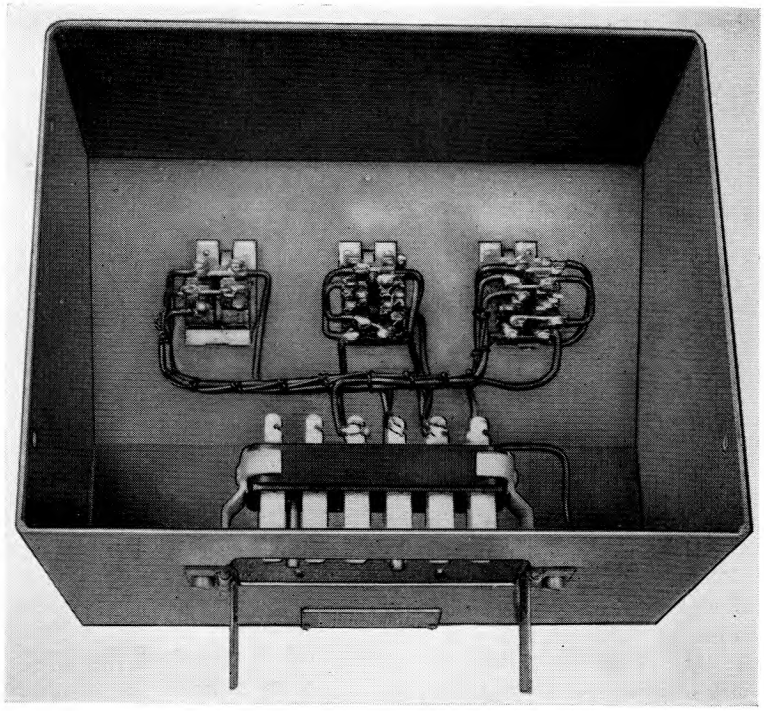

Fig. 4. Control unit 6014 : interior view

The – 50 V supply is fed via the contacts of relay RLA, and contacts 6 and 7 of the second wafer of SW B, to the waveform generators at the main and remote sites, respectively.

6. When SW B is set to ALTERNATE, one end of the coil of the Ledex switch is connected to the auto-align contact associated with one of the radar heads (normally the remote Type 7) and at each rotation of the aerial this contact completes the Ledex switch circuit to earth. The switch rotary contact consequently moves one step at each revolution of the aerial. With the Ledex switch contacts in the position shown in fig. 2 an earth is placed on one end of the coil of relay RLA. The relay is thereupon energized and its contacts change over, removing the – 50 V supply from the main site waveform generators and feeding it to the remote site. On the next revolution of the aerial the circuit to RLA is broken and the relay is de-energized so that the – 50 V supply is fed to the main site waveform generators only.

7. If IFF interrogations are to be made from either the main or remote site only, the manual control is set to either REMOTE or LOCAL as appropriate. In the first case relay RLA is permanently energized and – 50 V is fed to the remote waveform generator alone. In the LOCAL position of the switch, RLA is permanently de-energized and the – 50 V supply is fed to the main site waveform generators only.

Control unit 6014

8. This unit, which is illustrated in fig. 3 and 4, provides display switching facilities for the photographic projector system similar to those on console 64 and is consequently mounted in a position adjacent to the screen of the photographic display. The unit consists simply of a box carrying three GPO-type switches, two of which are marked DISPLAY SELECT and MODE SELECT. In the present application the third switch is not used.

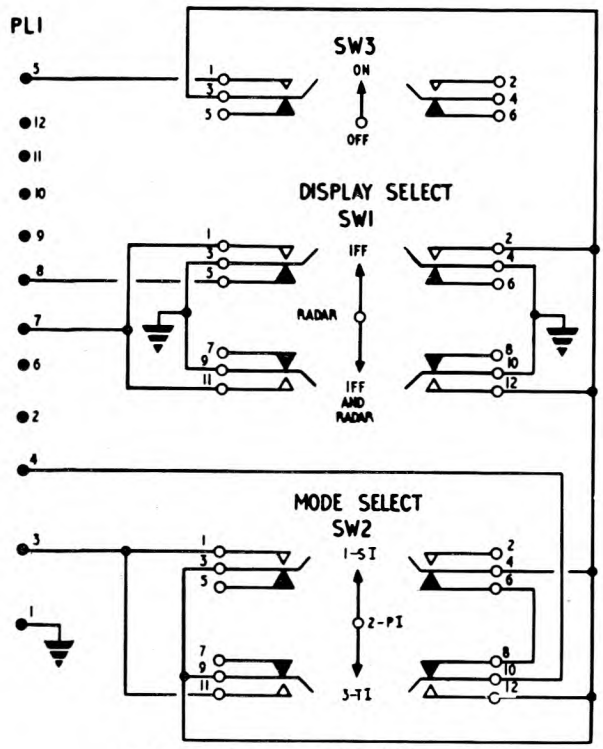

Fig. 5. Control unit 6014 : circuit

Fig. 6. Control unit 6022 : exterior view

9. SW1 (*fig.* 5) controls the display and enables the desired presentation to be obtained, i.e. IFF and radar, radar only or IFF only. In either of the IFF positions this switch completes an earth connection to the mode selector switch and causes the IFF video relay within the photographic projector to be energized. In the IFF & RADAR and RADAR positions of the DISPLAY SELECT switch, the line to the radar on/off relay in the photographic projector is earthed and radar signals are passed to the display.

10. SW2 controls the IFF mode selection and earths the appropriate point in the associated relay unit 6009 depending upon the mode selected. SW3 was originally provided to give a facility no longer required and is not now used.

11. It will be noted from fig. 3 that the positions of switch SW2 are annotated SI, PI and TI in addition to modes 1, 2 and 3. These abbreviations denote respectively Security Identification, Personal Identification and Traffic Identification (*i.e. the functional classification of an aircraft*) and are used in the U.S.A. in preference to the mode numbers. They are included on control unit 6014 in order to provide a link with the American system of nomenclature.

12. Since the photographic projectors are installed in pairs, provision has to be made to change over the IFF control circuits of control unit 6014 when the standby projector is brought into operation. For this reason the leads from control unit 6014 are routed through the companion control unit 6022.

Control unit 6022

13. Control unit 6022, illustrated in fig. 6 and 7, contains two switches and three relays and has three functions : —

(1) Control of mode 1 operation for the standby projector.

(2) Control of the radar on/off relay in the standby projector.

(3) Changeover of the IFF control facilities when the roles of the standby and operational projectors are exchanged.

14. The coils of the three relays RLA, RLB and RLC (*fig.* 8) are connected in parallel and are energized through the operation of a micro-switch mounted on the projector mirror. The leads from control unit 6014 are routed to their destinations through the relay changeover contacts with the result that, depending upon the condition of the relays, the control circuits are connected to the appropriate projector.

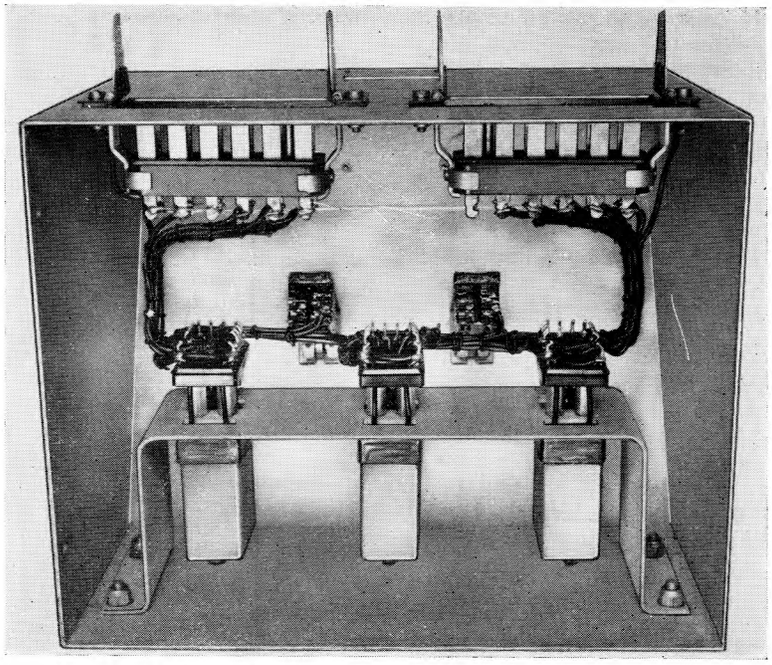

Fig. 7. Control unit 6022 : interior view

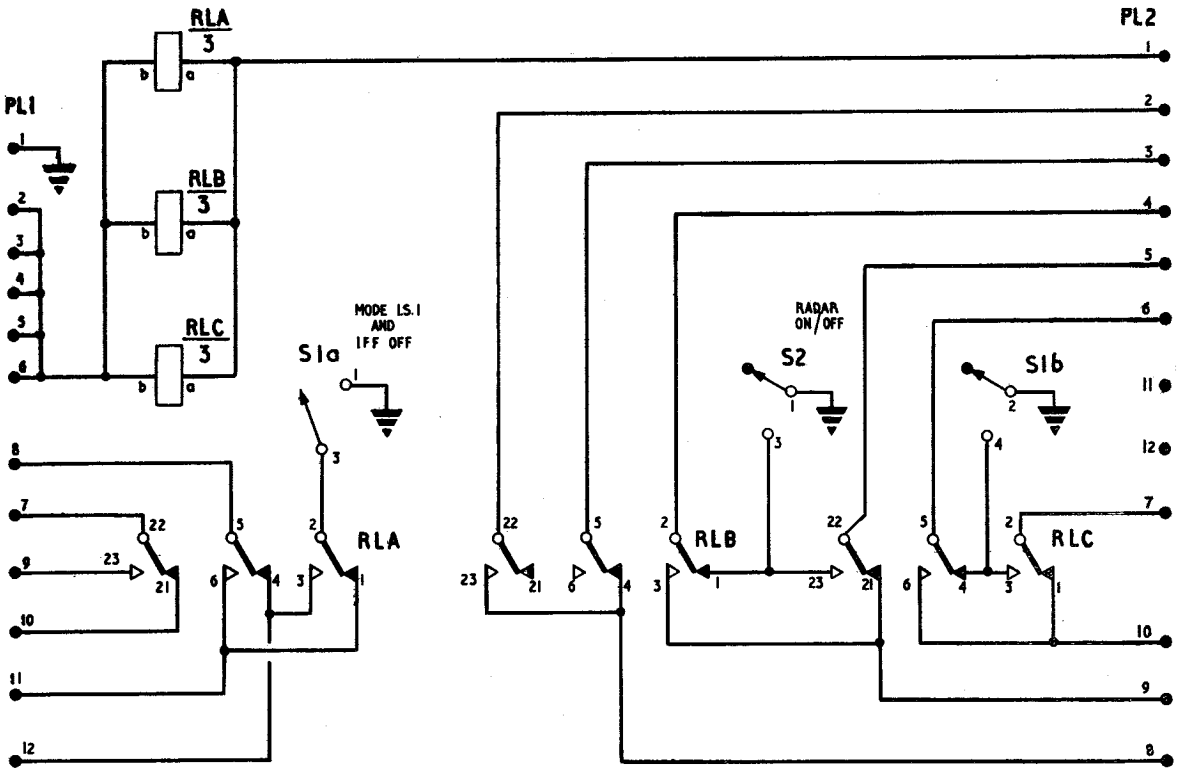

Fig. 8. Control unit 6022 : circuit

◀**15.** The switches on control unit 6022 are used in setting up the standby projector. SW1 (MODE 1 ON/OFF) earths the line to the IFF video relay in the projector so that IFF video may be displayed; at the same time it causes the mode 1 relay in the associated relay unit 6009 to be energized. SW2 (RADAR ON/OFF) causes the radar video relay in the projector to be energized thus permitting the display of radar signals (with or without IFF as required).

16. A diagram showing the interconnections between the two control units, the relay unit 6009 and the projectors is given in fig. 9.

Transformer unit 6428

17. This unit is normally used to provide a 26V centre tapped heater supply for the aerial array 4992. As stated in Sect. 1, Chap. 2 its application is limited and, when required, the unit is mounted in the racks (I.F.F. equipment) 4464 and 6790, and test bench 6042.

18. The unit (*fig.* 10) consists of a potted transformer fitted with a thermal cut-out FS3 and housed within a metal case which forms a mounting for a MAINS ON/OFF switch SW1, a mains input plug PL1, mains input fuses (anti-surge) FS1 and FS2, and output socket SK1, and an ammeter indicating the current being drawn from the unit.

19. Operation of the unit is straightforward, mains being fed via PL1/11 and 12, SW1 in the ON position, and the three fuses to the primary of the step-down transformer T1. The live side of the centre-tapped secondary is connected via ammeter M1 to SK1/A and the neutral side to SK1/B; the centre-tap is earthed via PL1/1.▶

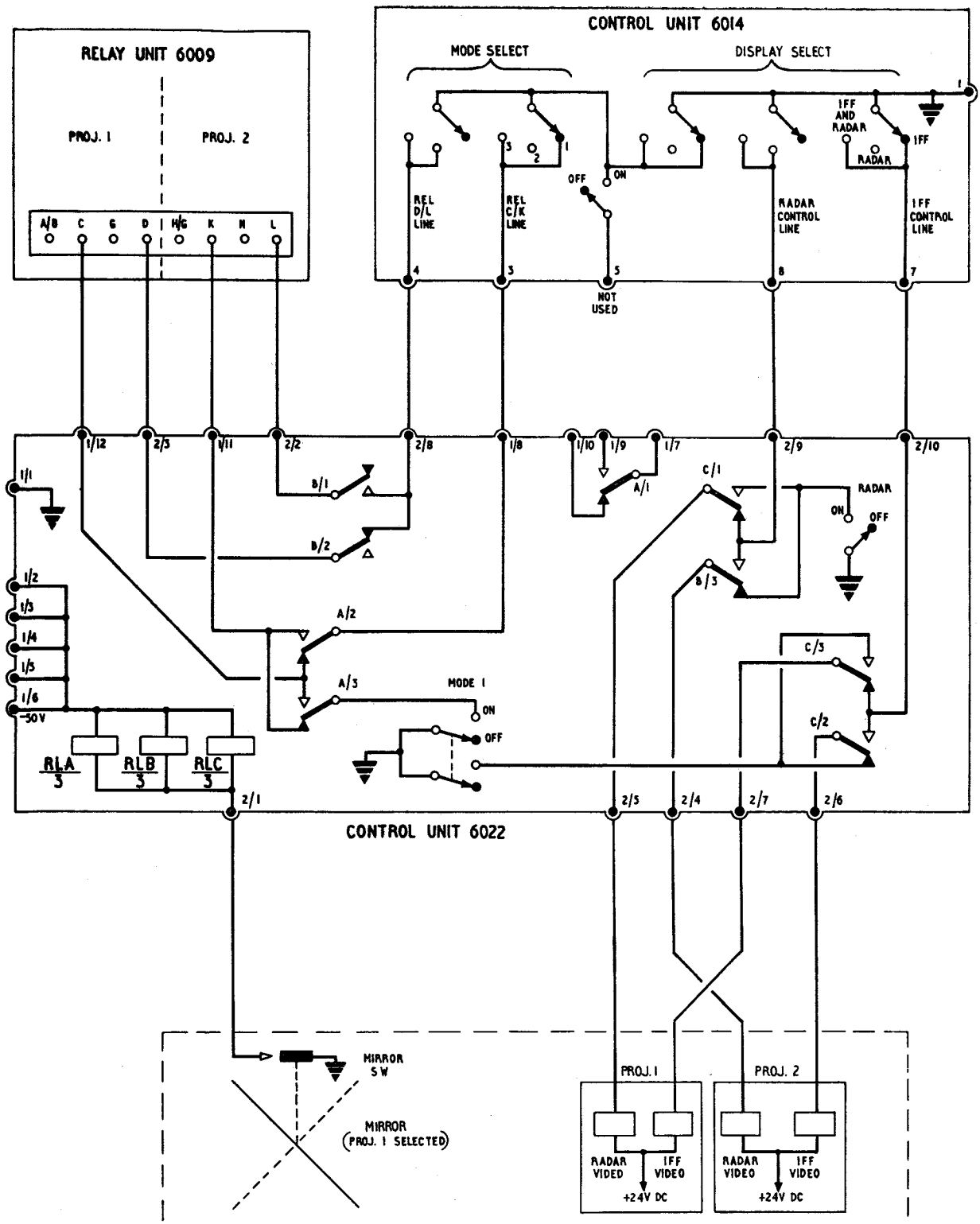

Fig. 9. R.P.D.S. 4498 control circuit

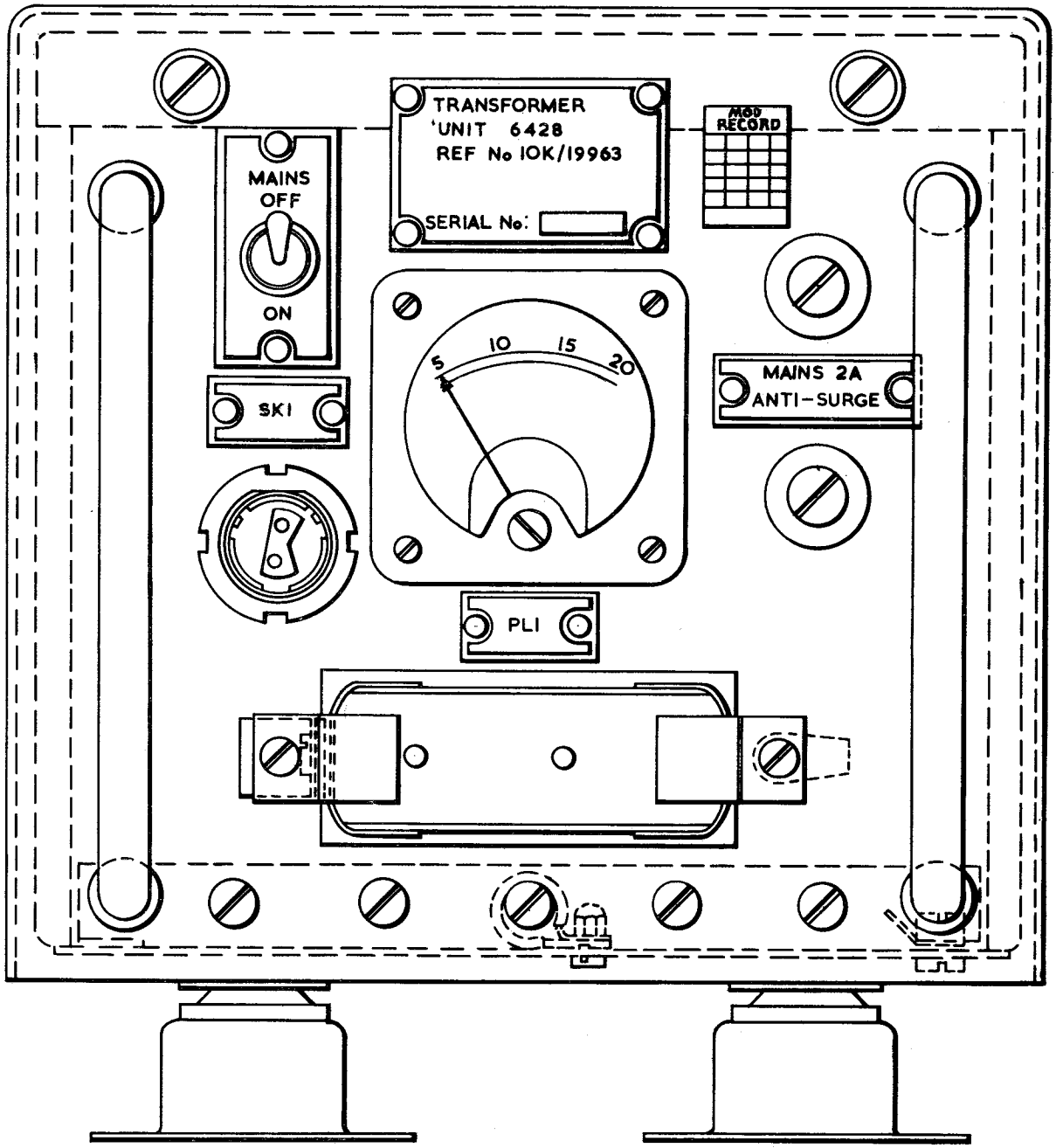

Fig. 10. Transformer unit 6428

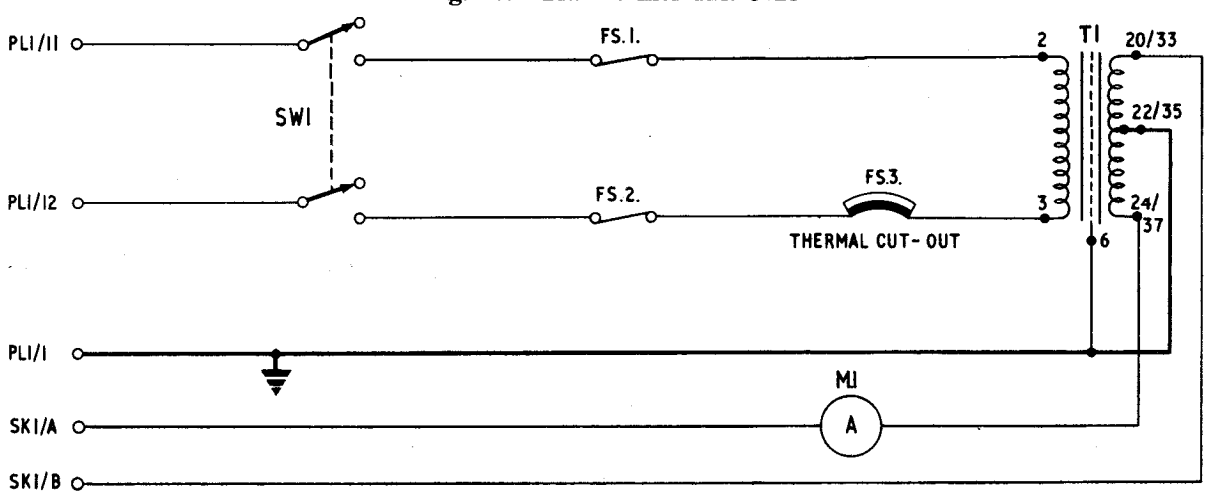

Fig. 11. Transformer unit 6428 : circuit

Chapter 8

STANDBY FACILITIES

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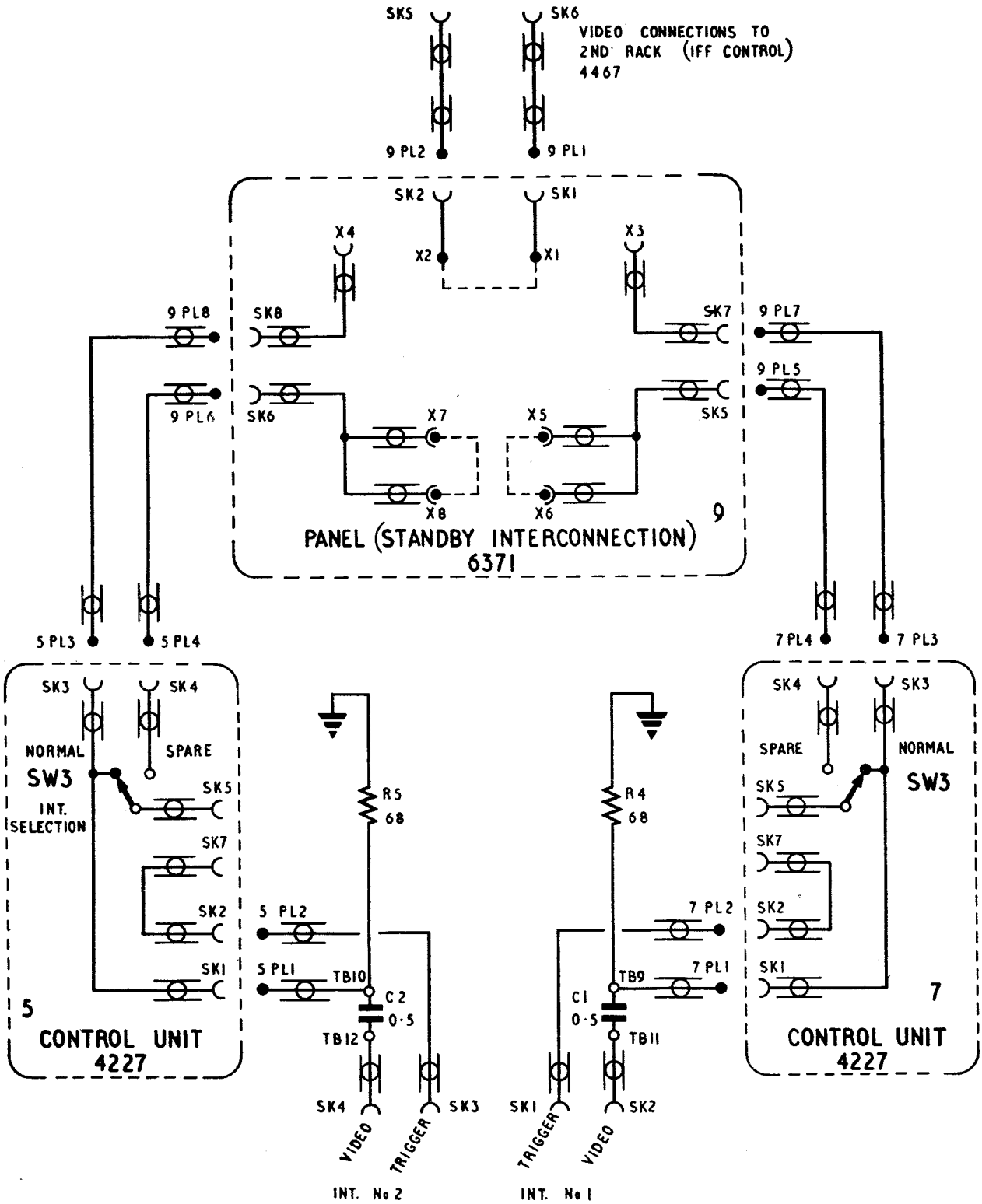

Fig. 1 Standby interconnection system

General

1. Provision is made for the inclusion in IFF Mk. 10 installations of an extensive range of standby facilities. The range is greater than is normally needed but ensures the maximum flexibility in the system. Such facilities are, in general, limited to multi-channel installations and are not provided on sites with only one interrogator.

2. It should be noted that the use of the term 'standby' in IFF Mk. 10 does not imply idle equipment which may be brought into service when required but means that any video channel may derive its information from any interrogator. This point is more fully explained in para. 6.

Standby units

3. The units which afford the standby facilities are the panel (standby interconnection) 6371 and control units 4227 in rack (IFF control) 4467. A circuit diagram of the system is given in fig. 1.

4. Panel (standby interconnection) 6371 consists of a blank panel at the rear of which are sub-panels carrying six coaxial sockets and eight single-pole sockets. Jumper leads terminated with plugs are provided so that the single-pole sockets may be connected together in any desired manner. In fig. 1 the leads are shown in the stowage positions.

5. Consider the case of a site with two radar heads and interrogators. Video information from interrogator No. 1 is fed into the control rack at SK2 and thence to SK1 on control unit 4227 (unit 7). It is then routed via the INTERROGATOR SELECTION switch SW3 out through SK5 to the channel 1 waveform generator 6010 (unit 6). The same video is also fed through SK3 on the control unit to the standby interconnection panel. Similarly, video from interrogator No. 2 is fed into the other control unit (unit 5) and then to both the channel 2 waveform generator and the standby interconnection panel.

6. Provided the appropriate connections are made on the standby interconnection panel, i.e. X3 to X7 and X4 to X5, then video from interrogator No. 1 will appear at SK4 on the channel 2 control unit 4227 (unit 5) and video from interrogator No. 2 will be available at SK4 on the channel 1 control unit (unit 7). Assume now that for some reason channel 1 fails. It is only necessary to move the INTERROGATOR SELECTION switch on the channel 1 control unit 4227 (unit 7) from NORMAL to SPARE and the displays associated with channel 1 will then receive video information from interrogator No. 2. Similarly, if channel 2 fails, operation of the corresponding switch on unit 5 makes channel 1 video available to the channel 2 displays. Thus, each interrogator becomes a standby for the other since, although both are normally operative, the failure of either does not mean that the associated displays must cease to function.

7. For the standby system to be effective it is important that both heads are synchronized in p.r.f. and rotation and this point must be borne in mind when making the standby connections.

8. The foregoing description is based on the assumption of equipment failure but the standby facilities are not designed to meet this contingency only. For example, operational requirements may demand the ability to supply video to all the displays from one head only for a period and this is achieved by the same standby connections and switching operations. In addition, it may be desirable to regard one specific head as the standby in which case only one pair of connections would be made on the standby interconnection panel (X3 to X7, or X4 to X5) depending upon which head is to be the standby.

9. In the case of a site with three radar heads and interrogators two racks (IFF control) 4467 are fitted and the channel 3 waveform generator is housed in the second rack together with a control unit 4227 and a standby interconnection panel. The two standby interconnection panels are linked by cables between the two racks as shown in fig. 1. The connections from the bottom of one control rack to the next are provided as part of the installation.

10. By suitably disposing the jumper leads on both standby interconnection panels, any one of the three interrogators can be used as a standby for the other two. Also, if the standby interrogator fails, either of the remaining two can be arranged to serve as the standby or each can be made a standby for the other.

Power unit 4465

11. Although it is normally referred to as a spare unit and is described as such in Chapter 1, the additional power unit provided in rack (IFF control) 4467 may be regarded as part of the standby facilities since it is ready at all times to supply either waveform generator in the event of failure of one of the other two power units.

12. If one of the two operational power units fails, the corresponding failure lamp at the top of rack (IFF control) 4467 is extinguished enabling ready identification of the faulty unit ; the switching sequence which brings the spare unit into service is fully automatic (*Chap.* 1, *para.* 22). To remove the faulty unit for servicing, it is only necessary to move the appropriate switch on panel (metering) 4466 from NORMAL to REMOVE. When a serviceable unit is fitted into the rack the switch must be returned to NORMAL to ensure correct operation of the automatic switching system in the event of a subsequent failure.

Waveform generator 6010

13. The spare waveform generator (unit 10), which may sometimes be found at the top of rack (IFF control) 4467, does not in any way form part of the standby facilities. The provision of the stowage space at the top of the rack is purely a convenience for the accommodation of a spare serviceable waveform generator if available.

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Chapter 9

TYPICAL INSTALLATIONS

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LIST OF ILLUSTRATIONS

Scope of chapter

1. The purpose of this chapter is to provide some information of a general character showing how the IFF Mk. 10 system is used in conjunction with various primary radar installations. Since the operational requirements and facilities desired may vary widely at different sites, it is neither practicable nor desirable to give detailed descriptions of all the possible installations in this publication. In the light of experience and with changing requirements, details of specific installations might rapidly become out-of-date without the basic equipment being affected.

2. The information contained herein is intended to serve only as a guide to the layout of IFF Mk. 10 installations and to assist in determining the scale of equipment necessary to meet any particular requirement. For full details of individual installations the relevant publications covering the primary search radars should be consulted.

3. The installations are described under three broad headings: sites with only one interrogator, sites with two or more interrogators, and sites with which a remote head is associated. Installations may vary in detail but, in general, will fall into one of these categories.

Installations with one interrogator

4. A site with one radar head and one interrogator forms the simplest Mk. 10 installation and would probably provide the minimum facilities. Fig. 1 is a diagrammatic representation of such an installation. The primary radar is assumed to be a Type 80 in which the RF head consists of an aerial array and a cabin mounted on a turntable. Pending the availability of aerial array X4239 the American aerial system AS295 is fitted just below the lower lip of the Type 80 reflector assembly.

5. The IFF Mk. 10 interrogator, in a rack (IFF equipment) 6374, is housed in the cabin with the Type 80 RF equipment, the necessary connections to the radar office being made through the main slip ring unit located in the modulator building. Certain of the interrogator functions may be remotely controlled from the radar office (*Chap.* 1, *para.* 8).

6. The radar office equipment consists of a single rack (IFF control) 4467 and a relay rack. Since only one channel is employed, the minimum number of units is required in the control rack so that one waveform generator, its associated control unit and the standby interconnection panel are replaced by stowage panels (*Chap.* 1, *para.* 14). Two power units are fitted, the space for the third being left empty.

7. The number of relay units 6009 required i governed by the number of display consoles on which it is desired to present IFF information. For the purpose of housing the relay units a rack (relay unit) 4494 is fitted in the radar office adjacent to the control rack. Rack 4494 has a maximum capacity of 16 relay units (*Chap.* 5) providing video information to, and switching facilities for, 32 consoles but does not necessarily carry a full complement of units; only sufficient relay units to meet the station requirements, i.e., one for every two consoles, are normally installed.

8. The main interconnections of the IFF Mk. 10 installation are shown in fig. 1. It should be noted that the minimum facilities provided in the IFF equipment are not limited to the requirements of the simple installation described. Even though use is not made in such an installation of all the facilities available, their provision makes possible rapid expansion of the system when desired.

Installations with two or more interrogators

9. Fig. 2 illustrates the layout at a site with two radar heads, a Type 80 and a Type 7/Type 79. The installation of the IFF interrogator in the Type 80 head is similar to that described in para. 4 and 5 but the Type 79 installation employs a rack (IFF equipment) 4464 (*Sect.* 1, *Chap.* 2). Also, in this case, the normal IFF aerial is aerial system AS295 which is mounted on the roof of the cabin by means of a frame, mounting (upper), 6437 clamped with kit (lower aerial mounting) 6811. The Type 79 head is provided solely for the purpose of accommodating the IFF installation and is maintained locked in azimuth with the associated Type 7 radar head.

10. The radar office equipment differs principally in quantity from that employed at a site with only one interrogator. For two interrogators one rack (IFF control) 4467 with a full complement of units is required. The number of relay units is again determined by the number of displays on the site and if this does not exceed 32 a single rack (relay unit) 4494 will suffice. Where there are more than 32 displays a second rack 4494 fitted with the necessary additional units is required. In the event of the installation including more than one relay rack an impedance matching unit 12114 must be fitted at the bottom of rack (IFF control) 4467 to provide an adequately low video output impedance.

11. The layout at a site with more than two interrogators would be a duplication of fig. 2 up to and including rack (IFF control) 4467. Where the number of interrogators exceeds two a second control rack is required and the double-sided rack (relay unit) 4495 must be used in place of relay rack 4494. Rack 4495 can accommodate up to 32 relay units to provide video information and switching facilities for 32 displays from four interrogators.

Installations with remote radar

12. On those sites which include a remotely sited radar, e.g., Type 7/Type 79 installations, an additional Mk. 10 IFF installation is provided at the remote site synchronized in azimuth with the radar. The layout in such an installation is illustrated in fig. 3.

13. The remote IFF installation is similar to that at the main site but, since only the minimum facilities are required, consists simply of an interrogator and a single control rack fitted with one waveform generator and two power units. The modes selected by all operators using the remote Type 7 and IFF Mk. 10 are interlaced in the normal manner but separation of the video responses into the three channels corresponding to modes 1, 2 and 3 is not necessary at the remote site. In addition, no relay units are necessary.

14. The video responses, together with the synchronizing waveform, are fed to a mixer amplifier 3719 to which is also applied the radar IF and the composite signal is conveyed to the main site via a cable link. Here the signal is applied to a separator amplifier 3720, where the IFF video and synchronizing waveform are extracted, and then passed to a second waveform generator 6010, which distributes the video responses into the three channels. The remote and local waveform generators are synchronized in operation so that the responses to a particular interrogation are routed to the correct channel.

15. To prevent possible interference in airborne transponders between the isynchronous interrogations from the main and remote sites, it may be necessary to switch the interrogators at the two sites so that, on alternate rotations of the main site radar head, IFF interrogations can be made from each site in turn. The most convenient method of achieving this is to switch the 50V DC supply to the IFF control racks for which purpose selector unit 4535 forms part of the main site installation as shown in fig. 3.

16. The auto-align cam in the magslip resolver rack operates a stepping switch in the selector unit in such a manner that the 50V DC supply is switched to the particular waveform generator required, i.e., when interrogations are made from the main site, both waveform generators associated with the remote interrogator are inoperative while, when the remote interrogator is used, the 50V supply to the main site waveform generator is switched off. In addition to the cyclic switching a manual control on the selector unit enables either interrogator to be selected at will to operate continuously or for both interrogators to operate simultaneously if conditions permit.

17. The exact method of using this switching arrangement must be determined by the requirements at each individual site but the following points should be noted. If the remote and main site heads are interrogating simultaneously it is probable that at some point during their rotation they will be on the same heading in which case an airborne transponder within range will receive both interrogations. Since the remote interrogator must be triggered early due to the time delay in the cable link, the transponder will reply to this interrogation first and the response will be received direct at both sites. The resultant effect on the display, due to the direct signal at the main site, is that the response appears at a shorter range by up to three or four miles depending upon the spatial separation of the two sites and the azimuth bearing of the aircraft.

18. Interference between the two interrogators is not likely to be serious for aircraft at ranges greater than approximately 50 miles but, at shorter ranges, the question of alternate or simultaneous interrogation depends upon whether half the data rate free from interference or the full data rate with possible interference is the more tolerable condition.

19. It should be noted that fig. 3 shows only the interconnections associated with the remote radar head and should be studied in conjunction with fig. 1 or 2 to obtain a clearer picture of the complete site layout.

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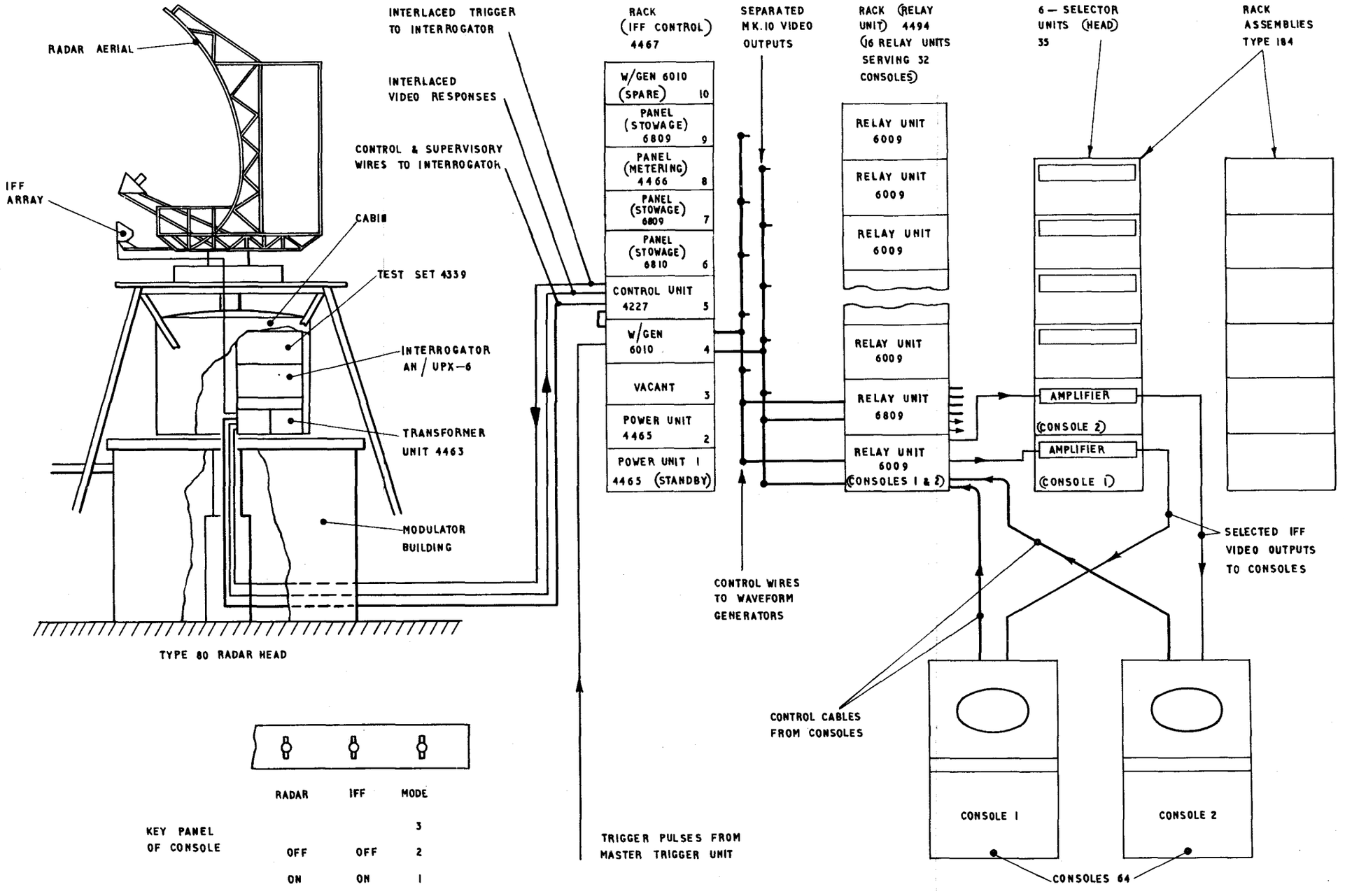

Fig. 1 Installation with one interrogator

Fig. 1
(A.L. 16 Oct. 58)

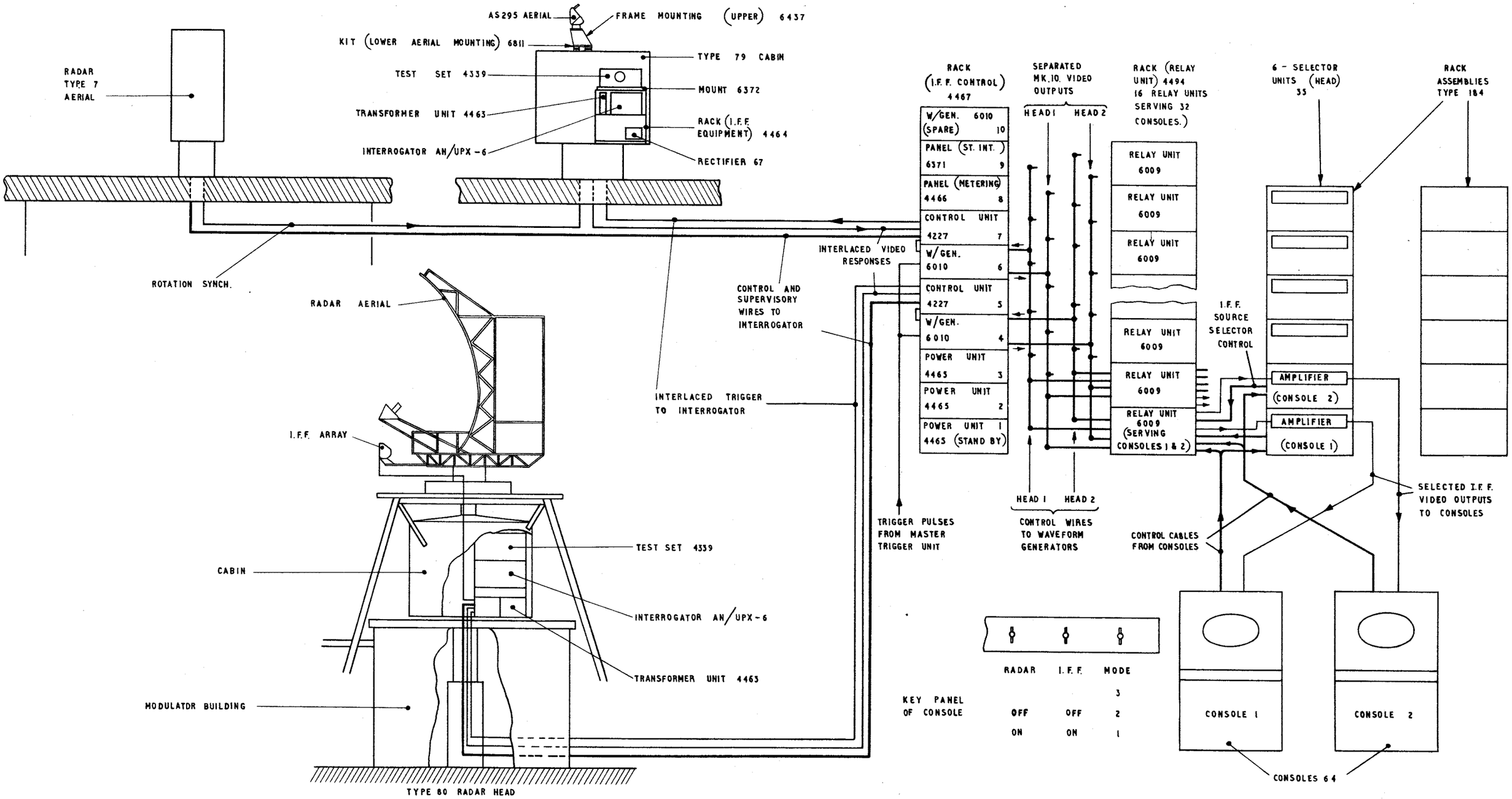

Fig. 2.

Installation with two interrogators.

Fig. 2.
(A.L.7 July '57)

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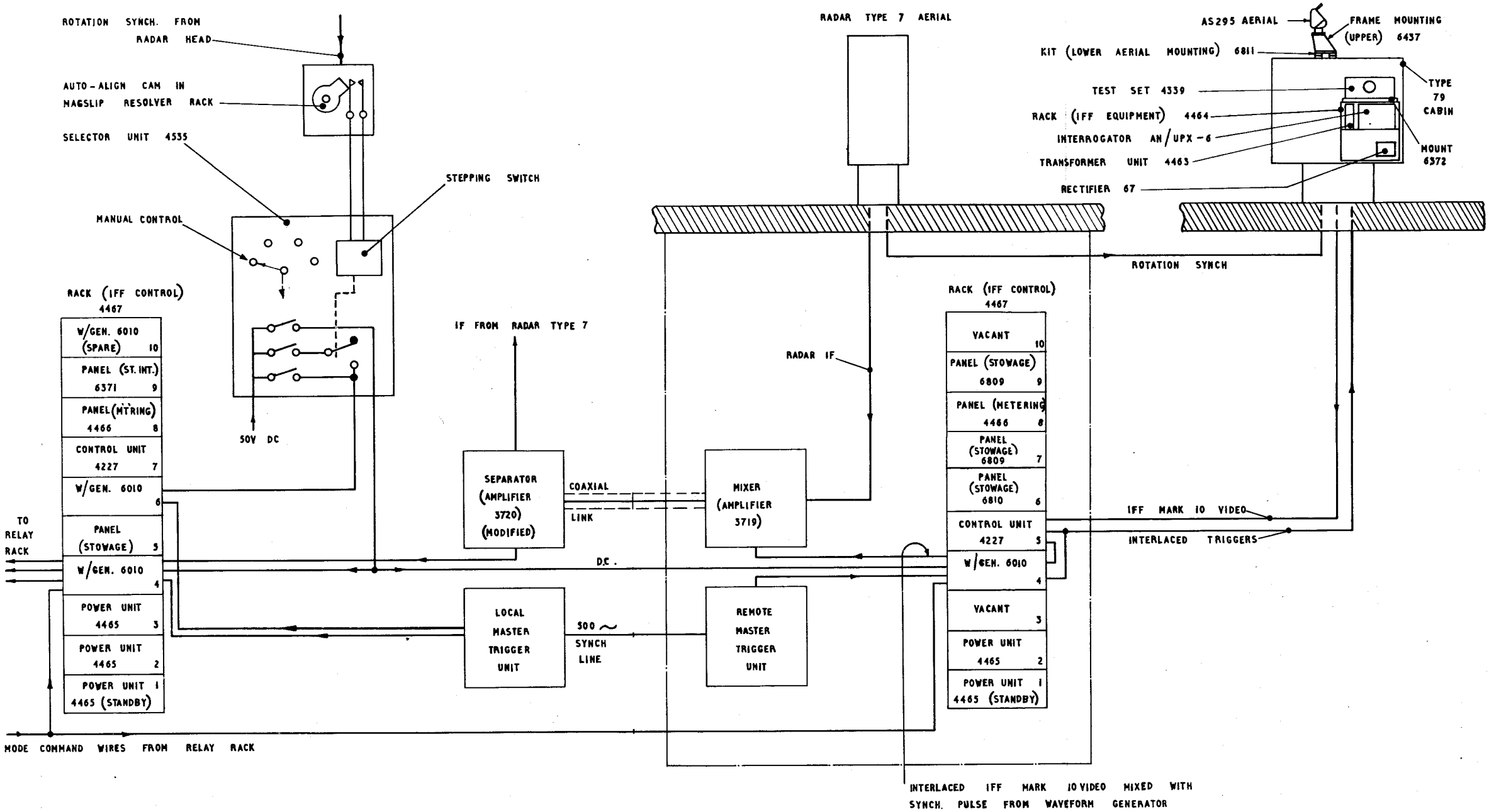

Fig. 3. Installation with remote type 7. Fig. 3.
(A.L.16, Oct. '58)

Chapter 10

DIVIDER, FREQUENCY AND POWER UNIT M2

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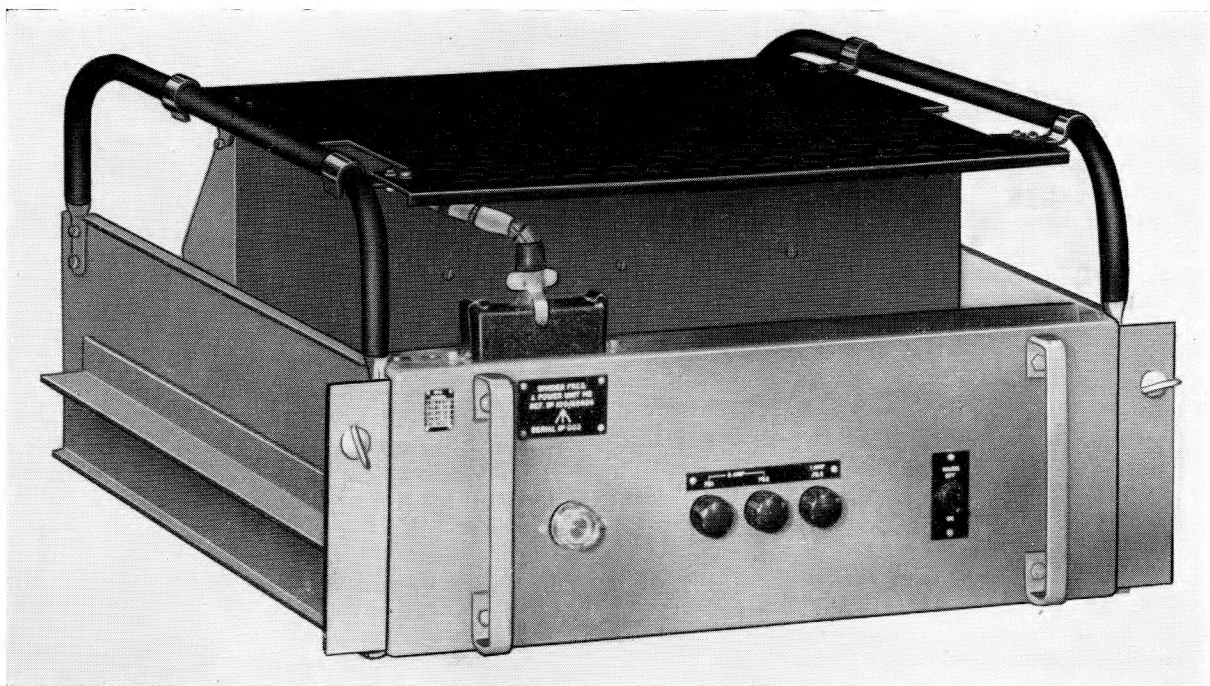

Fig. 1. Frequency divider and power unit M2: front view

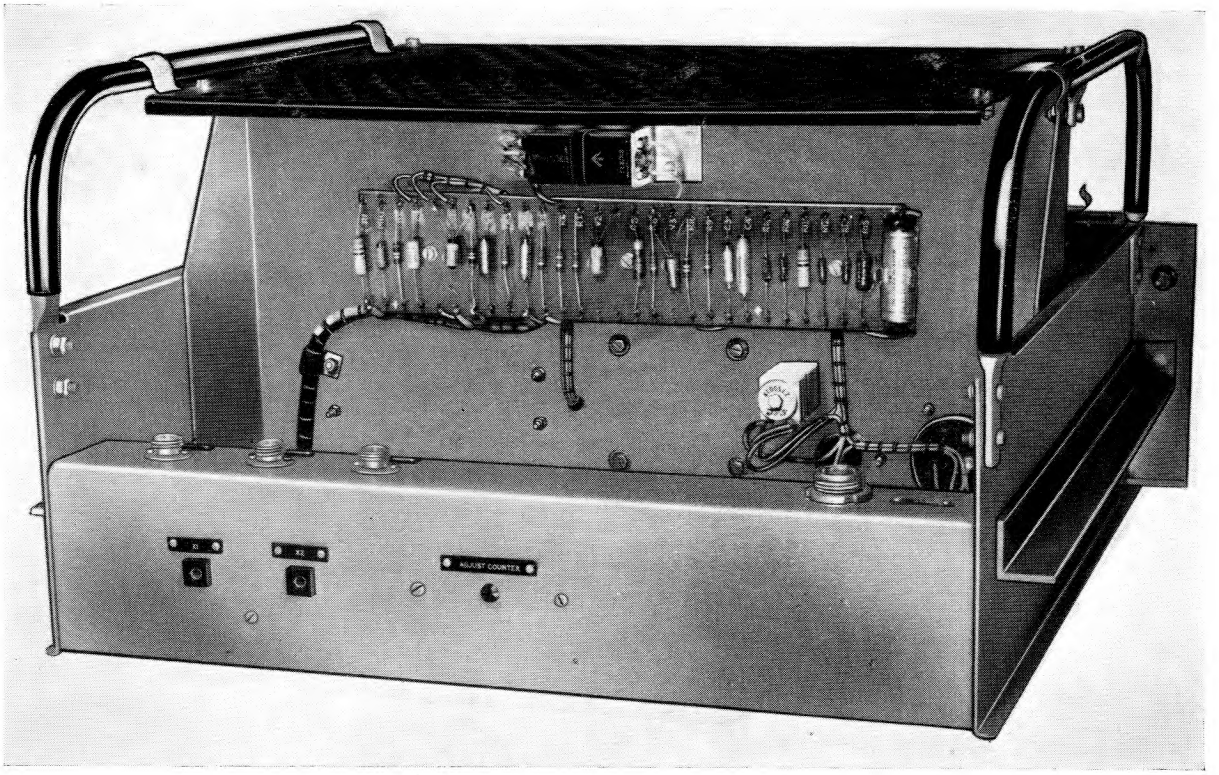

Fig. 2. Frequency divider and power unit M2: rear view

General

1. The station p.r.f. at the majority of radar sites is a nominal 250 p.p.s. and the IFF Mk. 10 equipment described in this publication has been designed to operate at that recurrence frequency. However, at some sites only a 500 p.p.s. recurrence frequency may be available with the result that difficulty may be experienced, particularly with test set 4339. To overcome this, a frequency divider unit is available which, when interposed between the master trigger unit and the IFF Mk. 10 equipment, furnishes a p.r.f. of 250 p.p.s. The unit also provides a 50V d.c. supply which can be used to meet the requirements of the IFF equipment independently of the station 50V supply.

Construction

2. Frequency divider and power unit M2, illustrated in fig. 1 and 2, is very similar to power unit 4465 and consists of a box-section sheet steel framework with tubular steel frames at the top of the side members to facilitate handling. It is mechanically inter-changeable with the power unit so that, when required, it can be installed in rack (IFF control) 4467 in position 2 and supplied by the mains power connector available in this position.

CIRCUIT DESCRIPTION

Frequency divider

3. The master trigger pulse from the MTU is fed in at SKA (fig. 3) and then to the anode of a diode MR1 whose cathode is returned, via the primary of pulse transformer T2, to the +10V line. The bias ensures that the divider does not respond to transient pulses picked up on the inter-cabling. Transistor V1 is connected in a blocking oscillator circuit with feedback between base and collector. The base is taken to −5V at the junction of R3 and R4 and the emitter is connected to earth through the timing network consisting of R5, RV1 and C2. V1 is thus bottomed and both plates of C2 are at earth potential.

4. A positive-going MTU pulse applied at SKA will cause MR1 to conduct and V1 is rapidly cut off by the normal blocking oscillator action. The collector falls from earth to −10V and C2 is charged. At the end of the pulse C2 commences to discharge through R5 and RV1. The reset time of the circuit is determined by the time constant C2, R5, RV1 and the preset is normally adjusted so that the circuit responds to alternate MTU pulses.

5. When V1 is cut off, a voltage pulse is developed across the third secondary winding on T2 and is applied to the base of an emitter follower V2. V2 base and emitter are both at approximately earth potential so that the transistor is conducting but the emitter of the output stage V3 is returned to about −0·02V at the junction of R9, R10 and this transistor is cut off.

6. The application of a positive voltage pulse to the base of V2 cuts off that transistor and the collector falls to −10V, causing V3 base to fall below earth. V3 thereupon conducts and the collector rises to earth with the result that a positive voltage pulse is developed across the collector load R8. This pulse is fed via C8 to SKC and thence to the IFF equipment.

Power supplies

7. The 50V supply and that for the frequency divider are derived from a single transformer T1. The 230V 50 c/s single-phase mains input is fed in on pins PLA/11 and 12 and then, via a double-pole switch and protective fuses FS1, FS2, to the primary winding. A neon lamp LP1 affords an indication that the unit is switched on.

8. One secondary winding on T1 delivers 82V r.m.s. to a bridge rectifier MR2, the d.c. output from which, after smoothing by the resistance-capacitance filter C7, R15, C6, is developed across the potential divider network R11, R12, R13, R14 and R16. The required outputs of +10V, −10V and −25V are taken from tappings on this network.

9. The other secondary winding on T1 delivers 55V r.m.s. to another bridge rectifier MR3. No smoothing is provided for this supply and the output is taken direct to a 2-pole socket SKD via a fuse FS3. The maximum loading of the 50V supply for the output voltage to remain within the limits of 40V to 60V is 150mA.

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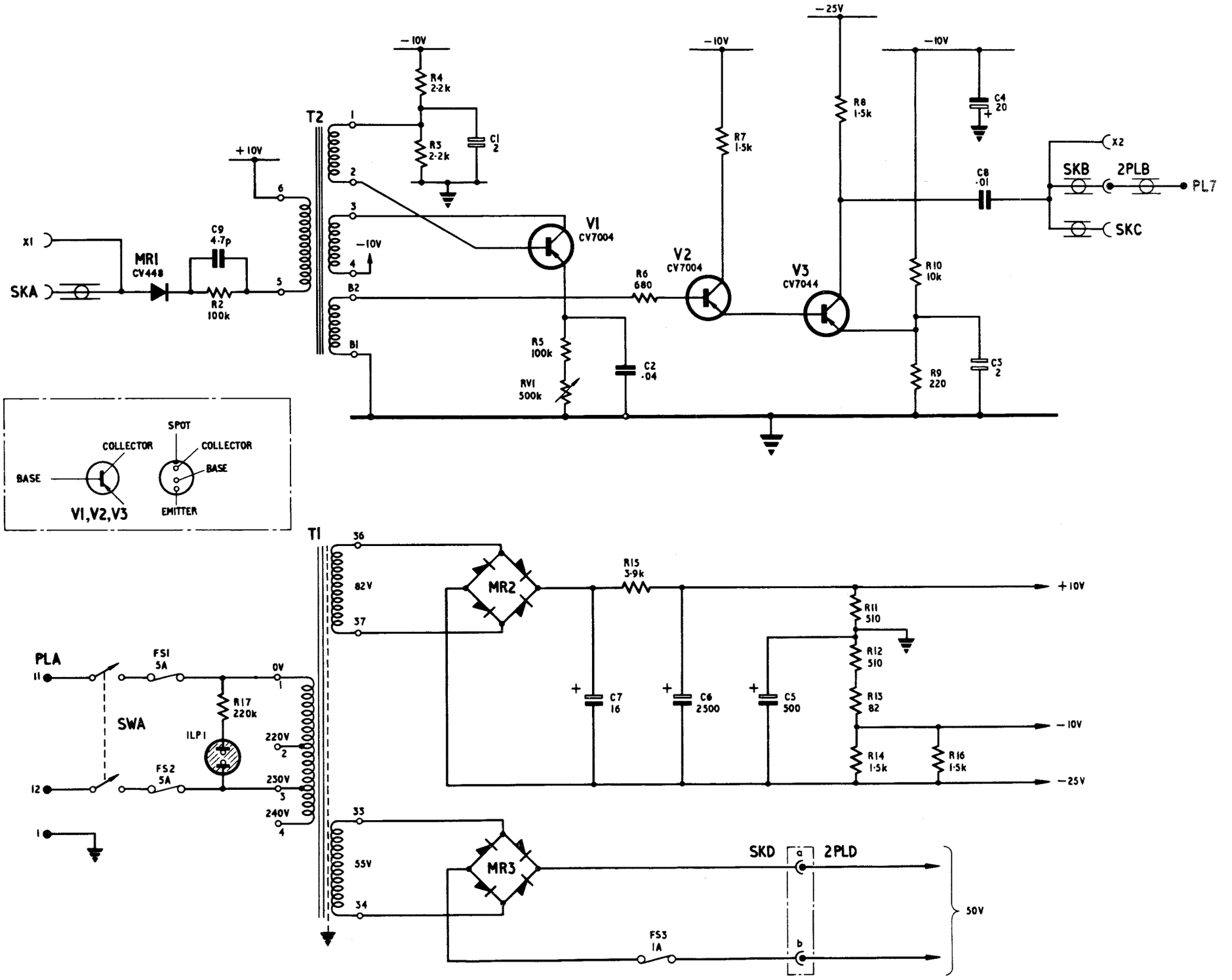

Fig. 3 Frequency divider and power unit M2 : circuit Fig. 3

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SECTION 3

MOBILE APPLICATION (RVT 511)

Chapter 1.— GENERAL DESCRIPTION OF RVT 511

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Fig. 1. RVT 511 : front nearside view

Introduction

1. Radio vehicle Type 511 Mk. 1, general views of which are shown in fig. 1 and 2, is a prime-mover vehicle consisting of an Austin 1 ton 4×4 chassis on which is mounted a standard "E" type body Mk. 3. It is used in conjunction with a radio vehicle Type 510 as a mobile IFF Mk. 10 installation.

2. The body of the vehicle houses the mobile equivalent of the radar office equipment mounted in a rack (IFF control) 4470. No air conditioning plant is fitted but provision is made for circulating air over the equipment when in use. Similarly, no heating is provided for the cabin but a radiator heater is available to keep the equipment dry and serviceable under storage conditions.

3. Entry to the interior of the body is through double doors at the rear of the vehicle, accessible by detachable steps. These steps may also be fixed to the near-side front so that the junction panel can be easily reached when connecting up the convoy cables. Ventilation of the cabin interior is afforded by adjustable louvred apertures in the walls.

4. At the front near-side of the vehicle is an aperture with a weatherproof cover immediately behind which is the cable junction panel. Although this panel is part of rack 4470 and is mounted thereon, it serves as the vehicle termination panel to which are connected all the cables linking the RVT 511 to the other vehicles in a convoy. The weatherproof cover consists of a rectangular plate hinged at the top end and two collapsible side members. When erected it forms a triangular box open at the lower end. The cover plate can be raised well clear of the side members and held in position with stays to facilitate connecting up the cables.

5. The interior of the vehicle, showing the layout of the equipment, is illustrated in fig. 3. All items of equipment, not normally removable, are secured through the wall panelling to jury strutting carried on the vehicle main members. It is not necessary to disturb this strutting when replacing defective items of equipment.

6. External communication is provided by means of a Type L telephone mounted on the off-side wall of the cabin below the window and connecting the RVT 511 with its associated RVT 510

Fig. 2. RVT 511 : rear nearside view

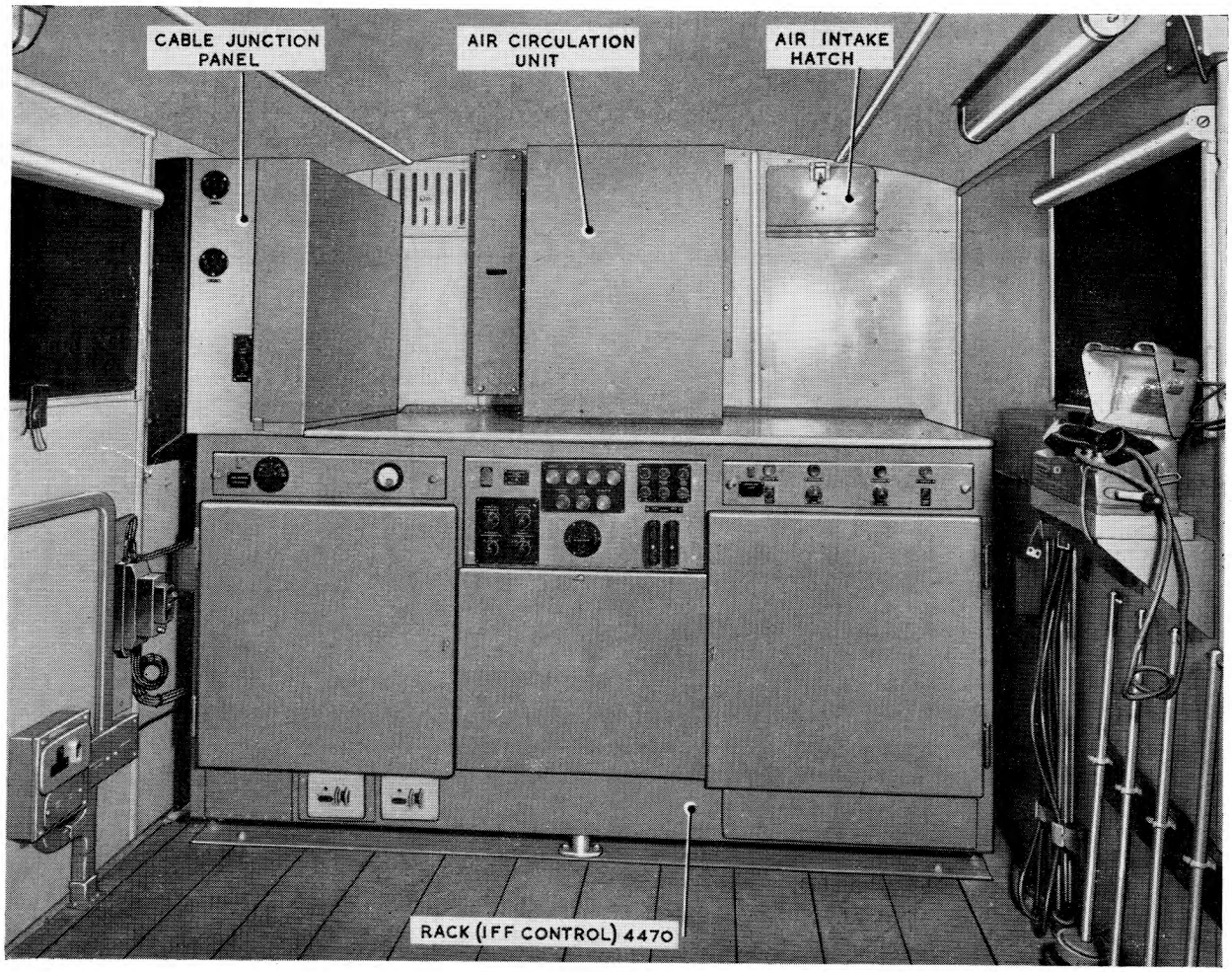

Fig. 3. View of cabin interior

(via the telephone socket on indicator, electrical, 4533 in the latter vehicle). It should be noted, however, that in operational use the RVT 511 is not normally manned and the equipment, when once switched on, is remotely controlled from the RVT 510.

Rack (IFF control) 4470

7. This rack, which is described in Chapter 2, contains the IFF Mk. 10 equipment and is mounted at the front end of the cabin. It is secured to the floor and the front wall. On top of the rack are the cable junction panel and the air circulating unit for the equipment.

Vehicle lighting

8. Both 230 V and low-voltage lighting circuits are provided in the cabin. Under normal operational conditions the 230 V circuit is used with the low voltage system providing an emergency circuit only. The 230 V lighting circuit consists of two daylight fluorescent tubes fitted to the ceiling on either side of the cabin. Spare tubes are stowed at the front of the cabin. Power for the low voltage circuit is derived from the vehicle starter battery which supplies two 12 V 30 W lamps located above the entrance doors.

9. The two lighting circuits are controlled by a single three-position switch at the right-hand side of the entrance doors. The switch assembly includes an emergency push-button which, when depressed, causes a red lamp on the instrument panel in the driving cab to light. Its purpose is to enable a passenger (should one be carried in the cabin whilst the vehicle is moving) to communicate with the driver. The lighting control switch is over-ridden by an interlock switch operated by the right-hand door. When the door is opened the main and emergency lights are automatically switched off.

10. Windows in each side wall and in the doors permit the entry of daylight. All the windows are provided with roller blinds so that the cabin may be effectively blacked out if required.

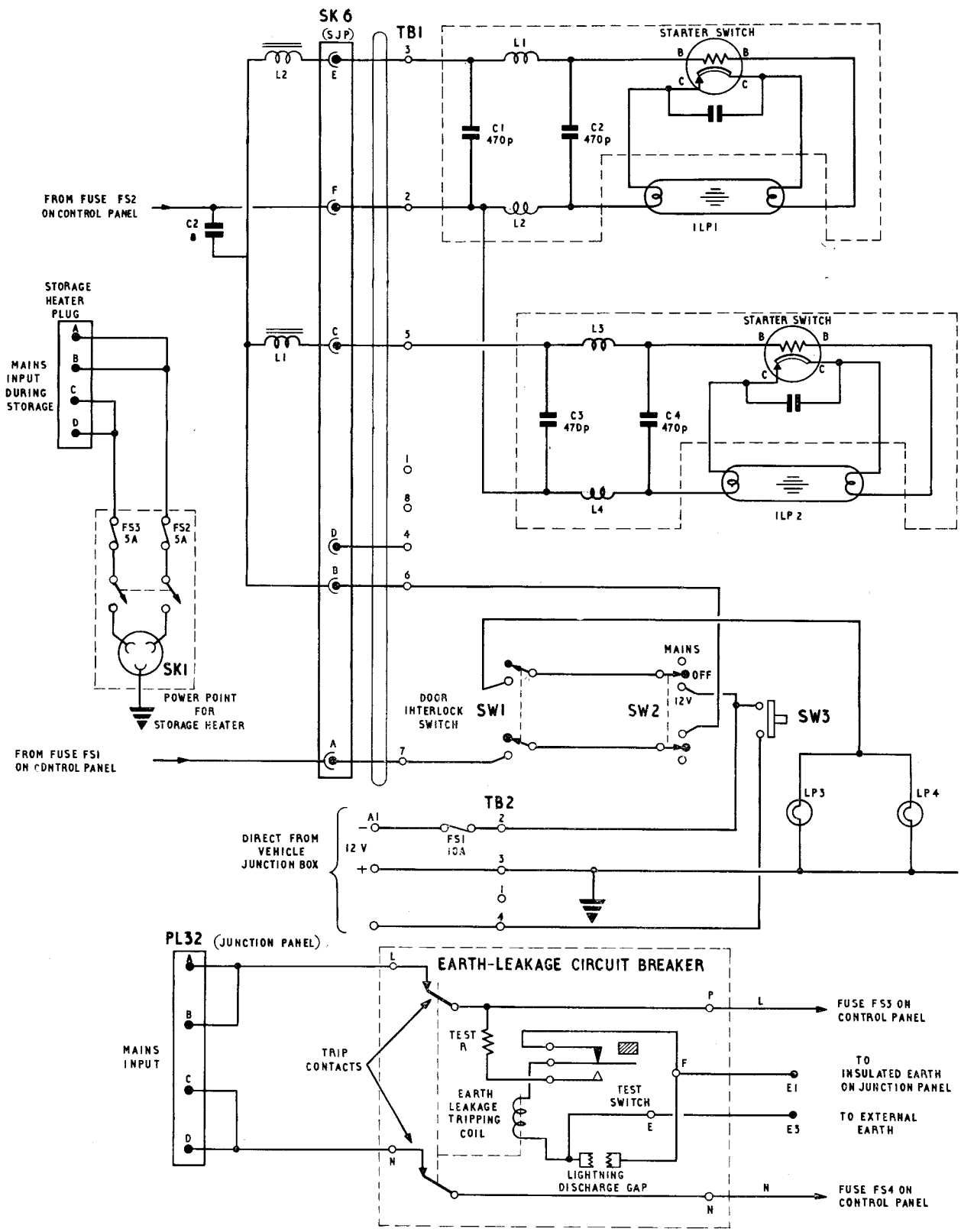

Fig. 4. Vehicle wiring diagram

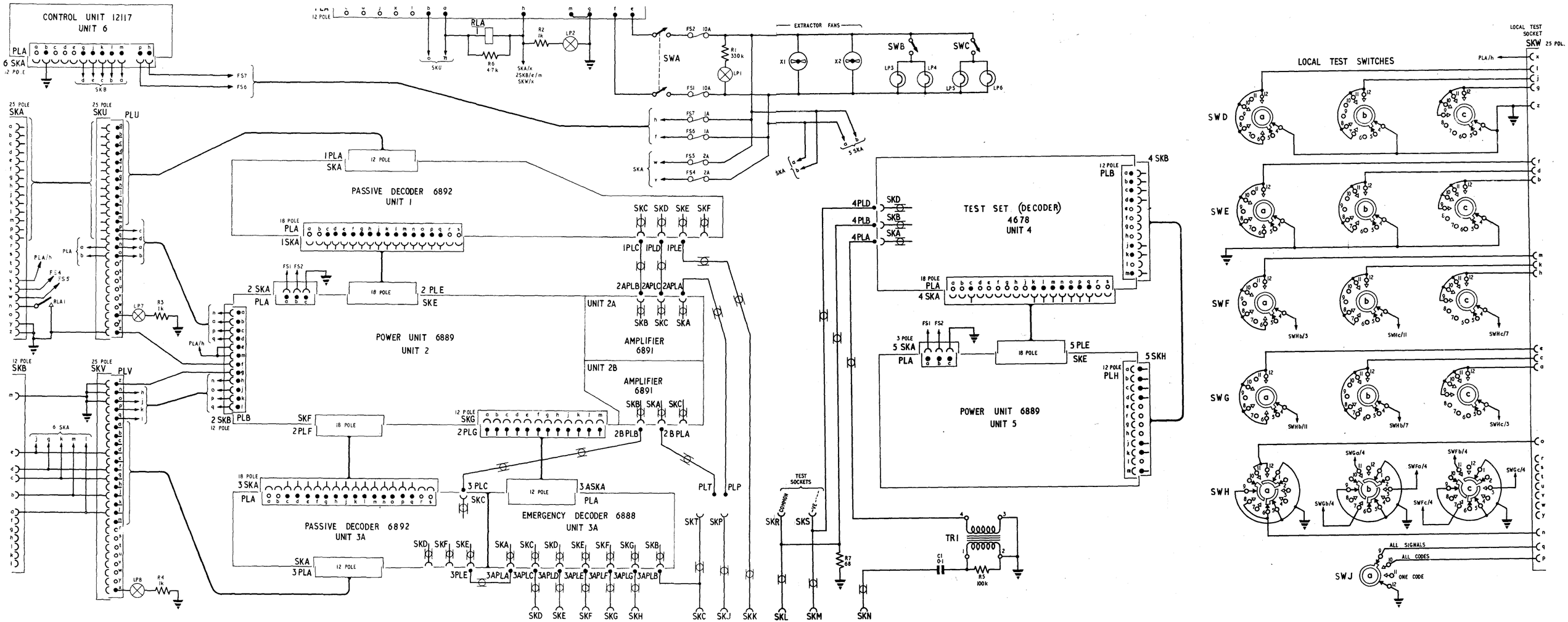

Fig. 5

Rack (decoder RH) 12807 : circuit

Fig.5

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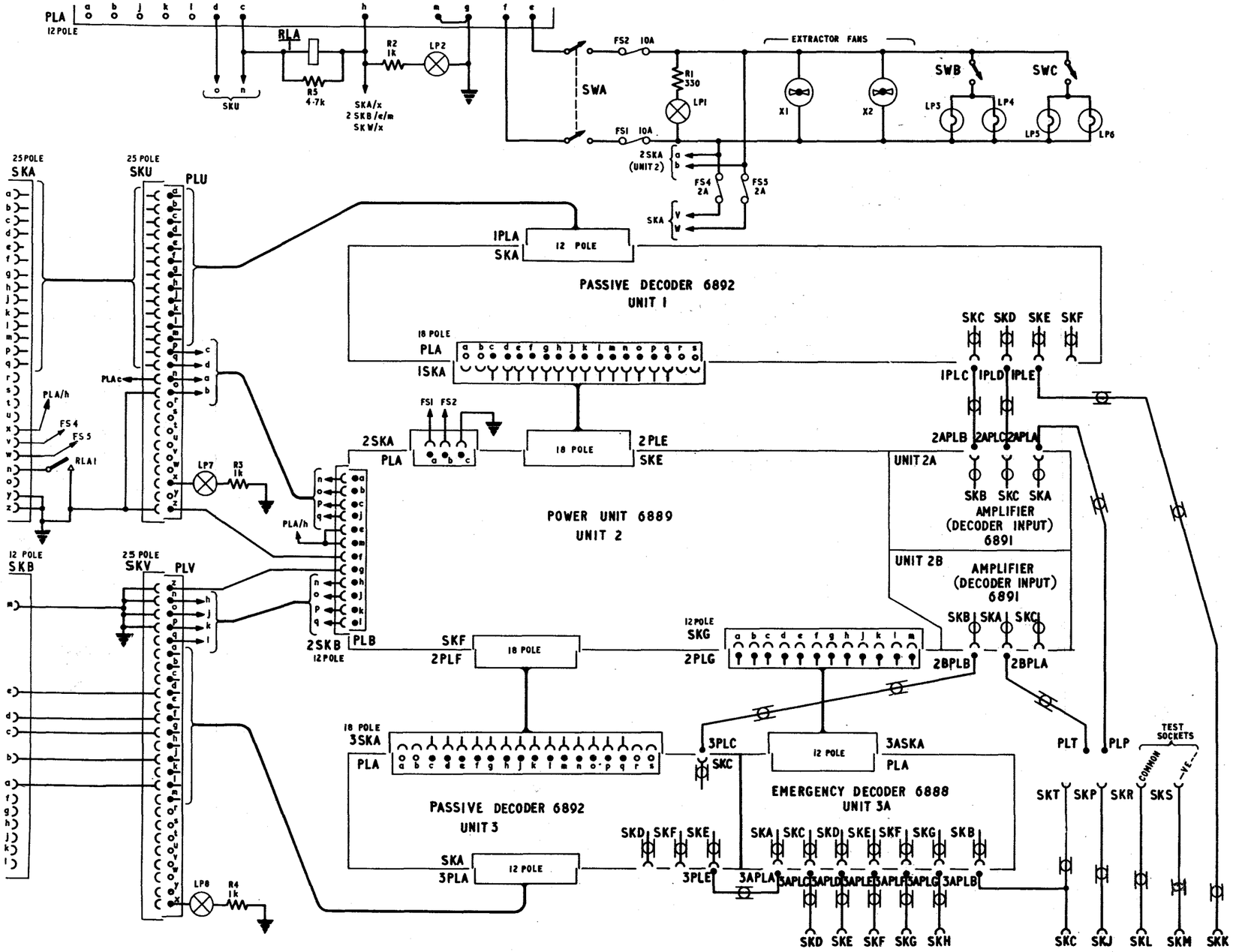

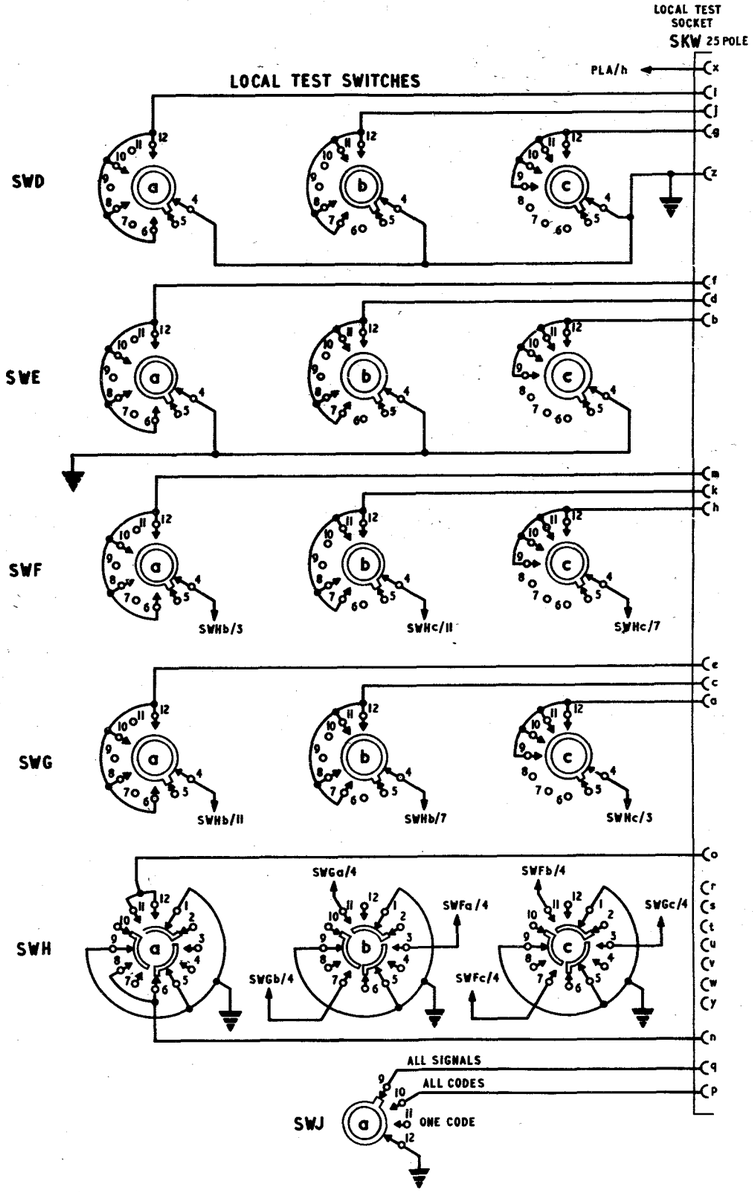

Fig. 6

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Rack (decoder LH) 12808: circuit

Fig 6

Chapter 2 — RACK (IFF CONTROL) 4470

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General

1. Rack (IFF control) 4470, which is mounted in radio vehicle Type 511 Mk. 1, serves the same main purpose as rack (IFF control) 4467 in the radar office in that it houses those units of the IFF Mk.10 installation associated with the production of the mode trigger pulses, viz. waveform generators 6010 and their power supplies. Control and metering panels are also included. However, since the display facilities in a mobile installation are, of necessity, limited, there are no relay racks and the functions of the control rack are extended

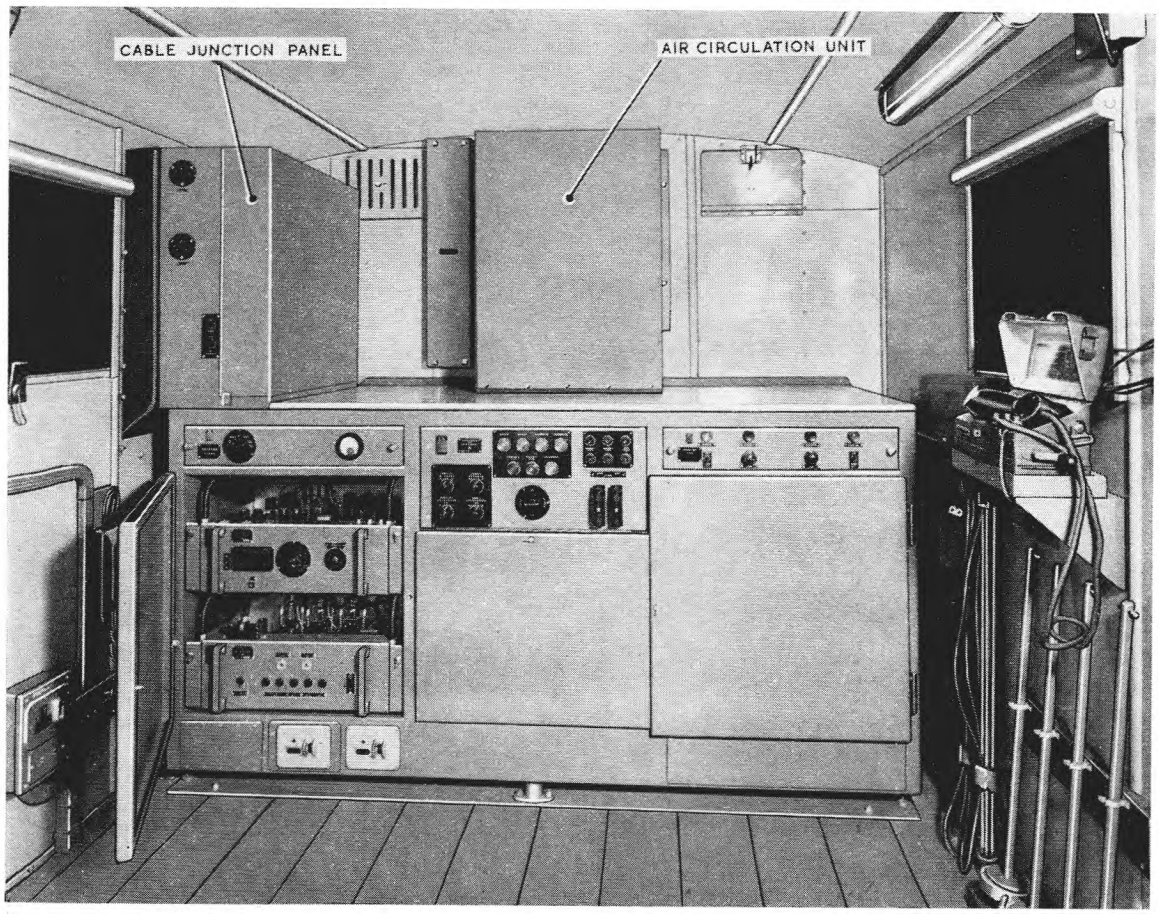

Fig. 1. General view of rack (IFF control) 4470

by the incorporation of a relay unit 6009 to provide the mode and video switching.

2. Each rack is designed to contain a maximum of seven units and can serve two interrogators. It is divided into three compartments disposed horizontally with the units mounted in the following order: —

Compartment	*Unit No.*	
Left hand	1	Panel (metering) 4466A
	2	Waveform generator 6010
	3	Power unit 4465
Right hand	4	Control unit 6373
	5	Waveform generator 6010
	6	Power unit 4465
Centre	7	Relay unit 6009

The panel above the centre compartment is part of the rack and carries the a.c. input switch, most of the indicating lamps and the waveform generator video output and control line switches. The space below the relay unit is used to provide stowage for the storage heater and its stand and also houses five servicing connectors as well as other spares.

Description

3. Rack (IFF control) 4470, illustrated in fig. 1 and 2, is a steel cabinet measuring approximately 66 in. long × 34 in. high × 28 in. deep. At the left-hand end the height is increased to 57 in. by the cable junction panel which, with its cover, is 10in. wide and extends the full depth of the rack. The control and metering panels are mounted along the top front of the rack and are normally accessible but the remaining units are concealed behind three detachable doors. For ease of servicing the waveform generators are mounted in a manner similar to that employed in rack 4467, *i.e.* they can be withdrawn and pivoted about their centres.

4. The centre panel carries the a.c. circuit fuses, controls associated with the 230 V distribution and the waveform generator connections and a number of indicator lamps. A wiring diagram of rack 4470 is given in fig. 8. The 230 V supply is fed through 25A fuses at the lower right of the panel and then through 5A fuses direct to the cabin lighting circuit. The equipment supply is also protected by 3A fuses but is routed through the rotary switch below the indicator lamps. During operation, air is circulated over the rack units and provision is made for this air to be heated when it is required to dry out the equipment after periods of storage (*para.* 15). The switch permits either the air heater or the equipment to be supplied with 230 V but not both together, thus avoiding the possibility of overheating.

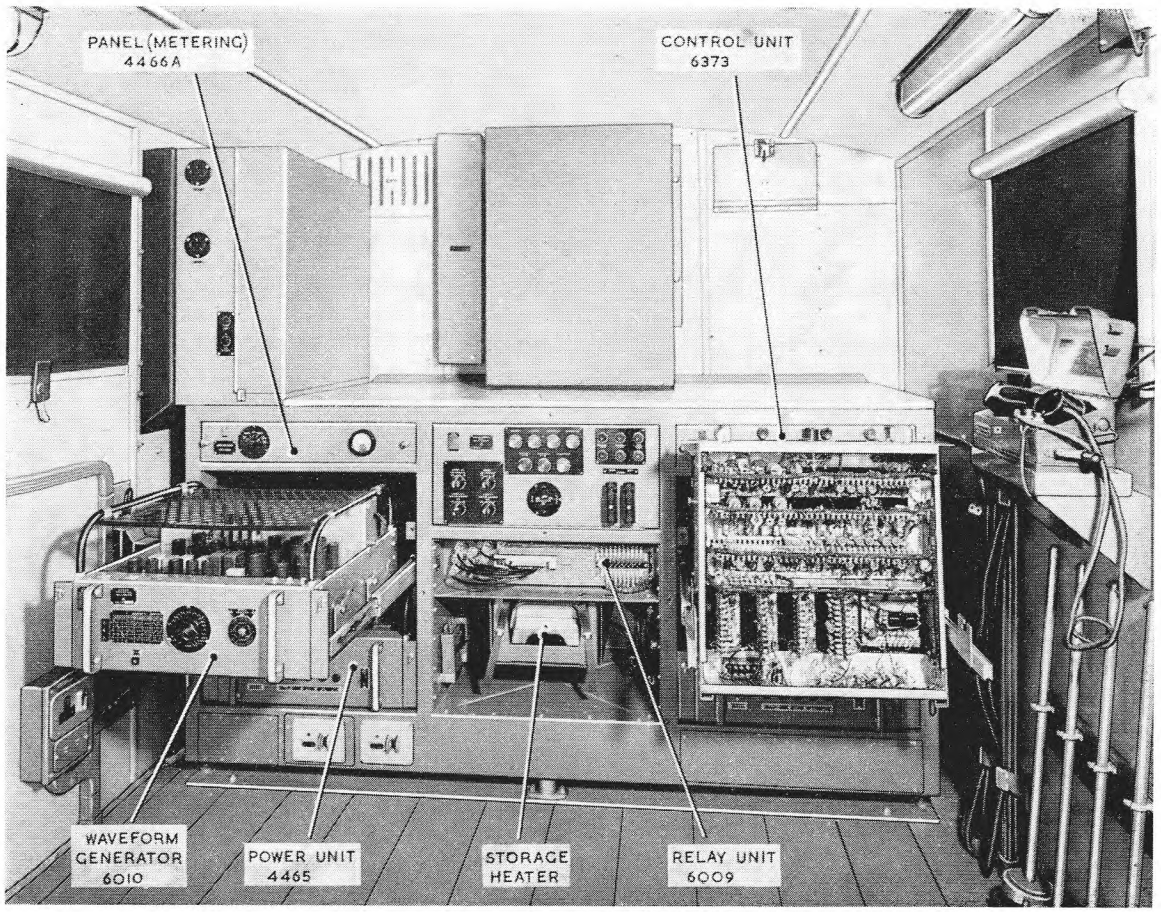

Fig. 2. View of rack with doors removed

5. The indicator lamps, seven in number, show which circuits are live. Those in the top row are associated with the a.c. input supply. LP1 lights immediately the 230V supply to the vehicle is switched on and LP2 shows when the air heater is on. With the rotary switch set to EQUIPMENT, LP2 is extinguished and LP3 lights to indicate that the 230V supply is fed to the power units and waveform generators. LP4 is connected across the a.c. supply to SK13 on the sub-junction panel to serve as an indicator when additional equipment is installed in the cabin. Of the three lamps in the bottom row, LP5 and LP6 are connected to the indicator lamp circuits of power units 4465. When a power unit is switched on, and is delivering h.t. the appropriate lamp will light. The remaining lamp indicates the presence of the 50V supply. This supply is derived from the RVT510 but is separately controlled within the RVT511 by a switch mounted on the cable junction panel.

6. The four switches grouped together at the left-hand side of the panel are controls for the waveform generator video outputs and mode command line connections. The operation of the IFF Mk. 10 equipment in the RVT511 is dependent upon the type of convoy and this, in turn, determines the number of vehicles employed. There is no fixed number and a convoy may contain one, two or three vehicles Type 511. In consequence, two switches are provided to enable the appropriate load terminations to be selected according to the type of convoy of which the vehicle forms a part. The other two switches permit the waveform generator video outputs and mode command connections to be switched in or out as required. Here again, the settings used are dependent upon the type of convoy. More information on the use of these switches is given in Chapter 3.

7. Mounted behind the centre control panel is a sub-junction panel carrying 23 coaxial, one 2-pole, one 6-pole and two 12-pole sockets. The 2-pole and 6-pole sockets provide the connections for the telephone and cabin lighting circuit respectively. The two 12-pole sockets, and certain coaxial sockets, are included for use when additional equipment is installed in the vehicle.

Fig. 3. Cable junction panel

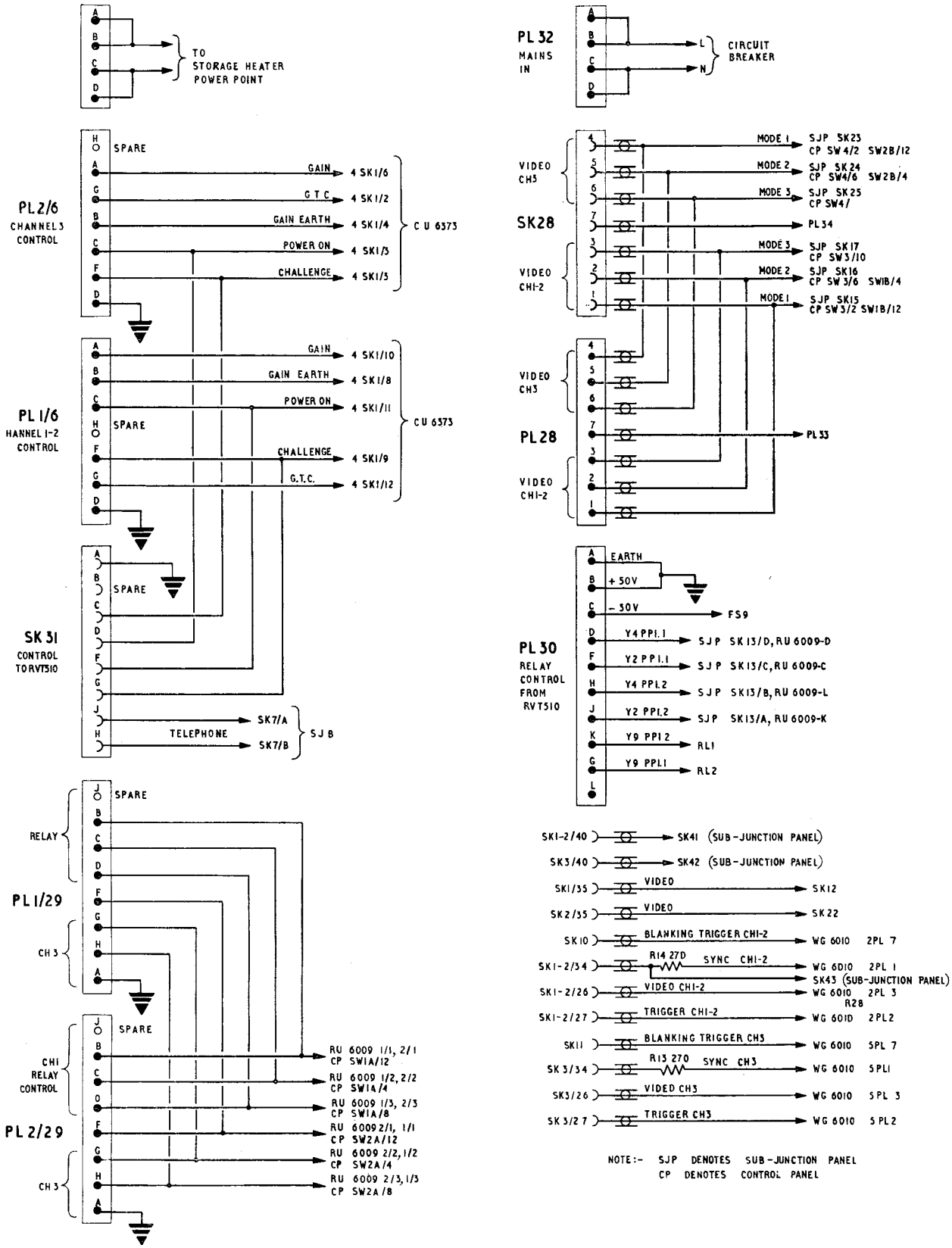

Fig. 4. Circuit diagram of cable junction panel

8. At the bottom of the rack are two 3-pole 5A switched a.c. outlets. They are provided to supply test gear and/or soldering irons when servicing the rack equipment. Although the illustrations show these sockets mounted together below the left-hand compartment they will, on production units, be separated, one being mounted below each end compartment.

Rack units

General

9. Waveform generator 6010, power unit 4465 and relay unit 6009 have already been described in Chapters 2, 3 and 4 of Section 2. The remaining units housed in rack (IFF control) 4470 are modified versions of those used in rack 4467 and are described in the following paragraphs.

Panel (metering) 4466A

10. The metering panel in rack 4470 fulfils only the main function of measuring the power unit voltages and the waveform generator valve currents. There is no spare power unit and hence no automatic switching circuit in the mobile installation. Panel 4466A thus carries only a meter and selector switch.

Control unit 6373

11. This unit provides facilities similar to those of control unit 4227 but contains two channels so that only one unit is required for the two waveform generators. The panel carries the following controls and indicators: —

Two GAIN potentiometers.

Two GTC LONG/SHORT switches.

Two CHALLENGE lamps.

Two POWER ON lamps.

Remote control facilities for the two associated interrogators are thus available. Since, however, there are no standby arrangements in the mobile installation, there is no interrogator selection switch. In addition, the video and mode trigger lines from and to the interrogators are not routed

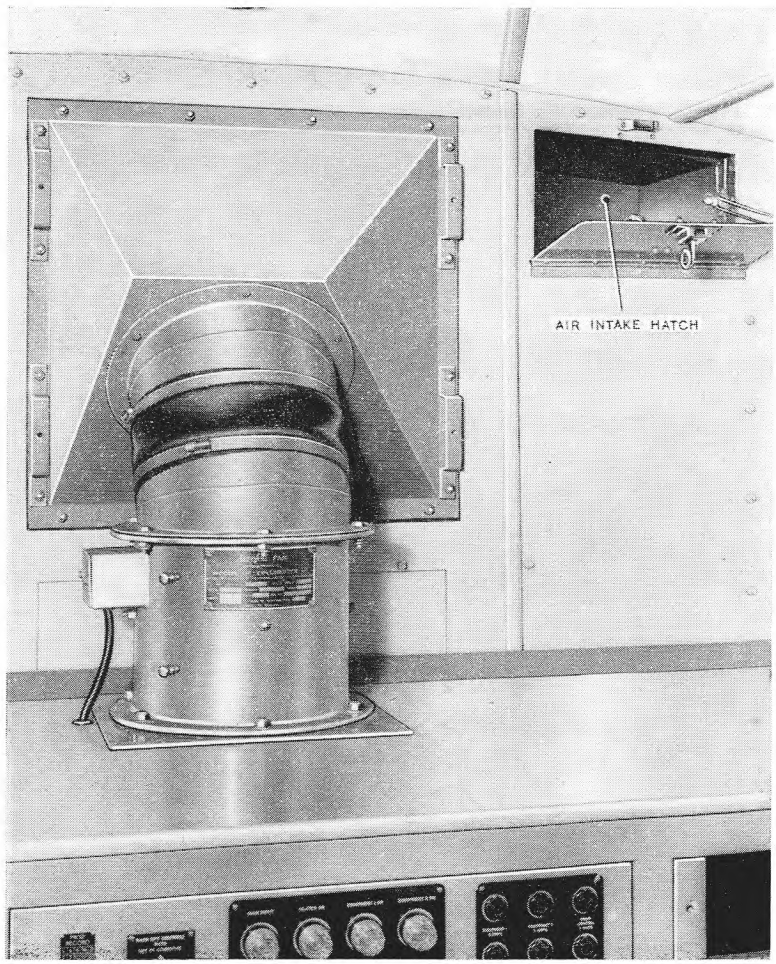

Fig. 5. Air intake assembly

through the control unit but run direct from the waveform generators to the cable junction panel.

Cable junction panel

12. Input and output connections for the complete rack are made through coaxial sockets and multi-pole plugs and sockets on a cable junction panel mounted on the top of the rack at the left-hand side in such a manner that it is accessible through the wall of the cabin. This panel forms part of rack 4470 but also serves as the vehicle connector panel. It is corrugated in construction with the plugs and sockets mounted on the downward facing corrugations to prevent the entry of water (*fig.* 3). A circuit diagram is given in fig. 4. In addition to the rack connections, two 3-pole 230 V a.c. outlets are provided on the side of the panel together with a 3A fuse and switch for the 50V supply. Fuses, rated at 1A, are also provided in the 50V supply to the left and right decoders.

Air circulation system

13. Air is circulated over the units through ducting incorporated in the rack. The entry is at the top centre of the rack through a section of cylindrical trunking, the upper end of which is coupled to a box on the front wall. A fan is housed in this trunking. The system may operate in one of two ways. A continuous flow of air from outside the vehicle can be drawn in through a filter and, after passing over the equipment, exhausted into the cabin. Alternatively, the external inlet can be closed to make the system re-circulative, *i.e.* the air within the cabin is circulated over the equipment.

14. Control of the air circulation is effected through a hatch in the front wall to the right of the intake trunking (*fig.* 5). When this hatch is closed, the external aperture is open and the fan draws in air from outside the vehicle. By opening the hatch cover the external aperture is closed; air from inside the cabin is then drawn into the trunking and circulated through the rack.

15. To enable the equipment to be dried out quickly after a period of storage, an 800 W heater is mounted in the intake trunking. It is controlled by the rotary switch on the centre control panel and when the switch is set to HEATER the equipment cannot be switched on. To ensure that the air temperature cannot continue to rise and become too high, a thermostat is incorporated in the heater circuit. It should be noted that although the heater is separately controlled, the air circulation system operates immediately the 230 V supply to the vehicle is switched on.

16. Provision has been made for an extension of the air circulation system, to other equipment which may be installed in the cabin, through outlets situated below the left and right-hand compartments of the rack. At present these outlets are fitted with cover plates.

Transformer assembly

17. Where a convoy contains only one RVT 511, impedance matching problems do not arise and the appropriate connections can be made direct to the waveform generators. If a convoy contains two or more vehicles Type 511, however, correct impedance matching of the interlace synchronizing circuits becomes important and, for this purpose, a transformer assembly is mounted at the base of the junction panel. It consists of two pulse transformers T1 and T2 (*fig.* 6) with the connections brought out to coaxial sockets mounted on the lid of the box. Other coaxial sockets are provided for straight-through connections and as stowage points for unused cables. The method of connecting the transformer assembly for different convoys

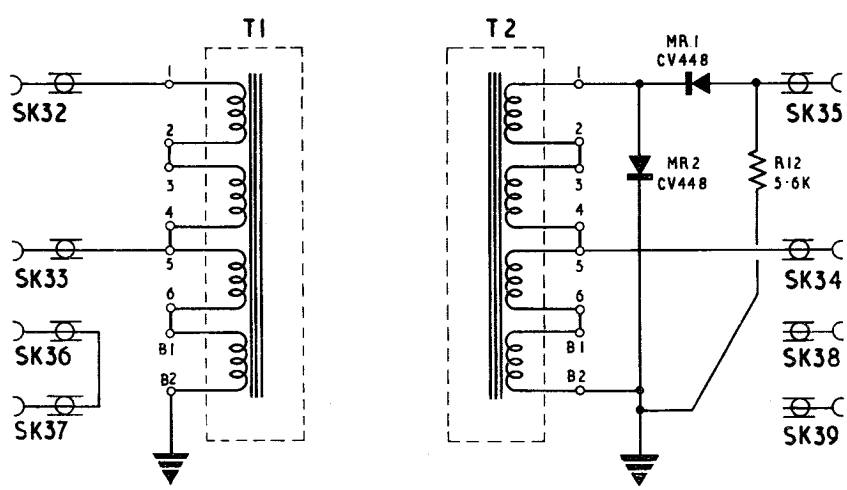

Fig. 6. Transformer assembly circuit

is clearly shown on a label attached to the junction panel cover and reproduced in fig. 7.

Servicing facilities

18. As stated in para. 8 and 12, a total of four 5 A 3-pole a.c. outlets is provided on the rack for supplying test equipment and soldering irons. In addition, the rack itself has a Formica working surface for first and second line servicing purposes. If desired, the UPX-6 interrogator can also be tested in the cabin but, to permit this, a transformer unit 4463 and suitable connecting leads must be available.

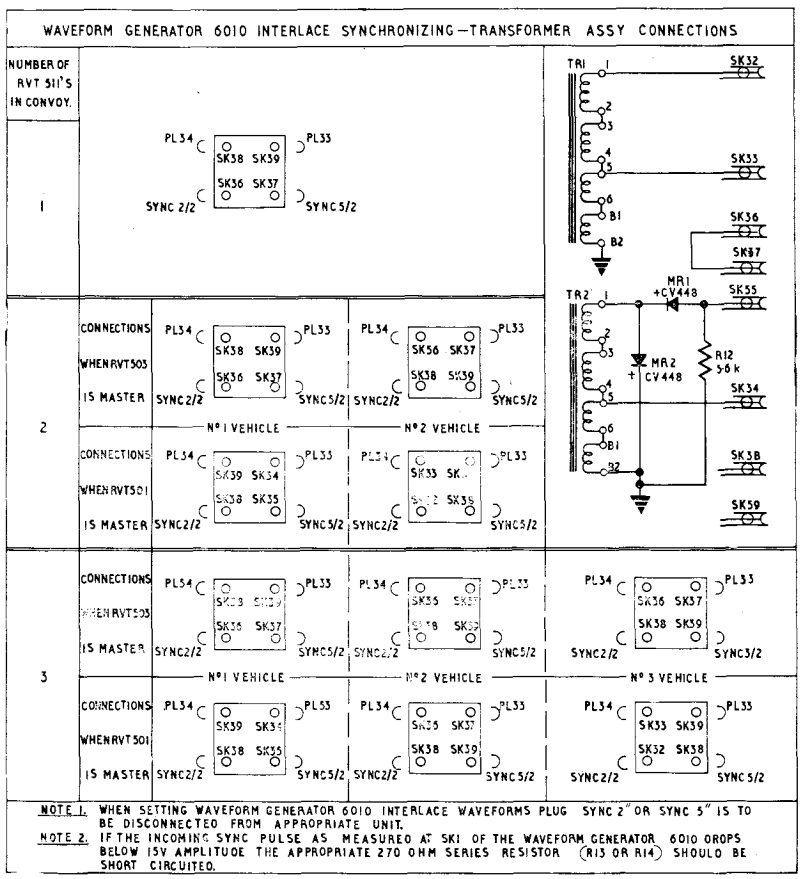

Fig. 7. Transformer assembly instruction label

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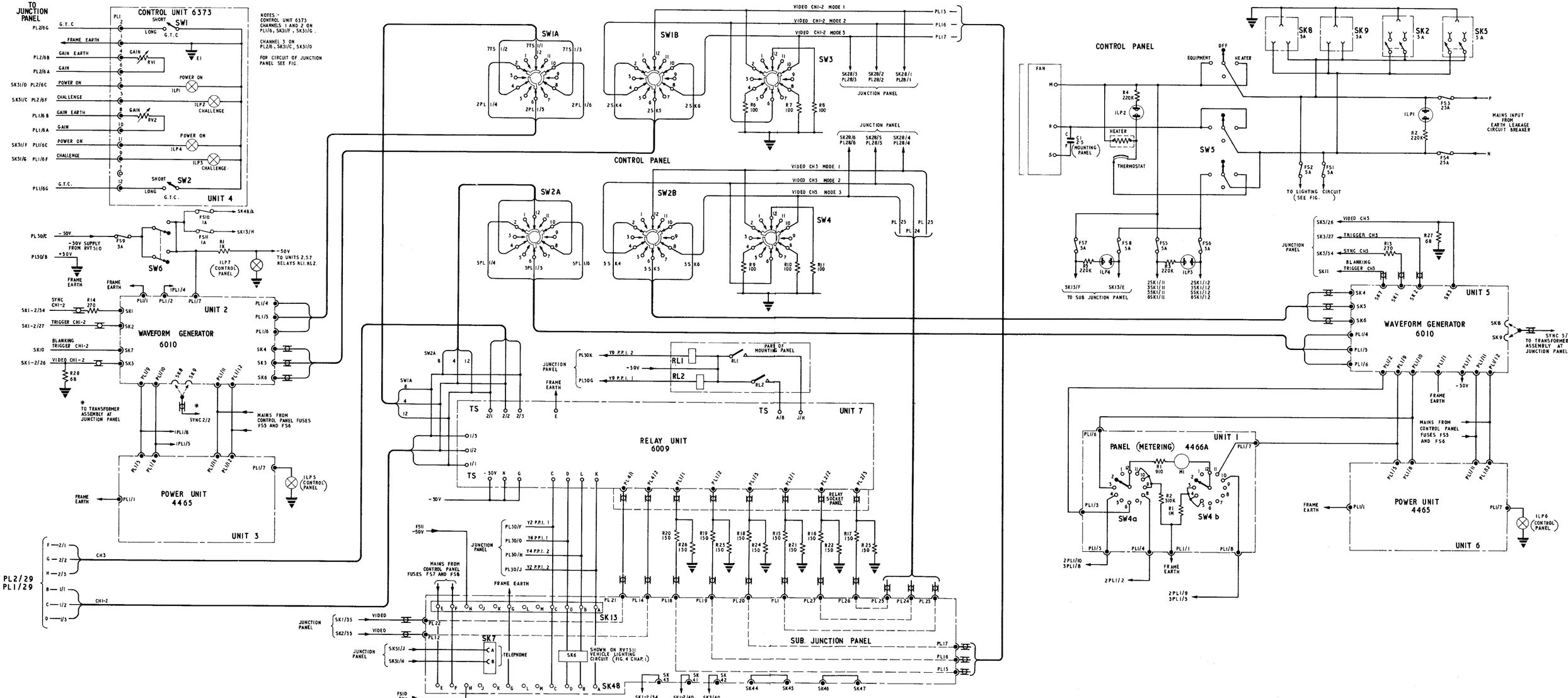

Rack (I.F.F. Control) 4470: circuit

Fig.8

Fig.8

Chapter 4
(Revised)

AERIAL ARRAYS 4992 AND 4992A

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General

1. Aerial array 4992 has been designed as an alternative to, and as a replacement for, the American IFF Mk. 10 aerial system AS295. ◀As explained in Sect. 1, Chap. 2, its initial application will be to mobile radars Type 14 and 15 but provision has been made for its eventual use on certain static radars so that it can be used, if necessary, as a direct replacement for an AS295.▶

Electrical characteristics

2. Aerial array 4992 is a vertically polarized broadside array consisting of 32 radiating elements and a feeder system. The requirements of the IFF Mk. 10 system demand as narrow a beam as is practicable in the horizontal plane and this, in aerial 4992, is 3 deg. at the half-power points. At −10dB the horizontal beam width is 6 deg.

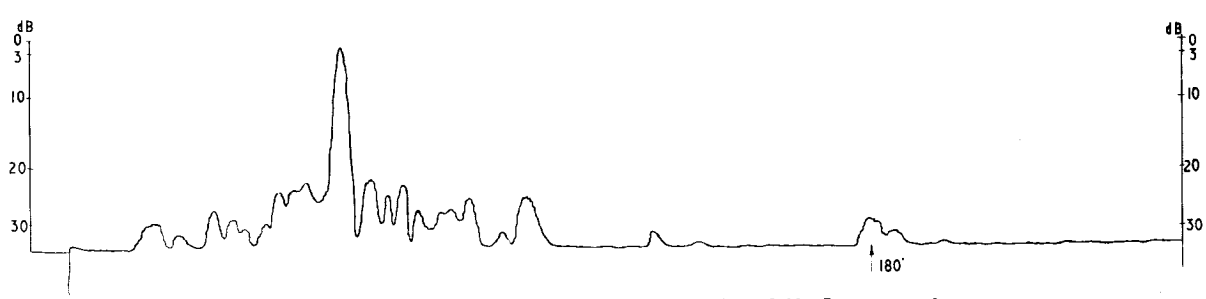

Fig. 1. Horizontal radiation pattern for 360 deg. rotation

3. In addition to a narrow beam width it is essential that any side lobes should be reduced to the minimum possible to prevent spurious responses. This is achieved by tapering the energy distribution to the radiating elements so that the magnitude of the current in the radiators at the centre of the array is greater than that in the radiators at the ends, resulting in a side lobe of the radiated energy below the horizontal plane to produce interference lobes. The precise resultant vertical coverage pattern depends considerably upon the mounting height of the aerial and the characteristics of the ground in the vicinity. In practice, the effect of the interference pattern should not be obvious. To the rear of the aerial the vertical pattern remains below ◀24dB▶ up to an elevation of 45 deg.

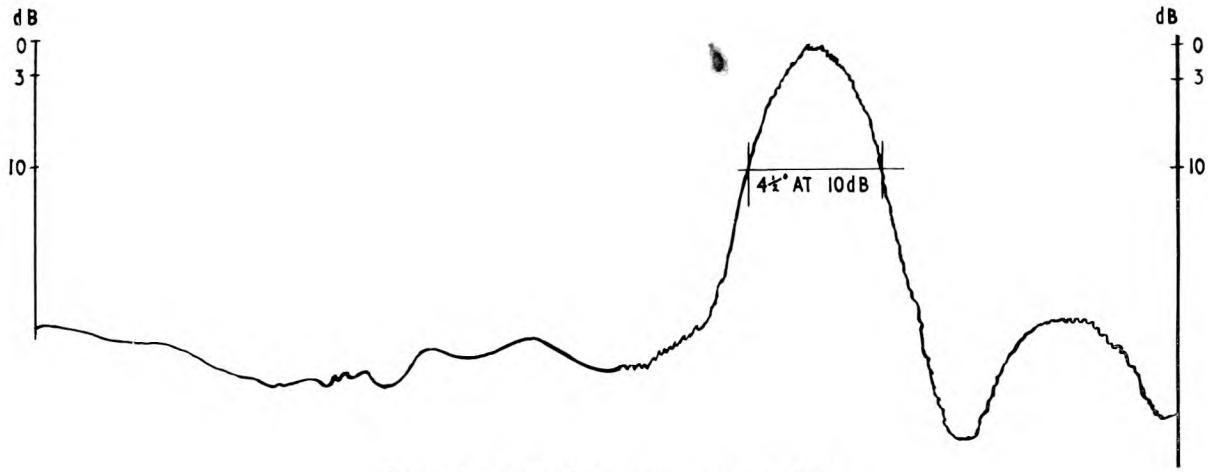

Fig. 2. Main lobe pattern expanded

level of ◀18dB▶ in relation to the main beam. The back lobe level in the horizontal plane is at least ◀24dB.▶

4. All the radiating elements are fed in phase and, in consequence, the direction of the main lobe is normal to the plane of the aperture. Hence, when used in conjunction with a radar aerial which squints (as is the case with any aerial employing a leaky waveguide) the mounting for the 4992 must be set at a suitable angle to align the two beams.

5. In order to cover targets at all angles of elevation, the vertical radiation pattern of the aerial should be theoretically of cosecant form up to 90 deg. In free space the forward vertical beam is broad, falling by approximately 3dB at an elevation of 45 deg., but the effect of the ground inevitably modifies the pattern by reflecting some

6. A horizontal radiation pattern, plotted over 360 deg. of rotation, is shown in fig. 1. Fig. 2 illustrates the main and adjacent lobes on an expanded scale.

7. The power handling capacity of the aerial is such as to give satisfactory operation with RF pulse powers up to 2·5 kW.

Construction

8. General views of aerial array 4992 are given in fig. 3 and 4. The aerial consists of four sections each approximately 5 ft long, a power distribution box and three support castings by which the complete assembly is secured to mounting 6437. The over-all length of the whole aerial is 20 ft 4 in and it weighs approximately 250 lb.

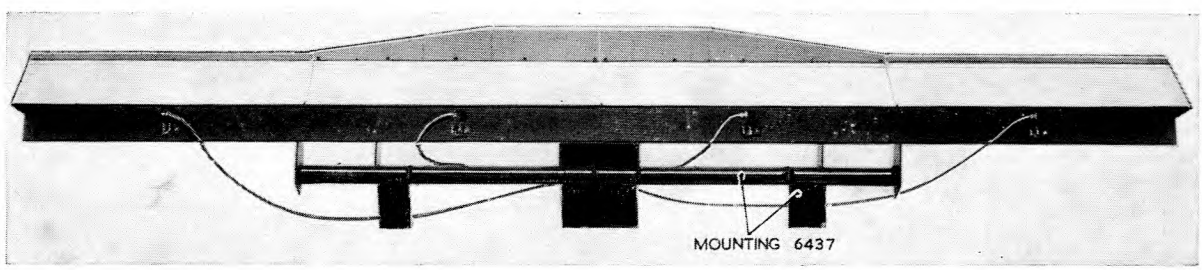

Fig. 3. Aerial array 4992 on mounting 6437: general view

9. Each aerial section consists of a sheet metal box triangular in shape with two cast brackets bolted to the back plate. The base of the triangle forms the support for the radiators and feeder system. The rear brackets carry three tubular tie-bars of which the inner pair are 1 in in diameter and the outer one $2\frac{1}{2}$ in. Considering the left-hand outer section (fig. 5) all three tie-bars end at the left-hand bracket but extend beyond the right-hand bracket to the edge of the section. The right-hand ends of the tie-bars are fitted with collars and knurled locking rings internally threaded.

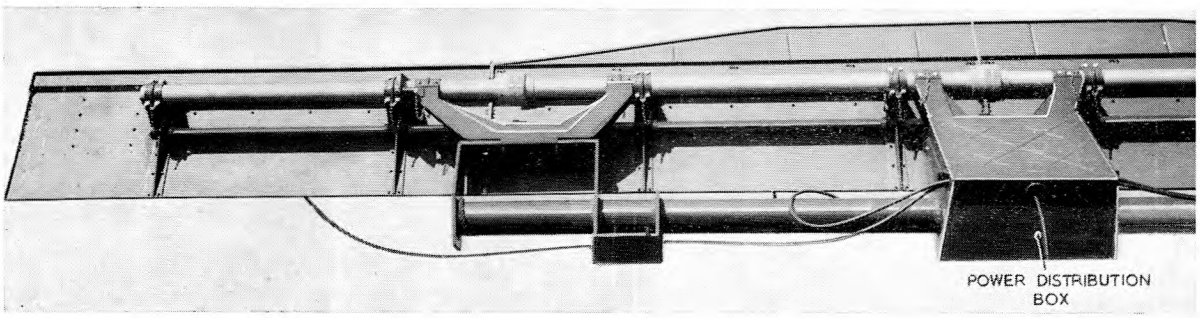

Fig. 4. Aerial array 4992: view of left-hand sections

10. The tie-bars on the adjacent section (left-hand inner) extend the full length of the section. On this section the left-hand ends of the inner tie-bars carry externally threaded collars while the outer is fitted with a collar and an internally threaded locking ring. Both sections are flanged, adjacent flanges being drilled to take fixing bolts. When the two sections are assembled, the flanges are bolted together and the locking rings on the tie-bars screwed home tightly so that a rigid structure is formed. The remaining sections of the aerial (right-hand inner and outer) are similarly constructed.

11. Part of the tie-bar assembly is shown in fig. 6 while the general arrangement of the complete aerial and mounting 6437 is given in fig. 16.

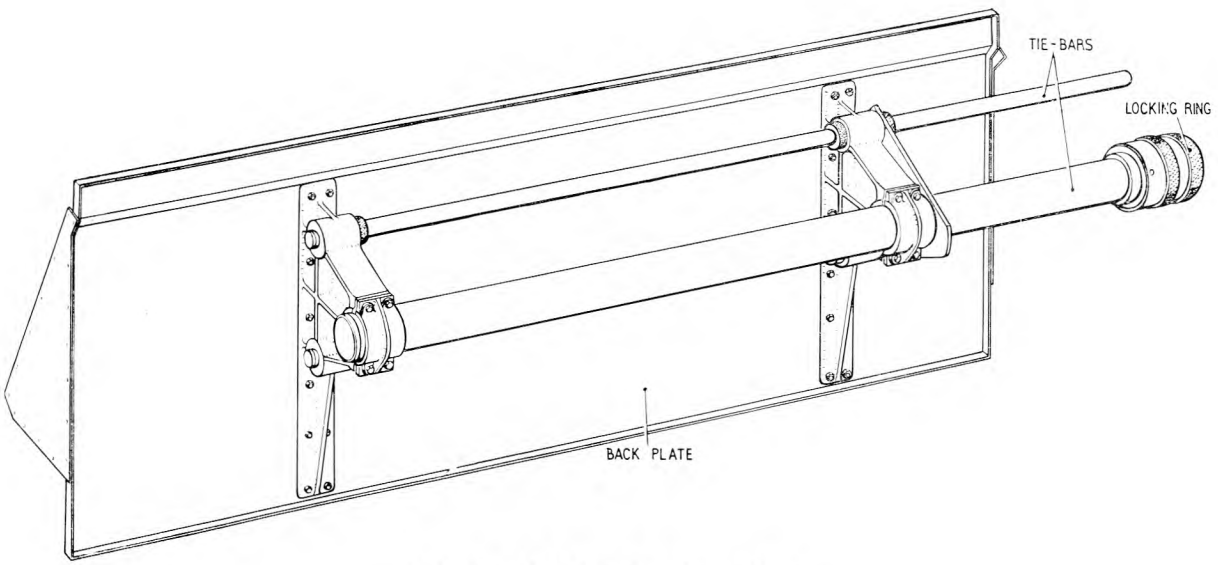

Fig. 5. Left-hand outer section

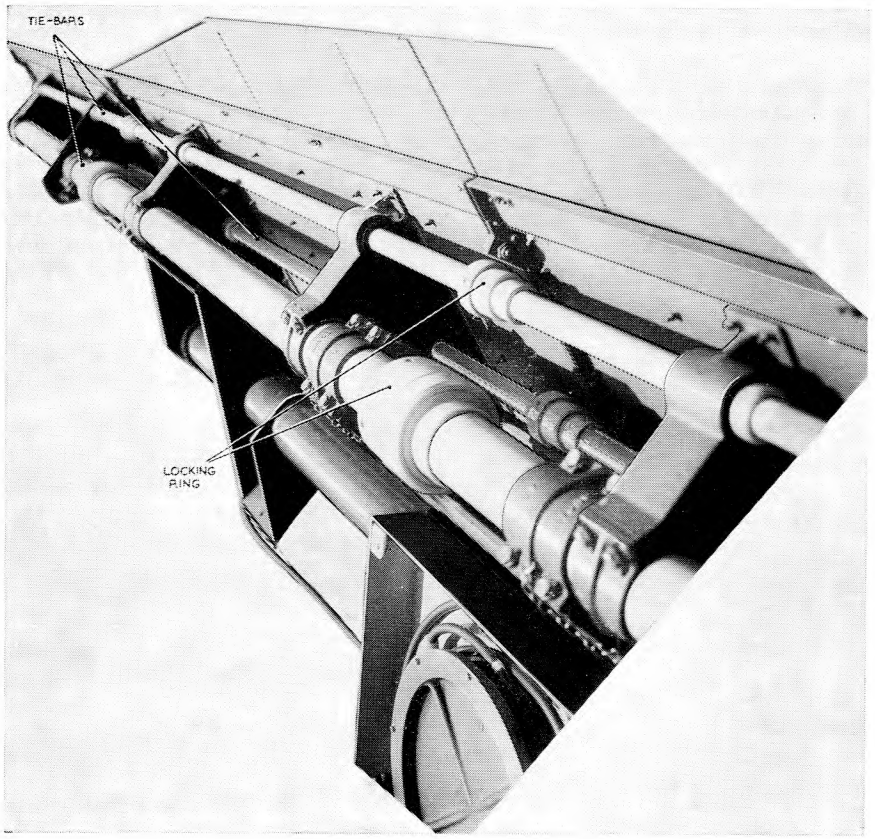

Fig. 6. View of tie-bar assembly

12. The front aperture is covered by a fibreglass window. The purpose of this is to prevent damage to the radiating and feeder system and to exclude the entry of water or dirt. It has a negligible effect on the electrical performance. To reduce the possibility of deterioration due to moisture or icing, a heating element is fitted at the front of each section. The two heaters in each half of the aerial (left-hand or right-hand) are connected in series and the two pairs are fed in parallel from a 24V, 13A source.

plane as shown in fig. 7. For a given distance between the copper conductor and the earth plane the impedance varies inversely as the width of the copper line whilst, for a given applied RF potential, the current flow towards each radiating element varies inversely as the impedance of the line feeding it. Thus, any required current distribution may be obtained by suitable design of the impedance of the feeder, i.e. the dimensions of the

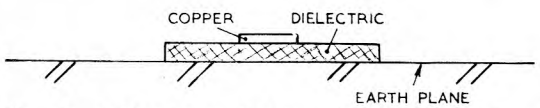

Fig. 7. Microstrip feeder: simplified diagram

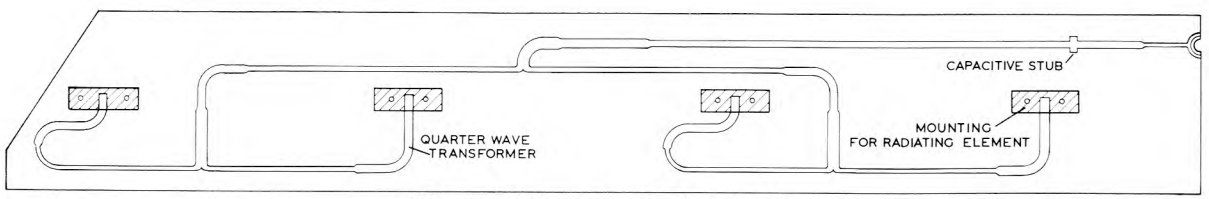

Fig. 8. Microstrip feeder section

Feeder and radiating system

13. The feeder system employs a new type of transmission line using a printed circuit technique. The feeder to the radiating elements is formed of microstrip transmission line which consists of a copper conductor deposited on a dielectric sheet of silicon-bonded fibreglass mounted on an earth

copper conductor and the thickness of the dielectric.

14. A feeder section is illustrated in fig. 8. Each aerial section contains two such feeders of 104 ohms impedance in parallel thus giving an input impedance of 52 ohms. Each feeder drives four radiating elements so that a single aerial section

contains eight radiators. The feeder system is matched to the radiating elements by quarter-wavelength transformers and to the input coaxial line by capacitive stubs.

15. The radiating element consists of a triangular blade one quarter-wavelength high with a $\frac{1}{4}$ in lip at the top and situated approximately one quarter-wavelength in front of the back plate of the aerial section. The element is vertically polarized and has a good match to 52 ohms over the frequency range of the aerial, 1000 to 1120 MHz. Fig. 9 illustrates a section with the fibreglass window removed to show the radiators and feeder system.

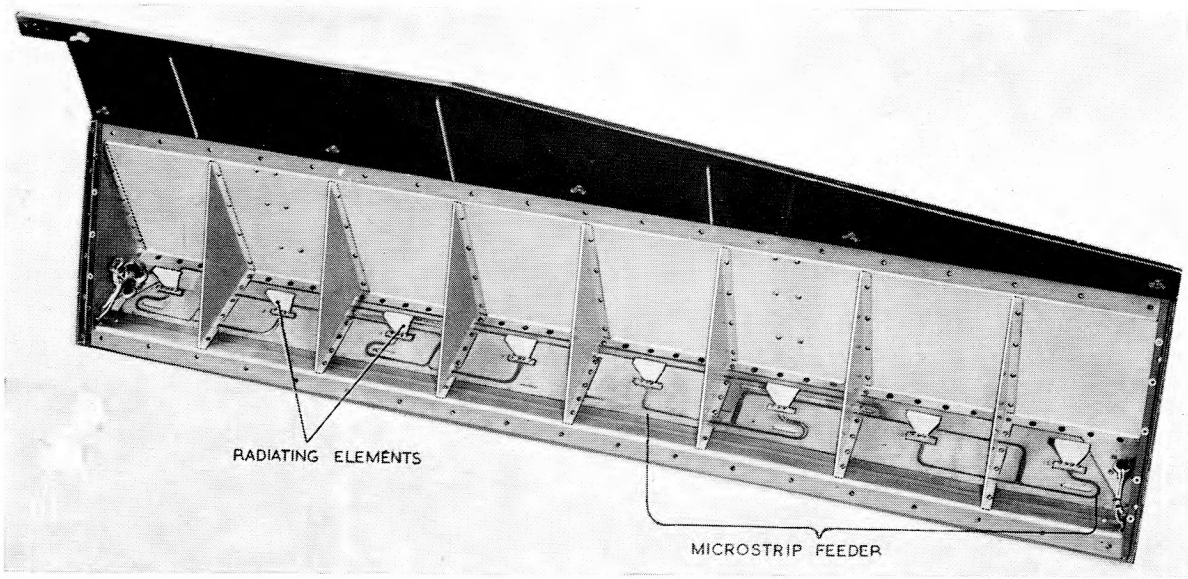

Fig. 9. Aerial section with fibreglass window removed

Power distribution box

16. The current to all the radiators is in phase but the amplitude is tapered, i.e. the power level decreases progressively from the centre to each end of the complete aerial in a symmetrical manner following approximately a cosine-squared pattern. Since the input impedances of the four separate aerial sections are equal, the distribution box coupling the sections to the main coaxial line is designed to share the power in the proportions necessary to provide the desired distribution law.

17. By the principle of reciprocity the aerial operates equally in a receiving role. The currents in the various elements are combined in the appropriate proportions within the aerial sections and within the distribution box to produce, at the main coaxial connection, an output which is a maximum when the received signals at all the elements are in phase.

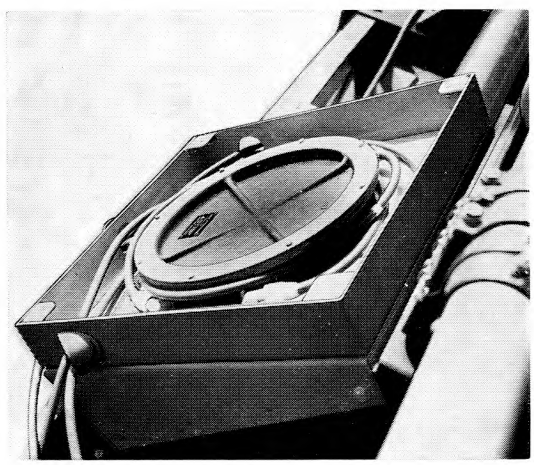

Fig. 10. Distribution box 106

18. A general view of the box in position at the rear of the aerial is given in fig. 10. The box contains an inner section which houses and forms part of the distribution and filter unit shown in fig. 11.

19. The distribution unit is similar in construction to the printed wiring feeders within the aerial sections but is formed of stripline which is a balanced transmission line with a mode of propagation analagous to that of coaxial line. The centre conductor is of copper strip printed and carefully registered on both sides of a dielectric sheet mounted between two earth planes as shown in fig. 12. Stripline is a high-Q form of transmission line in which little of the RF field penetrates the dielectric supporting the feeder and the losses associated with propagation are consequently small.

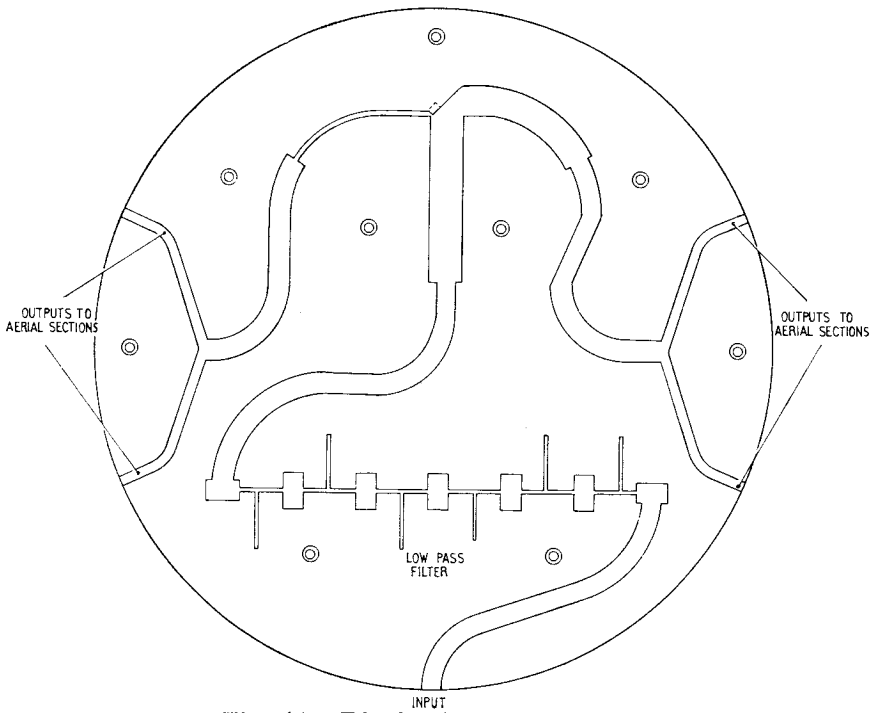

Fig. 11. Distribution and filter unit

20. In the aerial array 4992 distribution unit the earth planes are formed by the top and bottom of the circular inner section of the box shown in fig. 10, the printed circuit being supported between the two on insulating pillars.

21. RF energy is fed into the distribution box and first passes through a low-pass filter with a cut-off frequency of 2500 MHz and an attenuation region extending up to 4000 MHz. This filter forms a protection for the IFF equipment against neighbouring S-band radars.

22. From the low-pass filter the RF energy is fed to the power distributor which divides into two branches. The branches are further subdivided to feed each aerial section. Stripline has similar characteristics to microstrip (*para.* 13) in that the impedance is a function of the width of the copper conductor and the spacing from the earth plane. By appropriate variation in the widths of the branches the power is correctly divided between the inner and outer sections of the aerial. As with the microstrip feeder in the aerial sections, impedance matching is effected by the inclusion of quarter-wavelength transformers.

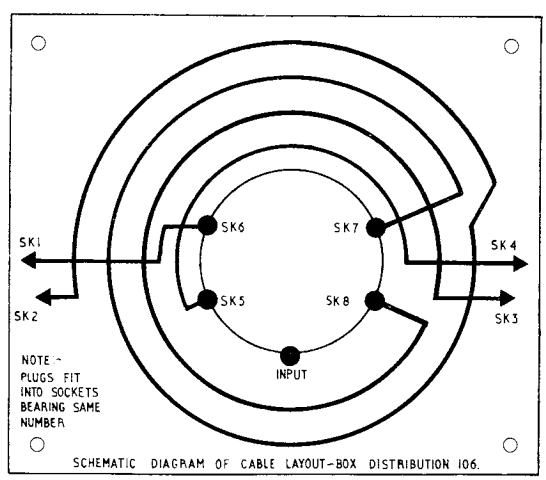

Fig. 13. Distribution box cover label

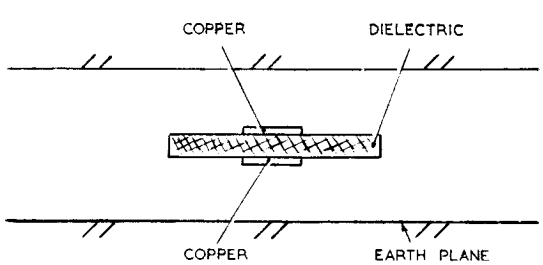

Fig. 12. Stripline: simplified diagram

23. The length and point of attachment of the individual coaxial cables from the aerial sections are important and to ensure correct assembly a label is secured to the cover of the distribution box. This label is illustrated in fig. 13.

24. It should be noted also that these coaxial cables are supplied in sets of four and that the cables forming a set have been selected in production for matched electrical lengths. The probability is that any change in electrical length with age and exposure to the weather will be similar in all four and they will thus remain substantially matched. If any one of these cables is damaged after installation it is important that all four be replaced by a new set.

AERIAL ARRAY 4992A

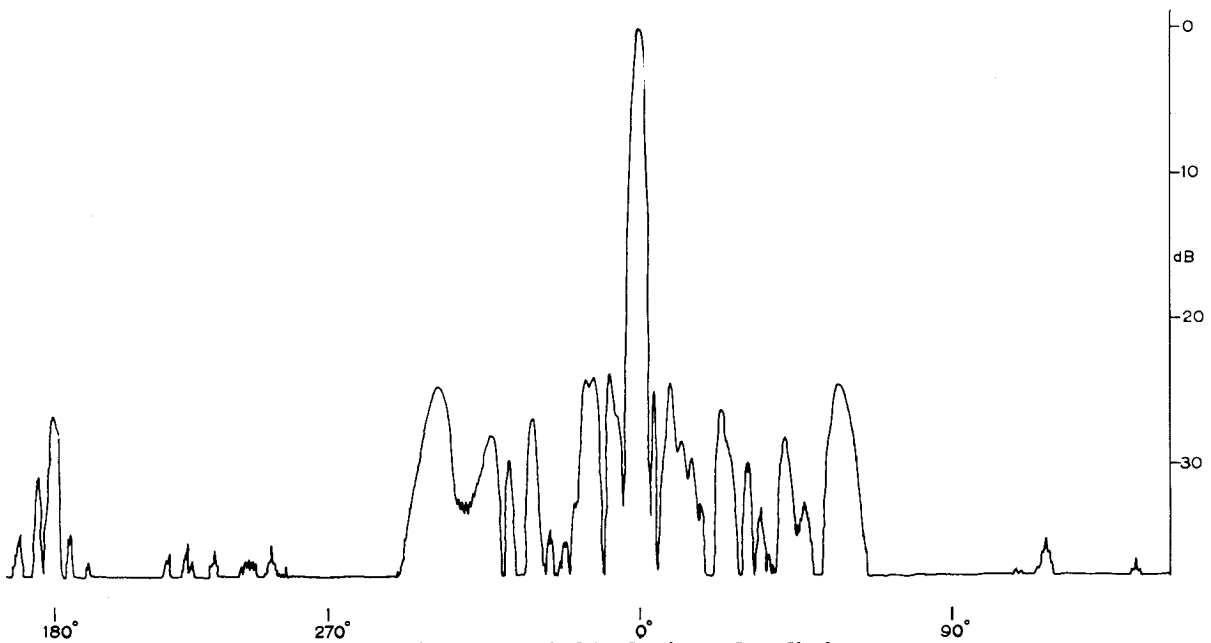

Fig. 14. Aerial array 4992A: horizontal radiation pattern

General

25. Aerial array 4992A is similar to and interchangeable with aerial array 4992 but includes some important modifications designed to improve its performance. The following paragraphs describe the differences between aerial array 4992A and aerial array 4992.

Electrical characteristics

26. The side lobe level is 21dB below the main beam. The back lobe in the horizontal plane is at least 24dB down and at the rear of the aerial the vertical pattern remains below −20dB up to an angle of 45 deg. The forward vertical pattern is approximately 3 dB down at an elevation of 30 deg. Typical radiation patterns are shown in fig. 14 and 15.

Mechanical construction

27. Aerial array 4992A is similar in construction to aerial array 4992. The front aperture of each of the radiating sections is covered by a fibre-glass window, whose primary purpose is to prevent damage to the radiating system and to exclude water and dirt. A grid of parallel wires is attached to the interior face of the window to reduce horizontally polarized radiation and to increase the forward gain of the aerial.

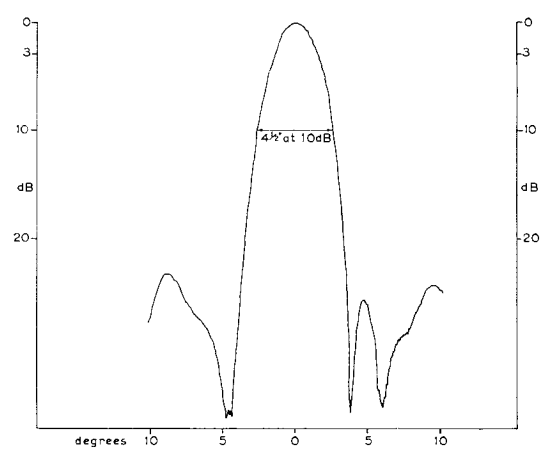

Fig. 15. Aerial array 4992A: main lobe pattern expanded

Feeder and radiation system

28. The feeder system, although identical in principle and construction with that of the aerial array 4992, differs slightly in the layout of the printed circuit, giving an improved sidelobe level. For greater reliability, all plug and socket connections on aerial array 4992A are 'N' type.

Residual phase-error correction

29. To correct residual phase errors in the four radiator sections, the four matched feeder cables may be effectively adjusted in length by the addition of short cables in series. None, some, or all of the sections may need adjustment and this is effected by the manufacturers once and for all. The short cables, although loose parts, are associated with individual radiator sections and are labelled correspondingly.

Note . . .

When a set of matched feeder cables is changed (para. 24) it is essential that the short cables be retained with their proper radiator sections.

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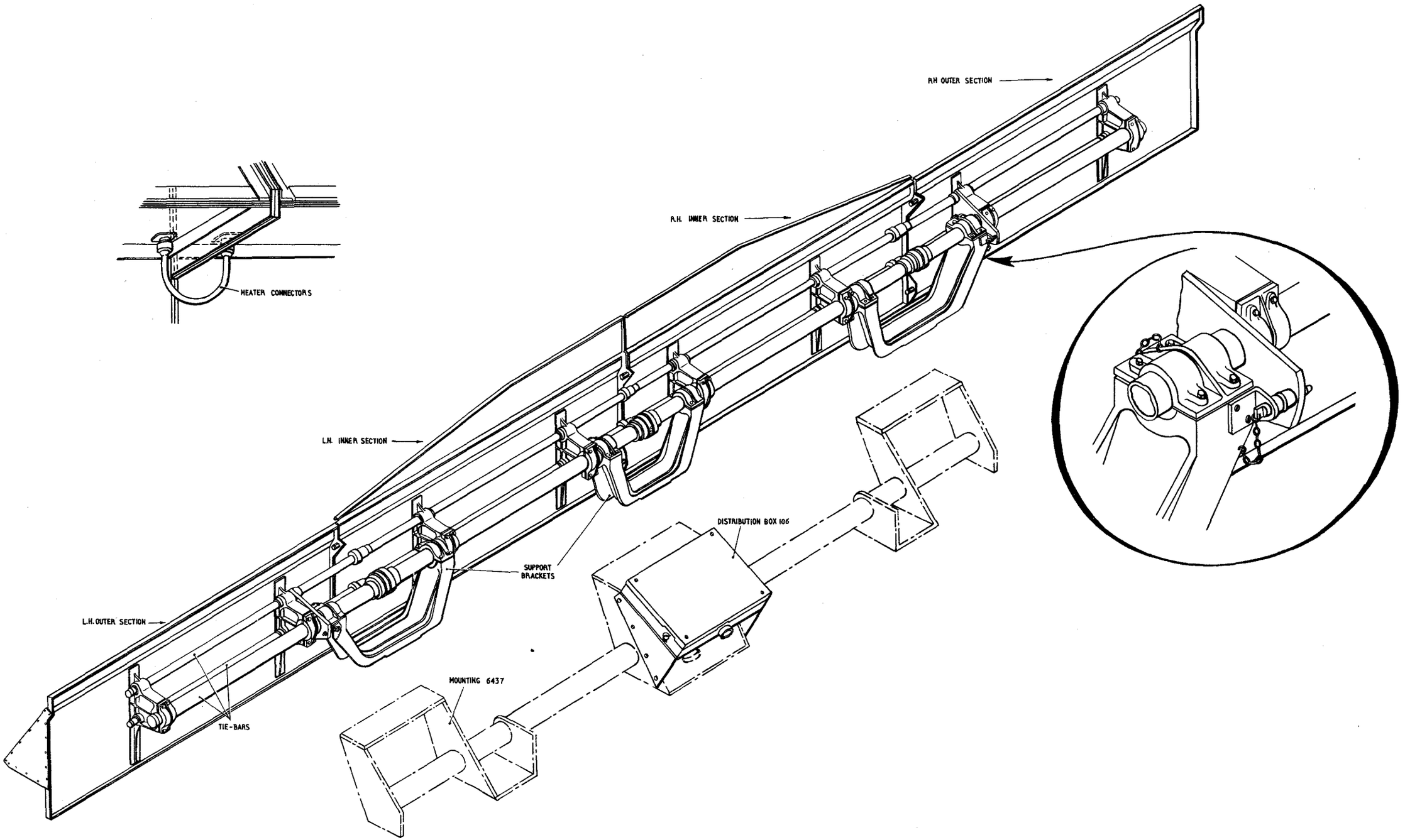

Fig. 15

Aerial array 4992 general arrangement

Fig. 16

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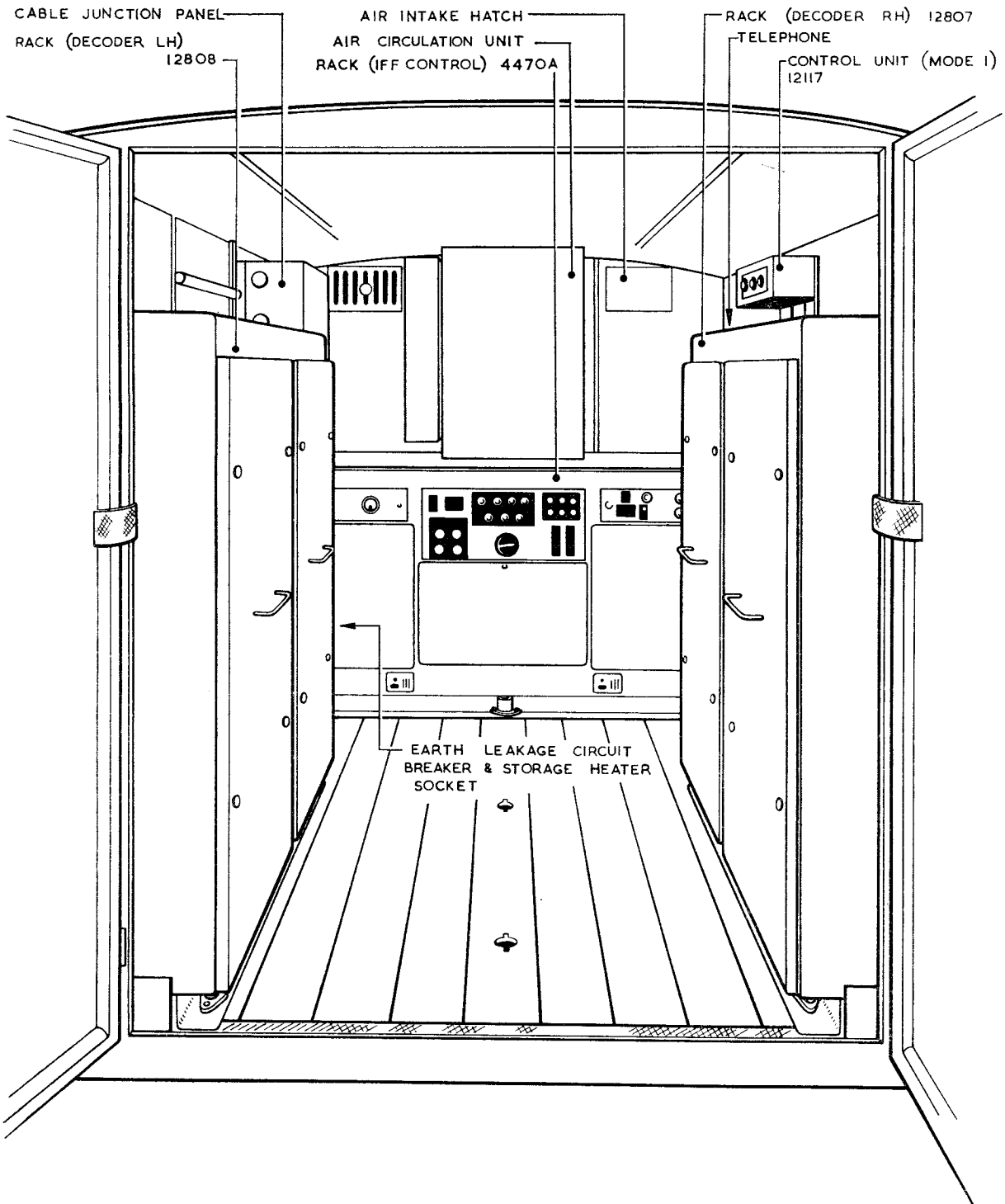

Fig. 1. RVT 511 Mk. 2: interior view

General

1. Radio vehicle Type 511 Mk. 2 is a RVT 511 Mk. 1 modified to include SIF facilities. This is achieved by the installation of two racks housing the SIF units, a junction box, the necessary cabling and a re-arrangement of certain existing items stowed in the vehicle in order to provide sufficient room for the racks. A general view of the interior of the modified vehicle is given in fig. 1.

Interior modifications

2. To accomodate rack (decoder RH) 12807, the telephone is moved from its location under the right-hand window and mounted on a shelf above the right-hand end of rack (IFF control) 4470A, while the earthing rods and cable drum support frames, formerly stowed against the right-hand wall below the fire extinguisher, are now stowed outside the vehicle under the cabin on the off side. The fire extinguisher is fitted on the inner side of the left-hand door.

3. It should be noted that, as a result of the modifications, only three small cable drums can be carried in the RVT 511 Mk. 2 during transit.

Rack (IFF control) 4470A (*fig.* 4)

4. With the introduction of the SIF decoders it becomes necessary to increase the amplitude of the video signals fed out from the control rack. This is accomplished by removing the video divider networks (resistors R15 to R26 in fig. 8, Chap. 2) from rack 4470. The rack is then re-identified as rack (IFF control) 4470A (Ref. No. 10D/23444). The cover plates over the outlets below the left and right-hand compartments of the rack are removed and a short length of ducting coupled to each outlet conveys air to the adjacent SIF rack.

SIF racks

General

5. The SIF equipment is housed in two racks, one (rack (decoder RH) 12807) against the right-hand wall of the cabin and the other (rack (decoder LH) 12808) against the left-hand wall, when viewed from the rear of the cabin. Each rack consists of a steel cabinet measuring 4 ft. 4 in. high × 1 ft. 3 in. deep × 3 ft. 8 in. wide overall and divided into two compartments. These compartments contain hinged sub-frames on which the SIF units are mounted but, whereas in the right-hand rack both compartments are used, only one compartment in the left-hand rack houses equipment. Provision is made for interior illumination by lamps connected across the 230V supply and controlled by switches mounted on either side of the indicating lamps at the top of the front frame. The racks are normally enclosed by removable panels held in position by Oddie fasteners.

6. Air from rack (IFF control) 4470A enters the base of each SIF rack and, after passing over the equipment, is exhausted into the cabin by fans mounted at the top of the rack.

Rack (decoder RH) 12807

7. The left-hand compartment of rack 12807 contains two passive decoders 6892 and a power unit 6889. An emergency decoder 6888 is mounted on the passive decoder occupying the bottom position. This assembly provides normal and emergency decoding on mode 1 for all consoles in the convoy. The other passive decoder affords mode 2/3 decoding for one PPI display.

8. The right-hand compartment contains a test set (decoder) 4678 and its associated power unit 6889, the remaining space being blanked off by two panels (stowage) 12473. A circuit diagram of the rack is given in fig. 5. The mode 1 control unit 12117, shown on the diagram as one of the rack units, is mounted externally on the top of the rack cabinet.

Rack (decoder LH) 12808 (*fig.* 6)

9. As stated in para. 5, only half of this rack is used and the left-hand compartment contains no sub-frame. The right-hand compartment houses two passive decoders and a power unit 6889. The passive decoder in the bottom position carries an emergency decoder sub-assembly to provide emergency decoding on mode 3 while the other passive decoder affords normal mode 2/3 decoding facilities for one PPI display.

10. For detailed descriptions of all the units contained by the racks reference should be made to Part 1, Sect. 4 and Part 2, Sect. 1.

Test facilities

11. In normal operation, control of the passive decoders is effected remotely from the RVT 510 display vehicle but, to facilitate testing the units in situ, local test switches simulating the switching provided in the remote control unit are included in each rack. A panel, mounted above the rack units, carries six switches. Four of these control the code selection relays in the passive decoder while the other two are for mode and function (ALL SIGS/ONE CODE/ALL CODES) selection.

12. The contacts of the local test switches are connected to a socket SKW mounted internally on the rack frame. In normal operation this socket has no mating plug and the switches are consequently inoperative. When it is necessary to test one of the passive decoders in the rack, the appropriate plug (PLU or PLV) is disconnected from its socket and coupled to SKW so that the local switches are connected to the decoder under test.

Control unit 6884

13. Although this unit is located in the display vehicle and does not form part of the additional

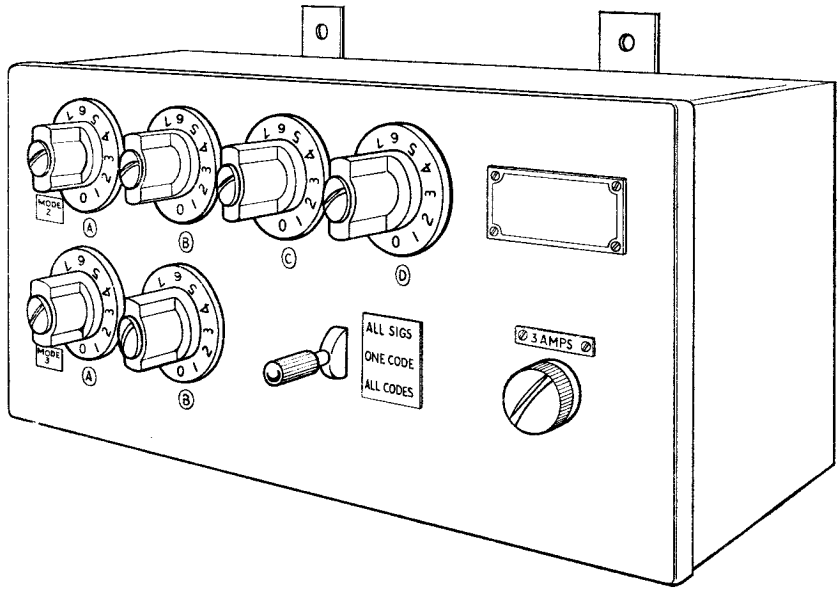

Fig. 2. Control unit 6884: general view

equipment in the RVT 511 Mk. 2, it is convenient to include it in this chapter since it provides remote control of code selection for the mode 2/3 decoders in the SIF racks.

14. Control unit 6884 is similar to control unit (passive) 12118 used in the static application and affords the same facilities. It consists of a rectangular steel case with two mounting plates fixed on the back (*fig.* 2). The front panel carries six wafer switches, four for mode 2 and two for mode 3. These switches are of the same type as those on control unit 12118 and the indicator plates are illuminated in a similar manner. In addition, the ALL SIGS/ONE CODE/ALL CODES switch is provided on control unit 6884 instead of on the console. A circuit diagram is given in fig. 3.

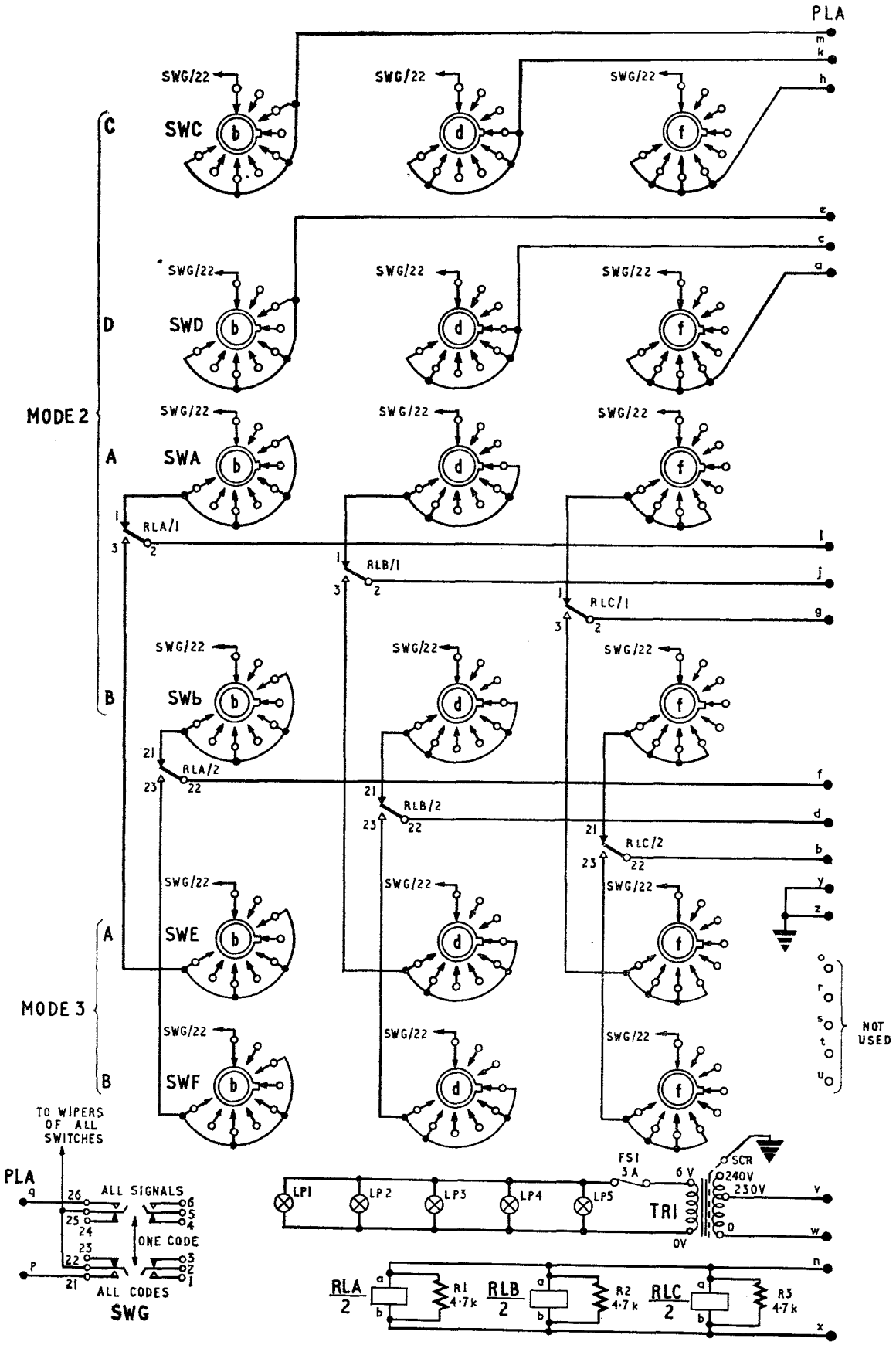

Fig. 3. Control unit 6884: circuit

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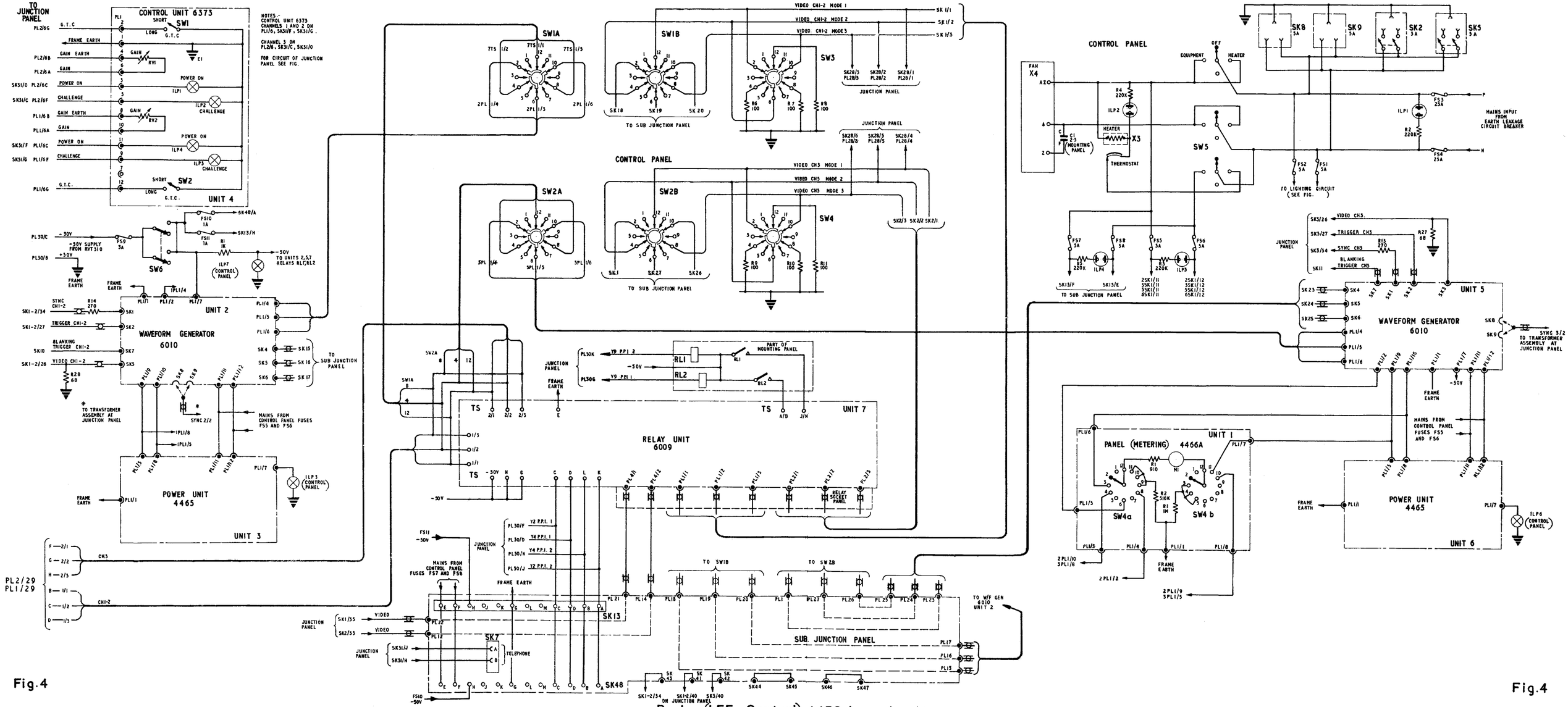


Fig.4

Rack (I.F.F. Control) 4470 A : circuit

Fig.4

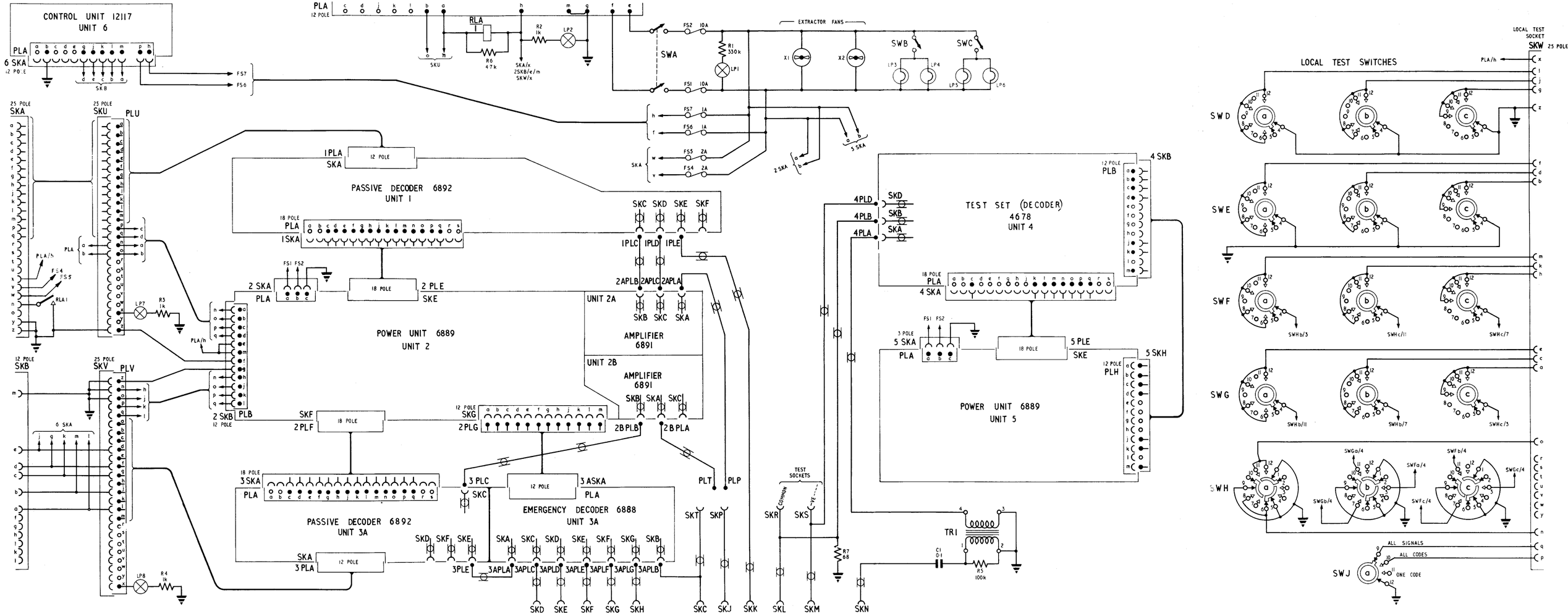


Fig. 5 2281/281490/21/5/63 J. T. & S.

Rack (decoder RH) 12807 : circuit

Fig.5

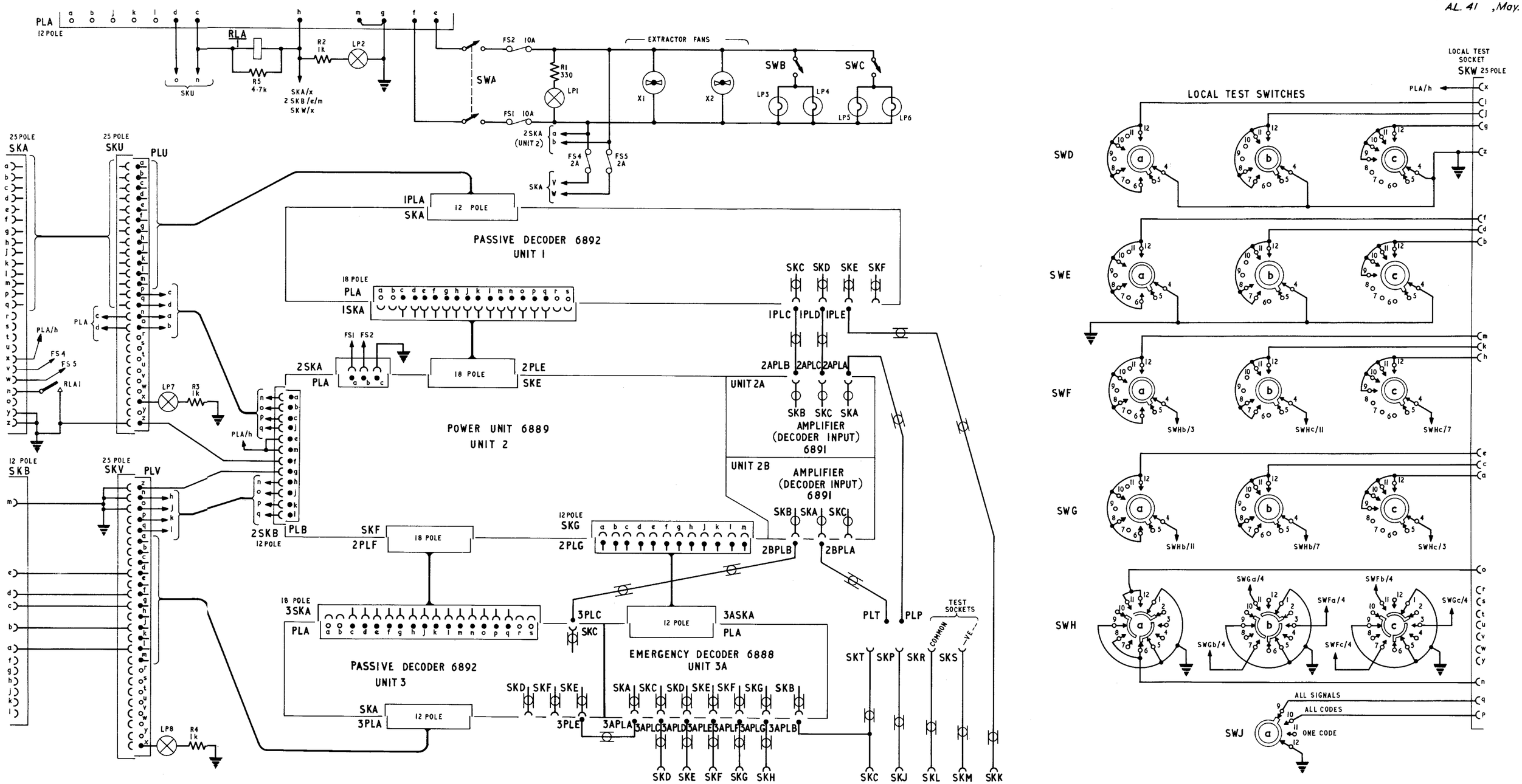


Fig. 6

2281/281490/21/5/63 J. T. & S.

Rack (decoder LH) 12808: circuit

Fig 6

SECTION 4

SIF

(including passive decoding)

Chapter 1

(Completely revised)

INTRODUCTION

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

General

1. The basic IFF Mk. 10 system is described in Sect. 1, Chap. 1 and a brief reference is made therein to additional coding facilities. When these are added, the system becomes IFF Mk. 10 (SIF) and the purpose of this section is to describe the operation of the selective identification feature (SIF) and the additional equipment required in the ground installation. SIF is an optional facility and, although it is probable that it will become universal in application, it does not form an essential part of IFF Mk. 10. Thus its omission (if not required) will not affect the use of the basic system.

2. The selective identification feature expands the basic three modes of the Mk. 10 system by introducing multiple pulse coding of the transponder replies to interrogation, the characteristics of the basic interrogations remaining unchanged. Thus, no modification of the interrogator is required and coding is achieved by fitting a suitable coding unit to the aircraft installation.

3. When a coder is fitted in an aircraft, the normal reply pulses of the transponder initiate a pulse train consisting of 14 pulses as shown in fig. 1. The first and last pulses are known as the frame (or bracket) pulses and their leading edges are separated by 20·3 microseconds; they are always transmitted in reply to any mode of interrogation.

4. Between the two frame pulses there are 12 pulse positions, but the number of pulses actually transmitted depends upon the code selected in a particular mode. Each of the 12 code or information pulses is allocated an identifying letter and a numerical value, as shown in fig. 1, so that four groups of three pulses are formed. Thus, the maximum unit which can be transmitted is 7, represented by the three pulses of any one letter group with values of 1, 2 and 4 — these values being added. If all 12 pulses are transmitted, the code 7777 is obtained (*fig.* 1(a)). When the frame pulses only are transmitted, the code becomes 0000.

5. If all 12 information pulses are used, it is possible to obtain a maximum of 4096 codes. At present, however, this figure is considerably in excess of requirements and it is probable that a maximum of only six information pulses will be employed to make available the following SIF codes on each interrogation mode: —

Mode 1 — 32 codes designated 00 to 73
Mode 2 — 400 codes from a possible total of 4096 designated 0000 to 7777
Mode 3 — 64 codes designated 00 to 77.

Mode 1

6. This mode is used for general identification and will normally have a fixed common code to be used by all aircraft, the code being changed only rarely. The transponder response will be limited to the A1, A2, A4, B1 and B2 information pulses so that a total of 32 codes is available.

Mode 2

7. Mode 2 is the personal identification mode and certain aircraft are each allotted an individual code which is preset before flight. It is probable that a fixed number of six information pulses will be used, consisting of three pulses from each half of the pulse train (*i.e.* three A and/or C pulses and three B and/or D pulses), so that initially there will be 400 codes.

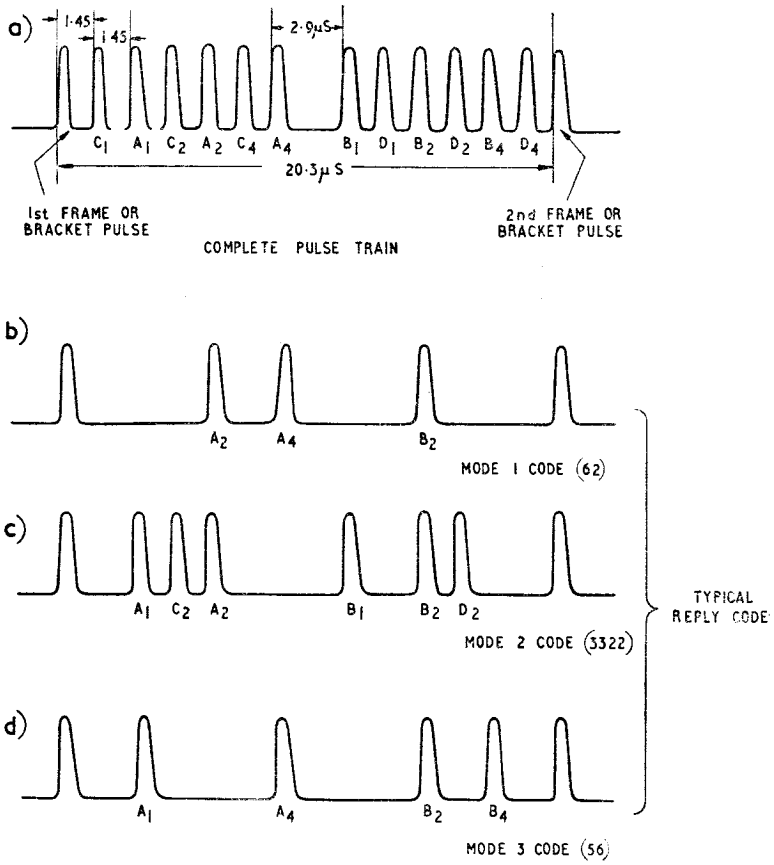


Fig. 1. SIF pulse trains

Mode 3

8. Mode 3 is used for traffic identification, *i.e.* it indicates the classification of an aircraft. Normally the code will be preset before flight but it may be changed in flight on instructions from the ground. The transponder response is limited to the A and B pulses, as in mode 1 operation, but B4 is included on mode 3 and, thus, all six information pulses are used. There is thus a total of 64 codes available.

Emergency

9. The facility whereby an aircraft can transmit a distress signal which produces a characteristic PPI display has been retained. When the transponder is switched to emergency, it transmits four pulse trains in reply to each mode 1 interrogation and the system is so arranged that the indication will appear at any PPI position where IFF is selected, irrespective of the interrogation mode in use. This is done by mixing the last three ◀decoded▶ pulse trains of the mode 1 four-train emergency signal with mode 2 and mode 3 responses. Certain coding units can, however, also provide an emergency train in reply to mode 3 interrogations.

I/P

10. Another facility known as identification of position (I/P) is provided for the rapid indentification of a particular aircraft. It is selected by a switch in the aircraft and the transponder then transmits a double mode 1 response, continuing to do so for 22·5 seconds after the I/P switch is returned to the off position. Here again, some coders can also provide an I/P response to mode 3 interrogations. The mode 1 I/P response is handled by the ground decoders in the same way as the emergency reply.

Decoding

General

11. The coded responses from an aircraft are received by the ground responsor in the usual manner and are then processed, by decoding equipment, to ascertain the answer to the original interrogation. The ground decoder is normally operated on one code of a particular mode at a time. There are two systems of decoding; passive decoding, which elicits the answer to the question "Where are you?", and active decoding, which provides the reply to the question "Who are you?". A block diagram of the SIF equipment in a typical installation is given in fig. 2.

12. The ground decoder may be operated in any one of three different ways depending upon the setting of a control switch at the console. The switch positions are designated as follows:

	British	*U.S. equivalent*
1.	ALL SIGNALS	Raw
2.	ONE CODE	—
3.	ALL CODES	Bracket decode

All signals

13. When the control switch is set to position 1, the decoder passes all IFF signals to the PPI unchanged except for the insertion of a systematic delay. This method of operation is used to display IFF responses from aircraft not fitted with coders. Alternatively, it may be employed where coder or decoder unserviceability is suspected.

One code

14. This is the normal setting of the decoder. The responses from all aircraft within range transmitting the code set up on the code selection switches of the ground equipment are processed by the decoder which presents a single pulse for display on the PPI.

All codes

15. With the control switch set to ALL CODES, only SIF responses are selected and the decoder decodes on the frame pulses, presenting a single pulse for display on the PPI. This condition is normally used when the reply code is unknown but it is also of value when two aircraft are on approximately the same bearing and within two nautical miles (radial distance) so that their coded pulse trains are mutually interfering and thus preventing normal decoding.

Mode selection

16. Each console has individual selector switches for both the mode 2 and mode 3 decoder settings. For mode 1 codes however, a single common control unit is provided and this is located in the radar office, adjacent to the SIF equipment racks.

Active decoding

17. If the SIF code of an aircraft is not known, its response cannot be decoded by the passive decoder except on the ALL CODES setting. To identify such an aircraft, the active decoder may be used. The ALL CODES response concerned is encircled by a ring strobe marker which controls the position of the active decoder gate. This gate is the area of a 3 mile square on the tube face (with a 6 mile square as an alternative) and may be marked on the PPI screen by lines, known as boundary marks, painted once per revolution in the same manner as the radar echoes. The active decoder then assesses, on a probability basis, only the responses enclosed within the gate and evolves an answer. The gate sizes quoted are provisional and are subject to alteration in the light of experience.

18. The gate waveform is used to gate the decoded frame pulses which provide the ALL CODES display and it is this output which operates the active decoder. Thus, the strobe marker need only encircle part or all of the ALL CODES response. If, for any reason, active decoding is required on the ALL SIGNALS setting, it is necessary only to encompass the first frame pulse of the pulse train with the marker.

19. The active decoder will only decode once per revolution and then only if the frame pulses are present (*i.e.* it will not decode if a group of random pulses is received). The answer given is then displayed on a numerical indicator associated with the console. Briefly, the answer is decided by a code criterion circuit which summates the information in the successive pulse trains received and presents on ◀numerical▶ indicators the designation of the code pulse combination received most frequently. If a consistent code occurs in approximately only half of the received pulse trains, an additional lamp (marked QUERY) will light.

20. Once a code has been given, it is necessary to reset the indicator before the next decoding operation can take place. A further check on the identity of the aircraft can then be provided by setting up the indicated code on the passive decoder control unit. The response should then appear as a single pulse on the PPI when the ONE CODE position is selected.

Emergency decoding

21. The emergency signal referred to in para. 9, after being decoded in the mode 1 decoder, is fed to an emergency decoder whose output is passed to all consoles irrespective of the mode called for. Since the airborne transponder can always transmit SIF emergency responses in reply to mode 1 interrogations, a modification has been introduced into relay units 6009 whereby mode 1 interrogations are transmitted whenever any mode is selected at a console. Thus, operation of the mode 2 and/or mode 3 switches causes mode 1 interrogations to be included in the mode combination. This arrangement has been chosen because mode 1 is the general identification mode and the code is common to all aircraft. Although certain airborne coders contain provision for the transmission of emergency signals on mode 3, such signals will not appear on the ground display unless the aircraft is being interrogated in the correct mode 3 code. When this is done both mode 1 and mode 3 emergency signals are displayed, one superimposed upon the other.

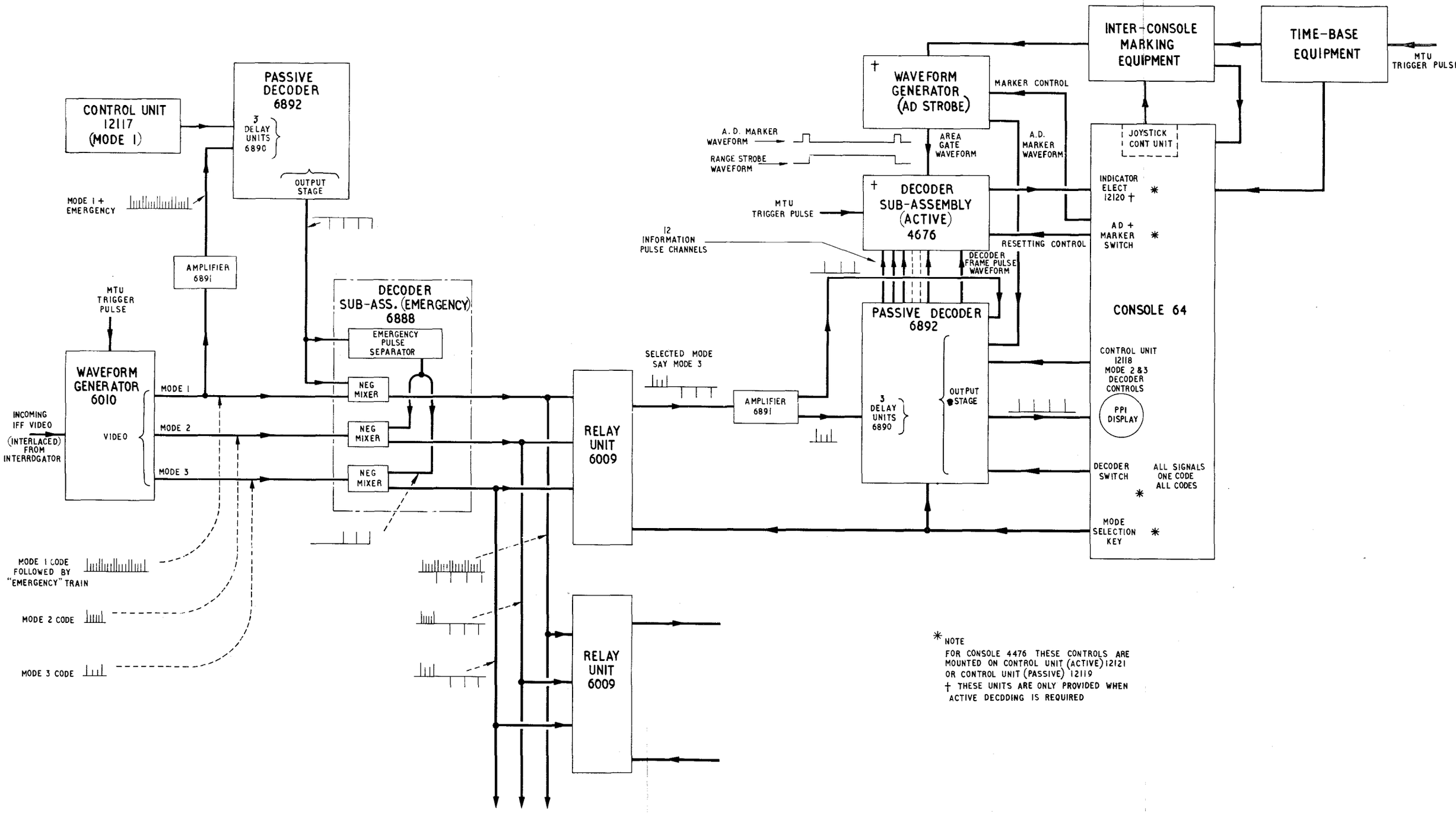
22. The SIF emergency signal, when decoded, produces a mode 1 display of four pulses similar to that of the basic system, but with a spacing of approximately 2 nautical miles instead of $1\frac{1}{3}$ nautical miles. During the decoding process, the last three pulses of the mode 1 emergency signal are mixed with the mode 2 and 3 responses. If the passive decoder is not set to the mode 2 or 3 code of the aircraft in distress, only these last three pulses will be displayed. In order to identify

the aircraft with the active decoder, the passive decoder is set to ALL CODES and the strobe marker positioned on the first of the four pulses obtained. Active decoding of the first pulse of the combined response then elicits the mode 1, mode 2 or mode 3 code designation according to the setting of the mode selector switch on the console. If the marker is placed on one of the later pulses of the response when the display is set to mode 2 or 3, no active decoding occurs.

23. An emergency signal may thus appear as a three or four pulse display depending upon the settings of the ground equipment controls, but the system is so arranged that no SIF distress signal can fail to produce a characteristic display on any PPI at which IFF is selected. Emergency responses from aircraft not fitted with SIF may also be received but can only appear on the display when the passive decoder is set to ALL SIGNALS.

I/P

24. The SIF I/P signal, when decoded, produces a mode 1 display of two pulses with the same spacing as those in the emergency train, *i.e.* approximately 2 nautical miles. The video mixing circuits referred to in para. 22 also ensure that the second of the two I/P pulses appears on all PPI consoles on which IFF is selected. In consequence, an I/P reply may be seen as a one or two pulse display depending upon the settings of the ground equipment controls. With a single pulse, the I/P response will occur at a spacing of $2\frac{1}{2}$ nautical miles after the associated radar echo. This, however, should not cause any confusion since I/P responses will normally be given only for the benefit of controllers who will, presumably, know the SIF codes of the aircraft concerned and have their decoders set accordingly. They will thus receive the two-pulse I/P display. Single delayed I/P responses are consequently of no concern to the operators observing them.



* NOTE
FOR CONSOLE 4476 THESE CONTROLS ARE MOUNTED ON CONTROL UNIT (ACTIVE) 12121 OR CONTROL UNIT (PASSIVE) 12119
† THESE UNITS ARE ONLY PROVIDED WHEN ACTIVE DECODING IS REQUIRED

Fig.2

SIF installation : block diagram

924/8/7536/66528/631/2/62 J. T. & S.

Fig.2

Chapter 2

(This chapter supersedes that issued with A.L. 28)

RACKS (DECODER) 4469 & 4469A and (MODE 1 DECODER) 12276

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General

1. When SIF facilities are included in an IFF Mk. 10 installation the decoding equipment required is housed in racks in the radar office; a minimum of two additional racks is necessary. The racks are similar in design but the units which they contain are determined by the particular application. Rack (mode 1 decoder) 12276 is associated with mode 1 only and racks (decoder) 4469 and 4469A with modes 2 and 3. The rack 4469A is introduced at certain sites which require decoders to operate from local or remote radar equipment.

Construction

2. Each rack consists of a steel cabinet 7 ft. high, $23\frac{1}{2}$ in. wide overall and 21 in. deep with doors at the front and rear. It contains two sub-frames on which the units are mounted. Each sub-frame is supported on hinges at the top and bottom of the left-hand side and can be moved through 90° to clear the cabinet, thus affording access to the rear. This facilitates servicing and permits the installation or removal of sub-assemblies without disturbing the main units. During normal operation, the frame is secured in place by a catch at the right-hand side.

3. Input and output connections to the rack are made through plug panels, designated A and B, mounted in the base. Interconnections between the rack units and between those units and the plug panels are made by free cables carried up the rack sides.

Rack (decoder) 4469

4. This rack, illustrated in fig. 1 and 2, can provide decoding facilities for up to eight consoles

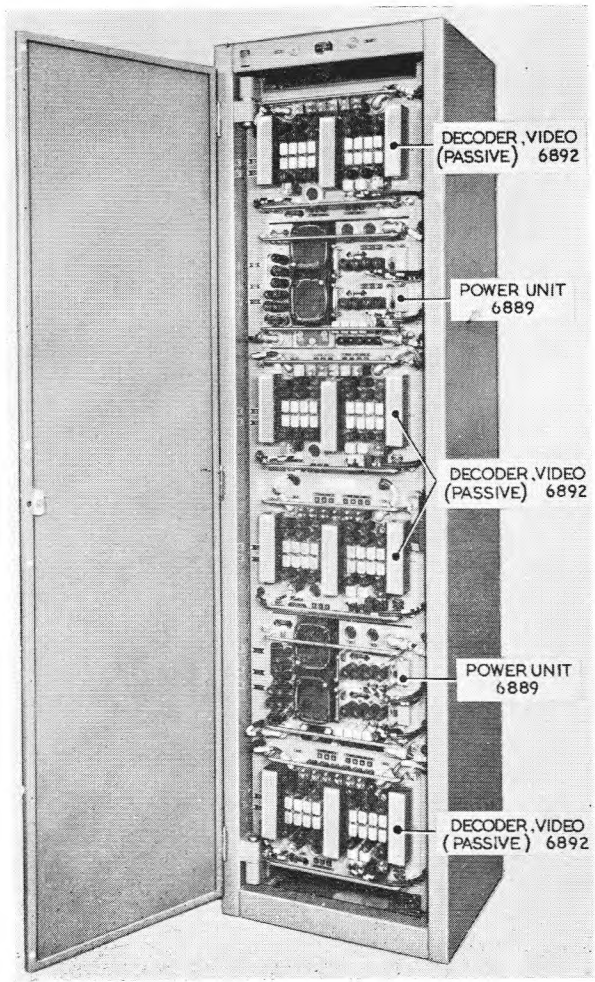


Fig. 1. Rack (decoder) 4469: front view of sub-frame

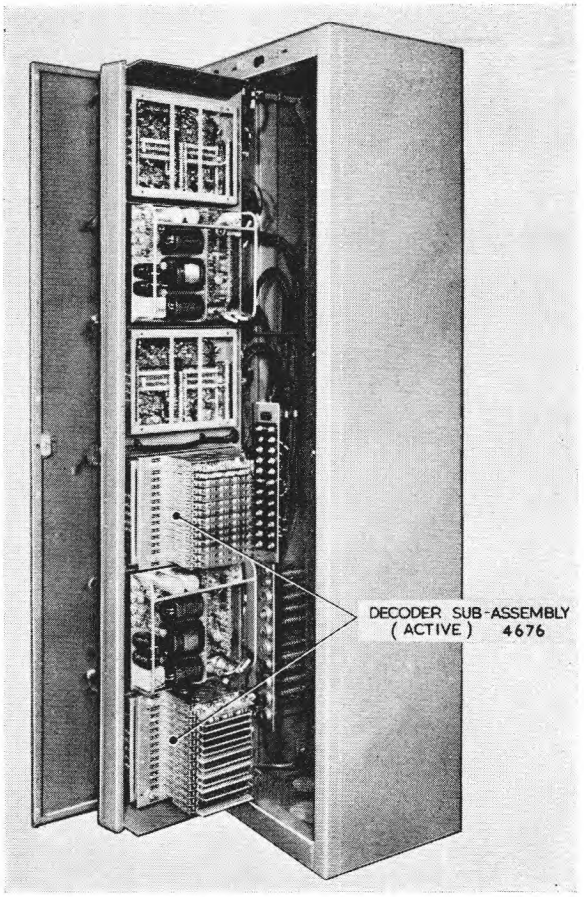


Fig. 2. Rack (decoder) 4469: rear view of sub-frame

and, if completely filled, contains the following twelve main units: —

8 decoders, video (passive) 6892

4 power units 6889

Each power unit will be fitted with two amplifiers (decoder input) 6891 and, in addition, active decoding facilities can be provided on four of the available channels so that four decoder sub-assemblies (active) 4676 may be fitted.

5. Where a rack does not contain a full complement of equipment, the units omitted are replaced by either or both of two stowage panels. Panel (stowage) 12742 replaces the passive decoder and provides stowage for all the associated leads, including those for the active decoder sub-assembly. Panel (stowage) 12744 replaces power unit 6889 and similarly provides stowage for the associated leads. Those passive decoders which have no active decoders fitted are provided with brackets (stowage) 12745 to afford stowage facilities for the active decoder leads.

6. Because of the disposition of the units, rack 4469 is symmetrical, *i.e.* the sub-frames appear identical when viewed from the front. To identify the front and rear sub-frames, the units are numbered in sequence starting from the bottom and the front sub-frame is considered to be that containing units 1 to 6. Sub-assemblies are identified by adding the suffix A to the main unit number. Labels bearing the unit numbers are affixed to the rack frame in the appropriate positions.

7. Ready identification of the front and rear of rack 4469 is necessary since the four passive decoders to which active decoder sub-assemblies may be fitted are always those on the front sub-frame. No active decoder connections are provided to the rear sub-frame.

8. An interconnection diagram for the rack is given in fig. 5. This does not include the coaxial cables which are shown separately in fig. 6.

◀Rack (decoder) 4469A

9. This rack provides similar facilities to the rack 4469 but provision is made for two sync. pulse inputs associated with either local or remote radar equipment. Each decoder sub-assembly (active) 4676 has an associated relay mounted on the panel carrying TR2 and TR3, and each relay enables the appropriate decoder to be fed with the correct sync. pulse for the signals to be decoded.

10. Fig. 7 is an interconnection diagram for the rack. Coaxial cables are not included and these are shown separately in fig. 8.▶

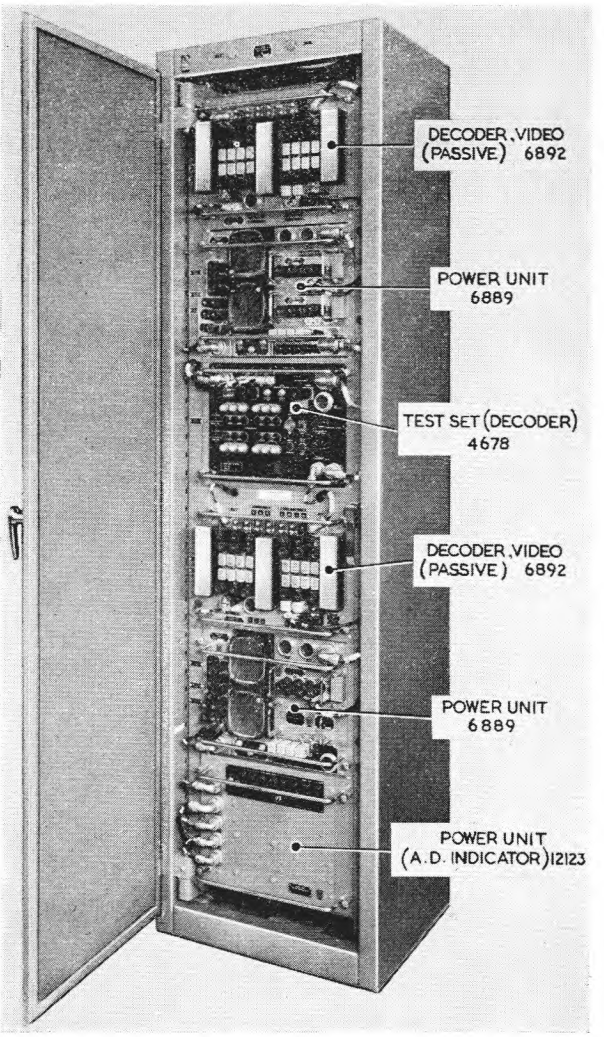


Fig. 3. Rack (mode 1 decoder) 12276: front view of sub-frame

Rack (mode 1 decoder) 12276

11. Rack 12276, illustrated in fig. 3 and 4, contains the mode 1 normal and emergency decoding equipment and also houses test set (decoder) 4678. A completely equipped rack provides up to three mode 1 channels and one standby mode 1 channel. It can thus serve three radar heads if necessary so that only one rack is required per installation.

12. Each rack 12276 can accommodate:

	Unit No.	
Front	1	Power unit (A.D. indicator) 12123
sub-frame	2	Power unit 6889
	3	Decoder, video (passive) 6892
	4	Test set (decoder) 4678
	5	Power unit 6889
	6	Decoder, video (passive) 6892
Rear	7	Power unit (A.D. indicator) 12123
sub-frame	8	Power unit 6889
	9	Decoder, video (passive) 6892
	11	Power unit 6889
	12	Decoder, video (passive) 6892

13. It will be noted that there is no unit 10. This space is occupied by a blank panel on which are mounted the relays shown in fig. 7; it also serves as a convenient interconnection point for some of the rack wiring. The panel is regarded as forming part of the rack assembly and is not removable.

14. As in rack 4469, any of the passive decoders or power units may be replaced by the appropriate stowage panel. Panel (stowage) 12742 may be fitted in place of power unit (A.D. indicator) 12123. All power units 6889 in the mode 1 decoder rack have only one input amplifier and the second amplifier is replaced by a panel (stowage) 12743. No provision is made for a stowage panel to replace test set (decoder) 4678 since this unit is always housed in rack 12276.

15. An interconnection diagram for rack 12276 is given in fig. 7. Relays A to J, which are located on the fixed panel described in para. 11, are associated with the control circuits and the operation of their contacts is shown on the coaxial cable diagram (*fig.* 8). Since mode 1 is common to all consoles, the control unit is located in a convenient position in the radar office. The switches

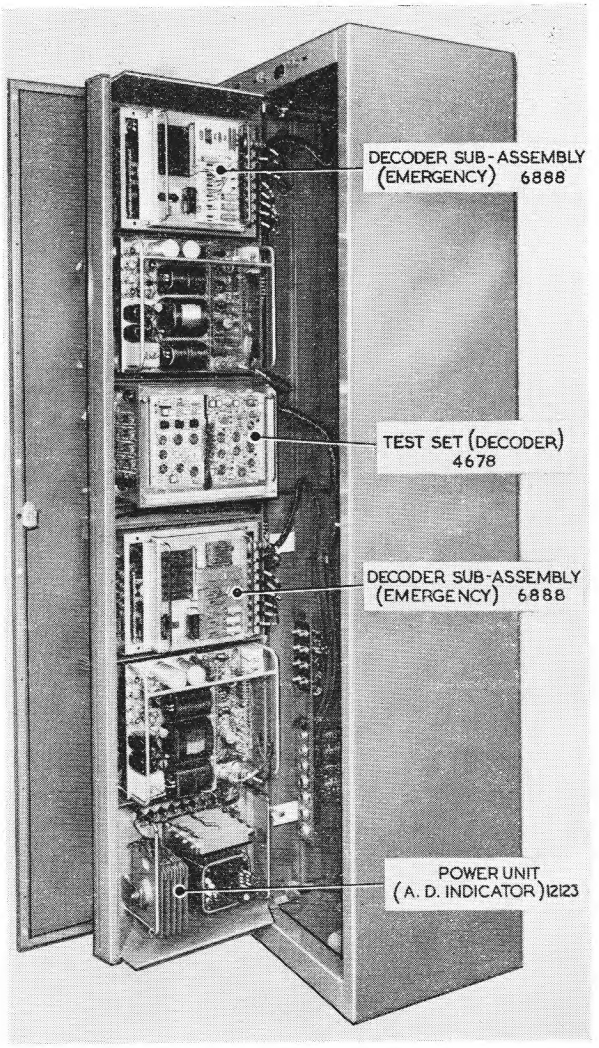


Fig. 4. Rack (mode 1 decoder) 12276, rear view of sub-frame

on this unit provide common control of all the operational and standby mode 1 decoders and enable the standby decoder to be switched into circuit in place of any one of the operational mode 1 decoders.

16. Transformers TR1 and TR2 (*fig.* 8) which are fitted in the rack are associated with the sync. pulse inputs. Two transformers are provided to permit the use of alternative synchronizing sources. The synchronizing waveform is taken from either PLA/1 or PLA/2 for test set 4678 and, via ASKE or ASKF, to rack (decoder) 4469.

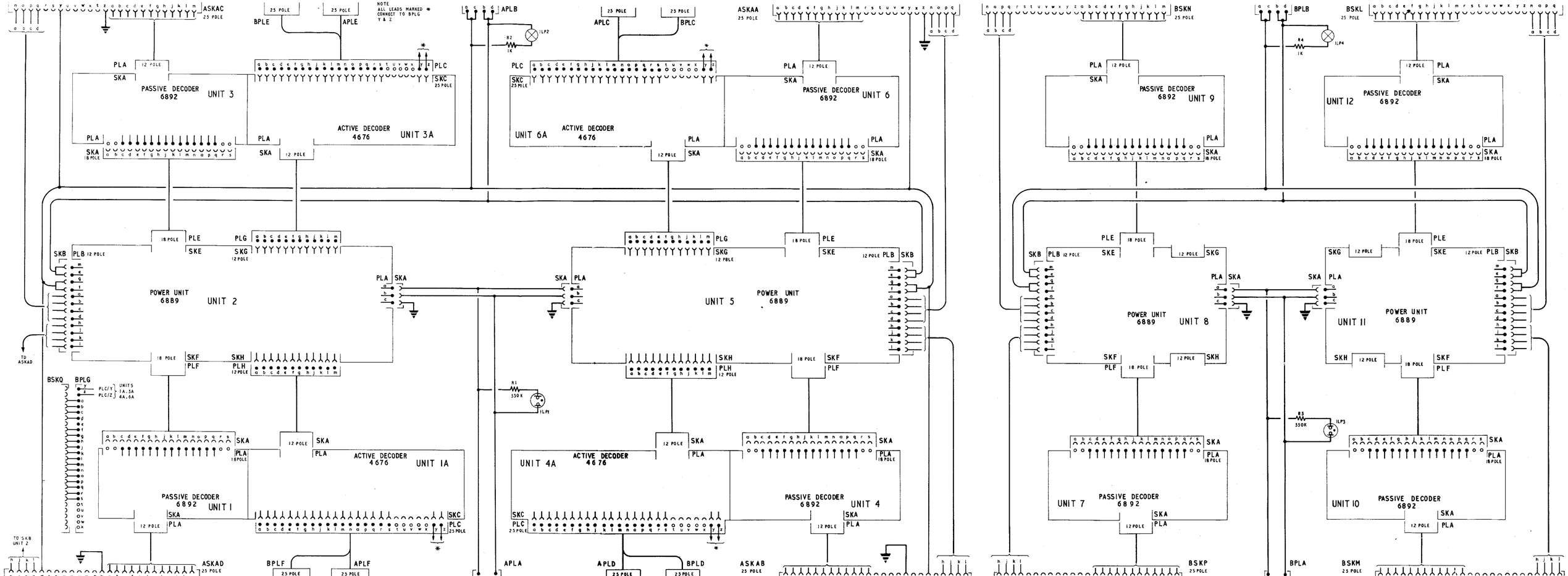


Fig.5

Rack (decoder) 4469 : interconnections (excluding coaxial)

924/8/7536/66528/631/2/62 J. T. & S.

Fig.5

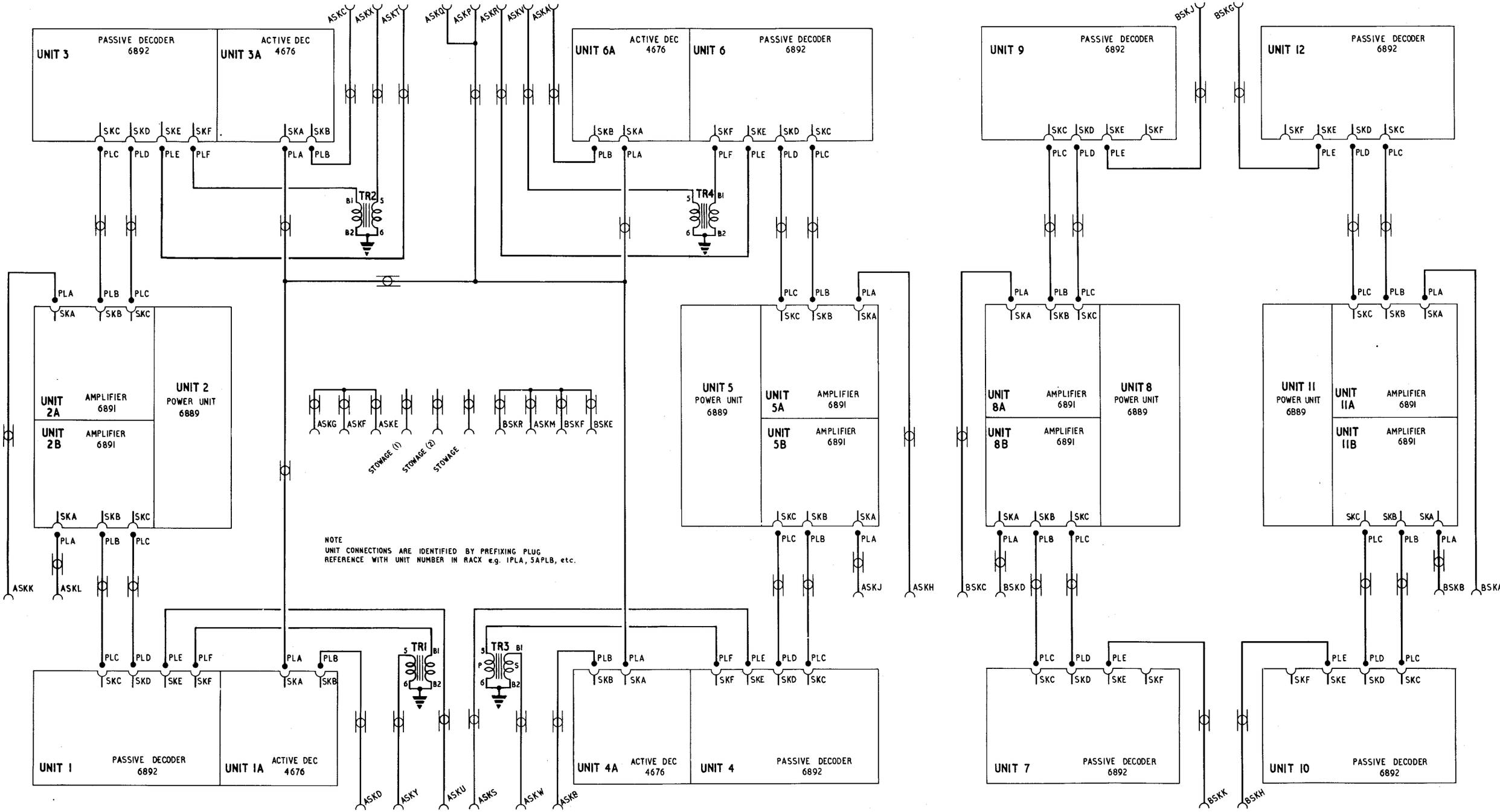


Fig. 6

Rack (decoder) 4469 : coaxial cabling

924/8/7536/66528/631/2/62 J. T. & S.

Fig. 6

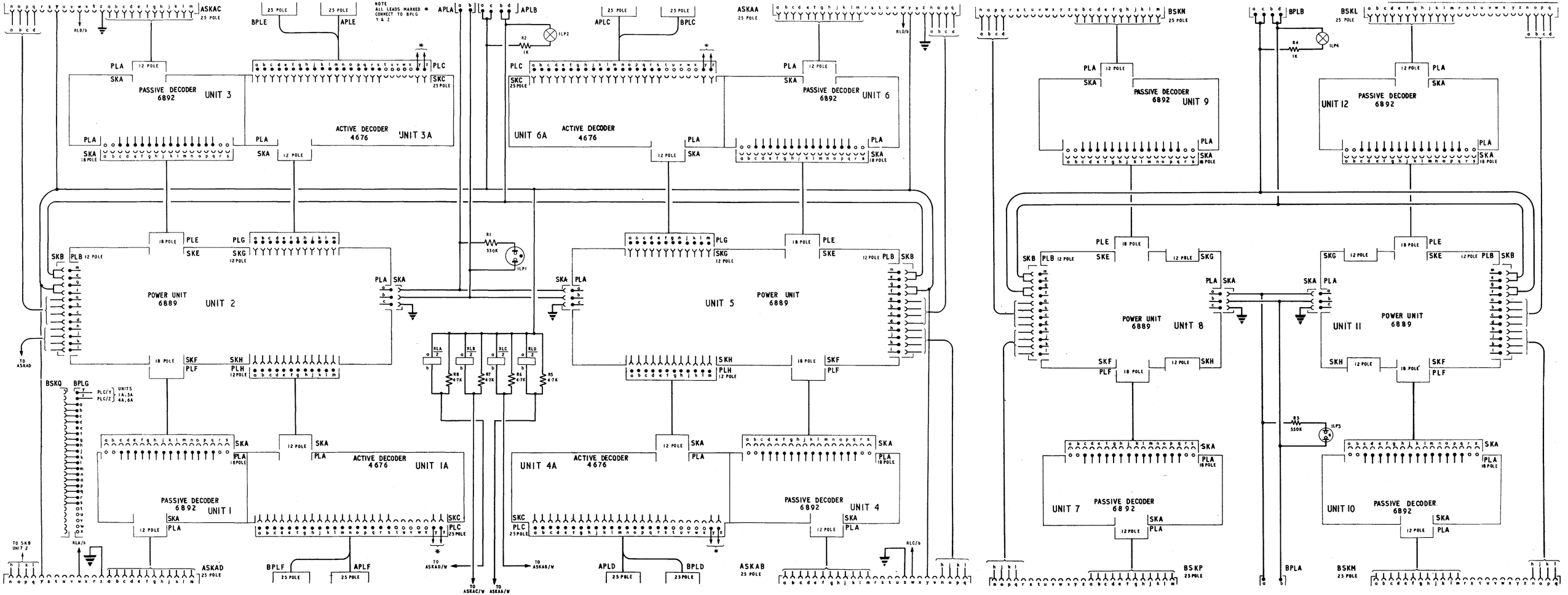
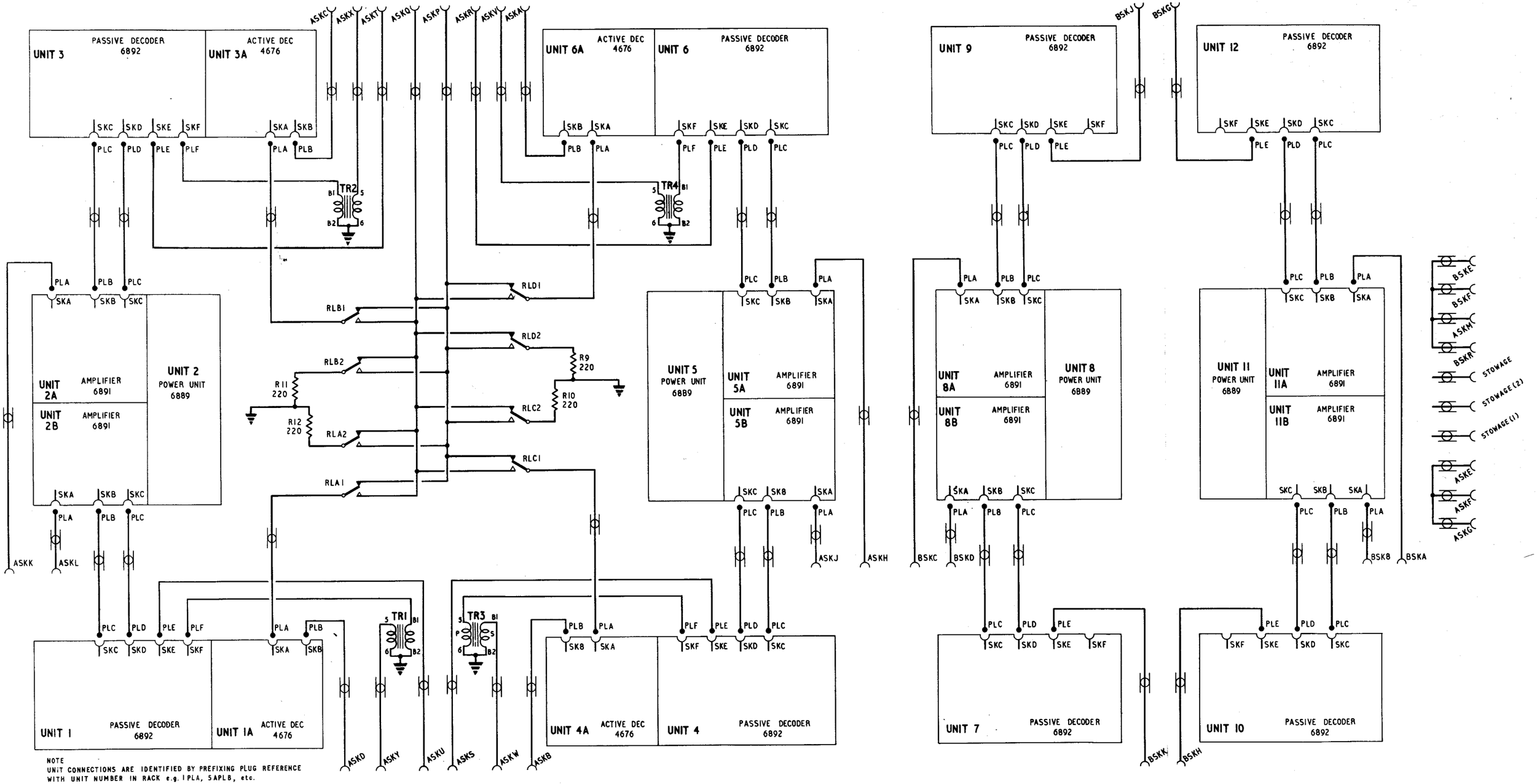


Fig.7

Rack (decoder) 4469A: interconnections (excluding coaxial)

Fig.7



NOTE
UNIT CONNECTIONS ARE IDENTIFIED BY PREFIXING PLUG REFERENCE WITH UNIT NUMBER IN RACK e.g. 1PLA, 5APLB, etc.

Fig.8

Rack (decoder) 4469 A: coaxial cabling

Fig.8

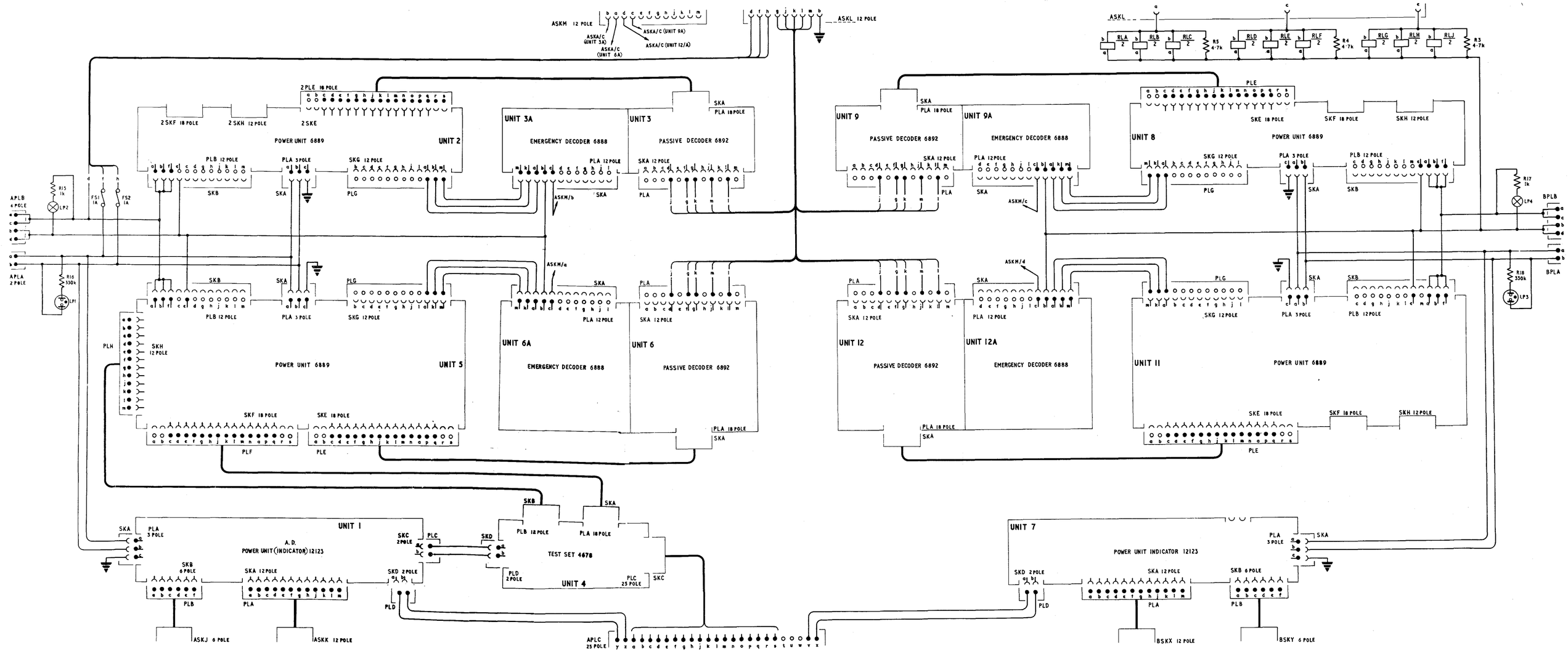
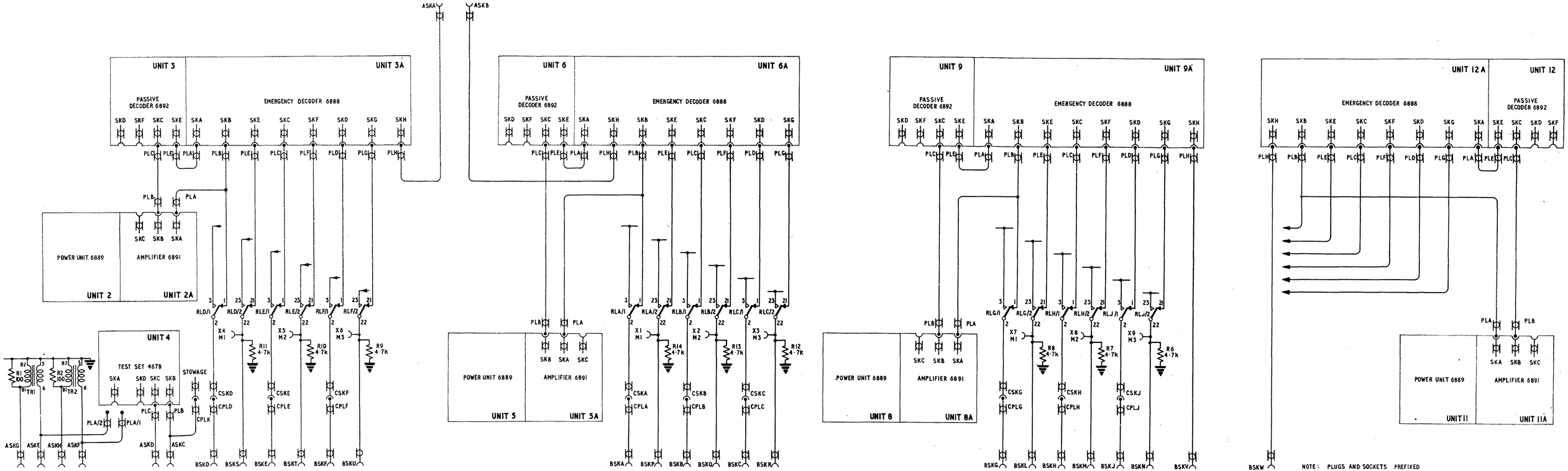


Fig. 9

D. 2118 470893 S.W. 2/65

Rack (mode I decoder) 12276 : interconnections (excluding coaxial)

Fig.9



NOTE: PLUGS AND SOCKETS PREFIXED A AND B ARE ON PLUG PANELS AT BASE OF RACK

Fig.10 D.2118 470893 S.W. 2.65

Rack (mode 1 decoder) 12276 : coaxial cabling

Fig.10

Chapter 3
AMPLIFIER (DECODER INPUT) 6891

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LIST OF ILLUSTRATIONS

General

1. Amplifier (decoder input) 6891 is one of the first units in the SIF decoding chain. Its function is to accept positive-going mode 2 or 3 code pulse trains and negative-going mode 1 or emergency decoded signals. Positive-going pulses are amplified and negative-going pulses are inverted and amplified. The resultant positive-going outputs are passed to the associated passive decoder.

2. The amplifier, illustrated in fig. 1 and 2, is a small sub-unit which is mounted on the chassis of power unit 6889. Since each power unit may supply two passive decoders, provision is made for it to carry two decoder input amplifiers but the number of units fitted is dependent on the application of the power unit. A power unit fitted in rack 4469 usually has two amplifiers. In the mode 1 decoder rack however, each power unit supplies one passive decoder and thus has only one input amplifier.

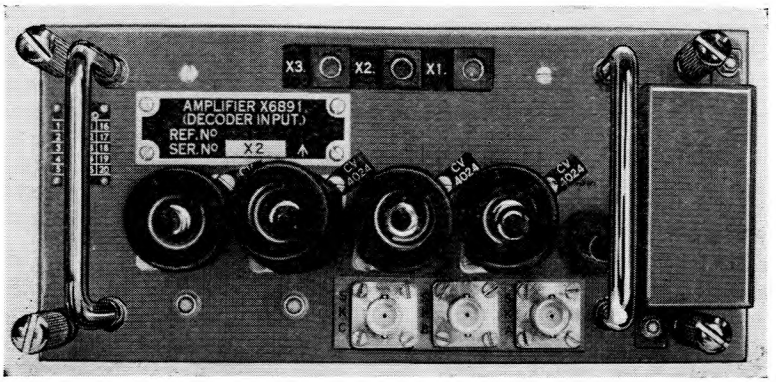

Fig. 1. Amplifier (decoder input) 6891 (front view)

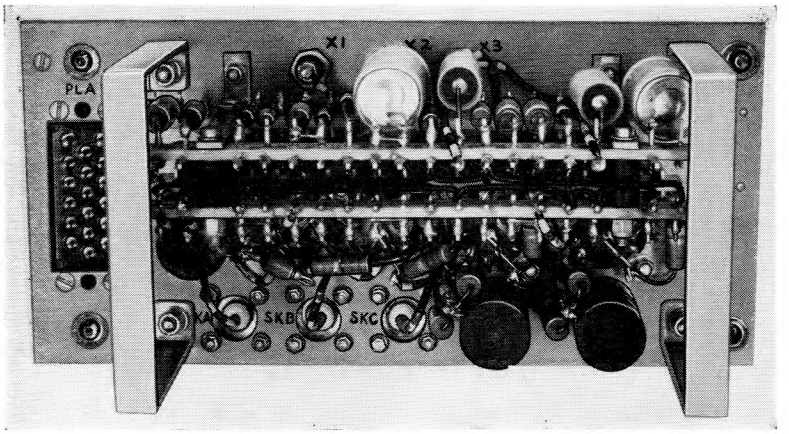

Fig. 2. Amplifier (decoder input) 6891 (rear view)

Circuit description

3. A circuit diagram of amplifier 6891 is given in fig. 3. Incoming signals, applied to the common input socket SKA, are passed to two very similar channels with separate outputs at SKB and SKC. Positive-going pulses at SKA cut off the diode MR1 but are passed by MR7 to V3a grid. Similarly, negative-going pulses at SKA cut off MR7 but are passed by MR1 to V1a grid.

4. Consider the application of a positive-going pulse to SKA. This is passed by MR7 to the grid of V3a which is one-half of a double-triode valve. V3a grid is returned to the junction of R27 and R28 and is held at about 4V. With the onset of the positive-going pulse (2 to 4V in amplitude) at V3a grid, the current through the valve rises sharply and the anode voltage falls. In V3a anode circuit is a short-circuited delay line DL2. Thus, when the anode voltage falls, a negative wave travels along the delay line to be reflected, with change of sign, at the short-circuit. The reversed voltage change returns to V3a anode and reduces to zero the voltage developed across R14. DL2 has a time delay of 0·25μs so that, provided the width of the input pulse is equal to or greater than 0·5μs, the negative-going pulse produced at V3a anode is 0·5μs in duration. When the input pulse is less than 0·5μs the duration of V3a anode waveform is nominally the same as that of the input.

5. The negative-going pulse appearing at V3a anode is fed to V3b grid which is held near earth by the limiting action of the diode MR6 on the grid potential produced by the current flowing through R17. MR5 is included to suppress the positive-going reflected input pulse due to the delay line in V3a anode circuit. V3b is a simple phase inverter and the pulse developed at the anode is applied to the grid of a cathode follower V4a. The positive-going output from V4a cathode is taken to SKB.

6. The second channel consisting of V1a, V2 and V4b is similar in operation, the main difference being that a phase inverter stage is included at the input. Thus a negative-going pulse at SKA is inverted by V1a to give a positive input to V2a. Due to the additional gain introduced by V1a, the signal at V2a grid is considerably greater in amplitude than that applied to V3a. In consequence V2a is biased to cut-off by returning the grid through R5 to −14V at the junction of R28 and R29. The operation of the circuit is exactly the same as described in para. 4 and 5, a positive-going output being obtained at SKC for a negative input at SKA.

7. The necessity for two separate channels is governed by the conditions under which the amplifier is employed. The alternative uses are shown in the block diagram (*Chap.* 1, *fig.* 2). In the simpler case, *i.e.* at the input of a mode 1 passive decoder, the amplifier input consists of positive-going mode 1 video pulses from waveform generator 6010. These pulses are passed by the channel consisting of V3 and V4a to SKB. The other channel is inoperative and there is no output at SKC.

8. When the amplifier is used before a mode 2/3 passive decoder however, the input waveform at SKA consists of positive and negative pulses fed from the associated relay unit 6009. The positive-going input is formed by the normal undecoded mode pulse trains but any negative-going pulses which may be present are produced by mode 1 responses in the following manner.

9. The video outputs in all three modes from the waveform generator are fed to decoder sub-assembly (emergency) 6888 which is a small sub-unit mounted on the mode 1 passive decoder. It contains a pulse separator together with three negative mixing circuits, one for each mode. Mode

◀1 signals (including any emergency signals) are also fed independently, via an amplifier 6891, to the mode 1 passive decoder which produces a single negative-going pulse for each pulse train received so that a decoded emergency response contains four pulses. The decoded mode 1 output is then fed into the emergency decoder and applied to both the pulse separator and mode 1 mixing circuits.

10. The function of the pulse separator is to separate decoded normal mode 1 responses from emergency signals and it thus delivers an output only when emergency pulse trains are present. In such an event the pulse separator output consists of the last three pulses of the four-pulse emergency train and these pulses are fed into the modes 2 and 3 mixing circuits. Thus the modes 2 and 3 outputs from the emergency decoder consist of undecoded positive-going video signals mixed with negative-going mode 1 emergency signals. The mode 1 output contains positive-going undecoded pulse trains, each followed by a positive-going decoded response.▶

11. The three outputs from the emergency decoder are passed to a relay unit 6009 through which the desired mode may be selected in the normal manner. From the relay unit the signals are fed direct to an amplifier (decoder input) 6891.

12. Thus, an input amplifier used before a mode 1 decoder has to accept undecoded mode 1 pulse trains only whereas a similar amplifier, preceding a mode 2/3 decoder, is required to give a decoded mode 1 output which is independent of the undecoded signal channel. This decoded output does not pass through the mode 2/3 passive decoder but is fed directly to the output circuit.

Power supplies

13. The input amplifier derives its power supplies from the power unit on which it is mounted and for this purpose an 18-pole plug is fitted to the right-hand side of the chassis. When the amplifier is inserted into the aperture in the power unit the plug engages with a socket and all the power connections are automatically made. Leads from the valve anodes are also routed via the plug to the monitoring sockets on the power unit so that the various potentials and currents can be measured.

Monitoring

14. To facilitate checking the waveforms under operating conditions, monitoring points X1, X2 and X3, coupled to the coaxial sockets, are provided on the front of the unit.

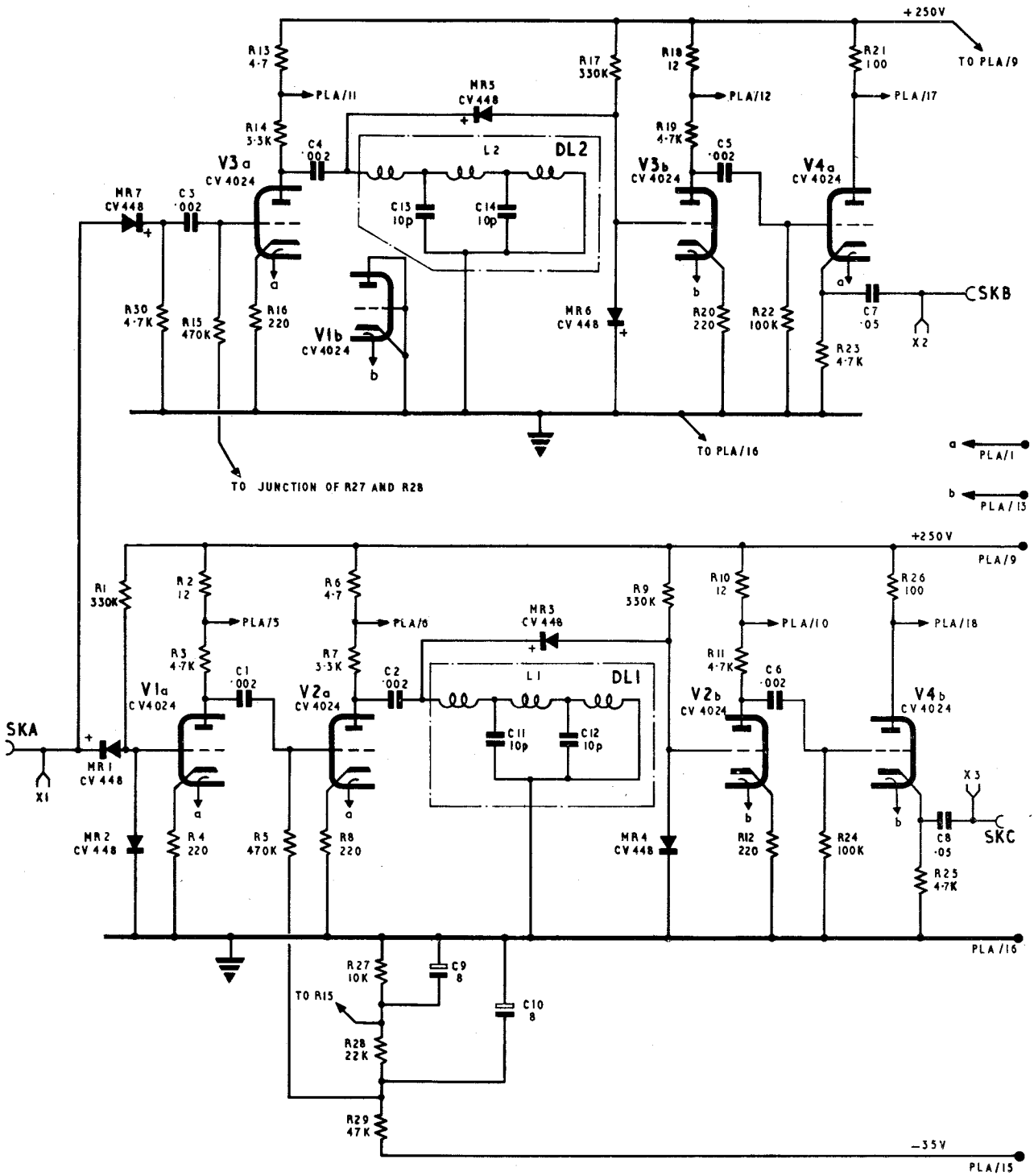

Fig. 3 Amplifier (decoder input) 6891: circuit Fig. 3

Chapter 4

DECODER, VIDEO (PASSIVE) 6892

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Introduction

1. Decoder, video (passive) 6892 is the main decoding unit in the SIF chain. Its principal function is to accept the code pulse trains and to produce a single pulse for each pulse train received. This single pulse is then fed to the console for display on the PPI. In addition, the passive decoder provides the necessary pulse train input to the active decoder.

2. The polarity of the decoder output pulse is determined by the conditions under which it is used. Mode 2/3 decoders deliver a positive-going pulse, but mode 1 decoders are required to give a negative output. Since all decoders are identical, the change is effected by reversing the connections to the output pulse transformer.

3. The number of passive decoders required in a given installation is governed by the number of radar heads and consoles. Since mode 1 is the general identification mode and is also the channel for emergency signals, it is common to all consoles and one passive decoder is used with each radar head. The control unit for the mode 1 decoder is located in the radar office. Mode 2/3 passive decoders may be used on a scale of one per console; alternatively, several consoles may share one decoder. In the first event each console is provided with a mode 2/3 control unit.

4. Whereas a mode 1 passive decoder is fed with mode 1 signals only, a mode 2/3 decoder has to accept undecoded video in any one of the three modes. This facility to select undecoded mode 1 video by the mode 2/3 decoder is necessary for the ALL SIGNALS display, to permit mode 1 bracket decoding when required and to provide mode 1 input to the active decoder. For the mode 1 ONE CODE display, the decoded mode 1 normal and emergency signals from the mode 1 passive decoder are fed direct to the mode 2/3 decoder output circuit.

5. The desired mode is chosen by the mode selection switch on the console in the normal manner, but the method of using the mode 2/3 passive decoder is determined by the setting of a switch on the associated console control unit and the decoder may be operated in any one of three ways:

ALL SIGNALS. All IFF signals in all three modes are fed into the decoder but bypass the decoding circuits so that they appear at the output unchanged and are passed to the display.

ONE CODE. Provided the correct code has been selected, the passive decoder decodes the SIF trains received and delivers a positive-going output pulse for each code group. If the correct code is not selected there is no output.

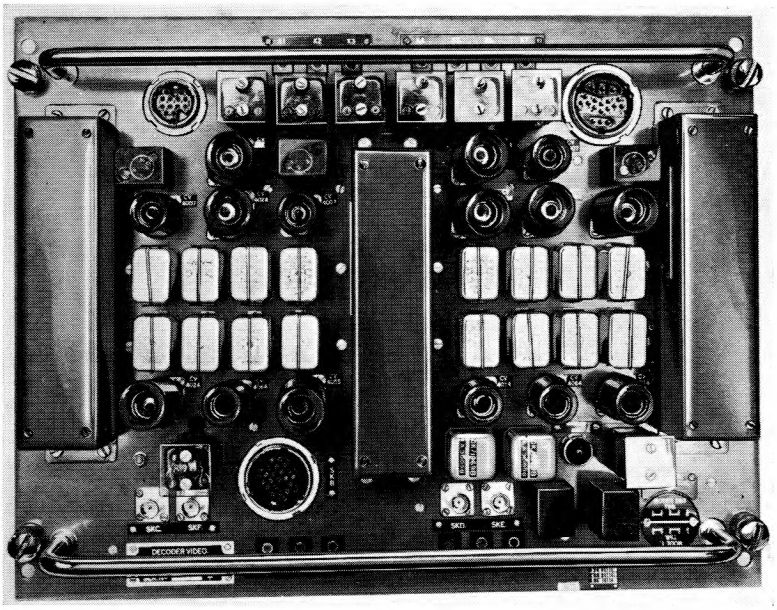


Fig. 1. Decoder, video (passive) 6892: front view

ALL CODES. The passive decoder decodes the code train bracket pulses only and, provided these pulses are present at the correct spacing, will give a single positive-going pulse out.

GENERAL DESCRIPTION

Construction

6. General views of the passive decoder are given in fig. 1 and 2. It consists of a box-form chassis which is mounted vertically in the rack, captive screws securing it to the rack sub-frame. The valves, relays, delay lines and plugs and sockets are mounted on the outer face of the chassis which forms the panel. The remaining components, consisting of capacitors and resistors, are located at the rear. To facilitate installation and removal of the unit, handles are provided.

Principles of operation

7. A block diagram of the unit is given in fig. 3. The input pulse train from amplifier (decoder input) 6891 is first fed to a pulse-shaping circuit consisting of a pulse-forming delay line giving a pulse length of 0·75μs, followed by an amplifier and a cathode follower. From this circuit the pulse train is passed to a delay unit 6890 with a total delay of 7·25μs.

8. From the end of the first delay unit 6890 the pulse train is fed through another shaping and amplifying circuit similar to the first and then to a second delay unit 6890. This is followed by a third shaping circuit and delay unit. The total delay is thus 21·75μs or 1·45μs more than the delay required for decoding a pulse train. *viz* 20·3μs. The additional delay of 1·45μs is intro-

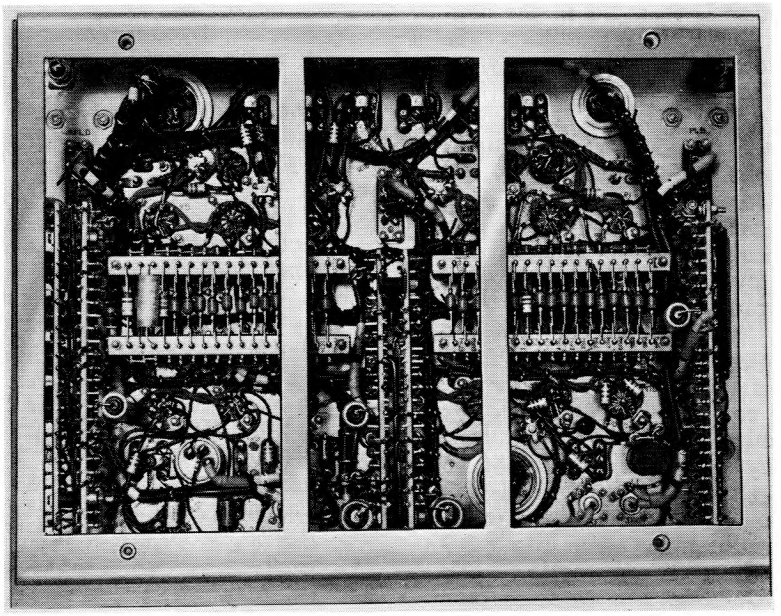


Fig. 2. Decoder, video (passive) 6892: rear view

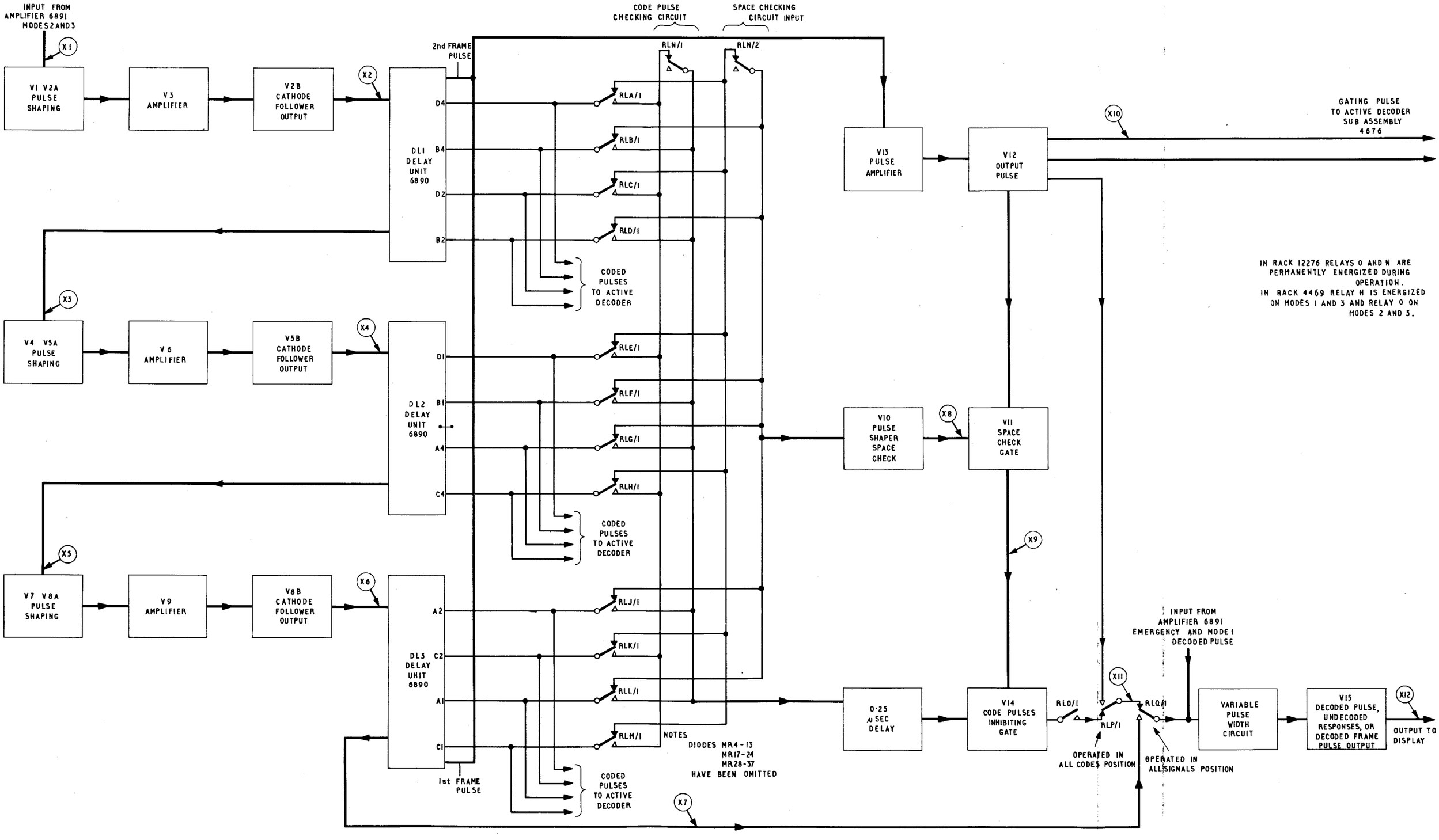


Fig. 3

Decoder, video (passive) 6892: block diagram

duced to facilitate mixing decoded emergency signals with the undecoded mode 2/3 responses and prevents the pulses being superimposed upon each other (*Chap.* 6).

9. Each delay line is tapped at intervals of 1·45μs. The outputs from the various tappings are fed, via contacts on the code selection relays and crystal diodes, to the decoding circuits. They may also be applied to the active decoder. The code selection relays have changeover springsets so that, in the de-energized condition, the pulses are fed to the space check circuit. When operating on modes 1 and 3, the unwanted tappings are disconnected through the contacts on relay N.

10. The frame (or bracket) pulses from the delay units are fed to crystal diode gates. Provided both pulses are present, the diodes pass a pulse to a pulse amplifier (V13). The output from V13 is fed to V12 whose output is used to gate the active decoder and space check circuit. In the ALL CODES position of the console control switch, V12 output is fed to the decoder output circuit and passed to the display. Although not shown in fig. 3, each bracket pulse is taken from two separate tappings on the delay line. The earlier tappings provide the input which produces the gating pulse and the ALL CODES display. The later tappings are used for pulse checking purposes in the ONE CODE condition.

11. The information pulses, appearing at the appropriate tappings on the delay lines, are similarly applied to crystal diode gates but, for a decoded output to be obtained, the bracket pulses must also be present to serve as a pulse check. In the ONE CODE position of the console switch a single pulse is passed by the diode gates to V14, provided the correct code has been selected. On mode 2 and mode 3 operation, the output from V14 is fed to the decoder output circuit. Should the selected code be incorrect, so that a space appears in place of a pulse, there is no output from the diode gates.

12. In the de-energized condition of the code selection relays, the outputs from the delay line tappings are fed, via the relay contacts, to the input of the space check circuit. Every pulse fed into the delay line will appear at each tap in turn as it travels along the line and will thus produce a pulse train at V10 input.

13. When a code is selected, the appropriate relays are energized and the information and bracket pulses are decoded. However, the unused tappings are still coupled to the input of the space check circuit. If the correct code has been selected so that pulses and spaces appear at the correct points on the delay line, there will be no output from the space check gate. Should the code be wrong, causing a pulse to appear where there should be a space, then at one point the error pulse will coincide with the output pulse from V12. As a result, the space check gate will produce an output and this is used to close the code pulse coincidence gate.

CIRCUIT DESCRIPTION

Pulse shaping circuits

14. The input to the passive decoder consists of a train of pulses, each pulse being 16V in amplitude and having a nominal duration of 0·5μs. However, the shaping circuit in the decoder input amplifier is essentially a clipping circuit in that it reduces to 0·5μs all pulses of greater length but has no effect on pulses less than 0·5μs. Since the length of the pulses radiated by the airborne transponder may lie anywhere between 0·35 and 0·55μs it will be seen that pulses of less than 0·5μs may appear at the decoder input. These narrow pulses have a large high frequency component and, in their passage through the decoding circuits, may suffer distortion. Additionally, a train may contain the two bracket pulses alone or the bracket pulses plus any number of information pulses up to the maximum of twelve. Thus, with input pulses of less than 0·5μs and subsequent distortion, it would be possible for some of the later pulses in the train to be lost altogether, rendering accurate decoding impossible. To overcome this difficulty the input circuit of the decoder is arranged to deliver a flat-topped pulse of constant length and amplitude to the later circuits.

15. The pulse train is fed in at SKC (*fig.* 8) and thence to a shaping circuit consisting of a pulse-forming delay line, a pulse amplifier and cathode follower. In the no-signal condition, the input diode MR1 is conducting and a current of approximately 5mA is flowing through R5, MR1 and the source impedance. There is no voltage drop across R2 and the grid of the cathode follower V2A is effectively at −13V.

16. With the arrival of a positive-going pulse at SKC, MR1 is cut off and the current through R5 is diverted, part flowing through C1 and R2. The remainder of the current flows through the diode V1A which thus limits the positive excursion at earth. MR2 now conducts in turn and V2A grid rises to earth.

17. The positive-going input pulse is also developed across the primary winding of a pulse transformer TR1 whose secondary is coupled to a delay line DL1 terminated in its characteristic impedance by R1. The pulse is inverted in polarity in TR1 and a negative pulse travels along the delay line. DL1 has a time delay of 0·75μs and its output is applied to the cathode of a diode V1B. Thus, 0·75μs after V2A grid has risen to earth, V1B conducts and V2A grid is driven negative, being limited at −13V by the action of the diode MR3.

18. The cycle is repeated for each input pulse so that the waveform developed at V2A cathode consists of a train of pulses, each pulse being 0·75μs in duration. V2A cathode is direct-coupled to the input of a pulse amplifier stage V3, which is a double-triode valve with both sections connected in parallel and having the primary winding of a pulse transformer TR2 as the anode load. From TR2 secondary the output is fed to a cathode follower V2B. To prevent ringing of the transformer winding, a damping resistor R8 is connected across the secondary.

19. V2B output, consisting of a train of 0·75μs pulses, between 50 and 55V in amplitude, is used to drive the first delay unit 6890. The delay unit is a normal LC network with a total delay time of 7·25μs and is tapped at intervals of 1·45μs. From these tappings the pulses are applied to the space check circuit or, when the code selection relays are energized, to the appropriate diode gates.

20. Due to the attenuation of the delay line, the pulses are progressively reduced in amplitude as they travel along it with the result that, at the end, the amplitude has fallen to approximately 25V. The output from the first delay unit (DL4) is fed into another shaping and amplifying circuit similar to that described in para. 15 to 18 and this, in turn, drives the second delay unit 6890. The output from the second delay unit is applied to a third shaping and amplifying circuit driving the third delay line. The three circuits in cascade thus afford a total delay of 21·75μs. ◀Some part of the delay inevitably occurs in the shaping circuits and, to compensate for this, the delay in the first section of each delay line is about 0·2μs less than the nominal value.▶ Since the output loading of the third delay unit is less than in the other two circuits, the pulse amplitude at DL6 output is approximately 35V.

Bracket pulse decoding

21. It will be noted that two separate bracket pulse outputs are taken from DL4 and DL6. This is necessary because the bracket pulses are employed in three different ways. In the ONE CODE position of the control switch, the bracket pulses are included with the information pulses to check that the correct pulses are present. With ALL CODES operation, the bracket pulses alone are decoded and, after passing through V13 and V12, provide the PPI display. However, the output from V12 is also used to gate the active decoder which is fed with code pulses directly from the delay line tappings. If the bracket pulses were taken from the same points on the delay line for all purposes there would, due to the amplifying circuit formed by V13 and V12, be a small time delay between the code pulses and the gating pulse fed to the active decoder. To ensure coincidence between code and gating pulses, the bracket pulses fed to V13 are taken from slightly earlier tappings on DL4 and DL6.

22. For bracket pulse decoding the pulses are taken off points just before the first tap on DL4 and the end of DL6 and applied to the cathodes of crystal diodes, MR4 and MR33. The diode anodes are connected together and taken to +250V through R31. Considering the simplified diagram of fig. 4, a current of approximately 2·5mA flows through both diodes to earth, via the delay line terminating resistors, with the result that point (a) is slightly above earth potential.

23. If a positive-going pulse appears at either point on the delay line, the corresponding diode will be cut off but no change will occur in the potential at (a) since the other diode still provides a conducting path. However, when the first bracket pulse has reached the end of the delay line, the second bracket pulse will arrive at the first tapping because the delay line length is equal to the bracket pulse spacing. During the overlapping period, ideally 0·75μs, both diodes will be cut off and the current will then be diverted through C9 and R33, causing a pulse voltage to be developed across the resistor.

24. V13 and V12 form a normal two-stage transformer-coupled pulse amplifier. In the no-signal condition the control grids of both valves are returned to negative potentials so that anode current is cut off. When the positive pulse from the diode gate is applied to V13 grid, the valve conducts and a negative-going pulse is developed across the

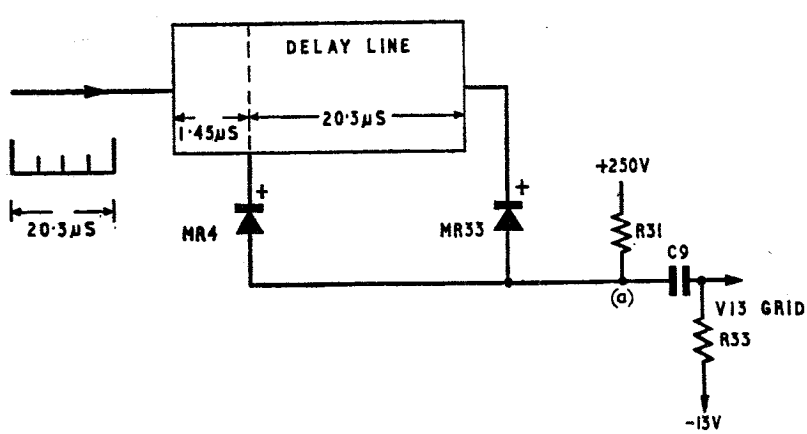


Fig. 4. Bracket pulse decoding: simplified diagram

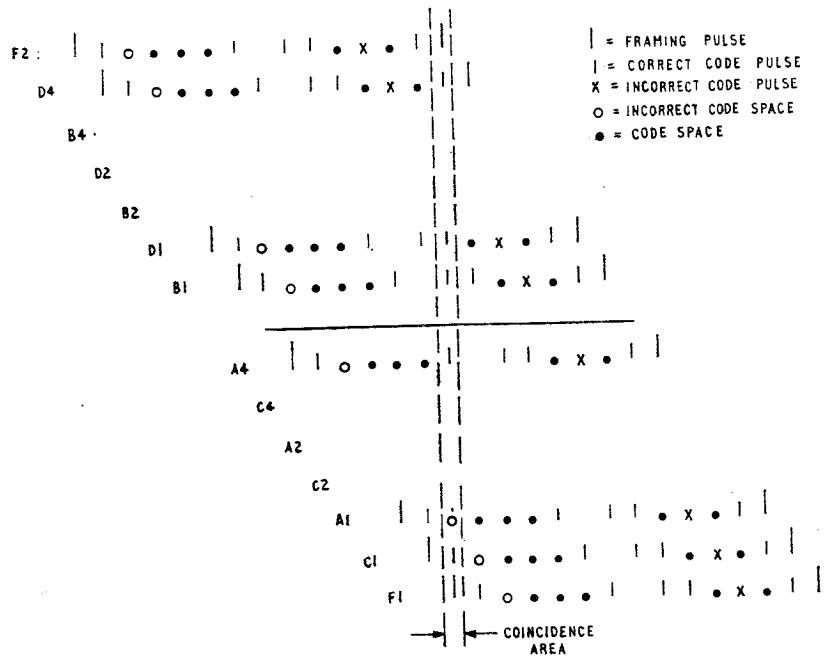


Fig. 5. Pulse check circuit input

primary of transformer TR8. This pulse is inverted in the transformer and fed to V12, which then conducts. The pulse appearing at V12 anode is again inverted in TR7.

25. TR7 has two secondary windings, one of which delivers the positive-going gating pulse to the active decoder. The output from the other winding is fed to contacts on relay P and also, via R44, to the suppressor of the space check gate valve V11. When the console control switch is set to ALL CODES, relay P is energized, with the result that the waveform representing the decoded bracket pulses is fed into the decoder output circuit.

Information pulse decoding

26. The information pulses are decoded in the same manner as the bracket pulses. When the code selection relays are energized, the change-over contacts switch the delay line tappings to the cathodes of the appropriate crystal diodes whose anodes are taken to +250V through R85. In addition, however, it will be noted that the bracket pulses are taken from the second tapping on DL4 and the end of DL6 and coupled through MR5 and MR32. In this application the bracket pulses are used as a pulse check of the complete train. The conditions are thus similar to those illustrated in fig. 4 with the sole difference that, in place of only two diodes, there are now three or more, depending upon the number of information pulses in the code train. Provided all the incoming pulses (including the bracket pulses) are present, all the diodes will be cut off so that current flows through C10 and R37, causing a pulse voltage to be developed at V14 grid. If, for any reason, one or more of the pulses is missing, the corresponding diode or diodes will not be cut off and no pulse will appear at V14 grid.

27. The conditions for one particular code are shown in fig. 5 in which the coincidence area represents the instant when the entire train is contained within the delay line. When the relays corresponding to the delay line tap positions C1, A1, A4, B1, D1 and D4 are energized, a pulse must be present at each of these positions (and also at both bracket positions) within the coincidence area to allow a single pulse to be passed to V14. It should be noted that error pulses occurring elsewhere in the code train do not affect the action of the circuit.

28. The single pulse produced by the decoding operation is fed to V14 grid via a delay line DL7. This introduces a small delay of the order of 0·25μs and its purpose is to ensure that, if an inhibiting pulse from the space check circuit appears at V14 suppressor, the valve is cut off before the grid voltage can rise. Since the leading edges of the pulses have a finite rise time, any tendency for V14 grid voltage to change before the valve is cut off on the suppressor might produce a spike at the anode.

29. V14 serves as a pulse amplifier for the decoded pulse train and also as a gating stage, inhibited by the negative pulse which may be fed to the suppressor from V11. In the no-signal condition, the valve is cut off by the negative bias applied to the control grid. The positive-going pulse from the code pulse gate, fed to the grid, causes the valve to conduct and a negative pulse is developed at the anode. This pulse is inverted in polarity in TR9 and fed, via contacts on relays O, P and Q, to the decoder output circuit. With the control switch set to ONE CODE, relay O is energized with the result that a positive-going pulse is passed to V15.

Space check circuit

30. It has already been shown (*para.* 26 *and* 27) that the circuit which decodes the information pulses also checks that all the pulses are present. It cannot, however, discriminate between wanted and unwanted pulses and, for this purpose, a space check circuit is included.

31. In the de-energized condition of the code selection relays, the information pulse tappings on the delay line are taken to the anodes of crystal diodes. The diode cathodes are connected together and returned to a common point at the junction of C16 and R42.

32. The space check circuit is similar to the first channel of the decoder input amplifier (*Chap.* 3, *para.* 4 *and* 5) and operates in the same manner. Any positive-going pulse which appears at V10A grid causes a positive-going 0·5μs pulse to be developed at V10B anode. In place of a triode cathode follower, however, the space check circuit output stage is a pentode used as a coincidence gate valve. The pulse from V12, produced by decoding the bracket pulses, is fed to V11 suppressor. If this gating pulse coincides with a pulse at V10A control grid, a negative-going output is obtained from V11 and employed to cut off V14.

33. When a code is selected, the corresponding relays are energized and the appropriate tappings on the delay line are coupled to the information pulse decoding circuit. All the other tappings remain connected to the input of the space check circuit. Every pulse fed into the delay line will appear at each tap in turn as it travels along the line and will thus produce a train of pulses at V10A grid, but this train will consist only of pulses appearing at the tappings which are not connected to the decoding circuit.

34. The operation of the circuit may be more easily followed by studying fig. 6 which represents the space check conditions for the same code as that illustrated in fig. 5. It will be seen that, when the relays corresponding to the delay line tap positions C2, A2, C4, B2, D2 and B4 are de-energized, a pulse appearing at any one of these positions during the period of the frame pulse coincidence gate will cause V11 to conduct and produce a negative output pulse.

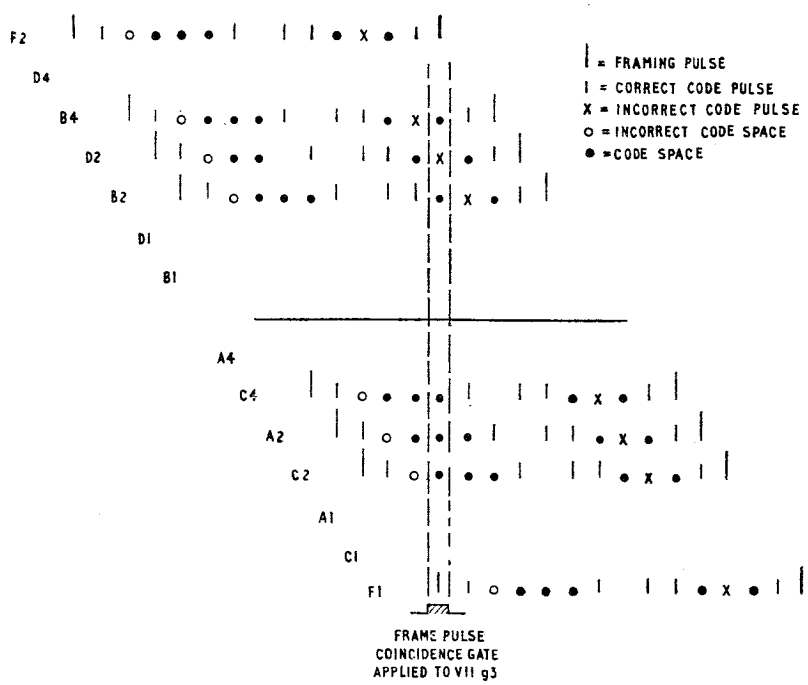


Fig. 6. Space check circuit input

35. V11 is normally cut off by the negative bias applied to both control and suppressor grids. If a pulse arrives at the control grid simultaneously with the gating waveform at the suppressor, VII draws current and the anode voltage falls. The negative waveform appearing at the anode is fed, via C14, to the suppressor of V14 and cuts off that valve, thereby preventing wrong information being passed to the output circuit.

Output stage

36. The output stage of the passive decoder consists of a pentode pulse amplifier V15 with the

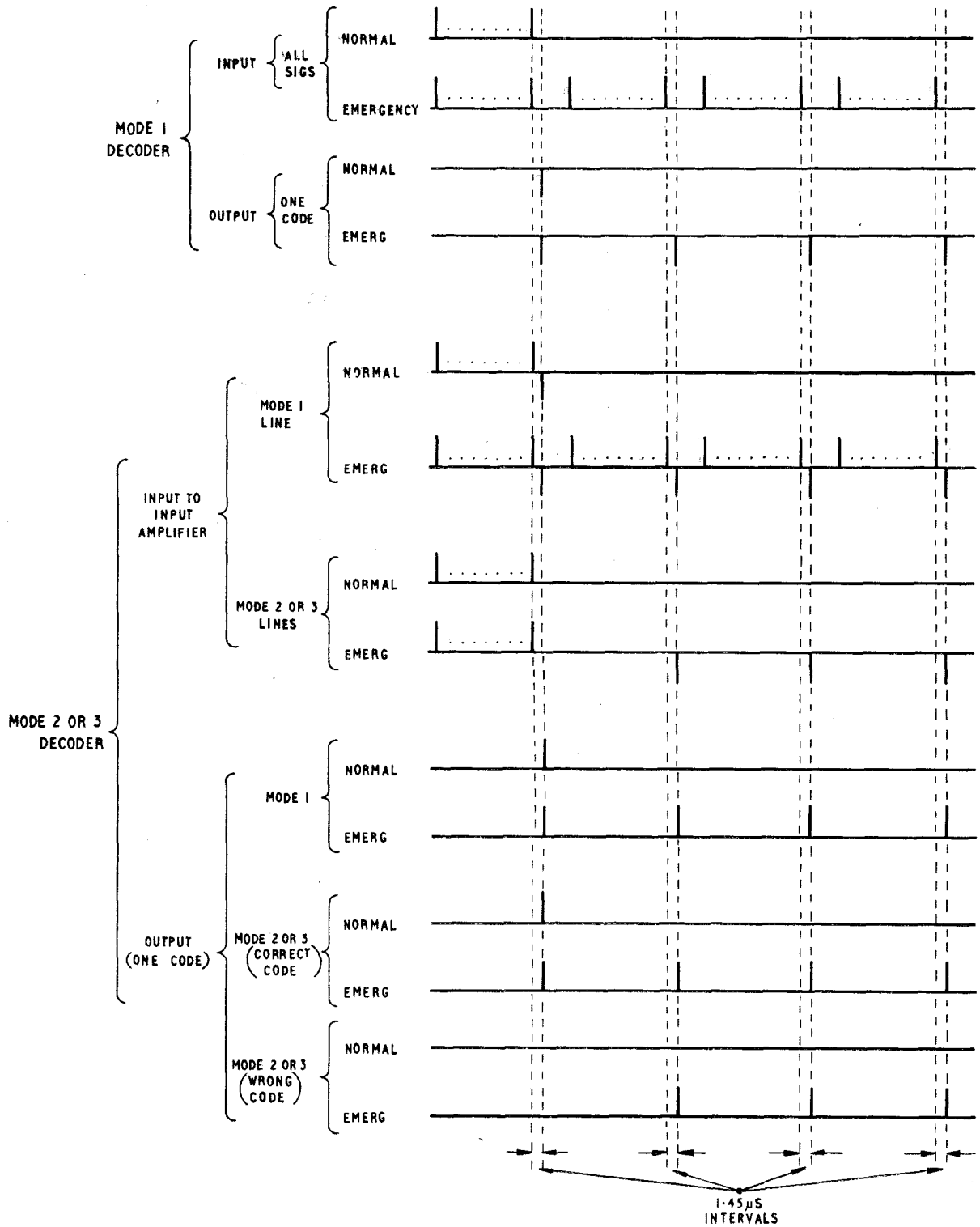


Fig. 7. Input/output pulse timing

primary of a pulse transformer TR10 as the anode load. V15 is normally cut off by the negative bias applied to the control grid. The input is derived from three sources, fed via a crystal diode mixer circuit formed by MR39, MR40, MR46 and MR50.

37. The primary purpose of the mode 2/3 passive decoder is to decode mode 2/3 pulse trains but facilities are included for the display of both mode 1 and uncoded signals. Decoded mode 1 pulse trains and emergency signals (if present) are fed in at SKD and, through the mixer circuit, to V15 grid. Thus, for mode 1 ONE CODE operation, the output from the mode 1 decoder is fed, via the mode 2/3 decoder output stage, direct to the display. With the control switch set to ALL SIGNALS, relay Q is energized and V15 input is taken from the end of the delay line. The resultant display will contain all IFF signals, whether coded or not, in the selected mode.

38. When the control switch is set to ALL CODES, relay P is energized so that V15 input is the single pulse produced by decoding the bracket pulses. At this switch setting the bracket pulses can be decoded for any one of the three modes. The input applied to SKF and the manual gain control RV1 consists of the active decoder marker pulse. It is mixed with the ALL CODES input at V15 grid and the composite signal is passed to the display.

39. The input network consisting of DL8 and the diodes MR47, MR48 and MR49 is included to meet circumstances where the length of the output pulse is considered inadequate. The nominal pulse length is 0·75μs and may even be slightly less. By short-circuiting the links shown, the output pulse can be stretched by increments of approximately 0·25μs, thereby enabling a maximum length of about 1·5μs to be obtained. No provision is made for easy variation of the pulse length and the facility is intended for use only when essential.

40. To meet the requirements for mode 1 operation, the connections to TR10 secondary are brought out to a tagstrip on the front of the unit. As shown in fig. 8 the connections may be arranged to give either positive or negative output as required.

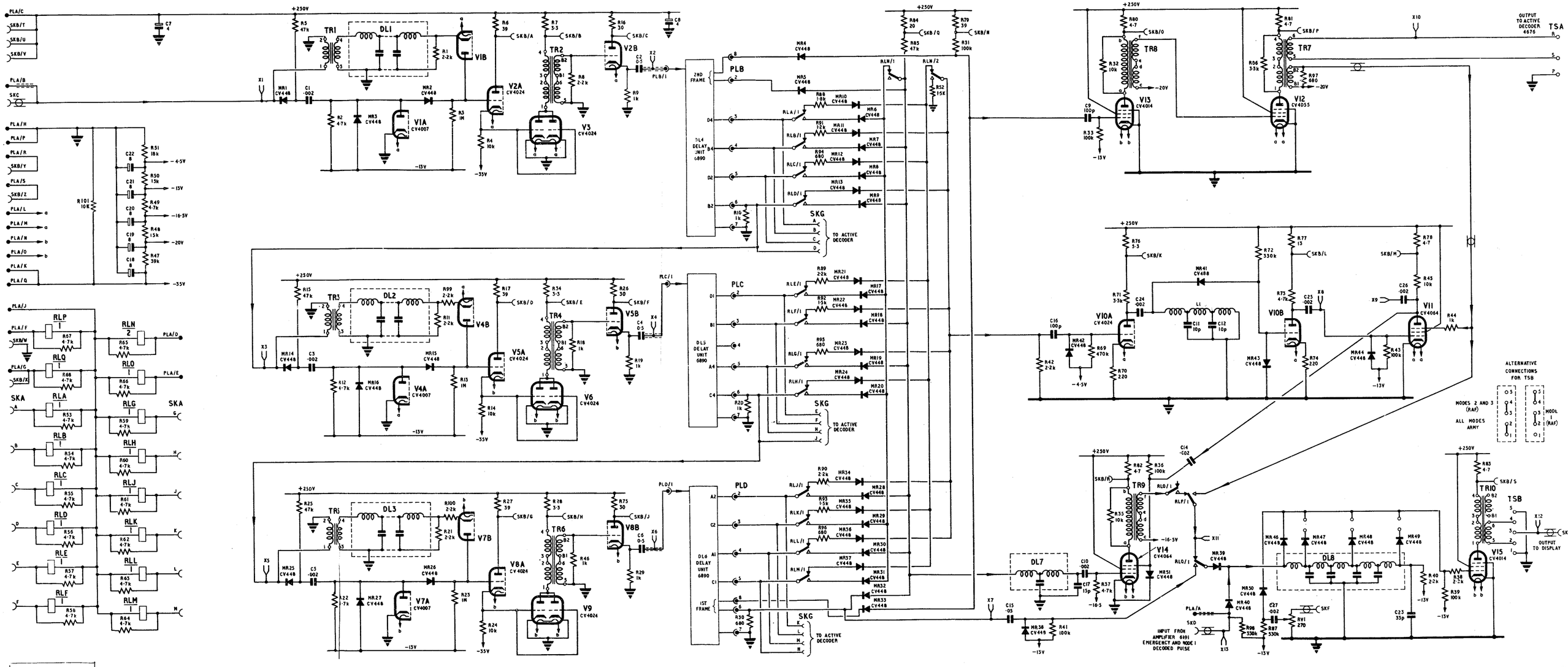
◀**41.** Fig. 7 illustrates the relative timing of the input and output pulses of the passive decoder and shows how the additional 1·45μs delay facilitates mixing of the decoded mode 1 emergency signals with the normal mode 2/3 responses.▶

Monitoring

42. To facilitate servicing and checking of the unit under operating conditions, numerous monitoring sockets are available for waveform observations.

Power supplies

43. The passive decoder derives all its power supplies from power unit 6889 described in Chapter 5.



Decoder, video (passive) 6892 . circuit

Fig. 8

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Appendix 1

DECODER VIDEO PASSIVE 5840-99-142-9183

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LIST OF ILLUSTRATIONS

Introduction

1. The decoder video passive 5840-99-142-9183 is similar to the decoder video passive 6952 described in Section 4 Chapter 4, but provides output pulses variable between 0·45μs and 6μs for acceptance at certain stations where the display equipment is designed to accept pulses of 2μs duration.

Description

2. A scrap view of the modified output stage is shown in fig. 1. VT1, VT2 and their associated components form a monostable circuit. The trimmer capacitor C1 facilitates variation of the output pulse width. The output from the monostable is fed to the display stage via an emitter follower VT3. The output from VT3 is a positive pulse variable between 0·45μs and 6μs at an amplitude of 13·5V to 17V.

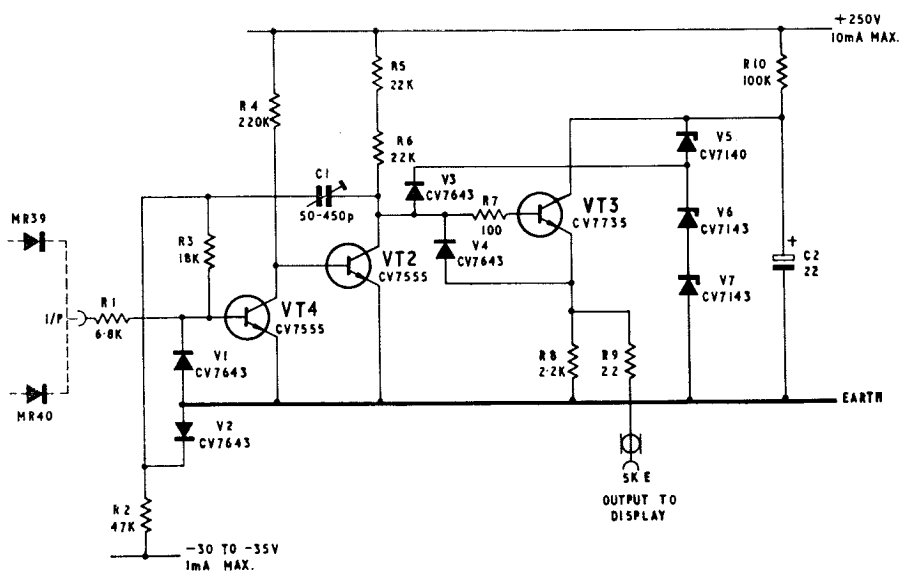

Fig. 1. Decoder video passive 5840-99-142-9183: output circuit scrap view

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Chapter 5

POWER UNIT 6889

(This chapter supersedes Chapter 5 issued with A.L. 25)

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LIST OF ILLUSTRATIONS

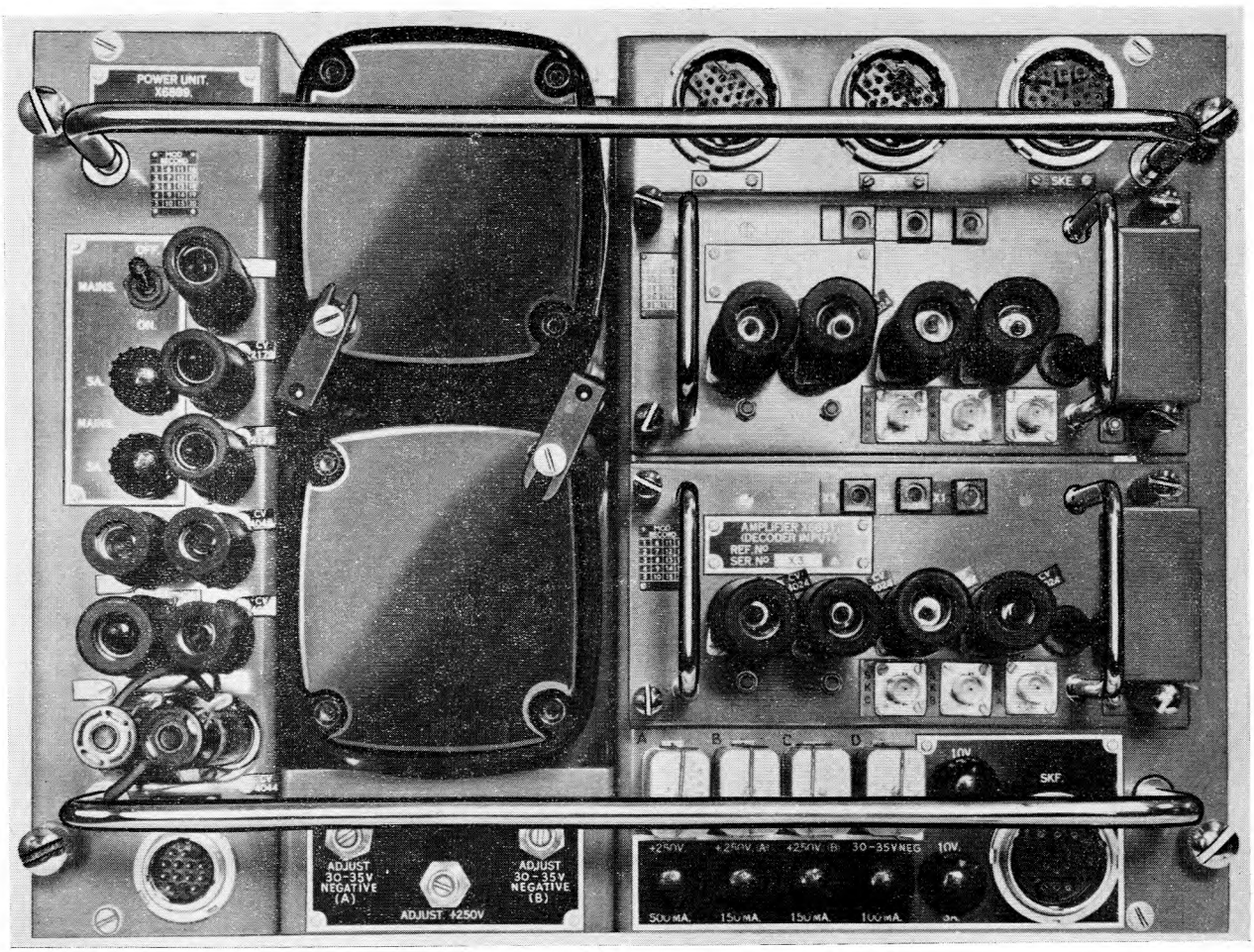


Fig. 1. Power unit 6889: front view

General

1. Power unit 6889 is designed for mounting in any of the SIF racks 4469, 12276, 12807 or 12808 and delivers the various potentials required by the decoding units. It operates from the 230V 50 c/s single-phase supply and, in addition to the normal heater and h.t. voltages for the valves, provides suitable positive and negative lines for the transistor circuits.

2. Each power unit is capable of operating more than one decoding unit and can supply two passive decoders 6892, two active decoder sub-assemblies 4676 and two decoder input amplifiers 6891. Alternatively, it can be used to supply a passive decoder, a test set 4678, an emergency decoder sub-assembly 6888 and an input amplifier. The group of units and sub-units associated with any one power unit is determined by the particular rack assembly in which the equipment is installed.

3. General views of the power unit are given in fig. 1 and 2. It consists of a tubular steel framework supporting a chassis on which the components are mounted. The chassis also forms the panel and is mounted vertically in the rack, captive screws securing it to the rack sub-frame. Cut-outs in the chassis are provided for the decoder input amplifiers. When only one amplifier is fitted, the second opening is covered by a panel (stowage) 12743.

Circuit description (*fig.* 3)

+250V stabilized supply

4. The 230V 50 c/s single-phase supply is brought in on pins A and B of the 3-pin plug PLA and is fed via the main on/off switch SWA and fuses FS1 and FS2 to the primary winding of transformer T1 and that of T2. A thermal fuse is included in the primary circuit of each transformer

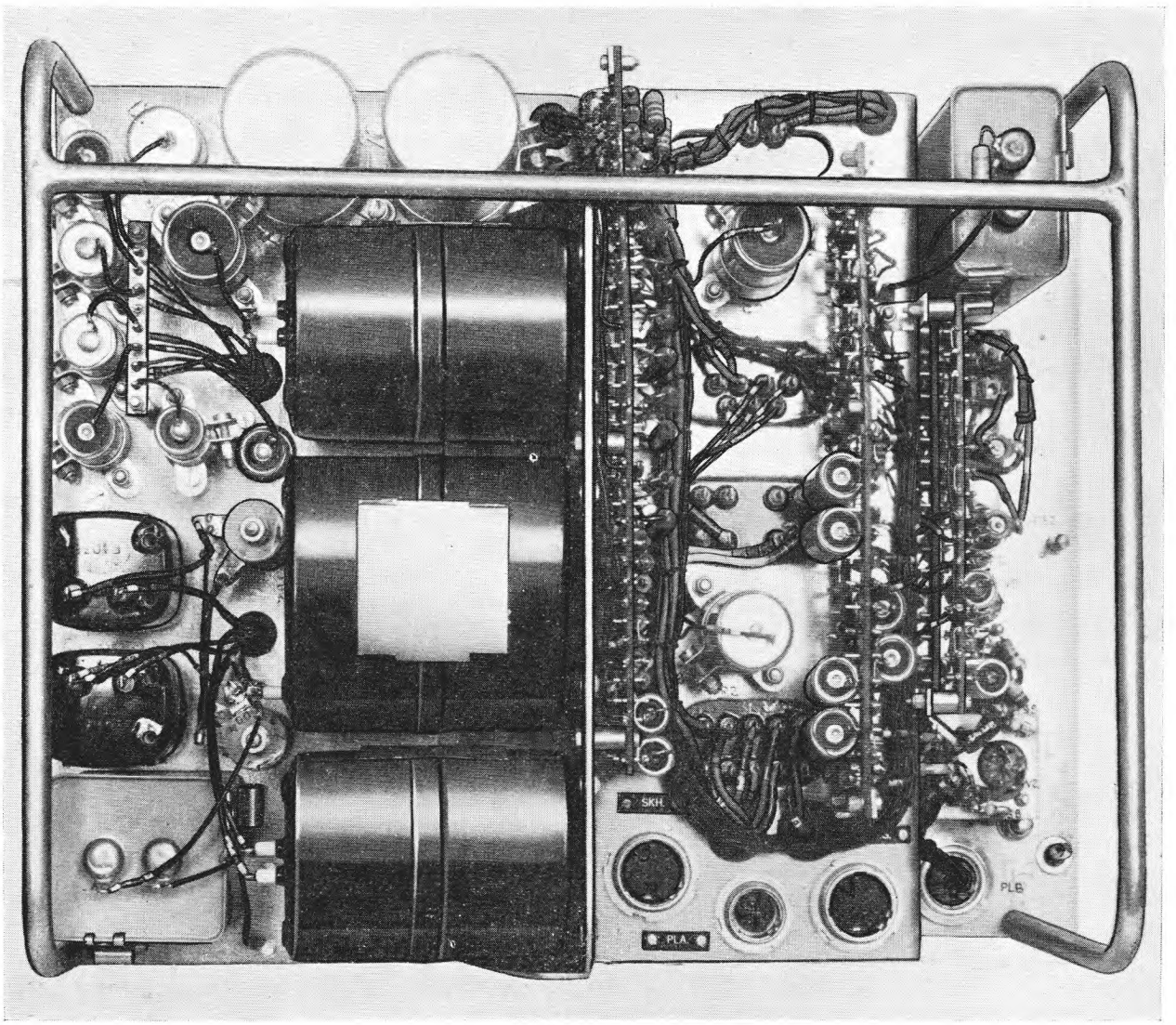


Fig. 2. Power unit 6889: rear view

to disconnect the mains supply in the event of the transformer becoming overheated.

5. T1 has a high-voltage secondary winding which delivers 400V-0-400V to two half-wave rectifier valves V1 and V2 and the resultant d.c. output is smoothed by the capacitance-input filter consisting of C1, L1 and C2. R3, connected in parallel with C1, is included to discharge the capacitor if L1 should become open-circuited.

6. From the filter circuit the d.c. output is fed to a stabilizer circuit formed by the series regulator valves V3, V4, V5 and the associated control valve V7. The reference level for V7 is established by the gas-filled stabilizer valve V8 which maintains V7 cathode at a constant potential irrespective of the current through the valve.

7. The unregulated d.c. is applied to the anodes of V3, V4 and V5. Due to the impedance of these valves a voltage drop occurs across them, its magnitude being dependent upon the common grid voltage. The grids of V3, V4 and V5 are returned to the anode of V7 whose grid is taken to the slider of a potentiometer RV1. RV1 forms part of a resistive network connected between the +250V output and earth and enables the output to be set to exactly +250V, thus compensating for component tolerances.

8. Any tendency of the h.t. output to vary from the nominal value of +250V causes a change of current through the network and a resultant change in potential at V7 grid. These changes in grid potential are amplified by V7 and applied to the grids of V3, V4 and V5 to counteract the original variation in output level.

9. Since the anode of V7 is connected to the grids of V3, V4 and V5 and these valves operate at a low value of grid/cathode bias, the anode potential of V7 would be slightly below +250V if R15 were returned to the stabilized line. However, in order to realise sufficient gain from V7 and ensure an adequate range of control, it is necessary to provide a h.t. source of considerably greater potential than +250V. This is achieved by the auxiliary stabilizing circuit consisting of R13 and the gas-filled stabilizer valve V6 from which an effective h.t. supply of +335V for V7 is derived.

10. In addition to the primary fuses, further protection is afforded by FS3, connected between the secondary centre tap and earth, and FS4 and FS5 in the stabilized output line.

11. The stabilized output is divided into two lines fed via contacts on relays A and B and fuses FS5, FS4 to sockets SKE and SKF which are connected to the passive decoders or to a decoder and test set depending upon the application of the power unit (*para.* 2). Other outputs are taken to sockets SKC and SKD for the decoder input amplifiers and to sockets SKA and SKB for metering purposes.

◀*30-35V neg supplies*

12. Separate bias lines for the decoders are derived from a 55V secondary winding on T1 supplying two bridge-connected rectifiers MR1 and MR2. The positive sides of the rectifiers are connected to earth through FS6 and the negative outputs are smoothed by capacitance-input filters consisting of C5, L2, C6 and C8, L3, C9. The d.c. outputs from the filters are fed through series variable resistors RV2 and RV3 to pins on SKA, SKB, SKC, SKD, SKE and SKF. RV2 and RV3 are preset controls enabling the negative lines to be adjusted to the correct value under load.

Negative-failure protection circuits

13. Protection circuits for the units connected to SKE and SKF are incorporated in the power unit and are formed by relays RLA and RLB and the two sections of the double-triode valve V9 having the coils of relays A and B in its anode circuits. The grid of V9A is taken to pin SKF/Q which is connected, within the passive decoder or test set, to pin SKF/K carrying the 30-35V neg. supply. V9B grid is taken to pin SKE/Q which is similarly linked to pin SKE/K. Thus, provided both −35V supplies are present, the two halves of V9 are cut off and the relays in the anode circuits are de-energized, the relay contacts are made and the +250V supply is fed out on both lines.

14. If a negative supply fails, the grid of the associated triode (V9A or V9B) is no longer held at 30-35V neg but is at earth potential and the valve draws current, causing the relay in the anode circuit to be energized. The relay contacts then break and the +250V supply is removed from all the sockets. ▶

Transistor supplies

15. The transistor circuits in the decoding units require various small d.c. potentials and these are derived from two lines, each of +10V and −10V with respect to earth. Transformer T2 has a 30V secondary winding which supplies two bridge-connected rectifiers, MR3 to MR6 and MR7 to MR10. The resultant floating d.c. outputs of approximately 20V from the rectifiers are applied to choke-input filters consisting of L4, C11 and L5, C12. Resistive networks from each positive and negative line to earth establish the necessary symmetry.

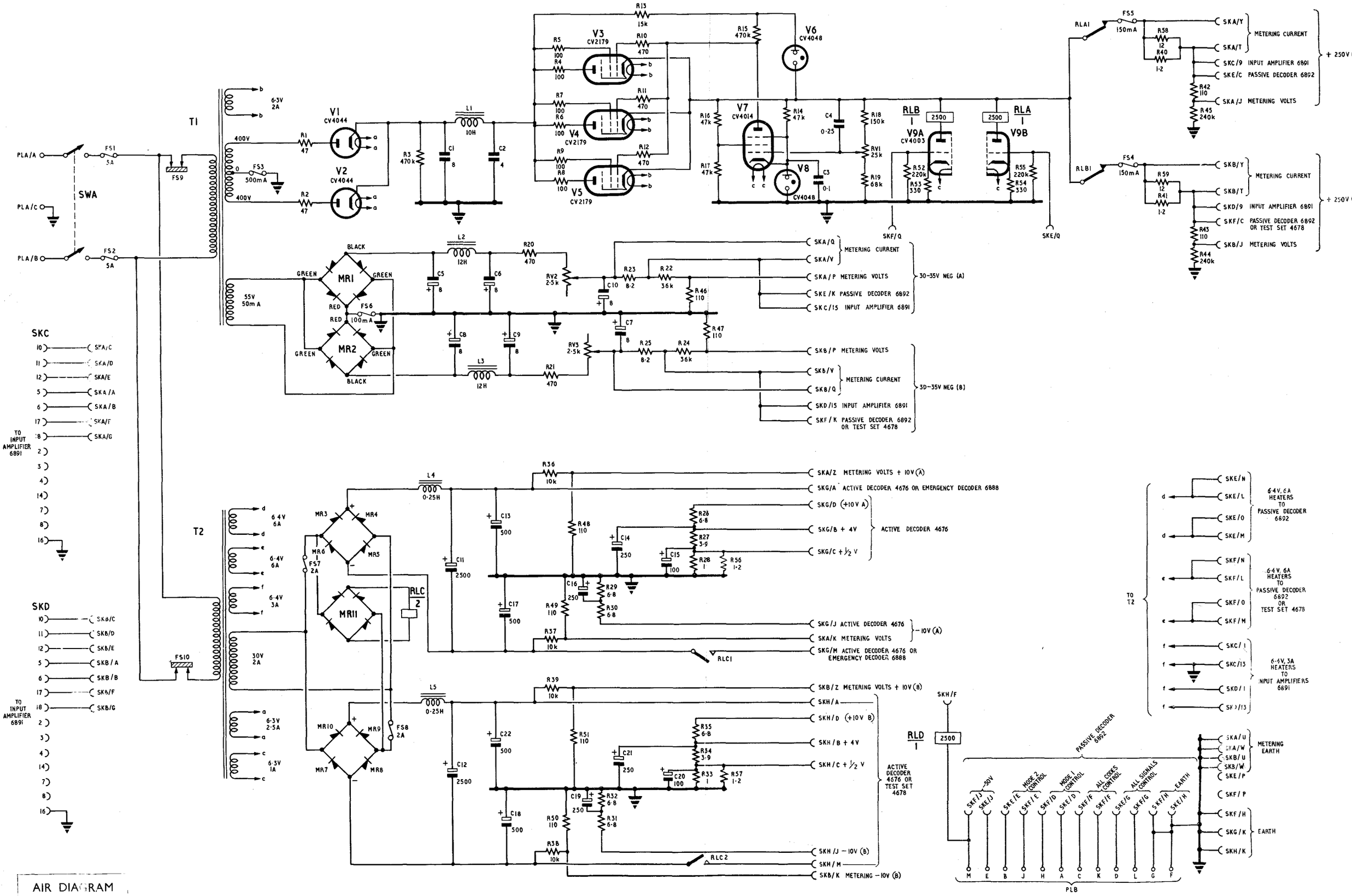
16. Intermediate voltages are obtained from potential divider networks connected between the 10V lines and earth. Suitable networks are provided in the emergency decoders but are not included in the active decoders or in test set 4678. In consequence, the potential dividers for the active decoder and test set are located in the power unit (R26-R30 and R31-R35). They are, however, only in circuit when an active decoder or test set is coupled to SKG or SKH since the appropriate connections, *e.g.* SKG/A to SKG/D, are made on the mating plug.

17. The springsets on relay C, connected in series with the −10V lines, are included to protect the output transistors in the active decoder. When an active decoder is used in conjunction with a passive decoder, part of the active decoder power requirements are supplied by power unit (A.D. indicator) 12123, the output stages being fed from both power units. Because of the large filter capacitances employed, the negative 10V outputs of power unit 6889 decay very slowly when the input is removed. If this power unit is switched off before power unit 12123 then, during the time that the −10V supply is falling to zero, circumstances can arise in which the maximum rated dissipation of the output transistors in the active decoder is exceeded (Sect. 5, Chap. 2).

18. To prevent the possibility of damage to the transistors relay C has its coil connected in parallel with the output from a bridge rectifier MR11 fed from the 30V winding. When the power unit is switched on, the relay is energized and the contacts make, connecting the −10V lines to the active decoder. On switching off, relay C is de-energized and the contacts break, removing the −10V supplies immediately.

Heater supplies

19. Heater supplies for all the valves in the decoding units are provided by the various 6·3V secondary windings on T2.



Power unit 6889 : circuit

Fig. 3

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Chapter 6 — DECODER SUB-ASSEMBLY (EMERGENCY) 6888

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LIST OF ILLUSTRATIONS

General

1. Decoder sub-assembly (emergency) 6888 is a small sub-unit associated with the passive decoder used for mode 1 decoding in rack 12276. It is also used in the mobile racks 12807 and 12808. The function of the unit is to select the last three pulses of any decoded emergency signals which may be received and to mix them with the undecoded mode 2 and 3 pulse trains. It also permits the decoded output from the mode 1 passive decoder to be mixed with undecoded mode 1 signals.

2. The emergency decoder (*fig.* 1) consists of a square chassis with all the components mounted on the top to facilitate servicing. It is designed for mounting on the back of the passive decoder and, for this purpose, has flanges along two sides. Captive screws in the flanges engage with tapped holes in the passive decoder frame.

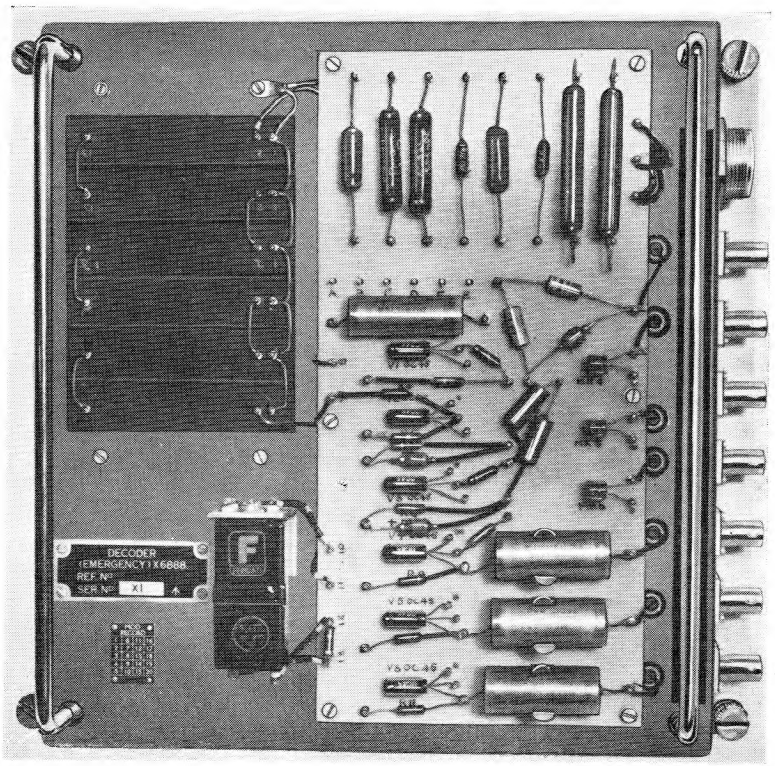

Fig. 1. Decoder sub-assembly (emergency) 6888: general view

Circuit description

General

3. The emergency decoder is a transistorized unit and some knowledge of transistor characteristics is necessary for a full understanding of the circuit operation. A discussion of transistor fundamentals is outside the scope of this chapter, but the general notes provided in Chapter 8 may be found helpful.

4. The output from the mode 1 passive decoder consists of either a single pulse, representing the decoded result from a normal response, or a train of four pulses, indicating an emergency signal. These pulses are negative-going and are approximately 14V in amplitude. They are fed into the emergency decoder at SKA and developed across the line terminating resistor R1 (*fig.* 3).

Mode 1 *mixing circuit*

5. The pulses at SKA are applied, via C3, to the base of a transistor V4 connected in a common collector (or emitter follower) circuit. The base is returned, through R8, to +8·2V and the emitter, via R9, to +2·5V. Since the base is positive with respect to the emitter, the transistor is cut off.

6. With the arrival of a negative-going pulse, a small current, limited by R18, flows into the base and this, in turn, causes a much larger current to flow into the collector. As a result, a negative voltage pulse is developed across the load resistor R9. The crystal diode MR3, connected in parallel with R8, is included to prevent lengthening of the input pulse whose positive-going back edge would otherwise decay with a time constant of R8, C3. The properties of the circuit may be regarded as similar to those of a triode cathode follower, *i.e.* the input impedance is moderately high, the output impedance is low and the output is in phase with the input. It will be seen that all the transistors, with the exception of V2 and V3, are employed in this circuit configuration.

7. V4 emitter is coupled to the junction of MR4 and C4, connected in series between SKB and SKE. Since, in the no-signal condition, V4 is cut off, MR4 cathode rests at the emitter potential of +2·5V. The positive-going undecoded mode 1 pulse trains from waveform generator 6010 are applied to SKB. When the input pulse amplitude exceeds 2·5V, MR4 conducts and the pulses are fed to SKE.

8. At the end of the undecoded pulse train, the output pulse from the mode 1 decoder causes V4 to conduct and the emitter approaches earth so that a negative pulse appears at SKE. Thus, the output at SKE consists of positive and negative-going pulses, starting from a level of 2·5V above earth (*fig.* 2).

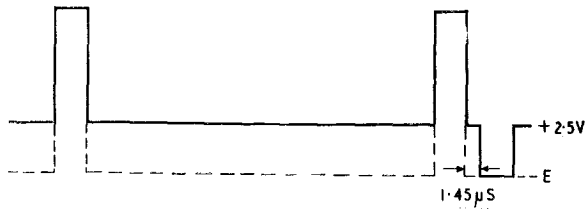

Fig. 2. Mixer output waveform

9. To prevent the decoded pulses being superimposed on the undecoded pulse trains, a small delay is introduced in the passive decoder. It will have been noted (*Chap.* 4, *para.* 8) that the total delay in that unit is 21·75μs, *i.e.* 1·45μs more than is required for decoding a pulse train. This 1·45μs occurs at the start of the decoding operation so that the single pulse produced as a result of decoding appears 1·45μs after the second bracket pulse. Thus, each negative pulse occurs 1·45μs after a pulse train.

Pulse separator and mode 2/3 *mixers*

10. It has already been stated (*Chap.* 1, *para.* 9) that provision is made for displaying emergency signals on all consoles at which IFF is selected, irrespective of the mode in use. This is done by mixing the decoded emergency response with the undecoded mode 2/3 pulse trains. The method adopted relies for its operation upon coincidence of the first emergency pulse, delayed by 21·65μs, with the second emergency pulse. Thus, one of the four pulses is lost in the coincidence circuit and only three pulses are available for mixing into the mode 2/3 channels. It should be noted that all four pulses are displayed when a mode 2/3 passive decoder is used for mode 1 ONE CODE operation.

11, Emergency signals, appearing at SKA, are routed through two channels, in one of which there is a time delay, to a coincidence circuit formed by the transistors V2 and V3. In the no-signal condition, V2 and V3 are cut off by the bias applied to the bases. V2 emitter is earthed and the collector is joined to the emitter of V3 whose collector is taken to −10V through the primary winding of transformer TR1. Both transistors are used in the common emitter circuit, V3 emitter being at earth potential for a.c. when V2 is conducting. Current must flow into both bases simultaneously before there is any collector current in V3.

12. The decoded emergency pulses, occurring at intervals of 24·65μs, are fed to the cathode of a crystal diode MR1. In the quiescent state, MR1 is conducting and a current of approximately 1mA flows through R2, MR1 and R1. The leading edge of the first pulse of the four-pulse train is passed by MR1 and a current, limited by R3, then flows into the base of V1 causing, in turn, a much larger collector current. When the back edge of the pulse appears at SKA, MR1 is cut off and C1 dis-

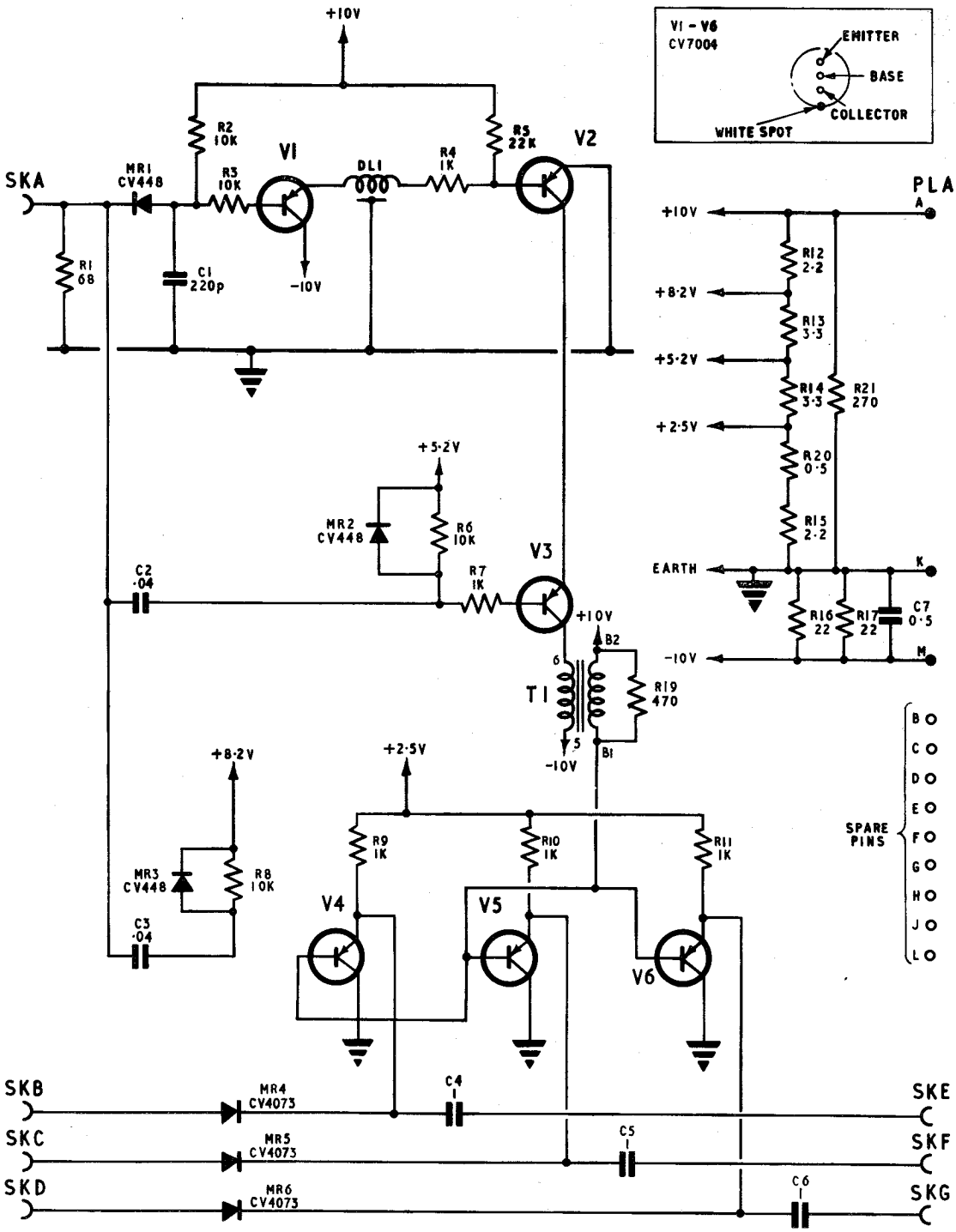

Fig. 3. Decoder sub-assembly (emergency) 6888 circuit

charges with a time constant of R2, C1 so that the input to V1 is an exponentially decayed pulse with a fast leading edge.

13. V1 is connected as an emitter follower with the emitter taken to the input of a delay line DL1. DL1 introduces a nominal delay of 24μs and its output is coupled, through R4, to the base of V2. Thus, V2 is switched on 24μs after the first pulse of the emergency train has appeared at SKA. By lengthening the pulse into DL1, coincidence with the narrower pulse fed to V3 is ensured without the necessity for very close component tolerances.

14. The first emergency pulse is also applied, via C2 and R7, to the base of V3. V3 is switched

on for the duration of the pulse but has returned to the cut-off state before the delayed pulse switches on V2. However, the second pulse of the train arrives at V3 base 24·65μs later to coincide with the delayed pulse at V2. Similarly, the second pulse of the train, after passing through the delay circuit, will coincide with the third and the third with the fourth.

15. Each time V2 and V3 are switched on together, a positive voltage pulse is developed across the primary winding of the pulse transformer TR1 whose secondary is coupled to the bases of V5 and V6. The pulse is inverted in polarity in TR1 and thus the waveform appearing across the load resistors R10 and R11 consists of three negative-going pulses corresponding to the last three pulses of the emergency train. The outputs from V5 and V6 are coupled into the mode 2 and mode 3 lines and mixed with the undecoded video applied to SKC and SKD. The action of MR5 and MR6 is similar to that of MR4 described in para. 7 and 8. On each channel the resultant output at SKF or SKG will be a positive-going undecoded pulse train followed, after approximately 25μs, by three negative-going pulses representing the emergency signal.

Power supplies

16. All the voltages required by the emergency decoder are derived from power unit 6889. It will be noted that the decoder incorporates a potential divider network from which the various intermediate voltages are taken. The plug connections are so arranged that the potential divider within the power unit is disconnected when an emergency decoder is being supplied.

Chapter 7

MISCELLANEOUS UNITS

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LIST OF ILLUSTRATIONS

General

1. The miscellaneous units of the IFF Mk. 10 SIF equipment are principally control units through which remote control of the decoders is achieved. Each passive decoder in rack (decoder) 4469 is associated with a particular console and the requisite control unit is mounted on the console or adjacent to it. For the decoders in rack (mode 1 decoder) 12276 a single common control unit is provided in the radar office.

2. The facilities provided by each control unit are determined by its application. For passive operation two control units are available, control unit (passive) 12118 for console 64 and control unit (passive) 12119 for console 4476. It should be noted that control units 12118 are fitted to all consoles 64 at which decoding facilities are required, even when active decoding is included, but that a different control unit is used with console 4476 if active decoding is required. This unit and the additions to console 64 for active decoding are described in Sect. 5, Chap. 7.

Control unit (passive) 12118

3. Control unit 12118, illustrated in fig. 1, consists of a box measuring approximately 14 in. × 6 in. × 7 in., accommodated on a mounting 12597 which is secured to the top of the framework of console 64.

◀**4.** The front of the unit consists of a frame behind which is mounted a perspex panel, blackened and engraved on the back face. The engraving is illuminated by edge lighting through ILP1 and ILP8. ILP2 to ILP7 floodlight three of the numbers on each of the switch scales so that, in operation, the switch positions are indicated. The illumination of the numerical indications is so arranged that the selected number is brightly lit while the numbers on each side are dimly lit. This enables the direction of rotation to be readily ascertained when it is desired to change the code.▶

5. Mounted on the panel are six 8-position wafer switches, four for mode 2 and two for mode 3. Each switch has an indicator plate bearing the numbers 0 to 7 and the code pulse group which it controls is identified above the plate. The moving contacts of all the switch wafers are taken to a common point at pin N of PL1 and thence to the positive pole of the radar office relay supply, designated 50V+ on the circuit (*fig.* 2) to distinguish it from the other 50V supplies. The fixed contacts on the switch wafers are connected, via other pins on PL1 and the interconnecting cable, to the code selection relays in the passive decoder. One side of every code selection relay in the decoder is returned to the negative pole of the 50V supply so that, as each switch is rotated clockwise, the corresponding relay (or relays) in the passive decoder is energized.

Fig. 1. Control unit (passive) 12118: general view

11. The remaining cut-outs in the upper portion of the cover enable the same assembly to be used for control unit (active) 12121 by the addition of an active decoding display. In control unit 12119 some of these apertures are covered with blank perspex panels but the mode indication lamps are retained. As shown in fig. 4, the lamps are controlled by the mode selector switch and enable the mode selected to be readily ascertained without the necessity for checking the switch position.

Control unit (mode 1) 12117

12. Each mode 1 passive decoder in rack 12276 is associated with a particular radar head and its output is fed, via the mode 2/3 passive decoders, to all the consoles deriving information from that head. In consequence, a single common control unit, providing code selection and standby switching facilities, is located in a convenient position in the radar office.

13. Control unit (mode 1) 12117 is illustrated in fig. 5 and a circuit diagram is given in fig. 6. In construction the unit is very similar to the control units previously described but is much smaller and carries only three switches. Two of these control mode 1 selection while the third enables the standby mode 1 decoder at the top of the rack to be switched into circuit in place of any one of the three main mode 1 decoders.

14. Since there are only two edge lighting lamps, a small step-down transformer T1 is incorporated, providing a 6V supply from the 230V mains input.

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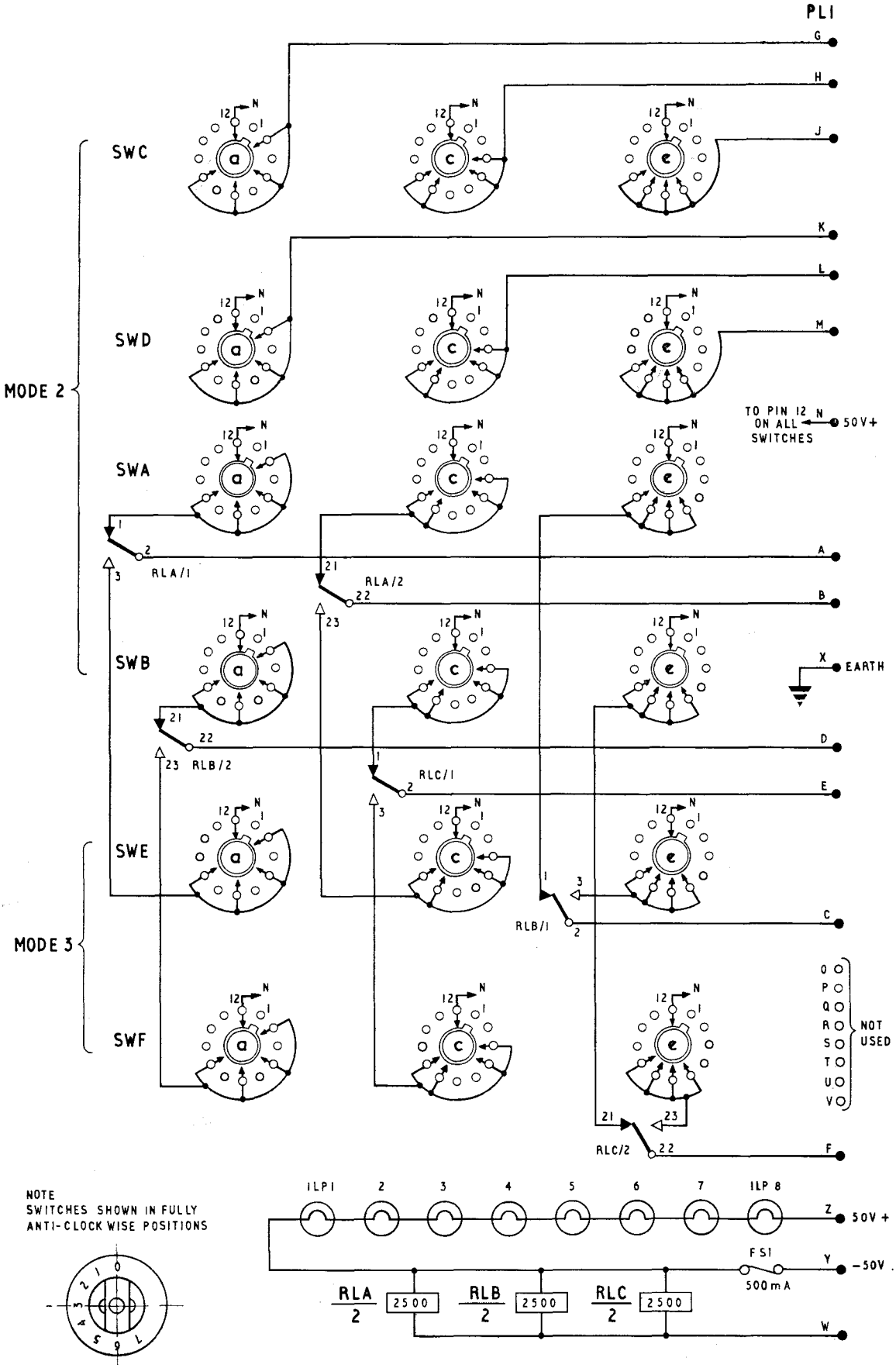


Fig. 2. Control unit (passive) 12118 : circuit

Fig. 3. Control unit (passive) 12119 : general view

6. The control unit also contains three relays, each with two changeover springsets. These relays are controlled by the mode selector switch and their purpose is to switch the connections to the pins of PL1 from the mode 2 A and B pulse group switches to the mode 3 switches when mode 3 operation is selected.

7. The facilities afforded by control unit 12118 are limited to code selection for modes 2 and 3, mode 1 switching being provided through the control unit in the radar office. The control switches for mode selection and function selection in the passive decoder are mounted on the control desk of console 64.

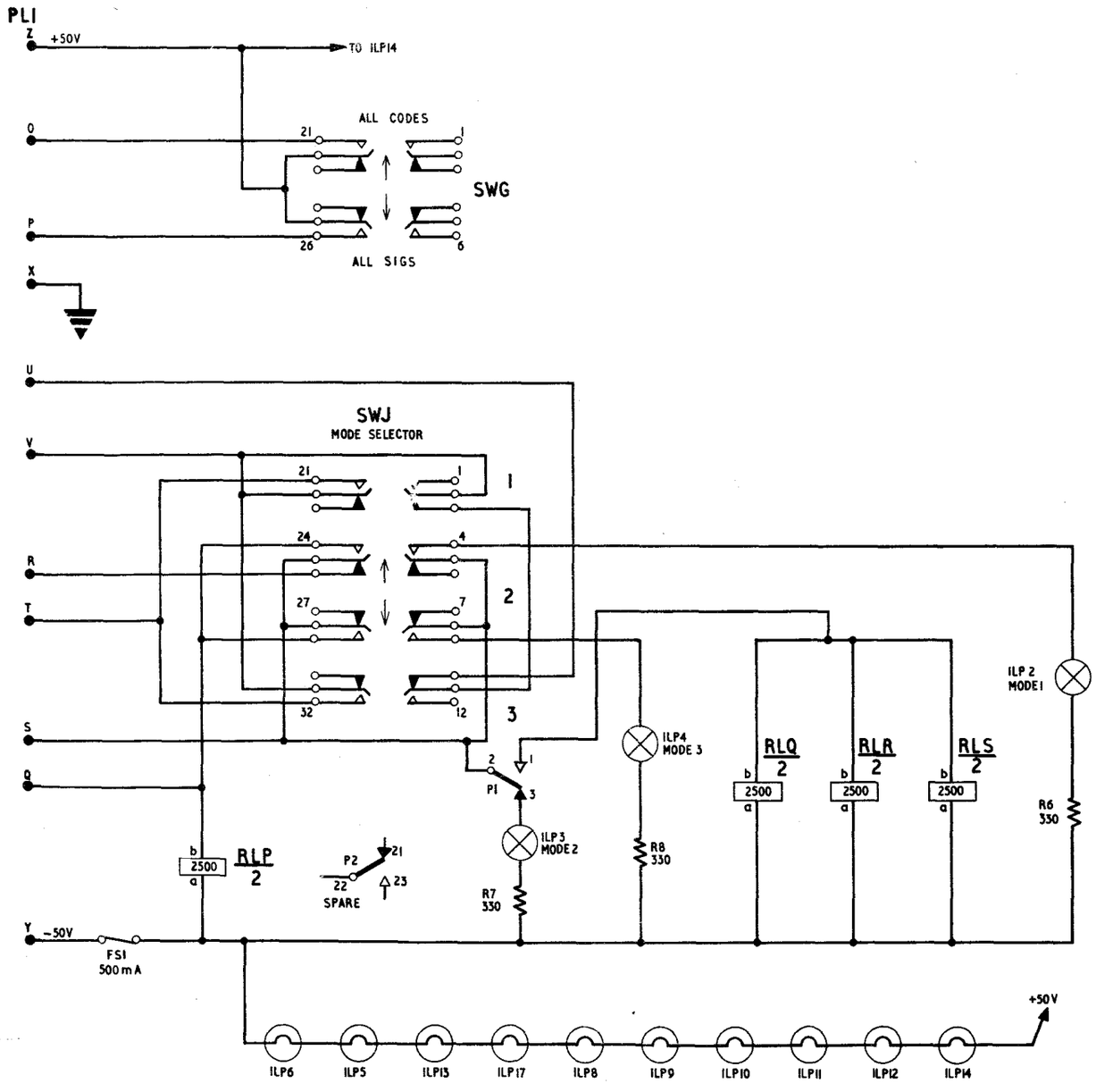
Control unit (passive) 12119

8. This unit, which is illustrated in fig. 3, provides similar facilities to control unit 12118 and is intended for use in conjunction with console 4476. The design of console 4476 is such that the simple addition of another control unit to the console is impracticable. For this reason the SIF control unit is supported on a pedestal adjacent to the console and has controls additional to those provided on control unit 12118.

9. Control unit 12119 takes the form of a hexagonal box designed to fit on top of a mounting (pedestal) 12809. This is a flanged tubular pillar, approximately 2ft. 6in. in height. In construction, control unit 12119 is similar to control unit 12118, i.e. the controls are mounted on perspex panels behind cut-outs in the front cover and are illuminated in the same manner.

10. The bottom controls are the code selection switches and, as will be seen from fig. 3 and the circuit diagram of fig. 4, this part of the unit is a duplicate of control unit 12118. Immediately above the code selection switches are the code selector and passive decoder function switches. The console mode selector switch, mounted on panel (control) 4658, is no longer used.

F.S./3



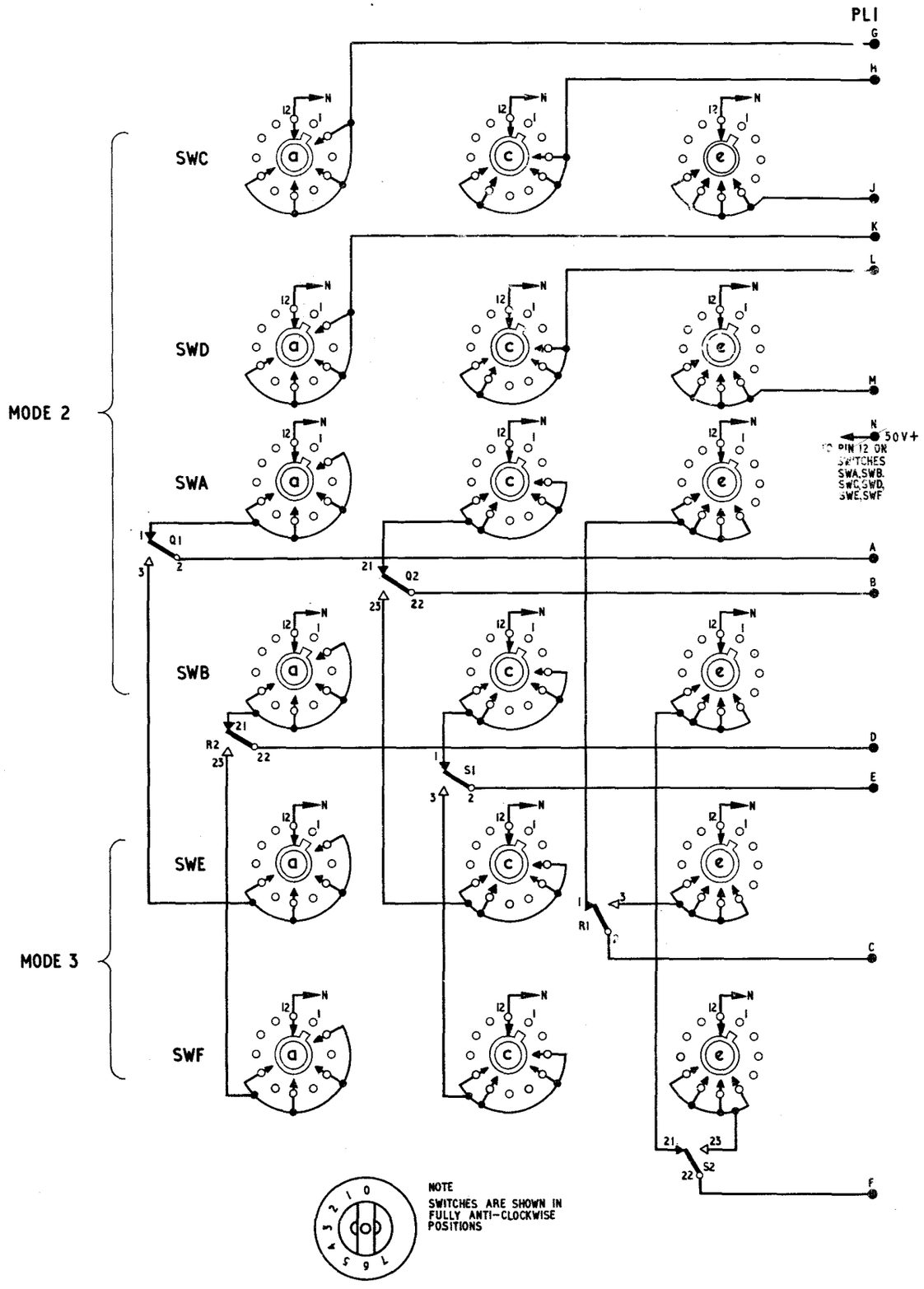


Fig. 4

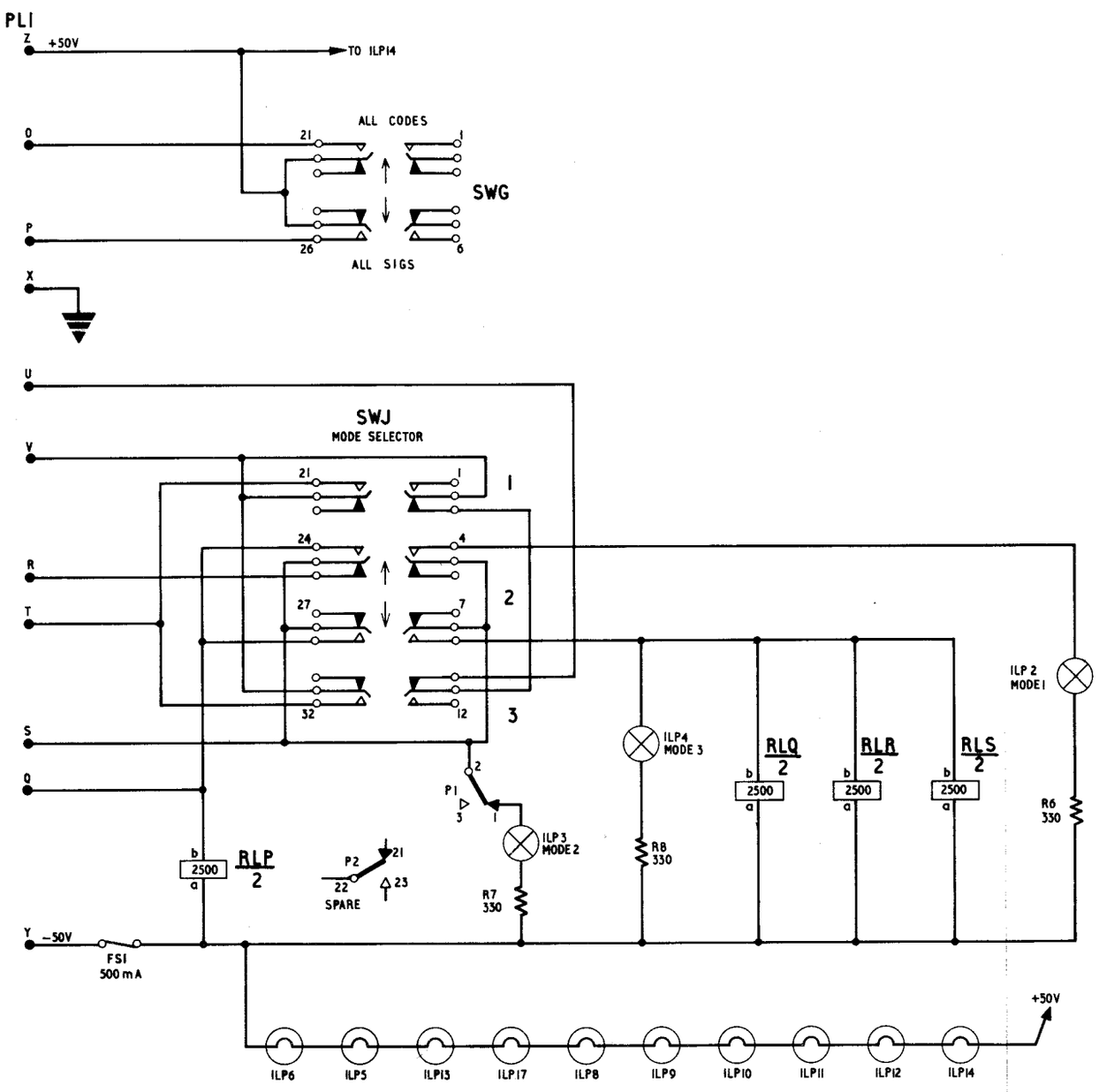
D.2118 470893 S.W. 2/65

Control unit (passive) 12119: circuit

RESTRICTED

Fig.4

F.S./3



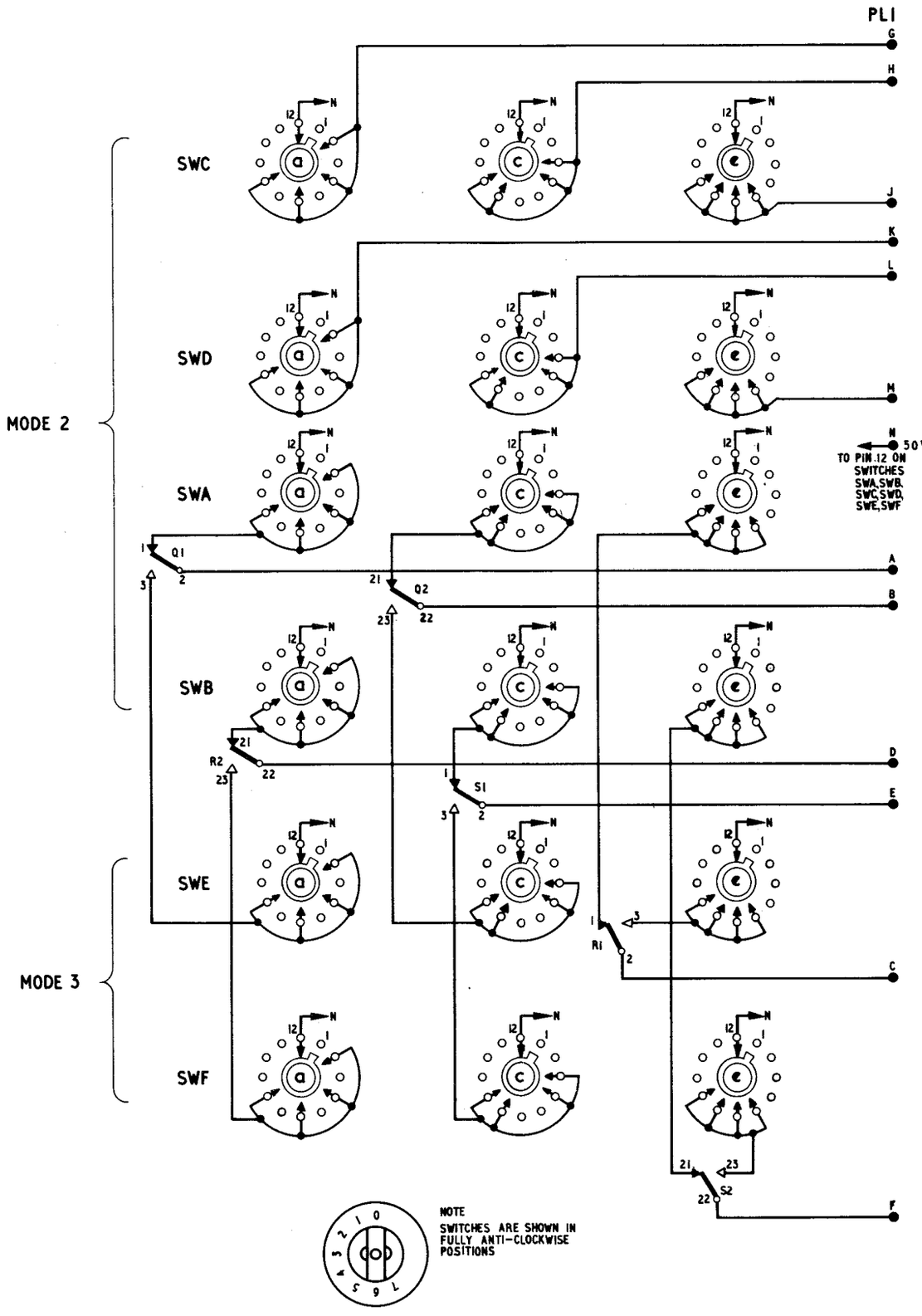


Fig. 4 Control unit (passive) 12119: circuit

924/8/7536/66528/631/2/62 J. T. & S.

Fig. 4

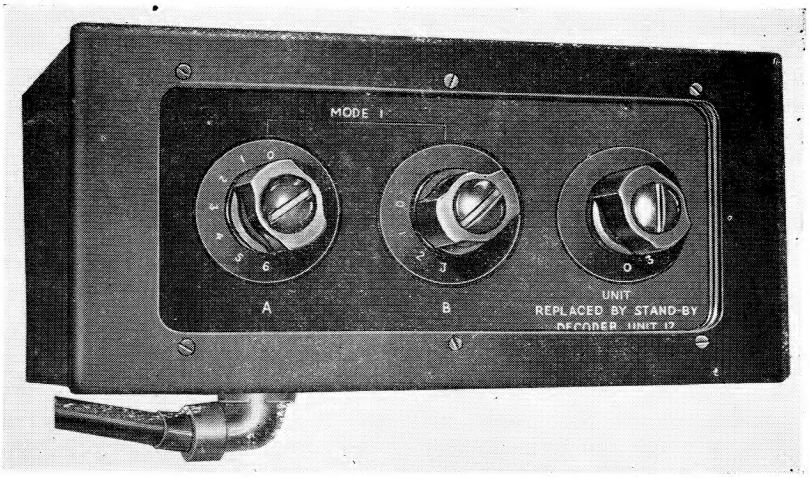


Fig. 5. Control unit (mode 1) 12117 : general view

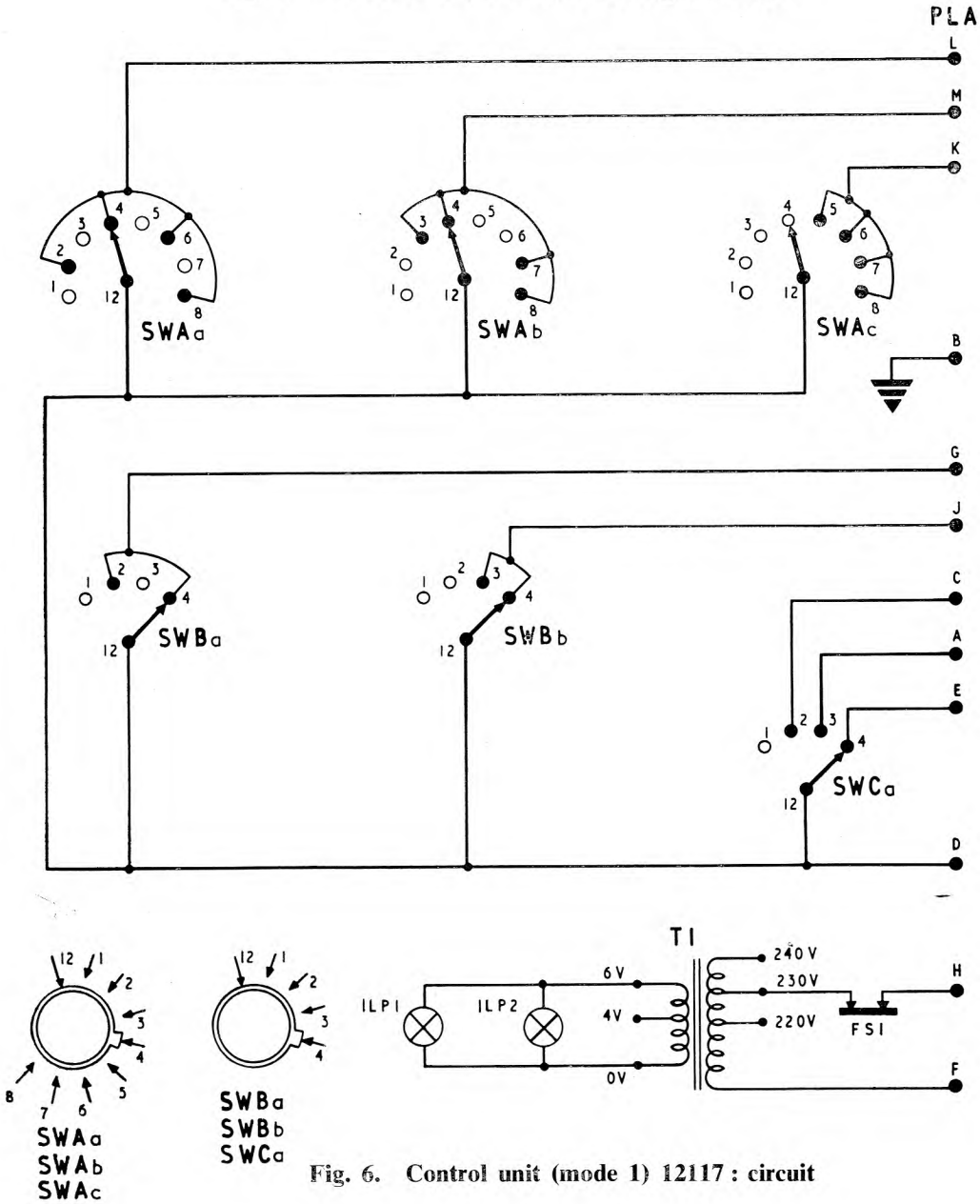


Fig. 6. Control unit (mode 1) 12117 : circuit

Chapter 5

RVT 511 Mk. 2

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Chapter 8

(This chapter supersedes Chapter 8 issued with A.L. 40)

INCREASED CODING FACILITIES

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LIST OF ILLUSTRATIONS

General

1. In the light of experience it has been found necessary to modify the original requirements for the SIF system. As explained in Chapter 1, it was intended that mode 1 should be used for general identification with a fixed common code for all aircraft, the code being rarely changed. This arrangement, when used independently of the mode 2 personal identification code has proved to give inadequate information. In addition, due to the use of a selection of six of the twelve available information pulses, mode 2 was restricted to a maximum of 400 codes.

2. Individual identification within the NATO area is now achieved by a combination of modes 1 and 2. Each member of NATO is allocated a number of mode 1 codes and can associate, with each mode 1 code, the 400 agreed mode 2 codes. Thus it is now possible to obtain a total of 32 × 400 personal identification codes, each of these codes providing more information than was practicable with the original system.

3. As a result of the change it is no longer possible to use the common mode 1 decoding system and the mode 2/3 decoders have to be able to decode responses in all three modes. This is achieved by simple modifications to the wiring of the decoder racks and to the mode 2 decoding equipment so that the decoded mode 1 signals formerly fed to the mode 2/3 decoders are removed and these decoders are enabled to operate on mode 1.

4. It should be noted that the changes affect only the normal mode 1 signals and that the arrangements for displaying emergency signals remain unaltered. Thus, decoded mode 1 emergency signals are still mixed into the mode 2/3 video channels to produce a 3-bar display. In addition, these decoded emergency signals are now also mixed into the mode 1 video channel to ensure their display on a PPI set to a different mode 1 code.

Rack (mode 1 decoder) 12276

5. The emergency decoders 6888 associated with the passive decoders 6892 in the mode 1 rack are modified by the removal of resistor R18 and the addition of a connection between the bases of V4 and V5, the changed part of the circuit being shown in fig. 1. The result of this modification is that decoded mode 1 signals no longer appear at the output of the unit and only decoded mode 1 emergency signals are fed out on the three video lines.

6. Relay P in the passive decoders is permanently energized under operating conditions by a modification to the rack wiring. This consists of the removal of the existing connection to pin C on each of the four free sockets SKB and linking pin C to pin F so that the relay coil is connected to earth. The mode 1 decoders now operate at all times in the ALL CODES condition.

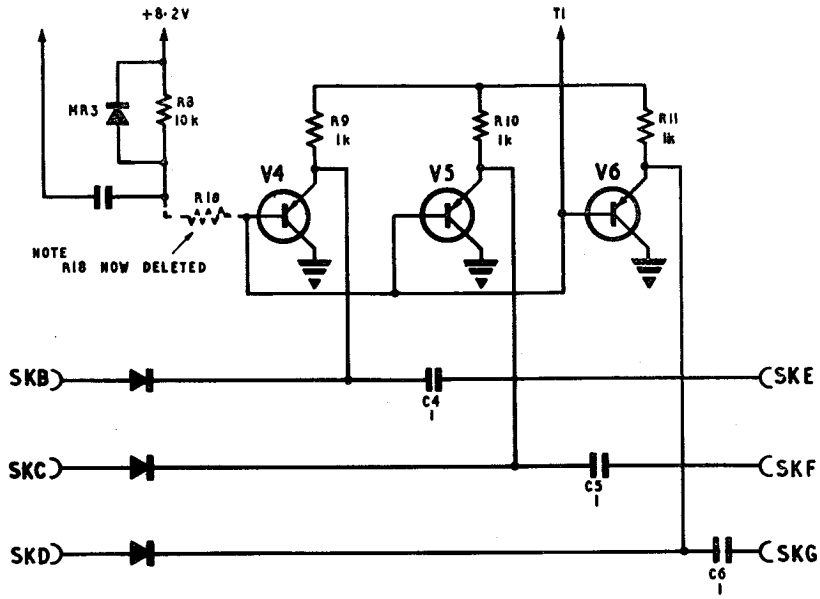

Fig. 1. Modification to decoder sub-assembly (emergency) 6888

Rack (decoder) 4469

7. To permit the mode 2/3 passive decoders to decode mode 1 signals in addition to modes 2 and 3, relay O in each decoder is permanently energized under operating conditions by removing the existing connection to pin E on each free socket SKA and linking pin E to pin H thereby earthing one side of the relay coil. As a result, decoded mode 1 signals appear at the decoder output when relay N is energized by turning the mode selector switch to mode 1. The mode 2 decoder control switches on the console control unit are used to set up the required mode 1 code.

Control unit (mode 1) 12117

8. Due to the changes enumerated, the code selection switches on the mode 1 control unit become redundant. This unit now serves only to switch into circuit the standby mode 1 decoder in rack 12276.

SECTION 5

ACTIVE DECODING

Chapter 1.— INTRODUCTION

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LIST OF ILLUSTRATIONS

General

1. The passive decoding equipment, described in the preceding section, permits known SIF coded signals from aircraft to be decoded and displayed on PPI consoles as single arc responses. The composition of SIF coded responses from aircraft whose identity is unknown cannot be ascertained by ONE CODE operation of the passive decoder, except on mode 1 which has a fixed common code.

2. An unknown code can only be handled by the passive decoder at one of two settings of the control switch, ALL SIGNALS or ALL CODES. In the ALL SIGNALS position, the complete pulse train is displayed and, on a long range PPI, the pulses tend to merge together into a solid paint, covering approximately 2 nautical miles. On the ALL CODES setting, only the bracket pulses are decoded to give a single arc display. In neither case can the information pulses which may be present be identified.

3. With the passive decoder set to ALL CODES, the resultant display indicates that a coded response is being received, although the decoder is unable to identify the code. The information can, however, be passed to the active decoding system which provides the means for decoding unknown responses.

4. Whilst passive decoding alone may fulfil many requirements, there is a number of occasions when an active decoder must be used. The following are two examples:

(1) Where the IFF responses of a number of aircraft have merged as the aircraft approached each other and then begun to separate. This may give rise to circumstances in which it is urgently necessary to identify a particular aircraft.

(2) Where there is some interest in the personal identity of an approaching aircraft (*e.g.* from long range) which shows a correct mode 1 response but does not correspond with a known operation.

5. The complete equipment required by an active decoding system may be grouped under four main headings.

Response selection

6. Selection of the desired response is achieved by the use of the inter-console marking equipment to provide a joystick-controlled ring marker. This is displayed on the PPI as an intertrace waveform and can be positioned, by means of the joystick, to embrace the estimated position of the next ALL CODES response. With the marking equipment is associated a waveform generator whose function is to provide a range strobe waveform every time the PPI timebase passes through the selected area. Alternative gated areas of 3 and 6 miles are available and facilities are included for the optional display, as a video waveform, of the outline of the gated area on the PPI. Normally, the intertrace ring marker (about 4 miles in diameter) is used to indicate the position of the gated area. The boundary marks outlining the gated area are provided mainly for setting-up and alignment purposes. The inter-console marking equipment is described in A.P.2527X and waveform generator (A.D. strobe) 12038 in Chapter 4 of this section.

Code pulse separation

7. Before active decoding can take place it is necessary to provide, on separate output wires, the individual code pulses forming the SIF code, together with a gating pulse representing the bracket pulses. This function is performed by decoder, video (passive) 6892 (*Sect.* 4, *Chap.* 4) which af-

fords twelve separate outputs (one for each information pulse position) and a gating pulse indicating the reception of a code train.

Code storage and cross-checking

8. This equipment consists of decoder sub-assembly (active) 4676 which can store and cross-check the coding information in up to eight SIF pulse trains. If there is a clear majority of pulse trains favouring one particular code, the code is stored in the output circuits of the decoder. Where, however, there is approximately an even distribution of the pulse trains between two codes, one of the codes is stored and a query circuit is energized. Such a condition can arise when the responses from two aircraft overlap. When more than eight SIF responses are received, the circuits are inhibited after the reception of the eighth. The active decoder is described in Chapter 2.

Active decoder display

9. When the code information contained in an SIF response has been produced and stored, it must be displayed in an easily identifiable manner. For this purpose neon-type numerical indicators are used. Each indicator consists of a neon tube on an octal base with the electrode assembly shaped to form the figures 0 to 7. The binary code information from one letter group of the SIF code pulse positions is employed to cause ionization of the gas surrounding the figures so that, depending upon the code, the appropriate figure is illuminated.

10. To obtain the necessary two-figure display on modes 1 and 3 or a four-figure display on mode 2, four of these neon indicators are used in the display units. Indicator, electrical (active decoder) 12120 (*Chap.* 5) forms the display for console 64 and control unit (active) 12121 that for console 4476.

Principles of active decoding

General

11. A block diagram of the active decoding system is given in fig. 1. The sequence of events is initiated by the action of setting the intertrace ring marker over the selected ALL CODES IFF response through operation of the console joystick control. The joystick voltage thus produced is applied, together with the timebase X and Y sawtooth waveforms, to the input of waveform generator (A.D. strobe) 12038.

12. When the relative amplitudes of each sawtooth voltage and its corresponding joystick voltage differ by a predetermined amount, a pulse is produced and, when the two pulses developed for the X and Y axes overlap, an IFF strobe waveform is generated. This waveform, which provides the range information, is fed to the active decoder gate.

13. It will be remembered (*Sect.* 4, *Chap.* 4) that the incoming code train is fed into the passive decoder and into a delay line with the same time characteristic as the train so that, at one instant of time, the entire train is contained within the delay line. At that instant the bracket pulses are decoded and the information pulses in the train appear at their appropriate tappings on the delay line. The twelve code pulse tappings of the line are connected, by separate wires, to the active decoder input and then to the code pulse gates.

14. The purpose of the active decoder gate is to pass the gating pulse resulting from bracket pulse decoding. Provided the decoder has been reset by operation of the manual control (A.D./OFF/A.D. + MARKER) on the console, the gate is prepared by an enabling voltage from the resetting trigger circuit. At the appropriate time the gate is opened by the range strobe and passes the gating waveform from the passive decoder. This waveform then operates the pulse train counter and opens those counter gates at whose inputs code pulses appear, to permit the counting of the code pulses.

Code pulse counting

15. It is possible that a pulse train may suffer interference, *e.g.* because of fading part of a pulse train may be missing. More probably, additional pulses may be injected due to random interference or garbling. For this reason, the active decoder does not decode on one pulse train alone. Instead, the information contained in up to 8 pulse trains is stored and automatically extracted at the end of the counting period.

16. The output from each code pulse gate is fed into a matrix decoder 6886, consisting of a counter chain with six outputs which are applied to a matrix store. The counter counts the code pulses received from its associated delay line tapping, each pulse causing the counter to step one stage and, in so doing, to produce a current pulse at the appropriate output. This pulse is then passed to the corresponding matrix store.

17. In the process of counting and storage, the pulses appearing at the input to each matrix decoder are assessed according to a code criterion based on the ratio of the number of pulses actually counted to the number of pulse trains received. The circuit operates on a possibility level of the order of 50%. Thus, if a particular code pulse occurs in that proportion of the pulse trains, the circuit assumes the possibility of the pulse being contained in the code and the query lamp will light although the presence of the pulse is not shown on the numerical indicator.

18. Except in the two special cases of one and two pulse trains,, a query indication is given for pulse train contents of 50% ± 1 pulse with an even number of trains or 50% $\pm\frac{1}{2}$ pulse with an odd number of trains. Whenever the pulse train content exceeds 50%, the presence of the pulse

(in the particular position concerned) is considered probable or definite, depending upon how closely the ratio of pulses to pulse trains approaches unity, and its presence is shown on the numerical indicator.

19. When one solitary pulse train is received, any information is considered unconfirmed and a query indication is given irrespective of whether a pulse is present or not. The numerical indicator shows the code designation corresponding to the code pulses received. In the case of two pulse trains a query indication is given only if their code content differs. Should both codes be identical it is considered probable that this code is the correct one and a definite indication is accordingly given.

20. The information derived as a result of the assessment by the matrix decoder is shown in the following code criterion table in which O is negative, OQ is possible, PQ is probable and P is positive.

Number of pulse trains received

1	2	3	4	5	6	7	8		
OQ	O	O	O	O	O	O	O	0	
PQ	OQ	OQ	OQ	O	O	O	O	1	
	P	PQ	OQ	OQ	OQ	O	O	2	Number of pulses counted in one code pulse position
		P	PQ	PQ	OQ	OQ	OQ	3	
			P	P	PQ	PQ	OQ	4	
				P	P	P	PQ	5	
					P	P	P	6	
						P	P	7	
							P	8	

It should be noted that although 8 pulse trains have been selected as the minimum for the code criterion, each code pulse counter only counts up to six since the receipt of six code pulses from 8 trains is considered to be a positive indication and, as will be seen from the table, the remaining two pulses would only add unnecessary information.

Pulse train counting

21. During the time that the individual code pulses are being counted, the incoming pulse trains must also be counted and this is achieved by feeding the gating pulse from the passive decoder, through the active decoder gate, to a pulse train counter 6887. This circuit counts the number of gating pulses arriving from the passive decoder and, on receipt of the eighth, initiates an inhibiting pulse to close the active decoder gate, thus preventing any code trains after the eighth from modifying the stored information.

22. It is possible that fewer than 8 pulse trains may be received. When this occurs the pulse train counter is unable to produce the inhibiting pulse and the active decoder gate then remains open until the arrival of the closing pulse from the interval timer, approximately 0·1 second after the start of the decoding operation.

Timing

23. The time required to extract and store the SIF code information is dependent upon the number of modes which are in use. If the ground station is interrogating on one mode only then eight SIF responses will occupy eight recurrence periods whereas, when all three modes are interlaced, a complete set of eight pulse trains in any one mode will require up to 24 recurrence periods. In consequence, the period allotted to each decoding operation is chosen to encompass 24 recurrence periods and is defined by timer, interval, 6885.

24. The operation of the interval timer is started by the first gating pulse from the passive decoder and it then proceeds to count the normal sync pulses from the master trigger unit. On receipt of the 25th recurrence pulse (*i.e. after* 0·1 *second for a station p.r.f. of* 250 *c/s*) the interval timer produces an output waveform which is the main read-out pulse. This pulse is fed out to the active decoder gate and the pulse train counter and controls the final operation of the decoder.

Code extraction and display

25. The interval timer output pulse is applied to the active decoder input gate as a gate trip waveform so that, if less than 8 pulse trains have been received, the gate is closed by the 25th recurrence pulse after the start of the decoding operation. It should be noted that no power is available to the active decoder indicator during decoding and that closure of the input gate causes the power supply to be connected to the indicator, either after the receipt of 8 pulse trains or on the arrival of the timer output pulse, whichever occurs first. Thus, in addition to preventing the receipt of more than 8 pulse trains, the gate must be closed before the gate closure allows the code to be displayed.

26. The read-out pulse from the interval timer is fed to the pulse train counter and causes it to move on one step. Although the counter counts only eight gating pulses it has nine steps so that one is available after eight pulse trains have been received and the gate is closed. The action of switching the pulse train counter one step causes an output current to be applied to the matrix stores, as a result of which voltage pulses may appear in the read-out windings of the stores. These voltage pulses are applied to the appropriate output gates.

27. During the process of code pulse counting, the switching operations cause pulses to appear at the output gates of the matrix stores but, since the gates have no supply voltage, these pulses cannot pass to the subsequent circuits. The necessary gate voltage is provided by the read-out pulse from the interval timer so that if, during this pulse, a store is switched in the appropriate direction, a voltage pulse is passed by the associated output gate.

28. The outputs from the store pulse gates are taken individually to trigger circuits whose operation causes relays to be energized. The relays convert the binary information to a decimal form or, more correctly, octal since the figures 8 and 9 are not used. From the relays the information is passed to the indicators. The outputs from the query gates are connected in parallel and fed to a single trigger circuit coupled to the query lamp. Thus, if a pulse appears at any one of the query gates the lamp will light.

29. The active decoder is a single operation device, *i.e.* it will decode one code and display it continuously until it is reset. To reset the decoder the A.D./OFF/A.D. + MARKER switch on the console must be returned to the OFF position. This action switches off the power supply to the A.D. indicator and the query lamp. When the switch is subsequently set to A.D. or A.D. + MARKER the resetting circuit of the active decoder is tripped, removing all the existing information and leaving the decoder ready for the next decoding operation.

30. It should be noted that, due to certain circuit limitations in the present system, the units forming an active decoder assembly are not electrically interchangeable. Each assembly of a passive decoder and active decoder consists of matched units and bears a label to this effect. In the event of unserviceability the combined units have to be returned to 3rd line and replaced by another matched assembly.

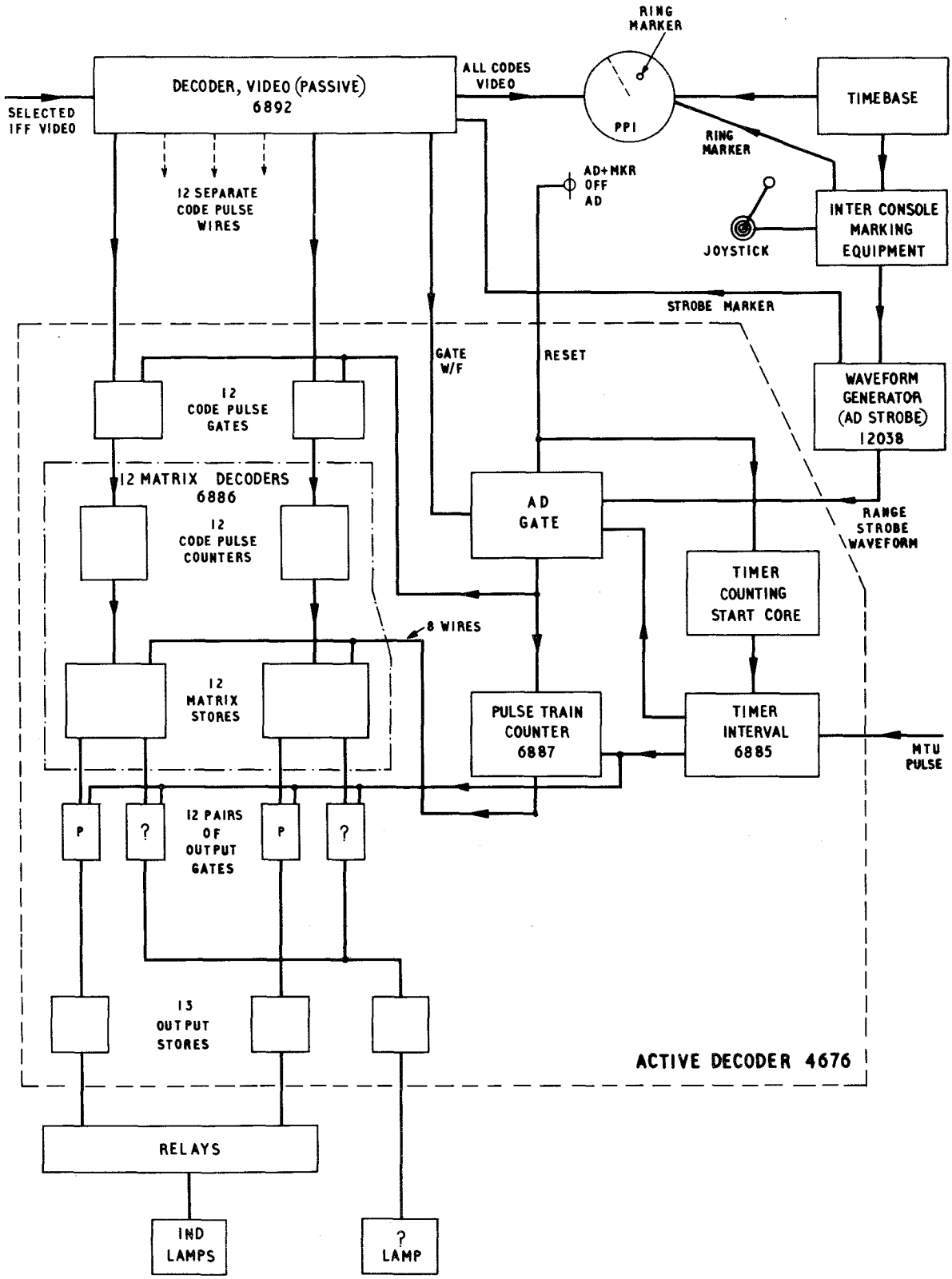

Fig.1 Active decoding system : block diagram

Chapter 2
DECODER SUB-ASSEMBLY (ACTIVE) 4676

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

General

1. Decoder sub-assembly (active) 4676 is the principal unit in the active decoding system, its function being to count the number of code pulses and pulse trains received. Having compared the number of pulses at each code pulse position with the number of pulse trains, it then stores the resultant information. The active decoder also times the decoding interval and, at the appropriate instant, delivers the stored information to the indicators.

2. Before the active decoder can operate, several input waveforms are required. These are: —

(1) The code information pulses which are contained in the code train.

(2) The pulse resulting from decoding the pulse train bracket pulses.

(3) A timing waveform derived from the master trigger unit pulses.

(4) A range (and bearing) strobe to ensure that only the selected response is fed into the unit.

3. Operation of the active decoder is manually controlled by a three-position switch mounted on the control desk of console 64 or on control unit (active) 12121 for console 4476. The switch positions are designated A.D., OFF and A.D. + MARKER. Movement of the switch to A.D. or A.D. + MARKER triggers the resetting circuit, causing the information from the previous decoding operation to be removed and placing the decoder in readiness for the next operation. In the A.D. + MARKER position the boundary marks which outline the strobed area are displayed on the PPI.

Construction

4. The active decoder (*fig.* 11) is a completely transistorized unit, each circuit being constructed on a printed wiring board. In all, there are fourteen such boards, one each for timer, interval 6885 and counter, electrical (pulse train) 6887 with twelve matrices (decoder) 6886 for the code pulses. The various input and output connections terminate at a row of contacts along one side of the board. All the boards are plugged into a framework which carries the multi-pole plugs and

sockets through which the decoder is connected into the system. Certain ancillary circuits are also located on this main frame work.

5. Like the emergency decoder, the active decoder is designed for mounting on the back of the passive decoder and, for this purpose, the framework has flanges along two sides. Captive screws in the flanges engage with the tapped holes in the passive decoder frame.

CIRCUIT DESCRIPTION

General

6. A block diagram of the active decoder is given in fig. 12. Since there are twelve matrices (decoder) 6886, all identical, a complete circuit diagram of the decoder is impracticable. However, a circuit diagram of the main frame wiring, showing the interconnections between the boards, is provided in fig. 16 and circuit diagrams for the boards are given in fig. 13, 14 and 15.

Glossary of waveforms

7. Some of the terms used to describe waveforms in this chapter are taken from the digital computer vocabulary and may be unfamiliar to those not versed in such techniques. To assist in understanding the circuit description, the following glossary of waveforms is included. This defines each waveform listed, its source and function and, if read in conjunction with fig. 12, will enable the operation of the unit to be more easily followed.

(1) Code pulse	SIF code information pulses from the tappings on the delay lines in decoder, video (passive) 6892. Fed to MR1 in each matrix (decoder) 6886.
(2) Range strobe pulse	The IFF response selection waveform from waveform generator (A.D. strobe) 12038. Fed to V8 of the main input gate on the pulse train counter 6887.
(3) Gating pulse	The formalized pulse produced by coincidence in the passive decoder of the bracket (or frame) pulses of the SIF pulse train. Fed to TR2 in the pulse train counter and to MR2 in each matrix (decoder) 6886.
(4) Regenerated gating pulse	The output from the blocking oscillator (V2/TR2) in the pulse train counter when triggered by (3). Used to trigger the pulse train counter.
(5) Main input gate closure pulses	(a) From the V13/MC11 stage in the interval timer to MR3 of the gate trip circuit on the pulse train counter. (b) From the V19/MC10 stage in the pulse train counter to MR4 of the gate trip circuit on the pulse train counter.
(6) Read-out trigger pulse	From the V13/MC11 stage in the interval timer (via R11) to the blocking oscillator (V1/TR1) in the pulse train counter.
(7) Regenerated read-out trigger pulse	The output from the blocking oscillator (V1/TR1) when triggered by (6). Fed to the pulse train counter stages.
(8) Read-out pulse	Generated in the pulse train counter stage storing "1" when triggered by (7). Fed to the appropriate winding in each matrix.
(9) Pulse output (10) Query output	Negative-going output pulses generated in the matrix pulse and query cores by the application of (8) whenever either or both of these cores are in the "1" condition.
(11) Matrix output gating pulse	The output of the V13/MC11 stage in the interval timer. Fed to V8 and V9 in each matrix (decoder) 6886.
(12) Current reset	The principal load current of the reset circuit on the main frame (V7) passing through the majority of the memcores in the decoder, but excluding MC2 to MC11 in the interval timer.
(13) Voltage reset	The voltage pulse developed at the collector of V7 on the main frame.
(14) Inhibiting pulse	The output from V3 on the main frame when the flip-flop (V1/V2) is triggered by (3).
(15) MTU pulse	The station synchronizing pulse fed to the blocking oscillator (V1/TR1) in the interval timer.
(16) Regenerated MTU pulse	The output from the blocking oscillator (V1/TR1) in the interval timer when triggered by (15). Fed to MC2 to MC6 in the interval timer and to MC10 in the pulse train counter.

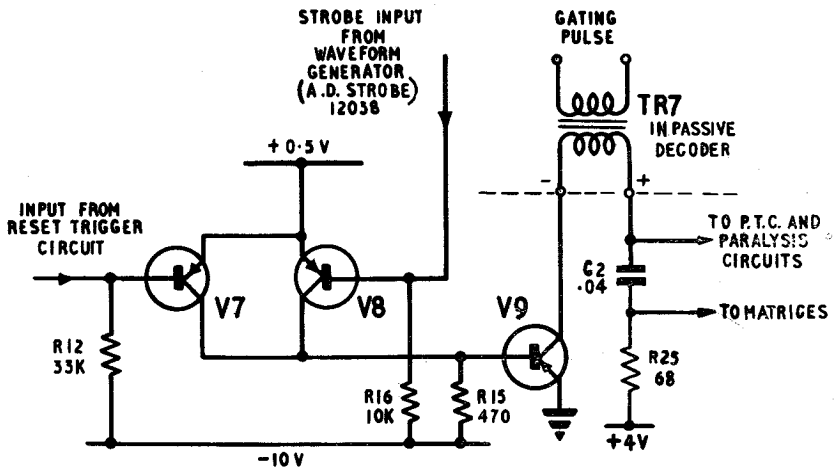

Fig. 1. Main input gate: simplified circuit

Active decoder main input gate

8. The gating waveform from the passive decoder is applied to the active decoder through a main input gate whose operation is controlled by a gate trip circuit and also by the range strobe waveform from waveform generator (A.D. strobe) 12038. The gate is located on the board containing the pulse train counter (*fig.* 13). Three transistors are employed and the circuit is shown in simplified form in fig. 1.

9. The emitters of V7 and V8 are connected together and taken to +0·5V while the bases are returned to −10V through R12 and R16 respectively. With no inputs, the base current of each stage is approximately 1mA so that both transistors are bottomed and the collectors are at emitter potential due to the very low output impedances. The collectors are connected together and coupled to the base of V9 whose emitter is earthed. Thus, V9 base is held positive with respect to the emitter and the transistor is cut off. A positive-going input to the base of either V7 or V8 alone will cut off the transistor to which it is applied, but will not cause V9 to conduct since its base will still be held at +0·5V through the transistor which remains bottomed.

10. To start a decoding operation, the required response is encircled by the ring marker and the circuit reset by operation of the console switch. In consequence, V7 is cut off by raising the base to a positive potential through the gate trip circuit. As the beam sweeps through the strobed area, waveform generator (A.D. strobe) 12038 generates a positive-going range strobe which is applied to the base of V8, cutting off that transistor. V9 base is now no longer held above earth and base current flows, causing the transistor to bottom. V9 collector, and hence the negative end of the transformer secondary, is almost at earth and the gating pulse is developed across the load. The collector current of V9 is not derived from the d.c. line but is provided by the gating pulse itself.

11. Range strobe pulses are continuously generated by the waveform generator during the time that the beam is sweeping through the strobed area and final closure of the main input gate is effected through the trip circuit by either the eighth gating pulse or the read-out pulse from the interval timer, whichever occurs first. That is, if less than eight pulse trains are received, the decoder counting circuits remain available for operation until the end of the decoding period.

12. It should be noted that the main input gate is not continuously open during the decoding period but at intervals whose duration is determined by one of two conditions. In the absence of a response there will be no gating pulse from the passive decoder and the gate will remain open for the time taken by the beam to sweep through the strobed area; this may vary from zero to 50 or 100 μs. When a normal response is received and a gating pulse reaches the active decoder, an inhibiting pulse is generated. This pulse is used to close the input gate approximately 1·5 μs after the arrival of the gating pulse, thus preventing the injection of pulses produced by unwanted responses.

Gate trip circuit

13. The trip circuit associated with the main input gate is also mounted on the pulse train counter board and consists of three transistors, V3, V4 and V5. V3 and V4 are connected in an Eccles-Jordan trigger circuit, shown in simplified form in fig. 2. Due to the d.c. coupling, this circuit has two stable states in which either transistor may be conducting with the other cut off.

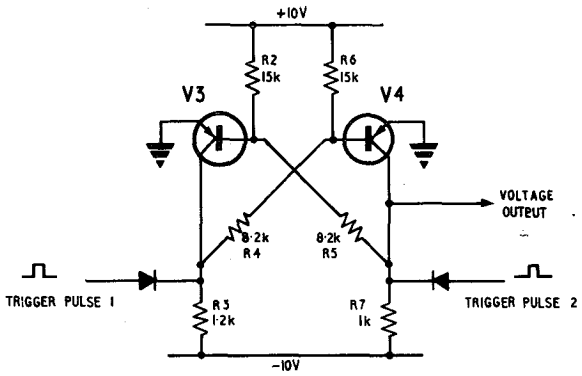

Fig. 2. Transistor Eccles-Jordan trigger circuit

14. Assume that, initially, V3 is conducting. A current of about 1mA flows through R5 and R7, holding V3 base at approximately 0·5V negative with respect to the emitter. The collector current of V3 is approximately 10mA so that the collector is virtually at earth and the potential at the junction of R4, R6 is about +3·5V. V4 is consequently cut off. A positive-going pulse, applied to the junction of R5, R7, causes V3 base potential to rise above earth and the collector current falls sharply. Because of the reduction in V3 collector current the collector voltage approaches -10V and base current flows in V4. V4 collector current rises rapidly until the collector potential reaches earth when V3 base, in turn, is held at +3·5V. The circuit has now attained its second stable condition with V4 conducting and V3 cut off. To restore the circuit to its original state a positive-going pulse must be applied to the junction of R3, R4.

15. The trigger circuit is followed by a common collector or emitter follower stage V5 (*fig.* 13). Initially, V3 is bottomed and V4 is cut off. During the time that V4 is cut off, V5 base current, flowing through R7 and R8, holds V5 base at about -0·5V. V5 is thus conducting and the collector current maintains V7 base near earth potential.

16. The reset voltage pulse, fed via the diode MR5 to V3 base, switches the trigger circuit to its second stable condition. V4 collector potential rises to earth and, since V5 base circuit is similar to that of V3, V5 base is also held at +3·5V. V5 is thus cut off, allowing the potential at the junction of R10, R12 to rise to approximately +2V. As a result, V7 base becomes positive with respect to the emitter and the transistor is cut off. In effect, V5 acts as a switch controlling a low impedance in parallel with R12.

17. The main input gate is closed through operation of the trip circuit by the application of a positive-going pulse to the base of V4, derived from one of two sources. In the first instance, the eighth gating pulse switches the core of MC10 to the "1" state. Trigger pulses from the MTU are fed through one of the windings on MC10 in the opposite sense so that the MTU pulse following the eighth gating pulse switches MC10 back to the "0" state, causing a pulse to be produced at V19 collector (*para.* 65). This pulse is coupled through MR4 to the base of V4. If less than eight pulse trains are received, the core of MC10 remains in the "0" state and is not switched. In this event the input gate continues to open on the arrival of the range strobe pulses in successive recurrence periods until the end of the decoding interval when a gate closure pulse from the interval timer, produced by the 25th recurrence pulse of the MTU, is applied to the base of V4 via MR3.

Note . . .

Reference should be made to Chapter 8 *for information concerning the characteristics of square-loop ferrite cores and a definition of the* "0" *and* "1" *states.*

18. It will be noted that the base of another transistor, V6, is coupled to the junction of R10, R12. V6 has as its collector load the coil of a relay through whose contacts the power supply to the active decoder indicator display is fed. During the decoding interval V6 is cut off and the relay coil is de-energized. With the arrival of the gate closure pulse V6 is switched on, causing the relay to be energized, thus connecting the power supply to the indicator display.

Pulse train counter

19. The action of opening the active decoder main input gate and, in so doing, providing an earth return for the secondary winding of TR7 in the passive decoder, allows the gating pulse to be applied to the counter. At this stage it is convenient to consider the operation of the remaining circuits on this board.

20. The gating pulse is developed across one of the input windings of a pulse transformer TR2. This transformer and the associated transistor V2 form a blocking oscillator, illustrated in simplified form in fig. 3. The circuit may be triggered by

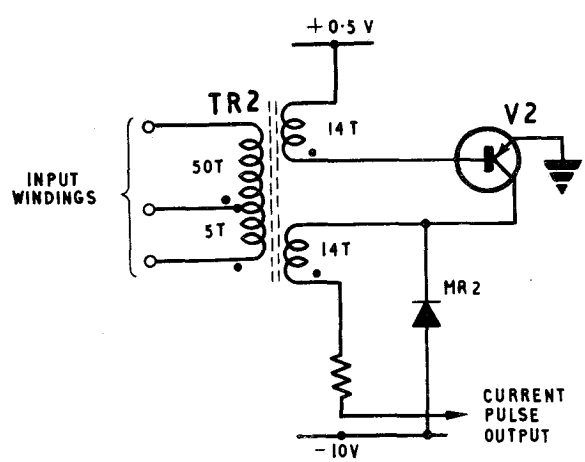

Fig. 3. Transistor blocking oscillator

a current pulse through the 5-turn winding or a voltage pulse across the 50-turn winding.

21. V2 emitter is earthed and the base is returned to a source of +0·5V so that the transistor is normally cut off. The gating pulse applied to the input winding overcomes the base bias and collector current starts to flow. The positive feedback causes this current to increase rapidly since the voltage induced in the base winding makes the base more negative with respect to the emitter, thus increasing the collector current. Because of the flow of collector current, the collector voltage rises from its initial value of −10V and, due to the feedback, the potential of the base decreases. The action is cumulative and the transistor bottoms when the collector-to-base potential approaches zero.

22. During this time the base current is rising but, when the transistor has bottomed, no further increase in base current is possible and the feedback current is then insufficient to maintain the increasing collector current required to hold the transistor in the bottomed condition. In consequence, at a time which is approximately proportional to the inductance of the transformer winding, the collector current begins to fall and the decay of this current gives rise to an e.m.f. of opposite polarity in the base circuit. The base voltage then rises and the transistor is cut off when the base becomes positive with respect to the emitter. To prevent overshoot the negative excursion of the collector voltage is limited by the action of the diode MR2.

23. The output of the blocking oscillator, which is a regenerated gating pulse, is taken via a series connection between the lower end of the limiting resistor and the −10V line. It is a current pulse of approximately 100mA with a duration of 0·75 to 1·5 μs. Similar circuits are used on all the boards and their purpose is to deliver pulses of substantially constant amplitude and length to the counting circuits (*para.* 32).

24. The counter chain is formed by a number of elements, each of which consists of a transistor and a wound ferrite core, designated a memcore (*Chap.* 8). A simplified circuit diagram of the basic unit is shown in fig. 4. The transistor is connected in the common emitter configuration and is normally cut off by returning the base to +0·5V. The collector is taken to −10V through a 15-turn winding on the core and a limiting resistor.

25. Assume that, initially, the core is in the "1" state and that a trigger pulse is applied to the 10-turn winding in the "0" sense. A flux change occurs in the core inducing an e.m.f. across the 50-turn winding. The phasing of this winding is

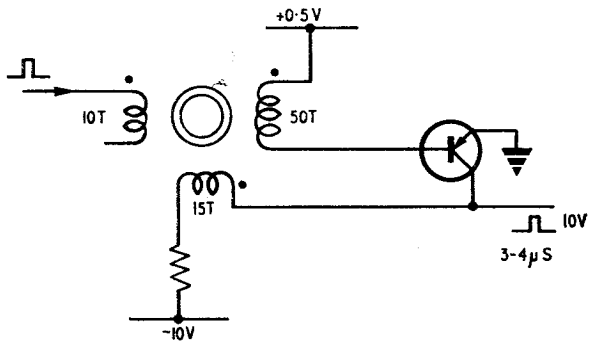

Fig. 4. Counter chain element

such that the e.m.f. opposes the +0·5V bias and when it exceeds that value the transistor will conduct. This, in turn, means that current will flow in the "0" sense in the 15-turn winding.

26. There is thus feedback from collector to base and the circuit is effectively a blocking oscillator. Regeneration occurs and the transistor bottoms, i.e. there is a very small potential difference between collector and emitter, the current flowing in the circuit (approximately 100mA) being determined only by the value of the limiting resistor. When the core has been switched, approximately 3 to 4 μs after the start of the trigger pulse, no further base current can flow and the feedback ceases. The collector current starts to fall and the circuit recovers to the quiescent state. Thus, the trigger pulse causes the transistor to conduct and so produce a pulse of current, some 3 to 4 μs in length. The trigger pulse merely initiates the action and need not exceed 1 μs in duration, provided its amplitude is sufficient to switch on the transistor.

27. It should be noted that regeneration only occurs when the core is initially in the "1" state and is switched to the "0" state. If the core is already in the "0" state when the trigger pulse is applied, it cannot be switched and the e.m.f. induced in the base winding is insufficient to overcome the cut-off bias. Should a pulse be applied to the trigger winding in the opposite sense to switch the core from the "0" to the "1" state, a positive e.m.f. is induced in the base winding and increases the cut-off bias, again preventing regeneration.

28. A typical counting chain is illustrated in fig. 5. The circuit is prepared for operation by passing a current pulse through the 3-turn reset windings, the winding on MC1 being fed in opposite phase to the other cores. As a result, MC1 is switched to the "1" state and all the other cores to the "0" state. When the first trigger pulse, after the resetting operation, is passed through the 10-turn trigger windings, MC1 is switched to the "0" state and regeneration occurs as described in para. 26. This trigger pulse can produce no change

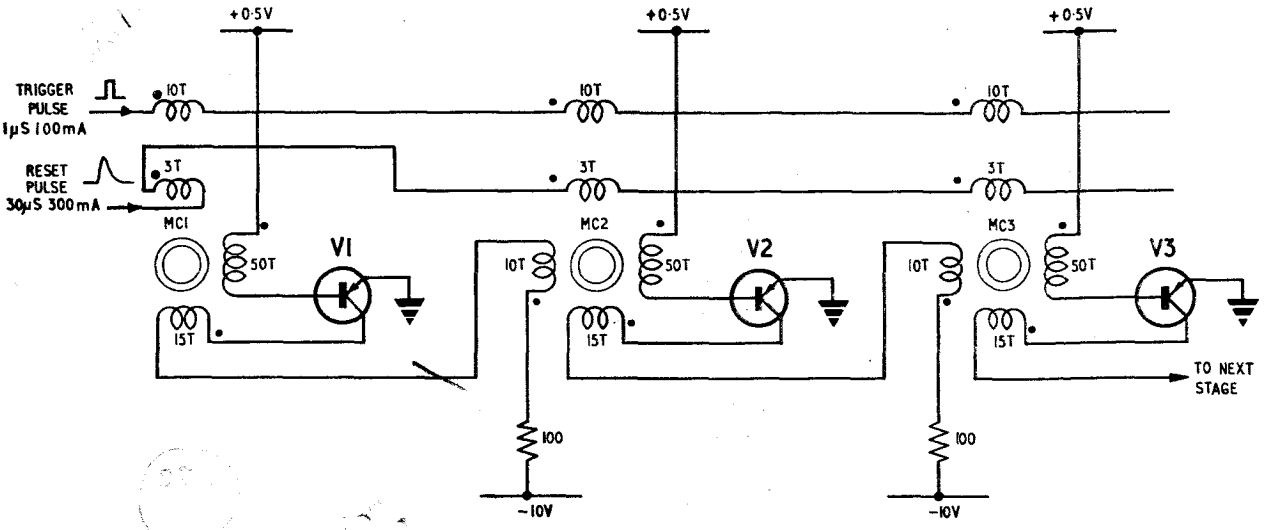

Fig. 5. Simple counting chain

in MC2 and MC3 since these cores are already in the "0" state.

29. The current pulse developed at V1 collector is coupled to MC2 through the 10-turn collector winding and switches that core to the "1" state. When the second trigger pulse arrives it will switch MC2 to the "0" state and cause regeneration, resulting in MC3 being switched to the "1" state. Similarly, the third trigger pulse sets MC3 to the "0" state, causing a "1" pulse to be applied to any subsequent stage. The circuit may be repeated with as many units as required.

30. The number of elements in the chain is a function of the number of operations required, i.e. the number of pulses to be counted. In general, the first element is preset to the "1" condition and for every pulse to be counted one extra stage is required. However, if the occurrence of the last pulse is not to be stored, the regenerative pulse produced at its time of arrival being sufficient indication, the last stage may be omitted. Thus, in the first instance (n+1) stages are required to count n pulses and in the second only n stages.

31. If required, the circuit can be used as a ring counter by coupling the output back to the input so that the nth. pulse resets the first core to "1". Cyclic operation then ensues and each sequence will be completed every nth pulse. This arrangement, in conjunction with a chain counter, is used in the interval timer to reduce the number of elements which would otherwise be necessary to count 25 MTU pulses.

32. It is important that the trigger pulse should be shorter than the shortest pulse produced by any unit in the counting chain for two reasons. Firstly, a long trigger pulse may initiate regeneration in more than one stage and cause the "1" to jump. Secondly, the trigger and switching pulses are present in the memcore windings of the next stage at the same time, in opposition to each other, and the switching pulse must override the trigger pulse in turning this next stage to the "1" state. To stabilize the duration of the trigger pulse at a suitable value, a blocking oscillator is interposed between the trigger source and the counter chain.

33. Considering fig. 13, it will be seen that MC1 to MC9 and the transistors V10 to V18 constitute a counter chain of the type described. MC10 and V19, although coupled to the chain, form part of the main input gate trip circuit. After the reset pulse has been passed through the 3-turn windings, MC1 is set to "1" and all the other cores are in the "0" state. The first trigger pulse, representing the bracket pulses of the first pulse train received, i.e. the first gating pulse from the passive decoder, switches MC1 to the "0" state and this action turns MC2 to the "1" state. Information that one pulse train has arrived is now stored in MC2. The second trigger pulse switches MC2 back to the "0" state, causing a current pulse to appear at PLJ/6 and a "1", indicating the second pulse train, to be stored in MC3. Subsequent trigger pulses continue the action through the chain.

34. In addition to counting the pulse trains the pulse train counter also provides read-out waveforms the last of which, when triggered by the interval timer, is used to extract the code information stored in matrix (decoder) 6886. Thus the pulses appearing at PLJ/6 – 12 and PLH/4 and 5 are fed to the matrix. It will be seen that, during the counting process, a pulse occurs from each stage in turn, causing current to flow through the

corresponding matrix read-out winding and this current will disturb any stored information. For any given total number of pulse trains received, the read-out trigger pulse causes one more operation of the pulse train counter. Thus the final effective read-out pulse always flows through the read-out winding following those which have been disturbed by the previous operations of the pulse train counter.

35. If eight pulse trains are received, the trigger pulse corresponding to the eighth train switches MC8 back to the "0" state. Since the output winding of MC8 and the input windings of MC9 and MC10 are in series, both cores are turned to the "1" state by the eighth pulse. MC10 is thus ready to produce the gate closure pulse when the next MTU pulse arrives (*para.* 17).

36. Once the main input gate is closed no more gating pulses can be applied to the pulse train counter and MC9 continues to store the "1" produced by the eighth pulse until the read-out trigger pulse from the interval timer is applied to the blocking oscillator formed by V1 and TR1 (*para.* 66).

Matrices (decoder)

General

37. Each code pulse tapping on the passive decoder delay lines is connected to the input of a matrix (decoder) whose function is to count the number of code pulses received and store the information. In all, twelve units are employed and a circuit diagram of one is given in fig. 14.

Code pulse input gate

38. To ensure that only the correct code pulses are fed into the active decoder they are applied, together with the gating pulse, to a diode gate similar to that employed in the passive decoder. The circuit is illustrated in simplified form in fig. 6.

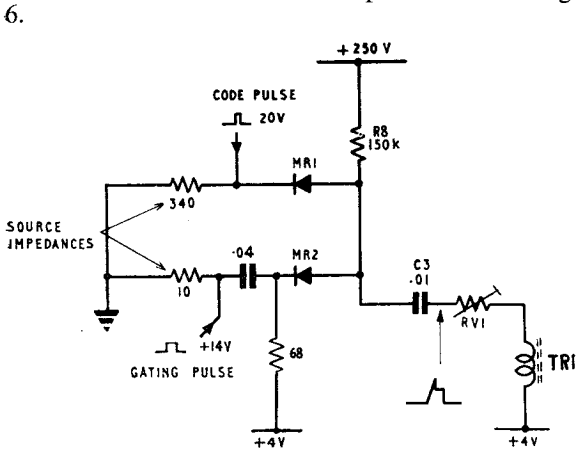

Fig. 6. Code pulse input gate: simplified diagram

◀**39.** With no input to the circuit, current flows from the 250V line through the 150 kilohm resistor R8 and the diode MR1 into the delay line tap, represented by the source impedance of 340 ohms. Since the voltage drop across MR1 and the delay line is small (of the order of 1V), MR2 is cut off, its cathode being held at +4V. A positive-going gating pulse applied to the cathode of MR2 increases the cut-off bias and can produce only a negligible effect on the potential at the junction of C3 and the diode anodes. A positive-going code pulse fed to the cathode of MR1 will cause the common anode voltage to rise to slightly more than 4V but, due to the standing bias, this rise can produce no significant change in potential at the junction of C3 and RV1.

40. Thus, for either input applied singly, there is no output from the gate. When gating and code pulses are coincident, MR1 and MR2 cathodes are raised simultaneously and the voltage at the junction of their anodes with C3 rises rapidly to a value determined by the ratio of the 150 kilohm resistor to the output impedance. If the output impedance is sufficiently high, the voltage at the junction of C3 and the diode anodes will be limited by the amount of current flowing through the diode to which the pulse of lower peak voltage is applied (the peak voltage of the gating pulse being equal to the pulse amplitude plus the 4V bias). The peak voltage at the common anode connection will then be approximately equal to this lower peak voltage input.

41. The gate output pulse is employed to trigger a blocking oscillator. Since both plates of C3 are at +4V, only pulses greater than 4V in amplitude are passed to the oscillator, the minimum triggering level of which is approximately 5V. There is an optimum value for the output impedance and this can be varied through the preset resistor RV1 in series with the input winding of TR1. The spike appearing on the leading edge of the output pulse is due to hole storage effect in MR1 and MR2 which are silicon diodes.▶

Code pulse counter

42. The counter chain, which is triggered by the blocking oscillator referred to in para. 41, consists of MC1 to MC6 and the transistors V2 to V7 (*fig.* 14). It will be seen that it is very similar to the pulse train counter chain except that there are only six stages. As explained in Chapter 1, para. 20, the receipt of six code pulses in eight pulse trains is considered a positive identification, rendering it unnecessary to count more than six code pulses. As a result, the code pulse counter contains only six elements. In this chain there is no storage of the last received pulse.

Matrix

43. Each matrix (decoder) 6886 contains a matrix which is a memcore assembly used as a

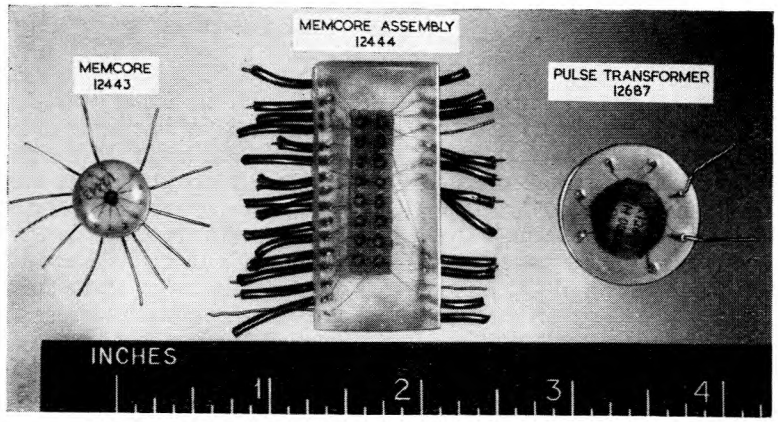

Fig. 7. Ferrite core components

memory store in which pulse train code information is retained and assessed. The assembly consists of sixteen wound ferrite cores arranged in two rows of eight. One row stores the identified code pulse information and the other row stores the queries. A matrix is illustrated in fig. 7.

44. Each core has four windings as shown in fig. 8. These are:

(1) Reset winding (yellow). Used to set the core to the start or zero condition. All 16 windings are in series and the reset pulse is passed through the cores in the "0" sense with the exception of the first query core which is connected in the opposite phase so that the reset pulse switches it to "1".

(2) Code pulse winding (red). The winding which enables the core to store the information passed to the matrix from the code pulse counter. These windings are connected together in groups in a pattern which is determined by the code criterion discussed in Chapter 1.

(3) Read-out winding (green). The winding to which the read-out pulse from the pulse train counter is applied. Each code pulse core winding and its associated query core winding are in series and the ends taken to pins on PLL and PLM for connection to the pulse train counter and the other matrices.

(4) Output winding (black). The winding from which the output pulse is taken (provided code pulse information has been stored in that particular core). All the code pulse windings are in series and connected to the output gate. Similarly, all the query windings are in series and connected to the query output gate.

45. The cores in both rows are interconnected in a pattern arranged to give sequential switching of the cores to meet the requirements of the code criterion. The operation of the matrix may be more clearly understood by considering fig. 8 in conjunction with the following table which shows the state of the cores after each successive code pulse has been injected into the appropriate windings. The bold symbols indicate the cores which have been switched by that particular pulse.

Number of pulse trains received

	1 2 3 4 5 6 7 8	
Pulse row	0 0 0 0 0 0 0 0	
		Reset or zero
Query row	1 0 0 0 0 0 0 0	
Pulse row	**1** 0 0 0 0 0 0 0	
		1st pulse
Query row	1 **1 1 1** 0 0 0 0	
Pulse row	**1 1** 0 0 0 0 0	
		2nd pulse
Query row	**0** 1 1 **1 1** 0 0	
Pulse row	1 **1 1** 0 0 0	
		3rd pulse
Query row	**0** 1 1 1 **1 1**	
Pulse row	1 1 **1 1** 0	
		4th pulse
Query row	**0 0** 1 1 1	
Pulse row	1 1 1 **1**	
		5th pulse
Query row	0 **0 0** 1	
Pulse row	1 1 1	
		6th pulse
Query row	0 0 **0**	

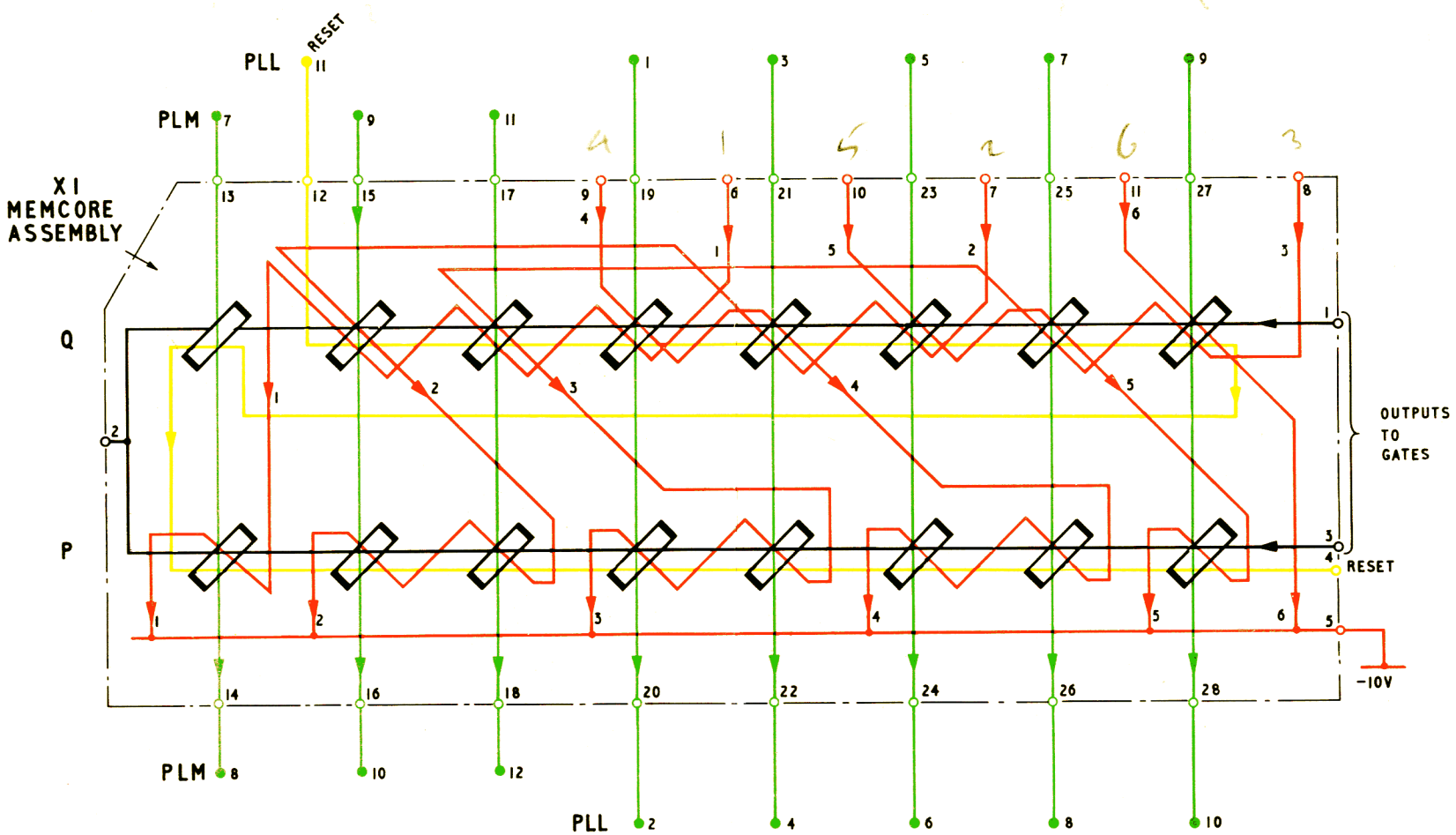

Fig.8 Magnetic core matrix Fig.8

46. It can be seen from the table that the required distribution of the information within the matrix is achieved by arranging for each pulse to switch several cores simultaneously. Each pair of symbols in each column may be regarded as representing the information passed to the indicator on the arrival of the main read-out pulse. The gaps in the table indicate where information has been disturbed by the counting pulses from the pulse train counter. It will be noted that this disturbance it not important since the current information is that which appears in the first and subsequent columns of each section.

47. To assist in interpreting the table, examples of the matrix operation for various combinations of pulse trains and code pulses are given in later paragraphs. Firstly, however, consideration is given to the two special conditions arising when only one or two pulse trains are received.

48. Where only a single pulse train has been received, the first pulse core in each matrix is switched to the "1" state if that particular code pulse is present; alternatively, the core is left unchanged if the code pulse is absent. Such unsupported information is, however, considered too indefinite for positive identification and so, for one pulse train only, the query lamp is made to light whether code pulses are present or not. It is for this reason that the resetting operation switches the first query core to the "1" state.

49. Now consider the situation when only two pulse trains are received. If a particular code pulse is present in only one of the trains, reference to the second section of the table shows that the second query core (but only the first pulse core) is switched to "1". Thus, the information passed to the indicator on the arrival of the main read-out pulse ignores this particular code pulse and includes a query. Where the same pulse is present in both trains, the second code pulse produces the condition indicated in the first column shown in the third section of the table. As a result, the code pulse is included in the display and there is no query indication since two code pulses in two trains is regarded as positive indentification.

50. When the number of pulse trains received exceeds two, the operation of each matrix is governed by the code criterion which requires that, with any particular code pulse, the pulse train content shall exceed 50% of the number of pulse trains before that pulse information can be included in the display. In the uncertain condition, where only a proportion of the pulse trains contains a particular pulse, a query indication is given if the number of code pulses counted falls within the zone of $50\% \pm 1$ for even, or $50\% \pm \frac{1}{2}$ for odd numbers of pulse trains. The number of pulse trains received and their code pulse content are determined by the conditions in which active decoding is attempted and the following examples show how variations can occur.

51, Consider first the simplest case of a single aircraft at short range radiating a succession of pulse trains, all of which are received. Each code pulse in each train is applied to the matrix associated with that particular code pulse position and successive pulses modify the state of the matrix as shown in the table of para. 45. With the receipt of the sixth code pulse, the matrix cores are switched to the condition shown in the last section of the table. When the seventh and eighth pulse trains arrive, the counting impulses which they produce will disturb the information in the first two columns of the last section, but the eighth pair of cores in the matrix still store the current information which will be extracted by the main read-out pulse. If, for any reason, particular code pulses are missing in one or two pulse trains, this will not affect the final answer provided the eight trains contain six pulses.

52. It is, however, probable that, on some occasions, less than eight pulse trains will be received or that code pulses may be missing, giving rise to a difference between the counts of the pulse train and code pulse counters. Either or both of these circumstances can occur when the interrogated aircraft is at long range or the strobe unavoidably includes the responses from two aircraft. Assume that an aircraft is being interrogated at very long range. It must be remembered that the airborne installation has two aerials, connected alternately to the transponder through a switch operating at 40 c/s. Each aerial in turn is coupled to the transponder for a period of 25 ms, representing approximately six recurrence periods at a p.r.f. of 250 c/s. If one of the aerials is screened, the only responses received by the ground station will be those from the other aerial so that, in the decoding interval of 0·1 second, the maximum number of pulse trains will be thirteen. This assumes interrogation on one mode only. Where the modes are interlaced, the proportion of responses for a given mode is less, depending upon the phasing of the interlacing cycle with the aircraft switching cycle. For example, with double mode interlacing, a response of one mode may be received as many as nine times or as few as four times within the $2\frac{1}{2}^{\circ}$ arc representing 25 recurrence periods. Similarly, with triple mode interlacing the maximum number of responses is reduced to five or four. Provided a particular code pulse occurs in every train, the matrix will still give a positive answer without any query. If, due to propagation conditions, one or more of the code pulses which should be present is missing, the information stored in the matrix will vary and the display to be expected can be ascertained from the table. The final information derived from the matrices is independent of the sequence of the missing pulses, i.e. it does not matter from which of the received pulse trains they are missing.

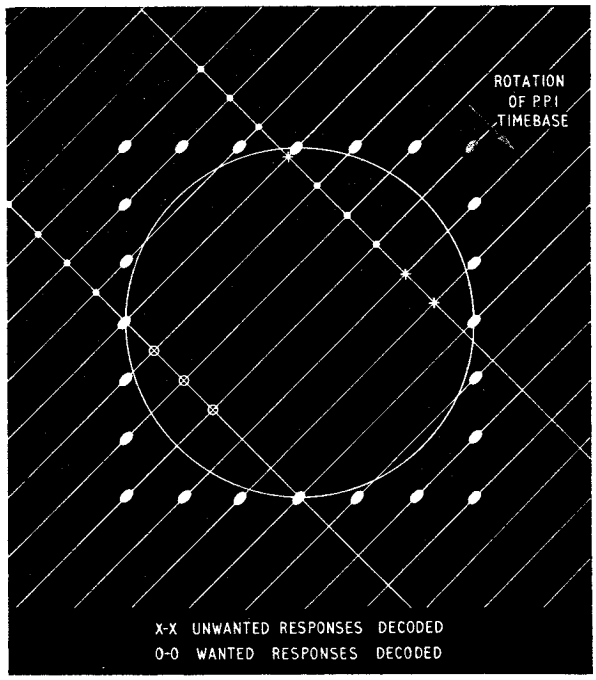

Fig. 9. PPI display showing two aircraft in strobe area

53. The condition when the responses from two aircraft are included in the strobe area is illustrated in fig. 9. It will be seen that the number of pulse trains which the decoder decodes may be composed of half from the wanted aircraft and half from the unwanted aircraft. If a pulse in the wanted responses does not form part of the code of the unwanted responses, that particular matrix will store the information that the pulse train content is only 50% and, on arrival of the read-out pulse, will deliver a query output only. The main input gate paralysis circuit (*para.* 69) is intended to prevent the decoder trying to decode responses from two aircraft within the strobe area, but can only discriminate when responses from both aircraft arrive in the same recurrence period. It cannot discriminate between responses in different recurrence periods.

54. In considering the storage of information and its extraction from the matrices it should be noted that the only relevant pulse from the pulse train counter to the matrices is the main read-out pulse generated by the trigger waveform from the interval timer. The earlier counting impulses from the second and subsequent stages of the pulse train counter pass through all the matrix read-out windings in series, disturbing the information in the cores, but this is immaterial since, in each case, the disturbed cores are one stage behind those holding the current information.

55. For example, assume that six pulse trains are received. The counting impulse generated by the receipt of the sixth train disturbs the information in the sixth stage cores of all the matrices while code information contained in this particular train is injected into any of the cores of the matrices, depending upon the current states of the counts of the various code counters. It is conceivable that, if only two particular code pulses had been received in the five previous trains, a third code pulse in this sixth train would attempt to switch the fifth pulse core to the "1" state (the third column of the fourth section in the table of *para.* 45) at the same time as the sixth counting impulse is tending to switch it back to "O". This, however, is unimportant as the subsequent read-out pulse will flow through the sixth stage cores in the matrices, i.e. the cores which hold the summated information of the six pulse trains.

Output gates

56. The remaining circuits on the matrix board are associated with the output gates. As a result of the counting impulses from the pulse train counter passing through the read-out windings, thereby disturbing the cores, it will be seen that output pulses will be generated if those cores are storing information. Since the only information of interest is that extracted by the main read-out pulse, the matrix outputs are taken to the bases of two transistors, V8 and V9, employed as gates.

57. The emitters of V8 and V9 are connected together and coupled, via PLM/4 to the collector of the final stage in the interval timer V13, whose collector is returned to – 10V via R11 on the timer and TR1 on the pulse train counter. Thus, in the quiescent condition, all three electrodes of both

V8 and V9 are at the same potential of – 10V, the bases being linked to the emitters via the read-out windings. Whatever inputs are applied between the bases and emitters cannot cause collector current to flow. When the 25th MTU pulse following the first gating pulse reaches the interval timer, regeneration occurs in the last stage of the counter chain on that unit, V13 collector rises to earth and the emitters and bases of all the output gates V8 and V9 take up the same potential. Both gates are then open and any core in the matrix which is turned from "1" to "0" during the period of the 25th MTU pulse causes base current to flow in the associated gate transistor. The positive-going pulse developed at the gate transistor collector is applied to a trigger circuit.

58. Since the query indicator is common to all twelve code pulse positions, the outputs of the query gates on all the boards are connected in parallel and fed to a trigger circuit located on the interval timer. Each matrix (decoder) has its own individual trigger circuit coupled to the pulse gate. The purpose of the trigger circuits is to store in permanent form, for as long as may be required, the transient output information from the matrices.

59. V10 and V11 are connected in an Eccles-Jordan bi-stable trigger circuit in which V10 is normally cut off and V11 is conducting. Because of the transient nature of the triggering pulse, capacitor C1 is included to speed up the switching operation. The positive-going pulse at V9 collector, produced by the code output from the matrix, switches the trigger circuit, cutting off V11 and causing V10 to conduct. The resultant current pulse at V11 collector is applied to an emitter follower V12. It will be seen that the circuit of the trigger and output stages is very similar to that of the gate trip circuit described in para. 13 and 14 and it operates in exactly the same manner. The collector of V13 is taken to PLP/6 and then to pin M of SKC on the main frame whence it is routed to the indicator. V13 collector load is the coil of the appropriate relay in the indicator.

60. When the trigger circuit has been switched by the matrix output pulse it will remain in the second stable state until it is reset by a pulse applied, through MR6, to the base of V10 when the console control switch is operated.

Interval timer

61. The primary purpose of the interval timer is to generate a read-out trigger pulse at the instant when it is required to extract the information from the matrices. The exact duration of the decoding interval and the method of producing the read-out trigger are not important provided two conditions are met. These are, that the interval should be long enough to permit the reception of up to eight responses in any mode when all three modes are interlaced and that the read-out trigger is not generated simultaneously with the reception of any response. Both requirements are conveniently met by using the MTU pulse. An interval of 25 recurrence periods allows eight responses in any one of the three modes to be received and, since the pulse occurs between timebases, there is no danger of coincidence between the read-out pulse and the last pulse train accepted.

62. The interval timer (*fig.* 15) counts the MTU pulses and consists mainly of two counters of the type already described (*para.* 28). MC2 to MC6 with V3 to V7 form a 5-stage counter whose output is coupled back, via the input winding on TR2, to MC2, constituting a ring circuit. Thus, every fifth pulse resets MC2 to "1" and the circuit will continue to count as long as input pulses are present.

63. MC7 to MC11 and V9 to V13 form a simple 5-stage chain counter operated by the output of the blocking oscillator V8 and TR2. Since the input to TR2 is the output from MC6, then the chain counter will count once for every fifth pulse, giving a final output from MC11 which is 5×5 or 25 MTU pulses after the starting pulse switches MC2.

64. It will be appreciated that MTU pulses are fed into the timer continuously whilst the equipment is switched on so that, at the start of a decoding operation, the next counter step may be anywhere in the chain. In addition, the resetting action, initiated by the operation of the console control switch, occurs well in advance of the receipt of the first pulse train. To ensure that the timer starts to count at the correct instant, a starting stage consisting of MC1 and V2 is included. MC1 is set to "1" by the reset pulse and is switched back to "0" by the first gating pulse to reach the active decoder. The subsequent regeneration causes MC2 and MC7 to be switched to "1" and all the other cores to "0". Thus, the counter chain starts counting on receipt of the MTU pulse following the first gating pulse.

65. The MTU pulses are fed to the input winding of the blocking oscillator transformer TR1 and the blocking oscillator output, which is a regenerated MTU pulse, is applied to the 10-turn trigger windings of MC2 to MC6 in series so that, for every MTU pulse into the chain, a corresponding pulse appears at PLG/10. PLG/10 is coupled to PLH/11 on the pulse train counter and thence to MC10 on that board. Since MC10 normally stores a "0", these pulses produce no effect, but, when the core is turned to "1" by an eighth gating pulse, the next output pulse from the ring counter switches it back to "0", causing the main input gate closure pulse to be generated (*para.* 17).

66. When the 25th recurrence pulse reaches MC11 on the timer, it generates an output which is fed to PLE/11 and 12. The output from PLE/

11 is taken to PLJ/7 on the pulse train counter and from there to the input winding of the blocking oscillator transformer TR1. The blocking oscillator output is applied to the auxiliary 10-turn trigger windings on the counter cores. Thus, the 25th MTU pulse serves as a read-out trigger pulse causing the pulse train counter to shift one step and so generate the main read-out pulse. PLE/12 is coupled to PLH/2 on the pulse train counter and to PLM/4 on the matrix (decoder) boards. This output is used as the matrix output gating pulse and opens the output gates of all the matrices (*para.* 57). At the same time, through the connection to PLH/2, the pulse is fed to the gate trip circuit so that, by operation of V5 and V6 on the pulse train counter, energizing current is fed to the appropriate relay in the indicator, thereby supplying power to illuminate the display. As a result of triggering the gate trip circuit the main input gate is also closed but this is, in fact, a redundant operation since the relevant information has been extracted from the matrices by the read-out pulse.

67. The remaining circuit on the timer board consists of an Eccles-Jordan trigger circuit, an emitter follower and an output stage, identical with that on the matrix (decoder). This circuit accepts the query outputs from all the matrices and a single output is fed, via PLE/5, to the query lamp in the indicator.

Main frame

68. The main frame serves as a support for the boards which make up the active decoder, provides all the interconnections between the boards and carries the plugs and sockets through which the input and output connections are made. In addition, there are two circuits on the frame; an input gate paralysis circuit and the resetting circuit for the decoder. A circuit diagram is given in fig. 16.

Paralysis circuit

69. The purpose of this circuit is to close the active decoder main input gate for a period of approximately 100 μs after the receipt of each gating pulse from the selected response to ensure that the decoder does not accept unwanted responses. When using the active decoder, the intertrace ring marker has to be placed over the estimated position of the next response, but it must be remembered that the actual strobed area is a square with three-mile sides. In consequence, if the ring marker is so placed that it only just encompasses the desired response, an unwanted response can be included in the strobe area. The maximum range at which this can occur is represented by the diagonal of the square, approximately $4\frac{1}{4}$ miles, so that, by closing the gate for a period of 50 μs after each wanted response is received, the elimination of unwanted responses within the strobe area can be achieved, provided such responses occur in the same recurrence period (*para.* 53). However, the strobe generator provides an alternative square with six-mile sides and, to cover the possible use of this facility, the paralysis time has been set at a minimum of 100 μs.

70. The paralysis circuit consists of two transistors V1 and V2 connected as a flip-flop, followed by a switching transistor V3. Initially, V2 base current, flowing through R5, holds the base slightly negative with respect to the earthed emitter and a collector current of about 10 mA flows through R6 so that the collector is almost at emitter potential. Thus, V2 is fully conducting and V1 is cut off since the base is held at approximately +2·5V at the junction of R3, R4.

71. Each gating pulse from the passive decoder, fed to the active decoder main input gate, is simultaneously applied, via C1 and the crystal diode MR1, to the flip-flop. Initially, little current is flowing through R2 and a very small bias voltage appears at MR1 cathode. The positive-going gating pulse is thus able to pass, via C2, to the base of V2. This tends to reduce the collector current of V2 and produces a decrease in the voltage at the junction of R3, R4 so that base current starts to flow in V1. The action is then cumulative until V2 is cut off and V1 is fully conducting. The positive waveform transmitted from the collector of V1 through C2 to the base of V2 commences to decay due to the negative leak through R5 until eventually a state of zero bias is reached and V2 collector current starts to flow again. The resulting rise in voltage at the junction of R3, R4 continues until V1 is cut off approximately 100 μs after the application of the triggering pulse.

72. The 100 μs negative pulse developed at V2 collector is employed to operate the switching transistor V3 which closes the input gate. V3 emitter is taken to +4V and the collector is coupled to the base of V9 on the pulse train counter. During the time that V2 is conducting, V3 base is held at about +4·5V so that the transistor is cut off. When the flip-flop is triggered by the gating pulse, V3 is switched on and +4V is applied to the base of V9 on the pulse train counter.

73. To ensure that the decoder does not respond to multiple pulse trains, the maximum delay between the arrival of a gating pulse and the closing of the gate should be 1·45 μs, i.e. the spacing between code pulses. The switching circuit provides an inherent nominal delay of 1·5 μs.

74. When a transistor is bottomed, a characteristic known as hole storage time comes into effect and modifies the switching speed. This is a transit time effect due to the recombination of holes with electrons in the transistor and results in a delay between the application of a switching pulse at the base and the point at which the collector bottoms. To achieve the highest switching speed, a transistor should not be allowed to bottom; alternatively, the hole storage time may be reduced if a very large base current flows after the transistor is turned on. It can be seen that V3 must bottom to obtain the lowest possible impedance between collector and emitter so that the full +4V bias is applied to V9 base. Thus, the operating conditions of V3 are so chosen that a

delay of approximately 0·5 μs due to hole storage time is obtained. Capacitor C3 is included to reduce the rise time but does not materially affect the hole storage time.

75. Similar considerations apply to V9 in the gate circuit. To achieve the minimum delay in opening the gate, a very large base current (of the order of 20 mA) flows when V9 is switched on. As a result, when the transistor is switched off, a delay of approximately 1 μs occurs between the application of the switching waveform at the base and the point at which the collector current falls to zero. In this way a total nominal delay of 1·5 μs is obtained between the arrival of the gating pulse at the flip-flop and the closing of the gate.

Resetting circuit

76. This circuit is similar to the paralysis circuit, consisting of a flip-flop, V4 and V5, an emitter follower V6 and an output stage V7. The operation of the flip-flop is as described in para. 71, the only difference being that the recovery time constant is of the order of 10 ms. The precise value of the time constant is not important provided it is sufficient to ensure that all the cores are completely switched.

77. The reset circuit is triggered manually and two inputs are provided; one of these is connected to the main control switch on the console while the other allows the decoder to be reset from a test set 4678. The two inputs are fed through crystal diodes MR2 and MR3 whose anodes are taken to −10V through R9 and R12. The diode cathodes are connected to potential dividers R10, R11 and R13, R14 and are held at −8V so that both diodes are cut off. This ensures that the resetting circuit cannot be triggered by any spurious waveforms picked up on the input leads when the resetting switches are in the off position.

78. When the console control switch is set to A.D. or A.D. + MARKER, the anode of MR2 is earthed and the diode conducts so that a voltage step of approximately +8V appears at the cathode. This voltage is coupled, via C4, to the base of V5 and triggers the flip-flop. Similarly, if a test set 4678 is in use, operation of its resetting switch earths MR3 anode, causing the flip-flop to be triggered. It will be observed that if the console switch is left in the A.D. or A.D. + MARKER position, MR2 anode will remain earthed. This does not preclude resetting from the test set since, although the positive-going 8V waveform at the base of V5 is

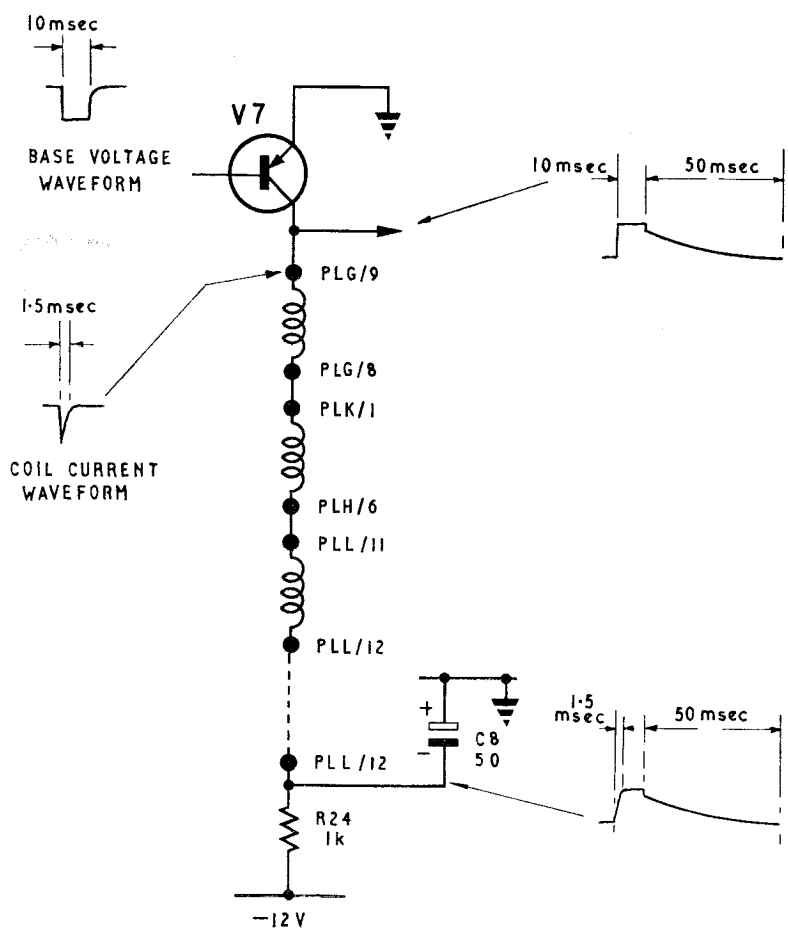

Fig. 10. Resetting circuit output stage

transmitted via C5 to the cathode of MR3, it only serves to reduce the existing – 8V potential at this point to approximately zero. Thus, the holding of MR3 anode at earth potential has no significant effect, except possibly at the peak of the waveform under certain component tolerance conditions when MR3 may conduct and tend to limit the waveform at slightly less than 8V.

Note . . .
The foregoing description of the triggering arrangement is based on the system adopted in the initial installations where pin Q of PLC at the base of the rack is connected to the console switch. The exact routing of the cables from PLC is a function of the station wiring and it does not follow that all installations will be the same. However, it is immaterial whether the console connection is made to pin Q or pin S since the reset input circuits are identical.

79. Approximately 300mA has to flow through the memcore reset windings during resetting and the flip-flop alone is incapable of turning on this amount of current. Accordingly, an emitter follower V6 is interposed between the flip-flop and the output transistor. The collector of the output stage V7 is connected to the start of the reset windings and the finish of the last winding in the chain is returned to – 12V through R24. The route is shown in fig. 10.

80. During the time that the resetting circuit is inoperative, C8 is maintained charged through R24 from the 12V source. When V7 is switched on by the resetting action, its collector potential rises to earth and the transistor and memcore windings present an extremely low impedance across the capacitor. C8 then discharges through the windings, providing a peak current of the order of 300 mA. By drawing the current from a capacitive source, the reset current waveform is a steep wavefront followed by an exponential decay. It should be noted that whenever the decoder is reset, only a small proportion of the total number of cores has to be switched, each of which generates a small back e.m.f. Cores already in the reset or zero state behave as ohmic impedances generating little back e.m.f. The exponential tail ensures that those cores which are switched to the zero state are not subsequently disturbed by transients that might occur if a square waveform were used.

81. The recovery time constant of the reset circuit is made sufficiently long (approximately 1·5 ms) to ensure that the chain reactions arising in the various counting circuits are completed. The initial effect of resetting any particular stage is to set the following stage into the "1" state. Thus, when the resetting current is maintained, the "1" condition is propagated from core to core, finally disappearing from the last stage.

82. The voltage excursion at V7 collector, when the transistor is switched on, produces a positive pulse of approximately 12V in amplitude, equal in duration to the flip-flop waveform and followed by an exponential recovery back to – 12V as C8 recharges through R24 with a 50 ms time constant. This pulse is applied to the reset inputs of all the Eccles-Jordan trigger circuits in parallel.

Power supplies
83. Power supplies for the active decoder are derived from power units 6889 and (A.D. indicator) 12123. The majority of the transistors in the decoder are supplied from power unit 6889 and, since the total load current is approximately constant, apart from transient pulses, the output voltages remain constant. However, V7 in the resetting circuit is switched on for many milliseconds at the start of a decoding operation and some of the thirteen output transistors of the matrices may be switched on when the code display is produced. Thus, these transistors impose a fluctuating load on their supply and their collectors are fed from a separate – 12V line derived from power unit 12123. This unit also provides a + 250V supply for the code pulse input gates.

84. Since the output transistors are supplied from two separate power units, precautions against excessive dissipation become necessary. If power unit 6889 is switched off before power unit 12123 while any of the active decoder output transistors are passing current (the decoder not having been reset) then, during the time that the – 10V supply is falling to zero, the base drive to these particular transistors will fall proportionately until they are no longer bottomed. At this point the collector/emitter voltage drop and, in consequence, the collector dissipation starts to rise and will eventually exceed the maximum rated value.

85. To prevent the possibility of damage to the transistors, a protective relay is included in power unit 6889 as described in Sect. 4, Chap. 5. This relay breaks the – 10V supply immediately the unit is switched off, thus cutting off completely the base drive to the output transistors. The decaying + 10V supply ensures that all the transistors remain cut off. The final condition, with zero volts on the bases of all the output transistors with power unit 12123 still providing full collector voltage, does not result in any appreciable dissipation; it is only the transitional state when a reduced negative drive is applied to the bases which can produce a dangerous condition.

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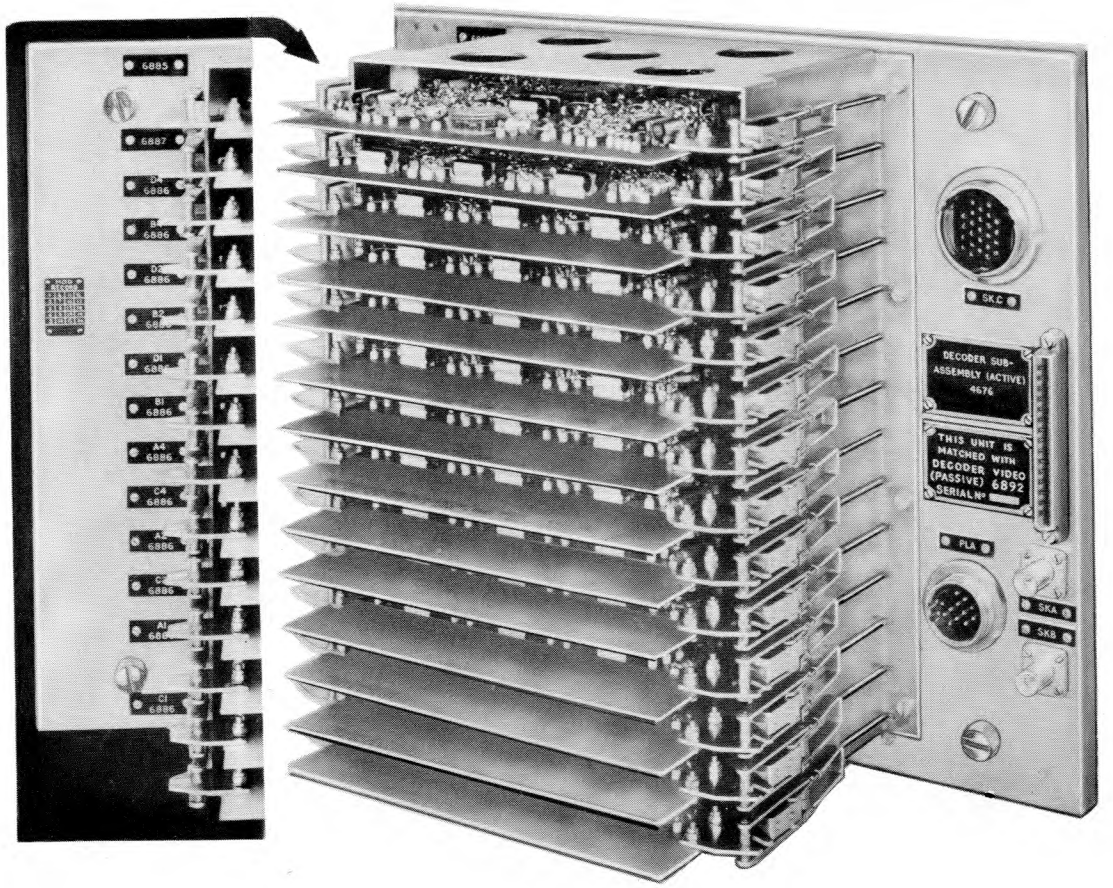

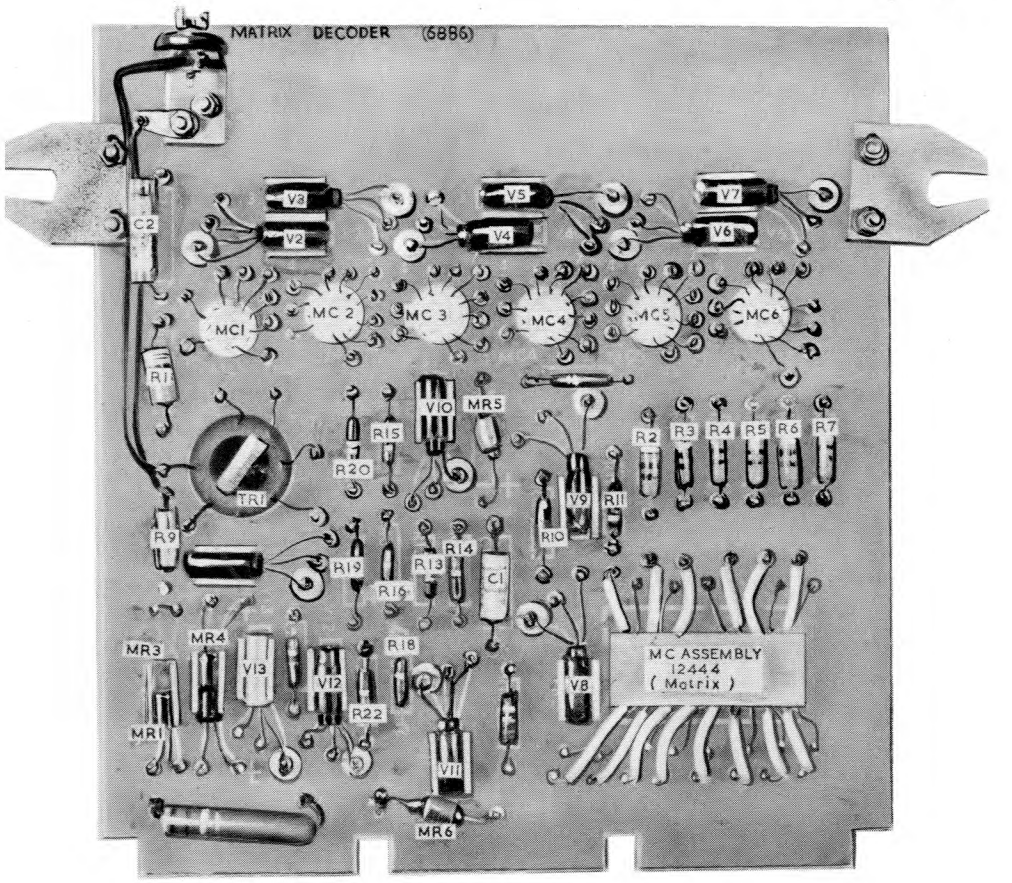

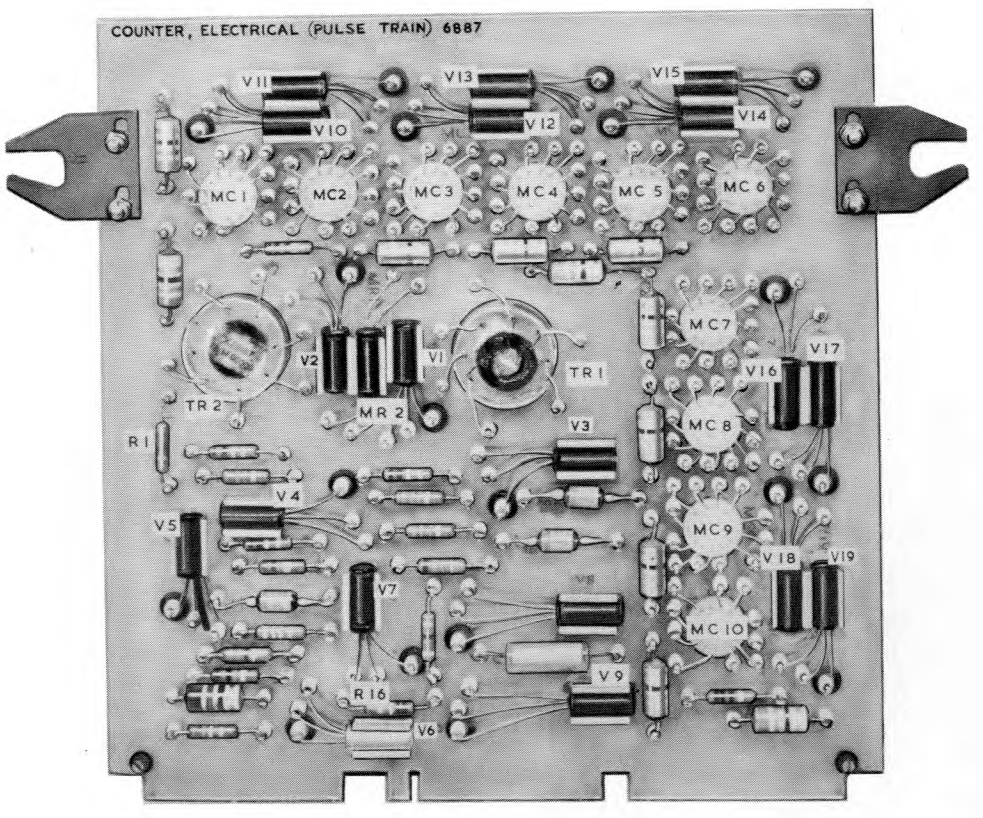

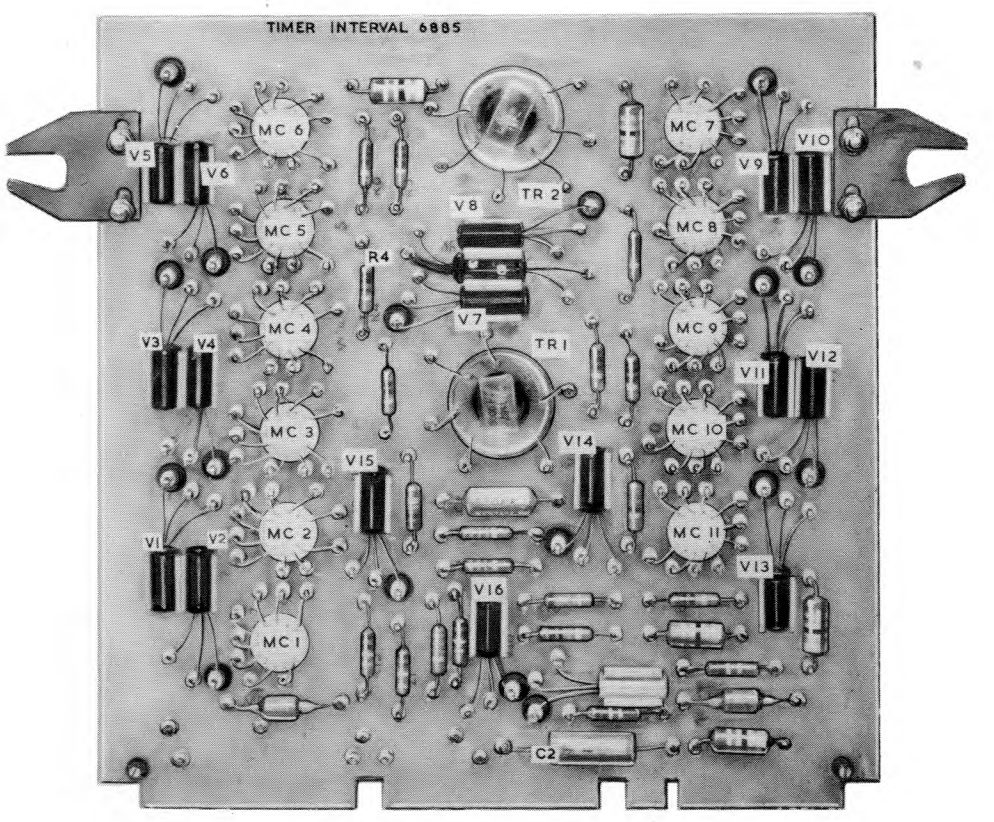

Fig. 11

Decoder, sub assembly (active) 4676

Fig. 11

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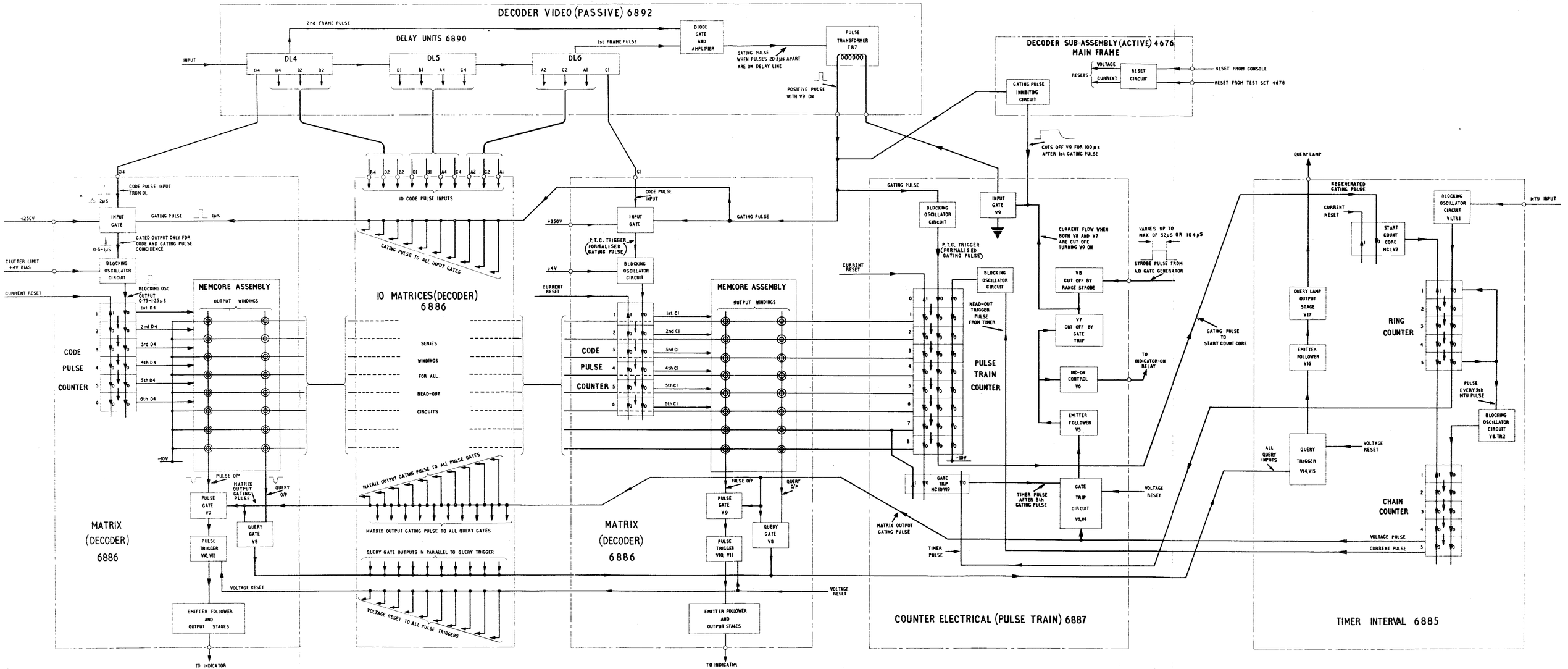

Fig.12

Decoder sub-assembly (active) 4676: block diagram

Fig.12

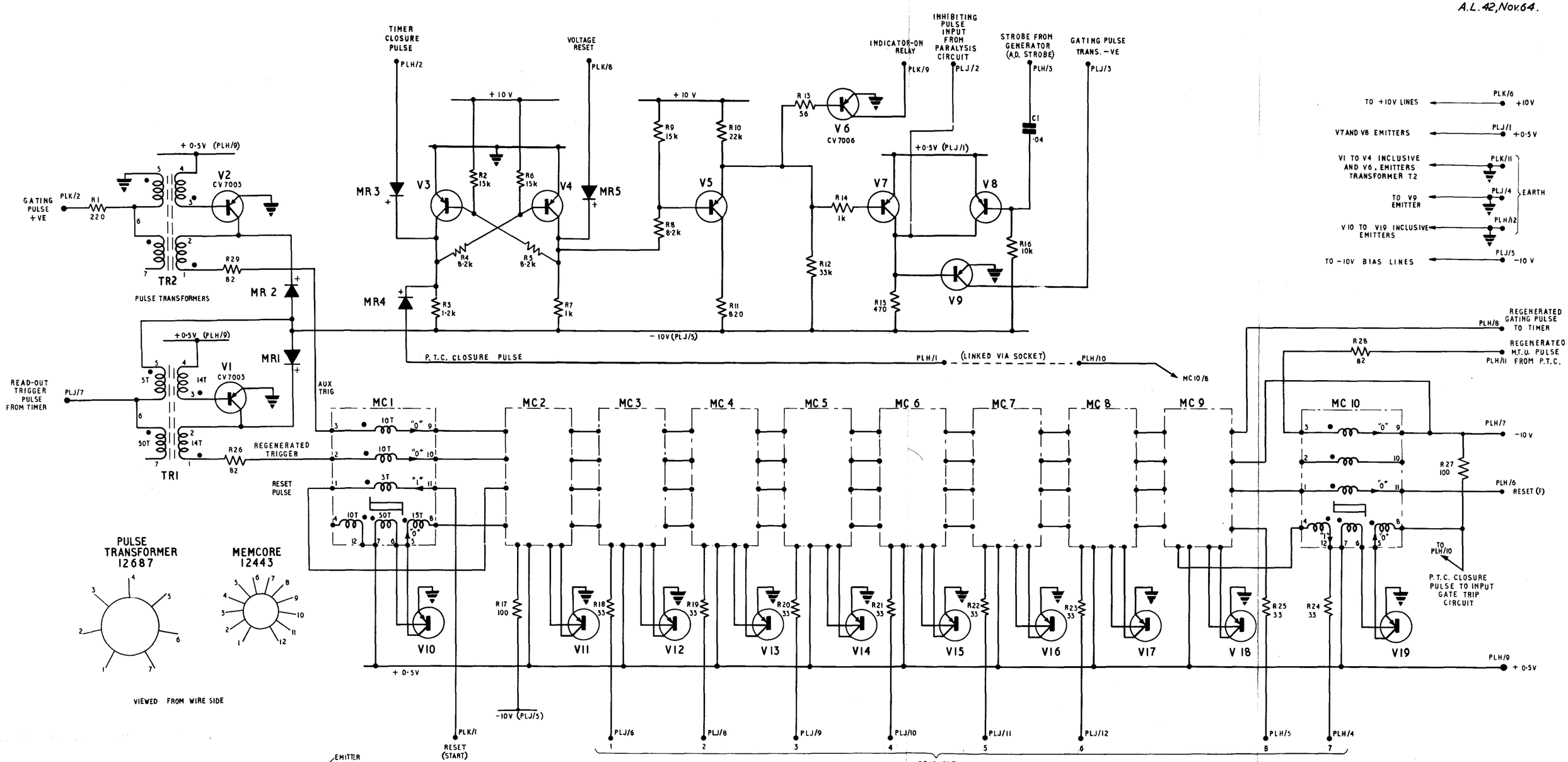

Fig. 13

Counter, electrical (pulse train) 6887 : circuit

Fig. 13

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PLP
9
+250V
R8 150k
CODE PULSE 1
MR1
GATING PULSE 3
MR2
C3 ·01
RV1 10k
2
+4V
TR
5
5T
6
50T
7
+0·5V
4
14T
3
V1 CV7005
2
14T
1
R1 82
MR4
−10V
REGENERATED GATED CODE PULSE

MC1
MEMCORE 12443
3
10T
"0"
9
2
10T
10
1
3T
"1"
11
4
10T
50T
15T
"0"
8
12
7
6
5

MC2
MC3
MC4
MC5
MC6
"0"
"1"
−10V
PLL/12 RESET
PLM/5 TEST O/P

R2 82
R3 82
R4 82
R5 82
R6 82
R7 82
V2
V3
V4
V5
V6
V7
+0·5V
+0·5V
C2 2
X1/4
X1/6
X1/7
X1/8
X1/9
X1/10
X1/11

X1
MEMCORE ASSEMBLY 12444
11 10 9 8 7 6 4
Q
P
12
5
−10V
RESET
28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13
11 10 9 8 7 6 5 4 3 2 1
12 11 10 9 8 7
PLL
PLM

PLM/4
GATING PULSE FROM TIMER
PLM/1
QUERY O/P
R10 100
1
V8
2
R11 100
3
V9
R12 15k
MR5
+10V
R15 15k
R14 15k
V10
V11
R17 8·2k
R16 8·2k
C1 220p
R13 1·2k
R18 1k
PLM/6
RESET (VOLTAGE)
MR6
+10V
R20 15k
R19 8·2k
+0·5V
R21 15k
V12
V13 CV7006
R22 1k
−10V
PLP/6 O/P TO INDICATOR
−10V LINES ← PLP/5
+10V LINES ← PLM/3
+0·5V LINES ← PLM/2

NOTE :— V2 V12 INCLUSIVE ARE ALL CV7004

MC1-6 MEMCORE 12443 VIEWED FROM WIRE SIDE

TR
PULSE TRANS 12687 VIEWED FROM WIRE SIDE
EMITTER
BASE
COLLECTOR
WHITE SPOT
V1-V13

MEMCORE ASSEMBLY 12444 VIEWED FROM WIRE SIDE

Fig. 14

Matrix (decoder) 6886: circuit

2042 281323 1280 5/63 VB 925/1

Fig. 14

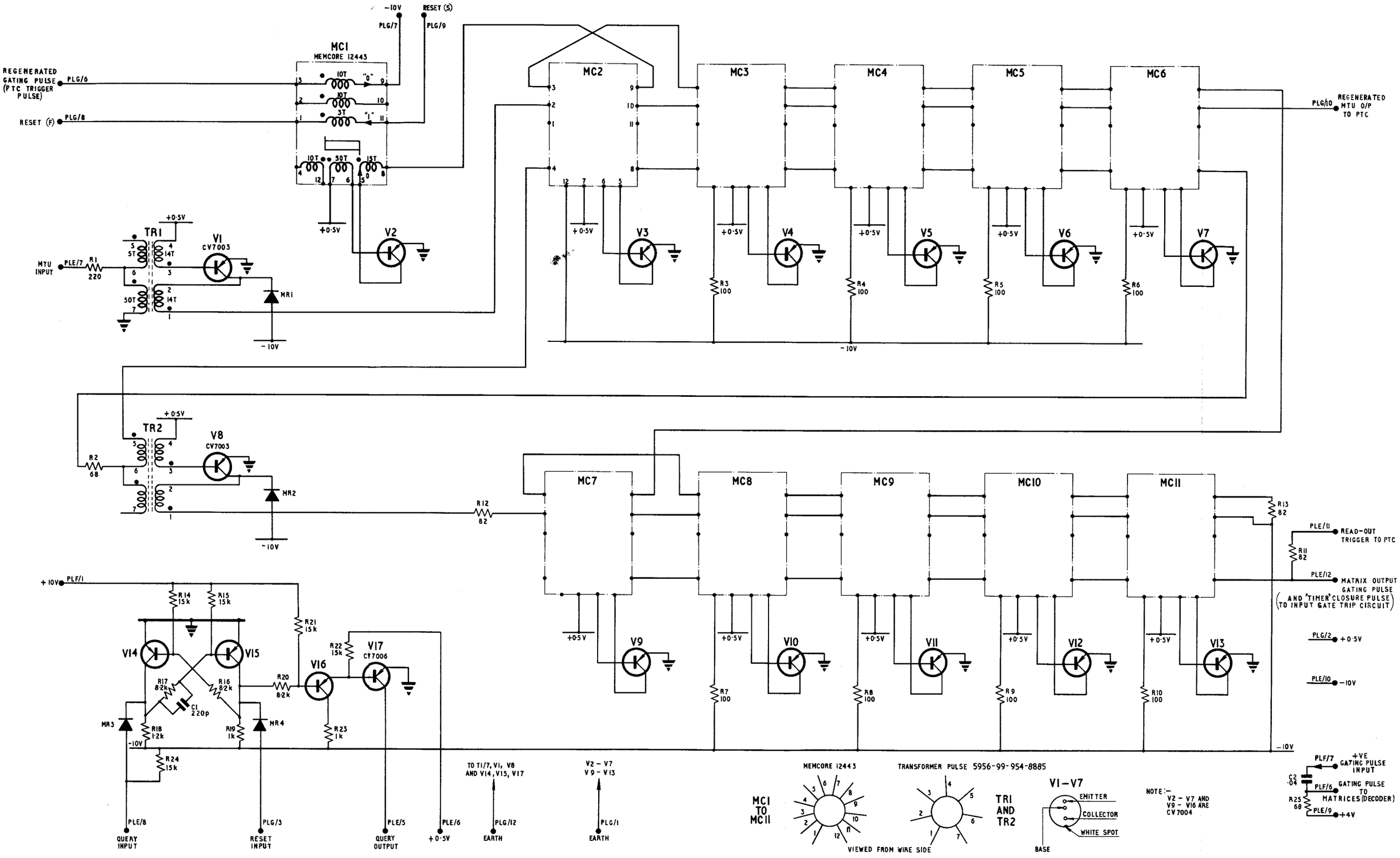

Fig. 15

Timer, interval 6885 : circuit

Fig. 15

Chapter 3.— RACK (A.D. STROBE) 12039

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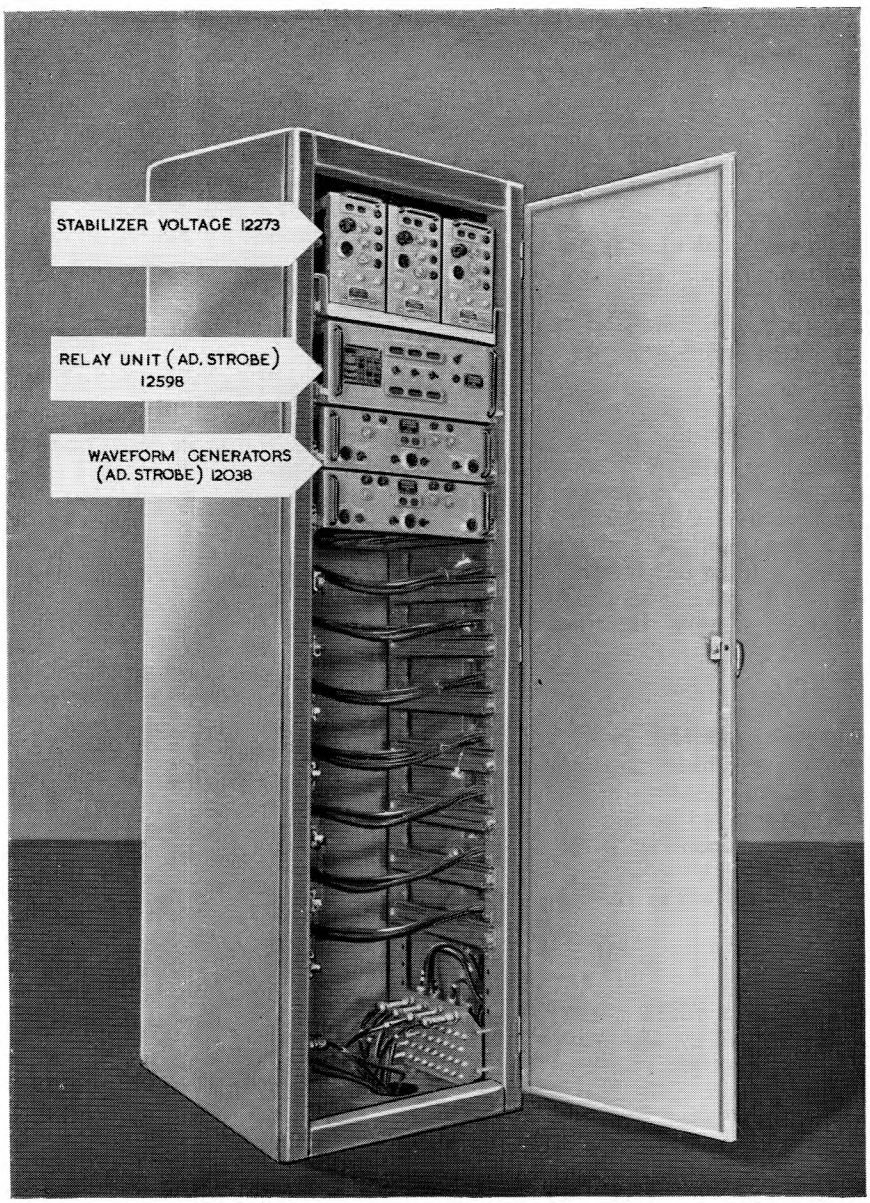

Fig. 1. Rack (A.D. strobe) 12039: general view

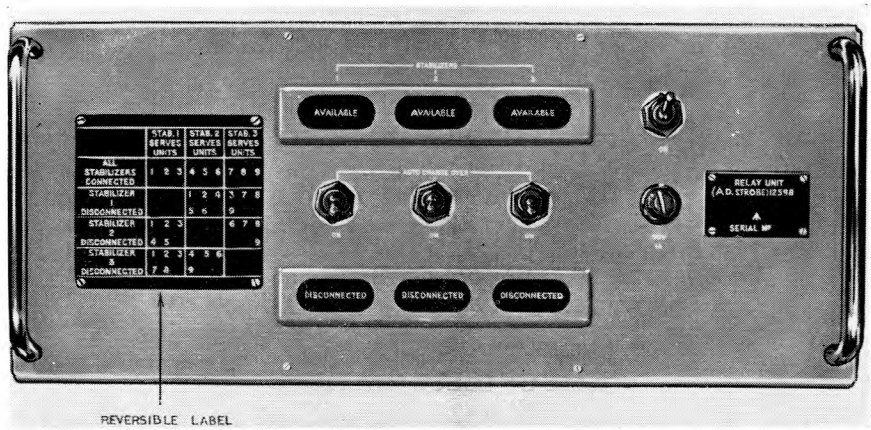

Fig. 2. Relay unit (A.D. strobe) 12598: front panel

General

1. Rack (A.D. strobe) 12039 houses the waveform generators (A.D. strobe) 12038 described in Chapter 4. It consists of a steel cabinet similar to the other SIF equipment racks in the radar office and can accommodate a total of nine waveform generators. In addition, space is available for up to three power supply units (stabilizers, voltage 12273) for the waveform generators and a relay unit (A.D. strobe) 12598 containing the control circuits.

2. The rack is illustrated in fig. 1 from which it will be seen that the stabilizers are mounted at the top with the relay unit immediately below. The remaining space is occupied by the waveform generators. Each unit is fitted on runners and the connectors are sufficiently long to enable the unit to be withdrawn for servicing in the operational condition.

3. The number of units mounted in the rack is dependent upon the facilities to be provided. Each waveform generator serves one console so that the number installed is determined by the number of consoles at which active decoding facilities are required. If more than nine consoles are to have active decoding, additional racks must be provided.

4. Each stabilizer, voltage 12273 is capable of supplying a maximum of five waveform generators but, if five or fewer waveform generators are fitted, two stabilizers share the load. When six or more waveform generators are installed, three stabilizers are provided. This arrangement ensures that, in the event of the failure of a stabilizer, the waveform generator load can be transferred to another unit. The necessary switching is done in the relay unit.

5. A wiring diagram of rack (A.D. strobe) 12039 is given in fig. 5. It should be noted that the numbering of the units in this rack constitutes a departure from the convention hitherto observed in the IFF Mk. 10 equipped whereby rack units are numbered from the bottom upwards. In rack 12039 numbering commences from the top, the right-hand stabilizer being unit 1.

Relay unit (A.D. strobe) 12598

6. The relay unit, illustrated in fig. 2, 3 and 4, consists of a front panel and framework on which are mounted twenty-seven relays controlling the power supplies to the various waveform generators. All relay springsets employed for switching the h.t. lines are shunted with resistance-capacitance networks to prevent arcing.

7. A circuit diagram of the relay unit is given in fig. 6. The 50V supply is fed in on PL1 (D) and (F), the positive pole being connected to one terminal of each of the relays A to AJ and to pin (E) of sockets SK6 to SK14. The negative pole is routed through SWD to pin (C) of sockets SK6 to SK14 so that the action of closing the switch makes the 50V supply available at all the waveform generators. At the same time the −50V line is fed out again via PL1 (C) to a rack (power distribution) 16650 to energize a relay which causes the 230V 50 c/s supply to be connected to PL1 (A) and (B).

8. The neutral pole of the 230V supply is taken direct to pin (B) of sockets SK6 to SK14 and the live pole, via springsets on relays A to J, to pin (A) of the same sockets. Thus, when the L.T. ON switch on a waveform generator is closed, the appropriate relay is energized and the 230V a.c. supply is fed to the heater transformer primary.

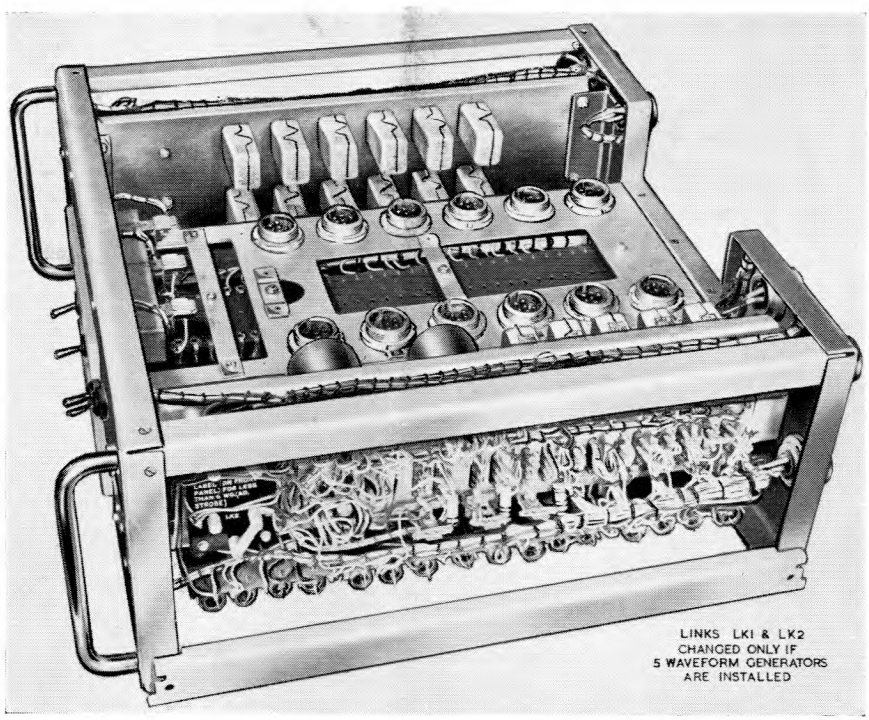

Fig. 3. Relay unit (A.D. strobe) 12598: right-hand interior view

9. The outputs from the voltage stabilizers are fed in on plugs PL3, 4 and 5 and taken to h.t. busbars from which connections are made, via relay contacts, feeding sockets SK15 to SK23. Provided the correct voltages from each stabilizer are present, relays T, U and V are energized, causing the changeover springsets to operate and illuminate the AVAILABLE indicator lamps LP1, 2 and 3. With relays K, M and O in the de-energized condition as shown in the circuit, each stabilizer supplies three waveform generators. By setting the H.T. switch on a waveform generator to ON, the appropriate relay (AA to AJ) is energized and h.t. supplies are fed to that unit.

10. The three switches SWA, B and C control the automatic changeover facility. With all three switches in the ON position, the failure of any one of the stabilizers causes the associated relay T, U or V to be de-energized, resulting in the corresponding AVAILABLE lamp being extinguished and relay L, N or P energized. When one of these relays is energized its contacts break the 50V circuit to the other two relays so that they cannot be energized and also cause the appropriate DISCONNECTED lamp LP4, 5 or 6 to be illuminated. Since the coils of relays K, M and O are connected in parallel with those of L, N and P, one of these relays will similarly be energized. Through the changeover springsets of K, M or O the load of the waveform generators, which were previously supplied from the now inoperative stabilizer, is transferred to the two remaining serviceable units, the distribution being indicated on the label affixed to the relay unit panel (*fig.* 2).

11. In the event of two stabilizers becoming unserviceable the automatic changeover system cannot operate when the second unit fails since its circuit is broken as a result of the first changeover. However, it is possible to vary slightly the choice of waveform generators remaining operational by setting to the off position the control switch of the first stabilizer which failed. For example, assume that stabilizer 1 fails so that the distribution becomes stabilizer 2 to waveform generators 1, 2, 4, 5 and 6 and stabilizer 3 to waveform generators 3, 7, 8 and 9. If stabilizer 3 subsequently fails, waveform generators 1, 2, 4, 5 and 6 continue to be supplied from stabilizer 2 but, by setting the control switch of stabilizer 1 to the off position, the changeover circuit associated with relay V will operate and the load on stabilizer 2 is then changed to waveform generators 4, 5, 6 and 9.

12. It will be observed that links are provided between the h.t. busbars and springsets 2 and 8 of relay K through which the h.t. supplies to waveform generator 3 are fed. These links are mounted on a small plate at the upper right-hand side of the unit just behind the front panel (*fig.* 3). When less

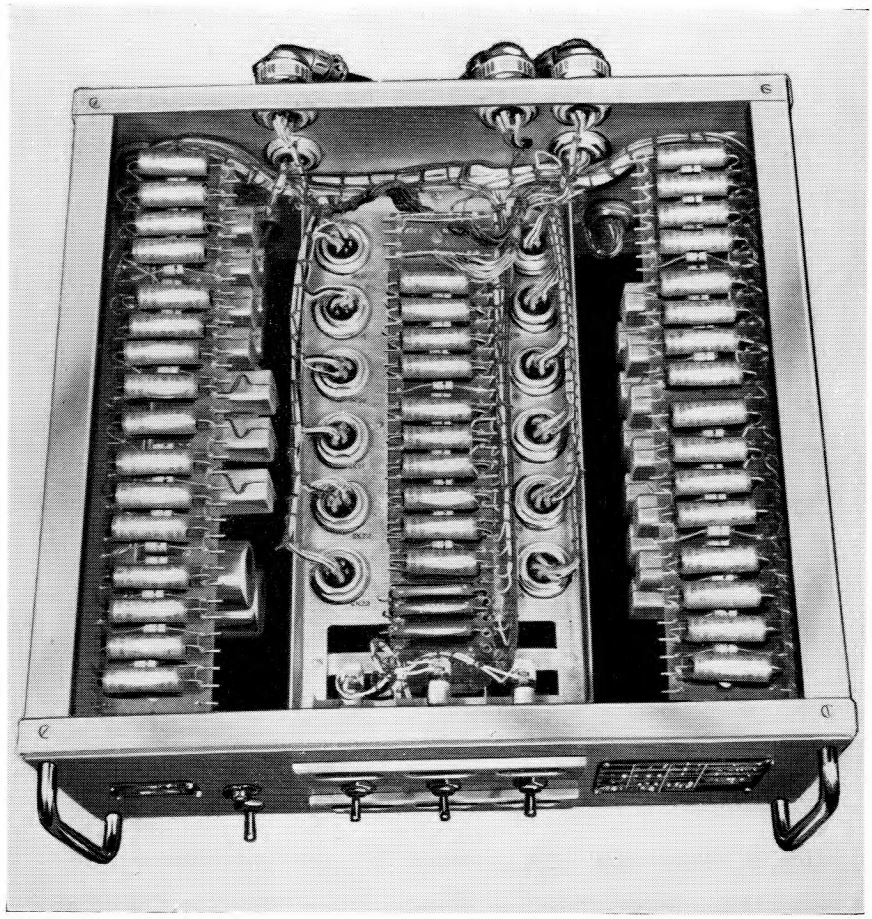

Fig. 4. Relay unit (A.D. strobe) 12598: underside interior view

than six waveform generators are installed in the rack only stabilizers 1 and 2 are fitted so that, with the links in the normal position, waveform generator 3 becomes inoperative should stabilizer 1 fail. To allow the load to be transferred to stabilizer 2, the links must be moved to connect the normally open relay contacts of the changeover circuit to the stabilizer 2 busbars.

13. If less than six waveform generators are installed, the normal procedure is to reverse the panel label and change over the links but movement of the links is only essential for the specific condition of five waveform generators in a rack. In this event the waveform generators are mounted in positions 1, 2, 3, 4 and 5 (i.e. rack positions 5, 6, 7, 8 and 9) and the links must be moved to ensure that the changeover circuit can transfer the load of waveform generator 3 to stabilizer 2 if stabilizer 1 fails.

14. For less than five waveform generators movement of the links is not essential since the positions for waveform generators 1, 2, 4 and 5 may be used. When a rack contains six or more waveform generators they may be installed in any order and all three stabilizers must be provided.

15. The control leads from the active decoder switches on the consoles to the boundary marks on/off relays in the waveform generators are also routed via the relay unit. These leads are terminated in socket SK2 which engages with PL2 and from PL2 connections are taken to the waveform generators via pin (F) of sockets SK6 to SK14.

Stabilizer, voltage (marker sequence) 12273

16. This is a standard unit employed in other racks in the radar office and is fully described in A.P.2527X. It contains a safety circuit which ensures that if the +300V supply deviates from its nominal value, both supplies are switched off. Thus, although the changeover circuit in the relay unit is operated only by the negative supply, any fault on the positive line causes both inputs from the stabilizer to disappear.

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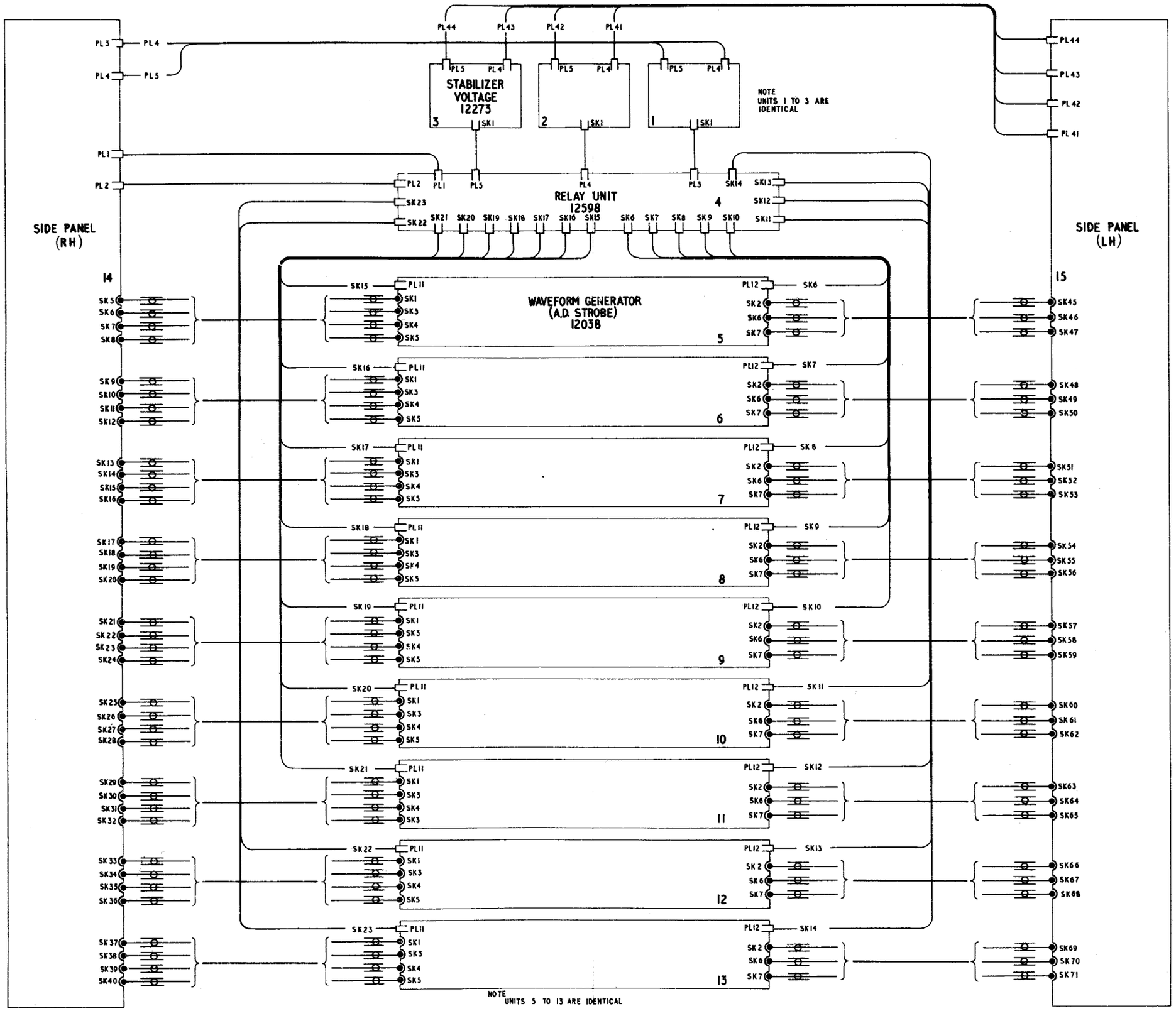
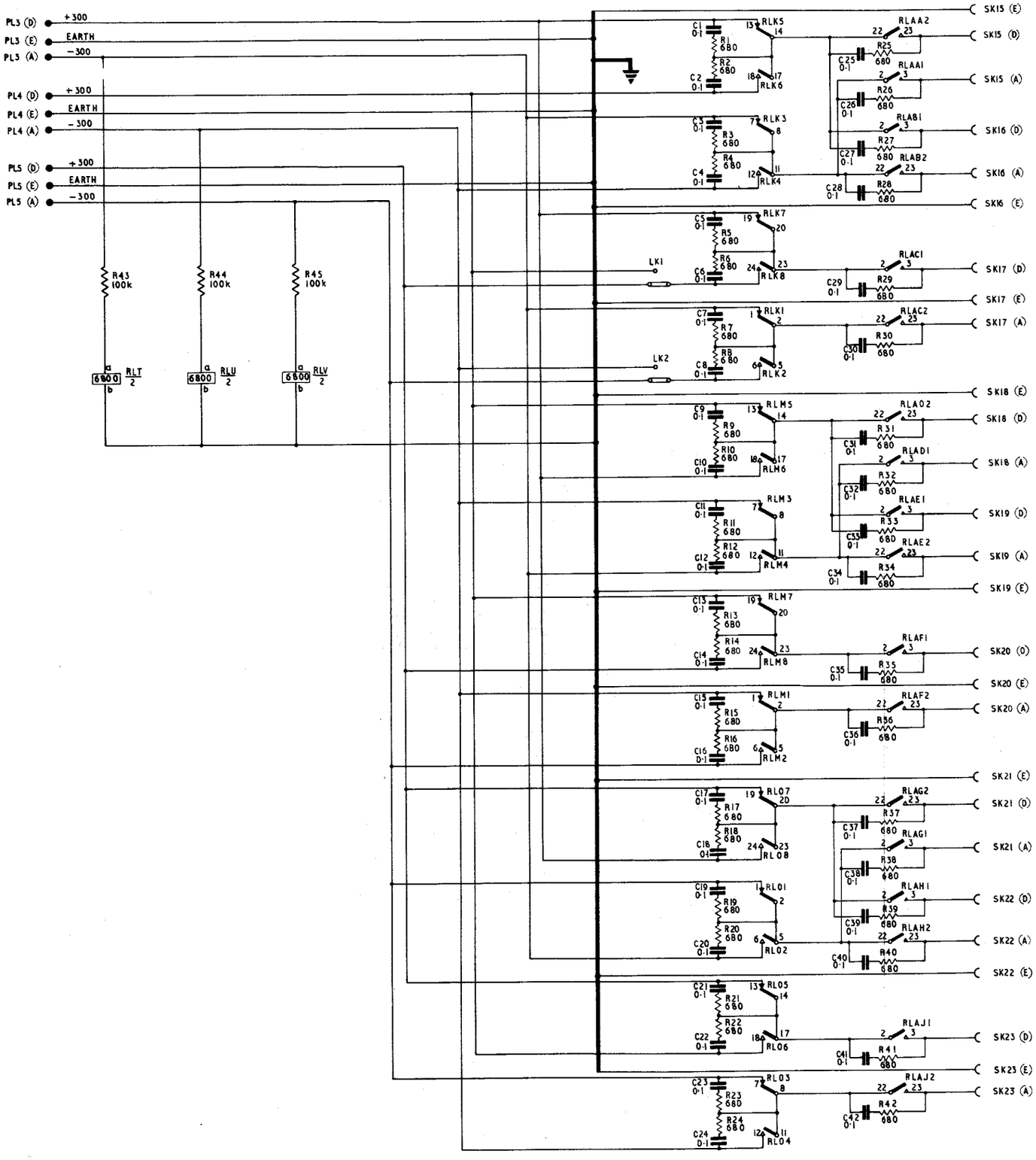


Fig. 5 924/8/4793/56563/625/3/61 J. T. & S. Rack (AD strobe) 12039 : interconnections Fig. 5



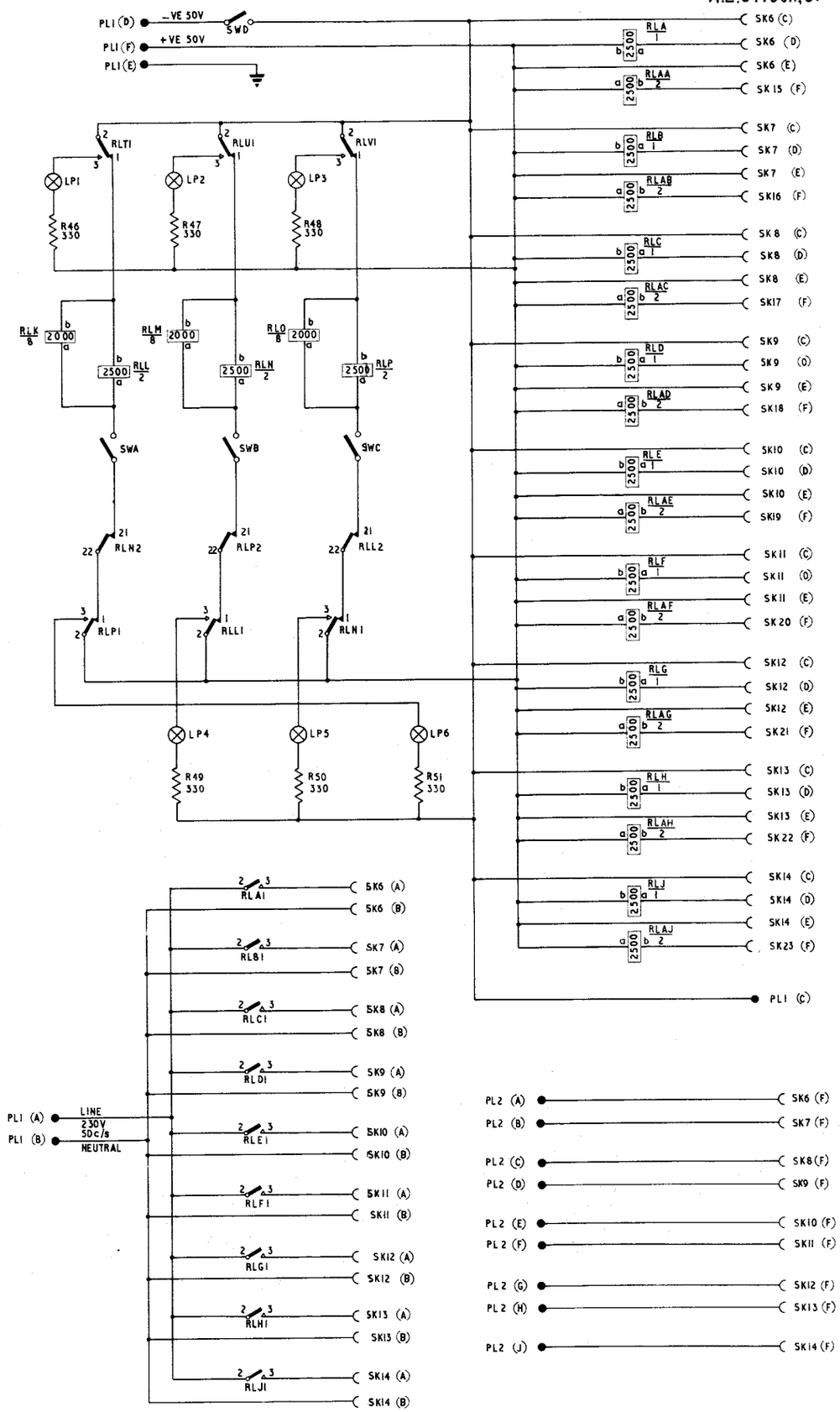


Fig.6

924/8/4793/56563/625/3/61 J. T. & S.

Relay unit (AD strobe) 12598 : circuit

Fig.6

Chapter 4

WAVEFORM GENERATOR (A.D. STROBE) 12038

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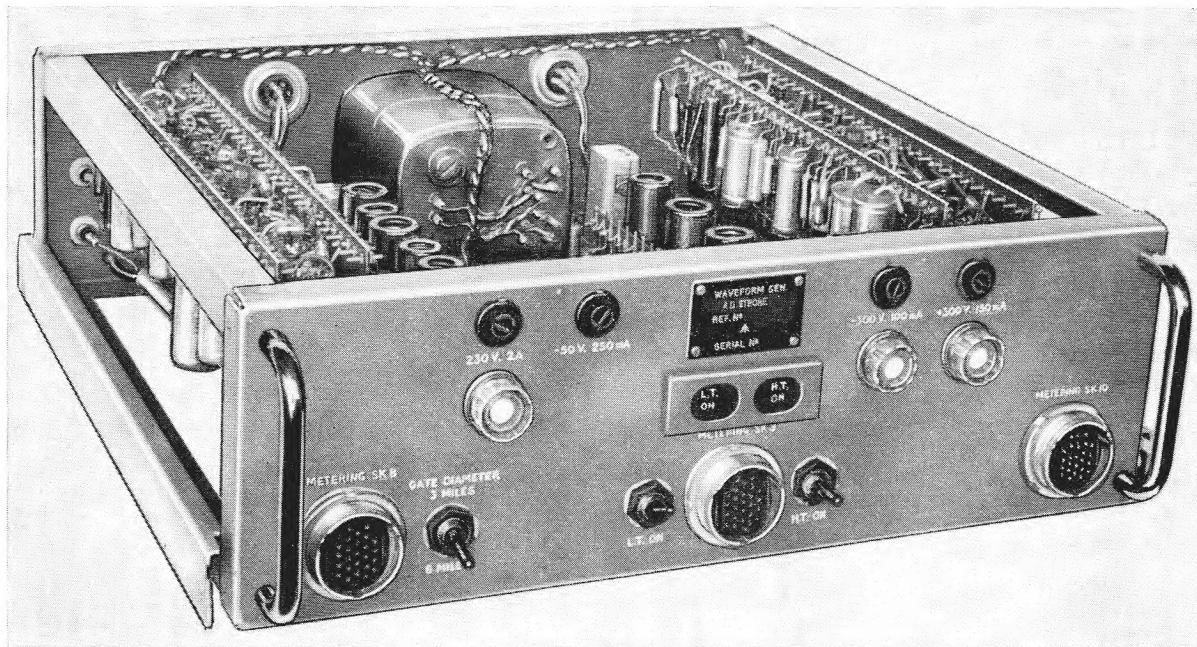

Fig. 1. Waveform generator (A.D. strobe) 12038: general view

Introduction

1. In order that the active decoder may accept only the response which it is desired to decode, a range strobe pulse must be produced to ensure that the decoder is operative only during the period when the response is received. The necessary waveform is generated by waveform generator (A.D. strobe) 12038 and applied to the active decoder main input gate.

2. The input to the waveform generator is derived from an amplifying unit (mixing) 4428 (A.P.2527X) and is a composite waveform consisting of the timebase sawteeth for the X and Y axes and the intertrace marking waveforms. At the appropriate point on the timebase sweep the amplitudes of the sawtooth and joystick voltages are proportional to the range of the required response. When each sawtooth voltage differs from the corresponding joystick voltage by more than a predetermined amount, a pulse is produced and when the pulses from the X and Y channels overlap the IFF strobe is generated for the active decoder.

3. Thus, the strobe is generated from pulses produced for each axis as the result of amplifying a small portion of the timebase sawtooth, the mid-point of the voltage excursion being determined by the corresponding joystick voltage. In addition, the waveform generator provides a marker waveform which the operator can display on the PPI to indicate the strobed area.

General description

4. Waveform generator (A.D. strobe) 12038, illustrated in fig. 1 and 2, includes a rack panel and a back plate, spaced apart and secured together by angle strips at the four corners. The valve decks are formed of narrow channel-section strips bolted to brackets welded to the panel and back plate. Tagboards carrying the small components are secured to the valve decks. Slides, fixed to the lower sides of the assembly, engage with runners in the rack and allow the unit to be fully withdrawn. This, together with the open form of construction, facilitates servicing in situ.

5. Plugs and sockets for the input and output connections are mounted on the back plate. The sockets on the panel are provided for metering purposes only.

6. The waveform generator is housed in a rack (A.D. strobe) 12039 which can accommodate a total of nine such units together with a relay unit (A.D. strobe) 12598 and three stabilized power units (stabilizer, voltage 12273) supplying the h.t.

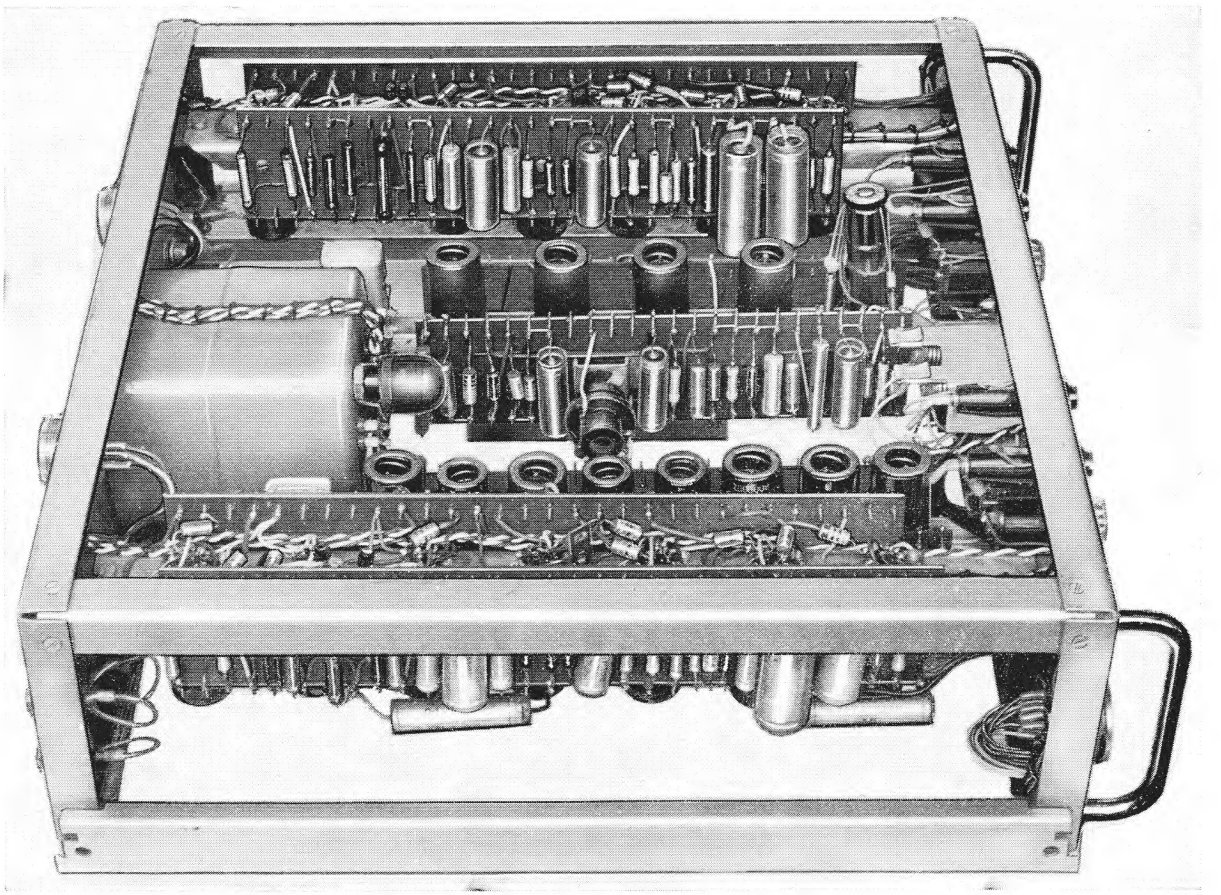

Fig. 2. Waveform generator (A.D. strobe) 12038: underside view

requirements of the waveform generators. Each waveform generator has an independent heater transformer incorporated.

7. A block diagram of the waveform generator is given in fig. 3. To assist in following the operation of the unit, this diagram should be studied in conjunction with fig. 4 which shows a typical waveform sequence from amplifying unit (mixing) 4428.

8. Considering one axis only, the composite input waveform is first applied to an amplifier with a gain of approximately 60 times. Limiting of the voltage excursions occurs on both positive and negative peaks, giving an output waveform similar to fig. 4 (5). Thus, the stage can amplify only that portion of the input signal which lies between two voltage limits, the mid-point being determined, as explained in the next paragraph, by the joystick voltage.

9. The joystick voltage is fed into a store which incorporates an automatic zero correction system similar to that employed in mixer 4428. Briefly, the store accepts and holds the joystick voltage for a number of successive recurrence periods. At intervals of 40ms, a pulse, derived from pulse generator (dekatron) 4425 in rack (marker sequence) 4195 and occurring at the time the joystick voltage is present in the composite waveform, is applied to a sampling pulse generator together with the inter-trace bright-up pulse. The resultant pulse, produced as the result of coincidence of these two waveforms, opens the joystick store gate. If any change has occurred since the last sampling pulse was applied, the store then charges or discharges to the new voltage, determining the mid-point of the input amplifier aperture. In this way the zero d.c. level is maintained and variations in the strobe timing due to drift are removed.

10. The dekatron is triggered by each recurrence pulse and counts down to one-tenth of the recurrence frequency so that pulses for ten different services are produced in sequence. One of these pulses is always used for automatic zero correction (a.z.c.) and nine are available for gating inter-trace marks to the PPI. It should be noted that, although in this chapter sequence 3 is shown as the IFF pulse, the only requirement is that a dekatron pulse for any one service should recur at intervals of 40ms. In general, the same dekatron pulse sequence is always used for a.z.c. purposes but the IFF pulse at a particular console may be any one of the other nine, depending upon the installation wiring.

11. Although the waveforms of one inter-trace period only are of consequence within the waveform generator, the console joystick in fact controls two consecutive inter-trace waveforms as shown in fig. 4. The first, with sine wave modulation, is employed to paint the ring marker on the PPI and the second, which is unmodulated, is used in the waveform generator.

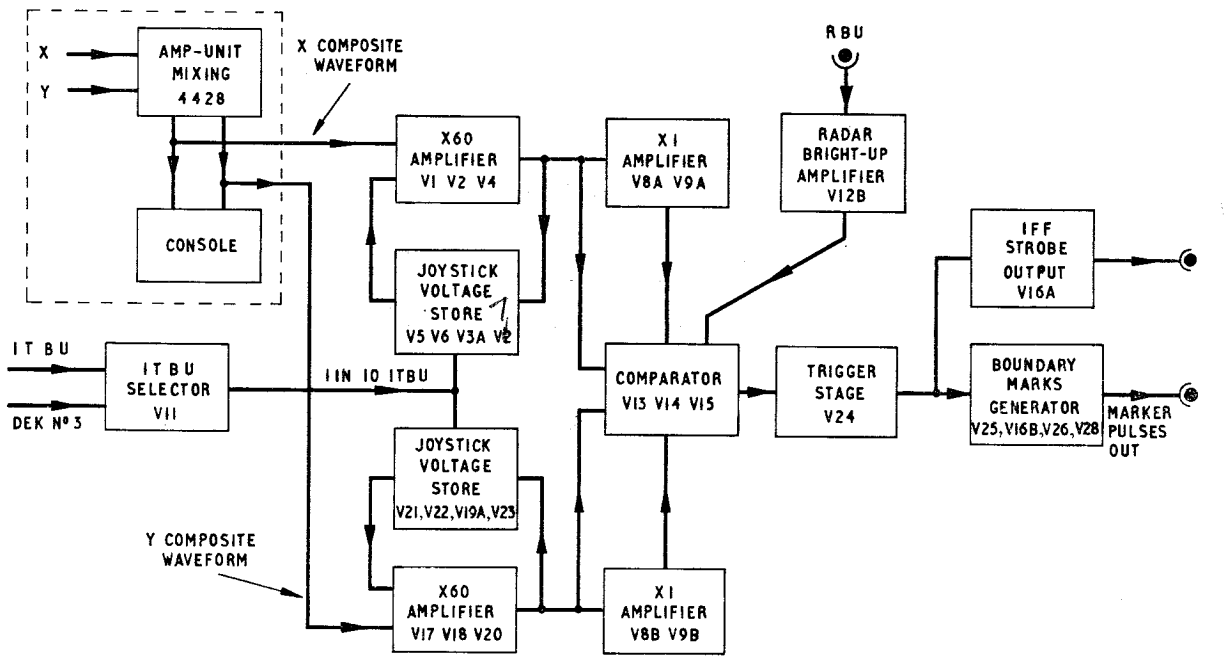

Fig. 3. Block diagram

12. The output from the ×60 amplifier is passed to a further amplifier with a gain of unity for negative-going inputs. Amplitude limiting occurs with positive-going inputs, allowing only the useful portion of the output waveform to be passed to the succeeding stage.

13. The outputs of the ×60 amplifiers and the inverted waveforms from the unity gain amplifiers for both X and Y channels are fed to the anodes of four adding diodes whose cathodes are taken to a common point at the cathode of the comparator valve. When any one of the four wave forms is

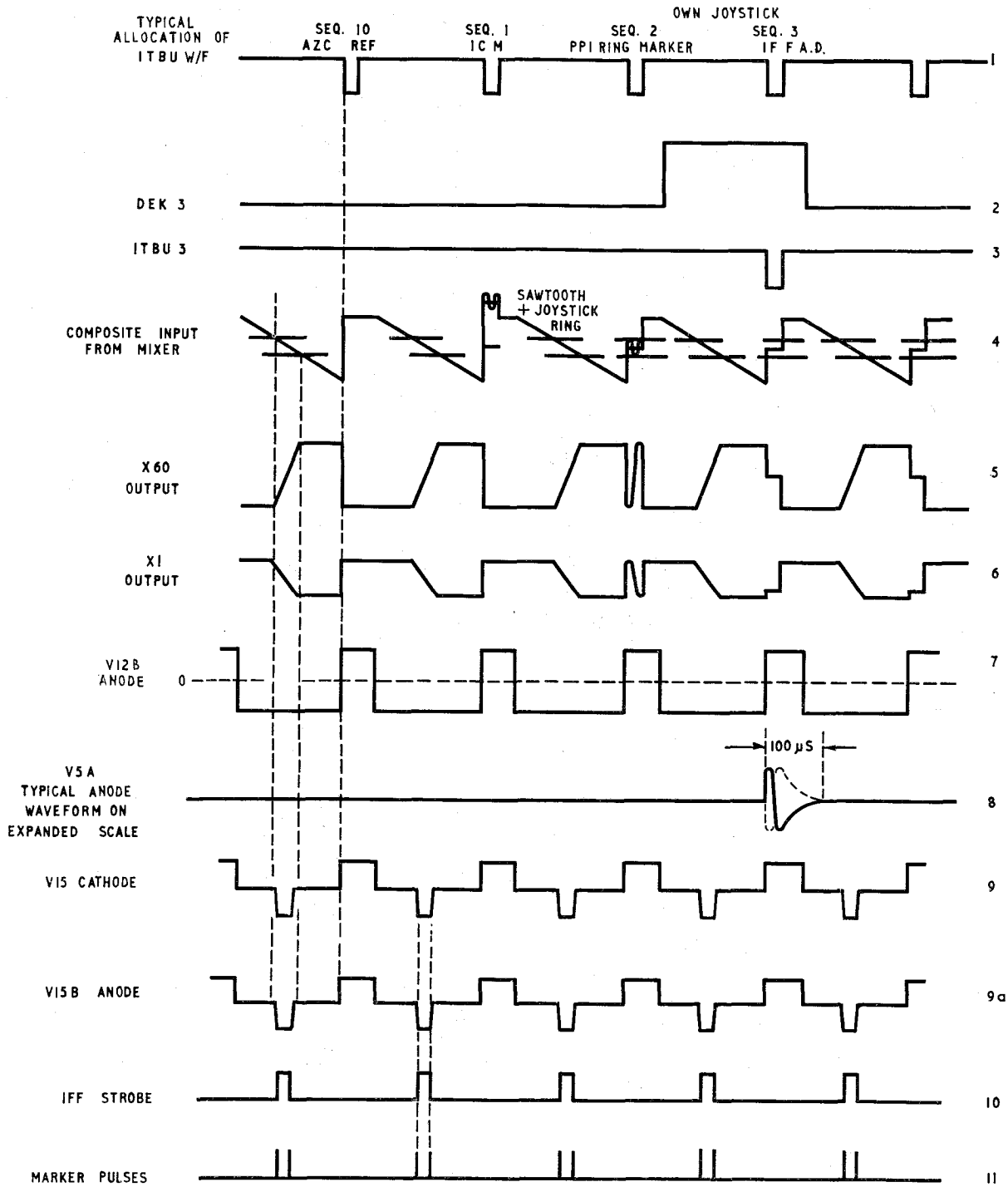

Fig. 4. Typical waveforms

more positive than the other three, the associated diode conducts and causes the comparator valve to be cut off. During the period when all four diodes are cut off, the comparator stage conducts and produces an output pulse whose duration is determined by a comparison voltage applied to the grid. Two values of d.c. potential are provided, either of which may be selected, allowing a strobe to be produced corresponding to 3 or 6 nautical miles in length.

14. The negative-going output from the comparator is applied to a trigger stage which is a regenerative pulse amplifier and phase splitter, delivering positive and negative outputs corresponding to the input waveform. The positive-going output from the trigger stage is fed to a cathode follower and thence to the output socket.

15. The comparator is suppressed for the inter-trace period by the application of a blanking waveform derived from the radar bright-up pulse.

16. The boundary marks generator consists of a ringing stage and a cable-drive amplifier. Both the positive and negative-going outputs from the trigger stage are differentiated and applied to the ringing stage which produces half sine waves of 1μs duration. These are then fed to the cable-drive amplifier whose output consists of positive-going pulses of well defined amplitude and with fast edges suitable for feeding direct to the passive decoder.

CIRCUIT DESCRIPTION

General

17. Each waveform generator has separate amplifiers and joystick voltage stores for the X and Y channels, the remainder of the circuit being common to both channels. In the following description only the X axis is considered and the circuit references derived from fig. 8 relate to this channel. The circuit and operation of the Y amplifiers and joystick voltage store are identical.

×60 amplifier

18. This is a normal voltage feedback amplifier consisting of a double-triode valve V1 connected as a cathode-coupled amplifier, a pentode amplifier V2 and a cathode follower V4. The input arm (R1) is 100 kilohms and the feedback arm (R22) is 6·8 megohms, giving an overall gain of approximately 60 times.

19. As stated in para. 8, the ×60 amplifier operates linearly over only a small amplitude range of the applied composite waveform, the centre of the range being determined by the particular value of voltage present at the cathode of the store valve V7. This voltage sets the potential at the grid of V1A and thereby, through the negative feedback action via V2, V4 and R22 together with the common cathode coupling of V1, determines the virtual earth potential at the grid of V1B. As explained in subsequent paragraphs (*para.* 23 *et seq.*) the inter-trace voltage level corresponding to the joystick voltage causes V7 cathode to take up such a potential that the virtual earth at V1B grid just equals this inter-trace level.

20. The composite waveform from amplifying unit (mixing) 4428 is fed in at SK1 and applied to V1B grid. The resultant change in grid potential due to the timebase sawtooth produces a corresponding change in the common cathode potential, and hence in the current through V1A. Thus, depending upon the polarity of the sawtooth, V1A anode moves in a positive or negative direction, in phase with the input. The waveform developed at V1A anode is applied to the grid of V2 through R8 with R10 returned to −300V to ensure the correct d.c. level at the grid of V2. C2 is included to improve the a.c. response.

21. V2 is a pentode amplifier which, in conjunction with the cathode follower V4, the diodes V29 and V30 and a secondary feedback loop to V2 grid, limits the portion of the timebase sawtooth that is amplified. Its anode is coupled to V4 grid through R15 with R14 returned to −300V to set the level at V4 grid. A.C. compensation is again provided through C3.

22. V4 cathode is taken to a resistive network R17, R18, R20 and R21 between +300V and −300V. The diodes V29 and V30 are also connected to the network and returned to V2 grid which is normally at approximately earth potential. Thus, when the voltage at the junction of R17, R18 rises above earth or that at the junction of R20, R21 falls below earth, the corresponding diode conducts and a feedback voltage, in antiphase with the input, appears at V2 grid. As a result, the output at V4 cathode consists of an amplified portion of the timebase sawtooth centred about earth, the limits of the positive and negative excursions being defined by the voltages at the junctions R17/R18 and R20/R21.

Joystick voltage store

23. The joystick voltage store consists of a gating stage formed by the double-triode valves V5 and V6, a triode amplifier V3A and a cathode follower V7. During the storage time, i.e. the 40ms which elapses between the appropriate dekatron pulses, V6B is cut off by the negative voltage derived from the junction of R25, R26 and all the current through the stage is taken by V6A whose grid is returned to the junction of R24 and R25. As a result, no current can flow in V5, the potentio-

meter chain R29, R27 ensuring that the cathodes of V5 are biased positively without exceeding the heater/cathode voltage rating.

24. The gating waveform which operates V6 is derived from the inter-trace bright-up (ITBU) pulse. Negative-going ITBU pulses, approximately 18V in amplitude, are fed in at SK3 and thence to the grid of V11A, one half of a double-triode valve connected as a cathode-coupled amplifier. V11A grid is taken to +5V at the junction of R67, R68 while the positive excursion of V11B grid is clamped at earth potential through the action of the diode-connected triode V12A, the normal potential (supplied externally via SK4 and R75) being −30V. Thus, all the current through the stage is taken by V11A. When ITBU pulses are applied to V11A grid the anode current falls and the cathode potential falls correspondingly by approximately the grid swing of V11A, i.e. 18V. However, since VIIB grid is at −30V that valve remains cut off.

25. At intervals of 40ms, the appropriate dekatron IFF pulse, starting at −30V and rising to +40V, is fed in at SK4 and then, via R75, to the grid of V11B. During the positive excursion of this waveform V11B grid is held at earth potential with the result that the arrival of the negative-going ITBU pulse at V11A grid causes a current of about 2mA to flow in V11B. V11B anode waveform is then a negative-going pulse approximately 13-14V in amplitude.

26. V11B anode is coupled, via C7, to the grid of V6A. Thus, when a pulse appears at V11B anode, V6A is cut off so that the current through the common cathode load R35 is diverted to V6B, the path from h.t. being completed through V5A and/or V5B depending upon the potential applied to V5B grid. A further result of V6A being cut off is that a positive-going waveform is developed across the anode load R36. A proportion of this waveform also appears across the anode load of V5A due to the coupling components R32 and C42, the capacitor compensating for stray capacitance at V5A anode. The actual resultant waveform appearing at V5A anode due to the positive coupled waveform and to the pulse current flowing through V5A itself depends upon the value of the pulse current which is controlled by the potential applied to V5B grid.

27. Since the waveform at V5A anode occurs during the IFF/A.D. inter-trace period selected by the dekatron equipment, the current waveform present at V5B grid represents the difference between the joystick voltage component of the composite input waveform and the stored joystick voltage. The parameters of the circuits of V5 and V6 are so chosen that when the difference is zero, i.e. V5B grid is at earth potential during this point on the composite waveform, the amount of current through V5A is just sufficient to balance out the coupled waveform from V6A anode circuit. If the stored voltage is too high, the potential at V5B grid rises above earth potential, the proportion of pulse current through V5A falls and the coupled waveform from V6A anode circuit is able to assert itself as a positive corrective waveform at V5A anode. Similarly, if the stored voltage is too low, the converse applies; the pulse current through V5A increases and there is then a negative correction waveform at the anode.

28. The output from V5A anode is fed, via C6, to the grid of V3A. In this stage the waveform is amplified and inverted and then applied, through C8 and a metrosil MR1, to the storage capacitor C11 in the grid circuit of the cathode follower V7. The impedance of the metrosil is dependent upon the voltage across it, e.g. it is 12 kilohms at 60V and 10 megohms at 1V. To ensure a small voltage drop across the metrosil in the storage condition, it is included in a negative feedback loop around V7 by feeding part of the cathode voltage back through R47. In consequence, the standing potential across MR1 is small, it has a high impedence and leakage is negligible.

29. Any movement of the joystick will bring about a state of unbalance between the joystick voltage component of the composite input waveform and the joystick voltage stored by C11. As described in para. 27, the result is that a corrective pulse of the appropriate sign appears at V5A anode. This pulse, through the inverter amplifier V3A and the metrosil MR1, charges or discharges C11 until balance is regained.

30. V7 cathode, the potential of which is proportional to the joystick voltage, is coupled to V1A grid. Since the composite input waveform is applied to V1B grid then, during the inter-trace period, V1B anode waveform is a measure of any difference between the stored voltage and the joystick voltage component of the input waveform. It is this difference which is amplified and used to correct the store, so completing the automatic zero correction system mentioned in para. 9. Thus, the composite waveform at V4 cathode is always so biased that both the inter-trace joystick voltage and the sawtooth waveform voltage are at approximately earth potential. The feedback circuit maintains the sawtooth at earth and the stored potential ensures that the joystick voltage remains at earth.

31. The series resistor R7 is included to limit the demand on V7 for cathode current and prevent the possibility of the valve running into grid current since this would slow down the rate at which the store attains its final potential.

Unity gain amplifier

32. This stage consists of a triode amplifier V8A d.c. coupled to a cathode follower V9A. The input is fed via R54 and V9A cathode is coupled back to the input through R60 and R64. The resultant negative feedback reduces the stage gain to approximately unity for negative inputs but, due to the action of the diode V10A shunting the feedback resistors, the stage gain for positive inputs is reduced almost to zero. The limiting action commences when the negative-going output waveform falls below the operating potential of V8A grid,

say −4V. That is, limiting occurs for all points on the input composite waveform more positive than 4V. V10A is included for the purpose of restricting the voltage swing at V8A anode, thus avoiding the possibility of grid current and consequent disturbance of the d.c. conditions.

Comparator stage

33. The output from V4 cathode is fed to one anode of the double-diode V13 and the antiphase waveform from V9A cathode is applied to one anode of V14. The outputs from the corresponding Y amplifiers are fed to the other anodes of the diodes. All four diode cathodes are connected together and returned to a common point at the cathode of V15. V15B grid is taken to a positive potential at the junction of R88, R89 and the cathode is at approximately the same potential due to the voltage drop across R85. For a square with 3-mile sides V15B grid voltage is about 16V and for a 6-mile square it is about 36V.

34. The outputs from the ×60 and unity gain amplifiers vary in amplitude sinusoidally as the radar aerial rotates. In consequence, the outputs from the X amplifiers are in quadrature with the outputs from the Y amplifiers. Since the output from the X channel ×60 amplifier is in antiphase with the output from the unity gain amplifier and similar conditions apply to the Y amplifiers, it will be seen that, at any point during the rotation of the PPI trace, the anode of at least one of the four diodes will be at a positive potential due to the applied waveform.

35. The operation of the comparator circuit may be more easily followed by reference to fig. 5. Considering this diagram, which shows the conditions on the east-west axis when there is no Y component, it will be observed that, initially, the output from the X channel ×60 amplifier holds the anode of V13A positive so that the diode is conducting. This produces a rise in the common cathode potential of V13 and V14, bringing about

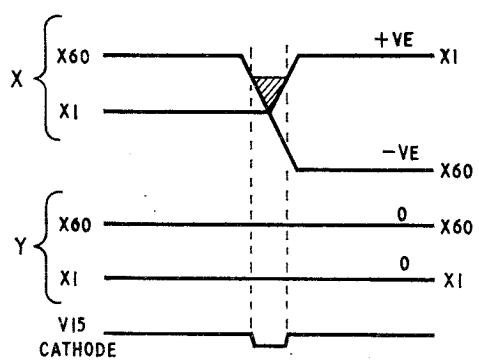

Fig. 5. Comparator input waveform on east-west axis

a corresponding increase in V15 cathode potential and causing V15B to be cut off. During the negative excursion of the applied waveform, V13A anode potential falls and a similar fall in voltage occurs at V15 cathode until the bias level maintained at V15B is reached. At this point V13A is cut off and V15B conducts. V15B continues to conduct until the positive excursion of the antiphase waveform from the unity gain amplifier, applied to V14A, causes that diode to conduct and the resultant rise in the common cathode potential cuts off V15B again. Thus, V15B conducts during the period indicated by the shaded triangle in fig. 5 and a negative-going pulse, approximately 38V in amplitude, is developed at the anode. The duration of this pulse is determined by the length of the base of the triangle which, in turn, is controlled by the d.c. potential applied to V15B grid.

36. Similar conditions apply at other positions of the trace when both X and Y components are present provided the transitions from positive to negative and from negative to positive for both channels overlap. If this does not occur there can be no output from V15B since one or other of the diodes will always be conducting. Fig. 6 illustrates the generation of the strobed area on the PPI and fig. 7 shows the X and Y transition waveforms applied to the comparator for the corresponding trace vectors.

37. It will be noted from fig. 7 that the duration of the negative pulse developed at V15 cathode is variable, depending upon the relative timing of the two transition waveforms which generate it. This duration is proportional to the length of the trace vector between the two points at which it cuts the square strobed area (*fig.* 6).

38. At this point it is necessary to consider the function of V15A. Normally, the valve is cut off since its grid is at earth and it has no effect on the operation of the comparator stage.

39. The radar bright-up waveform which is a rectangular pulse, positive-going during the time-base period and nominally 2V in amplitude, is fed in at SK5 and thence, via C14, to the grid of V12B. V12B cathode is connected to earth so that d.c. restoration occurs at the grid due to the flow of grid current; the positive excursion of the input waveform is therefore restored to a level of about −1V.

40. At the start of the bright-up waveform the anode of V12B falls and at the end of the trace period it returns in a positive direction. The negative-going waveform thus developed at the anode is approximately 70V in amplitude and is fed to the grid of V15A. The intervening positive excursions at V12B anode tend to drive V15A into grid current, but this is restricted to a low value due to the high resistance of the cathode load R85.

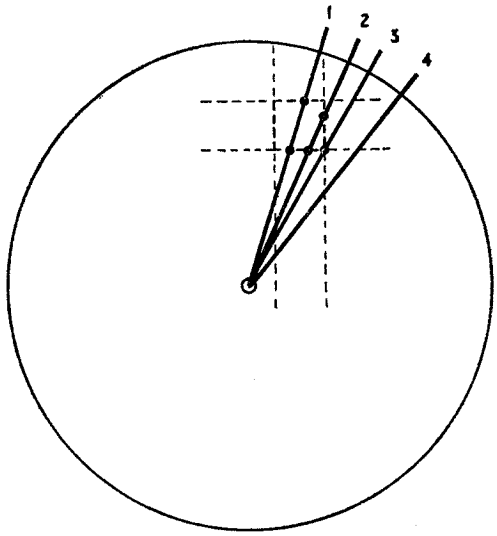

Fig. 6. Generation of strobed area

The corresponding positive excursions at the common cathode of V15 rise well above the fixed bias on the grid of V15B, thus cutting off that valve. As a result, any inter-trace pulse which appears at the anodes of V13 or V14 cannot overcome the increased cathode bias and so produce any output at V15B anode.

Trigger stage

41. The trigger stage, V24, is another double-triode valve connected as a cathode-coupled amplifier operating as a phase splitter. Anode-grid coupling is provided so that the two halves of the valve switch on and off regeneratively. The negative-going waveform from V15B anode which has relatively slow edges, is applied, through C16, to V24B grid, cutting off that valve, the process being aided by regeneration via V24A and the common cathode coupling. The postive-going waveform at the anode of V24B is coupled, through C30, to V24A grid which is returned to a negative potential at the junction of R170 and R171. Since the circuit is symmetrical, V24A anode output is an antiphase version of the waveform at V24B anode, the rising and falling edges at both anodes being considerably steepened by the regenerative action.

Strobe output

42. The output stage of the strobe circuit is a cathode follower V16A whose grid is returned, through R160, to a negative voltage at the junction of R209 and R210. The positive-going pulse appearing at V24B anode is coupled, through C29, to V16A grid and the resultant output at the cathode is fed to SK6. This pulse has an amplitude of approximately 8V and fast edges of the order of 0·2μs.

Boundary marks generator

43. The paraphase outputs from V24 are applied through differentiating circuits (C31, R168 and C32, R175) to the grids of a double-triode valve

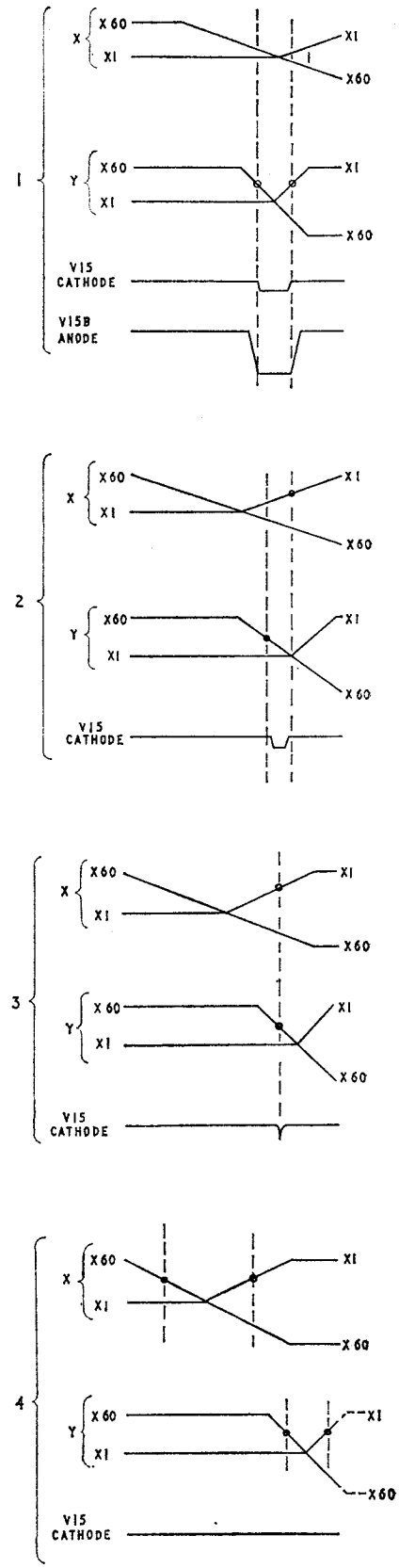

Fig. 7. Comparator input: X and Y transition waveforms

V25. V25 cathodes are connected together and returned through R172 and R195 to −300V. The anodes are also connected and taken through R208 and an inductor L1 to +300V. The inductance of L1 in conjunction with the circuit stray capacitance gives a frequency of the order of 1 Mc/s.

44. Between the differentiated drive pulses V25 is passing a very low current and the negative portions of the input waveform can produce only an insignificant effect at the common anode connection. However, when a negative differentiated input arrives at either grid, a positive differentiated input is present at the other grid. This positive input causes the corresponding half of V25 to conduct and the rate of change of current in L1, due to the flow of anode current, causes the inductor to ring. The ringing commences with a negative half cycle and subsequent rings are heavily damped due to the presence of R208 and the diode-connected triode V16B. Thus, V25 anode waveform consists of two negative half sine waves whose timing corresponds to the leading and trailing edges of the strobe pulse.

45. V25 anode waveform is applied to the cable-drive amplifier, consisting of a buffer cathode follower V26B, a triode amplifier V26A and an output cathode follower V28. In the quiescent state V26B is in grid current and the diode V27 is conducting due to the connection of its anode, via R180, to +300V and its cathode to the circuit R192, R185 and R182 between earth and −300V. Normally, V27 cathode, and hence V26A grid, tend to rest at approximately +4V, but the flow of grid current limits this to about earth potential. V26A is thus conducting and V28 is cut off since its grid is returned to about −50V at the junction of R187 and R188.

46. With the arrival of the first negative half cycle at V26B grid, that valve is cut off and the resultant fall in cathode potential cuts off the diode V27. With the cessation of the current flow through V27, V26A grid potential starts to fall below earth and V26A anode rises. This wavefront is transferred to the grid of V28 and causes V28 cathode to rise correspondingly, thus bringing about an increase in current through the capacitance-compensated feedback network R185, C36, C39 and hence limiting the extent to which V26A is cut off. To a first approximation the amplitude of the output pulse at the cathode of V28 is limited to $\frac{R185}{R182}\times 300V = \frac{12\,000}{200\,000}\times 300 = 18V$. With the ensuing small positive overshoot from V25, the cathode follower V28B drives V26A, through the diode V27, into grid current, thereby cutting off V28 and terminating the output pulse. During this phase, with the low impedance drive from V26B, the negative feedback through R185 has a negligible effect.

47. A similar sequence of events follows the arrival of the second half cycle at V26B grid so that the output waveform appearing at V28 cathode consists of two positive-going pulses, approximately 15V in amplitude, whose spacing is equal to the length of the strobe pulse. These pulses are fed, via the contacts of a relay RLB, to SK7 and from there to the associated passive decoder. RLB is controlled by the active decoder switch on the console control panel (or adjacent control unit for console 4476) and contacts RLB1 make when the switch is set to A.D.+MARKER.

48. It should be noted that, since the markers are generated once per scan, the boundaries displayed on the PPI will not consist of complete lines but are made up of a series of dots, although under certain conditions they may appear to be whole lines. It will be found that the definition of the square is dependent upon its position on the PPI screen. Reference to Chapter 2, fig. 9 will show how the square appears on the PPI. This illustration is drawn for a response occurring at approximately the 45° position and it will be seen that each sweep cuts the square diagonally. As a result, a complete pattern of dots is built up and the square is clearly defined. However, if the square is located near the north-south axis, only the horizontal lines are cut by a large number of sweeps and a considerably smaller number of dots will be produced on the vertical sides, resulting in a display which is effectively two-sided, only the horizontal components of the square being clearly defined. Similar conditions occur on the east-west axis, but here only the vertical sides are fully defined.

49. Some loss of definition is also to be expected as the square is moved out in range towards the tube periphery. The angular displacement of the trace increases with range so that, since the square dimensions are fixed, a smaller number of dots is displayed, thus reducing the definition.

Power supplies and control circuits

50. H.T. supplies for the waveform generator are derived from a stabilizer, voltage 12273 but the heater supplies are obtained from a transformer T1 within the unit. T1 derives its input from the 230V 50 c/s supply, fed via relay unit 12598. When the L.T. ON switch SWC is closed, −50V is applied from PL12/D to the relay unit and energizes a relay whose contacts make and switch the 230V supply to PL12/A and B. Fuse FS4 and the thermal cut-out FS3 protect the transformer primary circuit.

51. The action of closing SWC causes the l.t. indicator lamp LP4 to light and also connects −50V to one terminal of the coil of relay RLB, one contact of the H.T. ON switch SWD and a springset of relay RLA. The other terminal of

RLB is taken to PL12/F and from there to the active decoder switch on the console.

52. When SWD is depressed, LP5 is illuminated and −50V is fed out, via PL11/F, to relay unit 12598. This causes another relay to be energized, resulting in the +300V and −300V supplies being fed to the waveform generator through PL11/D and A. With the −300V supply present in the waveform generator, RLA is energized and contacts 22/23, which are in parallel with SWD, make. The −50V supply to the control relay in the relay unit is thus maintained when SWD is released.

53. SWD is a three-position switch, spring-biased to the centre position. When the toggle is raised, a pair of contacts connects the lower end of R92 to earth, thus effectively short-circuiting the coil of relay RLA. As a result, the relay is de-energized so that the +300V and −300V supplies are removed. This provision is made because each stabilizer, voltage 12273 may supply up to five waveform generators. The absence of an independent control would necessitate switching off the supplies to all the units.

54. The power supply unit, stabilizer, voltage 12273 is also used in rack (marker sequence) 4195. It is fully described in A.P.2527X.

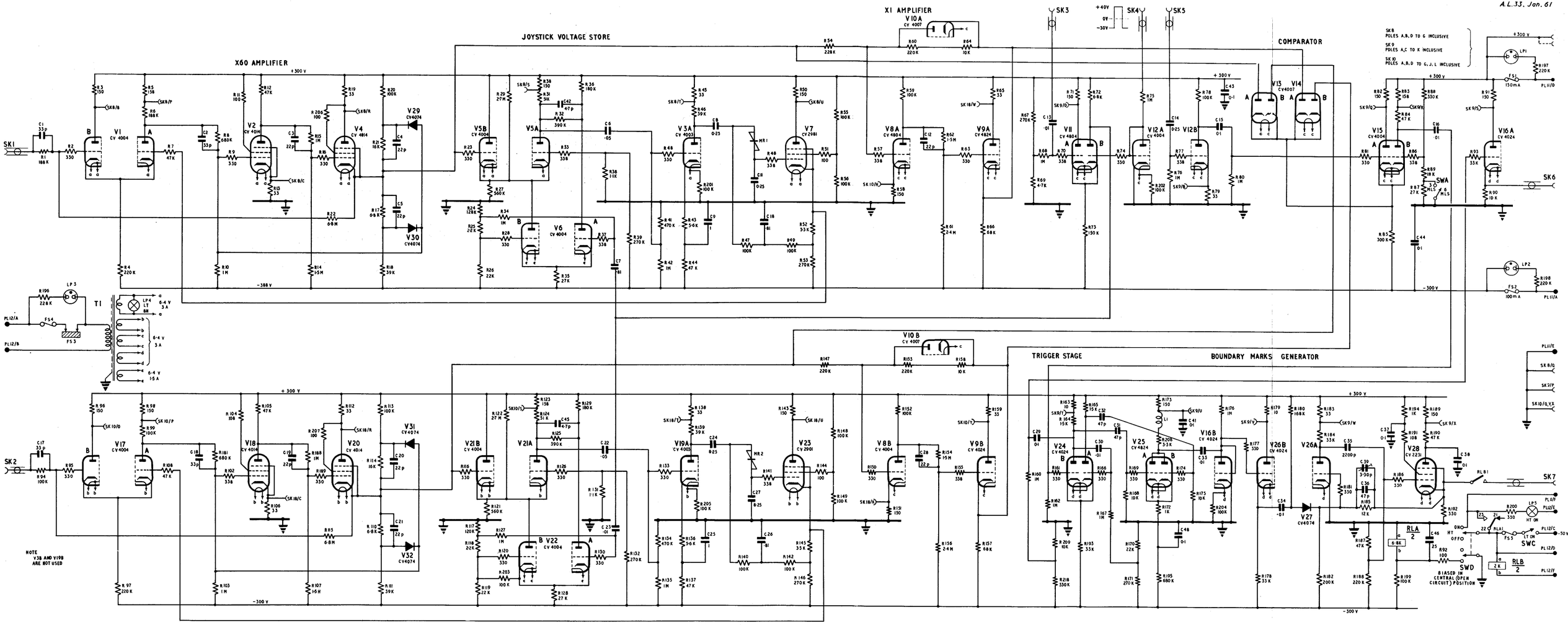

Fig. 8 924/8/4814/56739/625/3/61 J. T. & S.

Waveform generator (A D strobe) 12038 : circuit

Fig. 8

Appendix 1

GENERATOR VIDEO MARK 5840-99-947-1153

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LIST OF ILLUSTRATIONS

Introduction

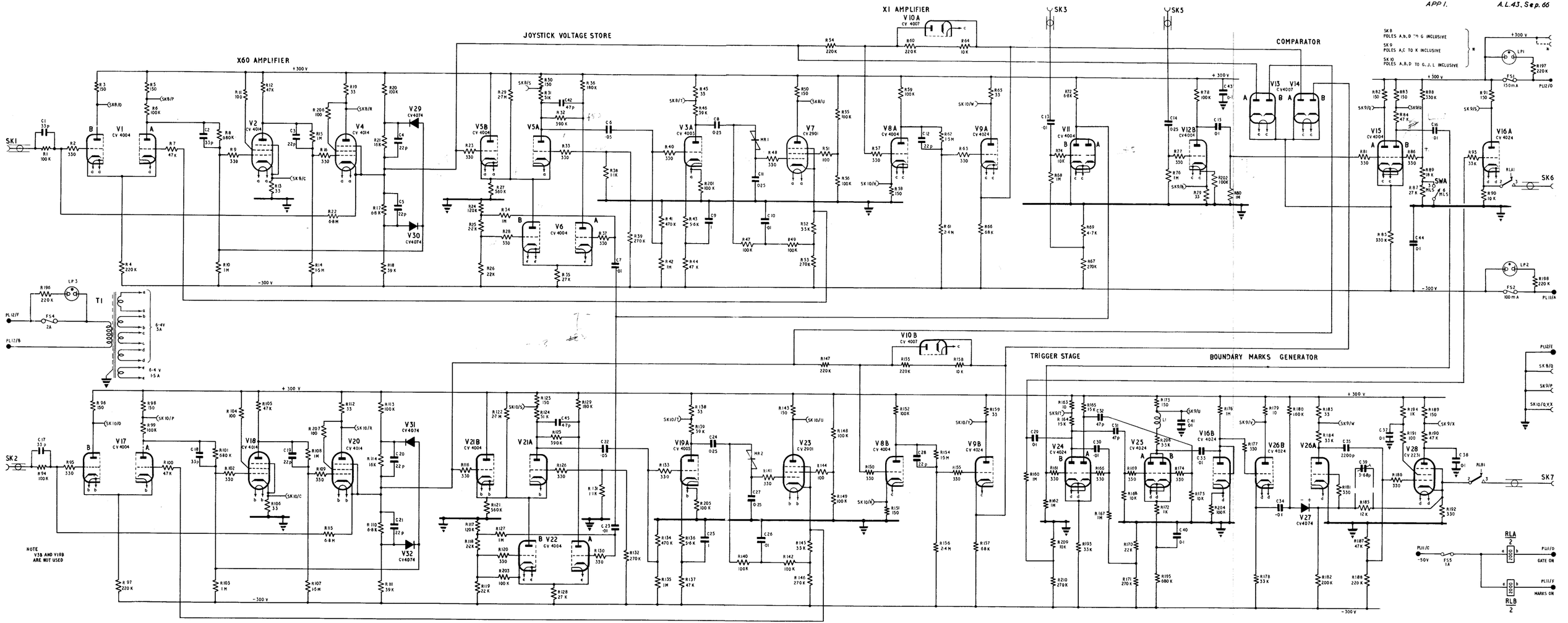
1. The waveform generator (A.D. Strobe) 12038 used in conjunction with the IFF S.I.F. active decoding equipment must be gated by the dekatron waveform from the full interconsole marking system.

2. At certain sites equipped with interim interconsole marking systems, this dekatron waveform is not available and the gating must be carried out by using the intertrace bright-up (ITBU) waveform alone, which is the only suitable waveform available with this system.

3. Generator video mark 5840-99-947-1153 has been designed for use in these circumstances and is a modification of the waveform generator (A.D. strobe). The circuit diagram of this modified unit is shown in fig. 1.

Description

4. The circuit is similar to that of the waveform generator (A.D. strobe) except that V11A is no longer used and V11 now functions as a simple triode amplifier. Also, the h.t. and l.t. switching circuit, and the thermal fuse in the primary of TR1 have been removed, and the output from V16a cathode to SK6 is now controlled by the gating relay RLA/2. RLB1/2 still functions as before.



Generator, video mark (NSNo.5840-99-947-1153): circuit

Fig. 1

Chapter 5

INDICATOR, ELECTRICAL (A.D.) 12120

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LIST OF ILLUSTRATIONS

General

1. It has already been explained in earlier chapters in this and the preceding section that the pulse output from the active decoder is displayed visually on a numerical indicator. Such an indicator may take one of several forms but initially the function is performed by indicator, electrical (A.D.) 12120 which displays the code on neon-type numerical indicators.

2. Each neon is capable of displaying any of the digits from 0 to 7, and to provide a two-figure display on modes 1 and 3 or a four-figure display on mode 2, four of these neons are used in the indicator.

Construction

3. Indicator, electrical (A.D.) 12120, illustrated in fig. 1, is housed in a box measuring $7\frac{1}{2}$in.$\times$6in.

Fig. 1. Indicator, electrical (A.D.) 12120 : general view

×7in. It is supported on the mounting 12597 which also accommodates the control unit (passive) 12118 on top of console 64.

4. Mounted on the front of the unit are two frames behind which are perspex panels. The neon tubes are supported behind the upper frame in such a manner that the code is displayed as a horizontal row of two or more digits. The lower frame has four cut-outs behind which are lamps. Of these the extreme left hand lamp is the query indicator while the other three serve to show the selected mode.

Circuit

5. A circuit diagram of the active decoder indicator is given in fig. 2. V1 to V4 are the numerical indicators consisting of neon tubes on 12-pin bases. The particular tube employed has 10 separate cathode assemblies, each shaped to form one of the digits from 0 to 9 although only 0 to 7 are used in this application. H.T. is applied to a common anode through a series resistor.

6. The cathodes of each tube are returned to earth via changeover springsets on the relays A to M, the coils of the relays being connected between −12V and the collectors of the output transistors on the matrix (decoder) 6886 boards in the active decoder. If there are no code pulses present in the train, all the relays remain de-energized and in this condition the code 00 or 0000 will be displayed according to the mode selected. Whenever an output pulse is produced by one of the matrices the corresponding relay is energized and, depending upon which pulses of a particular letter group are received, the appropriate numeral of the associated neon will be illuminated. A germanium diode is connected across the coil of each relay to protect the output transistor in the decoder from voltage surges caused when current through the coil is cut off.

7. The indicator is normally inoperative through the inclusion of relay N whose coil is connected in the collector circuit of a transistor associated with the active decoder main input gate (*Chap.* 2). When the gate is closed on the completion of a decoding operation, relay N is energized and contacts 2 and 3 make, connecting the 250V supply to the anodes of the neons. At the same time the query lamp circuit is completed through contacts 22 and 23.

8. Relay P is controlled by the mode selection switch on the console. When the switch is set to mode 2 the relay is de-energized and the position of the contacts is as shown in fig. 2, i.e. the mode 2 indicator lamp is connected across the 50V supply and illuminated while the 250V supply is connected to all four neons. In the mode 1 or mode 3 positions of the switch relay P is energized so that the 250V supply is disconnected from V3 and V4 and the 50V circuit to ILP3 is broken.

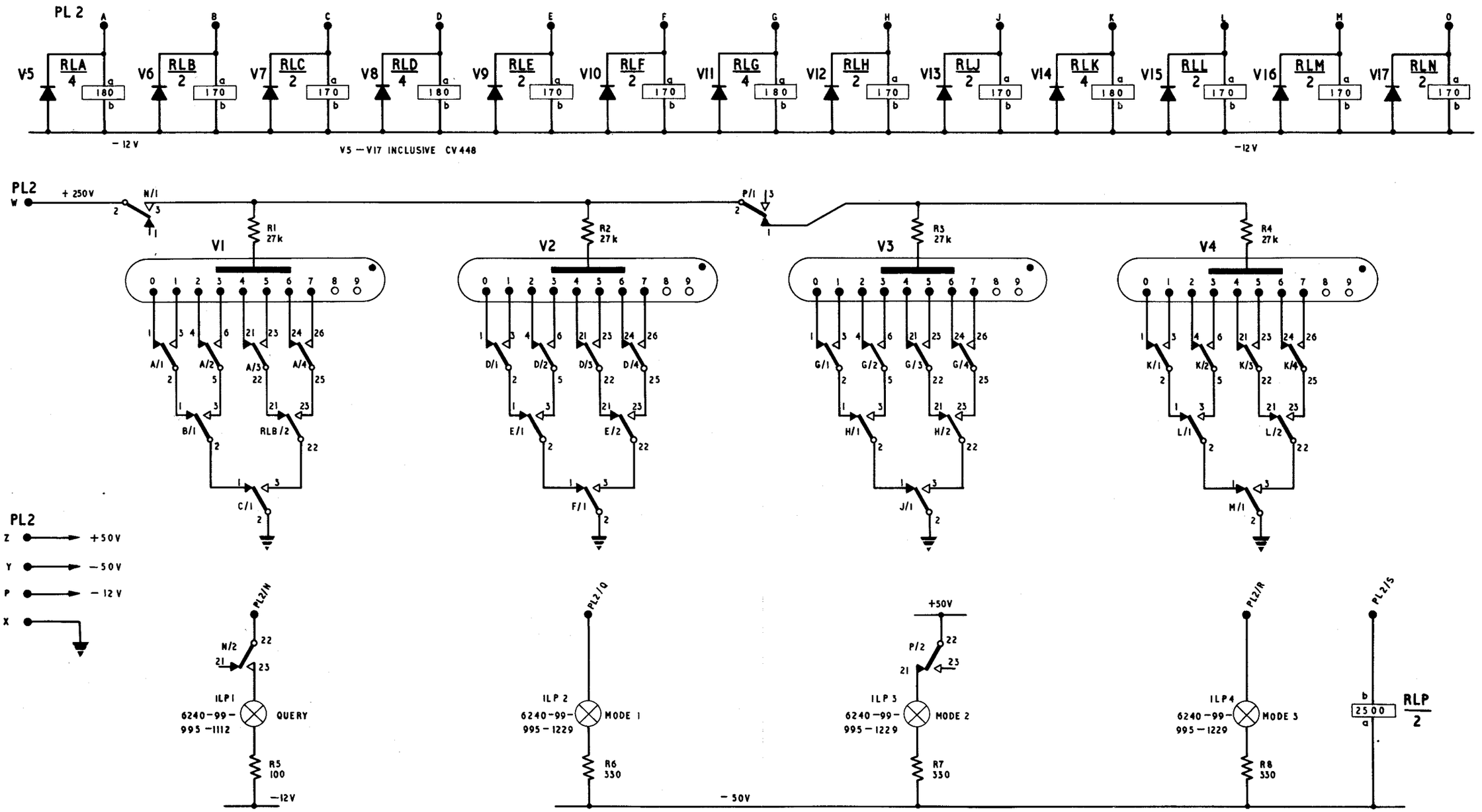

Fig. 2

924/8/4814/56739/625/3/61 J. T. & S.

Indicator electrical (A.D.) 12120: circuit

Fig. 2

Chapter 6.— POWER UNIT (A.D. INDICATOR) 12123

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LIST OF ILLUSTRATIONS

General

1. Power unit (A.D. indicator) 12123, which is mounted in rack (mode 1 decoder) 12276, provides the d.c. supply required by the neon tubes in indicator, electrical (active decoder) 12120. In addition, it supplies 250 V for the matrix decoder input gates as well as a – 12 V line which is used to feed the output stages and resetting circuit in decoder sub-assembly (active) 4676.

Construction

2. The unit (*fig.* 1 *and* 2) consists of a standard rack panel with the various components mounted on the rear side. On the front are mounted the input and output sockets, the mains on/off switch and sixteen fuses. Each output is separately fused. Handles at the front and rear of the panel facilitate handling during installation, removal or servicing.

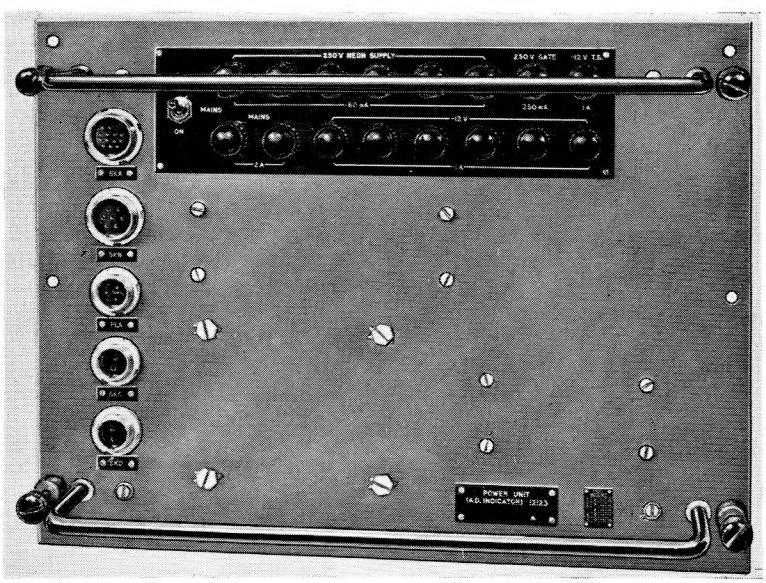

Fig. 1. Power unit (A.D. indicator) 12123 : front view

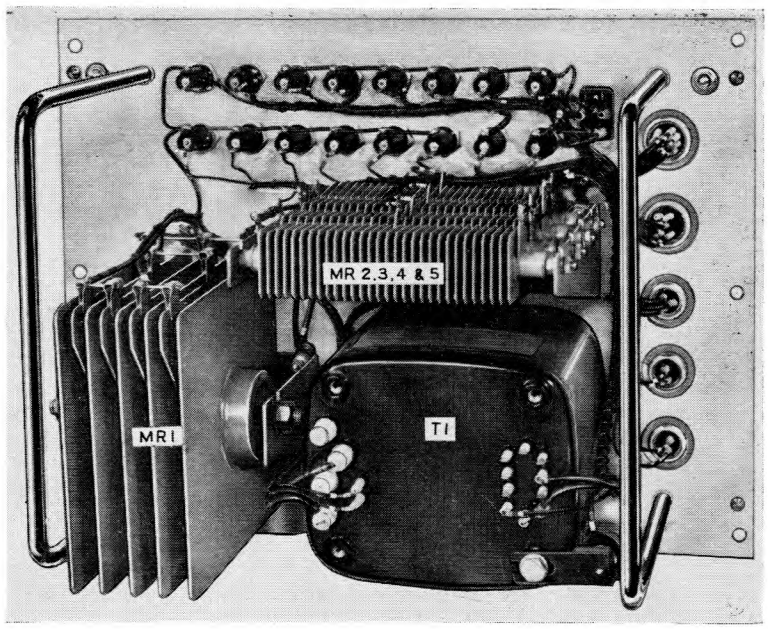

Fig. 2. Power unit (A.D. indicator) 12123 : rear view

Circuit description (*fig.* 3)

3. A single transformer T1 provides all the output voltages. The 230 V 50 c/s supply is fed in on pins a and b of PLA and thence, via fuses FS1, FS2 and FS3, to the primary of T1. FS1 is a thermal cut-out to protect the unit in the event of overheating.

4. The indicator neon supply is derived from a 350 V winding, tapped at 285 V, 300 V and 315 V, coupled to a bridge-connected rectifier consisting of MR4 and MR5. The resultant d.c. output is fed, via fuses FS12 to FS17, to SKB. Thus, there are six separate outputs, each capable of delivering the load current required by the four neons in the associated indicator. Since the d.c. supply is not normally connected directly to the neons, but is switched on when the decoder input gate is closed (*Chap.* 2, *para.* 17), a load resistor R1 is connected across the rectifier output to prevent excessive voltage fluctuations when the supply is switched on and off.

5. The other high-voltage secondary on T1 is a 315 V winding which supplies a second bridge-connected rectifier consisting of MR2 and MR3. This provides a d.c. output of 250 V at 180 mA for the matrix decoder input gates and is fed, through fuse FS11, to SKD. It will be noted that no smoothing circuit is incorporated in the power unit but reference to Chap. 2, fig. 14 will show that a filter is provided on each active decoder main frame; the 250V gate supply is fed into the active decoder on pin Z of SKC and thence to a resistance-capacitance filter consisting of R25 and C9.

6. The remaining secondary on T1 is a 12·5 V winding tapped at 10·5 V and 11·5 V and connected to a bridge rectifier MR1. A d.c. output of approximately − 12 V is obtained and fed, through fuses FS4 to FS9, to pins a to f of SKA. There are thus six separate − 12 V lines. A seventh output is taken through fuse FS10 to SKC for connection to test set (decoder) 4678. There is no filter in this circuit but adequate smoothing is provided on each active decoder by the charging circuit associated with the resetting operation (*Chap.* 2, *fig.* 16 *and para.* 75).

7. The − 12 V line serves two purposes; its primary function is to supply current to the active decoder output stages and hence energize the relays in the active decoder indicator. The output transistor of each matrix decoder has, as its collector load, the coil of a relay whose contacts control the application of the 250 V supply to the associated neon indicator .When the supply is fully loaded, the relays are operating at their lower voltage limit and a separate earth return is consequently provided for each − 12 V output.

8. The − 12 V supply also provides the reset current for the memcores in the active decoder. One of the outputs from SKA is routed, via SKX at the base of rack 12276, to rack 4469 and thence to the active decoder.

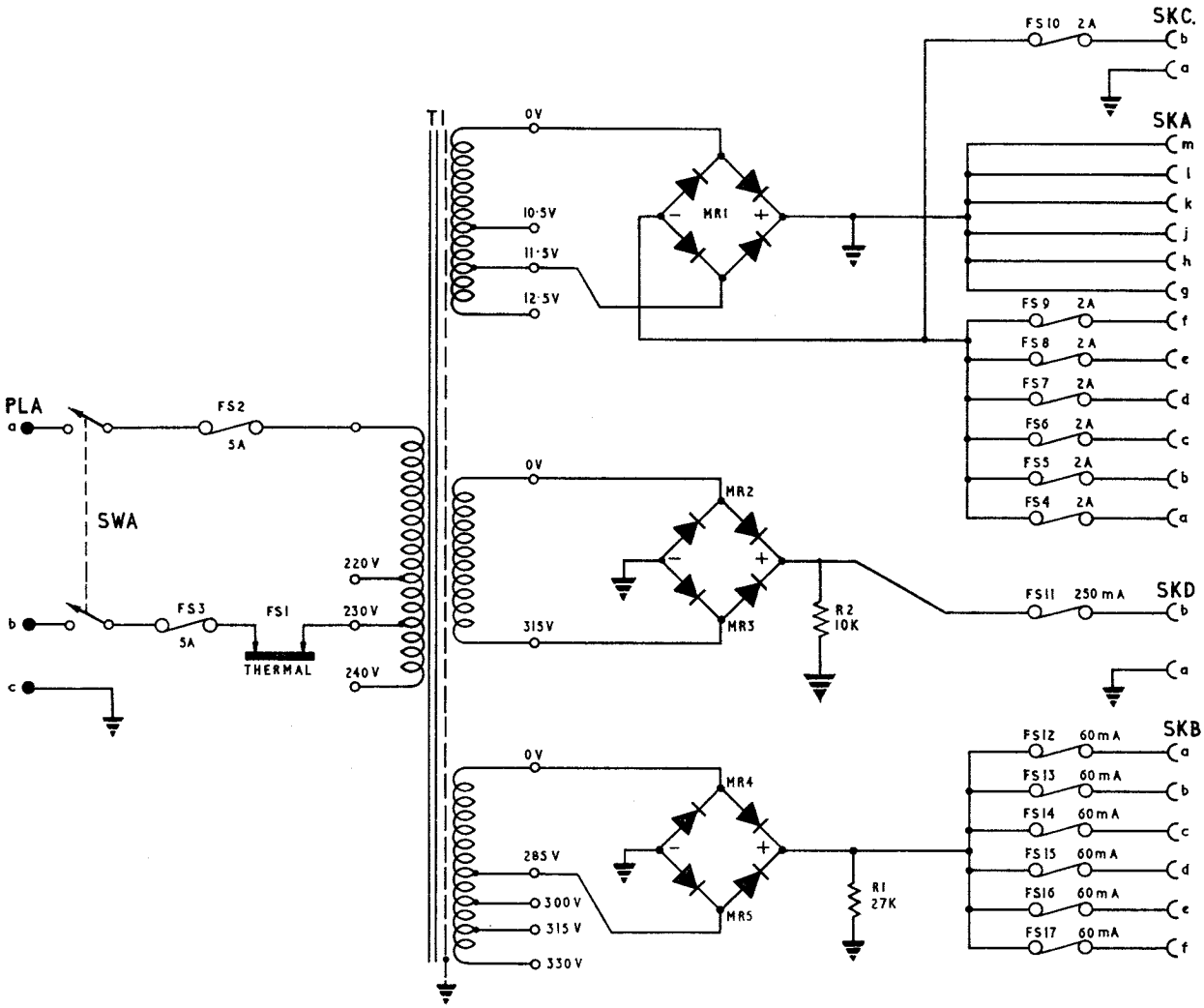

Fig. 3. Power unit (A.D. indicator) 12123: circuits

9. Each power unit 12123 is basically capable of supplying up to six active decoder indicators but, due to the requirements of the resetting circuits, one power unit in an installation can supply only five indicators since one of the −12V lines is taken direct to rack 4469. Provision exists in rack 12276 for two power units 12123, affording supplies for up to eleven active decoder indicators. Since active decoding is intended as a limited facility, it is unlikely that any installation will have a greater number of channels than this.

Chapter 7

CONTROL UNIT (ACTIVE) 12121

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LIST OF ILLUSTRATIONS

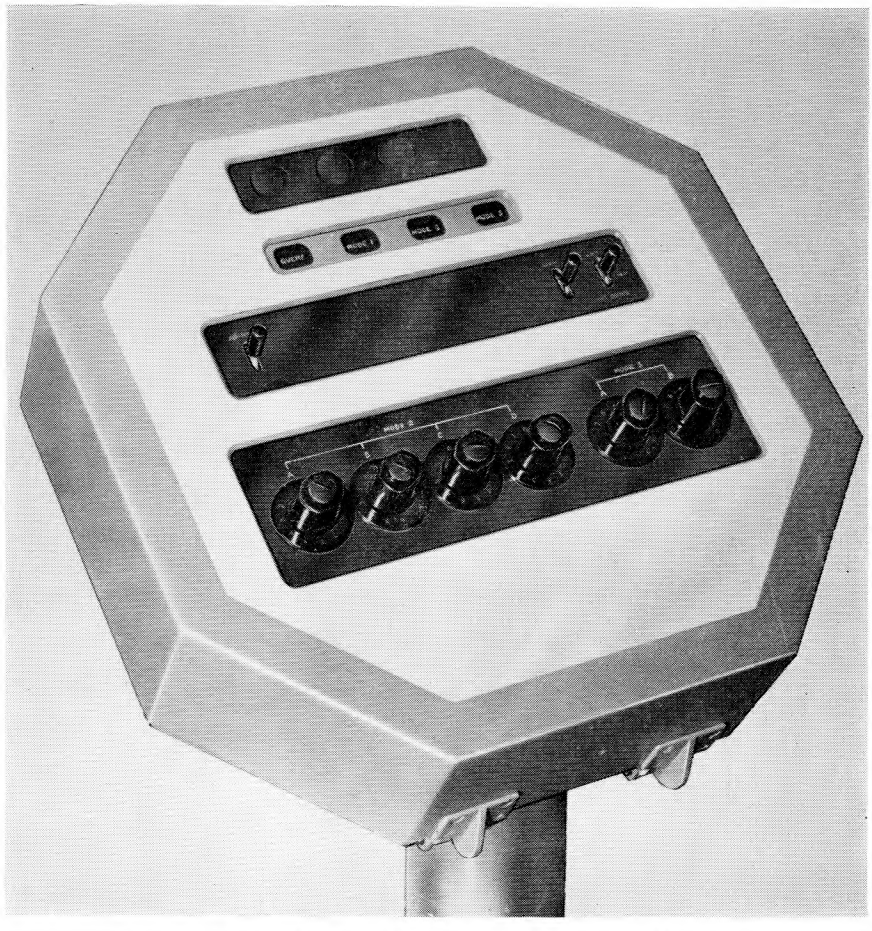

Fig. 1. Control unit (active) 12121 : general view

General

1. Remote control of the active decoder from console 64 positions is achieved by the addition of a switch to the control desk and the indicator is supported on mounting 12597 on top of the console. The same arrangement is not practicable on console 4476 and a separate control unit, embodying all the necessary controls and indicators for SIF, is provided.

Description

2. The unit, which is illustrated in fig. 1, is similar to control unit (passive) 12119 but incorporates, in addition to the facilities provided by that unit, an active decoder control switch and indicator.

3. Control unit (active) 12121 takes the form of a hexagonal box designed to fit on top of a mounting

(pedestal) 12809. This is a flanged tubular pillar, approximately 2 ft. 6 in. in height. The controls are mounted on perspex panels behind cut-outs in the front cover of the box and are illuminated from the rear.

4. As on control unit 12119, the bottom controls are the code selection switches with the mode selector and passive decoder function switches mounted immediately above. On the left-hand side of the upper panel is fitted the A.D./OFF/ A.D. + MARKER switch.

5. Behind the two cut-outs in the upper portion of the cover are the various indicator lamps forming a display similar to that of indicator, electrical (A.D.) 12120. At the top are four neon tubes arranged in such a manner that the code is shown as a horizontal row of two or more digits. Below these are the active decoder query lamp at the left-hand side and the three mode indicator lamps.

6. A circuit diagram of control unit (active) 12121 is given in fig. 2.

PL2

+25OV

W

N/1

P/1

NOT USED: Q, R, S, T

V1 R1 27k

V2 R2 27k

V3 R3 27k

V4 R4 27k

A/1 A/2 A/3 A/4

B/1 B/2 C/1*

D/1 D/2 D/3 D/4

E/1 E/2 F/1*

G/1 G/2 G/3 G/4

H/1 H/2 J/1*

K/1 K/2 K/3 K/4

L/1 L/2 M/1*

PL1/X

EARTH

PL2/X

RLA 4 180 V5 CV448

RLB 2 170 V6

RLC 2 170 V7

RLD 4 180 V8

RLE 2 170 V9

RLF 2 170 V10

RLG 4 180 V11

RLH 2 170 V12

RLJ 2 170 V13

RLK 4 180 V14

RLL 2 170 V15

RLM 2 170 V16

-12V

V5-V17 INCLUSIVE ALL CV448

R5 100

ILP1 QUERY

N/2

PL2/M

+50V

SWH AD+MKR

PL2/0

PL2/U

PL2/V

AD

RLN 2 170 V17

PL2/P

SWG ALL SIGS.

ALL CODES

PL1/Z

PL2/Z

PL1/O

PL1/P

SWJ MODE SELECTOR

PL1/V

PL1/R

PL1/T

PL1/S

PL1/U

PL1/Q

PL1/Y

PL2/Y

-50V

FS1 500mA

ILP2 MODE1

ILP4 MODE 3

ILP3 MODE 2

R6 330

RB 330

R7 330

RLQ 2 2500

RLR 2 2500

RLS 2 2500

RLP 2 2500

P/2

ILP6 ILP5 ILP13 ILP7 ILP8 ILP9 ILP10 ILP11 ILP12 ILP14

+50V

Fig. 2

D.2118 470893 S.W. 2.65

Control unit (active) 12121: circuit

PL1

MODE 2

SWC

SWD

SWA

SWB

SWE

MODE 3

SWF

Q/1 Q/2 R/2 S/1 R/1 S/2

TO PIN 12 ON ALL SWITCHES

W NOT USED

NOTE
SWITCHES SHOWN IN FULLY ANTI-CLOCKWISE POSITIONS

V1, V2, V3, V4,

K1 K2 K3 K4 K5 K6 K7 K8 K9 K0 NC

*NOTE
RELAY CONTACTS C/2, F/2 J/2 AND M/2 ARE NOT USED

Fig. 2

Chapter 8

GENERAL NOTES ON TRANSISTORS AND FERRITES

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Introduction

1. From the purely practical standpoint, transistors are simply circuit elements which require slightly different techniques from valves and have their own ranges of operation. Some knowledge of the properties of semi-conductors and their limitations is useful, however, both in understanding the operation of the circuits employed and when the necessity for servicing arises.

2. This chapter is not intended to be a substitute for a text book. It should be regarded simply as a collection of general notes designed (1) to be of help to those responsible for operating and servicing the IFF Mk. 10 SIF equipment and (2) to explain some of the less familiar terms used in the preceding chapters.

3. Semi-conductors are materials whose conductivity lies between that of metals and insulators. The most commonly used materials are germanium and silicon and these differ from metallic conductors in that current is conveyed by charged particles of both polarities.

4. In transistor electronics the basic unit is the junction, which is the region of transition between semi-conductors of different electrical properties within a single crystal of suitable material. The major property of such a junction is its asymmetrical conductivity characteristic which is greatly influenced by temperature. The electrical properties of a junction are not constant for all frequencies and are also modified by exposure to light and other forms of radiation.

Transistors

5. Most transistors consist of a piece of semi-conductor material in which two separate junctions have been formed, one to serve as emitter and the other as collector. When the transistor is operating, the emitter junction acts as a diode biased in the forward (or conducting) direction and the collector junction as a diode biased in the reverse direction. Both junctions have the properties outlined in para. 4. Depending upon the base and junction materials used, transistors can be divided into two main types, PNP and NPN. Only the PNP type is used in IFF Mk. 10.

6. Very approximately, the transistor may be considered as similar to a triode valve with the collector serving as the anode, the base as the grid and the emitter as the cathode, but this analogy must not be taken too far. In contrast to the valve, which is a voltage device, the transistor is a current amplifier. Because the input circuit is effectively a diode biased in the forward direction and the impedance changes with the current flowing, it is necessary to provide the drive from a current and not a voltage source.

7. It is due to this current amplifying property that care is necessary when observing waveforms in a transistor circuit. An oscilloscope displays voltage so that waveforms, particularly at the base, may often be misleading. It will be of assistance to remember that the voltage is usually developed across a low impedance.

8. Transistors are low impedance as well as low voltage devices. When a transistor is bottomed, the impedance between collector and emitter is of the order of 1 ohm so that some form of current limiting resistor must always be used in the circuit. The expression "bottomed", applied to a PNP transistor, means that the base is maintained negative with respect to the emitter. In this condition a transistor has advantages as a switch, the low impedance between emitter and collector being analagous to relay contacts and the base current representing the energized relay coil.

9. The input and output circuits are always interconnected through the internal impedance of the transistor. Thus, the external input circuit will always have some effect on the output circuit and vice versa. It should be noted that, for this reason, the transistor emitter follower, although analagous to the valve cathode-follower, does not have the almost perfect isolating property of the valve.

Circuit configurations

10. A transistor may be used in any one of three basic circuit configurations, indicated in terms of the electrode which is common to the input and output signal circuits, *i.e.* common emitter, common base or common collector. The common base connection is seldom used and in the IFF Mk. 10 equipment only the common emitter and common collector circuits are employed.

11. It is stated in para. 4 that the electrical properties of a junction are dependent upon frequency and, for this reason, the current gain of a transistor (denoted by α) starts to fall after a certain value of frequency is exceeded. The frequency response of a transistor is commonly expressed in terms of the frequency at which the current gain is reduced to $1/\sqrt{2}$ of the low frequency value. This frequency is called the cut-off frequency and is usually quoted for the common base connection, being indicated by f_α. It should be noted that f_α is not necessarily the maximum operating frequency of a transistor in any given circuit, but is usually a good indication of the inherent properties of the device.

12. Although the three basic arrangements can be evaluated in terms of equivalent circuits, the properties are, due to the frequency dependence and internal impedance of the transistor, more complex than in valve circuits. However, by making a number of approximations, simplified equations for the derivation of the circuit properties can be obtained. These are shown in the following table together with typical values for low power transistors.

Circuit	*Current gain*	*Input impedance*	*Output impedance*
Common base ...	α	$r_e + r_b(1-\alpha)$	r_c
	0·98	29 ohms	1 megohm
Common emitter ...	$\alpha/(1-\alpha)$	$r_b + r_e/(1-\alpha)$	$r_c(1-\alpha)$ base open-circuit
	50	1500 ohms	20 kilohms
Common collector ...	$1/(1-\alpha)$	$r_b + R_e/(1-\alpha)$	$r_e + R_b(1-\alpha)$
	50	50 kilohms if $R_e = 1$ kilohm	45 ohms if $R_b = 1$ kilohm

The expressions used in the table are identified as follows:

r_b is the intrinsic base resistance and is of the order of 200 ohms.

r_e is the intrinsic emitter resistance and is equal to $25/I_e$ where I_e is the d.c. emitter current in mA.

r_c is the intrinsic collector resistance.

R_b and R_e are the external circuit resistors.

13. The main characteristics of the three circuit configurations may be summarised thus:

Common base	*Common emitter*	*Common collector*
Low input impedance	Low input impedance	High input impedance
High output impedance	High output impedance	Low output impedance
Practically unity current gain	High current gain	High current gain
High voltage gain with no phase reversal	High voltage gain with phase reversal	Unity voltage gain

Types of transistor

14. Only three types of transistor are employed in the IFF Mk. 10 SIF equipment.

CV7004. A PNP junction transistor with a minimum alpha cut-off of 3 Mc/s. It has a good frequency response and is used for pulse circuits wherever a fast rising edge is required.

CV7006. A PNP output transistor which is capable of supplying up to 125mA of collector current. It is used as an electronic switch for the control of relays and indicator lamps.

CV7003. This is similar to the CV7004 but has a minimum alpha cut-off of $7\frac{1}{2}$ Mc/s.

15. The CV7003 and CV7004 are hermetically sealed in black painted glass envelopes. When re-

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placing either of these types, the greatest care must be taken not to damage the painted surface since the action of light on the junction may seriously impair its characteristics. The CV7006 is contained in a metal tube.

Note . . .
Some makes of the CV7003 and CV7004 are provided with a plastic sleeve over the glass shell, thereby reducing the possibility of damage to the painted surface.

Precautions
16. Because of the nature of the device, a transistor is susceptible to temperature increases and can easily be damaged by overloads, even of relatively short duration. Correct operation under normal circumstances is ensured in the circuit design but certain precautions are necessary in handling the equipment.

17. Care should be taken to ensure that all connections and polarities are correct before switching on the equipment. Associated components and the transistors themselves should not be replaced with the power supplies connected because of the surges which can occur, for example, from the discharge of capacitors. Care is also necessary when making circuit adjustments; accidental short-circuits from the base of a transistor to the power supply or a short-circuit across the emitter resistor can cause the flow of sufficient current to damage the resistor.

18. In some circumstances the use of an electric soldering iron which is earthed may cause damage to a transistor while the leads are being soldered into equipment. To avoid any possibility of leakage currents flowing through the transistor, it is preferable to disconnect the iron from the supply source during the actual soldering operation.

19. When soldering a transistor into a unit, it is essential to avoid the conduction of excessive heat along the leads. An adequate heat shunt must always be used and the iron should be the smallest available.

Ferrites
20. Ferrite is a non-metallic material which has magnetic properties together with a high value of internal resistance. The particular material used for the counting and storage circuits in the IFF Mk. 10 application has a nearly rectangular B-H loop characteristic which means that, in the absence of an applied magnetic field, it has two stable states, *i.e.* two possible directions of remanent magnetization.

21. Considering fig. 1, suppose that a ferrite core is magnetized to the extent that H lies in the region $X - X^1$, *i.e.* beyond saturation. When the magnetizing field is removed, the magnetic state of the material is shown by W^1; that is, there is appreciable remanent magnetization. If a demagnetizing force is applied, sufficient to move the operating point to W, a large proportion of the original remanence persists.

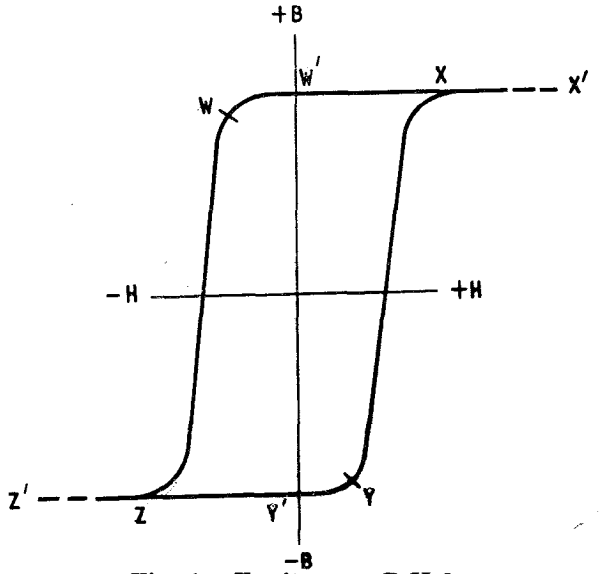

Fig. 1. Ferrite core B-H loop

22. To change the state of the core from W^1 to Y^1, the working point is moved along WZ by applying a demagnetizing field, of $-H$, sufficient to switch the magnetism from W to Z. Thus, once the ferrite core is magnetized in a particular sense, it will stay in that condition, even though subjected to appreciable demagnetizing fields, *i.e.* it has a magnetic memory. However, if a demagnetizing force above a certain critical value is applied, the state of magnetism will suddenly reverse.

23. In digital computer applications, a ferrite core magnetized in the direction of W^1 is said to represent a "1" while, if the working point lies on ZY, it is said to represent a "0". Thus, an assembly of ferrite cores can be used to store binary numbers. This technique and notation are employed in the IFF Mk. 10 active decoder.

24. The ferrite core used in the IFF Mk. 10 matrix decoder 6886 is a small ring with an overall diameter of 2mm. It has toroidal windings and forms a memory core; hence the designation of the complete component as a memcore 12443 or memcore assembly 12444. The magnetic fields are produced by current pulses passing through the windings. In the active decoder the memcore is used in two applications:

(1) As a single information element memory store which is employed almost exclusively as a counting chain element.

(2) As a store to hold and assess the aircraft pulse train information.

25. It should be noted that the rectangular B-H loop characteristic is dependent upon the composition of the ferrite material and that not all ferrites have this property. Thus, although transformer, pulse, 12687 used in the active decoder has a ferrite core, this is different in composition from the memory cores and has characteristics similar to those of more conventional core materials.

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SECTION 1

SPECIAL TEST EQUIPMENT

PART 2

SERVICING

Chapter 1

TEST SET, RADAR, 4339

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Fig. 1. Test set, radar 4339: general view

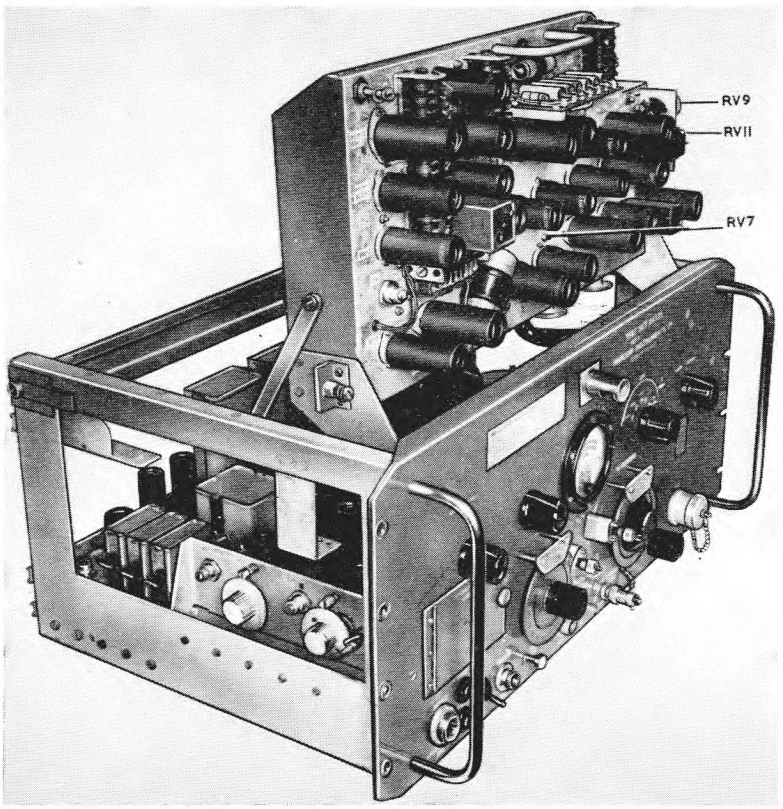


Fig. 2. Test set, radar, 4339: front view with top chassis raised

INTRODUCTION

1. Test set, radar, 4339 is designed for first line testing of the UPX–6 and similar interrogator-responsors operating in the 1000 Mc/s band. When suitably triggered, it is capable of checking certain characteristics of the interrogator transmitter and receiver and displays the results of these checks as a meter reading, the meter being scaled on a " go, no-go " basis. The tests which may be performed are

(1) Measurement of transmitter peak power output.

(2) A check of the transmitter frequency.

(3) A check of the interrogator moding.

(4) Measurement of receiver sensitivity.

(5) A check of receiver bandwidth.

When the appropriate connections between the test set and interrogator are made, all these tests can be performed by the operation of a single switch on the front panel of the test set.

2. In addition, the test set may be employed to set up the receiver GTC characteristic. Self checking facilities are incorporated to confirm the correct functioning of the various circuits in the test set and for certain setting-up purposes, thus obviating the need for additional test equipment.

3. For the tests detailed in para. 1, it is necessary to trigger the test set with a waveform identical with that used to trigger the interrogator. However, to enable the test set to be used in the absence of a suitable waveform, it includes a circuit capable of producing a single trigger pulse at the required repetition frequency so that all tests, except the check of the interrogator moding, may be performed.

4. In effect, test set 4339 is similar to the American test set UPM–6 but differs in several respects although it affords all the necessary facilities for interrogator testing. For example, no calibration charts are required with test set 4339 since the control and meter scales are directly calibrated. Also, test set UPM–6 is a portable instrument whereas test set 4339 is designed for rack mounting. It is permanently installed in a rack at the radar head adjacent to the interrogator which it serves and is also permanently interconnected with the interrogator trigger input, video output and RF output. The test set is not intended to be removed from the rack except when servicing becomes necessary.

GENERAL DESCRIPTION

Construction

5. A general view of test set 4339 in its cover is shown in fig. 1. To reduce the possibility of strong external fields disturbing the circuits, the test set is always mounted in a rack complete with the cover which provides additional screening. The bottom of the cover is provided with eight holes four of which are tapped, the other four being clearance holes for the fixing bolts. The appropriate set of fixing holes is selected according to the type of rack in which the test set is to be mounted. For certain applications two additional fixing holes are provided in the back of the cover.

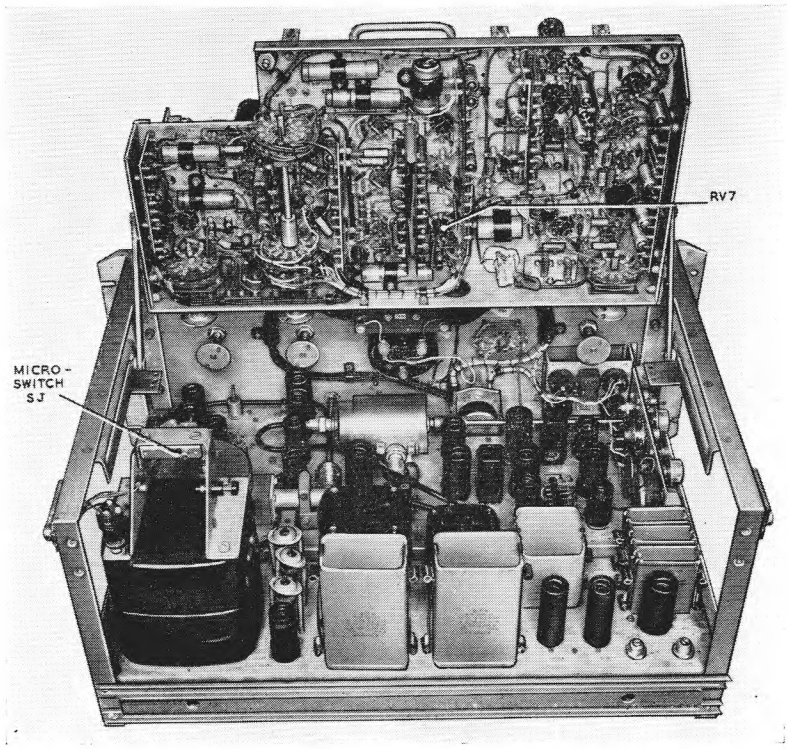


Fig. 3. Test set, radar, 4339: rear view with top chassis raised

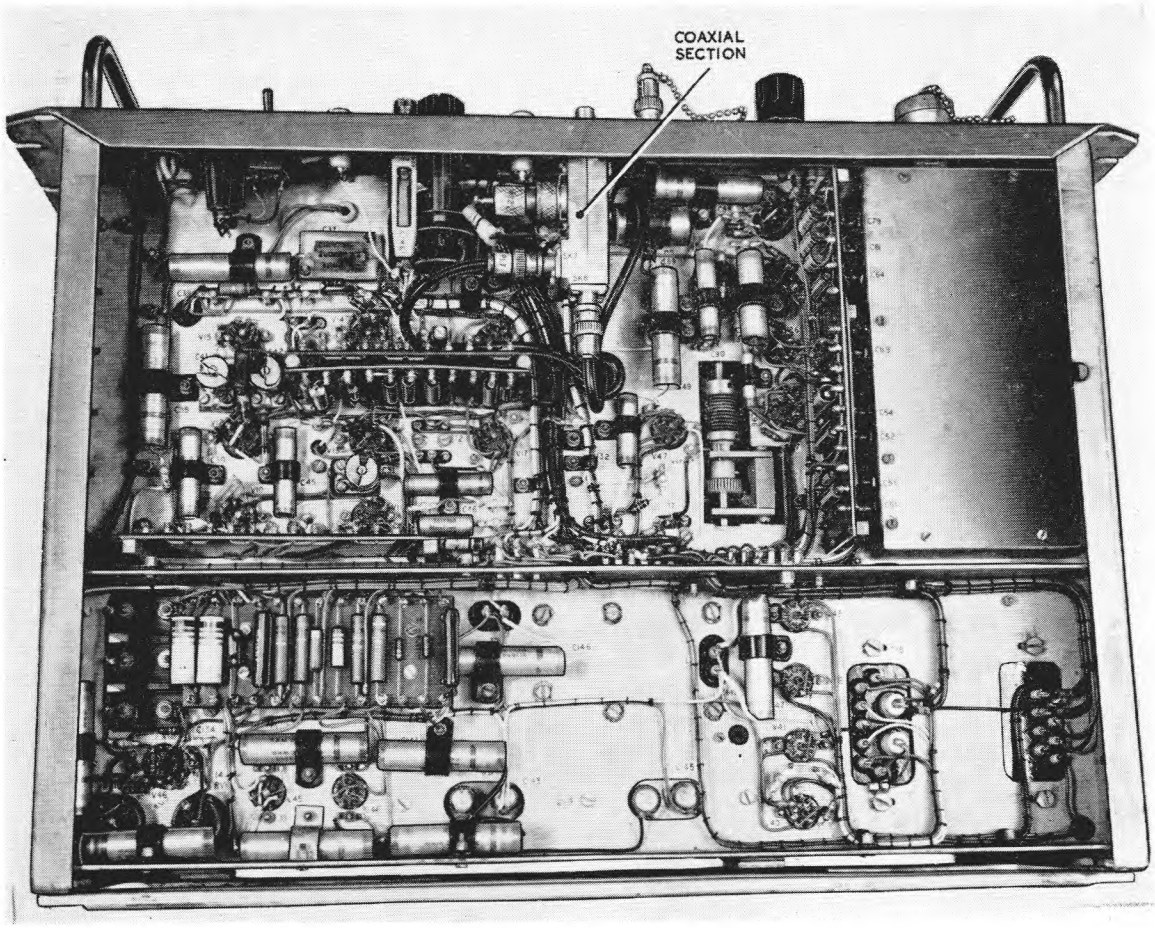


Fig. 4. Test set, radar, 4339: underside view of lower chassis

6. The various components are assembled on two independent chassis which are mounted one above the other and supported on an angle-section framework. Access to the underside of the upper chassis is facilitated by pivoting it at the two front corners so that, when the captive screws at the rear are released, it may be swung into a vertical position as shown in fig. 2 and 3. An underside view of the lower chassis is given in fig. 4.

7. All the operational controls are located on the front panel. Certain of the preset controls which may need most frequent re-adjustment are mounted behind a hinged flap at the left-hand side of the panel. The other preset controls are inside the unit and are only accessible when the test set is removed from its cover or partially withdrawn.

Transmitter testing

8. A block diagram of test set 4339 is shown in fig. 5. The pulsed RF output from the interrogator transmitter, appearing at the 20dB RF PROBE socket on the UPX–6, is fed into the test set at SK1 and is rectified to produce a train of video pulses with an amplitude equivalent to the peak amplitude of the RF signal. These pulses are then passed through an amplifier to an automatic slideback peak rectifier circuit. With the TEST switch in position 1 (POWER), the output from the peak rectifier circuit is applied to the meter which is calibrated on its outer scale arc in terms of the peak power available at the ANTENNA socket of the interrogator. This power measurement circuit is normally referred to as the peak power monitor circuit.

9. With the TEST switch still in position 1 and the adjacent switch set to SELF CHECK, a train of video pulses, stabilized in amplitude, is applied to the peak power monitor circuit and, when the gain of the circuit is set to the correct level, will produce a standard 0·75 kW deflection on the meter. By this means, the gain of the monitor circuit can be checked and re-adjusted if necessary.

10. It should be noted that position 1 of the TEST switch is the only setting at which the meter deflection is proportional to the test set input level. At all other settings of the switch the meter, in conjunction with a trigger circuit, operates as a p.r.f. sensitive device.

11. A portion of the signal appearing at SK1 is also fed into a preset tuned cavity wavemeter and, provided the interrogator transmitter is operating on the correct frequency, a video pulse is produced at the wavemeter output. When the TEST switch is set to position 2 (FREQ.), this pulse is amplified and used to trigger the meter circuit, causing the meter to read full scale deflection.

12. The self check facility is also available for testing the video section of the frequency measuring

circuit. On setting the appropriate switch to SELF CHECK, a pulse, derived from the trigger waveform, is applied to the video circuit which, if it is operating normally, will deliver an output sufficient to cause full scale deflection on the meter.

13. When the TEST switch is set to position 3 (MODE), the rectified RF input is switched to an interrogation mode checking circuit the purpose of which is to check that the duration of individual pulses is greater than 0·7 microsecond and that the spacing between adjacent pulses in the pulse pairs is 3, 5 or 8 microseconds ±0·5 microsecond. Provided these conditions are met, an output is obtained from the circuit and employed to trigger the meter circuit.

14. The meter deflection obtained when checking the interrogator moding is dependent upon the mode or modes in use and the position of the MODE DECODER switch on the test set. The normal readings are:—

Single mode—full scale deflection at one setting of the mode decoder switch and zero in the other two positions.

Double mode interlace—half full scale deflection for two positions of the switch and zero in the third position.

Triple mode interlace—one-third full scale deflection at all settings of the mode decoder switch.

15. On switching to SELF CHECK, the input trigger pulses are applied to the mode checking circuit and cause an output to be produced similar to that obtained with the RF pulse input. In this case however, the minimum allowable pulse width is reduced to 0·3 microsecond.

Receiver testing

16. For the purpose of testing the interrogator receiver the test set incorporates a crystal-controlled, pulse-modulated signal generator preset to the normal receiver frequency. Two outputs are provided, calibrated in terms of the signal appearing at the ANTENNA socket on the UPX-6:—

Output 1—fed via a piston attenuator to SK1 on the test set and variable from 55 to 100dB below 1V by adjustment of the RX SENSITIVITY control.

Output 2—fed to the adjacent socket and preset at 45dB below IV.

17. The signal generator consists of a crystal oscillator, amplifier and three frequency multipliers with an automatic level control circuit to maintain the output constant at the level set by the piston attenuator. Modulation pulses are derived from the input trigger pulses which are first applied to a delay circuit. Two ranges of delay are provided. With the RANGE switch on the test set in the SHORT position, the delay can be preset at any value between 2 and 20 nautical miles. When the switch is set to LONG the delay can be adjusted to any value between 20 and 250 nautical miles by operation of the RANGE control.

18. The delayed signal passes to a blocking oscillator circuit which produces a train of four pulses spaced at 1·2 to 1·5 microseconds intervals and having a duration of 0·35 to 0·55 microsecond. The same circuit also develops a 10 microseconds gating pulse for the RF stages of the signal generator. Thus, a pulse-modulated signal, delayed behind the original trigger pulse by a time equivalent to the desired range (which may be set at any value between 2 and 250 nautical miles) is fed to the interrogator receiver.

19. Provided the receiver is operating normally, a video signal will appear at the VIDEO OUT socket on the interrogator. This signal, which has a waveform similar to that of the input signal from the test set but further modulated with noise, is fed back to the VIDEO socket on the test set. From there it is passed through level checking circuits and, if of sufficient amplitude, will trigger the meter circuit. The meter circuit is adjusted to operate when a signal greater than a predetermined level in the range 1·5 to 3V is fed into the VIDEO socket.

20. With the TEST switch in position 4 (GAIN), the meter circuit will operate on receipt of a single pulse thus indicating that an output is being received from the interrogator receiver, *i.e.* that the receiver sensitivity reaches the desired level. When the switch is set to position 5 (BANDWIDTH) however, the meter circuit does not operate unless four pulses of the correct duration are received showing that the receiver bandwidth is satisfactory.

21. The self-check facility is also available for this part of the test set. When the appropriate switch is set to SELF CHECK, the modulating signal provided for the signal generator is fed directly into the level checking circuits. The amplitude of the signal is such that, if the circuits are operating normally, 100 per cent triggering of the meter circuit occurs and full scale deflection is obtained.

Internal pulse generators

◀**22.** Under certain conditions it is possible that the normal external trigger source may not be available and an internal pulse generator is provided to enable use of the test set in such cases. Alternatively, it may be necessary to use the internal p.r.f. generator for receiver sensitivity and bandwidth checks where the station p.r.f is very close to a multiple of the a.c. mains frequency (*para.* 78 and 103).▶

Note . . .

Since the trigger socket on the test set is always connected by the rack wiring in parallel with the trigger input socket of the interrogator, operation of the INT. PRF *switch immediately triggers the interrogator. In consequence the facility must not be used when the equipment is in normal service otherwise the additional interrogations will break through on the responsor video channel and produce a spiral interference pattern on the display.*

23. Since there may be occasions, such as in servicing the test set, when a delayed trigger pulse is required for a UPM-6 or oscilloscope, a suitable

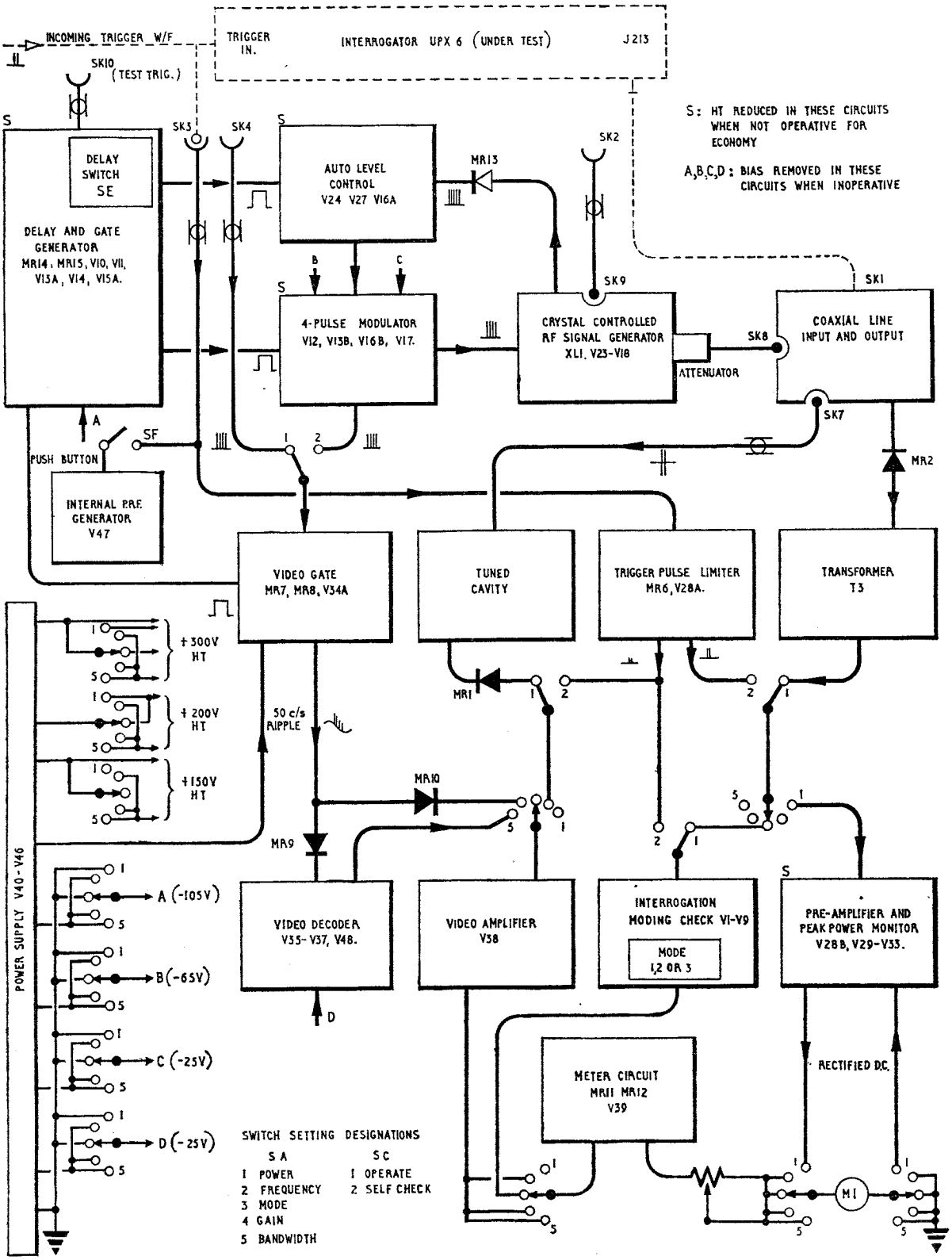


Fig. 5. Block diagram

pulse is developed by the same circuit which produces the 10 microseconds gating pulse for the signal generator (*para.* 18). This delayed pulse is brought out to a socket marked TEST TRIGGER located behind the hinged flap on the front panel of the test set.

Power supplies

24. Test set 4339 incorporates all its own power supplies and requires only a 230V or 240V 50 c/s single phase source. The appropriate transformer tapping is selected by a switch mounted behind the hinged flap on the panel. A microswitch is also provided in the input circuit to disconnect the AC supply when the test set is withdrawn from its cover. For setting-up and servicing purposes however, this microswitch can be operated manually to reconnect the AC supply (*para.* 87).

25. In order to reduce the load on the HT line those circuits which are not in use when the TEST switch is set to a particular function are operated at considerably reduced current. Thus, less heat is generated within the test set and a smaller power supply meets its requirements.

CIRCUIT DESCRIPTION

General

26. Although some of the circuits are interdependent due to the provision of the OPERATE/SELF CHECK switch, when considering the operation of the circuits which form test set 4339 each is regarded as an independent channel associated with the position of the TEST switch. In this way the sequence of events at each setting of the switch can be more clearly followed. The various positions of the TEST switch are

1 TX POWER
2 TX FREQ.
3 TX MODE
4 RX VIDEO GAIN
5 RX VIDEO BANDWIDTH

A circuit diagram of the test set is given in fig. 6.

Meter circuit

27. Since the meter is common to all five test circuits in the test set it is convenient to describe the operation of this circuit first to avoid numerous cross references. As stated in para. 10, for all but the first position of the TEST switch SA (at which the meter reading is proportional to the transmitter peak power output) the meter circuit is a p.r.f. sensitive device and is independent of the input level above a certain datum. The circuit employed consists of a flip-flop stage V39 and two crystal diodes MR11 and MR12. In the no-signal condition V39A is conducting since its cathode and grid are returned to earth. V39B is cut off by taking the grid through R200 to −25 V. A negative-going input is required to trigger the circuit.

28. Negative-going pulses fed to the cathode of MR12 cause the diode to conduct and the pulses are coupled via C127 and C128 to the grid of V39A. MR11 DC restores the junction of MR12 and the input capacitor to earth to prevent a charge being built up across the capacitor by successive pulses. On each pulse or group of pulses the flip-flop is triggered and V39B draws cathode current. The duration of the waveform at V39B anode is approximately 75 microseconds and the recovery time of the flip-flop is of the order of 0·5 millisecond so that on a train of four pulses the stage is triggered by the first pulse but ignores the three subsequent pulses. The meter, which is connected in series with R202 and the variable resistor RV12 between V39B cathode and earth, records the average cathode current flowing and the meter indication is thus proportional to the repetition frequency of the input pulses. By adjustment of RV12 the meter can be set to give full scale deflection at any given repetition frequency between 200 and 400 p.p.s.

29. The meter, which is an instrument with a range of 0—100 μA, is provided with five scales, one for each position of SA. The outer scale arc (1) is calibrated from 0—2 kW in steps of 0·5 kW. That section from 0—0·75 kW is coloured red and marked REJECT while the section from 0·75 kW to 2 kW is coloured green and marked ACCEPT. Scales 2 and 3 form an arc which is sub-divided into five parts, two red REJECT zones and three green sections marked 1/3, 1/2 and 1/1. For position 2 of SA the third green section only is used, any deflection outside this being in the REJECT area. With SA in position 3 all three green sections are used depending upon the interrogator mode or modes. The remaining two scales form an arc with only two calibration marks. One of these is at the centre and is marked SET GAIN. The other is marked SET METER and is the point to which the meter deflection is set by adjustment of RV12. It should be noted that the limits of scales 1, 4 and 5 do not denote the maximum deflection since in order to allow for small variations in the p.r.f. the meter is normally limited to approximately 95 per cent of its true full scale deflection.

Peak power monitor circuit (*SA—position* 1)

30. Power is measured by means of a slide-back peak valve voltmeter circuit in which the slide-back voltage automatically adjusts itself to the level of a pulse voltage proportional to the applied RF signal. The RF power to be measured on the test set is fed into the common input/output socket SK1 which is attached to a short section of fabricated coaxial line (*fig.* 4). At the other end of this coaxial section is a socket SK8 coupled by a short length of coaxial cable to the piston attenuator of the signal generator and the input line is terminated by resistor R247 in the attenuator. A preset adjustable coupling loop within the coaxial section samples the incoming signal to produce a voltage which is rectified by the crystal diode MR2. At the anode of MR2 appear negative-going video pulses with an amplitude proportional to the input RF voltage.

31. These pulses are applied to the primary of a pulse transformer T3 which has a step-up ratio of 1:3 so that across the secondary winding are developed positive-going pulses of greater amplitude. T3 secondary is connected via wafers on the

OPERATE/SELF CHECK and TEST switches to the grid of a triode pre-amplifier valve V29A via C99. The negative-going pulses developed at the anode of V29A are fed to the grid of a cathode follower stage V29B and the output from this valve is coupled via C101 to the cathode of a diode V28B which forms the input stage of the peak voltmeter.

32. V28B anode is taken via R152 and R245 to the junction of R168, R169 which is at approximately +50 V due to its connection through R170 to the 200 V line. The cathode of V28B is returned through R151 and R246 to the cathode of V32B and, in the no-signal condition, also rests at about 50 V. Capacitor C104, connected between V28B anode and earth, receives a small charge on each pulse (or the first pulse of the two interrogation mode pulses) which decays with a time constant of 1000 microseconds (C104 × R152). This sawtooth voltage waveform produced by successive recurrences is passed to a two-stage AC-coupled amplifier consisting of V30 and V31 and the resultant negative-going waveform developed at V31 anode is fed to a cathode follower V32A. A small amount of current negative feedback applied to both amplifier stages through the undecoupled cathode resistors R155 and R161 affords high frequency compensation.

33. Due to the AC coupling the DC level has been lost and the negative pulse output from V32A cathode is fed to a diode V33A whose action prevents any negative excursion but, in so doing, tends to limit the swing at V32A cathode. The resultant positive inverted exponential pulse waveform at V33A cathode is peak rectified by another diode V33B to produce a positive DC potential across C111. This capacitor and R165 have a sufficiently long time constant (1 second) to reduce the voltage ripple to negligible proportions. The voltage developed across C111 is applied to the grid of the output cathode follower V32B.

34. The DC potential at V32B cathode forms the slide-back voltage and is fed back through R246 and R151 to the cathode of V28B. Thus, any change in V32B cathode potential in a positive direction increases the bias on V28B cathode so that the diode conducts only on the peak of the input signal. The slide-back voltage is then approximately equal to the input voltage but must always be slightly less since the system operates as an error-actuated servo loop. However, the difference between the two voltages is a function of the amplifier gain and the slide-back voltage is equal to the true input voltage multiplied by a factor $\frac{1}{1+\frac{1}{G}}$ where G is the gain of the amplifier. Provided the gain is sufficient, i.e. greater than 100, the error will be less than 1 per cent.

35. Meter M1 is connected, through contacts on the TEST switch and series resistor R167, across R168 which forms part of V32B cathode load, the remainder of the load being made up of R166 and RV8. In consequence, the meter reading is proportional to the slide-back voltage, the ratio being dependent upon the setting of the preset control RV8. The outer scale arc of the meter is calibrated in terms of the peak RF power at the ANTENNA socket of the interrogator under test (0 to 2 kW), due allowance being made in the calibration procedure for the attenuation in the RF circuit linking the test set to the interrogator transmitter.

36. The overall gain of the power monitor circuit may be checked and/or set up by turning the OPERATE/SELF CHECK switch SC2 to SELF CHECK. When this is done the grid of the triode pre-amplifier valve V29A is disconnected from the secondary of T3 and connected to the anode of the diode V28A. The input to the circuit is then derived from the trigger pulses at SK3 and these pulses may come either from the external trigger source or from the internal p.r.f. generator if switch SF is depressed.

37. Since the amplitude of the trigger pulses may vary between wide limits, the incoming pulse train is first fed to a two-stage limiting circuit consisting of the crystal diode MR6, the diode valve V28A and the associated resistive networks. By doing the limiting in two stages, more effective clipping is achieved without the necessity for very high impedance circuits.

38. MR6 cathode is held at a fixed potential of 8V by its connection to the network R140, R143 and RV7 between the 150 V stabilized line and earth. The cathode of V28A is taken to the slider of RV7 and is also held at a fixed voltage derived from the stabilized line. When the amplitude of the input pulses exceeds 8V MR6 conducts so that pulses of substantially constant amplitude are passed to the second limiter. V28A anode is connected to the junction of the potentiometer resistors R229 and R144 and when the voltage at this point rises above the bias level at the slider of RV7, V28A conducts in turn. Thus, the amplitude of the input to the valve voltmeter circuit is determined by the setting of RV7 and is independent of the amplitude of the trigger pulses. Normally the amplitude of this input is adjusted by means of RV7 to correspond to 0·75 kW output from an interrogator (*para.* 98).

39. When the amplitude stabilized pulses are fed into the valve voltmeter circuit a deflection is obtained on the meter in exactly the same way as if an RF signal were applied to SK1 and RV8 in the cathode circuit of V32B can then be readjusted, if necessary, to set the meter to the standard reading of 0·75 kW. This peak power level is the minimum acceptable for the UPX-6 interrogator and on meter scale 1 is represented as the junction of the ACCEPT and REJECT zones.

Transmitter frequency checking circuit (*SA—position* 2)

40. For frequency checking a tuned cavity wavemeter is provided in the test set. The cavity is tunable and is calibrated over the range of 1000 to 1040 Mc/s. Normally it is preset and locked to the interrogator transmitter frequency of 1030 Mc/s.

41. The wavemeter input is derived through a coupling loop situated in the coaxial section into which the RF power is fed. A portion of the input

signal is picked up by the loop and passed, via a short length of coaxial cable, into the cavity where the line is terminated by a resistor R1. Provided the transmitter frequency coincides with the cavity tuning, the RF signal is rectified by a crystal diode MR1 in the wavemeter and fed through contacts on SC and SA to the grid of a video amplifier V38. The negative-going pulses developed at V38 anode are applied to the meter circuit to produce a meter deflection which is dependent upon the repetition frequency of the transmitter output.

42. Thus, a steady full scale deflection indicates that the meter circuit is receiving trigger pulses consistently above the minimum amplitude required and hence the presumption that the transmitter is on frequency within the bandwidth of the wavemeter cavity. On the other hand, no deflection at all or an unsteady one indicates a trigger pulse too low in amplitude and implies that the transmitter is off frequency for some reason or, if correctly tuned, is radiating an unacceptably low power.

43. If SC is set to the SELF CHECK position, the grid of V38 is connected to the junction of R141 and R142 so that the input trigger pulses, limited in amplitude by the action of MR6, are applied to the meter circuit. Since the trigger source p.r.f. is the same as that of the RF signal the meter deflection should be identical with that obtained when SC is in the OPERATE position, *i.e.* full scale if RV12 has been preset correctly.

Transmitter mode checking circuit (*SA—position* 3)

44. When the TEST switch is set to position 3, the output across the secondary of transformer T3, consisting of pulse pairs spaced at 3, 5 or 8 microseconds intervals, is switched from the power monitor circuit and applied to the input grid of a double-triode amplifying and limiting stage V1. The output at V1B anode is fed to both the control and suppressor grids of a coincidence valve V2. In the first case the signals pass to the control grid through a 0·63 microsecond delay line terminated in its characteristic impedance by R12, while undelayed signals are taken from the delay line input to V2 suppressor. V2 cathode is connected to the junction of R13 and R15 between +200 V and earth so that in the no-signal condition anode current through the valve is cut off.

45. The arrival of a pulse at either grid independently cannot cause anode current to flow and V2 conducts only when pulses appear simultaneously at both grids. Provided the duration of the input pulses exceeds 0·7 microsecond this condition is met and V2 conducts on each applied pulse to produce at its anode negative-going pulses whose duration is dependent upon the time overlap of the two pulses on the control and suppressor grids and thus upon the amount by which the input pulse duration exceeds 0·7 microsecond.

46. The negative-going pulses at V2 anode are applied to a flip-flop stage V3. V3B grid is returned to +200V via R21 and V3A grid is taken to the slider of RV1 which forms part of a potentiometer network between +200 V and earth. In the no-signal condition V3B is conducting and anode current through V3A is cut off. With the arrival of the pulses from V2 at V3B grid the flip-flop is triggered to produce at V3A anode negative-going pulses approximately 1 microsecond in duration. RV1 controls the level at which the flip-flop is triggered thereby also providing a means of setting the minimum duration of the input pulse at MR2 required to trigger the circuit. The waveform at V2 anode is approximately triangular in shape and any increase in V3A bias through adjustment of RV1 requires a corresponding increase in the input pulse duration to provide a larger trigger amplitude at V3A grid.

47. The 1 microsecond pulses developed by the flip-flop are passed to a video stage V4 in whose anode circuit is a short-circuited 0·27 microsecond delay line X2. The resultant output at V4 anode consists of positive-going pulse pairs, each pulse being 0·54 microsecond in duration.

48. From V4 anode the signal follows two paths to operate the pulse spacing checking circuit which employs the coincidence mixer principle. The leading edge of the first pulse in each pair initiates the action of a ringing circuit, preset to 3, 5 or 8 microseconds depending upon the position of the mode decoder switch SB, and the delayed output from the ringing circuit passes through a shaping circuit to one grid of the coincidence valve V9. Both pulses are applied direct to a second grid of the coincidence stage. The first pulse of the pair has no effect but provided the second pulse coincides with the pulse from the ringing circuit an output is obtained from V9.

49. The output from V4 anode is coupled to the grid of a triode valve V5A through C10. V5A is cut off by the positive bias applied to its cathode from the potentiometer network R32, R34 connected between +200V and earth. The anode of V5A is loaded with a capacitor C12 connected to earth and is coupled, via C13, to the grid of V5B whose anode load is a tuned circuit consisting of L3 and the associated capacitors C14 to C19 (the actual capacitors in circuit depending upon the position of SB). V5B is normally conducting.

50. With the onset of the first positive-going pulse from V4, V5A conducts and its anode potential falls, taking V5B grid below cut-off and discharging C12. The potential on this capacitor reverts exponentially towards the +300V HT line with a time constant of approximately 10 microseconds and V5B grid is held below cut-off for about 40 microseconds. When V5B is cut off, the tuned circuit in its anode oscillates for one positive half cycle, any further oscillations being damped out by the action of the diode V6A. Due to the limited time constant (of the order of 7 microseconds) of the coupling between the cathodes of V6A and V6B the positive half cycle is differentiated and the back edge appears at V6B cathode as a negative-going edge followed by an exponential rise to earth; this negative waveform causes V6B to conduct. In consequence, a negative edge ap-

pears at the grid of V7A and this edge is delayed by 3, 5 or 8 microseconds with respect to the leading edge of the first pulse of the pulse pair.

51. V7A is a triode amplifier which inverts the small negative pulse applied to the grid and produces a positive-going pulse of sufficient amplitude to trigger the succeeding flip-flop stage V8. V8 operates in precisely the same manner as the earlier flip-flop V3 so that a negative-going pulse exceeding 1 microsecond in duration is developed at V8A anode. This pulse is fed to the grid of V7B in whose anode circuit is another 0·27 microsecond short-circuited delay line X3. Thus, V7B produces positive-going pulses 0·54 microsecond in duration.

52. V9 is the coincidence valve and, in the no-signal condition, is cut off by the positive bias applied to the cathode from the potentiometer network R60, R61 connected between +200 V and earth. The positive-going pulse from V7B is fed to V9 control grid while the pulse pair from V4 is applied to the suppressor. The first pulse at the suppressor can initiate no action since there is no corresponding pulse at the control grid, but provided the pulse spacing of the input pulse pair is correct and the mode decoder switch SB is set to the appropriate position, the second suppressor pulse will coincide with the delayed pulse at the control grid thereby causing V9 to conduct.

53. The output at V9 anode is a negative-going pulse which is coupled through C27 and contacts on SA to the meter circuit input and triggers that circuit once for every pair of pulses with the correct spacing fed into the checking circuit. In consequence, the meter will give full scale deflection when only one mode corresponding to that selected by SB is consistently received. Where two or three modes are being interlaced (including the one selected by SB) the meter deflection will be one-half or one-third of full scale. In all cases the meter reading should be steady. If any of the readings is erratic or entirely absent it indicates one or more of the following defects:—

1. RF power output unacceptably low
2. RF pulse duration below specification
3. RF pulse spacing outside specification limts.

54. To check the operation of the circuit, switch SC is set to SELF CHECK. When this is done the trigger pulses at SK3, limited in amplitude by MR6, are applied to the grid of V1 in place of the RF input. At the same time the grid of V2 is switched to a tap on the delay line X1 so that the minimum pulse duration requirement is reduced to 0·3 microsecond. The reason for this reduction is that the minimum requirement of the interrogator is a trigger pulse of not less than 0·3 microsecond in duration and the circuit operation is checked on this basis although the normal duration of the pulses from waveform generator 6010 is 1 microsecond. Provided the mode checking circuit is operating normally the meter readings will be identical with those obtained when SC is set to the OPERATE position.

Receiver gain and bandwidth checking circuits (*SA—positions* 4 *and* 5)

Signal generator RF stages

55. The initial frequency for the signal generator is obtained from a crystal oscillator V23 employing a third overtone crystal XL1 in a series mode Colpitts circuit with the screen grid of the valve acting as the virtually earthed anode of the oscillator circuit. Inductor L9 is variable and is tuned to the series resonant frequency of the crystal. A DC return path for V23 cathode, which is above earth for RF potentials, is provided by a choke L8. An output is obtained from V23 anode due to coupling through the electron stream between screen grid and anode, a resistive load being used in the anode circuit to reduce pulling of the oscillator frequency.

56. The oscillator output is applied to the grid of a Class A amplifier V22 in whose anode circuit is an inductor L7 tuned to the fundamental frequency of the oscillator. The amplified signal from V22 is then passed to a chain of three frequency doublers V21, V20 and V19, each anode circuit being tuned to the second harmonic of the preceding stage so that the output at V19 anode is the eighth harmonic of the crystal frequency. V19 and V21 derive their HT supply from the 10 microseconds gating pulse (*para.* 62) and are thus non-conducting except within the gate period. This pulse HT supply enables the two valves to be operated at considerably higher current, so improving the second harmonic generation without any danger of excessive dissipation. HT for V20 comes from the automatic level control circuit (*para.* 70) which ensures that the output from the signal generator is held at a constant level.

57. The output stage of the signal generator is a grounded-grid triode valve V18 mounted in a hybrid cavity tunable by a variable capacitor C55. This stage operates as a frequency tripler so that the final output frequency is twenty-four times that of the crystal oscillator. Normally, V18 is cut off since its anode is returned, through R103, to −12·5V but the application of a pulse train from the modulator (*para.* 64) allows the valve to conduct and produce a pulse-modulated RF output.

58. Three outputs are taken from the final stage via pick-up loops within the cavity. The first is fed through a 52-ohm piston attenuator, to SK1 giving, at this socket, a signal which is variable from 35 to 80 dB below 1V corresponding to a signal level through the directional coupler into the UPX-6 receiver of 55 to 100 dB below 1V. The attenuator control is calibrated in terms of the voltage available at this input to the receiver. A second RF signal is brought out to SK2 and the coupling loop is adjusted to provide a preset level of 45 dB below 1V (again in terms of the signal available at the UPX-6 receiver input). The third output is applied to a crystal diode MR13 which produces at its cathode positive-going video pulses. These are used to operate the automatic level control circuit.

59. The normal output frequency of the signal generator is 1090 Mc/s ± 0·25 Mc/s but all the circuits are capable of being tuned over a range

of 1080 to 1120 Mc/s. By using the appropriate crystal, any frequency in this range can be selected. The oscillator crystal is located behind the screw cap marked XTAL on the front panel.

Delay and gating circuit

60. The delay circuit for the signal generator consists of a suppressor-triggered phantastron V11 and the clamping diodes V10A and V10B. In the quiescent condition, V11 suppressor is held negative with respect to the cathode so that anode current through the valve is cut off and all the space current is taken by the screen. The phantastron action is initiated by the positive-going trigger pulses fed in at SK3 and applied to the cathode of the crystal diode MR14 through C29. MR14 acts as an amplitude limiter for the incoming pulses while MR15 and C34 isolate V11 from the triggering source to prevent the stage being triggered back on the back edge of the pulse. While V11 anode is running down, the screen potential rises to produce a square pulse whose duration is controllable by RV2 or RV4 depending upon the position of switch SE.

61. The back edge of ◀V11▶ screen waveform, differentiated by C149 and R74, produces a small negative-going pulse which is applied to the grid of a triode amplifier V13A. At the anode of V13A appears a positive-going pulse occurring at a fixed time (depending upon the setting of the appropriate delay control) after the leading edge of the original trigger pulse.

62. The positive-going output from V13A anode is used to trigger a blocking oscillator V14A. In the no-signal condition V14A is cut off through the control grid connection to the potentiometer network R78, R79 between −105V and earth.. With the onset of the positive pulse from V13A, V14A conducts and regeneration occurs through the action of transformer T1 so that a pulse of approximately 10 microseconds in duration is developed. This pulse is then applied to the grid of a cathode follower V14B where it is limited in amplitude by the action of the diode V15A. At V14B cathode appears a positive-going pulse approximately 170V in amplitude which provides the HT supply for valves V19 and V21 in the signal generator and for V26 in the automatic level control circuit (*para.* 70). The same waveform, capacitance coupled through C151, is also applied to the video level checking circuit (*para.* 75) for gating purposes.

63. V14B cathode load is divided into two parts R82 and R83. Across R83 is developed a pulse of the same duration as the HT pulse but of considerably smaller amplitude and this is brought out to a socket SK10 (TEST TRIGGER) mounted behind the hinged flap on the front panel. A delayed trigger pulse is thus available for a UPM-6B or oscilloscope when servicing test set 4339.

Modulator circuit

64. The modulator for the signal generator consists of a cathode-coupled flip-flop stage followed by a blocking oscillator. The 10 microseconds pulse from V14B cathode, differentiated by C40 and R87, is applied to the grid of V12A and the positive pip coinciding with the leading edge initiates the flip-flop action. Due to the time constant of the input coupling R86 and C41 a small delay is introduced so that V12A can be triggered after the leading edge of the 10 microseconds pulse, the exact value of the delay being preset by C41. This is done to enable the pulsed RF stages in the signal generator (V19 and V21) to build up to full amplitude before the application of the modulation pulses to V18.

65. When the flip-flop is triggered, a positive-going pulse is developed at the anode of V12B. The duration of this waveform is controlled by the variable capacitor C42 which is normally preset to give a pulse duration just sufficient to allow V17A to produce a train of four pulses. V12B anode waveform is fed to the grid of a cathode follower stage V13B which is normally held beyond cut-off by the negative bias applied to the grid from the slider of RV5.

66. V17A is a triggered blocking oscillator modified by the addition of a delay line to determine the duration of the pulses produced by the circuit. The anode and grid are coupled together by means of two windings of a three-winding transformer T2 and the output pulses are taken from the third winding. One end of the grid winding is connected to an open-circuited 0·15 microsecond delay line X4, the circuit to earth being completed via R94 which is taken to −25V. V17A is thus cut off and the stage is triggered on the grid by the positive-going pulse from V13B.

67. When the trigger pulse is applied to the grid of V17A, regeneration due to the positive feedback causes the grid to rise rapidly and grid current flows with the result that a large negative voltage appears across the grid winding and acts as a charging source for the delay line. As the delay line charges, a negative-going rectangular wave travels towards the open end where it is reflected without change of phase. On its return to the input end the voltage across the line is increased to twice its original value and, since V17A grid falls by the same amount, anode current is cut off. The duration of the output pulse is thus twice the transit time of the delay line or about 0·3 microsecond. However, due to circuit tolerances, the output pulse duration is not entirely governed by the delay line and a preset trimmer capacitor C180 is connected across part of the line to enable the pulse-length to be set to 0·3 microsecond. While V17A anode current is cut off the delay line discharges through R95 and R94.

68. After the delay line has discharged, V17A grid rises but, since the gating pulse is still present at V13B cathode, is not held at its initial steady potential and continues to rise above earth. In consequence, the valve draws anode current, the anode voltage falls and the regenerative cycle is repeated, resulting in a second 0·3 microsecond

pulse. The recovery time of the blocking oscillator is mainly determined by the product of R95 and the total capacitance of the line and is approximately 1·5 microseconds, although a measure of control over the spacing between pulses can be achieved by variation of RV5 which governs the trigger pulse amplitude. Thus, provided C42 in the flip-flop circuit is correctly set, V17A produces four pulses of 0·3microsecond duration and spaced at 1·5 microseconds intervals during the period of the gating pulse. After the fourth pulse the back edge of the gate waveform cuts off anode current through V13B and V17A grid returns to its steady potential until the next triggering pulse arrives.

69. The train of four pulses developed across the tertiary winding on T2 is fed to the grid of a cathode follower V17B and the output from the cathode is limited in amplitude by the action of the diode V16B. Due to the presence of the diode some pulse stretching occurs so that the waveform applied to the anode of V18 in the signal generator consists of a train of four pulses, each of the order of 0·4 microsecond in duration and approximately 160V in amplitude. A small portion of the same signal (about 3·5V) appearing at the junction of R98 and R99 is fed to the video checking circuit (*para.* 83).

Automatic level control circuit

70. The purpose of this circuit, which consists of valves V24, V25, V26 and V27, is to ensure that the signal generator output remains at a constant level and is substantially independent of voltage flutcuations and changes in modulator pulse amplitude due to aging effects or variations in mains voltage. A portion of the signal generator RF output is rectified by the crystal diode MR13 to produce at the cathode positive-going video pulses whose amplitude is proportional to the output level of the signal generator. These are then applied to a two-stage video amplifier V27 and V26. V27 anode is returned through R135 to the + 150V line but the HT supply to V26 is the 10 microseconds gating pulse from V14 (*para.* 62) stabilized in amplitude by the action of the diode V16A whose cathode is connected to the + 150V stabilized line.

71. The pulses appearing at V26 anode are fed to a gas-filled tetrode valve V25 whose control grid is maintained at a large negative potential determined by the setting of RV6 connected between − 12·5V and − 105V. When the signal generator is delivering its normal output into the attenuator, the amplitude of the pulse appearing at V26 anode is just sufficient to cause V25 to conduct once on approximately each alternate group of pulses received and an output is developed at the cathode. Due to the long discharge time constant of C92 in the anode circuit of V25 the duration of the cathode waveform is long in comparison with that of the triggering pulse. This waveform is then smoothed by the RC filter consisting of R124, R125, R127 and C89, C90, C91, C93 to produce a ripple-free DC potential which is applied to the grid of a cathode follower V24B. The same DC potential also feeds back through the resistor chain and raises the bias at the cathode of V25 so that the valve is not normally triggered by the next pulse group. By the time a third pulse group has arrived this bias has decayed and V25 is probably triggered again.

72. V24B cathode is DC-coupled to the grid of V24A and V24A anode is connected to that of V20 in the signal generator. Thus, any variation in V24B cathode potential will produce a change of voltage at V24A anode and hence at the anode of V20. If, for any reason, the output of the signal generator falls, the proportion of pulses which succeed in triggering V25 will also fall and the DC potential at V24B grid is lowered. A decrease in V24B grid potential will cause V24A to pass less anode current so that its anode voltage rises, bringing about a corresponding rise at V20 anode. Conversely, any increase in the signal generator output will produce an increase in the potential at V24B grid so that V24A anode voltage falls. In this way, a state of equilibrium is maintained and the signal generator output is held constant at a level which is determined by the setting of RV6.

Video response checking circuits

73. The provision of the signal generator enables a suitable RF signal to be fed into the interrogator receiver but, in addition, some means of observing the receiver output is required. This facility is provided by the receiver video response checking circuits which examine the receiver output to check that both sensitivity and bandwidth are adequate.

74. When the signal generator is coupled to the interrogator receiver the signal appearing at the video output socket of the interrogator has similar characteristics to the waveform produced at the cathode of V17B but, depending upon the receiver gain control setting, may also be modulated with noise. This signal is coupled back into the test set at SK4 (VIDEO) and thence to the grid of a cathode follower V34A. Since the interrogator video output is positive-going, positive pulses of a few volts in amplitude are developed at the cathode of V34A and these are passed to a gate circuit consisting of the crystal diodes MR7, MR8 and resistors R173, R174, R175.

75. The common anode connection between the two diodes is taken via R122 and C151 to the anode of the HT pulse limiting diode V16A associated with the ALC amplifier valve V26. Normally, the anodes of both diodes rest at earth potential and the circuit does not respond to positive pulses. However, immediately the 10 microseconds gating pulse arrives at V16A anode, MR7 and MR8 conduct so that any coincident input pulses from the interrogator pass to the succeeding stages. The junction of MR7 and MR8 is also connected through R231 and C114 to one side of the 6·3V heater supply with the result that a small amount of AC ripple is introduced into the circuit. This ripple, which is added to any video pulses present, causes their peaks to fluctuate at 50 c/s and a similar amplitude variation occurs in the pulses appearing at MR8 cathode. The purpose of superimposing a sinusoidal waveform on the pulses is to facilitate setting the receiver gain control and the point is more fully explained in para. 77 and 78. The train of four

pulses appearing at the cathode of MR8 now follows two paths and, depending upon the setting of the TEST switch SA, one or other of the two channels applies a signal to the meter circuit.

Receiver gain check (SA—position 4)

76. For this test the signal is fed to the anode of a crystal diode MR10 whose cathode is held above earth potential through the positive bias developed across RV11 which forms part of a potentiometer network between +30V and earth. In position 4 of the TEST switch, MR10 cathode is connected via C124 to the grid of the meter circuit input amplifier V38. Thus, any signal pulse with an amplitude greater than the DC level at the slider of RV11 is amplified by V38 and triggers the meter circuit. If the resultant meter deflection is full scale, it indicates that during each recurrence of the gating waveform there is at least one pulse arriving from the receiver with an amplitude exceeding the level predetermined by the setting of RV11.

77. Due to the sinusoidal variation in the amplitude of the pulses at MR10 anode produced by the added AC waveform, there will be one setting of RV11 at which only 50 per cent of the pulses will trigger the meter circuit, giving half scale deflection. This condition is used as a criterion for setting the receiver gain control. RV11 is first preset to give half scale deflection on the meter, *i.e.* the central line of the green zone on scale 4, for a predetermined video input level which is normally 2V peak at SK4. The receiver gain control is then adjusted to produce a similar half scale deflection. If, at any subsequent check of the receiver (with the same attenuator setting) the meter reading is within the green zone on scale 4, the receiver gain is within approximately ±1dB of the correct setting.

78. Without the injected AC ripple the gain control would be more difficult to adjust, particularly at short ranges when the receiver gain-time control is switched on. Under these circumstances the receiver gain is low, no noise is present in the output and any variation in the amplitude of the video pulses is very small. As a result, the meter circuit is triggered either 100 per cent or not at all for small changes in the gain setting. By adding the AC ripple within the test set there is a smooth relationship between the meter deflection and adjustment of the receiver gain control. With a weaker RF signal and a higher receiver gain setting, noise modulation is added to the AC modulation and the resultant random fluctuation causes the meter needle to waver about a mean deflection.

◀**Note . . .**

Oscillation of the meter needle about a mean point may also be caused by a beat frequency where the p.r.f is within one or two cycles of a multiple of the a.c. mains frequency. Test set 4339 *is inherently sensitive to repetition frequencies of this order when used as a r.f. signal generator for checking the receiver sensitivity and bandwidth of the IFF interrogator. To ensure that this characteristic does not affect adjustment of the interrogator gain control a suitable test procedure has been devised and details are given in para.* 103 *to* 105.▶

Receiver bandwidth check (SA—position 5)

79. The signal at MR8 cathode is also applied to the anode of another crystal diode MR9 whose cathode is similarly returned to a potentiometer network between +30V and earth, the DC level being set by adjustment of RV9. MR9 cathode is coupled via C115 to the grid of a video amplifier V35 which, in turn, is coupled to another video stage V48. Any signal with an amplitude exceeding the value of the positive bias at RV9 slider is passed to the video amplifier to produce, at V48 anode, a positive-going pulse train.

80. The positive-going pulses from V48 anode are applied to the grid of a trigger valve V36A. V36A anode is DC-coupled to that of a line-controlled triggered blocking oscillator V36B which is normally cut off since its grid is taken to −25V. With the arrival of a positive-going pulse at V36A grid, the anode potential falls causing a similar fall at V36B anode and the valve conducts. The circuit associated with V36B is similar to that of the modulation pulse generator V17A (*para.* 66) so that the stage produces a 0·3 microsecond pulse for each triggering pulse at V36A grid. Provided a train of four pulses is fed to V36A, the resultant output developed across the tertiary winding on transformer T4 will be four pulses of equal amplitude and 0·3 microsecond in duration.

81. The signal appearing across the tertiary winding of T4 is then applied to an integrating circuit consisting of the diode V37A, capacitor C120 and resistor R187. V37A cathode is DC-coupled to the anode of a second diode V37B whose cathode is held at a fixed potential above earth. Each pulse produces an increase in the charge built up across C120 but the values are so chosen that only on the fourth pulse does the voltage across C120 rise above the bias level at V37B cathode. When this occurs V37B conducts and, provided SA is set to position 5, a single wavefront is fed to the grid of V38 to trigger the meter circuit. In consequence, as long as the interrogator receiver bandwidth is such that the video output is a faithful reproduction of the input RF signal from the signal generator, the meter circuit will be triggered by each pulse train.

82. Potentiometer RV9 is preset so that only pulses exceeding a predetermined level are of sufficient amplitude to operate the meter circuit. As described in para. 77, the four pulse decoding circuit including V36 is similarly triggered intermittently due to the superimposed AC ripple and in position 5 of SA (as in position 4) there is a smooth relationship between the meter deflection and the receiver gain control setting.

Video response circuit self check facilities

83. When SC is set to SELF CHECK, the input to

the video checking circuit is provided by that part of the modulation pulse train developed across R99 in the cathode circuit of V17B. This signal passes through the checking circuits in the same manner as the interrogator signal but, due to its amplitude (of the order of 3·5V), produces full scale deflection for normal settings of RV11 and RV9 in both positions 4 and 5 of the TEST switch.

Internal p.r.f. generator

84. Under certain conditions it is possible that the normal external trigger source may not be available for triggering purposes. To enable the test set to be used in such cases, an internal pulse generator is provided consisting of a double-triode valve V47 with transformers T6 and T7. V47B is connected as a conventional free-running blocking oscillator but is inoperative since its HT supply is broken through switch SF. When SF (INT PRF) is depressed HT is applied to V47B and V47A grid is connected to −25V. By the normal regenerative action of a blocking oscillator, V47B then produces pulses approximately 4 microseconds in duration, the repetition frequency of which is controlled by RV13. By adjustment of the preset control RV13 on the front panel the p.r.f. can be set to any value in the range 180 to 300 p.p.s.

85. The pulse appearing across the tertiary winding on T6 is fed to the grid of a cathode follower stage V47A in whose cathode circuit is the primary winding of a 3:1 step-down transformer T7. The output pulse is developed across T7 secondary winding and is fed, via contacts on switch SF, to socket SK3 (TRIGGER). It should be noted that the internally generated pulse is only available whilst SF is held depressed and also that a single pulse is generated and not a pulse pair. Even with a single pulse however, most of the interrogator checks can be performed and only the interrogator moding cannot be checked.

Power supplies

86. All the voltages required by the test set are provided by a single transformer T5 with suitable secondary windings. The transformer operates from a 230 or 240V 50 c/s single-phase source, the appropriate primary tapping being selected by a switch SG mounted under the hinged flap on the front panel. Adequate protection against overloads is afforded by fuses FS1, FS2 and a thermal cut-out in the primary circuit.

87. As a safety precaution, a micro-switch SJ is included which automatically breaks T5 primary circuit whenever the test set is withdrawn or partially withdrawn from its cover. However, many of the preset controls are mounted on the chassis and have to be adjusted under operating conditions. To achieve this the micro-switch can be locked in the on position manually by pulling the operating rod as far as possible towards the rear of the unit. When the test set is re-inserted in its cover the micro-switch will automatically revert to its normal spring-loaded mode of operation due to its pressure exerted by the bracket at the back of the cover.

88. The whole of the high voltage secondary winding on T5 supplies a full-wave rectifier valve V43 and the resultant DC output, after smoothing by a tuned choke input filter L1, C146 and C145, forms the +300V line. Any residual ripple on the line is cancelled by a ripple eliminator valve V46A to whose grid is fed a portion of the ripple voltage existing across C145. The antiphase voltage at V46A anode is fed back to the 300V line to cancel the ripple. RV14 provides the necessary adjustment of V46A input and is set for minimum ripple voltage at the output.

89. Tappings on T5 secondary supply two full-wave rectifier valves V41 and V42 which give, after smoothing by a tuned choke input filter consisting of L2, C147 and C143, a DC line of +200V. V46B serves as the ripple eliminator valve for this rail.

90. The +200V line is connected through R207 and R237 in parallel to a gas-filled stabilizer valve V44 to provide a stabilized reference potential of +150V. A potentiometer network R214 and R215 across this supply gives, at the junction of the two resistors, the +30V bias level for the receiver gain and bandwidth checking circuit.

91. The remaining tappings on T5 secondary are connected to the cathodes of a full-wave rectifier valve V40 the output from which, after smoothing by a RC filter C148, R222 and C144, is applied to a gas-filled stabilizer valve V45 to provide a stabilized negative line of 105V. All the remaining bias potentials are derived from a potentiometer network R218-R221 connected across the supply.

92. Transformer T5 has three low voltage secondary windings to supply the valve heaters. One side of the first winding is earthed but the second winding has one side connected to a potential of approximately 50V at the junction of R216, R217 across the 150V stabilized supply. This is done in order not to exceed the maximum heater/cathode voltage on some of the valves in the unit. The third winding is floating and supplies only the heater of the grounded-grid triode output stage in the signal generator since this valve has the cathode internally connected to one side of the heater.

93. It will be noted that all three HT lines are routed through contacts on the TEST switch SA and that in certain positions of the switch large value series resistors are introduced. The reason for this is that it is not necessary for all the circuits within the test set to be operative simultaneously and a considerable saving in HT current is possible if the circuits not required during any particular test can be switched off. It is, however, undesirable from consideration of valve life to remove the HT voltage completely from the valves concerned or even allow them to idle without any anode current flowing. In consequence, series resistors are switched into circuit to reduce the applied HT voltage whilst the grid bias of those valves which normally operate in a cut-off condition is removed by other sets of contacts on SA. The valves from which the grid bias is removed in this way are V14A, V13B, V17A and V36B. Valves which are

biased through cathode resistors have this bias automatically reduced when the HT voltage is lowered.

SETTING-UP PROCEDURE

General

94. The initial calibration and setting-up of the circuits employed in test set 4339 are performed by the manufacturer and the stability is such that this calibration can be relied upon for reasonably lengthy periods. In certain cases however, the original settings may be affected by ageing of components; alternatively, it may become necessary to change some of the operating levels. For this purpose, and for convenience in making adjustments at first line, as many as possible of the preset controls concerned are grouped together on the front panel and covered by a hinged flap. In some parts of the setting-up procedure however, it may be necessary to re-adjust a few of the internal presets and details of these are given in the succeeding paragraph.

95. The preset controls available on the panel are:—

RV6 — SET RF — Sets the signal generator output level.

RV8 — SET POWER METER — Sets the meter calibration for the peak power monitor circuit.

RV12—SET METER—Sets the meter circuit to the desired p.r.f.

RV13—INT PRF — Sets the internal pulse generator to the required p.r.f.

In the same compartment as the presets listed above are the coaxial socket SK10 (TEST TRIGGER) and switch SG (230-240V). The internal presets which may need re-adjustment are:—

RV7 — for setting up the peak power monitor circuit under self check conditions.

RV11—for setting up the receiver gain checking circuit.

RV9 — for setting up the receiver bandwidth checking circuit.

These controls are mounted on the top chassis and their location is shown in fig. 3.

Note . . .

No attempt should be made to re-adjust any preset controls not mentioned in the setting-up instructions.

96. As stated in para. 4, the test set is permanently mounted in a rack and interconnected with the interrogator. Removal is not intended except for servicing purposes. To facilitate access to the interior when setting up, the case is provided with a mechanical latching system which comes into operation immediately the test set is partially withdrawn. Using the handles provided, the test set should be withdrawn from its case and allowed to tilt gently down at an angle of approximately 30 deg. until it is held by the latching system. While in this position access to the lower chassis is possible by releasing the captive bolts at the rear of the upper chassis and raising it as shown in fig. 2. If the test set is to be removed completely from the rack it must be supported firmly underneath, using two hands, and held in a horizontal position while an assistant raises the latch bar. The test set can then be completely withdrawn.

WARNING . . .

No attempt must be made to remove the test set from the rack single-handed.

97. In the instructions which follow, it is assumed that the test set is in position in its rack and normally connected. Before commencing operations the UPX-6 interrogator, test set 4339 and test set UPM-6B must be switched on and allowed to settle down during a warming-up period of at least ten minutes. If it proves necessary to re-adjust any of the internal presets, the test set 4339 should be withdrawn from its case and allowed to hang down supported by the latching system. While thus withdrawn, the micro-switch SJ must be operated manually as described in para. 87.

Peak power monitor circuit

98. The following procedure should be adopted in setting up this circuit:—

(1) Disconnect the test set 4339 cable from the 20 dB RF PROBE socket on the interrogator and in its place couple the appropriate cable from a test set UPM-6B. Remove the cover over the interrogator tuning controls and detune the transmitter until the UPM-6B meter reading corresponds to 0·75 kW, making allowance for the necessary correction factors.

(2) Disconnect the test set UPM-6B and reconnect test set 4339 to the interrogator. Note the scale deflection on the test set meter. Should this be more or less than 0·75 kW, open the hinged flap on the panel and adjust RV8 (SET POWER METER) until the meter reading is 0·75 kW, *i.e.* the needle lies at the junction of the red and green arcs.

(3) Set SC to SELF CHECK and note that the meter reading is still 0·75 kW. If necessary, vary the internal preset RV7 until the correct deflection is obtained.

(4) Return SC to OPERATE and re-tune the interrogator transmitter for maximum power output as indicated on the test set 4339 meter. Replace the cover over the UPX-6 tuning controls.

Video response checking circuits

99. In setting up the receiver testing section of the test set the preferred method is first to set the video level and then to adjust the signal generator output. The procedure for setting up the video circuits is as follows:—

(1) Connect an oscilloscope CT316 in parallel with the video input to the test set from the associated interrogator. Trigger the oscilloscope with the pulse appearing at the TEST TRIGGER socket on test set 4339. Set the TEST switch to position 4.

Note . . .

The parallel connection normally taken to the radar office may be used to provide the input to the oscilloscope. The loss of a termination to the receiver output when the radar office cable is disconnected from the interrogator is unimportant for the purpose of this test.

(2) Set the test set ◀4339 attenuator▶ control to 60dB and reduce the interrogator receiver gain until the first pulse displayed on oscilloscope CT316 is 2V in amplitude

(3) Note the meter reading and, if necessary, adjust the internal preset RV11 until the meter deflection is half-scale, *i.e.* the mid-point of the green zone on scale 4.

(4) Set the TEST switch to position 5 and adjust the interrogator receiver gain control until the fourth pulse is 2V in amplitude. Again note the reading on the meter and, if necessary, adjust RV9 until half scale deflection is obtained.

Signal generator output level

◀**100.** The signal generator output is set by reference to a test set UPM-6B in the following manner: —

(1) Unlock the five captive retaining screws located at the edges of the front panel and withdraw the UPX-6 interrogator from its case until the rear right-hand sub-chassis is accessible. Remove V108, thereby disabling the transmitter modulator. Remove the GTC shorting link O-109 from its retainer and plug it into sockets J111 and J112. Push the UPX-6 right back into its case in order to operate the mains interlock switch.

Note . . .

These steps are necessary to safeguard the UPM-6B and to obtain full receiver gain independent of the gating and GTC circuits.

(2) Using either a special connector assembly or a BNC T-adaptor UG 274/U, connect the TEST TRIGGER socket on test set 4339 to the SYNC IN socket on the UPM-6B, maintaining the trigger connection to the oscilloscope made in para. 99(1). Connect the S-G OUT socket on the UPM-6B direct to the 20DB RF PROBE socket on the UPX-6 using the standard 10 ft. RF connector W703 supplied with the UPM-6B. Set the TEST SELECTOR switch on the UPM-6B to position 5 and the TEST switch on test set 4339 to position 4.

(3) Set the OUTPUT LEVEL control on the UPM-6B to give an input to the UPX-6 receiver equivalent to that of test set 4339 with its attenuator control set to 60 dB. To obtain this value, refer to the spot calibration table supplied with the UPM-6B; the appropriate dial setting is given in column (n). The nominal setting is 21·7dB less than the level required (to allow for the attenuation of the 20dB RF PROBE circuit and connector W703), *i.e.* 38·3 dB. Adjust the interrogator receiver gain control until the amplitude of the pulse observed on oscilloscope CT316 is 2V.

Note . . .

As the UPM-6B pulse is generated at the end of the trigger pulse, it is not gated by the test set 4339 *video detector circuit and does not, therefore, produce a deflection on the meter of test set* 4339.

(4) Disconnect the UPM-6B RF connector W703 from the UPX-6 and reconnect the test set 4339 RF cable to the 20DB RF PROBE socket. Set the test set 4339 attenuator control to 60dB and note the amplitude of the first pulse displayed on the CT316. This should be 2V. If it is not, adjust RV6 as necessary until an amplitude of 2V is obtained. When these adjustments (3) and (4) have been correctly done, the test set 4339 meter should indicate half-scale deflection.

(5) Reconnect the UPM-6B connector W703, to the 20DB RF PROBE socket on the UPX-6 and repeat the foregoing procedure to check the calibration of test set 4339 at 86 dB. This value represents a typical normal sensitivity setting for the UPX-6. Set the UPM-6B OUTPUT LEVEL control to the value given in column (m) of the spot calibration table (nominal value 86 − 21·7 = 64·3 dB) and readjust the UPX-6 receiver gain control until the pulse is 2V in amplitude, measured from the underside of the noise on the baseline to the mean of the noise and ripple on top of the pulse.

(6) Disconnect the UPM-6B connector W703 and reconnect the test set 4339 RF cable to the 20 DB RF PROBE socket on the interrogator. Vary the attenuator control on test set 4339 until the amplitude of the first pulse displayed on the CT316 is 2V. The reading of the test set attenuator control should then be within ±1 dB of 86 dB and the test set meter should fluctuate about the half-scale deflection mark.

Notes . . .

If this figure of 86 *db* ± 1 *dB cannot be obtained, it indicates that either the check has not been made with sufficient care, or one or other of the two test sets has a faulty attenuator. One possibility must be guarded against; the gain of the UPX-6 is affected by variations in mains voltage and by operating temperature. For this reason, the instructions in para.* 97 *concerning warming-up must be strictly adhered to and the period of ten minutes is the minimum permissible. In addition, it is important that the sequence of operations detailed in para.* 100 *be performed in the order given (each test following immediately after the preceding one) to avoid the effect of any further appreciable change in temperature or a possible variation in mains voltage.*

If the TEST *switch on test set* 4339 *is subsequently turned to position* 5 *it may be observed that the mean meter reading*

falls slightly. This is caused by the last of the four pulses being smaller in amplitude then the first pulse due to the limited low frequency video response of the UPX-6 receiver output circuits. It should, however, be possible to restore the half-scale deflection with the attenuator set to a reading approximately 1 dB lower than that required on position 4.

(7) Withdraw the UPX-6 from its case, remove the GTC shorting link from sockets J111 and J112 and replace it in the stowage clip provided. Replace V108. Re-insert the UPX-6 in its case and secure the retaining screws.

WARNING . . .

If, for any reason, test set 4339 is to be left switched on after the setting-up is completed, it is important to prevent interference with the PPI displays. Accordingly, ensure that the TEST switch is not left in position 4 or 5. ▶

Meter circuit

101. Since for all settings of the TEST switch except position 1 the meter circuit is a p.r.f. sensitive device, it is essential that the meter response should remain substantially constant if the readings are to be relied upon. For this purpose RV12 is provided to compensate for any variations which may occur in the trigger p.r.f. or in the characteristics of the meter circuit. To reset the meter circuit it is only necessary to set the TEST switch to position 2, SC to SELF CHECK and adjust RV12 until full scale deflection is obtained.

Internal pulse generator

◀**102.** As explained in para. 84, the repetition frequency of the internal generator is variable over a small range but it is normally set to the same value as the station p.r.f. Assuming that the meter circuit has been set up at the station p.r.f. then, with waveform generator 6010 switched off, SA in position 2, SC set to SELF CHECK and SF depressed, adjust RV13 until the meter reads full scale deflection. However, whilst this procedure may suffice in the majority of installations, there may be occasions when it is necessary to set the internal generator to a different p.r.f.

103. As stated in the note following para. 78, the test set is inherently sensitive to repetition frequencies of the order of multiples of the a.c. mains frequency and the effect is a beat frequency, causing the meter needle to swing between 40% and 60% of full scale deflection. For a routine check of the equipment settings this introduces no inaccuracy provided it is confirmed that the needle is swinging symetrically about the half-scale point, but difficulty may be experienced when adjustment of the interrogator gain control is necessary. It is possible to make a series of incremental changes in the gain control setting and, after each, to observe the symmetry or otherwise of the oscillation. This procedure is satisfactory for beat frequencies of 2 c/s and upwards but becomes cumbersome if the beat frequency is much lower.

104. The problem can be completely overcome by setting the internal generator to a slightly different frequency from the station p.r.f. and using it in place of the external trigger for interrogator gain control adjustment. The procedure is as follows.

(1) Set SC to SELF CHECK and check that the meter indicates full scale deflection. Adjust RV12 if necessary.

(2) Arrange for all mode generation to cease; e.g. by switching off the appropriate power unit 4465 or, if a test switch unit 4821 is in circuit, by setting all its switches to OFF.

(3) Depress the INT P.R.F. push button on the test set and adjust RV13 so that the meter reads 95% of full scale deflection, corresponding to the inner boundary of the green zone on scale 3. This sets the internal generator 5% or approximately 12 cycles, below the station p.r.f.

105. Once the adjustment of para. 104 (3) has been made and maintained by periodic checks all that is necessary for subsequent checking or adjustment of the interrogator gain control setting is to switch off the external triggers and depress the INT P.R.F. button. With a beat frequency of at least 10 c/s the only wavering of the meter needle will be that due to receiver noise.

Note . . .

In removing the external triggers, disconnection of the trigger and/or video connections in the radar head is not advisable. Unless special precautions are taken the pulse amplitudes on the lines concerned will be disturbed. The preferred method is to switch off the waveform generator or the associated power unit 4465 *in the radar office.*

P.r.f. limitations

106. Test set 4339 has been primarily designed to operate at repetition frequencies of the order of 250 c/s and although a wide tolerance is provided the following limitations of p.r.f. versus range should be noted.

P.R.F. *c/s*	*Maximum range* *(miles)*
200	250
250	250
280	220
300	205
350	180
400	160

107. If the p.r.f. at a particular setting of the RANGE control is outside the limits specified in the preceding paragraph, the phantastron circuit (V11 and V10) is unable to recover and begins to divide by two. This effectively halves the p.r.f. on receiver tests (positions 4 and 5 of the TEST switch SA) and a decreased meter reading results. ▶

Chapter 2
(completely revised)

MISCELLANEOUS TEST UNITS

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

General

1. In order to facilitate the setting-up or testing of certain major units in the IFF Mk. 10 radar office equipment, three small test units are provided in each installation. These are : —

Switch unit 4821 (*Stores Ref.* 10F/18185)

Test meter (voltage) 4883 (*Stores Ref.* 10S/16688)

Tester (relay unit) (*Stores Ref.* 10S/16689)

The switch unit is normally stowed in rack (IFF control) 4467 but the other two items are held in the workshop.

2. Switch unit 4821 and test meter (voltage) 4883 are designed to assist in setting up or checking waveform generators 6010 and power units 4465. By using these test units any necessary adjustments may be made without the necessity for switching on the whole installation.

3. Tester (relay unit) provides a means of checking a relay unit 6009 on the bench. When a relay unit develops a suspected fault it cannot conveniently be tested *in situ* and the normal practice is to replace it with a serviceable unit. The unserviceable unit may then be removed to the workshop where it is checked with the aid of tester (relay unit) until the fault is located.

4. In addition to the foregoing units, SIF installations have two additional test units, a multimeter 12124 and a test switch unit 12432. The multimeter provides facilities for monitoring d.c. voltages and currents in power unit 6889, decoder, video (passive) 6892 and test set 4678 under operational conditions. Test switch unit 12432 simulates the switching facilities of control units (passive) 12118 and (mode 1) 12117 when using test set 4678 to test decoders 6892 in the radar office.

Switch unit 4821

5. This unit, illustrated in fig. 1 and 2, is provided to afford local control of mode switching at a waveform generator 6010 completely independent of the normal display switching. A circuit diagram is given in fig. 3.

6. The unit consists of a small box carrying three switches ; a 12-pole plug is fitted at one end of the box and a 12-pole socket at the other. It is normally housed at the rear of rack (IFF control) 4467 by engaging the socket with an unwired 12-pole plug provided for stowage purposes.

7. When a waveform generator is to be set up or tested, the control rack lead terminated in SK1 is removed from PL1 at the rear of the waveform generator and switch unit 4821 is inserted in its

Fig. 1. Switch unit 4821 : exterior view

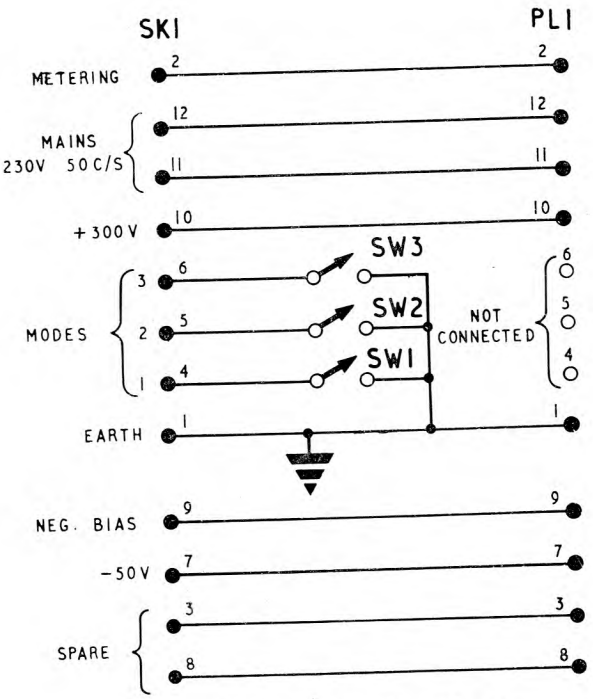


Fig. 3. Switch unit 4821 : circuit

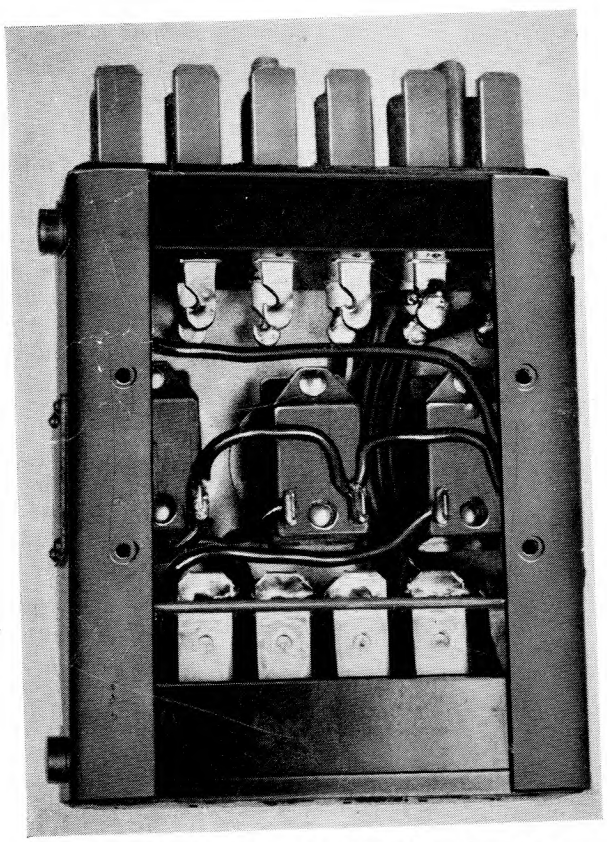


Fig. 2. Switch unit 4821 : interior view

Fig. 4. Test meter (voltage) 4883 : exterior view

place. SK1 is then coupled to PL1 on the switch unit. The supplies fed to the waveform generator via PL1/1, 2, 7, 9, 10, 11 and 12 pass through the switch unit uninterrupted but the mode switching leads from the relay unit are disconnected. Instead, mode switching is achieved by the operation of switches SW1, SW2 and SW3 which earth the appropriate points in the waveform generator depending upon the mode selected. In this way modes 1, 2 or 3 can be selected at the control rack independently of the usual switching system.

Test meter (voltage) 4883

8. Any change exceeding ±2V in the nominal +300V supply from power unit 4465 to the waveform generator after the equipment has been set up may disturb the operation of the counter circuits. To ensure that the HT supply remains constant in the event of operation of the automatic changeover system it is necessary for the HT lines in all three power units to be matched within the limits of ±1V. Test meter (voltage) 4883 enables this to be done accurately and quickly.

9. The test meter consists of a suppressed zero meter giving a wide scale difference per volt at the required voltage (+300), a resistor chain for setting-up purposes and a lead terminated with a 2-pole plug. The whole assembly is mounted in a metal case which has a stowage compartment at one end for the lead and plug (*fig.* 4 *and* 5). A circuit diagram is given in fig. 6.

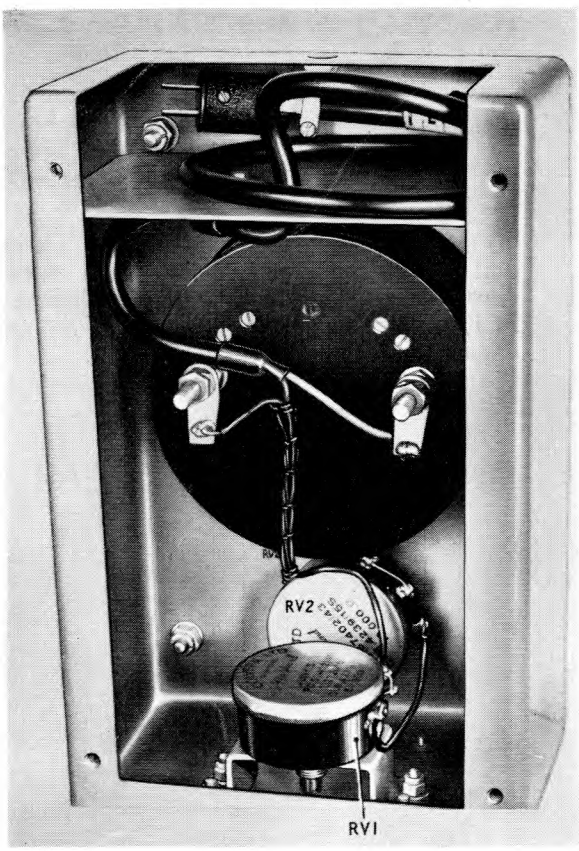


Fig. 5. Test meter (voltage) 4883 : interior view

10. Assuming that all three power units have been correctly set up on panel (metering) 4466, the method of using test meter (voltage) 4883 is as follows : —

(1) Connect the 2-pole plug on the test meter to the 2-pole socket marked +HT METER on power unit 4465 No. 1 (the bottom unit in the rack) and adjust RV2 on the test meter until the meter pointer coincides with the centre line on the scale.

(2) Without disturbing the setting of RV2, plug the meter into the +HT METER socket on power unit 4465 No. 2 and, if necessary, adjust the set +HT controls on that unit until the meter pointer again coincides with the centre line on the scale.

(3) Repeat operation (2) for power unit 4465 No. 3.

11. The lines on either side of the centre line on the meter scale are provided for use after the initial setting-up procedure is completed. When making subsequent day-to-day checks of the power unit HT lines the procedure described in para. 9(1) is first followed. The test meter is then connected to the other two power units in turn. In each case provided the meter pointer lies between the outer lines no further adjustment of the controls is necessary.

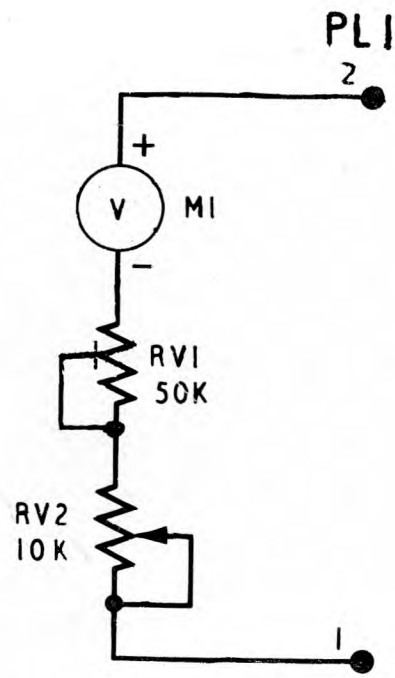


Fig. 6. Test meter (voltage) 4883 : circuit

12. RV2 is adjusted by the knob on the panel of the test meter and is the manual setting-up control as described in para. 9(1). The preset resistor RV1 in series with RV2 is included to set the meter range and, when once adjusted, should not be disturbed. If, for any reason, resetting of RV1 becomes necessary, a known source of voltage is required, such as a power unit 4465 accurately set up on panel (metering) 4466. With the meter connected across this source and RV2 slider set to the centre of its travel, RV1 is adjusted until the meter pointer coincides with the centre line on the scale.

Tester (relay unit)

13. Tester (relay unit), in conjunction with an ohmmeter, provides the facilities required for testing a relay unit 6009 on the bench. The unit contains a 50V 150mA supply and a wafer switch by means of which the internal supply may be used to energize the head and mode selection relays in the relay unit. The components are assembled in a metal case (*fig.* 7) with a stowage compartment at the top for the mains and test leads (*fig.* 8). On the underside of the lid of this compartment is a label bearing an abbreviated test procedure.

14. A circuit diagram of tester (relay unit) is given in fig. 9. The 230V 50 c/s mains supply is fed in via switch SW1, fuse FS1 and a thermal cut-out to the primary winding of transformer T1. FS1 affords protection against large and possibly temporary overloads due to circuit fault conditions while the thermal cut-out is included to protect the transformer against overheating caused by smaller but prolonged overloads.

15. The voltage developed across the secondary of T1 is fed to a full-wave metal rectifier MR1 and the negative side of the resultant DC output is taken, through fuse FS2, to the moving contact on SW2/a and direct to one tag of the 2-way fanning strip. The fixed contacts on SW2/a are connected to tags on the 4-way fanning strip so that −50V may be switched to relays AB/HJ or G/N. The positive side of the supply is earthed.

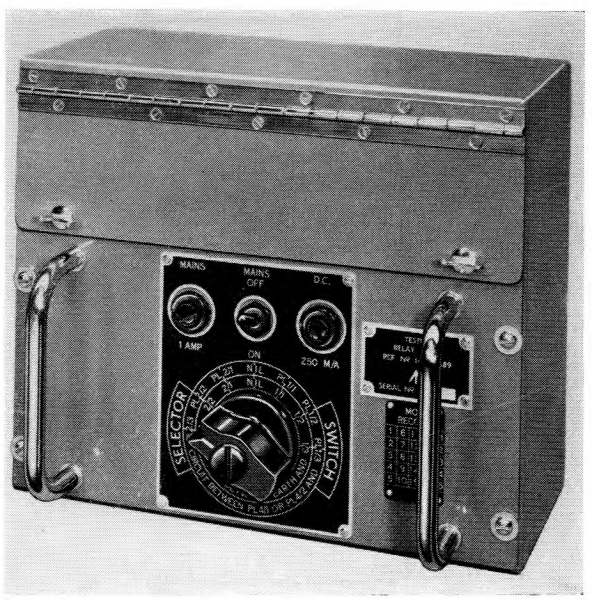


Fig. 7. Tester (relay unit)

Note . . .

The 4-way fanning strip bears dual markings because it is common to both channels of the relay unit. In use it is connected to the appropriate part of the relay unit terminal block, i.e. to A/B, G, C and D for channel 1 *or to H/J, N, K and L for channel* 2.

16. The moving contacts on the other two wafers of SW2 (b and c) are connected to earth and the fixed contacts are connected to tags C/K and D/L on the fanning strip. Thus, operation of the switch places an earth on one or both of these points so causing the mode selection relay in the relay unit to be energized.

17. The following procedure is used in checking a relay unit 6009.

(1) Open the stowage compartment on the tester (relay unit), extract the leads and connect the 2-way fanning strip marked −50V and E to those points on the 8-way terminal block on the relay unit.

(2) Depending upon which channel is to be tested, connect the 4-way fanning strip to A/B, G, C and D or to H/J, N, K and L on the 10-way terminal block on the relay unit.

(3) Set the SELECTOR SWITCH on the relay tester to NIL, connect the mains plug to a 230V 50 c/s source and set SW1 to ON.

(4) Using an ohmmeter, check that terminals 1/1, 1/2, 1/3, 2/1, 2/2 and 2/3 on the 8-way terminal block of the relay unit have no continuity to earth or with each other. Check similarly the coaxial lead connections PL1/1, PL1/2, PL1/3, PL2/1, PL2/2, PL2/3, PL4/1 and PL4/2.

Note . . .

There should be a resistance of approximately 33,000 *ohms between the centre conductors of PL*4/1 *and PL*4/2 *and earth.*

(5) Turn the selector switch to 1/1. Check that a connection is made between 1/1 on the 8-way terminal block and earth, also between PL1/1 and PL4/1. Check similarly for the other positions of the selector switch.

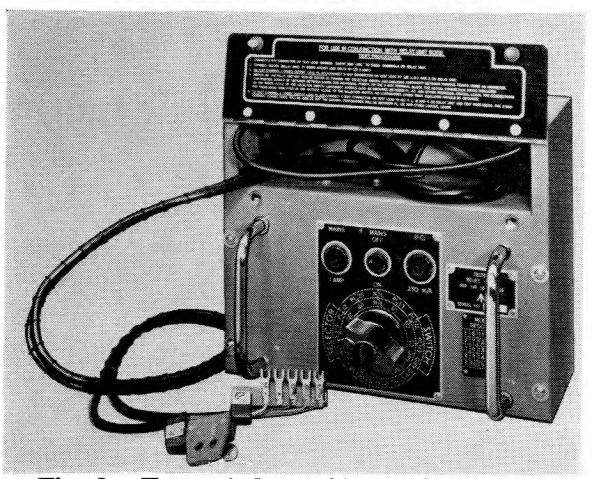
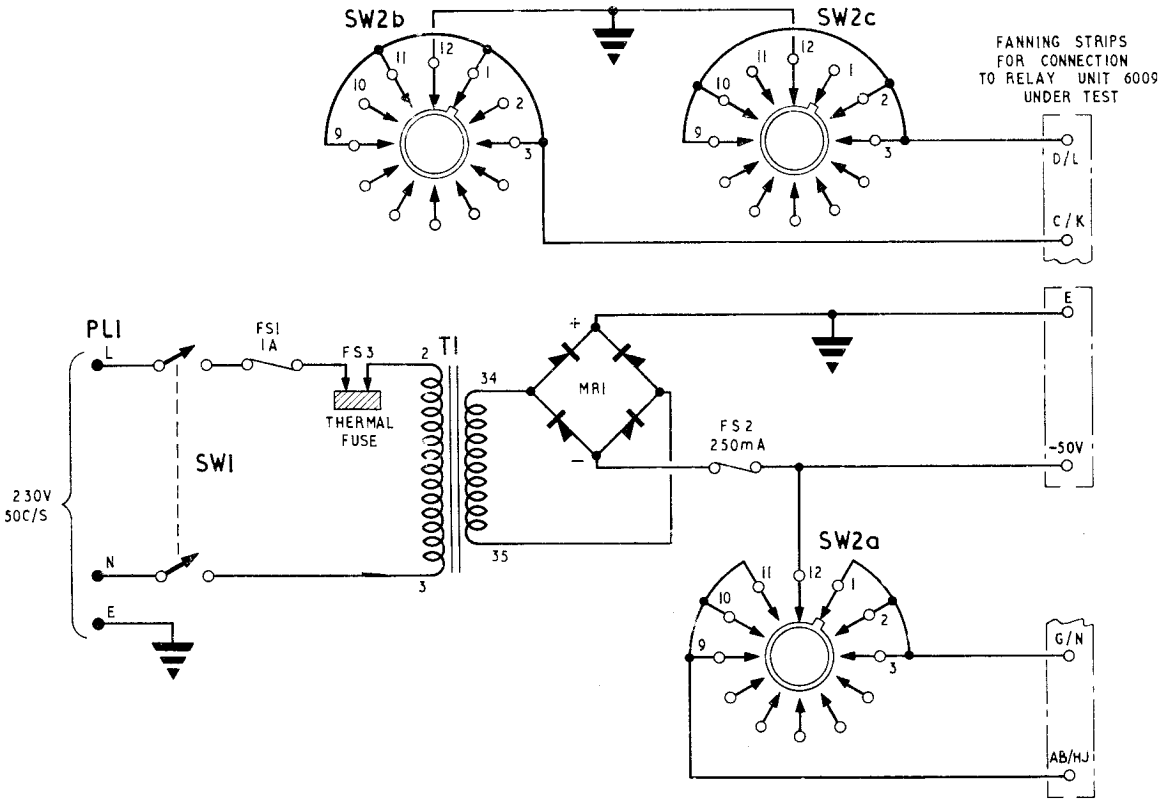


Fig. 8. Tester (relay unit) showing stowage compartment



SW2 POSN	RELAY UNIT 6009 FUNCTION	SW2 POSN	RELAY UNIT 6009 FUNCTION
1	1/1 TO EARTH PL1/1 TO PL4/1 OR PL4/2	9	2/3 TO EARTH PL2/3 TO PL4/1 OR PL4/2
2	1/2 TO EARTH PL1/2 TO PL4/1 OR PL4/2	10	2/2 TO EARTH PL2/2 TO PL4/1 OR PL4/2
3	1/3 TO EARTH PL1/3 TO PL1/1 OR PL4/2	11	2/1 TO EARTH PL2/1 TO PL4/1 OR PL4/2
		12	NIL

Fig. 9. Tester (relay unit) : circuit

18. A detailed test procedure for relay unit 6009 is given in Section 2.

Multimeter 12124

19. This unit, illustrated in fig. 10, consists of a sensitive moving-coil meter and selector switch housed in a steel case. Hooks, secured to the rear of the case, allow the meter to be hung on one of the handles of the unit with which it is being used. Connection to the unit is made through a length of cable terminated with a 25-pole plug. A tablet showing the monitoring point for each position of the selector switch is mounted on studs at the back of the case. Slots in the tablet permit it to be drawn out to the right-hand side.

20. A circuit diagram of multimeter 12124 is given in fig. 11. The instrument, which has a full scale deflection of 200μA, is connected in series with R1 to the moving contacts of the wafers of switch SWB, the fixed contacts of the switch being connected to the appropriate pins of PLA. R1 serves to protect the meter from overload damage and, when taking a reading, the safety switch SWA is depressed. This action removes R1 from circuit and substitutes R2.

21. No multipliers or shunts are provided in the multimeter. The units with which it is associated have the necessary resistors incorporated and the values are chosen so that a standard reading of 100μA $\pm$ 20μA indicates correct performance. Points at which a reading of less than 10μA is obtained are indicated on the tablet.

Test switch unit 12432

22. To permit testing the passive decoders in the radar office in situ, the functions of control unit (passive) 12118 and control unit (mode 1) 12117 are embodied in a single test unit. The unit also has mode selection and ALL SIGS/ALL CODES/ONE CODE switches.

23. Test switch unit 12432, illustrated in fig. 12, consists of a rectangular steel case with a top cover on which is mounted a sub-panel carrying the

switches. A U-shaped plate, welded to the back of the case, allows the unit to be hung on one of the handles of the decoder with which it is being used.

24. One side of the case is hinged and secured with spring fasteners. On releasing the fasteners the side plate drops down to reveal a stowage compartment housing two cables terminated in 12-pole and 25-pole plugs. These provide the interconnections between the test unit and the decoder rack.

25. A circuit diagram of the switch unit is given in fig 13. PLB is used when testing mode 1 decoders in rack 12276 and is coupled to ASKL on the rack. The required decoder can then be selected by rotation of SWG and the desired code set up on SWA and SWB. When testing mode 2/3 decoders in rack 4469, PLA is used and must be coupled to the appropriate console socket at the base of the rack. Since each rack 4469 may contain up to 8 passive decoders, each decoder serving a different console, there are 8 possible orientations of the inserts in the console sockets ASKAA to BSKP on rack 4469. In consequence, PLA is a modified item and serves as a master plug which may be coupled to any 25-pole socket.

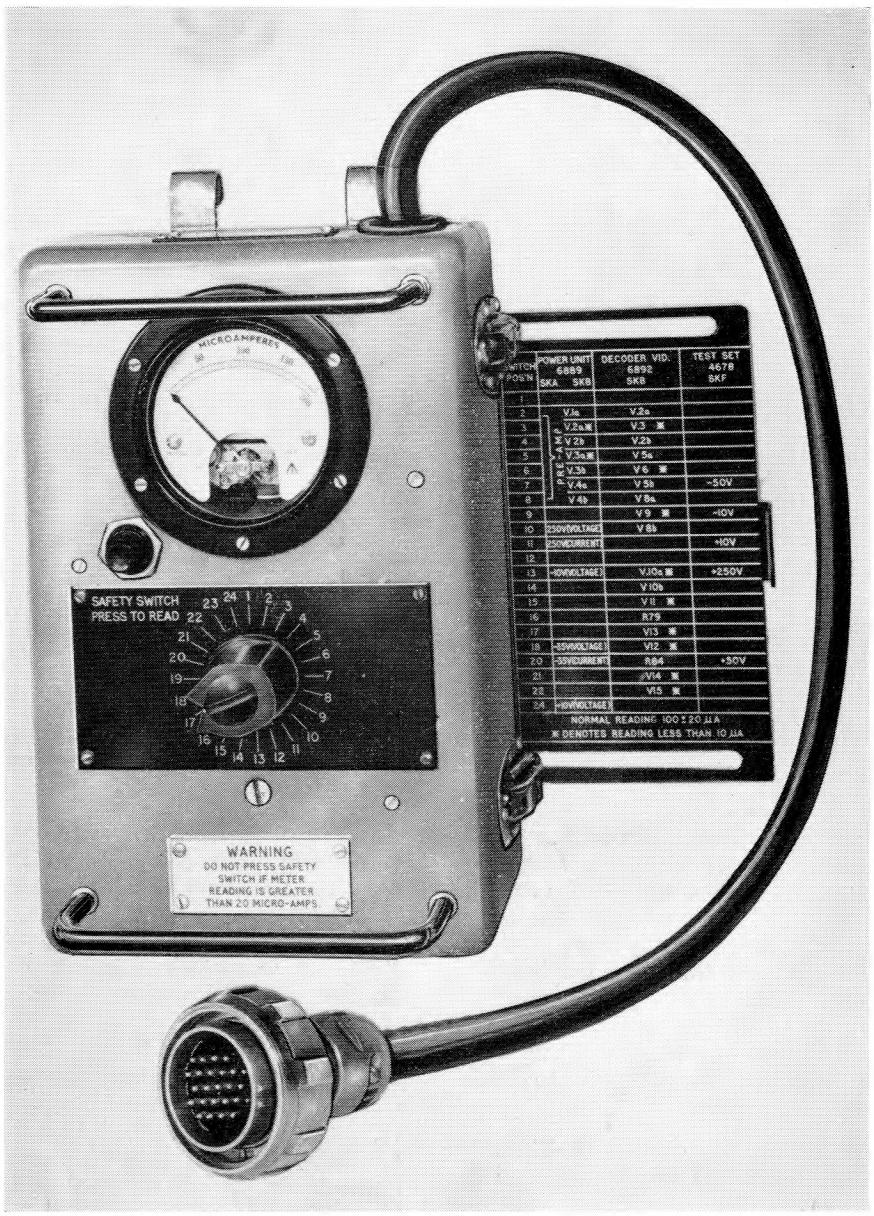


Fig. 10. Multimeter 12124

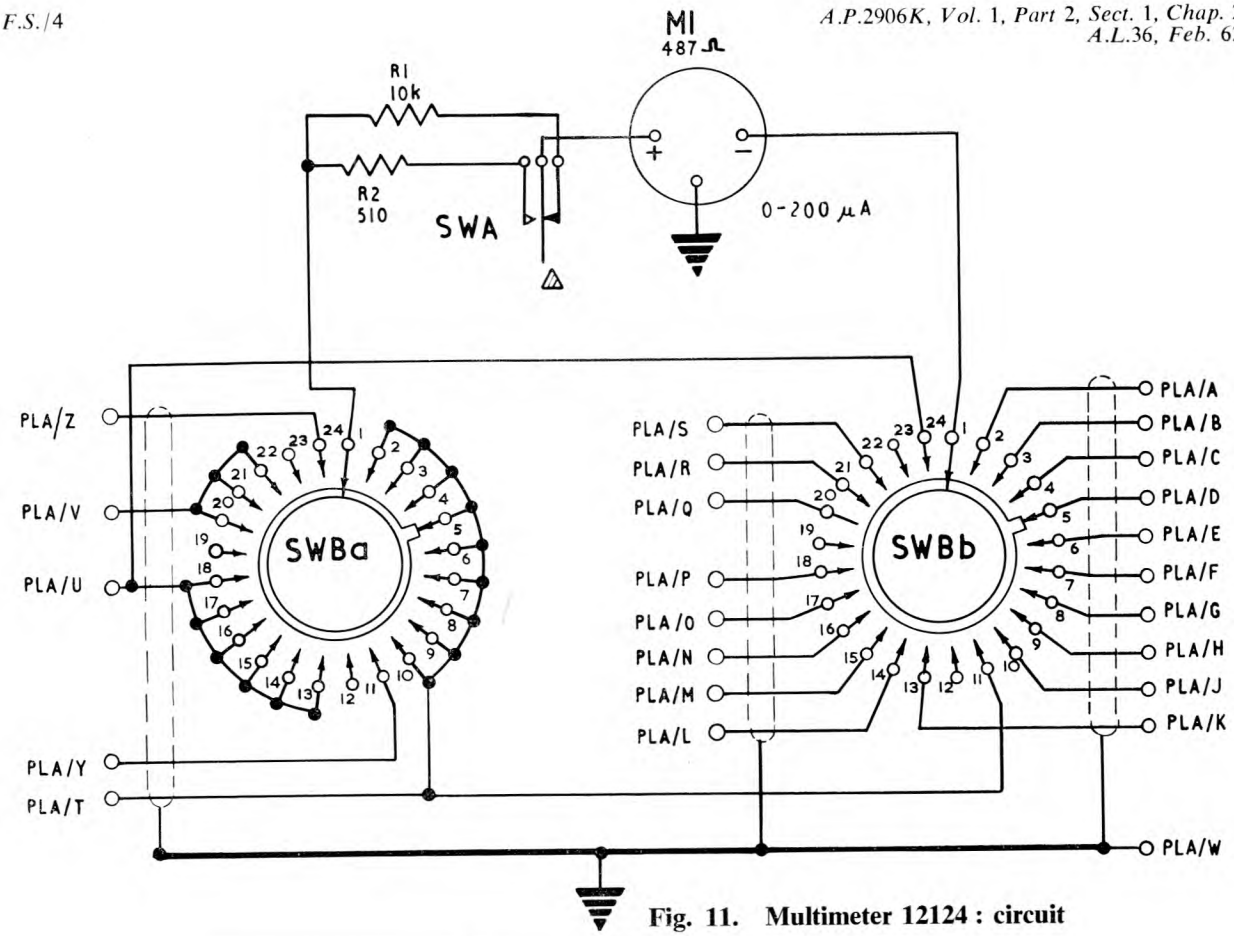


Fig. 11. Multimeter 12124 : circuit

Fig. 12. Test switch unit 12432

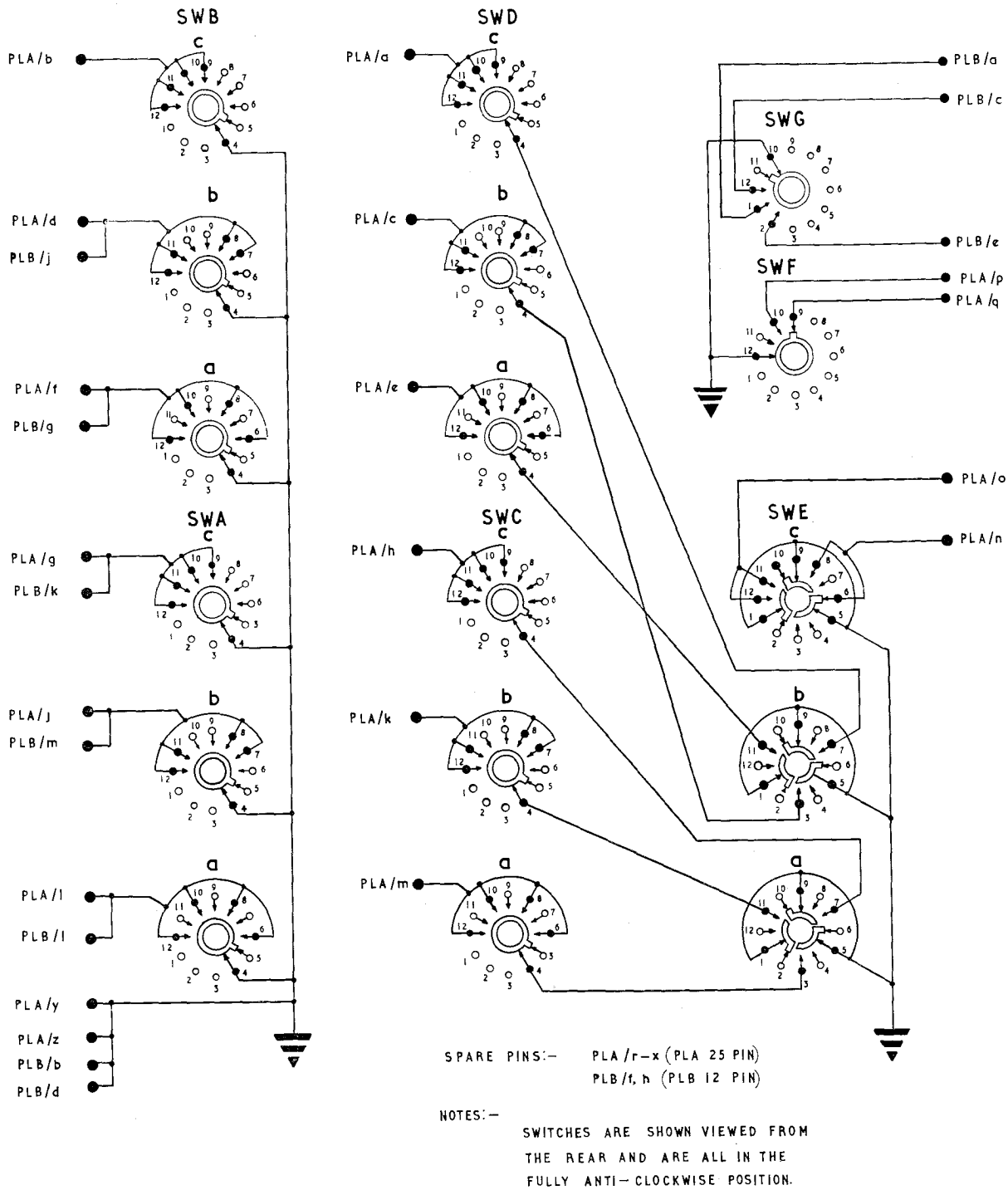


Fig. 13. Test switch unit 12432 : circuit

Chapter 3

TEST BENCH 6042

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LIST OF ILLUSTRATIONS

General

1. Test bench 6042 is intended to support an interrogator-responser and associated equipment during servicing operations. Originally, the test bench was designed for wider application and in one installation was provisioned as a means of housing all the IFF Mk. 10 radar head equipment with the exception of the interrogator. In consequence, a considerably greater range of facilities has been incorporated than is required for servicing purposes. The particular application mentioned however, no longer exists and most of the facilities are redundant although the bench has not been modified to remove them.

2. In the majority of installations the test bench is located in a workshop at the radar head. Its exact position depends upon the accommodation available at the head but it is usually sited in a reasonably close proximity to the interrogator to avoid the necessity for transporting equipment over appreciable distances.

DESCRIPTION

Test bench

3. A complete assembly of test bench, junction box and test set mounting is illustrated in fig. 1. The bench itself consists of an angle-section steel framework with a Formica-covered wooden top and measures approximately 28 in. wide × 22 in. deep × 34 in. high. A shelf and sub-frame are provided within the main framework for mounting transformer units 4463 and 6428 but since transformer unit 6428 is not now used with the bench the sub-frame is redundant.

4. At the right-hand side of the bench, and extending the full depth, is a junction box. As explained in para. 1, this incorporates many facilities no longer required and the junction box now serves mainly as a distribution panel for the AC supplies and trigger waveform to the test set and interrogator. A drawer, in which connectors and similar small items may be stored, is included.

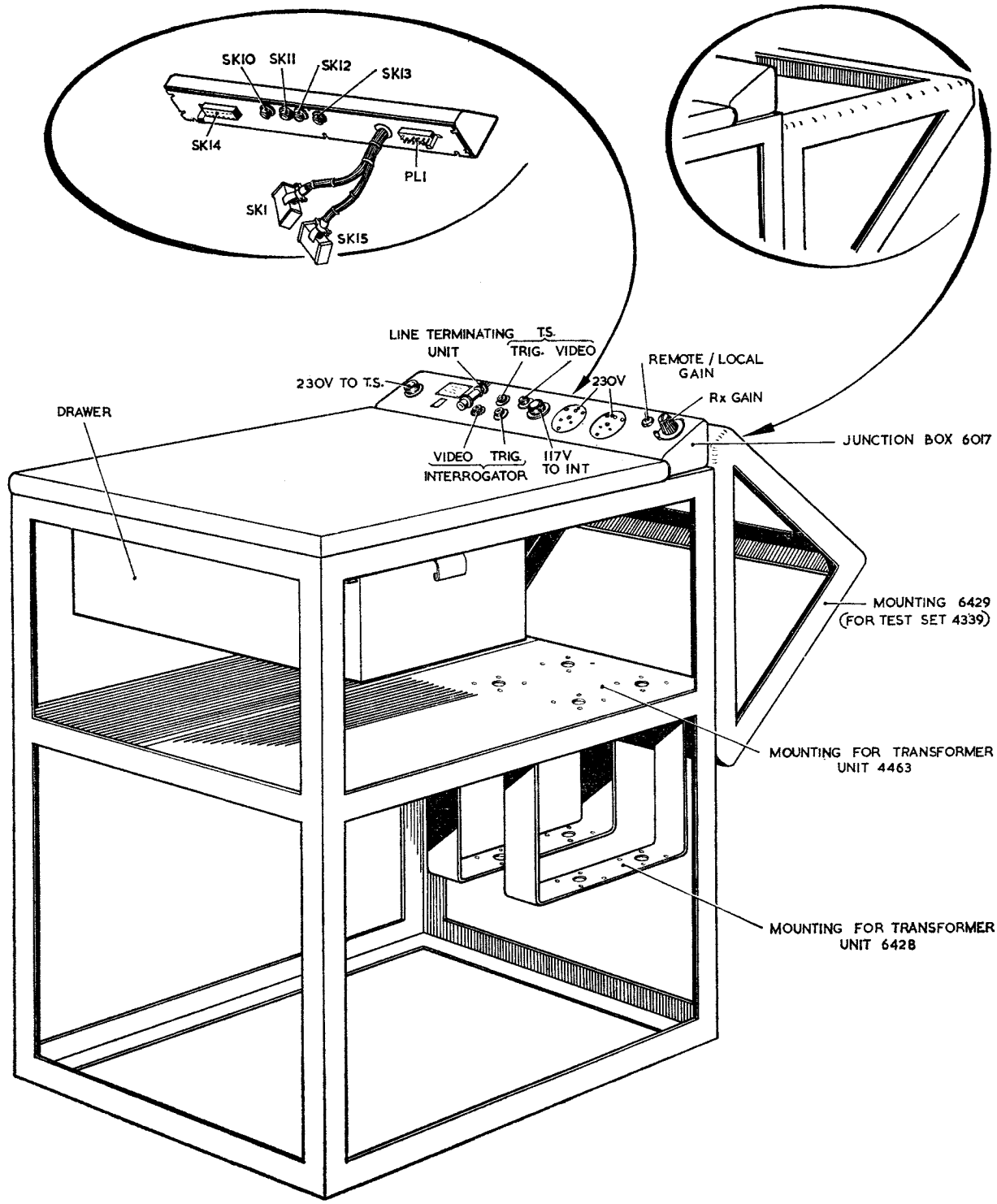

Fig. 1. Test bench 6042

Mounting 6429

5. This consists of a triangular framework also constructed of angle-section steel. It extends the full depth of the bench and is bolted to the right-hand side. If the mounting is to support a test set, radar, 4339, it is fitted with the longest side vertical so that the test set mounting face is at an angle of approximately 45 deg. to the bench top. In order that the mounting may be used to support a test set UPM-6B, one of the shorter sides is drilled to correspond with the bench fixing holes. By reversing the mounting it can then be attached with one face parallel to the bench top. This alternative position is shown inset in fig. 1.

6. The mounting is provided with four special bolts which engage with keyhole-shaped slots in the bench upright members and these bolts must be located in the appropriate set of holes in the mounting depending upon the fitting position desired. When the mounting is added, the width of the bench is increased to 40 in. or 42 in. according to the angle of the mounting.

7. Three connectors for interconnecting the interrogator and test set 4339 are provided with each mounting 6429. They form part of the mounting and are secured to it by clips.

8. It should be noted that mounting 6429 is not necessarily supplied as part of the test bench. In general, a mounting is included in all installations where a spare test set 4339 is likely to be available but in other cases it may or may not be provided. Where there is no spare test set 4339 but a mounting is supplied, it should be fitted so that one side is parallel to the bench top and a wooden platform added to support a test set UPM-6B. If no mounting is supplied, a suitable shelf must be constructed to support the UPM-6B.

Junction box 6017

9. This unit is illustrated in fig. 1 and a circuit diagram is given in fig. 2. Its primary purpose was to provide control facilities at the radar head, similar to those in the radar office, for an interrogator not readily accessible. These facilities are not now required and the junction box is used only as a distribution panel for the AC supplies and the trigger waveform.

10. The test bench is regarded as a movable device and, in general, will not be permanently wired to a 230V source. An input plug PL1 is provided and it is intended that this should be connected by a suitable cable to a convenient 15A outlet in the workshop. From PL1 the 230V supply is routed to sockets on the junction box and to transformer unit 4463. The 117V supply from the transformer unit for the interrogator is similarly brought out on the junction box.

11. The method of deriving the trigger waveform for the interrogator and test set depends upon the type of radar head. In some casese, e.g. radar Type 80, a separate cable is provided from the radar office to the head for the test bench with the radar office end either stowed or connected to a spare waveform generator 6010. In other installations, such as radar Type 79, the test bench may be supplied from a T-junction on the main trigger connector to the radar head.

12. It will be noted in fig. 1 that a line terminating unit is attached to the junction box. This again is one of the redundant facilities but it may be usefully employed to terminate the trigger line, in the absence of an interrogator, where a separate cable from the radar office is provided. It must however, not be used if the test bench is supplied from a T-junction on the main connector.

◀ Interconnections between test bench and waveform generator

13. In all IFF Mk. 10 installations a spare waveform generator 6010 is provided at the top of rack (IFF control) 4467. However, the rack only provides stowage for this unit so that it is unconnected and cannot be used in the existing position. In general, at a one-head station there will be only one operational waveform generator installed in position 4 or 6, the other position being blanked off by a panel, stowage 6810. On such sites it is possible to employ the spare waveform generator to provide a semi-permanent trigger connection to the test bench in the following manner.

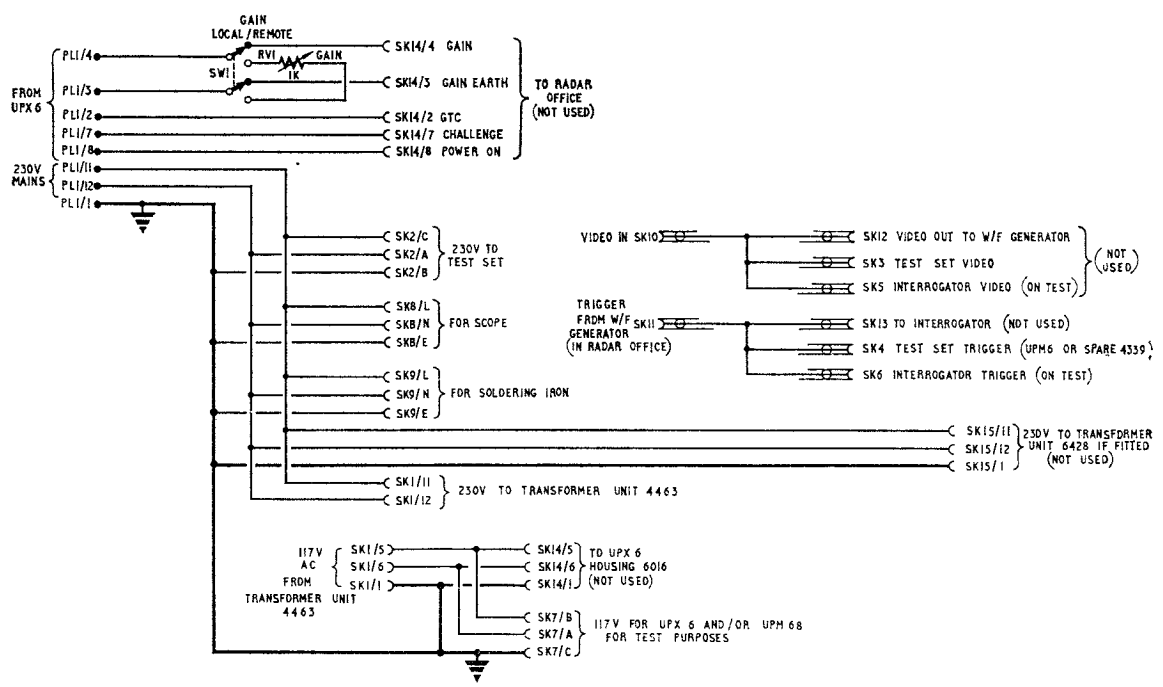

Fig. 2. Junction box 6017: circuit

14. The spare waveform generator is removed from the top of the rack, inserted in position 4 or 6 in place of the stowage panel and connected up with a switch unit 4821 interposed between PL1 and the control rack lead. If a spare control unit 4227 is available it should be fitted in place of stowage panel 6809 immediately above the waveform generator. Alternatively, it is necessary to patch the rack trigger lead to SK7 on the waveform generator. The rack trigger inputs must be connected in parallel as shown in Part 1, Sect. 2, Chap. 1, fig. 5 (b).

15. The cable coiled at the foot of the rack should be connected directly to the trigger out socket at the rack base. Power supplies for the waveform generator are obtained by setting the appropriate switch (PU1 or PU2) on panel (metering) 4466 to REMOVE, thus bringing the standby power unit 4465 into service. It should be noted that with either of the PU switches in the REMOVE position the automatic changeover circuit relay on the metering panel is energized so that the changeover facility ceases to be available for the operational waveform generator. In consequence, care must be taken to return the switch to the NORMAL position when the trigger is no longer required at the test bench.

16. At two-head stations there will be two operational waveform generators so that it is not practicable to employ the spare unit in the manner described. In such installations it will first be necessary to decide which of the two waveform generators can be spared from operational service when the test bench trigger is required. The cable normally stowed at the rack base should then be connected directly to SK7 on this waveform generator and a switch unit 4821 inserted in circuit. Since the waveform generator is already supplied by one of the power units 4465 in the rack, no other action is necessary. ▶

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Chapter 4.—TEST SET (DECODER) 4678

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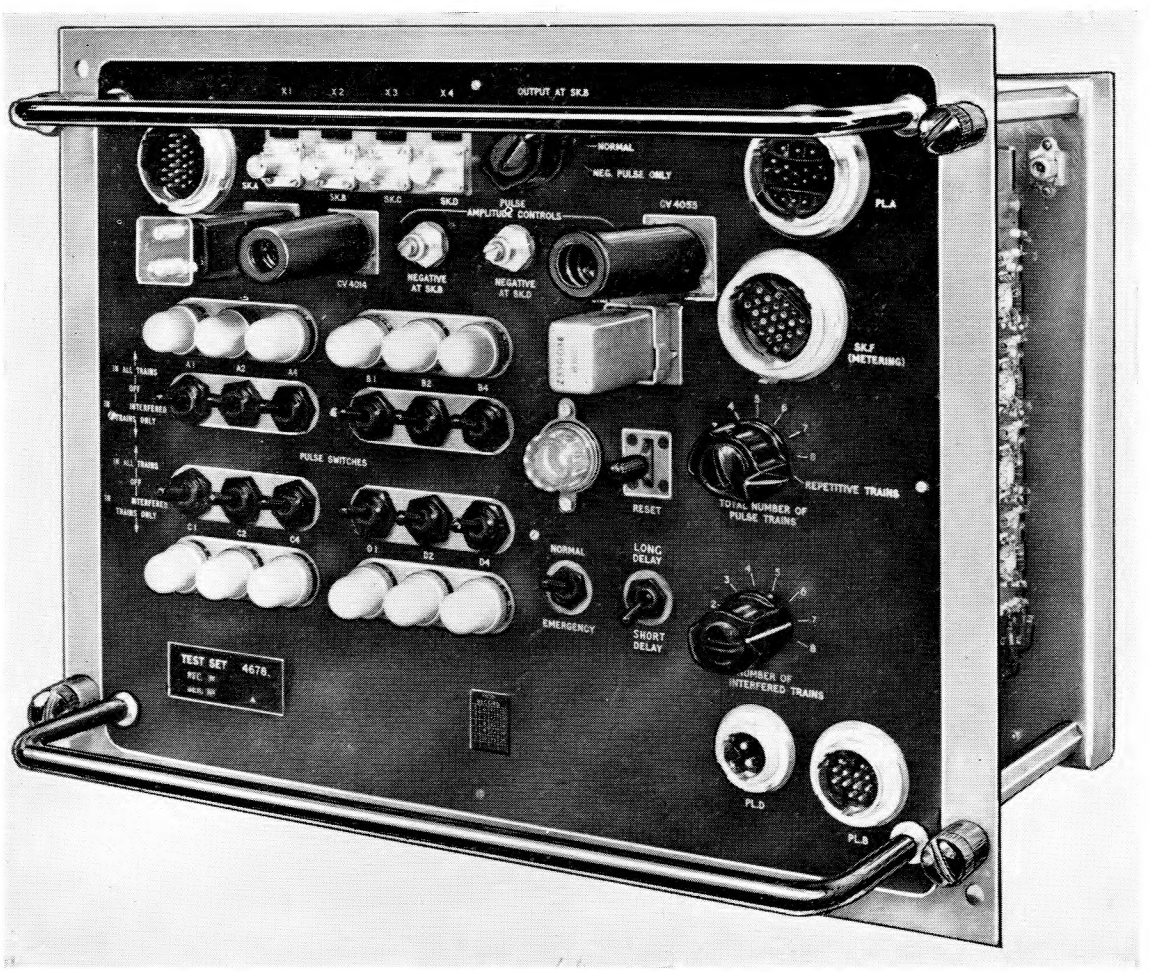

Fig. 1. Test set (decoder) 4678 : front panel

Introduction

1. Test set (decoder) 4678 is a built-in item of SIF test equipment designed for testing the various decoding units and sub-assemblies in situ. One test set is installed in each rack (mode 1 decoder) 12276 in the radar office and in rack (decoder RH) 12807 fitted to the RVT 511 in mobile installations. Provision is made through the wiring of the decoder racks for any decoding unit to be easily and rapidly coupled to the test set for checking.

2. The test set is capable of producing all the video inputs which may be applied to a decoder and generates positive pulses, negative pulses and pulse trains which may consist of positive pulses, negative pulses or a mixture of positive and negative pulses.

3. Test set 4678 provides the following facilities:-

(1) SIF code pulse trains, each train consisting of two bracket pulses 20·3 μs apart and up to 12 code pulses spaced at intervals of 1·45 μs. Each code pulse position is independently controlled and the pulse can be injected or omitted as required. The pulse trains may be generated continuously at the station p.r.f. or may be triggered once per recurrence period up to a maximum of eight periods. Interference can be simulated by injecting a particular code pulse into only a proportion of the pulse trains. Groups of four pulse trains may be generated to simulate an emergency response.

(2) A three-position switch controlling one of the outputs allows the pulse trains of (1) to be mixed with or replaced by a single negative pulse (or four negative pulses for an emergency response).

(3) A separate output of the negative pulses referred to in (2).

(4) Positive-going square pulses forming a range strobe for an active decoder.

(5) Indicator lamps for displaying the output from an active decoder.

All pulses are delayed behind the synchronizing pulse. Two delay ranges are provided; one short (of the order of 4 μs) and the other long (of the order of 500 μs).

General description

4. The test set (*fig.* 1 *and* 2) consists of a rack panel at the rear of which is a frame supported on stand-off pillars. All the controls and plugs and sockets as well as the output valves are mounted on the panel. The sub-assemblies which form the

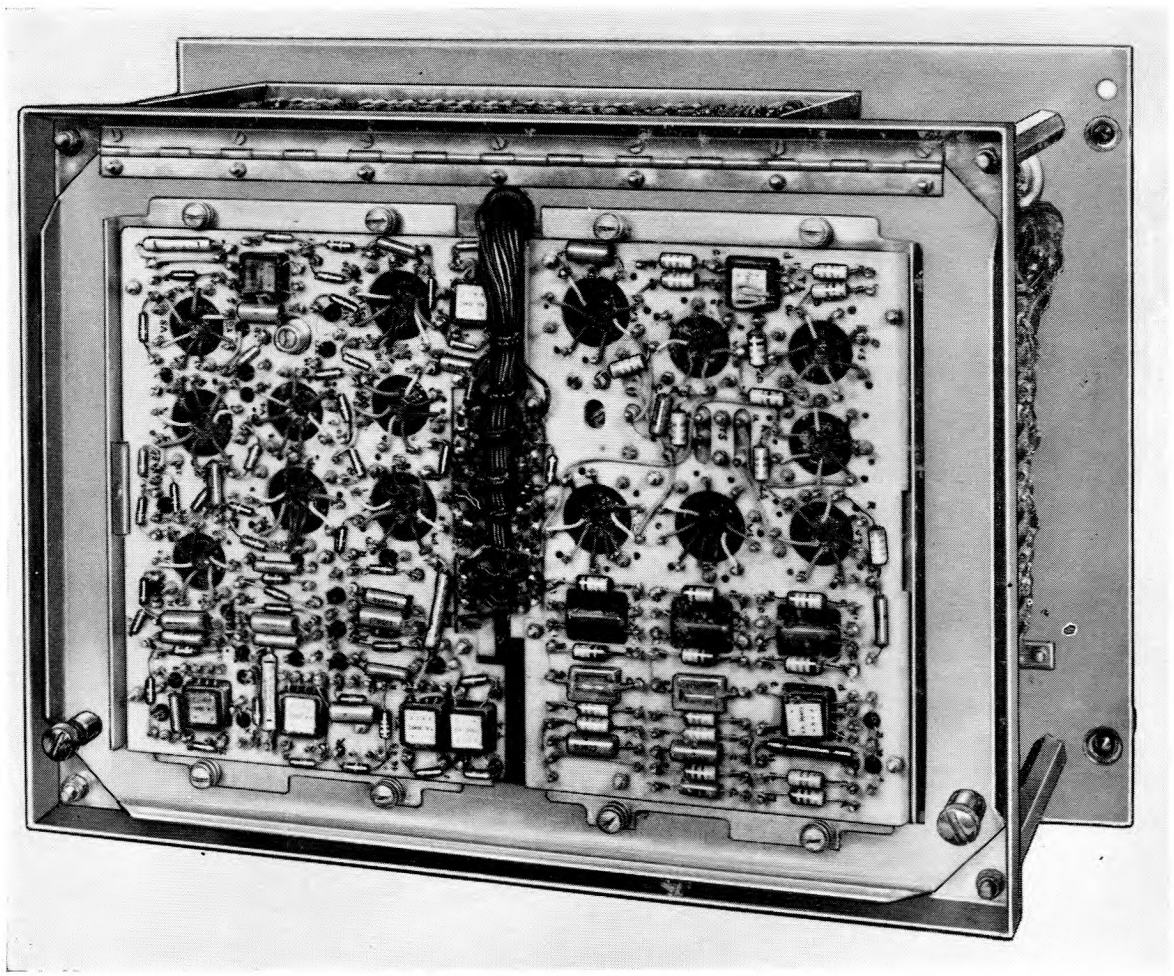

Fig. 2. Test set (decoder) 4678 : rear view

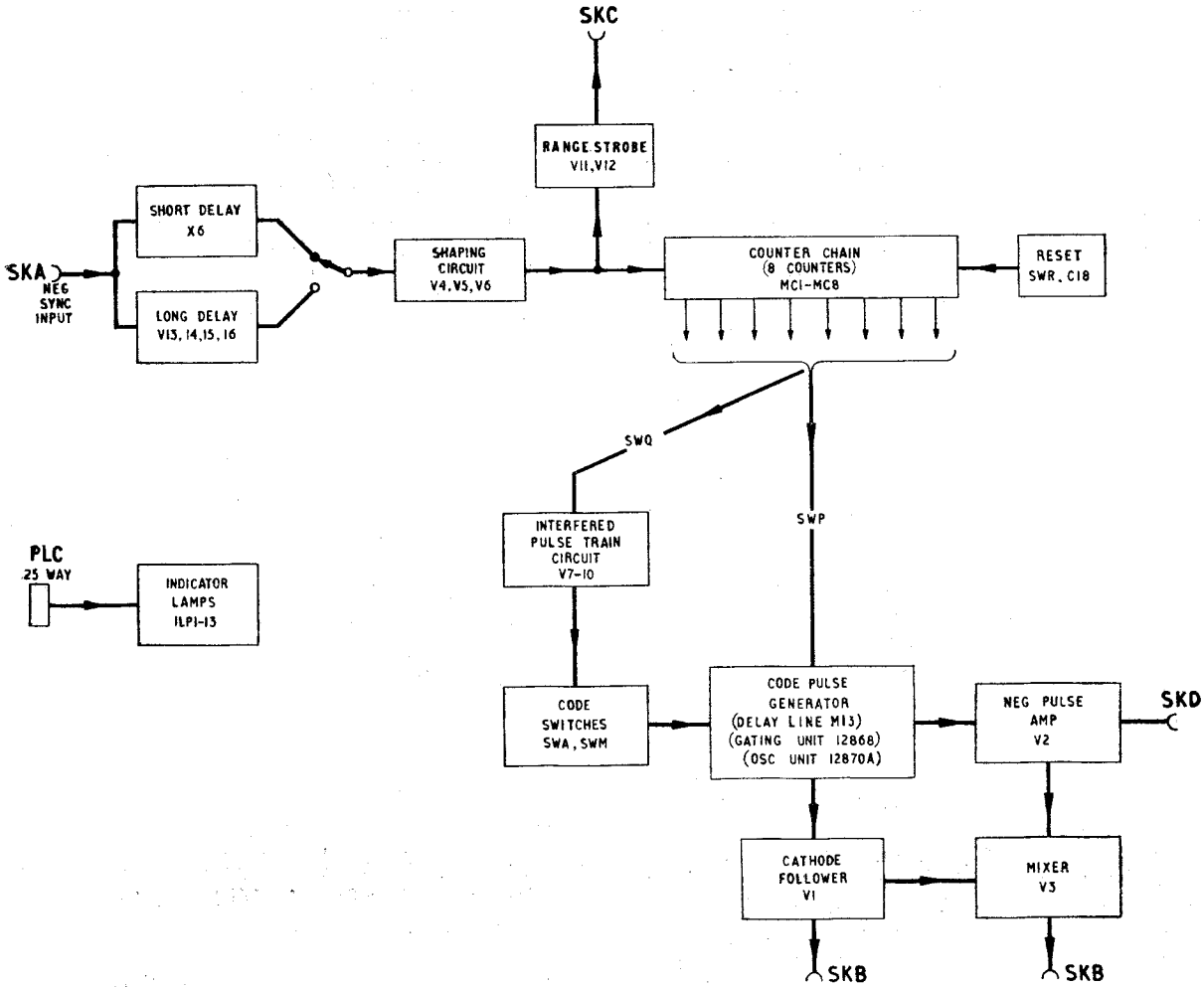

Fig. 3. Block diagram

test set are supported between the panel and rear frame and on the frame itself.

5. The two sub-units which are mounted at the rear of the test set are secured to a sub-frame which is hinged to the rear frame and retained in position by captive screws. By releasing these screws the sub-frame can be raised to give access to the interior. Handles are provided at the top and bottom of the front panel to facilitate installation, removal and servicing.

6. No power unit is incorporated in the test set which draws its supplies from power units 6889 and 12123 fitted to the rack in which it is installed.

7. A block diagram of test set 4678 is given in fig. 3. Operation is initiated by the synchronizing pulse, normally derived from the master trigger unit, applied to the inputs of the delay circuits, the desired output being selected by the delay switch. The delays are purely nominal and two ranges are provided to meet alternative viewing requirements. In general, when using an oscilloscope to monitor the output, the short delay will be used, but a long delay is preferable when observing the signals on a PPI.

8. The delayed signal is passed to a shaping circuit the output from which is applied to a flip-flop and also to a counter circuit. When triggered, the flip-flop produces a 50 μs pulse which serves as a range strobe when testing an active decoder.

9. The counter chain consists of eight stages very similar to the counters in decoder sub-assembly (active) 4676, described in Sect. 5, Chap. 2. It is triggered by the pulse from the shaping circuit so that, following each synchronizing pulse, the counter shifts one step, allowing any number of pulses up to eight to be counted. An output is taken from each stage in the counter and fed, via a selector switch, to a code pulse generator. Provision is made to operate the counter in either

of two ways. With the appropriate control set to REPETITIVE TRAINS, the last stage cycles continuously, providing an output pulse for every sync pulse. By setting the switch to the desired numerical value, the counter generates that number of pulses and is then inoperative until the RESET switch is depressed.

10. The code pulse generator consists of three sub-assemblies of coding unit 6466 and its function is to generate normal or emergency pulse trains, depending upon the setting of the NORMAL/EMERGENCY switch. The code pulses are derived from tappings on a delay line and their presence (or otherwise) in the code train is controlled by the code switches.

11. Two outputs are taken from the code pulse generator. The positive pulse trains are fed to a cathode follower and thence, via the output switch, to a coaxial socket SKB. With the switch in position 1, positive pulse trains only appear at SKB.

12. The second output is the final pulse from the delay line in the code pulse generator. This is a re-trigger pulse occurring approximately 3 μs after the second bracket pulse of the train. It is a positive-going pulse which is inverted in a negative pulse amplifier to give, at SKD, a negative pulse output.

13. The output from the negative pulse amplifier is also fed to a mixer stage where, with the output switch in the NORMAL position, it is mixed with the output from the pulse train cathode follower. The resultant output at SKB then consists of positive pulse trains, each followed after 3 μs by a negative-going pulse. The third position of the output switch allows the negative pulse only to be taken from SKB.

14. Interference is simulated through the NUMBER OF INTERFERED TRAINS switch which allows the output pulses from the counter chain to be applied to an interfered train circuit consisting of a flip-flop controlling a relay. The relay contacts are normally made so that by setting any one of the code switches to the IN INTERFERED TRAINS ONLY position that pulse is included in the train. The relay can be energised, through operation of the selector switch, by any of the counter pulses up to the seventh and will hold in for at least eight recurrence periods. Thus, an additional, or interference, pulse can be introduced into the first one or more of the pulse trains generated.

CIRCUIT DESCRIPTION

General

15. A circuit diagram of test set (decoder) 4678 is given in fig. 4. The three sub-assemblies of coding unit 6466 incorporated in the test set are oscillator unit 12870, delay unit 12867 and gating unit 12868. The first two sub-units are modified so that, when employed in the test set, they become oscillator unit 12870A and delay line M13. However, the changes are small and do not affect the circuit operation in any way. In particular, delay line M13 differs from the original delay unit 12867 only in the addition of a tag board on which all the input and output leads are accommodated and the fact that some connections are not used in the test set application. The circuits of the interconnected delay lines are identical.

16. Circuit diagrams of the sub-assemblies are given in fig. 5, 6 and 7. Coding unit 6466 has already been described elsewhere and the information contained in this chapter is only sufficient to explain the operation of the test set. For a detailed circuit description of the coding unit reference should be made to A.P.2887N, Vol. 1, Part 1, Chap. 12.

Input and delay circuits

17. The test set requires a negative-going synchronizing pulse of $10V \pm 5V$ in amplitude and approximately 4 μs in length at a p.r.f. of about 250 c/s. This pulse is fed in at SKA and thence to the two delay circuits, the desired output being selected by SWS.

18. The short delay is obtained by feeding the sync pulse through a nominal 4 μs delay line terminated by R50. The output end of the line is connected to one of the fixed contacts on the delay switch SWS.

19. The long delay is derived from a flip-flop circuit consisting of the transistors V13 and V14. Initially, V13 is cut off since its base is returned to the +10V line through R34 and V14 is just bottomed, the base current through R35 being slightly less than 0·5mA. V14 collector, and hence the anode of MR23, is at about earth potential.

20. With the arrival of a negative-going sync pulse, MR23 conducts and since its impedance (in the conducting state) is considerably higher than that of the transistor, most of the pulse voltage is developed across the diode. However, sufficient potential is produced across V14 to cause (through R36 and R34) V13 base to move negative from its initial potential of approximately +1·5V. Thus, collector current begins to flow in V13, the collector voltage rises, causing V14 base to be cut off, and the action is cumulative until V13 is fully conducting and V14 is completely cut off.

21. The positive waveform transmitted from the collector of V13 through C15 to the base of V14 commences to decay due to the negative leak through R35 until eventually a state of zero bias is reached and collector current starts to flow again in V14. The resultant rise in voltage at the junction of R34, R36 continues until V13 is cut off again, approximately 500 μs after the application of the triggering pulse.

22. A pulse suitable for triggering the subsequent circuit is derived from the back edge of the delay waveform by applying it to another flip-flop circuit of shorter time-constant formed by the transistors V15 and V16. Initially, V15 is cut off and V16 is bottomed, a base current of slightly more than 0·5mA flowing through R40.

23. R38 forms the common collector load of V14 and V15. In the un-triggered condition, V14 collector current (about 6mA) flows through R38 so that both collectors are near earth potential. When the first flip-flop is triggered, V14 is cut off, collector current ceases to flow and the only current through R38 is that required to hold V13 in the conducting state, i.e. the current through R34, R36 and MR5. As a result, the collectors of both V14 and V15 rest at about −8·5V.

24. At the end of the recovery period of the first flip-flop, V14 collector current again flows through R38 and the potential at the junction of the resistor with V15 collector rises towards earth, producing a positive edge of about 8·5V in amplitude. This edge is transmitted through the capacitor C17 to the base of V16 and triggers the second flip-flop. The recovery time-constant of this circuit is approximately one-thirtieth of that of the delay circuit so that V16 collector waveform is a negative pulse almost 10V in amplitude and of the order of 20 μs in length.

Shaping circuit

25. The pulses from the two delay circuits, although approximately of the same amplitude, differ considerably in length and are consequently passed to a shaping circuit which converts them to pulses of constant amplitude and length suitable for triggering the counter stages.

26. The shaping circuit consists of three transistors V6, V5 and V4. Normally, V6 is cut off by the +0·5V bias applied to the base through R48 and the input pulse, which may be derived from either the delay line or the flip-flop circuit depending upon the setting of SWS, is fed to V6 base through C13 and R49. R49 is included to limit the drive to V6 and, in parallel with R50, provides a termination to the delay line of 750 ohms which approximately matches the characteristic impedance of the line so that reflections are negligible.

27. The negative-going pulse applied to V6 base turns on a collector current of about 1mA and the collector rises to earth potential, producing a positive 10V pulse across R47. This pulse is fed via a differentiating circuit (C11 and R45) to V5 base. V5 emitter is taken to +10V and the collector, through R44, to earth. The base is returned to −10V via R45 and R46, a current of just under 2mA flowing through these resistors. V5 is fully conducting, the current through R44 being of the order of 30mA and the collector is only a fraction of a volt negative with respect to the emitter.

28. For effective triggering of the counter stages a current pulse of approximately 200mA is required and this current has to be turned on by V4. Under these conditions the gain of the transistor is unlikely to exceed 10 so that the base drive has to be of the order of 20mA. The positive-going edge of the differentiated pulse, applied to V5 base, drives the transistor towards cut-off so that the collector potential starts to fall, this negative wavefront being fed through C10 to the base of V4 and overcoming the 4V positive bias. As soon as V4 base commences to take current, the fall of V5 collector is arrested and the remaining current flowing through R44 (nearly 20mA) is diverted through C10 to provide the required drive to V4 base. Thus, for each input pulse, a 200mA pulse of current, lasting for approximately 1 μs, is passed through the trigger winding on MC1 to MC8.

Counter circuit

29. The counter circuit is similar to those employed in the active decoder and consists of a chain of eight memcores 12443 with their associated transistors V17 to V24. Initially, the first stage core (MC1) is set to the "1" state and all the other cores to "0". When a pulse from the shaping circuit is passed through the trigger windings, the first core is switched to "0" and regeneration occurs as described in Sect. 5, Chap. 2. As a result, a pulse is produced at V17 collector. The second memcore is switched to the "1" state ready for the next triggering pulse.

30. Successive triggering pulses switch each stage in turn until the eighth pulse arrives and this pulse switches MC8 back to the "0" state. All the cores are then in the "0" state and further triggering pulses can produce no effect. For another eight pulses to be counted the counter must be reset and this is achieved by operation of SWR. Through SWR, C18 is connected in parallel with all the reset windings which are in series, the junction remote from the switch being taken to −10V. When SWR is depressed, one terminal of C18 is disconnected from the memcore windings and taken through R81 to earth so that the capacitor charges. On releasing the switch, C18 is again connected to the reset windings of the memcores and discharges through them, causing MC1 to be switched to the "1" state and ensuring that all the other cores are at "0". It should be noted that one of the contacts on SWR is coupled to PLC/S which is connected to earth when the switch is depressed. This line provides a reset facility for an active decoder under test.

31. The output pulse from each stage in the counter, produced as the result of regeneration, is used to trigger the code pulse generator and is routed through an isolating diode and a selector switch SWP (TOTAL NUMBER OF PULSE TRAINS). SWP is a 9-position wafer switch with shorting rotors on two wafers, b and d. Thus, in the fully counter-clockwise position, the cathode of MR6 only is connected to C19; in position 2 the cathodes of MR6 and MR8 are connected and so on until in position 8 all the counter pulses are fed to the generator through C19.

32. In the ninth position of SWP (REPETITIVE TRAINS) the connection between MC7 and MC8 is broken through wafer f and the end of the winding

on MC8 is taken to earth. Since the other end of the winding is connected through R88 to −10V, a d.c. bias is applied and this is sufficient to hold MC8 in the "1" state. ◀To ensure regeneration, the current in the trigger windings is increased by returning the 10 turn windings to −10V via the 47 ohm resistor R83 instead of the 100 ohm resistor R81 (via SWPh).▶ Thus, each trigger pulse switches MC8 to "0" and, when the regenerative cycle is completed, the d.c. bias restores it to the "1" state. In this way an output is obtained from V24 for each sync. pulse. The other cores are all in the "0" state and can produce no output pulses.

Code pulse generator

33. The output pulses from the counter stages, taken from the rotors of SWP/b and d, are fed via C19 and the NORMAL/EMERGENCY switch to the code pulse generator which consists of delay line M13, oscillator unit 12870A and gating unit 12868. In their original form these sub-assemblies are part of coding unit 6466 and the following brief description is included to explain the operation of the test set. Detailed circuit descriptions are given in the relevant publication (*para.* 16) and are still applicable since, as explained in para. 15, the modifications introduced for the test set use do not affect the circuits.

34. With SWN in the NORMAL position, the trigger pulses are applied to the mode 2 trigger input. Considering the operation for one pulse train only, the pulse from the counter stage is fed to T2 (*fig.* 7) to trigger the gating flip-flop. It also triggers the first blocking oscillator (*fig.* 5). The pulse produced by the blocking oscillator is fed to the delay line and the resultant sequence of pulses from the delay line taps, determined by the settings of the code selector switches (SWA to SWM), is passed to the mode gate. During its transmission through the delay line the pulse is attentuated and is consequently regenerated by a second blocking oscillator (*V*2, *fig.* 5).

35. The purpose of the mode flip-flop is to produce a gating square wave which just encompasses a complete pulse train. This square wave is fed to the gate valve (*V*4, *fig.* 7) and the output from that stage is taken to the timing gate (*V*5, *fig.* 5). The modes 1 and 3 flip-flops are not triggered so that the associated gate valves remain cut off and the only gating waveform applied to the timing gate is that from the mode 2 gate.

36. In addition to feeding the delay line, the pulse from the first blocking oscillator triggers a 690 kc/s oscillator (*V3A and V*4, *fig.* 5) which delivers timing pulses spaced at intervals of 1·45 μs. These are also fed to the timing gate. Provided a timing pulse and a pulse from the delay line coincide, an output will be obtained from the gate and an accurately timed pulse is then passed to the output blocking oscillator.

37. The bracket pulses, which are taken from tappings on DL1 and DL8, are fed through isolating diodes to the gating circuits on all three modes. The code pulse tappings are connected through biased diodes whose operation is controlled by the PULSE SWITCHES. With all these switches in the OFF position, the output train consists of only the two bracket pulses spaced 20·3 μs apart. By moving any of the switches to the IN ALL TRAINS or IN INTERFERED TRAINS ONLY setting, the bias is removed from the associated diode and that particular code pulse will appear in the train.

38. When SWN is set to EMERGENCY, the counter output is fed to the mode 1 trigger input of the code pulse generator. The operation of the circuits is substantially the same but the mode flip-flop now generates a gating waveform long enough to embrace four pulse trains. In addition, the input pulses are also applied to a re-trigger flip-flop (*V*7, *fig.* 7) whose output consists of a pedestal on which are superimposed re-trigger gating pulses derived from an additional section of the delay line (*DL*9). The combined waveform is applied to a re-trigger gating valve (*V*8) which is supplied with h.t. only when SWN is set to EMERGENCY. A 690 kc/s timing pulse, which coincides with a re-trigger gate pulse, is passed to the first blocking oscillator, provided the pedestal is also present.

39. With the application of the re-trigger pulse to the first blocking oscillator, the valve initiates a second train of pulses and a total of four mode 1 trains is generated before the re-trigger gate is closed by the termination of the re-trigger flip-flop waveform.

40. The pulses derived from DL9 in delay line M13 also form a convenient source of negative-going output pulses for the test set.

41. The output blocking oscillator of the code pulse generator is a delay line-controlled stage (*V*6, *fig.* 5) which determines the duration of the output pulses (0·35 to 0·55 μs). These pulses are then amplified by a pulse amplifier (*V*7) and extracted via the final output terminal (tag 67) on delay line M13.

Output stages

42. Two output stages are provided in the test set; a cathode follower for the pulse trains and a pulse amplifier for the negative pulses. The positive pulse trains are developed across a potentiometer RV1 serving as an amplitude control. RV1 slider is connected, via C5, to V1 grid which is returned, through R56, to a negative potential at the junction of R55, R57. V1 cathode is connected to contacts on the output switch SWT. When SWT is set to POS. PULSE TRAINS ONLY, V1 cathode is coupled directly to SKB and the output at this socket will consist of positive pulse trains, the pulse amplitude being preset, by adjustment of RV1, to a level of +16V into 68 ohms.

43. Positive-going pulses, taken from the "final pulse from line" terminal on gating unit 12868, are developed across a potentiometer RV2 which forms the amplitude control. RV2 slider is connected, via C8, to V2 grid which is returned through R54 to approximately −4V at the junction of R52, R53. The anode load of V2 is the primary

winding of a pulse transformer TR1. TR1 has two secondary windings, one of which is coupled to SKD. The positive-going input is inverted in this stage so that the output at SKD consists of negative-going pulses, preset by adjustment of RV2 to a level of −16V (unterminated).

44. The output from the other secondary on TR1 is developed across the potentiometer chain R60, R61 and fed to the base of a transistor V3 connected as an emitter follower. One end of TR1 secondary is taken to +10V. MR22 limits the excursion at V3 base to earth.

45. V3 emitter is returned, via resistor R62, to the slider of a potentiometer RV3 connected between +4V and earth. Thus, the static bias between the base and emitter of V3 can be varied from +6V to +10V by means of RV3 and this control is preset to give an output level of −3V into 68 ohms at SKB when SWT is set to NEG. PULSE ONLY.

46. With SWT in the NORMAL position, the output from V1 cathode is fed via the diode MR1 to V3 emitter and thence to SKB through C9. The output at SKB then consists of positive pulse trains with a nominal amplitude of 13V, each followed, after approximately 3 μs, by a negative-going pulse having a nominal amplitude of 5V.

Interfered pulse train circuit

47. Mutual interference between pulse trains is simulated by a facility which allows an additional pulse to be injected into a proportion of the pulse trains. The circuit consists of a relay controlled by a transistorized flip-flop whose input is derived from the counter stages.

48. In addition to supplying the input to the code pulse generator, each stage in the counter chain delivers a second output through an isolating diode to the NUMBER OF INTERFERED TRAINS switch SWQ, the rotor of which is coupled, via diode MR3, to the collector of V10. SWQ is an 8-position selector switch so that the pulse from any one of the first seven stages in the counter can be fed to V10.

49. V9 and V10 form a normal flip-flop in which V9 is conducting and V10 is cut off. A positive-going pulse from the counter circuit, applied to the anode of MR3, initiates the flip-flop action which results in V9 being cut off and V10 conducting. The consequent fall in voltage at the junction of R70, R71 switches on V8 which is an emitter follower. The final stage in the circuit is V7 whose collector load is the coil of a relay RLA. When V8 conducts it switches on V7 and the relay is energized. The diode MR21 is included to limit the inverse peak voltage at V7 collector, due to the inductive load, when the transistor is switched off.

50. The normally closed contacts of RLA are connected in series with the common lead joining the interfered trains contacts of the code pulse switches and earth. Thus, while RLA is de-energized, the action of moving any of the code switches to the IN INTERFERED TRAINS ONLY position causes that particular code pulse to appear in the output trains. The operation of switching on V7 by the application of any of the counter pulses to the flip-flop energizes RLA and the contacts break so that the pulse is no longer included in the code train. The inclusion of the interference pulse in only the number of trains selected by SWQ is achieved by making the recovery time-constant of the flip-flop sufficiently long to ensure that RLA remains energized for longer than 32ms, i.e. more than eight recurrence periods ◀after the passage of the pulse selected by SWQ.▶

51. It should be noted that it is impracticable to set more than one of the code pulse switches to the IN INTERFERED TRAINS ONLY position at a time. The action of the circuit is equivalent to changing the code between successive recurrence periods and the code pulse generator is not designed to operate under such conditions. In its normal application it is intended for use with a fixed code. Large capacitances are associated with the diode gates which are controlled by the code selection switches. If several of them are connected in parallel the resultant total capacitance, together with the finite operating time of the relay, will prevent the pulse generating circuits setting down before the next recurrence period occurs.

Range strobe

52. When testing an active decoder one of the waveforms which must be available to open the main input gate is a range strobe and a suitable pulse for this purpose is provided by the test set. The source is the output pulse from the shaping circuit, applied to a flip-flop V11 and V12.

53. V11 is normally cut off and V10 is conducting. The positive-going 1 μs pulse from the shaping circuit initiates the flip-flop action and the output, taken from V11 collector, consists of a positive-going square pulse, approximately 10V in amplitude and 50 μs in duration. This pulse is brought out on SKC.

Indicator lamps

54. Provision is made for displaying the output of an active decoder through lamps on the front panel of the test set. There are thirteen lamps in all, one for each code pulse and one for the query output. Each code pulse lamp is situated adjacent to the corresponding code pulse switch. A connection to one terminal of each lamp is brought in from the active decoder on pins of PLC. The other terminal of the lamp is taken to a common lead terminated at PLD/B which is connected to the 12V supply in power unit (A.D. indicator) 12123.

Power supplies

55. The test set derives all its power supplies, with the exception of that for the indicator lamps, from a power unit 6889. Heater voltages, h.t. and the transistor supplies are fed in on PLA and PLB. The various voltages required by the transistor circuits are obtained from the potential divider network in the power unit. Those for the code pulse generator are supplied by a potential divider network within the test set.

56. It should be noted that the test set requires a different bias level from that in the passive decoder and that when a power unit 6889 is used in conjunction with a test set 4678 the preset bias control on the power unit (ADJUST – 35V (B)) must be reset to give an output of – 50V. This is done by coupling multimeter 12124 to the metering socket on the power unit and adjusting the preset until the meter indicates half-scale deflection.

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CORRIGENDA LEAFLET NO. 1/69

In Fig. 4 Test set (decoder) 4678: circuit, resistor R 95 below the earth rail in the bleeder network has been changed from 2·2k to 3·3k.

Note . . .

The information contained in this leaflet will be incorporated by normal amendment list action in due course.

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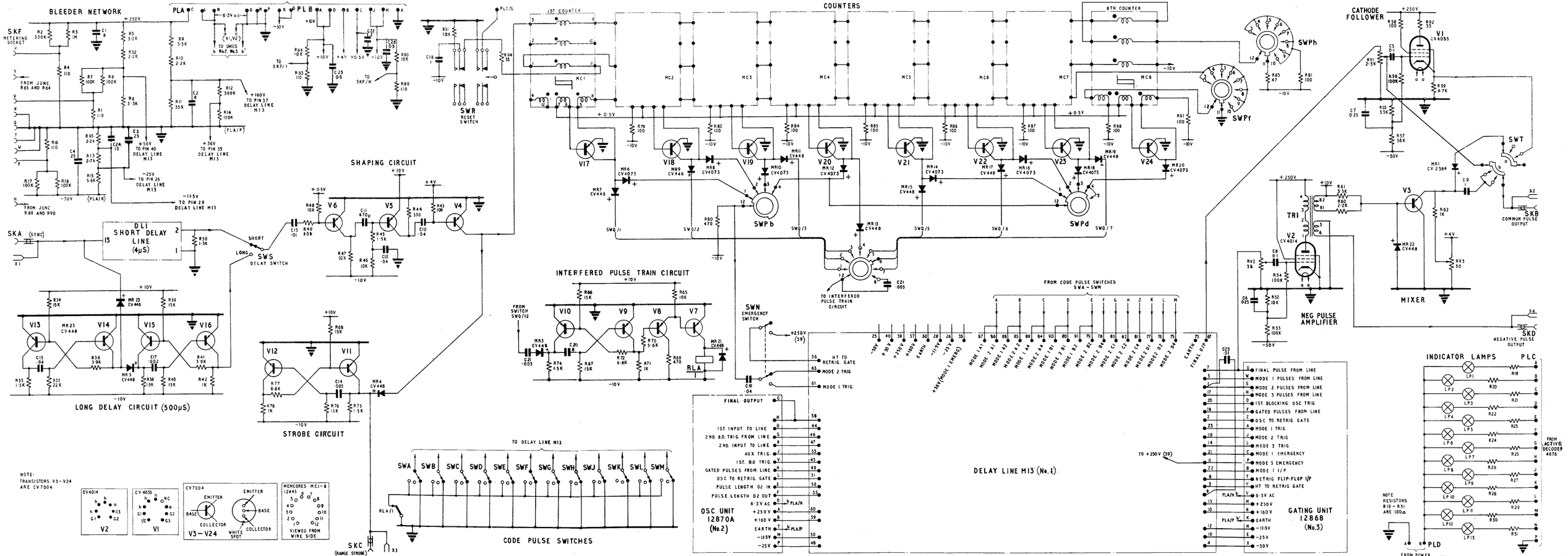

Fig. 4

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Test. set (decoder) 4678: circuit

Fig. 4

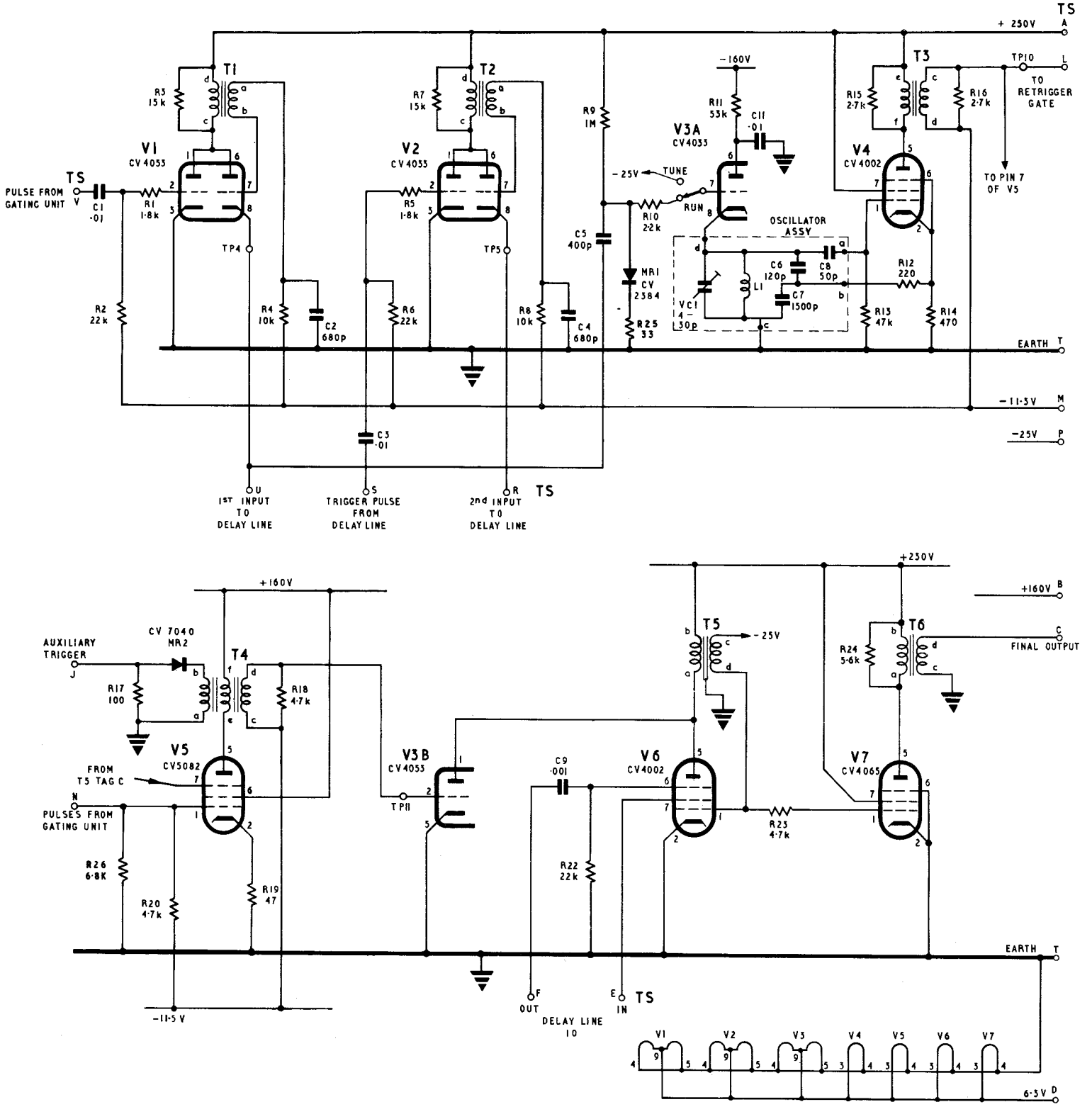

Fig. 5 Oscillator unit 12870A: circuit Fig. 5

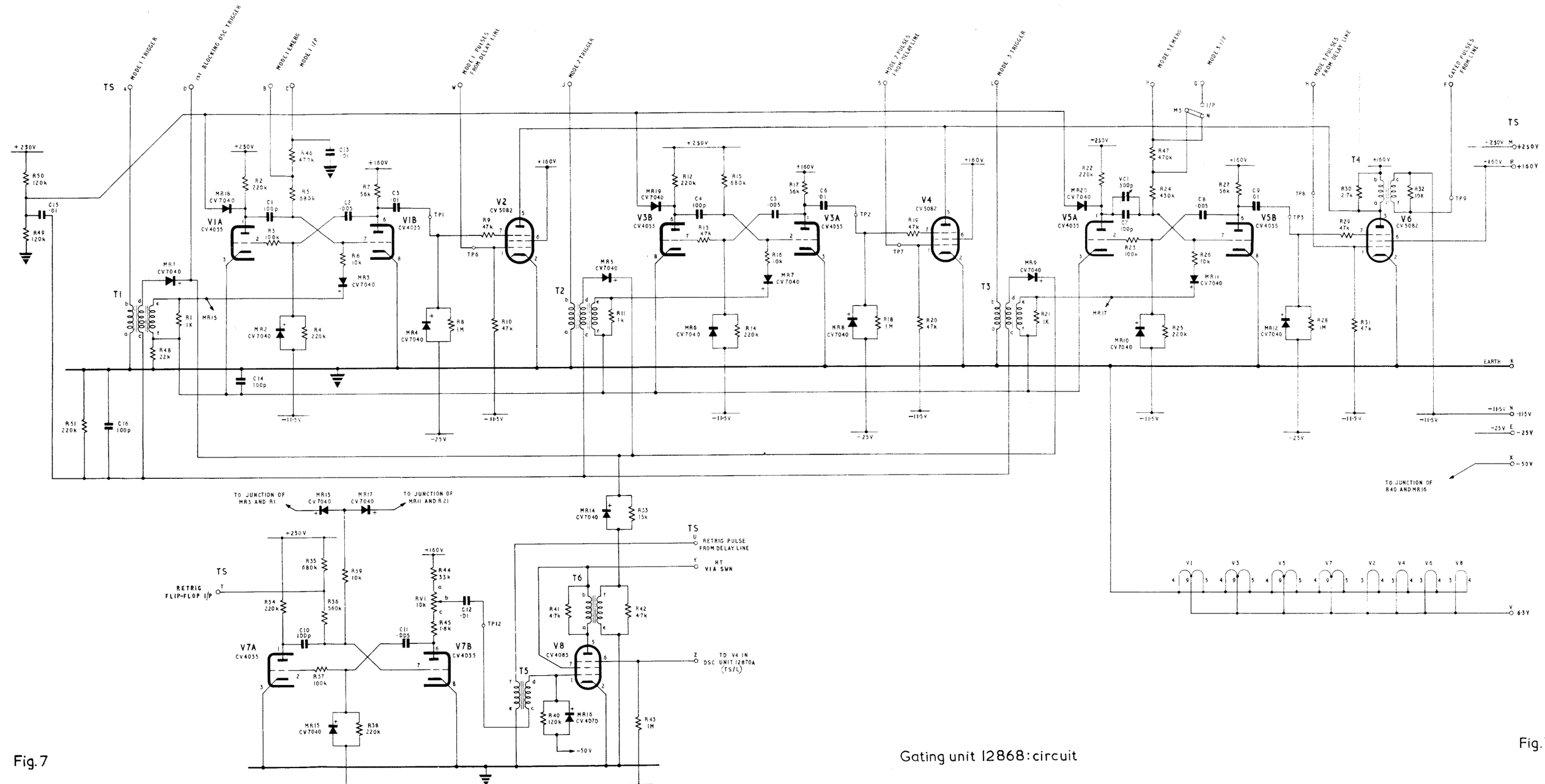

Fig. 7

Gating unit 12868: circuit

Fig. 7

Chapter 5

TEST SET, ELECTRONIC CIRCUITS

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Introduction

1. Test set, electronic circuits (JS 6625-99-580-1640) is a self-contained portable unit designed for fault-finding and testing the individual printed wiring boards in decoder sub-assembly (active) 4676. For these purposes a variety of pulses is generated to operate and reset the memcore counting chains, gating and Eccles-Jordan circuits. The boards, when withdrawn from the decoder, plug into sockets on the front panel and draw their power requirements from the test set.

2. A qualitative test can be applied to CV7004 transistors. The memcore assemblies mounted on matrix decoder 6886 may be tested in situ. An additional facility is a 345 kc/s crystal-controlled output provided for setting up the oscillator in test set 4678.

General description

3. The test set (fig. 1) consists of a panel and chassis housed in a steel case with overall dimensions of $17\frac{1}{4}$ in. × $10\frac{3}{4}$ in. × 9 in. It weighs $43\frac{1}{2}$ lb. A stowage compartment is provided at the left-hand side of the case for three boards, jumper 16375, 16376 and 16377. It should be noted that although the test set has this stowage provision, the boards are not supplied with the unit and must be demanded separately. Stowage for the mains input connector is afforded by clips and a dummy 3-pole socket on the right-hand end of the case.

Fig. 1. Test set, electronic circuits: general view

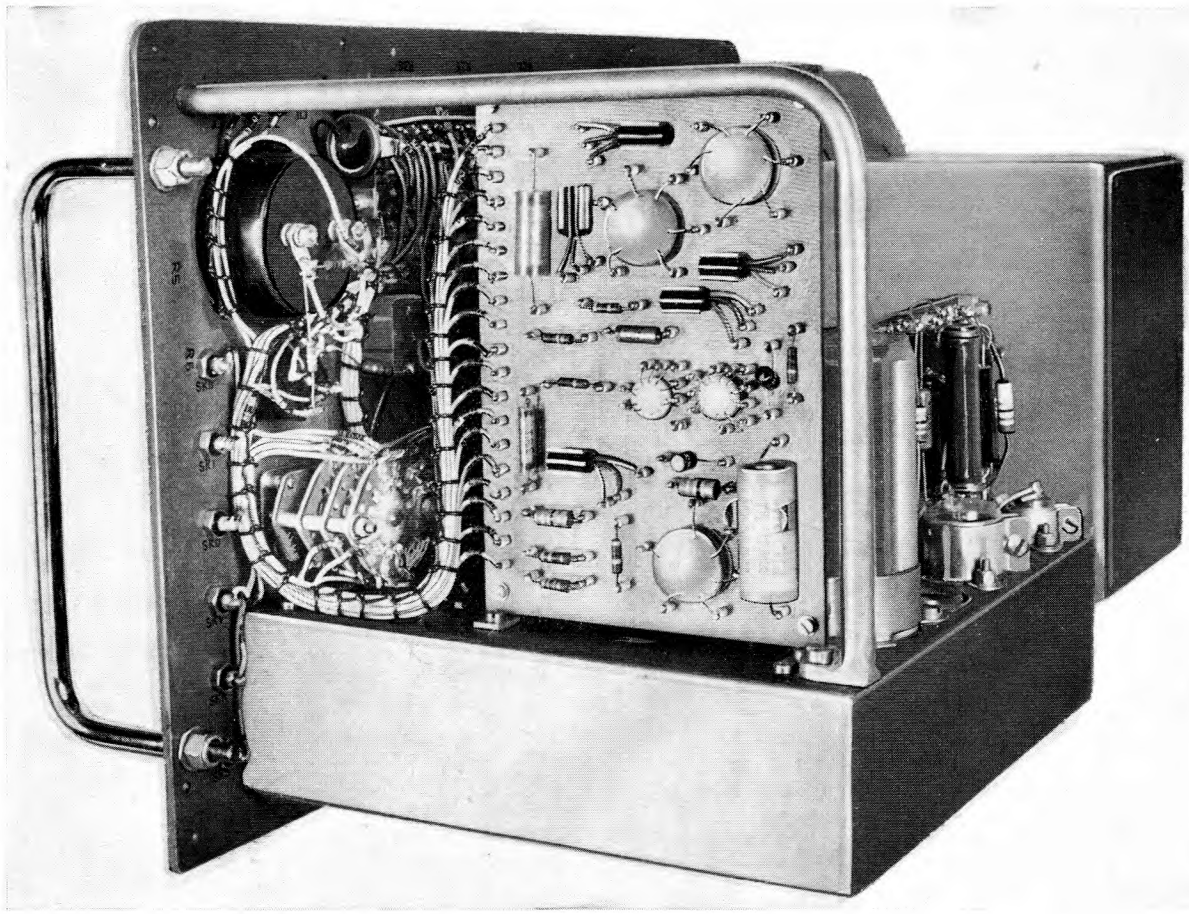

Fig. 2. Test set, electronic circuits: interior view

4. The panel carries the meter, sockets for the printed wiring boards and all the necessary test selector switches and manual controls. The remaining components, with the exception of the pulse generating and counting circuits, are located on the chassis (fig. 2). That part of the circuit, shown within chain-dotted lines in fig. 7, is mounted on a printed wiring board supported vertically at one end of the chassis.

5. The three groups of sockets located at the top of the panel are designated 6885, 6886 and 6887, corresponding to the nomenclature of the printed wiring boards in the active decoder. A board from a decoder under test is inserted into the appropriate sockets and, by operation of the selector switches on the test set, is supplied with pulses simulating the normal inputs. With an oscilloscope connected to the required points on the board in turn, the performance of the circuit can be readily ascertained or a fault located.

6. A simplified block diagram of the test set is given in fig. 3. Testing of CV7004 transistors is done through the standard transistor and memcore which form the first stage of the divide-by-two counter in the test set. The test set meter is connected in such a manner that it reads the mean value of the pulses of current from the stage so that, for fixed values of p.r.f. and peak current (nominally 100 mA), the reading is proportional to pulse duration and the meter may be calibrated in micro-seconds. Thus, each test set bears, at the side of the meter, a tablet on which is engraved the standard setting (in microseconds) for that particular unit. Since an external transistor replaces the internal one it can be checked against this standard reading.

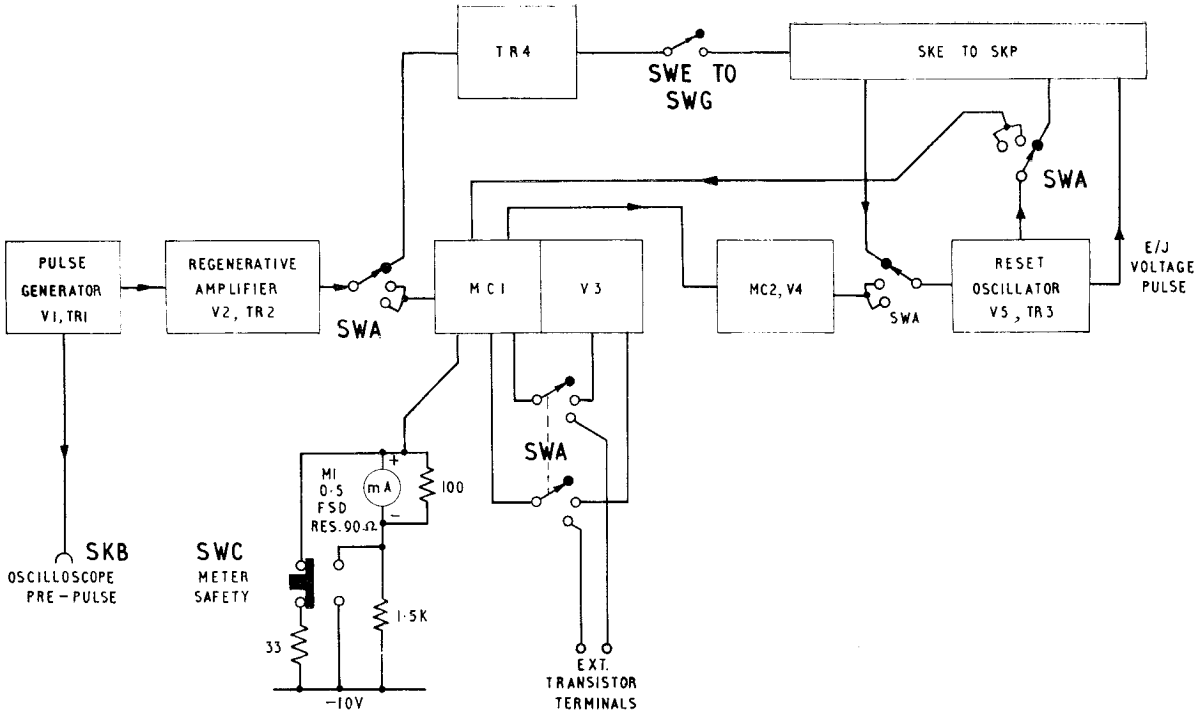

Fig. 3. Block diagram

CIRCUIT DESCRIPTION

Pulse generators (fig. 7)

7. Transistor V1 and pulse transformer TR1 form a blocking oscillator which generates a positive-going pulse approximately 5μs long. The base of V1 is returned to the -10V line through R1 and RV1, the variable resistor serving to control the p.r.f. RV1 is designated M.T.U. FREQUENCY since the generator output simulates the pulse normally derived by the active decoder from the station master trigger unit.

8. Two outputs are taken from V1. The voltage pulse developed at the collector is fed via C1 to socket SKB to serve as an oscilloscope trigger pulse. The current pulse produced across the series 14-turn windings is applied to the primary of TR2.

9. Transistor V2 and pulse transformer TR2 form a regenerative amplifier which is normally cut off by the $+0{\cdot}5$V bias on the base. The back edge of the pulse applied to TR2 primary overcomes the bias and normal blocking oscillator action ensues so that a 1μs pulse is produced at V2 collector. This pulse is delayed approximately 5μs behind the oscilloscope prepulse appearing at SKB.

10. The 1μs pulse output from the regenerative amplifier is fed to the test selection switch SWA. In the first position of this switch (COUNTING CHAINS) the pulse is developed across the primary winding of pulse transformer TR4 and the secondary output is fed, via switches SWE to SWK, to the printed wiring board sockets. At the other two settings of SWA the pulse is applied to the input of the internal two-stage counter.

11. Transistor V5 and pulse transformer TR3 constitute a blocking oscillator similar to the first pulse generator. V5 base is returned to the -10V line through R9 and a variable resistor RV2 which controls the recovery time of the oscillator and hence the reset frequency. The output is a current pulse approximately 5μs long which forms a resetting waveform for the counter chain in the test set and also for the counter chains on boards under test. The corresponding voltage pulse appearing at V5 collector is used to reset the Eccles-Jordan circuit.

Counter chain

12. MC1, V3 and MC2, V4 form a two-stage counter identical with those employed in the active decoder and described in Part 1, Sect. 5, Chap. 2. The main functions of the counter are to provide suitable waveforms for checking the memcore assemblies in the matrix decoder and facilities for the CV7004 transistor test. In this application the counter is not continuously operative and is controlled by the test selection switch. When SWA is set to COUNTING CHAINS, the circuit between MC1, V3 and MC2 is broken and the counter receives no trigger pulse. In the SET UP & E/J position of SWA the counter is triggered by the regenerative amplifier and is reset by the reset oscillator. In the TRANSISTOR position of the switch the memcore connections are brought out to the three terminals above the meter and the counter is then operative only when an external transistor is connected to the terminals.

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Test selection switch

13. This is the main function switch of the test set since it controls both pulse generators and the counter. Its operation may be more clearly followed by reference to fig. 3. When the switch is set to COUNTING CHAINS, the current pulse from the regenerative amplifier V2 is fed to transformer TR4 and thence, via the secondary on/off switches, to the printed wiring board sockets. The divide-by-two counter in the test set is inoperative as V3 is disconnected and there is no input trigger. The current pulse from the reset oscillator V5 is also fed, via contacts on SWA, to the sockets. Thus the counting chain on a board under test is supplied with trigger and reset pulses. However, the test set reset oscillator is free-running with its frequency controlled by RV2 so that, to ensure occurrence of the reset pulse at the correct instant, the output from the last stage in the counter chain being tested is fed back through SWA to the 14-turn winding on TR3 connected to terminals 3 and 4. With RV2 correctly adjusted, the reset oscillator is thus locked to the external counter.

14. When SWA is turned to SET UP & E/J, V3 in the test set is connected in circuit and the pulse from the regenerative amplifier is applied to the trigger winding on MC1. RV2 is now short-circuited and the reset oscillator is locked by the output pulse from the internal counter. The current pulse from V5 is fed into the reset winding on MC1. The same circuit conditions exist when SWA is set to TRANSISTOR with the exception that V3 is again disconnected and the memcore connections are brought out to terminals on the panel. With a transistor connected to these terminals the test set operation is the same as for the centre setting of SWA.

Crystal oscillator

15. Transistor V7 is connected in a Colpitts circuit in which the inductive reactance is provided by a quarz crystal XL1. The circuit oscillates at the parallel resonant frequency of the crystal (345 kc/s). The succeeding stage is an emitter follower V8, the output from which is fed to socket SKA. This oscillator is provided to facilitate setting up the oscillator in test set 4678 but its output is also applied, via SKH/3, to the strobe input when a pulse train counter board is being tested.

Power supplies

16. Power supplies for the test set itself and for printed wiring boards under test are provided by a built-in power unit. Transformer TR5 requires a 200-250 V, 50 c/s single-phase input which is fed in on the 3-pole plug PLA and thence, via the main on/off switch SWL, fuses FS3, FS4 and the thermal cut-out FS5, to the primary winding. One secondary on TR5 delivers 26-44 V r.m.s., in 2 V steps, to a bridge rectifier consisting of MR4, MR5, MR6 and MR7. The resultant d.c. output, with the correct tappings in use and after smoothing by the choke-input filter L1 and C9, is 20 V. This is developed across the output resistive network to give two lines of +10 and −10 V.

17. To protect the power supply and the associated equipment from damage which might be caused by overloading, an overload trip circuit consisting of transistor V6, relay RLA, RV3 and R21 is connected immediately after the filter. V6 emitter is taken to the +10V line and the collector which has the coil of relay A as its load, to the −10 V line. The base is returned to the slider of the preset potentiometer RV3. When relay A is energized by depressing SWD, so connecting the coil directly across the filter output, the contacts make and complete the +10 V line. Due to the low impedance of the resistive network across the nominal 20 V output, a steady current of approximately 1A is drawn from the supply, producing a potential drop of 0·5 V across R20 so that, with RV3 slider at the positive end of the track, V6 base is 0·5 V positive with respect to the emitter and the transistor is cut off. As RV3 slider is moved towards the junction with R21, V6 base bias is reduced until the transistor conducts and the flow of collector current causes relay A to be energized. RV3 thus operates as an overload sensitivity control and is normally adjusted, under full load conditions, to the point where just sufficient collector current flows to maintain the relay in an energized condition after SWD has been depressed.

18. If an overload occurs, due either to a fault within the test set or in an external circuit under test, the additional current drawn will increase the voltage drop across R20 and any fall in voltage at the junction of R20 and RV3 reduces the current through RV3 and R21. In consequence, V6 base bias rises and the collector current falls below the level required to keep the relay energized. When the fault has been cleared, operation of the SET OVERLOAD TRIP push-button switch SWD will restore the supply. It should be noted that, since the contacts of relay A are in series with the +10V line, operation of SWL alone is not sufficient to switch on the test set and it is necessary to depress SWD after closure of SWL.

19. The other secondary winding on TR5 delivers 210V to a half-wave rectifier MR8 and a resistance-capacitance filter consisting of C10, R23 and C7. The resultant d.c. output of approximately 250 V provides the supply for the matrix decoder input gates in place of that which is normally drawn from power unit (A.D. indicator) 12123.

METHOD OF USE

Preliminaries

20. Before attempting to use the test set the following precautions should be carefully noted: —

(1) The test set must at all times be switched off when connecting a transistor to (or disconnecting it from) the terminals and when inserting a board into (or removing one from)

the sockets. Failure to observe this rule may result in damage to the test set and/or the item under test.

(2) Only one printed wiring board at a time may be plugged into the test set.

(3) Always check the meter reading before depressing the meter safety switch. The switch must not be operated if the meter reading exceeds 0·2μs.

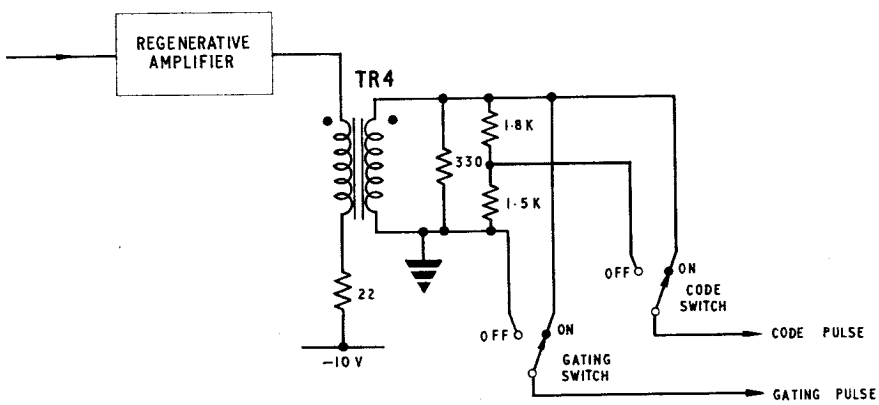
21. Before making any tests the test set should be set up, a process which merely requires adjustment of RV1 to ensure that the correct standard reading is obtained on the meter. With the test selection switch at SET UP & E/J, switch on the test set and check that the meter reading does not exceed 0·2μs. Then, with the meter safety switch depressed, adjust the M.T.U. FREQUENCY control (RV1) until the meter reading is the same as the value indicated on the tablet. It is advisable to check the setting of RV1 each time the unit is used for transistor testing but this is not important when testing active decoder boards.

22. When testing printed wiring boards the p.r.f. at which the circuits operate is not important and the optimum setting for RV1 is that which gives maximum brilliance of the oscilloscope display. With a printed wiring board inserted in the sockets and the test selection switch at SET UP & E/J, turn RV1 fully clockwise. It may be found that at this setting the meter reading falls to a lower value, in which event the control should be rotated clear of the point of instability.

23. Connect the oscilloscope signal lead to the collector of the last transistor of the counting chain of the board under test and set the test selection switch to COUNTING CHAINS. Turn RV2 fully anti-clockwise. Observing the pulse on the oscilloscope display, rotate RV2 clockwise until the pulse disappears, then turn the control back until the pulse re-appears.

Matrix decoder 6886 test

24. The circuit conditions when testing a matrix decoder counter are shown in simplified form in fig. 4. The 1μs pulse from the regenerative amplifier



◀ Fig. 4. Output circuit for matrix counter test : ▶ simplified diagram

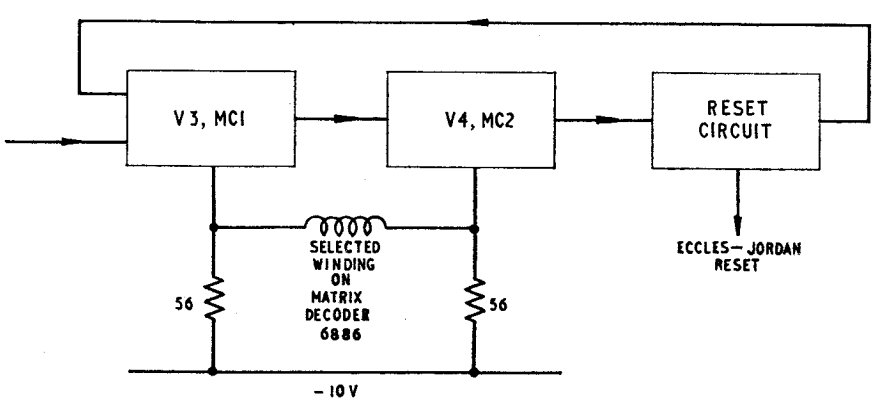


Fig. 5. Read-out winding test: simplified diagram

is developed across the primary winding of pulse transformer TR4 and a 17·5 V pulse is produced across the secondary. This output is employed as a gating and/or code pulse to check the input circuit and counting chain on the board. Detailed instructions are contained in the tabulated data at the end of the chapter. The counting chain on the board is reset by the test set reset oscillator and if a fault exists its position may be easily ascertained.

25. To test the memcore assembly forming the matrix, set the test selection switch to SET UP & E/J and rotate the READ OUT WINDING switch SWB to the required positions in turn. The relevant circuit is given in simplified form in fig. 5. Due to the action of the two-stage counter in the test set, current pulses will be passed in alternate directions through the particular read-out winding on the memcore assembly selected by SWB. These pulses will switch the two cores through which they pass to alternate "1" and "0" states, provided there are no short-circuited turns and that the cores are not cracked.

26. The core switching may be detected by observing the waveform present on the windings. This takes the form of two pulses of slightly differing amplitudes whose spacing is determined by the particular p.r.f. to which the test set oscillator is adjusted. Thus, by selecting each position of SWB in turn and examining the outputs on both the pulse and query read-out windings, it is possibl to test every core in the memcore assembly.

27. A switch SWH (O/P GATE) is provided to enable the operation of the output gate transistors V8 and V9 on matrix decoder 6886 to be checked. The collector of V8 is connected, via a 1 kilohm resistor in the test set, to the −10 V line. When SWH is in the OFF position, the emitters of V8 and V9 are taken to −10 V. Thus, V8 and V9 are operating under the same conditions as in a decoder, i.e. bases, emitters and collectors are all at the same potential and the pulses from the read-out windings, applied between base and emitter, have no effect.

28. When the O/P GATE is set to ON, the emitters of V8 and V9 are connected to earth. Both gates are then open and the pulses from the read-out windings will cause base current to flow in the transistors. Thus, V8 and V9 collector waveforms may be observed. The pulse developed at V9 collector should trip the Eccles-Jordan circuit (V10 and V11) to the on state.

29. The reset pulses generated within the test set are employed to reset the internal divide-by-two counter and the Eccles-Jordan circuit on the board. Thus, when regeneration occurs in the MC1, V3 stage, the pulse fed through the read-out windings will cause V10 and V11 on the board to be switched to the on state, provided the O/P GATE switch is set to ON. The subsequent voltage reset pulse from the test set switches the transistors back to the off state. This means that the state of the Eccles-Jordan circuit is changed at each trigger pulse with the result that a square waveform, with an amplitude of 10 V and a p.r.f. equal to one-half that of the trigger pulse, should be observed at the collectors of V10 and V11. At these two points the waveforms will be 180° out of phase.

30. To enable the performance of the output circuit on the board (V12 and V13) to be checked, a 100-ohm resistor is provided in the test set to serve as a collector load for V13. This resistor is connected to the −10 V line and takes the place of the relay coil which is the normal load. At V13 collector a square waveform similar to that at V10 collector should be observed. The waveform will, however, be slightly modified due to the greater hole storage effect of the CV7006 transistor.

31. The ninth position of the READ OUT WINDING switch is provided for testing the sensitivity of the Eccles-Jordan circuits. There are twelve memcore assemblies in an active decoder with their pairs of read-out windings in series and in certain circumstances all 24 cores bearing a particular read-out winding may have to be switched. In such an event the output will be reduced and may be insufficient to trip an insensitive Eccles-Jordan. This represents the worst condition under which the Eccles-Jordan has to operate and is simulated by providing in the test set a special assembly X4, consisting of 22 cores switched by a six twin winding. In the SENS. position of SWB, X4 is connected in series with the first read-out winding in the matrix.

Interval timer 6885 test

32. The output circuit of the test set for testing the interval timer is shown in simplified form in fig. 6. The trigger pulse is again taken from TR4 but is inverted in polarity to give a negative waveform. This negative pulse is used to trigger the input blocking oscillator on the board (V1 and TR1). The MTU output from the ring counter is coupled back, through a 100-ohm resistor in the test set, to the gating pulse input of the starting memcore.

33. The test set reset pulse sets the starting memcore to "1" and the next MTU pulse from the last stage in the ring counter switches it back to "0". The subsequent regeneration resets both counting chains on the board so that normal counting commences and the waveforms may be traced by observing the output at each collector.

34. The query Eccles-Jordan circuit on the timer board is switched by alternate pulses from V3 and the reset oscillator in the test set in a similar manner to the Eccles-Jordan on the matrix decoder, the only difference being that the on pulse is applied direct from the test set to the query in-

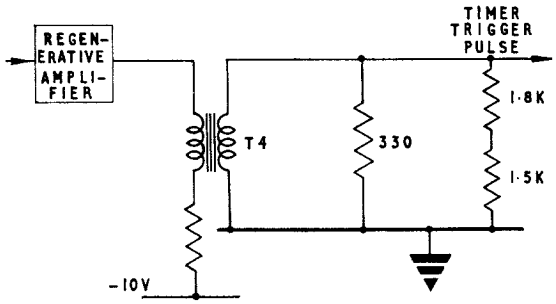


Fig. 6. Output circuit for interval timer test: simplified diagram

put. A 100-ohm load is provided in the test set for V17 so that the output transistors may be checked as described in para. 30.

Pulse train counter 6887 test

35. The counting chain on this board may be checked in the same manner as those on the other boards by setting SWK to READ OUT TRIGGER when the test set pulse developed across TR4 is applied to the read-out trigger blocking oscillator on the board. Testing of the gating pulse blocking oscillator is done by setting the switch to GATING PULSE 6887 INPUT but in this case the pulse is not fed to the board internally. The gating pulse supplied to the pulse train counter in normal operation is much larger in amplitude than that produced by the test set and a limiting resistor is connected in series with the transformer input. If the test set pulse were fed via this resistor the resultant attenuation would render it insufficient to trigger the stage. Accordingly, the gating pulse from the test set is fed out to socket SKC (FOR 6887 TEST) on the panel and to test V2, TR2 on the board it is necessary to connect the socket to terminal 6 on TR2.

36. The Eccles-Jordan circuit controlling the input gate may be tested in the same manner as with the other boards. However, since this circuit has alternative inputs, either the timer closure pulse or the P.T.C. closure pulse, a switch SWJ (DIODE CHANGE) is provided so that the test set pulse may be fed to either input. To permit testing of the decoder input gate and indicator-on circuits, 100-ohm collector load resistors for V6 and V9 on the board are included in the test set. In addition, the output of the 345 kc/s oscillator is applied to the strobe input so that V8 is switched on and off at this frequency.

Tabulated test data

37. At the end of the chapter will be found tables containing detailed test instructions, descriptions of the approximate waveforms which should be observed at the test points and the probable faults indicated by certain incorrect signals.

Transistor test

38. With the test set switched off, connect the transistor to the three terminals above the meter, taking care that the leads are correctly placed and not short-circuited. Turn the test selection switch to TRANSISTOR, switch on the test set and, if the meter reading does not exceed 0·2μs, depress the meter safety switch. The meter reading is now the length of the pulse produced by the external transistor and should be within $\pm$0·5μs of the standard value.

Boards, jumper 16375, 16376 and 16377

39. The three jumper boards for which stowage provision is made in the test set case are designed to facilitate testing an active decoder under operating conditions. Each consists of a printed wiring board with a normal edge connector coupled directly to sockets at the top of the board. In use, a jumper board replaces the decoder board which is then plugged into the top of the jumper, thus making the circuits accessible. Each jumper board is identified with a reference to the decoder board which it serves.

TABLE 1

Matrix decoder 6886 test data

(1) Test selector switch to COUNTING CHAINS

Pulse switch positions	*Inspection point*	*Correct signal*	*Possible signal*	*Probable fault*
M.T.U. PULSE OFF GATING PULSE ON	MR2 cathode	17·5 V, 1μs pulse	Nil	Edge connector faulty
CODE PULSE ON	MR1 cathode	17·5 V, 1μs pulse	Nil	Edge connector faulty
GATING PULSE and CODE PULSE ON	Junction of R8 and MR1	6-8 V, 1μs pulse	Nil	MR1 and/or MR2 faulty
GATING PULSE ON and CODE PULSE OFF	do.	Nil	12V, 1μs pulse 1 V, 4μs pulse	MR1 open-circuit MR2 short-circuit
GATING PULSE OFF and CODE PULSE ON	do.	Nil	12V, 1μs pulse 1 V, 4μs pulse	MR1 short-circuit MR2 open-circuit
GATING PULSE and CODE PULSE ON	Junction of RV1 and TR1 (terminal 7)	10 V, 1μs pulse	10 V, pulse with long decay	Edge connector faulty or 50-turn winding on TR1 open-circuit
			1V, 1μs pulse	V1 faulty
	V1 collector	10 V, 1μs pulse starting from −10 V	Nil (at earth)	A 10-turn winding on any memcore open-circuit Collector winding on TR1 open-circuit V1 faulty
			Nil (at −10 V)	V1 faulty or short-circuited turn on TR1
	Memcore assembly (pin 12)	10 V, 4-8μs pulse	Nil	Reset winding in memcore assembly or in any memcore open-circuit Edge connector faulty
	Junction of R2 and pin 6 of memcore	10 V, 3-4μs pulse starting from −10 V	Nil (at −10 V) Nil (at earth)	Code winding in memcore assembly open-circuit or V2 short-circuited (when R2 will overheat)
	Junctions of R3, R4, R5, R6, R7 and memcore assembly	10 V, 3-4μs pulse starting from −10 V	Nil	Faulty components corresponding to those indicated in preceding test

(2) Test selection switch to SET UP & E/J

READ OUT WINDING to 1 O/P GATE OFF	Terminal 3 on memcore assembly	1 V, 1·5μs pulse negative-going (with the CRO set to the fast range there will be two super-imposed traces. Observe the one with the − ve pulse)	Nil	Cracked core Short-circuited turn on core Open-circuit pulse winding Open-circuit read-out winding Faulty edge connector
READ OUT WINDING to all other positions up to 8, in turn	do.	do.	Nil	do.
READ OUT WINDING to 1-8, in turn	Terminal 1 on memcore assembly	do.	Nil	do.

Pulse switch positions	*Inspection point*	*Correct signal*	*Possible signal*	*Probable fault*
READ OUT WINDING to 1 O/P GATE ON	V9 collector	10 V, 2μs pulse with long decay (4μs)	Nil	V9 faulty
	V8 collector	do.	Nil	V8 faulty
O/P GATE OFF	V9 collector	Nil	Any	V9 faulty
	V8 collector	Nil	Any	V8 faulty
O/P GATE ON	V10 collector	10 V square wave	Nil (at – 10 V)	V10 cut off
			Nil (at earth)	V10 conducting
	V12 collector	7 V square wave	Nil (at – 10 V)	V12 open-circuit
			Nil (at – 3 V)	V12 short-circuit
	V13 collector	10 V square wave with long decay (100μs) on – ve edge	Nil	V13 faulty
READ OUT WINDING to SENS	V13 collector	do.	Nil (at – 10 V)	E/J insufficiently sensitive due to low gain of V9, V10, V11

Note . . .

(1) *The Matrix decoder* 6886 *input sensitivity must always be reset if its position within the Decoder sub-assembly (active)* 4676 *is changed, or the components associated with the regenerative amplifier V*1 *or the diode gate are changed.*

(2) *If the circuit fails to regenerate an input pulse, the cause can be attributed to saturation of the pulse transformers. This condition can be corrected by removing the affected board and using a defluxer, e.g. Wearite Defluxer, as directed by the manufacturer of the device.*

TABLE 2
Interval timer 6885 test data

(1) Test selection switch to COUNTING CHAINS

Pulse switch positions	*Inspection point*	*Correct signal*	*Possible signal*	*Probable fault*
M.T.U. PULSE ON	V1 collector	10 V, 1μs pulse starting from – 10 V	10 V, 1μs pulse with 10 V – ve overswing at end	MR1 open-circuit
			Nil	Open-circuit winding (pins 2 to 10) on any one of MC2 to MC6 V1 or TR1 faulty
	Junction of R13 and pin 9 on MC11	10 V, 3-4μs pulse starting from – 10 V	Nil (at – 10 V)	Open-circuit winding (pins 3 to 9) on any one of MC2 to MC6 Open-circuit 10-turn winding on any one of MC7 to MC11 V2 for MC1 faulty
	R2, R3, R4, R5, R6 as for matrix decoder chain	10 V, 3-4μs pulse starting from – 10 V	Nil	As for matrix decoder chain
	V8 collector	10 V, 1μs pulse starting from – 10 V	10 V 1μs pulse with 10 V – ve overswing at end	MR2 open-circuit
			Nil	Open-circuit winding (pins 2 to 10) on any one of MC7 to MC11 V8 or TR2 faulty
	R7, R8, R9, R10 and R11	10 V, 3-4μs pulse starting from – 10 V	Nil	As for matrix decoder chain

Pulse switch positions	*Inspection point*	*Correct signal*	*Possible signal*	*Probable fault*
(2) Test selection switch to SET UP & E/J				
	V14 collector	10 V square wave (timebase range 3)	Nil	Eccles-Jordan fault
	V16 collector	7 V square wave	Nil	V16 faulty
	V17 collector	10 V square wave	Nil	V17 faulty

Note . . .

If the circuit fails to regenerate an input pulse, the cause can be attributed to saturation of the pulse transformers. This condition can be corrected by removing the affected board and using a defluxer, e.g. Wearite Defluxer, as directed by the manufacturer of the device.

TABLE 3

Pulse train counter 6887 test data

(1) Test selection switch to COUNTING CHAINS

Pulse switch positions	*Inspection point*	*Correct signal*	*Possible signal*	*Probable fault*
6887 INPUT to READ OUT TRIGGER	V1 collector	10 V, 1μs pulse starting from − 10 V	10 V, 1μs pulse with 10 V − ve overswing at end	MR1 open-circuit
			Nil	An open-circuit 10-turn winding (pins 2 to 10) on any one of MC1 to MC9 V1 or TR1 faulty
6887 INPUT to GATING PULSE (connect SKC to terminal 6 of TR2 in counter via a short lead)	V2 collector	10 V, 1μs pulse starting from − 10 V	10 V, 1μs pulse with 10 V − ve overswing at end	MR2 open-circuit
	R17, R18, R19, R20, R21, R22, R23, R24, R25 as for matrix decoder chain	10 V, 3-4 μs pulse starting from − 10 V	Nil	As for matrix decoder chain
6887 INPUT to READ OUT TRIGGER	do.	do.	Nil	do.
(2) Test selection switch to SET UP & E/J				
DIODE CHANGE to MR3	V3 collector	10 V square wave (timebase range 3)	Nil	MR3 faulty Eccles-Jordan fault
DIODE CHANGE to MR4	V3 collector	10 V square wave)	Nil	MR4 faulty Eccles-Jordan fault
	V5 collector	5 V square wave	Nil	V5 faulty
	V6 collector	10 V square wave with long decay	Nil	V6 faulty
	V7, V8 common collector	Square waveform of fluctuating amplitude (0 to 10 V)	Nil 345 kc/s sine wave 1 kc/s (approx) waveform	V7 or V8 faulty V7 faulty V8 faulty
	V9 collector	Square waveform of fluctuating amplitude (0 to 10 V)	Nil	V9 faulty

Note . . .

If the circuit fails to regenerate an input pulse, the cause can be attributed to saturation of the pulse transformers. This condition can be corrected by removing the affected board and using a defluxer, e.g. Wearite Defluxer, as directed by the manufacturer of the device.

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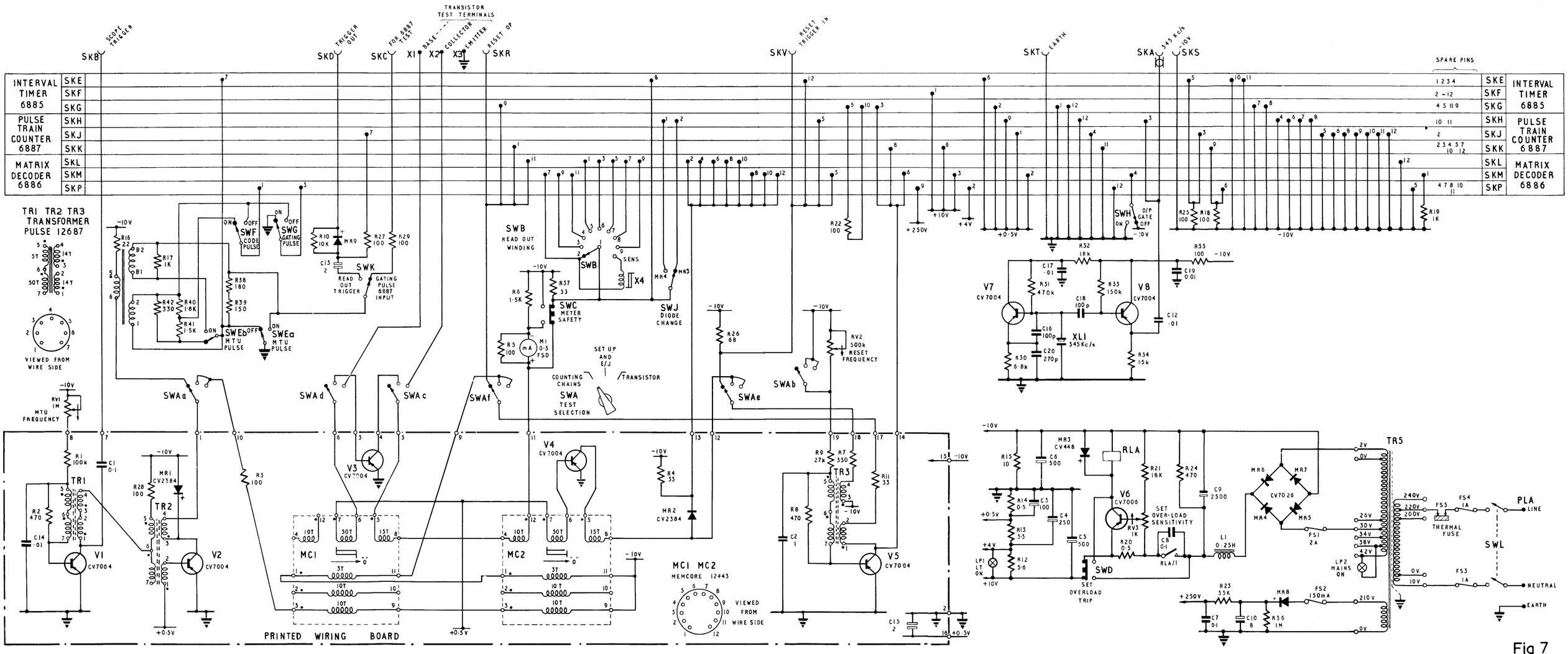

Fig. 7

Test set, electronic circuits (JS6625-99-580-1640): circuit

Fig. 7

A.P.2906K
A.L.19, Feb. 59

DATA FOR THIRD LINE SERVICING

SECTION 1

STATIC INSTALLATIONS

Chapter 1.— RADAR OFFICE EQUIPMENT

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

General

1. Whenever components have been replaced or major servicing has been done on any unit of the IFF Mk. 10 radar office equipment, the appropriate tests detailed in this chapter should be performed. These tests are sufficiently comprehensive to ensure that any unit which passes them satisfactorily may be regarded as fully serviceable and capable of operating at maximum efficiency.

2. Whilst the question of removing any particular unit from a rack for servicing will depend upon the degree of unserviceability and/or location of the fault, it will be found that, in general, most servicing can be done with the unit *in situ*. In addition, the majority of the tests specified are more easily performed with the equipment assembled in the racks since the necessary services, i.e. pulse waveforms and power supplies, are readily available.

3. This chapter is concerned only with those units which require extensive electrical tests. Tests on the racks alone and some of the units, e.g. panel (standby interconnection) 6371, are limited to routine continuity and insulation resistance measurements which require no detailed description.

Test equipment

4. The test equipment required when servicing units of the IFF Mk. 10 radar office equipment is given in the following lists. The first list contains those items of general application which should normally be readily available. The second list consists of test gear provisioned as part of the installation.

General test equipment

Multimeter Type 1 (Ref. No. 10S/16411)

Tester, insulation, Type H (Ref. No. 5G/1621)

High-speed calibrated oscilloscope CT316 (Ref. No. 10S/16605)

Double-beam oscilloscope Type 13A (Ref. No. 10S/831)

Output pad (local construction) (*para.* 19)

Power unit special connector (local construction) (*para.* 21)

Pulse generator with the following positive-going outputs at 250±12 c/s and 550±27 c/s:-

(1) Trigger pulse 4μS in duration and 15V in amplitude when coupled into a 68-ohm load

(2) 20V oscilloscope sync pulse, synchronized to the trigger waveform

(3) A video pulse 20V in amplitude variable in duration from 0·3 to 1μS and capable of being delayed by 0 to 30μS after the trigger waveform

Variac capable of providing a supply of 2A at 216 to 244V from a 50 c/s supply

Sources of +300V ±15V and −100V ±5V d.c., e.g. power unit 4465

Sources of 50V at 700mA d.c. and 240V 50 c/s single phase a.c.

Installation test equipment

Switch unit 4821 (Ref. No. 10F/18185)

Tester (relay unit) (Ref. No. 10S/16689)

Test meter (voltage) 4883 (Ref. No. 10S/16688)

Panel (metering) 4466

5. (1) Short-circuit the meter M1. Using multimeter Type 1, check that continuity exists between SW4 a/12 and PL1/8, PL1/2, PL2/5, PL2/7, PL2/8, SW4 a/9, SW4 a/10 and SW4 a/11 when the meter switch is set to PU3 +300V, PU2 +300V, PU1 +300V, W/GEN UNIT 6, W/GEN UNIT 4, PU1 −70V, PU2 −70V and PU3 −70V in turn.

(2) Similarly, check that continuity exists between SW4 b/12 and SW4 b/3, SW4 b/4, SW4 b/5, SW4 b/6, SW4 b/8, PL2/6, PL1/4 and PL1/10 when the meter switch is moved through the same positions as in (1).

(3) With the multimeter set to a resistance range, check that the resistance measured between SW4 a/12 and SW4 b/12 is 910 ohms ±9·1 ohms.

(4) Remove the short-circuit from the meter and connect the common earth of the +300V and −100V supplies to PL2/1. Connect the +300V to PL2/5 and turn the meter switch to PU1 +300V. Check that the meter reading is 3 ±0·3.

(5) Connect the −100V to PL2/6 and set the meter switch to PU1 −70V. Check that the meter reading is 2 ±0·2. Disconnect the 300V and 100V supplies.

(6) Using multimeter Type 1, check that only when SW1 is set to ON does continuity exist from PL2/11 to PL2/3 and from PL2/12 to PL2/4.

(7) Connect the 50V d.c. supply between PL1/6 (negative) and PL2/1 (positive). Set SW3 to REMOVE PU3 and check that continuity exists from PL1/9 to PL2/6 and from PL1/7 to to PL2/5. Check also that there is a potential difference of 50V between PL2/1 and PL1/12 only when SW3 is set to REMOVE PU3. Set SW3 to NORMAL.

(8) Set SW2 to REMOVE PU2 and check that continuity exists from PL1/3 to PL2/6 and from PL1/1 to PL2/5. Check also that there is a potential difference of 50V between PL2/1 and PL1/12 only when SW2 is set to REMOVE PU2. Set SW2 to NORMAL.

Control unit 4227

6. (1) With multimeter Type 1 set to a resistance range, connect the instrument between PL1/8 and PL1/10. Check that the resistance between these pins varies smoothly from a minimum not greater than 25 ohms to 1000 ohms ±200 ohms when the GAIN control is turned in a counter-clockwise direction.

(2) Check the continuity from PL1/3 to PL1/1 and from PL1/6 to PL1/1 via the lamps. The resistance indicated should be that of an individual lamp, i.e. 35 ohms ±15 ohms.

(3) With SW2 set to LONG, check that the resistance between PL1/1 and PL1/9 is zero. Set SW2 to SHORT and check that there is an open circuit between PL1/1 and PL1/9.

(4) Set SW3 to SPARE and check that continuity exists between SK4 and SK5, but not between SK1 and SK5. Set SW3 to NORMAL and check that continuity now exists between SK1 and SK5, but not between SK4 and SK5.

Waveform generator 6010

General

7. In order to test thoroughly and correctly set up a waveform generator 6010, a pulse generator of the type specified in the list of test equipment is essential. In particular, to obtain optimum settings of the preset controls for operation over the range of repetition frequencies which the waveform generator is designed to cover (225 to 550 c/s) the tests detailed in para. 16 should be performed as directed.

8. However, since it is improbable that a waveform generator will be separated from the installation of which it forms a part, a satisfactory alternative is to do all testing and setting up at the p.r.f. of the station where the unit is installed. Thus, when a suitable pulse generator is not available, the station p.r.f. should be ascertained and this figure used in all tests where specific p.r.f. values are quoted. For test purposes the most convenient source of pulse waveforms within the radar office is the output from a delay unit Type 31 (rack assemblies 180 - 183) associated with the master trigger unit.

Waveform definitions

9. Except where otherwise specified, the parameters of all waveforms in the waveform generator are to be measured as follows: —

(1) *Duration*: From the point on the leading edge at half the peak amplitude of the waveform to the corresponding point on the back edge.

(2) *Amplitude*: From the normal baseline to the peak of the waveform, ignoring any transient disturbances of the baseline in the vicinity of the waveform such as the recovery transient following a previous pulse.

(3) *Pulse spacing (i.e. the relative delay between two pulses occurring successively in the same circuit)*: The time measured between a point on the leading edge of one pulse at half of its peak amplitude to the corresponding point at the same voltage level on the leading edge of the other pulse. If the amplitudes differ, the measurement is to be made at a level equal to half the amplitude of the smaller pulse.

(4) *Pulse delay (i.e. the relative delay between two pulses occurring successively at different circuit points)*: The time measured between points on the leading edges of the two pulses concerned at one-half of their respective peak amplitudes.

(5) *Rise time*: Between points on the leading edge of the pulse which are at levels of 10% and 90% of the peak amplitude of the pulse.

(6) *Rise time of interlaced gating waveforms*: From the point at which the leading edge of the positive-going waveform starts to the point where the waveform crosses the zero voltage level. Apart from a slight positive overshoot above the zero voltage level the whole of each gating waveform is negative with respect to earth.

Preliminaries

10. (1) Check that the internal links are in the correct positions for normal operation.

(2) Remove SK1 and, in its place, couple switch unit 4821 to PL1. Connect SK1 to PL1 on the switch unit. Check that 50V d.c. is present between pins 1 and 7 of PL1.

(3) Close the MODE 1 switch on the switch unit. Check that lamp LP1 lights and that relay RLA in the waveform generator is energized so that socket X7 is connected to earth. Return the MODE 1 switch to the OFF position.

(4) Close the MODE 2 switch on the switch unit. Check that lamp LP2 lights and that relay RLB is energized so that socket X8 is connected to earth. Return the MODE 2 switch to the OFF position.

(5) Close the MODE 3 switch on the switch unit. Check that lamp LP3 lights and that relay RLC is energized so that socket X9 is connected to earth. Return the MODE 3 switch to the OFF position.

(6) Close both the MODE 1 and MODE 2 switches. Check that relays RLA, RLB and RLE are all energized so that X7 is connected to pin 2 of V8 and X8 to pin 7 of V8. Return the MODE 1 switch to the OFF position.

(7) Close the MODE 3 switch. Check that RLB, RLC and RLF are all energized so that X8 is connected to pin 2 of V8 and X9 to pin 7 of V8. Return the MODE 2 switch to the OFF position.

(8) Close the MODE 1 switch. Check that RLA, RLC and RLG are all energized so that X8 is connected to pin 2 of V8 and X9 to pin 7 of V8.

(9) Close the MODE 2 switch. Check that RLA, RLB, RLC, RLD, RLE, RLF and RLG are all energized so that X7 is connected to pin 2 of V8, X8 to pin 7 of V8 and X9 to the junction of C14 and R42. Set all three mode switches to the OFF position.

Voltages

11. (1) Set the MAINS switch on panel (metering) 4466 to ON and check that 230V 50c/s is present at pins 11 and 12 of PL1 on the waveform generator.

(2) Measure the heater voltages of all the valves at the valve bases and check that these are 6·3V ±0·3V.

(3) With the correct input supplies from a power unit 4465, measure the bias voltage between PL1/9 and earth and check that this is 75V ± 8V.

Currents

12. (1) Inject into SK1 on the waveform generator a positive-going 4μS sync pulse 15V in amplitude at a p.r.f. of 250 c/s ± 12 c/s. If a separate pulse generator giving this output is not available, the necessary waveform may be obtained (at the station p.r.f.) from a delay unit 31 associated with the master trigger unit. It should be noted that if the station p.r.f. is considerably higher than 250 c/s, e.g. 500 c/s, certain of the low level readings given in (2) may slightly exceed the maximum values quoted.

(2) Close the MODE 1 switch on switch unit 4821 and set the meter switch on panel (metering) 4466 to W/GEN UNIT 6 or W/GEN UNIT 4 according to the position of the waveform generator in rack (IFF control) 4467. Set the meter switch on the waveform generator to each position in turn and check that the following readings are obtained.

	Meter reading	
Switch position	*Lower limit*	*Upper limit*
V1	0·9	2·8
V2 and V3	0·65	2·0
V6B	0·3	0·9
V7	0·65	2·0
V8	0·3	0·9
V9, V10 and V11	0	0·25
V12	0	0·25
V13	0	0·25
V14	0	0·25
V15	1·5	4·5
V16	0·2	0·6
V18	0·8	2·5
V19	0·8	2·5
V20	0·8	2·5
V24	0	0·05
V25	0	0·25
V26	0	0·25
V27	0	0·25
V28 and V29	0·65	2·0
V30 and V31	0·65	2·0
V32 and V33	0·65	2·0
V36A	0·25	0·75
V36B	0·4	1·2

Mode trigger pulses

13. (1) Terminate SK2 (X2) with a 68-ohm ± 7 ohms resistor and connect the CT316 across it. Connect the oscilloscope SYNC input to either the X1 or X1A socket on the waveform generator. Close the MODE 1 switch on switch unit 4821.

(2) With the 4μS 15V pulse still applied to SK1, the two pulses observed at X2 should have the following characteristics:

Amplitude: not less than +25V peak
Duration at half amplitude: 1μS ± 0·2μS
Rise time: not greater than 0·2μS
Spacing: 3μS ± 0·2μS

(3) Check that the second pulse of the pair occurs 12μS ± 0·5μS after the trigger pulse at SK1. Return the MODE 1 switch to the OFF position.

(4) Close the MODE 2 switch and check that the two pulses appearing at X2 have the following characteristics:

Amplitude: not less than +25V peak
Duration at half amplitude: 1μS ± 0·2μS
Rise time: not greater than 0·2μS
Spacing: 5μS ± 0·2μS

(5) Check that the second pulse of the pair occurs 12μS $\pm$ 0·5μS after the trigger pulse at SK1. Return the MODE 2 switch to the OFF position.

(6) Close the MODE 3 switch and check that the two pulses appearing at X2 have the following characteristics:

Amplitude: not less than +25V peak
Duration at half amplitude: 1μS $\pm$ 0·2μS
Rise time: not greater than 0·2μS
Spacing: 8μS $\pm$ 0·2μS

(7) Check that the second pulse of the pair occurs 12μS $\pm$ 0·5μS after the trigger pulse at SK1. Return the MODE 3 switch to the OFF position.

Interlacing waveforms

14. Before attempting to make any tests on the interlacing circuits it should be noted that the circuit linking the cathode of V6A to the grid of V8A is very susceptible to the addition of earth capacitance and, in consequence, the procedure has been arranged to avoid coupling an oscilloscope to this part of the circuit during any adjustment of the interlacing controls RV1, RV2 and RV3. Instead, the operation of the circuit is observed at the grid of V8B, V7 then acting as a buffer amplifier.

15. With operation on three modes, X7 is connected to V8A grid and must only be used for observation of waveform characteristics or the adjustment of RV4. In two-mode operation, X7, X8 or X9 may be connected to the sensitive point depending upon the particular combination of modes. However, in the test procedure, all adjustments to the controls are made with a combination of either modes 1, 2 and 3 or modes 1 and 2, so that in both cases, X7 is connected to the sensitive point and all observations are made at X8, except when adjusting RV4.

16. (1) Increase the p.r.f. of the 4μS 15V trigger pulse to 550 c/s $\pm$ 27 c/s. Close the MODE 1 and MODE 2 switches on switch unit 4821. Turn RV4 fully counter-clockwise and adjust the SET 2 and SET 3 controls to the middle of their ranges.

(2) Vary the COUNTER ADJ control until there appears at X8 an unstable waveform which is intermediate between a square wave of equal mark-to-space ratio (divide by 2) and a stepped waveform with three horizontal levels (divide by 3). If this transition cannot be obtained within the limits of rotation, set the COUNTER ADJ control to that limit which gives a waveform most closely approaching the required mode of operation. That is, if 3 is the lowest division ratio obtainable the control should be set to the limit which gives this. Alternatively, if 2 is the highest division ratio attainable the control should be set to the limit giving that ratio.

(3) Adjust the SET 2 control to the optimum position to give a square wave of equal mark-to-space ratio at X8.

(4) Close the MODE 3 switch. Adjust the SET 3 control to the optimum position to give a stepped waveform at X8. This waveform should have three levels with one step which is of equal duration to the positive and negative-going portions of the waveform. Reset the trigger pulse p.r.f. to 250 c/s $\pm$ 12 c/s.

(5) Now turn RV4 in a clockwise direction until interference with the waveform at X7 is apparent on an oscilloscope slow timebase, i.e. the horizontal portions of the waveform start to slope. Turn RV4 counter-clockwise until this interference just ceases.

(6) Remove the trigger pulse from SK1. Check that there is no slow periodic waveform at X8. It should be noted that the presence of such a waveform may be due to RV4 having been turned too far counter-clockwise when setting-up the control as described in (5). Re-connect the trigger pulse to SK1 and set the MODE 3 switch to the OFF position.

(7) Check that the waveforms at X7 and X8 are square waves of not less than 10V in amplitude and that the positive-going wavefronts have a rise time of not more than 3·9μS.

(8) Set the MODE 2 switch to OFF and close the MODE 3 switch. Repeat (7), observing the waveforms at X7 and X9.

(9) Set the MODE 1 switch to OFF and close the MODE 2 switch. Repeat (7), observing the waveforms at X8 and X9.

(10) Close the MODE 1 switch. Check that the positive-going portion of the waveform at X8 is not less than 10V in amplitude and that the rise time is not more than 4μS.

(11) Observe the waveform at X7 and check that this is the X8 waveform inverted with an amplitude of not less than 10V and a rise time of not more than 4μS.

(12) Observe the waveform at X9 and check that this is a positive-going square wave with a mark-to-space ratio of 1:2. The positive-going portion should be not less than 10V in amplitude and the rise time not more than 3·9μS.

(13) Check that the combined output at SK2 meets the requirements laid down in para. 13.

17. When setting-up and testing a waveform generator on a remote Type 7 radar site, it is important to avoid RF interference from the Type 7 transmitter and the following precautions must be observed.

(1) Ensure that the door to the transmitter room is securely closed.

(2) When observing the waveforms at X7, X8 and X9, the connection between the monitoring point and the oscilloscope should be made via a 6 ft. length of uniradio 70 cable. The braiding of this cable must be earthed at the waveform generator but not at the oscilloscope.

(3) After the preset controls have been adjusted, the cable should be removed and the oscilloscope connected to SK2 (X2) by a length of wire for checking the pulse-pairs.

Video output

18. In order to check the video chain completely, a delayed video pulse variable in duration and amplitude is normally required. However, if a suitable pulse generator is not available, a pulse may conveniently be taken from one of the delay units 31 associated with the master trigger unit. The waveform from this source will be a 4μS 20V pulse variable in delay only, but will enable the majority of the tests to be performed since the video output of the waveform generator is determined by circuits within the unit and not by the characteristics of the applied video waveform. Thus, to test the video circuits in the absence of a pulse generator, the outputs from two delay units 31 are required, one to trigger the waveform generator and the oscilloscope and the other to provide a delayed video pulse.

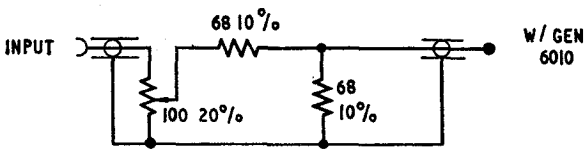

Fig. 1. Output pad for pulse generator

19. Construct an output pad as shown in fig. 1 and couple the video pulse via this pad to SK3 on the waveform generator. It should be noted that to discount the reactive loading effect of the input circuit at SK3, the duration of the video pulse must always be measured at the input to the pad but the peak amplitude is measured at the output, i.e. across the 68-ohm shunt resistor.

20. (1) Set the pad potentiometer to give maximum pulse amplitude (of the order of 5 to 10V) at SK3. Connect a 68-ohm termination across SK4 (X4) and close the MODE 1 switch. Set the delay of the video input to approximately 20μS.

(2) Check that the output at X4 is a positive-going pulse between 12 and 24V in amplitude with a duration not greater than 1·2μS at half amplitude. The duration at 10% of full amplitude should not be more than 1·4μS.

(3) Connect a 0·04μF capacitor in parallel with the 68-ohm termination and check that the output at X4 is now not less than 3V peak.

(4) Remove the 68-ohm resistor and 0·04μF capacitor and replace them by a 27-ohm resistor and 0·01μF capacitor. Check that the output at X4 is still not less than 3V peak, and that the duration at the 1V level is not greater than 1·4μS.

(5) By adjusting the pad potentiometer, reduce the amplitude of the video input pulse to 2V and check that the output at X4 still does not fall below 3V. With the input amplitude held at 2V, reduce the duration of the input pulse to 0·3μS and check that the output amplitude at X4 is not less than 3V. With the input amplitude reduced to 0.8V peak the output at X4 should be less than 1V.

Note . . .

The second of these three tests, in which the pulse duration is reduced, cannot be performed if the video pulse is derived from a delay unit 31.

(6) Set the MODE 1 switch to OFF and close the MODE 2 switch. Repeat (1) to (5), observing the output at X5.

(7) Set the MODE 2 switch to OFF and close the MODE 3 switch. Repeat (1) to (5), observing the output at X6.

(8) Close the MODE 1 and MODE 2 switches and disconnect PL8 from SK8. Check that there is a negative-going pulse at one-half the p.r.f. at SK8. This pulse should be not less than 30V in amplitude and delayed behind the trigger at SK1 by 4 ± 1μS. Reconnect PL8 to SK8, set the MODE 1 and MODE 2 switches to the c position.

(9) Temporarily connect together terminals 7, 8 and 9 of TBA (two of these will already be joined). Check that on these terminals there is a negative-going pulse at the full p.r.f. The amplitude should be between 32 and 38V and it should decay to zero within the limits of 7 50μS. Remove the temporary conn TBA, leaving the original co turbed.

Power unit 4465

21. Couple the power unit u form generator 6010. This is b ing both units into a rack (IFF some of the tests may then be perform. It is accordingly recommended that a connector be made up as shown in fig. 2 and

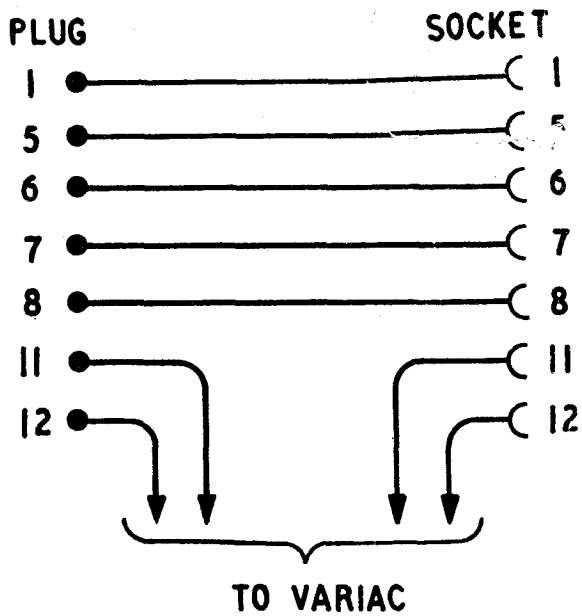

Fig. 2. Power unit test connector

inserted between the rack socket and the input plug on the power unit. This connector consists simply of male and female 12-pole Jones plug assemblies with the appropriate pins joined by lengths of wire. The overall length should not exceed 6 to 12 in. but the leads to pins 11 and 12 will need to be approximately 4 to 6 ft. so that the variac may be placed on the floor adjacent to the rack. The connector socket should not have its protective cover fitted, thus making the pins accessible as test points. However, it must at all times be remembered that high d.c. and a.c. potentials are present at some of the exposed pins when the equipment is switched on. The greatest care must be exercised to avoid shock, and also short-circuits which may cause damage to the equipment.

22. For the purpose of these tests it is essential that RV4 in the waveform generator should have been correctly set up as described in para. 16 (5). There must also be no trigger input to the wave- generator.

(1) Turn the SET +HT FINE control on the power unit fully counter-clockwise. Switch on both units and wait two minutes before making any tests. Check that the neon stabilizers V5 and V7 in the power unit have struck.

(2) Connect a multimeter Type 1 to the +HT METER socket on the power unit and check that the output voltage can be varied from a minimum which is not greater than 270V to a m of not less than 315V.

ive h.t. to 300V by adjustment RSE control and check that control has a range of operan 5V.

e waveform of the a.c. compositive h.t. supply at the meter n 8 of the connector socket and the ripple level is not greater than 10 mV peak-to-peak.

(5) Observe the a.c. component of the negative supply at pin 5 of the connector socket and ensure that the ripple level is not greater than 12mV peak-to-peak.

(6) Connect the multimeter Type 1 between pin 5 on the connector socket and earth and check that the output of the negative supply is 75 ± 5V.

(7) Disconnect SK1 from the waveform generator and check that the negative supply rises to 150V ± 10V. Reconnect SK1 to the waveform generator.

(8) Vary the a.c. input supply over the range 216V to 244V and check that the positive output as measured at the +HT METER socket does not change by more than 0·25V.

Note . . .

For the greatest accuracy in measurement, a suppressed zero voltmeter calibrated in steps of 1V should be used for this test. Alternative methods however, are to use a test meter Type D1 (Ref. No. 10S/10610) or a low reading voltmeter in conjunction with a backing-off voltage such as two 120V dry batteries in series.

(9) Similarly, using multimeter Type 1, check that the change in the negative output at pin 5 is not greater than 1V for a variation of input voltage from 216 to 244V. Reset the input voltage to 230V.

(10) Using multimeter Type 1, check that 6·3V ± 0·63V a.c. appears between pins 7 and 1 when the power unit is operating normally. Check that there is no connection between pins 1 and 6.

(11) Remove the positive line fuse (FS4) and check that: —

(a) there is no positive h.t. at pin 8

(b) there is no potential difference between pins 1 and 7

(c) there is a connection between pins 1 and 6

(d) the negative supply of 75V ± 5V remains between pins 1 and 5 for at least 10 seconds.

Replace FS4.

(12) Remove the negative line fuse (FS5) and check that: —

(a) there is no positive h.t. at pin 8

(b) there is no potential difference between pins 1 and 7

(c) there is a connection between pins 1 and 6

(d) there is no negative supply between pins 1 and 5

Replace FS5.

Relay unit 6009

Insulation resistance

23. With none of the relays energized and using tester, insulation, Type H, check the resistance between the following points and earth: −50V, 1/3, 1/2, 1/1, 2/3, 2/2, 2/1, C, K, PL1/1, PL1/2, PL1/3, PL2/1, PL2/2 and PL2/3. The indicated resistance should be not less than 40 megohms.

Electrical tests

24. (1) Using multimeter Type 1, check that the resistance between PL4/1, PL4/2 and earth is 33000 ohms ± 3300 ohms, between A/B, H/J and earth is 800 ohms ± 160 ohms and between G, N and earth is 1600 ohms± 320 ohms.

(2) Connect the flying leads A/B - H/J, C/K, D/L and G/N from tester (relay unit) to the terminals A/B, C, D and G on the relay unit. Connect the flying leads EARTH and −50v from tester (relay unit) to the corresponding terminals on the relay unit.

(3) Switch on tester (relay unit), turn the selector switch to NIL and, using multimeter Type 1, check that there is no continuity to earth from 1/3, 1/2, 1/1, 2/3, 2/2 and 2/1. Similarly, check that there is no continuity between PL4/1 and PL1/1, PL1/2, PL1/3, PL2/1, PL2/2, PL2/3.

(4) Turn the selector switch on tester (relay unit) to position 1/1. Using multimeter Type 1, check that there is continuity between PL4/1 and PL1/1, also between 1/1 and earth. Check that there is no continuity between PL4/1 and