Proposed new No Break Trigger system

designed by

Chief Technician Colin Hinson

and

Sergeant Tony Mellor

After some 6 years of operation it became apparent that the original No Break Trigger system was a cause of many hours of the station being “off the air”. Tony and I therefore decided that we would have a go at designing a semiconductor version of the (then) current valved system.

We designed what you see in this document between us and solved the problems that cropped up between us so that we both knew how the whole thing worked. The printed circuit boards were designed and made by us using copper plated boards from Vero Electronics who also supplied the 19 inch rack assembly.

Having got the “box” working, we obtained permission to connect it as the trigger source for the Type 85 radar, along with its ancilliary equipments (such as IFF etc). To my knowledge this ran for at least 5 years with no problems.

This document is a modernised version of the original. Scans of the original document are available on this site.

Colin Hinson, Oct. 2017.

SECTION 1 – NEW NBT SYSTEM

General Introduction

1. This paper discusses a design for a No-Break Trigger System which could be utilised at RAF radar stations where a high standard of timing precision and reliability is required. The equipment is capable of working in a wide range of environments and over the temperature range 0.C to 50.C requires no forced air cooling.

NBT System

2. ADRS's are triggered from an NBT equipment developed from early synchronising systems. This equipment has since its introduction been considerably modified in an effort to increase its reliability. However its serviceability still falls short of a working ideal.

3. The new NBT system is introduced in order to improve reliability and service-ability of the trigger system.

General Equipment Description

4. The equipment is mounted on 5 basic types of printed circuit board which are housed in a "Verorack" 19" rack assembly. This rack will mount directly into a 7' Sainsbury cabinet.

5. Power supplies are mounted in the same cabinet and are fed from the A.C. mains supply. Bulk D.C. power supplies are not required.

System Description

6. The equipment contains duplicated crystal oscillators, dividers and trigger output circuits. Each major sub-division of the equipment is mounted on its own printed circuit board. All active auto-changeover components are mounted together on one board, the system may be run manually with all the automatic fault detection circuitry disabled on removal.

7. The input to the system is designed to interface with the PRF control system in the Radar Type 84 MTI equipment.

8. The output triggers are compatible with the trigger inputs to all the equipments currently in use at ADRS's.

9. The existing underfloor mounted pulse distribution unit and the wall mounted pulse indicator panel are not required with the proposed system.

SECTION 2 – SYSTEM SPECIFICATION

PRF — Controlled by crystal stabilised oscillator, fine control by T84 MTI system.

$$\text{Basic PRF} = \frac{\text{Crystal frequency (kHz)}}{16.384} \text{ pps.}$$

PULSE WIDTH — 4uS.

500 Hz REFERENCE — Subdivision of oscillator frequency.

POWER REQUIREMENTS — 5 volts at 3 amperes +/- 5%
40 volts at 1 ampere +/- 5%

OUTPUT TIMINGS — Fixed triggers, referenced to "Zero" trigger.

(1) Zero
(2) -8us.
(3) -125us.
(4) -250us.
(5) -750us.

Delayed triggers, delayed by from 2us to 150us on any of the fixed triggers.

TRIGGERS AVAILABLE

Each delay board gives 4 outputs and each output board gives 6 outputs. The basic system may be extended in multiples of these figures by adding additional pairs of boards.

TRIGGER OUTPUT

Both the delay and the output boards use the same output circuit configuration. The output is capable of producing 100ns rise time triggers at the remote end of 100 meters of UR70 cable. The rise time is only degraded to 250ns when driving 800 metres of low loss cable. The output is open and short circuit proof.

SECTION 3 – BRIEF TECHNICAL DESCRIPTION OF SYSTEM

Refer to Annex

Oscillator Board

1. The 4Mhz oscillator is similar to the one used in the present NBT system, this is so that compatibility between the unti and the external PRF control system may be maintained. The 4Mhz nominal crystal frequency is converted to TTL levels and divided by 16 before leaving the board. The 250 kHz output is routed to both divider boards, the switching between main and standby oscillators is accomplished electronically on the divider boards.

2. A 500 Hz square to sine converter is also housed on this board, this accepts a 500Hz logic level square wave from the in use divider. The 500 Hz sine wave output is routed to the PRF control system.

3. Both the 250 kHz and the 500 Hz signals are checked to ensure correct operation by the fault detection circuit on the board. The output of the fault detector is fed to the control board where it is used to initiate auto changeover in the event of a failure.

4. LEDs indicating “In Use” and “Fault” conditions are mounted on the front panel.

Divider Board

5. The 250 kHz signal from the in use oscillator is divided by a series of bistables down to 250 Hz. Gating circuits accept outputs from individual bistables and generate the six timing pulses.

6. An align facility is provided so that the divider which is not currently in use may be kept exactly in step with the in use divider. This ensures that the output pulses from each board are precisely in line with each other and no timing errors will occur if changeover of divider boards takes place.

7. Each output from the board is monitored and a fault signal is sent to the control board should any output become unserviceable. In addition to the pulse outputs a 500Hz square wave is sent from the in use board to the oscillator.

8. The front panel carries “In Use” and “Fault” indicators.

Output Board

9. Two boards are used simultaneously to provide the output triggers, however the output circuit configuration is such that is one driver fails, the other will continue to function and no loss of triggers will occur.

10. Both dividers feed the output boards, selection of a particular divider is performed by the input gating on the output boards.

11. Each output board has 6 outputs of 35 volts, 4uS wide positive going pulses. Additional triggers are catered for by providing extra pairs of boards. The front panel carries monitor sockets and trigger presence indicators.

Delay board

12. This board accepts the outputs from the dividers and produces delayed triggers 35 volts in amplitude and 4us wide.

13. Each pair of delay boards have their delay circuits cross coupled, this ensures that both board produce outputs at the same time even if one delay has been incorrectly set.

14. The front panel carries monitor sockets, trigger presence indicators and delay controls.

Control board

15. The control board monitors the outputs of every other board within the system and controls the automatic changeover between boards. The power supplies are monitored but since they operate in parallel no switching is necessary.

16. When any fault is detected an alarm signal is generated and a record of
the part of the equipment which failed is kept. This record is in the form of
an LED display on the control panel which is kept lit until reset manually.

Power Supplies

17. Supplies of 5 volts and 40 volts are used within the system. Small modular units are used fed from the 240volts mains supply. Duplicate supplies are paralleled together, this ensures operation without break in the event of supply failure and eliminates the need for switching.

SECTION 4 PART 2 - DIVIDER BOARD.

1. This board accepts three 250Khz inputs, one from each of the two oscillators and one from an external signal source. One of these inputs is selected for use and then divided down to 250Hz by a ten stage binary counter.
2. 6 pulses each 4uS wide are obtained by gating the binary counter outputs, their timings are (with respect to zero and assuming a P.R.F. of 250pps), -1000us, -750uS,
-250uS, -125uS, -8uS, and zero. 5 of those pulses are fed to the Output boards and the Delay boards, the -1000us pulse is used on the control board. The 6 pulses are checked both for presence and correct sequence. An additional check performed on the -1000uS pulse ensures that the P.R.F. of the outputs is of the correct order.
3. The TTL counter has an 'Align' facility, this enables the standby divider to be run in exact synchronism with the in use divider.

Circuit Description

4. The input gating from the Control Panel is used to set bistable IC30c & d. The bistable outputs enable IC15a and allow the oscillator signal through, or enable IC15b allowing the B oscillator through. If SW1a is in the Ext position both IC15a and IC15b are disabled, IC14a, is enabled allowing an external signal to be applied to the divider.
5. The selected input is fed via IC15c to the ripple counter chain which consists of 4 bit binary counter IC9 followed by six JK flip flops IC2, 3, and 4. These flip flops are used in the divide by 2 mode, with their J inputs connected to their !Q outputs and K inputs connected to Q outputs to avoid having to connect them to VCC.
6. The align input is applied to all flip flops and inverted by IC18C before being applied to IC9. A logical 0 on this line will clear the flip flops and the logical 1 from IC18c will clear IC9. SW16 inhibits the align when an external signal is used to drive the divider.

Output Gating Circuit

7. The output gating circuit provides the 4uS wide pulses at the required timings. The Q & !Q outputs of the counter are the inputs to the gating circuit, To minimise the effects of propagation delay through the counter chain Q6 is delayed by passing it through successive stages of inversion in IC5a, b and c. The various triggers are produced in accordance with the truth table below:-

	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12	Q13	Q14
-10000	1	1	1	1	1	1	1	1	1	1
-750uS	1	1	1	1	1	1	0	0	0	0
-2500	1	1	1	1	1	1	0	1	0	0
-1250	1	1	1	1	1	0	1	1	0	0
-8uS	1	0	1	1	1	1	1	1	0	0
0uS	1	1	1	1	1	1	1	1	0	0

SECTION 4 - PART 3 - OUTPUT BOARD

General Description

1. This board accepts three inputs from each divider board at TTL logic levels. Each board produces six 35 volt, 4us positive going triggers. The board is powered from the 5 volt and the 40 volt power supplies.

Circuit Description

2. Input gating The divider A or B selection is carried out on the output board by IC1 and IC2. IC1c and IC2b form a cross coupled NAND bistable whose state depends on the control signal coming from the selector switch SW on the Control Panel. The purpose of this bistable is to ensure that only one divider is selected at one time. When the bistable is in the 'A' position due to a logical 0 at pin 52, a logical 1 is applied to the gating inputs of IC1a, b and d, allowing the input from divider A to pass through the gates. A logical 0 is applied to the gating inputs of IC2a, c and d thereby inhibiting the inputs from divider B. When a logical 0 is applied to pin 53 the gating is reversed, B inputs being allow through and A inputs inhibited.

3. The three outputs of the gating circuit are fed out from the board on pins 51, 56 and 58 and externally wired to the six inputs on pins 41 to 46. Each trigger is buffered and inverted by one element of IC3 and fed to the discrete component trigger driver.

Trigger Driver

Note:- Description is given for trigger driver A, see table for other driver component references.

4. The trigger is fed from IC3a through C1 and R7, C2 to the base of VT1. Diode MR1 prevents the output of IC3c being pulled above 5 volts by C1 charging during switch on.

5. VT1 is normally non-conducting and is driven into conduction by the trigger input. When VT1 conducts, the junction of R8 and R9 is pulled up to the 40 volt rail. Base current to turn an VT2 is supplied through R9. C3 and VT2 form a capacitive discharge circuit into the load. C3 is kept charged by current through R12.

6. Isolating diode MR2 enables the outputs from two boards to be paralleled to provide back-up should one driver fail.

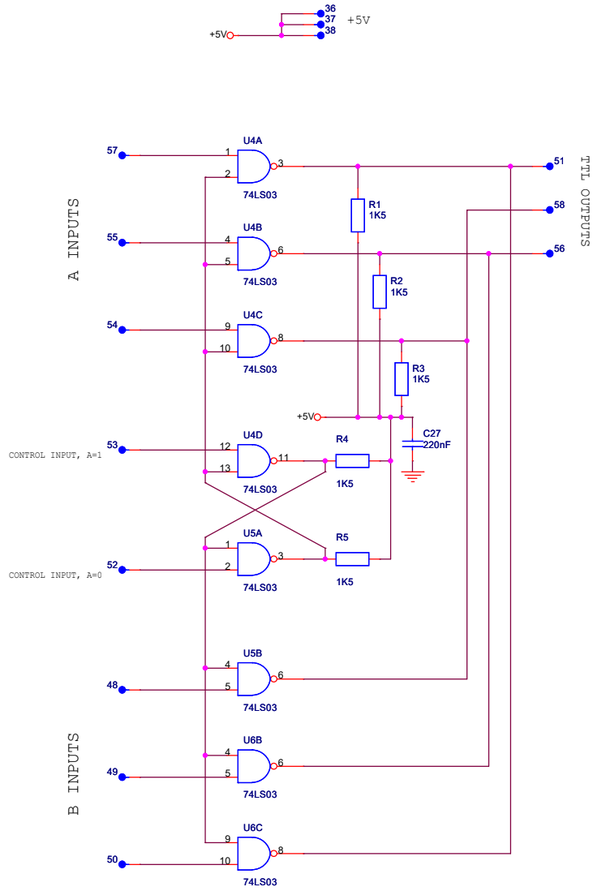
6. A portion of the output is tapped from potential divider R10, R11 and fed to the fault detector IC6b.

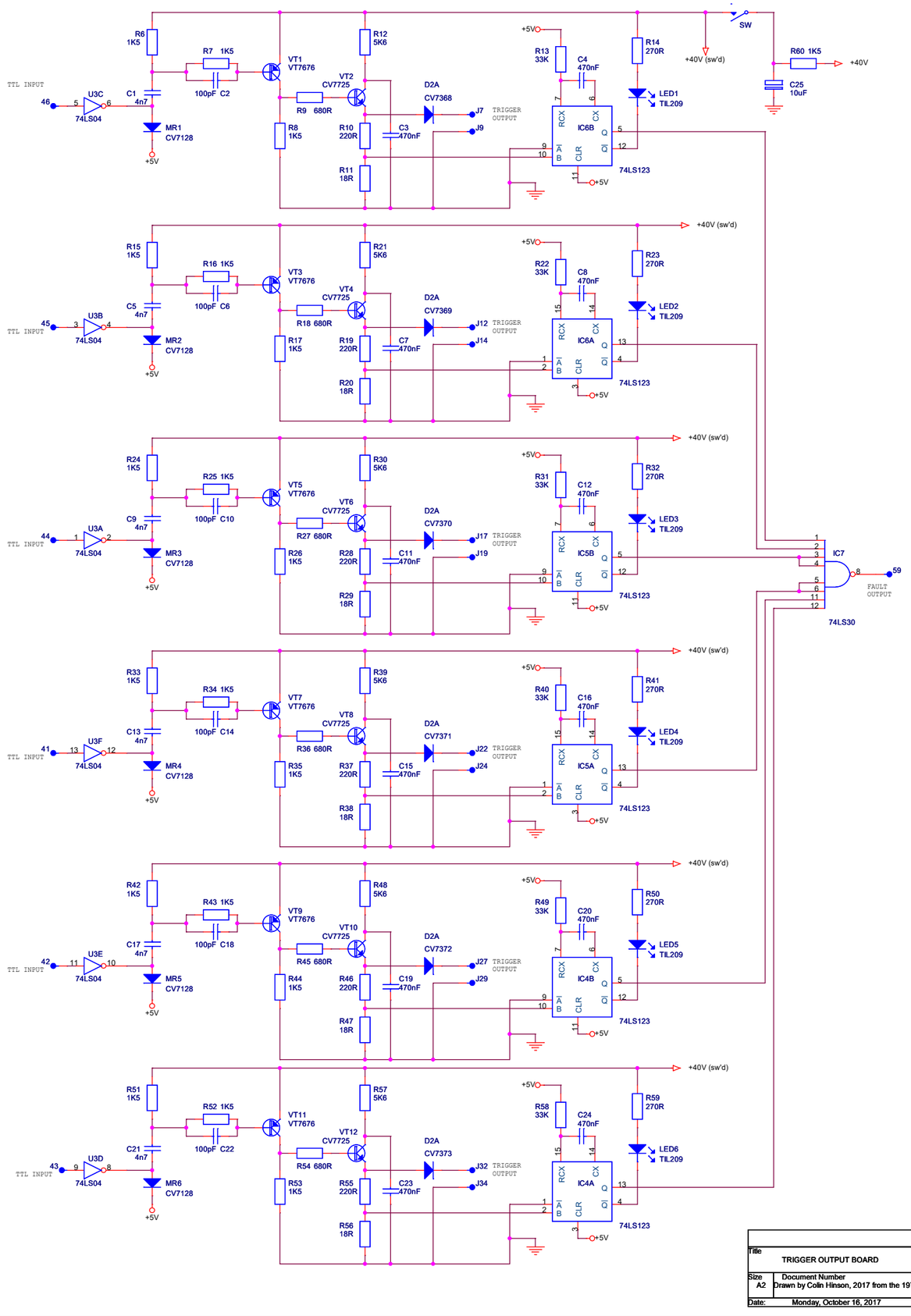
Fault Detector

8. The output trigger sample is fed to the retriggerable monostable multivibrator IC6b which timing period is set by R13 and C4 to be 5mSecs. As the pulse spacing is approximately 4mS the monostable will be retriggered before the completion of its timing cycle. The Q output of IC6b will therefore remain at a logical 1 and the !Q at logical 0, lighting the trigger presence indicator LED1.

9. Should any trigger fail, the appropriate LED will extinguish and the Q of the fault defector will go to logical 0. The presence of a logical 0 at any input of IC7 will cause its output to go to logical 1 signalling a fault to the control board circuitry.

10. Since two separate drivers are simultaneously providing each trigger, no change-over need take place if one trigger driver output fails.





Title	TRIGGER OUTPUT BOARD	
Size A2	Document Number Drawn by Colin Hinson, 2017 from the 1972 document	Rev A
Date: Monday, October 16, 2017	Sheet 1 of 1	

SECTION 4, PART 4 DELAY BOARD

1. The delay boards are operated in tandem in the same way as the buffer boards. If both delays on paired boards are not sot exactly the same it is possible to produce two output triggers on the same line. To prevent this double pulsing an align circuit is used to start the lagging trigger at the same time as the leading edge of the early trigger.

Input Gating

2. The input gating is identical to that used in the buffer board and is not described in detail here.

Delay Circuit (Considering trigger one circuit)

3. The positive edge of the input to IC3A B starts its timing cycle which period is set by Cl, C2, R6 and RV1. When the timing cycle is completed the Q output of IC3A returns to logical 0. This falling edge triggers IC3B which starts its timing cycle which is set to 4uS by R7, C3.

4. The 4uS pulse at the Q of IC3B is fed to the trigger drive amplifier and fault detector circuit identical to that used on the buffer boards.

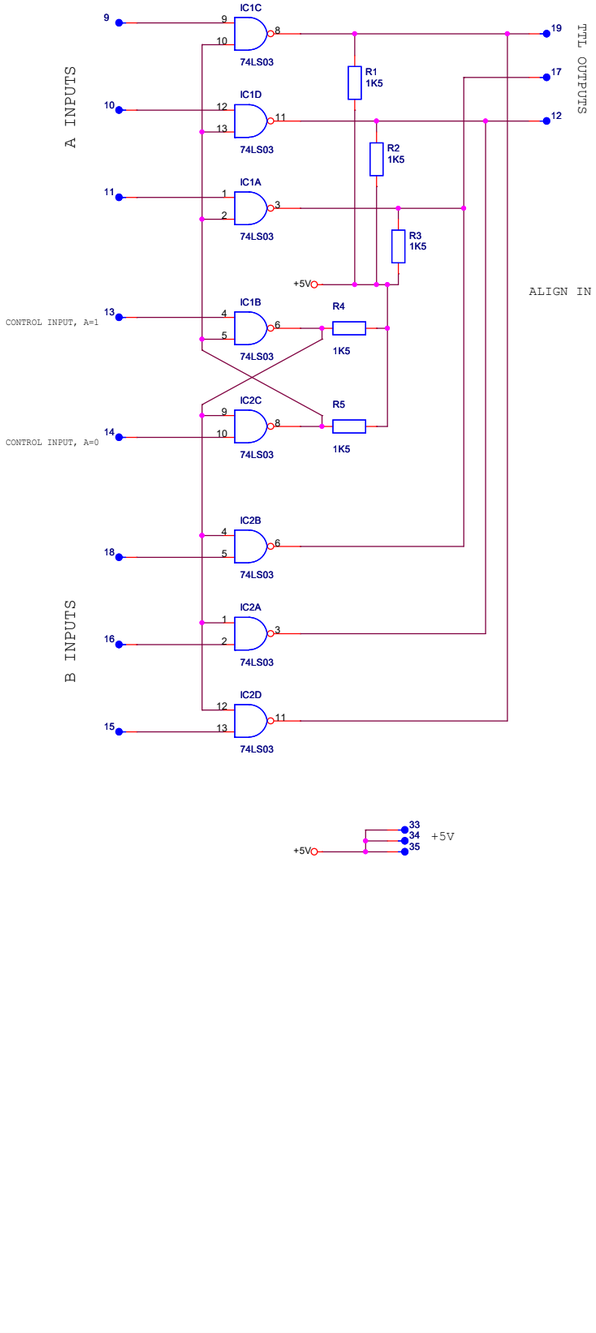
Align Circuit

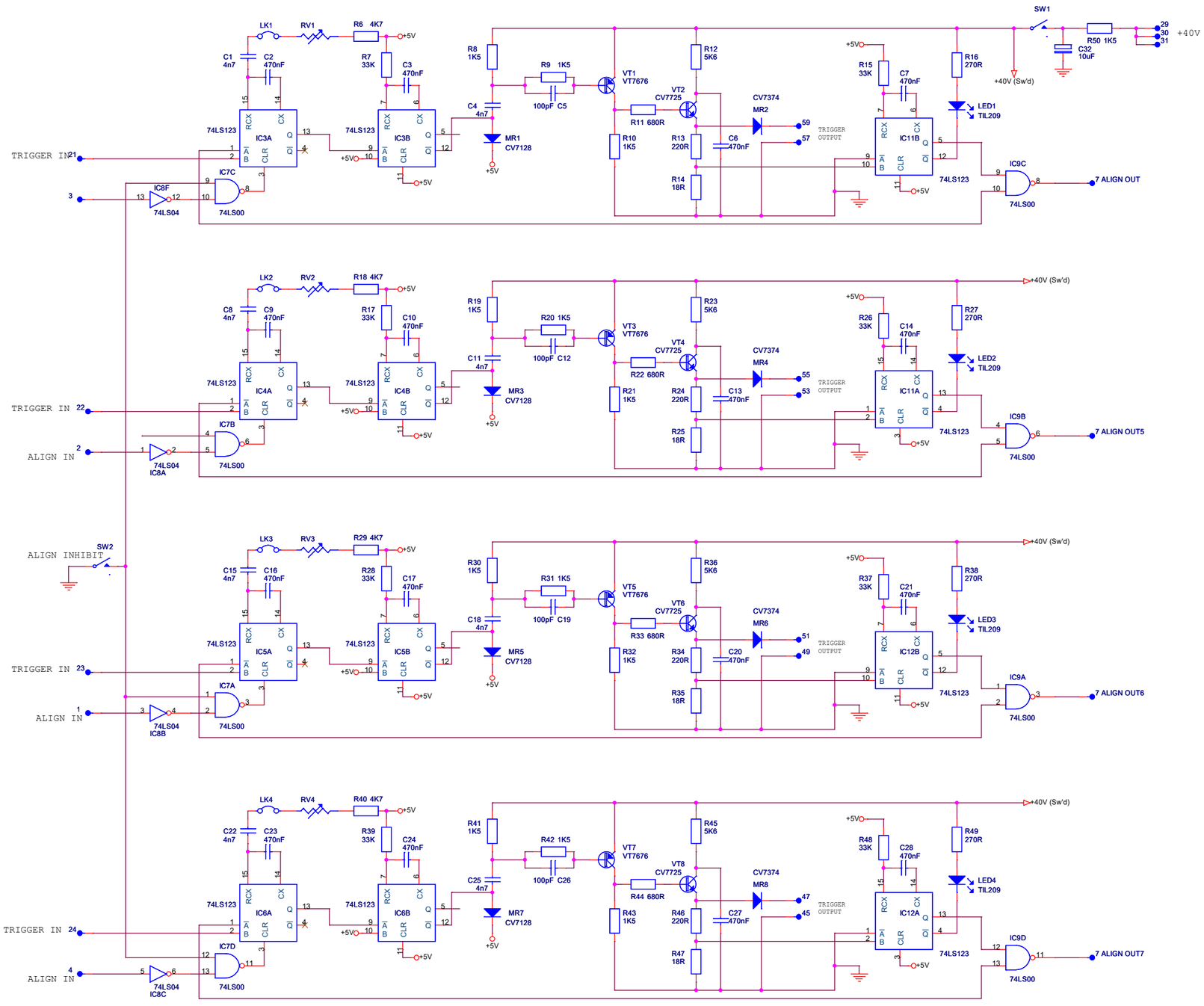
5. The 4uS pulse at IC3B Q, is fed to IC9c. This pulse is allowed to pass through IC9c and leave the board only if the trigger is serviceable. If the trigger is not present then IC11B will be at logical 0 and the align pulse will be inhibited at IC9c.

6. When the align pulse arrives at board B, it is inverted by IC8f and is passed to IC7C. Providing the align is not inhibited the align pulse is fed to the clear input of IC3a. Consider the circuit action when the delay on board B is set longer than that of board A. The align pulse which starts at the leading edge of the trigger from board A clears IC3A on board B. IC3A goes low and initiates the trigger pulse from board B. The align facility is inhibited on one board of the pair when the second is turned off on the control panel.

6. The two fixed ranges of each delay are set by a prewired link adjacent to the timing capacitors C1 and C2.

7. The fault outputs from each delay are commoned in IC10 and fed on the control board.





Title	TRIGGER OUTPUT BOARD	
Size A2	Document Number Drawn by Colin Hinson in 2017 from the 1972 document	Rev A
Date: Monday, October 16, 2017	Sheet 1 of 1	

SECTION 4 - PART 5 - CONTROL BOARD

General Description

1. The Control board contains the logic required to decide which part of the trigger system is serviceable, and in the case of the dividers and oscillators ensures that the in use boards are serviceable. Should an output board not be serviceable, the control board will indicate this, but do nothing about it.

2. This board also contains the logic required to align the dividers, and the pulse generator required to reset its own fault latches and those of the dividers and oscillators.

3. The conditions set by the control board may be manually over-ridden by the switches on the control panel.

Circuit Description

4. Oscillator Control The fault lines from Oscillators A and B are fed into the Board on pins 55 and 57 respectively to IC15a. These lines are at logical 0 for no fault and logical 1 for fault. When an oscillator fault occurs IC15a output goes to logical 0 and sets the fault latch formed by IC19a and b which in turn lights the oscillator fault LED and via IC17 the overall fault LED (and rings the bell).

5. The fault input lines also feed IC5e and IC5f which invert the logic to give a logical 0 as a fault. The output of IC5e is fed to IC5c and the K input of IC3a. The K input of IC3a going to logical 0 ensures that when IC3a is clocked, its Q will go to logical 0 and its !Q to logical 1 (this selects B oscillator as in use). The output of IC5c going to logical 1 causes the input to IC4c to go to a logical 1 for a time dependent upon C2 and R2. If IC4c's other input is at logical 1 at this time (i.e. oscillator A in use) its output will go to logical 0 for about luS. This pulse is fed via IC4b to the clock input of IC3a which causes IC3a Q to go to logical 1 which selects B Oscillator as in use, as mentioned above. Should the B oscillator already have been in, use when the A went faulty then IC4c will be inhibited (IC3a !Q at logical 0) and the only effect will be to operate the fault latch. In the case where one oscillator is faulty and the other goes faulty, both the J and K inputs to IC3a will be at logical 0 when it is clocked and so no change-over will take place. The 2 outputs of IC3a are fed via open collector inverters and the control panel switches to control the input gating on the divider boards. Open collector inverters are used in this position to allow the control lines to be grounded by a manual control switch on the control panel. The circuit action for the B oscillator going faulty is similar to that described above for the A side.

Divider control

6. The control circuit for the dividers is identical to that for the oscillators and the above description applies. The only exception is that the output has more drive capacity (three inverters in parallel) to allow it to feed a large number of output and delay boards. The pull up resistors are mounted on the control panel.

Alignment Control

7. If the standby divider is not in step with the In use divider, the -1000uS pulse from the in use divider is used to bring into alignment the standby divider IC15b and c, IC13c and IC14a and d form the gating circuit which extracts the -1000uS pulse from the in use divider and feeds it as an align pulse to the standby divider should the two dividers not be in step. Should 2 consecutive align pulses occur, bistable IC28a and b is set by the second of those align pulses. The output of IC28b presents a fault signal to the overall fault detector IC17.

Fault Reset

8. The operation of SW3 is fed as a clean signal to pulse generator circuit C5, R5 via the de-bouncer IC20a and b. The exponential signal is transformed into a square wave by IC18a and fed as a 10uS reset signal to the fault latches throughout the system.

Output Fault Circuit

9. Should a fault occur in any one of the output circuits, a logical 1 will be present at one of the inputs of IC25 or IC30. The logical 1 signal at the combined output of 1C25 and 1C30 is inverted twice by 1029 c and e and leaves the board to light the output fault LED. When a fault occurs the output fault latch IC28c and d will be set by the pulse from the pulse generator C6, R6 and IC29a. In order to avoid the masking of important faults by minor (output) faults, provision is made to allow the output fault latch to be reset even though the output fault still persists, however in this situation the output fault LEDs remain lit when the overall fault LED is extinguished.

Overall Fault

10. The outputs from the individual fault latches are fed to IC17 where they are commoned to provide an overall fault signal. This is inverted by IC13b and fed from the board to light the overall fault LED.

Osc. or Div	Osc.or Div B	
'S'	'S'	Select either for use.
Fault	'S'	Select B for use and operate fault latch
'S'	Fault	Select A for use and operate fault latch
Fault	Fault	operate fault latch

ALIGN

Divider A	Divider B	
In use	aligned	Do nothing
In use	mis-aligned	Apply a pulse tined at -1000uS to the align input of Divider B
Aligned	In use	Do nothing
Mis-aligned	In use	Apply a pulse timed at -1000uS to the align input of Divider A
More than one successive pulse applied to either align input.		Operate alignment fault latch and light the fault LED
Output fault		Operate overall fault latch with pulse and light output fault LED.

FAULT I/Ps FROM OUTPUT AND DELAY BOARDS

+5V
R7 1K
EC20 IC25A 74LS05
EC18 IC25F 74LS05
EC16 IC25E 74LS05
EC14 IC25D 74LS05
EC11 IC25B 74LS05
EC10 IC25C 74LS05
EC9 IC30A 74LS05
EC8 IC30F 74LS05
EC6 IC30E 74LS05
EC5 IC30B 74LS05
EC4 IC30D 74LS05
EC3 IC30C 74LS05

IC29B 74LS04 → IC29C 74LS04 → EC23 OUTPUT FAULT

IC29D 74LS04 → C6 100nF → IC29A 74LS04 → R6 1K
IC29A → IC28D, IC28C (74LS00) → OUTPUT FAULT

'B' OSC. FAULT → EC57 → IC5F 74LS04 → IC5B 74LS04 → C1 100nF → IC4D (74LS00)
'A' OSC. FAULT → EC55 → IC5E 74LS04 → IC5C 74LS04 → C2 100nF → IC4C (74LS00)
IC15A 74LS02 (EC57, EC55) → R1 1K, R2 1K
IC4D, IC4C → IC4B (74LS00)

IC4B → U3A 74LS76 (J, K, CLK, PR, CL, Q, Q̄)
U3A Q → IC8E 74LS04 → EC43 A=1
U3A Q̄ → IC8D 74LS04 → EC44 A=0
EC56 OSC. MANUAL 'A'
EC58 OSC. MANUAL 'B'
DIVIDER I/P CONTROL

OUTPUT FAULT → IC17A 74LS22 → IC13B 74LS04 → EC26 SYSTEM FAULT
OSCILLATOR FAULT → IC19B, IC19A (74LS00) → EC24 OSCILLATOR FAULT
DIVIDER FAULT → EC28 FAULT RESET
FAULT RESET → IC19C, IC19D (74LS00) → EC25 DIVIDER FAULT

'B' DIV. FAULT → EC61 → IC10F 74LS04 → IC10B 74LS04 → C3 100nF → IC9D (74LS00)
'A' DIV. FAULT → EC62 → IC10E 74LS04 → IC10C 74LS04 → C4 100nF → IC9C (74LS00)
IC15D 74LS02 (EC61, EC62) → R3 1K, R4 1K
IC9D, IC9C → IC9B (74LS00)

IC9B → U3B 74LS76 (J, K, CLK, PR, CL, Q, Q̄)
U3B Q → IC7A, IC7B, IC7C 74LS04 → EC45 A=2
U3B Q̄ → IC7E, IC7F, IC8A 74LS04 → EC46 A=1
EC59 DIV. MANUAL 'A'
EC60 DIV. MANUAL 'B'
O/P BD'S I/P CONTROL

ALIGN FAULT

ALIGN TO 'A' DIVIDER EC31
O/P BOARD I/P CONTROL, A=1 EC35
'B' -1000uS EC32
'A' -1000uS EC34
O/P BOARD I/P CONTROL, A=0 EC33
ALIGN TO 'B' DIVIDER EC30
IC15B 74LS02, IC14D 74LS00, IC13C 74LS86, IC15C 74LS02, IC14A 74LS00 → IC14B 74LS00

+5V, IC24A 74LS74 (D, CLK, Q, Q̄), +5V
IC14C 74LS00 → IC28A, IC28B 74LS00 → EC27 ALIGN FAULT

FAULT RESET SWITCH (NORMALLY MADE) EC22
FAULT RESET SWITCH (NORMALLY OPEN) EC29
IC20B, IC20A 74LS00 → C5 100nF → IC18A 74LS04 → R5 1K
FAULT RESET

Title	NEW NBT CONTROL BOARD CIRCUIT	
Size A3	Document Number DRAWN BY COLIN HINSON IN 2017 FROM A 1972 DOCUMENT	Rev A
Date: Monday, October 16, 2017	Sheet 1 of 1	

SECTION 4 - PART 6 - RACK WIRING INTERCONNECTIONS

Osc A	Osc B	Cont Bd	Cont Pan	Div A	Div B	0/P A	0/P B	Delay A	Delay B	Signal Description
		3z							40a	Delay B fault
		4z						40a		Delay A fault
		5z					59a			Output B fault
		6z				59a				Output A fault
		8z								)
		9z								) Spare fault input lines
		10z								) to Control Board
		11z								)
		14z								)
		16z								)Grounded when not used
		18z								)
		20z								)
56z	56z	21a		5z	5z					Fault latch reset pulse
		22z	a							Fault latch reset Switch (Norm made)
		23a	z							O/P fault Led. drive
		24a	z							Oscillator fault LED drive
		26a	z							Overall fault LED drive
		27a	z							Alignment fault LED drive
		28a	z							Divider fault LED drive
		29z	a							Fault reset switch(Norm. broken)
		30a			21z					Divider B align pulse
		31a		21z						Divider A align pulse
		32z			23a					Divider B -1000uS pulse
		33z	a		55z	52z	52z	13z	13z	Buffer i/p control (Sw'd) A=0
		34z		23a						Divider A -1000uS pulse
		35z	a	55z		55z	53z	14z	14z	Buffer i/p control (Sw'd) A=1
		40a	z							Buffer i/p control (Unsw) A=1
		41a	z							Buffer i/p control (Unsw) A=0
		43a	z							Divider i/p control (Unsw) A=1
		44a	z							Divider i/p control (Unsw) A=0
		46z		13a						Divider L fault
		48z			13a					Divider B fault
		50z	a							Divider Manual A
		51z	a							Divider Manual B
58a		55z								Oscillator A fault
		56z	a							Oscillator Manual A
	58a	57z								Oscillator B fault
		58z	a							Oscillator Manual B
	54z		a	34z	34z					Divider i/p (Sw'd) A=0
54z			a	41z	41z					Divider i/p control (Sw'd) A=1
	57a			32z	32z					250kHz - Oscillator B
57a				33z	38z					250KHZ - Oscillator A
				29a						-750uS - A)
					29a					-750uS - B)
				25a						-250uS - A)
					25a					-250uS - B)
				3a						-125uS - A)Inverted pulse o/p's
				11a	3a					-125u8 - B) at TTL logic level.
					11a					-8uS - A) To be wired as req'd.
										-8uS - B) to O/P & delay boards
				9a						0uS - A)
					9a					0uS - B)
			z	27a						Scope trigger (-1000uS)
			z		27a					Scope trigger (-1000uS)
			a					38		Inhibit align A delay
			a						38	Inhibit align B delay

Rack Wiring Interconnections (Continued)

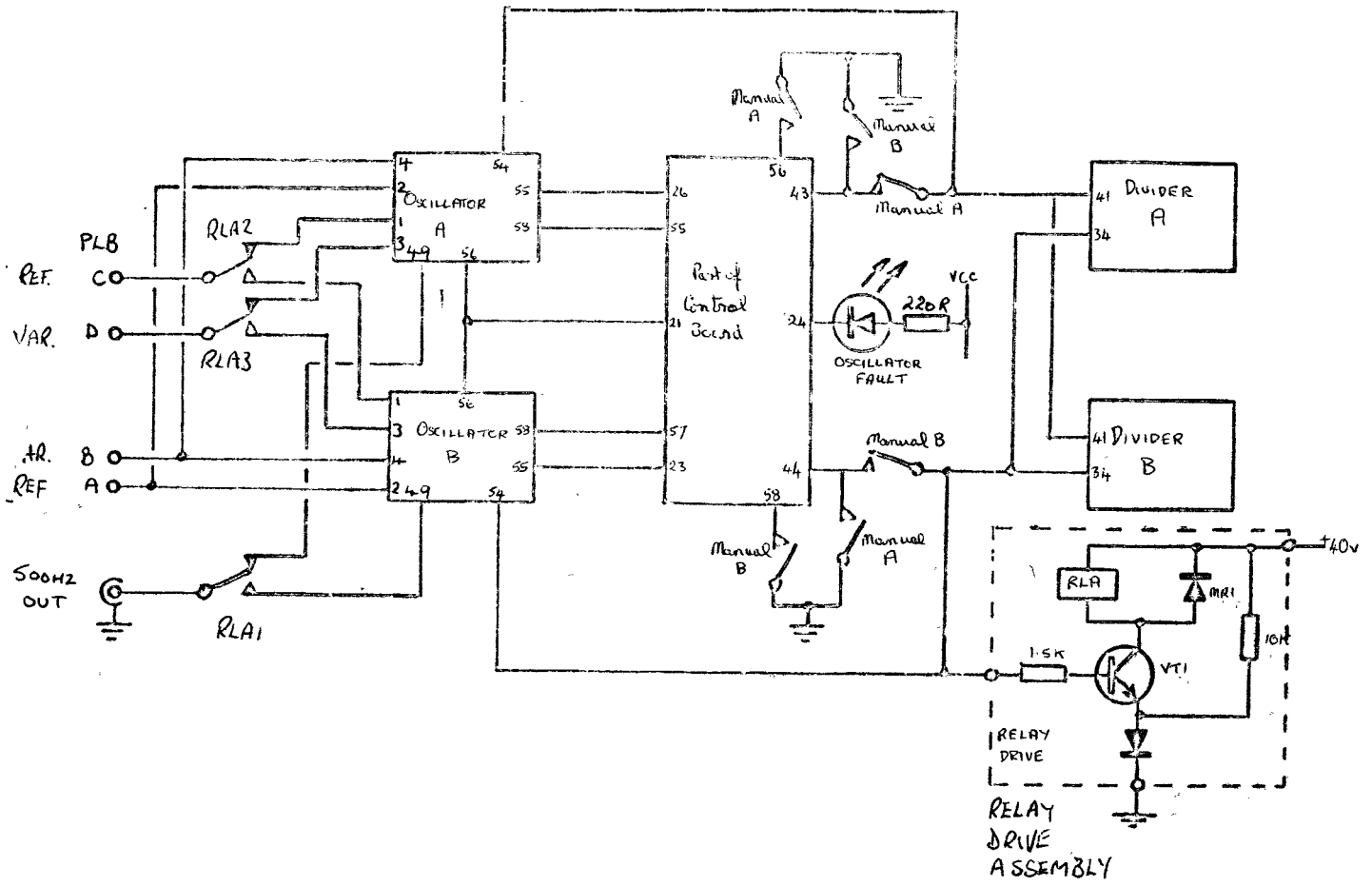
Osc A	Osc B	Cont Bd.	Cont Pan.	Div A.	Div B	O/P A	O/P B	Del A	Del B	Signal Description
49a			z							500Hz (to RLA)
48z	49a		z	15a	15a					500Hz (to RLA)
	48z									TTL 500Hz - parallel source
								1z	5a	Delay output align for trigger No. 2
								2z	6a	Delay output align for trigger No. 3
								3z	7a	Delay output align for trigger No. 1
								4z	8a	Delay output align for trigger No. 4
								5a	1z	Delay output align for trigger No. 2
								6a	2z	Delay output align for trigger No. 3
								7a	3z	Delay output align for trigger No. 1
								8a	4z	Delay output align for trigger No. 4
								9z	9z	B input No 3)
								10z	10z	B input No 2) Wire as required to
								11z	11z	B input No 1) the Divider inverted
								15z	15z	A input No 1) pulse outputs.
								16z	16z	A input No 2)
								13z	18z	A input No 3)
								12a		Selected output No 1)
									12a	Selected output No 1) Wire as
								17a		Selected output No 2) required to
									17a	Selected output No 2) input pins
								19a		Selected output No 3) 21-24 on the
								21z.	19a	Selected output No 3) same board,
										TTL input for Delay A output No 1
									21z	TTL input for Delay B output No 1
								22z		TTL input for Delay A output No 2
									22z	TTL input for Delay B output No 2
								23z		TTL input for Delay A output No 3
									23z	TTL input for Delay B output No 3
								24z		TTL input for Delay A output No 4
									24z	TTL input for Delay B output No 4
						48z	48z			B input No. 1) Wire as required to
						49z	4z			B input No. 2) the Divider
						50z	50z			B input No 3) inverted pulse
						54z	54z			A input No 3 }outputs.
						55z	55z			A input No 2)
						57z	37z			I input No 1)
						51a				Selected output No 1) Wire as
							51a			Selected output No 1) required to
						56a				Selected output No 2) input pins
							56a			Selected output No 2) 41-46 on
						58a				Selected output No 3) the same
							38a			Selected output No 3) board.
						41z				TTL input for O/P A output No 4
							41z			TTL input for 0/P B output No 4
						42z				TTL input for O/P A output No 5
							42z			TTL input for 0/P B output No 5
						43z				TTL input for O/P A output No 6
							43z			TTL input for O/P B output No 6
						44z				TTL input for 0/P A output No 3
							44z			TTL input for O/P B output No 3
						45z				TTL input for O/P A output No 2
							45z			TTL input for 0/P B output No 2
						46z				TTL input for O/P A output No 1
							46z			TTL input for 0/P B output No 1

Rack Wiring Interconnections (Continued)

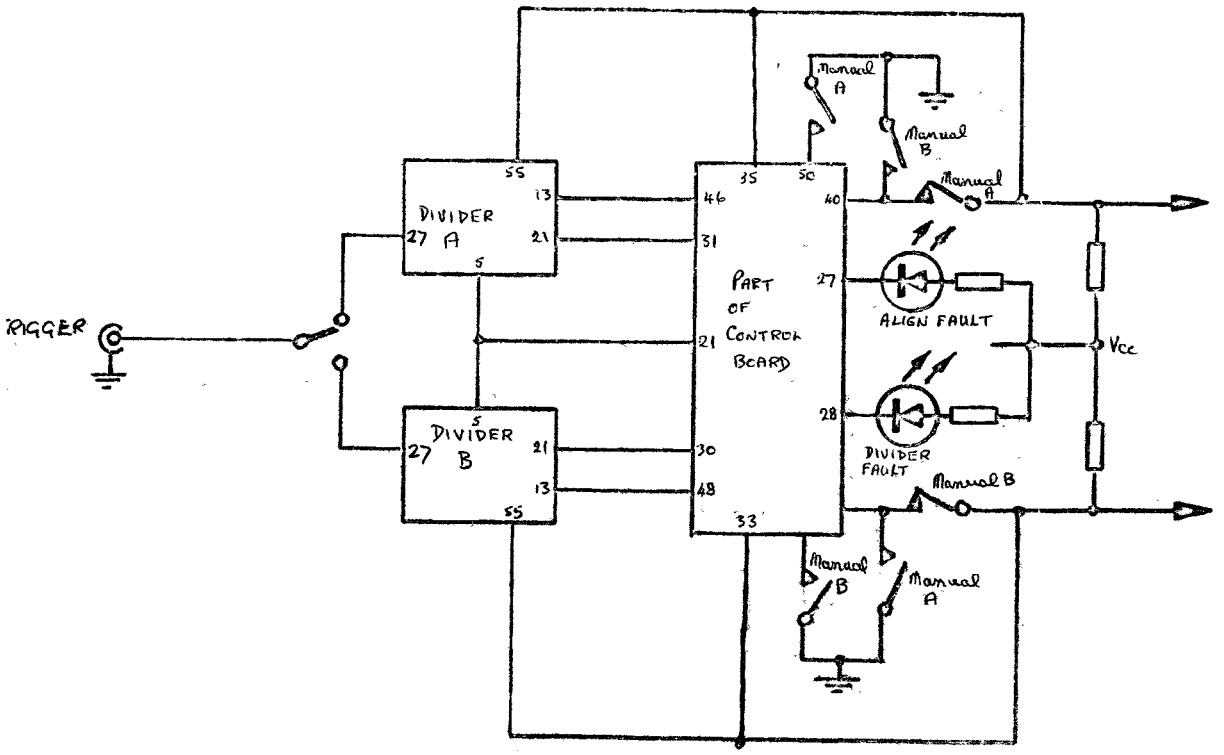
Osc A	Osc B	Cont Bd	Div A	Div B	O/P A	O/P B	Del A	Del B	Power Rail	
50-2	50-2								+5volts	
42-4	42-4								+40volts	
8	8								+5volts (screened)	
1										500Hz (Sw'd) Ref, phase.
	1									500Hz (Sw'd) Ref. phase.
2	2									500Hz Ref. phase return
3										500Hz Variable phase (Sw'd)
	3									500Hz Variable phase (Sw'd)
4	4									500Hz Variable phase return
			59/60	59/60					+5volts	
			1/2	1/2					Ground	
		59/60							+5volts	
		1/2							Ground	
			2-4							+40volts (Switched)
				2-4						+40volts (Switched)
						36-8	36-8		+5volts	
			1/2	1/2					Ground	
						29-31				+40volts (Switched)
							29-31			+40volts (Switched)
						37-8	37-8		+5volts	
						25-7	25-7		Ground	
					7	7				Fixed trigger output No :
					9	9				Screen for above
					12	12				Fixed trigger output No 2
					14	14				Screen for above
					17	17				Fixed Trigger output No 3
					19	19				Screen for above
					22	22				Fixed trigger output No 4
					24	24				Screen for above
					27	27				Fixed trigger output No 5
					29	29				Screen for above
					32	32				Fixed trigger output No 6
					34	34				Screen for above
							59	59		Delayed trigger output No 1
							57	57		Screen for above
							55	55		Delayed trigger output No 2
							53	53		Screen for above
							51	51		Delayed trigger output No 3
							49	49		Screen for above
							47	47		Delayed trigger output No 4
							45	45		Screen for above

RACK INTERCONNECTION DIAGRAM
(CONTROL)

ANNEX A TO
SECTION 4
PART 6

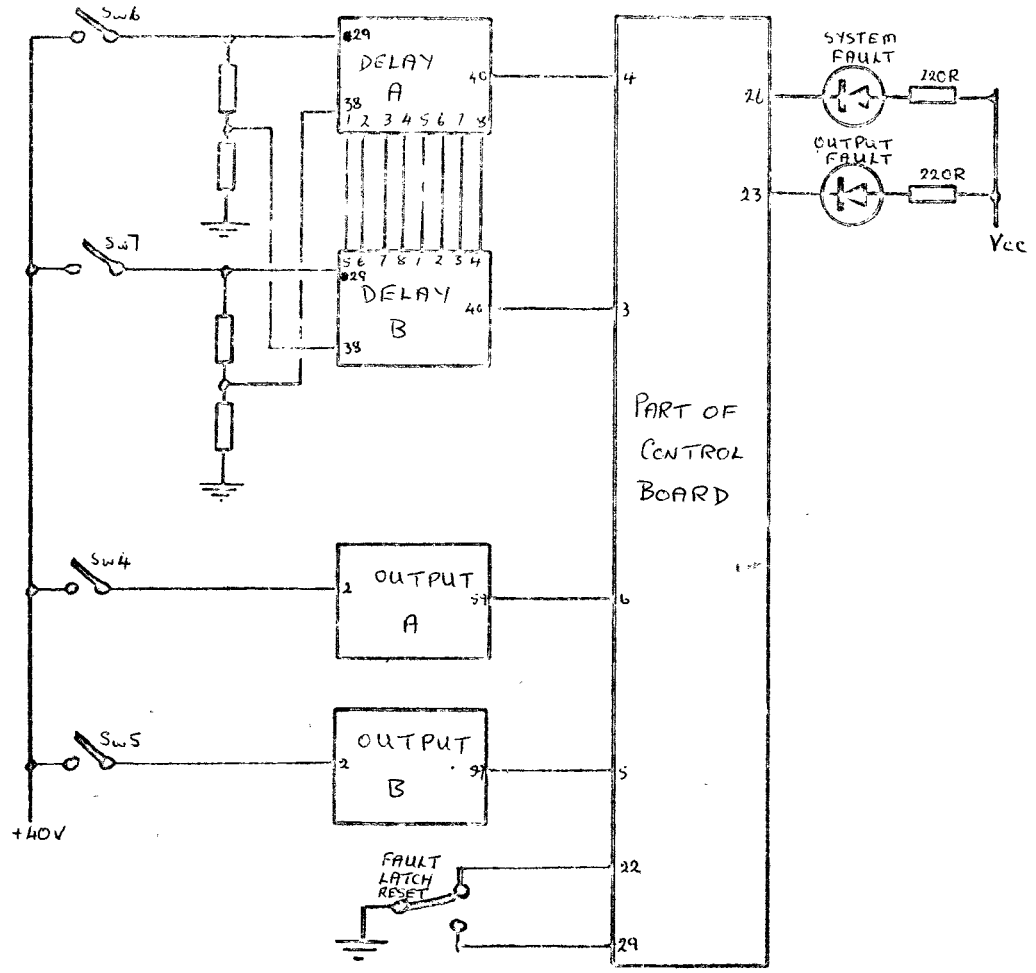


RELAY DRIVE ASSEMBLY



INPUT CONTROL WIRES TO OUTPUT AND DELAY BOARDS.

RACK INTERCONNECTION DIAGRAM
(PCW CP)



PLA B → +5v SCREENED

G, H, J, K → +5v (Vcc)

C, D, E, F → +GROUND (GND)

L, M → +40v