AP115H-0103-1A1

(Formerly AP115H-0103-1
Sections 1 to 4)

RADAR TYPE 84

DESCRIPTION OF SIGNAL PROCESSING EQUIPMENT

Service users should send their comments through
the channel prescribed for the purpose in:
AP 100B-01, Order 0504

WARNING

RADIATION HAZARDS

KEEP AWAY FROM RADAR AERIAL DURING TRANSMISSION

AVOID EXPOSURE AT AERIAL HEIGHT WITHIN TRANSMISSION ZONE

SEE LEADING PARTICULARS FOR SAFETY LIMITS

DO NOT STARE AT DISCHARGE TUBES

HIGH VOLTAGES

REMEMBER-APPARATUS IS SAFE-ONLY IF YOUR APPROACH IS CORRECT

1 This publication is now RESTRICTED. New or revised leaves will carry the new grading. AL4 called for the markings on pages already issued to be altered to read RESTRICTED and the CD captions to read AP. Holders must ensure that these alterations have been made before the publication or any part of it is disposed of as waste.

2 This publication was recodified at Amendment 12 of Oct. 1979. For reasons of economy, pages will retain the original code until changed by future amendments.

3. Changes of technical import are identified by the amendment indicator symbol '▶...◀' or 'x...x'

Amdt 14.

ASSOCIATED PUBLICATIONS

RADAR TYPE 84

Leading particulars and general information	CD 115H-0101-1
Description of radar head	AP 115H-0102-1A1 and AP 115H-0102-1A2
Description of signal processing equipment	AP 115H-0103-1A2
Special-to-type test equipment	AP 115H-0104-1
Functional diagrams	AP 115H-0105-10
Aerial mount and turning gear	AP 115J-0100-1 (AP 2886H)

CONTENTS

CONTENTS (Cont.)

SECTION 1

DESCRIPTION OF SIGNAL PROCESSING

(C784575)

Chapter 1

PRINCIPLES OF SIGNAL PROCESSING

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

Introduction

1. The term *signal processing* embraces the methods employed in order to obtain a radar display showing the maximum number of targets both in clear conditions and in the presence of clutter or jamming. Owing to the high power of modern radar systems, the presence of clutter might often make a display virtually useless without the use of some form of signal processing. Ground clutter echoes have been observed with a strength of up to 70 dB above noise and the returns from heavy rain are commonly 30 to 40 dB above noise. Angels may be troublesome up to at least 80 miles from the station and in abnormal conditions anoprop (anomalous propagation) has been observed at ranges up to 320 miles.

2. Clutter may consist of ground clutter or permanent echoes (such as those obtained from buildings or topographical features), sea clutter, precipitation returns (rain), angels or anoprop. Jamming may be either deliberate or accidental and includes pulse interference, noise, c.w. or carcinotron jamming and window. Although window is a form of deliberate jamming, the signal processing treatment is the same as that employed for slow-moving clutter such as precipitation.

3. The facilities which may be employed to suppress the various forms of clutter and interference are:—

(1) Circular polarization

(2) Swept gain

(3) Logarithmic amplification with pulse length discrimination (log + PLD)

(4) Pulse repetition frequency discrimination (PRFD)

(5) Moving target indication (MTI)

(6) Dicke Fix receiver (anti-noise jamming receiver).

4. Each of the facilities listed has its particular advantages but may also suffer certain limitations. It is therefore necessary to employ the best combination of facilities to suit the prevailing conditions. Of these facilities, MTI has the advantage that it can give a measure of sub-clutter visibility in normal conditions, i.e. targets may be seen in clutter even when their echo strength is less than that of the clutter. Returns from heavy rain may be of such a strength that the difference in amplitude between rain and target returns is greater than the sub-clutter visibility of the system. The use of circular polarization under these circumstances reduces the strength of rain returns by a greater amount than target returns so that the sub-clutter visibility of the system is sufficient to allow target returns to be seen. This does not necessarily apply to the other methods of signal processing. However, a conventional MTI system suffers from loss of targets due to blind velocities and blind phases (*para.* 40 *et seq.*), this loss occurring whether clutter is present or not. It is therefore desirable that MTI should only be used where the presence of clutter makes it necessary. Doppler compensation may be applied to the MTI circuits, in which case use is made of the blind velocities phenomenon to discriminate against moving clutter such as rain or window.

5. The use of a logarithmic amplifier followed by pulse length discrimination gives a degree of protection against certain forms of jamming and against permanent echoes but gives no measure of sub-clutter visibility. This type of signal processing, however, does not suffer from loss of targets due to blind velocities and may therefore be used in areas where the use of MTI is not necessary. It is therefore helpful to use a method of video switching whereby MTI is applied to the display in areas of bad clutter with a background of logarithmic, pulse length discriminated video. The switching is carried out electronically so that MTI video is applied to the whole of a particular area or it may be applied within the area by a process known as clutter switching. In the latter method, the use of MTI is confined almost exactly to the area in which clutter exists.

6. Circular polarization and swept gain may be used at the discretion of the operator but since their use causes a loss in the sensitivity of the system these facilities are used only when necessary.

7. A further facility is provided which discriminates against certain types of interference whose pulse repetition frequencies are not locked to the radar transmitter. This facility is known as p.r.f. discrimination and is best applied to follow any other forms of signal processing.

8. Interference pulses of short duration, such as would be received from a carcinotron jammer, may be reduced in amplitude by the use of a Dicke Fix type of radar receiver incorporating a filter with a bandwidth applicable to the transmitter pulse. The filter follows the limiting circuits, so that the shape of such interference pulses is considerably modified and their amplitude limited to be the same as that for normal radar signals. Provision is made for the signal processing equipment to accept either the input from such a receiver or that from a normal radar receiver.

TYPES OF CLUTTER AND INTERFERENCE

Ground clutter

9. Local topographical features return echoes to the radar which appear on the display as a solid patch of light. Since these returns may be of a strength sufficient to saturate the system, target echoes, although possibly much stronger than the clutter echoes, may not appear on the display. Circuits to alleviate this condition may do so either by reducing the amplitude of the clutter signal within the receiver to a level below the saturation limit (so that target signals superimposed on the clutter appear on the display) or by discrimination against signals with a duration longer than that of the transmitted pulse. Such circuits may therefore include MTI, instantaneous automatic gain control and logarithmic amplification with or without pulse length discrimination or swept gain.

Sea clutter, rain, angels and window

10. The term moving clutter is used generally to embrace all forms of clutter in which the returns are received from such objects as sea waves and rain clouds. The treatment for such returns, which affect the display in a similar manner, is the same as that for stationary clutter except that Doppler compensation should be associated with the MTI circuits.

Pulse interference

11. Pulse interference may be either deliberate or accidental and takes the form of pulse reception at a p.r.f. non-synchronous with the transmitter p.r.f. This type of interference may be eliminated by the use of a p.r.f. discrimination circuit.

C.W. jamming

12. C.W. jamming is characterized by an overall brightening of all or a part of the display. Since the pulse length discrimination facility eliminates pulses of more than twice the transmitted pulse length, the facility is also effective against this type of jamming.

Noise jamming

13. Noise jamming is described as a continuous transmission modulated by noise. Measures effective against this type of jamming are, in order of

efficiency, a Dicke Fix type radar receiver, logarithmic amplification or noise-operated a.g.c.

Carcinotron jamming

14. This type of jamming consists of a frequency modulated signal which sweeps through the receiver bandwidth and produces pulses of short duration and large amplitude. This type of interference is reduced by a Dicke Fix type receiver.

METHODS OF ELIMINATING CLUTTER AND INTERFERENCE

15. The signal processing system employs a video switching arrangement whereby the appropriate combination of the various facilities can be selected to suit the prevailing conditions. Certain of the available facilities (such as circular polarization, swept gain and area of blind velocity band) are under the control of an operator provided with monitor consoles whereon the effect of the various facilities can be assessed. These facilities are briefly described in this chapter, together with their relative advantages and disadvantages. Details of the circuits employed are given in other sections of this Part of the handbook.

Circular polarization

16. A facility is available whereby the radar aerial may be set for circular polarization. This facility does not form part of the signal processing system but since its operation is under the control of the signal processing controller its effects are briefly mentioned here. The facility is estimated to reduce the strength of rain echoes by about 18 dB, with a loss of target echo strength of 3 to 5 dB according to the aspect of the target. A gain of visibility in conditions of precipitation is thus obtained. Circular polarization affects the whole display area regardless of the methods of subsequent signal processing in use and therefore provision is made to switch it off when maximum sensitivity is required. With heavy rain 40 dB above noise masking a target 20 dB above noise, a sub-clutter visibility of 20 dB is required for the target to be visible and this is not achieved by MTI. However, under these conditions, circular polarization reduces the rain to +22 dB and the target to +15 dB, so that the required sub-clutter visibility is rather more than 7 dB and this lies within the capabilities of MTI. The use of circular polarization in conjunction with MTI under these circumstances makes a target visible in conditions of heavy precipitation whereas with either of these facilities on its own the target would not be seen.

Swept gain

17. Ground clutter, sea clutter and angels are normally at their strongest in a limited area round the station and it is therefore useful to attenuate signals over a limited range. Such attenuation is applied according to a law chosen to suit the characteristics of a particular aerial. It is inevitable that the use of swept gain must cause the loss of some weak targets but is sometimes the only effective means of reducing the returns from angels as the velocities of the latter may be too random for cancellation by doppler-compensated MTI.

18. For an MTI channel swept gain is applied to an amplifier stage in the i.f. circuits. This is not possible in a channel employing logarithmic amplification owing to the non-linear response obtained. The desired attenuation is therefore obtained in the video circuits immediately following the logarithmic i.f. amplifier and before the pulse length discriminator. As noise jamming causes a loss of signal to noise ratio (even though the screen may remain clear) arrangements may be made to decrease the swept gain by an equal amount in order to avoid loss of targets due to two causes acting at the same time.

Noise-operated a.g.c.

19. It is useful to protect a signal channel against noise jamming by the use of noise operated a.g.c. The system used is that in which the number of noise spikes occurring between two specific voltage levels are counted, after detection. The resulting count, after integration and amplification, provides an a.g.c. voltage which operates on a swept gain amplifier stage via an OR gate to which the swept gain waveform is also applied. The larger of the two bias voltages determines the gain of the stage. Counting of the noise spikes takes place over the second half of the trace, i.e. after 2 milliseconds, as otherwise the a.g.c. circuit would be operated by clutter.

Instantaneous automatic gain control

20. An instantaneous automatic gain control system operates in such a manner as to preserve gain control for a desired pulse but at the same time reduces the response to large signals. The occurrence of a long pulse, such as an extended ground clutter echo, biases back the amplifier and it remains sensitive to sharp variations in the echo amplitude such as those produced by target returns. Circuit time constants are chosen to give the best effect and the gain is restored very quickly after the end of the extended pulse.

21. For any individual i.f. stage there is a level of input such that any increase produces no further change in output. If the level of the interfering carrier at the grid of the stage is in the region of no change in output, the signal pulse superimposed on the interference envelope will be lost. This loss may be offset by two methods ; of which the first involves reduction of the gain in a previous stage (i.e. by the use of swept gain as previously discussed). The second method involves the provision of back bias, the magnitude of this bias ideally being equal to the peak voltage or envelope of the interfering carrier. In the latter method the interference is at a level approximating to the normal quiescent level of the stage and the signal peaks will be preserved.

22. This type of circuit is capable of providing up to 40 dB reduction in gain but preferably this

degree of reduction is not used. For this reason the i.a.g.c. amplifier is preceded by an amplifier stage controlled by a swept gain waveform.

Logarithmic amplification

23. In order to minimize the effects of receiver saturation in causing the loss of target signals superimposed on strong clutter, a receiver having detectors after successive i.f. stages is used. The output from such an amplifier is the sum of the outputs of the detectors so that, should the last stage be saturated, the previous stages will give an increase in output corresponding to an increase in input. The overall response of such a receiver is logarithmic for a range dependent upon the number of detected stages. The logarithmic receiver keeps the display clear in the presence of noise jamming but does not preserve the signal to noise ratio.

24. The essential difference between an i.f. amplifier of this type and a straight i.f. amplifier is that the latter has a single detector after all of its i.f. circuits whereas the former has a detector after every i.f. stage, the outputs of all detectors being added. Each stage therefore, besides feeding its output to the following stage, also feeds its own detector and thus makes an independent contribution to the output of the amplifier regardless of following stages.

25. Each detector feeds its own load and these loads are coupled together through sections of a video delay line. The delay line is necessary since the amplifier output is the sum of the outputs from all detectors, the delay per section of the delay line being equal to the delay in each amplifier stage. The detected outputs are added to produce a single-edged pulse output ; without the delay line, the output would appear as a stepped pulse.

26. If it is assumed that a particular amplifier consists of six stages, each having a stage gain of A, and that the i.f. voltage at the anode of a valve is V_a, when the voltage applied to the grid just saturates the stage, the difference in output, due to a voltage input change from $\frac{V_a}{A}$ to $\frac{V_a}{A6}$ is 6V, V being the output voltage for a saturated stage developed across the delay line termination. A logarithmic relationship exists between input and output over this range of input levels and is a ratio of A6 to 1.

27. If logarithmic amplification is followed by pulse length discrimination (which is a refinement of the differentiation process) signals with a duration up to the normal transmitter pulse length are passed at full strength whereas any signals with a pulse length of more than twice the transmitter pulse length are suppressed. This combination of circuits is equally effective whether clutter is moving or stationary.

28. The advantages of logarithmic amplification, when combined with pulse length discrimination, are that there is no loss of targets due to blind velocities as occurs with MTI and that target visibility is comparable with that from a linear receiver. The combination is effective against moving clutter without adjustment of controls, protects the display from saturation, and suppresses impulsive jamming of more than twice the transmitter pulse length. However, a target in clutter must be 5 to 10 dB stronger than the clutter to be visible, permanent echoes of short duration are passed at full strength and there is no protection against angels.

Pulse length discrimination

29. The pulse length discriminator (*fig.* 1) eliminates received video pulses of more than twice the duration of the transmitter pulse, delay lines being used as a standard of comparison.

30. If the signals (*fig.* 2(*a*)) are applied to a 5 microsecond delay line short-circuited at its far end, the original pulse is thus immediately followed by a pulse of the same duration but of opposite sign due to the reflection from the far end of the delay line (*fig.* 2 (*b*)). Overlapping parts of the pulse cancel out to give a result, particularly for pulses exceeding a width of 10 μS, similar to that obtained by differentiation (*fig.* 2 (*c*)). The composite pulses are amplified and applied to a phase splitter, the inverted output from which is applied direct and the other output via a 10 microsecond delay line to a coincidence detector (*fig.* 2 (*d*) *and* (*e*)). An output pulse (*fig.* 2(*f*)) is produced only where pulses of the same sense are coincident in time, all other pulses being eliminated. The output pulse is delayed by one pulse length compared with the input. A low-pass filter is included in the circuit to reduce noise peaks and improve target visibility.

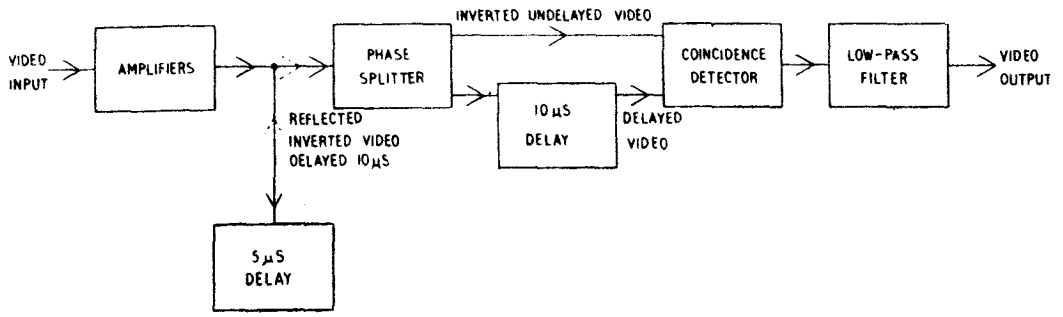
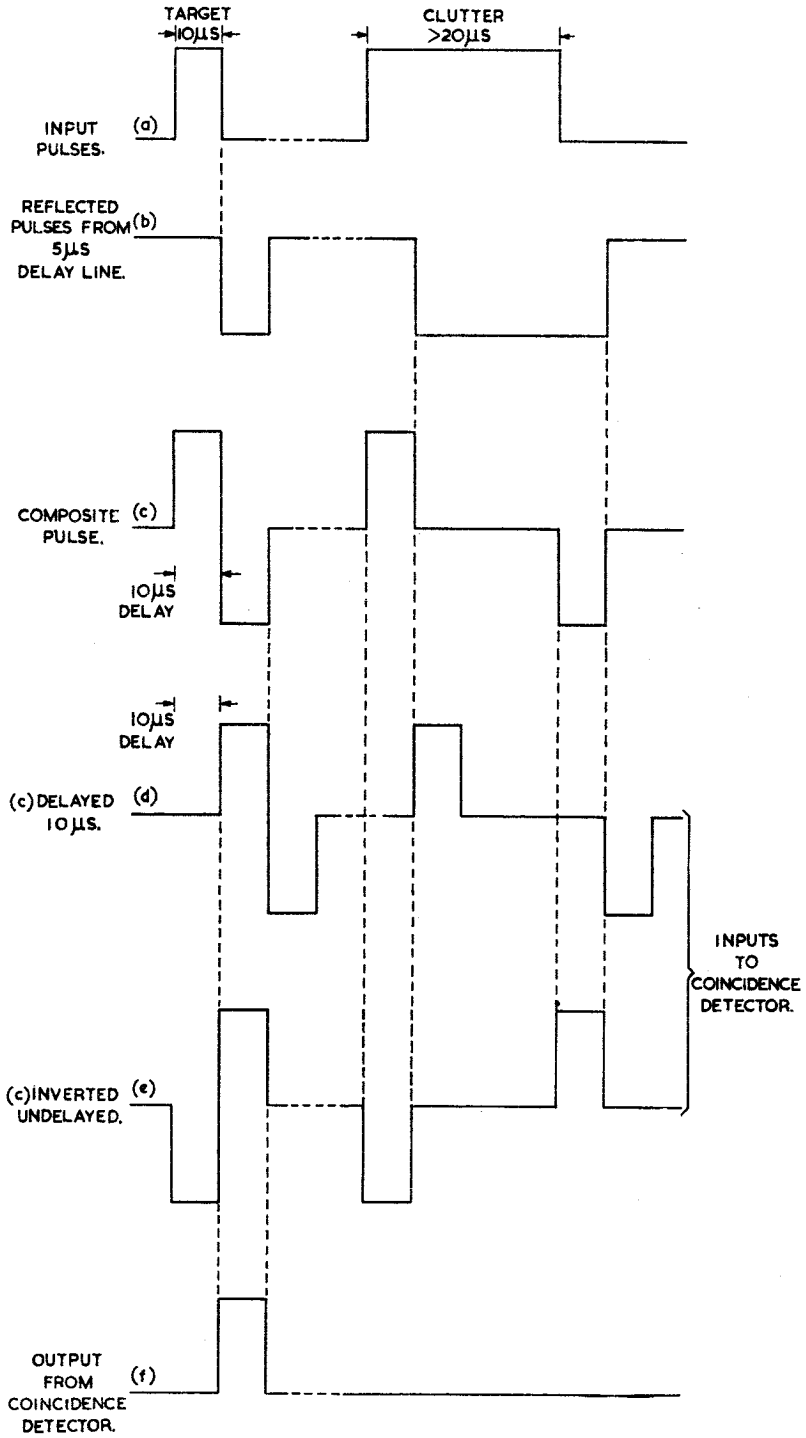


Fig. 1. Simple pulse length discriminator



◀ Fig. 2. Pulse length discriminator waveforms ▶

Moving target indication

31. The MTI circuits suppress (cancel) echoes from fixed objects such as hills, masts, towers, etc., while retaining maximum visibility of moving targets; these echoes are known as fixed clutter or permanent echoes. The basis principle may be extended to suppress echoes from moving clutter such as rain or window: this extension of the principle is known as MTI with Doppler compensation.

Single (or 2-pulse) cancellation

32. The principle of permanent echo suppression makes use of the fact that the phase relation between each transmitted pulse and the corresponding echo pulse depends upon target range. The phase relation is constant for a fixed target but changes from pulse to pulse if the target has a radial component of velocity.

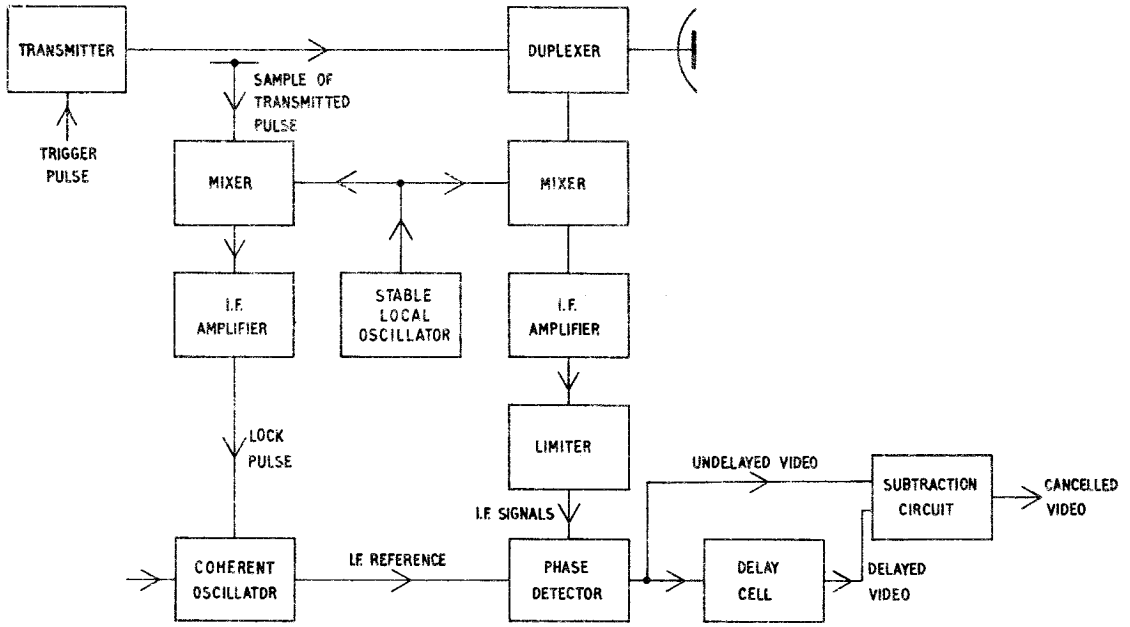


Fig. 3. Single cancellation with stalo

33. The cancellation process involves phase comparisons of the echo pulse with the transmitter pulse, but since the latter is of short duration and random starting phase it must be memorized for the duration of the longest echo time. A continuously running oscillator is of no use for this purpose and so a small proportion of the transmitter pulse is used as a lock pulse to control the starting phase of a reference oscillator, known as the coherent oscillator or *COHO*. This oscillator is stopped after a suitable period by an inhibiting pulse and then restarted by the lock pulse. A suitable period is the last 125 microseconds of the pulse repetition period. The output of the coherent oscillator is fed directly to the phase detector (coherent demodulator) where it is compared with the incoming echo signals. In a practical system (*fig.* 3) the local oscillator, which reduces the incoming signals to i.f., also feeds a second mixer which receives the r.f. sample. An i.f. lock pulse is thus produced to control the starting phase of the coherent oscillator, the latter also operating at i.f. For MTI purposes the phase changes from pulse to pulse must be due to Doppler and not to random frequency drifts. The local oscillator must therefore have a high degree of stability and is known as the stable local oscillator or *STALO*, the required frequency being derived from a crystal oscillator operating at approximately 10 Mc/s and multiplied by 128.

34. Echo pulses are compared with the reference frequency in a balanced phase detector, successive outputs from which will be similar for a permanent echo but will differ for a target moving with a radial velocity. If two successive outputs from the phase detector are applied simultaneously to a subtraction circuit the output from a permanent echo is ideally zero (cancelled) whereas the output from a moving target is dependent on the radial distance travelled between pulses.

35. This subtraction may be effected by delaying the first pulse for one pulse recurrence period and is normally made a continuous process by passing one input to the subtraction circuit via a delay line of suitable parameters; for a p.r.f. of 250 the delay required is 4 milliseconds and is obtained by an ultrasonic delay cell using mercury as the medium. In order to achieve good cancellation, pulses must pass through the delay cell with minimum distortion and the delay time must be accurately matched to the p.r.f. As the delay through the cell is affected by temperature variation, the delay time is used as the reference and the p.r.f. is automatically controlled to match it. The necessity for close control of the temperature of the delay cell is thus avoided.

36. The output of the phase detector is bipolar, the polarity being either positive or negative according to the phase of the incoming signals related to the reference frequency (*fig.* 4). The illustration shows three stable permanent echoes and returns from a moving target; the latter shows the butterfly effect due to phase variation from pulse to pulse. The returns from successive sweeps would give no output from the fixed echoes after subtraction in the cancellation circuits.

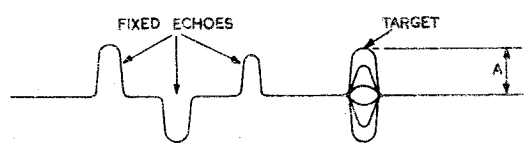


Fig. 4. Output from phase detector

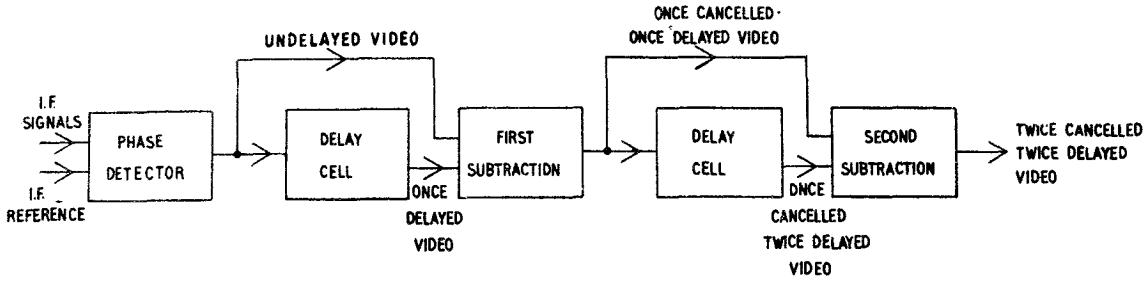


Fig. 5. Double cancellation

37. The degree of cancellation obtained is limited by the stability of the system, the fluctuations of the clutter returns and the scanning effect due to the rotation of the aerial. These effects may be minimized by the use of a long wavelength, a high p.r.f. and a large number of pulses per beamwidth. However, for a low p.r.f. (of 250), a beamwidth of 0·9° and an aerial rotational speed of 4 r.p.m. only 9 pulses are obtained per beamwidth. The scanning effect is thus severe and with 2-pulse cancellation and perfectly stable clutter, cancellation is limited to about 15 dB. The efficient cancellation of rain or angels is virtually impossible owing to variations in their apparent velocities.

Double (or 3-pulse) cancellation

38. The effects of pulse amplitude variations due to scanning or other variations is reduced in a system employing double cancellation ; this consists of two cancellation systems in series (*fig.* 5). The output is now the resultant of two subtractions of successive pulses. Reasonably stable ground clutter may be cancelled to about 21 dB. The signal to noise ratio is therefore limited to a maximum of 20 dB before the phase detector and the output of the phase detector is set to 20 dB maximum signal to shoulder noise. The sub-clutter visibility of an optimum velocity target at optimum phase is about 22 dB and the average for all phases is 17 to 18 dB. When dealing with moving clutter, cancellation may be limited to 14 or even 8 dB. This is due to the need to provide a sufficient width of blind velocity band to accommodate random internal motion in the clutter. The signal to shoulder noise ratios are 14 and 8 dB giving average sub-clutter visibilities of 12 and 6 dB.

Target visibility

39. The visibility of a target both in clutter and in the clear is subject to blind velocities and blind phases.

Blind velocities

40. If a target moves radially a distance equal to a whole number of half wavelengths between pulses the distance travelled by the pulse from aerial to target and back to aerial changes by a whole number of wavelengths. There is no change of phase between successive echoes and therefore the target return is cancelled. The radial velocities at which this occurs are given by the expression :—

$$V = \cdot 0097\, n\lambda f_r$$

V being the velocity in knots, λ the wavelength in centimetres, f_r the p.r.f. and n any whole number including zero.

41. For a system having a p.r.f. of 250 and a radiated wavelength of 23 cms., blind velocities occur at multiples of 56 knots.

42. Radial velocities which occur midway between blind velocities, i.e. at odd multiples of 28 knots, produce 180° phase change between successive pulses at the output of the phase detector and thus maximum output from the subtraction circuit. These are the optimum velocities for target visibility. Variation of the amplitude and phase of the moving target output from the phase detector occurs at the doppler frequency f_d, f_d being an exact multiple of the p.r.f. at blind velocities. If the first pulse from a moving target is of amplitude A, all successive pulses will also be of amplitude A and will produce no output from the subtraction circuit. At optimum velocities, if the first pulse is of amplitude A, successive pulses alternate between A and −A, the resultant output after subtraction being 2A.

Blind velocity bands

43. The response of an MTI circuit as a function of radial velocity is shown in fig. 6, the response for both single and double cancellation systems being shown. Targets at optimum velocity and optimum phase show an improved signal to noise ratio compared with a linear receiver, the signal to shoulder noise ratio of the input to the phase detector determining the output signal to noise ratio.

44. The target is submerged in noise over a band of velocities occurring every 56 knots. The widths of the blind velocity band for a double cancellation system are 9, 13 or 19 knots for input signal to shoulder noise ratios of 20, 14 or 8 dB respectively. The areas of blind velocities, in which some of the targets may lie and be consequently lost, provide a velocity tolerance for the cancellation of clutter. This tolerance is necessary in order to achieve cancellation in spite of clutter fluctuations and the scanning effect of the aerial (*para.* 37). When

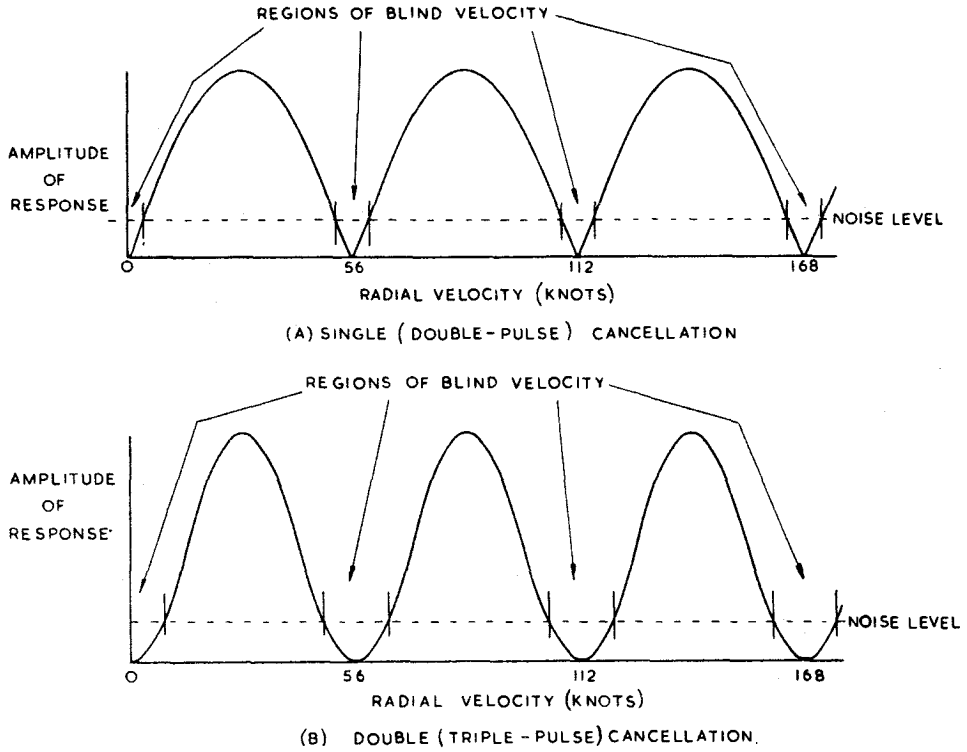


Fig. 6. MTI response patterns

clutter is turbulent, as in storm areas, the blind velocity band has to be increased; this may be achieved by increasing the amount of compression in the i.f. circuits preceding the phase detector. The blind velocity zones for double cancellation for a given signal to shoulder noise ratio are much wider than those for single cancellation.

Blind phases

45. The response (*fig.* 7) of a balanced phase detector is such that a target at optimum velocity causes a phase change between pulses of π radians so that if the first pulse occurs at zero phase on the diagram and the next at π radians the result, after subtraction, will be a large output. This is the case of optimum velocity with optimum phase. If the first pulse occurred at $\pi/2$ radians and the next at $3\pi/2$ radians however, the output from the phase detector would be zero and at optimum velocity all subsequent outputs would be zero. This is a combination of optimum velocity and blind phase and results in complete loss of target.

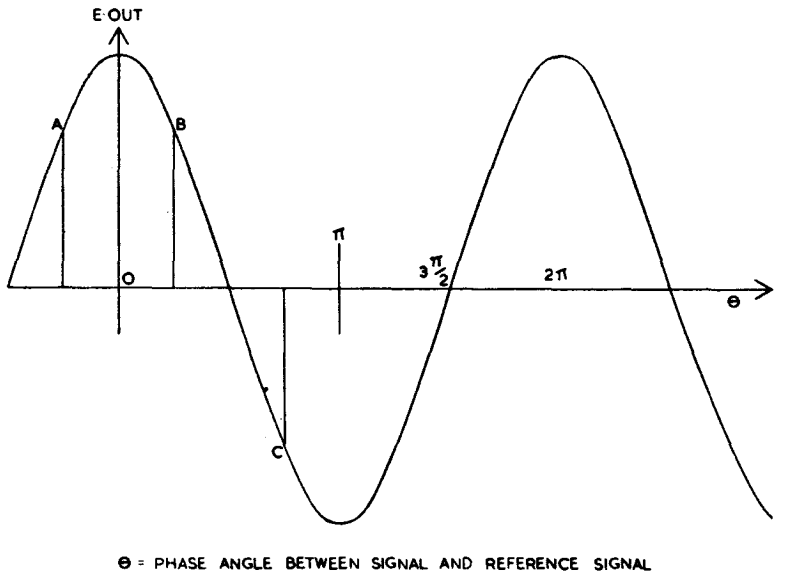


Fig. 7. Response of phase detector

46. Blind phases may also occur at velocities other than optimum. As an example, if one pulse occurred at A and the next at B, the result after subtraction would be zero. Only one pulse would be lost in this case as the next pulse arrives at C and gives an output when subtracted from B.

47. If the coherent oscillator frequency is off-set from the i.f. frequency the effect of blind phases is avoided, since by detuning the oscillator by 100 kc/s or more all phases are passed through during a 10 microsecond pulse. This facility is known as coherent low i.f. or *CLIF*.

48. The use of the *CLIF* facility will avoid blind phases when targets are in the clear but it is ineffective when strong clutter is present. The amplitude of clutter in the vicinity of the station may be very high and, as previously stated, it is compressed to the required signal to shoulder noise ratio before the phase detector in order that it may be cancelled effectively. A moving target in clutter may be regarded as a rotating vector modulating the fixed clutter vector in amplitude and phase. The phase detector will respond to both amplitude and phase changes but, after a large clutter vector with an amplitude exceeding the selected limiting level has been limited, only the phase variations remain. The moving target vector at optimum velocity rotates 180° between successive pulses so that if it is in phase with the clutter vector for alternate pulses it will be anti-phase for the remaining pulses and the phase detector will not distinguish between the phase change of successive pulses. Since changes of amplitude are removed in limiting, the phase detector will produce like outputs for each pulse and these are subsequently cancelled so that the target is lost. This is the blind phase. Optimum phase is in quadrature with this. Amplitude changes due to targets in weak clutter are not lost in limiting and therefore, although the phase may be blind, the target is not lost as the amplitude change is a maximum for targets at optimum velocity.

49. The effect of blind phases in clutter is reduced by the use of an i.a.g.c. amplifier instead of a linear amplifier with hard limiting. Strong signals are thus compressed but some amplitude variation remains, complete blindness is thus avoided when the phase is wrong. A further advantage of the i.a.g.c. receiver is that the sharp discontinuities of pulse amplitude which occur if a steeply rising aerial response curve is limited hard are avoided. These discontinuities tend to spoil the cancellation.

Doppler compensation for moving clutter

50. The output of the phase detector for a moving target differs between successive pulses due to the change in range of the target. The signal input to the phase detector therefore incorporates a doppler component, this component varying according to the apparent radial velocity of the target. If an area of rain surrounds the target and is moving at a uniform velocity its radial velocity varies according to a cosine law as the aerial revolves through 360°

51. In order to apply doppler compensation to the cancellation circuits the i.f. reference frequency input from the coherent oscillator to the phase detector is altered in frequency by an amount equal to the doppler component in the signal input. This alteration in reference frequency has the effect of moving the velocity response curve for the system along the velocity axis without altering the shape of the curve (*fig.* 8). The centre of one of the blind velocity bands is moved to correspond with the mean velocity of the moving clutter which it is desired to eliminate. In order to allow for aerial rotation the modulation of the i.f. reference frequency is made sinusoidal at aerial speed. In this way the i.f. signal and i.f. reference frequencies are made equal so that identical outputs are passed on to the cancellation circuits for successive pulses. The result is that moving clutter at the appropriate radial velocity, is cancelled whereas fixed targets remain. The block diagram of a practical doppler compensation system is shown in fig. 9.

52. Three different values of doppler compensation may be used at a time. These may be applied in three rectangular areas, adjustable in size and position, since it is seldom that a single velocity condition prevails over a large area.

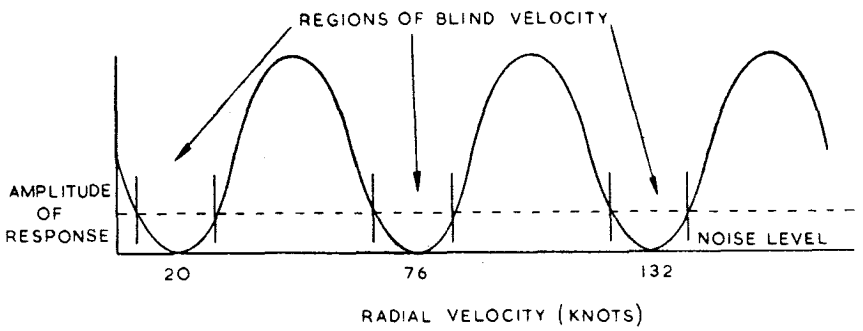


Fig. 8. MTI response pattern with doppler compensation

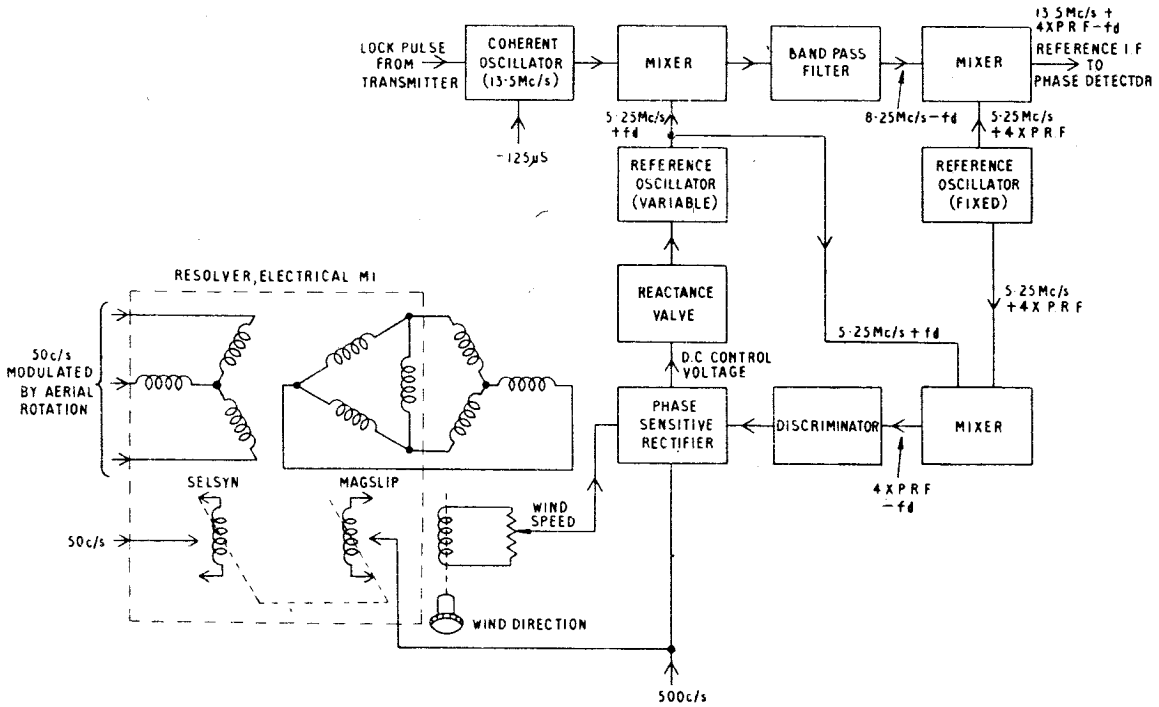


Fig. 9. Practical doppler compensation system

53. If doppler compensation for moving clutter is applied to an area in which ground clutter exists, the latter will not be cancelled. Similarly moving clutter is not cancelled in an area where doppler compensation is not applied. Two cancellation channels are used of which, for a certain area round the station, one channel has no doppler compensation applied and therefore cancels stationary clutter but not moving clutter. The second channel cancels moving clutter but not the fixed. The outputs from the two channels are applied to a coincidence detector which passes the smaller of the two signals where both types of clutter actually coincide. Elsewhere in the area the display is free from both fixed and moving clutter.

54. A pulse fed to either leg of the coincidence detector allows noise on the other leg to be passed at full strength, so that the pulse is visible on the output as a 3 dB increase of noise (*fig.* 10). This is minimized by also feeding the coincidence detector inputs to a subtraction circuit via an OR gate. The second input to the subtraction circuit is received from the output of the coincidence detector. Non-coincident pulses are passed by the OR gate only, so that, as no output is produced by the coincidence detector, the subtraction circuit receives only one input. The subtraction circuit produces an output which operates an electronically switched attenuator to reduce the output by 3 dB : the noise thus increased by the non-coincident pulse is restored to normal. Coincident pulses are fed to both inputs of the subtraction circuit so that the switched attenuator is not operated and no attenuation takes place. This type of switched attenuator is also used after the coincidence detector in the p.r.f. discrimination circuits for the same reason : in this instance, however, the pulses of noise in the output are produced by the non-synchronized interference pulses.

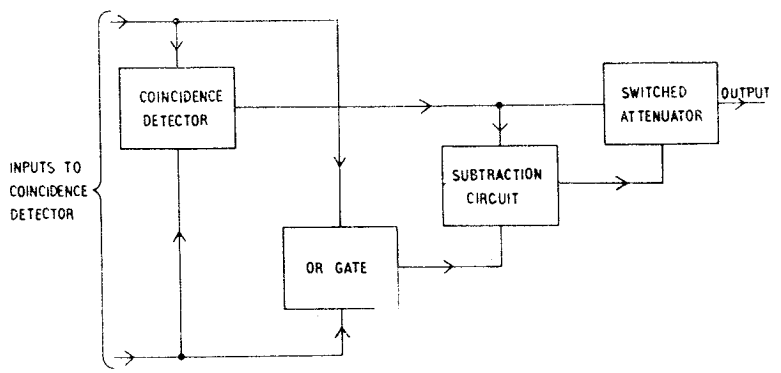


Fig. 10. Electronically switched attenuator

P.R.F. discrimination

55. The p.r.f. discriminator (*fig.* 11) suppresses interfering pulses which are not synchronized with transmitted pulses. Trains of pulses from targets are passed with the loss of only one pulse per train. The noise level is reduced 3 dB.

56. Signals are fed to one arm of a coincidence detector (*fig.* 12 (*a*)), and also to a servo controlled mercury delay cell with a delay equal to one pulse repetition period. The delay time of the delay cell is servo controlled by a motor fed with an error voltage developed in a p.r.f. controller. The delay

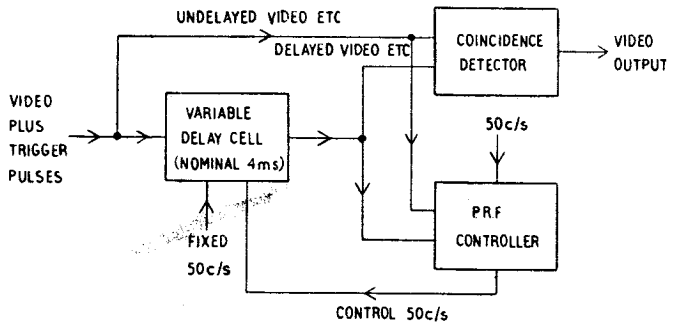


Fig. 11. Simple p.r.f. discriminator

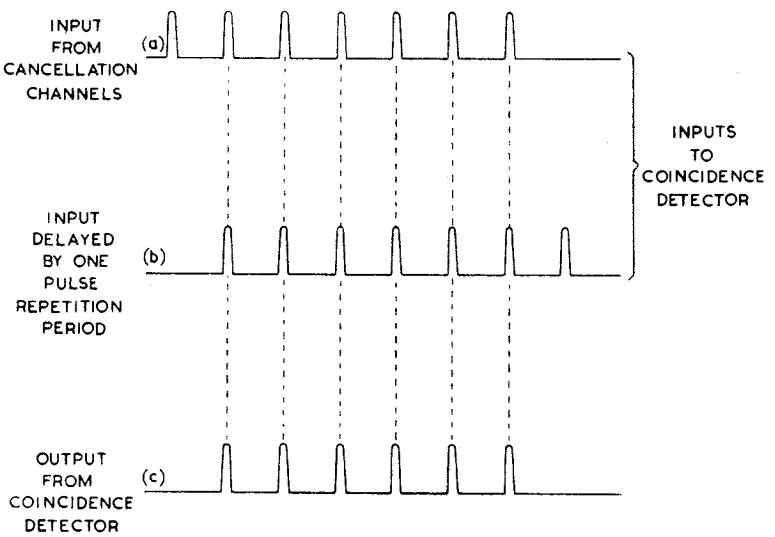


Fig. 12. Effect on train of target pulses

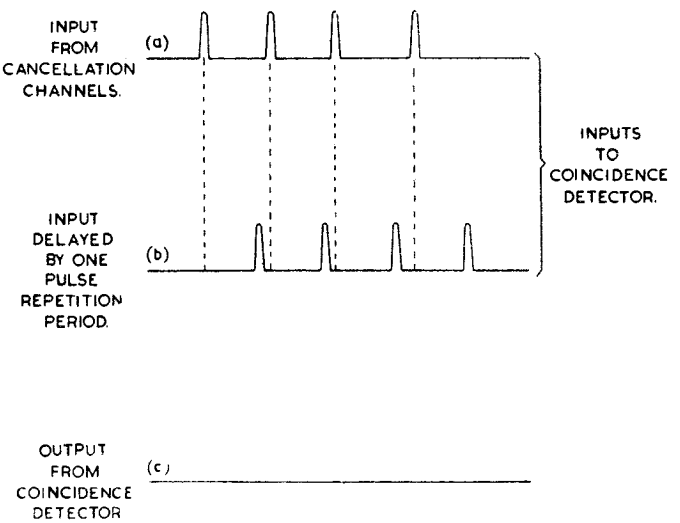


Fig. 13. Effect on interference pulses

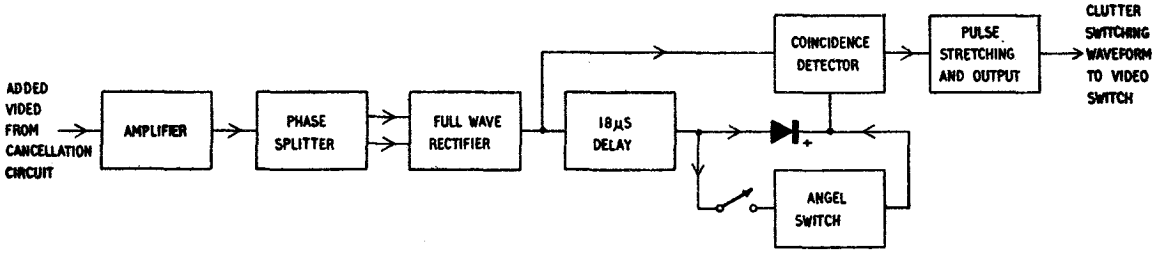


Fig. 14. Block diagram of clutter switching

time is made exactly equal to the pulse recurrence period in order to compensate for temperature variations: in a system also employing MTI the p.r.f. is already controlled by the MTI delay cell. The output from the delay cell (*fig.* 12 (*b*)) feeds the second leg of the coincidence detector from which an output is only produced when delayed and undelayed pulses are coincident in time (*fig.* 12 (*c*)).

57. As previously stated, target signals, being in trains of several pulses, are passed by the coincidence detector with the loss of only one pulse per train but interference pulses are suppressed unless they happen to be nearly synchronous with the p.r.f. (*fig.* 13 (*a–c*)). Since an interference pulse fed to either leg of the coincidence detector allows noise on the other leg to be passed at full strength, an electronically switched attenuator (*para.* 54) is used to prevent interfering pulses being visible on the output as an increase of noise.

SELECTION OF SIGNAL PROCESSING FACILITIES

58. Each of the signal processing methods previously discussed has its own advantages and disadvantages. It is therefore essential that the best combination of methods to suit the prevailing condition is used. Although MTI is the most effective method of eliminating clutter, it suffers from the disadvantages of blind velocities and blind phases and should therefore be used only where the presence of clutter makes this absolutely necessary. On the other hand, a logarithmic amplifier followed by a pulse length discriminator circuit is partially effective against clutter and certain forms of interference without the disadvantages of the MTI system. For clear conditions, i.e. where clutter and interference are at acceptable levels, the output of a linear channel provides the best display, since no loss of targets due to the shortcomings of the MTI or logarithmic channels is involved. Under conditions of severe jamming, possibly from an airborne jammer, the application of reverse swept gain to the linear channel outside a selected range gives an indication on the display of the direction from which the jamming is being received; range information will not be available since the jamming signals are not locked to the radar transmitter pulse. In the event of carcinotron jamming, which is not affected by any of the signal processing methods previously discussed, an anti-jamming channel utilizing a Dicke Fix type receiver is used. It is also possible, by i.f. switching, to use this receiver for MTI and logarithmic channels.

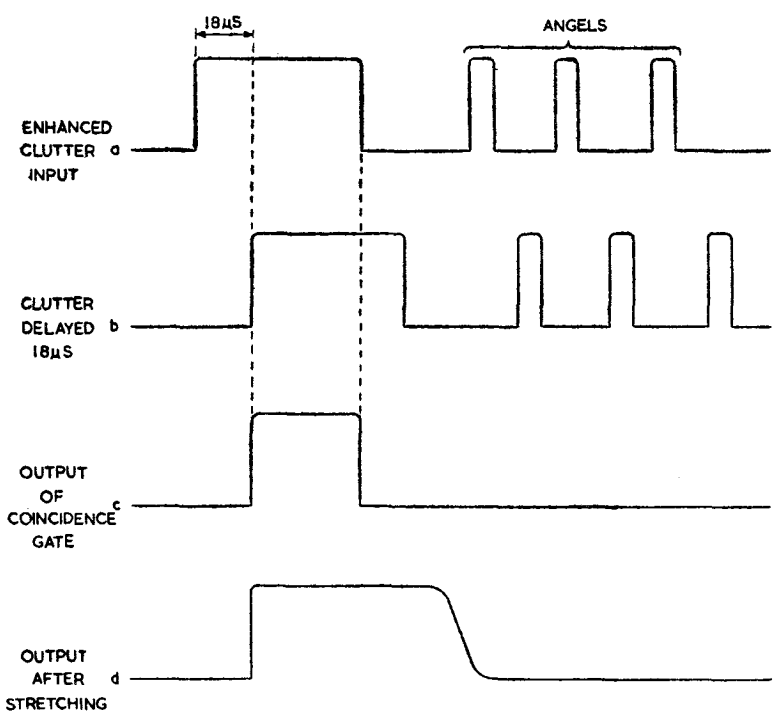


Fig. 15. Clutter switching waveforms

59. A combination of two methods of video switching is used, one employing diode switching and the other conventional relay circuits. Diode switches are operated by a switching waveform, this waveform being arranged to supply a certain form of video, such as MTI, to selected areas of the display or to incorporate clutter switching so that the MTI video is supplied to the display in areas of clutter within the selected areas. Switched relays are employed to select the required video combinations, in conjunction with the diode switches, for display. The five degrees of signal processing used are:—

(1) Fully processed—a background of logarithmic, pulse length discriminated video with MTI, Doppler compensated video in selected areas, clutter-switched for preference.

(2) Semi-processed—MTI video in the local clutter area with logarithmic video elsewhere.

(3) Log-PLD video all over the display.

(4) Linear video all over the display.

(5) Video from the anti-jamming channel all over the display.

60. The operator controlling the signal processing system as a whole is provided with monitor consoles upon which can be displayed video in certain stages of processing but without affecting the video supplied to the operational consoles. Selection of these displays is made by relay switching circuits.

Clutter switching

61. The clutter switching circuits initially receive a bipolar video output from the cancellation circuits in which the clutter signals are added (*fig.* 14). Clutter signals are therefore emphasized instead of being cancelled and this process is most effective when cancellation is operating at optimum efficiency. The enhanced clutter (*fig.* 15 (*a*)) feeds one arm of a coincidence detector, the other arm being fed with the same clutter signals but delayed 18 microseconds (*fig.* 15 (*b*)). The output of the coincidence detector is therefore delayed by 18 microseconds after the input signal and is shorter in duration by the same amount (*fig.* 15(*c*)). This output is amplified and stretched (*fig.* 15(*d*)) so that the duration of the clutter switching waveform is a little greater than that of the clutter to be switched to avoid display of the trailing edge of the clutter. As the clutter switching waveform is delayed a total of some 26 microseconds, the video channels must incorporate compensating delay networks, the delay times of which take into account inherent delays in the channels, so that the video signals are applied to the switching circuits after the clutter switching waveforms.

Angel switching

62. Owing to the short duration of angels there can be no coincidence and therefore no output from the coincidence detector. The circuit is therefore arranged, under the control of a switch, so that a switching output is produced when angel density is such as to result in point echoes separated by less than 100 microseconds. Input pulses (*fig.* 16 (*a*)) are delayed and stretched so that their amplitude, as indicated by the dotted line, is still appreciable after 100 microseconds (*fig.* 16 (*b*)). The residual amplitude of each stretched pulse is sufficient to provide an output from the coincidence detector by coincidence with the succeeding undelayed pulse (*fig.* 16 (*c*)). A train of four angels, for example,

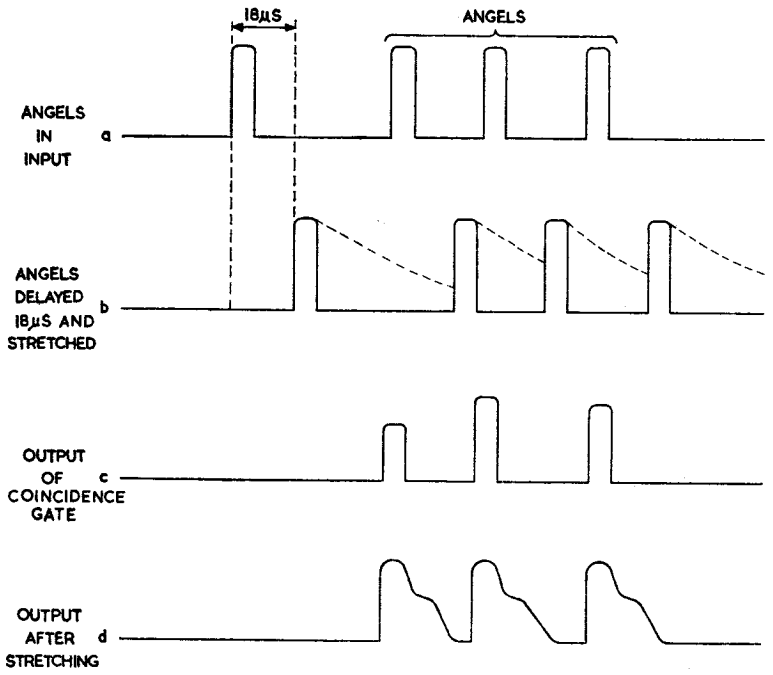


Fig. 16. Angel switching waveforms

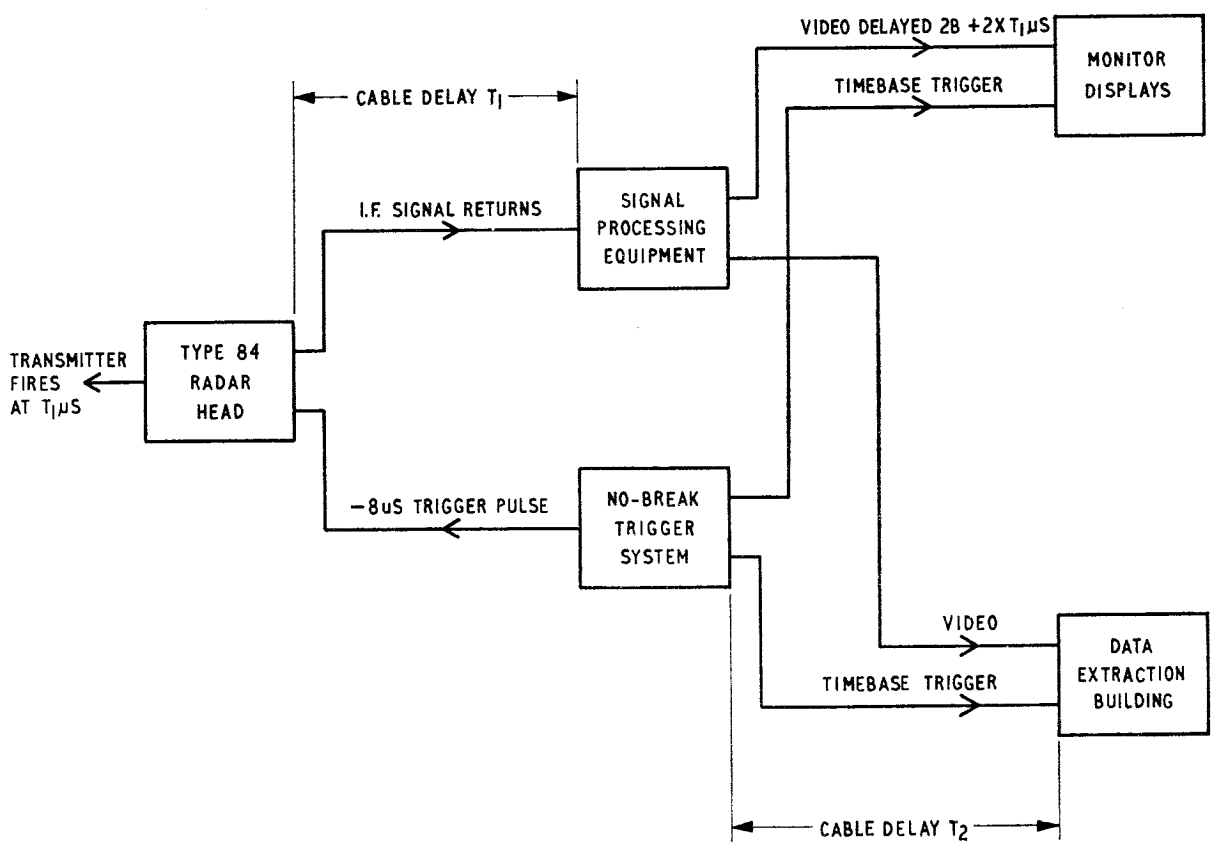
produces three switching pulses which are amplified and stretched in the same manner as a fixed clutter switching pulse (*fig.* 16 (*d*)). The first angel of a group is therefore allowed to appear on the display as the angel switching circuit produces switching pulses only when two or more angels are present. Isolated targets in the clear are therefore shown on the display. Since the angel switching circuits will also cause the returns from closely grouped aircraft to be switched to MTI the facility of angel switching is made the subject of a control on the monitoring display console. The angel switching circuits may thus be made inoperative but the normal clutter switching facility is retained.

◀COMPREHENSIVE STATION TIMING▶

◀**63.** The signal processing equipment and its associated radar forms part of a comprehensive station, the triggering pulses for which are derived from the no-break trigger system which is described in A.P.4769E. Because of delays introduced through sections of the circuits and through cabling, it is necessary that this p.r.f. system produces a series of timing pulses, all at the station p.r.f. (nominally 250 c/s), but advanced or delayed in time with respect to a nominal zero pulse which occurs at an arbitrary time T = O. Because the Type 84 radar employs MTI, it is necessary that the pulse recurrence frequency of the no-break trigger system (p.r.f. system) is controlled by the delay time of a mercury delay cell in the Type 84 signal processing circuits.

64. In the no-break trigger system the basic p.r.f. generator circuit consists of a crystal oscillator operating at a nominal frequency of 4·096 Mc/s ($2^{14} \times 250$ c/s), a series of divide-by-two frequency divider stages and a number of AND-gates, each of which combines the outputs of certain of the divider stages to produce the required trigger pulses. In some cases, phase shifting of the divider output is necessary in order to produce the required timings of outputs. By this means basic pulses are formed which are timed to occur 750, 500, 250, 125, and 8 microseconds before a nominal zero pulse and are designated −750, −500, −250, −125, and −8 microseconds pulses respectively. All of these pulses are fed to output circuits, where the requisite numbers of outputs at each timing are formed, at the required output levels and impedances to drive the external equipment. Certain of the basic pulses are fed to variable delay circuits, by means of which a further series of output pulses is generated delayed on the originating pulses by amounts adjustable between 5 and 170 microseconds.

65. In practice, the p.r.f. system incorporates two such timing chains, main and standby, whose outputs are aligned in time and fed out through OR-gates. Fault monitoring ensures that output from a faulty chain is automatically inhibited. The frequency of the crystal oscillators, main and standby, is controlled by a variable frequency-pulling capacitor which is driven by a two-phase motor. At any one time only one or the other of the two oscillators is providing the basic frequency for pulse production, and its motor is then driven by



◀**Fig. 17. Type 84 triggering**▶

500 c/s p.r.f. correction signals derived from a p.r.f. controller in the Type 84 signal processing circuits. The degree of correction required is ascertained by comparing a −8 microseconds pulse with another −8 microseconds pulse generated in the previous pulse period, after it has passed through the fixed mercury delay cell in the MT1 circuits. Correction signals are generated which drive the crystal oscillator, and hence the p.r.f., until the two pulses are coincident. The pulse period is then equal to the delay time of the mercury cell.

66. A typical site situation is illustrated in fig. 17, in which the no-break trigger system is housed in the same building as the signal processing equipment. In the Type 84 signal processing circuits a delay of 28 microseconds is introduced (mainly due to clutter switching); the timebase initiation pulse is delayed by a similar amount, to ensure that the timebase start coincides with the start of the radar video.

67. The Type 84 radar head may be at a distance of up to 1000 yards from the building housing the signal processing equipment. A cable delay is therefore involved in the transmission of the transmitter trigger pulse to the radar head and the same delay occurs in the return of i.f. signals from the radar head to the signal processing equipment.

68. In fig. 17 the cable delay between radar head and signal processing equipment is T_1 microseconds and that between signal processing equipment and data extraction building is T_2 microseconds. The −8 microseconds pulse is used to trigger the Type 84 transmitter. The cable delay is T_1 microseconds and as the transmitter fires 8 microseconds after the arrival of the trigger pulse the actual transmitter firing time is T_1 microseconds after the arbitrary time T = O.

69. The i.f. signals from the head are delayed T_1 microseconds in their return to the signal processing equipment so that they arrive at a time $2 \times T_1$ microseconds after T = O. After signal processing, the video signals are passed to the monitor displays after a delay of $28 + (2 \times T_1)$ microseconds. The initiation of the monitor time bases must therefore be by means of a pulse delayed by a similar amount in order to achieve coincidence between timebase trigger and video. The displays in the data extraction building are automatically aligned since the cable delay, T_2, is the same in both timebase trigger and video paths.

70. ◄ To assist in calibrating the equipment a full video zero range pulse is generated and inserted on the Type 84 video channels at $V_0 - 47$ microseconds with relation to the no-break trigger pulse. ► Other radars in the comprehensive station have their trigger pulses and video adjusted by variable delays to ensure alignment at the signal processing and the data extraction buildings. Certain transmitters may be triggered a considerable time before the Type 84 transmitter and the variable delay is adjusted to achieve coincidence of video and common timebase trigger.

Chapter 2

SIGNAL PROCESSING FACILITIES

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

INTRODUCTION

1. The signal processing equipment, which forms part of the Type 84 radar system, provides a means whereby the raw radar signals from the radar head may be processed in the most effective manner possible in order to show the maximum number of targets in the presence of various degrees of clutter and interference.

2. The equipment is designed to operate in conjunction with an L-band radar transmitter/receiver operating in the frequency range of 1215–1365 Mc/s with a pulse width of 10 microseconds and a nominal pulse repetition frequency of 250 per second.

3. Separate i.f. inputs are received from the radar head as follows:—

(1) An i.f. input at a centre frequency of 13·5 Mc/s from the narrow band linear channel of the head amplifier.

(2) An i.f. input with the same centre frequency from the broad band channel of the i.f. amplifier via a limiter and a narrow band amplifier. This arrangement is known as a Dicke Fix receiver and provides the anti-jamming i.f. input to the signal processing equipment.

4. The video outputs from the signal processing equipment are fed to the operational displays via two video channels, known as channels 1 and 2. Channel 1 video output is that selected by the MTI operator from the available signal channels according to the degree of signal processing required to suit prevailing conditions. Channel 2 is always supplied with the video output from the logarithmic channel with pulse length discrimination.

5. The MTI operator is provided with a monitoring console suite consisting of three Type 64 fixed coil displays. The right-hand display, console 3, is an unprocessed display showing the video output from the linear signal channel. Console 1, the left-hand display, continuously monitors the video output on channel 1. The video for the centre display, console 2, is selected by the operator from different points in the signal processing system and includes, in addition to the outputs on channels 1 and 2, limited video from the linear signal channel, MTI video as at the output of the cancellation channels without further processing, the video output from the anti-jamming channel and a test input.

◀**6.** Timing pulses required for the signal processing system are derived from the no-break trigger system, whose p.r.f. is locked to the delay time of the mercury delay cell used in the cancellation system. The same p.r.f. system also provides other pulse outputs to synchronize complementary systems with the Type 84 radar on a comprehensive radar station.▶

7. Major items of test equipment for routine maintenance, fault-finding and testing are provided as an integral part of the system.

8. A comprehensive monitoring system is provided from which it is possible to determine the serviceability and standard of performance of certain sections of the Type 84 system. The indicator panels associated with the monitoring system are positioned within view of the MTI operator so that video outputs for the operational displays may be selected according to the availability and serviceability of the various signal channels.

SIGNAL PROCESSING SYSTEM DESCRIPTION

9. The i.f. inputs to the signal processing systems are applied to an i.f. switch unit, from which the required i.f. signals are fed to four signal channels. The processed video outputs from the MTI, logarithmic and linear channels are supplied to the first stages of the channel selection circuits, the selected output from which is then applied, via a p.r.f. discriminator, to the final channel selection stage. This stage selects either the output from the p.r.f. discriminator or that from the anti-jamming channel for transmission to the operational displays via channel 1 (*fig.* 1).

10. Doppler compensation is applied to the MTI channel in three rectangular display areas, the positions and sizes of which are under the control of an operator using a joystick on the monitor console. The waveforms produced control electronic switches and these in turn apply Doppler compensation to the MTI channel in the rectangular areas and select the appropriate video outputs from the signal channels for application to the video paths for fully-processed and semi-processed displays.

11. The MTI channel incorporates two cancellation channels, the coherent demodulators for which are fed with an i.f. reference frequency produced by a coherent oscillator. The frequency of the oscillator is made coherent with the transmitter by an i.f. lock pulse, the latter being received from the aerial head via the i.f. switching unit.

12. The video existing at various stages of signal processing is selected by the monitor selection circuits for presentation on the central display on the monitor console.

I.F. and lock pulse switching

13. The electronic i.f. switch receives the linear and anti-jamming i.f. inputs and also the i.f. lock pulse from the radar head. Test i.f. signals and a test i.f. lock pulse are also received from the built-in test equipment.

14. The linear i.f. input is passed directly to the linear signal channel at a level 15 dB below the input level and the anti-jamming i.f. input directly to the anti-jamming signal channel. Under normal circumstances the MTI and logarithmic signal channels receive the linear input via a switched amplifier, the input to the MTI channel being at a level 15 dB below that to the logarithmic channel. In the event of carcinotron jamming, the linear i.f. input to these two channels may be replaced by the input from the Dicke Fix receiver, the changeover being performed by operation of the ANTI-JAM switch on the monitor console. Test signals may be injected into these signal channels and the radar signal inhibited, by means of manually-operated switches on the unit.

15. The i.f. lock pulse from the radar head is normally fed to the coherent oscillator, but may be replaced by a test i.f. lock pulse from the built-in test equipment on operation of the TEST/NORMAL switch on the switch unit.

Anti-jamming signal channel

16. In this channel, the input i.f. signal is demodulated and applied, after a compensating delay period of 28 microseconds, directly to the video switching circuits associated with channel and monitor selection.

17. This channel can also be used as an emergency channel, since the power supplies for the demodulator unit are independent of those for the remainder of the system. The channel can therefore be operated with the remainder of the system inoperative since the video switching circuits are so arranged that with all relays unoperated the video output from the channel is connected to channel 1 and thence to the operational displays.

Linear signal channel

18. Under normal circumstances, the linear channel provides linear amplification and demodulation of the linear i.f. input from the aerial head.

19. With the LINEAR INJECTION switch on the control desk operated, the gain of the amplifier is modified by a reverse swept gain characteristic at a range in excess of 200 nautical miles. The same control also causes a gating waveform to be supplied to an electronic video switch whereby the output of the linear channel, with reverse swept gain from 200 nautical miles, is included in channel 1 output from the system, instead of logarithmic video.

Logarithmic signal channel

20. The logarithmic signal channel first provides logarithmic amplification of the i.f. input selected by the i.f. switch unit. The video output from the amplifier is then applied to a video sweep generator, the main function of which is reduction of the strength of echoes from angels. This is achieved by using a swept gain waveform as a baseline clipping voltage operating on the video output of the logarithmic amplifier. Interference or noise results in a loss of signal to noise ratio, so that the use of swept gain would lead to an unnecessary loss of targets. The video sweep generator unit is therefore arranged so that sensitivity may be lost either by interference or by swept gain, whichever is the greater, but not by both at once. If the d.c. component of the signal increases owing to noise jamming or clutter, the applied clipping voltage is wholly or partially cancelled. The amount of

clipping can be selected in four levels, from zero to maximum, by relays operated from the SWEPT GAIN control on the monitor console.

21. The logarithmic channel is completed by a compensating delay network and a pulse length discriminator, the latter eliminating clutter responses having pulse lengths in excess of twice the transmitted pulse.

22. The logarithmic channel thus provides protection against clutter, both moving and stationary, noise and c.w. jamming and impulsive jamming of more than twice the transmitted pulse length, without the disadvantage of loss of targets due to blind velocities. Targets in clutter must, however, be 5 to 10 dB stronger than the clutter in order to be visible.

MTI signal channel

I.F. circuits

23. I.F. signals for the MTI channel are first applied to a noise control circuit incorporating a single-stage i.f. amplifier. The gain of the amplifier may be controlled by a gain control voltage which is a function of i.f. noise, or by a swept gain waveform controllable in steps by the SWEPT GAIN control on the monitor console or by a combination of both the foregoing, the greater of the voltages assuming control.

24. The i.f. signals are further amplified in an instantaneous automatic gain controlled (i.a.g.c.) amplifier. This type of amplifier provides controlled compression of signals and prevents the loss of phase and amplitude information which could occur in a linear amplifier due to saturation. This amplifier incorporates the first stage of compression, in that input signals with an amplitude range of 6 to 40 dB above noise are compressed to within an amplitude range of 14 dB at the output of the amplifier.

25. The subsequent i.f. amplifier incorporates a single stage of amplification, followed by further compression under the control of the BLIND VELOCITY BAND switch on the monitor console. With the switch in the 9 KNOTS position, no further limiting is applied, but with the switch in the 13 and 19 KNOTS positions, additional limiting is applied in two 6 dB steps to correspond with the 13 and 19 knots blind velocity bands.

26. The MTI channel is thus protected against clutter and noise jamming and its i.f. output is limited to a pre-cancellation limit level according to the width of the blind velocity band to be employed. The output provides the signal input to each of two coherent demodulators, one for each cancellation channel.

Coherent oscillator and mixer stages

27. The reference frequency input to each of the coherent demodulators consists of an i.f. reference frequency received from the coherent oscillator via the appropriate frequency mixer stage. It is convenient at this point to consider the operation of this part of the system from the aspect of permanent echo cancellation only, the effect on the circuits of doppler compensation will be detailed in later paragraphs.

28. The coherent oscillator is arranged to operate at a nominal frequency of 13·5 Mc/s but this frequency may be reduced by an amount up to 200kc/s where use of the coherent low i.f. (c.l.i.f.) facility is required in order to reduce the effect of blind phases. The oscillator is inhibited for the last 125 microseconds of each pulse repetition period by a −125 microsecond pulse and restarted by the i.f. lock pulse from the i.f. switch unit. The oscillator runs in phase with the lock pulse and continues, after the end of the lock pulse, until inhibited again by the next −125 microseconds pulse.

29. The output from the oscillator forms one input to the frequency mixer stages. Each frequency mixer stage consists of two mixers connected in series but, for permanent echo cancellation purposes, each of the two mixers is fed with the same input of 5·251 Mc/s (*nominal*) from the fixed reference frequency oscillator in the doppler compensation circuits. The output of the unit is therefore the coherent oscillator frequency without alteration. Each mixer stage feeds one coherent demodulator.

Cancellation channels and cancellation channel mixing

30. The two cancellation channels consist of identical units and differ only in function in that channel A cancels permanent echoes in the circle whereas channel B cancels slow-moving targets where any rectangle is so positioned as to overlap the circle. A video output is taken from channel B after the coherent detector and fed back to the noise-operated a.g.c. circuit in the MTI i.f. circuits. Delayed and undelayed video outputs, which include −8 microsecond pulses, are extracted from the first cancellation stage for p.r.f. correction purposes.

31. Each cancellation channel consists of two cancellation circuits in series and each provides three outputs, after different stages of cancellation. These outputs are rectified individually and then combined in a series of coincident detectors. The result is cancelled video from which the triple interference pulses resultant from double cancellation have been reduced to a single pulse.

32. The pulse length discriminator which follows is identical to that used in the logarithmic signal channel except that the LOG/ANTI LOG switch is set to LOG.

Rectangle and marker generation circuits

33. The three rectangular areas in which doppler compensation is applied may be adjusted in position and size to cover the area in which compensation is required.

34. The position and size of the rectangles is controlled by the operator by means of a joystick on the monitor console, the rectangle to be adjusted

being selected by the appropriate MOVE/SIZE switch. Only one rectangle can be adjusted at a time and the adjustments of position and of size are performed as separate operations. Alternatively, the rectangles may be set to a predetermined position by operation of the relevant RESET switch.

35. For any given position of a rectangle, switching waveforms are produced which, together with a switching waveform for the circle, are used in three functions under the control of three LOCAL/USERS switches on the monitor console :

(1) To control the application of doppler compensation to each of the three rectangles.

(2) To produce a composite switching waveform in conjunction with clutter switching waveforms to control an electronic video switch for the fully processed video output from the system.

(3) To produce display markers for circle and rectangles for use on the signal processing monitor consoles.

Doppler compensation

36. The degree of doppler compensation applied to each rectangle is controlled by three WIND SPEED and WIND DIRECTION controls. Each of the WIND DIRECTION controls consists of a magslip on the control desk, the stator windings being fed with a 500 c/s waveform modulated by aerial rotational information received from a resolver driven at aerial rotational speed. The rotor of the magslip is set according to the direction of correction to be applied, and the level of the 500 c/s output is set by a potentiometer to control the amount of correction, i.e. wind speed.

37. The doppler compensation circuits are thus fed with three 500 c/s waveforms (*one for each rectangle*) modulated to allow for aerial rotation. Each waveform is fed to an electrical frequency control, which in turn controls the output frequency of a variable reference frequency oscillator.

38. With no doppler compensation applied, the output of the variable reference frequency oscillators is nominally 5·25 Mc/s, so that the output from the first mixer in the frequency mixer stages is the coherent oscillator frequency (13·5 *Mc/s nominally*) minus 5·25 Mc/s. In the second mixer this is mixed with the output from a fixed reference frequency oscillator of 5·251 Mc/s (5·25 *Mc/s* + 4 × *p.r.f.*) to give an output frequency to the coherent demodulator of 13·5 Mc/s plus 1 kc/s. This frequency corresponds to the fourth blind velocity region, so that no doppler compensation is applied to the cancellation channels and therefore permanent echoes are cancelled.

39. The outputs from the four reference frequency oscillators are fed to the two frequency mixer stages via two electronic reference frequency switches. These switches are supplied with rectangular waveforms under the control of LOCAL/USERS switches on the monitor console, so that the outputs of the variable reference oscillators are fed to the mixers when rectangle waveforms are present, both mixers in the frequency mixer stages being fed with the output of the fixed reference frequency oscillators at all other times. The switches are so arranged that where rectangles overlap, rectangle 1 takes precedence over rectangles 2 and 3 and rectangle 2 over rectangle 3. A similar order of precedence exists in the video switching waveforms.

40. With doppler compensation applied to a particular rectangular area, the output of the variable reference frequency oscillator associated with that area is varied up to a maximum of ±500c/s about the nominal oscillator frequency. It follows that the output of the mixer stage to the coherent demodulator will be varied about that obtained without compensation by the amount of variation of the variable reference frequency oscillator. The i.f. reference frequency applied to the coherent demodulator is thus shifted by an amount equal to the doppler component of the radial velocity of the moving clutter. This causes the blind velocity band to be moved, so that echoes with a radial velocity containing a doppler component equal to the applied doppler compensation are cancelled, but permanent echoes are uncancelled.

41. Should a rectangle overlap the circle, permanent echoes are cancelled by channel A and slow-moving echoes by channel B. Where permanent and slow-moving echoes overlap, the lesser of the two is passed by the combined cancellation channels to subsequent circuits.

Video switching

42. The video switching circuits are mainly centred in two relay assemblies and three electronic video switches. The circuits may be divided into two sections. Those which select the video for channel 1 (the user's main display) are controlled by the 5-position, CHANNEL SELECTOR switch and those which select the video to be displayed on console 2 are controlled by the MONITOR SELECTOR switch.

43. The initial video switching operations are performed by the three video switches. These are operated by switching waveforms, so that the output from the switch consists of video from one source for a certain part of the timebase range and of video from a second source for the remainder of the range.

44. The three video switch units are identical in circuit but differ in function. The switches associated with the fully processed and semi-processed signal paths normally pass background video from the logarithmic signal channel, but change over to MTI video on receipt of a switching waveform. The switching waveform for video switch 1 (*fully processed*) is a composite waveform for circle and rectangle areas, but that for video switch 2 (*semi-processed*) is for the circle only. The MTI video passed is cancelled for permanent echoes in the circle, and doppler compensated in rectangles, with the exception of video switch 1 in areas where rectangles and circle overlap. In the overlapping area, the clutter passed is the smaller of the two. The third video switch normally passes video from the linear signal channel but changes

over to logarithmic video on receipt of a switching waveform. The switching waveform in this case covers a range of 0 to 200 nautical miles. The output from this switch unit is used only with the LINEAR INJECTION switch operated on the signal processing monitor console.

45. The outputs from the video switches, together with direct outputs from the logarithmic, linear and anti-jamming signal channels, are applied to the manually controlled video switching circuits. The required video for channel 1 and console 2 is selected by operation of the CHANNEL and MONITOR selector switches as described below.

Channel selection

46. The CHANNEL SELECTOR switch on the control console has five positions.

47. Position 1 of the switch provides a fully processed video output which consists of:

(1) Permanent echo cancellation in a circular area set to embrace the local ground clutter pattern. The radius of the circle is set by a range gate to be as small as possible consistent with particular site conditions. The cancellation is provided by the double cancellation MTI system without doppler compensation. The MTI video is either applied over the whole circular area or switched in automatically within the circle, according to the setting of the CIRCLE CLUTTER SWITCHING control on the signal processing monitor console.

(2) Doppler-compensated, double cancellation within up to three rectangular areas. CLUTTER SWITCHING controls, one for each rectangle, operate in the same manner as in the circle area. Moving clutter within the circle may be eliminated by positioning a rectangle to enclose the moving clutter, so that both permanent echo cancellation and slow-moving target cancellation operate in the same area. Combination of both processes produces clutter-free signals except where the two forms of clutter overlap; in the overlapping area the smaller of the two clutter signals is displayed.

(3) In areas where MTI is not displayed, the video output is from the logarithmic signal channel which also includes a pulse length discriminator.

The selected video signals are then applied to a p.r.f. discriminator and then via the final channel selection circuits to the video output from channel 1.

48. Position 2 of the CHANNEL SELECTOR switch provides a semi-processed video output consisting of permanent echo cancelled MTI video within the circle area, without clutter switching, and of video from the logarithmic signal channel outside the circle area. The selected video signals are also subject to p.r.f. discrimination.

49. Video signals from the logarithmic signal channel with p.r.f. discrimination are applied all over the display with the CHANNEL SELECTOR switch in position 3.

50. Video signals from the linear signal channel are applied to the entire display with the CHANNEL SELECTOR switch in position 4. P.R.F. discrimination is used as for positions 1–3.

51. With the CHANNEL SELECTOR switch in position 5, the video output of a linear detector fed directly from the anti-jamming i.f. input is applied directly to channel 1. Since the linear detector operates from a separate power supply, this channel can be operated independently of the remainder of the signal processing equipment.

52. A second video output for the user's displays is provided on channel 2. This output is taken directly from the logarithmic signal channel and includes pulse length discrimination. P.R.F. discrimination is not used for this output.

53. The video output on channel 1 in positions 1–4 of the CHANNEL SELECTOR switch is modified when the LINEAR INJECTION (*para.* 19) facility is in use. This facility gives indication of the direction from which jamming is being received. In position 4 of the CHANNEL SELECTOR switch, the linear video output is modified by reverse swept gain. In positions 1–3 inclusive the video output is modified as stated in para. 19.

Monitor selection

54. Signal processing control and monitoring circuits are centred in a monitoring console suite fitted with three fixed coil displays and with the signal processing control panels. The three display consoles are situated adjacent to each other and with the right- and left-hand displays mounted at an angle of 45 degrees (in plan) to the centre display. By reference to these displays and to the trigger and indicator panels situated on a wired framework located near the monitor console suite, the signal processing operator is able to select the best video for transmission to the user's displays.

55. The left-hand monitor display, console 1, normally displays the video as transmitted to the operational displays on channel 1.

56. The centre display, console 2, displays video as selected by the operator from the following by operation of the MONITOR SELECTOR switch:

(1) In position 1 the display is the same as that on console 1.

(2) Linear video at the output of the linear channel, i.e. unprocessed video, which has been limited to reduce the intensity of clutter is displayed in position 2.

(3) MTI video is provided for the whole display in position 3. This display gives indication of the operation of the cancellation circuits and enables the doppler compensation circuits to be set up and adjusted for optimum effect at this stage of processing. Malfunction of the cancellation circuits might otherwise be masked by subsequent processing facilities.

(4) Position 4 displays the video output of the logarithmic signal channel as transmitted on channel 2 but without p.r.f. discrimination.

(5) The output of the anti-jamming signal channel is displayed with the MONITOR SELECTOR switch in position 5.

(6) Position 6 is a spare position and may be used for servicing purposes with test inputs connected to relay assembly M2 in the video cabinet.

57. Operation of the MONITOR SELECTOR switch does not affect the video transmitted on channel 1 as selected by the CHANNEL SELECTOR switch, but the video displayed on the monitor consoles, i.e. console 2 with the MONITOR SELECTOR switch in position 1 or console 1, is affected by operation of the CHANNEL SELECTOR switch.

58. The right-hand display, console 3, normally displays the video output of the linear signal channel. This video is completely unprocessed and shows the operator the full extent of clutter and interference as received at the linear i.f. input to the signal processing system.

59. A facility is provided whereby the video displayed on consoles 2 and 3 can be interchanged in the event of a failure of either display.

60. The monitor displays have normal expansion and off-centering facilities. A separate video input is provided on the display for console 2 for circle and rectangle markers. Intertrace facilities are provided on console 2 so that dot markers indicate rectangle corners during adjustment of position or size of rectangles.

Technical control and monitoring

◀**61.** The −250V regulators for the i.f., cancellation, Doppler and video cabinets must be switched on individually by spring-loaded keys. Remote controls and remote monitoring facilities are also provided for the radar transmitter/receiver and the aerial turning gear.

62. Monitoring equipment for certain sections of the Type 84 radar system is contained in a wall-mounted rack situated within the view of an operator seated at the monitor consoles. The rack accommodates three panels and provides indicator lamp supplies for the panels together with the station auto-align relays, fuses and distribution blocks. A further small unit is mounted on the wall at the lower right-hand corner of the rack.

63. The indicator panel, at the top of the rack, takes the form of an illuminated mimic diagram and provides visual indication of the availability of the inputs to the signal processing system, of the serviceability and availability of the various units in the system and of the video selected by the operator for the operational displays. The lamp indications on the panel are modified by the operation of fault relays in the signal processing cabinets and also by the operation of switches, one for each unit, on a control panel adjacent to the signal processing cabinets. The control panel provides a means of informing the operator of the availability state of the panels in the cabinets in order that the appropriate video can be selected.

64. The trigger panel, on the right-hand side at the bottom of the rack, provides remote control and monitoring facilities for the radar transmitter/receiver, and the signal processing equipment. In the non-linesman version of the trigger panel indication is given of p.r.f. A and B condition. In the linesman version no indication is given on Type 84 equipment. Lamp indications are given of the operational state of the trigger equipments as a whole. Fault indication is also given for each frame in each of the cabinets except the power cabinet and a general fault indication by a flashing lamp: the latter indication is repeated on the control panel. The panel control (fault override), mounted at the lower right-hand corner of the rack, enables the operator to store the fault indication by operating an appropriate switch which also resets the fault lamp so that it may indicate, by flashing, further faults.

65. By observation of the indications given by the panels it is possible to determine the approximate location of a fault, i.e. to the frame of a particular cabinet, and to determine the available signal processing facilities.▶

Test equipment

66. Items of test equipment for routine testing are included in the signal processing cabinets. These items include the following:—

(1) An i.f. signal generator which produces—

(*a*) 10 microseconds 13·5 Mc/s pulses commencing at 0 microseconds,

(*b*) 13·5 Mc/s pulses gated by 10 microsecond pulses occurring 50 to 1500 microseconds after the 0 microseconds pulse, and

(*c*) 1000 microseconds pulses starting at 0 microseconds. The gating pulses are received from the video signal generator. Pulses of 10 microseconds at 13·5 Mc/s are also produced at a p.r.f. adjustable between 4 and 30 times the system p.r.f.

(2) A video signal generator which produces the gating waveforms for the i.f. signal generator and also a waveform consisting of combined 10 microseconds and 1000 microseconds waveforms with variable amplitude.

(3) A noise amplifier assembly which produces a noise output of not less than 300 millivolts.

(4) A push-button attenuator variable in 1 dB steps between 0 and 99 dB.

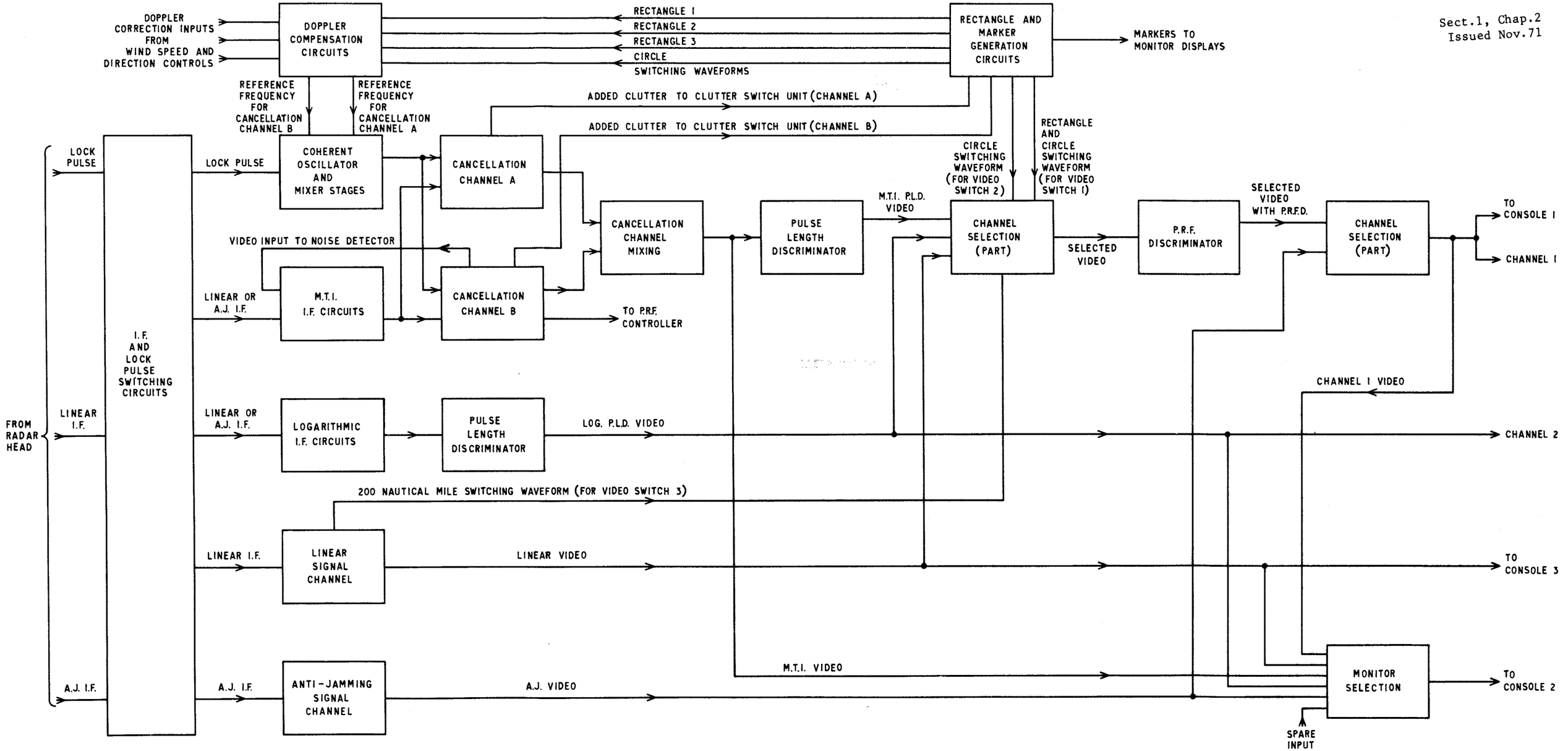


Fig. 1

Functional block diagram of Type 84 signal processing system

Fig.1

Chapter 3

CANCELLATION CHANNELS AND P.R.F. DISCRIMINATION

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

Introduction

1. Two cancellation channels (A and B) are used in the signal processing system. The channels are similar in operation, the main difference being that within a range of about 50 nautical miles from the station, channel A has no doppler compensation applied (and therefore cancels permanent echoes) whereas channel B may have doppler compensation applied in selected portions of the area and thus cancels slow-moving echoes. The outputs from the two channels are combined in a coincidence detector and the smaller of the two signals is passed to video switching circuits.

2. The output from one of three signal channels, i.e. cancellation, log-PLD and linear is selected by the video switching circuits and applied to a p.r.f. discrimination circuit. In this circuit signals which are not synchronized with the p.r.f. are eliminated.

3. A functional block diagram of the cancellation channels and the p.r.f. discrimination circuits showing their relationship with the remainder of the signal processing system is given in fig. 4.

Cancellation channels (*fig.* 4)

4. Each cancellation channel receives a bi-polar video input derived from a coherent demodulator. The amplitude and phase of each input is determined by the phase relationship of successive returned echo pulses to that of the i.f. reference input from the doppler compensation circuits. The circuits for the two cancellation channels are identical, except that channel B makes provision for the correction of the overall system p.r.f. in such a way that the interval between successive transmitter pulses is exactly equal to the delay time of the fixed delay cell regardless of temperature changes. The video output from the coherent demodulator for channel B is also used in the noise-operated a.g.c. circuits for the MTI channel as a whole.

5. The delay line driver for cancellation channel B receives the bi-polar video input from the coherent demodulator and also a −8 microsecond pulse from the p.r.f. generator circuits. In order that the −8 microsecond pulse can operate without interference from video signals, the coherent demodulator is made quiescent for the last 125 microseconds of the pulse repetition period.

6. Each cancellation channel virtually consists of two cancellation circuits in series but with each cancellation circuit utilizing the same fixed delay cell. The two cancellation paths are separated in the delay cell by the use of two carrier frequencies. In the first cancellation circuit the video output from the coherent demodulator modulates an 8·19 Mc/s carrier. The once-cancelled video output from the signal comparator then modulates a 6·14 Mc/s carrier for the second cancellation process. The two outputs from the delay line driver therefore consist of an 8·19 Mc/s carrier modulated by uncancelled video and a 6·14 Mc/s carrier modulated by once-cancelled video. These two outputs are combined in the first hybrid network (which also provides impedance matching for the fixed delay cell crystal transducer). Additional outputs at a level some 40dB lower than the output to the fixed delay cell are provided for two variable delay networks, one for the first cancellation circuit and the other for the second cancellation circuit. These networks are situated in a delay line (variable) unit and provide compensating delays, adjustable between zero and 0·7 microseconds to allow for manufacturing tolerances in the fixed delay cell.

7. The fixed delay cell provides a delay equivalent to one pulse repetition period (approximately 4mS) and the delayed output is fed to a further hybrid network providing two outputs, one to the signal comparator for the first cancellation circuit and the other to that for the second cancellation circuit. These outputs, together with those from the variable delay networks, provide delayed and undelayed inputs for each of the signal comparators.

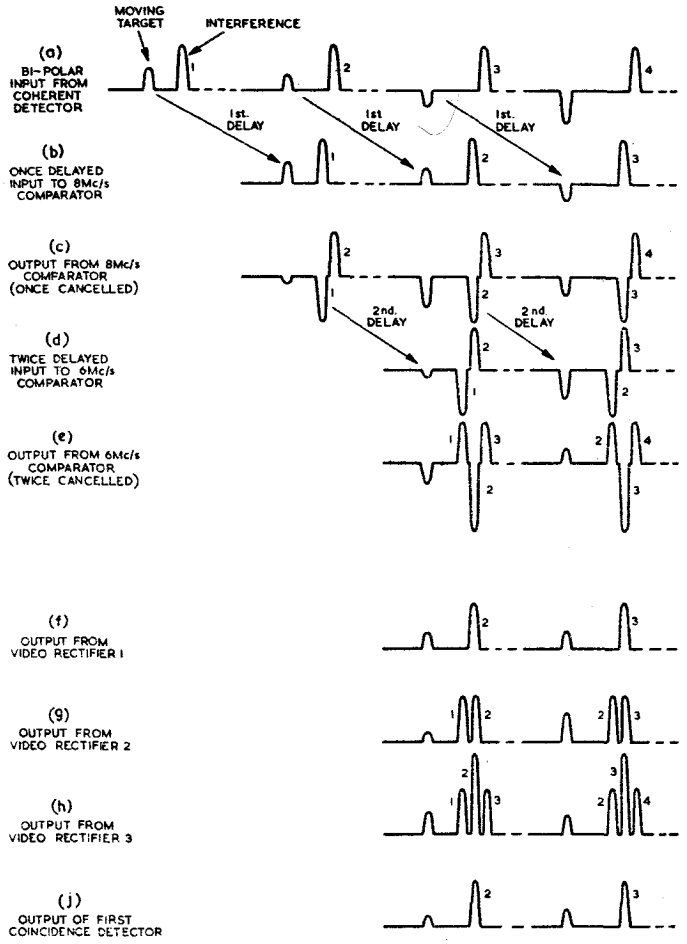


Fig. 1. Cancellation waveforms for channel A

8. It is convenient at this stage to relate the action of a cancellation channel to the waveform shown in fig. 1. The waveforms shown are those typical of channel A for a moving target echo and an interference pulse.

9. The relationship between the incoming pulses is indicated in waveform (a) which shows the returns associated with four successive transmitted pulses. The first signal comparator receives undelayed and delayed 8·19 Mc/s inputs, the envelope of the latter being shown in waveform (b). The two inputs are amplified and compared in a differential amplifier circuit which subtracts the delayed input from the undelayed input. The output is again bi-polar video, waveform (c), resembling that of the coherent demodulator but with the permanent echoes cancelled by about 17 dB, waveform (d). This output modulates the 6·14 Mc/s carrier in the delay line driver and provides the undelayed and delayed inputs to the second signal comparator; the envelope of the delayed input is shown in waveform (d). Comparison of delayed and undelayed inputs takes place in the comparator, the bi-polar output from which consists of moving target echoes and interference pulses, permanent echoes having been cancelled down to noise level, waveform (c).

10. The once-cancelled once-delayed, once-cancelled twice-delayed and twice-cancelled twice-delayed bi-polar video outputs, waveforms (c), (d) and (e), are each applied to video rectifier circuits in the video rectifier amplifier unit and thence to a coincidence detector circuit. The triple interference pulses produced as a result of the double cancellation are now reduced to one, as shown in waveform (j). Reduction to single interference pulses is necessary for p.r.f. discrimination purposes.

11. An output, in which the clutter waveforms are added instead of subtracted, is provided by the first signal comparator. This output is used in the electronic clutter switch unit for the production of the clutter switching and angel switching waveforms which are fed to the area switching panel. These waveforms are used when the cancelled video is clutter switched on the displays.

12. A similar cancellation process is followed in channel B. The difference between the outputs from the two channels is that for channel A permanent echoes are cancelled in the circular area, whereas for channel B doppler compensation may be applied where a rectangle overlaps the circular area—so that returns from slow-moving clutter are cancelled and permanent echoes are uncancelled in the overlapping area. Outside the circular area the same cancellation applies to both channels.

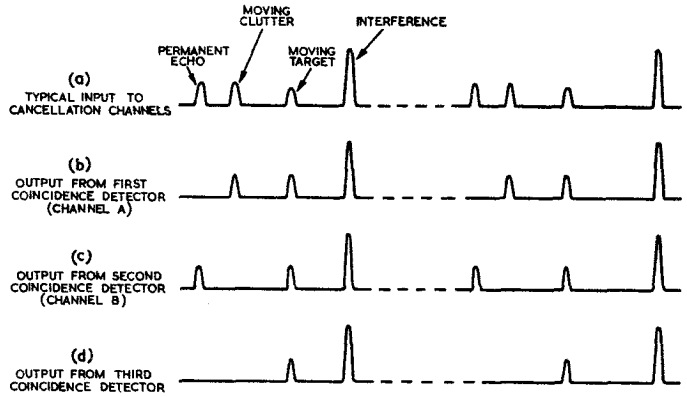


Fig. 2. Combination of two cancellation channels

13. A typical input to the cancellation circuits is shown in fig. 2(a) and typical outputs from the two cancellation channels are shown in waveforms (b) and (c). These two outputs are applied to a coincidence detector so that coincident pulses, such as would be the result of moving targets and interfering pulses, are passed on to subsequent circuits. However non-coincident pulses, such as those obtained from permanent echoes (channel B) and slow moving clutter (channel A) are eliminated. Should permanent echoes and slow moving clutter coincide, the resultant output from the coincidence detector will be the smaller of the two inputs.

14. The cancelled video output is passed via a pulse delay network and a video signal comparator to the video switching circuits.

P.R.F. correction (*fig.* 4)

15. It is essential for correct cancellation that the time interval between successive transmitted pulses should correspond exactly to the delay time of the fixed delay cell. Two delay paths are provided, one for channel A and the other for channel B, in the same delay cell so that the delays are subject to similar temperature changes. It is therefore only necessary to effect p.r.f. correction for one delay path and in this instance that for Channel B is chosen.

16. A −8 microsecond pulse, which occurs during the period when the coherent demodulator is quiescent, is fed ◀from the p.r.f. system▶ to the 8·19 Mc/s modulator in the delay line driver for channel B. This pulse then follows the same delay paths as those for the video signals and is applied with them in delayed and undelayed form to the first signal comparator and thence, after amplification, to the p.r.f. controller.▶◀The p.r.f. controller compares the time interval, which represents error, between delayed and undelayed pulses and modulates the phase of a 500 c/s output according to the direction of p.r.f. correction to be applied to correct the error. This output, together with a fixed 500 c/s from the reference frequency generator, provides the motive power for a two-phase motor driving, through a reduction gear, a tuning capacitor across the crystal oscillator in the◀p.r.f. system.▶This action continues until the p.r.f. matches the delay time of the cell, i.e. when delayed and undelayed pulses coincide, so that no 500 c/s output is produced by the controller.

P.R.F. discrimination circuits (*fig.* 4)

17. The p.r.f. discrimination circuits receive an input from the video switching circuits according to the setting of the CHANNEL SELECTOR switch on the display console and pass a video output to channel 1 and console 1 in positions 1–4 of the switch (*Chap.* 4).

18. The selected uni-polar video input is first applied to the 8·19 Mc/s section of a driver delay line, identical to those used in the cancellation channels, where it modulates the carrier. The delay line driver also accepts a −8 μs timing pulse. The circuits for production of delayed and undelayed inputs for the signal coincidence comparator are simpler than those in the cancellation channels in that no variable delay network is used, the video input to the delay line driver being fed directly to the comparator and the hybrid networks used for matching purposes only.

19. As in the cancellation circuits a need exists for an accurate match between the p.r.f. and the delay time of the fixed delay cell. Since, however, the p.r.f. is already controlled by circuits associated with cancellation channel B, it is necessary in this instance to control the length of the delay path in the delay cell. This is done by means of a p.r.f. controller similar to that used to control the p.r.f. but using the 50 c/s mains supply as the motive power for the delay cell motor.

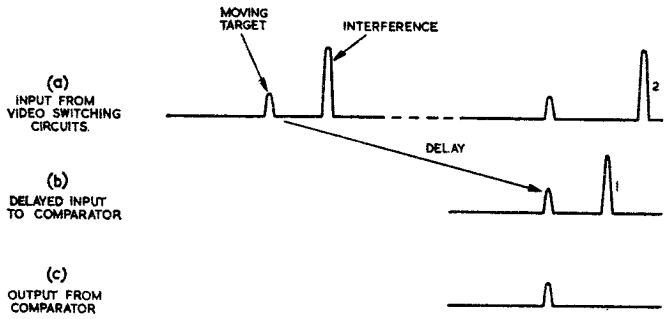


Fig. 3. P.R.F. discrimination waveforms

20. Typical waveforms such as would be obtained in the p.r.f. discrimination circuits for a moving target return and a non-synchronized interference pulse are shown in fig. 3 (a). The envelope of the input modulating the 8·19 Mc/s carrier and delayed by one pulse recurrence period is as shown in waveform (b). The two waveforms are applied to a coincidence detector circuit so that the output is as shown in waveform (c), the moving target return being passed on to subsequent circuits whereas the interference pulses have been eliminated.

Noise attenuator

21. A pulse fed to either leg of a coincidence detector allows noise on the other leg to be passed at full strength so that the pulse is visible in the output as a 3 dB increase of noise. This effect is minimized by feeding the coincidence detector inputs to a subtraction circuit via an OR gate together with the output from the coincidence detector. When non-coincident pulses are received by the coincidence detector an output is produced by the subtraction circuit and is used to operate an electrically switched attenuator. The output is reduced by 3 dB and the noise thus increased by the pulse is restored to normal. This type of switched attenuator is used in the video amplifier rectifier associated with the MTI circuits and in the signal comparator associated with p.r.f. discrimination.

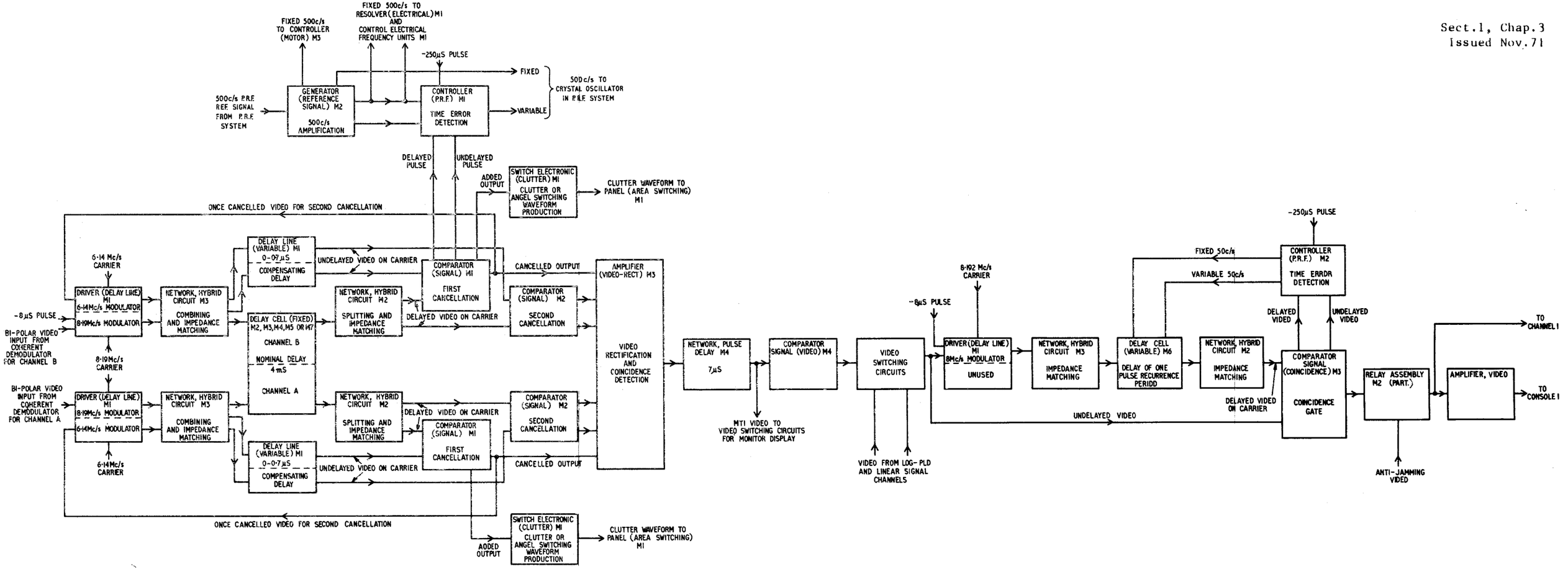


Fig.4

Cancellation channels and P.R.F. discrimination circuits

Fig.4

Chapter 4

SIGNAL CHANNELS AND VIDEO SWITCHING

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

Introduction

1. The i.f. signals at 13·5 Mc/s are received by the signal processing equipment from two sources, one from the linear head amplifier and the other from the anti-jamming receiver. An i.f. lock pulse is also received from the radar transmitter/receiver.

2. The signals undergo various degrees of signal processing in four signal channels and are then fed to the video switching circuits whereby the operator selects the best combination of video outputs to suit the prevailing conditions. Selection is made by reference to three monitor displays so that the video output at channel 1, which provides the users display, shows the maximum number of targets both in clear conditions and in the presence of clutter or jamming. A second video output for the user is provided directly from the log-PLD signal channel.

3. The monitor display on console 1 shows the video sent to the user on channel 1. The display on console 2 is selected to show the video obtainable after certain stages of signal processing and is used when setting up the controls for doppler compensation. A third monitor display, console 3, provides a completely unprocessed display so that the extent and nature of clutter and jamming can be seen.

Signal channels (*fig.* 4)

4. The two i.f. inputs and the transmitter lock pulse are first brought in to the i.f. switch unit. This unit also accepts test signals and a lock pulse from the test equipment associated with the system. The two i.f. inputs are derived from the head amplifier which has broad band and narrow band outputs.

5. The i.f. switch unit incorporates electronically switched amplifiers under the control either of a relay circuit, energized by the ANTI-JAM switch on the control desk, or of the RAD.SIG. ON/OFF and TEST SIG. ON/OFF switches on the unit. According to the operation of these controls the i.f. inputs to the MTI and logarithmic signal channels may be selected from either the linear or anti-jamming i.f. inputs or from the test equipment. Since the i.f. input level for the logarithmic channel is too high for the MTI channel the output for the MTI channel is reduced in level by 15 dB. The linear i.f. input is directly connected to the linear signal channel but is also reduced in level by 15 dB. The i.f. input from the anti-jamming receiver is fed directly to the anti-jamming channel but, since this input is at a higher level than the linear i.f. input, is reduced in level by 6 dB before it is applied to the appropriate switched amplifier and thence to the MTI and logarithmic channels.

6. Selection of the lock pulse, fed to the coherent oscillator, is made by a TEST/NORMAL switch on the switch unit so that under normal operating conditions the lock pulse is received from the radar transmitter/receiver. Under test conditions the lock pulse is obtained from the test equipment.

MTI channel

7. The i.f. signal from the switch unit is first amplified in an electrical noise limiter which may be negatively biased by either a swept gain waveform the amplitude of which is controlled by the SWEPT GAIN switch on the control desk, or a noise detector, subject to the setting of a four-position switch situated on the electrical noise limiter in the i.f. cabinet. The positions of this switch are such that the gain of the amplifier may be either (a) fixed, (b) controlled by the noise level remaining over the second half of the trace after coherent demodulation of the signal, (c) subject to a swept gain law which follows the optimum form in consideration of the aerial polar diagram or (d) whichever of the two bias voltages is the greater as selected by an OR gate. An approximation of the swept gain law is :

(1) A fourth power law from zero to forty miles.

(2) Constant 15 dB from forty to eighty miles.

(3) A fourth power law from eighty to one hundred and twenty miles.

8. Further amplification takes place in an amplifier employing instantaneous automatic gain control in such a manner that i.f. input signals ranging in level from 6 to 40 dB above noise are compressed to within 14 dB, amplification of signals up to 6 dB above noise being linear.

9. The output of large signals is further compressed to 14 or 8 dB above shoulder noise by circuits in an i.f. amplifier, under the control of the BLIND VELOCITY BAND switch on the control desk. Ratios of 20 dB, 14 dB, or 8 dB are thus obtained so that, after subsequent cancellation, the blind velocity bands of 9, 13, or 19 knots occur. The appropriate band may be selected by the switch.

10. The lock pulse, derived from the transmitter pulse, sets the coherent oscillator in oscillation so that its starting phase is coherent with the transmitter pulse. The nominal frequency of the coherent oscillator is 13·5 Mc/s but this may be reduced by 100 kc/s to provide coherent low i.f. The output of the coherent oscillator is applied to the coherent demodulators via the doppler compensation circuits (*Chap.* 5).

11. The cancellation circuits are the subject of a separate description (*Chap.* 3). After cancellation, the video is delayed by 7 microseconds before application to a signal comparator unit. This delay is necessary since the clutter switching waveform subsequently used in the video switching circuits is delayed by 26 microseconds. A delay of approximately 9 microseconds has occurred in the MTI channel up to this point and the signal comparator has an inherent delay of 12 microseconds : a further delay of 7 microseconds is therefore added to ensure that the clutter switching facility operates before the arrival of the video.

12. The signal comparator unit contains the circuits in which the high level d.c. due to c.w. jamming is eliminated. The cancelled video obtained from this signal channel provides one of the two video inputs to video switches 1 and 2 for fully processed and semi-processed signals respectively.

Log-PLD channel

13. The i.f. signal from the switch unit is first amplified by a logarithmic amplifier, the characteristics of which are such that the relationship between input and output levels is logarithmic with an input dynamic range of 90 dB and a maximum non-limited gain of 100 dB. Since rectification occurs in each of the six stages of the amplifier the output is video and is applied to a video sweep generator unit.

14. The sweep generator unit incorporates swept gain and noise level control, the swept gain law being approximately the same as that used in the MTI channel. The amount of swept gain applied is remotely controlled from the SWEPT GAIN switch on the control desk so that the amount used may be increased in three equal steps from zero to maximum. The amount of swept gain used also depends on the strength of noise received in the output from the logarithmic amplifier, since target signals decrease in amplitude with increase of noise. The biasing voltage is therefore decreased with increase of noise level input.

15. A delay of 16 microseconds is introduced into the channel at this stage which, together with the inherent delay in the signal comparator which is next in circuit, matches the overall delay in the channel with that in the circuits producing the clutter switching waveform.

16. The signal comparator unit contains the pulse length discrimination circuits in which any signals with a pulse length of more than twice the transmitted pulse length, i.e. clutter signals, moving or stationary, are suppressed. Its video output is used to provide one of the two alternative video inputs for video switches 1 and 2, one of the video inputs for video switch 3 and also the video output to the user on channel 2 via a video amplifier.

Linear channel

17. The linear channel accepts the i.f. input from the linear radar receiver at the same level as that applied to the MTI channel. Under normal circumstances, i.e. with the LINEAR INJECTION switch on the control desk unoperated, the gain of the i.f. amplifier is linear up to a maximum of 82 dB with a manual gain control range of 40 dB. After amplification the i.f. signals are detected in a linear demodulator unit. The resulting video output is then delayed by 26 microseconds for reasons previously described , there is an inherent delay of 2 microseconds in the linear channel and therefore a compensating delay of 26 microseconds is applied by a delay network so that the total delay in the channel becomes 28 microseconds.

18. With the LINEAR INJECTION switch on the control desk operated, the gain of the i.f. amplifier is controlled by a reverse swept gain waveform which commences at a range of 200 nautical miles. The gain of the amplifier is therefore linear for the first 200 nautical miles after which it is decreased with range. Returns from sources of jamming are

thus progressively decreased so that those from the point source of interference are strongest on the bearing of the source of jamming. The reverse swept gain waveform is produced by the reverse sweep generator which is itself triggered by the switching pulse generator producing the switching waveform for the third video switch.

19. The video output from the linear channel provides the second video input to video switch 3 and the unprocessed display which is always available on console 3.

Anti-jamming channel

20. The anti-jamming channel accepts the i.f. input from the anti-jamming radar receiver and this is fed directly to a linear demodulator unit identical to that used in the linear channel. Previous i.f. amplification is not necessary in this case as the level of the anti-jamming receiver input to the channel is much higher than that received from the linear radar receiver. The video output from the demodulator is delayed 28 microseconds in order to match the overall video delay in this channel with that in the other signal channels.

21. The linear demodulator unit in this channel operates from an independent +250V and −250V power supply so that this channel may be operated independently from the remainder of the signal processing system. By this means, an emergency video is provided on channel 1 with all video switching circuits inoperative.

Video switching (*fig.* 4)

22. The outputs from the signal channels are selected by a series of three video switches, controlled by gating waveforms, and two relay assemblies, controlled by the VIDEO SELECTOR, MONITOR SELECTOR and LINEAR INJECTION switches on the control desk, for transmission to the user on channel 1 and for display on console 2. An additional facility on the operators console suite is that in which the displays on consoles 2 and 3 may be interchanged by the operation of the DISPLAY EMERGENCY CHANGEOVER switch on the console suite to the STANDBY position.

Video switch units

23. The video switch units are so arranged that in the absence of a gating waveform they pass a background signal which is the video output from the logarithmic signal channel in the case of switch units 1 and 2 and the output from the linear channel for switch unit 3.

24. Video switch 1, which provides the output (via the p.r.f. discrimination circuits) for the fully processed display, is supplied with a composite switching waveform from the area switching panel.

25. The area switching panel, which forms part of the doppler compensation circuits since it also controls the application of doppler compensation in rectangular areas, combines a switching waveform with a duration of approximately 50 nautical miles for the permanent echo circle with those for the three rectangles and also generates the circle and rectangle markers for the monitoring display. Rectangular waveforms are only present in the composite waveform if the appropriate LOCAL/USERS switches are operated to their USERS positions. These waveforms provide one input to a coincidence gate, the other input to which consists of clutter-switching waveforms from the two electronic clutter switches. With clutter switching in operation a switching waveform output to the video switch is produced only when circle or rectangular waveforms and clutter waveforms coincide. With clutter switching inoperative the whole of the circle and rectangular waveforms is passed to the video switch.

26. Video switch 2, which provides the output (via the p.r.f. discrimination circuit) for the semi-processed display, is supplied with the circle switching waveform, with no clutter switching. The video outputs from switches 1 and 2 therefore consist of log-PLD video in background areas with MTI video where a switching waveform is applied.

27. Video switch 3, the output from which is only used when the LINEAR INJECTION switch is operated, is supplied with the 200 nautical mile switching waveform, this being the waveform used to trigger the reverse sweep generator. The video output from the switch consists of Log-PLD video from 0 to 200 nautical miles and the output of the linear signal channel with a decreasing gain characteristics after 200 nautical miles.

28. The outputs of all three video switches are applied to the video switching circuits in the M2 and M3 relay assemblies.

Channel I

29. The video output to channel 1 may be selected by means of the VIDEO SELECTOR switch on the control desk to provide the best possible display according to the prevailing conditions. The switch has five positions so that the operator can select five degrees of signal processing :—

(1) *Fully processed.* In position 1 of the switch the user receives the best display that can be produced under given conditions. Such a display is that in which three rectangles are in use (*fig.* 1). The centre circle defines the area within which cancellation channel A is doppler compensated so that permanent echoes are cancelled. Where the circle is overlapped by rectangle 1 channel B is doppler compensated for the velocity of rain. Rain and permanent echoes are cancelled where they overlap, the minimum clutter signal being shown on the display. In rectangle 1 outside the circle, channels A and B cancel rain. In rectangle 2, both channels are compensated for window and in rectangle 3 anomalous propagation is cancelled without doppler compensation. Precedence of rectangle 1 over 2 and 2 over 3 is illustrated in fig. 1, where the boundary markers for rectangles 2 and 3

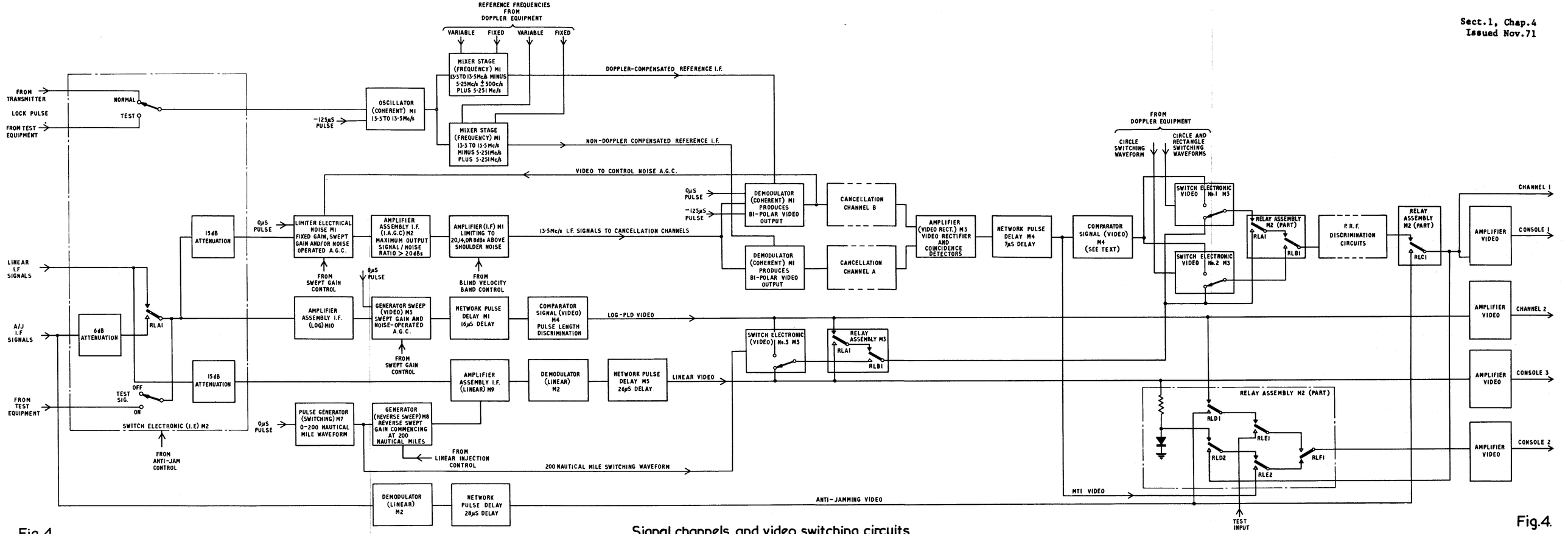


Fig.4.

Signal channels and video switching circuits

Fig.4.

Chapter 5

DOPPLER COMPENSATION

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

Introduction

1. The Type 84 signal processing equipment incorporates two cancellation channels—A and B. The facilities provided by the channels differ only in the type of cancellation applied in the centre circular area (hereafter referred to as the circle) in that channel A cancels permanent echoes only, whereas channel B cancels permanent echoes *and* permits cancellation of unwanted returns from slow moving echoes in selected areas. Outside the circle, the cancellation in both channels is the same. The areas in which cancellation of slow moving echoes is effective are in the form of rectangles and these may be adjusted in position and size to cover the areas of moving clutter. In order to achieve cancellation of slow moving echoes, doppler compensation may be applied in each of three rectangles according to the mean wind speed and direction in the particular area. Use is thus made of the regions of blind velocities to cancel echoes due to rain, window or angels. In order to make due allowance for turbulence of clutter, the width of the region of blind velocities may be set to 9, 13 or 19 knots by control of the amount of compression in the i.f. amplifier circuits preceding the coherent demodulator stages.

2. Cancellation of overlapping fixed and moving clutter within the circle area is achieved by the use of two cancellation channels. A rectangle is made to overlap the circle and the doppler compensation in the rectangle area is adjusted to cancel the moving clutter in channel B. The outputs from the two channels are fed to a coincidence detector which passes the smaller of the two signals. Where the two types of clutter do not coincide the clutter is fully cancelled.

3. In order to reduce the loss of wanted echoes the outputs from the cancellation circuits may be clutter-switched. With clutter switching in operation doppler compensation is still applied to the whole of each rectangle but the video switching circuits are operated by a clutter signal derived from an addition circuit in the first cancellation unit. Under these circumstances the circle and rectangles merely define the area in which clutter switching may take place.

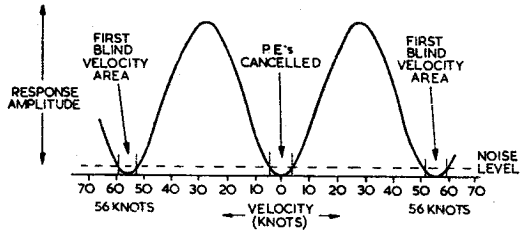


Fig. 1. Basic response pattern

Doppler compensation

4. The response of the triple-pulse MTI system follows the pattern shown in fig. 1. By injection of a doppler compensating frequency corresponding to the wind velocity, the whole response pattern is moved as shown in fig. 2. Each rectangle may have a different compensating velocity vector applied to it and each is separately adjustable in size and position. As the aerial rotates, the radial velocity of rain changes according to a cosine law so that the doppler compensating frequency must be modulated by a magslip resolver driven at aerial rotational speed. The response pattern is therefore moved sinusoidally along the velocity axis about the position at which it is set by the doppler compensation controls.

5. The rotor of the resolver, electrical M1 (*Sect.* 7, *Chap.* 3) is fed with a 500 c/s supply from the reference signal generator (*Sect.* 3, *Chap.* 11) and is driven at aerial rotational speed (*fig.* 7). The outputs from the stator windings of the resolver are 500 c/s sine and cosine waveforms which are amplitude modulated due to aerial rotation and these are applied to the stator windings of three magslips on the control console. The rotors of these magslips may be set to the angle appropriate to the wind direction compensation required. The amplitude of the 500 c/s output from the rotors is set by a potentiometer to apply the required wind speed compensation.

6. The output from each magslip rotor is applied to an electrical frequency control unit (*Sect.* 4, *Chap.* 11). There it is compared in phase and amplitude with a fixed 500 c/s input in a phase sensitive rectifier circuit to produce the controlling d.c. potential required to modulate the frequency of a quartz crystal reference oscillator (*Sect.* 4, *Chap.* 9).

7. The nominal frequency of the output from the oscillator is 5·25 Mc/s and is varied between limits of ±500 c/s by the d.c. output from the phase sensitive rectifier.

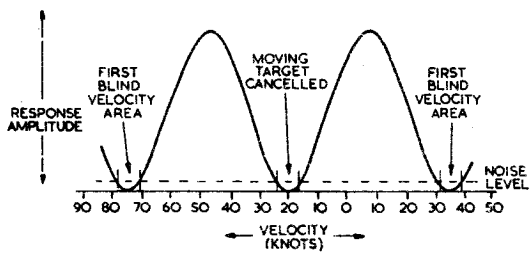


Fig. 2. Response pattern with doppler compensation (20 knots) frequency shift 89 c/s

8. With no doppler compensation applied, there is no output from the phase sensitive detector, so that the output from each variable oscillator is at a frequency of 5·25 Mc/s. Under these circumstances the difference frequency between the output of any variable oscillator and that of a fixed reference oscillator with an output frequency of a nominal 5·251 Mc/s (5·25 Mc/s+4×p.r.f.) should be a nominal 1000 c/s (4×p.r.f.). As this corresponds to the fourth blind speed it does not introduce any doppler compensation and only stationary echoes are cancelled (*fig.* 3). The difference frequency of 1000 c/s is a convenient mid-frequency for the discriminator in the feedback circuit, which thus operates between 500 and 1500 c/s. This difference is maintained, should either oscillator drift in frequency due to temperature variation, by a feedback loop completed by a frequency discriminator via a mixer circuit which receives fixed and variable reference frequencies as its inputs. The d.c. error voltage output from the frequency discriminator is subtracted from that of the phase sensitive rectifier so that, should either of the reference oscillators tend to drift in frequency, the output from the frequency discriminator modulates the frequency of the variable reference oscillator. By this means the correct frequency difference is maintained between the outputs of the two oscillators.

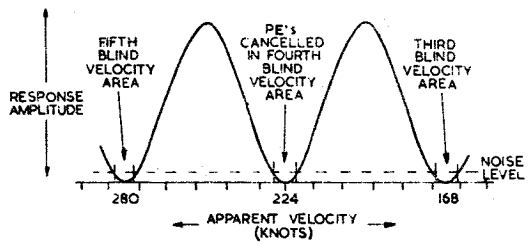


Fig. 3. Response pattern as used with Type 84 system, frequency shift 1000 c/s

9. The outputs from the four reference oscillators, one fixed and three variable, are fed to the first of two electronic reference frequency switches (*Sect.* 4, *Chap.* 8) in which identical switching circuits, connected in series, are operated by the rectangle switching waveforms when the rectangles are in use. The arrangement of the switches is such that an order of precedence exists between the rectangles, rectangle 1 taking precedence over rectangles 2 and 3 and rectangle 2 over rectangle 3.

10. Application of the rectangle switching waveforms to the reference frequency switch is under the control of the LOCAL/USERS switches, one for each rectangle, on the control desk. If none of the LOCAL/USERS switches are operated, no rectangle waveforms are applied to the reference frequency switch, so that the output from the fixed reference oscillator is applied to the mixer stage for channel B and also to the second reference frequency switch. Since the second switch feeds channel A, no doppler compensation is applied to either cancellation channel.

11. Operation of any one or more of the LOCAL/USERS switches causes the appropriate switches on the reference frequency switch to be operated so

that the doppler compensated reference frequency is fed to the mixer stage for channel B in the appropriate rectangular areas and also to the second reference frequency switch. Since the latter is operated by the circle switching waveform at all times, the output from the fixed reference frequency oscillator is fed to the mixer stage for channel A in the circular area : outside the circular area the reference frequencies for channel A are the same as for channel B.

12. Where rectangles overlap, the appropriate switches are operated, but as the switch for rectangle 1 follows these for rectangles 2 and 3, the doppler compensated frequency for rectangle 1 will appear at the output of the switch unit where rectangles 1 and 2 or 1 and 3 overlap. Similarly the doppler compensated reference frequency for rectangle 2 appears where rectangles 2 and 3 overlap.

13. Cancellation of slow moving clutter in subsequent cancellation channels is achieved by making the amplitude and phase of the returns from consecutive transmitted pulses equal at the output of the coherent demodulator. In order to achieve this, the i.f. reference frequency applied to the coherent demodulators is shifted by an amount equivalent to the doppler frequency caused by the radial velocity of the moving clutter. A separate mixer stage is used for each of the two cancellation channels. The output from the coherent oscillator, at a nominal frequency of 13·5 Mc/s, is first mixed with the output from the appropriate reference frequency switch ; in rectangular areas the frequency of this output is 5·25 Mc/s plus a doppler compensation component f_d, the latter varying between the limits of $\pm$500 c/s. The resultant frequency is 8·125 Mc/s minus f_d and this is in turn mixed with the output of the fixed reference oscillator at a nominal 5·251 Mc/s to give an output from the mixer stage to the coherent demodulator at a frequency of 13·501 Mc/s minus the doppler component f_d. With no rectangles in use, and in areas outside rectangles, the i.f. reference frequency input to the coherent demodulator is the same as the output from the coherent oscillator since the reference frequency inputs to the mixer stages are both at a frequency of 5·251 Mc/s (nominal).

14. Doppler compensation may thus be applied to cancellation channel B in all rectangular areas and to cancellation channel A in rectangular areas outside the circle. It should be noted that compensation is applied over the whole area in question and is not affected by the clutter-switching facility since this applies to video switching circuits only.

Adjustment of rectangle position and size

15. The position or size of a particular rectangle may be adjusted by manipulation of the joystick control on the control desk with the MOVE/SIZE switch operated to the required position. Operation of the switch on the top of the joystick causes relay RLE in the electronic joystick switch unit (*Sect.* 4, *Chap.* 5) to be energized (*fig.* 8). D.C. outputs from the X and Y potentiometers in the joystick are then applied to two pairs of Schmidt trigger circuits controlling four relays in the electronic switch unit. With an input of less than 6V from either of the joystick potentiometers only one relay in each pair is operated, so that no through path is provided for a fixed 500 c/s supply to the motor assemblies. When the input to the Schmidt circuits exceeds 6V both relays in each pair are either operated or released to connect the fixed 500 c/s to the motor assemblies.

16. A 500 c/s supply, controllable in phase and amplitude according to the d.c. input from the joystick potentiometers is provided by the motor controller (*Sect.* 4, *Chap.* 4) and also fed to the three motor assemblies.

17. Since the MOVE/SIZE switch for the particular rectangle is already operated, the fixed and variable 500 c/s supplies are available, via. operated relay contacts, to the X and Y move or size motors according to the switch position selected. The motors then rotate until the rectangle is adjusted to the required position or size when the movement is terminated by releasing the joystick button. In order to facilitate this adjustment, dot markers are made available on console 2 as soon as the MOVE/SIZE switch is operated. The motor drive shafts are coupled to the move and size potentiometer sliders and the positions of the sliders determine the d.c. levels into the rectangle pulse generator (*Sect.* 4, *Chap.* 2) and thence to the intertrace equipment.

Rectangle reset facility

18. A facility is provided whereby the position and size of the rectangles may be set according to the setting of four cam-operated micro-switches on the motor assembly. This is achieved by operating the appropriate RESET switch, one for each rectangle, on the control desk. Relay E on the electronic joystick switch is operated by contacts of the RESET switch. Relay A on the motor controller is similarly operated to connect a fixed negative d.c. potential to the Schmidt circuits so that fixed 500 c/s supplies are fed to the motor assemblies. The move and size motors on the appropriate motor assembly are fed with 500 c/s fixed supplies via the operated contacts of the move and size relays, these being energized via the operated contacts of a RESET relay, itself energized by the RESET switch and the micro-switch. The sequence is such that the MOVE motor turns until the move micro-switches are opened by the cam, the move relays are then released and the size motors then turn until the size micro-switches are opened. The rectangle is then set at a position and size determined by preset adjustments to the cam-operated micro-switch and no further action takes place until the MOVE/SIZE switch is again operated.

Production of rectangles

19. The foregoing paragraphs have described the method of production of the doppler compensation frequencies and their application to the cancellation

channels. The following paragraphs describe the production of the waveforms used to gate the reference frequencies into the mixer stages and to operate the video switching circuits.

20. Production of a single typical rectangle is illustrated in fig. 4 from which it is apparent that as the trace sweeps over the display the time intervals involved between the sides of the rectangles as traversed by the trace and the beginning and end of the trace change from trace to trace.

21. Production of a rectangle may be considered as the production of two segments AA′, BB′, CC′ and DD′, one in the X axis and the other in the Y axis across the face of the display, the rectangle being formed at the common intersecting point of the

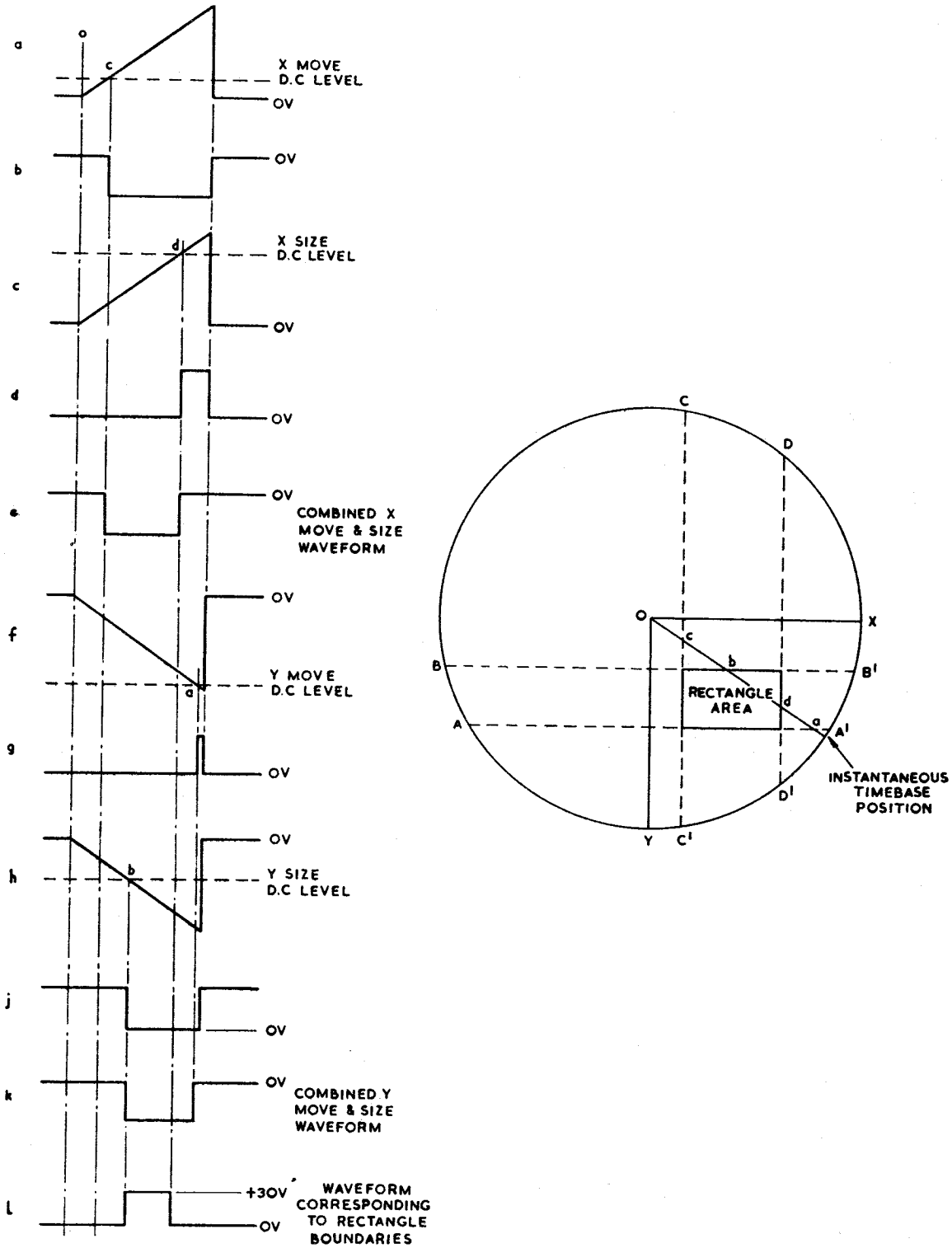


Fig. 4. Rectangle waveform generation

two segments by a suitable gating circuit. The position of the rectangle is determined by AA′ and CC′ and the size by BB′ and DD′, these boundaries being set by d.c. levels originating in one of three motor assembly units (*Sect.* 4, *Chap.* 3) and applied to one of three rectangle pulse generators (*Sect.* 4, *Chap.* 2).

22. For each intersection of the trace with the boundaries of the segments illustrated, a rectangular waveform is produced commencing at the point of intersection and with its trailing edge at the end of the trace. Each waveform is produced by gating the X or Y resolved timebase with the X or Y d.c. level from the motor assembly (*waveforms a, c, f and h*). In each case the waveform determining the position of the rectangle is negative going (*waveforms b and j*) whereas the waveforms determining the size of the rectangle are positive going (*waveforms d and g*). These waveforms represent the distance Oc, Oa, Ob and Od respectively as measured along the trace. The X move and X size waveforms are combined, as are the Y move and Y size waveforms, to produce the composite waveforms e and k which represent distances cd and ab respectively. These two waveforms are finally combined in a coincidence gate to produce the final waveform l representing the distance bd.

Waveform generation

23. In a typical arrangement of rectangles and circle waveforms as shown in fig. 5, it is seen that rectangle 1 overlaps the circle and rectangles 2 and 3 and that rectangle 2 also overlaps rectangle 3. The arrangement whereby doppler compensation is applied to the cancellation circuits according to rectangle precedence has already been described

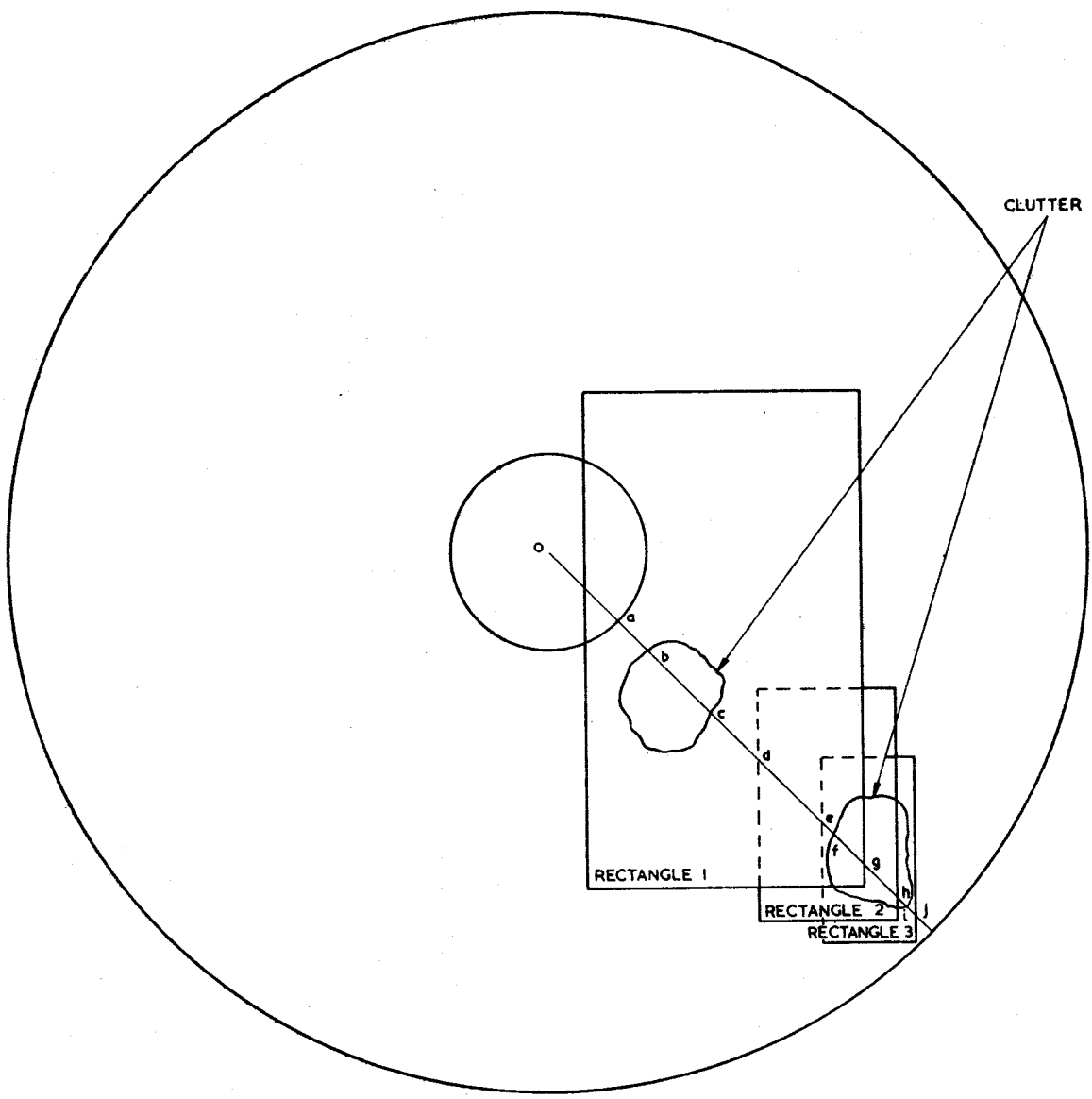


Fig. 5. Typical fully processed display

(*para.* 12). Circuits giving a similar order of precedence in the generation of markers and switching waveforms are included in the area switching panel (*Sect.* 4, *Chap.* 7) which also includes the clutter switching waveforms.

24. Rectangle markers and switching waveforms are produced under the control of three LOCAL/USERS switches, one for each rectangle, so that with the switch for a particular rectangle in the USERS position, both switching waveforms and rectangle markers are generated; with the switch in the LOCAL position, markers only are generated. The circle switching waveform and marker are generated regardless of LOCAL/USERS switch operation. With clutter switching in operation, as determined by the operation of the clutter switches for the circle and the three rectangles, marker waveforms are generated but the switching waveforms are used to gate the clutter waveforms received from the electronic clutter switches. A switching waveform is therefore only produced when clutter is present.

25. Fig. 5, shows a typical display such as would be obtained with all three rectangles in operation with clutter switching in the rectangular area. The trace starts at O and runs out to (a) at the periphery of the circle. In this area, cancelled video is displayed which is a combination of cancellation of stationary echoes and slow moving clutter from the two cancellation channels, the smaller of the two clutter signals being displayed. At (a) rectangle 1 takes precedence but since clutter switching is in operation no switching waveform is produced and the video displayed is log-PLD. A marker is produced to define the edge of the circle. The clutter switch operates at (b) so that the video displayed is cancelled video, doppler compensated according to the wind speed and direction setting for rectangle 1. Clutter switching ceases at (c) so that the display reverts to log-PLD video. Rectangle 2 overlaps rectangle 1 at (d) but since rectangle 1 takes precedence, no change takes place and no rectangle marker is produced. This occurs at (e) where rectangle 3 overlaps rectangles 1 and 2. The clutter switch again operates at (f) to display cancelled video with doppler compensation for rectangle 1. The trace reaches the boundary of rectangle 1 at (g) and as rectangle 2 takes precedence over rectangle 3 in the overlap area the cancelled video displayed is now doppler compensated according to the setting for rectangle 2. A rectangle marker is produced. At (h) the boundary of rectangle 2 is reached so that the cancelled video displayed is doppler compensated for rectangle 3 and a further rectangle marker is produced. Clutter switching ceases at (i) so that the display reverts to log-PLD video. The boundary of rectangle 3 is reached at (j) and a rectangle marker is produced. The displayed video remains log-PLD since no switching waveform is present.

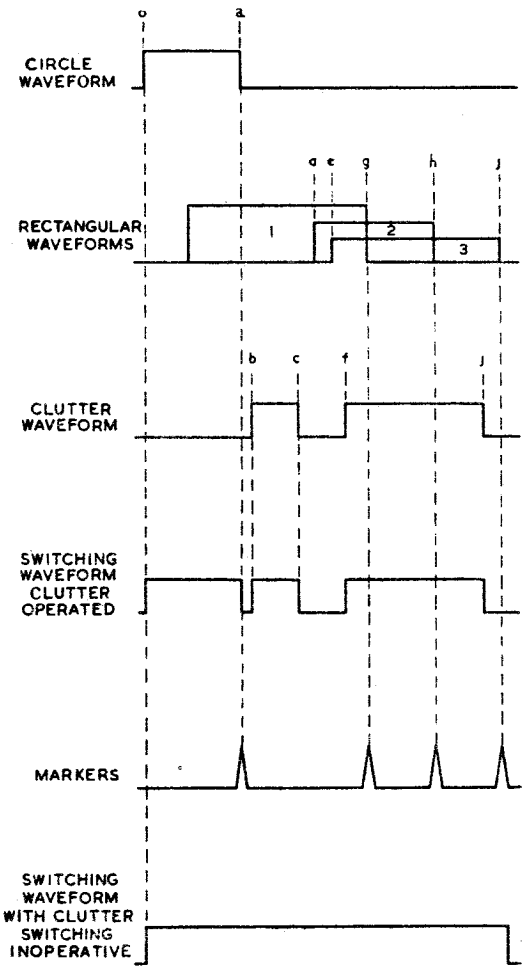


Fig. 6. Relationship between waveforms

26. With clutter switching inoperative the video displayed from a–g, g–h and h–j is cancelled video, doppler compensated according to the setting of the wind speed and direction controls for the respective rectangles.

27. The relationship between the original circle and rectangle waveforms and the markers and switching waveforms is shown in fig. 6.

Doppler compensation controls

28. The doppler compensation circuits described above are under the control of the WIND SPEED and WIND DIRECTION controls and the MOVE/SIZE and LOCAL/USERS switches on the control desk. The clutter switching facility is also mentioned here since the CIRCLE and RECTANGLE CLUTTER switches on the control desk directly affect the switching waveforms produced by the area switching panel. Although the WIND SPEED and WIND DIRECTION controls may be set to provide doppler compensation this is not effective until the LOCAL/USERS switches are operated. The marker and switching waveform for the circle is always produced so that the semi-processed video output to the user, with the CHANNEL SELECTOR switch on position 2, consists of cancelled video, without doppler compensation, in the circle and of log-PLD video elsewhere. The fully processed display, with the channel selector switch on position 1, will also have cancelled video in the circle unless circle clutter switching is in operation when the circle video is cancelled video, clutter-switched on a background of log-PLD video.

29. With the LOCAL/USERS switch unoperated the rectangles are not produced, no doppler compensation is applied to the cancellation channels and no rectangle switching waveforms or markers are produced. The video switch for the fully processed display is therefore unoperated so that the display consists of log-PLD video outside the circle.

30. The circuits concerned with operation of the various control switches affecting the doppler compensation circuits are shown in fig. 9 and the action of the circuits is summarized in Table 1, for control of rectangle position and size and in Table 2, for the application of doppler compensation.

31. The MOVE/SIZE and RESET switches are so interconnected that no reset circuit can operate when any MOVE/SIZE switch is operated and that the MOVE/SIZE switch for rectangle 1, when operated, makes those for rectangles 2 and 3 inoperative, as also does that for rectangle 2 with respect to rectangle 3. The circuit action takes place in the rectangle pulse generator and motor assembly for the rectangle under consideration, the units concerned with the other two rectangles remaining inoperative, since only one rectangle can be adjusted at a time.

32. The rectangles can be adjusted for test purposes by a LOCAL JOYSTICK control on the motor controller with the MOTOR CONTROL switch on the unit in the LOCAL position. The NORMAL/MOVE switches on the motor assemblies are set to the MOVE position for this operation, a separate switch being provided for each motor on the assembly. Fault lamps at the top of the cabinet and on the motor controller are lit when the MOTOR CONTROL switch is operated to the LOCAL position. The motor controller fault lamp is also lit when any of the NORMAL/MOVE switches on the motor assembly is in the MOVE position.

TABLE 1

Circuit operation for control of rectangles

Switch operation	Unit concerned	Relay operation	Effect
MOVE/SIZE switch operated to MOVE or SIZE or RESET switch operated	Panel, control desk (centre)	—	Earth connected to intertrace equipment.
	Pulse generator (rectangle)	RLB operated	D.C. output connected to intertrace equipment according to setting of MOVE/SIZE potentiometers on motor assembly. Dot corner markers appear on console 2.
MOVE/SIZE switch operated to MOVE	Motor assembly	RLA and RLC operated	Variable 500 c/s from motor controller connected to X and Y move motors.
Joystick switch operated	Electronic joystick switch unit	RLE operated RLA–RLD either operated or released in pairs	When joystick is moved, the fixed 500 c/s from motor controller is applied to X and Y move motors. Motors turn until joystick switch is released at required rectangle position, as shown by dot markers.
MOVE/SIZE switch operated to SIZE	Motor assembly	RLB and RLD operated	Variable 500 c/s from motor controller connected to X and Y size motors.
Joystick switch operated	Electronic joystick switch unit	RLB operated RLA–RLD either operated or released in pairs	When joystick is moved, fixed 500 c/s from motor controller is applied to X and Y size motors. Motors turn until joystick switch is released at required rectangle size as indicated by dot markers.
RESET switch operated	Electronic joystick switch unit	RLE operated	500 c/s input from motor controller connected to motor assemblies.
	Motor controller	RLA operated	Fixed d.c., instead of variable d.c. from joystick, connected to switch electronic joystick.
	Motor assemblies	RLE and RLF operated	RLA–RLD operating coils connected to cam-operated micro-switches. Move and size relays operated in sequence to apply 500 c/s supplies to motors which turn until rectangle is in preset position with preset size according to micro-switch setting.

TABLE 2

Circuit operation for control of doppler compensation

Switch operation	Unit concerned	Relays operated	Effect
USERS/LOCAL switch operated to either position	Pulse generator (rectangle)	RLA	Rectangle waveform output passed to panel (area switching).
	Panel (area switching)	RLD, RLE or RLF, according to rectangle selected	Rectangle marker generated and passed to display equipment. Rectangle switching waveform passed to reference frequency electronic switch No. 1, i.e. doppler compensation applied in appropriate rectangle area.
USERS/LOCAL switch operated to USERS position	Panel (area switching)	RLA, RLB or RLC, according to rectangle selected	Rectangle switching waveform produced and passed to the video switch associated with the fully processed display. Doppler compensated cancelled video is therefore applied to the controllers' display in the rectangle area subject to clutter switching.
RECTANGLE 1, 2 or 3 or CIRCLE clutter switches operated	Panel (area switching)	RLG, RLH, RLJ or RLK	The circle or rectangle switching waveforms are made operative area the whole of the selected area so that clutter switching is made inoperative. The fully processed video in the appropriate rectangle or circle area, as selected, will now be video with MTI,non-clutter switched, over the whole of the area.

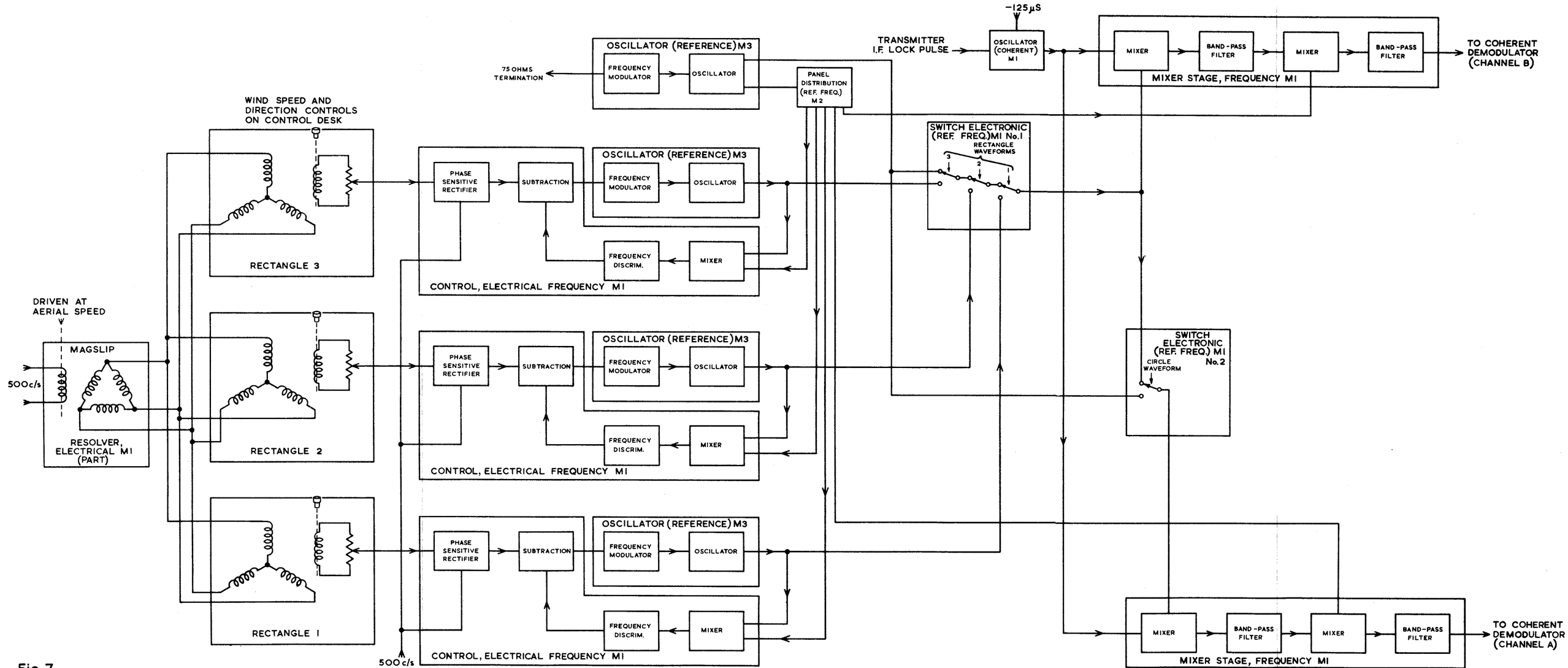


Fig. 7

Doppler compensation channels

Fig. 7

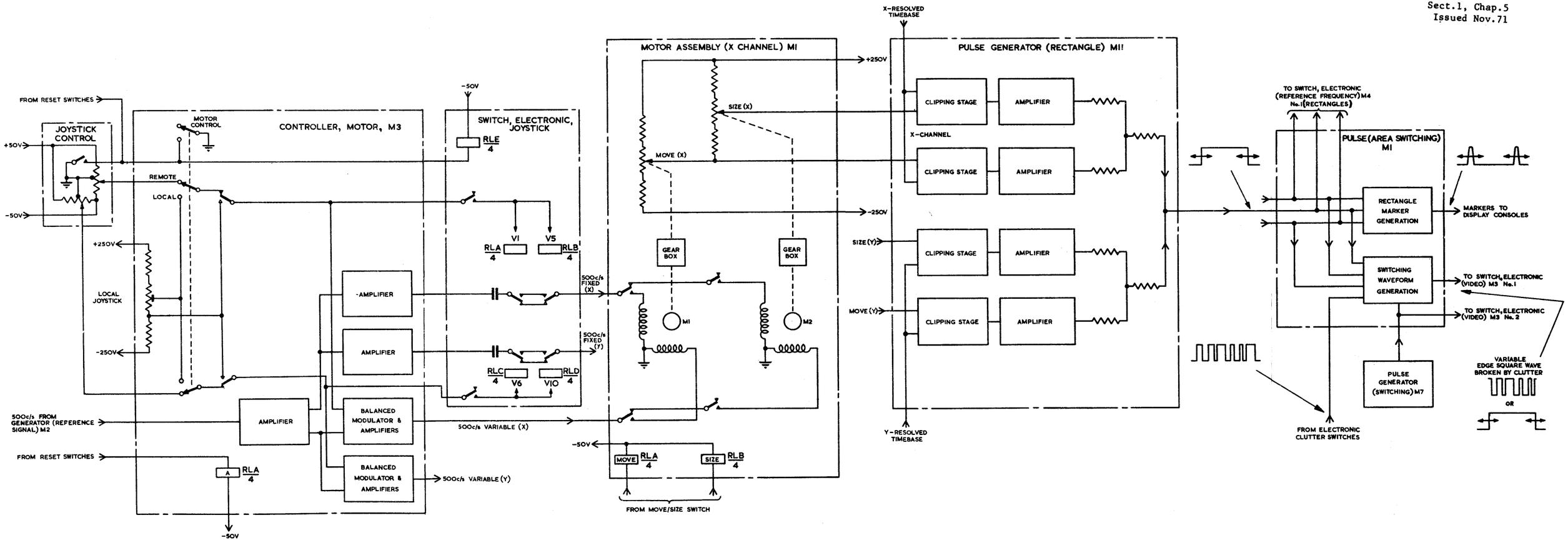


Fig. 8

Production, movement and sizing of rectangles

Fig. 8

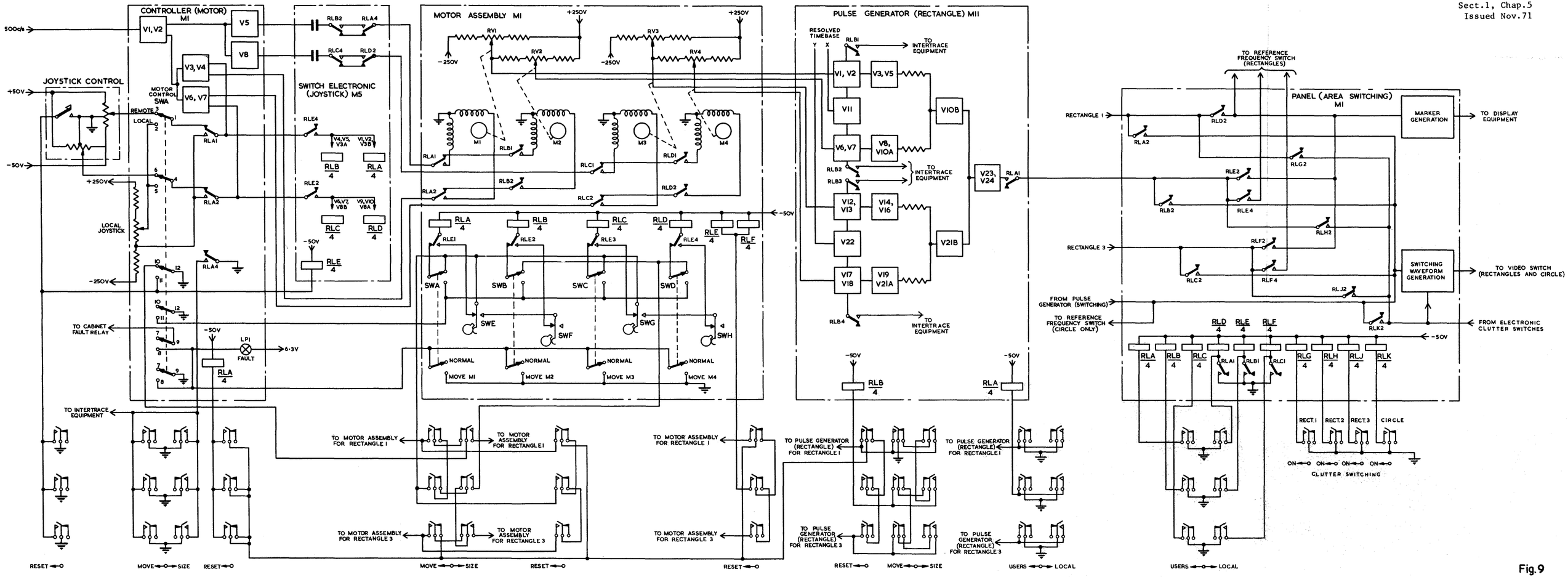


Fig.9

Doppler control circuits

Fig.9

Chapter 6
(Completely revised)

TRIGGERING AND TIMING

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

Introduction

1. General station timing is controlled by the no-break trigger system, which is described in A.P.4769E. This system is designed to provide triggering pulses and r.f. carrier signals for the Type 84 radar and/or other equipment. Triggering pulse outputs, which are derived from crystal-controlled oscillators, are subject to external p.r.f. correction.

2. The nominal timings of the pulse outputs are illustrated on fig. 1. All timings are with respect to the 0 microsecond datum pulse, the timings of normal (un-delayed) pulses being fixed, while those of delayed pulses are variable over the range +5 μs to 170 μs with respect to the initiating pulse. The delayed pulses are provided so that triggering times may be set to take into account cable and other delays which may vary from site to site. The

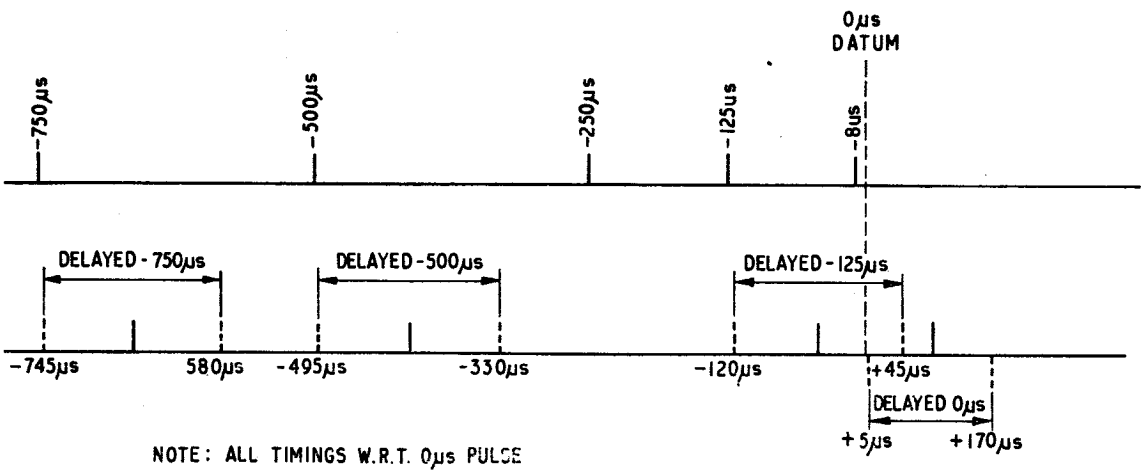


Fig. 1. Pulse timing relationships

p.r.f. can be anywhere in the range 245 c/s to 275 c/s as determined by the station requirements. To provide a reference for the external p.r.f. comparison circuits a sine wave at a nominal frequency of 500 c/s (twice the p.r.f.) is derived from a subdivision of the crystal frequency and is fed out to them. Besides these outputs derived from the crystal oscillator, sinusoidal carrier outputs at frequencies of 6·14 Mc/s and 8·14 Mc/s are obtained from L-C tuned oscillators. The numbers of each type of output provided are given on the simplified block diagram of the no-break trigger system, fig. 2, while the connections between this system and the Type 84 radar are listed in Table 1.

TABLE 1

Connections between Type 84 radar and the no-break trigger system

Source/destination Type 84 radar		Service	Source/destination no-break trigger system	
Cabinet	Distribution/ connector		Distribution unit, pulse	Relay assembly
I.F.	403/SKB	0 μs pulse	SKT EJ	
	403/SKC	0 μs pulse	SKT EM	
	403/SKD	0 μs pulse	SKT EF	
	403/SKE	0 μs pulse	SKT EQ	
	403/SKF	−125 μs pulse	SKT AQ	
	403/SKG	−125 μs pulse	SKT AF	
Cancellation	403/SKA	−125 μs pulse	SKT AC	
	403/SKB	−8 μs pulse	SKT CZ	
	401/SKC/1	Var. phase 500 c/s		PLA/4
	401/SKC/3	Ref. phase 500 c/s		PLA/3
	403/SKS	P.R.F. reference		SKTD
	403/SKC	8·19 Mc/s carrier		SKTU
	403/SKD	8·19 Mc/s carrier		SKTX
	403/SKE	6·14 Mc/s carrier		SKTG
	403/SKF	6·14 Mc/s carrier		SKTK
Doppler	403/SKA	0 μs pulse	SKT DZ	
Video	403/SKA	−125 μs pulse	SKT W	
	403/SKB	−8 μs pulse	SKT DT	
	403/SKC	0 μs pulse	SKT ET	
	403/SKZ	0 μs pulse	SKT DW	
	403/SKD	8·19 Mc/s carrier		SKT AA
Transmitter	Term. 5J/SKTK	−8 μs pulse	SKT DJ	
			P.R.F. cabinets	
Cancellation	401/SKC/2	Ref. phase return	Main & stby	401/SKTD/18
	401/SKC/4	Var. phase return	Main & stby	401/SKTD/19
Power	401/SKA	Scope sync.	Standby	402/SKTBC
Indicator connections				
See Sect. 8, Chap. 3		Maint. switch	Main & stby	401/SKTD/2
		System state maint.	Main & stby	401/SKTD/1
		System state normal	Main & stby	401/PLE/16
		System state fault	Main & stby	401/PLE/18
		Frame No. 1 fault	Main	401/SKTC/3
		Frame No. 2 fault	Main	401/SKTC/4
		Frame No. 3 fault	Main	401/SKTC/5
		Frame No. 1 fault	Standby	401/SKTC/3
		Frame No. 2 fault	Standby	401/SKTC/4
		Frame No. 3 fault	Standby	401/SKTC/5
		Emergency trigger lamp	Main	401/SKTD/11

General description

3. Dual operation is provided in the no-break trigger system by means of main and standby channels, change-over being automatically controlled through fault monitoring circuits. Functionally the trigger system can be divided into three sections, namely:—

(1) R.F. generation.
(2) Pulse generation.
(3) Output distribution.

R.F. generation

4. The fundamental frequency from which the final triggering pulses are formed is produced by a crystal oscillator. The crystal frequency is chosen to suit the p.r.f. in use, typically 4·096 Mc/s for a p.r.f. of 250 c/s, fine tuning being accomplished by means of a motor-driven crystal pulling capacitor, which is controlled by the external p.r.f. correction signals. Two such oscillators are provided, one main and one standby. After one stage of division-by-two the oscillator outputs are continuously monitored and are fed to r.f. gates. Then:—

(1) As long as the main crystal oscillator output is present, a select main signal is generated. This

(*a*) Allows the r.f. from the main crystal oscillator to pass in parallel to the flywheel oscillators, main and standby.

(*b*) Is fed to the relay assembly (*para.* 13) causing the main p.r.f. reference signal and 6·14 Mc/s and 8·19 Mc/s carrier signals to be routed out, and p.r.f. correction to be applied to the main crystal oscillator.

(2) If the main crystal oscillator fails and the standby r.f. is present, a select standby signal is generated. This—

(*a*) Allows the r.f. from the standby crystal oscillator to pass in parallel to the flywheel oscillators.

(*b*) Is fed to the relay assembly causing the standby p.r.f. reference signal and 6·14 Mc/s and 8·19 Mc/s carrier signals to be routed out, and p.r.f. correction to be applied to the standby crystal oscillator.

5. When the no-break trigger system is used in conjunction with the Type 84 radar, the p.r.f. correction signals are derived from circuits in the Type 84 cancellation cabinet (*Sect.* 3), to which the p.r.f. reference signal from the p.r.f. system is fed. The cancellation principle used in the signal processing circuits depends upon the signal delay in a mercury delay cell being exactly equal to the pulse recurrence period. Compensation to correct for any discrepancies between the delay period of the cell and the recurrence period is applied to the crystal oscillator in use at the p.r.f. system. The p.r.f. correction signals consist of a fixed (reference) phase 500 c/s (nominal) signal, which is an amplified version of the p.r.f. reference signal fed from the p.r.f. system to the cancellation circuits, and a variable phase 500 c/s (nominal) signal. The phase of this latter signal is either leading or lagging by 90 degrees with respect to that of the reference phase, according to the direction of the required p.r.f. correction. The fixed and variable 500 c/s signals between them provide the motive power for the motor which drives the frequency-pulling capacitor of the crystal oscillator, thus making the necessary basic frequency correction between the delay cell and pulse recurrence periods.

6. The main and standby flywheel oscillators are synchronous oscillators tuned to the nominal half crystal frequency. As long as r.f. input is present from either the main or standby crystal, output from the flywheel oscillators, which drive the respective pulse generation circuits, is synchronized with it. Under these circumstances the pulse outputs finally produced are subject to p.r.f. correction. If output from both the main and standby crystal oscillators fails, the flywheel oscillators run at their pre-tuned frequency but are no longer synchronized to external demands or with each other. When this occurs, one of the flywheel oscillators is automatically inhibited, in accordance with pre-selected demand, to prevent the misalignment of main and standby output pulses. Thus triggering pulse output is still maintained, though it is not subject to p.r.f. correction; a warning to this effect is given to the pulse users by the lighting of an external emergency trigger indicator lamp.

7. Separate main and standby 6·14 Mc/s and 8·14 Mc/s L-C oscillators are provided, their outputs being distributed via the relay assembly in accordance with whether the main or standby crystal oscillator is selected.

Pulse generation

8. The pulse generation circuits consist of frequency dividers and gating circuits through which pulses are formed at the required timings. These pulses are fed to buffer amplifiers, where the required number of outputs is formed. These normal (un-delayed) pulses are then:—

(1) Fed to the external equipment, via the distribution unit, pulse.

(2) Used to initiate delayed pulse outputs. Each of these outputs may be delayed by from $+5$ μs to 170 μs with respect to the initiating pulse, the delays being continuously variable. The delayed pulses are then also fed to the external equipment via the distribution unit, pulse.

9. So that the normal main and standby pulses may be aligned in time, a phase shifter is connected between the output of the standby flywheel oscillator and the standby pulse generation circuits. This allows the main and standby pulses to be manually aligned to compensate for any phase changes between the main and standby pulse generation circuits. The delayed pulse outputs have to be separately aligned with their opposite numbers, since an optional delay can be introduced in each individual pulse.

10. Fault monitoring circuits ensure that there is no appreciable (less than 1 μs) misalignment between the main and standby normal pulses. If there is misalignment then either the main or standby pulse outputs are automatically inhibited, the choice being pre-selected. Pulse outputs are also automatically inhibited from a pulse generation channel in which a fault is detected.

Output distribution

11. The no-break trigger system contains the following items of equipment:—

(1) P.R.F. cabinet (main).
(2) P.R.F. cabinet (standby).
(3) Panel indicator, pulse.
(4) Distribution unit, pulse.
(5) Relay assembly.

12. The r.f. and pulse generation circuits and fault monitoring circuits are contained in the two cabinets. All trigger pulse outputs are distributed via the distribution unit, pulse. This unit contains a two-input OR-gate for each output pulse, the inputs being the corresponding main and standby pulses. Thus with normal operation both pulses are represented in the output, and this is the reason why pulse alignment is so important; if the pulses drifted apart, then double triggering could result. This system of distribution ensures that there is no break in pulse output should either the main or standby pulses fail. Pulse inputs to the distribution unit are continuously monitored by fluorescent grid indicators contained in the panel indicator, pulse. This unit is wall-mounted at a location adjoining the p.r.f. cabinets; the distribution unit, pulse is mounted under the floor adjacent to the cabinets.

13. Distribution of the 6·14 Mc/s and 8·14 Mc/s carriers, of the p.r.f. reference output, and of the live sides of the reference and variable phase 500 c/s p.r.f. correction input signals, is made through the change-over contacts of relays in the relay assembly. This unit is also mounted under the floor, being bolted to the distribution unit, pulse.

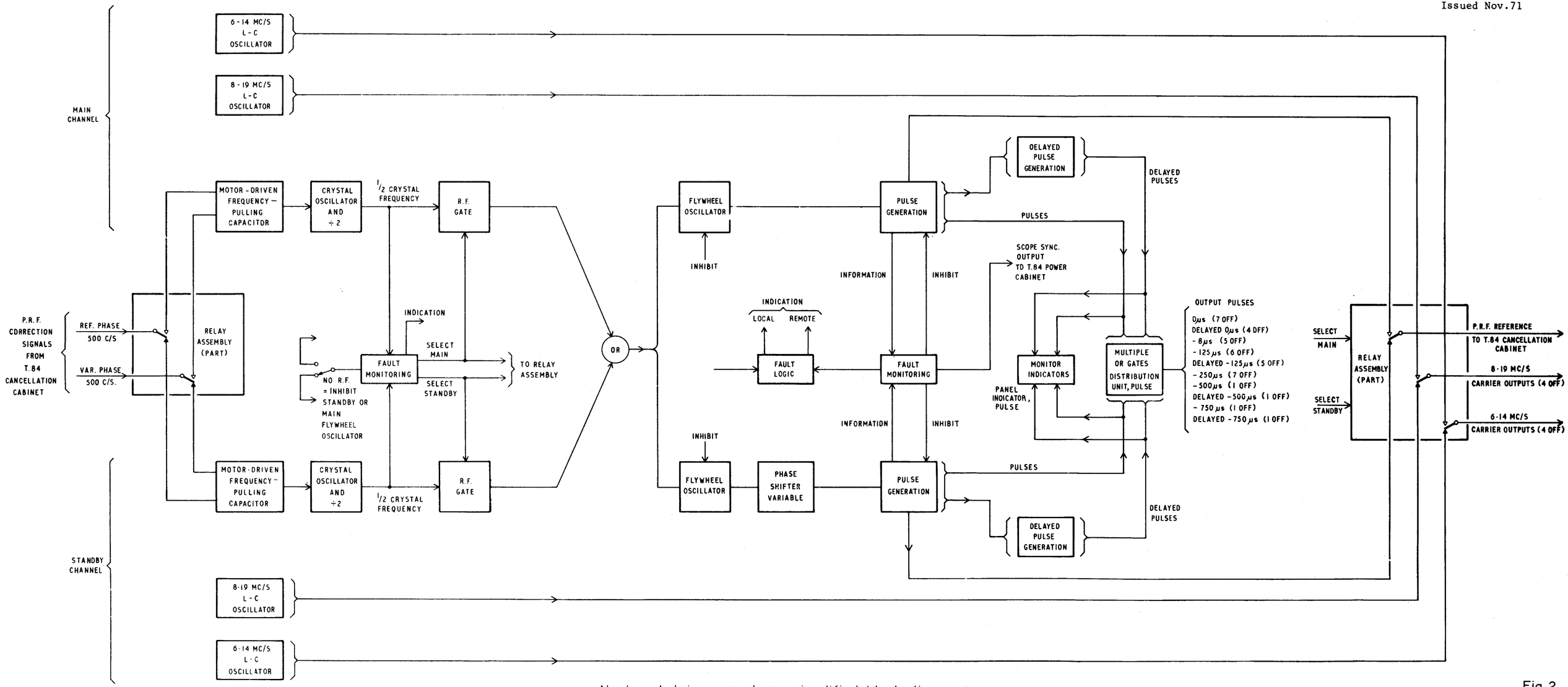
14. The connections between the Type 84 radar and the no-break trigger system are listed in Table 1. Besides the connections made to the distribution unit, pulse and the relay assembly, the following connections are made directly to the p.r.f. cabinet terminations:—

(1) The returns of the reference and variable phase p.r.f. correction signals.

(2) A scope sync. output pulse, at the p.r.f. frequency, from the p.r.f. system to a built-in oscilloscope in the Type 84 power cabinet.

(3) Connections from the p.r.f. system to the remote system state and emergency p.r.f. indicators. The connection details at the remote end vary according to the site; see Sect. 8, Chap. 3.

15. In general, in the text and drawings of this Type 84 handbook, connections to the no-break trigger system are referred to as to the p.r.f. system; this can be taken to mean to the cabinets, or to the distribution unit, pulse or relay assembly as appropriate.



No-break trigger system - simplified block diagram

Fig. 2

Chapter 7

(Completely revised)

SIGNAL PROCESSING LAYOUT AND ANCILLARY SYSTEMS

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

System layout

1. The type 84 radar signal processing circuits are housed in five equipment cabinets. The association of units with cabinets for the signal processing circuits proper is shown in the overall block diagram (*fig.* 1). The functions of the units accommodated in the cabinets are summarized below.

Power cabinet

2. Negative h.t. (−250V) supplies for the cancellation, video, i.f. and Doppler cabinets are produced by four voltage regulators contained in two −250V regulator units. An independent h.t. supply (+250V and −250V) is produced by a power supply unit for the linear demodulator associated with the anti-jamming signal channel. A lampholder assembly provides initial distribution of the +450V and −50V static supply inputs and provides the 6·3V a.c. supply for fault lamps. In addition to the units associated with generation and distribution of power supplies, the cabinet provides a mounting for the monitoring oscilloscope and for the resolver unit which converts 50 c/s rotational information from the aerial head into 500 c/s rotational information for use in Doppler compensation circuits.

Cancellation cabinet

3. Two cancellation channels, A and B (*Chap.* 3) are the main items in the cancellation cabinet. Since the circuits for p.r.f. control are associated with cancellation channel B, these also are to be found in the cabinet.

Video cabinet

4. The video cabinet contains the following:—

(1) Units forming the linear signal channel.

(2) The amplifier (video rectifier), pulse delay network and comparator signal (video) in the MTI channel.

(3) The electronic video switches and relay assemblies associated with channel and monitor selection and the output video amplifiers.

(4) The p.r.f. discrimination units.

I.F. cabinet

5. The i.f. switch unit in the i.f. cabinet receives the linear and anti-jamming i.f. inputs and the lock pulse from the radar transmitter/receiver. The cabinet also contains the i.f. and demodulating units

for the MTI and the logarithmic signal channels, together with the coherent oscillator and mixer stages associated with the MTI signal channel.

6. Test equipment for the signal processing system is located in the i.f. cabinet and consists of the following:—

(1) An i.f. signal generator.
(2) A video signal generator.
(3) A noise amplifier assembly.
(4) A 0–99 dB variable attenuator.
(5) A cable storage box for the patching leads used with the test equipment.

Doppler cabinet

7. Doppler compensation units are fitted in this cabinet, which also includes units associated with the generation of waveforms used for video and reference frequency switching and of the rectangle and circle markers.

Control panel

8. Associated with, but not connected to, the signal processing cabinets is a control panel which is wall-mounted in the equipment room. This panel forms part of the technical monitoring system installed on the indicator panel rack in the control room.

Control position

9. A monitoring console assembly and a wall-mounted rack assembly are installed at the control position. The monitoring console assembly contains three identical fixed coil display units and is fitted with control desks, the latter incorporating the operational controls for the signal processing system as a whole.

10. The wall-mounted rack assembly incorporates technical controls for the transmitter/receiver, the aerial turning gear and the signal processing systems. The indicator and trigger panels on the rack indicate the serviceability state of the system, so that an operator seated at the monitor consoles can select the best available type of signal processing.

Power supply system

11. The h.t. (+250V and −250V) supplies for the majority of units in the signal processing cabinets are derived from the station bulk power supplies of +450V, −425V, −625V, −50V and −500V (reference). The −250V power supplies for the cancellation, video, i.f. and Doppler cabinets are provided by the power supply cabinet. In all cabinets a +250V regulator provides the h.t. supply for each frame of the cabinet and also provides distribution for the a.c. mains, −250V and −50V supplies for the units on that frame. The h.t. supplies for the linear demodulator in the anti-jamming channel are derived directly from the a.c. mains by the power supply unit M1 in the power cabinet.

12. The −50V supply for the signal processing equipment is derived from the station supplies and brought into the power cabinet at the lamp holder assembly. The supply then passes via the power cabinet distribution system and a link in the rack electrical equipment to the cancellation, i.f. Doppler and video cabinets through the power cabinet distribution system once more.

13. The +450V for the +250V regulators in all cabinets is distributed directly from the lampholder assembly in the power cabinet. The bulk power supplies for −250V regulators are received directly by the cabinet concerned from the station supplies.

14. The a.c. mains supplies are received directly by each cabinet from the station supplies. Mains supplies for test equipment, etc., are available from 3-pin sockets located on the distribution unit at the bottom of the front of the power cabinet.

Fault circuits

15. Lamp indication of power supply failures or of malfunction or mis-operation of certain units on the cabinets is provided, these lamps being lit when a fault is present.

Frame faults

16. Failures of the +250V output from, or −250V input to, any +250V regulator will cause the fault lamp on the regulator to light. Either of these failures will also cause the cabinet fault lamp to light, and will disconnect an earth from the fault wire to the indicator panel on the indicator panel rack assembly. The illuminated block diagram on the indicator panel will then be modified because certain lamps will be extinguished, as also will the frame fault lamp on the trigger panel. A cabinet fault lamp may be lit and the earth removed from the fault wire by failure or mis-operation of other units in certain cabinets; these units are listed in Table 1.

TABLE 1

Units with fault circuits

Cabinet	Frame	Unit	Fault	Unit indication
Cancellation	1	Controller (p.r.f.) M1	Large error in p.r.f.	LP1 lit
Video	2	Controller (p.r.f.) M2	Large error in p.r.f.	LP1 lit
Video	2	Delay line (variable) M1	Mercury leak	Nil
I.F.	1	Switch, electronic (i.f.) M2	SWC in TEST position	Nil
Doppler	1	Controller motor M3	SWA in LOCAL position	LP1 lit

−250V failure

17. Failure associated with a −250V regulator in the power cabinet (that is, failure of any of the inputs to the regulator from the bulk power supplies or failure of the regulator itself to produce a −250V output) will cause the fault lamp on the regulator, and the −250V fault lamp on the power cabinet, to light. In all cases of failures of a −250V regulator the 6·3V supply for fault lamps in the +250V regulators is removed, so that indication of failure on a +250V regulator is not given as a result of failure of a −250V regulator.

18. In all cases of failure of +250V or −250V regulators, −50V is removed from the power call wire so that the bulk power supplies are removed from the faulty unit.

19. Failure of either output (+250V or −250V) from the power supply M1 will light the unit and the power cabinet fault lamps. An earth will be removed from the fault wire for the LINEAR DETECTOR (A.J.I.F.) circuit in the indicator panel. The illuminated block diagram will therefore be modified in respect of the anti-jamming signal channel.

Indicator panel

20. The following circumstances also cause the light pattern on the indicator panel to be modified:—

(1) Linear or anti-jamming i.f. channels under test at the radar head, i.e. if the wobbulator switch for the appropriate channel is operated.

(2) The stabilized local oscillator is off tune.

21. In order to provide indication at the control position of the availability of the channels in the system, a control panel is situated near the signal processing cabinets. The panel is provided with a switch for each unit, except units associated with power supply in the cabinets. Operation of any switch implies a 'known fault' and modifies the illuminated pattern of the indicator panel. The non-availability of any part of a signal channel for the users' displays is thus indicated to the MTI operator.

Trigger panel

22. The trigger panel carries a number of fault and state indicators in addition to those appearing on the indicator panel. These may be classified as follows:—

(1) FRAME FAULT indicators, one for each frame of each cabinet, normally lit but extinguished if a fault occurs.

(2) Two EMERGENCY TRIGGER indicators one for each p.r.f. system (A or B) normally extinguished but illuminated if a fault occurs in either p.r.f. system which might lead to a loss of long term stability.

(3) A FAULT indicator, normally extinguished, which flashes if a fault occurs as in (1) above or if any of the switches on the control panel are operated.

(4) A MAINTENANCE indicator, normally extinguished, which is illuminated if a known fault is set on any of the switches in the control panel.

(5) A STALO ON TUNE indicator, normally illuminated, which is extinguished when the stabilized local oscillator is off tune.

(6) A P.R.F.D. BYPASSED indicator illuminates when the pulse recurrence frequency discrimination circuits have been bypassed by operation of switch SWG on the trigger panel.

(7) Two I.I.S. BYPASSED indicators, one for each impulse interference suppression system (A or B), are normally extinguished but are illuminated when the I.I.S. is bypassed.

(8) In the non-linesman version the P.R.F. A and B states are indicated by P.R.F. NORMAL and P.R.F. FAULT indicators for each channel. The P.R.F. NORMAL indicators are illuminated when no faults are present. If any fault develops the P.R.F. FAULT lamp will illuminate. The p.r.f. equipment may however continue to operate.

Control panel (fault override)

23. If any of the switches have been set to the fault lamp override position an indicator on the control panel (fault override) illuminates.

Control panel

24. A lamp on the control panel flashes if any of the switches on the control panel are operated, with the system otherwise in a serviceable condition. An override switch may be operated in order to cancel the flashing indications.

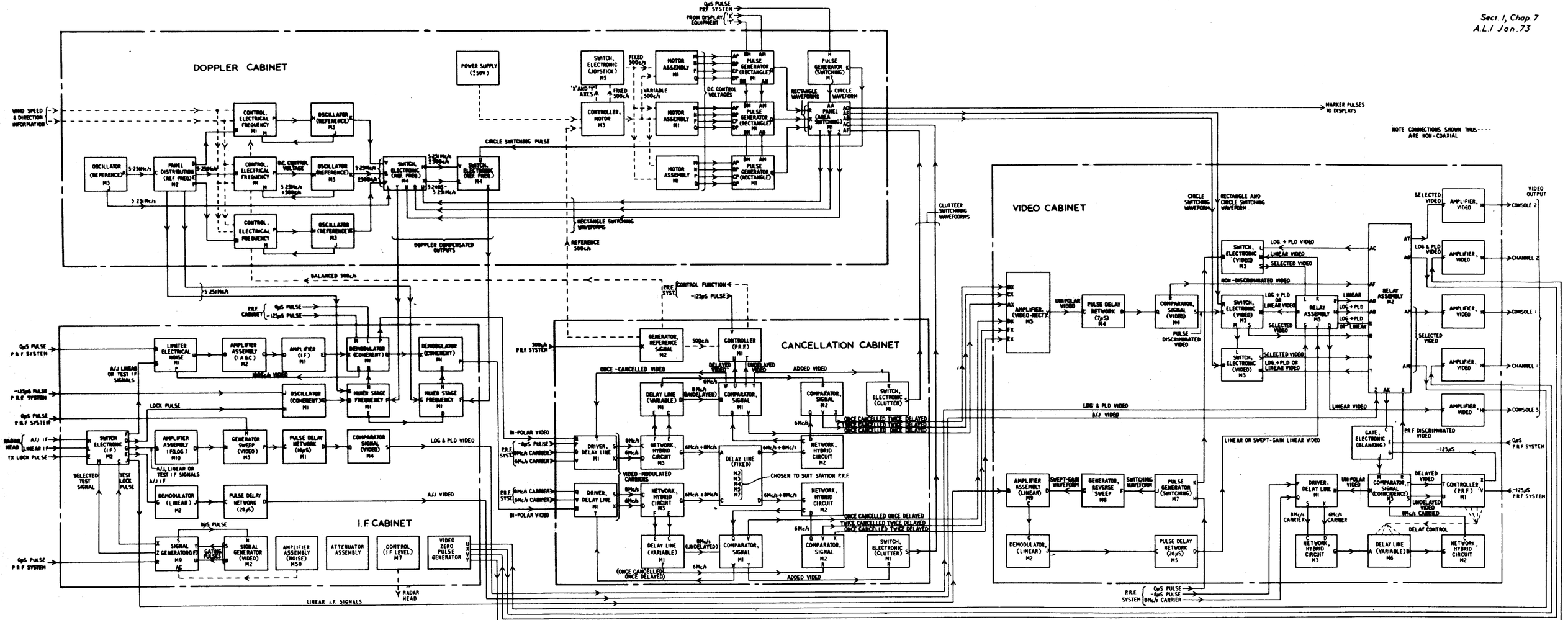


Fig.1

Signal processing: block diagram

Fig.1

SECTION 2

I.F. CABINET

Chapter 1
(completely revised)

IF CABINET AND INTERCONNECTIONS

CONTENTS

PURPOSE OF CABINET

1 The IF cabinet (fig.1 and 2) receives linear and anti-jamming i.f. signals at 13.5 MHz from the radar head. These signals are selected and processed into four channels to produce bipolar MTI, log + PLD and antijamming video and linear i.f. (unprocessed) outputs. Lock pulse and i.f. test signals are also produced within the cabinet which also houses the video zero range pulse generator.

2 Referring to the block diagram (fig.5); selection of input signals to the processing channels is effected by the switch electronic (i.f.) M2. This unit also receives and reroutes the test i.f. signal and selects either transmitter or test lock pulses as required. At stations fitted with the multifilter MTI processor S7110 the linear i.f. and lock pulse are routed via an additional

unit, the i.f. bypass relay (Mod. No. CA8125/3). This modification does not affect the i.f. cabinet processing channels. The bypass relay is described in Chap.20.

3 After selection, the i.f. signals are distributed to the four signal channels. Since signals feeding the linear channel are not processed in the i.f. cabinet, they are routed to the video cabinet. Processing of signals for the antijamming channel consists only of demodulation and, after delay compensation, the resultant video is passed to the video cabinet.

4 The input to the circuits forming the log + PLD channel may be either linear or antijamming i.f. signals. These signals are first amplified and demodulated in a logarithmic amplifier, the resultant video signals then being passed through a gain-sweeping ciruit, the function of which is to modify the video signals in such a way as to counteract the effect of 'angels' on the display. The gain-swept video signals are passed via a delay compensating network to the pulse-length discrimination circuit in the comparator, signal (video) M4. This unit is essentially a pulse-lenth comparator, its purpose being to reject pulses of more than a certain duration, thereby reducing the effects of clutter on the displays. After discrimination, the video signals are routed out of the i.f. cabinet and fed to the video cabinet.

5 The i.f. circuits of the MTI channel receive linear or antijamming i.f. signals from the electronic switch unit, and also the transmitter lock pulse from the same source. The i.f. signals pass through stages of noise suppression and amplitude compression to two coherent demodulator circuits, in which the phase relationship of the i.f. signals is compared to that of a reference frequency, derived from coherent oscillator and mixer circuits.

6 The outputs of the coherent demodulators consists of bipolar video signals at 100 kHz, and these outputs, designated channel A and channel B, are routed to the cancellation cabinet, where one is used for the suppression of stationary responses and the other for the suppression of moving clutter.

MECHANICAL DESCRIPTION

7 A mechanical description common to all cabinets is given in Appendix 1, while mechanical features peculiar to the i.f. cabinet are given herein. A list of weights and dimensions of individual units is given in Table 1.

ELECTRICAL DESCRIPTION

Rack wiring

8 Inter-unit wiring is carried in cable harness at the rear of each frame, provision being made for withdrawing the frames from the cabinet by the use of flexible cable loops at the bottom of each frame.

9 Inter-cabinet wiring enters via the bottom of the cabinet, the coaxial wiring going to a distribution panel at the lower rear of the front channel of the left-hand side member. From the distribution panel, coaxial connections are made to units within the frames. All other wiring is taken to multipole plugs and sockets located at the lower rear of the front channel of the right-hand side member.

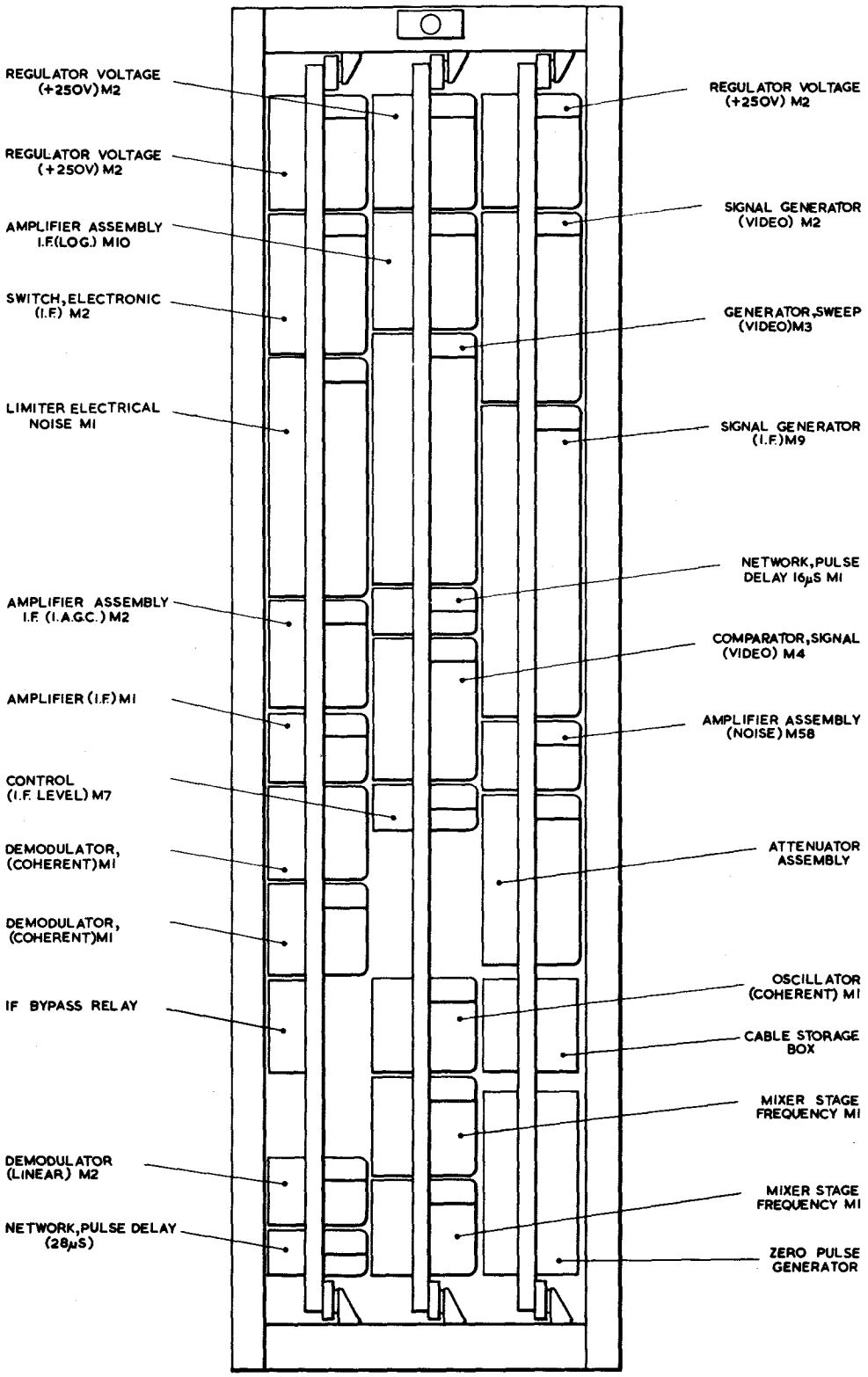


Fig.1 IF cabinet: front view

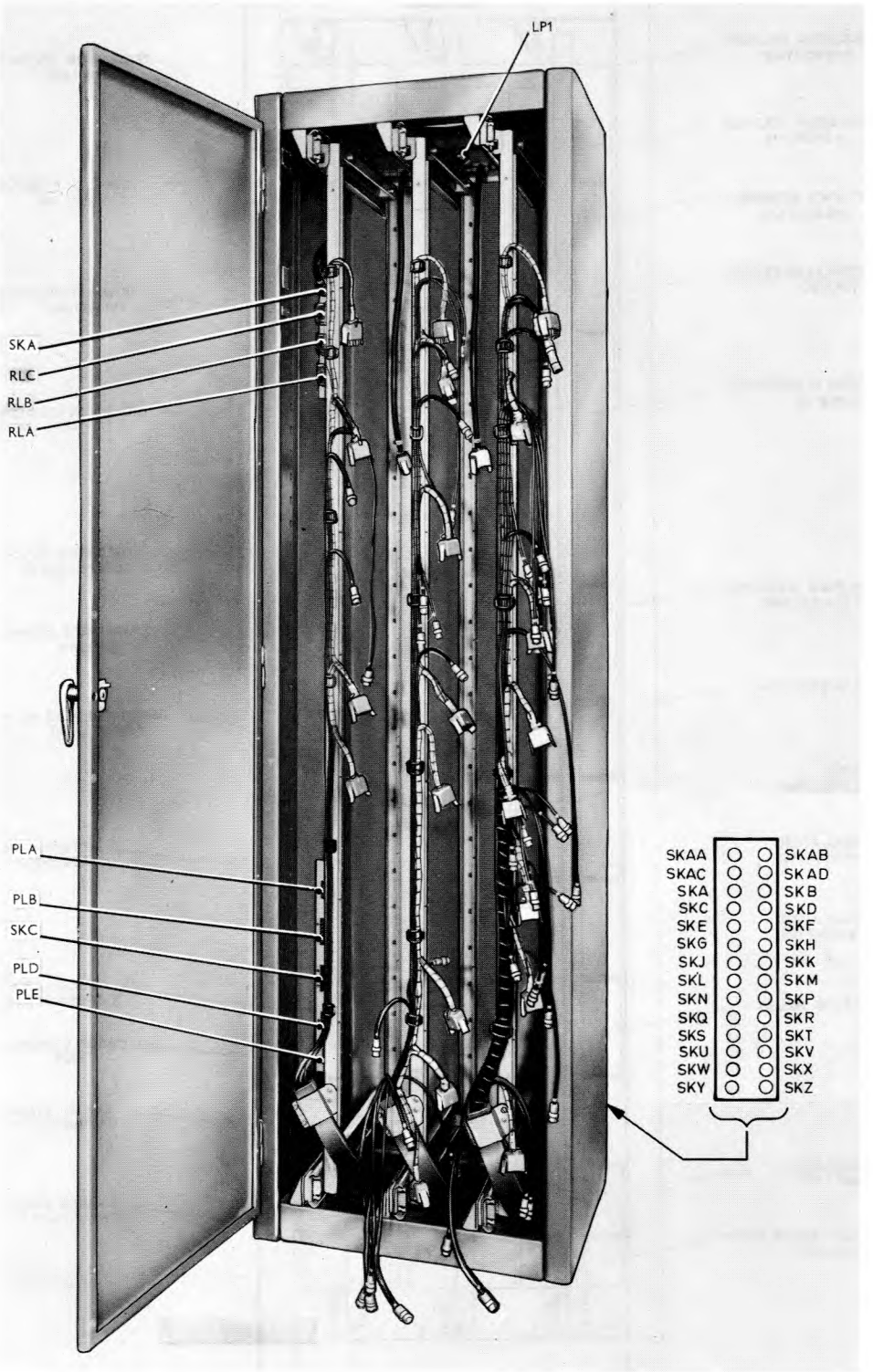


Fig.2 Cabinet, electrical equipment M43: rear view

Power distribution

10 Distribution of power supplies within the cabinet is shown in fig.6. This drawing includes a circuit diagram of the cabinet fault relay assembly, a description of which follows.

Fault relay assembly

11 The fault relay assembly, which is mounted at the upper rear of the front channel of the right-hand side member of the cabinet, functions in conjunction with relays in each of the voltage regulators (+250V) M2. The purpose of the circuit is to light the FAULT lamp, LP1, at the top of the cabinet, when either or both the +250V and -250V supplies are not available, plus the added facility of showing a system fault when SWC on switch electronic (i.f.) M2 is in any position other than NORMAL.

12 The circuit consists of three relays, RLA to RLC. One side of the energizing coils of these relays is connected to the cabinet -50V supply, while the other side is taken via individual fault wires to the voltage regulators associated with each frame.

13 In the voltage regulator, the fault wire is connected to the contacts of two h.t. failure relays such that if a failure of either the +250V or -250V supplies occurs, one or other of the relays is de-energized, thereby connecting the fault wire to earth and energizing the appropriate relay in the fault relay assembly. Contacts RLA1 and RLB1 complete the 6.3V supply to the cabinet FAULT lamp LP1 and contacts RLA2, RLB2 and RLC2 break the earth circuits of the normally energized i.f. cabinet frame fault relays in the indicator panel. Indication of a fault in the frame 3 voltage regulator is provided by a POWER FAILURE lamp on the regulator panel but not by the cabinet FAULT lamp.

TEST FACILITIES

14 The i.f. cabinet contains built-in facilities for checking the functioning of the signal processing channels under test conditions. These facilities are provided by the video and i.f. signal generators, which are described in Chap.11 and 12 respectively of this section, and the amplifier assembly (noise), described in Chap.13.

Attenuator assembly

15 Associated with the test signal generators is the attenuator assembly (fig.3 and 4). This unit, which is mounted in frame 3 of the cabinet, consists of two variable attenuators connected in series. One attenuator operates from 0 to 9 dB in 1 dB steps, while the other operates from 0 to 90 dB in 10 dB steps. Thus, a range of attenuation is available of from 0 to 99 dB in steps of 1 dB, the level of attenuation being selected by push-buttons. No permanent connections are made to the attenuator, the signal requiring attenuation being 'patched' into SKC, and the attenuated signal taken from SKD. Both input and output connections present an impedance of 75 ohms.

Fig.3 Attenuator assembly: front view

Cable storage box

16 This provides facilities for the storage of any test leads, terminating resistors, etc., when these are not in use. The box is mounted on frame 3 of the cabinet and the frame must therefore be withdrawn from the cabinet before the box is accessible.

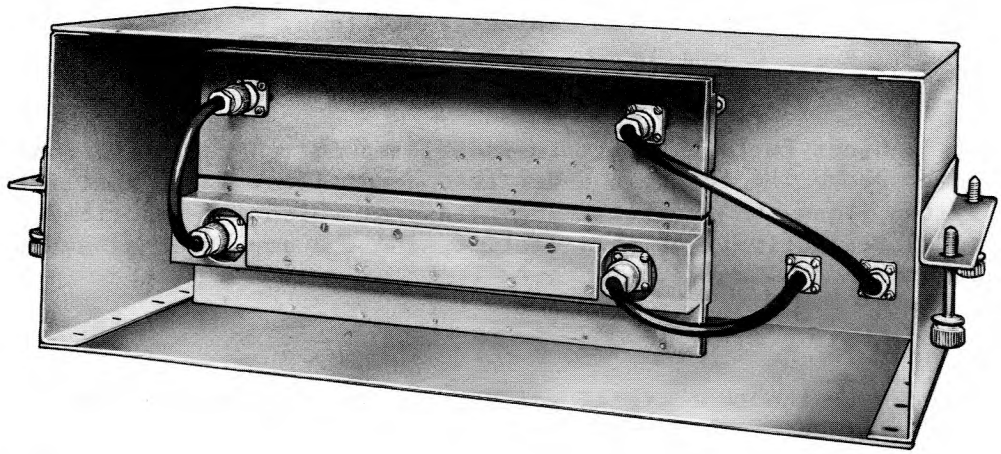


Fig.4 Attenuator assembly: rear view

TABLE 1 WEIGHTS AND DIMENSIONS

Title	Dimensions (inches)	Weight	NATO Stock No.	Chapter
Cabinet, electrical M43	84½x23½x25½	425 lb	5975-99-999-2833 or 5975-99-659-4690	1 and Appendix 1
Switch electronic (i.f.) M2	17½x9x6	7 lb	5840-99-999-9006	2
Amplifier assembly i.f. (log) M10	17½x7½x6	8 lb	5840-99-999-2675	3
Amplifier (log) M7	13½x2 13/16x2¾	3 lb	5840-99-999-1967	3
Generator (sweep) (video) M3	17½x13½x6	10½ lb	5840-99-913-3247	4
Pulse delay network (16 us) M1	17½x3x6	2 lb	5915-99-999-2683	5
Pulse delay network (28 us)	17½x3x6	2 lb	10D/5915-99-913-2173	5
Comparator signal (video) M4	17½x9x6	8 lb	5840-99-999-2296	6
Limiter electrical (noise) M1	17½x15x6	13½ lb	5840-99-999-2695	7
Amplifier assembly i.f. (i.a.g.c.) M2	17½x7½x6	8 lb	5840-99-999-2916	8
Amplifiier (i.a.g.c.) M4	13½x2 13/16x2¾	3 lb	5840-99-999-1970	8
Amplifier (i.f.) M1	17½x4½x6	5 lb	5840-99-999-2676	9
Demodulator (coherent) M1	17½x6x6	5¼ lb	5840-99-999-2670	10
Signal generator (video) M2	17½x12x6	12½ lb	5840-99-999-9005	11
Signal generator (i.f.) M9	17½x19½x6	17½ lb	5840-99-999-9004	12
Amplifier assembly (noise) M58	17½x4½x6	6½ lb	5840-99-999-9167	13
Amplifier (noise) M68	10¼x2 3/8x3½	2½ lb	5840-99-999-9168	13
Demodulator (linear) M2	17½x4½x6	5 lb	5840-99-999-2693	14
Oscillator (coherent) M1	17½x6x6	5½ lb	5840-99-999-2913	15
Mixer stage (frequency) M1	17½x6x6	5½ lb	5840-99-999-2685	16
Regulator voltage (+250V) M2	17½x7¼x6	9 lb	6110-99-999-2664	17
Control (i.f. level) M7	17½x6x3	2 lb	5840-99-999-9049	18
Attenuator assembly	17¾x7½x5¾	11 lb	10W/5905-99-999-8873	1
Cable storage box assembly	17½x7½x6	-	-	1
Generator pulse, video zero	14x9x5	6 lb	5840-99-624-8669	19
IF Bypass relay (Cabinet 5975-99-659-4690 only)	17½x4 7/8x6	-	-	20

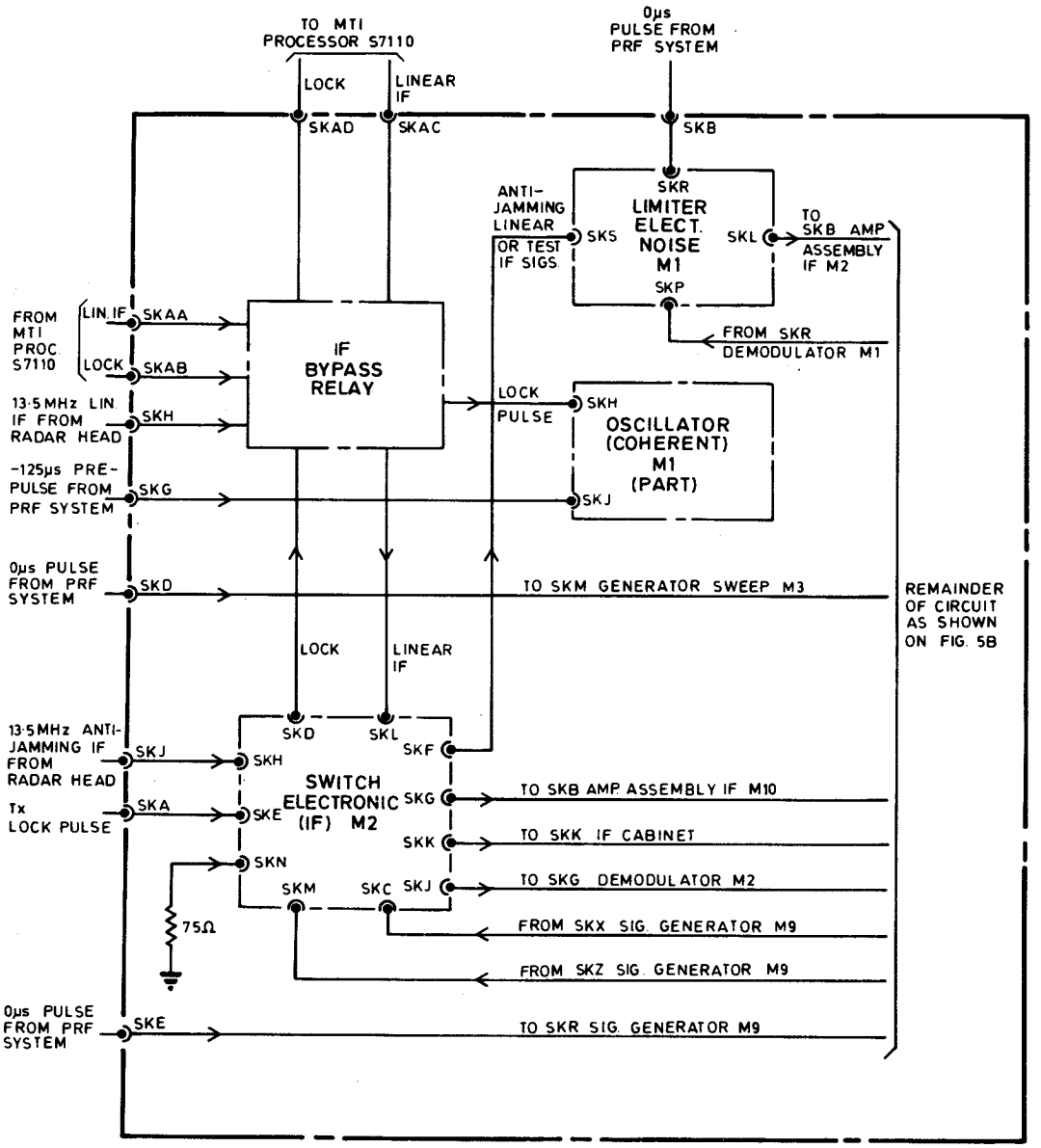


Fig.5A IF cabinet (CEE 5975-99-659-4690) signal interconnections (part circuit) (post mod CA8125/3)

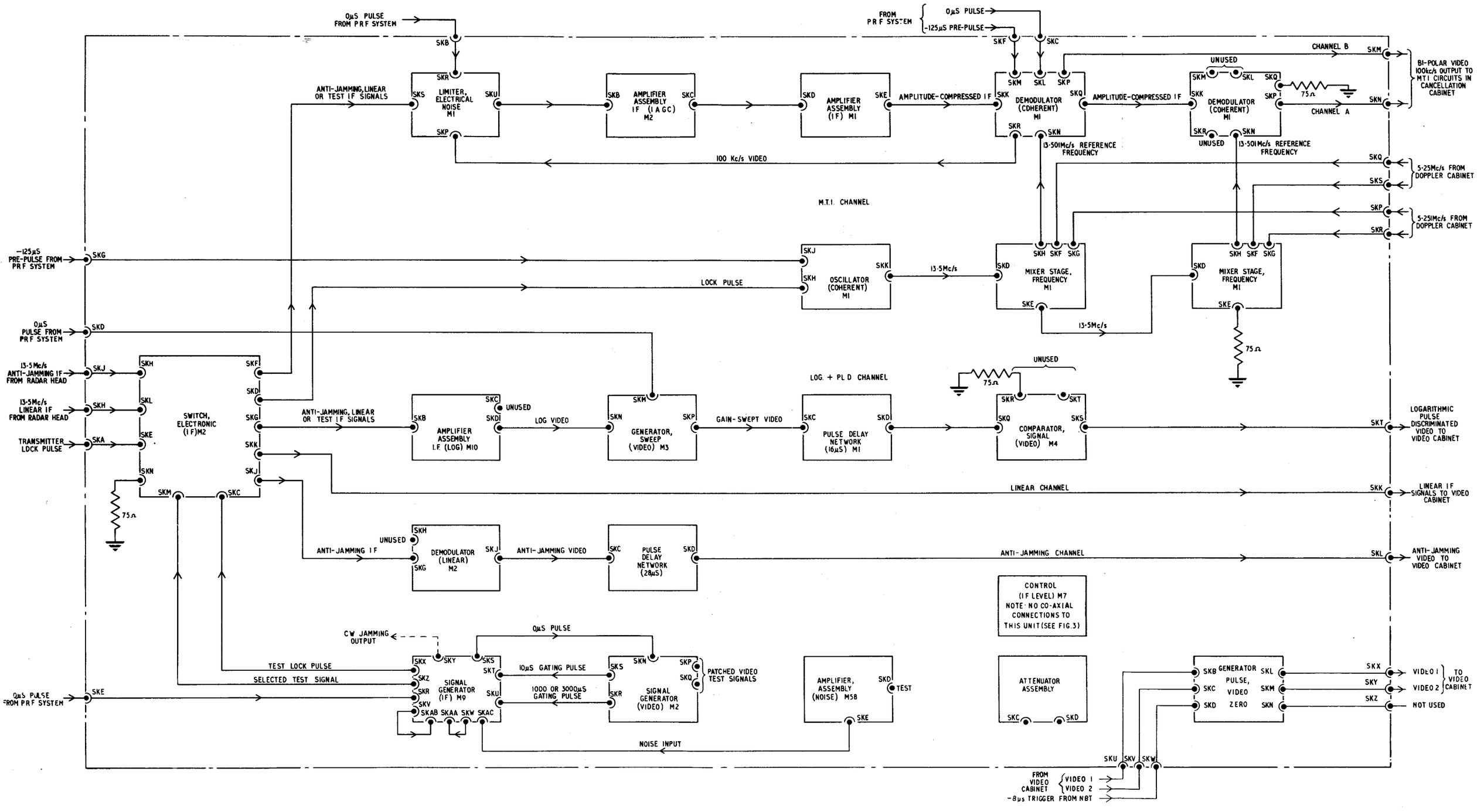
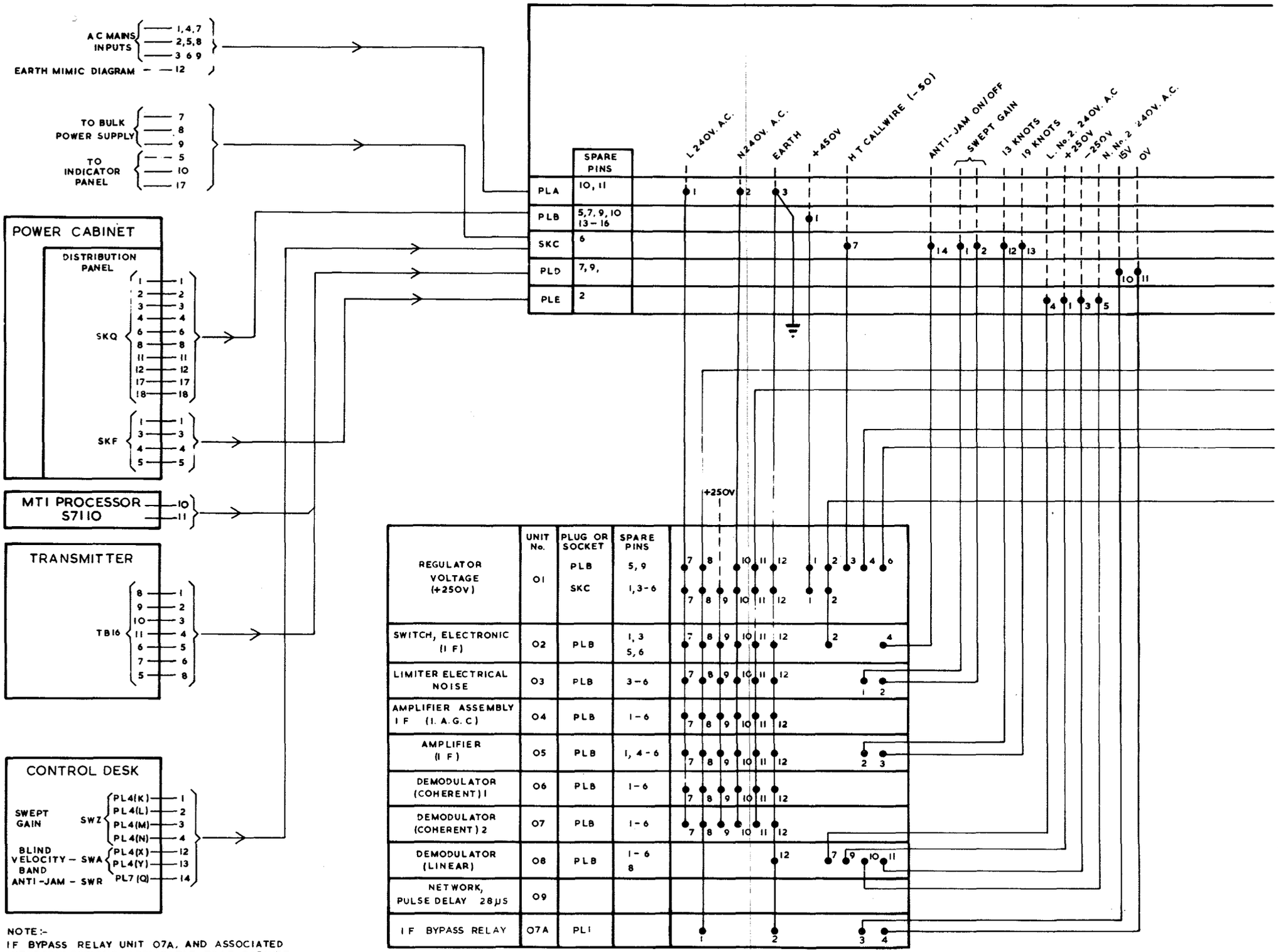


Fig. 5B

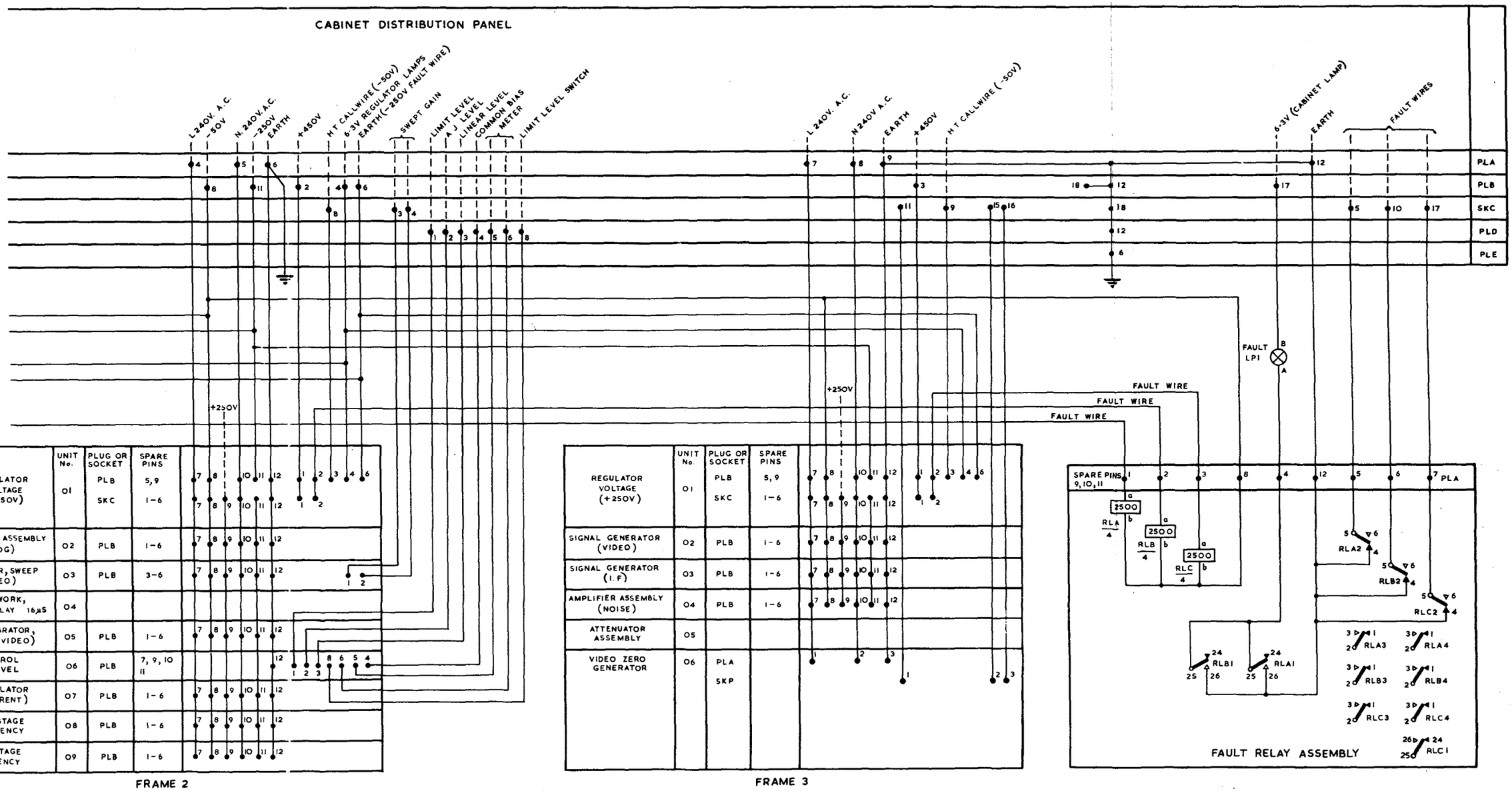
IF Cabinet: signal interconnections (5975-99-999-2833) and part circuit for IF Cabinet (5975-99-659-4690)

Fig. 5B



NOTE:-
I F BYPASS RELAY UNIT 07A, AND ASSOCIATED INTERCONNECTIONS APPLICABLE TO I F CABINET 5975-99-659-4690 ONLY — MOD. No. CA8125/3. (INTEGRATION OF MULTI-FILTER MTI PROCESSOR S7110 INTO SIGNAL PROCESSING SYSTEM)

Fig. 6A I F Cabinet (5975-99-999-2833) and (5975-99-659-4690): power distribution part circuit Fig. 6A



REGULATOR VOLTAGE (+250V)	UNIT No. 01	PLUG OR SOCKET PLB	SPARE PINS 5, 9
		SKC	1–6
AMPLIFIER ASSEMBLY I F (LOG)	02	PLB	1–6
GENERATOR, SWEEP (VIDEO)	03	PLB	3–6
NETWORK, PULSE DELAY 16μS	04		
COMPARATOR, SIGNAL (VIDEO)	05	PLB	1–6
CONTROL (I F) LEVEL	06	PLB	7, 9, 10 11
OSCILLATOR (COHERENT)	07	PLB	1–6
MIXER STAGE FREQUENCY	08	PLB	1–6
MIXER STAGE FREQUENCY	09	PLB	1–6

FRAME 2

REGULATOR VOLTAGE (+250V)	UNIT No. 01	PLUG OR SOCKET PLB	SPARE PINS 5, 9
		SKC	1–6
SIGNAL GENERATOR (VIDEO)	02	PLB	1–6
SIGNAL GENERATOR (I.F)	03	PLB	1–6
AMPLIFIER ASSEMBLY (NOISE)	04	PLB	1–6
ATTENUATOR ASSEMBLY	05		
VIDEO ZERO GENERATOR	06	PLA	
		SKP	

FRAME 3

Fig. 6B

IF Cabinet: power distribution (5975-99-999-2833) and (5975-99-659-4690) part circuit

Fig. 6B
Chap. 1
Page 11/12

Appendix I

CONSTRUCTIONAL DETAILS OF CABINET

LIST OF CONTENTS

Introduction

1. The information given in this appendix refers to a standard cabinet, electrical equipment, i.e., a cabinet having three full-length unit frames. Mechanical deviations from this type of construction are described in the individual cabinet chapters.

General construction

2. The cabinet, electrical equipment (*Chap.* 1, *fig.* 2) is of the standard Air Ministry type, its overall dimensions being 7 ft. $0\frac{1}{4}$ in. high, $23\frac{1}{2}$ in. wide and $21\frac{1}{8}$ in. deep. The construction is of preformed, sheet steel sections, the top and bottom sections being bolted to the sides. Electrical earth continuity is ensured by the use of bonding connectors at each inside corner of the cabinet.

3. Full length doors are fitted at the front and rear of the cabinet, giving access to the unit mounting frames. To gain full access to the units, however, the frames must be withdrawn from the front of the cabinet. It should be noted that door or frame interlocks are not fitted in these cabinets, and that with either door open points are exposed which carry h.t. potentials.

4. The unit frames are mounted on telescopic runners, enabling the frames to be extended clear of the cabinet. When the frames are fully inserted in the cabinet they are automatically locked in position by a spring-loaded catch on the top runners. To release a frame for withdrawal from the cabinet, the catch is released by moving the lever to the left, and while holding it in this position the frame is pulled towards the operator.

Unit removal

5. When it is required to remove a unit from a frame, the following procedure should be adopted :

(1) Remove all connections from the rear of the unit.

(2) Withdraw the frame from the cabinet to the full extent of the runners.

(3) Remove all coaxial connectors, if any, from the unit chassis.

(4) Unscrew the four captive screws securing the unit to the frame, and remove the unit.

Frame removal

6. The frame is secured to the runners by four hexagon-headed bolts, two at the top and two at the bottom. To remove a frame from the cabinet, it is only necessary to extend the frame to the full extent of the runners, and remove the four bolts. It is assumed that all units have been removed from the frame, and all frame wiring disconnected.

Ventilation

7. The cabinet is provided with forced-air ventilation, air being ducted into the bottom of the cabinet, passing over and between the unit frames, and finally being exhausted via a trunking at the top of the cabinet. The front or rear door of the cabinet may be opened without interrupting the air flow.

Chapter 2

SWITCH ELECTRONIC (I.F.) M2

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

Fig. 1 Switch electronic (I.F.) M2 : front view

INTRODUCTION

General

1. The electronic i.f. switch unit (*fig.* 1 *and* 4) is housed in frame 1 of the i.f. cabinet. The unit enables the input to the MTI and logarithmic signal channels to be selected from three inputs consisting of anti-jamming i.f. and linear i.f. signals both from the radar head, and locally generated test signals. Under operational conditions selection of the inputs to the signal channels is effected by means of the ANTI-JAM switch on the operator's console, whilst under test conditions selection is effected by the RADAR SIG. and TEST SIG. switches on the unit. The anti-jamming i.f. signal is attenuated by 6dB within the unit to compensate for differences in level between the two i.f. signal inputs, and all signals fed to the MTI channel are attenuated by a further 15dB.

2. In addition to the selective function described above, the unit also provides two unswitched outputs, one of which is derived from the unattenuated anti-jamming i.f. signal and fed via linear demodulator M2 to the anti-jamming channel, and the other is derived from the linear i.f. signal, attenuated by 15dB, and fed to the i.f. amplifier assembly (linear) M9 (*Sect.* 5, *Chap.* 8) in the linear channel.

3. A lock pulse output, used to initiate the operation of the coherent oscillator in the i.f. cabinet, is selected within the unit from pulses derived from either the radar transmitter or the i.f. signal generator M1 (*Chap.* 12) within the i.f. cabinet.

Performance characteristics

4. The relationship between the various switching combinations and the outputs supplied to the MTI and logarithmic signal channels is given in Table 1.

Inputs

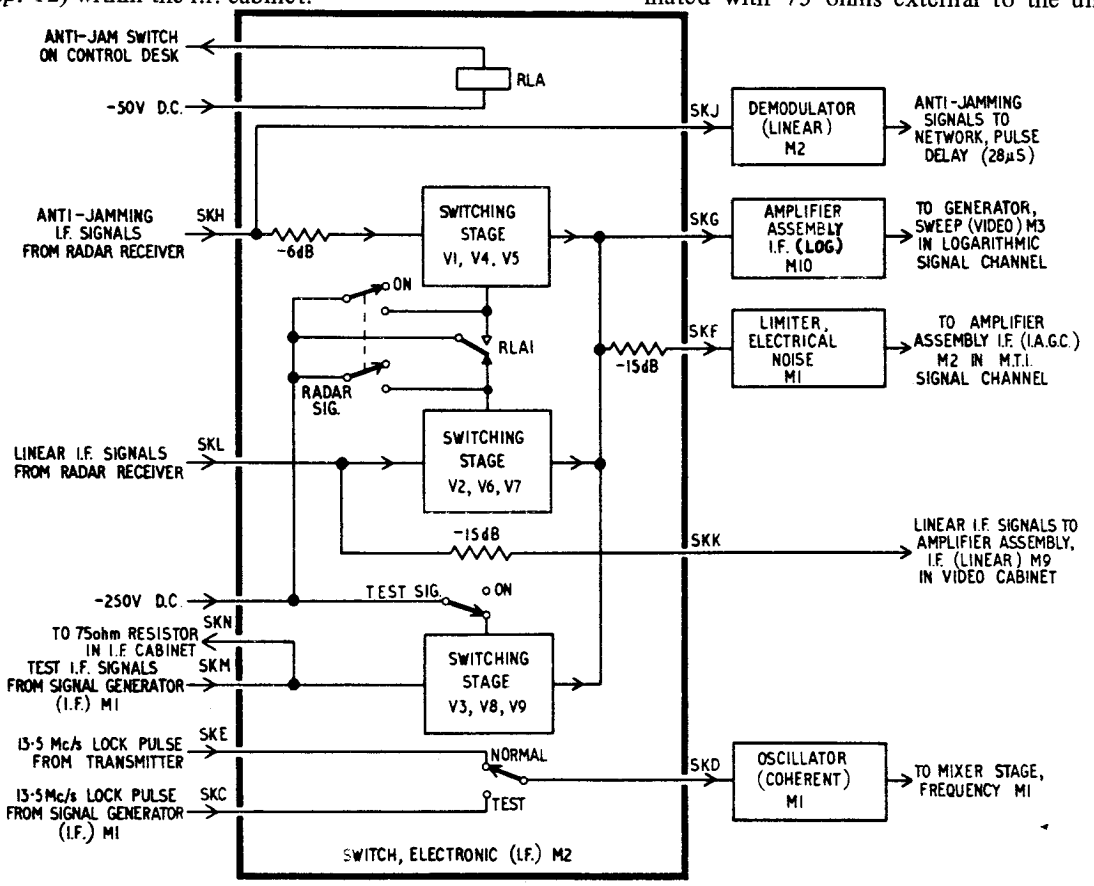
5. The unit receives the following inputs:

(1) SKH
Anti-jamming i.f. signals derived from the Dicke-Fix receiver system (*Part* 2, *Sect.* 2, *Chap.* 4), at a noise level of approximately 50mV r.m.s. at 13·5 Mc/s ± 100kc/s, terminated in 75 ohms.

(2) SKL
Linear i.f. signals from the radar receiver at a noise level of approximately 300μV r.m.s. at 13·5 Mc/s ± 10kc/s. The input impedance at 75 ohms.

(3) SKM
Test i.f. signals, from the i.f. signal generator M1. 1·5V r.m.s. of signal at 13·5 Mc/s ± 10kc/s, and 200mV r.m.s. of noise, terminated in 75 ohms.

◄(4) SKN
Is wired in parallel with SKM but when the unit is fitted to the i.f. Cabinet SKN is terminated with 75 ohms external to the unit.►



◄ Fig. 2 Functional block diagram ►

(5) SKE

0 microseconds 13.5 Mc/s lock pulse derived from the transmitter (*Part* 2, *Sect.* 4, *Chap.* 7) at a nominal p.r.f. of 250 per second. The pulse duration is 9 (±2) microseconds with an input termination of 75 ohms when not in use.

(6) SKC

0 microseconds 13.5 Mc/s lock pulse derived from the i.f. signal generator M1 at a nominal p.r.f. of 250 per second. The pulse duration is 9 (±2) microseconds with an input termination of 75 ohms when not in use.

Outputs

6. The following outputs are provided by the unit:

(1) SKG

Radar i.f. signal selected from the 13.5 Mc/s inputs to the SKH, SKL and SKM and fed to the i.f. amplifier assembly (log.) M10 in the logarithmic signal channel. The output has a gain of unity over the inputs at SKL or SKM, and of nominally −6dB when the input at SKH is selected. The output impedance is 75 ohms.

(2) SKF

Radar i.f. signals selected as those for SKG above, but all output signals are attenuated by 15dB prior to application to the electrical noise limiter M1 in the MTI channel where the output is terminated in 75 ohms.

(3) SKJ

Anti-jamming i.f. signals. As the input to SKH; fed to demodulator (linear) M2 in the anti-jamming channel and terminated in 75 ohms in that unit.

(4) SKK

Linear i.f. signals. As the input to SKL but attenuated by 15dB and fed to the i.f. amplifier assembly (linear) M9 in the linear channel in the video cabinet. Output impedance is 75 ohms.

(5) SKD

Lock pulses selected from the inputs at SKE or SKC and fed to the coherent oscillator M1.

Channel isolation

7. Isolation between switched channels is greater than 60dB.

TABLE 1

Switching combinations

ANTI-JAM switch on console	TEST SIG. switch SWA	RADAR SIG. switch SWB	Output i.f. signal
Off position	Off position	ON	Linear signal
ANTI-JAM	Off position	ON	Anti-jamming signal
Off position	ON	Off position	Test signal
ANTI-JAM	ON	Off position	Test signal
Off position	ON	ON	Linear signal, plus test signal
ANTI-JAM	ON	ON	Anti-jamming signal, plus test signal
Off position	Off position	Off position	No output
ANTI-JAM	Off position	Off position	No output

Brief circuit description

8. The unit comprises three single-stage i.f. amplifiers each of unity gain and sharing the primary of an output transformer as a common anode load. Each stage receives a separate input signal, and any two of the three stages may be biased off independently. Selection of the operative stage is effected by a relay controlled by the ANTI-JAM switch on the radar operator's control desk, and also by switches within the unit. It is also possible to obtain the condition whereby one of the i.f. signal channels (linear or anti-jamming) is biased off, leaving the other i.f. signal channel and the test signal channel still operative.

CIRCUIT DESCRIPTION

Power supplies

9. The 240V a.c. mains supply to the fused primary of the valve heater transformer TR1 is routed via PLB/7 and PLB/10. Power at these points is controlled by the main system switch for all units of the system. The transformer produces 6.3V at 2A from its secondary and interference isolation of the heaters line is provided by r.f. filter X2 and inductors L3, L5 and L7.

10. +250V from the +250V regulator in frame 1 is fed into the unit on PLB/9 (+250V) and PLB/12 (earth). Interference isolation is provided by X1, L1, L2, L4 and L6.

11. A −250V supply is used to switch off the channels not required. This supply enters the unit at PLB/11 and PLB/12 (earth), and interference isolation is provided by filter X3.

I.F. amplifiers

12. Three separate i.f. amplifiers are employed within the unit, each being separately screened. but sharing a common anode load provided by TR4. Since the three amplifiers are similar only one is described, and a simplified circuit of this is shown in fig. 3. For the purpose of this description the component references used in fig. 3 are the same as those for the anti-jamming amplifier, V1.

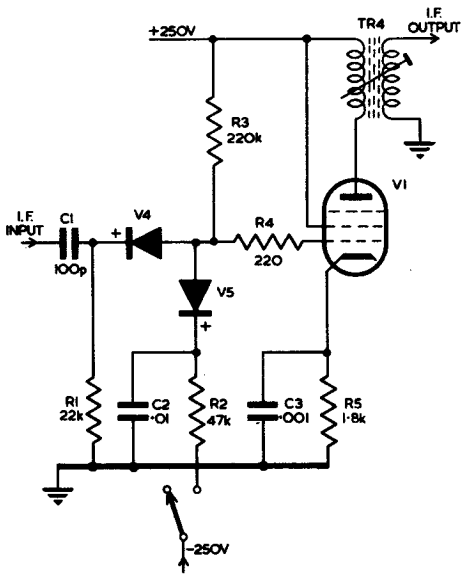


Fig. 3 I.F. amplification state

13. Under operating conditions the diode V4 is conducting through R3 and R1. The resulting positive potential at the junction of diodes V4 and V5, in conjunction with the self-bias developed across R5 and C3, maintains V1 in a conducting condition.

14. I.F. signals at 13.5 Mc/s are passed via C1 and V4 to the grid of the amplifier V1, which has a stage gain of unity. The resultant output is developed in the primary of the anode load transformer TR4. The tranformer is tuned to 13.5 Mc/s and the output is taken from its secondary.

15. If no output is required from the amplifier, a bias of −250V is applied through R2 to the diode V5. This diode will then conduct, and the ratio of R3 to R2 is such that the potential at the junction of V4 and V5 is reduced to approximately −50V thereby causing V1 and V4 to stop conducting, rendering the amplifier inoperative.

Anti-jamming signal amplifier

16. Anti-jamming i.f. signals originating from the Dicke-Fix receiver in the radar head enter the unit on SKH, and, after 6dB attenuation by the potential divider R25 and R26, are fed to the amplifier formed by V1 and its associated components. The unattenuated anti-jamming i.f. is also made available at SKJ, from where it is routed direct to the anti-jamming channel.

Linear signal amplifier

17. Linear i.f. signals from the radar receiver are applied via SKL to the amplifier formed by V2 and its associated components. The input circuit of this stage comprises a potential divider, formed by R8 and the GAIN LINEAR potentiometer RV1, the purpose of which is to provide compensation for differences in input levels between this stage and the anti-jamming amplifier. Input impedance matching at 75 ohms is provided by R7 in parallel with the potential divider. An output to the linear channel is provided at SKK, the signals at this socket being the linear i.f. input signal at SKL, but attenuated by 15dB by R27.

Test signal amplifier

18. Test signals derived from the i.f. signal generator are fed into the unit on SKM, which is connected in parallel with SKN. From SKM the signal is routed to the i.f. amplifier formed by V3 and its associated components. The input circuit of this stage consists of a potential divider, formed by GAIN TEST potentiometer RV2 with R15, the purpose of which is to provide compensation for differences in input levels to the channels.

Channel selection

19. Selection of the signals to be fed to the logarithmic signal and MTI channels is determined by the condition of relay RLA and the RADAR SIG.(SWB) and TEST SIG.(SWA) switches on the unit. The

relay receives its energizing supply via PLB/8, and the earth return is completed via PLB/4 and the ANTI-JAM switch on the radar operator's control desk. Under normal operating conditions SWB is set to the ON position and SWA to the OFF position (i.e. closed), thus the test signal amplifier is switched off and the operation of the other two amplifiers is controlled solely by RLA.

20. With RLA de-energized, i.e. anti-jamming switched on, RLA1 contacts 1 and 2 are made and −250V via R6 is supplied to the diode V7 in the linear signal amplifier and the stage is switched off. When RLA is energized RLA1 changes over and the −250V is removed from the linear signal amplifier and applied to diode V5 in the anti-jamming signal amplifier. This latter amplifier is thus switched off and the linear signal amplifier is allowed to conduct.

21. When it is required to switch off both radar signals, relay RLA is overidden by setting the RADAR SIG. switch, SWB, to the off position, thereby applying the −250V bias to both the anti-jamming and linear signal amplifiers.

22. To inject test signals into the MTI and logarithmic signals channels, both radar signal amplifiers can be switched off by SWB as described in the previous paragraph, and the test signal i.f. amplifier allowed to conduct by placing the TEST SIG. switch, SWA, to the ON position thus removing the −250V bias from the diode V9.

23. The output of the selected amplifier is developed at the secondary of TR4 and is fed to SKG and also, after 15dB attenuation by R24, to SKF. The signal at SKG is applied to the logarithmic signal channel and that at SKF to the MTI channel.

Lock pulse selection

24. The source of the lock pulses required by the coherent oscillator is selected by the three-position rotary TEST/NORMAL switch, SWC. When the switch is set to the NORMAL position, lock pulses fed from the transmitter at the radar head via SKE are switched to SKD, and thence to the coherent oscillator. Similarly, when the switch is set to the TEST position, the lock pulses produced by the i.f. signal generator are routed via SKC and SKD to the coherent oscillator. In either of these two positions of the switch the lock pulses not in use are terminated in 75 ohms by R23. A third position of the switch, midway between TEST and NORMAL, is not used.

25. When switch SWC is set to TEST or to its unused position, contacts on the front section of the switch wafer complete the supply circuit to earth, via PLB/2, for the fault relay assembly on the i.f. cabinet. The fault relay for frame 1 of the cabinet is thus energized to light the cabinet fault lamp, thereby indicating that an abnormal condition exists in that frame of the cabinet.

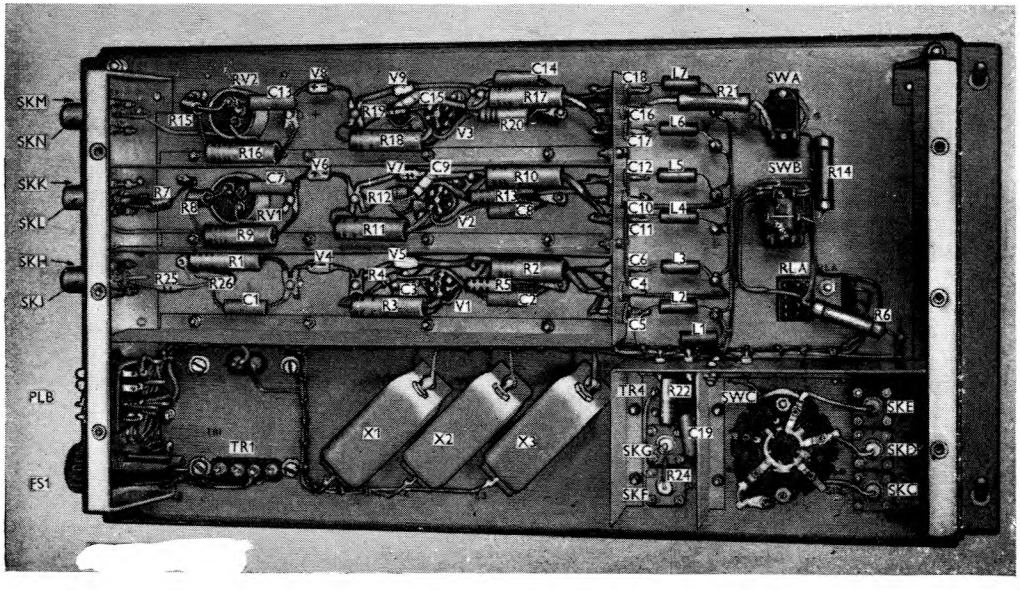


Fig. 4. Switch electronic (I.F.) M2 : rear view

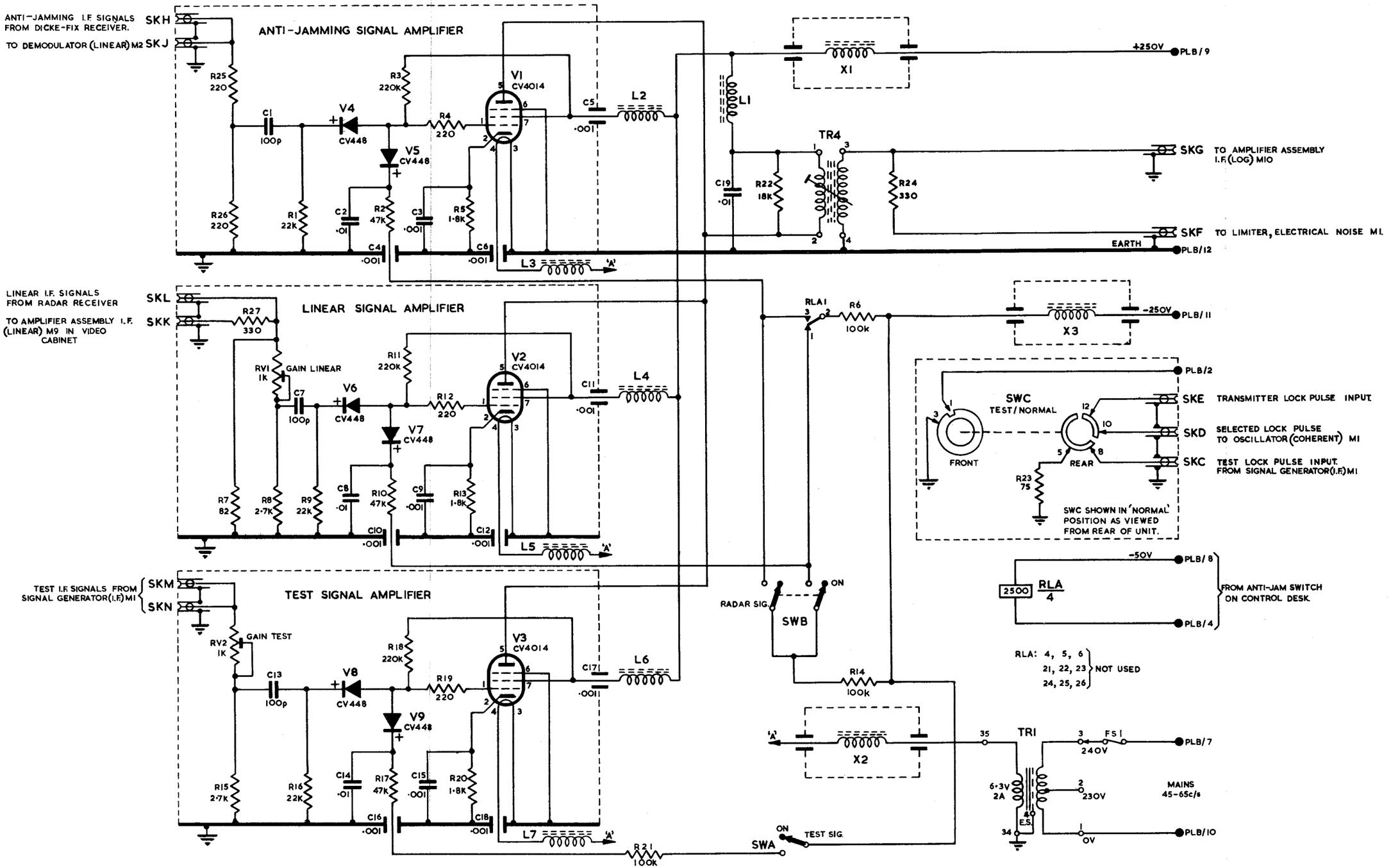


Fig.5

Switch electronic (i.f.)M2: circuit

Fig.5

Chapter 3

AMPLIFIER ASSEMBLY, I.F. (LOG.) M10

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

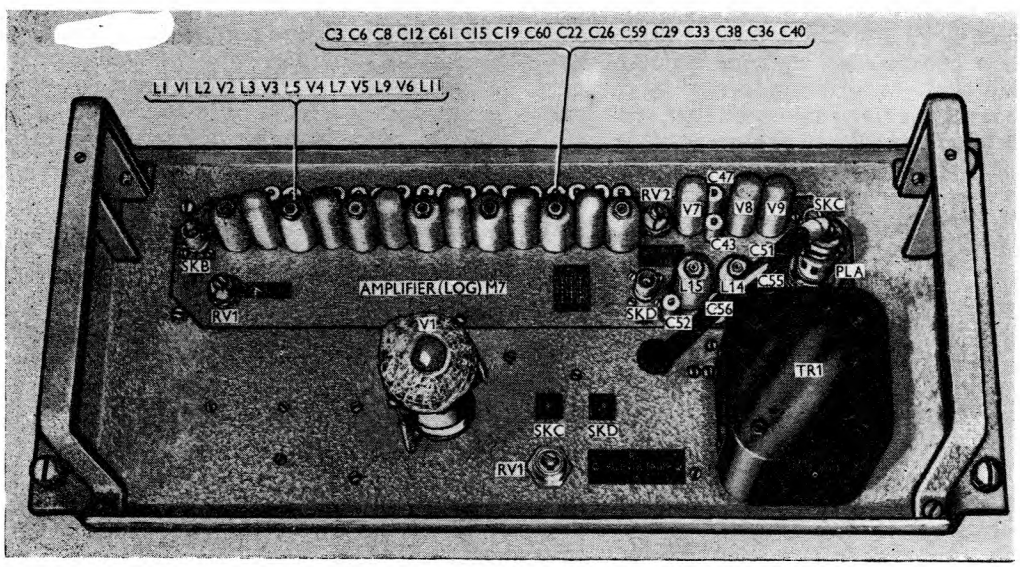


Fig. 1. Amplifier assembly, i.f. (log.) M10: front view

INTRODUCTION

General

1. The log. i.f. amplifier assembly M10 (*fig.* 1) forms part of the logarithmic signal channel and is situated on frame 2 of the i.f. cabinet. The unit consists of a main chassis on which is mounted an interchangeable sub-assembly comprising the log. i.f. amplifier M7. Input power connections are brought to the main chassis, where a series regulator valve stage reduces the h.t. potential to a level suitable for application to the log. i.f. amplifier M7. A mains transformer, also on the main chassis, provides a supply to the heaters of all valves within the unit.

2. The unit provides logarithmic amplification and detection of the 13·5 Mc/s i.f. signals selected by the electronic switch unit M2 (*Chap.* 2), and produces a video output which is fed to the video sweep generator M3 (*Chap.* 4). The characteristics of the amplifier are such that the detected output is proportional to the logarithm of the i.f. input amplitude. This logarithmic law of amplification ensures that the unit will adequately amplify weak signals, and will continue to deliver an output for progressively stronger input signals.

Performance characteristics

3. The log. i.f. amplifier operates at a centre frequency of 13·5 Mc/s, and has a bandwidth at 3dB points of 900 (±100) kc/s. The amplifier has a maximum overall gain of approximately 100dB, and the input dynamic range is 90dB.

4. An I.F. GAIN control on the unit allows the overall gain to be varied through a range of 12dB and a second preset control, OUTPUT LEVEL, enables the output from SKC to be adjusted over a range of 20dB.

Inputs

5. Anti-jamming, linear or test i.f. signals, at 13·5 Mc/s, as selected by the electronic switch unit, are fed directly into the log. i.f. amplifier at SKB, the input impedance being 75 ohms.

Outputs

6. The unit provides two video outputs; one of these, from SKC on the sub-assembly is positive-going (a.c. connected) into 75 ohms and is not used. The other output, from SKD on the sub-assembly, is negative-going (d.c. connected) with an output impedance of 1·35 kilohms; video signals from this socket are passed to the video sweep generator M3.

DETAILED DESCRIPTION

Main chassis

7. The power supplies required by the unit are brought in on PLB on the main chassis (*fig.* 2). The +250V supply enters on PLB/9 and PLB/12 (earth), and is applied to a voltage regulating circuit formed by V1 and its associated components. V1 acts as a conventional cathode follower, the cathode load of the valve being formed by the h.t. load of the amplifier (log.) sub-assembly. The grid of V1 is held at +100V by the potential divider formed by R1, ◀RV1▶ and R4, connected between the +250V line and earth, with the result that by cathode follower action the output at the cathode of the valve is held at a positive potential of 100V ±5V, irrespective of variations of cathode loading. This +100V supply is fed to the amplifier sub-assembly via SKA/D and SKA/F (earth).

8. The valve heaters supply required by the unit is produced by the mains transformer TR1, mounted on the main chassis. The primary of the transformer receives the a.c. mains supply from PLB/10 and PLB/7, via FS1, and produces at its secondary 6·3V, which is fed to the heaters of V1, on the main chassis, and, via SKA/C, to the heaters of the valves in the sub-assembly.

Amplifier (log.) M7

Constructional details

9. The screened amplifier (log.) M7 sub-assembly is mounted on the underside of the unit main chassis by four 4BA cheesehead screws through the main chassis into hank bushes on the sub-assembly. A flanged baseplate on the sub-assembly completes the screening and is secured by fourteen 8BA cheesehead screws with crinkle washers into tapped holes in the two flanges.

10. Valves V1–V9 are of the sub-miniature wired-in type and are inserted from the chassis underside into screening cans integral with the chassis. A phosphor-bronze heat dissipator inside each screening can provides a heat conduction path from valve to chassis. Fig. 3 indicates the method of fitting the valves. Most of the decoupling capacitors are also fitted into screening cans integral with the chassis. Connections to these capacitors are made as shown in fig. 4.

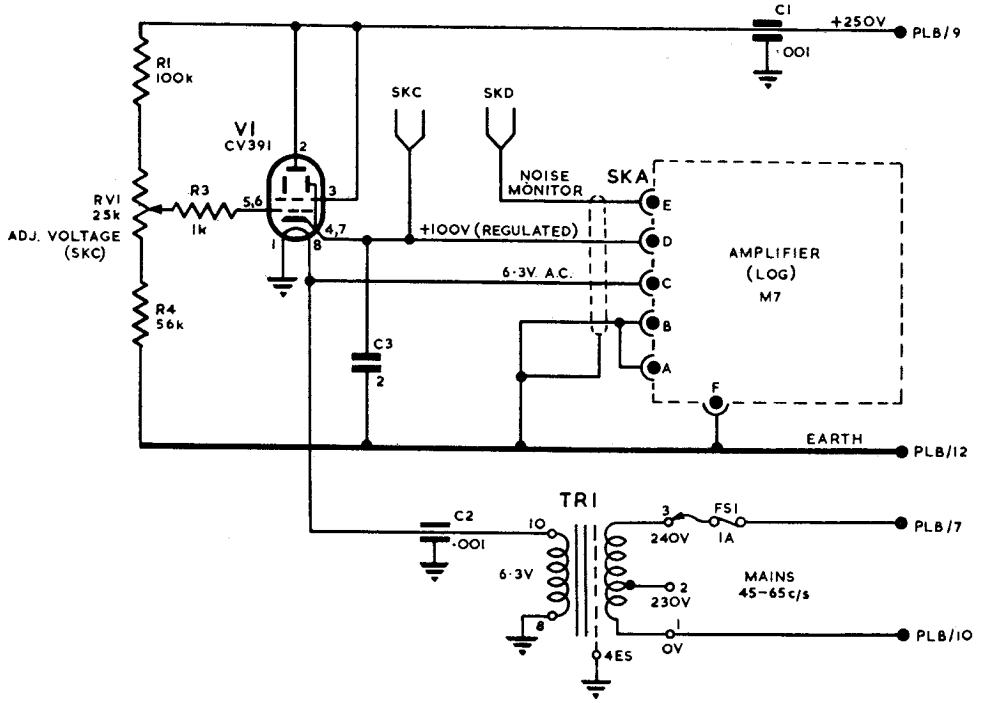


Fig. 2. Main chassis: circuit

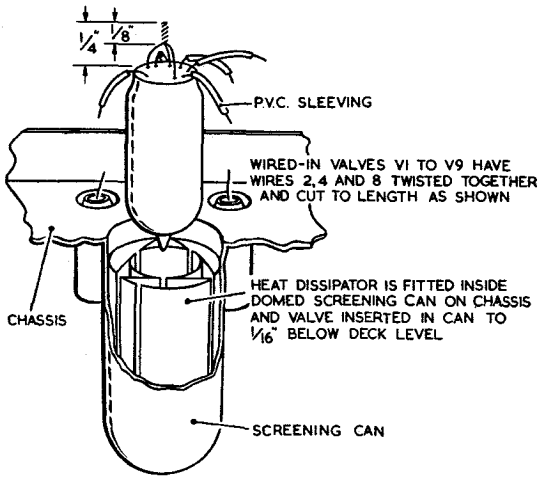


Fig. 3. Mounting details for wired-in valves

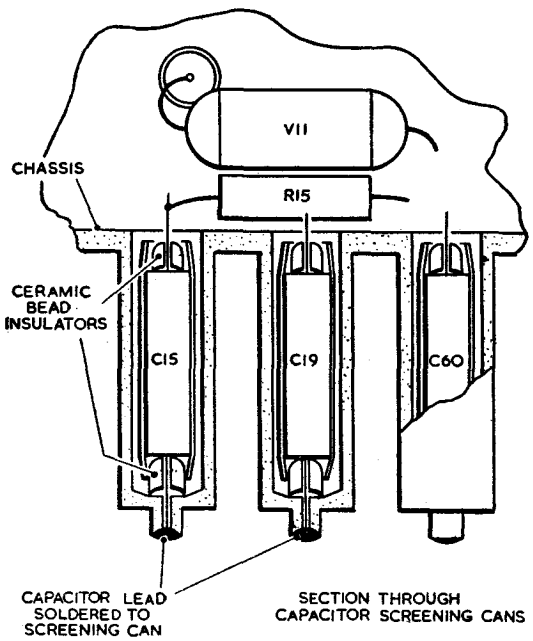


Fig. 4. Method of fitting decoupling capacitors

Principles of logarithmic amplification

11. A radar receiver giving a linear or square law response to small input signals will usually saturate when the input voltage exceeds a few millivolts. Response to clutter, from jamming or storms, can therefore saturate the receiver, and in so doing cause loss of target signals, even though the target signal may be of a higher amplitude than the clutter. This may be overcome by using a receiver which gives full amplification to small signals and near unity amplification to large signals. The logarithmic receiver, which has a response such that the output is the logarithm of the input, fulfils these requirements, and behaves in such a way that the amplitude of noise or clutter at its output is held substantially constant, whilst signals above noise or clutter are subject to the logarithmic compression.

12. The log. amplifier described here uses the successive detection principle and the essential difference between this amplifier and a straightforward i.f. amplifier is that the latter has a single detector at the end of its i.f. chain, whereas the logarithmic amplifier has a detector following each i.f. stage in the chain, the outputs of all the detectors being added. Each amplifying valve in the chain therefore, besides feeding its output at i.f. to the following valve, also feeds into its own rectifier and can thus make an independent contribution to the output of the amplifier regardless of the valves that follow it. The basic circuit in fig. 5 shows this arrangement.

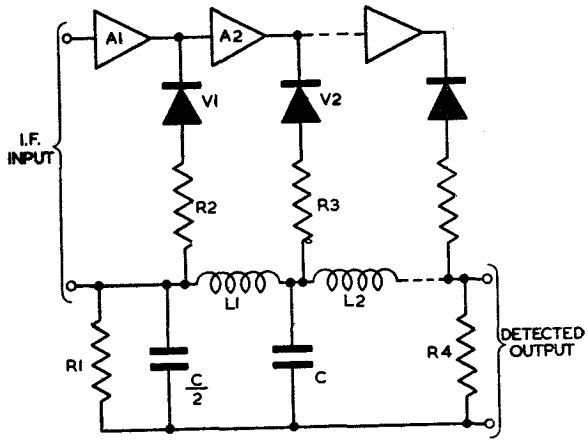


Fig. 5. Log amplifier: basic circuit

13. Each detector feeds its own load, these individual loads (R2,R3) being coupled together through a common impedance formed by the delay line, which is terminated by resistors R1 and R4.

14. The video delay line is necessary in this type of amplifier because the video output is built up by adding the contributions from all the detectors of the amplifier. Without the delay line, this would appear on the c.r.t. as a pulse consisting of a series of steps. By having a correctly terminated delay line, with the delay per section being equal to the delay of the i.f. pulse through the amplifying stage, and with the sections inserted between detector outputs, the detector outputs add in phase, and the resultant output resolves into a single-edged pulse. Since the line is formed by a succession of pi-section networks, each section consisting of a series inductance with a shunt capacitor connected at each end, when the sections are connected in series the shunt capacitors between sections become twice the value of the input and output shunt capacitors. Thus, in fig. 5, the intermediate shunt capacitors are referred to as C, and the input capacitor as $\frac{C}{2}$. The delay line also serves as i.f. decoupling between successive stages of the amplifier.

15. The logarithmic amplifier operates on the principle that each i.f. valve in the amplifier will saturate as the input is increased. This is due to

grid current damping and to curvature of the dynamic characteristic of the valve.

16. Assume that the amplifier in fig. 5 has six amplifying stages, each having a stage gain of A, and that the i.f. voltage at the anode of the valve is Va when the voltage applied to the grid saturates the stage. This output voltage is rectified and applied to the delay line and a portion of this voltage will be developed across the terminating resistance; let this voltage be V.

17. With a signal at correct i.f. fed to the input of the amplifier, the signal amplitude being just sufficient to saturate the sixth amplifying stage, voltages developed across the delay line terminating resistance will be: V due to stage 6, $\frac{V}{A}$ due to stage 5, $\frac{V}{A^2}$ due to stage 4, and so on. It follows that the input signal voltage required to achieve this result would have an amplitude $\frac{Va}{A^6}$.

18. If the signal is now increased A times so that the fifth amplifying stage becomes saturated, this stage will now contribute V volts to the delay line, so that the output is now: V due to stage 6, V due to stage 5, $\frac{V}{A}$ due to stage 4, and so on. Since each stage is working at a high gain the small outputs from the stages preceding the saturated stage can be neglected in this simplified approach. By increasing the input signal in steps of A times, thus saturating each stage in turn, the results are as follows:

Input	*Output*	*Output Difference*
$\frac{Va}{A^6}$	V	V
$\frac{Va}{A^5}$	2V	V
$\frac{Va}{A^4}$	3V	V
$\frac{Va}{A^3}$	4V	V
$\frac{Va}{A^2}$	5V	V
$\frac{Va}{A}$	6V	—

19. In this simplified description it may be stated that the difference in output, due to a voltage input change from $\frac{Va}{A}$ to $\frac{Va}{A^6}$ is 6V. Therefore, a logarithmic relationship exists between input and output over an input range of $\frac{Va}{A^6}$ to $\frac{Va}{A}$, and the output range is 1 to 6.

Logarithmic amplifier circuit

20. The full circuit of the log. amplifier is given in fig. 8. The h.t. and heaters supplies enter the sub-assembly at PLA, via SKA of the main chassis, and are filtered respectively by L14, C55, C53, C51 and L15, C52, C54, C56, with ·01μF capacitors across the heaters of V1 to V6.

21. The amplifier chain consists of six similar stages of i.f. amplification, V1 to V6, each stage being tuned to a centre frequency of 13·5 Mc/s. The input to the chain is at SKB, and consists of anti-jamming, linear or test i.f. signals, as selected by the electronic switch unit. From SKB the signals are applied to the grid of the first amplifier stage, V1, via a potential divider formed by the I.F. GAIN control, RV1, and R39. The potentiometer provides manual control of the maximum gain of the unit over a range of 12dB.

22. The i.f. output of V1 is developed across its 13·5 Mc/s tuned anode load L2. This output is fed via C7 to the grid of the next stage, V2, and also to the detector circuit formed by the crystal rectifier V15, in conjunction with C2, R38 and the delay line.

23. Pentode V2 functions in a similar manner to V1, and its output is detected as well as being fed to V3. The same process is repeated for all six stages of the amplifier chain, and the individual outputs of the six detector circuits are fed at successive points into a delay line composed of five pi sections, terminated at each end in its characteristic impedance of 2·7 kilohms. The delay line compensates for the inherent delay occurring in each stage of amplification with the result that the output from SKD, connected to the end of the line through filter choke L13 is a single, negative-going pulse formed by the in phase summation of the individual detector outputs, instead of a stepped pulse which would occur if the outputs were added without delay compensation. From SKD the output is routed directly to the video sweep generator.

24. In addition to this d.c.-connected negative output the unit also provides an a.c.-connected positive output at SKC; this output is not used in the existing application of the log. amplifier. To produce the positive-going output a sample of the negative-going output at the end of the delay line is applied to a polarity inverting amplifier, V7, and the resultant positive-going output from the anode of this valve is fed via the parallel connected cathode followers V8 and V9 to the output socket SKC. The level of the signal applied to the grid of V7, and hence the final output level at SKC, is controlled by the OUTPUT LEVEL potentiometer RV2 which forms part of the delay line terminating resistance. The high-value capacitance of C57 avoids any differentiation of the output when coupled to the input impedance presented by a succeeding unit.

Monitoring points

25. Test socket SKC on the main chassis is provided for checking the 100V d.c. output of the voltage regulator stage by means of a multimeter Type 1 or similar instrument.

26. The noise level of the amplifier may be checked with an oscilloscope at output socket SKD on the sub-assembly. For this check, the coaxial connection to the sweep generator should be disconnected. The amplitude of noise-plus-d.c. output should be not less than —2V.

Note . . .

Monitoring socket SKD on the main chassis provides an output at a lower level than that at socket SKD on the sub-assembly.

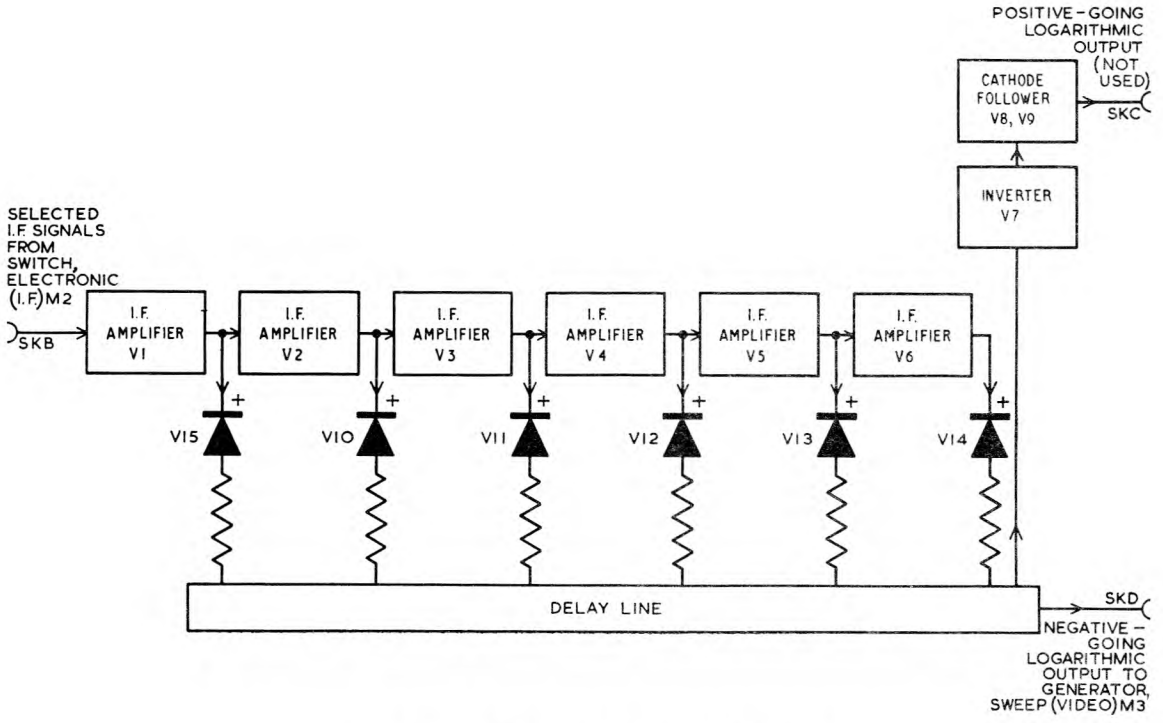
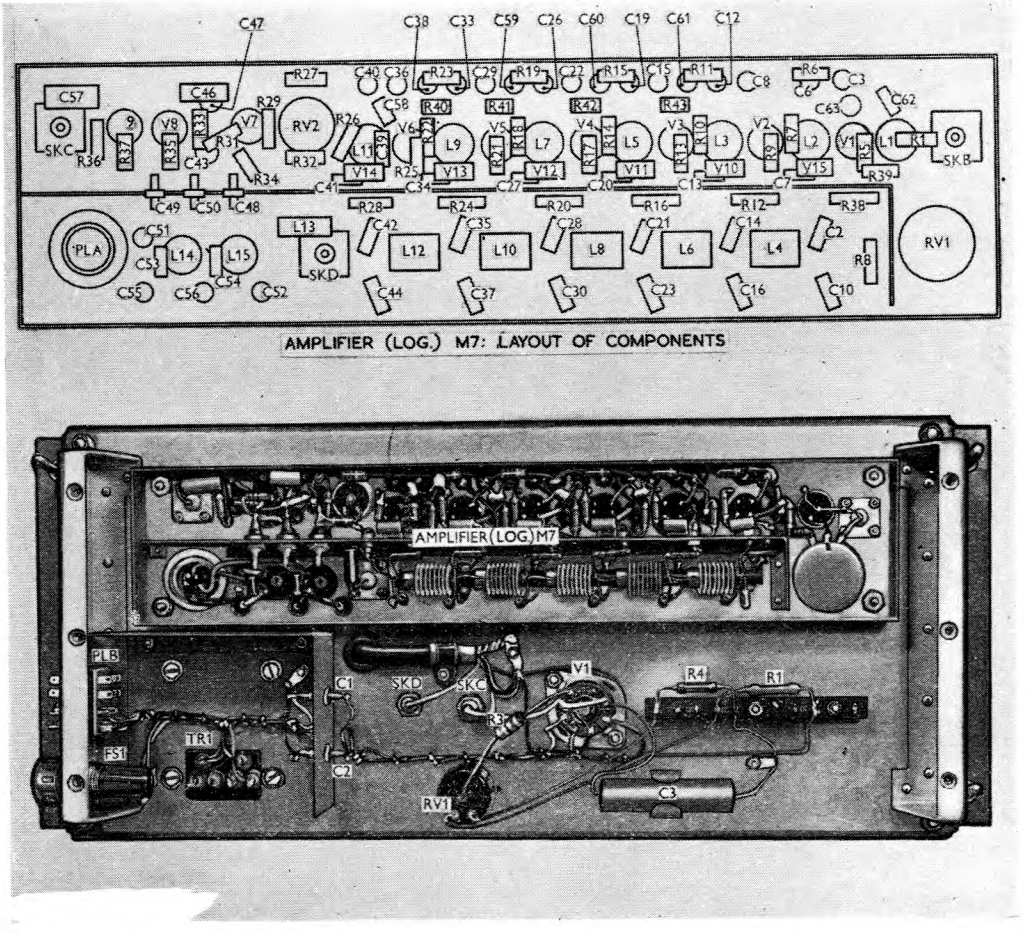
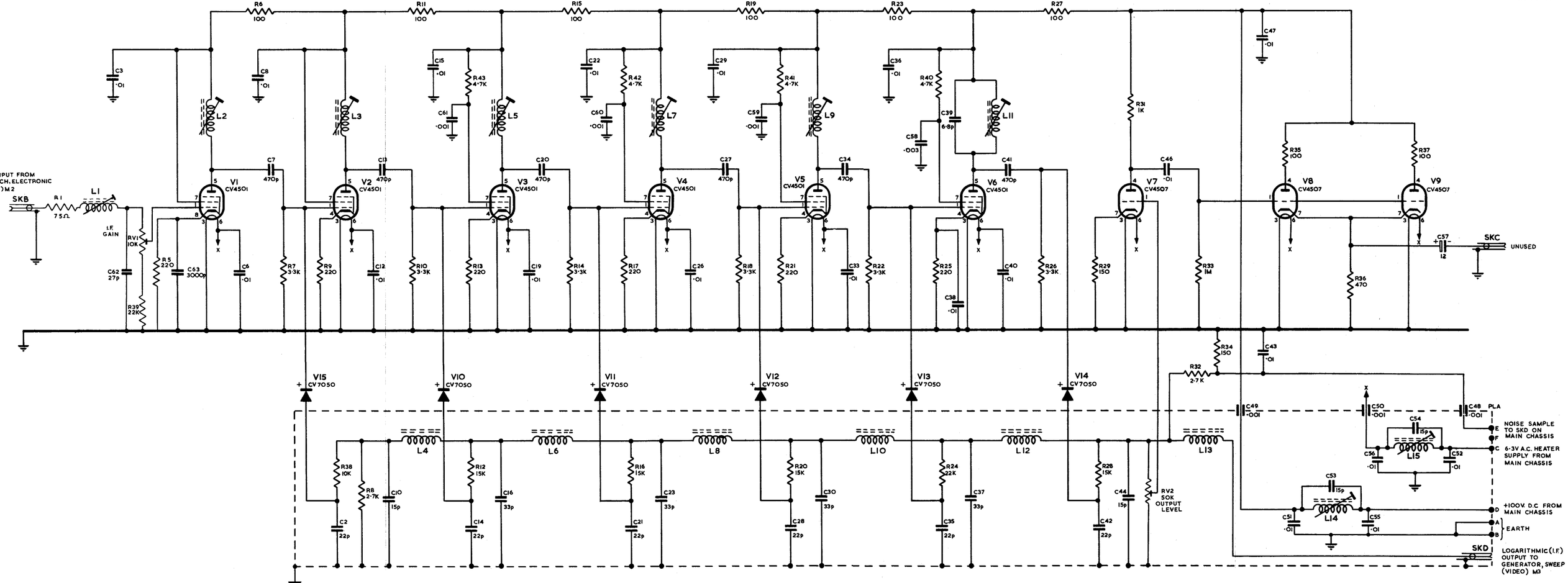


Fig. 6. Amplifier (log.) M7: block diagram



(C45570)

Fig. 7. Amplifier assembly, i.f. (log.) M10: rear view



Amplifier (log) M7: circuit

Fig.8

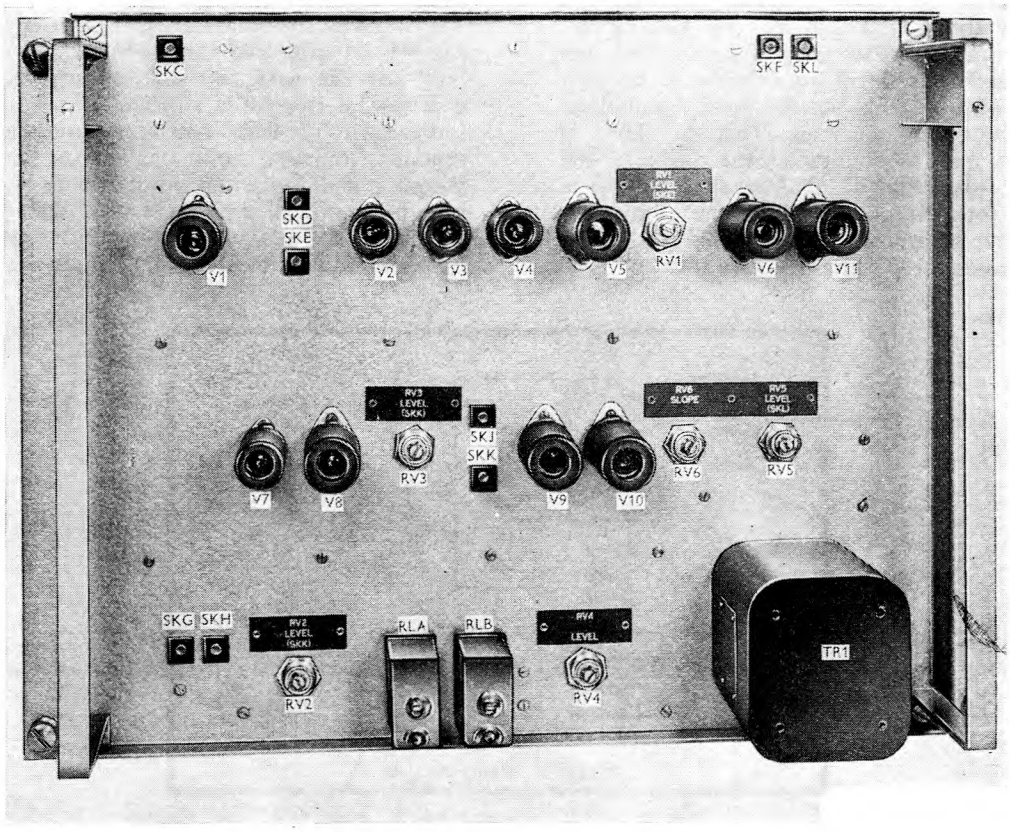
Chapter 4

GENERATOR SWEEP (VIDEO) M3

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS



(C37836)

Fig. 1. Generator sweep (video) M3: front view

Introduction

1. The generator sweep (video) M3 (*fig.* 1 *and* 5) forms part of the log channel and is mounted on frame 2 of the i.f. cabinet. The unit serves two purposes:—

(1) To eliminate the effect of angels from the displays.

(2) To prevent noise jamming from saturating the displays.

2. The first of these functions is achieved by effectively varying the amount of clipping which is applied to the video signals from the logarithmic i.f. amplifier M10 (*Chap.* 3). In practice, the potential at which clipping occurs is fixed, while the i.f. signal is negatively biased by an amount determined by a voltage waveform of suitable shape. The time duration of this waveform, which starts at a time equivalent to the instant of transmitter firing, is 4 milliseconds, during the first 500 μs (40 miles) of which the voltage rises exponentially towards the clipping level. During the next 500 μs (total 80 miles), the rise is interrupted and the voltage remains at a constant level. At the end of this period the voltage assumes an exponential rise for a third period of 500 μs (total 120 miles) after which it remains at a constant level for the remainder of the radar sweep. Since the waveform can be said to vary the level of the video signals with respect to time, it is referred to as a swept gain waveform.

3. The second of the unit functions is to minimize the effects of noise jamming which causes a degradation of the signal-to-noise ratio of the system. The function is achieved by making use of the fact that on an increase of input noise, the log i.f. amplifier produces an increase in the d.c. level of the output signal but the noise fluctuations remain substantially constant. This d.c. level is used in this unit to counteract the effect of the swept gain waveform, so that when jamming is present the amount of bias applied to the video signal is reduced, and less of the signal is clipped, thereby stabilizing the signal-to-noise ratio.

Performance characteristics

Inputs

◀4. The input to SKM consists of a positive-going 0 microseconds pulse from the p.r.f. system. The pulse duration is nominally 4 microseconds, at a p.r.f. of 250 p.p.s., while the amplitude is not less than 15V into an input impedance of 220 ohms.▶

5. The negative-going video signal from the amplifier assembly i.f. (log) M10 enters the unit at SKN, at a maximum amplitude of 6V.

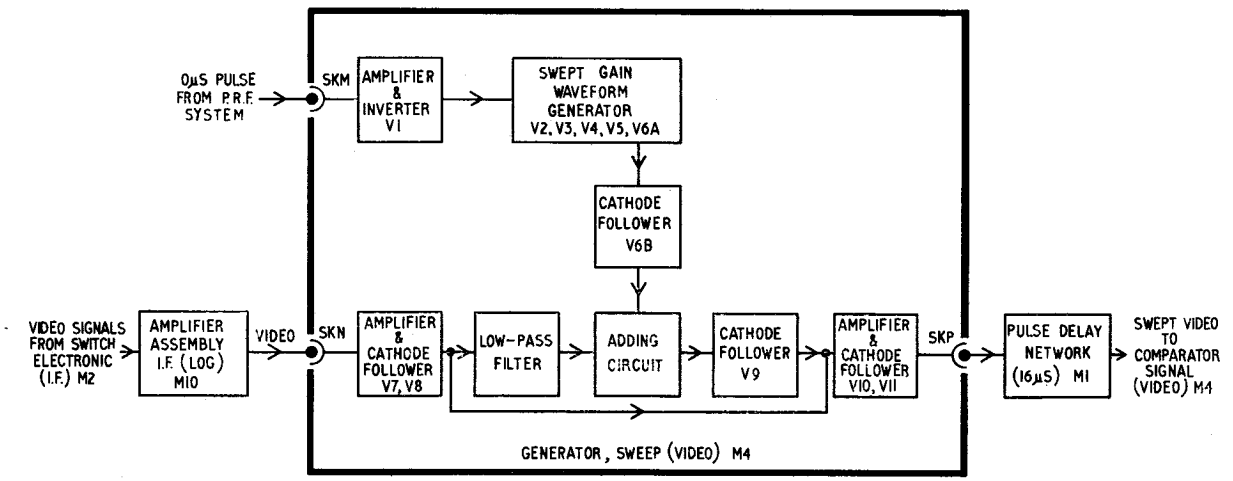
Output

6. The positive-going output at SKP comprises the video input at SKN modified by a voltage which is a function of time relative to 0 μs, and a function of the mean input voltage level. The maximum output amplitude is 1·5V into 75 ohms.

Brief circuit description

7. A functional diagram of the unit is given in fig. 2. The circuit consists basically of three parts; one part produces the swept gain waveform, the second part produces the d.c. level derived from the noise present in the video input, while in the third part of the circuit the swept gain waveform and d.c. level are added and the resultant used to determine the amount by which the video signals are clipped.

8. The circuit which produces the swept gain waveform is triggered by a pulse which occurs at 0 μs relative to the instant of transmitter firing. This pulse is amplified and inverted and used to charge a capacitor, the exponential discharge of which is controlled by a diode switching circuit. The result is a waveform which rises exponentially for 500 μs after the start, remains at a constant level for the next 500 μs, and assumes another exponential rise for a further 500 μs after which the capacitor is fully discharged and the potential remains constant until the arrival of the next trigger pulse. Since the input trigger pulses occur at a p.r.f. of 250 p.p.s., the total duration of the waveform is 4 ms, and this waveform is fed via a cathode follower to an adding circuit.



◀Fig. 2. Functional schematic▶

9. The video output of the logarithmic i.f. amplifier is fed into the unit where it is amplified, inverted and applied to a low-pass filter circuit. The output of the filter consists of a d.c. potential, the level of which is dependent upon the degree of noise jamming present on the video input. Thus for an increase of noise jamming, a proportional increase of the d.c. output of the filter is obtained, and this output is fed to the adding circuit mentioned previously.

10. In the adding circuit, the positive-going d.c. output of the filter is added to the negative-going swept gain waveform, the effect being to reduce the negative excursion of the waveform. If the d.c. level reaches approximately +28V, any further increase will tend to raise above earth that part of the waveform which is normally at earth potential. The resultant waveform is fed via a cathode follower to an amplifier stage, where it is used as a variable bias potential.

11. The amplifier stage also receives the amplified, unfiltered video signal. The amplitude of the video output produced therefore depends upon the instantaneous bias potential produced by the swept gain waveform. The video signal is fed via a cathode follower to the output socket of the unit, from where it is routed to the comparator, signal (video) M4 via the 16 μsec pulse delay network M1.

Circuit description (*fig.* 7)

Power supplies

12. The 240V a.c. mains supply to the fused primary of the valve heater transformer TR1 is routed via PLB/7 and PLB/10. Power at these points is controlled by the main system switch for all units of the system. The transformer has a centre-tapped 6·3V secondary and this supplies all the valves within the unit.

13. +250V from the +250V regulator in frame 1 is fed into the unit on PLB/9 and PLB/12 (earth), and the −250V supply on PLB/11 and PLB/12 (earth).

14. A 50V relay energizing supply enters the unit on PLB/8, either or both of the two relays in the unit being operated by earthing either PLB/1 or PLB/2, or both. Operation of the appropriate relays is effected from the control desk.

Swept gain function generator

15. The swept gain function waveform (*fig.* 3) is produced by the circuit comprising V1, V2, V3b, V4, V5 and V6. The circuit action is initiated by the positive-going 0 μsec trigger pulse which enters the unit at SKM. This pulse, which has an amplitude of 20V and a duration of 5 μsec, is fed from SKM to the pulse stretching circuit formed by V12, C1 and R1. The effect of this circuit is to increase the duration of the trigger pulse by approximately 10 μsec. The stretched pulse is amplified and inverted by V1, which is normally conducting due to self bias. The negative-going pulse developed at the anode of V8 is limited in amplitude to approximately −32V by the diode V18, which conducts for pulse amplitudes in excess of this level (set by the potential divider R5/R6).

16. The resultant negative-going pulse from V1 anode charges C5 via V2b, and C6 via V2a. At the cessation of the pulse, both halves of V2 and both halves of V4 are cut off. C6 begins to discharge exponentially via R12 and V3b towards earth potential, and at the same time C5 begins to discharge towards h.t. via R9 and R11.

17. During this period the diode V16 is conducting, and at the junction of R23 and R24 a potential of −2·5V exists. This potential is applied to the cathode of V4a and when the potential at the anode of the valve, as determined by the voltage across C6, becomes more positive than the cathode potential, the valve conducts, thereby preventing any further discharge of C6.

18. Simultaneously with the above action, C5 continues its discharge towards h.t., until the potential at the anode of V4b reaches the cathode potential of the valve, as determined by the divider chain R13 and R14, i.e. approximately −2·5V. This occurs approximately 1 msec after the circuit action has been initiated by the 0 μsec pulse. V4b then conducts, and the rising exponential waveform is applied via R16 to the grid of V5b.

19. The negative-going edge produced at the anode of V5b is further amplified by V5a and the resultant positive-going waveform, at an amplitude of approximately +70V, is fed via the cathode follower V6a and capacitor C9 to the cathode of V16, thereby causing the diode to cut off. With V16 cut off, the voltage at the junction of R23 and R24 rises positively to cut off V4a, thus allowing C6 to continue its discharge through R12. However, the discharge is not now aiming at earth potential through V3b, as this diode has been cut off by the positive-going pulse from V6a, this pulse thus setting the new aiming potential. Since the discharge of C6 is now aiming at a much higher potential, the effect is for the capacitor to reach its fully discharged state 500 μsec after the resumption of the discharge, and this portion of the waveform is almost linear, as shown in fig. 3. The circuit then remains in its quiescent state until the arrival of the next trigger pulse.

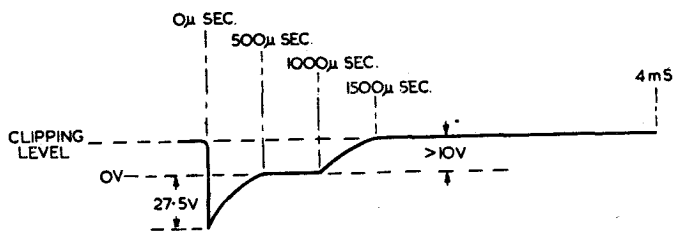


Fig. 3. Swept gain waveform

20. The negative-going waveform produced by the circuit is fed to the grid of the cathode follower V6b. The d.c. level of the waveform developed at the cathode of the valve is adjustable by means of the LEVEL (SKE) potentiometer, RV1, and this control is adjusted to set the level of the centre, horizontal portion of the waveform to 0V. The amplitude of the waveform is adjustable by means of the SLOPE potentiometer, RV6, and the final waveform is fed to the video circuit.

Video circuit

21. The video input to the unit at SKN consists of negative-going video signals at a maximum amplitude of −6V, the signals being derived from the logarithmic i.f. amplifier. Under conditions of noise jamming, the d.c. level of the video input becomes increasingly negative, but the noise fluctuations remain substantially constant. From SKN the video signal is applied to the grid of V7, which, with V8, comprises a d.c. amplifier with the gain limited to approximately 5 by negative feedback taken from the cathode of V8 and applied via R41 to the grid of V7. The LEVEL (SKK) potentiometer, RV2, determines the potential at the grid of V8, and thereby the gain of the circuit.

22. The positive-going signal produced at the cathode of V8 is split into two paths ; the low-pass filter formed by R48 and C12 extracts the d.c. component, while C11 passes the a.c. component, of constant noise amplitude, to the grid of V10b.

23. The positive d.c. component of the signal and the negative-going swept gain waveform are added by R49 and R50, and the resultant, if negative, is passed by the diodes V14 and V15 to the grid of the cathode follower V9. It follows that an increase in the d.c. component, caused by an increase of noise, will allow less of the swept gain waveform to pass through the diode circuit.

24. The output of V9 is developed across the LEVEL (SKK) potentiometer, RV3, and the d.c. level of the waveform is set to zero by means of the control. The resultant waveform is applied to a switched attenuator network formed by R56, R57, R58 and contacts of RLA and RLB. By means of the relays it is possible to select combinations of the three resistors from the control console, thereby providing four levels of amplitude of the waveform, i.e. zero, one-third, two-thirds and full amplitude. After amplitude selection the waveform is fed via the LEVEL potentiometer, RV4, to the grid of V10b, where it is added to the unfiltered video signal (*fig.* 4). Any possible negative excursion of the video signal is prevented by the diode V13.

25. The grid circuit of V10b includes the diode V17, connected between grid and earth in such a way that it conducts on negative inputs. Since the video signal at the grid of V10b is positive-going, it follows that in the absence of any negative potential produced by the swept gain circuit V17 will not conduct, and the full video signal is amplified by V10b and V10a, and passed via the cathode follower V11 to the output socket SKP. However, in operation a proportion of the swept gain voltage will always be present, thereby causing V17 to conduct and clip the base of the video signal, the degree of clipping being dependent upon the instantaneous swept gain voltage.

26. Under conditions of noise jamming, the swept gain waveform becomes progressively less negative as the noise increases. Consequently, less of the video signal is clipped.

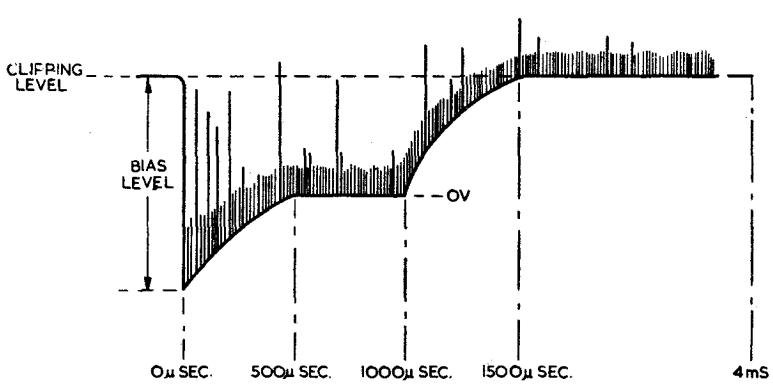


Fig. 4. Swept gain waveform with video signals

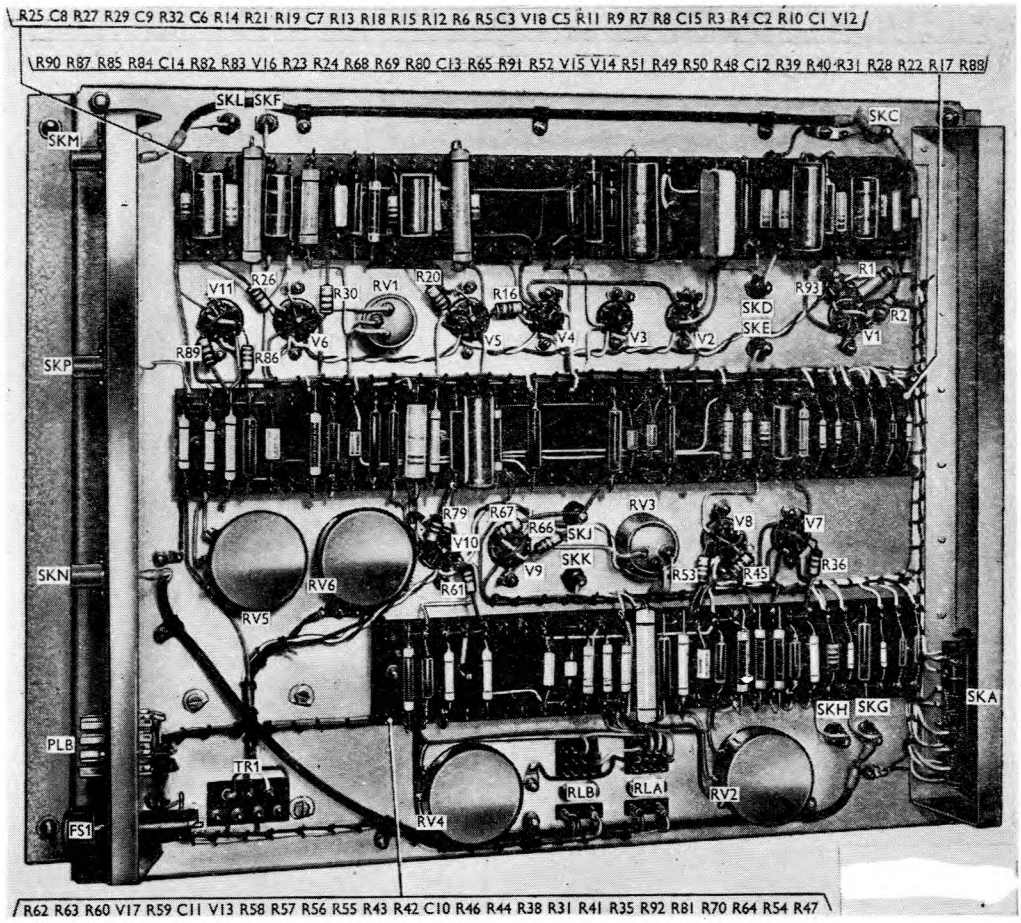


Fig. 5. Generator sweep (video) M3 : rear view

27. The d.c. level of the video signal appearing at the cathode of V11 is adjustable by means of the LEVEL (SKL) potentiometer, RV5, this control being adjusted to give a d.c. level of zero at SKP. From SKP the video signal is routed to the pulse delay network M1.

Monitoring points

28. Monitor test points are provided at sockets SKC to SKL. The waveforms obtainable at these points are illustrated in fig. 6.

Multimeter readings

29. In addition to the monitoring points detailed above, the performance of all valves within the unit, with the exception of V2, V3 and V4, may be checked by connecting a multimeter Type 100 to SKA via a plug-to-socket adapter. The readings obtained should be as given in Table 1.

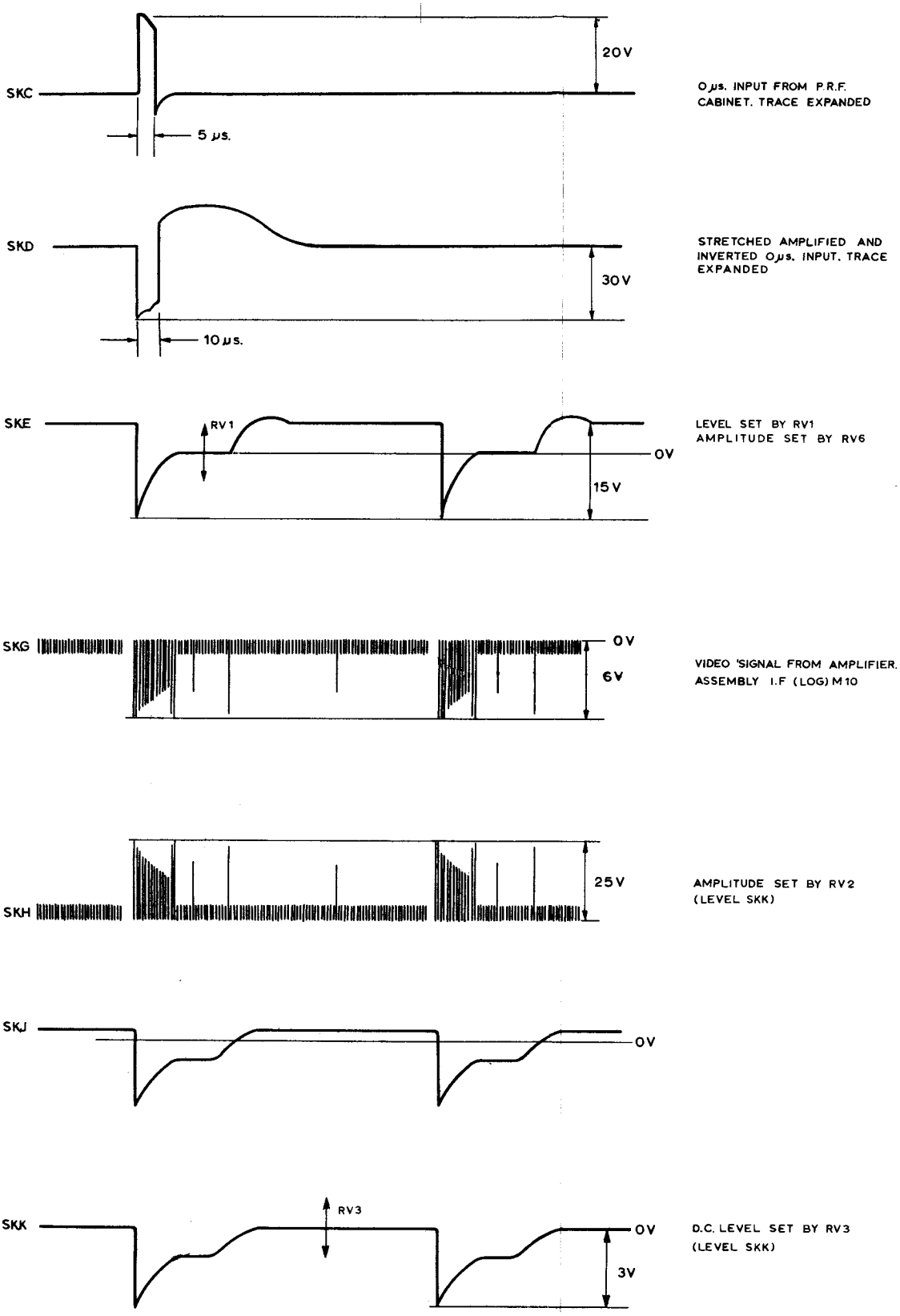
TABLE 1

Multimeter readings

Multimeter switch position	Stage checked	Measured across	Reading	Tolerance
A	V11	R88	0·44	±0·09
B	V5b	R18	0·50	±0·1
C	V5a	R21	0·57	±0·11
D	V6a	R28	0·53	±0·11
E	V6b	R31	0·41	±0·08
F	V7	R40	0·53	±0·11
G	V8	R47	0·46	±0·09
H	V9	R54	0·43	±0·09
J	V10b	R64	0·48	±0·10
K	—	—	ZERO	—
L	V10a	R81	0·46	±0·09
M	V1	R92	0·44	±0·09

Note . . .

Readings are taken with RV1, RV3, RV4, RV5 and RV6 set fully counter-clockwise, and RV2 fully clockwise.



Wt.9110. R.C.1646

Fig. 6 Monitor point waveforms

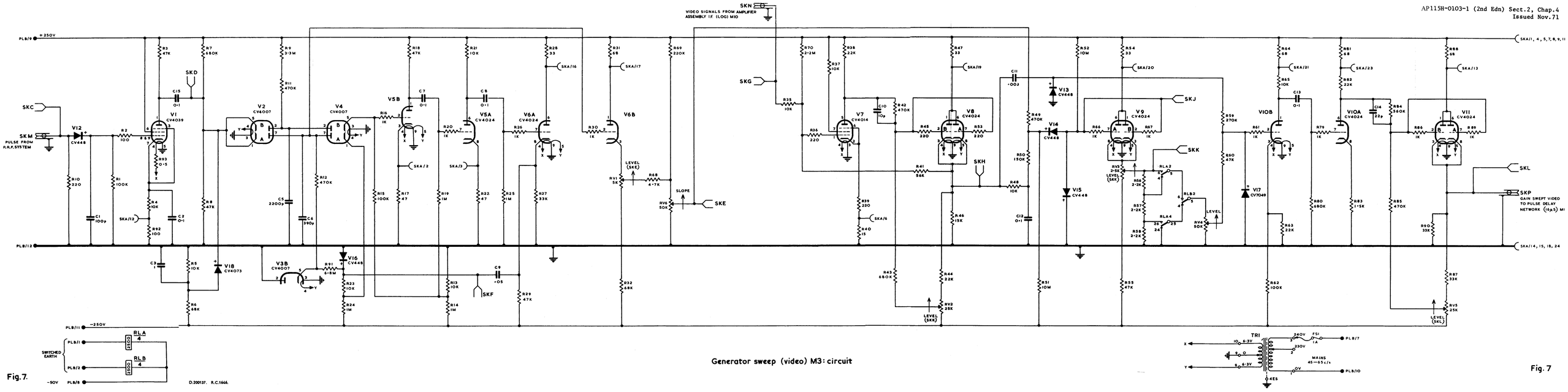


Fig.7.

Generator sweep (video) M3: circuit

D.200137. R.C.1666.

Fig. 7

Chapter 5

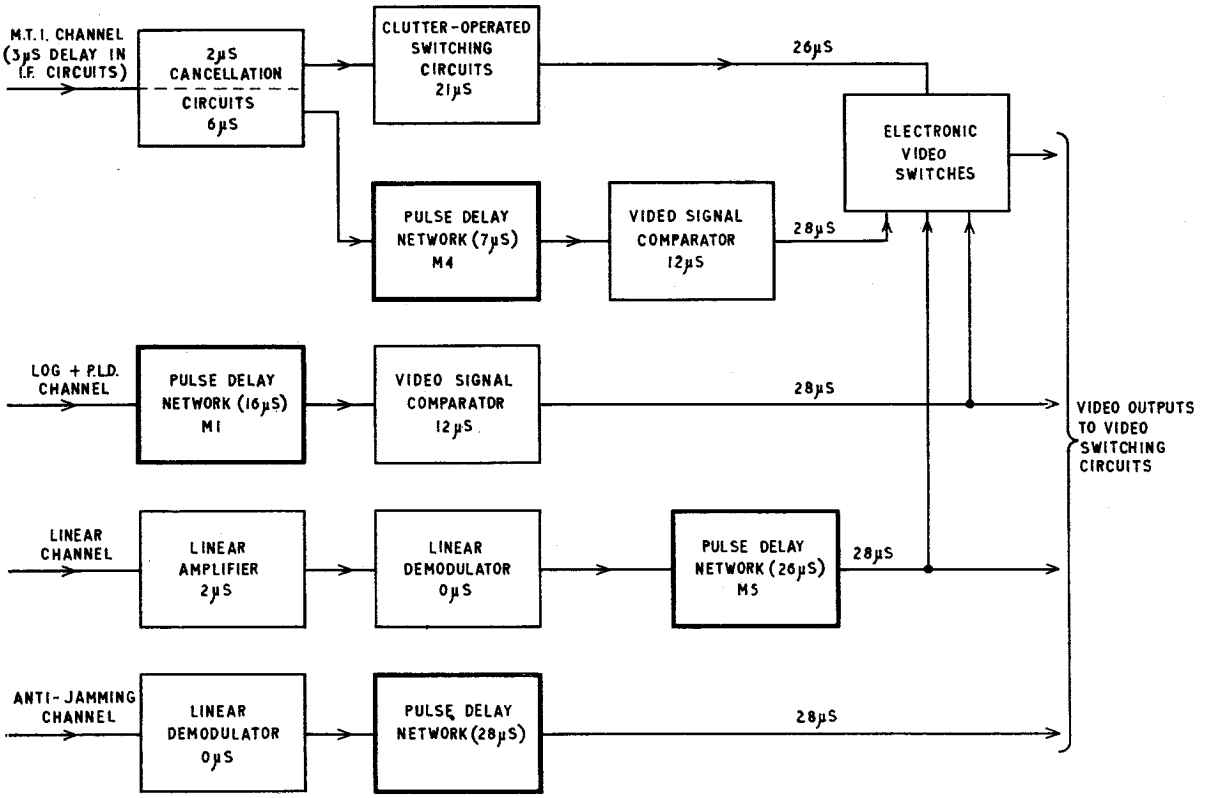
PULSE DELAY NETWORKS

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

Introduction

1. Four pulse delay networks of different delay times are used in the Type 84 radar signal processing system, their purpose being to compensate for the delays introduced by the clutter-operated switching circuits and in the M.T.I. channels. A schematic diagram, showing the application of the delay networks, is given in fig. 1.



(C39642)

Fig. 1. Pulse delay networks : application

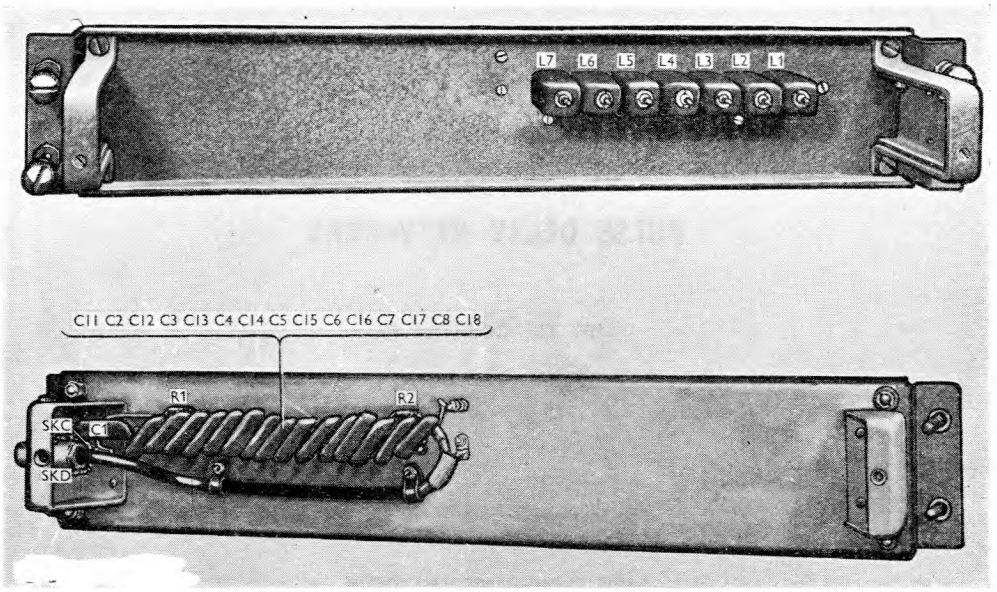


Fig. 2. Pulse delay network (7μs) M4 : front and rear views

2. In the M.T.I. channel, the clutter switching waveform, when applied to the video switching circuit, has been delayed by a total of 26 microseconds. In order to ensure that the waveform arrives at the video switch before the radar signals, artificial delays are introduced in the signal channels, so that the signals are delayed by a total of 28 microseconds.

3. Since signals in the anti-jamming channel do not pass via the video switches, these signals must also be delayed by such a time as to ensure that signals from all four channels arrive at the displays simultaneously.

4. The four delay networks used in the signal processing system are as follows :—

(1) Pulse delay network (7μs) M4 (*fig.* 2). This unit is located in frame 1 of the video cabinet and introduces a 7-microsecond delay in the M.T.I. channel.

(2) The pulse delay network (16μs) M1 (*fig.* 3) is located in frame 2 of the i.f. cabinet and forms part of the log +P.L.D. channel.

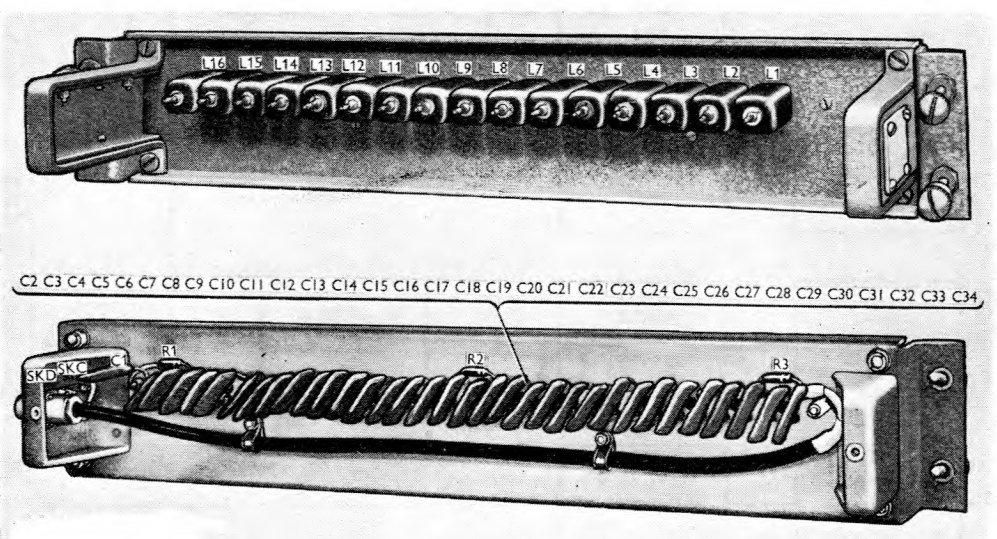


Fig. 3. Pulse delay network (16μs) M1 : front and rear views

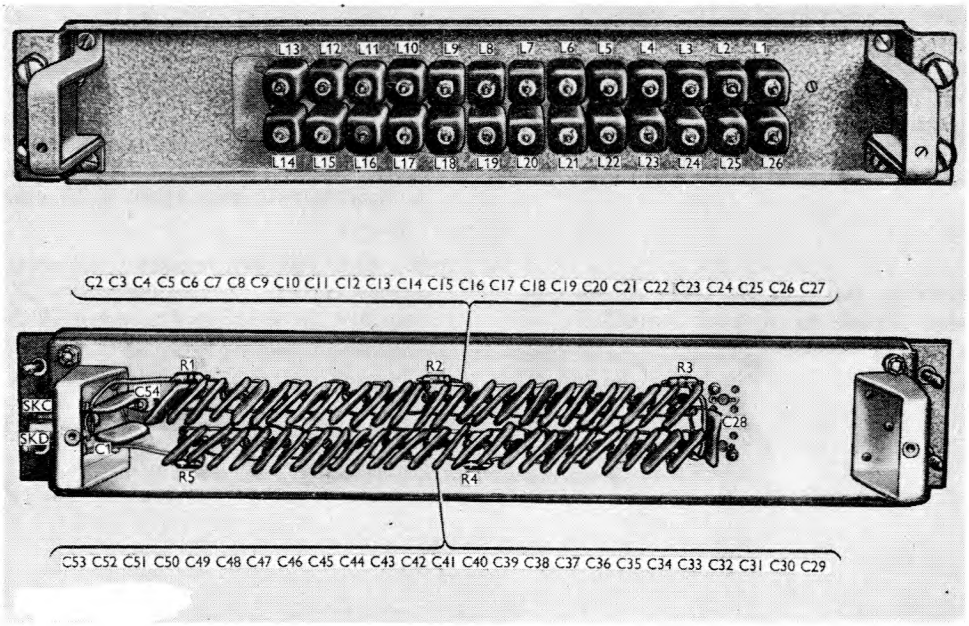


Fig. 4. Pulse delay network (26μs) M5 : front and rear views

(3) Pulse delay network (26μs) M5 (*fig.* 4) is located in frame 3 of the video cabinet and forms part of the linear channel.

(4) Pulse delay network (28μs) (*fig.* 5). This unit, which forms part of the anti-jamming channel, is located in frame 1 of the i.f. cabinet.

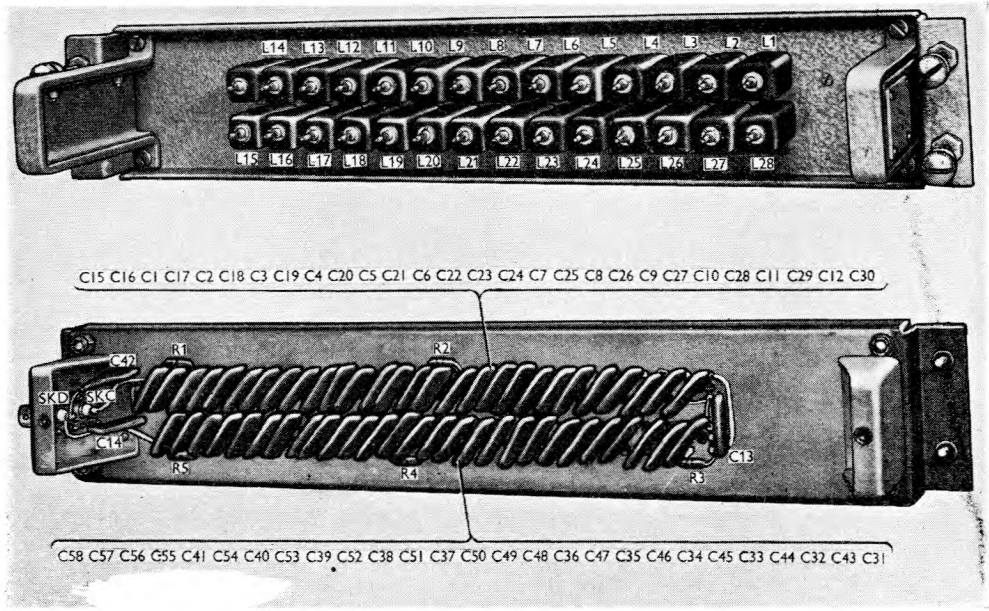


Fig. 5. Pulse delay network (28μs) : front and rear views

Performance characteristics

5. The four pulse delay networks all have similar characteristics, the only significant difference being their respective delay times. The following information therefore applies to all of the units.

Input

6. The input to SKC consists of unipolar video signals at a peak amplitude such that the output is 1·5V ±0·1V. The pulse length varies depending on the nature of the signal passing through the system.

Output

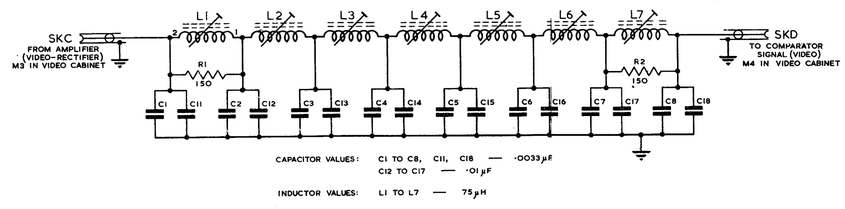
7. The output of the unit at SKD consists of unipolar video signals at a peak amplitude of 1·5V ±0·1V, but delayed with respect to the input by a time dependent on the individual delay characteristics of the networks. The characteristic impedance of all of the networks is 75 ohms.

Circuit description

8. The circuit diagrams of the four delay networks are given in fig. 6. Each network is made up of conventional π-section filters in cascade, each section having a delay time of 1 microsecond and a characteristic impedance of 75 ohms.

9. The 150-ohm resistors connected in parallel across certain of the inductors are included to improve the frequency response of the networks.

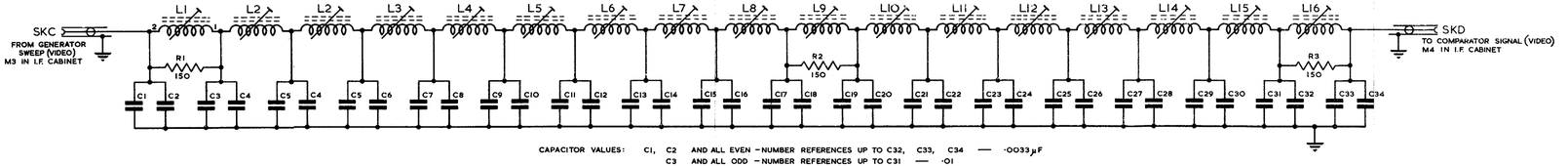
NETWORK PULSE DELAY M4 (7μS)



CAPACITOR VALUES: C1 TO C8, C11, C18 — ·0033μF
C12 TO C17 — ·01μF

INDUCTOR VALUES: L1 TO L7 — 75μH

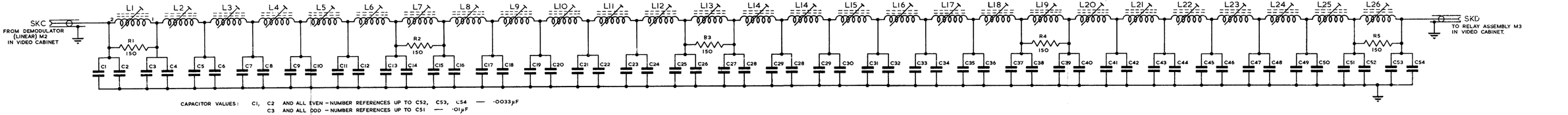
NETWORK PULSE DELAY M1 (16μS)



CAPACITOR VALUES: C1, C2 AND ALL EVEN – NUMBER REFERENCES UP TO C32, C33, C34 — ·0033μF
C3 AND ALL ODD – NUMBER REFERENCES UP TO C31 — ·01

INDUCTOR VALUES: L1 TO L16 — 75μH

NETWORK PULSE DELAY M5 (DELAY M5 (26μS)



CAPACITOR VALUES: C1, C2 AND ALL EVEN – NUMBER REFERENCES UP TO C52, C53, C54 — ·0033μF
C3 AND ALL ODD – NUMBER REFERENCES UP TO C51 — ·01μF

INDUCTOR VALUES: L1 TO L26 — 75μH

NETWORK PULSE DELAY (DELAY (28 μS)

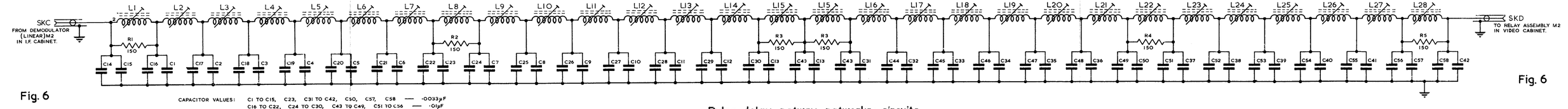


Fig. 6

CAPACITOR VALUES: C1 TO C15, C23, C31 TO C42, C50, C57, C58 — ·0033μF
C16 TO C22, C24 TO C30, C43 TO C49, C51 TO C56 — ·01μF

INDUCTOR VALUES: L1 TO L28 — 75μH

Pulse delay netway networks: circuits

Fig. 6

Chapter 6

COMPARATOR, SIGNAL (VIDEO) M4

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

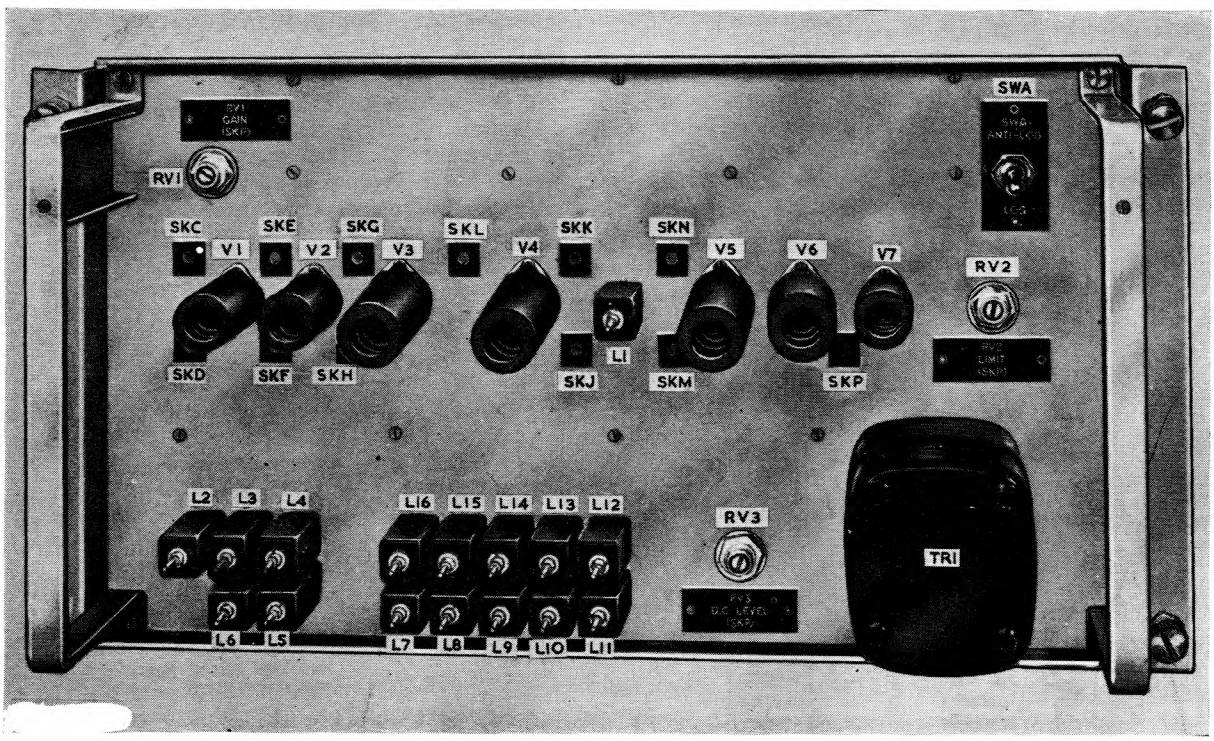


Fig. 1. Comparator, signal (video) M4: front view

Introduction

1. The signal comparator (video) M4 (*fig.* 1 *and* 6) is used in two applications. In the first application the unit forms part of the MTI channel, where it follows the cancellation circuits and is used to reduce the d.c. level resultant from c.w. jamming: at this stage all other forms of jamming and clutter, with the exception of impulsive jamming and c.w. jamming, have been eliminated. In the second application the unit follows the 16 microseconds pulse delay network in the logarithmic channel, where its function is to remove clutter. The operation of the unit is identical in both applications.

2. Unwanted clutter is reduced by the rejection of video signal pulses whose duration is greater than twice the 10 microseconds transmitted pulse length (i.e. signals with a duration greater than 20 microseconds) and attenuating the length of pulses whose duration is between 10 and 20 microseconds. The technique used, which is known as pulse length discrimination, is to compare in a coincidence gate the duration of received pulses against the delay time of a 10 microseconds delay line.

3. The signal comparator unit in the MTI channel is fitted in frame 1 of the video cabinet and that in the logarithmic channel in frame 2 of the i.f. cabinet.

Performance characteristics

Input

4. Socket SKQ accepts unipolar video signals of between 1V and 2V peak amplitude. In the i.f. cabinet application of the unit the input is derived from the amplifier i.f. (log.) M4 (*Chap.* 3) via the pulse delay network M1 (*Chap.* 5), and in the video cabinet application a linear input is derived from the pulse delay network M4 (*Chap.* 5). The source impedance in both cases is 75 ohms.

5. A parallel connection to SKQ is provided at SKR and in the video cabinet application the input signal is re-routed via SKR to the relay assembly M2 (*Sect.* 5, *Chap.* 6). In the i.f. cabinet application, SKR is terminated by a 75-ohm terminating connector.

Output

6. The pulse length discriminated video output leaves the unit at parallel-connected sockets SKS and SKT. In the i.f. cabinet application of the unit, the output at socket SKS is fed to relay assembly M3 (*Sect.* 5, *Chap.* 9) in the video cabinet. In the video cabinet application, the output at socket SKS is fed to the electronic switch (video) M3. In both applications, socket SKT is unused. The peak amplitude of the output signals is limited to between 1V and 1·5V, and the output impedance is 75 ohms.

Brief circuit description

7. The following description should be read in conjunction with the block diagram (*fig.* 2) and the idealized waveforms shown in fig. 3.

8. The input to the unit at SKQ consists of video pulses comprising target returns, jamming and clutter signals. Since most clutter signals and some jamming signals have a pulse duration considerably longer than the target returns, it follows that under severe clutter conditions targets would be obscured.

9. The transmitted pulse length is 10 microseconds and therefore returns from targets will have the same duration. Clutter returns and c.w. jamming signals have a duration considerably greater than that for target signals and are suppressed for durations greater than 20 microseconds, or attenuated for durations between 10 and 20 microseconds; target signals are unaffected. This is achieved by the method of pulse length discrimination described below.

10. The video signals (*fig.* 3(*a*)) are applied to the input of a negative feedback amplifier, and simultaneously to a 5-microseconds delay line which is terminated in a short-circuit. This method of termination causes phase reversal and complete reflection of the applied signal (*fig.* 3(*b*)), with the result that the input to the amplifier is a composite waveform (*fig.* 3(*c*)) consisting of a positive pulse and a negative pulse, both of 10 microseconds duration. The time relationship of the two pulses is dependent upon the length of the applied pulse, so that for an input pulse of 10 microseconds duration the trailing edge of the input pulse and the

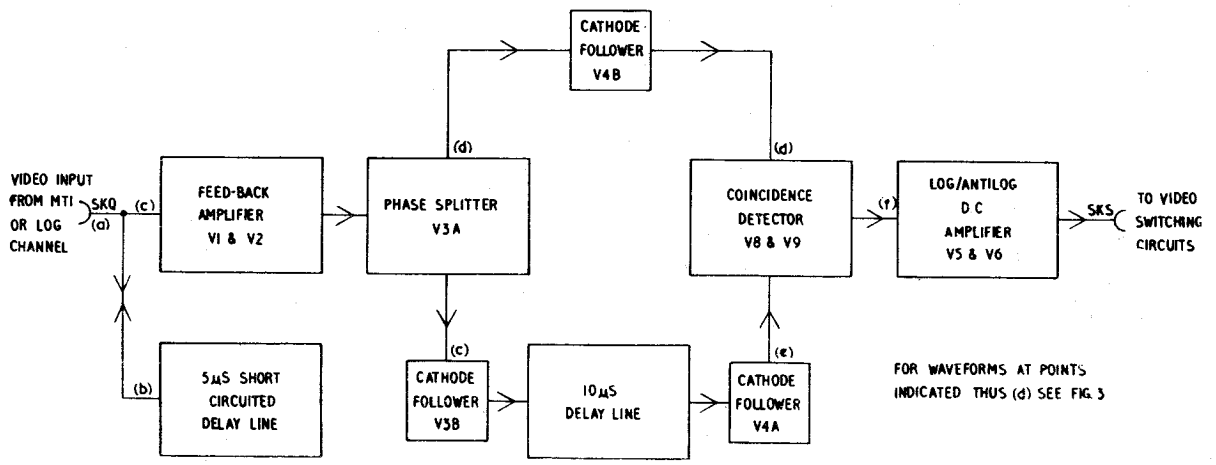


Fig. 2. Comparator, signal (video) M4: block diagram

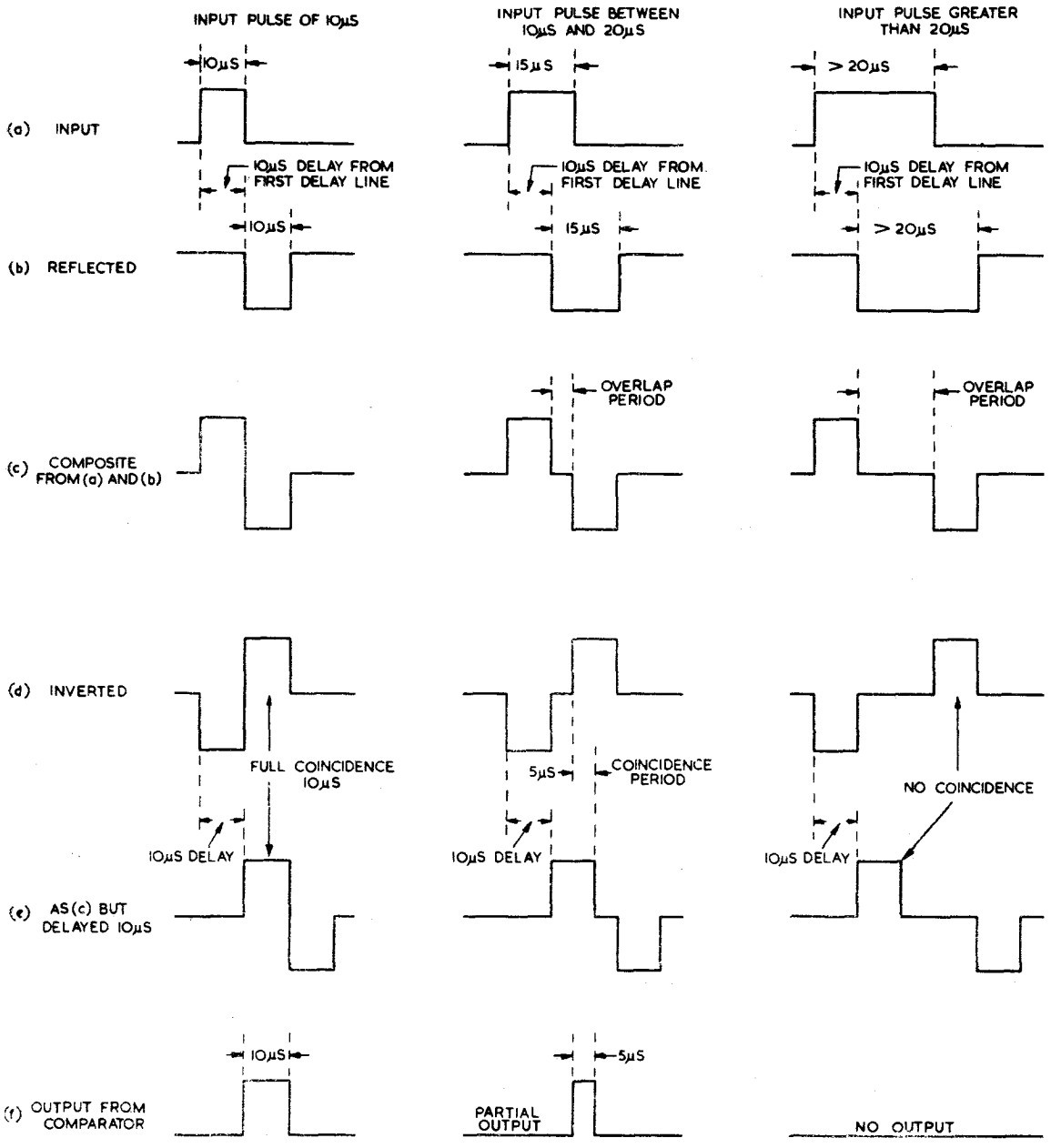


Fig. 3. Pulse length discrimination : explanatory waveforms

leading edge of the delayed-reflected pulse, which form the composite waveform, are coincident. With input pulses of duration greater than 10 microseconds a degree of separation occurs between the pulses, the duration of the separation being determined by the anti-phase cancellation caused by the time overlap between the input and reflected pulses. It follows that for input pulses of durations greater than 10 microseconds, the separation duration of the composite waveform will be the input duration minus 10 microseconds.

11. The composite waveform is amplified by V1 and V2 and applied to a phase splitter, V3a, which produces the anti-phase outputs shown in fig. 3(*c*) and 3(*d*). The output from the cathode of the phase splitter is passed through a 10-microseconds delay line (*fig.* 3(*e*)) and both phase-split waveforms are applied to a coincidence detector, V8 and V9. If the video input pulse to the unit is of 10 microseconds duration, the positive-going portions of the compared waveforms will be in full coincidence and the detector circuit produces an output pulse of maximum duration (*fig.* 3(*f*)). For input pulses of between 10 microseconds and 20 microseconds duration, the waveforms are in partial coincidence (*fig.* 3) and the detector produces an output pulse of correspondingly reduced length. If the input duration exceeds 20 microseconds the positive-going portions of the compared waveforms do not coincide (*fig.* 3) and no output pulse is produced.

12. Output pulses produced by the coincidence detector are applied to a high stability d.c. amplifier, V5 and V6, the feedback characteristic, and therefore gain, of which can be altered so that the output follows either a logarithmic or a linear law.

Circuit description (*fig.* 8)

Power supplies

13. The power supplies required by the unit are fed in at PLB. The +250V supply is applied between PLB/9 and PLB/12 (earth), and the −250V supply between PLB/11 and PLB/12 (earth). The 6·3V a.c. valve heater supply is produced within the unit by the mains transformer TR1, the 240V input at 45–65 c/s being routed via PLB/7 and PLB/10, and fused by FS1.

Comparison waveform generator

14. The output of a pulse delay network, consisting of unipolar video pulses, is applied to the input of the video signal comparator at SKQ. From SKQ the signal is fed to the grid of V1 via the GAIN (SKP) potentiometer, RV1. The signal at the slider of RV1 is also applied to a 5-microseconds delay line, formed by L2 to L6, C11 to C15, and terminated in a short-circuit which causes complete reflection and phase reversal of the applied pulse. Consequently the reflected pulse appearing at V1 grid is inverted, and delayed by 10 microseconds on the original pulse. Should the original input pulse duration be more than 10 microseconds, the original and the reflected pulses will overlap, during this period the pulses cancel each other and the resultant will be zero, producing the composite waveform shown in fig. 3(*c*).

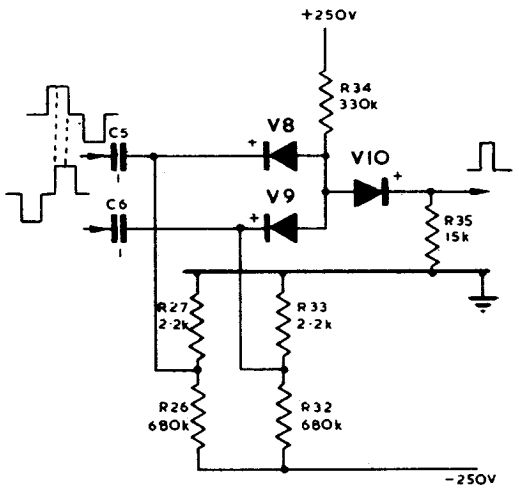


Fig. 4. Coincidence detector : simplified circuit

15. Pentodes V1 and V2 comprise a negative feedback amplifier, the feedback path being formed by R11. The output of the amplifier is fed via C2 to the grid of a phase splitter, V3a, which produces anti-phase versions of the composite waveform at its anode and cathode.

16. The anode waveform of V3a is fed, via C3 and cathode follower V4b, to diode V9, which forms part of a coincidence detector circuit, whilst the waveform produced at the cathode of V3a is fed via cathode follower V3b to the input of a 10-microseconds delay line formed by L7 to L16 and C16 to C26. Resistors R60, R61 and R62 are

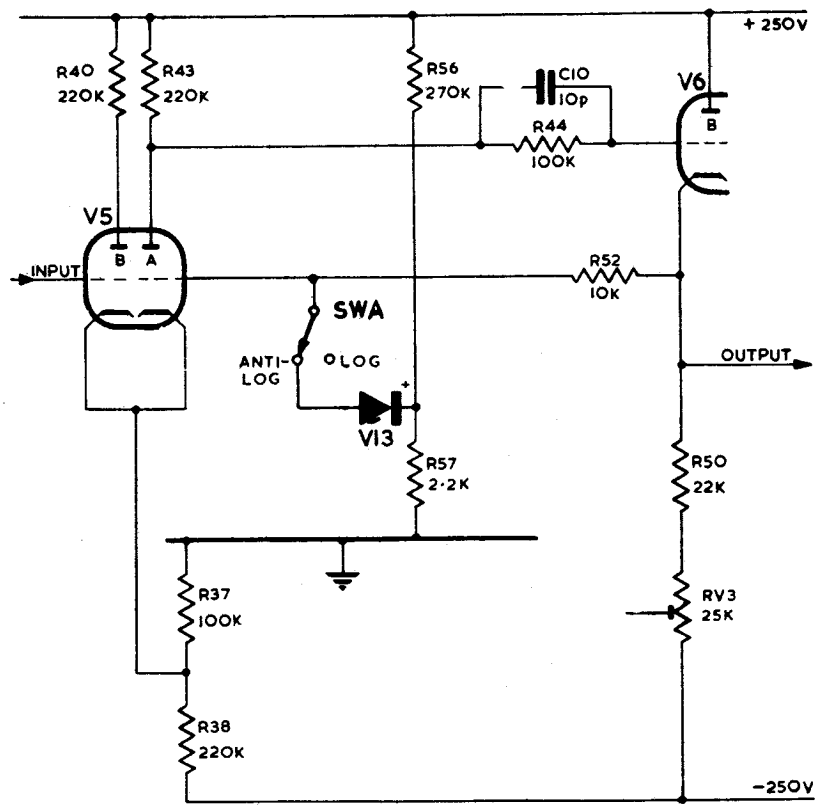


Fig. 5. Log/anti-log d.c. amplifier : simplified circuit

included in the delay line to improve the response characteristic of the line. The delayed output of the line is applied, via cathode follower V4a, to V8 which is the second diode of the coincidence detector.

Coincidence detector

17. ◄ A simplified circuit of the coincidence detector is shown in fig.4. Diodes V8 and V9 are normally conducting due to the resistor chains R34, R26, R27 and R34, R32, R33 respectively, so that the common anodes of the diodes are at a low positive potential with respect to earth. Diode V10 is therefore passing a very low current, as its cathode is returned to earth. When positive pulses, or portions thereof, are in coincidence at the cathodes of V8 and V9, the diodes cut-off and the anode of V10 goes more positive. The current in V10 increases producing a single positive pulse across R35. ►

18. A condition whereby a positive pulse is applied to either V8 or V9 only (input pulse longer than 20 microseconds) will not produce an output from the circuit, since with only one of the two diodes cut off the potential at their anodes will not rise to a value sufficient to cause V10 to conduct.

19. The diode V11 (fig.8) positively restores the d.c. level of the output from the coincidence circuit to earth potential prior to its application to the succeeding stage, via the filter circuit formed by L1, C7 and C8. This filter has a 240 kc/s cut-off characteristic, and reduces short-duration noise spikes to a common amplitude. The filter can be by-passed, for certain applications, by changing the input and output connections.

Log/anti-log d.c. amplifier

20. A simplified circuit of the log/anti-log d.c. amplifier is given in fig.5. Pulses produced by the coincidence detector are applied to the grid of V5b, which, in conjunction with V5a and V6, forms a high stability, low gain d.c. amplifier. Negative feedback is incorporated in the amplifier by returning the cathode of the output stage, V6, to the grid of V5a via R52. The feedback ratio, and therefore gain characteristic, can be selected by the position of the LOG/ANTI-LOG switch, SWA. When the switch is set to the LOG position, the feedback ratio is a fixed amount and the gain of the amplifier is kept at a minimum. The overall response of the amplifier with the switch in the LOG position is therefore linear.

21. With SWA set to the ANTI-LOG position the feedback ratio is variable and is determined by the pulse amplitude. Control of the feedback ratio is effected by the circuit comprising the diode V13, the anode of which is connected through SWA to the feedback path. The cathode of V13 is returned to a potential of +2·1V at the junction of R56 and R57. With a feedback amplitude of less than 2·1V the diode is cut off, so that the full negative feedback voltage is applied to the grid of V5a. When the feedback amplitude is greater than 2·1V, V13 conducts, and R57 is shunted between the feedback path and earth, reducing the feedback voltage and thereby increasing the gain of the amplifier. The overall characteristic of the amplifier then approximates to a logarithmic law.

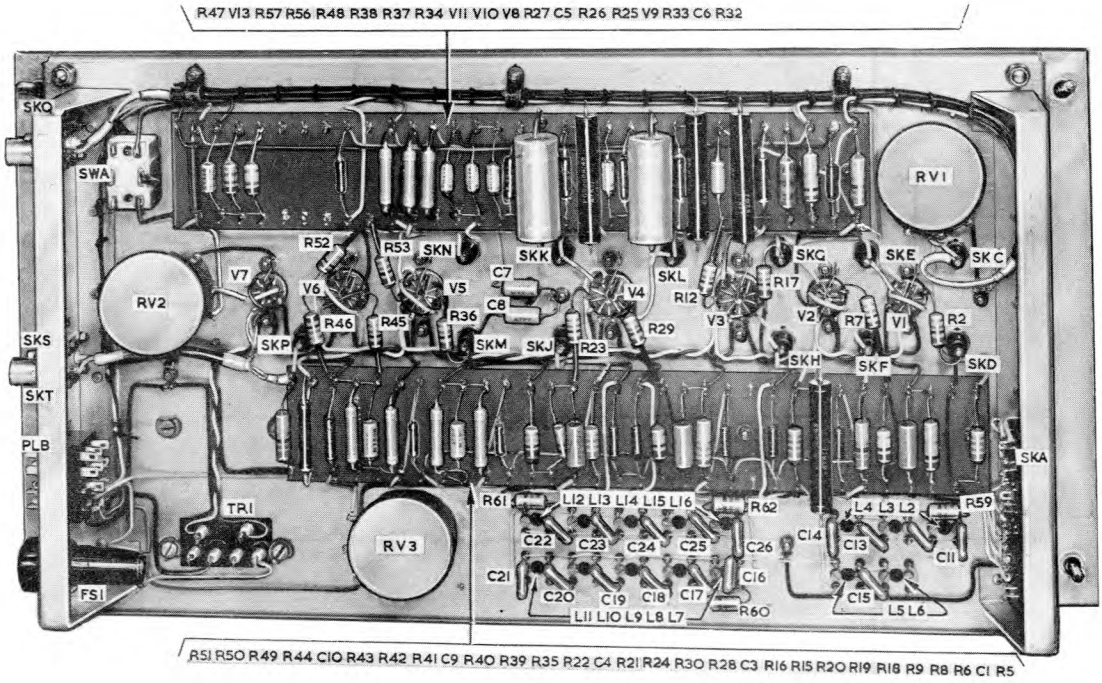


Fig. 6. Comparator, signal (video) M4: rear view

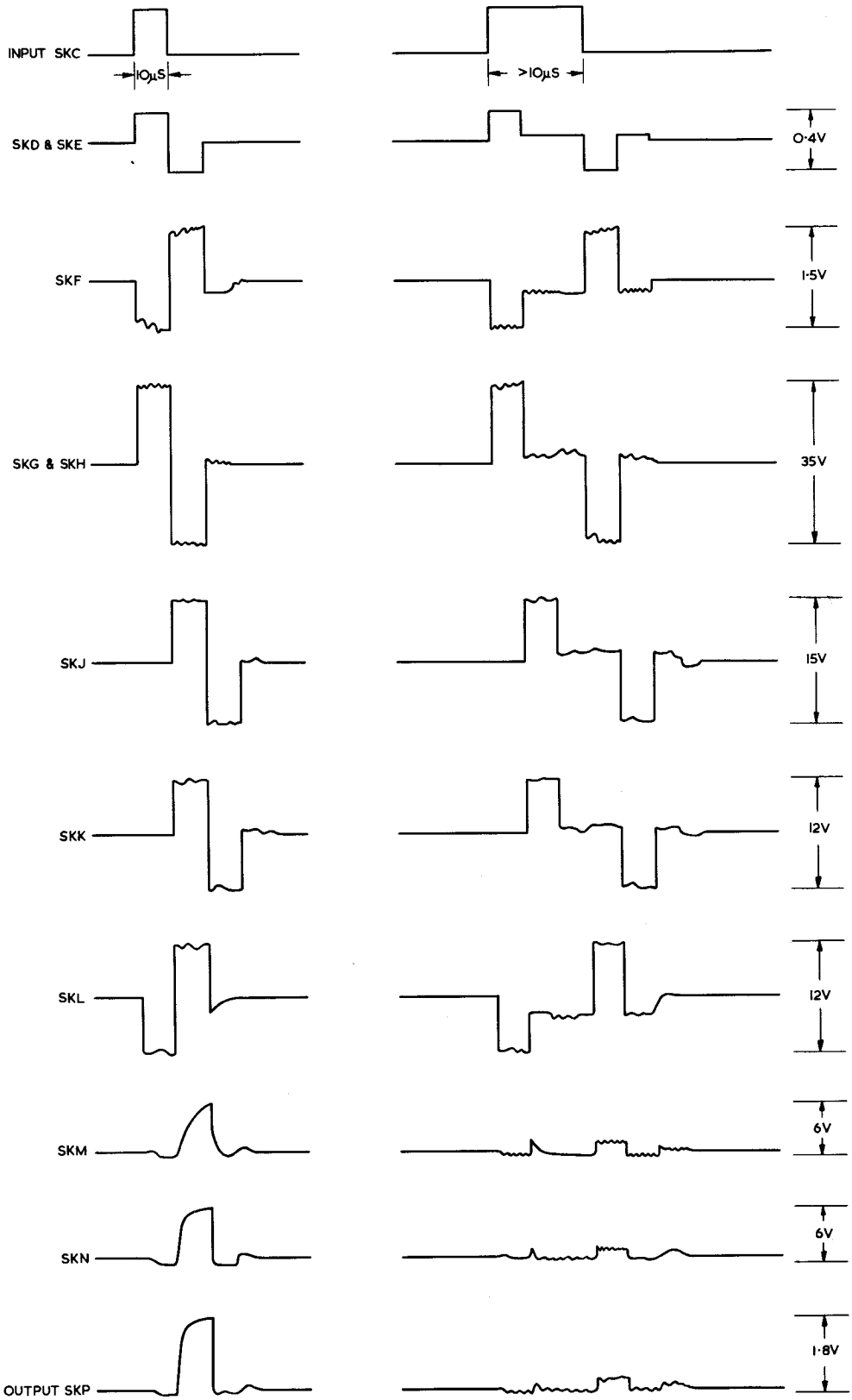


Fig. 7. Monitor point waveforms

22. The amplitude of the output pulse at SKS and SKT (monitored at SKP) is limited to 1·8V by the diode V7 (*fig.* 8), the limiting level being set by the LIMIT (SKP) control, RV2. The d.c. level of the output pulse is set to zero by the D.C. LEVEL (SKP) control, RV3.

23. In the i.f. cabinet application of the unit, the LOG/ANTI-LOG switch is normally in the ANTI-LOG position as the input pulses have previously passed through the i.f. log amplifier. In the video cabinet application, the input has been linearly amplified and the switch is set to the LOG position.

Monitor points

24. Test sockets SKC to SKP are provided for monitoring purposes. Using the monitoring oscilloscope M1 (*Sect.* 7, *Chap.* 4) the waveforms under normal operating conditions obtainable at these points are illustrated in fig. 7.

Multimeter readings

25. With the multimeter Type 100 connected to socket SKA via the plug-to-socket adaptor, the readings obtained under normal operating conditions should agree with those listed in Table 1.

TABLE 1

Multimeter readings

Multimeter switch position	Stage monitored	Measured across	Reading	Tolerance
A	V1	R4	0·64	±0·13
B	V2	R9	0·58	±0·12
C	V3a	R15	0·58	±0·12
D	V3b	R20	0·47	±0·09
E	V4a	R24	0·55	±0·11
F	V4b	R30	0·57	±0·11
G	V5b	R39	0·52	±0·10
H	V5a	R42	0·50	±0·11
J	V6	R48	0·52	±0·11

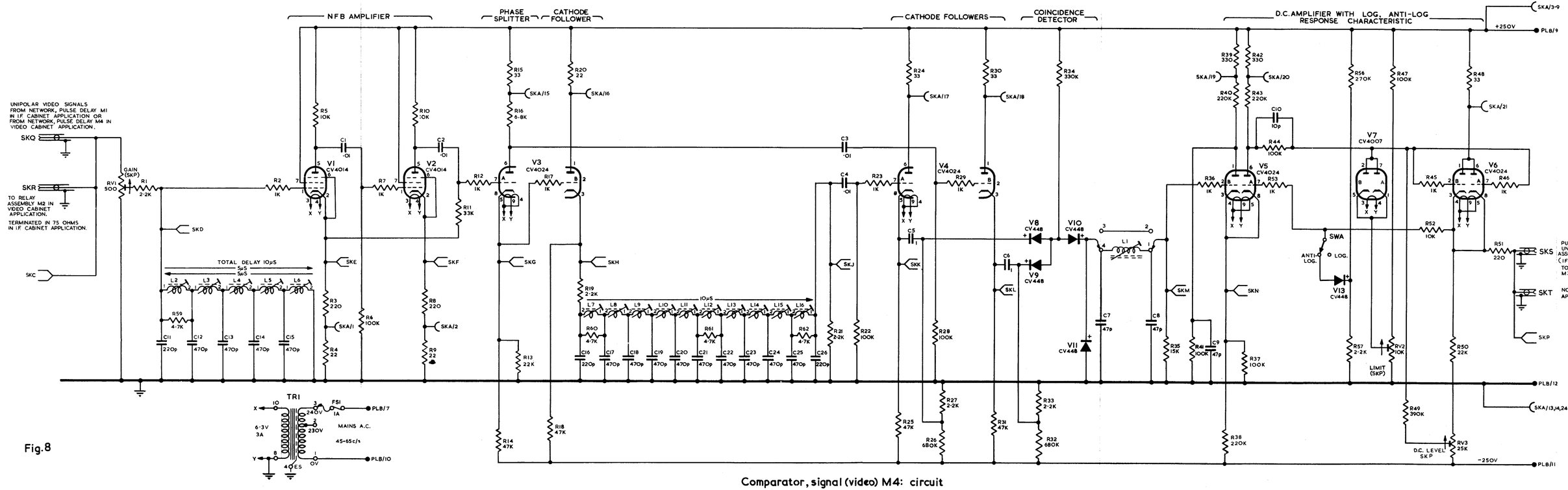


Fig.8

Comparator, signal (video) M4: circuit

Fig.8

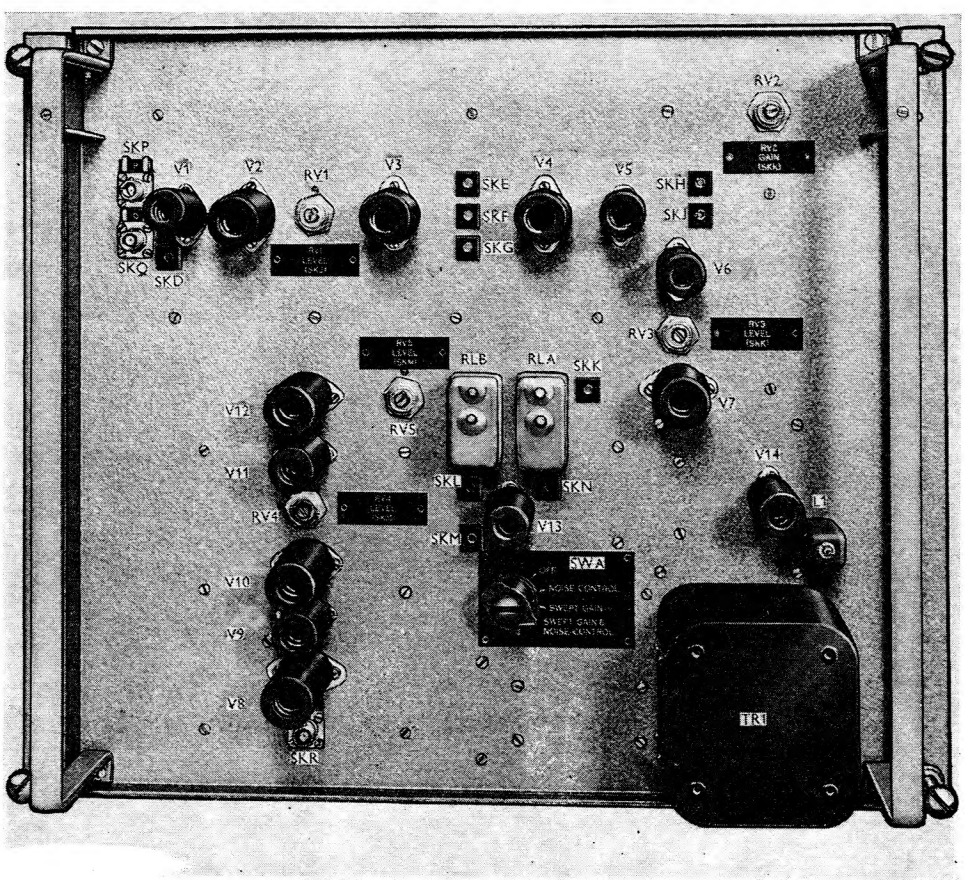
Chapter 7

LIMITER ELECTRICAL NOISE M1

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS



(C37836)

Fig. 1. Limiter, electrical noise M1: front view

Introduction

1. The electrical noise limiter (*fig.* 1 *and* 5), mounted in frame 1 of the i.f. cabinet, provides facilities for suppressing excessive noise and/or angels.

2. The unit consists basically of a single stage i.f. amplifier, the gain of which may be controlled by one, or the greater of both, of two internally-generated voltages. The unit, which is part of the MTI channel, receives either linear or anti-jamming i.f. signals (as selected by the electronic switch (i.f.) unit M2 (*Chap.* 2)) which are amplified and fed to the i.f. amplifier (i.a.g.c.) M2 (*Chap.* 8). Should excessive noise or angels be present on the display, the i.f. signal may be processed by modifying the gain of the i.f. amplifier by application of control voltages. These voltages are:—

(1) A voltage dependent upon the rate of occurrence of noise peaks at the output of the coherent demodulator unit M1 (*Chap.* 10).

(2) A swept gain voltage which follows a law derived from the aerial polar diagram, and is such that the effects of angels are minimized.

Performance characteristics

3. When operating in the fixed gain condition the unit has a nominal gain of unity. The output impedance under all gain control conditions is 75 ohms.

4. When the gain of the amplifier is controlled by the noise, an increase of 50dB in the noise level of the i.f. input to the unit results in an increase of less than 3dB in the noise level at the output of the coherent demodulator unit.

Inputs (*fig.* 7)

5. Socket SKS accepts i.f. signals at a nominal frequency of 13·5 Mc/s as selected by the electronic switch (i.f.) unit. When linear signals are selected the input noise level is 50 microvolts r.m.s. into 75 ohms impedance, and is 4mV r.m.s. into 75 ohms impedance when anti-jamming signals are selected.

6. Socket SKP accepts bipolar video signals derived from the coherent demodulator at a level of 3V peak-to-peak. The parallel input socket SKQ is not used during normal operation.

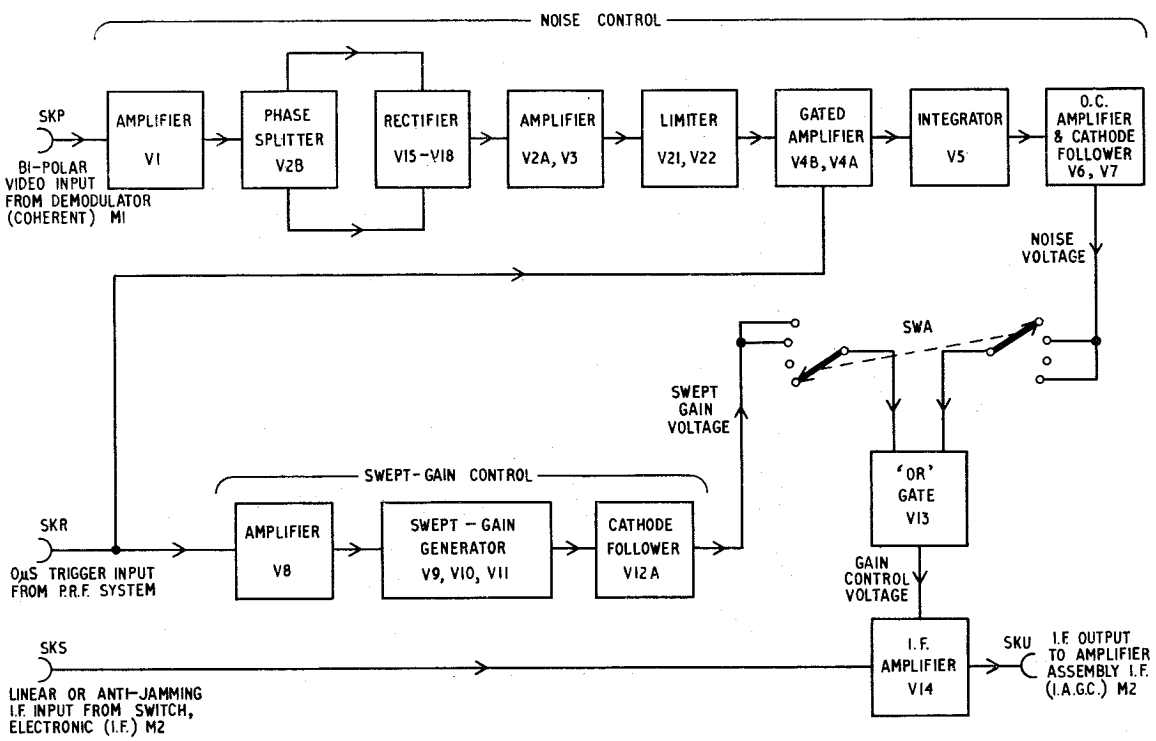
◀**7.** Socket SKR accepts a positive-going 0-microseconds pulse from the p.r.f. system. The pulse duration is nominally 4 microseconds, at a p.r.f. of 250 p.p.s., while the amplitude is not less than 15V.▶

Output (*fig.* 7)

8. The i.f. output of the unit at socket SKU is at approximately the same level as the input to socket SKS, when the unit is operating in the fixed-gain condition. When either of the two gain control functions is selected, the output level at SKU will never represent a gain of greater than unity. The parallel output socket SKV is not used during normal operation.

Brief circuit description

9. The unit comprises a variable-mu i.f. amplifier stage, with two associated circuits for developing noise and swept gain control voltages, as shown in the block diagram (*fig.* 2). Switch SWA enables the two control voltages to be applied to an OR gate, which then passes the greater of the two into



◀**Fig. 2. Limiter, electrical noise M1: block diagram**▶

the gain control circuit of the i.f. amplifier. Alternatively, the switch enables either or both of the voltages to be switched off.

10. To obtain the noise control voltage, a bipolar video output from the coherent demodulator unit is first amplified and then phase-split and applied to a bridge rectifier circuit. The rectified signals are amplified and passed through a limiter circuit, which allows only those signals which fall between predetermined upper and lower amplitude limits to pass to the integrator circuit. The effect of the limiter is to ensure that the voltage produced by the integrator is not a function of the amplitude of the noise pulses, but is dependent only upon the frequency of occurrence.

11. Before integration the noise pulses pass through an amplifier which is gated by the 0 microseconds pulse derived from the p.r.f. system. This pulse renders the amplifier inoperative for the initial part of each radar sweep, so that only signals free from clutter and permanent echoes are passed to the integrator.

12. The integrator circuit produces an output voltage, the level of which is dependent upon the rate of occurrence of noise peaks and is independent of their amplitude. This output is passed through a d.c. amplifier and cathode follower, and applied via switch SWA to the OR gate.

13. The swept gain control voltage is produced by a circuit which is triggered by the 0 microseconds pulse. This pulse is amplified and used to charge a capacitor, the exponential discharge of which is interrupted by a diode switching circuit. The result is a waveform which is exponential for approximately the first 500 microseconds, shows no change for the next 500 microseconds and continues exponentially for the final 500 microseconds. This waveform is fed via a cathode follower to a relay-controlled attenuator circuit, which allows the amplitude of the waveform to be selected from the control console (*Sect.* 8, *Chap.* 2). After attenuation the waveform is applied via switch SWA to the OR gate.

14. Switch SWA enables either or both of the gain control functions to be selected, and when both noise and swept gain control voltages are selected, the OR gate passes the greater of the two to the control circuit of the i.f. amplifier. With the switch in this position or in the swept gain only position, full control of the swept gain function is available at the console by means of relay switching, which enables the swept gain to be selected at one of three levels of attenuation, or switched off. As the noise control functions only when excessive noise is present, it follows that when the swept gain is switched off and no excessive noise is present the i.f. signals are unprocessed by this unit ; with unprocessed signals the i.f. amplifier has a nominal gain of unity.

15. The input to the i.f. amplifier stage consists of linear or anti-jamming i.f. signals, as selected by the electronic switch (i.f.) unit, and the output is routed to the amplifier assembly, i.f. (i.a.g.c.).

Circuit description (*fig.* 7)

Power supplies

16. The power supplies required by the unit are brought in via PLB, the +250V supply entering on PLB/9 and PLB/12 (earth), and the −250V supply on PLB/11 and PLB/12 (earth). The supplies required by the majority of the circuit are wired directly from these pins, but the supplies for the i.f. amplifier, V14, are first filtered by X1 and C26 (+250V) and X2 and C25 (−250V).

17. Valve heater supplies are derived from TR1. The transformer receives its primary mains supply at 45 to 65 c/s from PLB/7 (via FS1) and PLB/10 and produces at the secondary a centre-tapped output of 12·6V. Valve V8 has 6V heaters and the 6·3V supply is dropped to this level by means of a 0·5-ohm dropping resistor in its heater line.

18. The −50V d.c. supply required by relays RLA and RLB enters the unit on PLB/8, the earth returns being completed via PLB/1 and PLB/2 respectively.

Noise control circuit

19. A bipolar video signal, derived from the coherent demodulator unit, is applied to SKP at a level of 3V peak-to-peak. This signal is amplified by V1, and the resultant output applied to the grid of a phase-splitter, V2b. The anti-phase outputs produced at the anode and cathode of V2b are rectified by the full-wave bridge circuit formed by V15 to V18, thereby producing positive-going, unidirectional pulses across the LEVEL (SKJ) potentiometer, RV1.

20. The operating characteristics of V1 and V2b are stabilized by returning the valve cathodes to the −250V supply via R6 and R11 respectively. However, the valves are also provided with a conventional cathode-to-earth bias arrangement formed by R5 and R10. Consequently, variations in the supply potential or valve characteristics cause a change in current through R6 or R11, thus producing adjustments in the valve electrode potentials which tend to compensate for the variations. Changes in the valve currents caused by signals applied to the grids occur through R5 or R10, so that the circuit operation of the valves is not significantly affected by the bias arrangements. Similar bias circuits are also provided for valves V3a, V6, V7, V12 and V14.

21. The rectified video pulses appearing at the slider of RV1 are amplified by V2a and the negative-going pulses from the anode of the valve are d.c. restored to earth by the diode V19, before being amplified further by V3b. After amplification and inversion by V3b, the pulses are fed via a cathode follower, V3a, to the limiter circuit formed by V21 and V22.

22. The purpose of the limiter is to provide a noise sample to the succeeding circuits which is independent of amplitude variations after a predetermined level of noise has been reached. This is achieved by taking a 1V 'slice' from the amplified video signal.

23. Since the limiter circuit is level-sensitive, positive-going input pulses are d.c. restored to earth by the diode V20, which remains conducting for all negative excursions of the input, and also for all positive excursions up to the potential set by the divider network R24 and R25, i.e. approximately 60V. For positive excursions above this level V20 ceases to conduct, and the excess voltage is allowed to appear at the anode of V21. However, V21 is maintained in a non-conducting state by a back potential of approximately +7V at its cathode derived from the divider chain R27, R28, and applied via V22.

24. Should the potential at the anode of V21 exceed 7V, the diode conducts, and the potential is transmitted as a back potential to the cathode of V22. This diode remains conducting for approximately 1V reverse voltage, therefore positive pulses are sampled between the limits of 67V and 68V before being admitted to the grid of V4b. Thus the sample has a constant amplitude of approximately 1V.

25. The amplifier V4b is rendered inoperative for approximately the first 2 milliseconds of the radar timebase sweep in order to prevent local clutter and short-range signals from contributing to the final noise control voltage. This is achieved by rapidly charging C8 with the positive-going 0 microseconds pulse from SKR. The pulse, which has an amplitude of 20V, charges the capacitor through R32 and the grid-to-cathode resistance of V4b. At the cessation of the pulse, the discharge current through R29 maintains the grid of V4b sufficiently negative for the valve to remain cut-off for approximately 2 milliseconds. Thus only those positive-going pulses sampled after this gating period will pass to the succeeding stage.

26. The negative-going, amplitude-standardized, pulses developed at the anode of V4b are further amplified and inverted by V4a before being coupled to the integrator circuit, which includes V5. The inter-stage coupling capacitors C9 and C10 are relatively low in value in order to block any of the gating waveforms which may pass through V4b.

27. The pulses produced at the anode of V4a are positive-going, and their rate of occurrence represents the noise level at the input to the circuit (SKP). Each pulse is applied through C10 to the junction of the diodes V5a and V5b (*fig.* 3). As V5a anode is connected to earth, the positive pulse applied to its cathode causes it to be cut-off, and the charging current of C10 to be passed through V5b to C11. Since C11 has a much larger capacitance than C10, the change of potential across C11 is negligible. At the cessation of the pulse, C10 discharges rapidly to earth via V5a. This charge-discharge cycle is repeated for each noise pulse, with V5b remaining cut-off between cycles.

28. Between pulses, C11 discharges slowly through R38 and R39 towards the potential at the junction of R106 and R107. However, its discharge rate is sufficiently slow to enable further pulses to increase the potential build-up, until a state of equilibrium is reached when the loss of charge on the capacitor is equal to its increase in charge for each noise sample. Once equilibrium is reached, which occurs very rapidly with a high noise level, the potential on C11 is proportional to the pulse rate at the anode of V4a. This final positive potential, which can be regarded as the noise control voltage, is filtered by the long time constant combination of R38 with C12, and applied to the grid of V6.

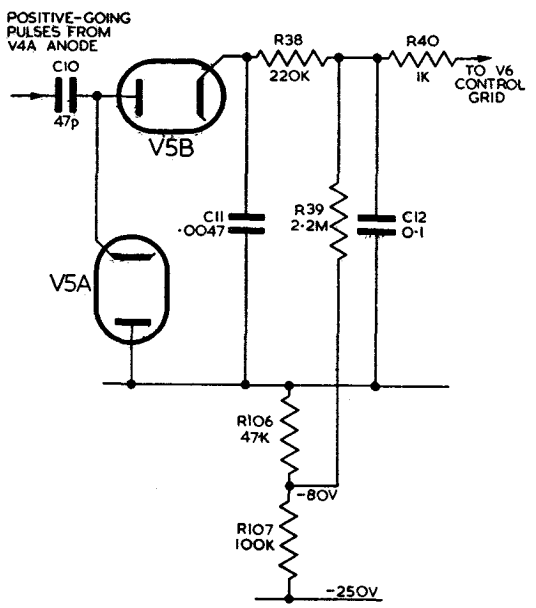


Fig. 3. Integrator : basic circuit

29. Pentode V6 is a d.c. amplifier, producing an output, the mean d.c. level of which is adjustable by means of the GAIN (SKK) potentiometer, RV2. The output of V6 is d.c. coupled to V7b via the LEVEL (SKK) potentiometer, RV3, the setting of which is such that the mean d.c. level of the final output of the circuit is zero. The requisite portion of the negative noise control voltage at the slider of RV3 is fed via cathode follower V7b to SWAa. When the switch is set to either the NOISE CONTROL or SWEPT GAIN & NOISE CONTROL position, the noise control voltage is applied to the cathode of the diode V13b, which, together with V3a, forms an OR gate circuit.

Swept gain function generator

30. The swept gain function waveform (*fig.* 4) is produced by the circuit comprising V8, V9, V10, V11, and V12a. The circuit action is initiated by the positive-going 0 microseconds trigger pulse

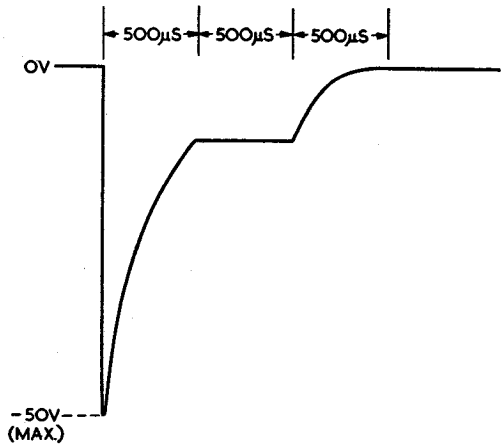


Fig. 4. Swept gain function waveform

which enters the unit at SKR This pulse, which has an amplitude of 15 V and a duration of 4 microseconds is fed from SKR to the noise control circuit, where it is used as a gating pulse (*para.* 25), and also via V23 to the input of the swept-gain control circuit.

31. The diode V23, in conjunction with C13 and R52, forms a pulse stretching circuit, the effect of which is to increase the duration of the trigger pulse by approximately 10 microseconds. The stretched pulse is amplified and inverted by V8, self-bias being provided by R55, decoupled by C15. The negative-going pulse developed at the anode of V8 is limited in amplitude to approximately −54V by V26 which conducts for pulse amplitudes in excess of this level, as set by the potential dividers R56–R57, and R59 and R110.

32. The resultant negative-going pulse from V8 anode charges C17 via R58 and V9b, and C20 with C30 via V11a. At the cessation of the pulse both halves of V9 and both halves of V11 are cut off. Parallel-connected capacitors C20 and C30 begin to discharge exponentially via R74, towards the +8V determined by the potential divider R72–R73, and at the same time C17 begins to discharge towards h.t. via R60.

33. Diode V24 is conducting, and at the junction of R69 and R70 a potential of approximately −10V exists, depending on the setting of RV4. When the voltage across C20 and C30 becomes more positive than the voltage at the junction of R69–R70, V11b conducts and prevents any further discharge of C20 and C30.

34. Simultaneously with the action described above C17 continues its discharge towards h.t. until, after approximately 1 millisecond, the potential at the anode of V9a reaches the cathode potential of the valve, as determined by the divider chain R64 and R65, i.e. approximately −2·5V. Diode V9a then conducts, and the rising exponential waveform is applied via R62 to the grid of V10a.

35. The negative-going edge produced at the anode of V10a approximately 1 millisecond after the initiation of the circuit action is further amplified by V10b, and the resultant positive-going waveform is applied via C19 to V24, thereby causing the diode to cut-off. With V24 cut-off, the voltage at the junction of R69 and R70 rises positively to cut-off V11b, thus allowing C20 to continue its discharge through R74 towards +8V.

36. The waveform produced by the swept gain function generator is shown in fig. 4. This waveform is applied to the grid of the cathode follower V12a, which develops its output across the LEVEL (SKM) potentiometer, RV5, in the cathode circuit of the valve. Since the waveform at the grid of V12a commences from a d.c. level of +8V the end of RV5 connected to the valve cathode is also at approximately this same positive value. The remote end of RV5 is held at a slightly negative potential via R76, and it therefore follows that by adjustment of the potentiometer the d.c. level of the waveform at the slider can be set to zero.

37. The output of V12a is applied to a switched attenuator network formed by R77, R78, R79 and contact of relays RLA and RLB. By means of the relays it is possible to select arrangements of the three resistors from the control console, thereby providing the levels of attenuation of the swept gain waveform, i.e. one-third, two-thirds, and full amplitude. The relays also allow the swept gain waveform to be switched off, in which case the output of the cathode follower is terminated in 30 kilohms. After amplitude selection in the attenuation circuit the waveform is fed to switch SWA. When this switch is in either the SWEPT GAIN or SWEPT GAIN & NOISE CONTROL position the swept gain waveform is applied to the cathode of diode V13a, which, together with the V13b forms an OR gate circuit.

OR gate and gain control selection circuit

38. The inputs to the OR gate formed by double diode V13 are controlled by SWA, which gives a choice of three methods of i.f. gain control and an OFF position.

39. With SWA set to the OFF position, the cathodes of V13a and V13b are connected to earth and the i.f. amplifier V14, operates on fixed gain. When SWA is set to either NOISE CONTROL or SWEPT GAIN, the negative-going output of the selected gain control circuit is connected to the cathode of the appropriate half of V13, while the cathode of the unused diode is earthed. The common anodes of V13 are kept at a slight positive potential via R81 in series with V25, and the application of a negative-going pulse to one of the diode cathodes causes that half of the valve to conduct. The selected gain control voltage is then applied to the grid circuit of the i.f. amplifier.

40. When SWA is set to the SWEPT GAIN & NOISE CONTROL position the output of the noise control circuit is applied to V13b cathode, and the output of the swept gain circuit to the cathode of V13a. When both control voltages are present simultaneously at V13, the output developed at the common anodes of the diodes is a function of the more negative of the two waveforms, and this output is then passed to the grid circuit of V14. However, if only one of the control voltages is present the selective action of V13 ceases, and the operation of the circuit reverts to the method described in para. 39.

41. The trailing edge of the gain sweeping waveform from V12 rises towards a potential which is slightly positive with respect to earth. The diode, V25, connected between the anodes of V13 and earth clamps the waveform at earth and thus ensures a definite termination to the exponential waveform.

I.F. amplifier

42. The grid circuit of V14, the i.f. amplifier, is fed with either linear or anti-jamming i.f. signals at 13·5 Mc/s, via SKS. The grid circuit also receives either the noise control or swept gain control voltage, as selected by SWA and the OR gate, V13.

43. Under fixed gain conditions, i.e. with neither control circuit operational, V14 has a nominal gain of unity. However, when either of the negative-going control voltages are applied, the gain is modified, and the output of the valve is reduced.

44. The anode circuit of V14 is tuned to 13·5 Mc/s by the variable inductor L1, and the final output of the unit, developed across the inductor, is fed via C29 to the parallel-connected sockets SKU and SKV. In the application of the unit described in this chapter, SKV is not used, and the output from SKU is routed to the i.f. amplifier (i.a.g.c.) M2.

Multimeter readings

45. With the multimeter Type 100 connected to socket SKA via a plug-to-socket adaptor, the readings obtained under operating conditions should be as indicated in Table 1.

TABLE 1

Multimeter readings

Multimeter switch position	Stage monitored	Measured across resistor	Reading	Tolerance
A	V1	R92	0·45	±0·09
B	V2b	R93	0·55	±0·11
C	V2a	R94	0·45	±0·09
D	V3b	R95	0·45	±0·09
E	V3a	R96	0·55	±0·11
F	V4b	R97	0·45	±0·09
G	V4a	R98	0·40	±0·08
H	V6	R99	0·50	±0·10
J	V7a	R100	0·55	±0·11
K	V10b	R103	0·50	±0·10
L	V12b	R104	0·45	±0·09
M	V10a	R102	0·45	±0·09

Monitor points

46. Monitor test points are provided at sockets SKD to SKN. The waveforms obtainable at these points are shown in fig. 6.

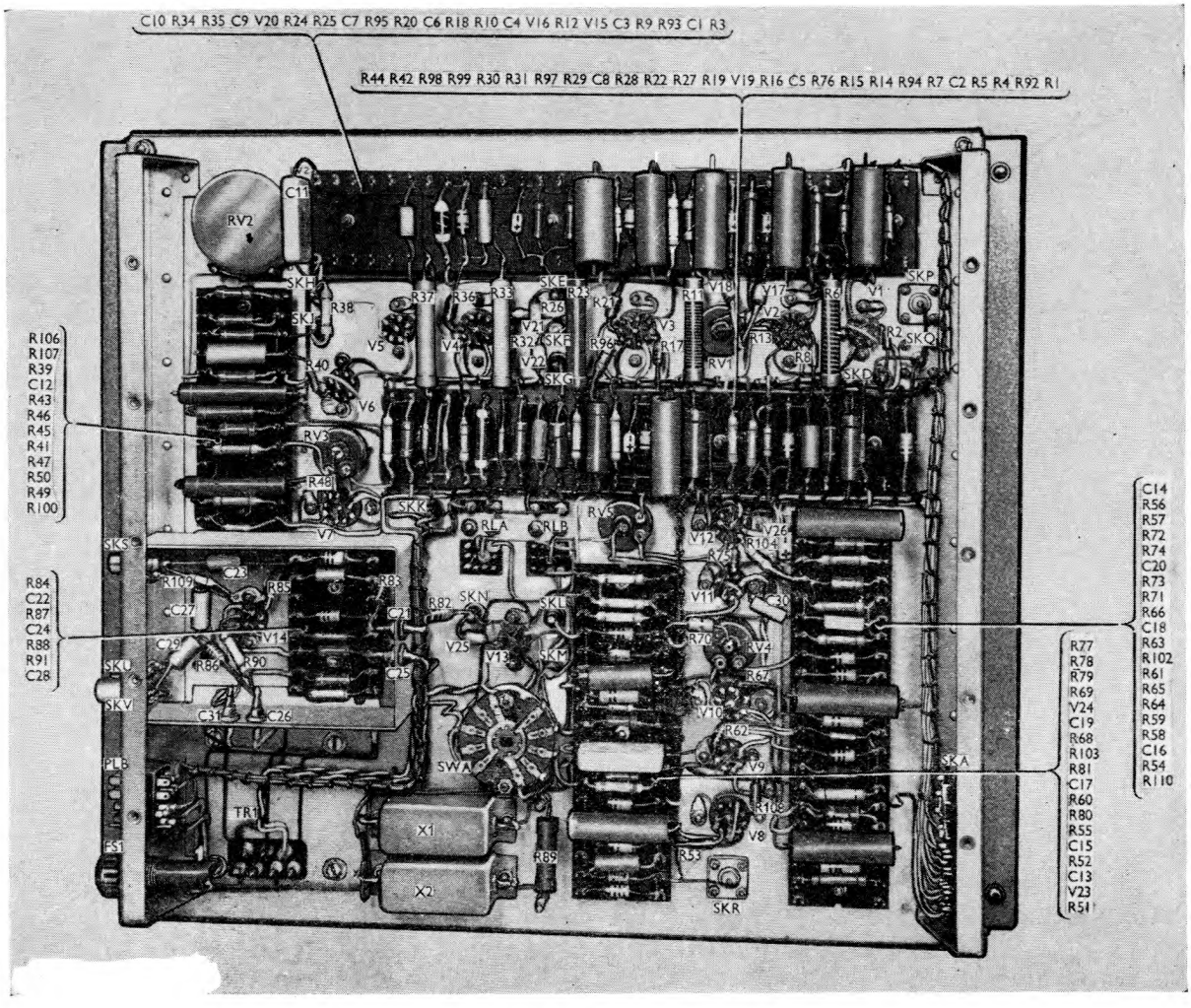


Fig. 5. Limiter, electrical noise M1 : rear view

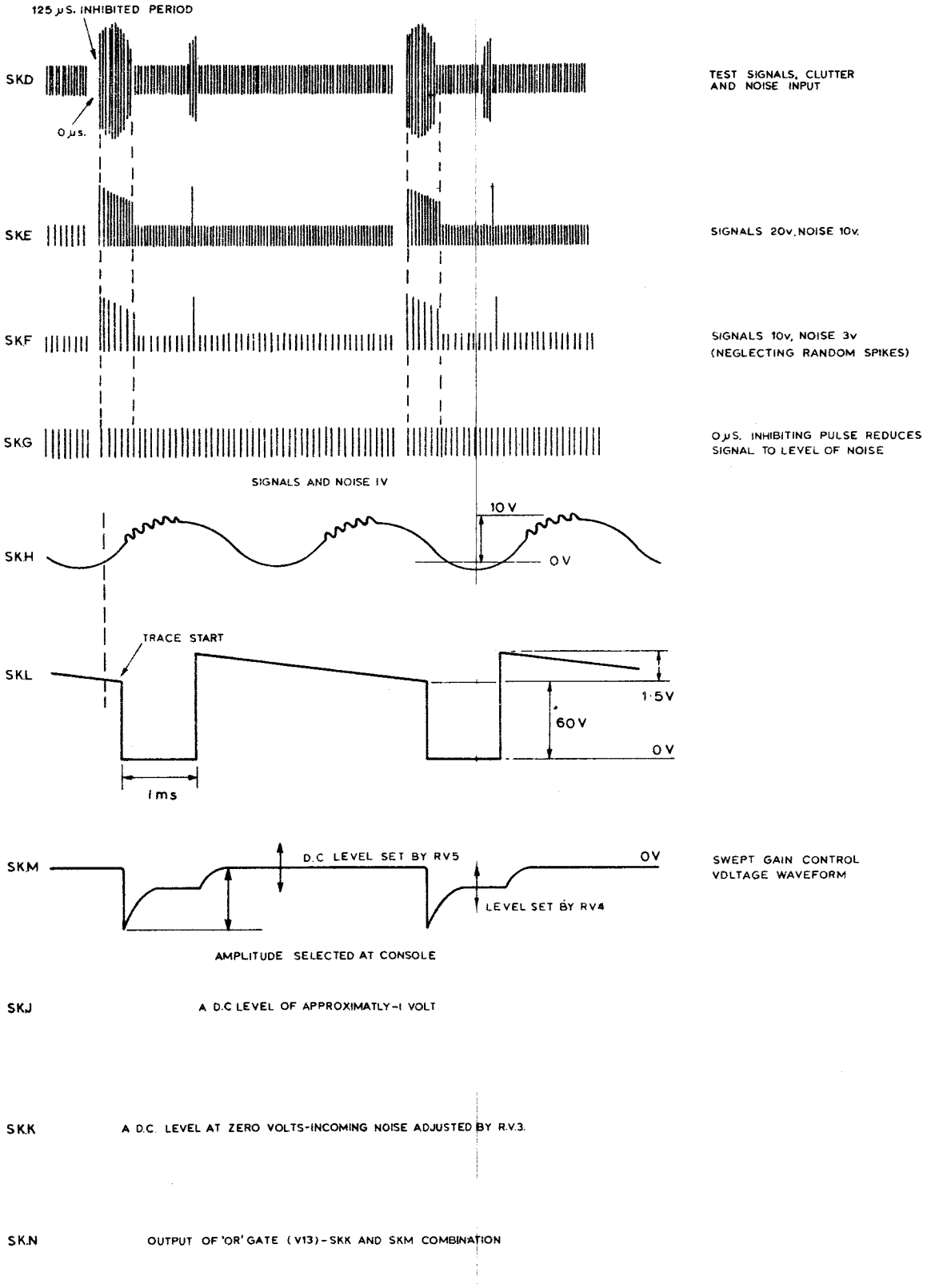


Fig. 6 Waveforms at monitor points

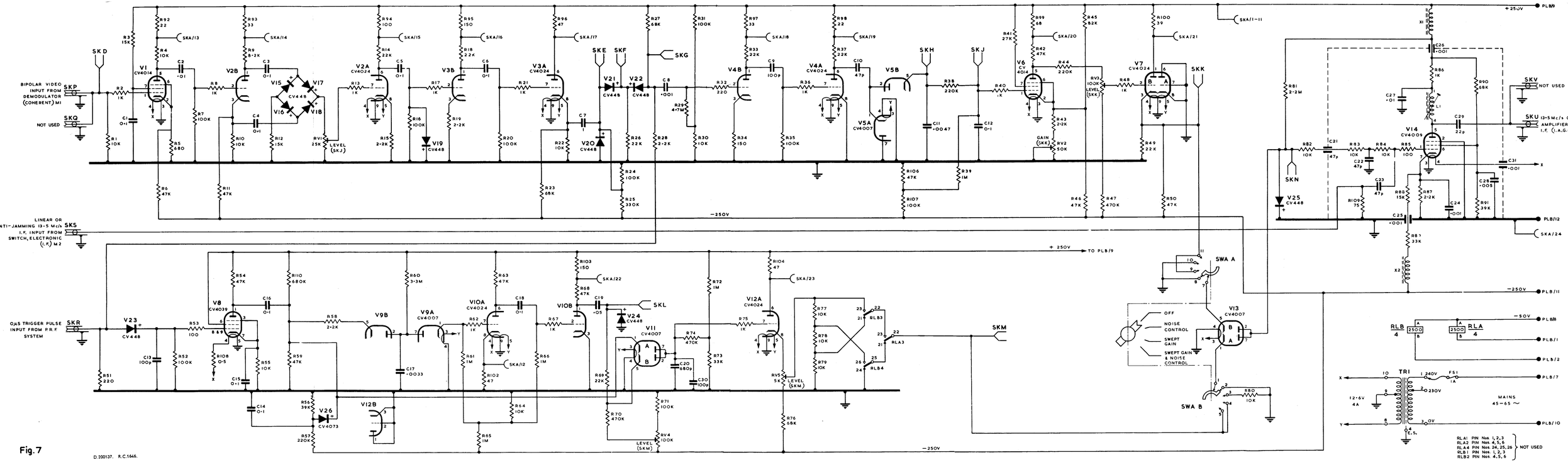


Fig. 7

D.200137. R.C.1646.

Limiter, electrical noise M1: circuit

Fig.7

Chapter 8

AMPLIFIER ASSEMBLY I.F. (I.A.G.C.) M2

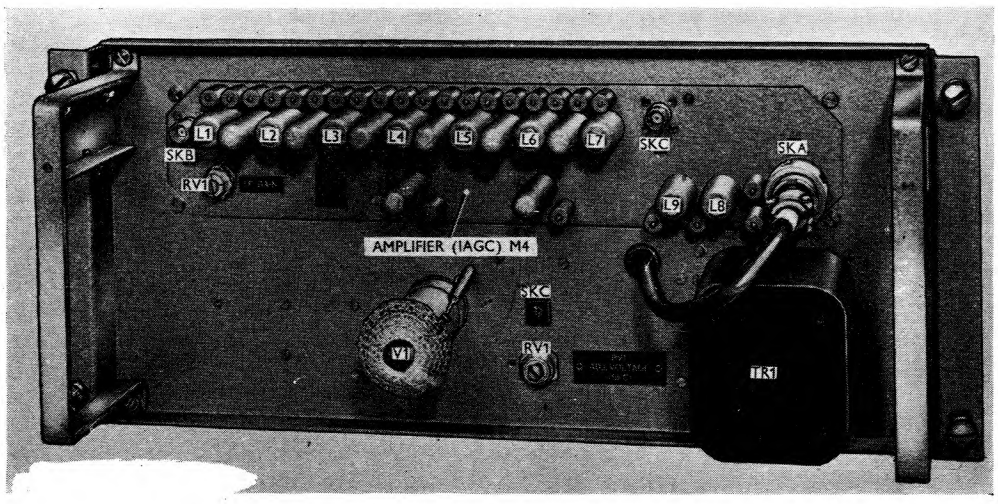
LIST OF CONTENTS

LIST OF ILLUSTRATIONS

Introduction

1. The i.f. amplifier assembly (i.a.g.c.) M2 (*fig.* 1 *and* 5) forms part of the MTI signal channel and is situated on frame 1 of the i.f. cabinet. The unit consists of a main chassis on which is mounted an interchangeable sub-assembly comprising the amplifier (i.a.g.c.) M4. Input power connections are brought to the main chassis, where a series regulator valve reduces the h.t. potential to a level suitable for application to the amplifier (i.a.g.c.) M4. A mains transformer, also on the main chassis, provides a supply to the heaters of all valves within the assembly.

2. The function of the assembly, which accepts either linear or anti-jamming i.f. signals at 13·5 Mc/s, is to preserve the amplitude and phase characteristics of the signal which is fed to the succeeding MTI circuits. This is achieved by providing instantaneous control of i.f. gain, as distinct from the more conventional form of a.g.c. (which has an appreciably delayed response and recovery time). The disadvantage of the conventional system is that strong target and clutter returns, or c.w. interference, could saturate the i.f. amplifier to such an extent that a weaker target return could be lost. This is avoided by the use of



(C40039)

Fig. 1. Amplifier assembly i.f. (i.a.g.c.) M2 : front view

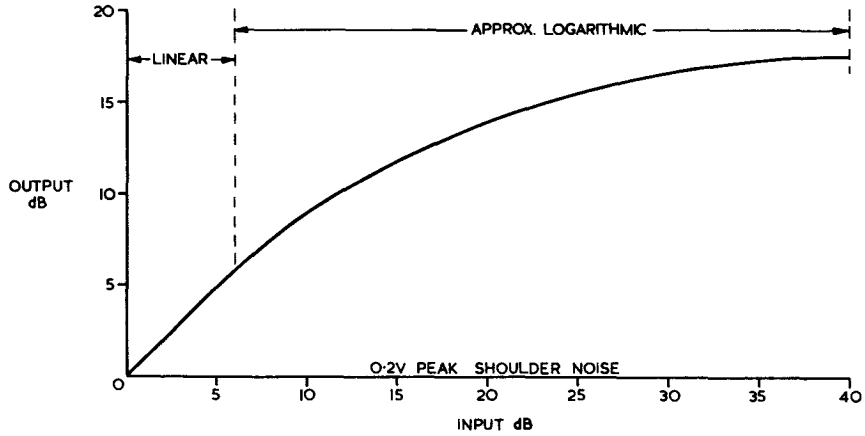


Fig. 2. Specimen response characteristic

an i.a.g.c. amplifier in which amplified negative feedback is applied across individual stages of the amplifier chain. The overall gain of the amplifier is unaffected at low signal levels but is progressively reduced as the input signal amplitude is increased. Such an amplifier has a lin/log characteristic, input signals up to a certain level being subject to linear amplification whereas inputs above that level receive logarithmic amplification. A specimen response curve for the i.a.g.c. i.f. amplifier M4 is given in fig. 2. It will be seen from this curve that, with the shoulder noise level set to 0·2V peak (by means of a manual gain control) the transition from linear to logarithmic operation occurs at an input level of approximately 6 dB. Thus low level amplitude variations, i.e. between 0 and 6 dB, are allowed to appear as such at the amplifier output while input variations above 6 dB are compressed at the output.

Performance characteristics

3. The i.a.g.c. i.f. amplifier operates at a centre frequency of 13·5 Mc/s and has a bandwidth at 3 dB points of 800 kc/s $\pm$ 100 kc/s. The maximum linear gain of the unit is 80 dB $\pm$ 5 dB while the i.a.g.c. compresses input signals of from 6 to 40 dB above noise to within 12 dB at the output. The manual I.F. GAIN control has a range of 45 dB $\pm$6 dB.

Input

4. Anti-jamming or linear i.f. signals at 13·5 Mc/s are fed into the unit at SKB, which presents an input impedance of 75 ohms.

Output

5. The 13·5 Mc/s i.f. output produced by the unit appears at SKC at an output impedance of 75 ohms and is fed to the amplifier (i.f.) M1.

Constructional details of amplifier (i.a.g.c.) M4

6. The screened amplifier (i.a.g.c.) M4 sub-assembly is mounted on the underside of the main chassis by four 4BA cheesehead screws locating through the main chassis into hank bushes on the sub-assembly. A flanged baseplate on the sub-assembly completes the screening and is secured by fourteen 8BA cheesehead screws.

7. Valves V1 to V8 are of the sub-miniature wired-in type and are inserted from the chassis underside into screening cans integral with the chassis. A phosphor bronze heat dissipator inside each screening can provides a heat conduction path from valve to chassis. The method of fitting the valves is described in Sect. 2, Chap. 3. The majority of the decoupling capacitors are also fitted into screening cans integral with the chassis; connections to these capacitors are made as shown in Sect. 2, Chap. 3.

Brief circuit description

8. The circuit, a block diagram of which is shown in fig. 3, consists basically of six stages of 13·5 Mc/s i.f. amplification in cascade. Manual gain control is applied to the first two stages, giving a range of manual control of 45 dB.

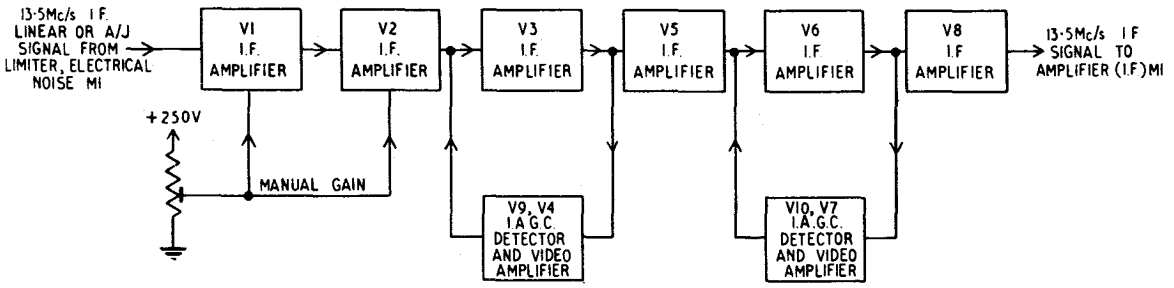


Fig. 3. Amplifier (i.a.g.c.) M4: block diagram

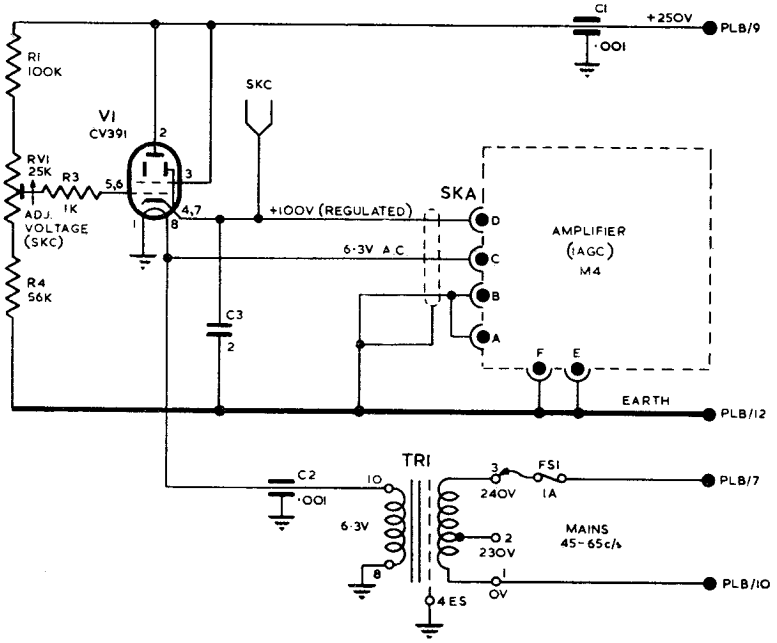


Fig. 4. Amplifier assembly i.f. (i.a.g.c.) M2 : circuit

9. Outputs are taken from the third and fifth stages and these outputs are detected by diode circuits which have time constant characteristics which are short compared with the pulse width. The video outputs of the detector circuits are amplified and fed back as i.a.g.c. bias potentials to the grids of the third and fifth stages.

Circuit description

Power supplies

10. The power supplies required by the assembly are brought in at PLB on the main chassis (*fig.* 4). The 250V supply enters on PLB/9 and PLB/12 (earth) and is supplied to a voltage regulating circuit formed by V1 and its associated components. V1 acts as a conventional cathode follower, the cathode load of the valve being formed by the h.t. load of the amplifier i.a.g.c. sub-assembly. The grid of V1 is held at +100V by the potential divider formed by R1, RV1 and R4, connected between the +250V line and earth, with the result that by cathode follower action the output at the cathode of the valve is held at a positive potential of 100V ± 5V, irrespective of variations of cathode loading. This +100V supply is fed to the amplifier sub-assembly via SKA/D and SKA/F (earth).

11. The valve heaters supply required by the assembly is produced by the mains transformer TR1, mounted on the main chassis. The primary of the transformer receives the a.c. mains supply from PLB/10 and PLB/7. via FS1, and produces at its secondary 6·3V which is fed to the heaters of V1 on the main chassis and, via SKA/C, to the heaters of the valves in the sub-assembly.

I.A.G.C. i.f. amplifier

12. The circuit of the i.a.g.c. i.f. amplifier is given in fig. 6. The h.t. and heater supplies enter the sub-assembly at PLA, via SKA of the main chassis, and are filtered respectively by L8, C31, C33, C35, C37 and L9, C32, C34, C36, C38 with 0·01 microfarad capacitors connected across the heaters of V1, V2, V3, V5, V6 and V8.

13. The amplifier chain consists of six similar stages of i.f. amplification V1, V2, V3, V5, V6 and V8, each stage being tuned to a centre frequency of 13·5 Mc/s. The input to the unit at SKB consists of linear or anti-jamming i.f. signals at 13·5 Mc/s derived from the limiter, electrical noise M1. The input stage consists of the series circuit formed by R1, L1 and C2, giving an input impedance of 75 ohms. From SKB the signals are applied to the grid of the first amplifier stage, V1. The i.f. output of V1 is developed across the primary of the bifilar wound inductor L2, which forms the anode load and is tuned to 13·5 Mc/s. The resultant i.f. output is fed to the grid of the next amplifier stage, V2, which is identical in operation to V1. Manual control of the gain of the first two stages, and hence the overall gain of the amplifier, is effected by the I.F. GAIN potentiometer, RV1. This control, with R2, forms a potential divider between the +100V h.t. line and earth. The potential appearing at the slider of RV1 is fed via R4 and R8 to the cathode circuits

of V1 and V2 respectively, thereby adjusting the cathode bias potential of the valves. The range of control available by means of the potentiometer is 45 dB. The i.f. output from V2 is fed to the succeeding amplifier stages V3, V5, V6 and V8 with i.a.g.c. (*para.* 14) applied to V3 and V6. The output from V8 is fed, via SKC, to the amplifier i.f. M1.

I.A.G.C. circuit

14. The 13·5 Mc/s output from V3 is detected by V9, R18, C18 and fed to the grid of the video amplifier V4. The ferrite bead, L10, in the grid circuit of this valve provides stability. The output appearing at the anode of V4 is passed to the grid of V3 as a bias potential. The diode V11 is placed across V4 anode resistor, R14, and has the effect of varying the anode load according to the signal level, thereby enabling the desired shape of the input/output characteristic to be obtained.

15. A second i.a.g.c. loop, similar to that described in the preceding paragraph, is applied to the i.f. amplifier stage V6. In this case the output of V6 is detected by V10, R29, C28, amplified by V7 and the resultant bias potential fed back to the grid of V6.

Monitoring point

16. Test socket SKC on the main chassis is provided for checking the 100V d.c. output of the voltage regulator stage by means of a multimeter, Type 1, or similar instrument.

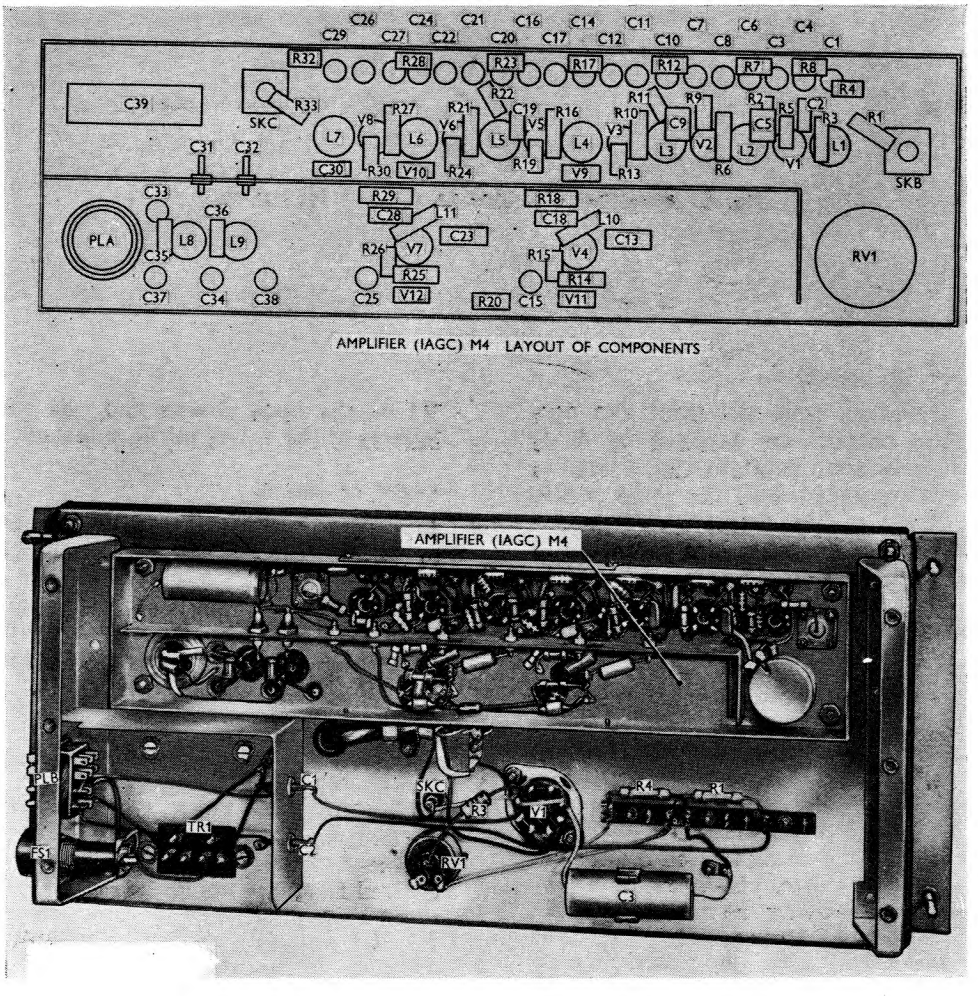


Fig. 5. Amplifier assembly i.f. (i.a.g.c.) M2 : rear view

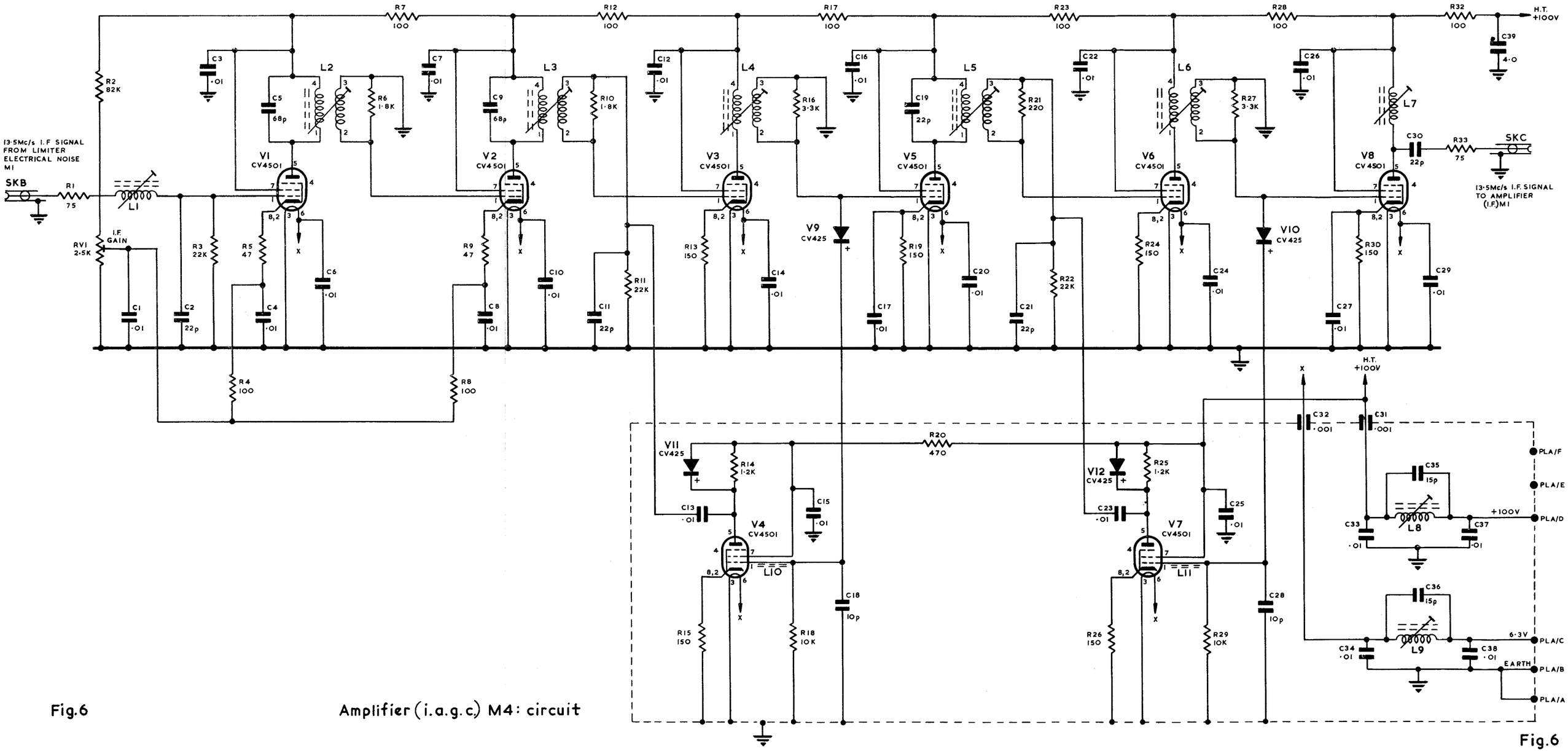


Fig.6

Amplifier (i.a.g.c.) M4: circuit

Fig.6

Chapter 9

AMPLIFIER (I.F.) M1

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

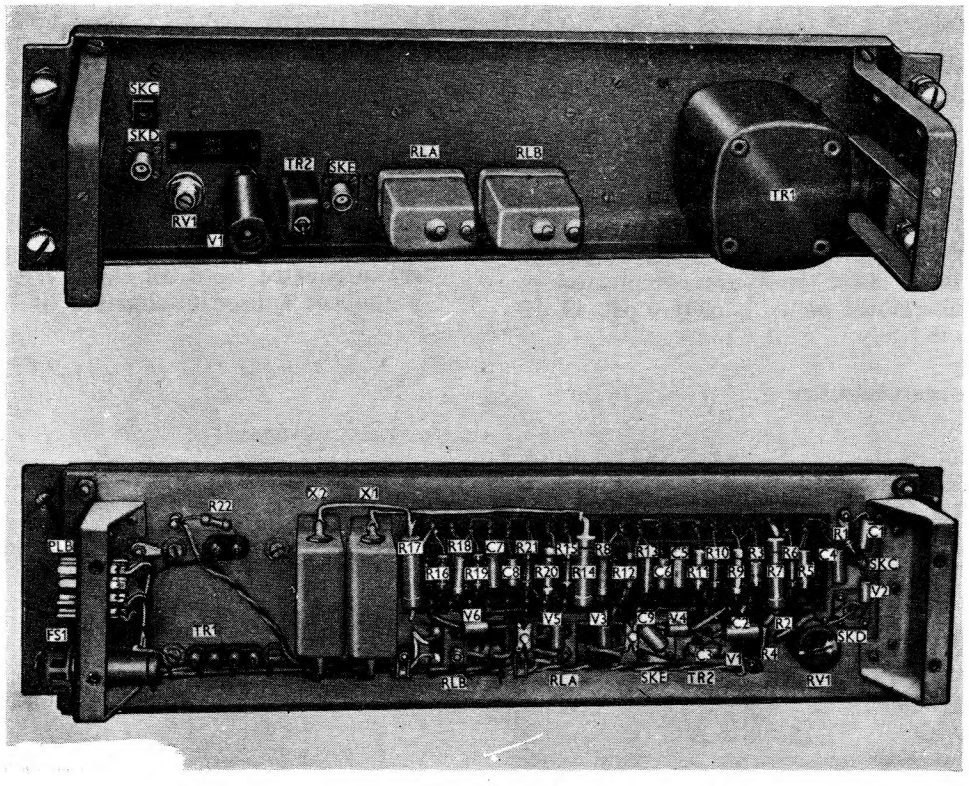


Fig. 1. Amplifier (i.f.) M1: front and rear views

Introduction

1. The amplifier (i.f.) M1 (*fig.* 1) is mounted in frame 1 of the i.f. cabinet. The unit, which forms part of the MTI channel, is used to provide amplitude compression of the 13·5 Mc/s i.f. signals fed to the demodulator (coherent) M1 (*Chap.* 10). The level of compression determines the width of the blind velocity band (*Sect.* 1, *Chap.* 1).

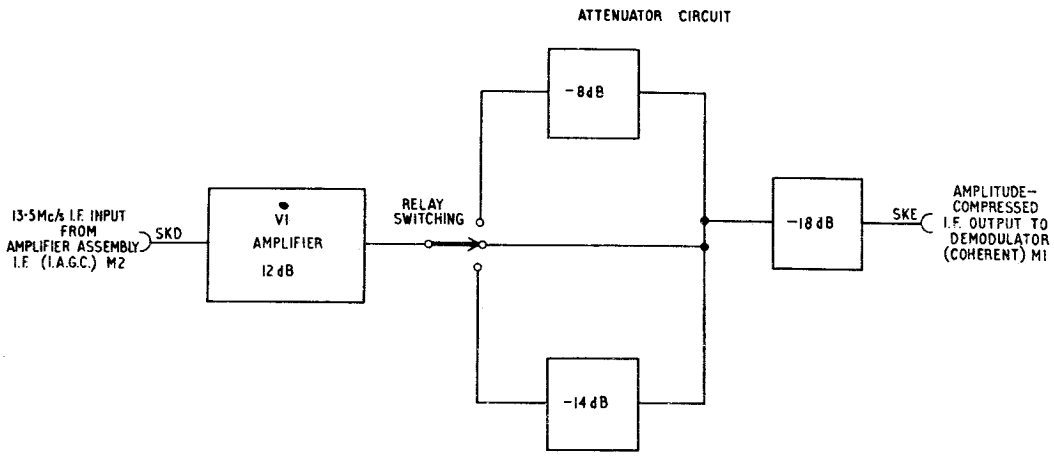


Fig. 2. Amplifier (i.f.) M1: simplified block diagram

2. Use is made of the phenomenon of blind velocities in order to suppress the effect of radially-moving clutter. This is achieved by arranging the speed of the characteristic blind velocity of the system to be equivalent to the mean speed of the clutter (*Sect.* 1, *Chap.* 6). However, under conditions of severe turbulence, random movement within the clutter may occur at slightly different speeds. To compensate for this, the blind velocity is given a tolerance; e.g., for a blind velocity of 56 knots, a tolerance of $\pm 6\frac{1}{2}$ knots may be chosen, thereby giving a blind velocity band with a width of 13 knots between 49·5 and 62·5 knots.

3. The width of the blind velocity band is determined by the level of compression applied to the i.f. signals. Band selection is effected within the i.f. amplifier by relays, the operation of which is controlled by the BLIND VELOCITY BAND switch on the control console. With this switch in one of the three available positions, i.e., 9 KNOTS, 13 KNOTS or 19 KNOTS, variations of signal amplitude above the input noise level are compressed to within pre-determined limits, namely 6 dB, 14 dB or 20 dB respectively.

Performance characteristics

Input

4. The input to the unit at socket SKD consists of 13·5 Mc/s $\pm$ 50 kc/s i.f. signals at a level of 1V peak-to-peak. These signals are fed to the unit via the amplifier assembly i.f. (i.a.g.c.) M2 (*Chap.* 8), at an input impedance of 75 ohms.

Output

5. For an input signal level of 1V peak-to-peak, the output from the i.f. amplifier at socket SKE consists of i.f. signals at 13·5 Mc/s at a level of 0·5V, 0·25V or 0·16V peak-to-peak dependent upon the degree of compression selected by the relays. These output levels only obtain when socket SKE is terminated in 75 ohms by the input impedance of the demodulator (coherent) M1 (*Chap.* 10).

Brief circuit description

6. A simplified block diagram of the unit is shown in fig. 2. The unit, comprising a single stage of amplification followed by relay-controlled attenuation circuits, receives its 13·5 Mc/s i.f. signal input from the i.f. amplifier assembly (i.a.g.c.) which compresses amplitude variations to within 14 dB. The signal is then amplified 12 dB in the amplifier V1 before being passed to the attenuator circuit which introduces the selected amount of compression.

7. The attenuator circuit consists of two pairs of diodes, biased so that conduction starts when the amplified output of V1 reaches a pre-determined level, thereby damping the amplitude excursion of the positive and negative half-cycles. By altering the bias level, the diodes can be made to conduct at a lower level and the signal is damped still further.

8. Selection of the bias level, and therefore of signal attenuation, is effected by two relays, controlled from the control console. With both relays de-energized all i.f. signals, including noise, are attenuated by 6 dB (since the output circuit introduces a fixed attenuation of 18 dB and V1

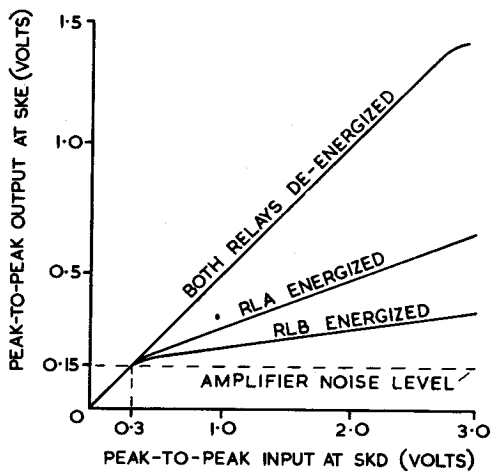


Fig. 3. Effects of blind velocity band switching: response characteristic

has a gain of 12 dB). With either of the relays energized, signal inputs of up to approximately 400 mV peak-to-peak are attenuated by 6 dB, but amplitudes in excess of this level are attenuated by either 14 dB or 20 dB, dependent upon which relay is energized. An approximate response curve for the i.f. amplifier is given in fig. 3.

Circuit description (*fig.* 5)

Power supplies

9. The +250V h.t. supply is fed into the unit at PLB/9 and PLB/12 (earth), with 13·5 Mc/s filtering provided by X1. The −250V supply is fed in at PLB/11 and PLB/12 (earth), filtering being provided by X2. The heater supply for V1 is obtained, via the series dropping resistor R22, from the secondary winding of TR1. This transformer is supplied with mains from PLB/7, via FS1, and PLB/10.

Amplifier and compressor circuit

10. ◀Incoming i.f. signals at SKD are applied via the GAIN control, RV1, to the amplifier V1. Facilities for monitoring the envelope of the modulated 13·5 Mc/s i.f. are provided at SKC by the rectifying circuit V2, C1 and R1.▶

11. ◀Pentode V1 and its associated circuit comprise an r.f. amplifier, the output of which is developed across the bifilar-wound anode transformer TR2, tuned to 13·5 Mc/s. Negative feedback is provided by R4.▶

12. With RLA and RLB de-energized the input at SKD is amplified by V1 and fed via C9 to the output socket SKE. With SKE terminated in 75 ohms by the input impedance of the succeeding unit, C9 introduces approximately 18 dB attenuation and the GAIN control is adjusted so that the overall attenuation of the unit is 6 dB (i.e. V1 having a gain of 12 dB).

13. If the amplitude of the signal produced at the anode of V1 exceeds the bias applied to V3 to V6 inclusive (approximately 10V) the diodes conduct, V3 and V5 on the positive half-cycles, and V4 and V6 on the negative half-cycles. The diode bias potentials are determined by divider networks (e.g. R8, R12, R13) and with either pair of diodes conducting V1 anode load is shunted—in the case of positive excursions by the series-parallel arrangement of R12, R13, R20, R21, and for negative excursions by R10, R11, R18, R19. The overall effect is therefore a considerable damping of the signal output above approximately 10V.

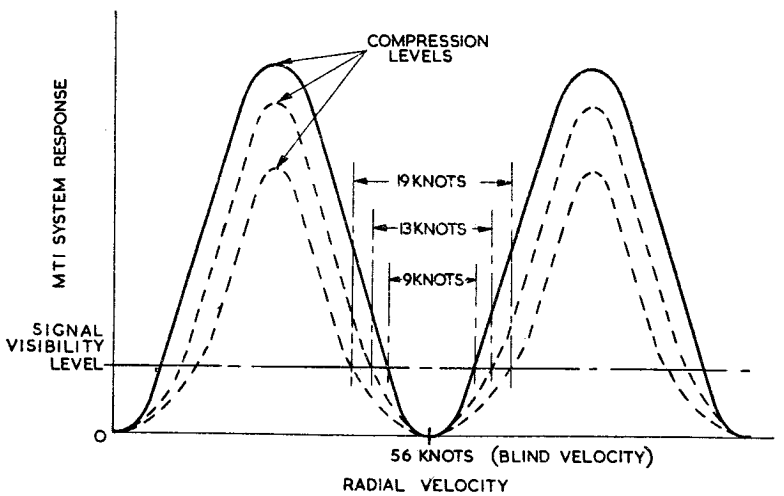
14. With RLA energized by the application of an earth at PLB/2, R12 and R10 are connected directly to earth, thereby adjusting the bias levels at V3 cathode and V4 anode to approximately 0·8V. Compression of the output signal now starts at this level, V1 anode load being shunted by R12 on the positive half-cycles and by R10 on the negative half-cycles.

15. When the earth is removed from PLB/2 and applied to PLB/3, RLA is de-energized and RLB is energized. R20 and R18 are thus connected directly to earth, adjusting the bias levels at V5 cathode and V6 anode at approximately 0·9V. As previously described, signal compression starts at this level, but the damping effect is more severe since V1 anode load is shunted by resistors of lower value (R20 and R18).

16. Fig. 4 shows how the compression or damping of the i.f. signal has the effect of increasing the width of the blind velocity bands.

Monitoring point

17. Monitor socket SKC provides facilities for monitoring the i.f. input to the unit. The waveform to be found at this point consists of a 13·5 Mc/s i.f. envelope at a level of approximately 1V peak-to-peak.



(C45570) **Fig. 4. Relationship between blind velocity band and signal compression**

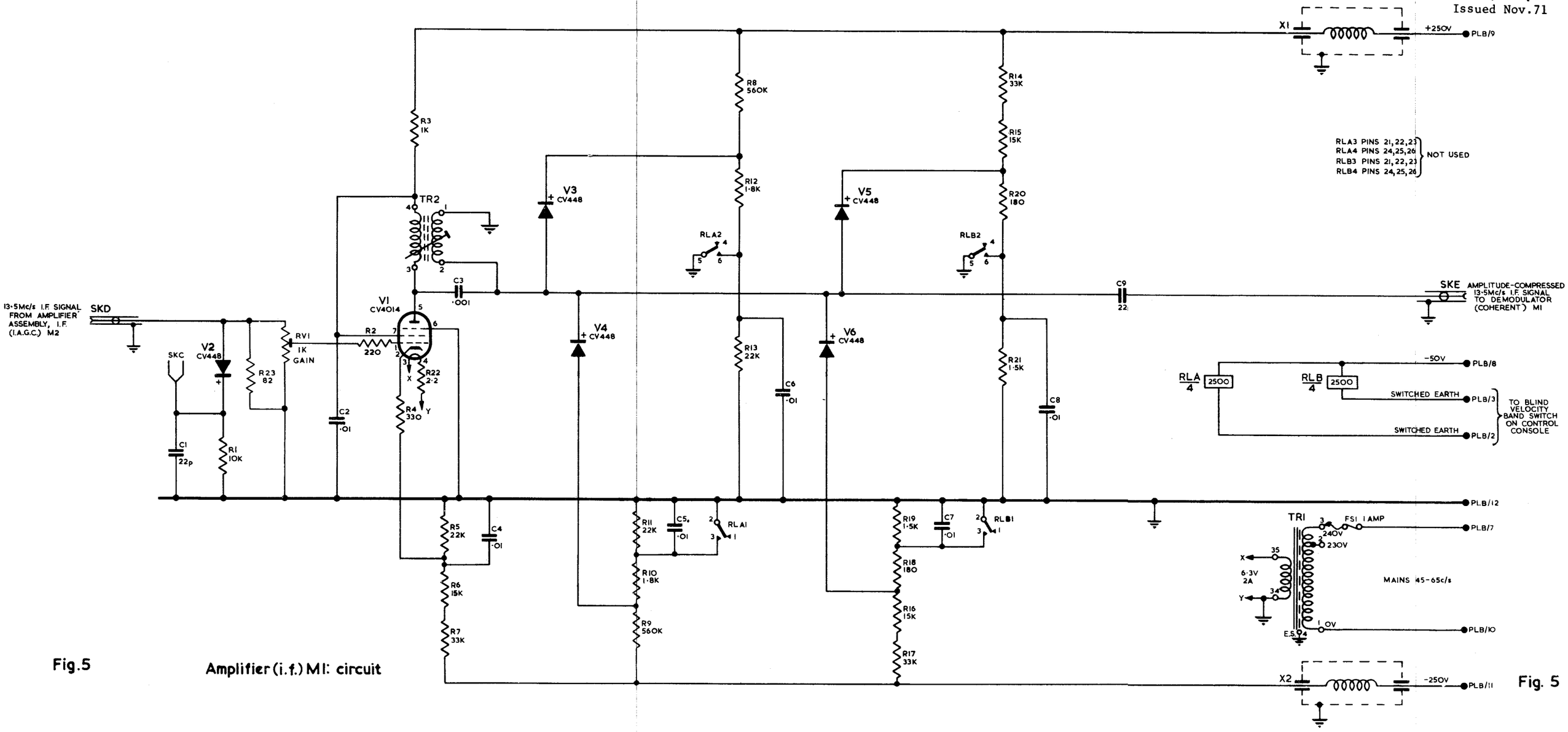


Fig.5 Amplifier (i.f.) M1: circuit

Fig. 5

Chapter 10

DEMODULATOR (COHERENT) M1

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

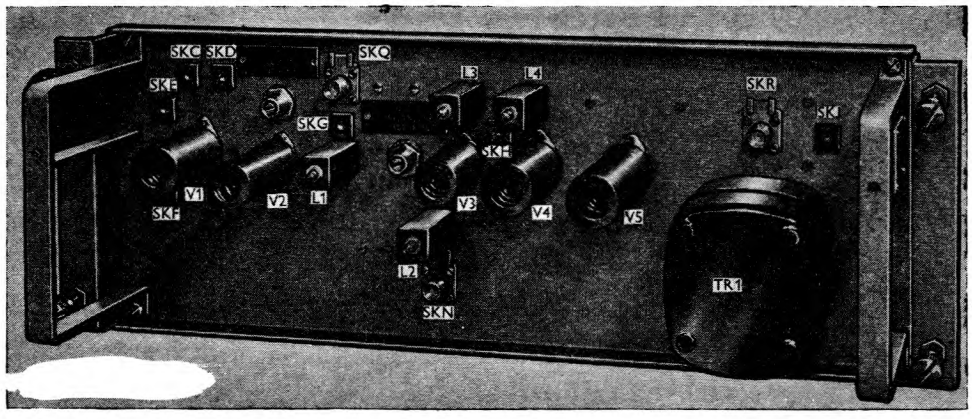


Fig. 1. Demodulator (coherent) M1 : front view

Introduction

1. Two coherent demodulators M1 (*fig.* 1 *and* 7) are used in the MTI signal channel. Both are located in frame 1 of the i.f. cabinet.

2. In an MTI system, the relationship between the phase of the transmitted pulse and the phase of the resulting echo received from a fixed target is the same for successive transmitted pulses reaching the target. The relative phase between the transmitted pulse and the returns from a moving target is continually changing as the distance to the target changes. Within the MTI system, the signals of one sweep are delayed a whole repetition period and compared with the signals from the next sweep.

3. Phase comparisons between the received signals and the transmitted pulse are carried out within the coherent demodulator. The i.f. signal is fed into the unit from the amplifier (i.f.) M1 (*Chap.* 9) and compared with a reference signal which is locked to the transmitter pulse and derived from the oscillator (coherent) M1 (*Chap.* 15). Comparison is effected by means of a phase sensitive detector which produces bi-polar video signals whose amplitude and polarity depend upon the instantaneous phase difference of the i.f. and reference signals. Provision is also made for blanking off the i.f. signals between the -125 μs and the 0 μs pulses in order that the -8 μs pulse, which is used for p.r.f. control purposes, may be clear of noise.

4. Both the coherent demodulators are identical in circuit and similar in operation, one occurring in each of two channels designated channel A and channel B, the difference between the two channels is that channel A is used for suppressing returns from fixed targets and channel B for suppressing returns from moving clutter.

Performance characteristics

Inputs

5. The unit accepts the following inputs :

(1) SKK (channel A) : i.f. signals from the amplifier (i.f.) M1 via the coherent demodulator of channel B.

SKK (channel B) : i.f. signals from the amplifier (i.f.) M1.

(2) SKL (channel A) : the socket is not used in channel A.

SKL (channel B) : 0 μs positive-going pulse from the p.r.f. system.

(3) SKM (channel A) : this socket is not used in channel A.

SKM (channel B) : -125 μs positive-going pulse from the p.r.f. system

(4) SKN (channel A) : 13·5 Mc/s i.f. reference signal from the coherent oscillator and routed via the mixer stage (frequency) M1 (*Chap.* 16) in channel A.

SKN (channel B) : as SKN (channel A) except that the reference signal is routed via the mixer stage (frequency) in channel B.

Outputs

6. The following outputs are provided by the unit :

(1) SKQ (channel A) : this socket is not used in channel A.

SKQ (channel B) : i.f. signals routed to the coherent demodulator of channel A.

(2) SKP (channel A) : bi-polar video signals up to 3V peak-to-peak at a d.c. level of approximately +2V, taken out to the channel A driver (delay line) M1 (*Sect.* 3, *Chap.* 2) in the cancellation cabinet.

SKP (channel B) : as SKP (channel A) except that the output is taken to the channel B driver (delay line) M1.

(3) SKR (channel A) : this socket is not used in channel A.

SKR (channel B) : output as at SKP routed to the limiter electrical (noise) M1 (*Chap.* 7).

Brief circuit description

7. A block schematic diagram is given in fig. 2. Both units receive 13·5 Mc/s i.f. signals from the

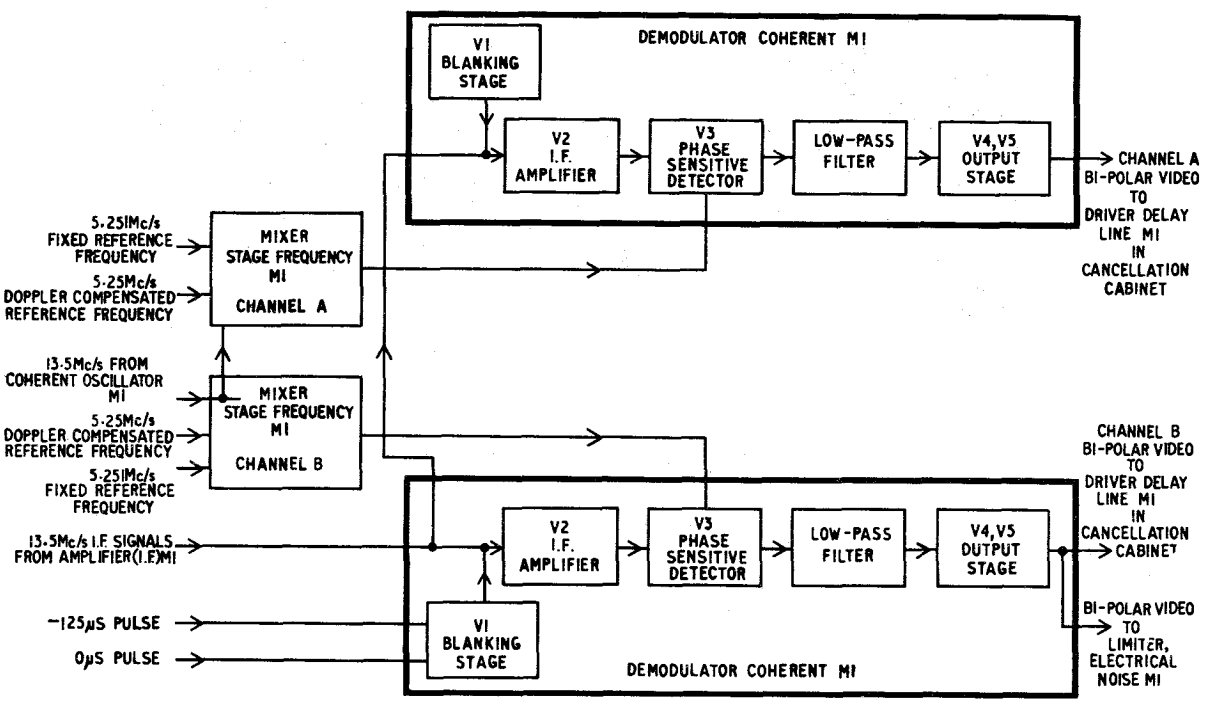


Fig. 2. Demodulator (coherent) M1 : block schematic

i.f. amplifier which are amplified and applied to a phase sensitive detector circuit. In channel B a pulse which starts 125 μs prior to the transmitter pulse is used to switch in a blanking stage which effectively blanks off the i.f. signals. Coincident with the transmitter pulse a 0 μs pulse is fed in, which renders the blanking stage inoperative, thus allowing continuation of the i.f. signals.

8. The phase sensitive detector receives a reference signal which is phase-locked to the transmitter pulse. This signal, which is derived from the coherent oscillator M1, is compared with the receiver i.f. signal and the detector produces a bi-polar video output, the amplitude and polarity of which depend upon the phase difference between the two signals. The reference signal may be modified within the mixer stage (frequency) M1 (*Chap.* 16) for doppler compensation purposes.

9. Both units provide a bi-polar video output to the driver (delay line) units in the cancellation cabinet and in addition the channel B unit provides a similar output to the limiter electrical (noise) M1.

Circuit description (*fig.* 9)

Power supplies

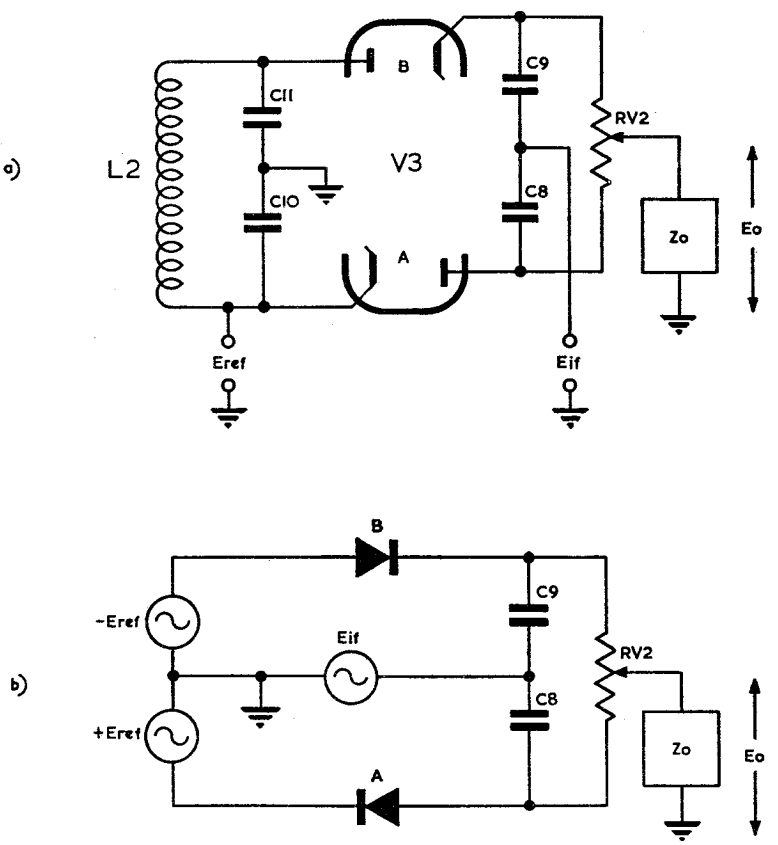
10. The a.c. mains supply to the fused primary of the valve heater transformer, TR1, is routed via PLB/7 and PLB/10. Power to these points is controlled by the main system switch for all units of the system. The transformer produces 6·3V at 2A from its secondary for valves V1 to V5.

11. H.T. supplies of +250V and −250V are fed into the unit on PLB/9 and PLB/11 respectively, the earth connection for both being PLB/12.

I.F. amplifier and blanking stage

12. The incoming i.f. signals at SKK are applied, via RV1, to the grid of V2, a 13·5 Mc/s amplifier which has a bandwidth of approximately 1·25 Mc/s and a gain of 8. The envelope of the incoming i.f. signals is made available for monitoring at SKG by means of the detection circuit V7, C3, R11.

13. By the action of V1 and its associated circuit it is possible to blank off the i.f. signals to the grid of V2 for a pre-determined time, in this case 125 μs prior to the firing of the transmitter. R2 and R3 set the grid potential of V1b at approximately −8V so that V1b is cut off. A positive-going pulse at SKM which arrives at a time of −125 μs (with respect to the transmitter pulse) charges C1 via V1a. V1b is then held conducting while C1 discharges slowly through R4, with a time constant greater than 125 μs. A positive-going pulse at SKL at time 0 μs attempts to raise the grid potential of V1b, and so discharges C1 by grid current through V1b. This produces at the anode of V1b, and hence at the grid of V2, a negative-going pulse of 125 μs duration which cuts off V2 and so blanks off the i.f. signals to the detector. The diode V6 clamps the grid of V2 to earth potential after each 0 μs pulse.



(C38157)

Fig. 3. Phase sensitive detector: simplified circuit

14. The phase sensitive detector, V3, is fed with the amplified i.f. signals from V2 anode and also with a coherent reference signal of about the same amplitude as the i.f. signal. The coil L2 is tuned by C10 and C11 to the reference frequency and provides a balanced output by virtue of the tuning capacitor being in effect centre-tapped and earthed. The reference waveform on V3b anode is thus made 180° out of phase with that on V3a cathode.

15. A simplified circuit diagram of the phase sensitive detector is shown in fig. 3a, whilst fig. 3b shows the equivalent circuit to be used in the following explanation. For the sake of simplicity it is assumed that the amplitude of the reference signal, E_{ref}, equals the amplitude of the i.f. signal, E_{if}, and that these two signals have the same frequency.

16. Consider the case when the phase difference between the i.f. signal and the reference signal is equal to some angle 0. The angle θ is a function of the distance of the target from the radar transmitter, and in the case of a fixed target this will remain constant from pulse to pulse. In the case of a moving target, θ will vary by a finite amount $\delta\theta$ as the target moves a radial distance δD between pulses, where

$$\delta\theta = 2 \times 2\pi \frac{\delta D}{\lambda} \text{ radians.}$$

It will be seen that when δD equals a half wavelength, or a multiple of a half wavelength, $\delta\theta$ will equal 2π, or a multiple of 2π, and there will be no apparent change in θ from pulse to pulse. This is known as a ' blind velocity ' For the purpose of this explanation, it can be assumed that the target being considered is not moving at a ' blind velocity ' and θ is therefore changing from pulse to pulse.

17. Fig. 4 shows the vector diagram of the circuit of Fig. 3b. In this diagram O may be regarded as a fixed point about which the vector components are rotating in a counter-clockwise direction at an angular velocity of $2\pi f$ where f equals 13·5 Mc/s. Vector OA is proportional to the voltage across diode A and its associated load circuit, and vector OB to the voltage across diode B. Diode B will

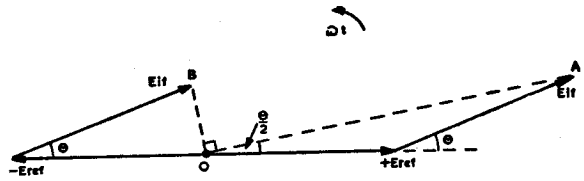


Fig. 4. Phase sensitive detector : vector diagram

conduct whenever its anode goes positive with respect to its cathode and this will occur when vector OB is in the first and the second quadrants. Similarly, diode A will conduct whenever its cathode goes negative with respect to its anode and this will occur when vector OA is in the third and the fourth quadrants. Hence each diode feeds current into the load, charging the capacitors C8 and C9 (*fig.* 3b). The currents through the diodes will be in opposition and are proportional in magnitude to the length of the vectors OA and OB. The load voltages produced by each diode are represented in fig. 5, and the output voltage E_o is proportional to the difference between OB and OA.

18. Consider the following cases :

(1) When $\theta = 0°$. Vector OB will be zero and OA will be a maximum. Diode B will therefore not conduct and the output voltage E_o will be maximum negative.

(2) When $\theta = 180°$. Vector OB will be at a maximum and OA will be zero. Diode A will therefore not conduct and E_o will be a maximum positive.

(3) When $\theta = 90°$. The vectors OA and OB will be equal and therefore, E_o will be zero assuming that RV2 (*fig.* 3b) which adjusts the balancing of the diode outputs under these conditions, has been correctly adjusted. This condition is known as a ' blind phase '

19. An approximate response curve for this type of phase sensitive detector is shown in fig. 6. If the i.f. and reference signals are of the same amplitude, the detector approximates very closely to a linear device, i.e. the d.c. output is directly proportional

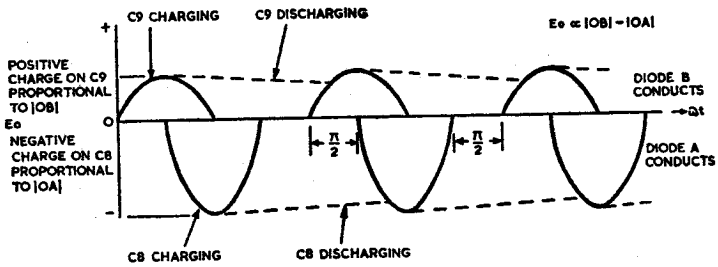


Fig. 5. Phase sensitive detector : theoretical waveforms

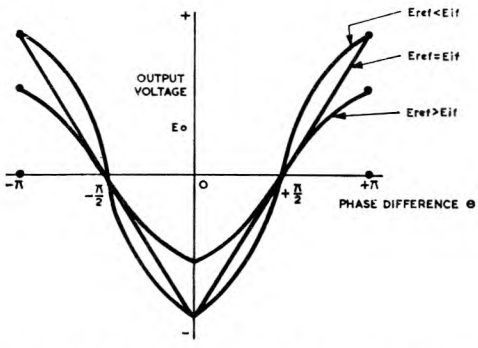


Fig. 6. Phase sensitive detector : response pattern

to the phase difference. For E_{ref}, greater than E_{if} or E_{ref} less than E_{if} the curve tends towards a cosine relationship.

20. In the above explanation it has been assumed that the i.f. and reference frequencies are equal, so that the output at RV2 slider is positive or negative-going video, the pulse to pulse permanent echo cancellation information being contained in the amplitude and polarity of these signals. As explained above, when θ equals 90° the phase sensitive detector has an inherent ' blind phase ' and it produces zero output. The effect of this blind phase may be avoided by using a reference frequency of up to 200 kc/s below the i.f. signal frequency. The output from the detector in this case will, therefore, be a sine wave at the difference frequency, say 200 kc/s, 100 per cent modulated by the video signal. The permanent echo cancellation information is then contained in the relative phase, and not the amplitude, of the video signal. The pulses of 200 kc/s will be extremely short, a 5 μs signal will consist of only one complete cycle at 200 kc/s.

Output stage

21. The bi-polar output from the detector is taken via the 650 kc/s low-pass filter L3, L4, C12, C15, C16, to the output stage V4 and V5. This circuit comprises an amplifier, V4, and a cathode-follower, V5, and has an overall gain of approximately unity. Negative feedback from the output to the first amplifier, V4b, is provided by R37 and R26.

22. A steady d.c. level at the output (monitored at SKJ) is maintained at +1·8V by R32 and R33 and the output signals are set to approximately 3V peak-to-peak by RV1.

Monitoring points

23. The waveforms which should be available at the various monitoring points throughout the unit are shown in fig. 8.

Multimeter readings

24. With multimeter Type 100 connected to SKA the meter readings obtained should be as indicated in Table 1.

TABLE 1

Multimeter readings

Switch position	Stage metered	Meter reading	Measured across
A	V2	0·47 ± 10%	R13
B	V4b	0·59 ± 10%	R24
C	V4a	0·52 ± 10%	R29
D	V5	0·43 ± 10%	R35

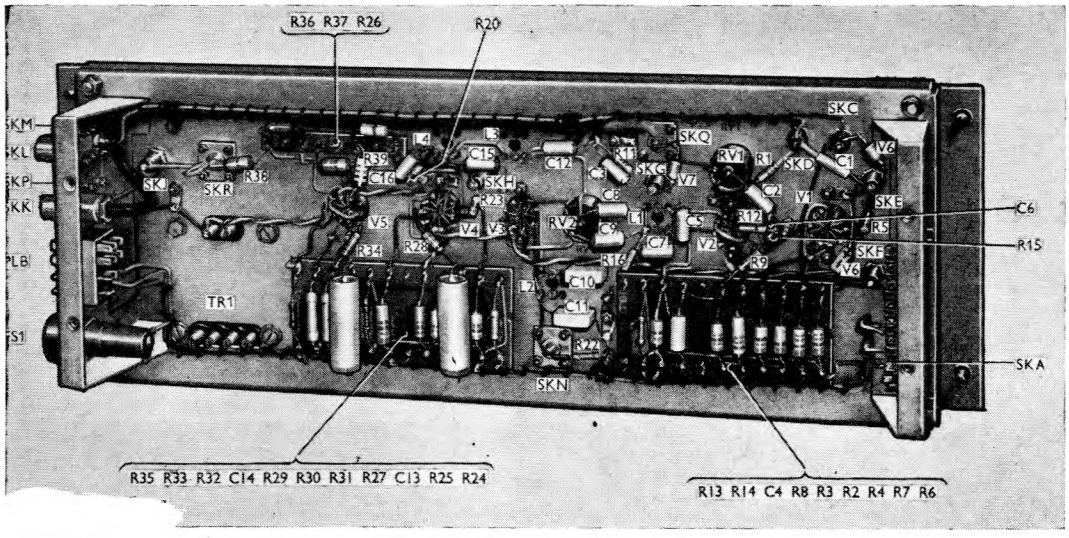


Fig. 7. Demodulator (coherent) MI : rear view

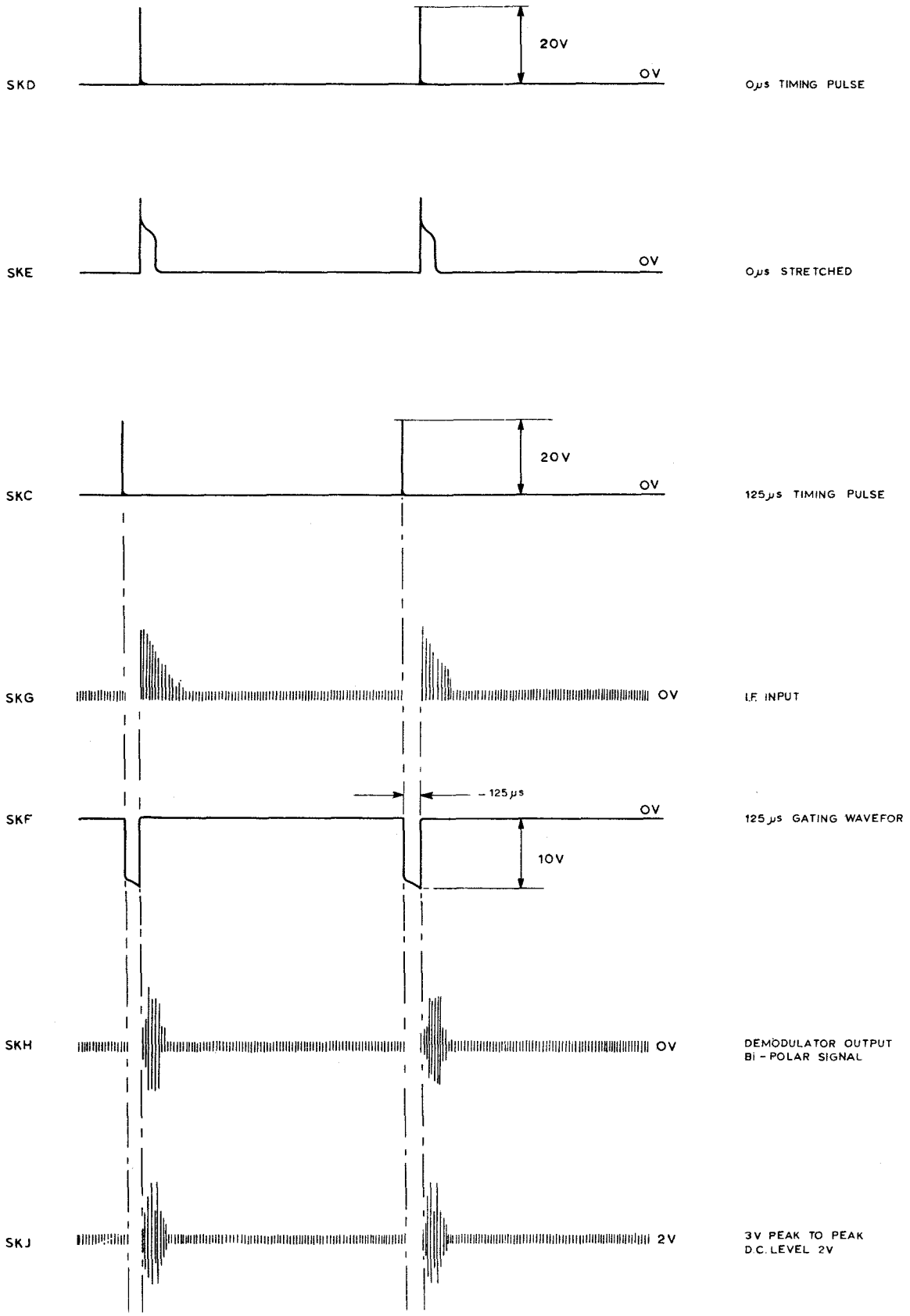


Fig. 8 Demodulator (coherent) MI: monitor point waveforms

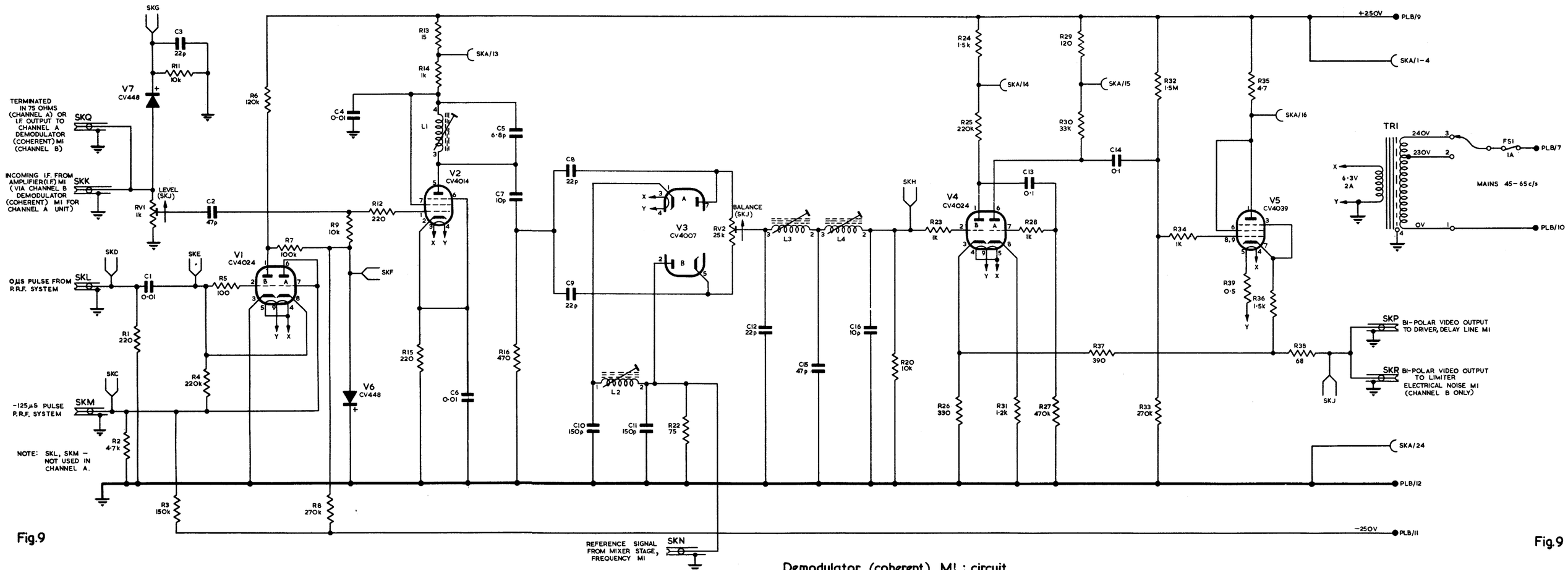


Fig.9

Demodulator (coherent) MI : circuit

Fig.9

Chapter 11

SIGNAL GENERATOR (VIDEO) M2

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

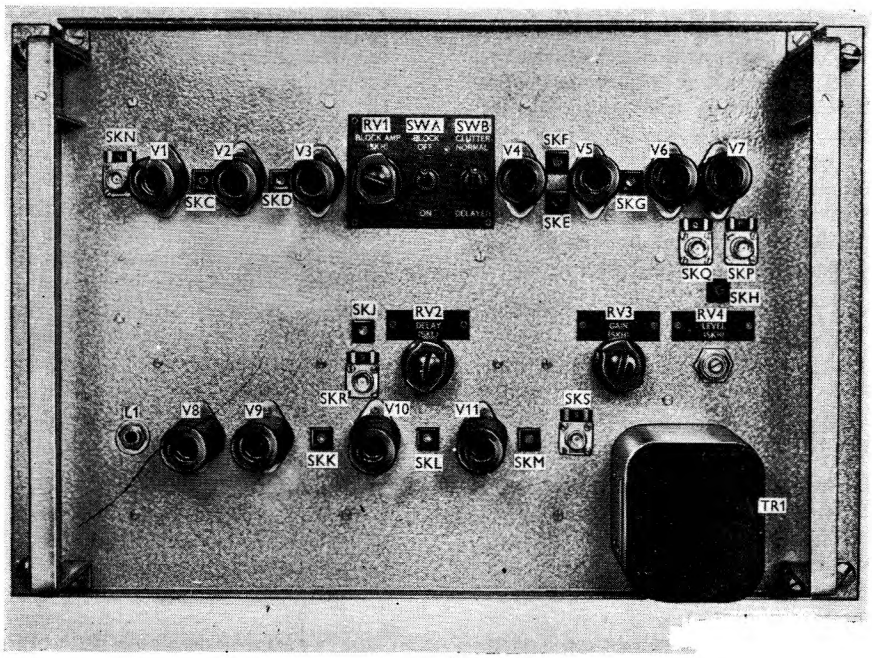


Fig. 1. Signal generator (video) M2 : front view

Introduction

1. The video signal generator (*fig.* 1 *and* 4) is mounted on frame 3 of the i.f. cabinet. The unit is ancillary to the signal processing channels, in that it provides a means of checking their correct functioning. These checks are performed in conjunction with the signal generator (i.f.) M9 (*Chap.* 12).

2. When triggered by the 0 μs pulse from the i.f. signal generator, the unit produces three outputs, as follows :—

(1) A 10 μs pulse, variable in time by between 50 and 1500 μs after the trigger pulse. This output, which is used to gate a 13·5 Mc/s oscillator in the i.f. signal generator, produces an i.f. signal representative of an aircraft echo.

(2) A pulse representative of clutter. The start of this pulse is either coincident with the start of the input pulse (in which case its duration is 1000 μs) or else it starts 1000 μs after the input pulse and ends with the start of the next input pulse (which gives an effective pulse duration of 3000 μs). As in the case of the 10 μs pulse described in (1), the pulse is used to gate a 13·5 Mc/s oscillator in the i.f. signal generator.

(3) A combination of the 10 μs pulse described in (1) and the 1000 μs pulse, starting at 0 μs described in (2). Both these waveforms are at low impedance and the amplitude of the 1000 μs pulse is adjustable. In operation, the 10 μs pulse may be partially or completely masked by the longer pulse unless the latter is switched off or has its amplitude reduced.

Performance characteristics

Input

3. The input to the unit at SKN is a 0 μs trigger pulse derived from the i.f. signal generator, and consists of a positive-going pulse of 5 to 10 μs duration at a nominal p.r.f. of 250 p.p.s. The pulse amplitude is between 10V and 20V when fed into the 220 ohms input impedance presented at SKN.

Outputs

4. The output at SKR is a positive-going rectangular pulse of not less than 12V amplitude into a load of 3·3 kilohms. The pulse will either start at a time coincident with the input pulse and end 1000 μs ± 200 μs later, or start 1000 μs ± 200 μs after the input pulse and end on the arrival of the next input pulse. In either event, the pulse edge occurring between input pulses does not jitter more than 0·5 μs in any period of one second and its rise or fall time does not exceed 2·5 μs. From SKR, the pulse is fed to the i.f. signal generator.

5. A positive-going pulse of 10 μs ± 1 μs duration is produced at SKS and fed to the i.f. signal generator. The pulse amplitude is not less than 12V into a load of 3·3 kilohms, and its occurrence after the trigger pulse is variable in time between the limits of 50 μs and 1500 μs.

6. Sockets SKP and SKQ are connected in parallel and the output appearing at these sockets consists of either the 10 μs pulse described in para. 5, or the result of mixing the 10 μs pulse with a rectangular pulse of 1000 μs ± 200 μs duration, the start of which is coincident with the trigger pulse. The output levels of both pulses are based on earth potential and their amplitudes are independently adjustable from 0V to not less than 1·5V into 75 ohms. The outputs from SKP and SKQ are not permanently routed to any part of the i.f. cabinet, but are available as video test signals, and are fed to the appropriate points in the signal channels when required.

Brief circuit description (*fig.* 6)

7. The unit consists basically of two pulse generators, both triggered by the 0 μs pulse derived from the i.f. signal generator.

8. The 0 μs pulse is first amplified and inverted, and then applied as a trigger pulse to two flip-flop circuits. The output of one of these flip-flops (V2) is fixed at a duration of 1000 μs but by inverting this output and d.c. restoring the two pulses to the same level, a choice is given by SWB between a 1000 μs pulse starting at 0 μs, or a 3000 μs pulse starting 1000 μs later. The selected pulse is fed via a cathode follower (V3b) to SKR, from where it is routed to the i.f. signal generator. The 1000 μs pulse is also fed via a cathode follower (V4b) and SWA to a diode mixer circuit (*para.* 11).

9. The output of this pulse generator circuit is used in the i.f. signal generator to produce a simulated clutter signal. It is important that the trailing edge of the pulse is free from jitter, as with jitter present positional changes of the trailing edge of successive pulses could give the effect of a moving target. To obviate jitter, the recovery time of the flip-flop is synchronised by pulses at 50 kc/s, derived from an oscillator circuit which is itself gated by the flip-flop pulse.

10. The other flip-flop circuit which is triggered by the 0 μs pulse (V9) produces an output pulse, the duration of which is adjustable between 50 to 1500 μs. After differentiation, the pulse coincident with the trailing edge of the undifferentiated waveform is used to trigger a further flip-flop (V10) which produces an output pulse with a duration of 10 μs, the time of occurrence of which is determined by the duration of the pulse from the triggering flip-flop V9. The resultant pulse is fed via a cathode follower (V11) to SKS, and via another cathode follower (V4a) to the mixer circuit (*para.* 11).

11. The 1000 μs and 10 μs outputs of the two pulse generator circuits are fed to the mixer circuit (V16, V17) which comprises two pulse-passing diodes, arranged as an OR gate. A characteristic of the gate is that where time coincidence or overlap of the applied pulses occurs, there is no potential addition at the output. Since the amplitude of the 1000 μs pulse is adjustable, the presence of the 10 μs pulse may be completely masked if its amplitude is equal to or less than that of the longer pulse. Where there is no time coincidence, the circuit will produce an output when one or other of the pulses is present.

12. The output of the mixer circuit is amplified (V5) and coupled via cathode followers (V6, V7) to the parallel-connected output sockets SKP and SKQ, where it is available for use as a video test signal. Since it is necessary that the rectangular pulse shape is maintained during amplification, a.c. negative feedback is applied to the final amplifier stage. It is also important that the d.c. level of the output is maintained constant at zero and this is effected by means of a d.c. feedback circuit incorporating a d.c. amplifier (V6a). The d.c. level is preset by a restoration circuit controlled by a potentiometer, the preset level being maintained by the feedback loop.

Circuit description (*fig.* 7)

Power supplies

13. The 240V a.c. mains supply to the fused primary of the valve heater transformer TR1 is routed via PLB/7 and PLB/10. Power at these points is controlled by the main system switch for all units of the system. The transformer produces a 12·6V, 4A centre-tapped output at the secondary and this output supplies all the valves within the unit.

14. A positive h.t. supply of +250V from the +250V regulator in frame 1 of the i.f. cabinet is fed into the unit on PLB/9 and PLB/12 (earth). A negative supply of −250V enters the unit on PLB/11 and PLB/12 (earth).

Input circuit

15. The positive-going 0 μs trigger pulse from the i.f. signal generator enters the unit on SKN, from where it is applied to the grid of the amplifier V1b. The diode V12, connected between the grid circuit of V1b and earth, prevents any stray negative-going input pulses from appearing at the output of the amplifier. Such pulses could cause premature re-setting of the flip-flop circuits which are triggered by the output of V1b. V1a is not used and its electrodes are connected to earth.

16. The output at the anode of V1b consists of an amplified and inverted version of the input at SKN, and this output is used to trigger the two pulse generator circuits.

1000 μs pulse generator

17. The negative-going output from the anode of V1b is a.c. coupled to the grid of V2a, which, with V2b, forms a cathode-coupled flip-flop circuit. V2a is normally conducting due to the positive potential of approximately +19V applied to its grid from the divider circuit formed by R7 and R8, connected between the +250V h.t. line and earth. The trigger pulse initiates normal regenerative action, whereby V2a is cut off and V2b conducts.

18. To speed up the recovery time of the circuit, the diode V13 in parallel with R14 is included in the grid circuit of V2b. The diode is so connected as to conduct the discharge current of the time-constant capacitor C4 which occurs when the flip-flop resets. This prevents the grid of V2b from going negative, and also results in a low time constant for the discharge circuit. The time taken for the circuit to reach quiescence is therefore reduced. The negative-going pulse output at the anode of V2b for one cycle of operation has a duration of 1000 μs, the leading edge of the pulse being coincident in time with the 0 μs trigger pulse.

19. Associated with the action of the flip-flop circuit is the gated Hartley oscillator formed by V8a. The 50 kc/s tuned circuit L1, C16, in the cathode-grid circuit of the valve, is shunted by the input impedance at the cathode of V8b. This valve is normally conducting, and its damping effect on the tuned circuit is sufficient to prevent oscillation. When V2 is triggered, the negative pulse produced is coupled to the grid of V8b via C6, and the valve is cut off, thereby removing the load from the oscillator circuit for the period that the flip-flop is in its unstable state and allowing the circuit to oscillate.

20. Excitement of the oscillator is obtained by connecting the anode and grid of V8a to opposite ends of the LC circuit with respect to the cathode connection. At the start of the oscillation, the grid of the valve is at zero potential, and self-biasing during oscillation is provided by the grid capacitor C15 and the grid leak R63. Oscillation builds up until the bias on the valve due to grid current is such that both anode and grid current flow for less than a half-cycle. At the stable operating point, the anode current waveform of V8a consists of a current pulse in each cycle of oscillation, as shown in fig. 2 (a), the p.r.f. being 50 kc/s. Adjustment of the oscillator frequency may be effected by means of the iron dust core of L1.

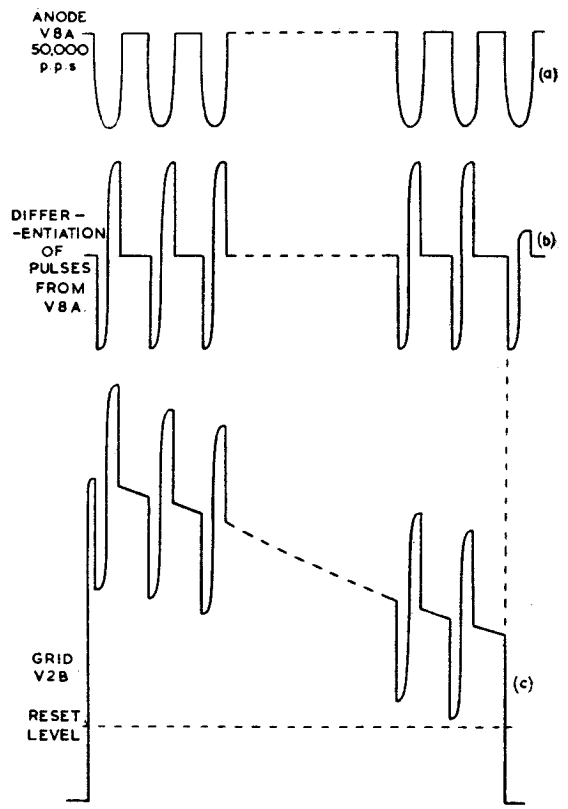


Fig. 2. Action of synchronising pulses

21. The current pulses at the anode of V8a produce corresponding voltage pulses to be developed across the anode load resistor R65. These pulses are coupled into the anode circuit of V2a via C5 and R13, and differentiated by these two components, producing the waveform shown in fig. 2(b). Since the differentiated peaks are developed across R13, they also appear at the grid of V2b, and cause the recovery time of the flip-flop to be synchronised with a particular peak in the differentiated pulse train. By adjustment of the oscillator frequency it is arranged that the recovery time always coincides with a particular negative-going peak of the pulse train, as shown in fig. 2 (c).

When the flip-flop recovers, the gating pulse is removed from the oscillator circuit and oscillation ceases.

22. By injecting synchronising pulses which occur at highly stable intervals into the flip-flop circuit, the principal cause of trailing-edge jitter (i.e. a slow approach to the recovery threshold) is minimised. As the flip-flop timing circuit charges (or discharges) exponentially, the rate of the charge (or discharge) continuously decreases. If the threshold potential at which the flip-flop resets is close to the final potential at which the timing circuit aims, then by the time this potential is approached the rate of approach will be very slow. In the threshold zone the circuit is very unstable, and could be triggered back to its quiescent state by any random pulse that may occur, thereby causing the trailing edge of the output produced by the flip-flop to jitter between successive pulses. By introducing steep-sided pulses into the circuit, the recovery threshold is cut sharply by one particular pulse and jitter is removed, provided the pulses have sufficient amplitude and their recurrence frequency is properly selected.

23. The negative-going, 1000 μs pulse produced at the anode of V2b is fed to the grid of V3a, and also to the DELAYED position of the CLUTTER switch SWB. V3a produces an inverted version of the 1000 μs pulse at its anode and this positive-going pulse is connected to the NORMAL position of SWB. From SWB, the selected pulse is coupled via the cathode-follower V3b to the output socket SKR. A d.c. restoration circuit formed by the diode V14 is included in the grid circuit of V3b, such that the d.c. level of the selected pulse is restored to the level determined by the potential divider R23, R24, i.e., approximately +15V. Thus, the two pulses available at the grid of V3b consist of a positive-going pulse of 1000 μs duration, starting at 0 μs (NORMAL) or a positive-going pulse of 3000 μs duration, starting 1000 μs later (DELAYED). The time and polarity relationship of the two pulses is shown in fig. 3.

24. The cathode circuit of V3b, in addition to incorporating the conventional cathode resistor R27, connected between cathode and −250V, also includes another resistor, R26, connected between cathode and earth. The purpose of this arrangement is to provide protection of the heater-to-cathode insulation should the valve be inserted while cold with the unit switched on. The potential divider formed by the two resistors ensures that

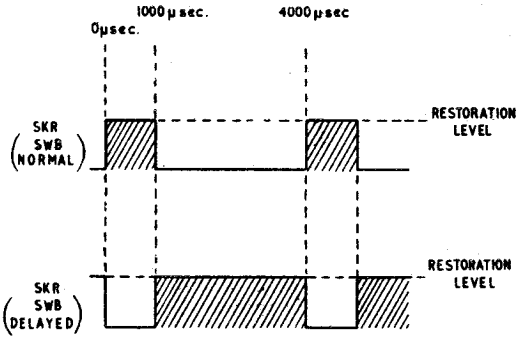


Fig. 3. Normal/delayed pulse production

the cathode potential when cold is approximately −60V, instead of the −250V that would otherwise exist. As the valve approaches its normal working condition and begins to draw current through R27, the potential at the cathode rises towards earth potential, and the current through R26 falls, until at the operating point the current through R26 is negligible, and is insufficient to affect the normal functioning of the circuit. This cathode-protection arrangement is also used on a number of other stages throughout the unit.

25. A second positive-going output pulse is developed across the BLOCK AMP (SKH) potentiometer RV1, in the anode circuit of V3a. This pulse, at an amplitude selected by the position of the potentiometer slider, is fed via the BLOCK ON/OFF switch SWA, to the mixer circuit (*para.* 31).

10 μs pulse generator

26. The 10 μs pulse generator is formed by the two flip-flop circuits V9 and V10, and the cathode follower V11b. The negative-going 0 μs pulse produced at the anode of the trigger pulse inverter, V1b, is coupled via C2 to the grid of V9a, which, with V9b, forms a cathode-coupled flip-flop circuit. V9a is normally conducting due to the potential of approximately +19V applied to its grid from the potential divider network R66, R68, while V9b is cut off. On the arrival of the 0 μs trigger pulse, V9a is cut off, thereby initiating the flip-flop action. The circuit time constant, and therefore the output pulse duration, may be varied by adjustment of the DELAY (SKL) potentiometer RV2. This control determines the potential at the grid of V9b, and thereby the aiming potential of the flip-flop. The range of output pulse duration available by adjustment of the control is from 50 μs to 1500 μs. The diode V20, in the grid circuit of V2b, assists the resetting action, as described in para. 18.

27. The negative-going pulse generated by V9 is differentiated by C18 and R78, resulting in a negative-going peak at 0 μs (produced by the leading edge of the pulse), and a positive-going peak 50 to 1500 μs later (produced by the trailing edge).

28. The differentiated peaks are applied to the grid of V10a, which with V10b forms a cathode-coupled flip-flop circuit. In the quiescent state, V10a is cut off and V10b conducting, therefore the arrival of the negative peak of the differentiated waveform at V10a grid will have no effect. However, on the arrival of the positive peak, V10a conducts and the flip-flop action is initiated.

29. A positive-going pulse with a duration of 10 μs determined by C20, R84, is developed at V10b anode, the time of occurrence of the pulse being adjustable from 50 μs to 1500 μs after the 0 μs trigger pulse. This output pulse is coupled via the cathode follower V11b to the output socket SKS. V11a is unused and its electrodes are connected to earth.

30. A second positive-going pulse is developed at the anode of V10b, and this pulse is coupled to the mixer circuit described below.

Mixer circuit

31. The 10 μs and 1000 μs pulses produced by the pulse generator are coupled via C9 and C10 to the

respective grids of cathode followers V4a and V4b. The 1000 μs pulse is d.c. restored to earth potential by the diode V15. Resistor R37, in the cathode circuit of the diode, serves to protect the diode from voltage surges when the unit is switched on. Restoration of the input to V4a is unnecessary, since the mean value of the 10 μs pulses is not significantly different from earth potential.

32. The positive-going outputs produced at the cathodes of V4a and V4b are applied to the diodes V16 and V17, which are connected to form an OR gate. Thus, pulses applied to either diode cause that diode to conduct, and the pulse is passed to appear across the GAIN (SKH) potentiometer, RV3, which forms the common diode load. However, when pulses occur simultaneously at both diodes, there is no summation at the output of the circuit, since if the pulses are of unequal amplitude, the pulse of greater amplitude will be passed, but its presence at the output will provide a back potential to the other diode which is sufficient to render it non-conducting. Therefore only the pulse of greater amplitude is passed by the circuit. Should the pulses be of equal amplitude, then the output of the circuit will be the same as when only one pulse is present.

33. The output of the mixer circuit is fed via RV3 to the grid of the cathode follower V5a, the potentiometer providing a means of controlling the gain of the output circuit. At the grid of V5a, the positive-going pulse is d.c. restored to earth by the diode V18.

34. V5a is cathode-coupled to the amplifier V5b, and the negative-going output produced at the anode of this valve is d.c. coupled to the grids of the parallel-connected cathode-followers V6b, V7a and V7b. The output of the cathode followers is developed across the common cathode resistor R57, and this output is fed to the output sockets SKP and SKQ.

35. Both a.c. and d.c. negative feedback are used in the output circuit. The a.c. feedback, the purpose of which is to maintain the pulse shape during amplification, is taken from the output of the circuit and coupled via C14 to the grid of the amplifier V5b.

36. The purpose of the d.c. feedback is to maintain the d.c. level of the output pulse. The feedback is obtained through the grounded-grid d.c. amplifier V6a, which is coupled to the output circuit by sharing the cathode resistor R57 in common with the cathode followers. Feedback is taken from the anode of V6a and coupled to the grid of V5b via R49.

37. The a.c. component in the d.c. feedback loop is eliminated by means of the capacitor C13, connected between anode and grid of V6a. By Miller integrator action, this capacitor smooths any a.c. fluctuations that appear at the anode of the valve, so that only long-term variations in d.c. level are passed to V5b.

38. Provision is made for setting the d.c. level of the final output of the circuit at SKP and SKQ by means of the LEVEL (SKH) potentiometer, RV4.

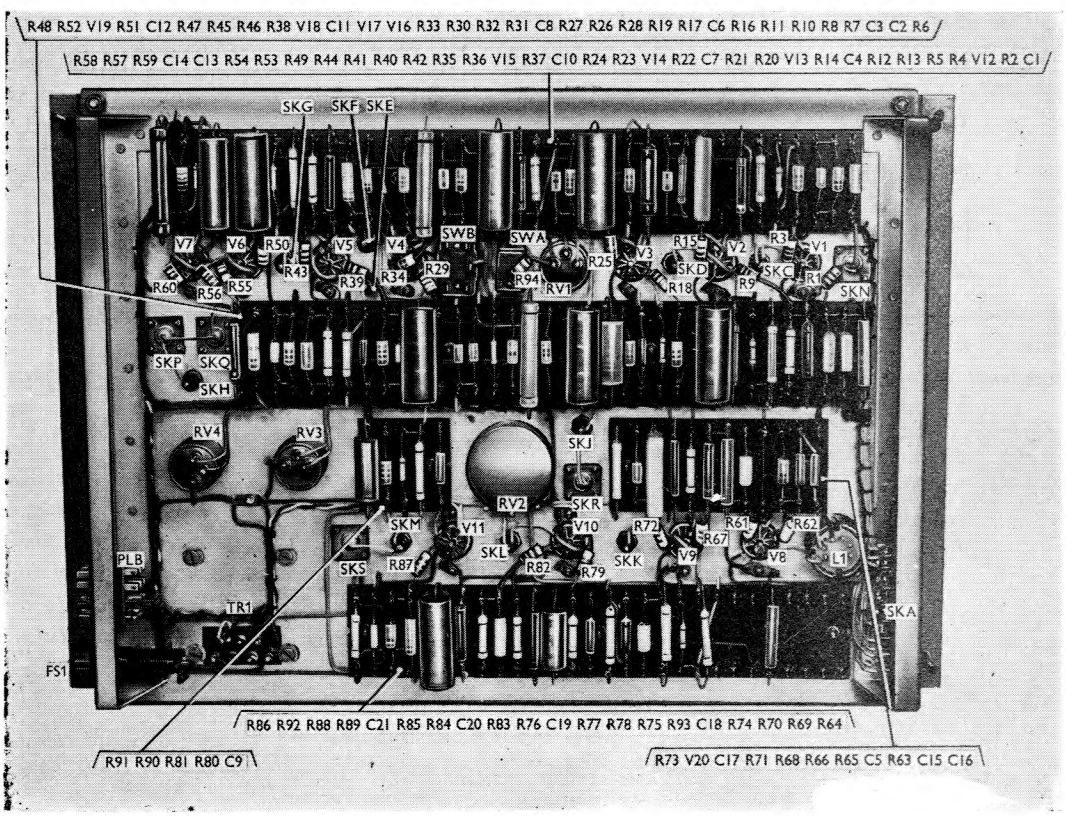


Fig. 4. Signal generator (video) M2 : rear view

(C39786)

This control determines the potential to which the grid of V6a is d.c. restored by the diode V19, and thus the level at which the feedback loop tends to stabilize. The control is adjusted to set the output level to zero, and this may be regarded as the comparator potential to which the voltage on the cathode of V6a is referred. Any change in the d.c. level across R57 causes a corresponding change in the potential difference between cathode and grid of V6a, which results in a compensating change of potential at the anode of the valve. This change is transferred to the grid of V5b, and is in such a direction that it opposes the change that produced it. The output d.c. level at SKP and SKQ is thus held constant at zero (earth) potential.

Monitor test points

39. Monitor test points are provided at sockets SKC–SKM. The waveforms obtainable at these points are illustrated in fig. 5.

Multimeter readings

40. In addition to the monitoring points detailed above, the performance of certain valves within the unit may be checked by connecting a multimeter Type 100 to SKA via a plug-to-socket adaptor. The readings obtained should be as indicated in Table 1.

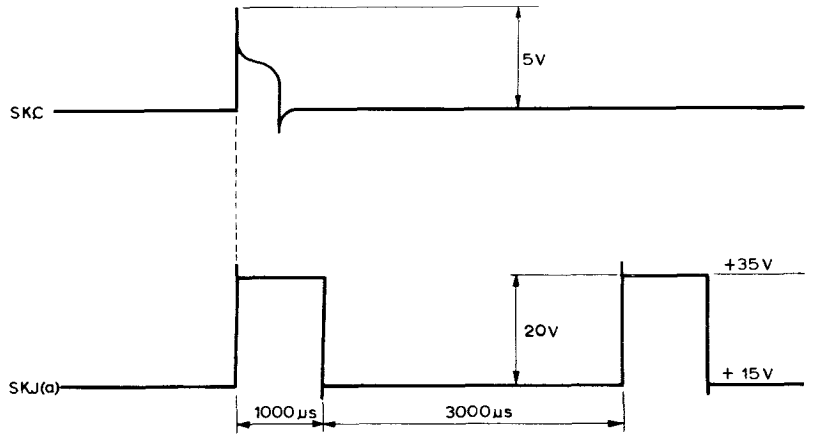
TABLE I

Multimeter readings

Multimeter switch position	Stage monitored	Measured across resistor	Reading	Tolerance
A	V1	R5	0·45	±0·09
B	V9	R70	0·43	±0·09
C	V10	R81	0·42	±0·08
D	V11	R92	0·41	±0·08
E	V2	R11	0·43	±0·09
F	V3b	R28	0·62	±0·12
G	V4	R33	0·54	±0·11
H	V5a	R42	0·44	±0·09
J	V5b	R46	0·61	±0·12
K	V6a	R54	0·42	±0·08
L	V6b, V7	R59	0·41	±0·08
M	V3a	R19	0·49	±0·10

Note . . .

Readings are taken with RV4 set to give zero volts d.c. level at SKH and with no input to SKN.

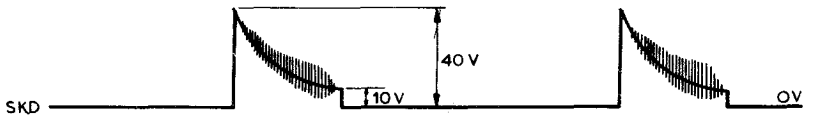


0 µs TIMING PULSE STRETCHED FROM 5 TO 10 µs. TRACE EXPANDED

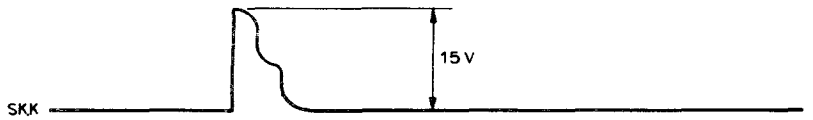
1000 µs - CLUTTER BLOCKS

3000 µs. CLUTTER BLOCKS

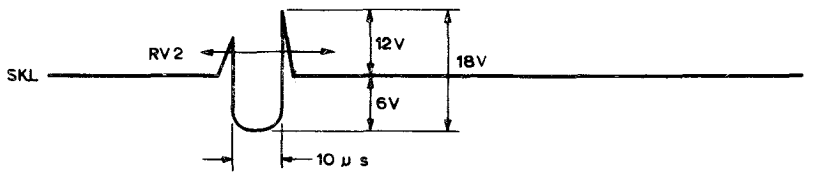
SKJ (a) OR SKJ (b) SELECTED BY SWB. NORMAL/DELAYED



0 µs TIMING PULSE STRETCHED FROM 5 TO 10 µs.



TRACE EXPANDED



TRACE EXPANDED AND RV2 FULLY COUNTER CLOCKWISE

Wt.9110. R.C.1646

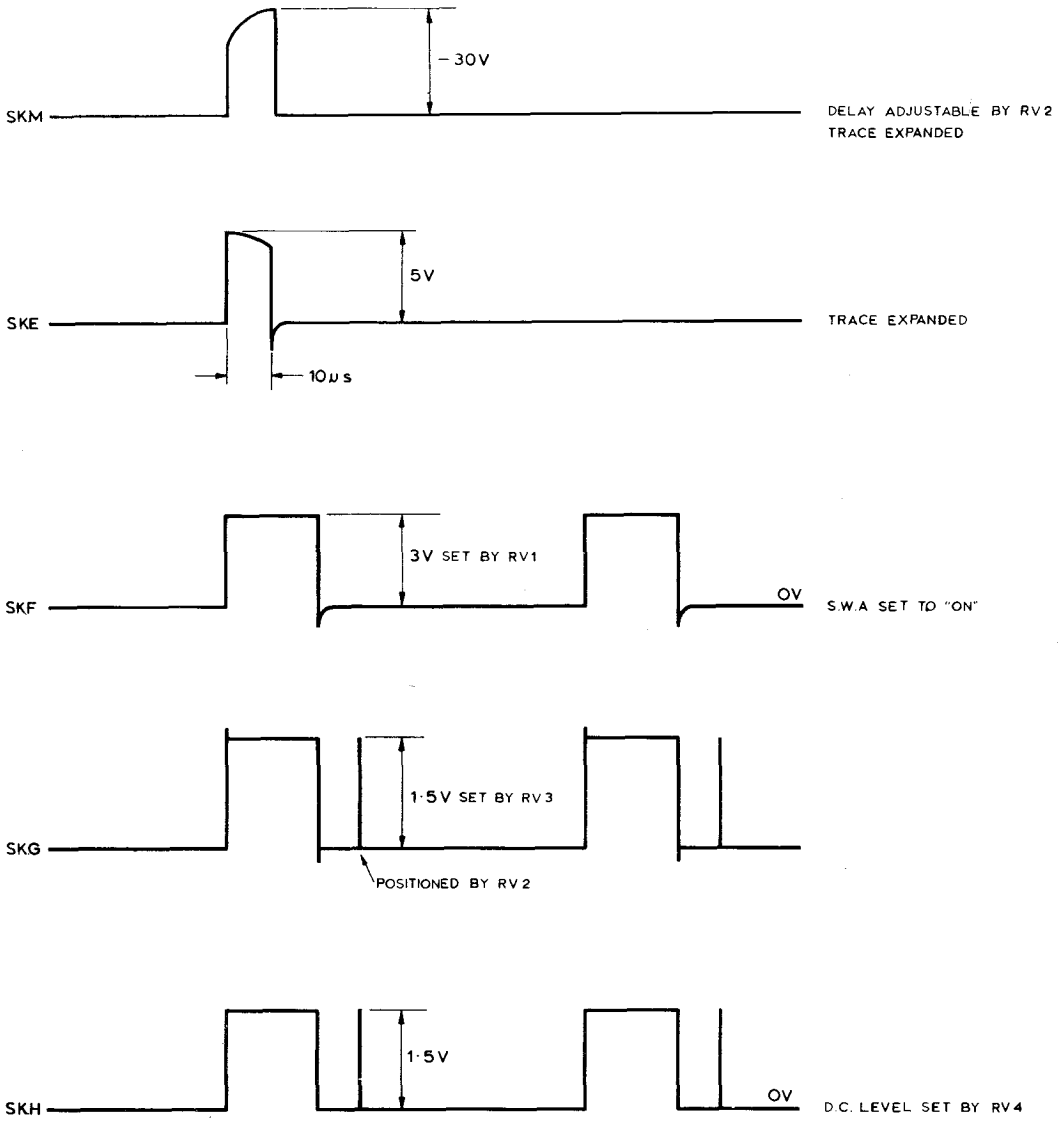


Fig.5 Monitor Point Waveforms

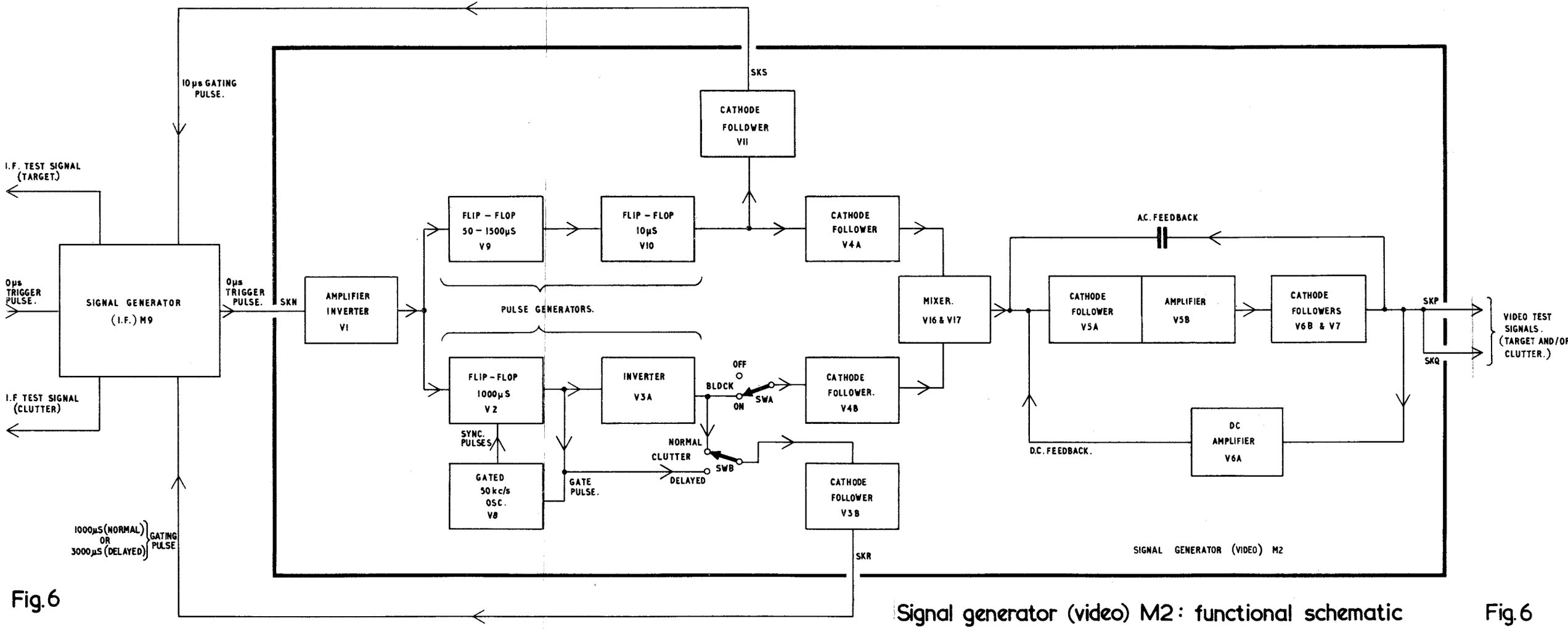


Fig.6

Signal generator (video) M2: functional schematic

Fig.6

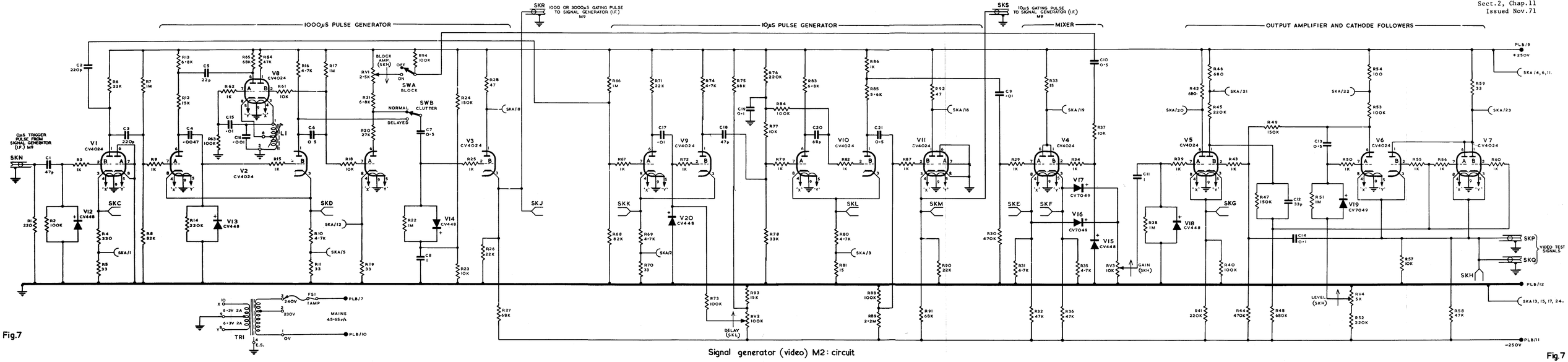


Fig.7

Signal generator (video) M2: circuit

Fig.7

Chapter 12

SIGNAL GENERATOR (I.F.) M9

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

Introduction

1. The signal generator (i.f.) M9 (*fig.* 1 *and* 4) is mounted on frame 3 of the i.f. cabinet. The unit is used to provide the following test signals to the i.f. cabinet :

(1) A signal which is representative of a target return.

(2) A simulated clutter signal.

(3) A simulated impulsive jamming signal.

(4) A lock pulse which is used in place of the transmitter lock pulse during testing.

The signals described in (1) and (2) are only produced when gating pulses from the signal generator (video) M2 (*Chap.* 11). are present.

Performance characteristics

Inputs

2. Socket. SKR receives positive-going pulses of 4 microseconds nominal duration at 15 V amplitude This pulse, which is derived from the p.r.f. system. occurs at 0 microseconds with a nominal p.r.f. of 250 per second.

3. Socket SKT receives positive-going pulses of not less than 20V amplitude (into 3·3 kΩ load) from the video signal generator. The pulse is of 10 microseconds, ± 2 microseconds duration, at a p.r.f. of 250 per second, and occurs at a time between 75 to 1500 microseconds after the 0 microsecond pulse.

4. Socket SKU is fed with a positive-going 1000 microseconds, ± 200 microseconds rectangular pulse from the video signal generator. The pulse starts at 0 microseconds and has a p.r.f. of 250 per second, while the pulse amplitude is not less than 20V (into 3·3 kΩ load). By means of a switch on the video signal generator the pulse may be reversed, starting at 1000 ± 200 μs and ending on the arrival of the next 0 μs pulse, i.e. a duration of 3000 microseconds.

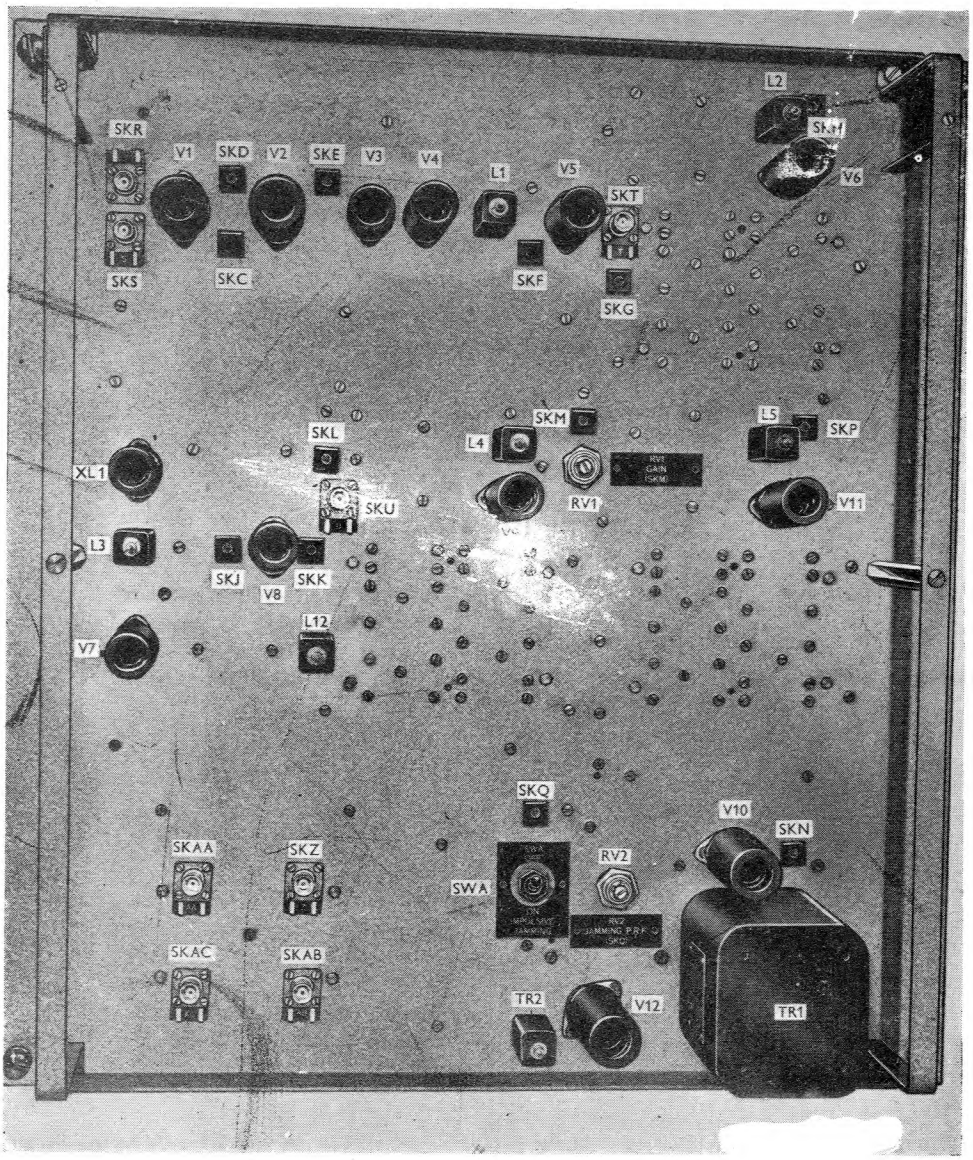


Fig. 1. Signal generator (i.f.) M9 : front view

Outputs

5. The output at SKV consists of a 13·5 Mc/s, 10 microsecond duration pulse at an amplitude of not less than 1·5V peak into 75 ohms. The pulse occurs at a time of from 75 to 1500 microseconds after the 0 microsecond pulse and is used to simulate a response from a moving target.

6. At SKW, the output consists of a 13·5 Mc/s pulse at an amplitude of not less than 1·5V peak into 75 ohms. The pulse duration is either 1000 ±200 microseconds starting at 0 microseconds, or 3000 microseconds, starting at 1000 ±200 microseconds after 0 microseconds. This pulse is used to simulate a clutter response.

7. The output at SKX consists of a 13·5 Mc/s, 9 microsecond, ±2 microsecond duration pulse starting at 0 microseconds, at an amplitude of not less than 1·5V peak into 75 ohms. The pulse is used during testing to replace the transmitter lock pulse.

8. At SKY, the output consists of a 13·5 Mc/s, ±100 kc/s pulse at a duration of 10 microseconds, ±3 microseconds, and amplitude of not less than 1·5V peak into 75 ohms. Since this pulse is used to simulate noise jamming, its p.r.f. is not critical, but is of the order of 1000 to 7500 p.p.s.

Brief circuit description

9. A block diagram of the unit is shown in fig. 2. The circuit consists basically of a 13·5 Mc/s, crystal-controlled Hartley oscillator driving three independent 13·5 Mc/s output amplifier stages, the r.f. signal to each output stage being gated by a video-operated r.f. switch. The r.f. pulse outputs produced by the three stages therefore occur at a duration, p.r.f. and time determined by the characteristics of the gating pulses.

10. Thus, the output at SKV, which is used during testing to simulate a response from a moving target, is gated by a video pulse from the video signal generator. This pulse, of 10 microseconds duration, occurs at a time of from 75 to 1500 microseconds after the occurrence of the transmitter 0 microsecond pulse, and the r.f. pulse produced by the i.f. signal generator therefore has the same characteristics. However the pulse-to-pulse phase relationship of the output pulses is changed by 180° with respect to the phase of the input signal by means of phase splitter and multivibrator circuits within the unit, the multivibrator being triggered by the 0 microseconds pulse from the p.r.f. cabinet.

11. The r.f. pulse produced at SKW is gated by a video pulse produced by the video signal generator and is used to simulate a response from clutter. Two pulse durations are available, one of 1000 microseconds and another of 3000 microseconds. The 1000 microseconds pulse starts at 0 microseconds, while the longer pulse starts 1000 microseconds later. A change from one pulse duration to the other is effected at the video signal generator; but adjustments of the output pulse amplitude are made by means of the GAIN (SKM) potentiometer RV1, this control adjusting the gain of the output amplifier stage.

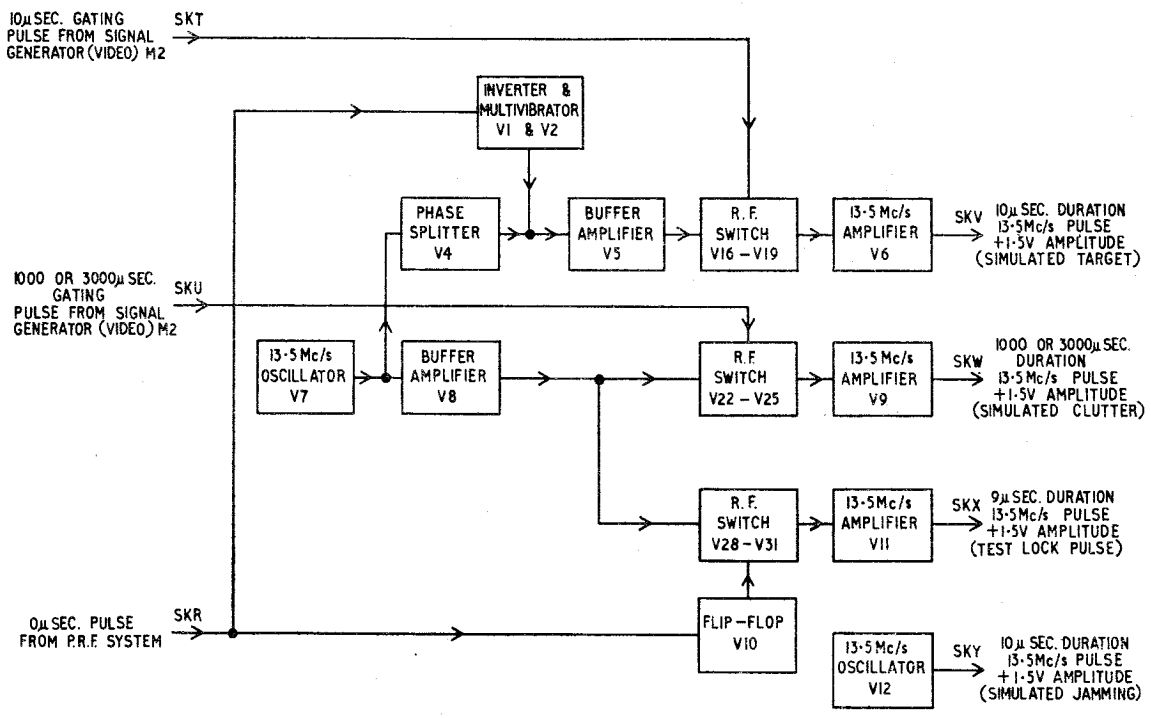


Fig. 2. Block diagram

12. The third output pulse derived from the 13·5 Mc/s oscillator is developed at SKX. This pulse is of 9 microseconds nominal duration, starting at 0 microseconds, and is used during testing to replace the transmitter lock pulse. Unlike the two outputs described previously, the output at SKX is gated by a pulse produced by a flip-flop within the unit, the flip-flop being triggered by the 0 microseconds pulse from the p.r.f. cabinet.

13. A fourth r.f. pulse output is produced by the unit at SKY. This is a pulse representative of impulsive jamming and is produced by a squegging oscillator. The output of the oscillator is ungated, the nominal duration of the pulse produced being 10 microseconds as determined by the natural time constant of the circuit. However, the p.r.f. of the output may be adjusted between 1000 and 7500 p.p.s. by means of the JAMMING P.R.F. control, RV2. Provision is also made, by means of the IMPULSIVE JAMMING ON/OFF switch SWA, for removing the h.t. from the oscillator, thereby allowing the output to be switched off.

14. In operation, only one simulated signal output is taken from the unit, at SKZ. This socket is the output point of a signal mixing network, and in operation the outputs from SKV and SKW are coupled into the network via SKAB and SKAA respectively. Provision is also made for feeding a noise input into the network, via SKAC, the input being derived from the amplifier assembly (noise) M58 (*Chap.* 13).

Circuit description

15. A circuit diagram of the unit is given in fig. 6.

Power supplies

16. The +250V h.t. supply enters the unit at PLB/9 and PLB/12 (earth). The supply to the three output amplifiers V6, V9 and V11 is filtered by C31, C32, L6; C52, C53, L8 and C71, C72, L11 respectively. The −250V supply enters the unit at PLB/11 and PLB/12 (earth).

17. The valve heater supply required by the unit is provided by transformer TR1. The 45–65 c/s mains supply is fed to the primary of the transformer from PLB/10 and PLB/7 (via fuse FS1), producing an output of 6·3V–0–6·3V at the secondary.

Crystal oscillator

18. The 13·5 Mc/s driving signal required by three of the pulse-producing circuits in the unit is derived from the crystal-controlled oscillator circuit formed by V7 and its associated components. The circuit arrangement is basically that of a Hartley oscillator, with the addition of the crystal XL1 in the grid circuit to maintain frequency stability. The 13·5 Mc/s sinewave developed at the anode of V7 is split into two paths, one path feeding the target simulating circuit, while the other path feeds a buffer amplifier stage, V8. A detector circuit formed by the diode V21 and C39 provides a means of monitoring at SKJ the signal produced by V7.

19. The pentode V8 is a conventional buffer amplifier, the output signal being developed across the anode load formed by the tuned circuit L12 and C43. From V8, the signal is again split into two paths, one feeding the clutter simulating circuit and the other feeding the lock pulse circuit. For descriptive purposes each of the three pulse-producing circuits is dealt with separately.

Target simulation circuit

20. The 13·5 Mc/s sinewave from the oscillator is applied to a phase-splitting circuit formed by V4 and its associated components. The anode circuit of this stage consists of a 13·5 Mc/s tuned circuit formed by L1 and C13, with L1 being electrically centre-tapped. The outputs of the valve, taken at opposite ends of L1, therefore consist of anti-phase versions of the input sinewave. These two signals are then coupled via C15 and C16 to a diode switching circuit formed by V13 and V14.

21. The switching circuit operates in conjunction with an equivalent free-running multivibrator circuit formed by V2a and its associated components, the operation of which is synchronized by the 250 p.p.s., 0 microseconds pulse fed in at SKR (or SKS, which is a parallel connection). Before being applied simultaneously to the grids of V2a and V2b, the positive-going pulse is first inverted by V1.

22. The multivibrator time constants are such that the output produced at the anode of either valve occurs at a frequency of 125 c/s. Since these outputs are in anti-phase the circuit can be considered as giving an output pulse of a particular polarity at a frequency of 125 c/s. The diodes V3a and V3b, in the grid circuits of V2a and V2b respectively, are included to improve the recovery time of the multivibrator by preventing either grid from becoming more negative than the potential set by the divider network R6 and R7, i.e. approximately −100V.

23. The anti-phase outputs from the anodes of V2 are d.c. coupled to the cathodes of the switching diodes V13 and V14. The switching sequence is shown in simplified diagrammatic form in fig. 3.

24. Consider the condition whereby V2a is conducting and V2b cut off. In such a case the anode potential of V2a is below h.t. and V13 is conducting via R30 and R31, producing a voltage drop at the common diode anodes. Since V2b is cut off, the cathode of V14 is at h.t. potential, and as the anode potential is less than h.t. the diode is cut off.

25. When the multivibrator changes condition, i.e. V2a cut off and V2b conducting, the diode states are also reversed, so that V14 conducts to give the voltage drop necessary to cut off V13.

26. The time for which a given diode is conducting is determined by the time for which its cathode potential is below h.t. Thus, with a multivibrator period of 8 milliseconds (125 c/s) the diodes will conduct in turn for periods of 4 milliseconds, allowing the 13·5 Mc/s anti-phase outputs of V4 to appear alternately at the diode anodes. The

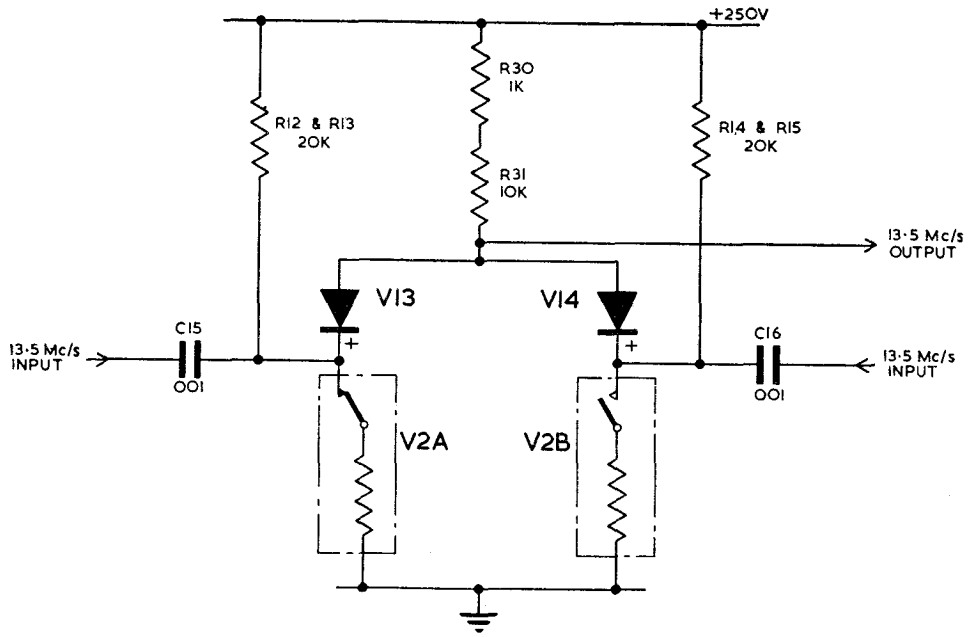


Fig. 3. Multivibrator switching : equivalent circuit

oscillation for each 4 millisecond period is therefore 180° out of phase with that for adjacent periods.

27. The 13·5 Mc/s signal passed by V13 and V14 is applied to the grid of the amplifier stage V5, monitoring facilities being provided by C20 and V15, and the output developed at the anode of the valve is fed to the r.f. switching circuit formed by the diodes V16 to V19 and their associated components.

28. The switching circuit is normally in such a condition (open) that the 13·5 Mc s signal is prevented from passing. When the video switching pulse arrives at SKT, the switch is closed and the r.f. signal is allowed to pass to the final output stage.

29. Consider first the circuit in its open condition. In this condition V16 is cut off, as its cathode is at a potential of approximately +4·4V derived from the divider network R40 and R39, and its anode is maintained at 0V by V17, conducting via R41. V18 is also cut off, since the cathode is at 0V in common with the anode of V17, and its anode is at approximately −4·9V, derived from the divider network formed by R44, R42, R43 and V19. The r.f. signal is therefore prevented from passing through the circuit.

30. On the arrival of the +20V gating pulse at SKT, V19 is cut off, and the anode of V18 rises to approximately +15V, causing the diode to conduct. With V18 conducting, the anode of V16 also rises positively, so that when the anode potential exceeds the cathode potential of +4·4V the diode conducts, thus closing the switch and allowing the 13·5 Mc/s signal to pass through the circuit.

31. The gating pulse is of 10 microseconds duration at 250 p.p.s. Its time of occurrence, however, is variable (within the video signal generator) from 75 to 1500 microseconds after the 0 microsecond pulse. The input to the switching circuit consists of a 13·5 Mc/s sinewave which reverses its phase every 4 milliseconds (250 p.p.s.). The instant of change is coincident with the 0 microsecond pulse, therefore the output of the switching circuit consists of 10 microseconds duration pulses of the 13·5 Mc/s sinewave, each pulse being in anti-phase with adjacent pulses and occurring at 250 p.p.s. The time of occurrence with respect to the 0 microsecond pulse is determined by the gating pulse and lies between 75 and 1500 microseconds.

32. From the r.f. switch, the 13·5 Mc/s pulses are fed to the output amplifier V6. This is a conventional stage of amplification, the output signal being developed across the 13·5 Mc/s tuned circuit formed by L2 and C26. This signal, at a final peak amplitude of 1·5V, is fed to SKV, the output impedance of 75 ohms being determined by the point on L2 at which the output is taken. Monitoring facilities are provided at SKH by means of the detector circuit formed by V20, C30 and R51.

Clutter simulation circuit

33. The circuit which produces the simulated clutter signal comprises a video-operated r.f. switch, incorporating V22 to V25, and an output amplifier stage, V9.

34. The input to the circuit consists of the 13·5 Mc/s sinewave from the buffer amplifier V8. This signal is applied to the r.f. switch, which is identical in circuit and operation to the r.f. switch

already described, the only difference being the characteristics of the video switching pulse. This pulse, which is derived from the video signal generator, is applied at SKU at a maximum amplitude of +20V. The pulse duration may be of 1000 microseconds, starting at a time coincident with the 0 microsecond pulse, or of 3000 microseconds, starting 1000 microseconds after the 0 microsecond pulse. Therefore the r.f. pulse produced at the output of the switching circuit is of the same duration as the video switching pulse.

35. After switching, the r.f. pulse is fed to the output amplifier stage V9, which is similar in operation to V6, except that the gain is adjustable by means of the GAIN (SKM) potentiometer, RV1. This control, with R115, forms a potential divider between the +250V line and earth and adjustment of the control alters the bias potential at the cathode of the valve, and thereby the stage gain. The output is taken from a 75 ohm tapping on L4 which, with C49, forms the anode load of V9 and is tuned to 13·5 Mc/s. This output, at an amplitude of not less than 1·5V peak, is fed to SKW, monitoring facilities being provided at SKM by V27, R79 and C54.

Lock pulse circuit

36. In order to produce an r.f. pulse which may be used in place of the transmitter lock pulse, the 0 microsecond pulse from SKR is used to trigger the cathode-coupled flip-flop circuit formed by V10 and its associated components. The duration of the pulse produced at the anode of V10b is 10 microseconds, determined by R85 and C59, while the repetition rate of 250 p.p.s. is determined by the p.r.f. of the 0 microsecond trigger pulse.

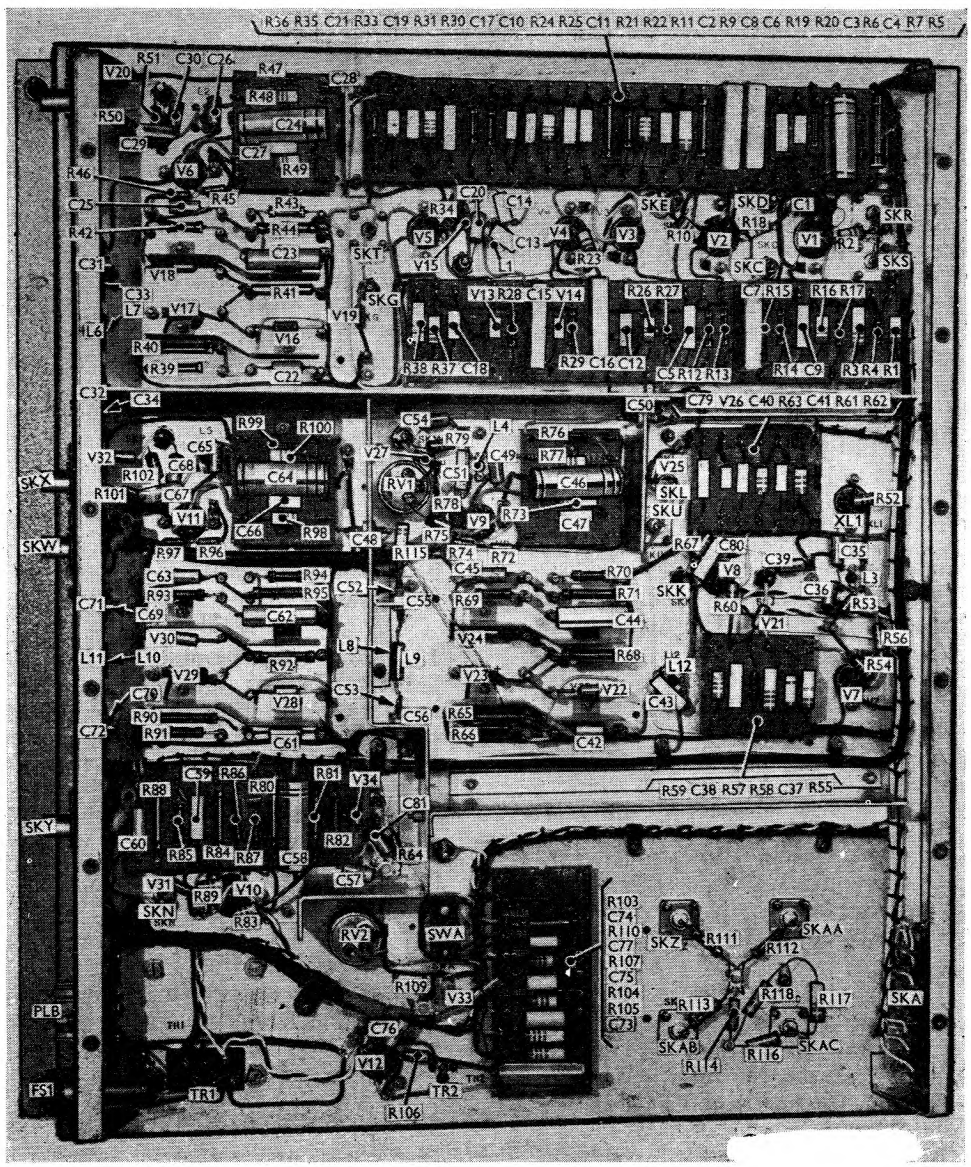


Fig. 4. Signal generator (i.f.) M9 : rear view

37. The 10 microsecond pulse from the flip-flop is used as a switching pulse in the r.f. switch formed by the diodes V28, V29, V30, V31 and their associated components. The switching circuit is identical in operation to the two switching circuits described previously, the input consisting of the 13·5 Mc/s sinewave from V8. The output of the circuit is therefore a 13·5 Mc/s pulse of 10 microseconds duration, occurring at 250 p.p.s. This pulse is fed to the output amplifier stage V11, which is identical in all respects to the circuit comprising V6 (*para.* 32). The output of V11 is developed across the anode tuned circuit L5 and C65 and fed to SKX at a peak amplitude of 1·5V in 75 ohms, monitoring facilities being provided at SKP by the detector circuit comprising V32, C68 and R102.

Jamming simulation circuit

38. The impulsive jamming simulation circuit is completely independent of the rest of the i.f. signal generator circuits in that it does not rely upon an input from the crystal controlled oscillator or require a triggering input.

39. The circuit, as formed by V12a, TR2 and their associated components, is a squegging oscillator. When the noise output is required, the IMPULSIVE JAMMING switch, SWA is set to the ON position, thereby applying h.t. to the anode of V12a and initiating the squegging action. The frequency of oscillation is tuned to 13·5 Mc/s ±100 kc/s by means of the dust-iron core of TR2, while the output p.r.f., or period of oscillation, is determined by the JAMMING P.R.F. (SKQ) control, RV2. This control, which sets the bias potential on the grid of the valve, allows the output p.r.f. to be adjusted to between 1000 and 7500 p.p.s. The circuit time constants are such that the output pulses have a duration of 10 microseconds, ±3 microseconds, and these pulses are fed from the anode of V12a to the output socket, SKY. Facilities for monitoring the output signal are provided at SKQ by the detector circuit formed by V33, C77 and R110.

Matching pad

40. During testing of the signal processing system, the simulated clutter and moving target signals produced at sockets SKV and SKW are coupled into a built-in matching pad via sockets SKAA and SKAB respectively. The moving target signal, however, is first passed through an external variable attenuator assembly, which is mounted in the i.f. cabinet.

41. Socket SKAC on the matching pad receives the output of the amplifier assembly (noise) M58 (*Chap.* 13). The signal is attenuated by 36 dB in the matching pad before mixing with the other input signals and passing to the common output socket, SKZ.

Monitor test points

42. The waveforms which should be available at monitor points SKC to SKQ are as shown in fig. 5.

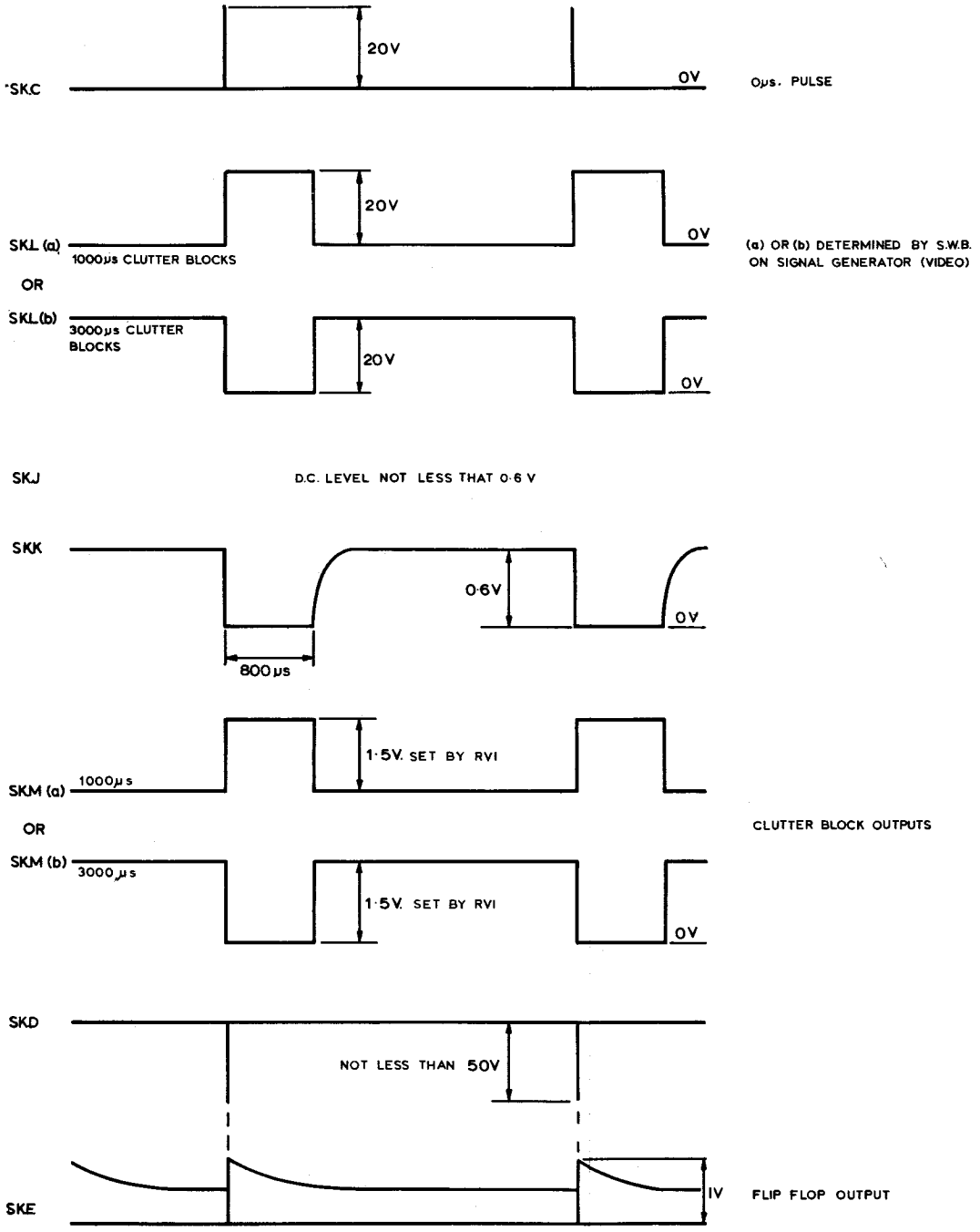
Multimeter readings

43. With multimeter 100 connected to SKA via a plug-to-socket adaptor, the readings obtained should be as given in Table 1.

TABLE 1

Multimeter readings

Switch position	Stage metered	Measured across	Meter reading	Tolerance
A	V1	R4	0·49	±0·10
B	V2a	R17	0·43	±0·09
C	V4	R27	0·42	±0·09
D	V5	R36	0·50	±0·10
E	V6	R47	0·70	±0·14
F	V7	R57	0·50	±0·10
G	V8	R62	0·50	±0·10
H	V9	R76	0·11	±0·02
J	V10	R87	0·55	±0·11
K	V11	R99	0·70	±0·14


SKC
20V
0V
0μs. PULSE
SKL (a)
1000μs CLUTTER BLOCKS
20V
0V
(a) OR (b) DETERMINED BY S.W.B. ON SIGNAL GENERATOR (VIDEO)
OR
SKL (b)
3000μs CLUTTER BLOCKS
20V
0V
SKJ
D.C. LEVEL NOT LESS THAT 0·6 V
SKK
0·6V
0V
800μs
SKM (a)
1000μs
1·5V. SET BY RVI
OR
CLUTTER BLOCK OUTPUTS
SKM (b)
3000μs
1·5V. SET BY RVI
0V
SKD
NOT LESS THAN 50V
SKE
1V
FLIP FLOP OUTPUT

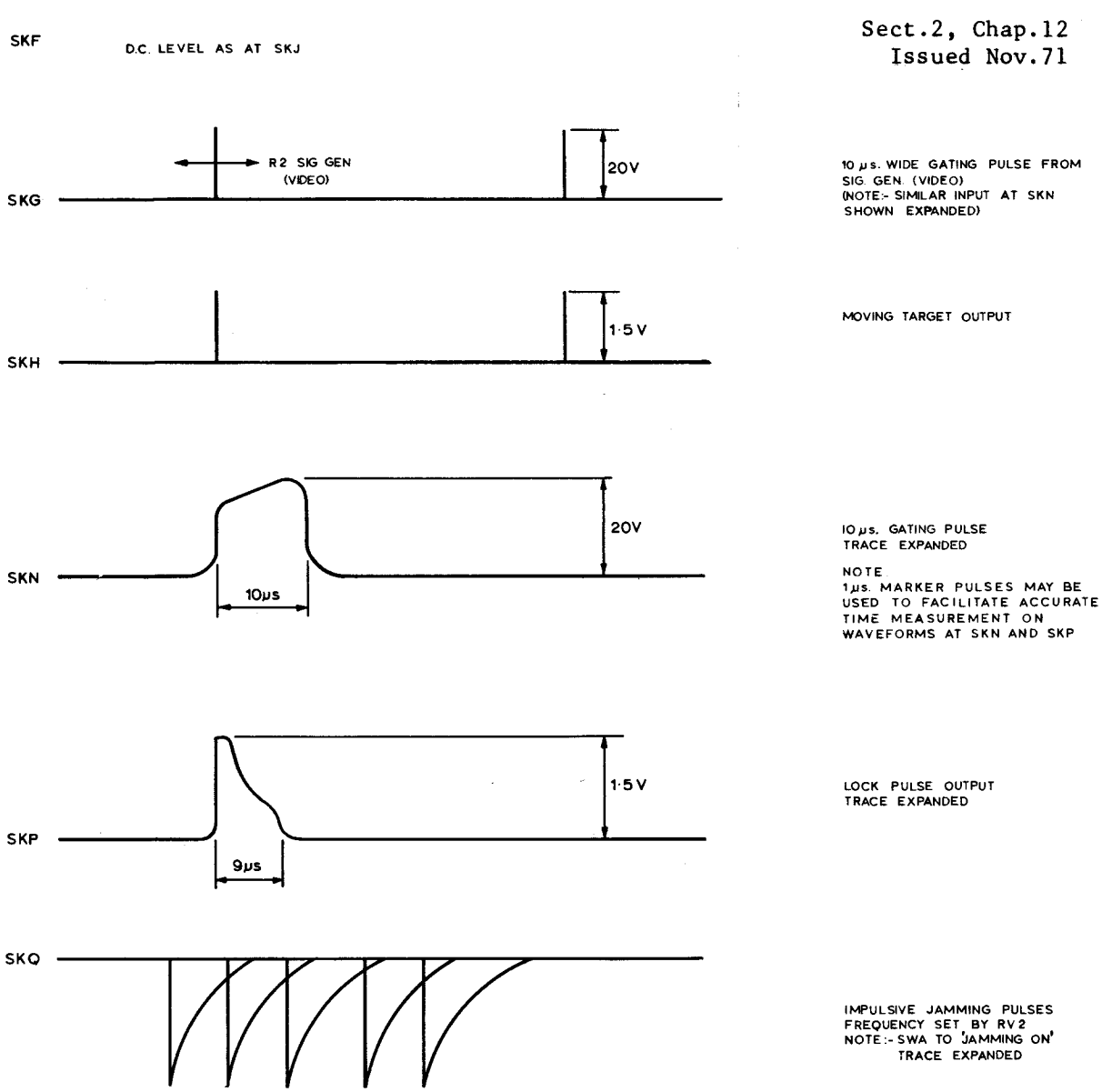
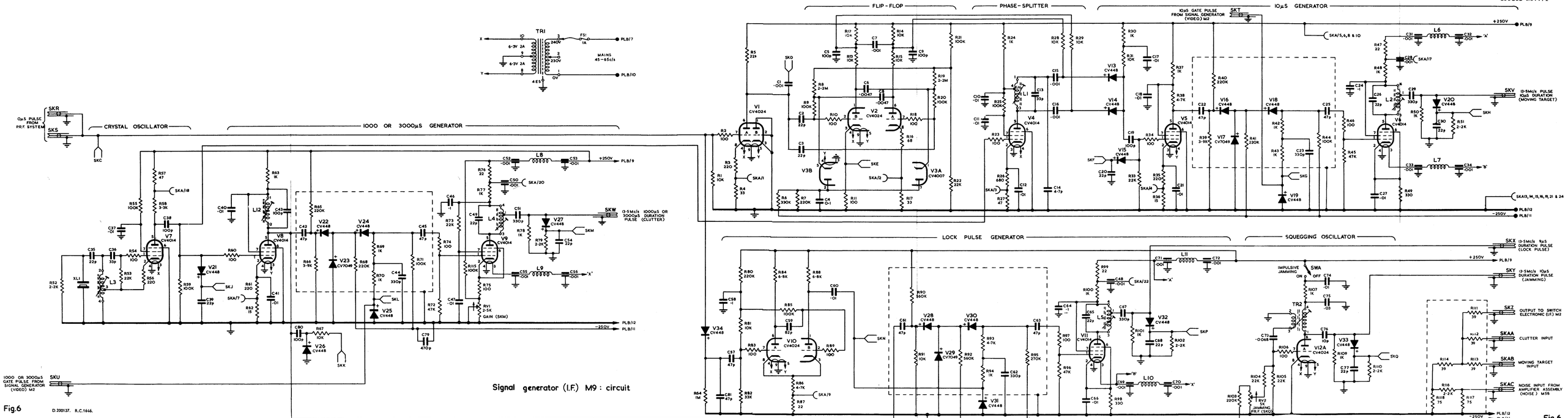


Fig.5 Monitor Point Waveforms



Signal generator (I.F.) M9 : circuit

Fig.6

D.200137. R.C.1666.

Fig.6

Chapter 13

AMPLIFIER ASSEMBLY (NOISE) M58

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

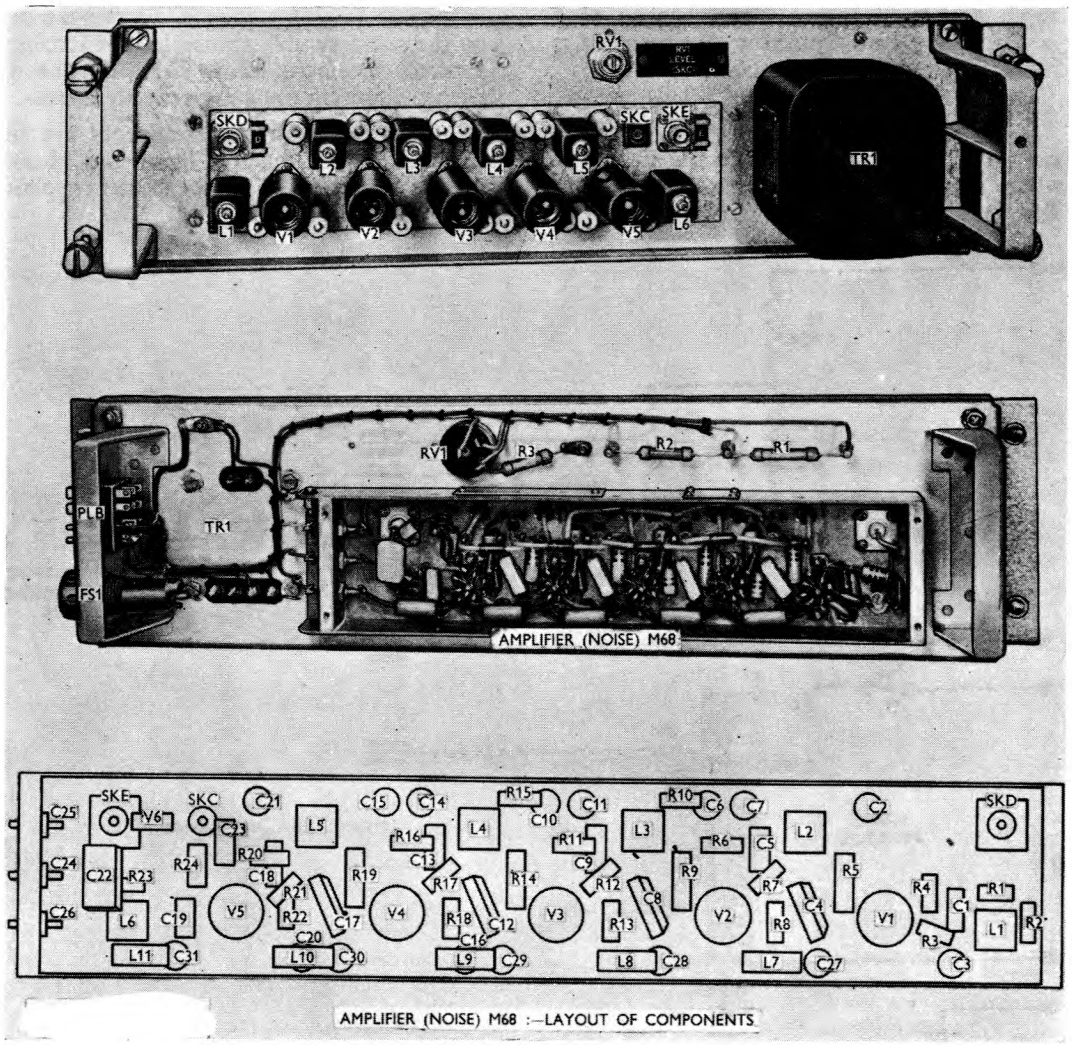


Fig. 1. Amplifier assembly (noise) M58: front and rear views

Introduction

1. The amplifier assembly (noise) M58 (*fig.* 1) forms part of the inbuilt test equipment for the Type 84 radar signal processing equipment and is situated on frame 3 of the i.f. cabinet. The unit consists of a main chassis on which is mounted an interchangeable sub-assembly comprising the noise amplifier M68. Input power connections are brought to the main chassis where a potentiometer, connected across the −250V supply, provides a bias control for the sub-assembly and thus controls the level of output obtained from the assembly. A mains transformer, also on the main chassis, provides a supply to the heaters of all valves in the sub-assembly.

2. The unit provides an output at the intermediate frequency of the i.f. amplifiers in the signal processing system.

Performance characteristics

3. The noise amplifier operates at a centre frequency of 13·5 Kc/s and has a bandwidth at 3 dB points of 600 (±150) Mc/s. The noise output is greater than 200 mV at maximum gain.

Input

4. The input socket SKD provides a means of injecting a 13·5 Mc/s c.w. signal for alignment of the tuned circuits on the sub-assembly.

Output

5. The output from the sub-assembly is delivered at SKE where it is fed to the i.f. signal generator (*Chap.* 12).

Main chassis

6. The power supplies required by the sub-assembly are brought in on PLB on the main chassis (*fig.* 2). The +250V supply enters on PLB/9 and PLB/12 (earth) and is taken straight to the sub-assembly via feed-through capacitor C24. The −250V supply is applied to a potential divider network R1, R2, R3 and RV1 to provide the adjustable bias which is fed to the grids of V2 and V3 on the sub-assembly via the feed-through capacitor C25.

7. The valve heaters supply required by the sub-assembly is produced by the mains transformer TR1, mounted on the main chassis. The primary of the transformer receives the a.c. mains supply from PLB/10 and PLB/7, via FS1, and produces at its secondary 6·3V which is fed to the heaters of the valves on the sub-assembly via the feed-through capacitor C26. The supply to each valve is filtered by the network L7 to L11 and C27 to C31 on the sub-assembly.

Amplifier (noise) M68

Constructional details

8. The noise amplifier M68 is a screened unit fixed to the main chassis by four 4BA cheesehead screws through the main chassis into tapped holes in the sub-assembly chassis. A flanged cover plate on the sub-assembly completes the screening and is secured by eight 8BA cheesehead screws into tapped holes on the sub-assembly chassis.

9. Certain decoupling capacitors are fitted into screening cans integral with the chassis. The method of connection for these capacitors is as shown in Chap. 3.

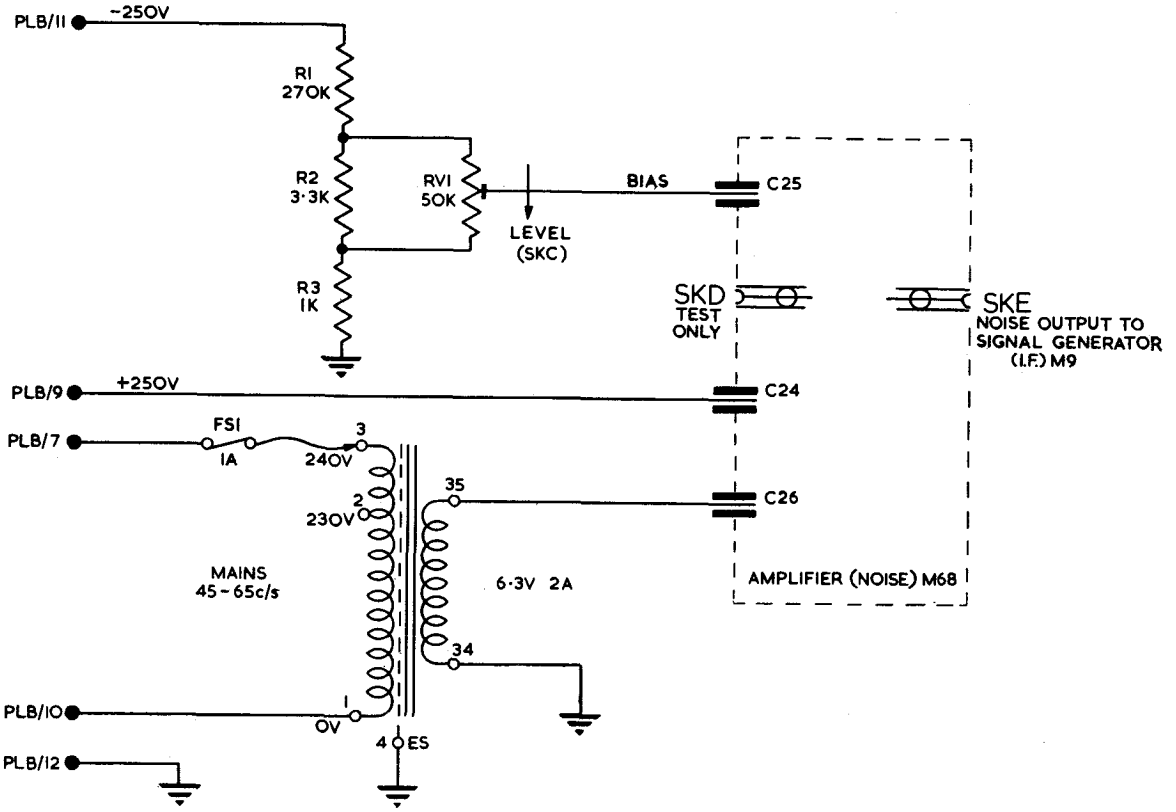


Fig. 2. Amplifier assembly (noise) M58: circuit

Noise amplifier circuit (fig. 3)

10. The amplifier (noise) M68 is a sub-assembly of the amplifier assembly (noise) M58. The circuit comprises a resistor noise source R2, and five similar stages of amplification. SKD is used to inject a c.w. signal for aligning the unit at 13·5 Mc/s, impedance matching for this input being provided by R1.

11. Each amplification stage is tuned to 13·5 Mc/s by an inductor in its grid circuit. An output, which is variable in amplitude, is taken from SKE to the i.f. signal generator. This output is detected by V6, R24 and C23 for monitoring at SKC where the output level is set by means of the LEVEL (SKC) control (RV1 on the main chassis) which alters the grid bias, and hence the gain, of V2 and V3.

Monitor point waveform

12. With RV1 at maximum, the waveform at SKC should consist of not less than 200 mV of noise.

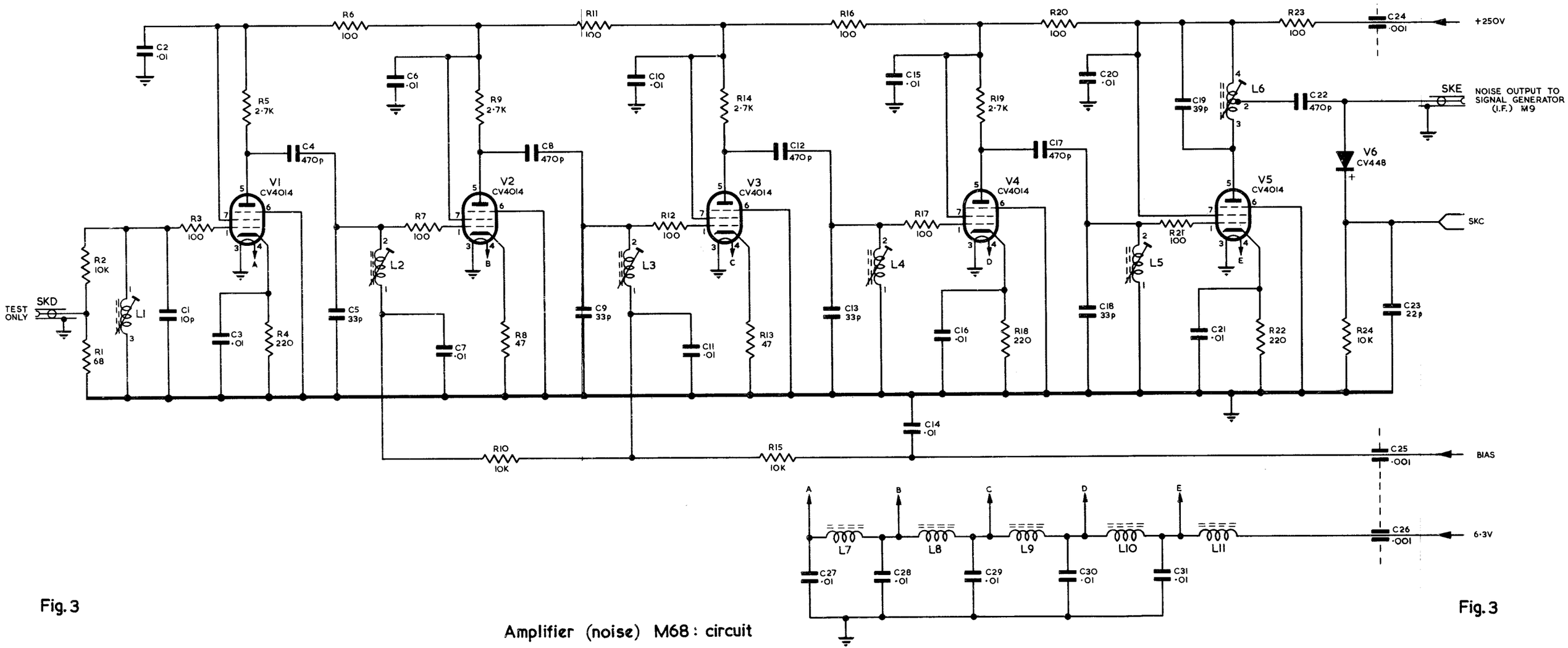


Fig. 3

Amplifier (noise) M68 : circuit

Fig. 3

Chapter 14
DEMODULATOR (LINEAR) M2

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

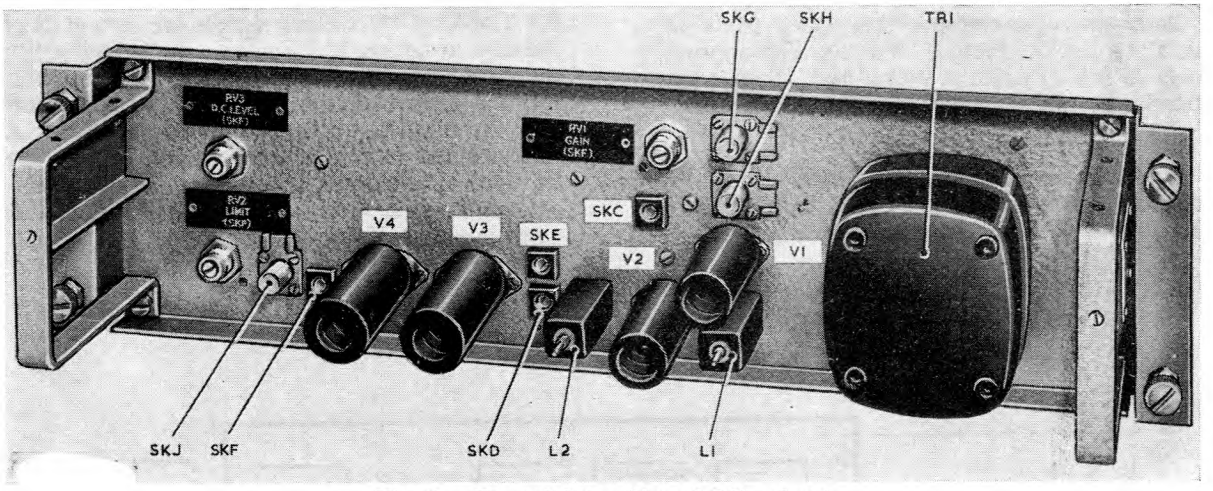


Fig. 1. Demodulator (linear) M2: front

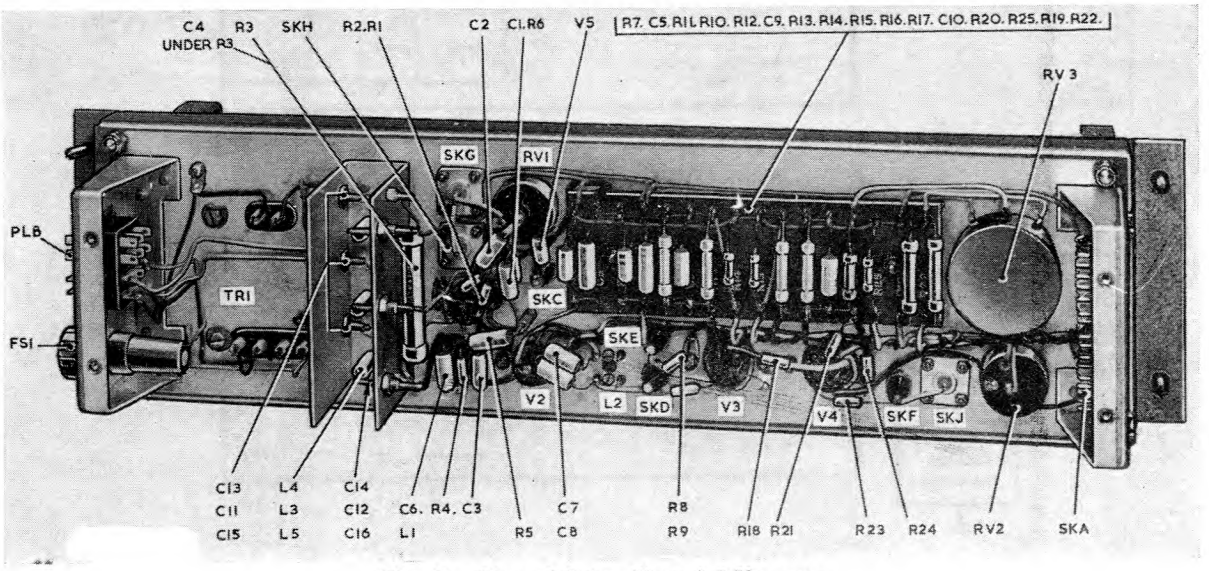


Fig. 2. Demodulator (linear) M2: rear

Introduction

1. The linear demodulator M2 (*fig.* 1 *and* 2) is used in two applications, one being in the i.f. cabinet and the other in the video cabinet (*Sect.* 5). In both applications the units demodulate the 13·5 Mc/s i.f. signals and produce video outputs for application to the video switching circuits.

2. In the i.f. cabinet, the unit is mounted in frame 1 and forms part of the linear (anti-jamming) channel. It receives a 13·5 Mc/s anti-jamming i.f. input (*fig.* 3) from the radar transmitter/receiver via a through-connection in the electronic i.f. switch unit M2 (*Chap.* 2). The video output is fed to relay assembly M2 (*Sect.* 5, *Chap.* 6) in the video cabinet via a 28 microseconds delay network.

3. In the video cabinet, the unit is mounted in frame 3 and forms part of the linear signal channel. It receives a 13·5 Mc/s linear i.f. input from i.f. amplifier assembly (linear) M9 (*Sect.* 5, *Chap.* 8). The video output is fed to relay assembly M3 (*Sect.* 5, *Chap.* 9) via a 26 microseconds delay network M5.

Operating characteristics

Inputs

4. Both the units receive their 13·5 Mc/s i.f. signals at a level of about 0·7V r.m.s. with approximately 70 mV of noise at socket SKG. Socket SKH is terminated in 75 ohms by an external resistor.

Outputs

5. In both applications the video output at socket SKJ is at a level of 1·5V peak on a d.c. level of zero volts. The shoulder noise level is 0·3V.

Brief circuit description

6. The 13·5 Mc/s input signals are first amplified in a single parallel-fed, tuned amplifier stage (V1) and then detected in V2a and passed through a low-pass filter circuit to the video amplifier stage. Automatic gain control of the d.c. amplifier V3 is provided by feedback from the output at SKJ. The level of the output is adjusted by a LIMIT control (RV2) in conjunction with V2b, and the d.c. output level by a D.C. LEVEL control (RV3), which sets the standing bias on the grids of V4.

Circuit description

7. Heater voltages for the valves are supplied from TR1, the 240V a.c. primary supply for the transformer being received via FS1 from PLB/7 and PLB/10. This supply is controlled from the main system switch which controls the mains supply to all units of the complete system.

8. The −250V supply from the power cabinet is brought in at PLB/11 (−250V) and PLB/12 (earth). The +250V supply from the +250V voltage regulator at the top of the frame is brought in at PLB/9 (+250V) and PLB/12 (earth).

9. The 13·5 Mc/s input signals are brought in to the unit at socket SKG and are applied directly to the GAIN (SKF) potentiometer RV1 (*fig.* 5), which forms a gain control for the input amplifier stage V1. An input test point is provided at SKC, which is connected in the rectifier circuit V5, C1, R6; this type of test circuit is used to avoid the need for an oscilloscope with a high-frequency response extending to 13·5 Mc/s.

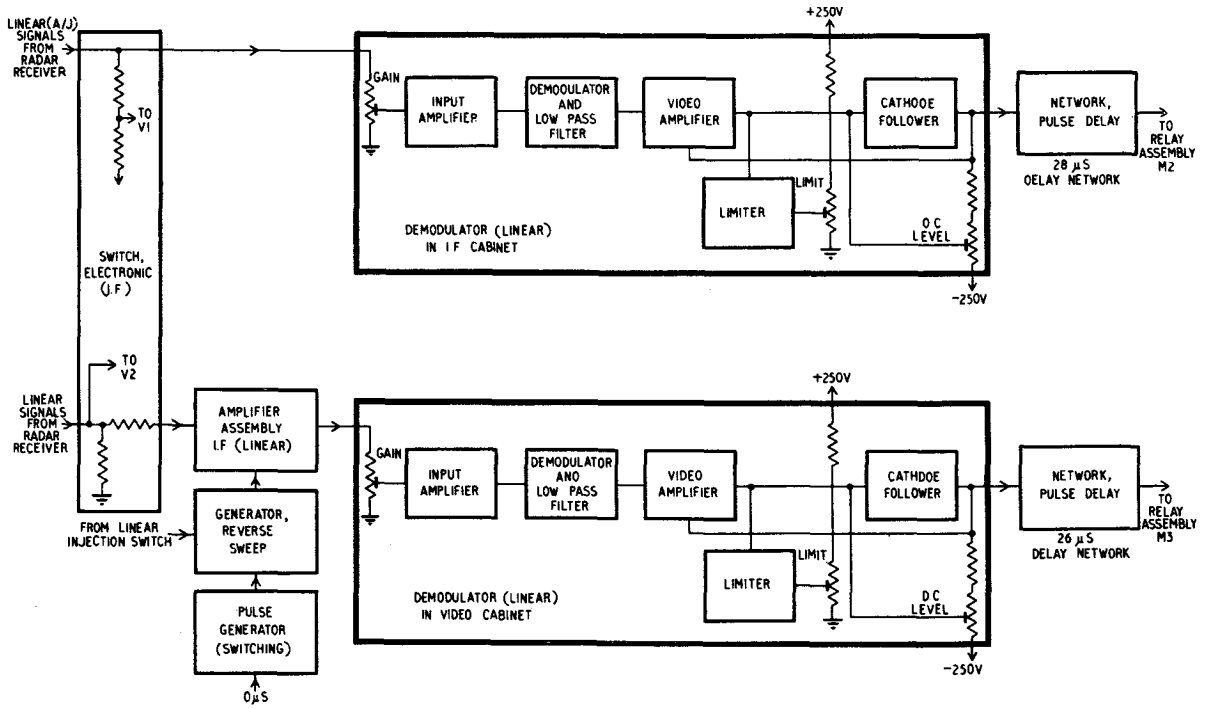


Fig. 3. Block schematic for linear demodulators

10. The amplified signals are developed across the parallel-fed tuned circuit L1–C6 of which L1 is tuned to provide maximum video output at SKJ. Inductor L2 and capacitors C7 and C8 form a low-pass filter with a cut-off frequency of 1 Mc/s so that the 13·5 Mc/s component of the demodulated output from V2a is removed.

11. The video output from the filter is amplified by a unity-gain, high-stability amplifier consisting of V3 and V4. The two halves of the double-triode V3 are connected as a long-tailed pair in which the gain of V3b is controlled by negative feedback from the output at SKJ, so that the gain of the amplifier as a whole is controlled automatically. The video output level is limited at +1·5V with respect to earth by the limiting diode V2b in conjunction with the potential divider R19 and RV2 across the +250V supply. Potentiometer RV2, LIMIT (SKF) is set to give this level of limiting, with a nominal input to the unit, and provide an acceptable signal-to-noise ratio. A variation in ratio of between 3 : 1 and 5 : 1 is normally possible using this control.

12. The output from the cathode follower stage V4 is taken from SKJ, the d.c. level being set by RV3, D.C. LEVEL (SKF) to be zero volts with no input to the unit, or with test socket SKD short-circuited to earth.

13. Decoupling filters (L3, L4 and L5, with their associated capacitors) are provided in the +250V, −250V and 6·3V a.c. supply circuits.

Monitor test points

14. Monitor test points are provided at sockets SKC–SKF. The waveforms obtainable at these points are illustrated in fig. 4.

Multimeter readings

15. In addition to the monitoring points detailed above, the performance of V3 and V4 can be checked by connecting a multimeter Type 100 to socket SKA via a plug-to-socket adapter. The readings obtained with the LIMIT control set fully clockwise and the D.C. LEVEL control set for zero volts d.c. level should be as indicated in Table 1.

TABLE 1

Multimeter readings

With RV2 fully clockwise and RV3 adjusted to give zero volts d.c. level at SKF, the readings should be as stated below.

Multimeter switch position	Stage checked	Measured across resistor	Reading	Tolerance
A	V3a	R14	0·5	±0·1 } i.e. 20 per cent
B	V3b	R15	0·5	±0·1 } i.e. 20 per cent
C	V4	R25	0·5	±0·1 } i.e. 20 per cent

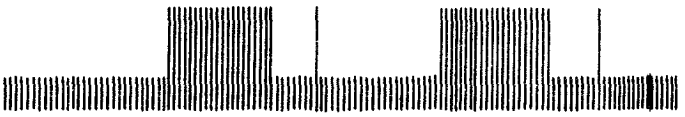
SK.C		TEST INPUT SIGNAL DETECTED AT MONITOR SOCKET. AMPLITUDE SET BY RV1
SK.D	DETECTED WAVEFORM SIMILAR TO SK.C	AMPLITUDE SET BY RV1
SK.E	D.C. AMPLIFIER CATHODE WAVEFORM SIMILAR TO SK.C	AMPLITUDE SET BY RV1
SK.F	VIDEO OUTPUT WAVEFORM SIMILAR TO SK.C D.C. LEVEL AT ZERO, SET BY RV3 (NO INPUT SIGNAL)	SIGNAL LEVEL SET TO 1·5V BY RV2 NOISE LEVEL SET TO 0·5V BY RV1

Fig. 4 Waveforms at monitor points

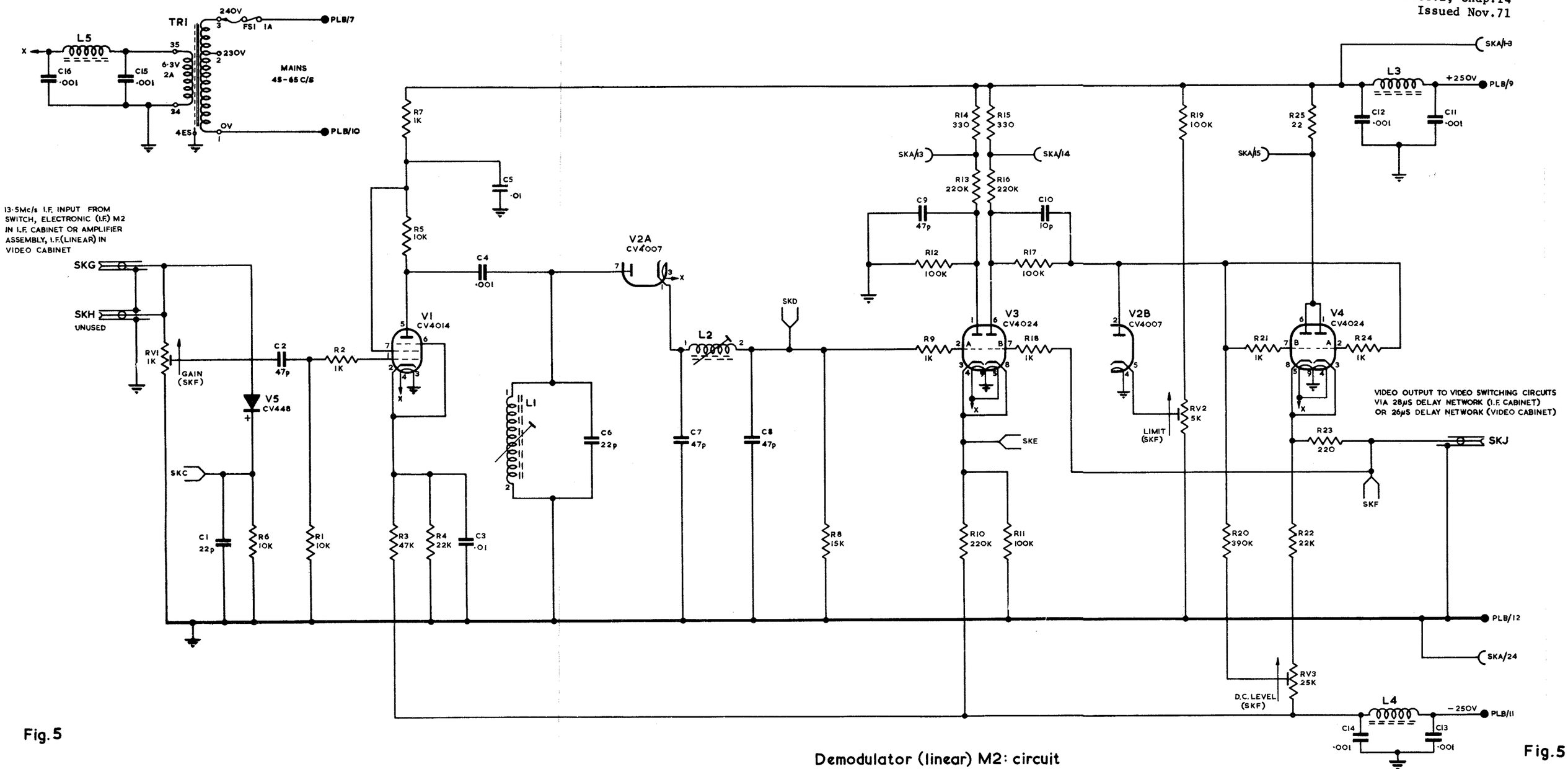


Fig.5

Demodulator (linear) M2: circuit

Fig.5

Chapter 15

OSCILLATOR (COHERENT) M1

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

Introduction

1. The oscillator (coherent) M1 (*fig.* 1 *and* 3) is used to supply a reference signal in the MTI channel. The unit is located in frame 2 of the i.f. cabinet. It produces an i.f. reference signal which is made phase coherent with the transmitter output by a locking pulse. The oscillator is gated into the off condition by a positive-going pre-pulse and re-started by the locking pulse. Provision is made for off-setting the oscillator frequency from the nominal 13·5 Mc/s in order to eliminate the effect of ' blind phases ' which might otherwise occur in the demodulator (coherent) M1 (*Chap.* 10).

2. In the MTI system, echo signals obtained from a transmitter pulse are delayed by a time interval equal to that which occurs between successive transmitter pulses, the returned signals being subtracted from the preceding delayed signals in the cancellation circuits. Prior to the cancellation circuits the returned i.f. signals are detected in a phase sensitive detector, where they are compared with a reference signal, the starting phase of which is coherent with the transmitter lock pulse. It is this reference signal which the coherent oscillator produces and the correct phasing of the signal is achieved by switching off the oscillator for the last 125 microseconds of the pulse repetition period and then restarting it, in the correct phase, with an i.f. lock pulse. The i.f. lock pulse is obtained from the mixer at the transmitter head or, under test conditions, from the signal generator, i.f. M9 (*Chap.* 12), at the time of the transmitter pulse (referred to as time t_0).

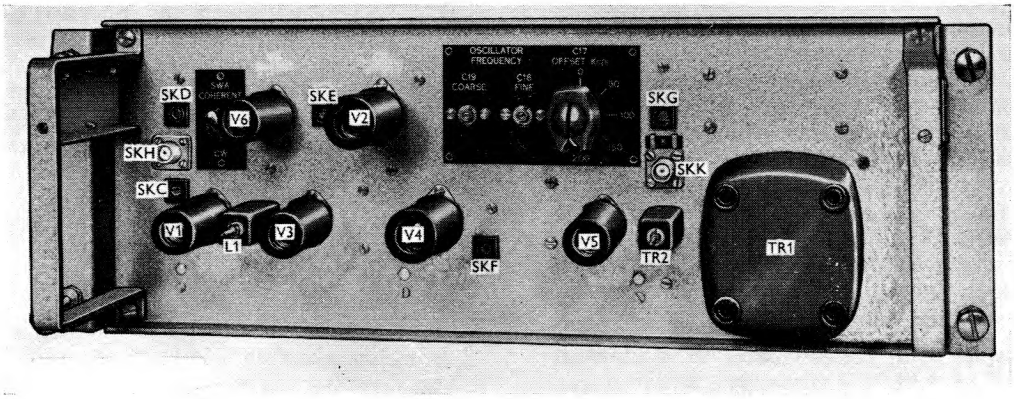


Fig. 1. Oscillator (coherent) M1: front view

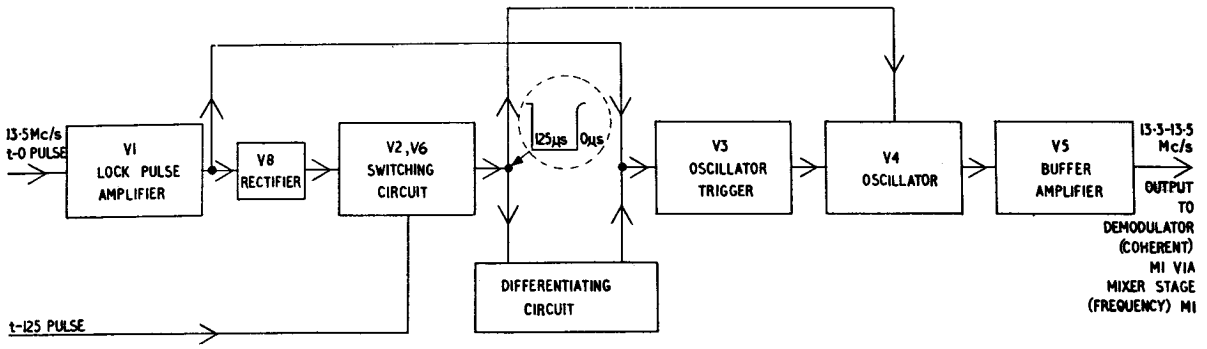


Fig. 2. Oscillator (coherent) M1: block diagram

Performance characteristics

Inputs

3. The unit accepts the following inputs:

(1) SKH. A lock pulse at 13·5 Mc/s from the switch electronic (i.f.) M2.

(2) SKJ. A pre-pulse at time −125 μs from the p.r.f. ~~cabinet SYSTEM~~

Outputs

4. An output i.f. reference signal of 13·3 to 13·5 Mc/s at 2V peak is obtainable at SKK.

Brief circuit description

Note . . .

Throughout the remainder of this chapter the lock pulse will be referred to as occurring at time t_0 and the pre-pulse at time t_{-125}, these being coincident with the transmitter pulse and 125 μs prior to it, respectively.

5. During the major part of the pulse repetition period the circuit is oscillating so that the unit is producing an output. At time t_{-125} the unit receives a positive-going pulse which is applied to the switching circuit, V2 and V6 (*fig.* 2). The result at the output of this stage is the sharp fall in potential of the waveform shown in the inset of fig. 2. This sudden drop in potential is applied to the oscillator valve V4, and stops it oscillating until time t_0 when it is restarted.

6. At time t_0 the lock pulse at 13·5 Mc/s is applied to the lock pulse amplifier V1. One output from this valve is rectified, and the negative-going rectified pulse operates the switching circuit producing the rise in potential at the output of the stage as indicated on the inset waveform. The rise is applied to V4 (the oscillator valve) and is also used to cut-on V3, the oscillator trigger valve, via a differentiating circuit. V3 has, until this time, been held cut-off and the negative-going spike of the differentiated waveform has had no effect on the valve, however the positive-going spike raises the grid potential of the valve, which simultaneously receives a burst of 13·5 Mc/s signal from V1. This sudden burst of oscillation is passed to the oscillator circuit, shock exciting it into phase-coherent oscillation with the transmitter pulse.

7. An output from the oscillator at a nominal frequency of 13·5 Mc/s is taken via a buffer amplifier to the ◀mixer stage (frequency) M1 and▶ demodulator (coherent) M1.

Circuit description (*fig.* 5)

Power supplies

8. Heater supplies for valves V1 to V6 inclusive, at 6·3V 2A, are obtained from the secondary winding of the heater transformer TR1. The primary winding of this transformer is fed with mains at 45–65 c/s from PLB/7 and PLB/10, being fused by FS1.

9. An h.t. supply of +250V is fed to the unit via PLB/9 and PLB/12 (earth) decoupling being provided by the filter network X1 to prevent r.f. feedback to the power supplies. A negative 250V supply is fed in via PLB/11 and PLB/12 (earth) the decoupling being provided by X2.

Oscillator

10. Consider the circuit to be in an oscillatory condition, with SWA in the COHERENT position. Capacitor C9 is charged negatively to a value of approximately −5·5V, which is set by the divider chain R16, R17, so that V2b is non-conducting. At t_{-125} a positive-going pulse is applied to the unit via SKJ. This pulse (which is monitored at SKD) is applied via C5 to the anode of V6b causing the valve to conduct and discharge C9. The grid of V2b is thus brought up to earth potential causing the valve to conduct, the resultant fall in its anode potential is passed to the screen grid of the oscillator valve V4. The fall in screen grid potential of this valve is sufficient to stop it oscillating.

11. At this stage, V3 is held cut-off because its cathode is returned to a positive potential of approximately +9V at the junction of R22 and R23. V3, which shares the oscillator tuned circuit as a common anode load with V4, therefore has no effect on the circuit which remains in the non-oscillatory condition for 125 μs until the lock pulse is received. The incoming lock pulse at SKH is detected by the circuit V7, R1, C1, for monitoring at SKC, and is also applied to the grid of V1, which, with its associated circuit, comprises a tuned r.f. amplifier. One of the two outputs taken from the anode circuit of V1 is rectified by V8 and the resultant negative-going pulse of approximately 50V amplitude is applied to the grid of the cathode follower V2a. The cathode potential of this valve then falls, allowing V6a to conduct and charge C9 negatively to the potential set by R16 and R17. V2b is then cut-off by the negative potential at its grid so that its anode potential, and hence the screen

grid potential of V4 rises. The rise in potential of V2b anode can be regarded as the trailing edge of a negative-going pulse of 125 μs duration. This negative-going pulse produced at V2b anode is differentiated by C10 and the resistive network R15, R18 and R20. The negative spike which results from the differentiation has no effect on V3 as the valve is already cut-off, but the positive spike when applied to the grid causes the valve to conduct. At the same time a second output which is taken from a tapping on L1, in the anode circuit of V1, is applied to V3 grid via C6. This simultaneous application of the 13·5 Mc/s signal and the positive-going differentiated spike to V3 is passed to the tuned oscillator circuit and shocks it into oscillation in the correct phase.

12. The tuned circuit of the modified Colpitts oscillator V4, consisting of L2, C15, C17–C21, and C23, is set to oscillate at 13·5 Mc/s by means of the capacitors C19 and C18 which are COARSE and FINE controls respectively. When the phase of the output is compared with the phase of the 13·5 Mc/s i.f. signals in the phase sensitive detector, no output is obtained from the detector when the phase difference between the two signals is $\pm 90°$. These two phase differences are known as ' blind phases ' and to eliminate their effect the coherent oscillator frequency may be decreased by an amount of up to 200 kc/s by means of the OFF-SET KC/S control C17. The output from the phase sensitive detector then consists of bi-polar video at the difference frequency (100 kc/s) of the i.f. and reference signals. Tuning of the oscillator to 13·5 Mc/s is carried out with C17 set to 0. After tuning C17 is reset to 100 kc/s decreasing the overall frequency to approximately 13·4 Mc/s.

13. With SWA in the CW position, the time t_{-125} pulse is disconnected from the switching circuit of V6 and R8 is connected to the −250V line so that V2a grid is returned, via R7, to a potential of about −33V as set by R8 and R9. This potential will appear at V2a cathode and hence at V6a cathode, thus maintaining V6a in conduction and a negative charge on C9. V2b will therefore remain cut-off and the oscillator will free-run, producing a c.w. output. The incoming lock pulse will have no effect on the oscillator because V3 is cut-off by the positive potential at its cathode.

14. The proportion of the oscillator voltage appearing across C23 is applied to the grid of the buffer amplifier V5, which produces, at the output taken from SKK, a signal of approximately 4V peak to peak amplitude. The peak carrier level of the output is made available for monitoring at SKG by the rectifying circuit V9, C27, R34.

Test point waveforms

15. The waveforms obtainable at the five monitor points with SWA in the COHERENT and CW positions are as shown in fig. 4.

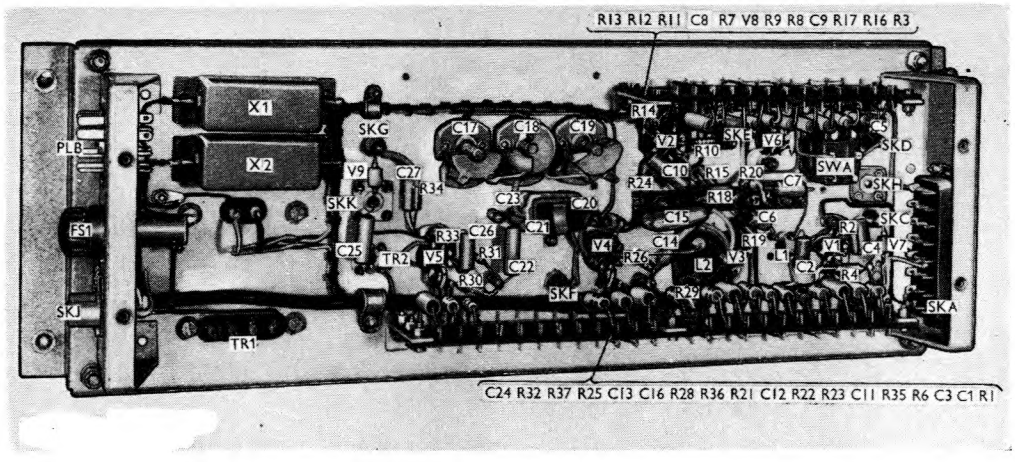
Multimeter readings

16. With a multimeter connected to SKA and the two inputs disconnected the readings obtained with the switch in the CW position should be as indicated in Table 1.

TABLE 1

Multimeter readings

Switch position	Reading	Tolerance	Measured across
1	0·46	20%	R35
2	0·44	20%	R36
3	0·46	20%	R37



(C39254) 61 5 62

Fig. 3. Oscillator (coherent) MI : rear view

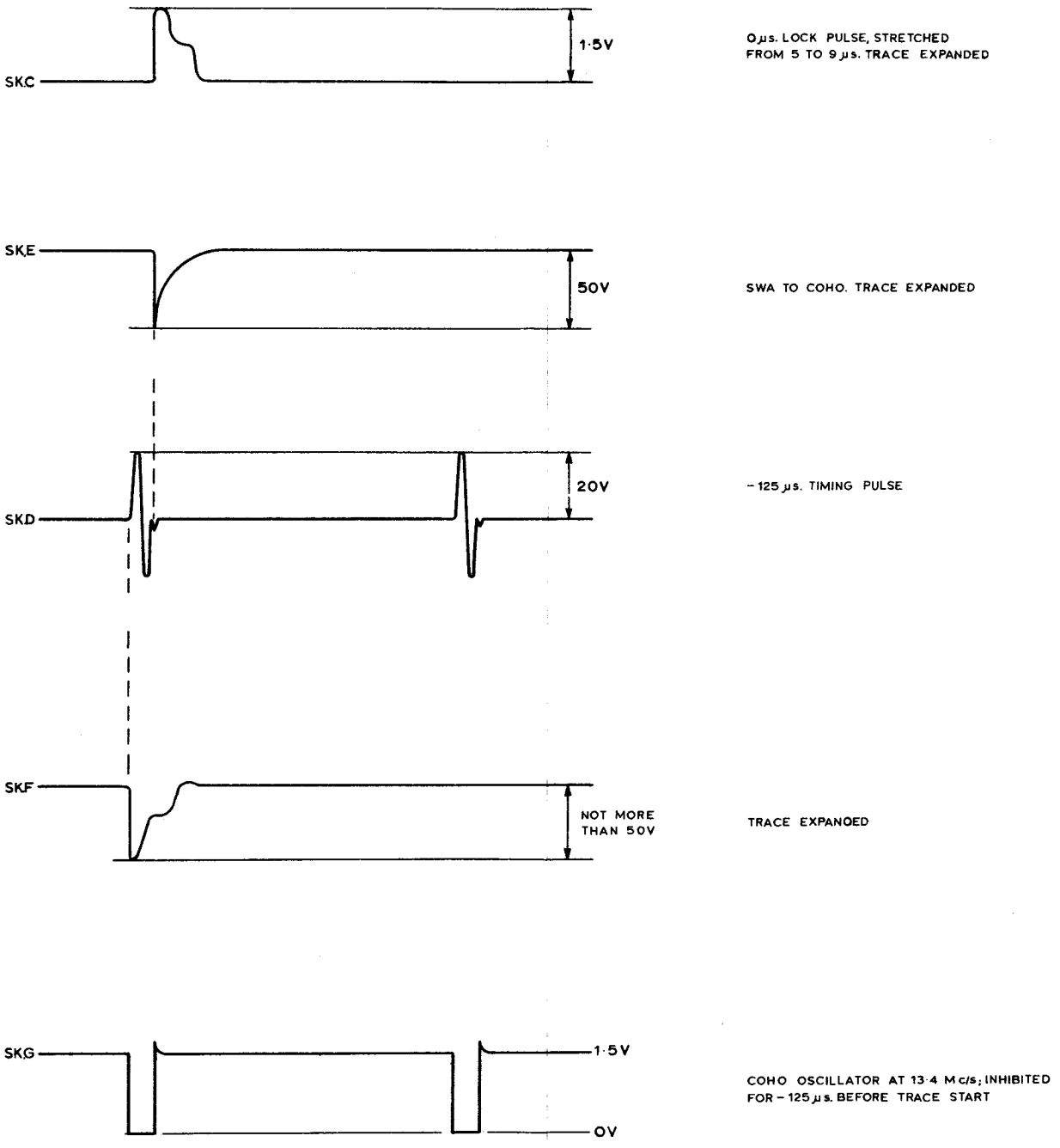


Fig.4 Oscillator (coherent) MI: waveforms.

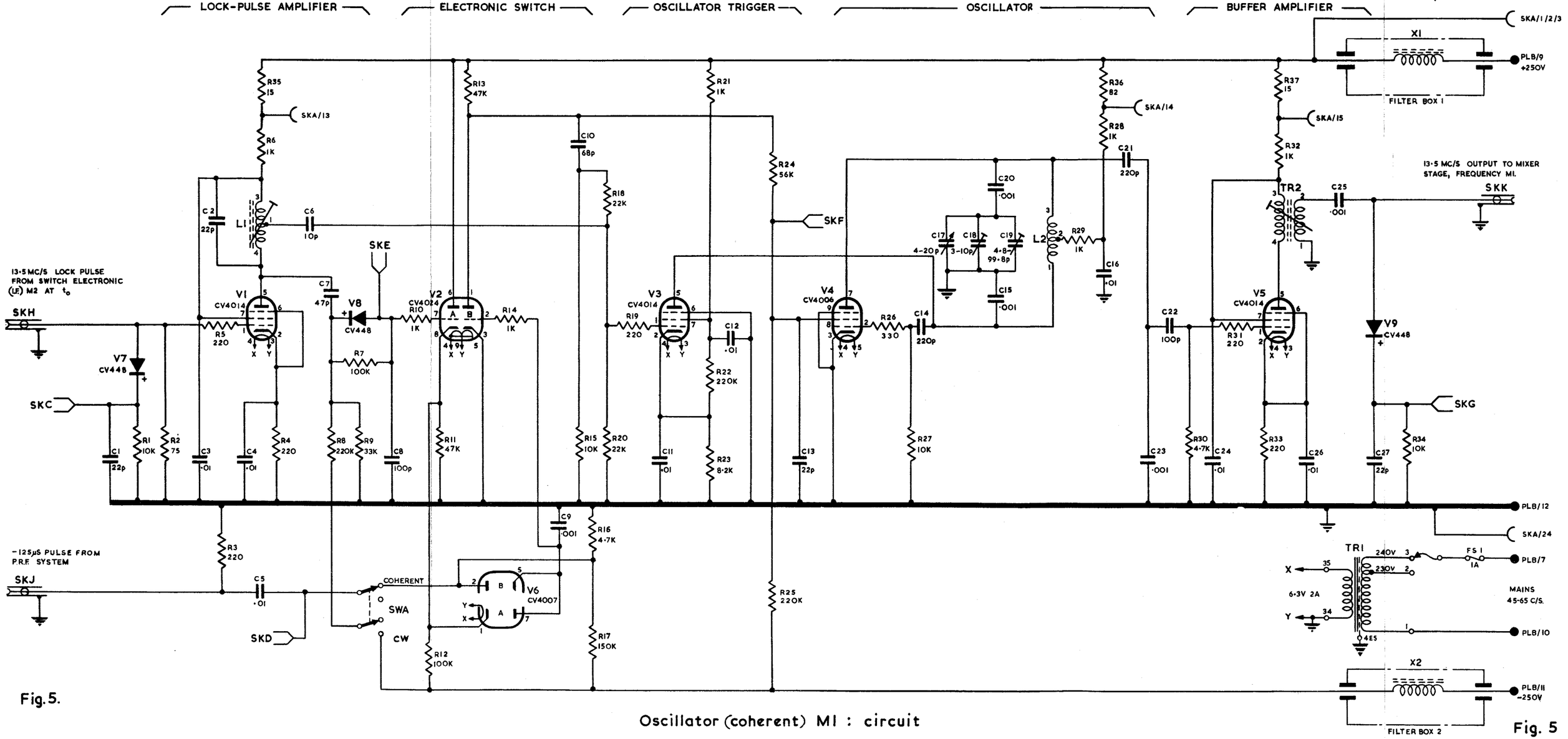


Fig.5.

Oscillator (coherent) M1 : circuit

Fig. 5

Chapter 16

MIXER STAGE (FREQUENCY) M1

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

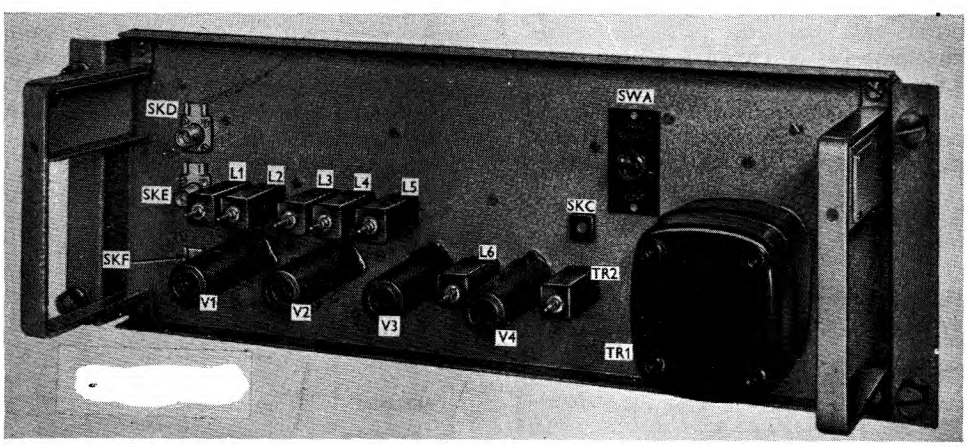


Fig. 1. Mixer stage (frequency) M1 : front view

Introduction

1. There are two mixer stage (frequency) M1 units (*fig.* 1 *and* 3) in the Type 84 radar signal processing system. Both are located in frame 2 of the i.f. cabinet, that for cancellation channel A being at the bottom of the frame and the other, for cancellation channel B, immediately above it. In each application the unit produces a reference signal which is fed to the coherent demodulator (*Chap.* 10) in the appropriate channel.

2. The reference signal is derived by first subtracting the output from one of two electronic reference frequency switches (*Sect.* 4, *Chap.* 8) from that of the coherent oscillator (*Chap.* 15) and then adding the resultant to the output from the fixed

reference frequency oscillator (*Sect.* 4, *Chap.* 9). The latter signal is received via a reference frequency distribution panel (*Sect.* 4, *Chap.* 10).

3. The nominal frequency of the input from the coherent oscillator is 13·5 Mc/s, but this may be reduced by 100 kc/s to incorporate the coherent low i.f. facility (*Sect.* 1, *Chap.* 1). The frequency of the input from the electronic reference frequency switch may be either a fixed frequency of a nominal 5·251 Mc/s (5·25 Mc/s plus 4 × p.r.f.) in non-doppler compensated areas, or a nominal frequency of 5·25 Mc/s which is controlled within the limits of plus and minus 2 × p.r.f. (about 500 c/s) according to the amount of doppler compensation applied. The doppler compensation system is described in Sect. 1, Chap. 5.

4. In non-doppler compensated areas the inputs from the reference frequency switch and the fixed reference frequency oscillator are at the same frequency, so that the output from the mixer stage frequency unit is at the frequency of the input from the coherent oscillator. When doppler compensation is in use, the doppler component f_d is introduced at the first stage of mixing, the output from which is at a frequency determined by the expression: $f_{coho} - 5{\cdot}25$ Mc/s $\pm f_d$ where f_{coho} is the frequency of the coherent oscillator input. The output from the second mixer stage is then given by:

$$f_{coho} - 5{\cdot}25 \text{ Mc/s} \pm f_d + 5{\cdot}251 \text{ Mc/s}$$

or f_{coho} + 1 kc/s $\pm f_d$ (for a p.r.f. of 250 c/s). The basic difference frequency of 1 kc/s is selected as suitable for the mid-frequency in the frequency discriminators in the electrical frequency control units (*Sect.* 4, *Chap.* 11) and corresponds to the fourth blind velocity.

5. The two frequency mixer stage units are identical in circuit and operation. The difference between the two cancellation channels is that doppler compensation is not used in channel A for the local clutter area (the circle) whereas doppler is used in channel B, where a rectangle is positioned so as to overlap the circle. Channel A therefore cancels fixed echoes and channel B cancels moving clutter in this area.

Performance characteristics

Inputs

6. (1) SKD (channel B).
13·5 Mc/s at 2V peak amplitude from the oscillator (coherent) M1.
SKD (channel A).
As channel B but received via the mixer stage (frequency) M1 for channel B.

(2) SKF (both channels).
5·25 Mc/s nominal at 2·5V peak amplitude from respective channel A and B switch electronic (ref. freq.) M4 units in the doppler cabinet.

(3) SKG (both channels).
5·251 Mc/s at 5V peak amplitude from the panel distribution (ref. freq.) M2 unit in the doppler cabinet.

Outputs

7. (1) SKH (both channels).
13·501 Mc/s nominal at an amplitude greater than 4V peak to the respective channel A and B demodulator (coherent) M1 unit.

(2) SKE (channel B).
This socket is used to feed the input from the coherent oscillator to the mixer stage (frequency) M1 for channel A.

(3) SKE (channel A).
This socket is not used. This output is fed into a 75-ohm terminating connector.

Brief circuit description

8. Each unit (*fig.* 2) consists of two mixer circuits followed by an amplifier and an output stage. The first mixer accepts a nominal 13·5 Mc/s i.f. signal from the coherent oscillator and a 5·25 Mc/s i.f. signal, with doppler compensation, from the reference frequency switch unit in the doppler

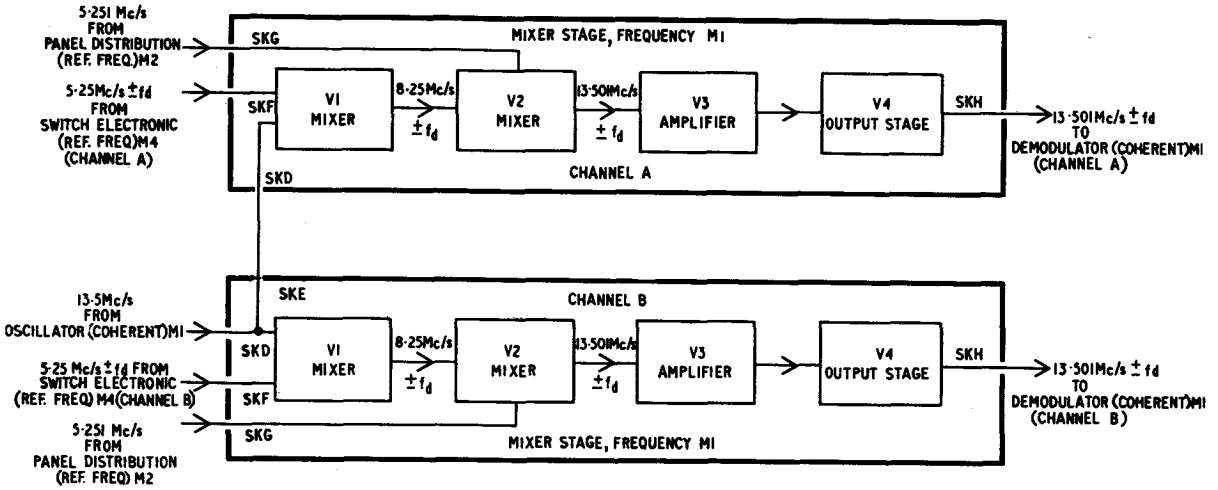


Fig. 2. Mixer stage (frequency) MI : block schematic

cabinet. From these the difference frequency of 8·25 Mc/s is produced. The second mixer accepts this difference frequency together with a nominal 5·25 Mc/s frequency from the fixed reference oscillator in the doppler cabinet and produces the sum frequency of 13·501 Mc/s.

9. The output of the second mixer is amplified and fed out of the unit to the coherent demodulator as the reference signal with which the phase of incoming signals is compared.

Circuit description (*fig.* 4)

Power supplies

10. The a.c. mains supply to the fused primary of the valve heater transformer, TR1, is routed via PLB/7 and PLB/10. Power at these points is controlled by the main system switch for all units of the system. The transformer produces 6·3V at 2A from its secondary for the heaters of V1 to V4.

11. An h.t. supply of +250V d.c. is fed into the unit on PLB/9 and PLB/12 (earth). Filtering in the h.t. line is provided by X1. The TUNE/NORMAL switch, SWA, introduces a resistor R30 into the supply to the screens of the mixer valves (V1 and V2) to facilitate tuning while the unit is operational. The reduced screen supply effectively reduces the gain of the two valves.

Mixing stages

12. Two mixing stages are employed to introduce doppler compensation into the i.f. 13·5 Mc/s reference signal. The first mixer, V1, produces the difference frequency between the 13·5 Mc/s i.f. reference signal and the doppler compensated 5·25 Mc/s reference frequency. The second mixer, V2, produces the sum frequency of this difference with a further reference signal of 5·251 Mc/s.

13. Pentagrid valves are used for the two mixing stages. The use of a pentode valve for suppressor grid modulation suffers from the disadvantage that the anode resistance approximates to that of a triode valve rather than the normally high value of a pentode. This disadvantage is overcome in the pentagrid valve which introduces an additional screen grid, operated at the same potential as the first screen grid, and an additional suppressor grid, connected to the cathode. As well as providing an output characteristic corresponding to that of a pentode, the pentagrid has an additional advantage of eliminating coupling between the two modulated signals to a greater degree than in a pentode.

14. A 13·5 Mc/s i.f. signal from the oscillator (coherent) M1 is brought into the unit at SKD. The input is taken to grid 3 of V1 via an input circuit tuned to 13·5 Mc/s by L1. A further signal at a nominal frequency of 5·25 Mc/s, but with doppler compensation up to a maximum ±500 c/s, is brought into the unit at SKF from the switch electronic (ref. freq.) M4, and applied to grid 1 of V1. The output taken from the anode of the valve is tuned to the difference frequency of 8·25 Mc/s by L2 and C7.

15. In order to eliminate the unwanted components of the mixed frequencies the output from V1 is applied to a capacitor voltage divider circuit, C6 and C7, which passes a small percentage of the output, thus reducing any unwanted frequencies which are present to a negligible amount (only a small-amplitude signal is required for mixing in the following stage). C6 also provides coupling between the two resonant circuits L2-C7 and L3-C8. Current circulating in L2, C7 flows through the common coupling element, C6, and the voltage developed across this element causes current to flow in L3, C8, which forms the input circuit to the second mixer stage.

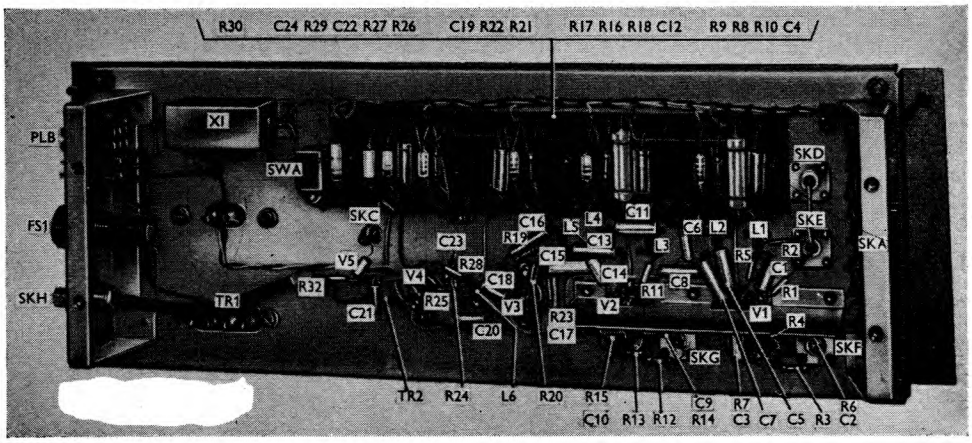


Fig. 3. Mixer stage (frequency) M1 : rear view

16. A reference signal at 5·251 Mc/s from the panel distribution (ref. freq.) M2 is applied to the grid circuit of V2 via SKG. This signal is mixed with the difference frequency produced by V1, and the output is tuned to the addition frequency of these two by the resonant circuit formed by L4-C13. Coupling between this resonant circuit and the resonant circuit formed by L5-C16 is effected by C14, the latter circuit forming the input to the following amplification stage, V3.

Amplifier and output stage

17. The reference signal produced at the output of the two mixing stages is further amplified by V3 and by V4, the output valve. The anode circuits of both valves are tuned, to eliminate unwanted frequencies. A transformer coupling is used in the anode of V4 to feed the output to the demodulator (coherent) M1, via SKH. A detector circuit in the output, formed by V5, R29 and C24 enables the envelope of the output signal to be monitored at SKC.

Test point waveform

18. The waveform obtainable at monitor point SKC is a positive-going square wave of duration 3·875 ms with an amplitude of greater than 4V peak at a p.r.f. of 250 per second.

Multimeter readings

19. With a multimeter connected to SKA and SWA set to NORMAL the readings obtained under operational conditions should be as indicated in Table 1.

TABLE I

Multimeter readings

Switch position	Reading	Tolerance	Measured across
A	0·48	±0·1	R8
B	0·48	±0·1	R16
C	0·44	±0·09	R21
D	0·44	±0·09	R26

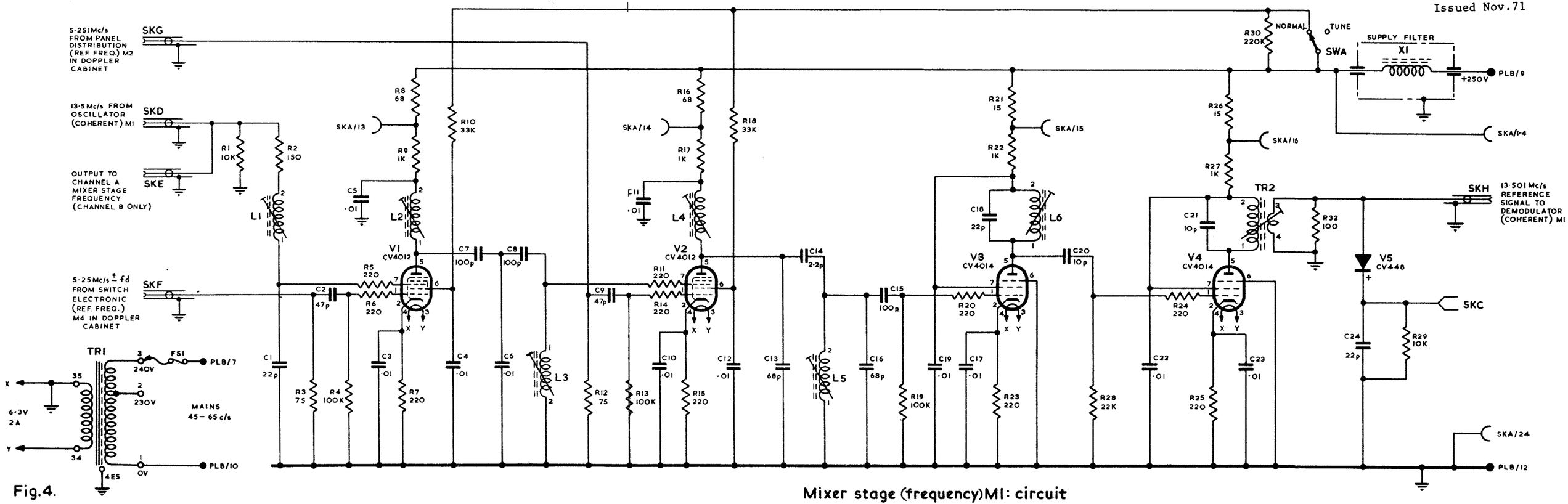


Fig.4. Mixer stage (frequency)M1: circuit

Chapter 17

VOLTAGE REGULATOR (+250V) M2

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

Introduction

1. The purpose of the regulator unit (*fig.*1) is to produce a +250V regulated supply from a +450V d.c. input. It also acts as a distribution point for +450V, −250V, −50V d.c. and the a.c. mains supply to units contained within the associated frame. In the regulator unit the −250V and +250V outputs act as hold voltages for two relays which, when de-energized, due to failure of the +450V or −250V supplies, close the circuits of three fault lamps to give visual indication of which frame, within the cabinet, has failed.

2. Twelve of these units are used in the signal processing equipment and are located in the following cabinets :

Cancellation cabinet	Frame 1,2,3
Video cabinet	Frame 1,2,3
I.F. cabinet	Frame 1,2,3
Doppler cabinet	Frame 1,2,3

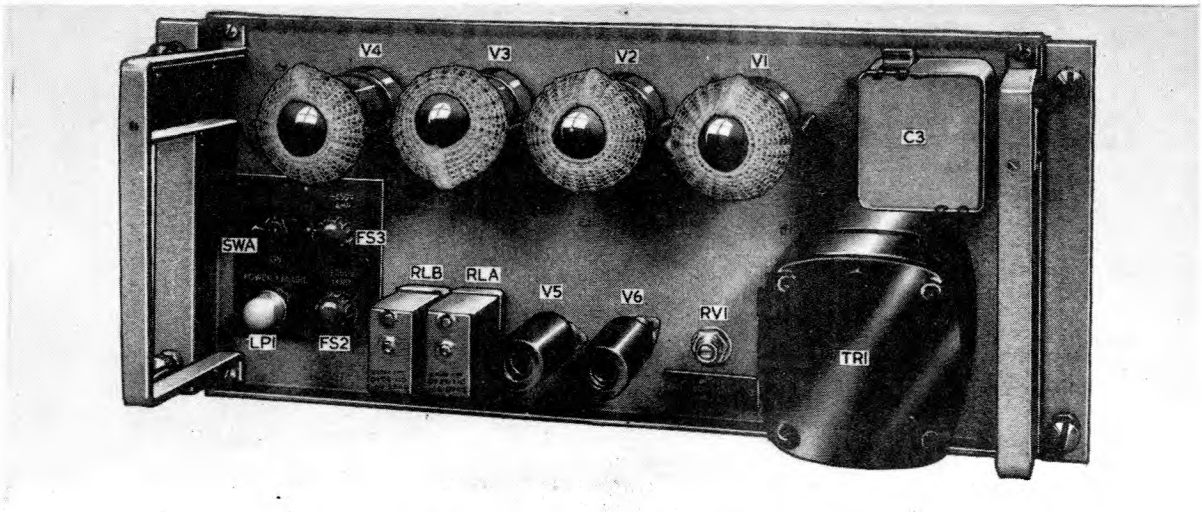


Fig. 1. Voltage regulator (+250V) M2 : front view

Performance characteristics

Inputs

3. The regulator unit requires the following inputs:

(1) +450V unregulated supply from the radar office distribution rack.

(2) −250V regulated, as set by regulator voltage (−250V) M3 (*Sect.* 7, *Chap.* 5).

(3) 240V 50c/s a.c. mains at approximately 0·25A.

(4) −50V.

(5) 6·3V 50 c/s a.c. at 0·3A.

Outputs

4. With input supplies provided as above the following outputs are available :

(1) +450V as required by individual frame units. This output is not fused in the regulator unit.

(2) +250V ± 1·25V with ripple not greater than 10mV at 750mA.

(3) −250V. Current limitations are as required by the frame being supplied. Fused at 1 ampere in the regulator unit.

(4) 240V 50 c/s a.c. as required by the individual frame units. This output is not fused in the regulator unit.

(5) −50V as required by the individual frame units. This output is not fused in the regulator unit.

Circuit description

Heater supplies

5. Heater voltages to the valves are supplied from TR1 (*fig.* 3). The 240V a.c. primary supply for this transformer is via PLB/7 and PLB/10. This supply is controlled by the mains system switch, which **routes** mains to all units of the complete system.

Regulating circuit

6. The +450V station supply from the radar office distribution rack enters the unit on PLB/1 (*fig.* 3). This supply cannot be made however until the −250V supply from the power cabinet has been established, and RLB energized. Contact **RLB/3 routes out the** 50V coming in on SKC/8 to PLB/3. At the radar office distribution rack this −50V operates a relay which makes the +450V supply available at PLB/1.

7. V1, V2, V3 and V4, connected in parallel, are the series control valves for the regulated +250V. V5 and V6, connected as two long-tailed pairs, comprise a high gain d.c. amplifier. The −250V rail is used as the reference voltage for the regulated +250V output.

8. The regulating action of the circuit is explained by considering a change in the output voltage due to variation of load current.

9. Assume that the output voltage tends to rise. The voltage of V6b grid rises, the anode voltage falls, an increased voltage drop occurs across the common cathode load R30 and, as V6a grid is returned to earth, V6a anode rises. The two outputs, of opposite polarity from V6, are then applied to V5. The result will be, under the conditions assumed, that V5b anode potential falls. As the grids of the series valves are returned to this point, the anode to cathode potential across the four series valves will increase and counteract the original rise of output voltage. As V5b is operated in an almost cut-off condition, with resulting low amplification, the anode current is increased by connecting the anode to the +450V input line via R15. This tends to increase the ripple in the anode circuit, but as the amplification of the valve, and the loop gain of the stage are increased the resultant is an improvement in overall performance. The regulated output voltage is set to +250V by adjustment of RV1.

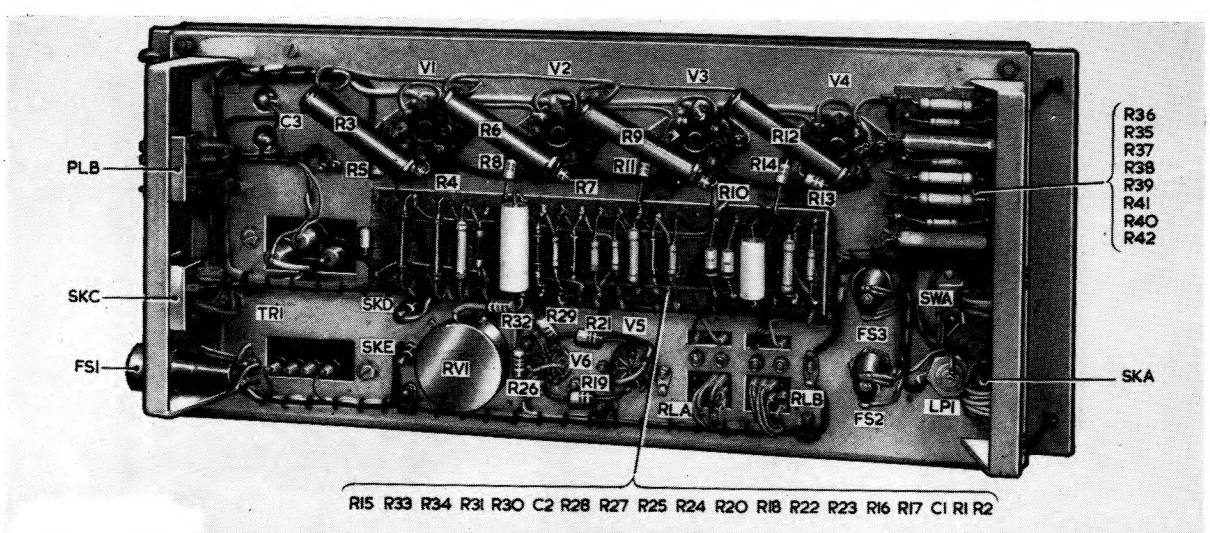


Fig. 2. Voltage regulator (+250V) M2 : rear view

10. The purpose of C2 is to improve the a.c. voltage gain to counteract ripple which may be present on the +250V rail. The ripple is coupled by C2 to V6b grid. The result is to produce a potential, across the controlled valves, in antiphase to the ripple.

Fault lamps

11. Three fault lamps are associated with the regulator unit; they will light if either relays RLA or RLB are de-energized. ◀MR1 obviates incorrect fault indication in the event of RLA being incidentally de-energized.▶ The location and method of operation of the lamps is as follows :—

(1) *Front panel of the regulating unit.* This lamp, POWER FAILURE, LP1 will light if either or both the +450V and −250V supplies fail to enter the unit. It will also light if the regulating circuit fails. Contacts ◀ RLA1 ▶ and ◀ RLB1 ▶ connected in parallel are normally made, so completing the 6·3V supply from PLB/4 to LP1. To extinguish the lamp, indicating correct operation, both relays will therefore have to be energized.

(2) *Front of the cabinet containing regulating unit.* This fault lamp has one side parallel connected through the units in the cabinet and is lit when the paralleled side is earthed. In the regulating unit, contacts ◀RLA2▶ and ◀RLB2▶ control the operation of the lamp. Connections to the external circuit are made by SKC/2 coming in and PLB/2 going out. Failure of the +450V, or −250V supplies, or the regulating circuit, will de-energize either or both RLA and RLB, completing the earth connection via contacts of ◀RLA2 and RLB2.▶

(3) *Front of the power cabinet.* If the −250V supply fails, contact ◀RLB4▶ on the regulating unit closes completing the earth return to the fault lamp on the power cabinet, which should then light. PLB/6 connects the moving contact of ◀RLB4▶ to the power cabinet fault lamp circuit.

Test readings

12. With the multimeter Type 100 connected to SKA via the adaptor, plug to socket (*Ref. No.* 10H/23364) the readings obtained should be as indicated in Table 1. The output voltage of the +250V line can be monitored by connecting a multimeter Type 1 across the monitoring points SKD and SKE.

TABLE 1

Multimeter readings

SKA socket pole	Multimeter switch position	Voltage across Resistor No.	Reading	Tolerance
1	A	R2	0·5	±0·1 (20%)
2	B	R35	0·6	
15	C	R38	0·6	
16	D	R40	0·6	
5	E	R23	0·55	
18	F	R20	0·5	
19	G	R24	0·45	
20	H	R27	0·45	

SERIES CONTROL VALVES

D.C. AMPLIFIERS

PLB/1 +450V

R1 470k

SKA/1

R2 330

R15 2·2M

R13 100 R14 1K

R12 270 V4 CV4060 Y X

R10 100 R11 1K

R9 270 V3 CV4060 Y X

R7 100 R8 1K

R6 270 V2 CV4060 Y X

R4 100 R5 1K

R3 270 V1 CV4060 Y X

FS2 1A

R16 180K

R17 68K C1 0·1

R18 220K R20 33 SKA/18

R24 150 SKA/19 R27 150 SKA/20

R25 100K R28 100K

C2 0·1

V5 CV4024

V6 CV4024

R19 1k R21 1K

R22 22k SKA/5

R23 33

R26 1K R30 10K

R31 100K

R29 1K R32 1M R33 330K

ADJ VOLTS RV1 25K

C3 4

R34 330K

SKD

+450V SKC/1

+250V SKC/9

SKA/6.7.8

R36 220K SKA/2

R35 330

R37 15K

MR1 CV7045

2500 RLA 4

RLA. RLB

RLA3 PINS 1.2.3 } NOT USED
RLA4 PINS 4.5.6 }

SKA/3.4.13.14.17.24

SKC/12

PLB/12

R38 330 SKA/15

R39 220K

POWER OUTPUT SWA

PLB/11 -250V

R40 330 SKE SKA/16

R41 220K

2500 RLB 4

R42 15K

FS3 1A

-250V SKC/11

PLB/7

FS1 1A

TRI

240 230 27 35 30

3·15V 8·5A

3·15V 8·5A

MAINS 45-65 C/S

X Y

PLB/10

RLB4 RLB3 RLA2 RLB2 RLA1 RLB1

LP1 POWER FAILURE

MAINS 45-65 C/S SKC/7 SKC/10

PLB/6 TO FAULT LAMP ON POWER CABINET

PLB/3 TO RADAR OFFICE DISTRIBUTION RACK

PLB/4 6·3v IN FROM -250V REGULATOR

PLB/2 TO CABINET FAULT RELAY ASSEMBLY SKC/2

PLB/5 NOT USED NOT USED SKC/5

PLB/8 -50V -50V SKC/8

	2	3
4	5	6
7	8	9
10	11	12

Fig. 3

Regulator, voltage (+250v) M2: circuit

Fig. 3

Chapter 18

CONTROL (I.F. LEVEL) M7

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

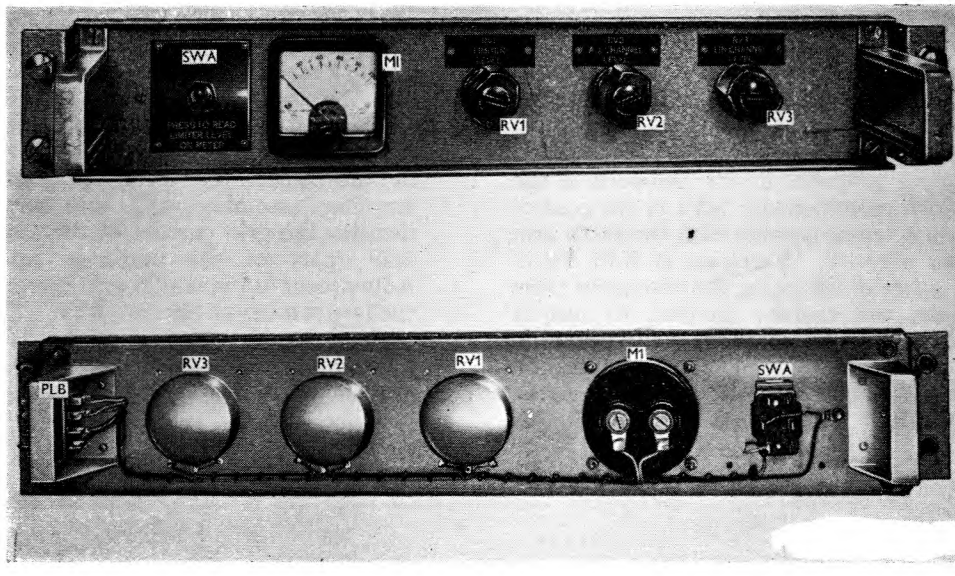


Fig. 1. Control (i.f. level) M7 : front and rear views

Introduction

1. The control (i.f. level) M7 (*fig.* 1), which is mounted on frame 2 of the i.f. cabinet, provides facilities for remotely controlling the gain of the anti-jamming channel and the linear channel i.f. amplifiers in the radar receiver (*Part* 2, *Sect.* 4). Facilities are also provided for controlling the pre-limiter gain and monitoring the grid current of the limiter i.f. amplifier in the anti-jamming channel.

Performance characteristics

2. The ranges of gain control available by means of the three potentiometers on the unit are as follows :—

RV1, LIMITER LEVEL : not less than 45 dB

RV2, A.J. CHANNEL LEVEL : 15 dB $\pm$ 3 dB

RV3, LIN. CHANNEL LEVEL : 32 $\pm$ 5 dB

Circuit description (*fig.* 2)

3. The unit consists of three level controls, together with a 100 mA meter and a toggle switch.

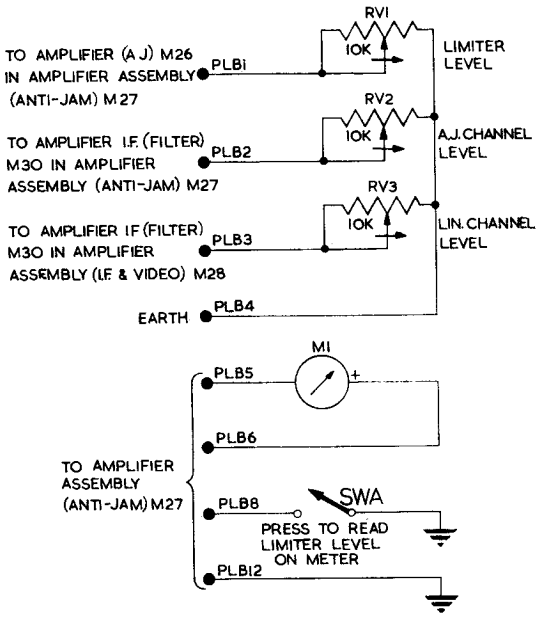


Fig. 2. Control (i.f. level) M7 : circuit

LIMITER LEVEL *control*

4. Potentiometer RV1 is used in conjunction with the limiter grid current meter M1, to adjust the gain control bias potential fed to the amplifier (anti-jam) M26, in the amplifier assembly (a.j.) M27. (*Part* 2, *Sect.* 4, *Chap.* 4.) The bias potential is provided by a potential divider network in the latter unit, with potentiometer RV1 in the control (i.f. level) connected in parallel with the earth arm of the divider network. Variation of RV1 therefore has the effect of adjusting the resistance ratio of the divider, and thereby controls its output potential. It should be noted that the potentiometer is only operative when the A.J. GAIN CONTROL switch on the amplifier assembly (a.j.) is in the REMOTE position. The normal setting of this potentiometer is that which gives a reading of 50 mA on the LIMITER GRID CURRENT meter with the transmitter switch off.

A.J. CHANNEL LEVEL *control*

5. Potentiometer RV2 is used to adjust the bias potential fed to the amplifier i.f. (filter) M30, in the amplifier assembly (a.j.) M27 The circuit arrangement is the same as that described in para. 4, except that local control facilities are not provided and therefore gain control can only be effected from the control (i.f. level). This potentiometer is set to give the required anti-jamming input level to the signal processing equipment.

LIN. CHANNEL LEVEL *control*

6. Potentiometer RV3 provides gain adjusting facilities similar to those already described. In this instance however, the potentiometer, which forms part of a potential divider network in the amplifier assembly (a.j.), supplies a bias potential to the i.f. (filter) unit M30, in the amplifier assembly (i.f. and video) M28 (*Part* 2, *Sect.* 4, *Chap.* 5), and also to the amplifier i.f. (head) M21 (*Part* 2, *Sect.* 4, *Chap.* 3), in the amplifier assembly i.f. (head) M23. The control is only operative when the I.F. GAIN switch on the amplifier assembly (i.f. and video) is in the REMOTE position. This potentiometer is set to give the required linear input level to the signal processing equipment.

Limiter grid current monitoring

7. The meter M1 is connected in parallel with the LIMITER GRID CURRENT meter in the amplifier assembly (a.j.) When the LOCAL/REMOTE switch on this unit is set to the REMOTE position, operation of the PRESS TO READ LIMITER LEVEL switch SWA on the control (i.f. level) energizes RLA on the amplifier assembly (a.j.), and both meters then monitor the grid current of the amplifier (limiter) M29 (part of the amplifier assembly (a.j.)). Adjustment of the limiter grid current is effected by the LIMITER LEVEL control, RV1. The grid current reading is also obtained with SWA in the OFF position when the LOCAL/REMOTE switch on the amplifier assembly (a.j.) is set to the LOCAL position.

Chapter 19

GENERATOR PULSE, VIDEO ZERO
(5840-99-624-8669)

CONTENTS

INTRODUCTION

1. The Generator Pulse Video Zero (GPVZ) is mounted in frame 3 of the i.f. cabinet, and provides a marker pulse which is inserted on the type 84 video channel 1 (selected video) and video channel 2 (log and PLD) to assist in calibration of the ADRS trigger system. The insertion is achieved without interference to either video channel.

2. The generation of the video zero range pulse is time dependent on the distribution unit trigger pulse 't_o-8' μs, from the 'no break' trigger cabinet (Sect.1, Chap.6); this trigger pulse controls the operation of the digital delay circuit.

3. The delay circuit performs two main functions:-

(1) Provides gating signals to a mixing circuit, to blank out a portion (29.6 μs) of video and noise on the two video channels immediately before insertion of the video zero range pulse.

(2) Provides the video zero range pulse for insertion on the two video channels at the output amplifier stage.

4. An output of the video zero range pulse is also sampled, via an amplifier stage, for monitoring purposes.

5. The GPVZ contains its own independent power supplies, so that should the type 84 video processing equipment fail, the video zero range pulse may still be generated and inserted on the two video channels.

6. In the event of failure of the GPVZ or the power supply, the type 84 video processing function and the two video channels are still maintained; this is achieved by relay contact links which bypass the GPVZ when the relays are de-energised.

PERFORMANCE (fig.1)

Inputs

7. SKD receives the trigger pulse from the 'no break' trigger source, timed at 't_o-47' μs, of 15V amplitude into 220Ω output impedance.

8. SKB receives video channel 1 from the type 84 video cabinet electronic switching assembly M2, in the form of positive-going video signals of not more than 3.0V amplitude which are terminated in a high impedance.

9. SKC receives video channel 2 from the type 84 video cabinet electronic switching assembly M2, in the form of positive-going video signals not not more than 3.0V amplitude which are terminated in a high impedance.

Outputs

10. SKN passes the video zero range pulse only, timed to start 47 μs after the reception of the 'no break' trigger pulse. This sample pulse is used for monitoring.

11. SKL passes video channel 1, which has a 4 μs pulse inserted at range zero. The first 16.6 μs of the video and noise is gated out to provide easier recognition of the video zero range pulse.

12. SKM passes video channel 2, which has a 4 μs pulse inserted at range zero. The first 16.6 μs of video and noise is gated out to provide easier recognition of the video zero range pulse.

Monitor points

13. The points at which the performance may be measured are listed as follows:-

SKG - trigger input
SKE - video channel 1 input
SKF - video channel 2 input
SKK - sample video zero range pulse output
SKH - video channel 1 output with superimposed video zero range pulse
SKJ - video channel 2 output with superimposed video zero range pulse.

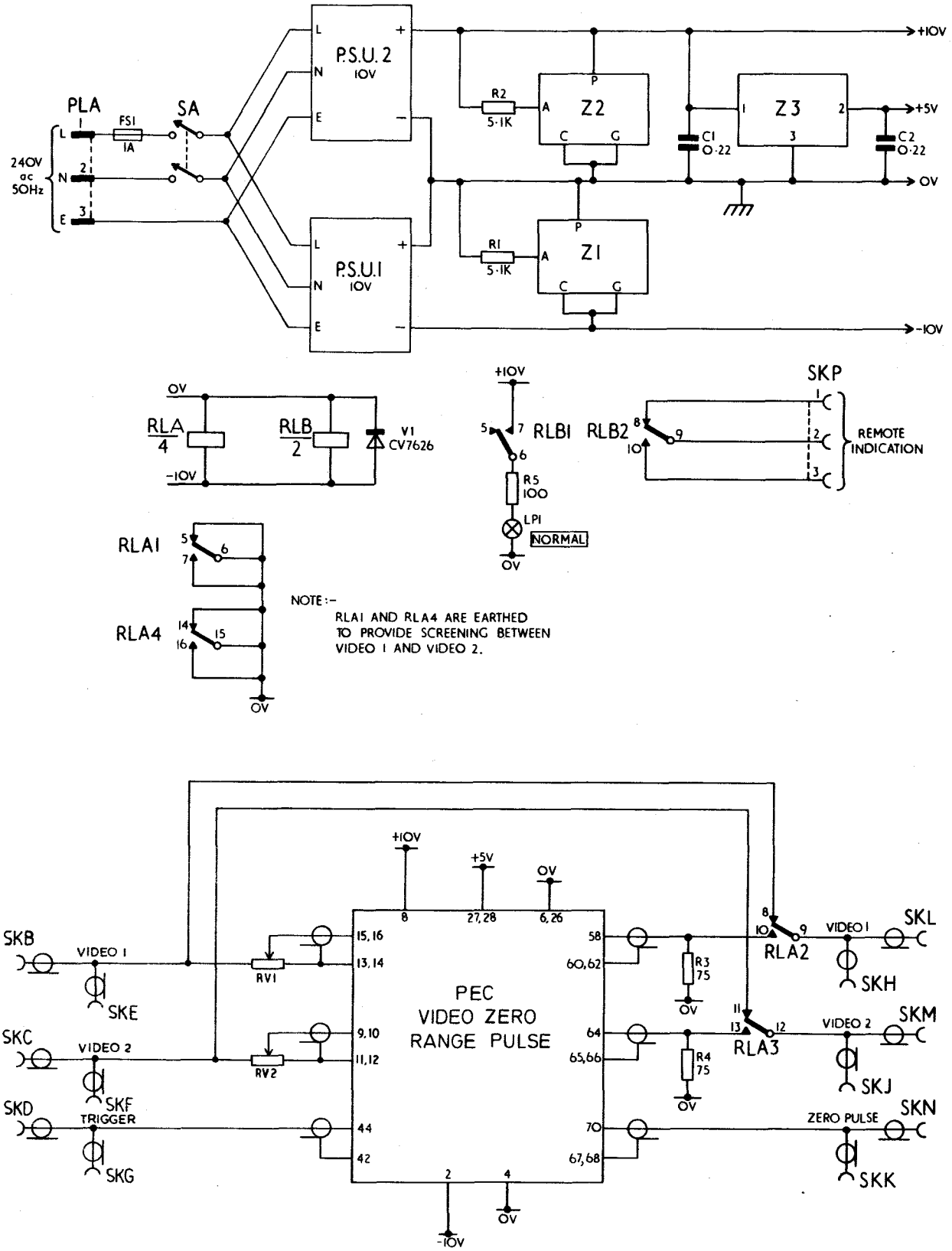


Fig.1 Generator pulse video zero: circuit diagram

CIRCUIT DESCRIPTION (fig.1 and 2)

Power supplies (fig.1)

14. The GPVZ power supplies are generated internally by two ASB 50 power supply units, i.e. PSU1 and PSU2, which are energised by 240V, 50 Hz mains single-phase a.c. via plug PLA. PLA/1 and PLA/2 are line and neutral respectively, and are controlled by a double-pole 5A ON/OFF switch. PLA/3 carries the earth connection. FS1 is a 1A fuse in the line circuit.

15. PSU1 and PSU2 are connected in a negative and positive configuration; they are linked to provide 20V d.c., -10V d.c. and +10V d.c., at 0.5A with respect to the central earth tapping.

16. Two KRO-30 over-voltage protection units (OVPU) Z1 and Z2 are connected across PSU1 and PSU2 outputs. The OVPU detect an increase in voltage output above a Zener set level, as an analogue signal which is fed back to an amplifier circuit; this circuit uses 'crowbar' technique to shunt the excess voltage from the positive rail to negative. No servicing is possible on these encapsulated units.

17. PSU1 output is fed to the GPVZ circuit board, and also to bypass relay RLA and status indication relay RLB.

18. PSU2 output is fed to the GPVZ circuit board, and also to LM 109K regulator (Z3) which produces a 5V d.c. stabilised supply for the delay circuit logic units. The NORMAL indicator (ILP1) supply is taken from PSU2 and illuminates when relay RLB is energised.

19. As with OVPU Z1 and Z2, regulator Z3 is an encapsulated unit which cannot be serviced. Filter capacitors C1 and C2 are respectively connected across the +10V d.c. input to earth, and +5V d.c. output to earth. The regulator circuit is a standard series arrangement, using differential comparison and Zener references for quick response.

Outline of system (fig.1, 2 and 4)

20. Channel 1 (selected video) and channel 2 (log and PLD) are passed from relay assembly M2 in the video cabinet (Sect.5), to SKB and SKC respectively of the GPVZ.

21. The two channels are taken through a mixing stage, which uses series and shunt connected FET. When the switching amplifier is triggered by level changes developed in the delay circuit, a common command signal instructs the series and shunt FET to gate the video channels to produce the required video blank period.

22. The driver/buffer amplifiers receive the two video channels from the mixing stage. The video zero range pulse is inserted by the delay circuit at the amplifier stage, and is timed to occur during a 29.6 μs blank period. The amplifiers outputs are then directed via bypass relay contacts RLA2 and RLA3, to the amplifier video in the video cabinet (Sect.5) through socket SKL - channel 1 and SKM - channel 2 respectively.

23. The delay section of the system receives a trigger pulse from the distribution unit pulse in the 'no break' trigger cabinet (Sect.1); this pulse which is timed to start at 't_0 -8' μs, starts an integrated circuit counter programme via the START/RESET bistable and a dual NAND gate.

24. A 10 MHz crystal controlled oscillator, continuously running, provides the pulse train for the clock input to the counter; this is normally gated by the dual NAND logic, but enabled when the trigger pulse sets the START/RESET bistable. The counters then set their outputs in sequence as the counts register.

25. The counter outputs fan out from level setting buffer stages to a group of four decoding NAND gates, except for the 29.6 µs gating signal (fig.2B) which is first fed through an intermediate dual NAND gate to assist in obtaining an accurate run of the outputs for the specific times required.

26. The four NAND group outputs control two bistables, one of which generates the 4 µs video zero range pulse between 't_o+39' µs, and 't_o+43' µs. The second bistable provides a gating signal of 22.9 µs for the mixer circuit, (fig.2C) starting at 't_o+22.4' µs and resetting at 't_o+52' µs.

27. The 4 µs video zero range pulse (fig.2D) fans out through three tandem buffer stages, before being presented to the driver amplifier circuits for insertion on the video channels and for sample monitoring.

Section detail (fig.4)

28. 10 MHz oscillator. This circuit comprises a Colpitt's resonant feedback oscillator connected in the common base configuration, which uses a QO 1670 B/F 10 MHz crystal (XL1) for frequency truth. The required voltage feedback level to sustain oscillation, is fed to the emitter of VT1 from the junction of capacitors C4 and C5 which are linked across VT1 collector output and ground. The sinewave output is passed via d.c. blocking capacitor C6 through the NAND gate stage to the counters. The waveform may be monitored at terminal point 38.

29. Input stage. The positive-going pulse received from the 'no break' trigger source is passed via R27 at a level set by Zener diode V1, and then established via an inverter stage as a level change to enable the START/RESET bistable. The bistable output is set high and, until reset, enables the following NAND gate to allow the clock pulses to stream through via a buffer stage to the counters. The bistable output also provides the counters clear input when reset.

30. Counter group. The first section of the delay circuit consists of a group of three 4-bit counters connected in cascade. The counter J-K bistables are arranged to be triggered on the rising (positive-going) edge of the clock input waveform, when enabled by the high level on the clear input. Three outputs are taken from the first counter for the NAND decoding stage. A carry output triggers the second counter from which all four outputs are utilised, and again the carry output triggers the third counter for two outputs. The counters all reset when the clear line is reset low by the following circuit.

31. Decoding stage. This contains a group of eight buffers to provide high and low level fan out of the counter outputs. The buffer outputs are fed to four 8-input NAND gates, together with a direct link and an indirect link via a dual NAND gate and further buffer for the divide by 4 and 8 outputs of the first counter. The output of an 8-input NAND gate is low when all inputs are high, and this low triggers a timing bistable.

32. Timing bistables. The first bistable is triggered at 't_o+39' µs, and resets at 't_o+43' µs, producing the 4 µs video zero range pulse. The second bistable is triggered at 't_o+22.4' µs, and resets at 't_o+52' µs, this produces the mixer gating period of 29.6 µs. The second bistable output also resets the input stage START/RESET bistable, to stop the sequence.

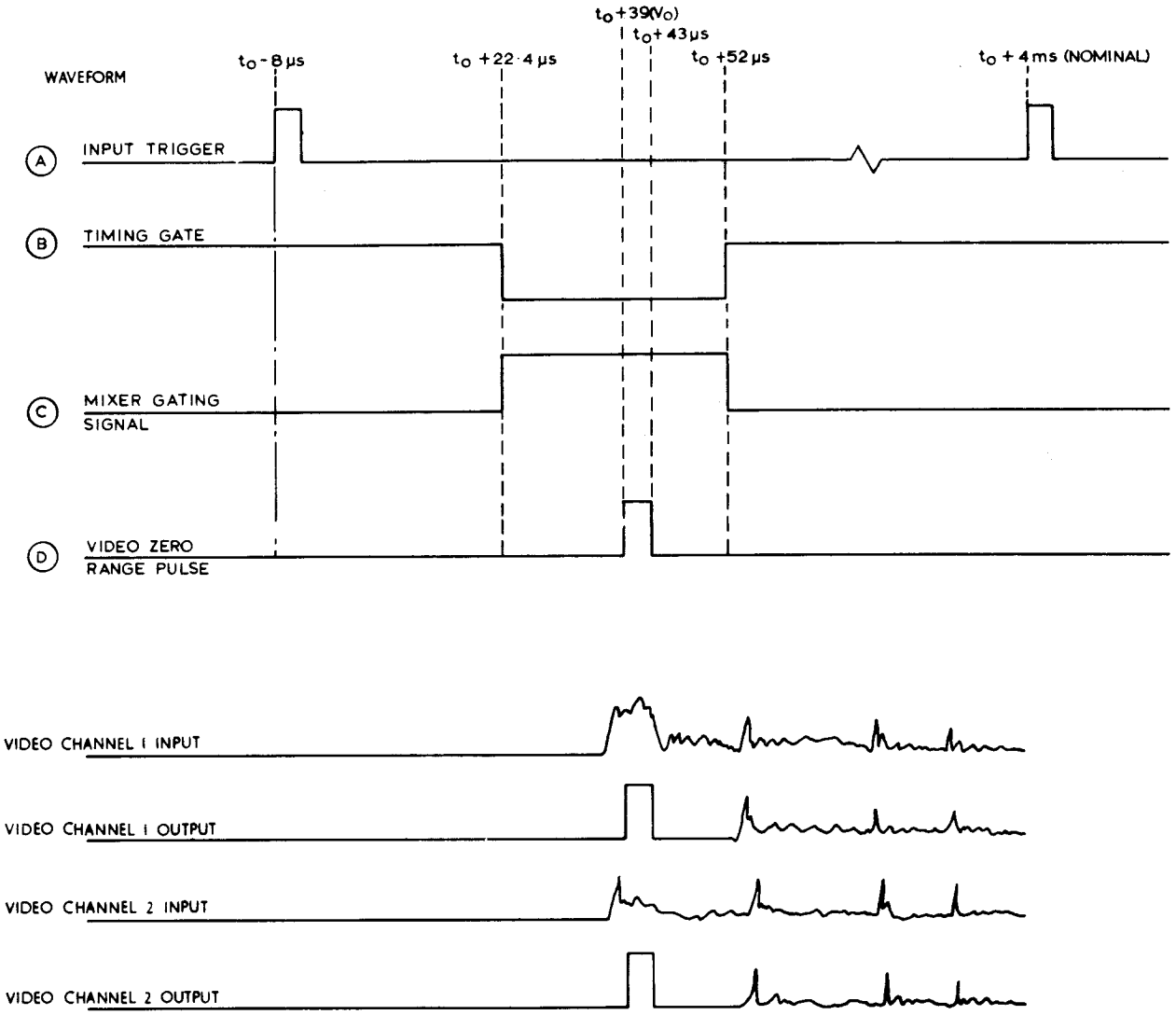


Fig.2 Generator pulse video zero: timing chart

33. Mixing circuit. A complementary switching amplifier VT12 and VT11 receives the 22.4 µs gating signal, and this switches VT10 to turn FET VT7 and VT9 off, and VT6 and VT8 on to inhibit the video waveform for the required blank period. At the 52 µs reset pulse, VT7 and VT9 turn on, and VT6 and VT8 turn off to restore the video waveform.

34. Driver amplifier stages. The driver (buffer) amplifier stages for channel 1 and 2 are identical. The video signals are conducted through differential circuits VT2/VT15 and VT5/VT16. During the blank period, the differential amplifiers output remains stable until triggered by the insertion of the 4 µs pulse in the middle of the period. VT3/VT17 and VT4/VT18 complementary drive amplifiers are stabilised by emitter connected Zener diodes V10 and V9 respectively, and have a measure of negative feedback to cancel any inherent gain. VT13/VT14 is a complementary driver circuit, providing a collector coupled video zero range pulse for monitoring. RV1 and RV2 are used during setting up to ensure channel 1 and 2 output waveforms are at the correct baseline levels. These components are located on the PEC Video Zero Range Pulse.

35. Video output switching. (fig.1) Channel 1 and 2 video, having been processed by the PGVZ, pass to N.O. contacts RL2 and RL3 of a Varley VP4 TC CBB 12V plug-in relay RLA. RLA is normally continuously energised by PSU1, and the video with the impressed pulse is passed to SKL and SKM respectively. In the event of supply failure, RLA2 and RLA4 contacts relax and channel 1 and 2 bypass the GPVZ circuit board. The converse is also true, i.e. should the video channels fail, provided a trigger signal is present, the GPVZ will still produce a 4 µs marker pulse.

36. RLA1 and RLA4 are earthed to provide screening between the two video channels.

37. Video gain control. RV1 and RV2 (video gain controls), mounted on the unit panel, provide adjustment for the video outputs of the GPVZ. For a 2.0V positive pulse input at SKB or SKC, they are adjusted to give an output, at SKL and SKM respectively, of not less than 2.0V.

38. Indication. (fig.1) Varley VP2 TC CAB 12V plug-in relay RLB is also continuously energised by PSU1 and this closes N.O. contacts RLB1, allowing a 10V supply from PSU2 to illuminate lamp ILP1 (green) via 100Ω dropper resistor R5. Contacts RLB2 are connected across SKP to facilitate remote indication.

Delay links (fig.4)

39. Links are provided to allow different timings of the video zero range pulse for varying site requirements. Fig.4 shows the links connected for a pulse starting at 47 µs after the 'no break' trigger pulse (t_o-8 µs), and finishing 4 µs later. Alternative delay settings are shown on Table 1 (Start) and Table 2 (Finish); item 1 on Table 1 is associated with item 1 of Table 2, linked to produce a 4 µs pulse.

TABLE 1 START LINKS

Item	Delay time	Z11 Pins			
	From t_o-8 µs	10	4	2	1
1	40.0 µs	4	8	11	15
2	40.8 µs	4	8	9	15
3	41.4 µs	4	8	9	13
4	43.2 µs	4	6	11	15
5	44.6 µs	4	6	9	13
6	46.4 µs	2	8	11	15
LINK No.		2	4	6	8

TABLE 2 FINISH LINKS

Item	Delay time	Z10 Pins				Pulse width
	From t_o -8 µs	10	4	2	1	µs
1	44.0 µs	3	5	9	14	4.0 µs
2	44.6 µs	3	5	9	12	3.8 µs
3	46.4 µs	1	7	10	14	5.0 µs
4	47.2 µs	1	7	9	14	4.0 µs
5	49.6 µs	1	5	10	12	5.0 µs
6	50.4 µs	1	5	9	14	4.0 µs
	LINK No.	1	3	5	7	

POWER SUPPLY UNITS (fig.3 and 5)

40. Two Coutant ASB 50 power supply units are used, PSU1 and PSU2. Each is set to provide a 10V d.c. stabilised output for 240V, 50 Hz a.c. mains supply.

Outline of unit

41. The ASB 50 is a series-regulated power supply source. The input voltage to the power supply unit is applied to the primary windings of transformer T1 through an antisurge fuse FS1. The split primary windings of T1 are connected in series for use with a 240V supply.

42. The d.c. output of the supply is derived from a full-wave bridge rectifier comprising V11a, 11b, 12a and 12b. The output of the bridge rectifier is fed, via a series-regulating transistor VT50, and resistor R50, to the output terminals.

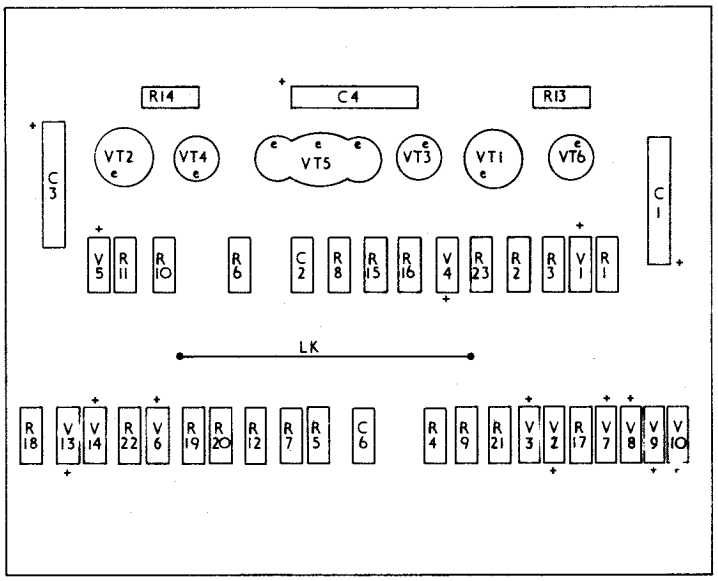
43. A subsidiary secondary winding of T1 supplies the bridge rectifier formed by V7, 8, 9 and 10, the d.c. output of which is used in conjunction with a constant current source VT1 and VT6, to supply the Zener diode chain V2, V3 and V4.

44. The d.c. supply for the regulation control circuit is developed across V3 and V4. The junction of V2 and V3 clamps the common reference and forms the positive sensing line.

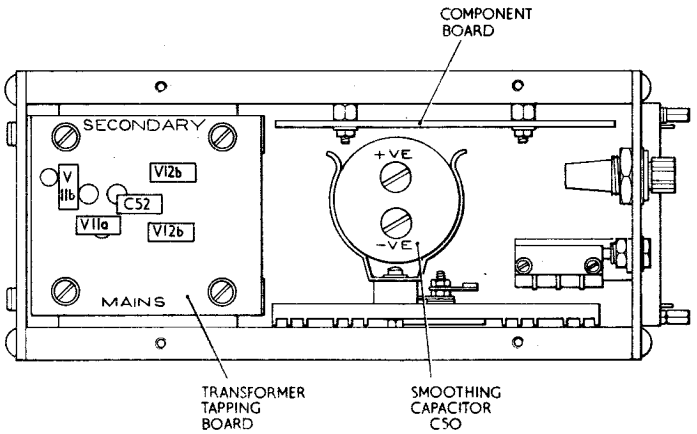
Regulation circuit

45. Zener diode V6 and resistor R17 form a voltage source from which R19 derives a reference current which is applied to the base of VT5b and is compared with a current developed in resistor R20, which is directly proportional to the output voltage of the power supply unit. The value of R20 establishes the output voltage; variable resistor RV1 gives some measure of adjustment of this voltage.

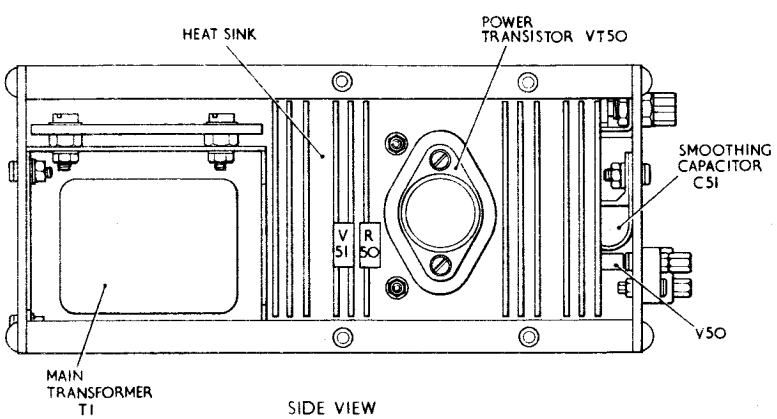
46. If the power supply voltage rises, the current through R20 to the base of TR5b decreases, because the positive sensing line is clamped to the common reference rail. This causes the collector voltage of VT5b to increase, and the consequent positive increase at the base of VT3 decreases the base voltage of VT2. This in turn reduces the output voltage of the power supply unit by increasing the collector/emitter voltage of VT5b.



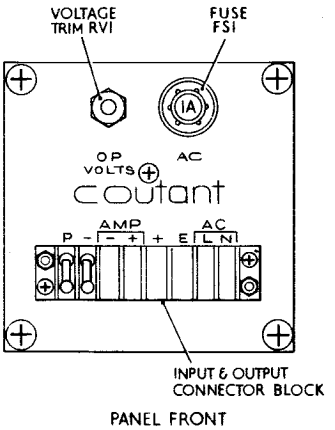
COMPONENT BOARD



PLAN VIEW



SIDE VIEW



PANEL FRONT

Fig.3 ASB 50 Power supply unit: component layout

47. The lag network formed by capacitor C2 and resistor R8 ensures high frequency stability of the closed loop. Capacitor C4 and resistor R18 bypass R20 to provide a degree of ripple attenuation, thus increasing the low frequency a.c. loop gain.

48. Resistor R12 is incorporated to improve the output resistance by providing positive current feedback into the comparator VT5a and VT5b. This current is proportional to the output current.

Overload protection

49. Overload protection is provided by VT4, which compares the voltage across resistor R50 with a reference voltage from potential divider R6 and R10. When the voltage across R50 increases sufficiently, VT4 conducts and diverts the drive to VT2 causing the output voltage and current to fall to a low level. When the output voltage falls the reference voltage from the potential divider decreases, hence the voltage drop across R50, required for conduction of VT4, decreases and the available output current falls.

50. When VT4, is conducting, the drive voltage to VT2 is developed across resistor R9 thus preventing VT3 from interfering with the operation of VT4.

Re-entrant overload protection

51. When the unit is first switched on, capacitor C3 starts to charge up and because the base of VT4 is more positive than the emitter, VT4 conducts. The power supply maintains a constant current characteristic so that it cannot be overloaded when switched on or when recovering from an overload condition. This constant current characteristic is maintained until the potential on C3 equals the potential at the base of VT4, at which point VT4 ceases to conduct and the power supply adopts its NORMAL operating condition. Diode V5 prevents C3 causing voltage overshoots when the supply unit is switched off.

Reverse voltage protection

52. Diode V50 is fitted to protect the power supply from reverse voltages applied across the output terminals.

NOTE.
LINKS 1 TO 8 ARE SHOWN FOR A DELAY START OF 47µs, AND A DELAY FINISH OF 51µs. FOR LINK POSITIONS TO OBTAIN OTHER START AND FINISH TIMINGS SEE TABLES 1 AND 2.

NOTE:- POLARISING SLOT PINS 19 & 20

PACKAGE	TYPE	
Z1, 7, 8	9002	FIG.1
Z2, 3, 4	9316	FIG.2
Z5, 6, 13	9016	FIG.1
Z9 10 11 12	9007	FIG.1

FIG. 1

FIG. 2

Video zero range pulse p.e.c. : circuit diagram

Fig 4

AL 8 Feb. 77

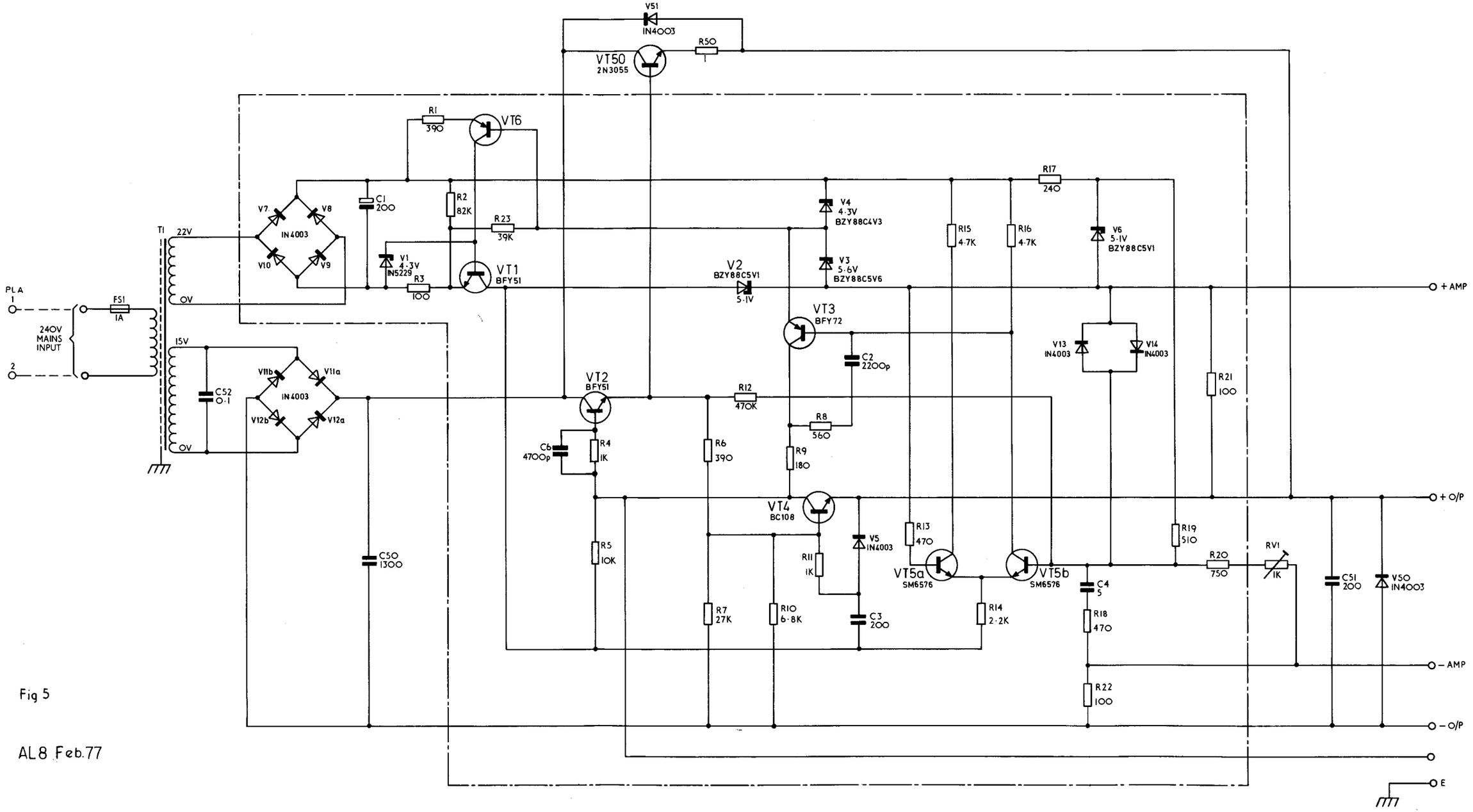


Fig 5

AL8 Feb.77

ASB 50 Power supply unit: circuit diagram

Chapter 20

IF BYPASS RELAY S40-9131-01

CONTENTS

INTRODUCTION

1 The IF bypass relay S-40-9131-01 (fig.1) is fitted on frame 1 of the i.f. cabinet at those stations fitted with the modifier MTI processor S7110. The bypass relay consists essentially of four coaxial switching relays operated from the -50V d.c. supply and a control relay energized by a +15V d.c. supply from the MTI processor.

2 The linear i.f. signal from the radar head and the selected lock pulse from switch electronic M2 are rerouted when Mod. No.CA8125/3 is embodied and taken as inputs to the bypass relay unit. Under normal operating conditions these signals are fed to the S7110 interface unit and input to buffer amplifier (1:1), splitter circuits. Buffered signals are then returned to the i.f. cabinet and routed via the bypass relay unit to the signal processing circuits.

3 The control relay, normally energized, holds the switching relays de-energized and the i.f. and lock signals are routed as described in para.2. Should the S7110 power supplies fail the control relay is de-energized and the switching relays energized. The switching circuits then bypass the inter-cabinet connections and apply the signals direct to the i.f. cabinet processing circuits.

CIRCUIT DESCRIPTION (fig.2)

Power supplies

4 The bypass relay unit receives the following d.c. supplies:

4.1 +15V (PL1, pins 3 and 4) from the multifilter MTI processor.

4.2 -50V (PL1, pins 1 and 2), station supply.

Switching circuits

5 The signal input/output connections to the four switching relays, RLA,B,C and D are by coaxial plug terminated flying leads from the cabinet termination panel (unit 403) and the cabinet inter-unit cabling, direct to the relay termiantion concerned. Switch S1 provides normal control of the bypass function and lamp LP1 is illuminated when the switching relays are in the bypass condition (signals not fed to MTI processor).

6 With switch S1 closed to complete the +15V circuit to RLE, the switching relays are held de-energized by contacts RLE1. The i.f. (SKH) and lock pulse (SKD) are passed via RLC and RLD respectively to the MTI processor via SKAC (i.f.) and SKAD (lock). The return signals from the MTI processor, input at SKAA and SKAB are passed by RLA (i.f.) and RLB (lock) to the switch electronic and the coherent oscillator respectively to restore the normal input requirements of the i.f. cabinet signal processing channels.

7 If the +15V supply fails or S1 is switched to BYPASS, RLE is de-energized and the switching relays are energized via contacts RLE1. The input signals at relays RLC and RLD are routed via the coaxial links RLC/3-RLA/3 and RLD/3-RLB/3 direct to the i.f. cabinet signal processing circuits, thus bypassing the inter-cabinet connections and removing the i.f. and lock pulse inputs to the multifilter MTI processor S7110.

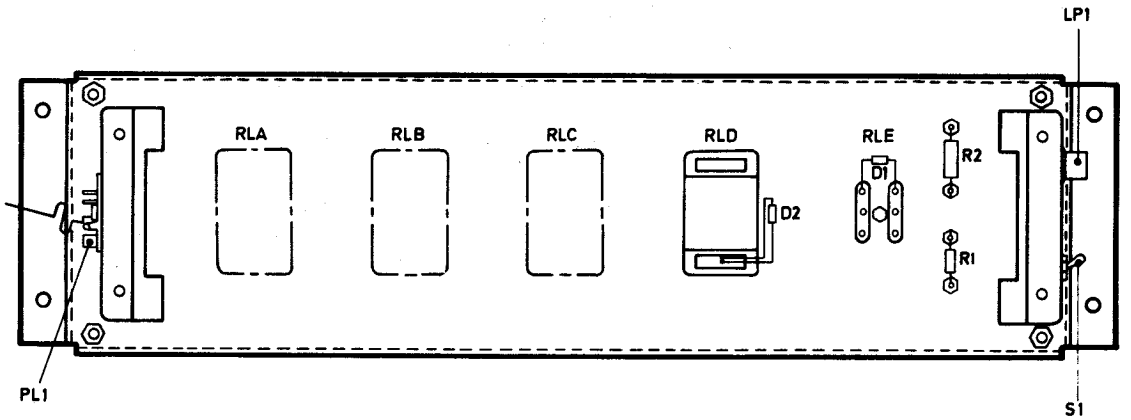


Fig.1 IF bypass relay S40-9131-01: component layout

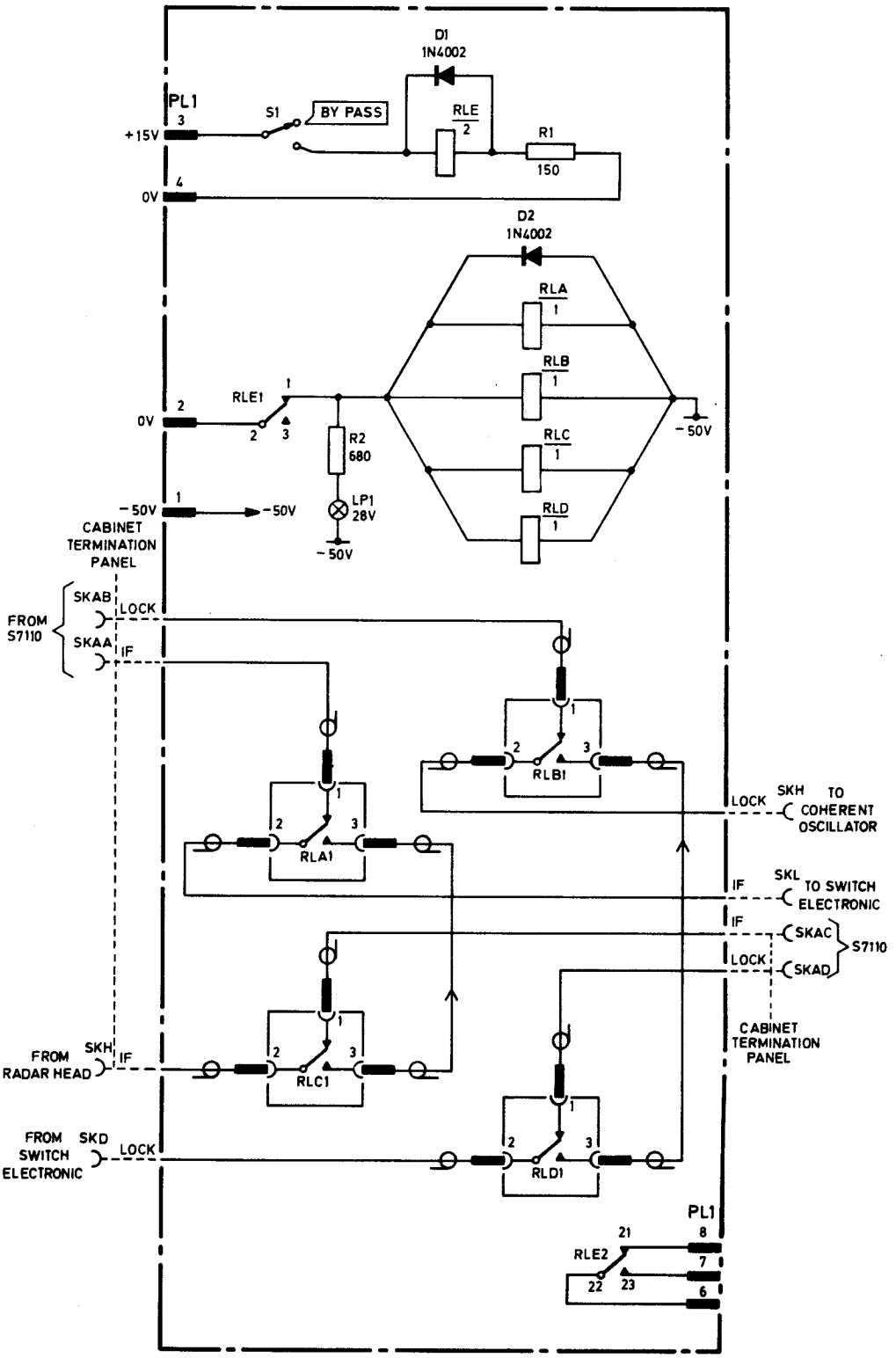


Fig.2 IF bypass relay S40-9131-01: circuit

SECTION 3

CANCELLATION CABINET

Chapter 1

CANCELLATION CABINET AND INTERCONNECTIONS
(Completely revised)

CONTENTS

TABLE

ILLUSTRATIONS

Purpose of cabinet

1. The cabinet, electrical equipment M44 (fig. 1 and 2) contains the units which provide a three-pulse permanent echo cancellation system incorporating doppler-compensated clutter cancellation. A block diagram of the cabinet is given in fig. 3.

2. The system uses a process involving two stages of cancellation and from fig. 3 it will be seen that similar circuits are provided for channel A and channel B. Since channel B also includes the p.r.f. correction circuits, this is the channel that will be described.

3. Bipolar video signals from the channel B coherent demodulator in the i.f. cabinet are applied to the driver (delay line) M1. This unit also receives 6.14MHz and 8.19MHz carriers from the p.r.f. system and produces outputs consisting of carriers at the same frequency as the input but amplitude modulated by video signals. In the case of the 8.19MHz output modulation is by the original input video signal: the 6.14MHz carrier is modulated by a video signal which has already been through one stage of cancellation.

4. The outputs of the driver delay line are applied to a hybrid network, where they are combined and fed through a mercury delay line whose delay is equal to one p.r.f. period, after which the combined carriers are applied to a second hybrid circuit, which functions as a splitter, producing separate, delayed 6.14MHz and 8.19MHz carriers. These carriers are then applied to separate signal comparator units.

5. The combining hybrid network also feeds the separate carriers to a variable delay line which produces two outputs consisting of an undelayed 8.19MHz carrier and a once cancelled, once delayed 6.14MHz carrier. These outputs are then applied to the respective signal comparator units, where they are compared with the delayed carriers from the hybrid splitter circuit.

6. The comparator (signal) M1 produces a once cancelled, once delayed video output which is fed to the video cabinet. A second output, which is the result of addition of the two input signals, is fed to the switch, electronic (clutter) M1.

7. The clutter switch unit discriminates between wanted signals due to targets and unwanted signals due to clutter or 'angels', and only produces an output when the input signal is clutter-derived. This output, in the form of uni-polar video, is fed to the doppler cabinet for gating.

8. Comparator (signal) M2 produces two video outputs, once cancelled, twice delayed, and twice cancelled, twice delayed. Both of these outputs are fed to the video cabinet for further processing.

9. The p.r.f. correction circuits comprise the generator (reference signal) M2 and the controller (p.r.f.) M1. The generator (reference signal) produces a 500Hz waveform output which is fed to the p.r.f. controller. This unit also receives delayed and undelayed bipolar video signals from the comparator (signal) M1, and produces a 500Hz output, the phase and amplitude of which are dependent upon the time error between the two video signals. The output sine-wave is used in the p.r.f. system as the power supply for a motor-driven capacitor which controls the frequency of the p.r.f. generator, thus ensuring that the pulse recurrence peiod is always equal to the signal delay introduced by the mercury delay cell in the cancellation cabinet.

10. Two amplifiers, video and switching 5840-99-626-7183 are fitted in the cancellation cabinet for use in conjunction with an external plot and code extractor. The amplifiers, when fitted, are designated units 104 and 105. The input to amplifier unit 105 is a rectangular outline marker from the doppler cabinet (M46). The inputs to amplifier unit 104 are MT1 video and switching waveforms from the video cabinet (M45). The outputs of amplifier, unit 105 are two buffered rectangle outline markers, one of which is fed to the plot and code extractor, whilst the other is fed to the monitor suite. The MT1 video and switching waveform outputs from unit 104 are both fed to the plot and code extractor.

Mechanical description

11. A mechanical description common to all cabinets is given in Appendix 1 to Sect. 2, Chap. 1, while mechanical features peculiar to the cancellation cabinet are given herein.

12. The cabinet generally is the same as described in Appendix 1, with the exception that the unit frames are not full-length. The lower section of the cabinet is reinforced to accommodate the horizontally-mounted mercury delay cell, which rests on nylon rollers. A list of weights and dimensions of individual units is given in Table 1.

Electrical description

13. An electrical description applicable to the cancellation cabinet is given in Sect. 2, Chap. 1.

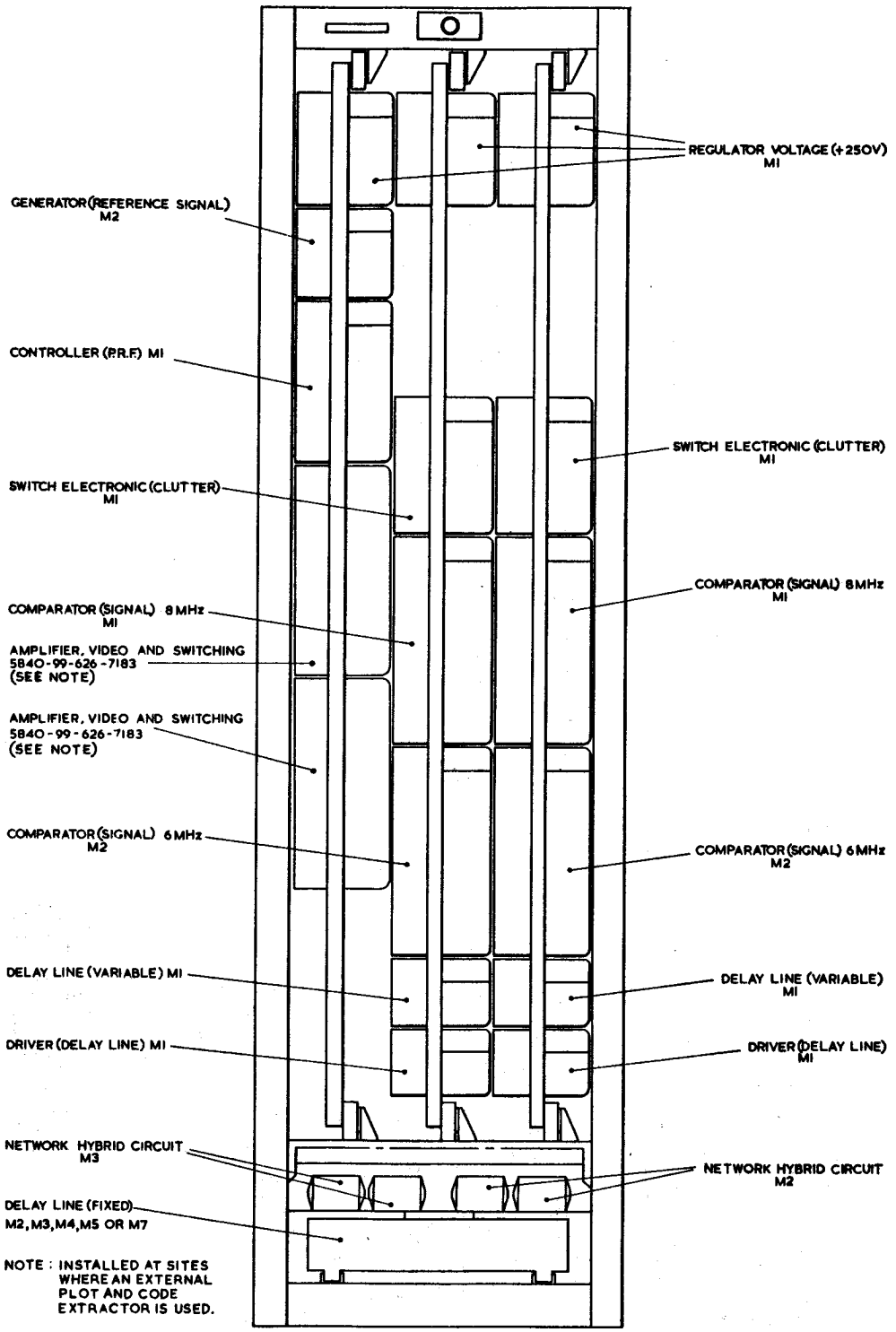


Fig. 1. Cancellation cabinet : front view

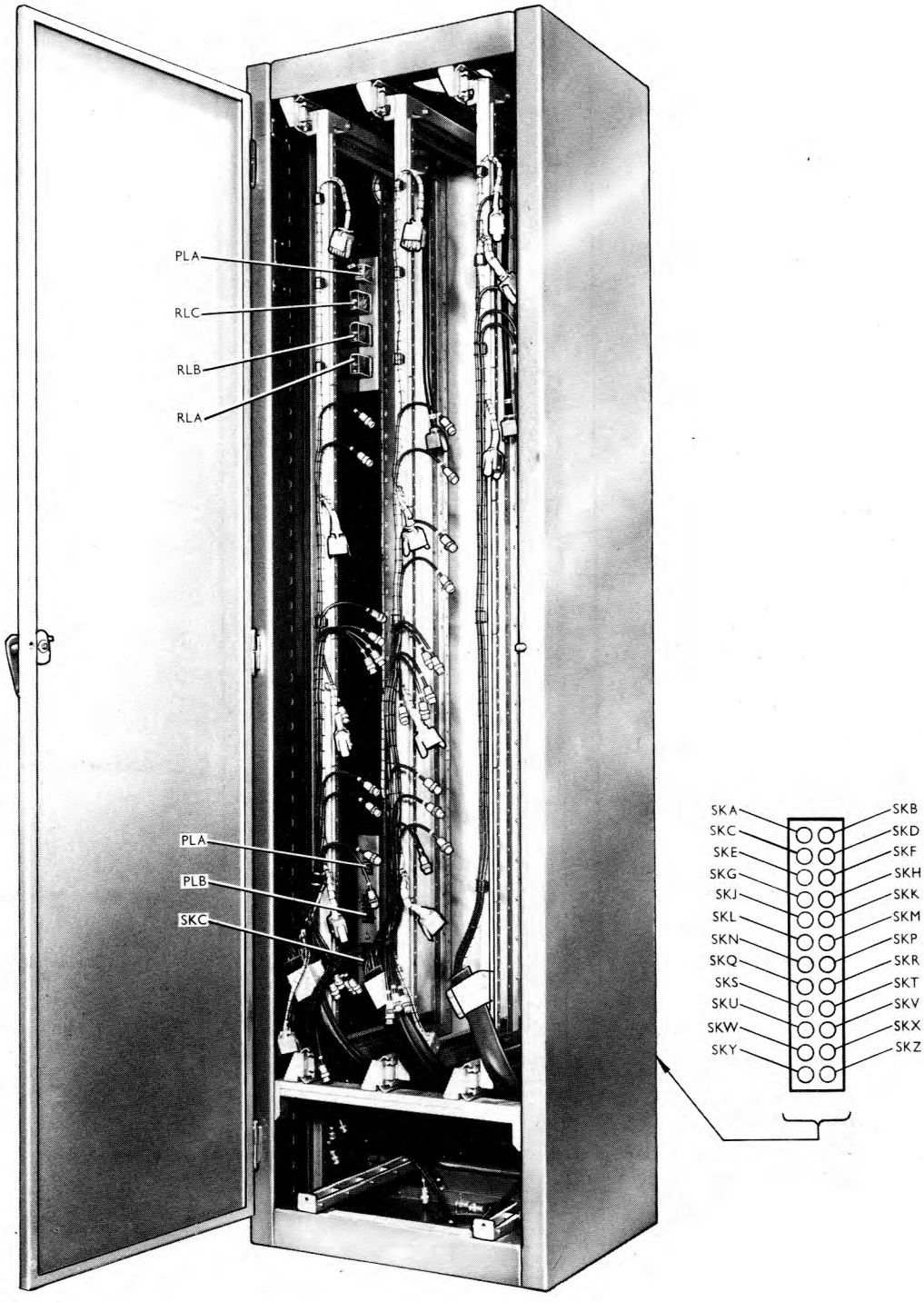


Fig. 2 Cabinet electrical equipment M44: rear view

Power distribution

14. Distribution of power supplies within the cabinet is shown in fig. 4. This drawing includes a circuit diagram of the cabinet fault relay assembly, a description of which is given in Sect. 2, Chap. 1. However, in the cancellation cabinet application of the unit, an additional fault indication is given by the controller (p.r.f.) M1, when the delay synchronisation is incorrect.

TABLE 1

Weights and dimensions

Title	Dimensions (inches)	Weight	A.M.Ref.	Chapter
Cabinet, electrical equipment M44	84¼ x 25¼ x 23½	425 lb	10D/23277	Sect. 2, Chap. 1 and Appendix
Driver (delay line) M1	17½ x 6 x 4½	5 lb	10D/22628	2
Network, hybrid circuit M2	4½ x 4 1/8 x 3	½ lb	10D/22634	3
Network, hybrid circuit M3	4¼ x 4 1/8 x 3	½ lb	10D/22635	3
Delay line (fixed) M2	18 x 18 x 6¼	224 lb	10D/22696	4 (See note below
Delay line (fixed) M3			10D/22697	
Delay line (fixed) M4			10D/22698	
Delay line (fixed) M5			10D/22699	
Delay line (fixed) M7			10D/22801	
Comparator (signal) M1	17½ x 13 x 6	15 lb	10D/22624	5
Comparator (signal) M2	17½ x 13 x 6	15 lb	10D/22625	6
Amplifier, delay line M5 and M6	9½ x 3¼ x 2	1½ lb	10U/17489	7
Delay line (variable) M1	17 x 6 x 4½	2½ lb	10D/22623	8
Switch electronic (clutter) M1	17½ x 9 x 6	8¼ lb	10F/20585	9
Controller (p.r.f.) M1	17½ x 10½ x 6	8 lb	10L/16756	10
Generator (reference signal) M2	17½ x 6 x 6	7 lb	10V/16454	11
Regulator voltage (±250V) M2	17½ x 7¼ x 6	9 lb	10D/22632	Sect. 2, Chap. 17
Amplifier, video and switching (units 104 and 105)	17½ x 8 7/8 x 6	13 lb	5840-99-626-7183	Sect. 3, Chap.12

Note ...

The delay line (fixed) is selected from those given in the above list, choice being governed by the particular station p.r.f.

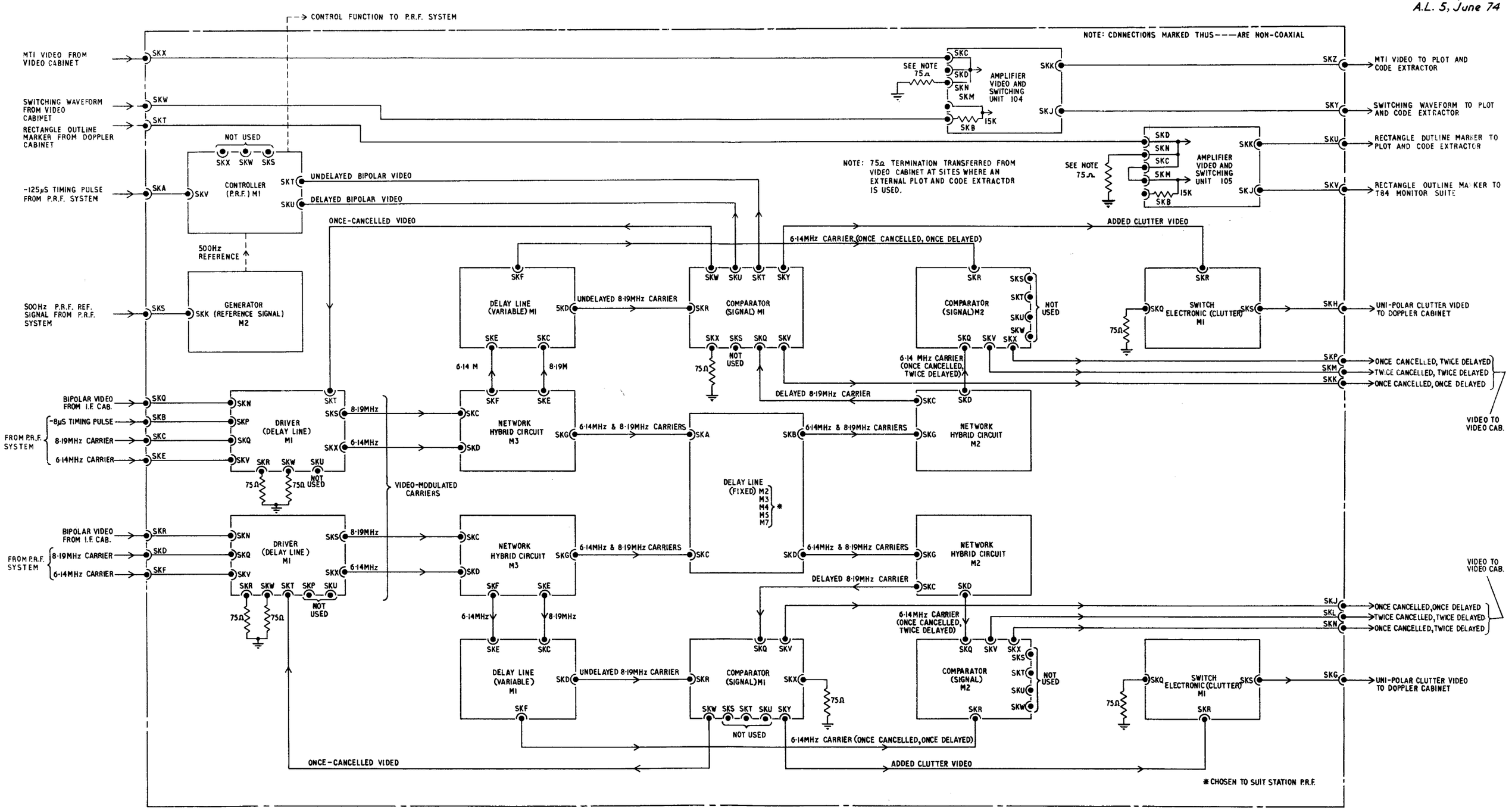


Fig. 3

Cancellation cabinet: signal interconnections

Fig. 3

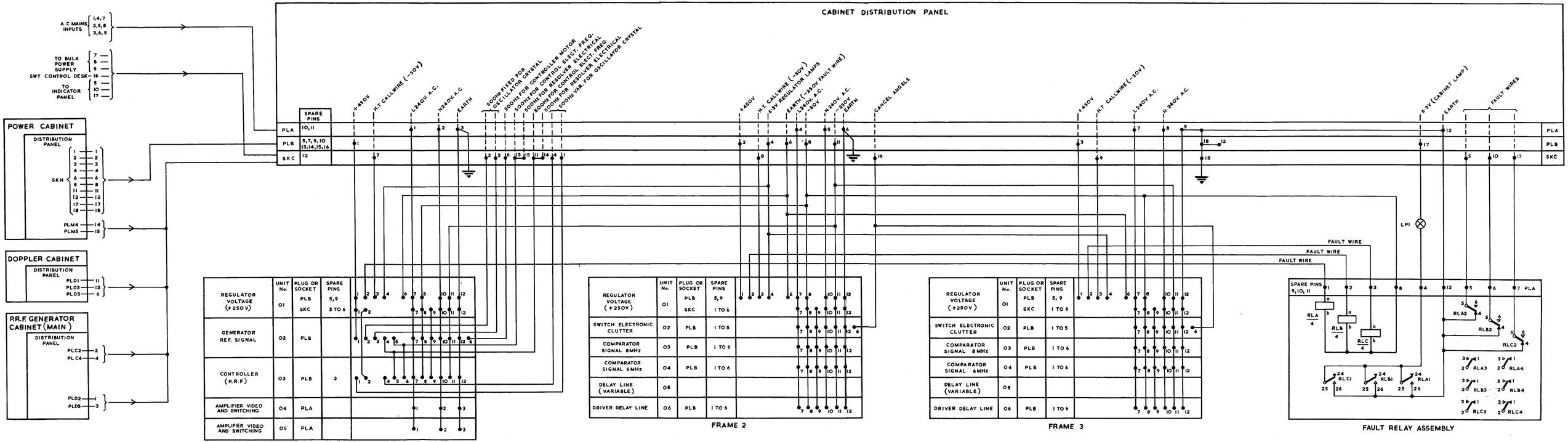


Fig.4

Cancellation cabinet : power distribution

Chapter 2

DRIVER, DELAY LINE, M1

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

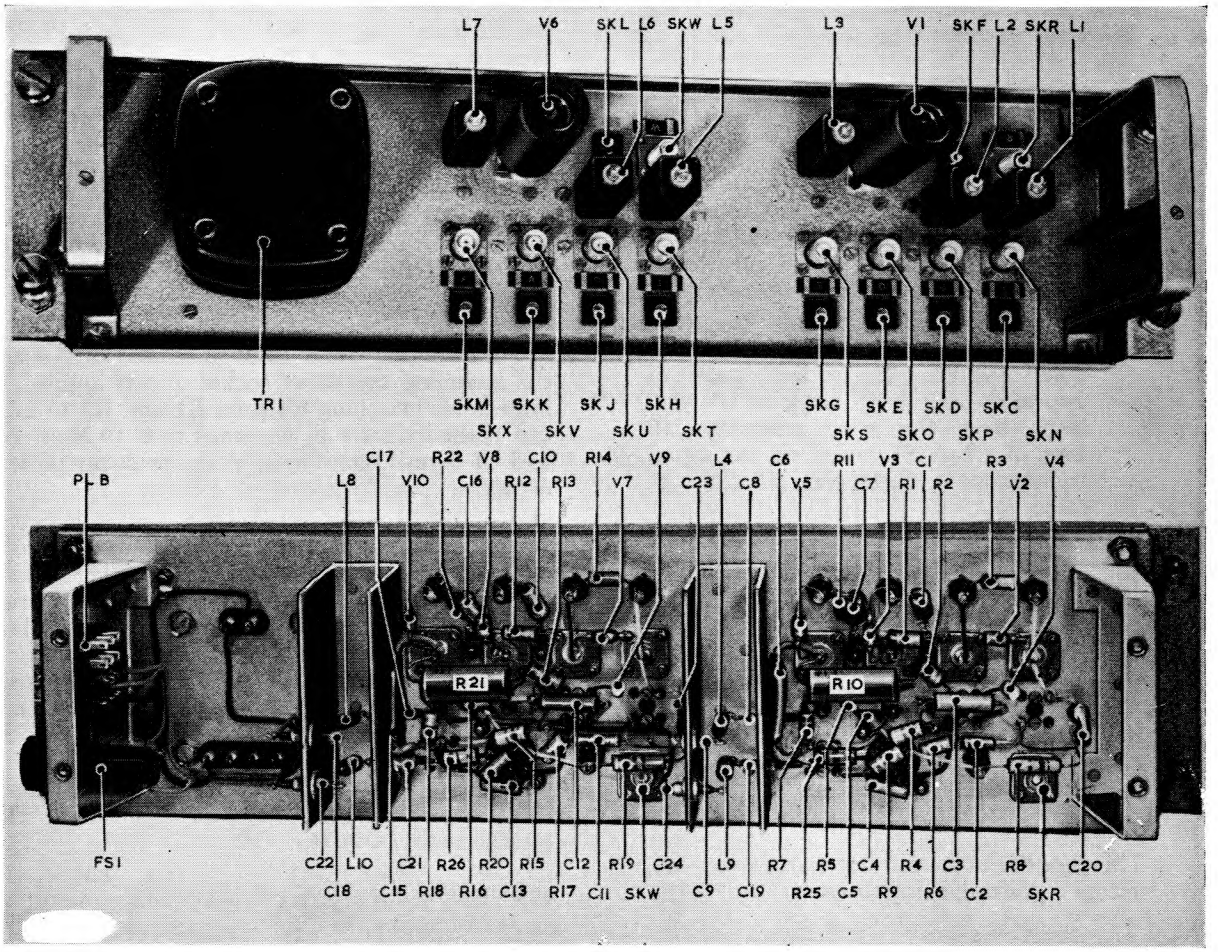


Fig. 1. Driver, delay line, M1 : top and underside views

Introduction

1. There are three delay line driver units (*fig.* 1) in the radar Type 84 signal processing system. Two delay line drivers corresponding to the cancellation channels A and B are located in frames 3 and 2 respectively of the cancellation cabinet. The third delay line driver, in the p.r.f. discrimination channel, is located in frame 2 of the video cabinet. The p.r.f. discrimination channel, having only one 4 ms delay stage, uses only the 8 Mc/s section.

2. It is not possible to transmit video pulses directly through the 4 ms delay cell (*Sect.* 3, *Chap.* 4) because of its bandwidth limitations. In order to avoid any undue distortion it is necessary to impress the video waveform as a modulating signal on a carrier. The delay line driver M1 serves the purpose of modulating a carrier, whose frequency is that of the resonant frequency of the crystal transducers in the delay cell, with the video signal.

3. This unit consists of two similar circuits on one chassis, corresponding to the two stages of cancellation used in the Type 84 MTI system. One circuit accepts the 8·19 Mc/s carrier and the other the 6·14 Mc/s carrier ; each circuit accepts video signals which amplitude-modulate the carrier. Provision is also made in each circuit for modulating the carrier with a timing pulse for p.r.f. control purposes. A description of the cancellation system is given in Sect. 1, Chap. 3.

Performance characteristics

Inputs

4. (1) SKQ

8·19 Mc/s carrier, 6V peak-to-peak, from the p.r.f. system

(2) SKV

6·14 Mc/s carrier, 6V peak-to-peak, from the p.r.f. system.

(3) SKN

(i) In the cancellation cabinet this socket receives bi-polar video signals of up to 3V peak-to-peak at +2V d.c. level, from the demodulator (coherent) M1 (*Sect.* 2, *Chap.* 10).

(ii) In the video cabinet SKN receives unipolar positive-going video signals of approximately 1·5V peak at 0V d.c. level, from the relay assembly M2 (*Sect.* 5, *Chap.* 6) routed via the signal comparator (coincidence) M3 (*Sect.* 5, *Chap.* 4).

(4) SKT

Bi-polar video signals up to 3V peak-to-peak at a +2V d.c. level, from the signal comparator M1 (*Sect.* 3, *Chap.* 5).

(5) SKP

8μS positive-going pulse, not less than 15V peak, from the p.r.f. system (Channel B and p.r.f. discrimination channel only ; not used in channel A).

(6) SKU

This input is not used, but can if necessary accept a positive-going timing pulse.

Outputs

5. (1) SKS

(i) In the cancellation cabinet socket SKS delivers the 8·19 Mc/s carrier, amplitude modulated by the bi-polar video signals. The carrier level is approximately 5V peak, up to 50% modulated. This output is fed out to the hybrid network M3 (*Sect.* 3, *Chap.* 3).

(ii) In the video cabinet SKS delivers 8·19 Mc/s carrier, amplitude modulated by positive-going video signals. The carrier has a level of approximately 1·5V peak, modulated up to approximately 4·5V peak, and is fed out to the hybrid network M3.

(2) SKX

6·14 Mc/s carrier, amplitude-modulated by the bi-polar video signals. The carrier has a level of approximately 5V peak, up to 50% modulated, and is fed out to the hybrid network M3.

6. In the cancellation cabinet SKR and SKW are terminated with 75 ohms terminating connectors. In the video cabinet SKR is left open-circuit, the 75-ohm termination being provided in the signal comparator (coincidence) M3 (*Sect.* 5, *Chap.* 4).

Circuit description

7. The 6·0V heater supply for V1 and V6 (*fig.* 3) is obtained from TR1 which is supplied with 50c/s mains from plug PLB/7 (via FS1) and PLB/10. Resistors R25 and R26 serve as series droppers. The other power supply used with this unit is the +250V supplied at PLB/9. The 8·19 Mc/s and 6·14 Mc/s circuits are decoupled at the h.t. and heater lines thereby preventing any interaction between the circuits or feedback of r.f. into the mains and h.t. supplies. The mains and h.t. supplies are fed to the delay line driver from the +250V regulated power unit, housed in the same frame.

8. Considering the 8·19 Mc/s section of the unit, the incoming carrier at socket SKQ is applied via impedance matching resistors R1 and R2 to L2 at tap 1, the inductor being tuned to 8·19 Mc/s. V3 and C1 permit monitoring of the peak carrier level at SKE.

9. Diode V4 and inductor L2 form a simple crystal modulator which operates in the following manner. The peak-to-peak carrier level at 8·19 Mc/s across L2 is determined by the instantaneous d.c. voltage at V4 cathode since this d.c. voltage biases off V4 and thereby controls the level at which L2 is heavily damped by C2 and the 75-ohm socket SKR (*para.* 6). Therefore, the peak-to-peak carrier level across L2, applied to V1 grid, will vary continuously in response to any variable positive potential (i.e. in this case, the incoming video signals via SKN) applied to V4 cathode.

10. The positive-going −8μS pulse (monitored at SKD) applied via V2 modulates the carrier in a similar manner. Components L1, C20 and C2 form a 1 Mc/s low-pass filter to block the 8·19 Mc/s carrier from the inputs at SKN and SKP.

11. Valve V1 and its associated circuit form a tuned driver stage with potential divider R4-R5 providing a steady d.c. potential of approximately +5V at V1 grid. The suppressor grid is returned to cathode potential by R9 and decoupled by C4.

Resistor R8 provides a low impedance source at which to monitor, at SKF, the modulated carrier being applied to V1; it also provides a small amount of negative feedback. L3, the anode load of V1, is tuned to 8·19 Mc/s.

12. The impedance of the carrier source is matched to the input of the tuned driver stage by L2. Matching impedance L3 feeds the amplitude-modulated carrier to the low impedance output circuit at SKS. The envelope of the output from the tuned drive stage is made available for monitoring at SKG by V5, R11 and C7.

13. The 6·14 Mc/s modulator and tuned driver stage operate in a similar manner to that described above except that in this case there is no input at SKU. Although a positive-going timing pulse may be fed in at SKU if necessary, this facility is not required in the radar Type 84 equipment. Inductors L6 and L7 are tuned to 6·14 Mc/s.

Monitor point waveforms

14. Using the monitoring oscilloscope M1 (*Sect.* 7, *Chap.* 4) the waveforms and d.c. levels observed under operational conditions at monitor points SKC to SKM should be as shown in fig. 2.

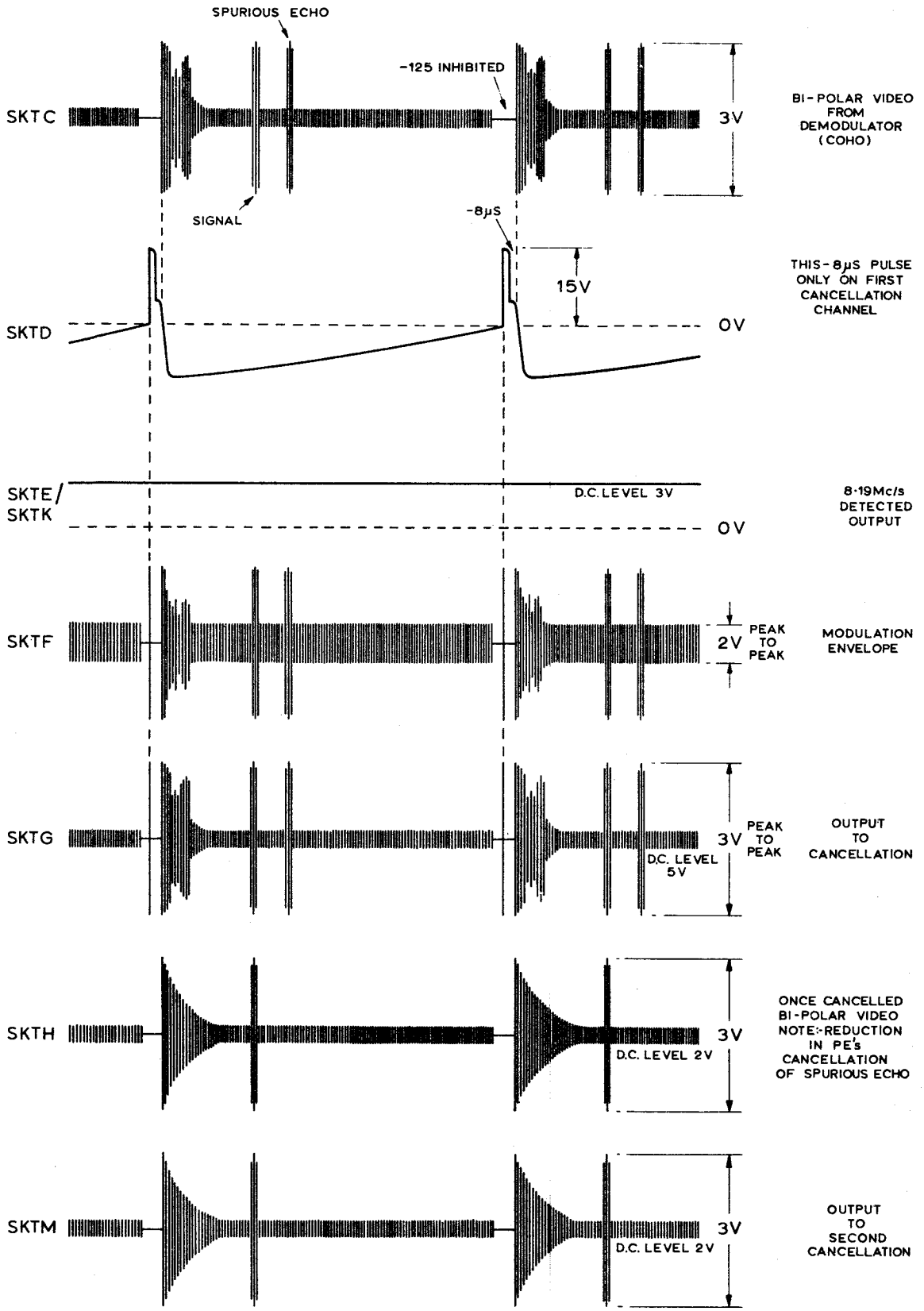


Fig. 2. Driver delay line M1: waveforms at monitor points

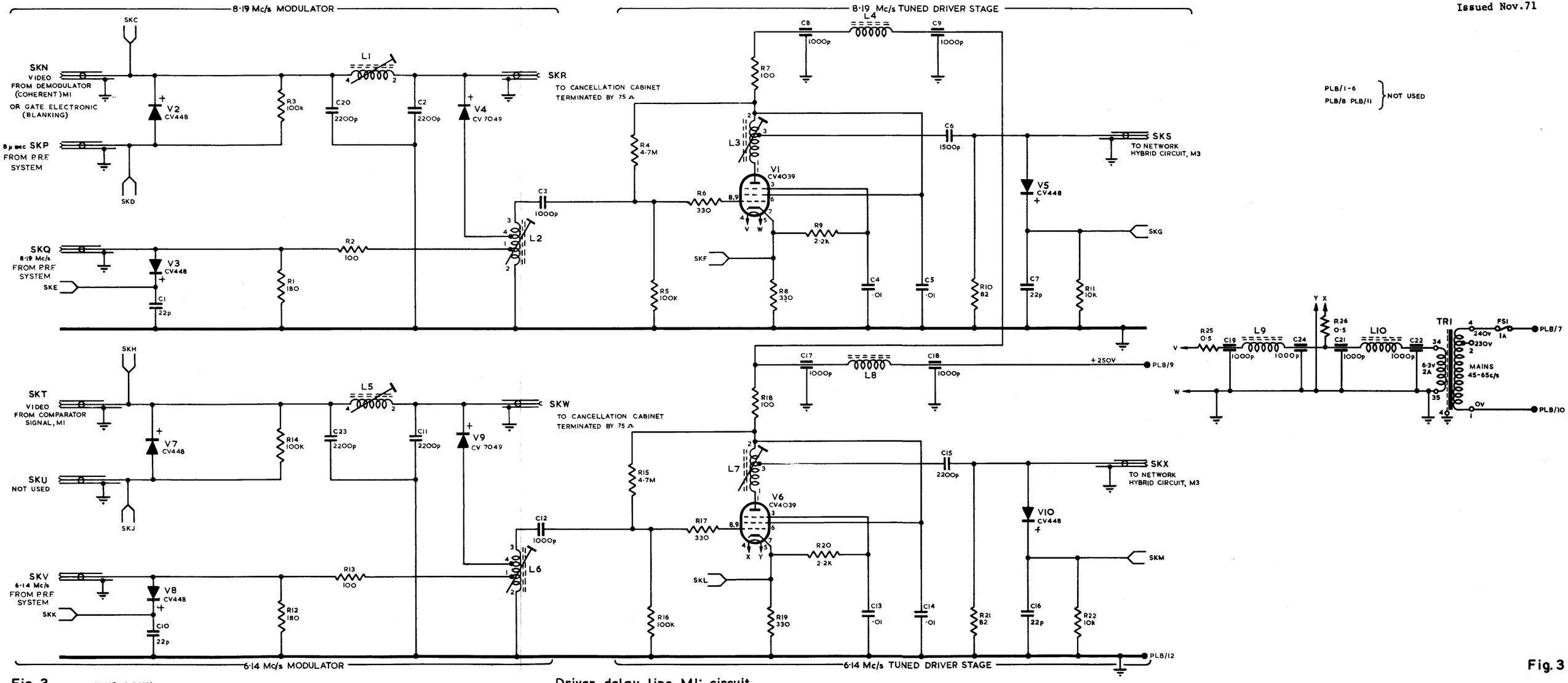


Fig. 3 D.200137. R.C.1646.

Driver delay line. MI: circuit

Fig. 3

Chapter 3

HYBRID CIRCUIT NETWORKS M3 AND M2

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

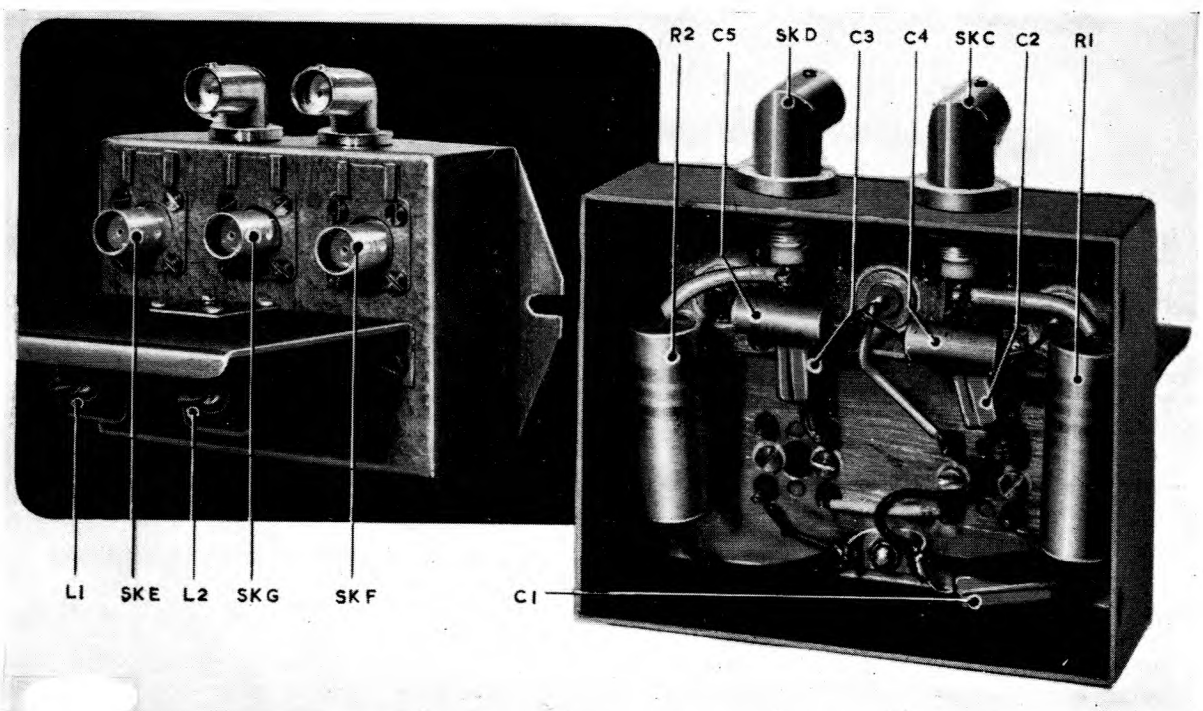


Fig. 1. Network, hybrid circuit, M3: general views

Introduction

1. There are three pairs of hybrid networks used in the radar Type 84 signal processing system. Each pair consists of one hybrid network M3 (*fig.* 1) and one hybrid network M2 (*fig.* 2). Two pairs are used in the cancellation channels, one pair for each channel. They are mounted in the bottom of the cancellation cabinet, above the fixed mercury delay cell (*Chap.* 4). Hybrid networks M3 are placed to the left ▶◀ and networks M2 to the right. The other pair is used in the p.r.f. discrimination channel, and is similarly located in the video cabinet.

2. The 6·14 and 8·19 Mc/s amplitude-modulated carriers from the delay line driver (*fig.* 3) are fed into the hybrid network M3 which combines the two carriers and provides a single line input to the mercury delay cell. This network also provides two single line inputs to the variable delay lines which also form part of the cancellation system (*Sect.* 1, *Chap.* 3).

3. When the signals have passed through the fixed mercury delay cell they are passed to the hybrid network M2 and separated into two modulated carriers again, and fed into separate signal comparators.

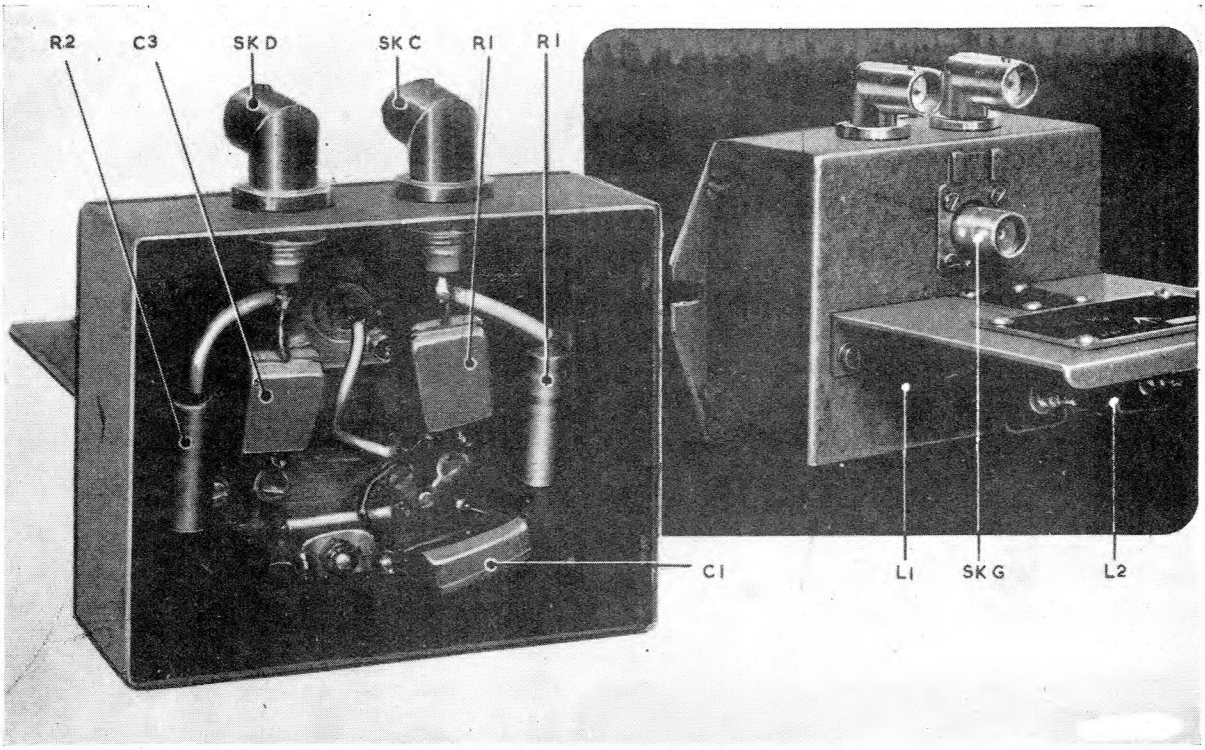


Fig. 2. Network, hybrid circuit, M2: general views

4. The purpose in combining the two modulated carriers, and passing them through one delay cell, is to ensure that the modulated video in both carriers is delayed by exactly the same amount; unequal delays would result in incomplete cancellation (*Sect.* 1, *Chap.* 3).

5. The networks also provide an impedance match between the delay line driver and the crystal transducers of the delay cell.

Performance characteristics

*Hybrid network M*3

6. *Inputs*

(1) SKC

(i) In the cancellation cabinet ; 8·19 Mc/s carrier, amplitude-modulated by bipolar video signals. This input has a steady carrier level of approximately 10V peak-to-peak, up to 50% modulated, and comes in from the delay line driver M1 (*Chap.* 2).

(ii) In the video cabinet; 8·19 Mc/s carrier, amplitude-modulated by positive-going video signals. This input has a steady carrier level of approximately 3V peak-to-peak, modulated up to approximately 10V peak-to-peak, and comes in from the delay line driver M1.

(2) SKD

(i) In the cancellation cabinet; 6·14 Mc/s carrier, amplitude-modulated by bipolar video signals. The steady carrier level is approximately 10V peak-to-peak, up to 50% modulated, and comes in from the delay line driver M1.

(ii) In the video cabinet ; SKD not used.

7. *Outputs*

(1) SKG

(i) In the cancellation cabinet; 8·19 Mc/s and 6·14 Mc/s carriers at approximately twice the input level, fed out to the mercury delay cell.

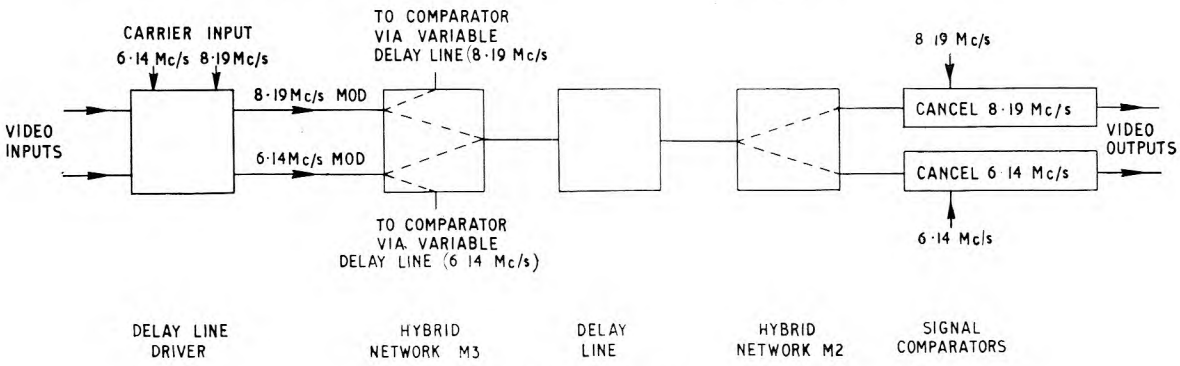


Fig. 3. Hybrid networks: block diagram

(ii) In the video cabinet; 8·19 Mc/s carrier at approximately twice the input level, fed out to the mercury delay cell.

(2) SKE

(i) In the cancellation cabinet; 8·19 Mc/s and 6·14 Mc/s carriers, attenuated approximately 50dB on the input, fed out to the 8·19 Mc/s section of the variable delay line M1 (*Chap.* 8).

(ii) In the video cabinet; SKE not used.

(3) SKF

(i) In the cancellation cabinet; 8·19 Mc/s and 6·14 Mc/s carriers, attenuated approximately 50dB on the input, fed out to the 6·14 Mc/s section of the variable delay line M1.

(ii) In the video cabinet; SKF not used.

Hybrid network M2

8. *Input*

SKG

(i) In the cancellation cabinet; 8·19 Mc/s and 6·14 Mc/s carriers approximately 50% amplitude-modulated by bi-polar video signals, from the mercury delay cell.

(ii) In the video cabinet; 8·19 Mc/s carrier, amplitude-modulated by positive-going video signals, from the mercury delay cell.

9. *Outputs*

(1) SKC

(i) In the cancellation cabinet; 8·19 Mc/s carrier at approximately half the input level, fed out to the signal comparator M1 (*Chap.* 5).

(ii) In the video cabinet; 8·19 Mc/s carrier at approximately half the input level, fed out to the signal comparator (coincidence) M3 (*Sect.* 5, *Chap.* 4).

(2) SKD

(i) In the cancellation cabinet; 6·14 Mc/s carrier at approximately half the input level, fed out to the signal comparator M2 (*Chap.* 6).

(ii) In the video cabinet; SKD not used.

Circuit description

10. Consider first the hybrid circuit M3 (*fig.* 4). The delay cell presents an input capacitance of 100 pF at SKG. ◀TR1▶ is tuned to 8·19 Mc/s by C1 and the delay cell input capacitance in series across terminals 1 and 3. L2 is tuned to 6·14 Mc/s by C1 and the delay cell input capacitance in parallel across terminals 1 and 4.

11. The input impedance of the delay cell is made to equal the impedance of C1 by adjustment of the length of the coaxial cable between SKG and the delay cell. *It is, therefore, important that the length of this lead is not altered.*

12. Considering the 8·19 M/cs signal entering at SKC, the signal is induced into the secondary of ◀TR1▶ which is tuned to electrically balance about terminal 2 (*fig.* 4). When ◀TR1▶ is tuned, ideally, there will be zero voltage at terminal 2 and therefore no 8·19 Mc/s signal developed across L2, or SKD. The secondary voltage is fed to the delay cell, and is also equally developed across C1.

13. The 6·14 Mc/s entering at SKD is applied at terminal 2 of L2, a tunable auto-transformer. Since ◀TR1▶ is tuned to balance at 8·19 Mc/s, the 6·14 Mc/s signal fed into ◀TR1▶ at terminal 2 will see an unbalance. By tuning L2, the balanced circuit of ◀TR1▶ secondary can also be balanced at 6·14 Mc/s, L2 providing the necessary impedance. When the 6·14 Mc/s circuit is balanced, equal currents (due to the 6·14 Mc/s signal) will flow in ◀TR1▶ secondary but in opposite directions, and therefore will not be induced into the primary. The 6·14 Mc/s signal is fed through one half of ◀TR1▶ secondary from terminal 2 to terminal 1 and developed across the delay cell, for the other path, terminals 2 and 3 of ◀TR1▶ and C1, terminate the signal.

14. The principal purpose of the transformers is impedance matching. They both give approximately a voltage gain of two, but this is incidental and the gain is lost when the two frequencies are separated in the hybrid network M2. The advantage of using step up transformers is that the voltage breakthrough induced into the primary is reduced. The leakage reactances of ◀TR1▶ and L2 are tuned out by capacitors C2 and C3.

15. C4 and C5 in series with the two outputs to the delay line provide approximately 50dB of attenuation when terminated in 75 ohms.

16. The hybrid network M2 (*fig.* 4) functions in a manner similar to that described for the hybrid M3. The input at SKG is mixed 8·19 Mc/s and 6·14 Mc/s carriers. ◀TR1▶ accepts the 8·19 Mc/s component, feeding it out at SKC, and L2 accepts the 6·14 Mc/s component, feeding it out at SKD. In this case ◀TR1▶ and L2 provide a voltage attenuation of approximately two.

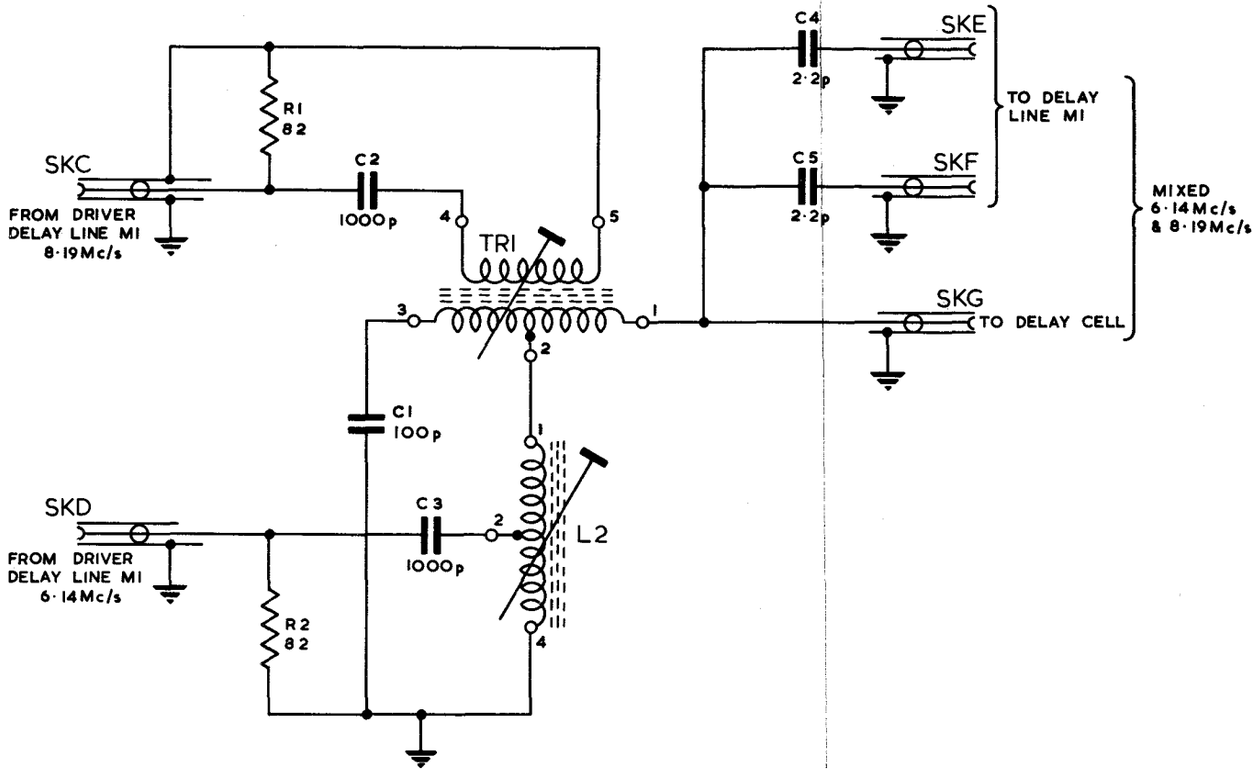


Fig. 4 NETWORK, HYBRID CIRCUIT, M3

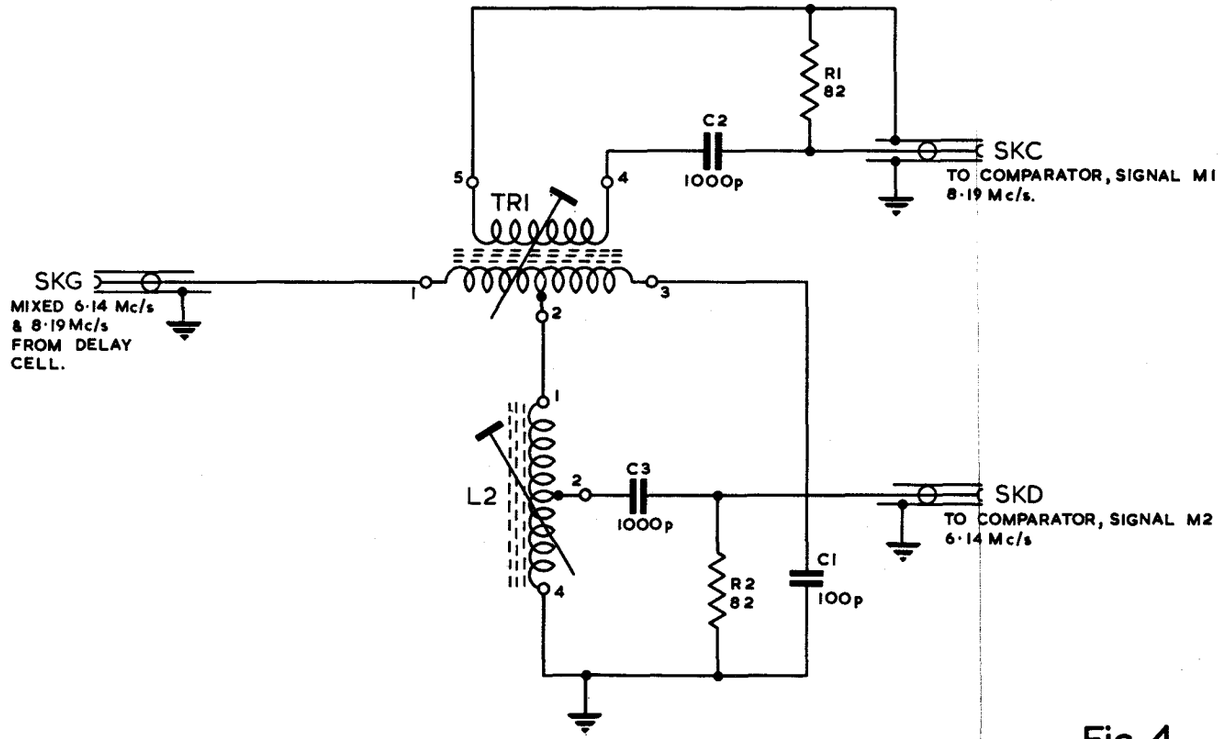


Fig. 4 NETWORK, HYBRID CIRCUIT, M2

Hybrid networks: circuits

Chapter 4

FIXED DELAY LINES

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

Introduction

Caution . . .

The following points should be carefully noted :—

(1) *If it becomes necessary to change the delay line it must be handled very carefully and not dropped or bumped in any way. It must be maintained in a horizontal position and only transported by means of the truck, hand platform* (*Cat. No.* 3920–99–913–1222).

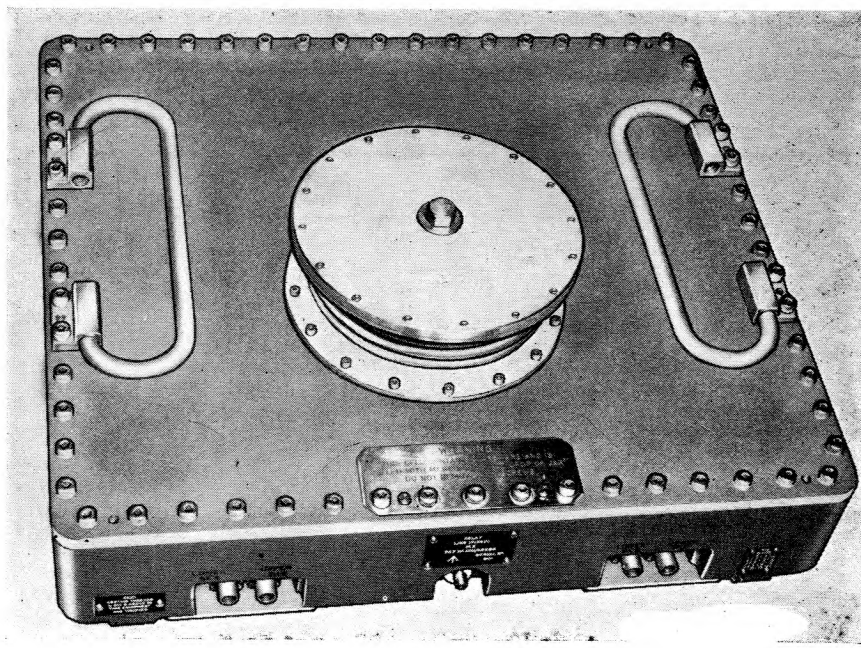
(2) *When the unit is being removed from the cabinet it must not be held or stopped by means of the bellows assembly on the lid.*

(3) *No attempt should be made to lift or carry the unit by fewer than four men, due to its weight* (2 *cwt*).

(4) *Under no circumstances should the lid be removed.*

(5) *The sealed-in set screws which hold the plate glass reflectors in position must not be tampered with.*

1. The delay line (fixed) (*fig.* 1) forms part of the cancellation system used for MTI purposes. It contains two independent mercury delay paths, one associated with channel B and the other with



(C40299)

Fig. 1. Fixed delay line : external view

channel A. The unit is located in the base of the cancellation cabinet and its purpose is to delay signals by one pulse period. The principles of the mercury delay line are given in para. 7 *et seq.*

2. Initially, in each cancellation channel, the video signals are superimposed on an 8·19 Mc/s carrier in the driver (delay line) M1 (*Chap.* 2) and are applied to the delay line via the network, hybrid circuit M3 (*Chap.* 3). They are then propagated through the mercury via a quartz crystal transducer mounted in one corner. After being reflected within the unit the necessary number of times to give the required delay, the signals are received by a further quartz crystal transducer and passed to the comparator, signal M1 (*Chap.* 5) via the network, hybrid circuit M2 (*Chap.* 3). Here they are amplified and compared with the undelayed video signals in a subtractor circuit and the resultant output signals (once cancelled, once delayed) are passed back to the driver (delay line) where they are again superimposed on a further r.f. carrier (6·14 Mc/s). The modulated carrier is again applied to the delay line in the same manner as before. This twice delayed output is then compared with the previous once delayed output in a subtractor circuit in the comparator, signal M2 (*Chap.* 6). The resultant output (twice cancelled, twice delayed) is applied together with the once cancelled, one delayed output to the amplifier (video rectifier) M3 (*Sect.* 5). Fig. 2 shows the function of the delay line in channel B.

3. The p.r.f. of the station is controlled by the delay line. A −8 microsecond timing pulse is passed through the delay line and compared with a similar but undelayed timing pulse in the controller (p.r.f.) M.1 (*Chap.* 10). The comparison is used to correct any errors in the p.r.f. and for this reason it is necessary for the delay line to be matched to the required p.r.f. To this end, separate delay lines designated delay lines (fixed) M2, M3, M4, M5 and M7 are used, the difference between these units being confined to small changes in the internal dimensions.

Performance characteristics

Delay times

4. The delay times of the various types of delay line (fixed) and their associated p.r.f.s are as follows :—

(1) M2 4053 microseconds ± 4 microseconds (246·7 p.p.s.).

(2) M3 3981 microseconds ± 4 microseconds (251·2 p.p.s.).

(3) M4 3909 microseconds ± 4 microseconds (255·8 p.p.s.).

(4) M5 3945 microseconds ± 4 microseconds (253·5 p.p.s.).

(5) M7 4017 microseconds ± 4 microseconds (248·9 p.p.s.).

All these delay times are for an ambient temperature of 20°C. The times vary approximately 1 microsecond/°C over the range 14°C to 30°C, rising at the higher temperatures and falling at the lower. The overall attenuation of each delay line lies between 70 and 90 dB for each carrier frequency.

Inputs

5. The unit requires carriers at 8·19 Mc/s and 6·14 Mc/s at a level of 20V peak-to-peak, modulated up to 50 per cent by video signals, at sockets SKA and SKC.

Outputs

6. The unit delivers signals at 8·19Mc/s and 6·14Mc/s, the level being determined by the overall attenuation of the line, at sockets SKB and SKD.

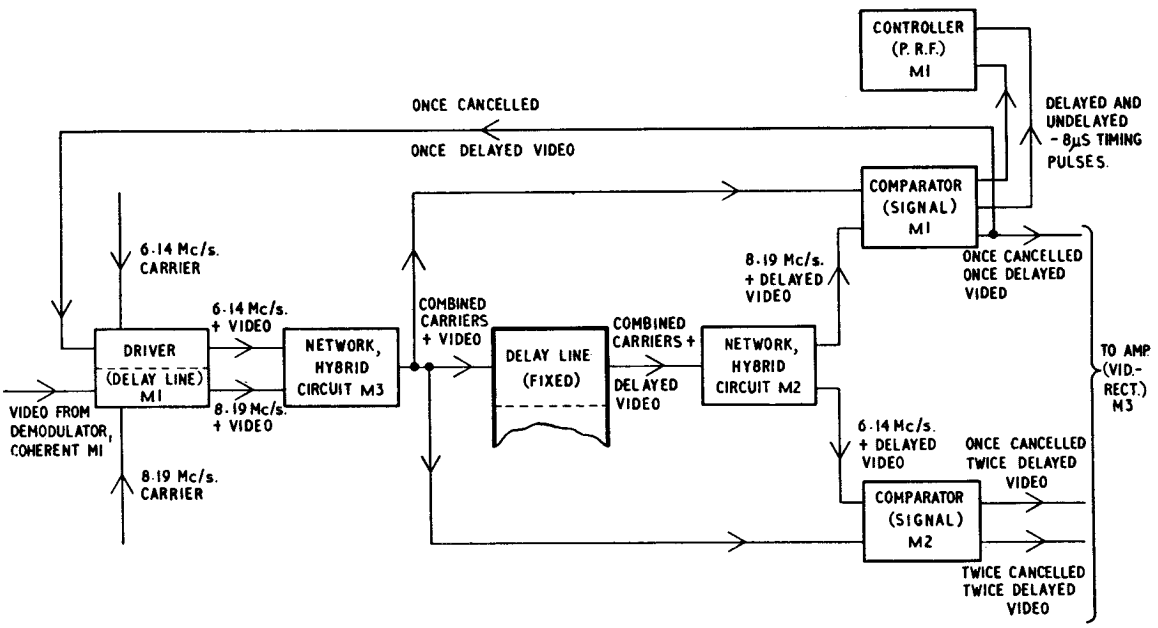


Fig. 2. Functional block schematic (channel B only)

Principles of the mercury delay line

7. The delay path through the unit must have the following properties :—

(1) A sufficiently large inherent bandwidth to reproduce the applied signals with a high degree of fidelity.

(2) Good amplitude linearity to preserve small echoes from moving targets both superimposed on or near large fixed echoes and also in other areas.

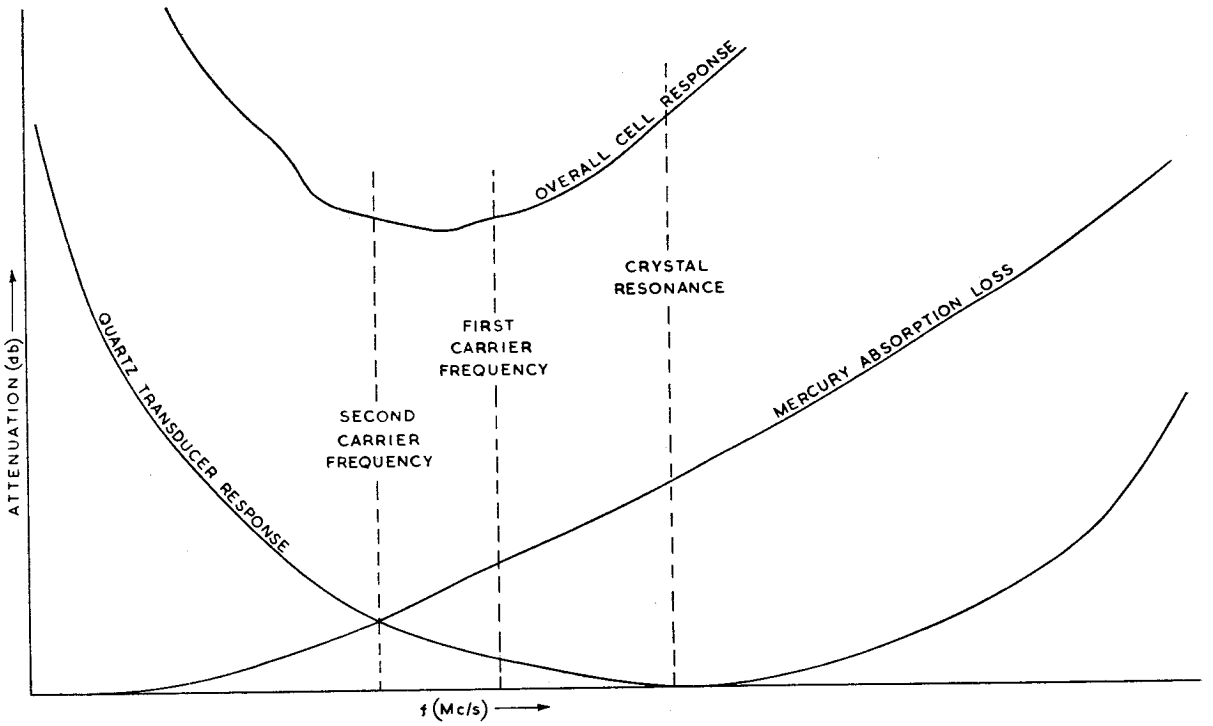
(3) With its associated circuits, it should not introduce noise or stray signals.

8. The delay required is as listed in para. 4 and the type of line used in the signal processing equipment is based on the principle of ultrasonic propagation in mercury. In this instance mercury is used because it has an acoustic impedance which is high enough to permit sufficient damping on the transducers to provide the necessary large bandwidth and also offers a relatively low attenuation to the passage of ultrasonic waves.

9. The design of the unit is based upon 45° reflections from the inside faces of a rectangle of optically flat glass plates. As this angle is greater than the minimum angle for total reflection, no energy enters the reflectors. The dimensions of the reflectors determine the delay time of the unit and are so chosen that every part of the mercury, with the exception of small " clearance " areas, is traversed by the beam twice, i.e. once in each of two directions normal to one another. The path length is given by the product of the required delay time and the acoustic velocity for mercury. By a suitable choice of beamwidth it is possible to obtain the required path length with a minimum number of reflections thus giving the lowest possible line attenuation.

10. The transmitting and receiving transducers are quartz crystals which, for a given resonant frequency, have an acoustic bandwidth of the order of half that frequency. Transmission is zero at zero frequency, which may lead to distortion in the video signals if they are applied directly to the line. Thus, to take full advantage of the bandwidth of the line, the video signals are impressed on to an r.f. carrier wave, and it is this amplitude-modulated wave which is propagated through the delay line.

11. The quartz transducers are cut to resonate at a frequency higher than that of the carrier wave, the reason for this being that the absorption loss in the mercury combined with the response of the transducers provides the lowest level of attenuation at a band of frequencies somewhat lower than the resonant frequency of the quartz transducers. The transducer frequency and the carrier wave frequency are selected so that the carrier lies at or near the lowest attenuation point, whilst the transducer frequency is outside the carrier bandwidth. The relationship is shown in fig. 3. The level of attenuation is also affected by other factors, namely, a certain amount of attenuation caused by mismatching and a beam spreading loss which does not materially affect the shape of the line attenuation curve. The mismatching occurs due to the transducer impedance being much higher than the load impedance and remains constant at all frequencies, thus generally raising the level of attenuation of the line. The figure also shows how,



(C40299)

Fig. 3. Response characteristics of a mercury delay line

in a double path delay line, the two carrier frequencies are spaced along the minimum attenuation band to give the necessary bandwidth for adequate video response.

12. To lessen the beam spreading effect and to prevent signals which pass close to the receiving transducer during reflection from giving a spurious output, the beam is collimated in the horizontal plane. This is done by placing studs in the " clearance " areas mentioned in para. 9. In the vertical plane, collimation is achieved by diagonal ridges formed on the top and bottom of the line. These ridges suppress glancing reflections which might lead to a longer delay path out of phase with the main path. This would result in spurious pulses being present at the output. The effect of beam collimation is shown in fig. 4.

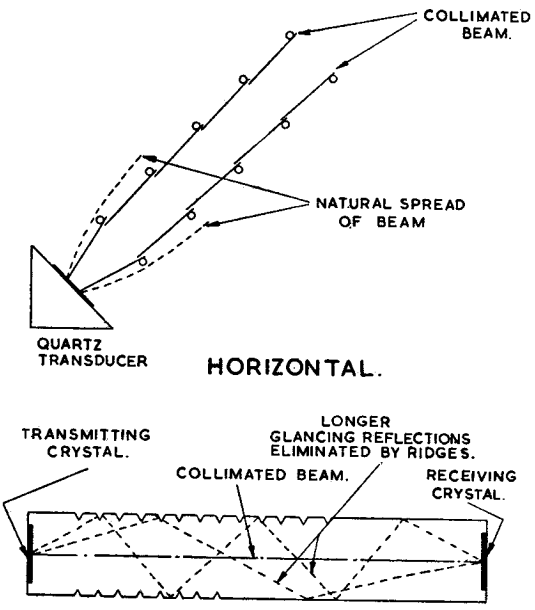


Fig. 4. Beam collimation

Mechanical description

13. The base of the delay line is a box-shaped iron casting. The grade of iron used has been chosen for its relatively high resistance to fracture and to corrosion. To enclose the delay elements an iron lid is attached to the base by socket-headed screws. All metal parts, other than those made of stainless steel, are nickel plated. The line is separated into two delay paths by means of a moulded fibre-glass separation plate. Over the delay area, the base, separation plate and lid have a diagonal ridged formation on their surfaces for the purposes of beam collimation. In addition, and for the same reason, the lid is fitted with studs which locate in holes drilled in the base. Three of these studs form supports for the separation plate which is held in position by lock nuts. Holes are drilled in the separation plate to equalize the mercury temperature between the two delay paths. The line is completely filled with mercury and all air is bled out. A bellows assembly is fitted to the lid to allow for thermal expansion of the mercury.

14. The reflectors which form the line are made of optically flat plate glass and are mounted round the delay area in an accurate rectangular formation. They are held in position by mild steel shoes adjusted by set screws. These shoes allow for expansion due to temperature changes. The arrangement of the interior of the line is shown in fig. 5.

15. Each transducer consists of an X-cut quartz crystal mounted on rubber. Two of these are fitted to a glass wedge to make up the double-path transmitting or receiving element. The wedges are set in corners of the line at either end of one reflector. The back of each crystal is sputtered with gold to form an electrode, with a length of 36 s.w.g. wire soldered to it to provide a connection to the external coaxial socket. The other electrode is formed by the mercury. The edges of the crystal and its rubber backing are sealed over with epoxide resin to prevent mercury leaking to the back of the crystal, thus short-circuiting it.

Electrical description

16. The 8·19 Mc/s and 6·14 Mc/s carriers modulated with video signals are applied to the delay line at socket SKA for channel B and socket SKC for channel A. The outputs for each channel are taken from sockets SKB and SKD respectively. The pairs of sockets are designated UPPER and LOWER on the unit to denote to which delay path they are connected.

Replacement of coaxial sockets

Caution . . .

Every care must be taken in carrying out this operation as fracturing of the crystal connecting wires will result in the unit becoming unserviceable and very difficult to repair.

17. During service it is possible that the coaxial input and output sockets may become damaged. These may be replaced in the following manner :—

(1) Remove the unit from the cabinet, observing the cautionary notice at the beginning of this chapter.

(2) Place it on a firm bench with the side carrying the sockets overhanging, so that the plates covering the socket connections underneath the unit are accessible.

(3) Remove the plates to expose the underside of the sockets and the crystal connections.

(4) Remove the connector strip assembly carrying the damaged socket and support it below the unit without allowing the crystal connections to take the weight of the strip.

(5) Remove the adhesive tape securing the plastic sleeving to the socket pin.

(6) Unsolder and unwrap the wire connection from the pin with a pair of fine nose pliers (a short length of wire has been left unsoldered for this purpose).

(7) Remove the damaged socket and fit a new one.

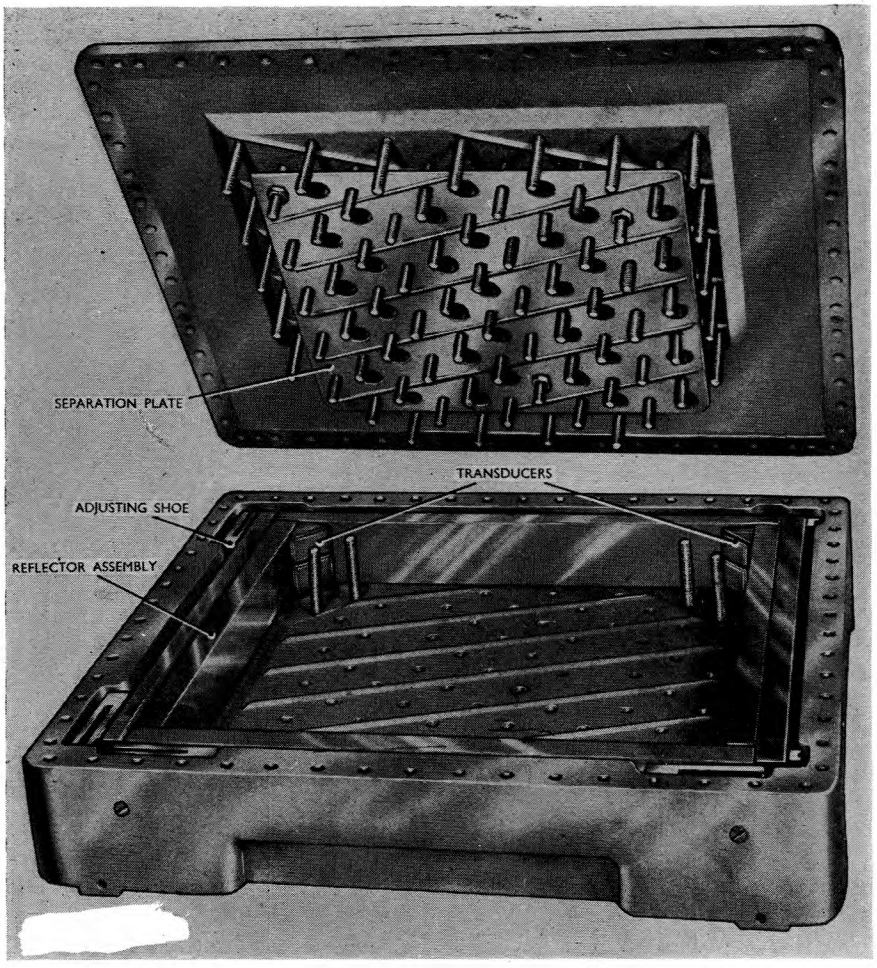


Fig. 5. Fixed delay line : internal view

(8) If it is necessary to remake the end of the connection, the plastic sleeving over the wire must be burnt off with a soldering iron (on no account should any form of stripping tool be used). Sufficient length of wire has been left to enable this to be done.

(9) The end of the wire should be wrapped round the pin of the replacement socket, leaving approximately 1/16 inch free, and soldered.

(10) Secure the plastic sleeving to the socket pin with about three turns of adhesive tape.

(11) Replace connector strip assembly.

(12) Replace cover plates, taking care that any excess lead is located in the groove in the casting where it may be held in position with adhesive tape.

The method of terminating the crystal connections is shown in fig. 6.

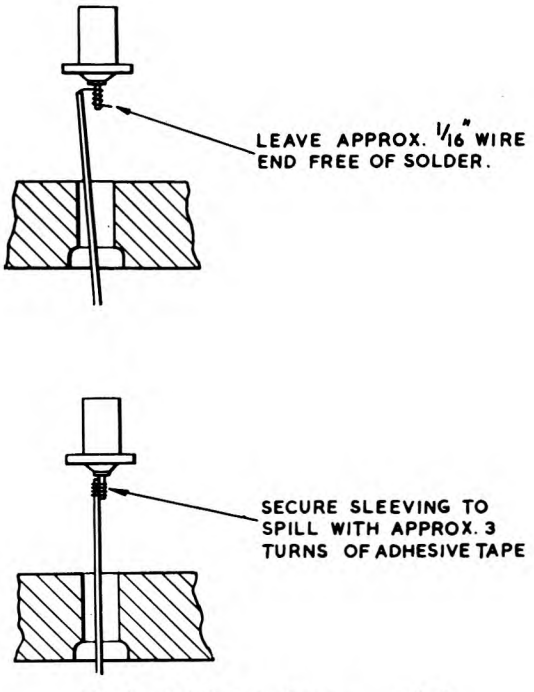


Fig. 6. Soldering of coax. sockets

Hand platform truck

18. The hand platform truck (*fig.* 7) is designed for the transportation of fixed and variable delay lines. It consists of a welded steel angle framework fitted with runners to accommodate the delay lines. These runners are similar to those used to carry the delay lines in the cancellation and video cabinets.

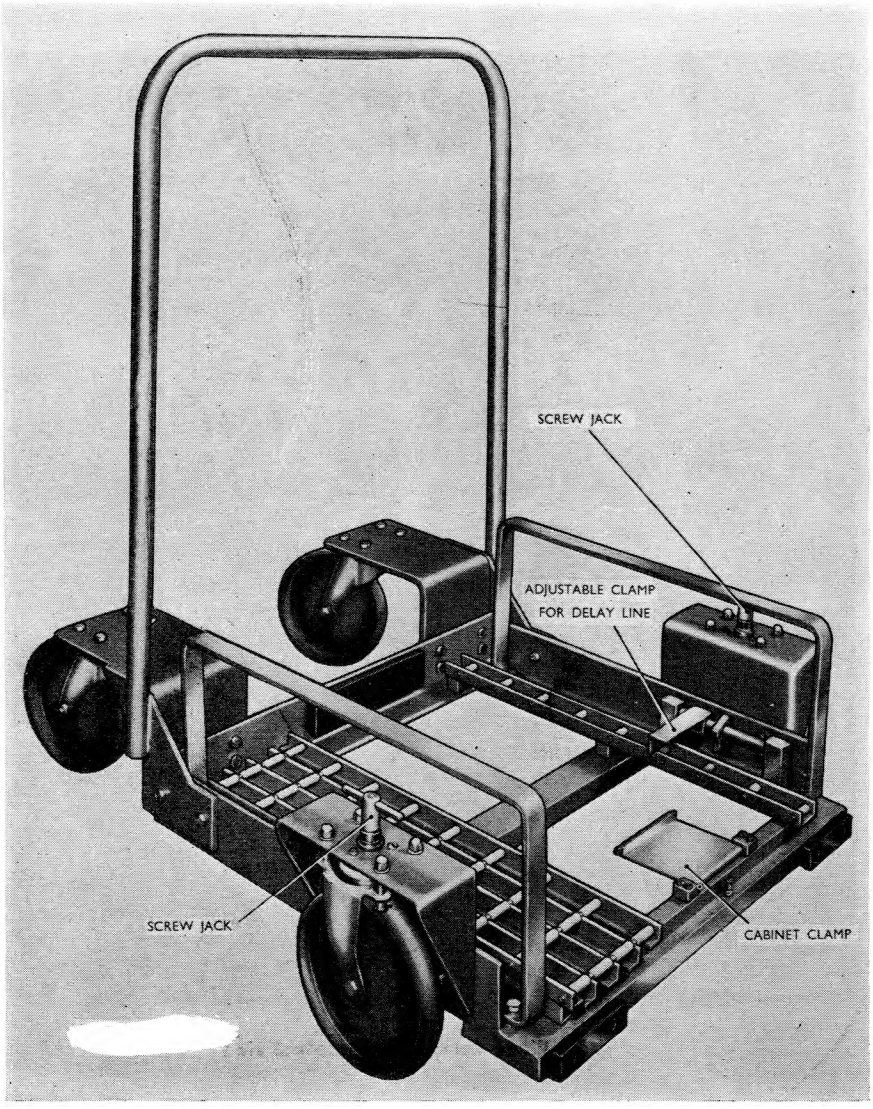


Fig. 7. Hand platform truck : general view

19. The truck is fitted with four castor wheels, the front two being adjustable in height by means of individual screw jacks. These enable the truck to be set to the correct height for different cabinets. A hinged plate fitted to the front of the truck is used to anchor the truck to the cabinet when a delay line is being changed and a pair of rubber buffers prevent damage to the truck or the cabinet during this operation. An adjustable clamp is provided to prevent the delay line from moving during transportation. The truck handle is sprung into two tubes welded to brackets fitted to either side of the main framework and can be removed to facilitate manhandling the delay line off the truck.

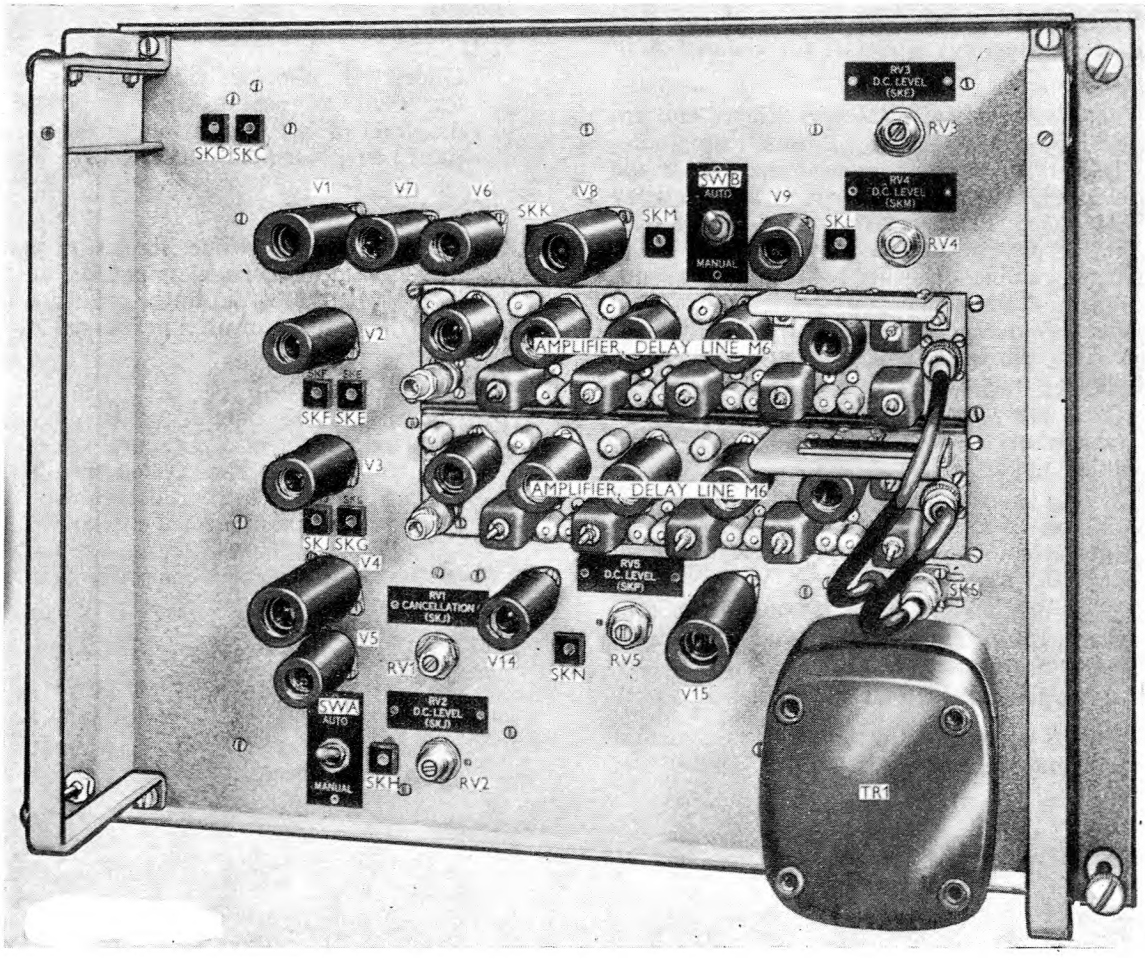
Chapter 5

COMPARATOR (SIGNAL) M1

LIST OF CONTENTS

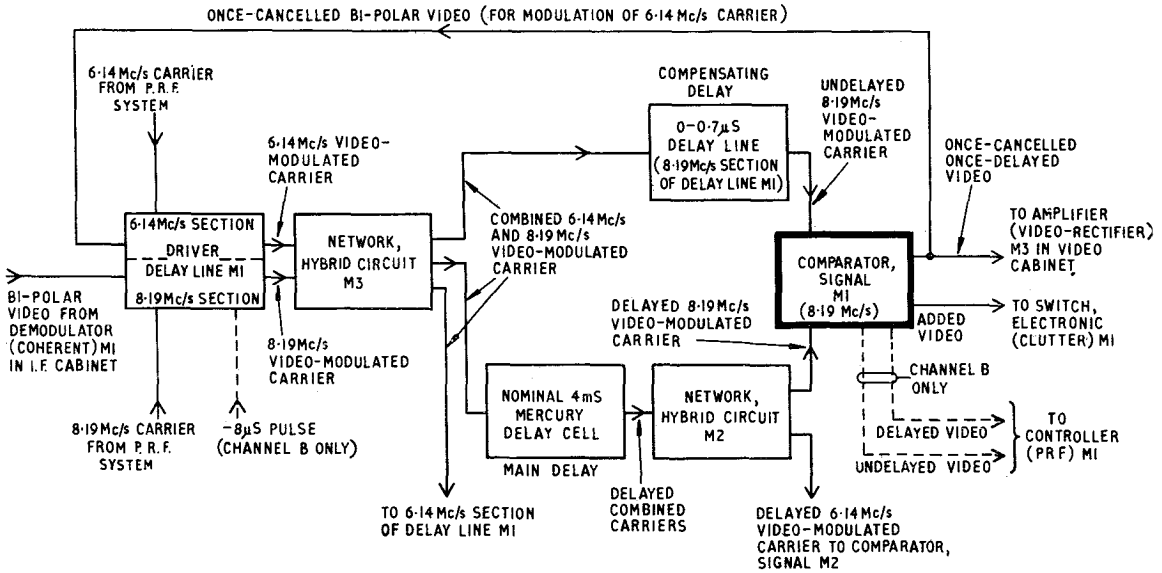
LIST OF TABLES

LIST OF ILLUSTRATIONS



(C37836)

Fig. 1. Comparator, signal M1: front view



◀Fig. 2. First cancellation stage: block diagram▶

Introduction

1. The primary function of the signal comparator M1 (*figs.* 1 *and* 4) is to provide the first stage of cancellation in the double cancellation MTI system (*Sect.* 1, *Chap.* 3). One signal comparator M1 is used in cancellation channel A and a second identical unit is used in channel B. A functional block schematic of this 8·19 Mc/s stage (the first stage of cancellation) is shown for channel A in Fig. 2.

2. The signal comparator accepts delayed and undelayed 8·19 Mc/s carriers, each amplitude-modulated with bi-polar video signals from the hybrid circuit network M2 (*Chap.* 3) and the delay line M1 (*Chap.* 8) respectively. The two carriers are first separately amplified by two 8·19 Mc/s amplifiers (amplifier delay line M6) mounted as sub-assemblies on the signal comparator unit. These amplifiers (*Chap.* 7) each provides a detected video output from which the signal comparator produces the following outputs:—

(1) A *cancelled* output, resulting from the subtraction of the two signal amplitudes by a differential amplifier.

(2) An *added* output, resulting from the addition of the two signal amplitudes by a differential amplifier. This output is also used for clutter switching.

(3) A delayed and an undelayed video output (channel B only; not used in channel A). This output is also used for p.r.f. control purposes.

(4) A delayed video output which is not used.

3. The two signal comparators M1 are located in frames 3 and 2 respectively, of the cancellation cabinet.

Performance characteristics

Inputs

4. (1) SKQ

Delayed 8·19 Mc/s carrier, amplitude-modulated with bi-polar video signals, from the hybrid circuit network M2 (*Chap.* 3).

(2) SKR

Undelayed 8·19 Mc/s carrier, amplitude-modulated with bi-polar video signals, from the delay line M1 (*Chap.* 8).

Outputs

5. (1) SKT

Undelayed bi-polar video signals of not less than 2V peak-to-peak amplitude at a d.c. level of +10V, fed out to the controller (p.r.f.) M1. Not used in channel A.

(2) SKU

Delayed bi-polar video signals of not less than 2V peak-to-peak amplitude at a d.c. level of +10V, fed out to the controller (p.r.f.) M1 (*Chap.* 10). Not used in channel A.

(3) SKV and SKW

Cancelled video output, up to 3V peak-to-peak amplitude, at a d.c. level of +2V, fed out to the amplifier (video rectifier) M3 (*Sect.* 5, *Chap.* 2) in the video cabinet, and to the 6·14 Mc/s section of the delay line driver M1 (*Chap.* 2). These outputs are terminated in 75 ohms at the delay line driver by a 75 ohm terminating connector.

(4) SKX

Delayed video output of up to 3V peak-to-peak amplitude at a d.c. level of +2V. This output is not used, and is terminated with a 75 ohm connector.

(5) SKY

Added bi-polar video output, up to 3V peak-to-peak amplitude, at a d.c. level of +2V, fed out to the electronic switch (clutter) M1 (*Chap.* 9). This output is terminated in 75 ohms at the input to the clutter switch by a 75 ohm terminating connector.

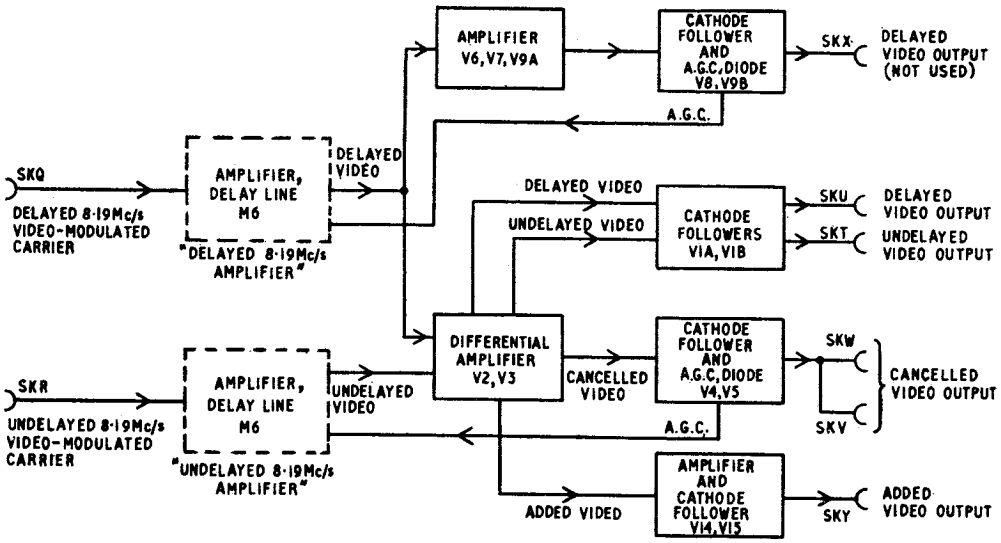


Fig. 3. Comparator, signal M1 : block diagram

Brief circuit description

6. A block diagram of the signal comparator is shown in fig. 3. The delayed and undelayed video-modulated 8·19 Mc/s carriers are first amplified and the video signals detected in two 8·19 Mc/s amplifiers. Both detected video signals, delayed and undelayed, are then applied to a differential amplifier to obtain an added video output, a cancelled output, and delayed and undelayed video outputs.

7. The delayed and undelayed outputs from the differential amplifier are fed out via cathode followers and used for p.r.f. control purposes. The added output is amplified and fed out via a cathode follower and used for clutter switching purposes. The cancelled output is applied to a cathode follower output and an a.g.c. circuit which feeds out the cancelled output and also produces an a.g.c. signal to be fed back to the undelayed 8·19 Mc/s amplifier.

8. In addition to being applied to the differential amplifier, the delayed video signal from the delayed 8·19 Mc/s amplifier is also amplified and fed to a cathode follower output and a.g.c. circuit similar to that referred to in para. 7. This circuit, in addition to feeding out the delayed video signal, also produces an a.g.c. signal which is fed back to the delayed 8·19 Mc/s amplifier.

Circuit description

Power supplies

9. Heater voltages for valves V1 to V9, V14 and V15, and for valves in the two 8·19 Mc/s amplifiers are obtained from TR1. This transformer is supplied with 50c/s mains from the input at PLB/7, via FS1, and PLB/10. Valves of the CV4039 type (V4, V8 and V15) require a 6·0V heater supply and therefore R72, R73 and R74 are included as series dropping resistors. The +250V supply from the +250V regulator at the top of the appropriate frame is brought in across PLB/9 (+250V) and PLB/12 (earth). This +250V input is also supplied to the two 8·19 Mc/s amplifiers. The −250V supply is brought to the unit via the +250V regulator at PLB/11 (−250V) and PLB/12 (earth).

Note . . .

Owing to the large number of valve heaters supplied by TR1, there is a high current surge upon switching-on when the valves are cold. For this reason, a fuse-link of the anti-surge type is used for FS1. The requirement is indicated by a green dot adjacent to the fuseholder on the unit panel.

Input circuit

10. Amplification and detection of the 8·19 Mc/s delayed and undelayed carrier inputs at SKQ and SKR is effected by the separate 8·19 Mc/s amplifier sub-assemblies M6 (*Chap.* 7). Resistors R1 and R2 at the input to the undelayed amplifier provide approximately 30dB attenuation, which, when combined with the 40dB attenuation of the undelayed signals from the hybrid circuit network M3 (*Chap.* 3), approximately balances the attenuation suffered by the delayed signals in passing through the mercury delay cell (*Chap.* 4).

Differential amplifier

11. The delayed and undelayed bi-polar video signals detected in the 8·19 Mc/s amplifiers are of 3V peak-to-peak amplitude at a d.c. level of +3V and are applied to the grids of V2 and V3 respectively. V2 and V3 and their associated circuit form a differential amplifier which functions in the following manner.

12. When the delayed and undelayed pulses of bi-polar video arriving at V2 and V3 grids are in phase and of equal amplitude, the signal returns are from either a fixed target or a target moving radially at one of the *blind velocities* (*Sect.* 1, *Chap.* 5). The potentials at the cathodes will tend to follow those at the grids so that an added output will be developed at the junction of R16 and R18.

This added output is approximately equal in amplitude to the signals being applied to the grids, so that the effective grid-to-cathode potential of V3 remains unchanged and therefore the resultant output at V3 anode is negligible and the signal has been effectively cancelled.

13. Consider the condition when the delayed and undelayed pulses of bi-polar video are in antiphase, indicating returns from moving targets. V2 cathode potential will tend to follow the grid potential negatively while V3 cathode follows its grid positively. The resultant added output at the junction of R16 and R18 is therefore zero. This condition produces a signal between the grid and cathode of V3 and therefore an output at V3 anode.

14. At all other phase differences between 0 deg. and 180 deg. there will be both an added and a cancelled output from the amplifier, the former tending towards zero and the latter towards maximum as the phase difference increases. Rectifier V10 prevents the potential at the cathodes of V2 and V3 from falling below earth potential and thereby prevents maximum heater-to-cathode potential being exceeded under fault conditions.

15. The added output produced across R17 is amplified by V14 and fed out via cathode follower V15 and R69 to the output socket SKY, the overall gain of the stage being unity. The d.c. level at socket SKY is set to approximately +2V by RV5.

P.R.F. pulse outputs

16. Delayed and undelayed signals are separately developed across R16 and R18 at the cathodes of V2 and V3 respectively. These signals are fed out via the cathode followers V1a and V1b and sockets SKU and SKT to the p.r.f. controller unit M1. The signal that controls the p.r.f. (by producing a nominal 500c/s (2 × p.r.f.) waveform in the p.r.f. controller, which in turn drives the motor in the crystal oscillator) is the −8 microseconds positive-going pulse. This pulse is made free from noise and other extraneous signals by the −125 microseconds to 0 microseconds blanking circuit in the demodulator (coherent) M1 (*Sect.* 2, *Chap.* 10).

Cancelled output and a.g.c. circuit

17. The cancelled output at V3 anode is d.c. coupled to the cathode follower V4 and fed to the output sockets SKV and SKW via resistor R28. The overall gain of V3 and V4 is approximately unity. A.G.C. for the undelayed 8·19 Mc/s amplifier is taken from RV2, by way of smoothing circuit R29 and C5, and is at a d.c. level of approximately −3·5V. Double diode V5, the cathode of which is taken to the junction of R54 and R55 across the −250V supply, prevents the a.g.c. level rising beyond −2V, thereby protecting the valves in the 8·19 Mc/s amplifier from being over-run. Potentiometer RV2 thus controls, via the a.g.c. loop, the d.c. level of the signals being applied to V3 grid and hence, due to the d.c. coupling between V3 and V4, the d.c. level at the output of V4 (monitored at SKJ). This output d.c. level is set to approximately +2V by adjustment of RV2.

18. The CANCELLATION (SKJ) balance control RV1 varies both the amplitude and the d.c. level of the signal applied to V4 grid from V3 anode. By this means RV1 controls the d.c. potential at V4 cathode and hence, via the a.g.c. loop described above, the d.c. level of the signals applied to V3 grid. This d.c. level is made equal to the potential at V6 grid (monitored at SKK), at approximately +3V. The two controls RV1 and RV2 interact, and therefore careful adjustment of each is necessary so as to obtain the required d.c. levels at test sockets SKG and SKJ.

Delayed output and a.g.c. circuit

19. The function of amplifier V6–V9 is similar to that described for V2–V5, except that there is no signal input to V6 grid. This grid is maintained at a d.c. level of about +3V by the circuit V9a, R33, R34 and R35. The video output from the delayed 8·19 Mc/s amplifier is applied to V7 grid, and from V7 anode is d.c. coupled to the cathode follower V8 and fed to socket SKX via the attenuating resistor R56. Automatic gain control for the delayed 8·19 Mc/s amplifier is obtained by way of RV4 and associated circuit in a similar manner to that described for the undelayed 8·19 Mc/s amplifier.

20. The d.c. level at the output of V8 (monitored at SKM) is set by RV4 to +2V, and the d.c. level at the control grids of V2 and V7 is set by RV3 to be the same potential as that at V6 grid. This ensures that the grids of V6 and V7 are at the same d.c. level. Similarly, the grids of V2 and V3 are at the same d.c. level, this being essential for effective cancellation to take place. As with RV1 and RV2, careful adjustment of RV3 and RV4 is necessary so that the required d.c. levels are obtained at test sockets SKE and SKM.

MANUAL/AUTO switches

21. When set to MANUAL, switches SWA and SWB connect the circuit for manual gain control, as required during testing, instead of a.g.c. to the undelayed and delayed 8·19 Mc/s amplifiers respectively. This is achieved for the undelayed amplifier V4, V5, by connecting the junction of R26 and RV2 to earth and controlling the gain by RV2; and, for the delayed amplifier V6, V7, and V9a, by connecting the junction of R50 and RV4 to earth and controlling the gain by RV4. For normal operation, a.g.c. is applied by setting the switches to AUTO.

22. The undelayed delay line amplifier M6 has its output impedance modified by components C3 and R7 to simulate the input impedance of V7 across the output of the delayed delay line amplifier M6, thus ensuring that the two 8·19 Mc/s amplifiers are terminated in similar impedances.

Diodes V11, V13, V16

23. Connected to the outputs from cathode followers V4, V8 and V15 is a compensating circuit consisting of a diode returned to a potential divider network (e.g. V11 and R31–R32 for V4). This circuit distorts slightly the positive-going signals to compensate for a similar distortion of the negative-going signals due to the type of valve used (CV4039). The resulting output is bi-polar with slight amplitude distortion but still symmetrical about its d.c. level.

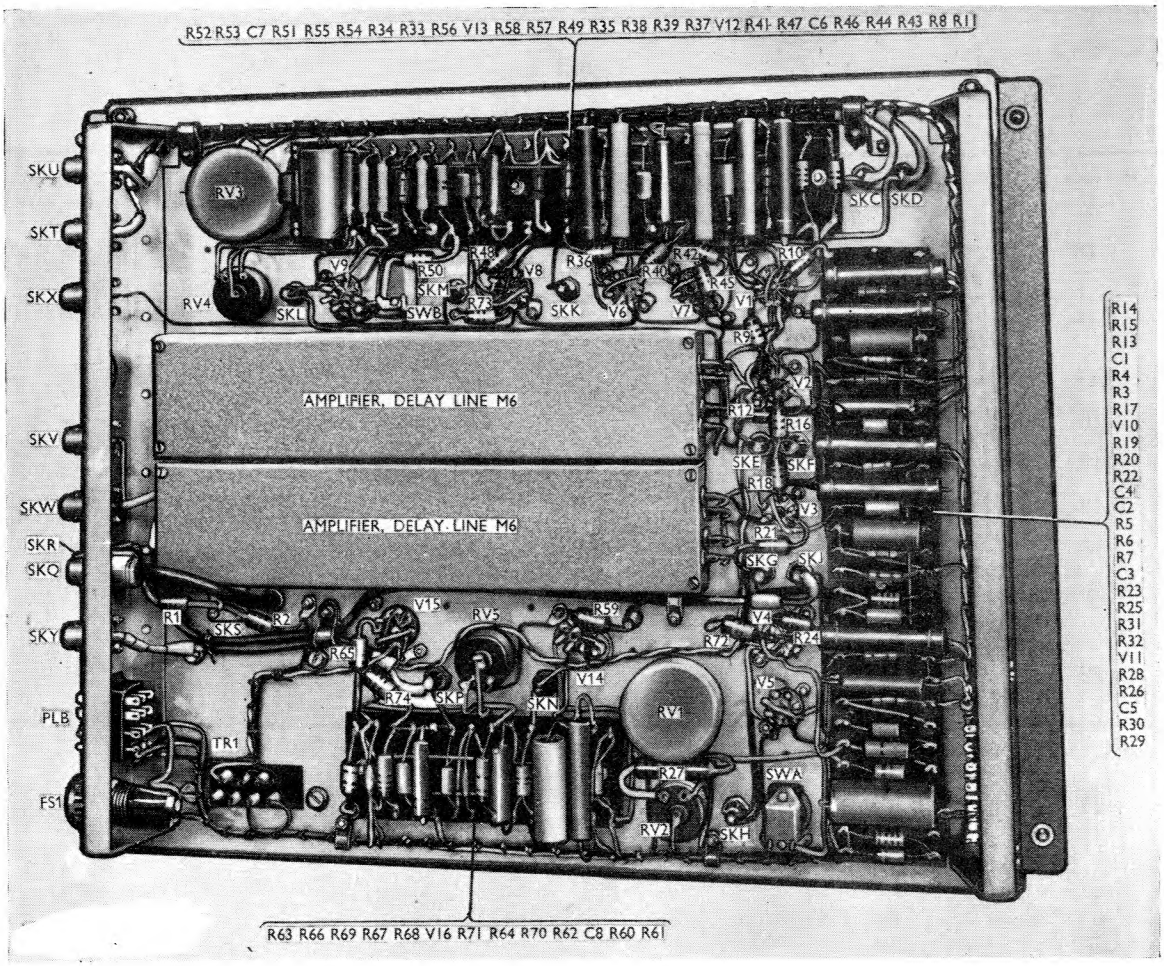


Fig. 4. Comparator, signal M1 : rear view

Monitor points

24. Twelve monitoring sockets, SKC to SKP, are provided on the unit and these are primarily intended for checking the various d.c. levels during the initial setting-up procedure. Under operating conditions the only waveforms that can be observed at these sockets are bi-polar video signals. Using the monitoring oscilloscope M1 (*Sect. 7, Chap. 4*), the approximate peak-to-peak amplitudes of these video signals, and the steady d.c. levels about which they are centred, are listed in Table 1.

TABLE 1
Monitor point waveforms

Monitoring socket	Waveform to be observed
SKC	Delayed video signals, greater than 2V peak-to-peak, at +10V.
SKD	Undelayed video signals, greater than 2V peak-to-peak, at +10V.
SKE	Delayed video signals, up to 3V peak-to-peak, at +3V.
SKF	Added video signals, up to 3V peak-to-peak, at +3V.
SKG	Undelayed video signals, up to 3V peak-to-peak, at +3V.
SKH	Either an a.g.c. voltage level of −3·5V (SWA set to AUTO position), or a variable level of between −2V and −12V (SWA set to MANUAL position). No video signals are observed at this point.
SKJ	Cancelled video output, up to 3V peak-to-peak, at +2V.
SKK	+3V. No video signals are observed at this point.
SKL	Either an a.g.c. voltage level of −3·5V (SWB set to AUTO position), or a variable level of between −12V and −2V (SWB set to MANUAL position). No video signals are observed at this point.
SKM	Delayed video signals, up to 3V peak-to-peak, at +2V.
SKN	Added video signals, up to 3V peak-to-peak, at +2V.
SKP	Added video signals, up to 3V peak-to-peak, at +2V.

Multimeter readings

25. With the multimeter Type 100 connected to socket SKA of the unit via a plug-to socket adaptor, the meter readings obtained should be as indicated in Table 2.

TABLE 2

Multimeter readings

SKA poles	Multimeter switch position	Stage checked	Measured across	Reading	Tolerance	
1,13	A	Delayed amplifier	R4, C1	0·4	±0·08	
2,14	B	Undelayed amplifier	R5, C2	0·4	±0·08	
3,15	C	V2	R15	0·45	±0·09	
4,16	D	V3	R20	0·45	±0·09	
5,17	E	V4	R25	0·55	±0·11	i.e. ±20%
6,18	F	V6	R39	0·45	±0·09	
7,19	G	V7	R44	0·45	±0·09	
8,20	H	V8	R49	0·55	±0·11	
9,21	J	V14	R61	0·55	±0·11	
10,22	K	V15	R66	0·55	±0·11	

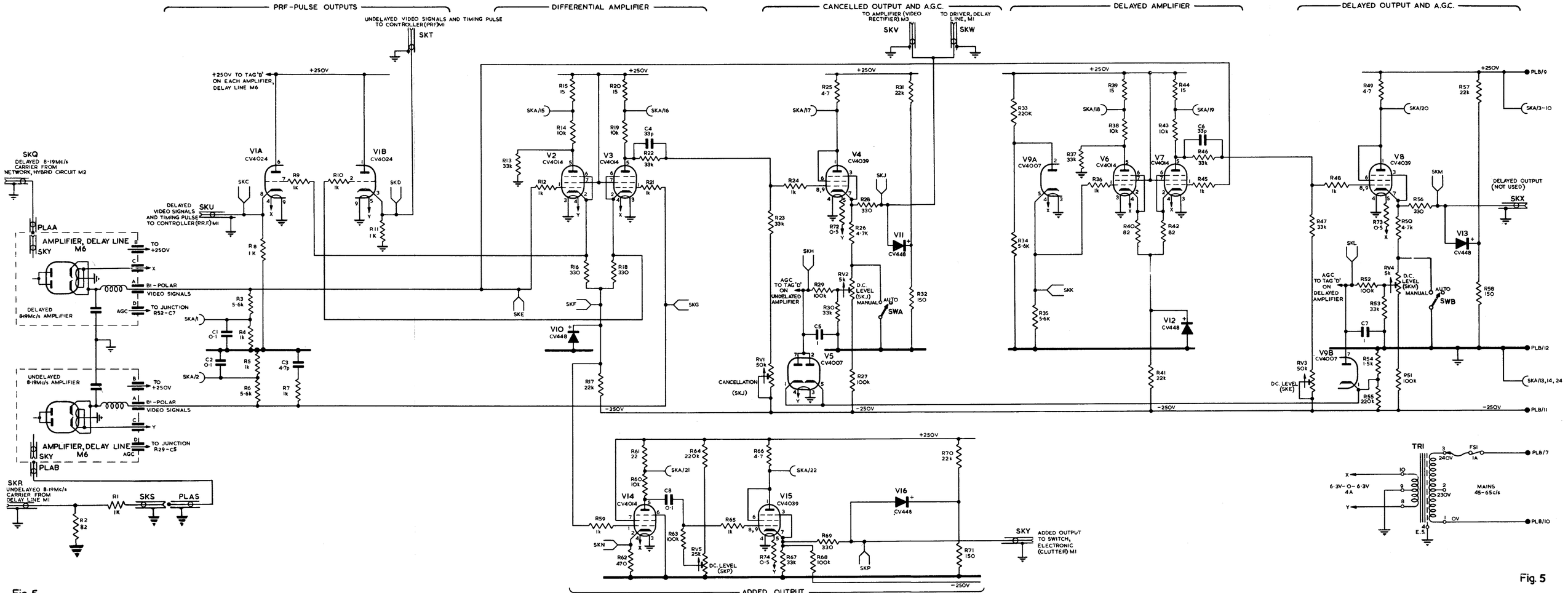


Fig. 5

Comparator signal MI: circuit

Fig. 5

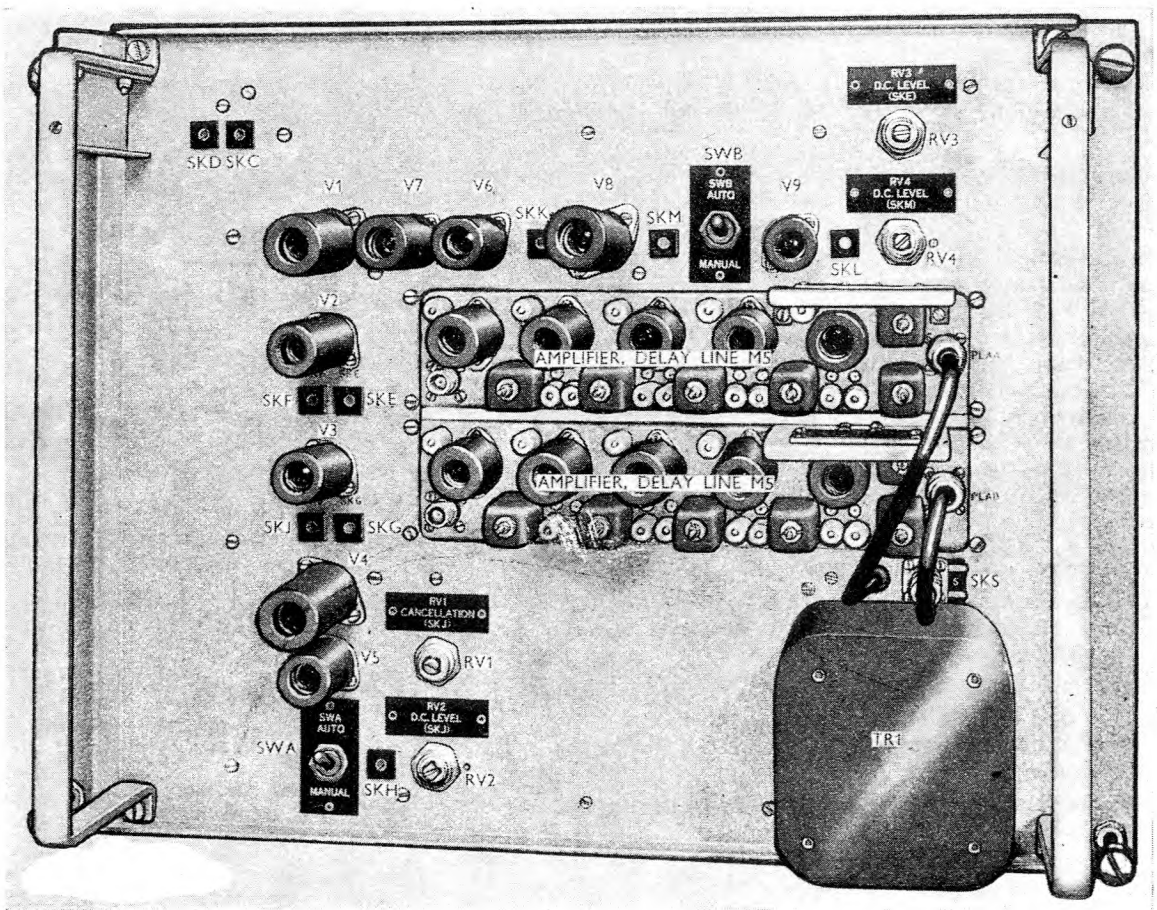
Chapter 6

COMPARATOR (SIGNAL) M2

LIST OF CONTENTS

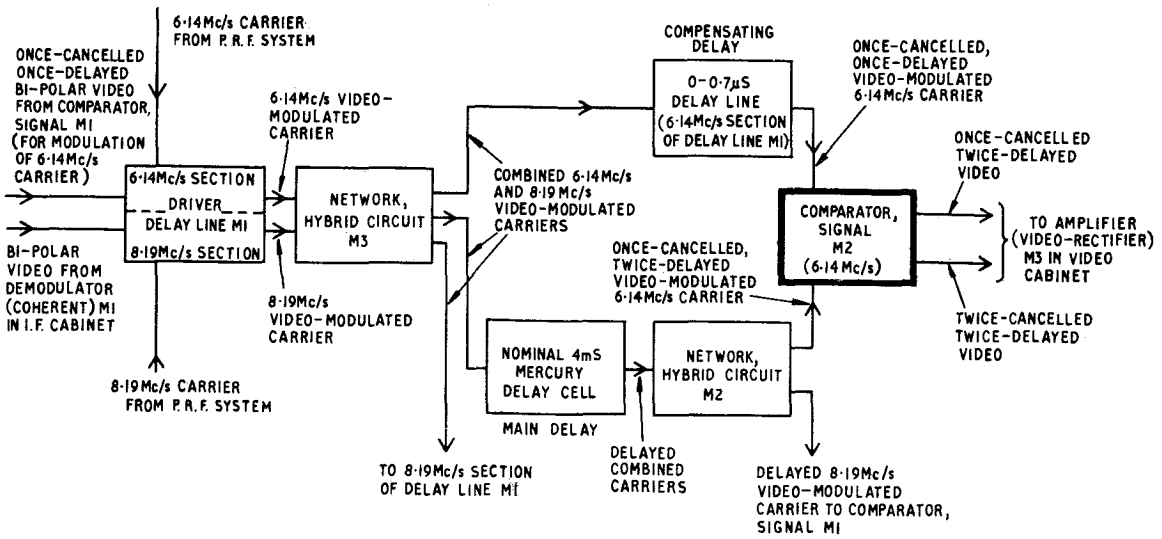
LIST OF TABLES

LIST OF ILLUSTRATIONS



(C37836)

Fig. 1. Comparator signal M2: front view



◀Fig. 2. Second cancellation stage: block diagram▶

Introduction

1. The function of the signal comparator M2 (*figs.* 1 *and* 4) is to provide the second stage of cancellation in the double cancellation MTI system (*Sect.* 1, *Chap.* 3). One signal comparator M2 is used in cancellation channel A and a second identical unit is used in channel B. A functional block schematic of this 6·14 Mc/s stage (the second stage of cancellation) is shown for channel A in fig. 2.

2. The signal comparator M2 accepts 6·14 Mc/s carriers, each amplitude-modulated with once-cancelled bi-polar video signals. The bi-polar video signals have already undergone a first stage of cancellation at a carrier frequency of 8·19 Mc/s (*Chap.* 5) and therefore the inputs to this signal comparator, will have both passed through the mercury delay cell; the signal received from the hybrid circuit network M2 (*Chap.* 3) having been twice delayed in this manner and that from the delay line M1 (*Chap.* 8) only once delayed, so that to the signal comparator M2, these inputs are presented as twice delayed and once delayed signals respectively. The two carriers are first separately amplified by two 6·14 Mc/s amplifiers (amplifier delay line M5) mounted as sub-assemblies on the signal comparator unit. These amplifiers (*Chap.* 7) each provides a detected video output from which the signal comparator produces the following outputs:—

(1) A cancelled output, resulting from the subtraction of the two signal amplitudes by a differential amplifier.

(2) A twice delayed and a once-delayed video output which are not used.

(3) A twice delayed video output.

3. The two signal comparators M2 are located in frames 3 and 2 respectively, of the cancellation cabinet.

Performance characteristics

Inputs

4. (1) SKQ

6·14 Mc/s carrier, amplitude-modulated with twice delayed once-cancelled bi-polar video signals, from the hybrid circuit network M2 (*Chap.* 3).

(2) SKR

6·14 Mc/s carrier, amplitude-modulated with once delayed, once-cancelled bi-polar video signals, from the delay line M1 (*Chap.* 8).

Outputs

5. (1) SKT

Once-delayed bi-polar video signals of not less than 2V peak-to-peak amplitude at a d.c. level of +10V. This output is not used.

(2) SKU

Twice delayed bi-polar video signals of not less than 2V peak-to-peak amplitude at a d.c. level of +10V. This output is not used.

(3) SKV and SKW

Twice-cancelled, twice delayed video output, up to 3V peak-to-peak amplitude, at a d.c. level of +2V, fed out from socket SKV to the amplifier (video rectifier) M3 (*Sect.* 5, *Chap.* 2) in the video cabinet. The output at socket SKW is not used. These outputs are terminated in 75 ohms at the input to the amplifier (video-rectifier) by a 75 ohm terminating connector.

(4) SKX

Once-cancelled, twice delayed video output of up to 3V peak-to-peak amplitude at a d.c. level of +2V, fed out to the amplifier (video rectifier) M3 (*Sect.* 5, *Chap.* 2). This output is terminated in 75 ohms at the input to the amplifier (video-rectifier) by a 75 ohm terminating connector.

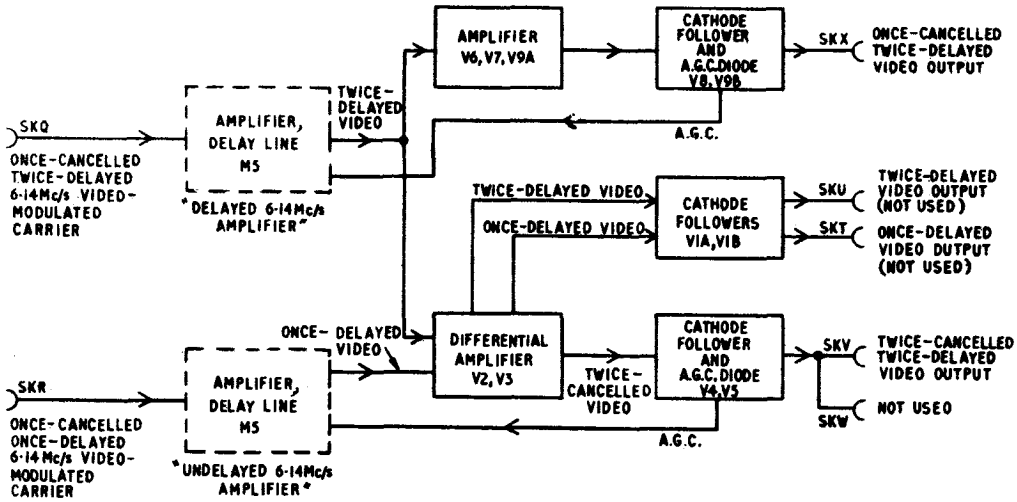


Fig. 3. Comparator signal M2 : block diagram

Brief circuit description

6. A block diagram of the signal comparator is shown in fig. 3. The twice delayed and once delayed video-modulated 6·14 Mc/s carriers are first amplified and the video signals detected in two 6·14 Mc/s amplifiers. Both detected video signals are then applied to a differential amplifier to obtain a cancelled output, and two twice-delayed video outputs.

7. The twice-delayed and once-delayed outputs from the differential amplifier are fed via cathode followers to output sockets on the unit, and may, if necessary, be used for p.r.f. control purposes (this facility is normally provided by the comparator M1). The cancelled output is applied to a cathode follower output and a.g.c. circuit that, in addition to feeding out the cancelled output, produces an a.g.c. signal to be fed back to the undelayed 6·14 Mc/s amplifier.

8. In addition to being applied to the differential amplifier, the twice-delayed video signal from the delayed 6·14 Mc/s amplifier is also amplified and fed to a cathode follower output and a.g.c. circuit similar to that referred to in para. 7. This circuit, in addition to feeding out the twice-delayed video signal, also produces an a.g.c. signal which is fed back to the delayed 6·14 Mc/s amplifier.

Circuit description

Power supplies

9. Heater voltages for valves V1 to V9 and for valves in the two 6·14 Mc/s amplifiers are obtained from TR1. This transformer is supplied with 50c/s mains from the input at PLB/7, via FS1, and PLB/10. Valves of the CV4039 type (V4 and V8), require a 6·0V heater supply and therefore R59 and R60 are included as series dropping resistors. The +250V supply from the +250V regulator at the top of the appropriate frame is brought in across PLB/9 (+250V) and PLB/12 (earth). This +250V input is also supplied to the two 6·14 Mc/s amplifiers. The −250V supply is brought to the unit via the +250V regulator at PLB/11 (−250V) and PLB/12 (earth).

Note . . .

Owing to the large number of valve heaters supplied by TR1 there is a high current surge upon switching-on when the valves are cold. For this reason, a fuse-link of the anti-surge type is used for FS1. The requirement is indicated by a green dot adjacent to the fuseholder on the unit panel.

Input circuit

10. Amplification and detection of the 6·14 Mc/s twice-delayed and once-delayed carrier inputs at SKQ and SKR is effected by the separate 6·14 Mc/s amplifier sub-assemblies M5 (*Chap.* 7). Resistors R1 and R2 at the input to the undelayed amplifier provide approximately 30dB attenuation, which, when combined with the 40dB attenuation of the undelayed signals from the hybrid circuit network M3 (*Chap.* 3), approximately balances the attenuation suffered by the twice-delayed signals in passing through the mercury delay cell (*Chap.* 4).

Differential amplifier

11. The twice-delayed and once-delayed bi-polar video signals detected in the 6·14 Mc/s amplifiers are of 3V peak-to-peak amplitude at a d.c. level of +3V and are applied to the grids of V2 and V3 respectively. V2 and V3 and their associated circuit form a differential amplifier which functions in the following manner.

12. When the twice-delayed and once-delayed pulses of bi-polar video arriving at V2 and V3 grids are in phase and of equal amplitude, the signal returns are from either a fixed target or a target moving radially at one of the *blind velocities* (*Sect.* 1, *Chap.* 5). The potentials at the cathodes will tend to follow those at the grids so that an added output will be developed at the junction of R16 and R18. This added output is approximately equal in amplitude to the signals being applied to the grids so that the effective grid-to-cathode potential of V3 remains unchanged and therefore the resultant output at V3 anode is negligible, and the signal has been effectively cancelled.

13. Consider the condition when the twice-delayed and once-delayed pulses of bi-polar video are in antiphase. V2 cathode potential will tend to follow the grid potential negatively while V3 cathode follows its grid positively. The resultant added output at the junction of R16 and R18 is therefore zero. This condition produces a signal between the grid and cathode of V3 and therefore an output at V3 anode.

14. At all other phase differences between 0 deg. and 180 deg., there will be both an added and a cancelled output from the amplifier, the former tending towards zero and the latter towards maximum as the phase difference increases. Rectifier V10 prevents the potential at the cathodes of V2 and V3 from falling below earth potential and thereby prevents maximum heater-to-cathode potential being exceeded under fault conditions.

15. Twice-delayed and once-delayed signals are separately developed across R16 and R18 at the cathodes of V2 and V3 respectively. These signals are fed out via the cathode followers V1a and V1b and sockets SKU and SKT.

Cancelled output and a.g.c. circuit

16. The cancelled output at V3 anode is d.c. coupled to the cathode follower V4 and fed to the output sockets SKV and SKW via resistor R28. The overall gain of V3 and V4 is approximately unity. A.G.C. for the undelayed 6·14 Mc/s amplifier is taken from RV2, by way of smoothing circuit R29 and C5, and is at a d.c. level of approximately −3·5V. Double diode V5, the cathode of which is taken to the junction R54–R55 across the −250V supply, prevents the a.g.c. level rising beyond −2V, thereby protecting the valves in the 6·14 Mc/s amplifier from being over-run. Potentiometer RV2 thus controls, via the a.g.c. loop, the d.c. level of the signals being applied to V3 grid and hence, due to the d.c. coupling between V3 and V4, the d.c. level at the output of V4 (monitored at SKJ). This output d.c. level is set to approximately +2V by adjustment of RV2.

17. The CANCELLATION (SKJ) balance control RV1 varies both the amplitude and the d.c. level of the signal applied to V4 grid from V3 anode. By this means RV1 controls the d.c. potential at V4 cathode and hence, via the a.g.c. loop described above, the d.c. level of the signals applied to V3 grid. This d.c. level is made equal to the potential at V6 grid (monitored at SKK), at approximately +3V. The two controls RV1 and RV2 interact, and therefore careful adjustment of each is necessary so as to obtain the required d.c. levels at test sockets SKG and SKJ.

Delayed output and a.g.c. circuit

18. The function of amplifier V6–V9 is similar to that described for V2 to V5, except that there is no signal input to V6 grid. This grid is maintained at a d.c. level of about +3V by the circuit V9a, R33, R34 and R35. The video output from the delayed 6·14 Mc/s amplifier is applied to V7 grid, and from V7 anode is d.c. coupled to the cathode follower V8 and fed to socket SKX via the attenuating resistor R56. Automatic gain control for the delayed 6·14 Mc/s amplifier is obtained by way of RV4 and associated circuit in a similar manner to that described for the undelayed 6·14 Mc/s amplifier.

19. The d.c. level at the output of V8 (monitored at SKM) is set by RV4 to +2V, and the d.c. level at the control grids of V2 and V7 is set by RV3 to be the same potential as that at V6 grid. This ensures that the grids of V6 and V7 are at the same d.c. level. Similarly, the grids of V2 and V3 are at the same d.c. level, this being essential for effective cancellation to take place. As with RV1 and RV2, careful adjustment of RV3 and RV4 is necessary so that the required d.c. levels are obtained at test sockets SKE and SKM.

MANUAL/AUTO *switches*

20. When set to MANUAL, switches SWA and SWB connect the circuit for manual gain control, as required during testing, instead of a.g.c. to the undelayed and delayed 6·14 Mc/s amplifiers respectively. This is achieved for the undelayed amplifier by connecting the junction of R26 and RV2 to earth and controlling the gain by RV2; and, for the delayed amplifier, by connecting the junction of R50 and RV4 to earth and controlling the gain by RV4. For normal operation, a.g.c. is applied by setting the switches to AUTO.

21. The undelayed delay line amplifier M5 has its output impedance modified by components C3 and R7 to simulate the input impedance of V7 across the output of the delayed delay line amplifier M5, thus ensuring that the two 6·14 Mc/s amplifiers are terminated in similar impedances.

Diodes V11 and V13

22. Connected to the outputs from cathode followers V4 and V8 is a compensating circuit consisting of a diode returned to a potential divider network (e.g. V11 and R31–R32 for V4). This circuit distorts slightly the positive-going signals to compensate for a similar distortion of the negative-going signals due to the type of valve used (CV4039). The resulting output is bi-polar with slight amplitude distortion but still symmetrical about its d.c. level.

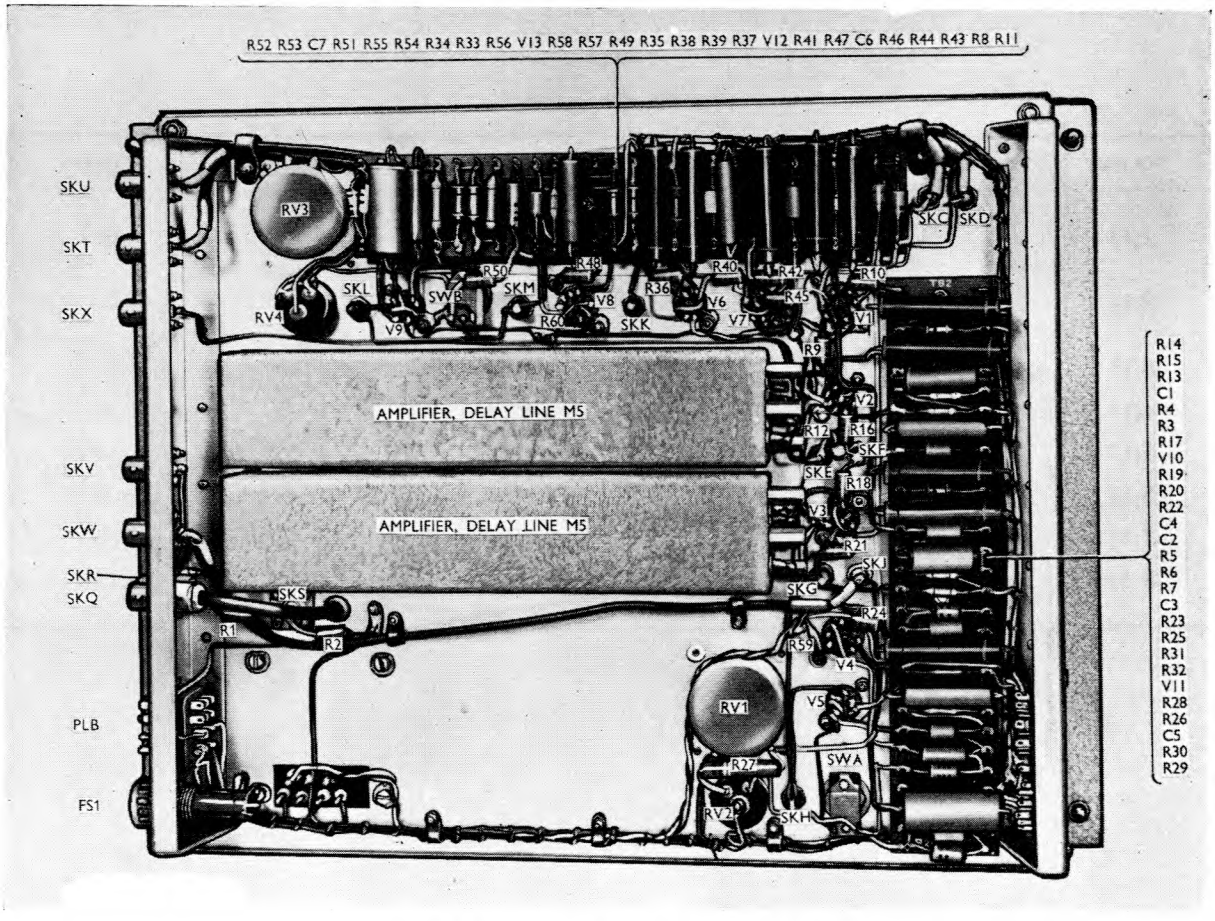


Fig. 4. Comparator signal M2 : rear view

Monitor points

23. Ten monitoring sockets, SKC to SKM, are provided on the unit and these are primarily intended for checking the various d.c. levels during the initial setting-up procedure. Under operating conditions the only waveforms that can be observed at these sockets are bi-polar video signals. Using the monitoring oscilloscope M1 (*Sect.* 7, *Chap.* 4), the approximate peak-to-peak amplitudes of these video signals, and the steady d.c. levels about which they are centred are listed in Table 1.

TABLE I

Monitor point waveforms

Monitoring socket	Waveform to be observed
SKC	Twice-delayed video signals, greater than 2V peak-to-peak, at +10V.
SKD	Once-delayed video signals, greater than 2V peak-to-peak, at +10V.
SKE	Twice-delayed video signals, up to 3V peak-to-peak, at +3V.
SKF	Added video signals, up to 3V peak-to-peak, at +3V.
SKG	Once-delayed video signals, up to 3V peak-to-peak, at +3V.
SKH	Either an a.g.c. voltage level of −3·5V (SWA set to AUTO position), or a variable level of between −2V and −12V (SWA set MANUAL position). No video signals are observed at this point.
SKJ	Cancelled video output, up to 3V peak-to-peak, at +2V.
SKK	+3V. No video signals are observed at this point.
SKL	Either an a.g.c. voltage level of −3·5V (SWB set to AUTO position), or a variable level of between −12V and −2V (SWB set to MANUAL position). No video signals are observed at this point.
SKM	Twice-delayed video signals, up to 3V peak-to-peak, at +2V.

Multimeter readings

24. With the multimeter Type 100 connected to socket SKA of the unit via a plug-to-socket adaptor, the meter readings obtained should be as indicated in Table 2.

TABLE 2

Multimeter readings

SKA poles	Multimeter switch position	Stage checked	Measured across	Reading	Tolerance	
1,13	A	Delayed amplifier	R4, C1	0·4	±0·08	
2,14	B	Undelayed amplifier	R5, C2	0·4	±0·08	
3,15	C	V2	R15	0·45	±0·09	
4,16	D	V3	R20	0·45	±0·09	i.e. 20%
5,17	E	V4	R25	0·55	±0·11	
6,18	F	V6	R39	0·45	±0·09	
7,19	G	V7	R44	0·45	±0·09	
8,20	H	V8	R49	0·55	±0·11	

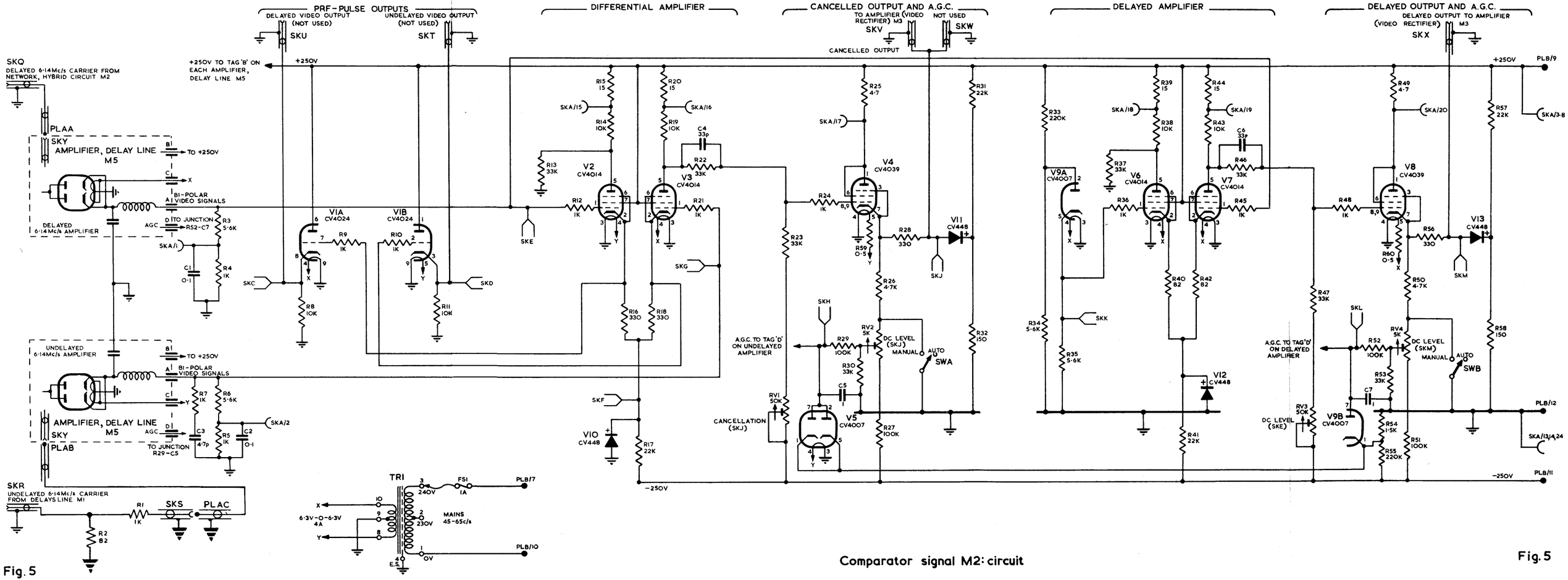


Fig. 5

Comparator signal M2: circuit

Fig. 5

Chapter 7

DELAY LINE AMPLIFIERS M5 AND M6

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

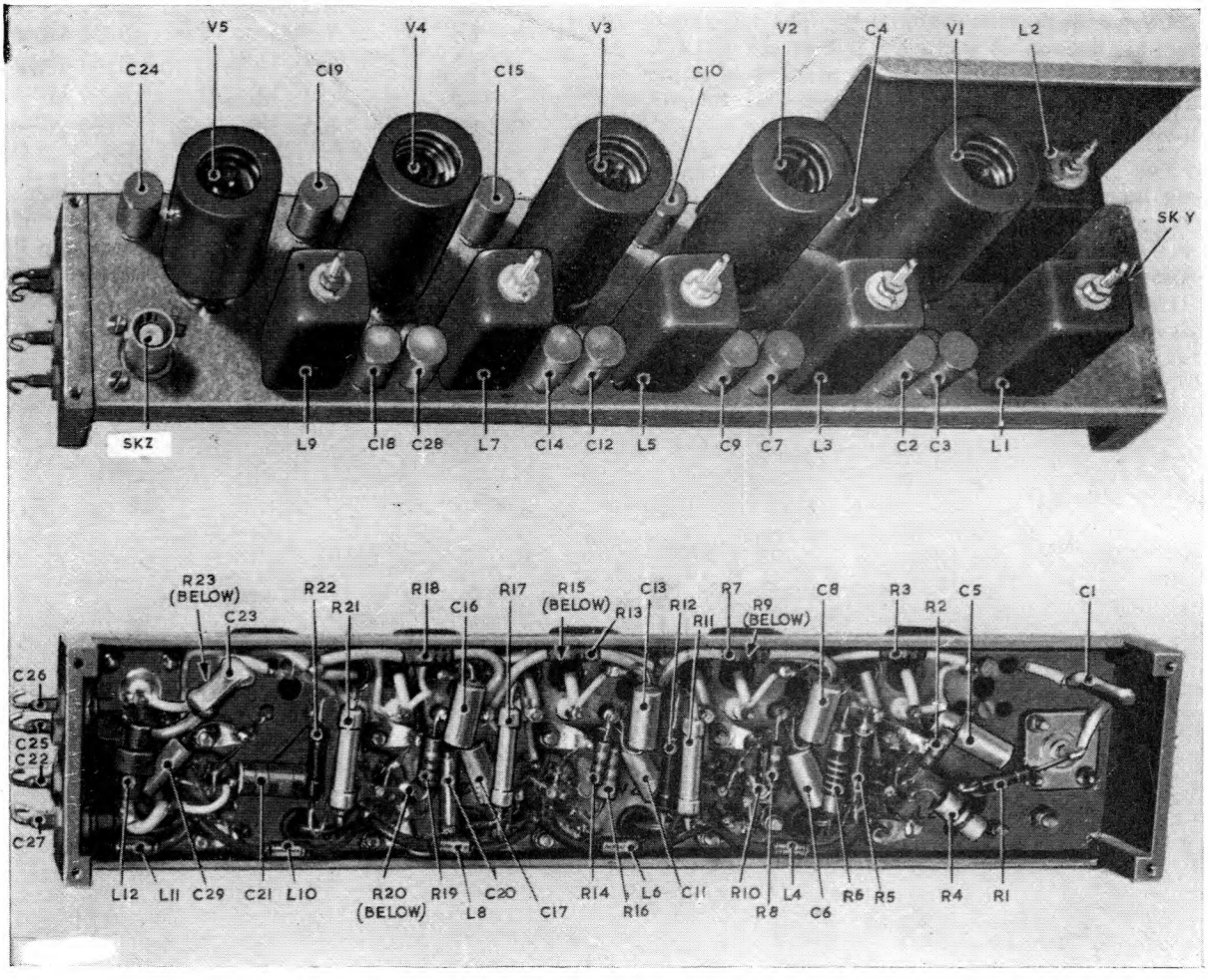


Fig. 1. Delay line amplifier: top and underside

Introduction

1. The amplifier delay line M5 (6 Mc/s) and the amplifier delay line M6 (8 Mc/s) have similar circuits (*fig.* 2 *and* 3), differing mainly in the values of inductance of the tuning coils. The purpose of the amplifiers is to amplify the delayed and undelayed 8 and 6 Mc/s carriers (modulated by video signals) which are obtained in channels A and B from the coherent demodulator (*Sect.* 2, *Chap.* 10) and in the p.r.f. discrimination channel from the relay assembly M2 (*Sect.* 5, *Chap.* 6).

2. In the radar Type 84 signal processing system, there are five M6 delay line amplifiers, and four of the M5 type. They form sub-assemblies on the following units:—

M6 delay line amplifiers
Comparator signal M1 (channel A)—2 off
Comparator signal M1 (channel B)—2 off
Comparator signal (coincidence) M3—1 off
M5 delay line amplifiers
Comparator signal M2 (channel A)—2 off
Comparator signal M2 (channel B)—2 off

Operating characteristics

Input

3. SKY. 8·19 Mc/s or 6·14 Mc/s carrier, amplitude modulated by video signals.

Outputs

4. *Terminal* A. Video signals, up to 3V peak-to-peak at a d.c. level of approximately +3V are fed out to the signal comparator for which the amplifier is a sub-assembly.

SKZ. The input signal amplified approximately 50db; this output is not used in the radar Type 84 system.

Circuit description

5. The 6·3V heater supply (one side earth) for the five valves is supplied from the signal comparator, at terminal C. Also supplied from this unit is the +250V h.t. supply at terminal B. The individual valves are decoupled at the h.t. line by R7 and C2, R13 and C9, R18 and C14, R23 and C18 and at the heater supply by L4 and C4, L6 and C10, L8 and C5, L10 and C19, L11 and C24.

6. The circuit is a conventional four stage staggered tuned r.f. amplifier of 1·5 Mc/s bandwidth, giving an overall gain of the order of 75dB. A.G.C. at a d.c. level of approximately −3·5V is applied to the first three stages from the comparator unit at terminal D. The a.g.c. line is decoupled from each stage by R3 and C3, R9 and C7, and R15 and C12.

7. L2 and C5 in the cathode of V1 comprise either a 6 Mc/s or an 8 Mc/s rejection circuit. In the case of the 8 Mc/s amplifier L2 is tuned to 6·54 Mc/s, and in 6 Mc/s amplifier, to 7·80 Mc/s. This rejection circuit is necessary because the undelayed signal supplied to the signal comparators M1 and M2 from the hybrid circuit M3 (*Sect.* 3, *Chap.* 3) in the delay line M1 (*Sect.* 3, *Chap.* 8) consists of mixed 8 and 6 Mc/s modulated carriers.

8. The amplifying stages are tuned by the adjustable dust cores in the tuned anode circuits of V1 to V4. The frequency to which each stage is tuned is given below.

Inductance	*M6 amplifier* (8 *Mc/s*)	*M5 amplifier* (6 *Mc/s*)
L1	8·19 Mc/s	6·14 Mc/s
L3	8·9 Mc/s	5·48 Mc/s
L5	7·5 Mc/s	6·78 Mc/s
L7	8·16 Mc/s	6·10 Mc/s
L9	8·19 Mc/s	6·14 Mc/s
L2	6·54 Mc/s	7·80 Mc/s

9. V5 detects the video signals and feeds them out to the signal comparator, for which the amplifier is a sub-assembly, via the ◀800 kc/s▶ low pass filter L12, C29, C26. An additional output, for use with a valve voltmeter when tuning the coils of the amplifier, is taken from the centre tap of L9 via C23 and the CARRIER OUT socket SKZ.

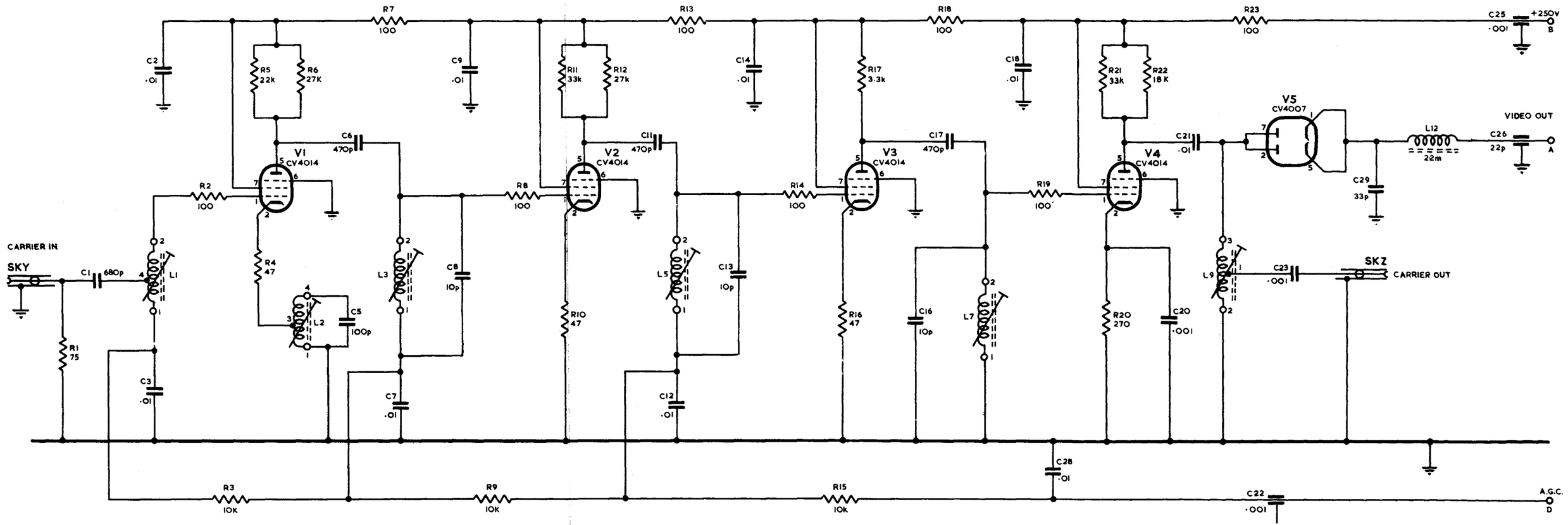


Fig. 2
M.F.R

Amplifier delay line M5:circuit

Fig.2

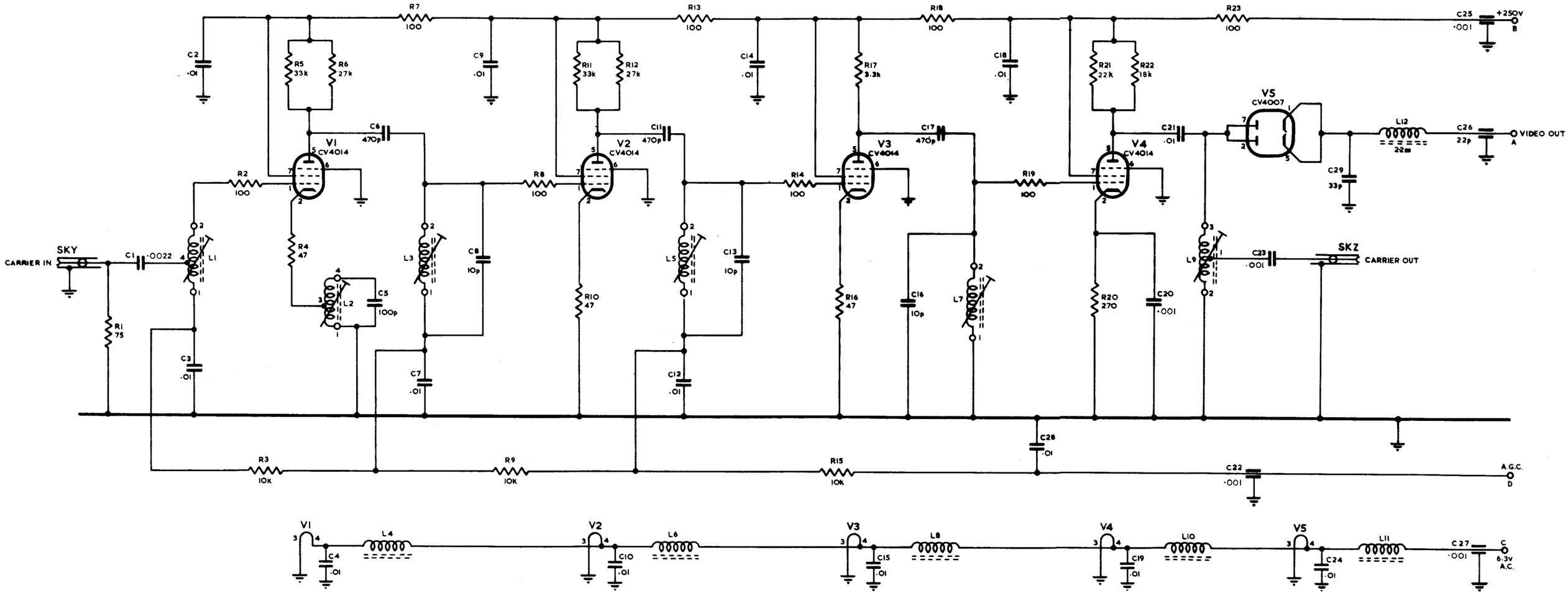


Fig.3

Amplifier delay line M6:circuit

Fig.3

Chapter 8

DELAY LINE (VARIABLE) M1

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

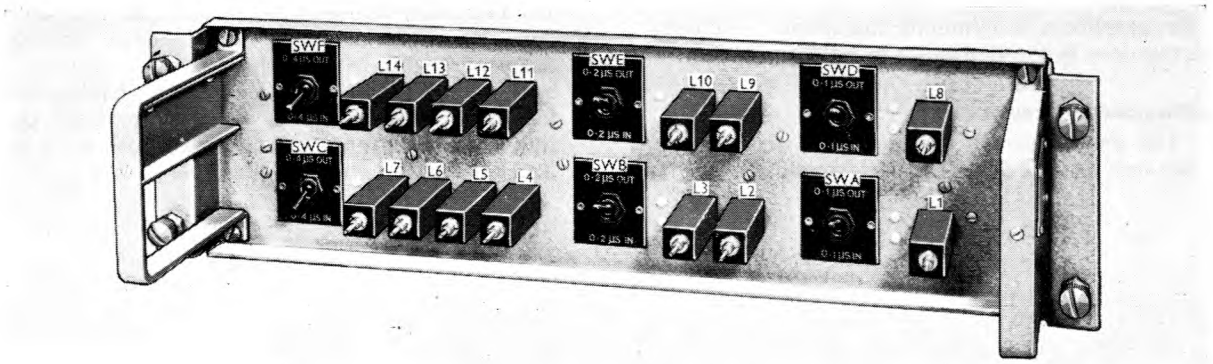


Fig. 1. Delay line, M1: front view

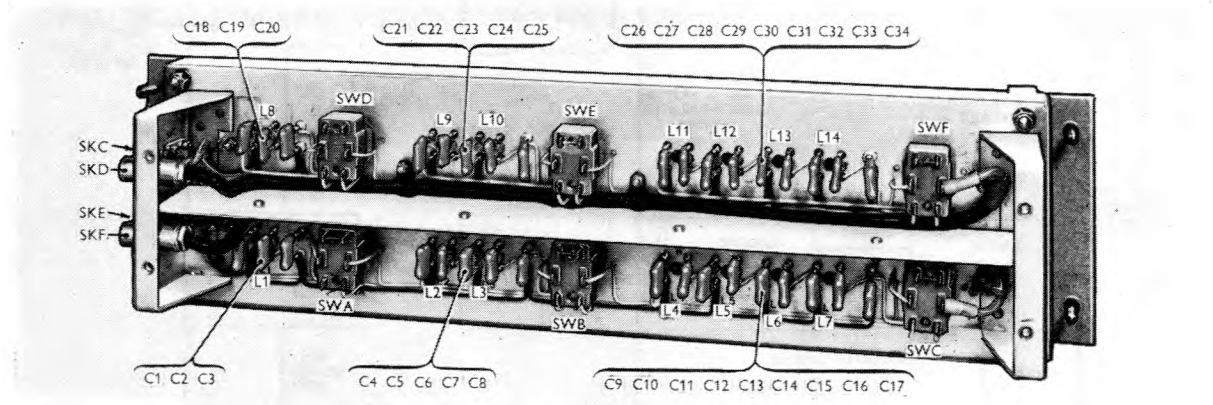


Fig. 2. Delay line, M1: rear view

Introduction

1. The variable delay line M1 (*fig.* 1 *and* 2) is used in two similar applications, one being in cancellation channel A and the other in cancellation channel B. The function of the delay line is to compensate for ◀any difference in the overall delay of the 8·19 Mc/s and 6·14 Mc/s channels, by providing adjustment to ensure▶ that the time interval between the arrival of delayed and undelayed video modulated inputs to the signal comparators is exactly equal to

one pulse recurrence period. The small delay introduced, is adjustable between 0 microseconds and 0·7 microsecond in 0·1 microsecond steps, the appropriate delay being selected by the operation of one or more of the switches on the unit designated 0·1μS, 0·2μS or 0·4μS IN/OUT. Switches SWA, SWB, and SWC control the 6·14 Mc/s delay line and switches SWD, SWE, and SWF the 8·19 Mc/s delay line. The channel A unit is located in frame 3, and the channel B, in frame 2 of the cancellation cabinet.

2. Each unit consists of two separate delay lines (*fig.* 3) with a characteristic impedance of 75 ohms. An 8·19 Mc/s delay line delays the video-modulated 8·19 Mc/s carrier signals, and a 6·14 Mc/s delay line delays the 6·14 Mc/s video-modulated carrier signals in the undelayed paths to the signal comparators M1 and M2 respectively.

3. The delay lines each receive an identical input of mixed 6·14 Mc/s and 8·19 Mc/s video-modulated carrier from the hybrid circuit network M3 (*Chap.* 3) and the output, suitably delayed, is fed to a delay line amplifier (*Chap.* 7) on the appropriate signal comparator; rejection circuits are incorporated in the amplifiers to eliminate the carrier frequency not required in the particular signal comparator.

Performance characteristics

4. The characteristics of the inputs and outputs of the unit are the same for both applications.

Inputs

5. Identical inputs are received at sockets SKE and SKC for the 6·14 Mc/s and 8·19 Mc/s delay lines respectively. The inputs are received from the hybrid circuit network M3 and consist of mixed 6·14 Mc/s and 8·19 Mc/s video-modulated carriers with a carrier level of 15 mV, 50 per cent modulated by video signals, into a nominal characteristic impedance of 75 ohms.

Outputs

6. Outputs from the 6·14 Mc/s and 8·19 Mc/s delay lines are taken from sockets SKF and SKD respectively. The outputs are delayed with respect to the inputs by a time interval depending on the setting of the switches up to a maximum of 0·7μS. The output level at the carrier frequency is at a maximum of 3 dB below the input level for the 6·14 Mc/s delay line and at a maximum of 4 dB below the input level for the 8·19 Mc/s delay line, with all switches at the IN position.

Circuit description

7. The delay line unit M1 consists of two similar delay lines, one of which is designed to provide a delay of 0 to 0·7μS for the 8·19 Mc/s carrier frequency, and the other to provide an identical delay for the 6·14 Mc/s carrier frequency. Each delay line accepts an input consisting of both 6·14 Mc/s and 8·19 Mc/s carrier frequencies.

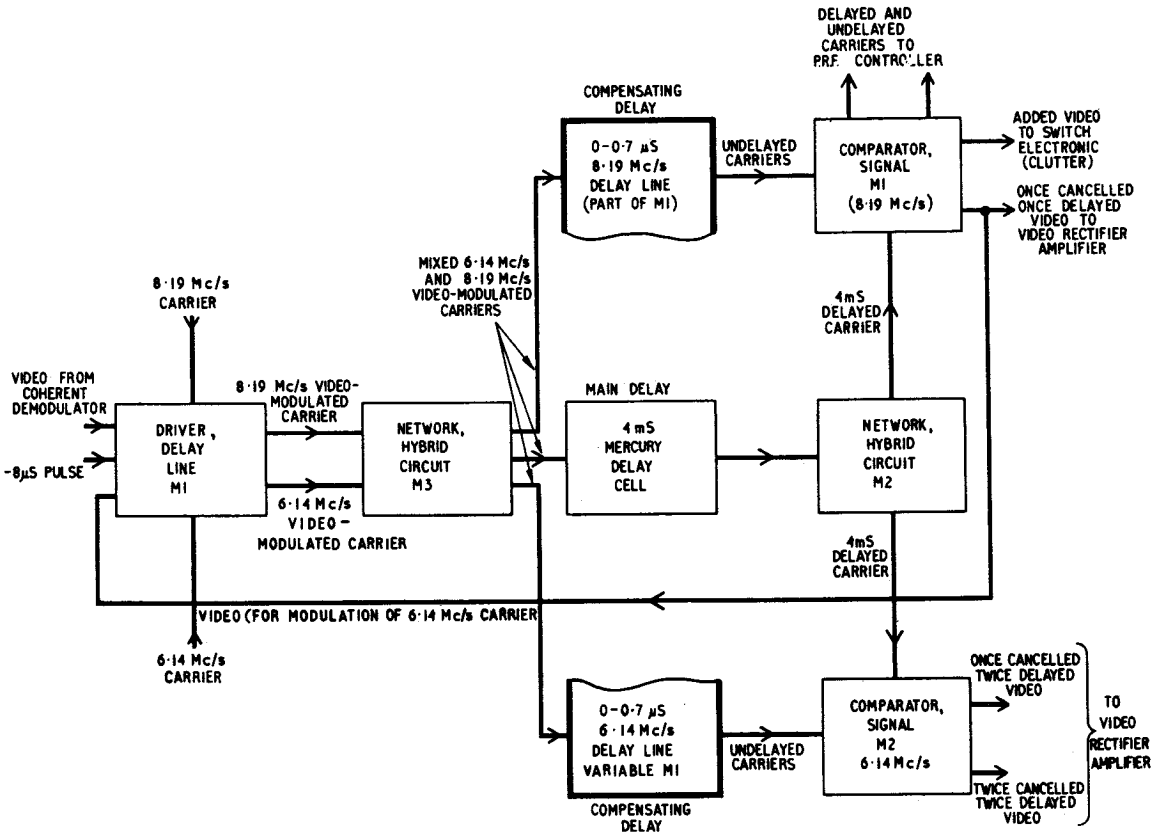


Fig. 3. Single-channel cancellation: block diagram

8. Each delay line consists of seven, three-element band-pass filters, each section providing a delay of 0·1 microsecond at the appropriate carrier frequency. The sections are arranged in three groups (one, two and four sections) which may be connected into circuit by means of three, two-way toggle switches so that by operation of the switches, compensating delays between zero and 0·7 microsecond, switched in 0·1 microsecond steps, may be introduced in the undelayed carrier path to the signal comparator.

9. The required delays are switched in during the initial setting-up of the cancellation system *after which no further adjustment should be necessary unless the delay cell has been changed.* Switches SWD, SWE, and SWF on the 8·19 Mc/s delay line are set to give optimum cancellation at monitor point SKJ on the signal comparator M1 (*Chap.* 5). Similarly, switches SWA, SWB, and SWC on the 6·14 Mc/s delay line are set for optimum cancellation at SKJ on the signal comparator M2 (*Chap.* 6).

10. In addition to the required delays, the delay lines introduce attenuation at a maximum of 4 dB in the 8·19 Mc/s delay line and a maximum of 3 dB in the 6·14 Mc/s delay line with all switches operated to the IN position.

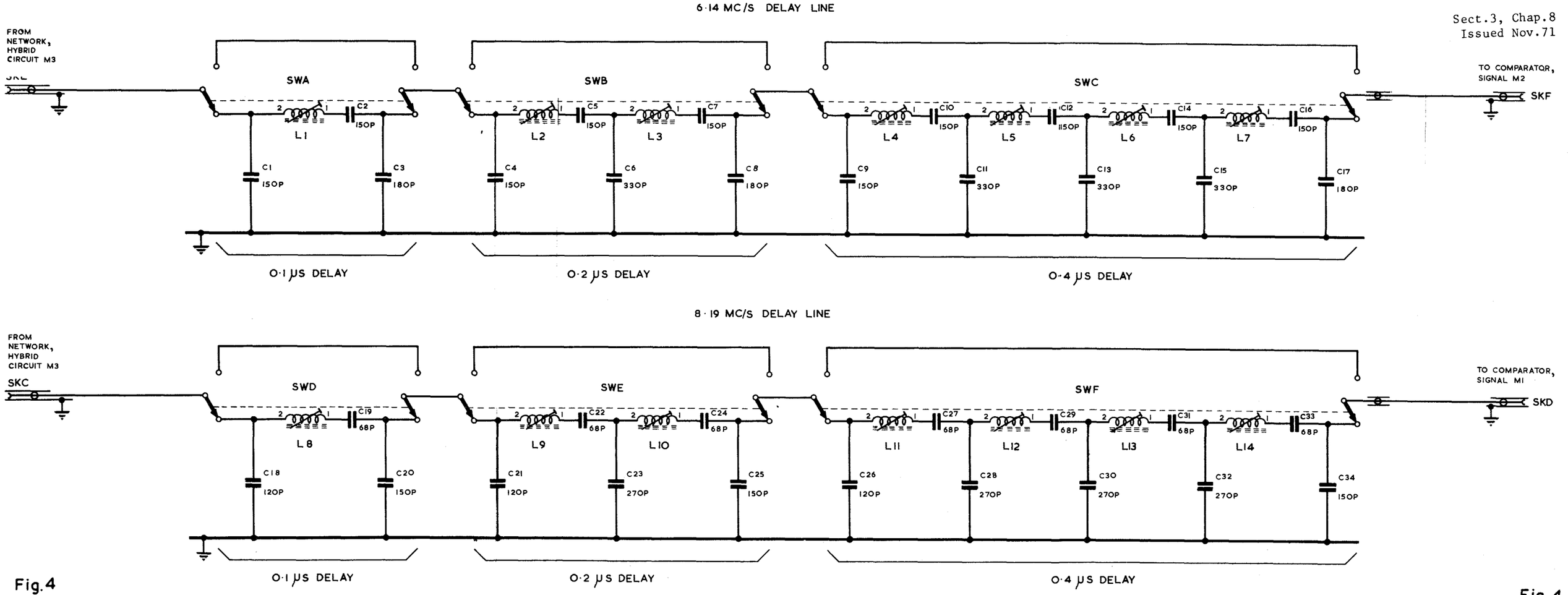


Fig.4
M.E.P.

Delay line M1: circuit

Fig.4

Chapter 9

SWITCH, ELECTRONIC (CLUTTER) M1

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

Fig. 1. Switch electronic (clutter) M1 : front view

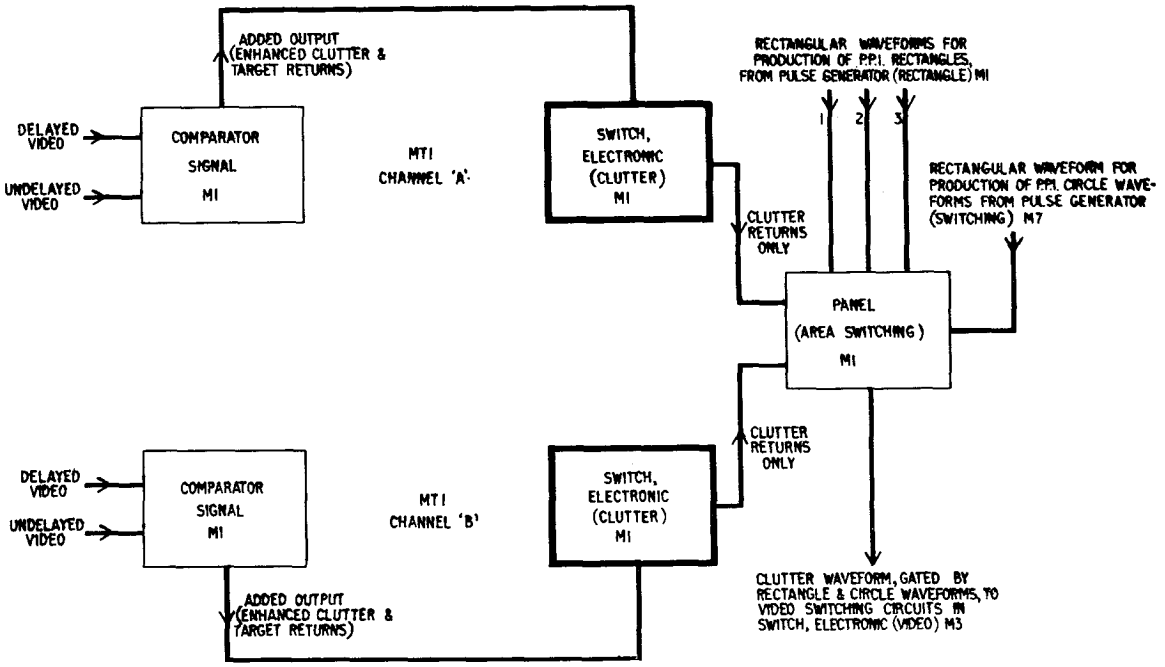


Fig. 2. Functional block schematic

Introduction

1. The two electronic switch (clutter) M1 units, corresponding to the cancellation channels A and B, are located in frames 3 and 2 respectively of the cancellation cabinet.

2. This unit accepts bi-polar video signals from the adding circuit in the signal comparator M1 (*Chap.* 5) and its purpose is to discriminate between wanted signals due to significant targets and unwanted signals due to clutter or angels. For this purpose clutter returns are defined as returns which are greater in duration than about twice the transmitter pulse width, and angels are defined as a series of recurring signals, other than clutter returns, spaced approximately 100–150 microseconds or less apart.

3. The unit only produces an output, in the form of a uni-polar video signal, when the input signal is produced by clutter or angels. As indicated in the functional block schematic (*fig.* 2) this output is gated by the display rectangle waveforms and the gated output is used to switch out the unwanted video.

Performance characteristics

Input

4. The input at socket SKR consists of bi-polar video signals with an amplitude of up to 3V peak-to-peak at a d.c. level of +2V, from the signal comparator M1. Socket SKQ is terminated in a 75-ohm terminating connector assembly.

Output

5. There are two modes of operation for the unit affecting the output at socket SKS as follows ;

(a) *Normal operation* (angel cancellation circuit switched out by operation of the CANCEL ANGELS switch on the control console). No significant output pulse appears until the input pulse length is greater than 15 microseconds. The positive-going output pulse is approximately of equal length to the input pulse, but delayed on it by 21 microseconds, and is about 30V amplitude.

(b) *Angel cancellation circuit* switched in. When the time interval between any pair of signals is 125 (±25) microseconds or less, the unit produces a positive-going output, coincident with the second of the pair of signals and having a length equal to the input pulse length plus 20 microseconds. The amplitude is about 30V. When the time interval is greater than about 150 microseconds the operation of the unit is as in (a) above. The output from SKS is taken to the panel (area switching) M1 (*Sect.* 4, *Chap.* 7), and thence to switch, electronic (video) M3 (*Sect.* 5, *Chap.* 5).

Circuit description

Power supplies

6. The 6·3V heater supplies for V1 to V8 are obtained from TR1 which is supplied with 50c/s mains from plug PLB/7 (via FS1) and PLB/10 (*fig.* 9). The other power supplies used on this unit are +250V, −250V and −50V supplied at PLB poles 9, 11 and 8 respectively. The mains and h.t. supplies are fed to the unit from the +250V regulated power unit in that particular frame.

Amplifier

7. The bi-polar video signals are a.c. coupled into the amplifying stage V1 and V2 which consists of two stages of amplification (V1a and V2b), separated by a cathode follower (V1b) with a cathode follower output (V2a) to the phase splitter V3 and V4. Gain control is effected by negative feedback from the second cathode follower to the cathode of the first amplifier. Potentiometer RV1 GAIN (SKP) is adjusted so that noise signals are just beginning to appear at the output of the unit, monitored at SKP.

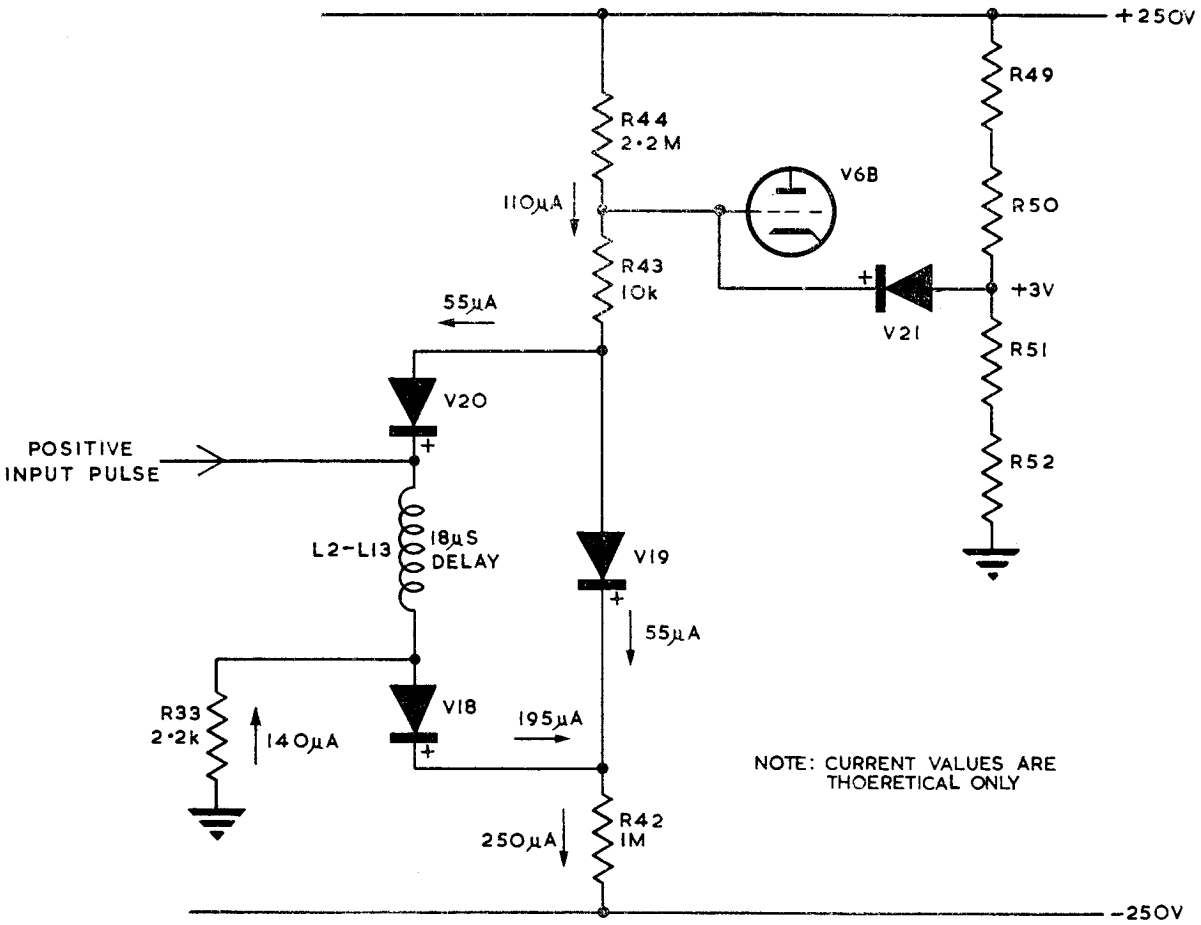


Fig. 3. Coincidence gate: simplified circuit

Phase splitter, bridge rectifier and delay line

8. The output from V2a (monitored at SKF) is applied to the cathode-coupled phase splitter V3 and V4. This stage produces paraphase outputs at the anodes of V3 and V4 to be fed to the bridge rectifier V9–V12 (monitored at SKG and SKH).

9. The bridge rectifier produces a positive-going output of approximately 6V amplitude.◀This is smoothed by the filter L1, C7 and positively-limited to 5·2V by diode V15 in conjunction with R71, R72 and C31. The output voltage at V15 anode is applied directly to V20 (one-half of a coincidence detector) and this input can be monitored at SKJ. The other half of the coincidence detector, V19, is fed via the 18-microsecond delay line (L2 to L13) and V18. The delay line is terminated at one end by R32 and at the other by R33, both these resistors having values approximately equal to the characteristic impedance of the delay line. The reason for R66, R67 and R68 is that with delay lines of this type it is possible to improve the frequency response by placing resistors of about twice the characteristic impedance in parallel with the end coils and approximately every sixth coil. The amplifier stages V1 and V2 have sufficient gain to ensure that the output from the bridge rectifier is positively limited by V15,▶

Coincidence detector

10. The purpose of the coincidence detector V19 and V20 is to produce at V6b grid a positive-going pulse only when there are signals at both V19 and V20 cathodes. Due to the delay line, therefore, unless the incoming video signal is longer than 18 microseconds there will be no signal at V6b grid. In practice, however, because of the pulse rise and fall times, the minimum pulse length required to produce this signal approximates 15 microseconds.

11. A simplified circuit of the coincidence detector is shown in fig. 3. The d.c. resistance of the coils L2–L13 is low and can be ignored in this description. Triode V6b is normally conducting; its grid is at about −3V, this level being set by current flow through R44, R43, V19 and V20. Noise clipper V21, with R49 to R52, prevents V6b grid potential from falling below this level thus preventing any stray noise signals, which may otherwise have operated the coincidence detector, from reaching V6b grid. The current flow through R44 is approximately 110μA. The voltage drop across R43 and the diodes, which have a very low forward resistance, will be low and so the diode cathodes will be at about earth potential. Thus, the current flow through R42 will be approximately 250μA. The current through R44 will split approximately equally and flow through V19, V20 and V18 in series. The remaining 140μA to make up the current

through R42, takes the path from earth through R33 and V18.

12. If V20 is cut off by the positive-going input pulse, the total 110μA will flow through V19. Similarly, if V19 is cut off by the positive-going input pulse (delayed and applied via V18), all of the 110μA will flow through V20 and V18. In either case there will be no change of potential at V6b grid. If, however, both V19 and V20 are cut off simultaneously, as in the event of an input pulse longer than about 21 microseconds, then V6b grid will be free to rise towards +250V causing V6b to conduct more and produce a negative pulse at the anode.

Pulse-stretching and output stage

13. The negative-going pulse thus produced at V6b anode is stretched by approximately 25 microseconds. This is achieved by C25 being charged negatively through V22 and discharged slowly through R54. At V6a anode, therefore, a positive-going pulse of a width approximately 25 microseconds greater than that of the incoming video signal, and delayed with respect to it by 18 microseconds, is produced.

14. The output from V6a anode is d.c. restored to earth by V7a and clipped to approximately +28V by V7b. R59 and R60 set the grid potential on V8 to about −14V so that it is normally cut off. The pulse from V7b anode brings cathode-follower V8 into conduction producing at its cathode and at output socket SKS, a positive-going output of about 30V amplitude.

15. Fig. 4 shows theoretical waveforms for the operation of the clutter switching circuit in the event of two input signals, one less than 20 microseconds and the other greater than 20 microseconds, being received. To ensure that the clutter switching facility is not displaced from the clutter due to the delay between input and output of this unit, an additional delay of 7 microseconds is incorporated in the signal circuit by the pulse delay network M4 (*Sect.* 2, *Chap.* 5). With the 12 microseconds delay inherent in the video signal comparator M4 (*Sect.* 2, *Chap.* 6), the delay of the cancelled video input to the video switch is made compatible with the delay of the clutter switching waveform which is applied to the video switch via the area switching panel (*Sect.* 4, *Chap.* 7).

Angel cancellation circuit

16. Double triode V5 and its associated circuit form an angel detector stage which is switched in by RLA and energized via plug PLB poles 8 and 9, by operation of the CANCEL ANGELS switch on the radar operator's control console. Relay contacts RLA2 and RLA1 complete the cathode circuits of V5a and V5b respectively, bringing both triodes into conduction. The positive-going video signals, after being delayed 18 microseconds, are applied via R34 to the grid of the cathode follower V5a. All signals above the noise level of approximately 2·5V, set by the noise clipper V13 and R52, will appear at V5a cathode and C22 will be charged negatively by grid current through V5b. At the termination of the signal V5b will be cut off as C22 discharges slowly through R37. The time constant of C22 and R37 is such that V5b will remain cut off for 100–150 microseconds thereby producing at its anode a positive-going pulse of the same duration. This pulse is d.c. restored to earth by V16 and applied, via V17, to V19 cathode. Diode V18 prevents the pulse from being fed back to V5a grid.

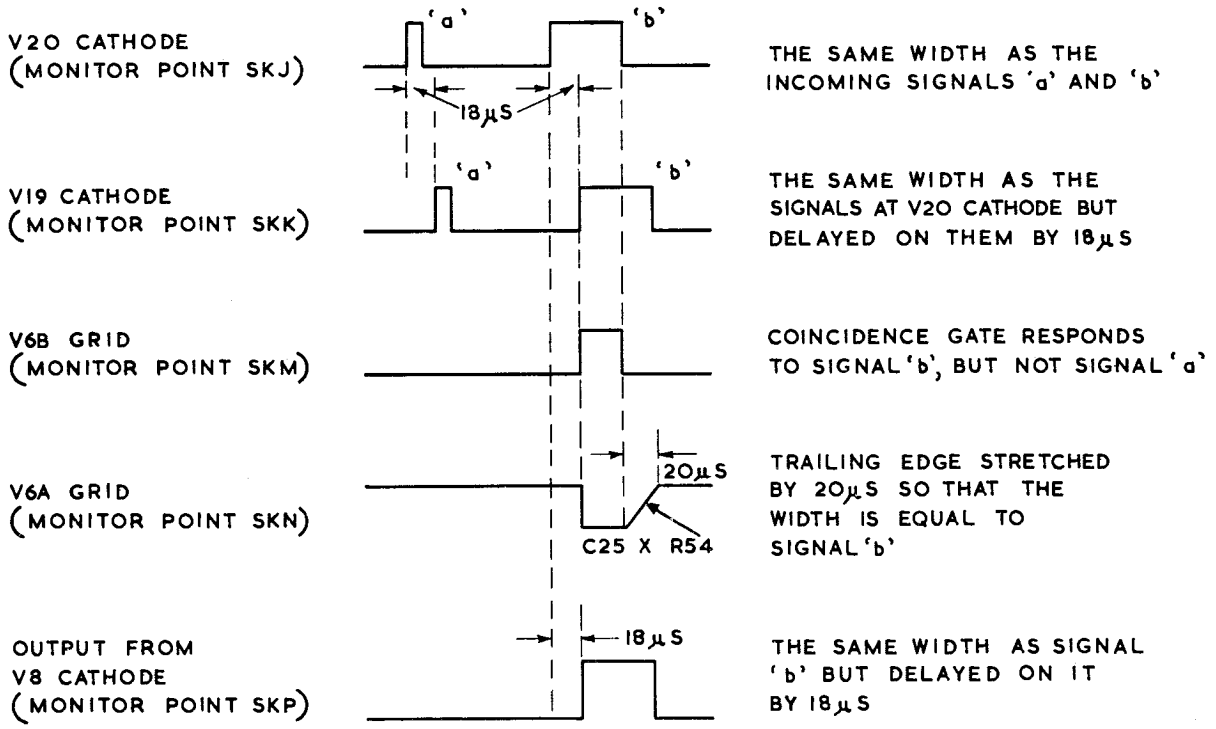


Fig. 4. Clutter switching waveforms

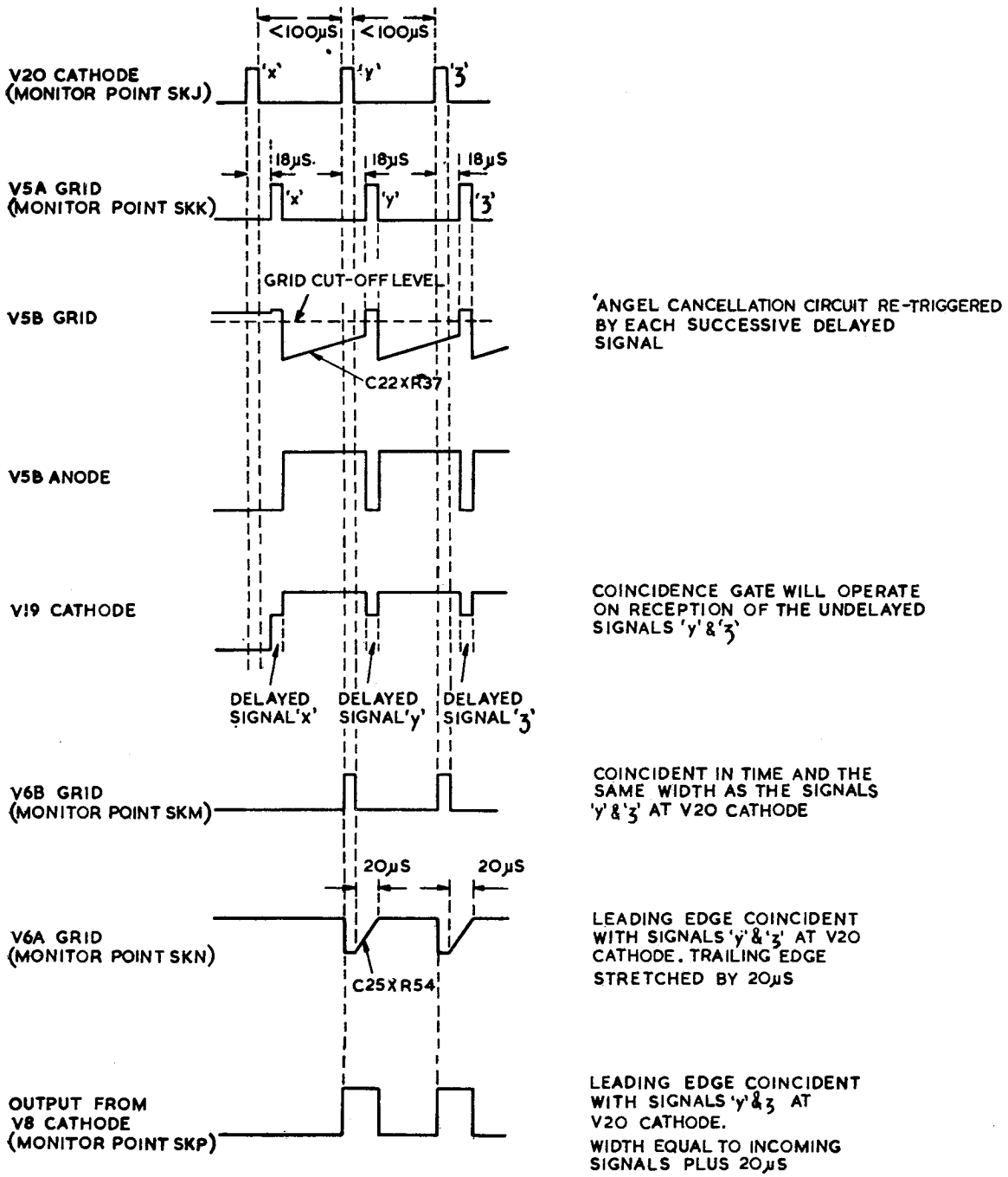


Fig. 5. Angel cancellation : signals less than 150μS apart

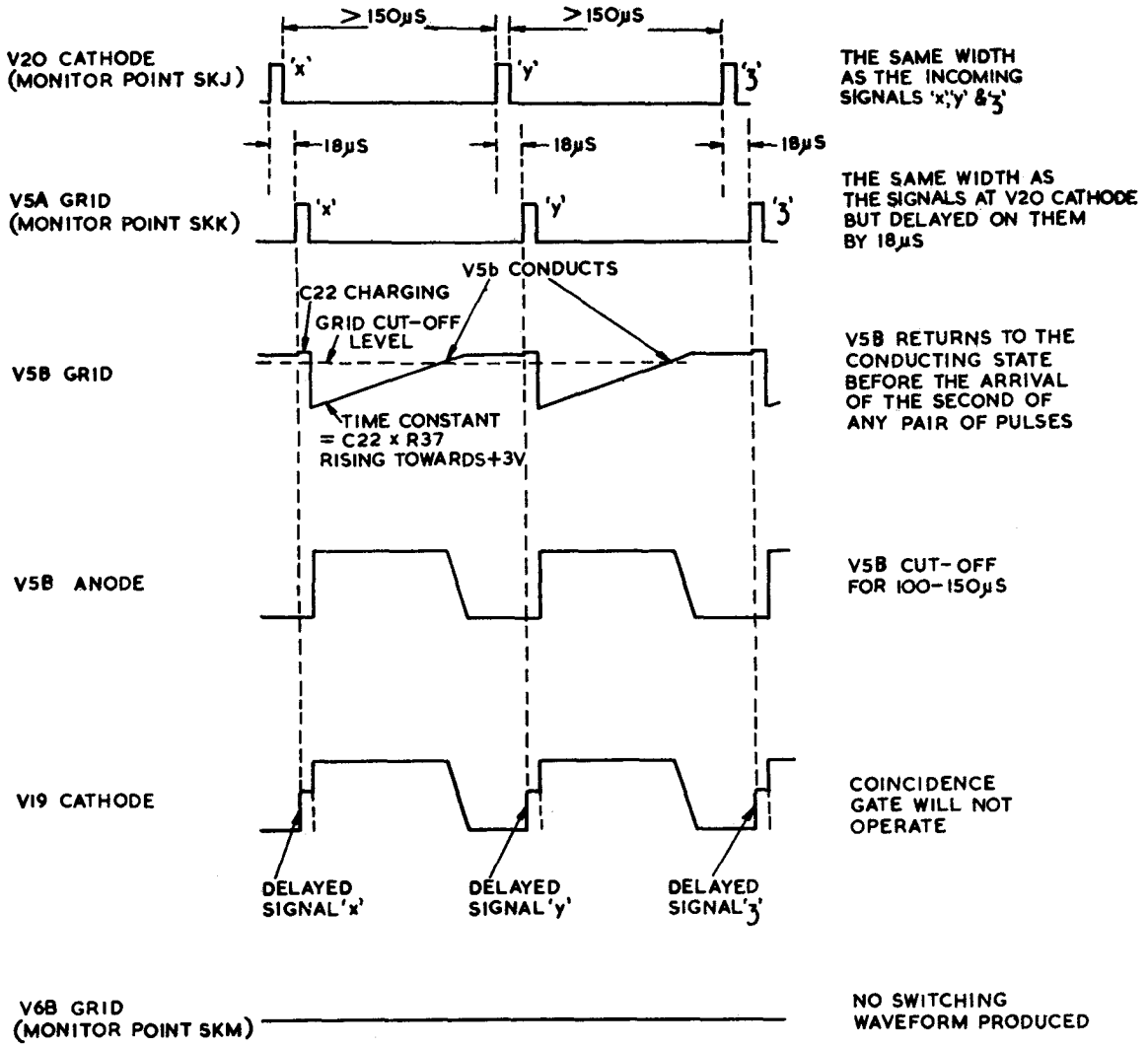


Fig. 6. Angel cancellation : signals greater than 150μS apart

17. Consider now the theoretical waveforms shown in figs. 5 and 6. The delayed signal *x* triggers the angel detector circuit producing at V19 cathode a positive-going pulse. Then, if the time interval between signals *x* and *y* is less than 150μS (*fig.* 5), there will be produced at V6a grid a pulse equal in length and coincident in time with the undelayed signal *y*. This will be amplified and stretched in the circuit V6–V8, described above in paragraphs 14 and 15, producing an output (monitored at SKP) the leading edge of which is coincident with the incoming signal *y*, and the length of which is equal to signal *y* plus 25 microseconds. The delayed signal *y* will retrigger the angel detector, and the circuit will also function in the above manner with signal *z*.

18. If the signals are greater than 150 microseconds apart (*fig.* 6) V5b will be cut off by signal *x* but reach conduction before the onset of signal *y*. Due to the conduction of V5b, V17 is cut off, and signal *y* will not be passed to the coincidence gate. V19 will draw a small amount of current through R44 and R43 for the duration of the delayed signal because it will be forward biased during this time, and V6b grid will remain conducting. The sequence is repeated for signal *z*.

19. The purpose of the 25 microseconds stretching circuit (*para.* 13) is to ensure that the change-over from cancelled to log-PLD signals in the video switch occurs after the end of the unwanted signals. Without the stretching of the switching waveform the last 4 microseconds of the unwanted signals from the log-PLD channel would be passed to subsequent circuits since the total delay in the log-PLD channel is 4 microseconds greater than the total delay in the path including part of the cancellation circuit and the electronic clutter switches.

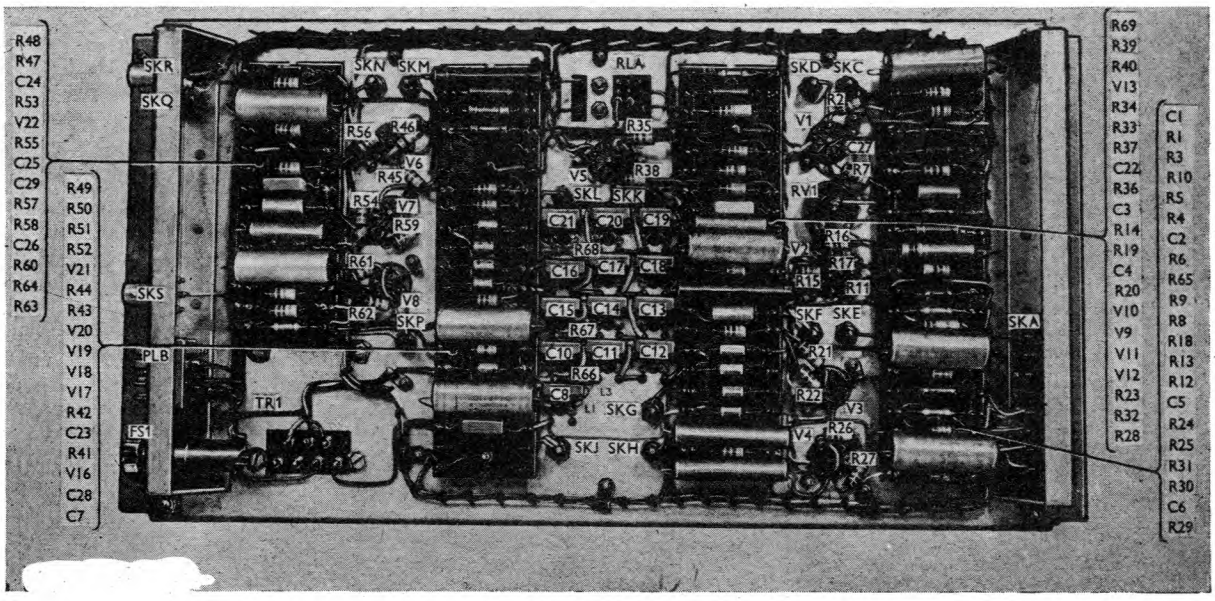


Fig. 7. Switch electronic (clutter) M1 : rear view

Monitor point waveforms

20. Using the monitoring oscilloscope M1 (*Sect.* 7, *Chap.* 4), the waveforms observed at the various monitor points in the circuit are as shown in fig. 8.

Test readings

21. With the multimeter Type 100 connected to SKA via the plug-to-socket adaptor, RV1 set fully clockwise (maximum gain) and RLA energized, the multimeter readings are as given in Table 1.

TABLE 1

Multimeter readings

Multimeter switch position	Valve stage monitored	Measured across resistor	Multimeter reading	Tolerance
A	V1a	R5	0·43	±0·1
B	V1b	R10	0·53	±0·1
C	V2b	R13	0·49	±0·1
D	V2a	R18	0·51	±0·1
E	V3	R25	0·53	±0·1
F	V4	R31	0·51	±0·1
G	V5	R69	0·44	±0·1
H	V6b	R48	0·6	±0·1
J	V6a	R58	0·42	±0·1
K	V8	R63	zero	—

BI-POLAR TEST SIGNAL INPUT
No D.C. AT MONITOR POINT
SWITCH ELECTRONIC (I.F) TO TEST

S.K.D	AS S.K.C, D.C LEVEL OF 3V	CATHODE V1A
S.K.E	AS S.K.C, D.C LEVEL 3V	CATHODE V1B
S.K.F	AS S.K.C, 10V PEAK TO PEAK AMPLITUDE	CATHODE V2A AMPLITUDE AFFECTED BY SETTING OF RV1
S.K.G	AS S.K.C. BUT APPROXIMATELY 20V PEAK TO PEAK	INPUT TO BRIDGE RECTIFIER. AMPLITUDE AFFECTED BY SETTING OF RV1
S.K.H	AS S.K.G (PHASE REVERSED)	INPUT TO BRIDGE RECTIFIER. AMPLITUDE AFFECTED BY SETTING OF RV1
S.K.J S.K.K S.K.L S.K.M S.K.N S.K.P	THESE WAVEFORMS ARE SHOWN IN FIGS. 4.5 AND 6.	

Fig.8 Switch electronic (clutter) MI: monitor point waveforms.

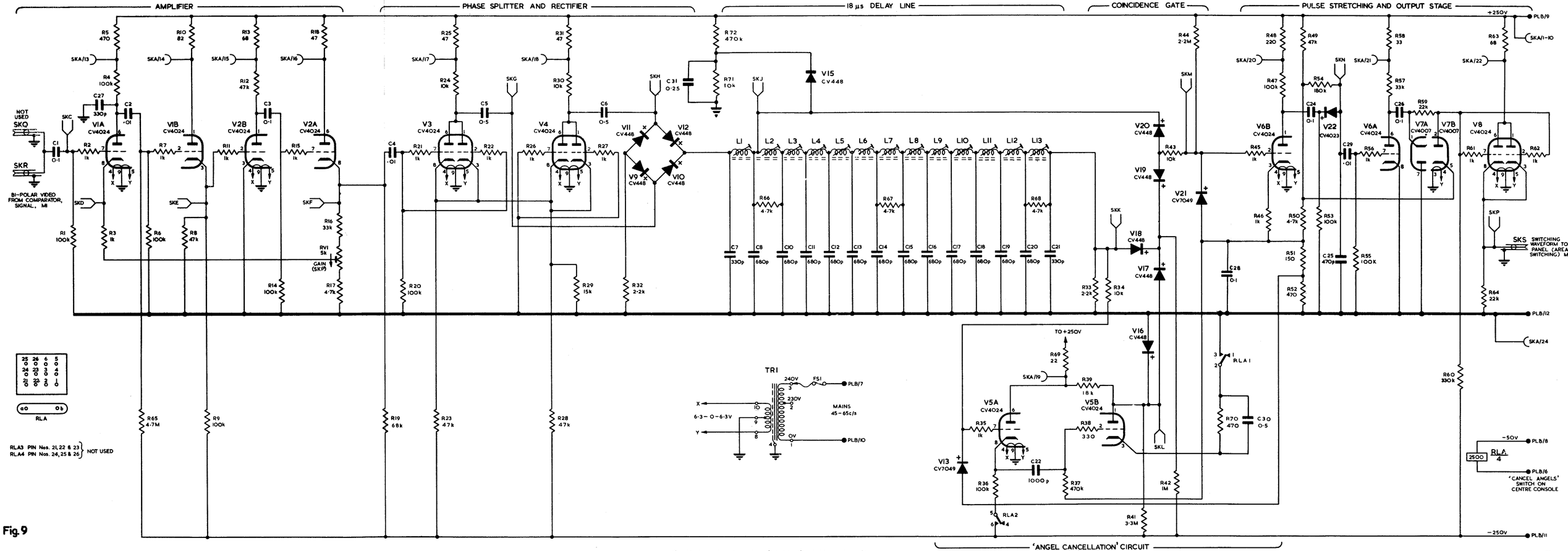


Fig.9

Switch, electronic (clutter) MI : circuit

Fig.9

Chapter 10

CONTROLLER (P.R.F.) M1

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

Introduction

1. For optimum cancellation of clutter the signal processing system used in the Type 84 equipment depends on the signal delay in the mercury delay cell being equal to the pulse recurrence period. Both of these periods are liable to drift due to temperature changes and since only a slight error (in the order of microseconds) is sufficient to impair the signal cancelling properties of the system, some form of control is needed to ensure that the delay provided by the delay cell will always be equal to the pulse recurrence period.

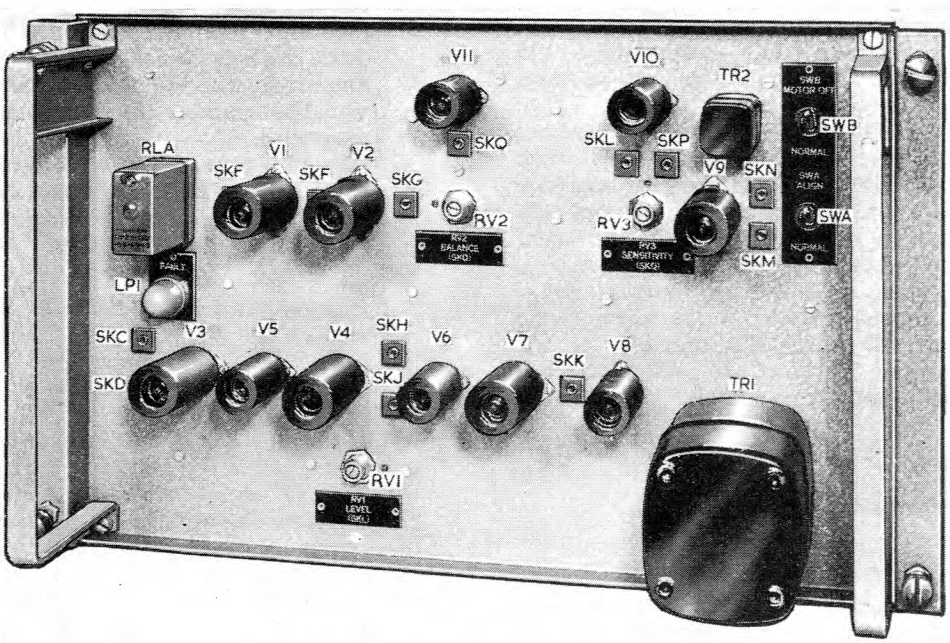
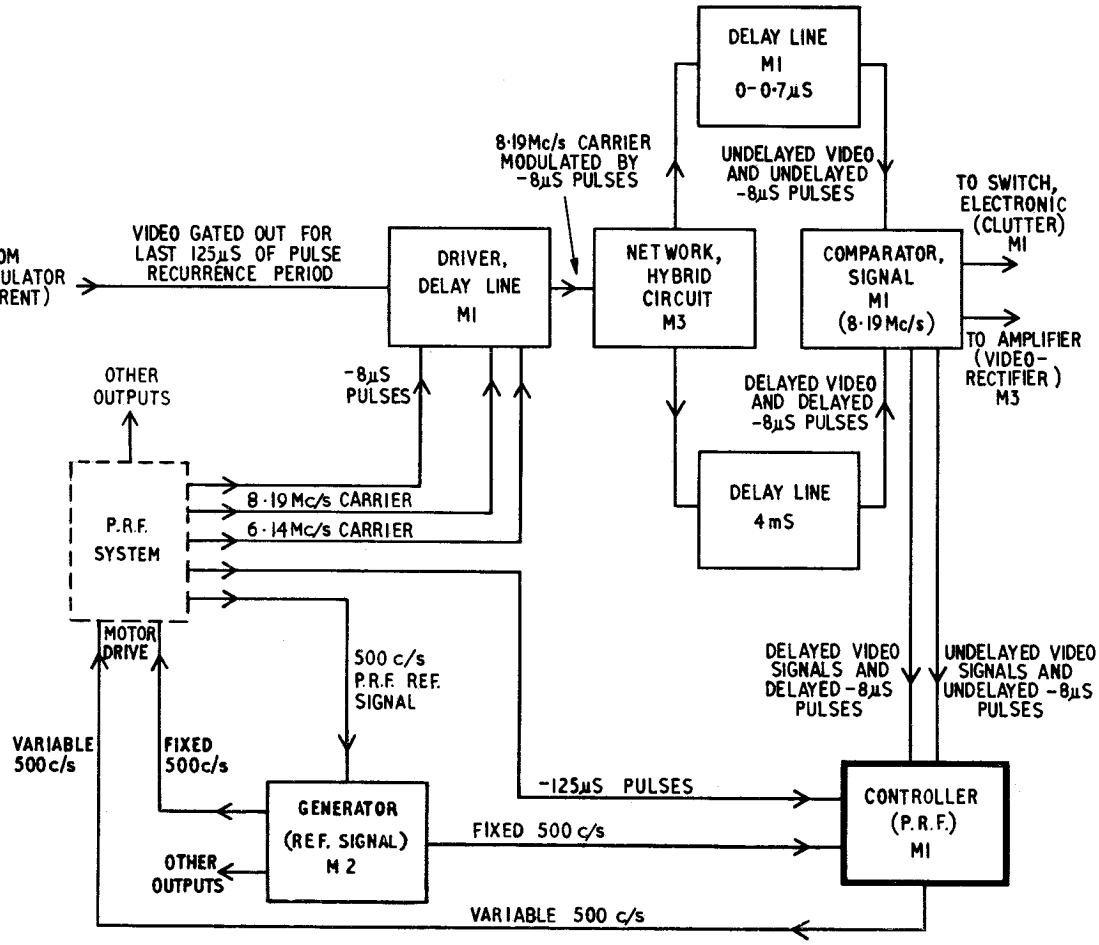


Fig. 1. Controller (p.r.f.) M1: front view



◀Fig. 2. Functional schematic▶

2. It is more convenient to control the frequency of the oscillator that determines the p.r.f. and hence the pulse recurrence period, than to control the delay of the delay cell, and this control is achieved by the controller (p.r.f.) M1 unit located in frame 1 of the cancellation cabinet.

3. The p.r.f. controller unit accepts the −125 microseconds pulse and also the delayed and undelayed −8 microseconds pulses (*fig.* 2). From these inputs the unit produces a 500 c/s control voltage, which either leads or lags by 90° with respect to a fixed 500 c/s output from the reference signal generator M2 unit and has an amplitude dependent upon the time error between the delayed and undelayed pulses. This control voltage is used to drive a two-phase motor in the ◀crystal oscillator of the p.r.f. system.▶ Coupled to the motor is the variable crystal-pulling capacitor that controls the oscillator frequency and hence the pulse recurrence period of the output from the p.r.f. generation circuits.▶◀

Performance characteristics

Inputs

4. The inputs to the unit are as follows:

(1) SKV receives a −125 microseconds positive-going pulse, 4 microseconds wide and not less than 15V amplitude from the ◀p.r.f. system.▶

(2) SKT receives an undelayed −8 microseconds positive-going pulse, 4 microseconds wide and approximately 1V in amplitude, with bi-polar video signals, from the signal comparator M1 (*Chap.* 5) of the signal processing channel B.

(3) SKU receives a delayed −8 microseconds positive-going pulse, approximately 1V in amplitude, with bi-polar video signals, from the signal comparator M1 of the signal processing channel B.

(4) PLB poles 5 and 6 receive a 500 c/s sine wave input of 60–0–60V r.m.s. balanced about earth potential (pole 12) from the generator (reference signal) M2 (*Chap.* 11).

Note . . .

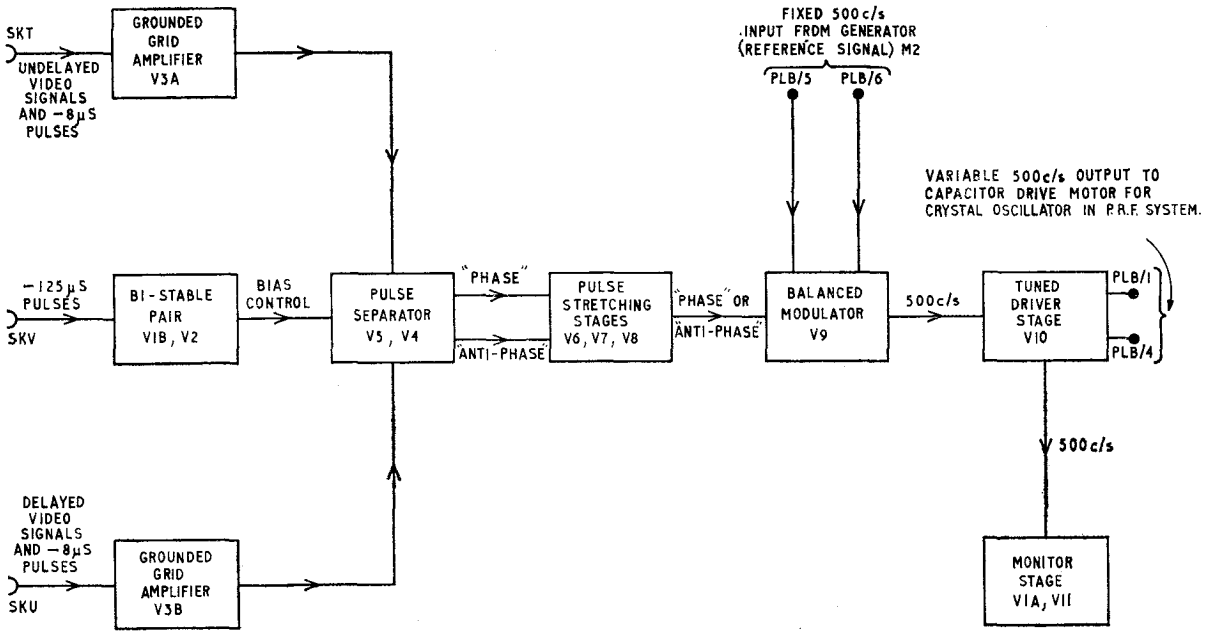
Coaxial sockets SKS, SKX and SKW in parellel with sockets SKT, SKV and SKU respectively, are not used in this application of the unit.

Output

5. PLB poles 1 and 4 (earth) provide a 500 c/s output waveform of variable amplitude and phase, fed out to the ◀p.r.f. system▶. This output is used as the controlling voltage for the two-phase motor that drives the oscillator variable capacitor.

Brief circuit description

6. The circuit consists essentially of a bi-stable pair, triggered by the −125 microseconds pulse, gating a pulse-separating stage into which are fed



◀Fig. 3. Controller (p.r.f.) M1: block diagram▶

the delayed and undelayed −8 microseconds pulses (*fig.* 3). In the event of an error in the timing of the −8 microseconds pulses this circuit produces either a 'phase' or an 'anti-phase' output which, after application to pulse stretching circuits, becomes a d.c. level with a polarity dependent on whether the delayed pulse or the undelayed pulse arrived first at the pulse separator. This d.c. error signal is then fed to a balanced modulator stage to control the production of a 500 c/s waveform of the required amplitude and phase with respect to a 500 c/s reference voltage. The 500 c/s waveform is fed out by way of a tuned driver stage.

Circuit description

7. The 6·3V a.c. heater supply for V1 to V11 is obtained from transformer TR1 which is supplied with 50 c/s mains from PLB/7, via FS1, and PLB/10. The other power supplies used with this unit are +250V applied at PLB/9 and PLB/12 (earth), and −250V at PLB/11 and PLB/12 (earth). The mains and h.t. supplies are taken from the +250V voltage regulator unit at the top of frame 1 of the cabinet.

Bi-stable pair

8. Double triode V2 and its associated circuit form a cathode-coupled bi-stable pair. Initially V2a is conducting and the cathodes of V2 (monitored at SKG) are at approximately +23V, while V2b grid is at approximately +12V, set by the divider chain R4, R5 and R6, so that V2b is cut off.

9. The incoming −125 microseconds positive-going pulse at SKV is stretched to a width of about 10 microseconds by V12, C1 and R2 and applied to V1b grid.▶◀. Stretching of the pulse is necessary because the time constant of C2–R9, and therefore the time required to switch the bi-stable circuit, is slightly greater than the nominal width of the −125 microseconds pulse.

10. V1b is a cathode follower and applies the stretched pulse (monitored at SKF) to V2b grid bringing V2b into conduction and, due to the d.c. coupling between V2b anode and V2a grid, cutting off V2a. The potential at the common cathodes of V2 and V4 will now be approximately +7V (*fig.* 4).

Pulse amplifying and separating circuit

11. The inputs at sockets SKT and SKU consist respectively of undelayed and delayed video signals. As previously stated, the particular video signal used for the p.r.f. control function is the positive-going −8 microseconds pulse. This pulse is made free from noise and all other extraneous video signals by a blanking circuit in the coherent demodulator unit (*Sect.* 2, *Chap.* 10) so that all i.f. signals for the 125 microseconds period from the −125 microseconds pulse to the 0 microseconds pulse are blanked off. Since the −8 microseconds pulse is fed into the video circuits at the delay line driver M1 unit following the coherent demodulator unit, this pulse is the only signal received at sockets SKT and SKU during the 125 microseconds period.

12. The undelayed and delayed video signals at SKT and SKU are amplified by V3a and V3b respectively. These triode sections are connected as grounded grid amplifiers so as to retain the polarity of the signals. The amplified signals are limited to +13V peak by V5a and V5b in conjunction with the potential divider R25–R26, the undelayed signals being applied to V4a grid and

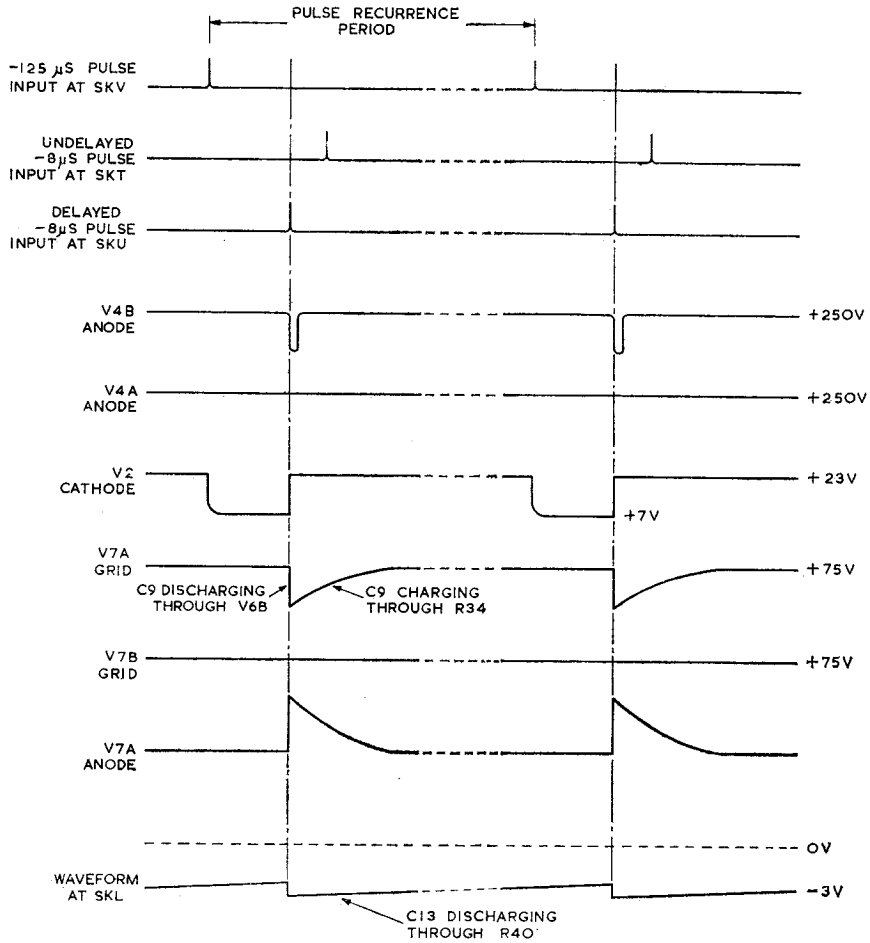


Fig. 4. Theoretical waveforms

the delayed signals to V4b grid. The 22 pF capacitors C25 and C26 swamp any stray capacitance that might affect the shape of the video signals from V3, thus ensuring that the delayed and undelayed signals at the grids of V4 are of similar shape.

13. While the cathodes of V4 are at +23V, V4a and V4b will not be brought into conduction by any video signals applied to their grids, but after the −125 microseconds pulse has switched over the bi-stable pair and reduced V4 cathode potential to about +7V any incoming signal will bring V4a or V4b into conduction. As explained in para. 11, the first signals to reach the grids of V4a and V4b after the −125 microseconds pulse has switched over the bi-stable pair are the delayed and undelayed −8 microseconds pulses. If either V4a or V4b conducts it will immediately raise the common cathode potential of V2 and V4, which is equivalent to applying a negative-going pulse to V2b grid, thereby restoring the bi-stable pair to its initial condition. Depending on which half of V4 conducts there will be produced at one anode of V4 a short negative-going pulse. If the video signals arriving at the grids of V4a and V4b are coincident then both halves will conduct and produce negative-going pulses at both anodes.

Pulse stretching circuits

14. The negative-going pulses produced at V4a anode and V4b anode are stretched to approximately 100 microseconds by V6a, C8 and R33 (monitored at SKJ) and V6b, C9 and R34 (monitored at SKH) respectively. These pulses are then applied to the grids of the differential amplifier V7, the d.c. potential at the grids being set by the potential divider R29–R30 across the +250V supply. The output developed at V7a anode (monitored at SKK) is either a positive-going pulse, in the case of a signal at V4b anode, or a negative-going pulse in the case of a singal at V4a anode.

15. A positive-going pulse at V7a anode will charge C11 through V8a producing at the storage capacitor C13 (monitored at SKL) a d.c. level of −3V, the discharge path for C11 being via R40. A negative-going pulse at V7a anode will charge C12 through V8b producing at C13 a d.c. level of +3V. If there is no error in the p.r.f. the delayed and undelayed −8 microseconds pulses will be coincident and negative pulses will be applied to both grids of V7 producing zero output at V7a anode. The d.c. level on C13 will therefore also be zero. Potentiometer RV1 LEVEL (SKL) is set to obtain this condition by compensating for any unbalance in the two signal paths.

16. If the p.r.f. is high the undelayed −8 microseconds pulse will arrive at V4 first, resulting in a positive d.c. level on C13. If the p.r.f. is low the delayed −8 microseconds pulse will arrive at V4 first, resulting in a negative d.c. level on C13. Fig. 4 illustrates the theoretical waveforms obtained in the event of the p.r.f. being low.

Balanced modulator and output circuit

17. A 500 c/s sinusoidal voltage, balanced about earth potential, from the generator (reference signal) M2 unit is applied via the two 90° phase shift networks R43 with C14, and R49 with C18 to the grids of the balanced modulator V9. This phase shift is necessary as the motor to be driven in the crystal oscillator unit is a two-phase motor requiring a supply having 90° phase difference between voltages for its control and reference phase windings. The 500 c/s supply for the reference phase winding of the motor is also derived from the generator (reference signal) M2.

18. The phase shift networks attenuate the 500 c/s input so that the waveforms at V9 grids are approximately 2V r.m.s. in amplitude. As these waveforms are in antiphase, when the d.c. levels on the grids are equal, i.e. at earth potential, the output from RV2 BALANCE (SKQ), assuming it to be balanced, will theoretically be zero. In practice however, the output is a 1 kc/s signal at low level. If the d.c. level at V9b grid changes to +3V or −3V due to an error in the p.r.f. there will be a 500 c/s output from RV2, its phase relative to the reference phase supply being dependent on the polarity at V9b grid.

19. The sinusoidal output from RV2 is applied to V10 grid. Pentode V10 and its associated circuit form a tuned driver stage producing an output at the secondary of TR2 (monitored at SKP). The tuning of TR2 by C20 is very wide-band and does not eliminate the 1 kc/s component from the output, but this 1 kc/s component will not drive the motor in the crystal oscillator unit. The gain of V10 is set by RV3 SENSITIVITY (SKQ) control during the initial setting-up of the unit to give a 1 kc/s output of 15V peak-to-peak amplitude at monitor point SKQ. This setting will provide at TR2 secondary a 1 kc/s output of 1·5V peak-to-peak and, in the event of an error in the p.r.f., a 500 c/s output of up to 100V peak-to-peak (maximum error).

Fault indicating lamps

20. Valves V11 and V1a and their associated circuit form a monitoring system to indicate when the p.r.f. is being adjusted. Initially V1a is conducting with its grid at cathode potential due to grid current through R57 and R56, and RLA is energized. The 500 c/s error signal developed at V10 anode is d.c. restored by V11 so that it appears at V11 anode (monitored at SKQ) as a sine wave about a negative d.c. level equal to approximately

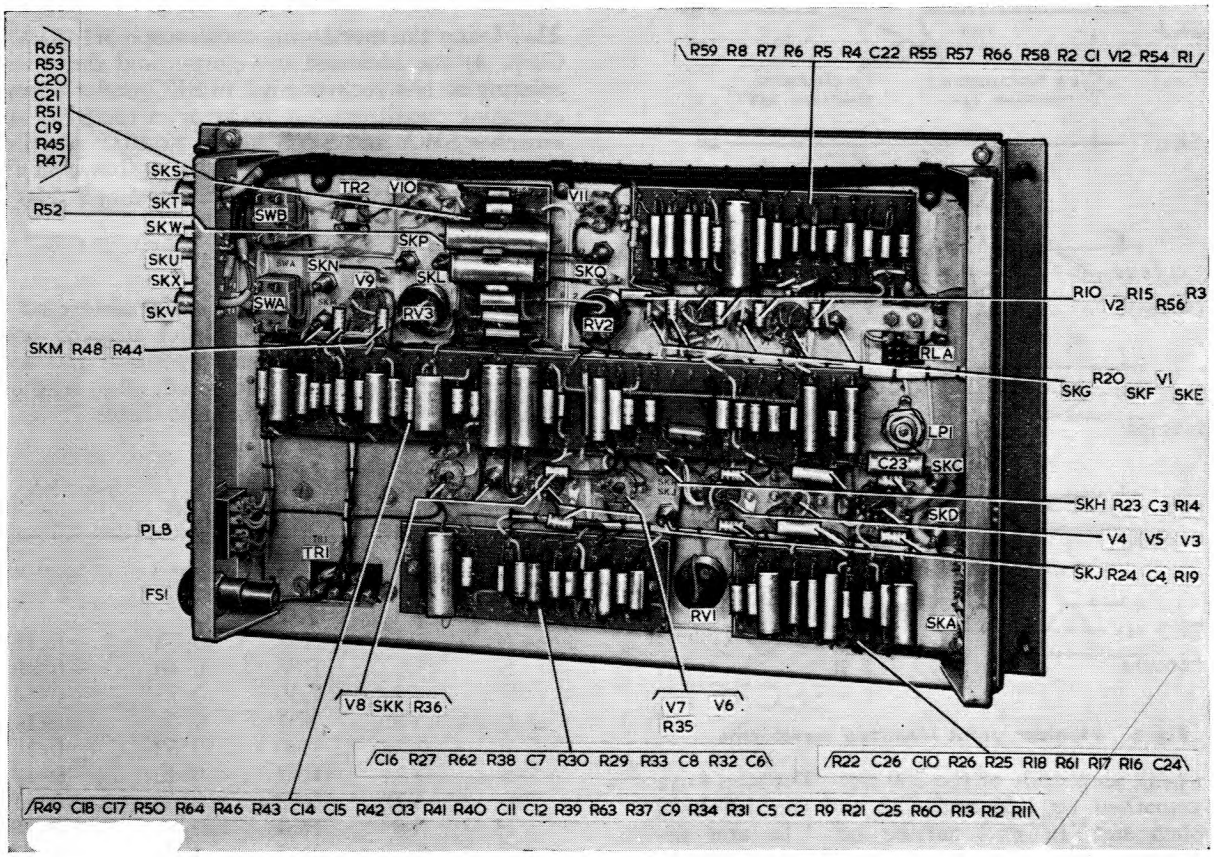


Fig. 5. Controller (p.r.f.) M1 : rear view

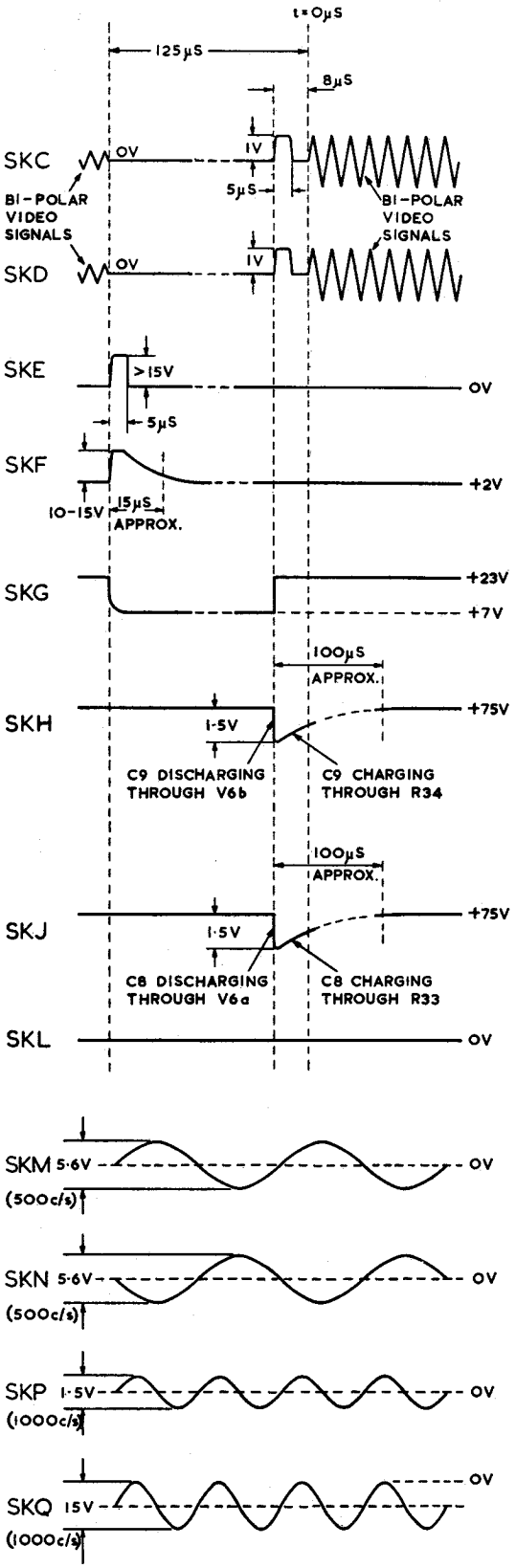


Fig. 6. Monitor point idealized waveforms

the peak amplitude of the 500 c/s. The sine wave is smoothed by R55 and C22 and the d.c. level applied to V1a grid cutting off V1a and de-energizing RLA. Contacts RLA1 connect the 6·3V a.c. supply to the fault lamp LP1, and contacts RLA3, via PLB2 and the fault relay assembly, complete the supply circuit to another fault lamp at the top of the cancellation cabinet. The circuit utilizes Miller effect by connecting C22 from grid to anode instead of from grid to earth, reducing considerably the size of the capacitor.

21. The purpose of the monitoring circuit is to indicate when there is a large error in the p.r.f. It will not indicate the small adjustments of p.r.f. which are continually taking place due to temperature drifts.

Alignment switches SWA and SWB

22. Switches SWA and SWB are used during the initial setting-up of the equipment. SWA, when switched to the ALIGN position, applies the undelayed −8 microseconds pulse to both grounded grid amplifiers V3a and V3b and thence to both grids of V4. The steady d.c. level on V9b grid (monitored at SKL) can then be set to zero by RV1, i.e. so that the outputs from V4a and V4b are balanced. With SWA in this position, RV2 is adjusted to produce a 1 kc/s waveform at V10 anode (monitored at SKQ), i.e. zero output from the balanced modulator V9. Switch SWB, when switched to the MOTOR OFF position, open-circuits the output from TR2 preventing the motor in the crystal oscillator unit from being driven unnecessarily during the setting-up procedure. Both SWA and SWB, when not in the NORMAL position, disconnect the h.t. supply to V1a (via SWA2 and SWB2), thus de-energizing RLA and switching on the fault lamps.

Monitor point waveforms

23. Using the monitoring oscilloscope M1 (*Sect.* 7, *Chap.* 4) the idealized waveforms and d.c. levels existing at test sockets SKC to SKQ under normal operating conditions (i.e. no error in the p.r.f. and switches SWA and SWB in the NORMAL position) are as indicated in fig. 6. Voltages shown in the illustration indicate the approximate amplitudes of the waveforms.

Test readings

24. With the multimeter Type 100 connected to socket SKA via the plug-to-socket adaptor, with SWA and SWB in the NORMAL position and with RV1 to RV3 correctly adjusted, the readings obtained should be as indicated in Table 1.

TABLE I

Multimeter readings

Multimeter switch position	Stage monitored	Measured across resistor	Reading	Tolerance
A	V1b	R58	0·65	±0·13
B	V1a	R66	0·46	±0·09
C	V2a	R59	0·7	±0·14
D	V3b	R61	0·5	±0·1
E	V3a	R60	0·52	±0·1
F	V7a	R63	0·49	±0·1
G	V7b	R62	0·54	±0·11
H	V9	R64	0·8	±0·16
J	V10	R65	0·25	±0·05

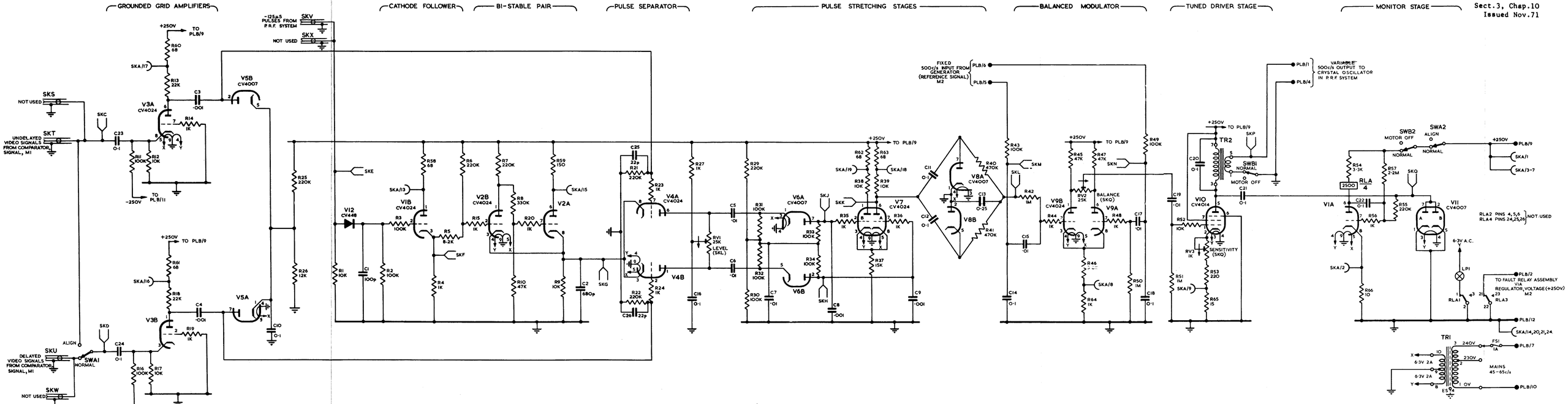


Fig.7

Controller (p.r.f.) M1: circuit

Fig.7

Chapter 11

GENERATOR (REFERENCE SIGNAL) M2

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

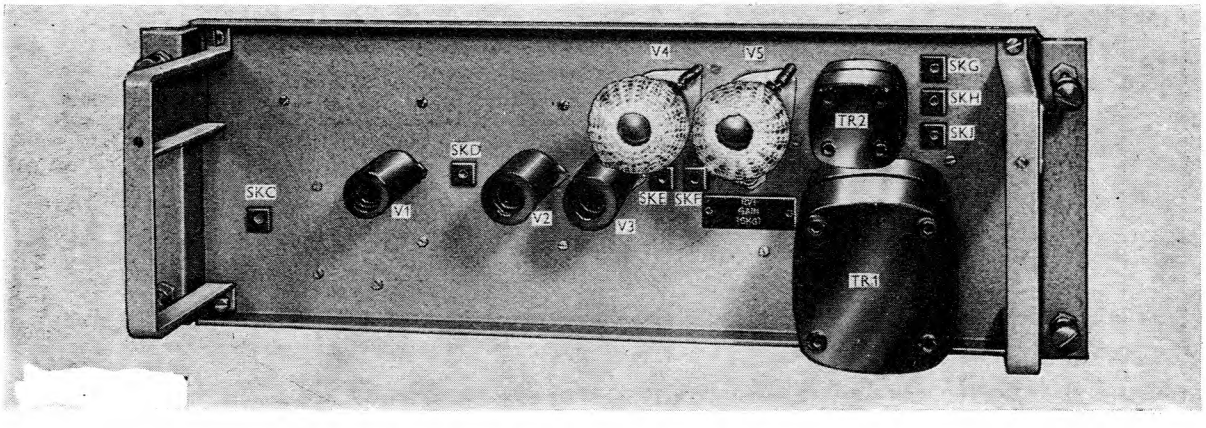


Fig. 1. Generator (reference signal) M2: front view

Introduction

1. The generator (reference signal) M2 (*fig.* 1 *and* 2) produces a 500 c/s sine wave output which is locked to the 500 c/s input originating from frequency division ◀of the output of the crystal oscillator in the p.r.f. system▶ oscillating at approximately 4 Mc/s. The signal generator is located in frame 1 of the cancellation cabinet.

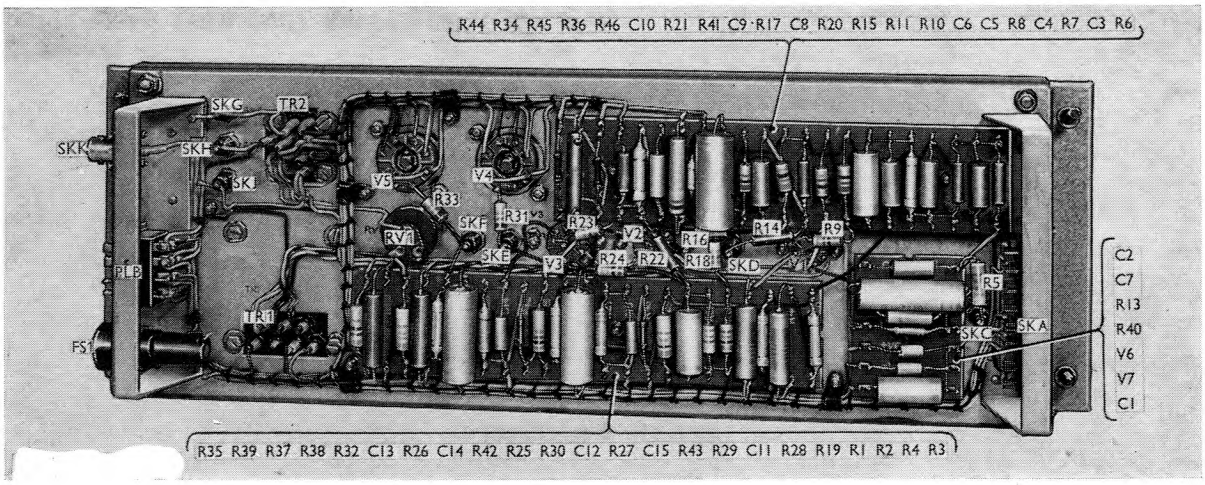


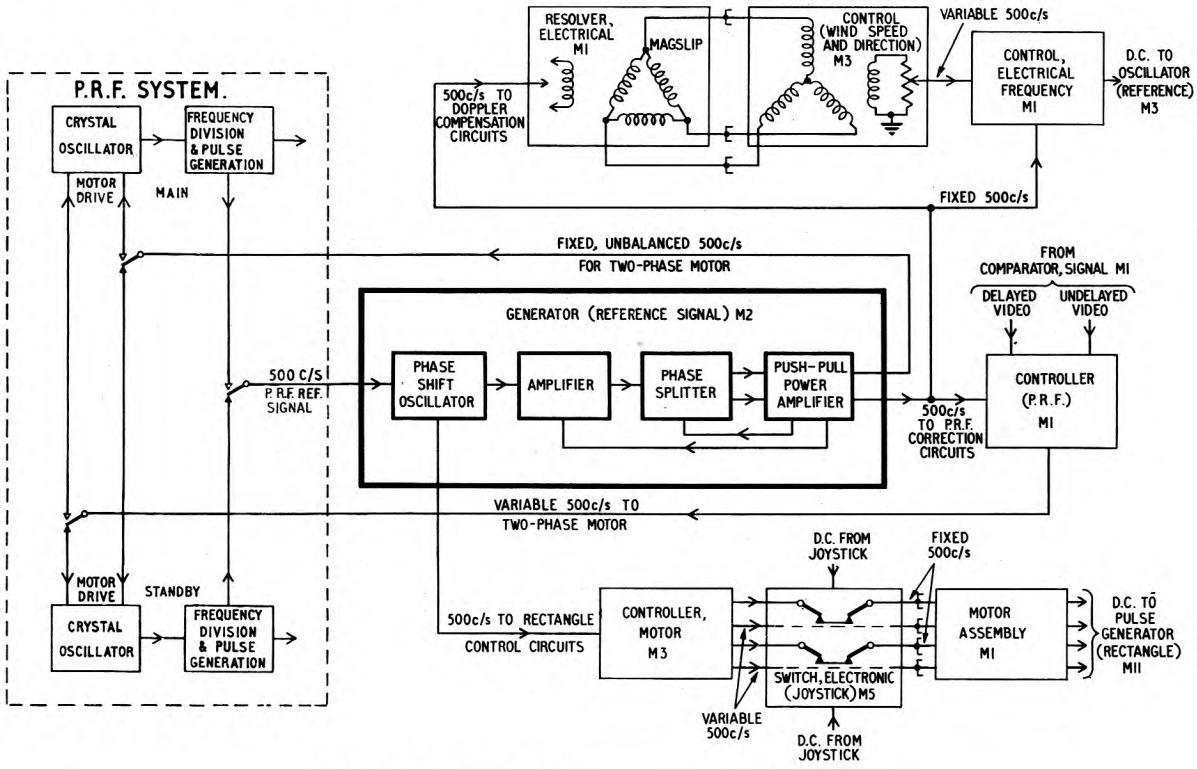
Fig. 2. Generator (reference signal) M2: rear view

2. The 500 c/s sine wave output produced by the unit provides the reference supply frequency for three independent functions in the Doppler compensation system (*fig.* 3).

(1) In the Doppler compensation circuits, the 500 c/s sine wave is used in the production of the modulating d.c. which controls the frequency of the output from the variable reference frequency oscillators, i.e. 5·25 Mc/s with a variable Doppler compensation increment or decrement of up to 500 c/s.

(2) In the rectangle control circuits, the 500 c/s sine wave is amplified and used to drive the rectangle size and move motors in the three control circuits under the control of the joystick and MOVE, SIZE, RESET switches on the control desk.

(3) In the p.r.f. control circuits, the 500 c/s sine wave is fed to the p.r.f. controller M1 (*Chap.* 10). If the p.r.f. departs from that required by the fixed mercury delay cell (*Chap.* 4), a 500 c/s driving voltage is fed from the p.r.f. controller to the motor-driven variable capacitor in the crystal oscillator ◀of the p.r.f. system▶ to correct the deviation.



◀Fig. 3. 500 c/s reference supply: block diagram▶

Performance characteristics

Input

◀3. A nominal (twice the p.r.f.) waveform input (p.r.f. reference) with an amplitude of 20V peak-to-peak is received at SKK from the p.r.f. system. This output originates from either the main or standby crystal oscillator in the p.r.f. system, according to which is in use.▶

Outputs

4. A low level 500 c/s output with an amplitude of not less than 1V peak-to-peak is taken from PLB/6 to the motor controller M3 (*Sect.* 4, *Chap.* 4) in the Doppler cabinet.

◀5. An unbalanced 500 c/s output with an amplitude of approximately 20V r.m.s. is taken from PLB/3 and PLB/2 (earth) to the p.r.f. system, where it is applied to control whichever crystal oscillator, main or standby, is originating the p.r.f. reference input.▶

6. An output, balanced about earth, with an amplitude of approximately 60–0–60V r.m.s. is taken from PLB/4 and PLB/5 to p.r.f. controller M1, the three frequency control units M1 in the Doppler cabinet, and to the electrical resolver M1 (*Sect.* 7, *Chap.* 3) in the power cabinet.

Brief circuit description

7. A 500 c/s waveform input at SKK drives the phase-shift oscillator V1, and the output from the cathode is used to supply the motor controller. A reduced output from V1 cathode is amplified by V2b and applied to the phase-splitter stage V3 so that antiphase outputs are available to drive the push-pull power amplifier stage V4 and V5. Two outputs are taken from windings of TR2. A further two windings are used to provide negative feedback, and automatic gain control, the level of which is set by RV1.

Circuit description

8. The heater supplies for the valves are obtained from TR1, the 240V a.c. supply for the transformer being received at PLB/7 and PLB/10 and applied to the transformer via FS1. The +450V supply for V4 and V5 is brought in at PLB/1, the −250V supply from the power cabinet across PLB/11 (−250V) and PLB/12 (earth) and the +250V supply from the +250V voltage regulator at the top of frame 1 across PLB/9 (+250V) and PLB/12 (earth). The +450V and −250V supplies are received via the +250V voltage regulator.

9. To prevent overdriving of the subsequent amplifier stages, the incoming 500 c/s pulse at SKK is limited to about 16V peak-to-peak by V6 and V7 in conjunction with the potential divider networks R1, R2, and R3 R4. The waveform is then applied, via the phase shift network R5 to R8, and C2 to C5 to the grid of V1 which, with its associated circuit, forms a phase-shift oscillator, frequency locked by the incoming signal. At V1 cathode (monitored at SKD) is produced a sine wave with an amplitude of not less than 1V peak-to-peak to provide an output at PLB/6. R11 is incorporated to ensure that the bias at the control grid is determined only by the amplitude of the waveform appearing at the junction of C6 and R10.

10. An output is taken from the junction of R14 and R15, and amplified by V2b. The gain of V2b is controlled by an a.g.c. loop from the output stage.

11. The output at V2b anode is applied to the cathode-coupled phase-splitter V3, the halves of which produce anti-phase outputs at the anodes; this stage is also controlled by negative feedback from winding 11–12 of the output transformer. The anode loads are shunted by capacitors C14 and C15 for suppression of parasitic oscillation.

12. The push-pull, power amplifier stage V4 and V5 operates from the +450V h.t. supply, and is driven by the anti-phase outputs from the anodes of V3 (monitored at SKE and SKF). The 500 c/s output is developed across the primary winding of transformer TR2, the outputs from the four secondary windings being used as detailed below:

(1) Winding 7–8 provides an unbalanced 20V r.m.s. output to PLB/3 (monitored at SKG) and PLB/2 (earth).

(2) Winding 4–5–6 provides a balanced 60–0–60V r.m.s. output to PLB/4 and PLB/5 (monitored at SKJ and SKH).

(3) Winding 11–12 provides negative feedback for V3b. The d.c. blocking capacitor C11 is inserted between the transformer winding and earth since the grids of V3 are at a d.c. level of approximately +45V with respect to earth as set by the divider network R28 and R29.

(4) Winding 9–10 provides a.g.c., in conjunction with RV1, for the amplifier stage V2b.

13. Manual control of the output level is provided by the GAIN (SKG) potentiometer RV1 which sets the d.c. level, between approximately +25V and earth, at the cathode of V2a. With RV1 in the maximum gain position the positive bias at the cathode of V2a is such that the valve is cut off since the negative swing at its cathode, due to the 500 c/s output from winding 9–10 of TR2, is insufficient to drive the cathode negative with respect to the anode. C9, therefore, is uncharged and V2b operates under maximum gain conditions.

14. As the setting of RV1 is reduced from the maximum gain position the positive bias on V2a cathode is reduced so that the valve conducts on negative half-cycles of input from the transformer, the degree of conduction being dependent on the setting of RV1 and on the amplitude of the 500 c/s sine wave across the transformer winding. The output from V2a anode is developed across R19 and smoothed by C9 so that a potential, negative with respect to earth, is applied to V2b grid. The

gain of V2b is therefore under the control of RV1 and of the negative feedback from the output of the unit. RV1 is adjusted to give an output of 20V r.m.s. at PLB/3.

15. The possibility of parasitic oscillation in the output is reduced by R38 and R39, across the balanced output windings of the transformer. By this means the transformer is always loaded to a certain extent.

Monitoring points

16. Test sockets, SKC–SKJ are provided and may be used for monitoring purposes. The waveforms existing at these points are illustrated in fig. 4.

Test readings

17. With the multimeter Type 100 connected to socket SKA via a plug-to-socket adaptor the readings obtained should be as indicated in Table 1.

TABLE 1

Multimeter readings

Multimeter switch position	Stage checked	Measured across resistor	Multimeter reading	Tolerance
A	V1	R40	0·68	±0·14
B	V2b	R41	0·1 to 0·6 (according to setting of RV1)	
C	V3b	R42	0·46	±0·09
D	V3a	R43	0·45	±0·09
E	V4	R44	0·59	±0·12
F	V5	R45	0·59	±0·12

i.e. ±20 per cent

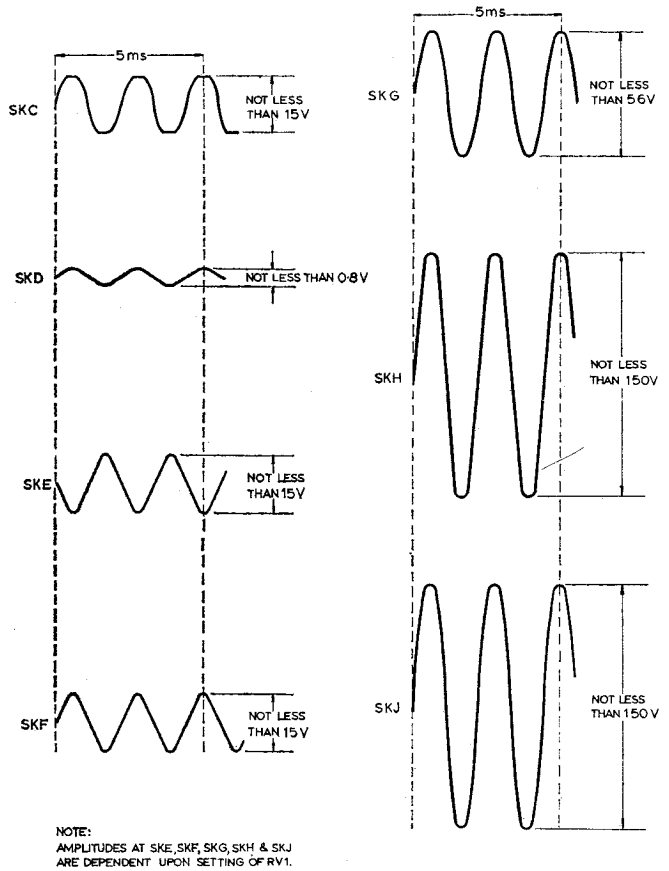


Fig. 4. Generator (reference signal) M2: monitor point waveforms

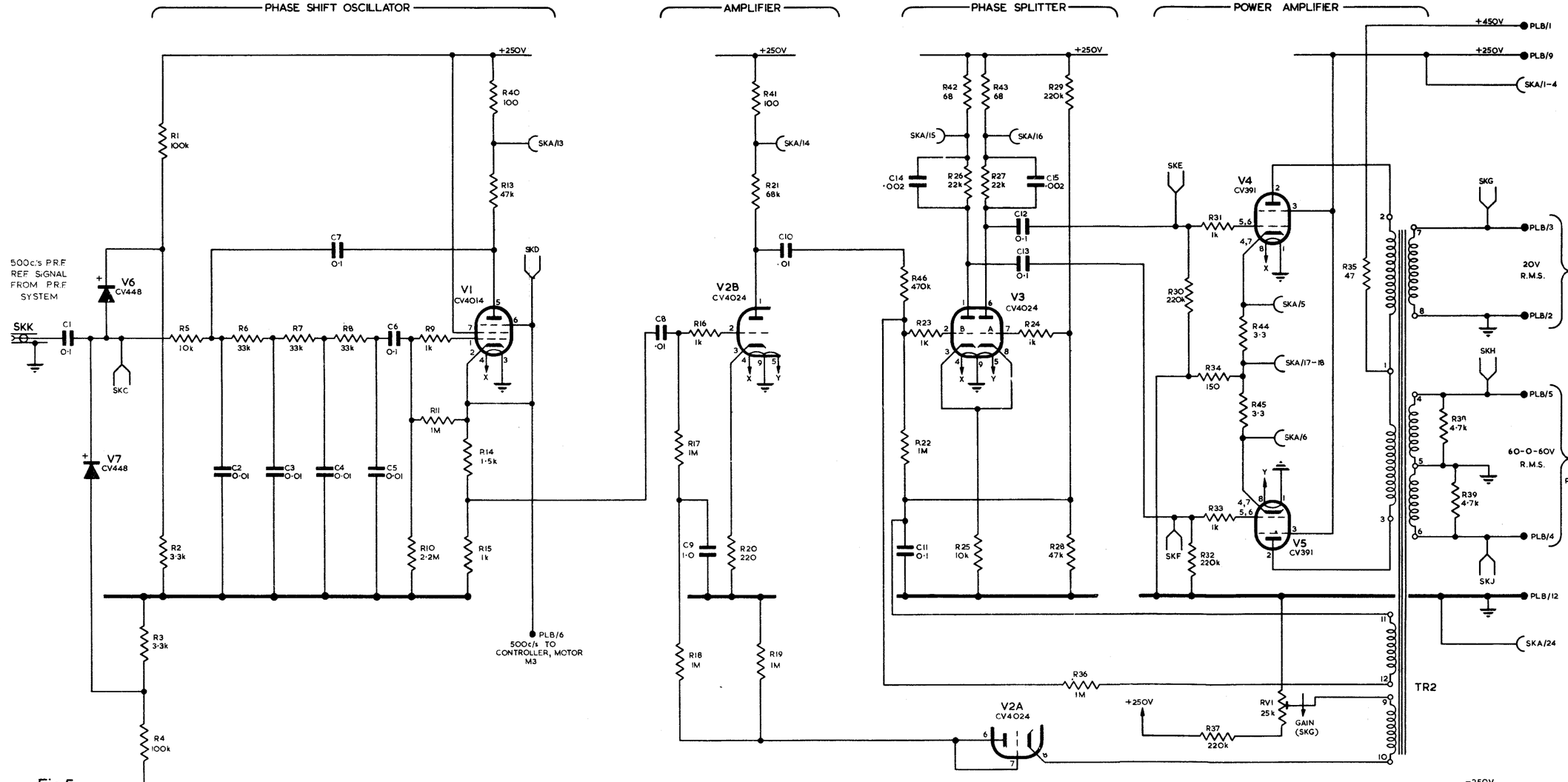


Fig.5

Generator (reference signal) M2 : circuit

Fig.5

Chapter 12

AMPLIFIER, VIDEO AND SWITCHING 5840-99-626-7183

CONTENTS

ILLUSTRATIONS

Introduction (fig. 1)

1. Two amplifiers video and switching 5840-99-626-7183 are located in the cancellation cabinet; units 104 and 105. The units are used to interface the Type 84 signal processing system with a plot and code extractor, when this unit is installed.

2. Each amplifier video and switching has a framework, with front and rear panels, and contains two power supply units and a video buffer printed circuit (panel, electronic circuit). The front panel carries mains ON/OFF switch SA, mains fuse and NORMAL lamp, two gain controls RV1 and RV2 and four monitor sockets. The rear panel carries six BNC input and output coaxial sockets, one Sealectro socket SKB and the mains plug PLA.

3. The two power supply units, PSU1 and PSU2, are attached one to the top and the other to the bottom of the frame. To the rear of PSU1 is a stand-off angle bracket carrying RL1, together with terminal posts and some components. Mounted vertically on the left-hand side, is the video buffers panel, electronic circuit, held by a guide at the bottom, and locating in socket SKL on the rear panel.

Performance (fig. 3)

4. The performance characteristics of the amplifier, video and switching 5840-99-626-7183 are as follows:-

(1) Input socket SKB, video switching waveform input: SKB will accept input signal levels up to a maximum of +15V ± 5.0V, input impedance 17.5Ω with a pulse width in the range 1 to 20ms and a repetition rate giving a 1:1 mark/space ratio. The rise and fall times should be less than 100ns between 10% and 90% points.

(2) Input socket SKC, (2 input, 2 output configuration) MTI video input: SKC will accept input signal levels up to a maximum of +5.0V, input impedance 75Ω, with a pulse width not less than 1μs.

(3) Input sockets SKD (1 input, 2 output configuration), rectangle outline marker input: SKD will accept input signal levels up to a maximum of +5.0V, input impedance 75Ω, with a pulse width not less than 1μs and a repetition rate of 12μs.

(4) Input sockets SKC and SKM: patching sockets for use with 1 input, 2 output configurations.

(5) Input socket SKN: terminated in 75Ω.

(6) Output socket SKJ: video switching waveform or rectangle outline marker outputs, amplitude +5.0V maximum into 75Ω, rise and fall times less than 150ns between 10% and 90% points and overshoots less than 0.1V.

(7) Output socket SKK: MTI video or rectangle outline marker outputs, amplitude +5.0V maximum into 75Ω, rise and fall times less than 150ns between 10% and 90% points and overshoots less than 0.1V.

(8) Mains input plug PLA: PLA accepts a mains input of 240V ± 10% 50Hz a.c. at 100mA.

5. The performance characteristics of the panel, electronic circuit 5840-99-626-7184 are as follows:-

(1) Inputs: Pins 38 and 78 will accept input signal levels up to a maximum of ±2.0V, input impedance 75Ω in each case.

(2) Outputs: Pins 26 and 64 will produce output signal levels up to a maximum level of ±5V, output impedance 75Ω in each case.

(3) Power supplies: Regulated positive and negative 10V ±0.5V d.c. at 0.5A.

Description (fig. 3)

6. The 240V a.c. main supply is fed into the amplifier video and switching at plug PLA pins 1(L), 2(N) and 3(E), via mains fuse FS1 and switch SA to the input terminals of power supply units P.S.U.1 and P.S.U.2. The output of P.S.U.2. is +10V d.c. and P.S.U.1 -10V d.c. Lamp ILP1 mounted on the front panel indicates that both power supply units are functioning correctly. When the -10V d.c. supply is available relay RLA operates, contact RLA1 closes and completes the circuit for the NORMAL lamp ILP1. The +10V d.c. is fed via socket SKL pins 74 and 32 of the video buffers panel and the -10V d.c. to pins 50 and 10. The power supply units are described in Sect. 2, Chap. 19.

7. The video buffers panel, electronic circuit contains two identical circuits, only one of which is described. The input signal at a level of ± 1.5 to ± 2.0V is fed to the long-tailed pair VT1, VT2 from pin 78. D.C. SET control RV1 sets the operating point for VT1. In practice RV1 is adjusted

such that the output at pin 64 (SKJ) is 0V when the input pin 78 is earth. VT3 is a buffer for the push-pull output circuit VT4, VT5. The overall gain of the amplifier is 2.5:1 and the bandwidth is better than 1MHz.

1 input, 2 outputs configuration

8. The rectangle outline marker from the doppler cabinet at SKM is fed into the cancellation cabinet at SKT, and then to unit 105 SKD. SKD is linked internally to SKN and SKC which in turn is linked externally to SKM. The marker input signal is thus fed to both video buffer amplifiers on the panel. SKN on unit 105 is terminated by a 75Ω terminating resistor. The rectangle outline markers are fed out of the cancellation cabinet unit 105 at SKU and SKV to the plot and code extractor and monitor suite respectively.

2 inputs, 2 outputs configuration

9. The MT1 video and switching waveform inputs are fed in at SKX and SKW respectively in the cancellation cabinet, and then to SKC and SKB of unit 104. The switching waveform input is reduced in amplitude to approximately 3V by dropping resistor R1. The video buffers function in the same manner as described in para. 7 above. The MT1 video and switching waveform outputs are fed out at SKZ and SKY respectively to the plot and code extractor.

10. A 75Ω terminating resistor is connected to socket SKN of unit 104 when the amplifier is fitted into the cancellation cabinet. Otherwise this termination is connected to SKX in the video cabinet.

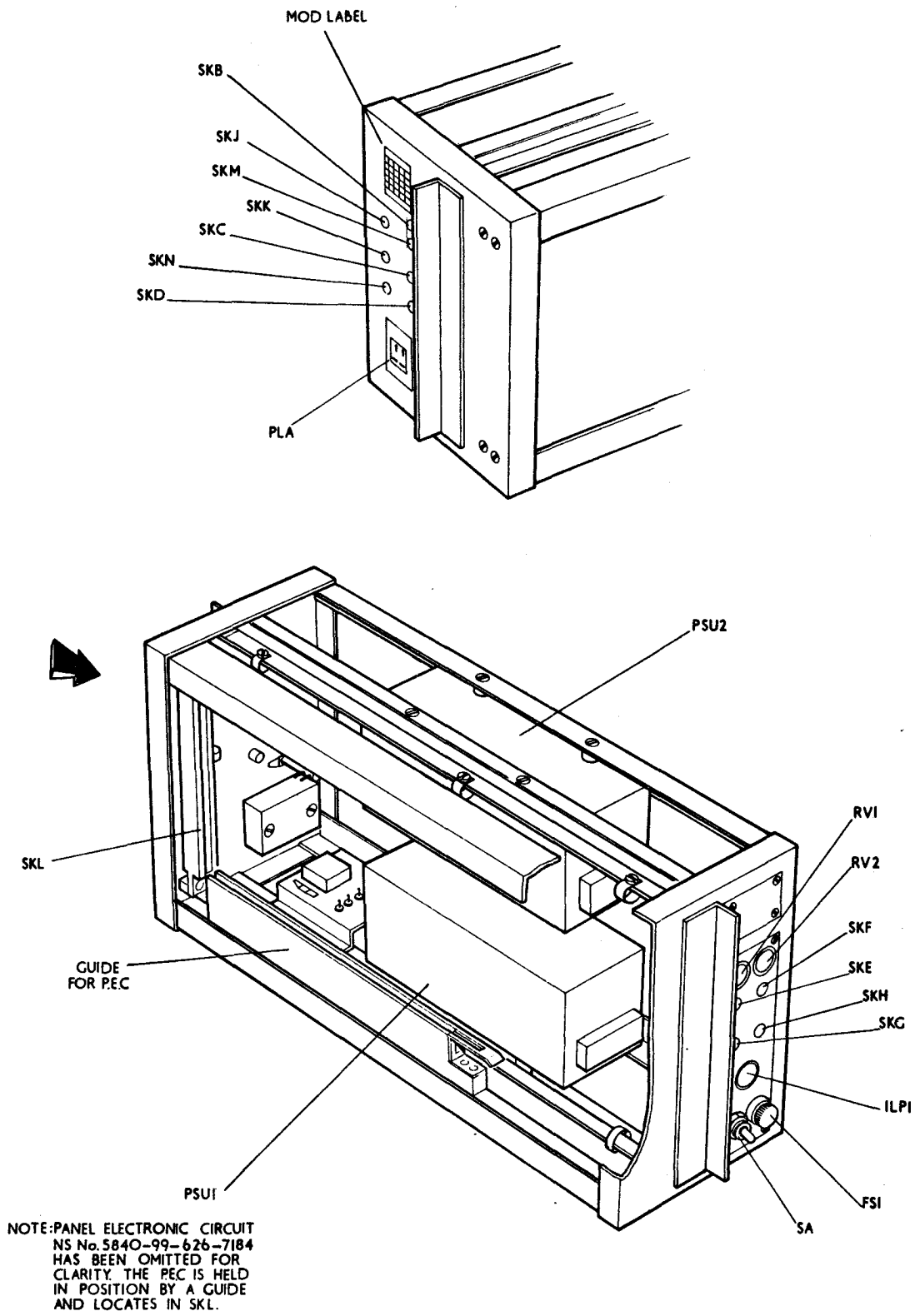


Fig. 1 Amplifier, video and switching
5840-99-626-7183: layout

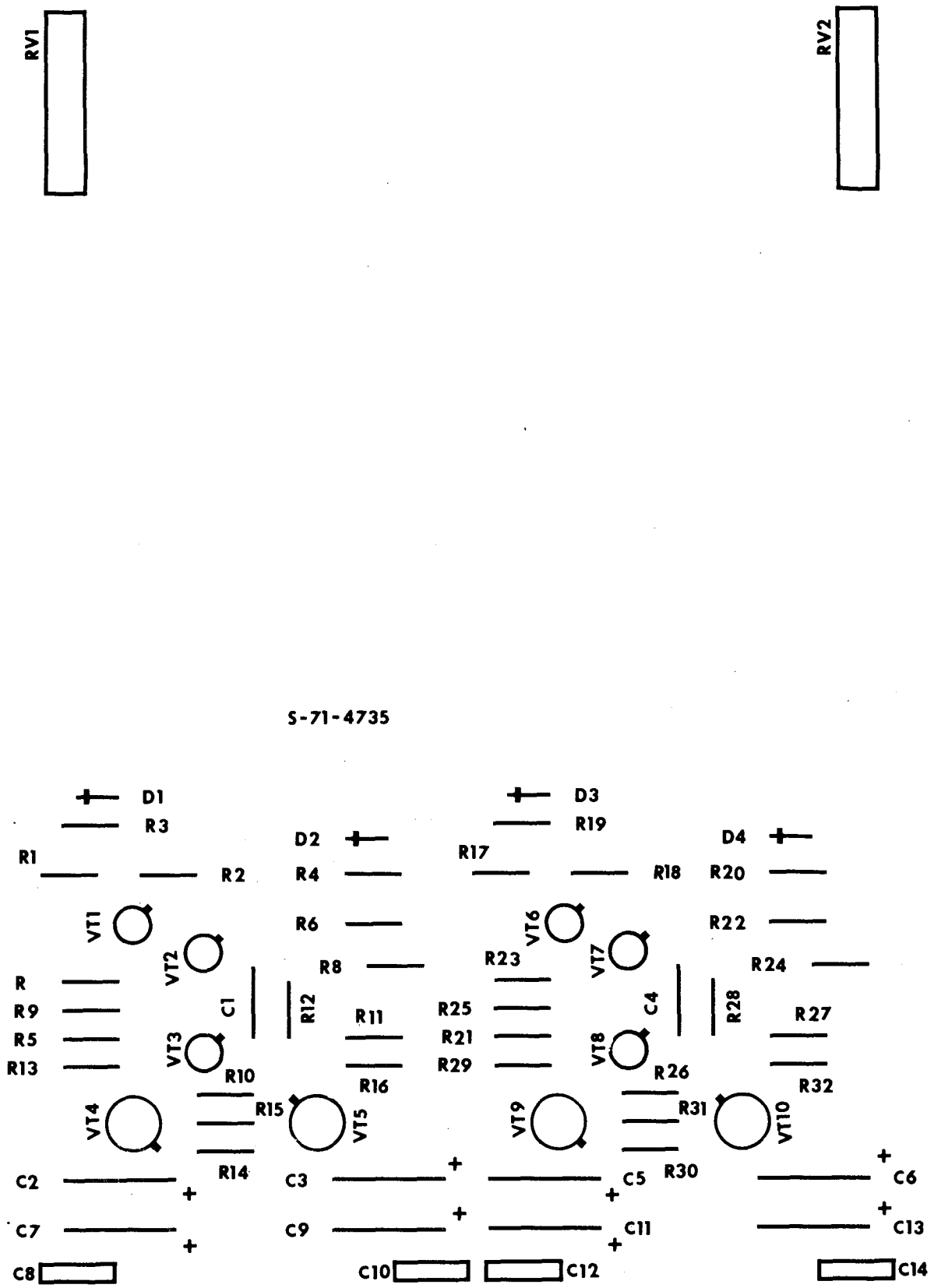
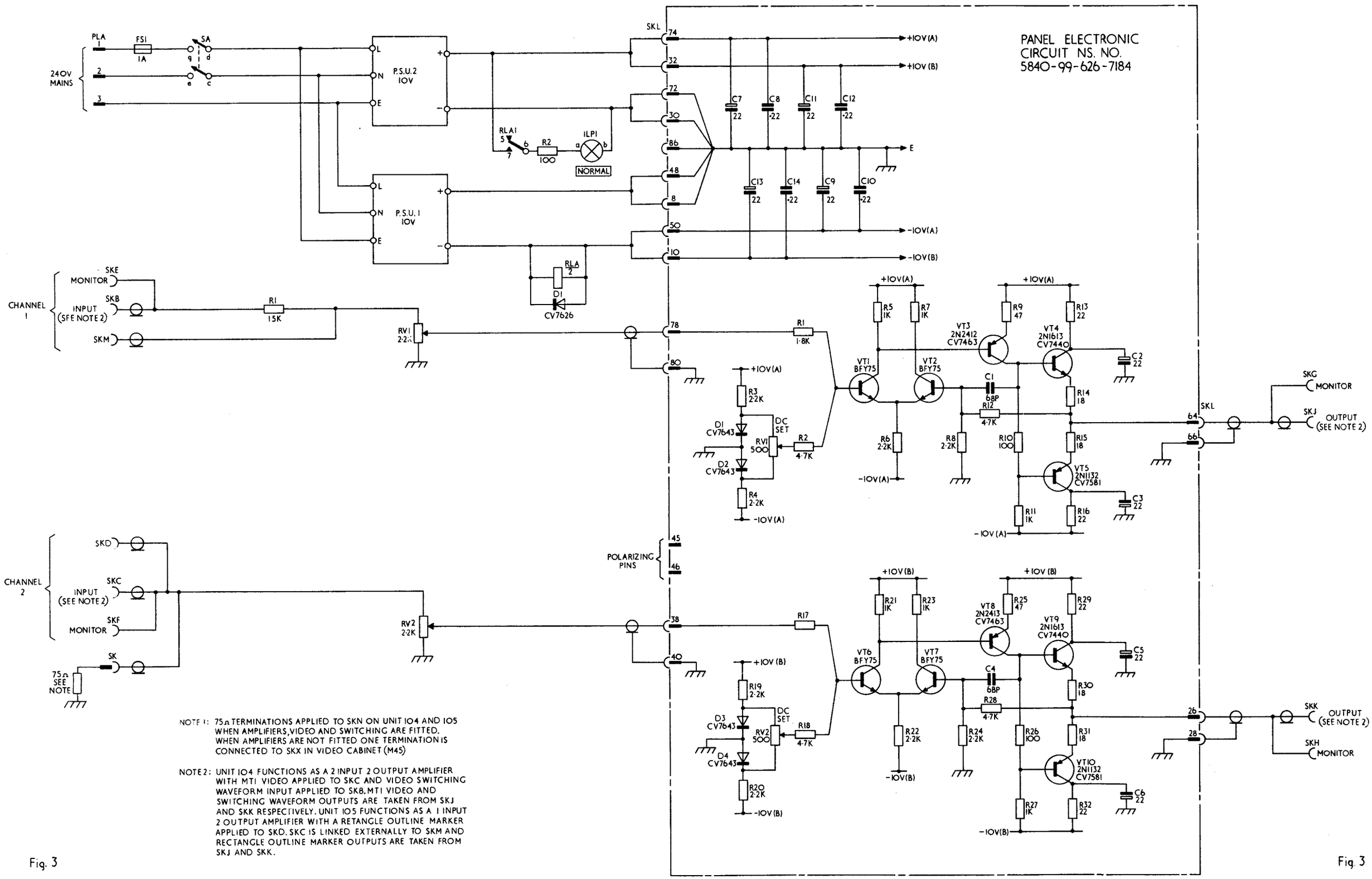


Fig. 2 Panel electronic circuit
5840-99-626-7184: layout from circuit side



NOTE 1: 75Ω TERMINATIONS APPLIED TO SKN ON UNIT 104 AND 105 WHEN AMPLIFIERS, VIDEO AND SWITCHING ARE FITTED. WHEN AMPLIFIERS ARE NOT FITTED ONE TERMINATION IS CONNECTED TO SKX IN VIDEO CABINET (M45)

NOTE 2: UNIT 104 FUNCTIONS AS A 2 INPUT 2 OUTPUT AMPLIFIER WITH MTI VIDEO APPLIED TO SKC AND VIDEO SWITCHING WAVEFORM INPUT APPLIED TO SKB. MTI VIDEO AND SWITCHING WAVEFORM OUTPUTS ARE TAKEN FROM SKJ AND SKK RESPECTIVELY. UNIT 105 FUNCTIONS AS A 1 INPUT 2 OUTPUT AMPLIFIER WITH A RETANGLE OUTLINE MARKER APPLIED TO SKD. SKC IS LINKED EXTERNALLY TO SKM AND RECTANGLE OUTLINE MARKER OUTPUTS ARE TAKEN FROM SKJ AND SKK.

Fig. 3

AL.5 June 74

Amplifier, video and switching NS. No. 5840-99-626-7183: circuit

Fig. 3

Chap. 12

Page

SECTION 4

DOPPLER CABINET

Chapter 1

DOPPLER CABINET AND INTERCONNECTIONS

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

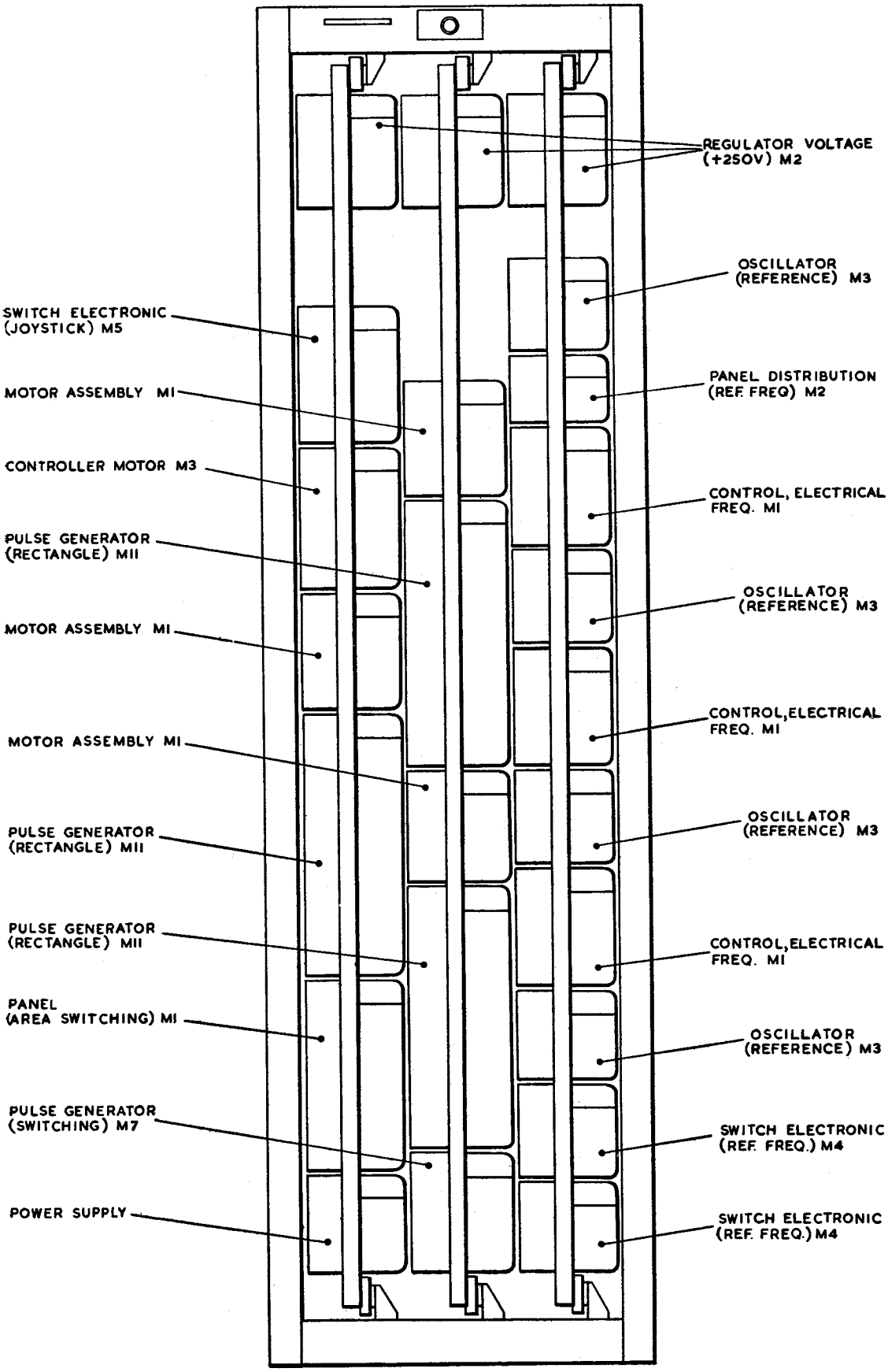


Fig. 1. Doppler cabinet : front view

Purpose of cabinet

1. The cabinet, electrical equipment M46 (*fig.* 1 *and* 2) forms part of the signal processing system, its function being to accommodate a number of units which generate the waveforms required for the production of three rectangles and a centre circle on the displays. The cabinet also contains the circuits which produce a doppler-compensated reference frequency for application to the frequency mixer stages in the i.f. cabinet, thereby providing velocity compensation for moving clutter within the three rectangles. A block diagram of the cabinet showing the various signal paths is given in fig. 3.

2. From fig. 3 it will be seen that a clear division exists between the doppler compensation and pulse generation circuits, the only interrelationship being the rectangle and circle switching waveforms fed to the electronic switches in the doppler compensation circuit.

3. In the doppler compensation circuit, a fixed frequency reference oscillator produces an output at 5·251 Mc/s. This output is fed direct to one of the two electronic switch units, and, via the distribution panel, to the three frequency control units. These units each produce a d.c. output potential derived from the input reference signal, but the polarity and level of the output is determined by wind speed and direction information derived from the console suite.

4. Each frequency control unit is associated with one of three variable frequency reference oscillators. These produce outputs at a nominal frequency of 5·25 Mc/s, but this is variable by $\pm$500 c/s, the ultimate frequency being determined by the d.c. potential from the frequency control units. A feedback loop between each pair of units maintains the frequency difference between the fixed and variable frequency oscillators.

5. The doppler-compensated outputs of the reference oscillators are fed to one of the two electronic switch units, where one of the reference signals is selected by means of rectangular switching waveforms derived from the pulse generation circuits. The selected signal is used to change the frequency of one of two frequency mixer units in the i.f. cabinet, thereby providing doppler compensation for moving clutter within the area of the selected rectangle.

6. The other electronic switch unit receives the fixed and one variable reference frequency, selection of one of these being effected by the waveform which is used to produce the centre circle on the display. The selected reference signal is used to change the frequency of the second of the two frequency mixer units, providing cancellation of fixed clutter within the circle.

7. Both frequency mixer units receive the 5·251 Mc/s output of the fixed frequency reference oscillator in addition to the variable frequency reference signal. The two reference frequencies are used in a two-stage mixing process to obtain the required amount of change in the frequency of the coherent oscillators in the i.f. cabinet.

8. The rectangle and circle markers and switching waveforms are generated in the doppler cabinet ; the three rectangles are produced by waveforms generated in the three pulse generators (rectangle) M11, while the circle is produced by a waveform generated in the pulse generator (switching) M7.

9. The display positions and sizes of the rectangles are independently variable and are determined by the MTI operator's joystick control. The control information is in the form of fixed and variable 500 c/s supplies. These supplies are used to drive motors in the motor assembly M1, producing d.c. control potentials which are fed to the appropriate rectangle generator.

10. The rectangle generators each produce a rectangular waveform, the leading and trailing edges of which vary in time according to the d.c. levels received from the appropriate motor assembly, and according to the X and Y resolved timebase waveforms from the display equipment. With the appropriate controls on the display console operated, these waveforms are fed to the panel (area switching) M1 for the production of rectangle markers, a combined gating waveform for the three rectangles and centre circle, and switching waveforms for the doppler compensation circuits.

Mechanical description

11. A mechanical description common to all cabinets is given in Appendix 1 to Sect. 2, Chap. 1. A list of weights and dimensions of individual units in the doppler cabinet is given in Table 1.

Electrical description

12. An electrical description applicable to the doppler cabinet is given in Sect. 2, Chap. 1.

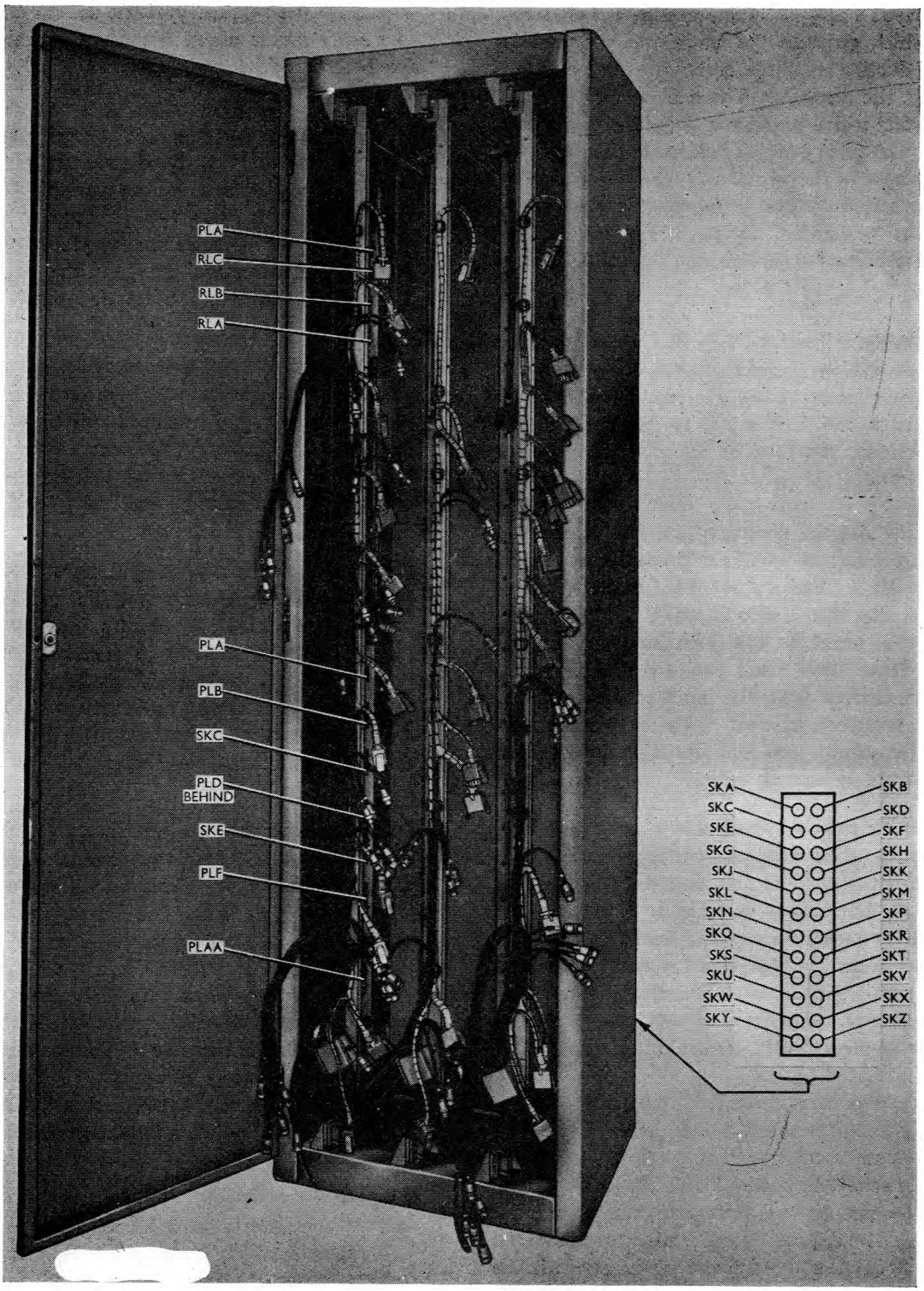


Fig. 2. Cabinet, electrical equipment M46 : rear view

Power distribution

13. Distribution of power supplies within the cabinet is shown in fig. 3. This drawing includes a circuit diagram of the cabinet fault relay assembly, a description of which is given in Sect. 2, Chap. 1. It should be noted, however, that in the doppler cabinet application an additional fault indication is given when the REMOTE/LOCAL switch on the controller motor M3 is in the LOCAL position.

TABLE I

Weights and dimensions

Title	Dimensions (inches)	Weight	A.M. Ref. No.	Chapter
Cabinet, electrical equipment M46	$84\frac{1}{4} \times 23\frac{1}{2} \times 25\frac{1}{4}$	425 lb	5975-99-999-2689 ~~10D/22648~~	1 and Appendix to Sect. 2, Chap. 1
Pulse generator (rectangle) M11	$17\frac{1}{2} \times 16\frac{1}{2} \times 6$	$12\frac{1}{2}$ lb	10V/16464	2
Motor assembly M1	$17\frac{1}{2} \times 6 \times 7\frac{1}{2}$	8 lb	10K/21350	3
Controller, motor M3	$17\frac{1}{2} \times 9 \times 6$	10 lb	10L/16759	4
Switch, electronic (joystick) M5	$17\frac{1}{2} \times 9 \times 6$	8 lb	10F/20592	5
Pulse generator (switching) M7	$17\frac{1}{2} \times 7\frac{1}{2} \times 6$	$6\frac{1}{2}$ Lb	10V/16460	6
Panel (area switching) M1	$17\frac{1}{2} \times 12 \times 6$	11 lb	10D/22652	7
Switch, electronic (ref. freq.) M4	$17\frac{1}{2} \times 6 \times 6$	5 lb 12 oz	10F/20591	8
Oscillator (reference) M3	$17\frac{1}{2} \times 6 \times 6$	$5\frac{1}{2}$ lb	10V/16463	9
Panel, distribution (ref. freq.) M2	$17\frac{1}{2} \times 6 \times 4\frac{1}{2}$	5 lb	10D/22653	10
Control, electrical freq. M1	$17\frac{1}{2} \times 6 \times 7\frac{1}{2}$	$5\frac{1}{2}$ lb	10L/16760	11
Power supply ($\pm$50V)	$17\frac{1}{2} \times 6 \times 6$	$7\frac{1}{2}$ lb	10K/5840-99-999-9082	12
Regulator, voltage (+250V) M2	$17\frac{1}{2} \times 7\frac{1}{4} \times 6$	9 lb	10D/22632	Sect. 2, Chap. 17

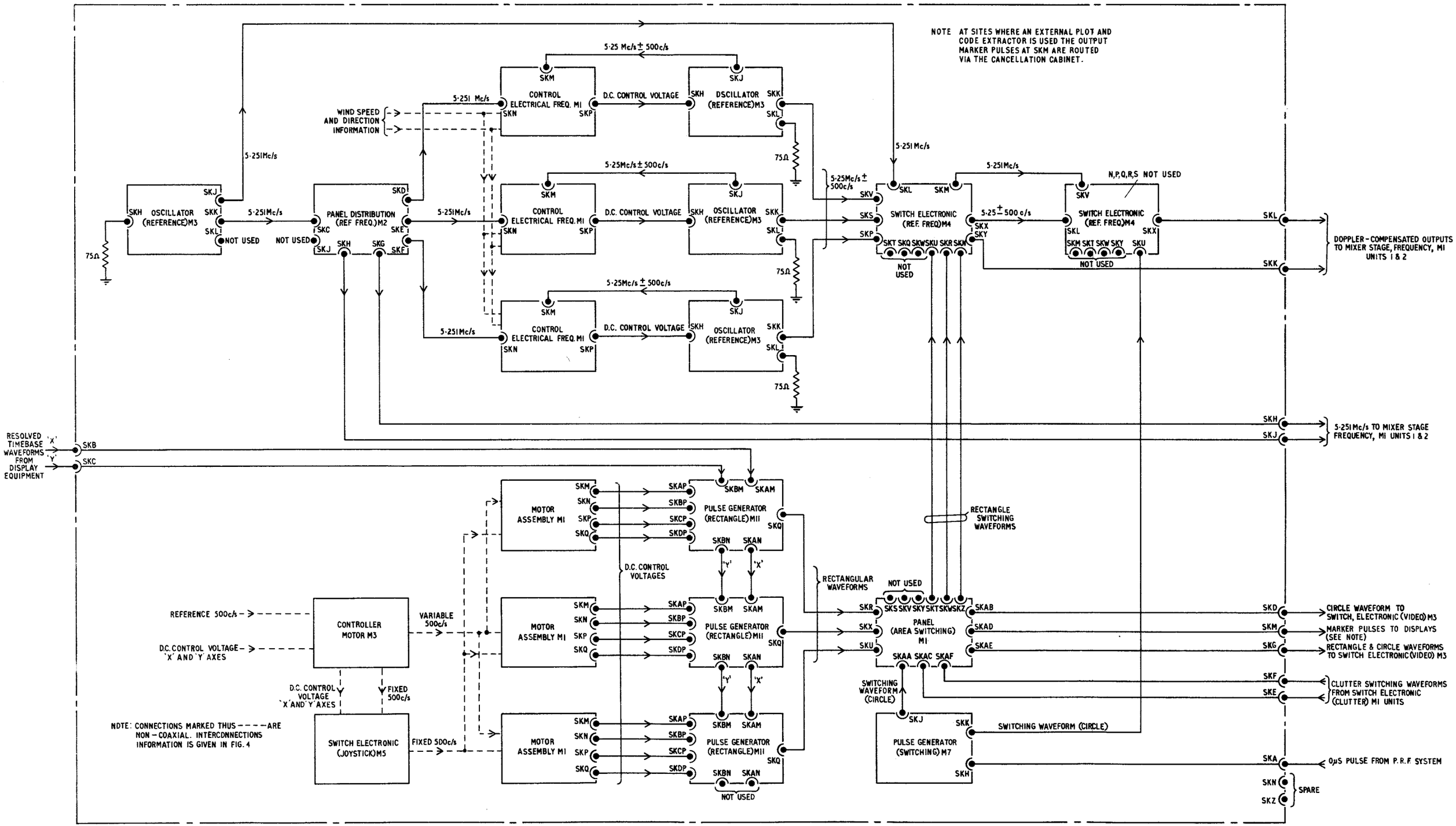


Fig. 3

Doppler cabinet: signal interconnections

Fig. 3

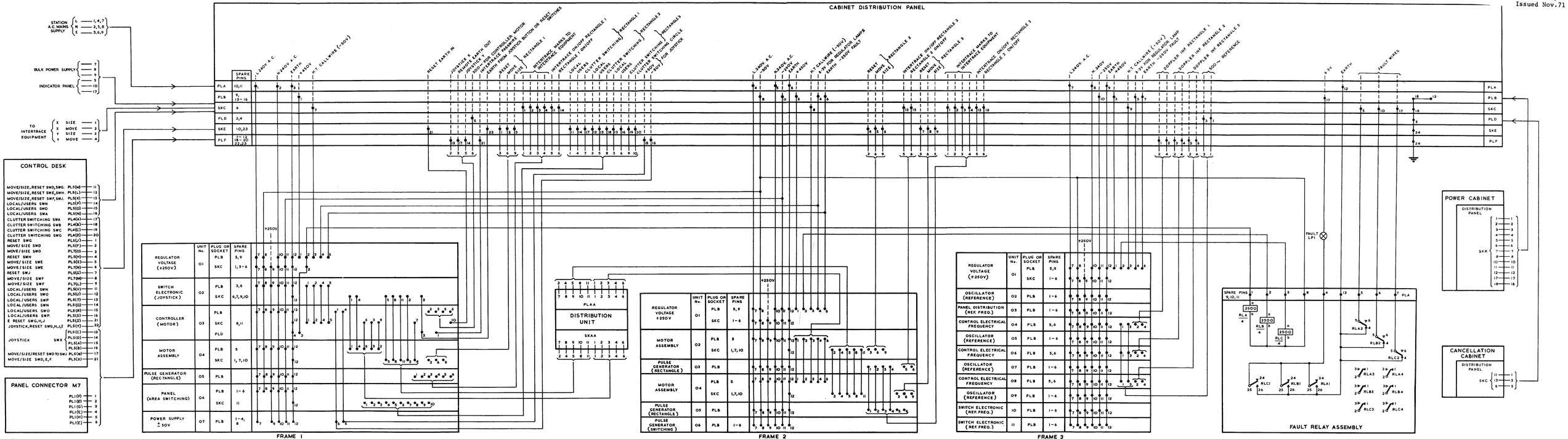


Fig.4

Doppler cabinet: power distribution

Fig.4

Chapter 2

PULSE GENERATOR (RECTANGLE) M11

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

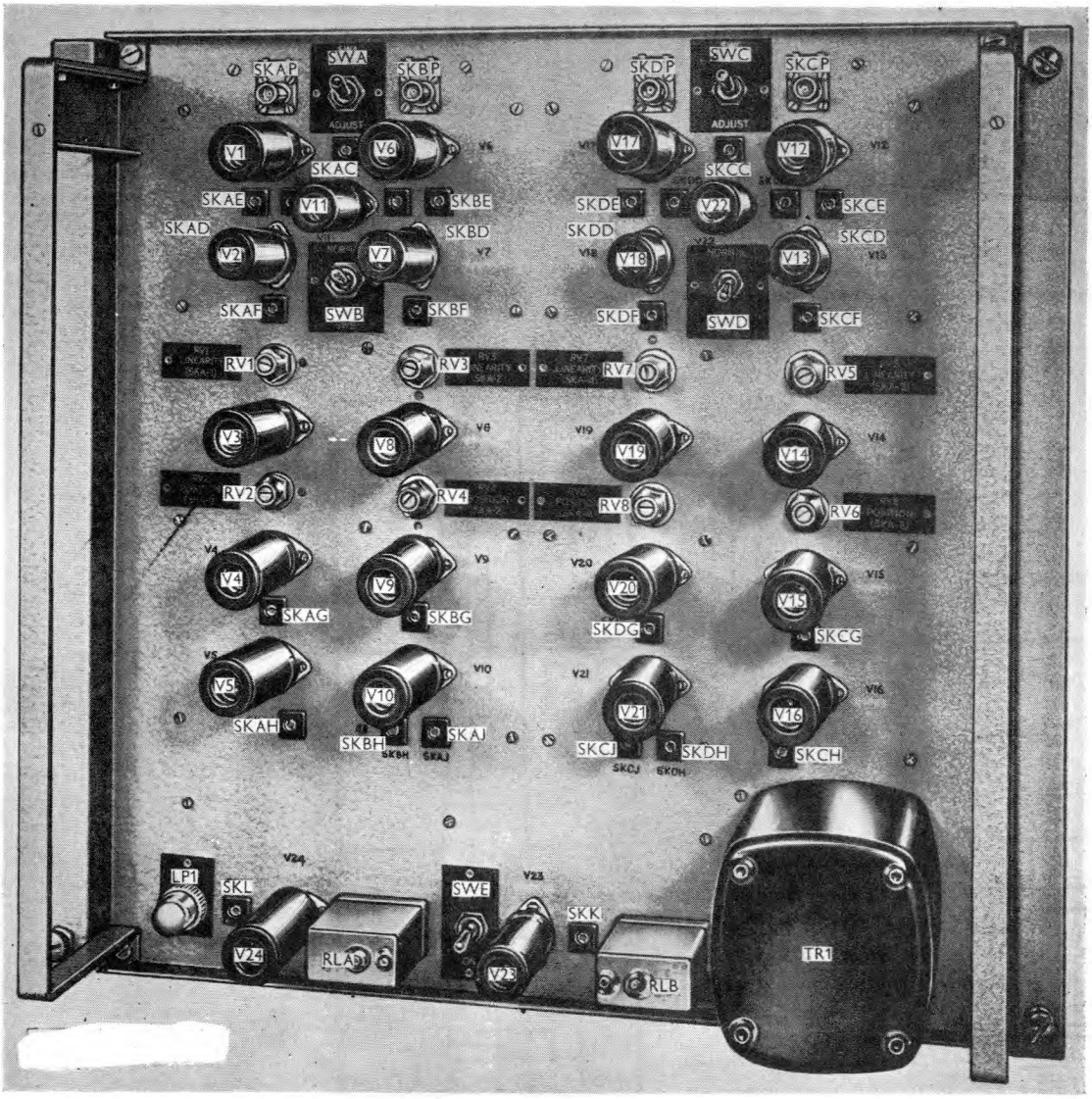


Fig. 1. Pulse generator (rectangle) M11 : front view

Introduction

1. The purpose of the pulse generator (rectangle) (*fig.* 1 *and* 8) is to produce a rectangular waveform whose leading and trailing edges vary in time according to the d.c. levels received from a motor assembly M1 (*Chap.* 3) and according to the resolved timebase waveforms received from the display equipment. Three pulse generators are used, their outputs being fed to the panel (area switching) M1 (*Chap.* 7) for the production of :

(1) Three rectangle markers.

(2) A combined video gating waveform for the three rectangles and the circle areas.

(3) A reference frequency gating waveform.

With the MOVE/SIZE switches or the RESET switches on the display console operated, d.c. outputs from the pulse generators are fed to the display intertrace circuits for the production of dot markers at the corners of the rectangles.

2. In order to adjust the position or the size of a particular rectangle, the appropriate MOVE/SIZE switch on the display console is operated and the joystick control moved to a position which sets the rectangle corner dots moving in the required direction at a suitable speed (the latter being controlled by the amount of radial movement of the joystick) (*fig.* 2). The d.c. outputs from the joystick operate circuits in the motor controller M3 (*Chap.* 4) and the electronic switch (joystick) M5 (*Chap.* 5) to provide fixed and variable 500c/s inputs for three motor assemblies M1. The 500c/s supplies are applied to the MOVE or SIZE motors in the appropriate motor assembly and the motors rotate to drive potentiometers connected across the +250V and −250V supplies. The resulting d.c outputs are fed to the appropriate pulse generator (rectangle). The rectangle may be returned to its preset position by the operation of the appropriate RESET switch, the joystick being inoperative under these circumstances.

3. With the LOCAL/USERS switch on the display console in either operated position, three rectangle markers are produced for the monitor displays. With the switch in the USERS position a comprehensive switching waveform, giving precedence to rectangle 1 over rectangles 2 and 3 and to rectangle 2 over rectangle 3, is produced for the video switch controlling the rectangle areas. Gating waveforms are fed to the electronic switch (reference frequency) M4 in either operated position of the LOCAL/USERS switch, so that doppler compensation is applied to the rectangle areas.

4. The pulse generator associated with rectangle 1 is mounted in frame 1 of the doppler cabinet and those associated with rectangles 2 and 3 are located in the third and fifth positions from the top of frame 2 in the same cabinet.

Performance characteristics

Inputs

5. Each of the pulse generators receives six inputs. Four d.c. levels, each at a selected value between +50V and −50V according to the setting required by the operator, are received from the associated motor assembly at sockets SKAP, SKBP, SKCP and SKDP. X and Y resolved timebase waveforms are received from the associated display equipment, at sockets SKAM and SKBM respectively.

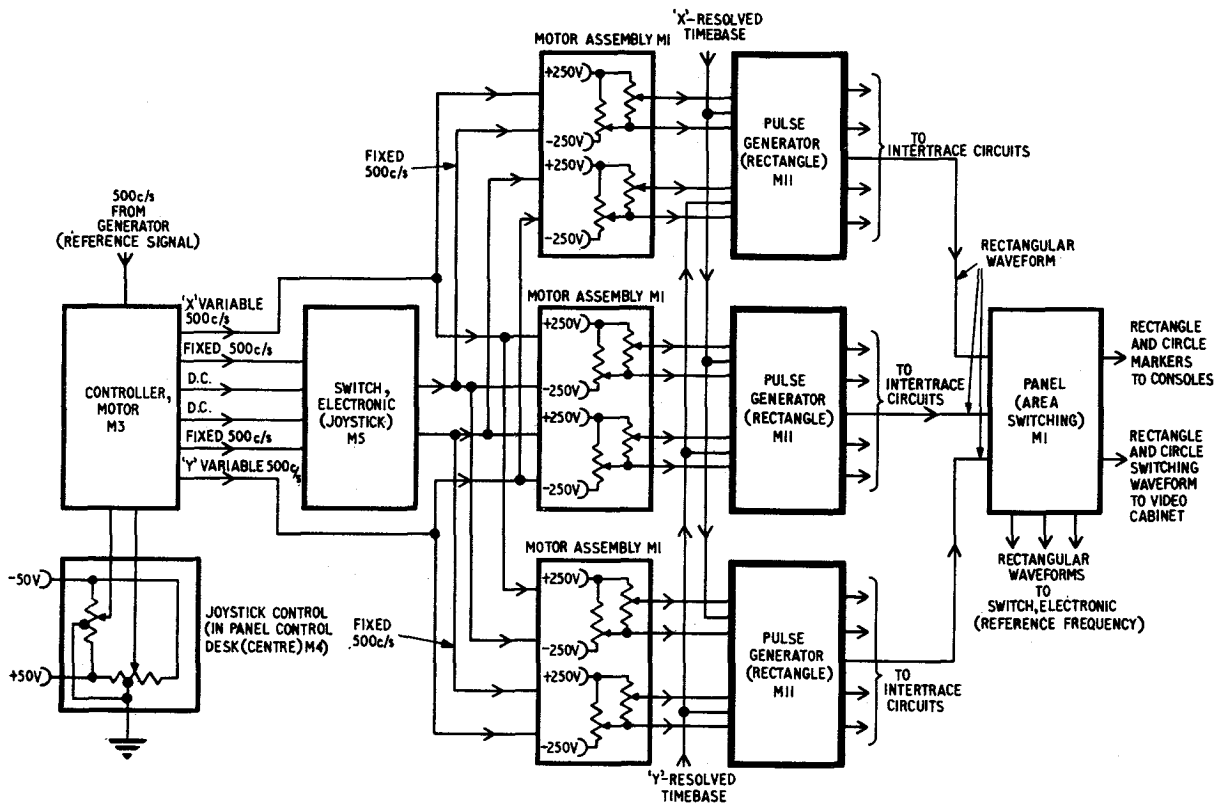


Fig. 2. Pulse generator (rectangle) MII : functional schematic

Outputs

6. The output at SKQ consists of a rectangular waveform at the p.r.f. of the timebase waveforms, with a mark-to-space ratio according to the inputs received. Four secondary outputs, which are d.c. levels proportional to the four input d.c. levels, are fed to the display equipment for intertrace marker production.

Brief circuit description

7. By referring to the block diagram (*fig.* 3) it will be seen that each of the two resolved timebases is applied to two diode stages, the cut-off points of which are set by d.c. level inputs via cathode follower stages. Each of the diode stages is followed by an amplifier stage which is arranged to conduct just below cut-off voltage, so that it amplifies that portion of the timebase selected by the input d.c. level to produce a positive-going waveform at its anode. The rectangular waveforms thus produced are amplified, limited, and applied in the correct phase to two adding circuits, one for the outputs derived from the X resolved timebase and the other for the outputs derived from the Y resolved timebase. The two rectangular waveforms thus produced are added in an AND gate to produce a single rectangular waveform with its leading and trailing edges variable in time as determined by the input d.c. levels and the instantaneous levels of the timebase waveforms. This waveform is amplified, limited and applied via a further cathode follower stage to the output socket of the unit.

8. D.C. outputs for the intertrace circuits in the associated display equipment are taken from one half of each of the input cathode follower stages.

Circuit description (*fig.* 10 *and* 11)

9. Heater voltages for the valves are supplied from TR1, the 240V a.c. primary supply for the transformer being received at PLB/7 (via FS1) and PLB/10. The supply is controlled by the main system switch. The −250V supply from the power cabinet is brought in across PLB/11 (−250V) and PLB/12 (earth). The +250V supply from the +250V voltage regulator is brought in via PLB/9 (+250V) and PLB/12 (earth).

Note . . .

The fuse-link in the a.c. mains input line to the valve heaters supply transformer is of the anti-surge type. This type of fuse-link is fitted as a precaution against rupture during the initial current surge that occurs upon switching-on when the valves are cold.

10. The incoming d.c. potentials, which may lie at any level between +50V and −50V according to the operation of the joystick control, are brought in at sockets SKAP, SKBP, SKCP and SKDP where they are connected via switch SWA and SWC (in the NORMAL position) to the grids of both halves of each of the double-triode cathode follower stages (V1, V6, V12, V17). The conducting levels of each cathode follower and thus the potential across the separate cathode resistors are set by the incoming d.c. potential. In figs. 3 and 4,

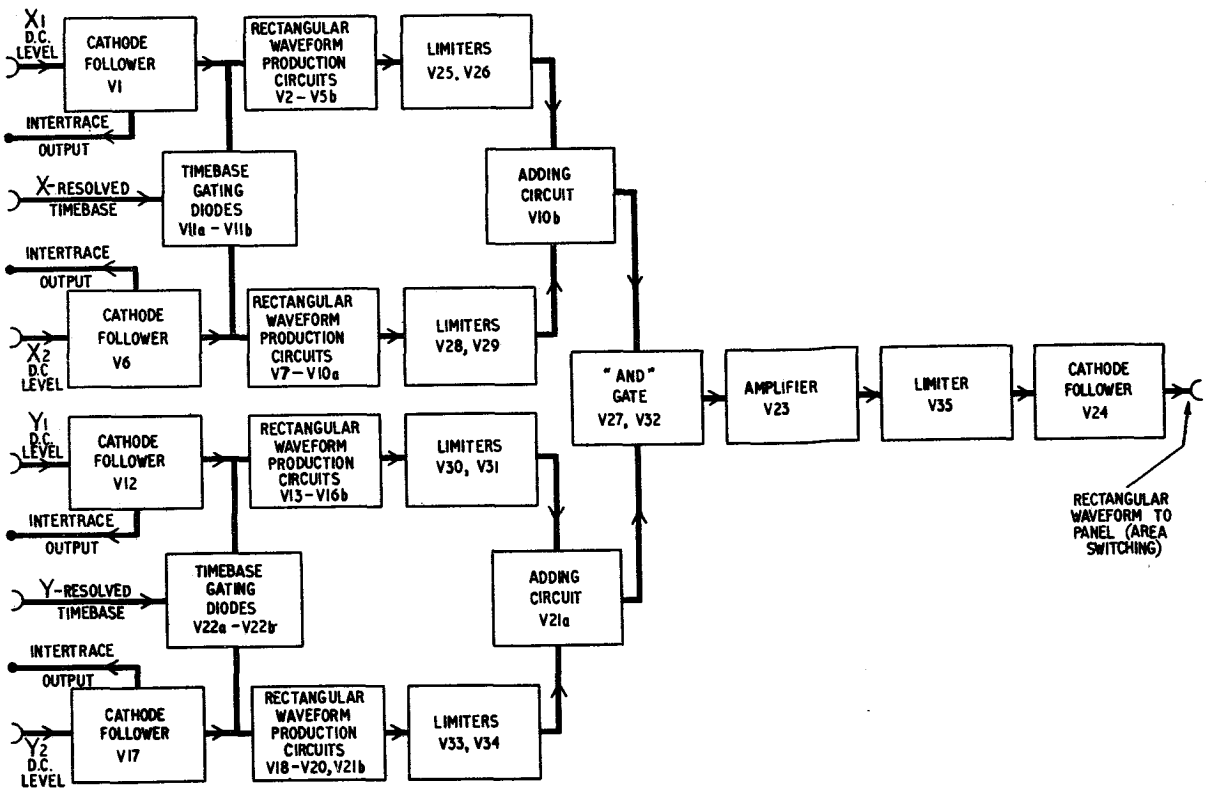


Fig. 3. Pulse generator (rectangle) M11: block diagram

these incoming d.c. potentials are referred to as X1, X2, Y1 and Y2 (at sockets SKAP, SKBP, SKCP and SKDP respectively).

11. The d.c. output from one half of each of the cathode followers (e.g. V1b) is taken via contacts of RLB, which is operated to provide intertrace markers in the display equipment, to the intertrace output sockets PLB/1–4. With SWB and SWD in the ADJUST position the outputs are connected to the grids of the pentode stages (V2, V7, V13, V18) for test purposes.

12. Considering the circuits associated with V11a and V2, the resistor R5 in the cathode of V1a is included in the potential divider chain R6, R7, R5 which determines the potential at the anode of V11a and thus (with SWB operated to the NORMAL position) at the grid of the pentode stage V2.

13. The resolved timebase waveforms at SKAM and SKBM are fed to the cathodes of the double diodes V11 and V22. These waveforms vary in amplitude from maximum positive through zero to maximum negative, as the p.p.i. trace rotates. The limits are approximately +50V and −50V.

14. ◀With V11a cathode potential at an instantaneous value positive to its anode, V11a is cut off and V2 grid potential is determined by the resistor chain R5–R7. Under these circumstances, V2 conducts and a negative-going waveform appears at its anode (*fig.* 4(*a*)). When the potential at V11a cathode changes to such a value that V11a conducts through R8, R7 and R5, V2 is cut off and a positive-going waveform is produced at its anode (*fig.* 4(*b*)). The leading edge of this waveform commences when V11a conducts, and the trailing edge occurs when V11a is cut off, allowing V2 to conduct again.▶

15. The production of waveforms at the anodes of V7, V13 and V18 follows the same process but, as will be shown later, it does not follow that all, or indeed any, of these waveforms will be produced at a given instant. An example of this is shown in fig. 4(*c*) where the timebase is positive-going but the d.c. input is negative, so that the diode is cut-off for the whole of the timebase period and V2 conducts steadily.

16. Since the cathode of V2 is returned via R12 to the cathode of V1a, the potential at the lower end of R12 is varied according to the input d.c. level to the unit and hence the gain of the valve is varied. The grid of V3b is returned to the slider of a potentiometer RV1, LINEARITY, connected in series with R13 so that the potential at the grid of the valve is determined proportionally from the input d.c. level which appears across R5.

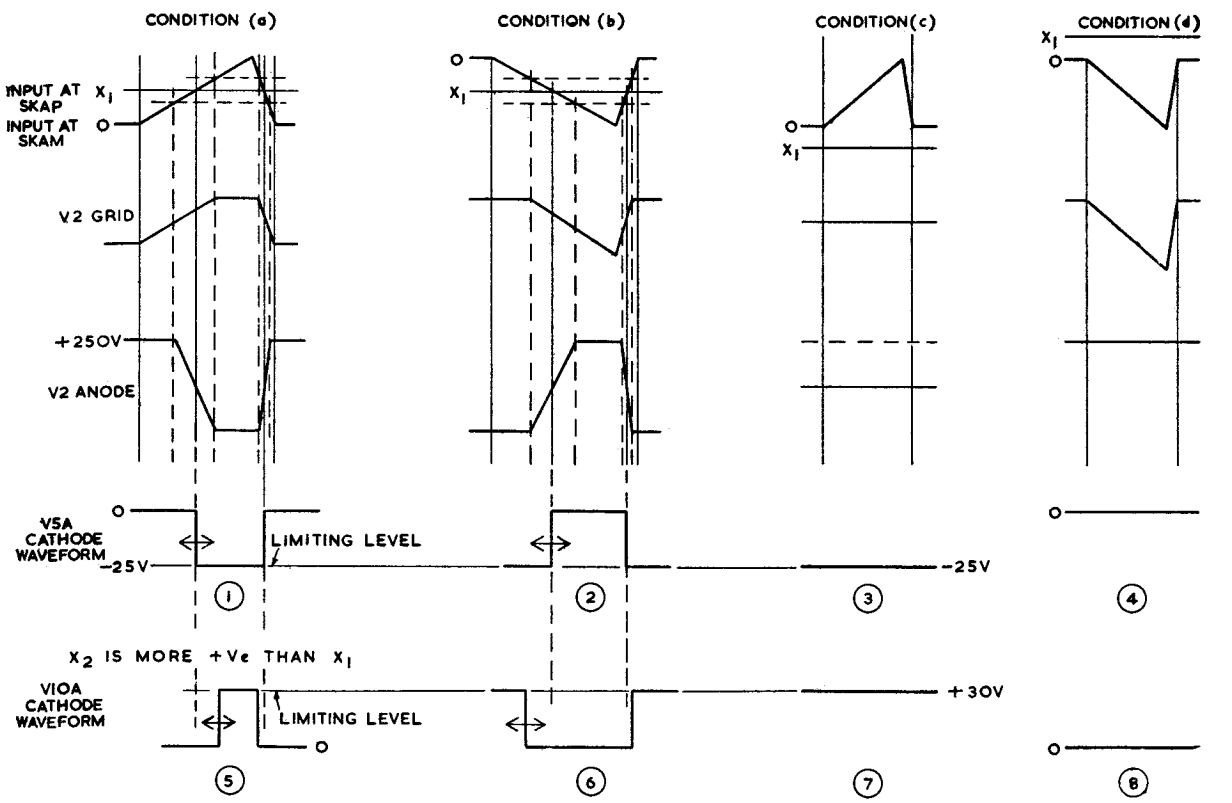


Fig. 4. Initial waveform production

17. Thus, with a positive d.c. input level, V2 is cut-off for the majority of the time so that its average anode potential is high. The grid of V3b is therefore made more positive, and its anode potential is low. The reverse happens with a negative d.c. level. The mean potential applied to the grid of the following stage, V3a, is the same for all input d.c. levels, since the input to V3a grid consists of the means of the potentials at the anodes of V2 and V3b as taken from the junction of resistors R14 and R15. RV1 is adjusted to obtain substantially equal readings, on a meter connected between SKA/1 and earth, for all levels of d.c. input at SKAP (with SWB switched to ADJUST).

18. The junction of R14 and R15 is d.c. coupled to the grid of V3a via resistors R19–R20 and potentiometer RV2 ; R19 and a portion of RV2 being bypassed by capacitor C1 which sharpens the leading and trailing edges of the waveform. RV2, POSITION (SKA–1), is adjusted so that V3a operates under the correct conditions. V3a, V4b, V4a and V5b are connected as d.c. amplifiers and a rectangular waveform is produced at the anode of V5b during the period selected by the input d.c. level. V5b anode waveform is fed to the grid of V5a so that a rectangular waveform is produced at V5a cathode. This waveform is held between the limits of earth and approximately −25V by the action of the diodes V25 and V26 and the potential divider chain R41–R42 across the −250V supply.

19. Similar action takes place in the circuit V6–V10a and V11b, except that in this instance the number of d.c. amplifier stages is reduced by one so that the waveform at the cathode of V10a is opposite in polarity to that at V5a cathode. This waveform is held between the limits of +30V and earth by the action of the diodes V28–V29 and the resistor chain R86–R87 across the +250V supply.

20. From the examples of the waveforms (*fig.* 4) it will be seen that four different combinations of waveforms can be produced. These may be summarized as follows :

(1) When the input at SKAM consists of a positive-going timebase and the d.c. inputs at SKAP and SKBP are also positive, a negative-going waveform with its leading edge variable in time and its trailing edge at the end of the timebase is produced at the cathode of V5a (*fig.* 4(*a*)). The waveform produced at the cathode of V10a is positive-going with its leading edge variable in time, but after that at V5a cathode, and with its trailing edge near the end of the timebase.

(2) When the inputs at SKAM, SKAP and SKBP are all negative the waveform produced at V5a cathode is negative-going, with its leading edge at the end of the preceding timebase but with its trailing edge variable in time (*fig.* 4(*b*)). The waveform produced at the cathode of V10a is positive-going, with its leading edge near the end of the preceding timebase and with its trailing edge variable in time but preceding that at the cathode of V5a.

(3) When the input at SKAM consists of a positive-going timebase, that at SKAP of negative d.c. and that at SKBP of positive d.c., a positive waveform as in (1) above is produced at V10a cathode but, as under these circumstances V11a does not conduct, the output at V5a cathode is a steady potential of −25V. Should the input at SKBP also be negative d.c., V11b will not conduct so that the output at V10a cathode is a steady potential of +30V (*fig.* 4(*c*)).

(4) When the input at SKAM consists of a negative-going timebase, that at SKAP of negative d.c. and that at SKBP of positive d.c., the output at V5a cathode consists of a negative-going waveform as in (2) above. However, as under these circumstances V11b is conducting all the time, V10a cathode is at a steady earth potential. Should the input at SKAP also be positive d.c. V11a will conduct all the time, so that the output at V5a cathode is a steady earth potential (*fig.* 4(*d*)).

21. The waveform at V5a cathode is fed to the grid of V10b via R43 and that at V10a cathode to the grid of V10b via R88, the waveforms being added in the resistive network R43 and R88. The resultant waveform in the cases (1) and (2) above (*fig.* 5(*a*)), is a negative waveform with its leading and trailing edges variable in time, whereas in cases (3) and (4) (*fig.* 5(*c*)), only the trailing edge is variable in time, the leading edge occurring at the end of the preceding timebase. Where, as shown in fig. 4(*c*) and (*d*), the outputs from V5a and V10a cathodes are steady d.c. levels, the addition of the outputs results in d.c. levels (*fig.* 5(*b*)).

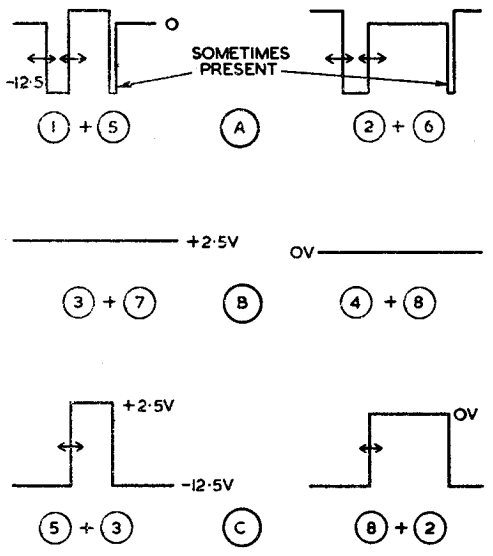


Fig. 5. Combination of initial waveforms

22. Similar waveforms, but with different time intervals, are produced at the grid of V21a from the inputs at SKBM, SKCP and SKDP.

23. The waveforms from the cathodes of V10b and V21a are added in the AND gate comprising the diodes V27, V32 and the potential divider network R180–R181 across the −250V supply, so that during the coincidence periods of the negative waveforms at both cathodes a negative waveform is fed to the grid of V23 (*fig.* 6). The positive waveform produced at the anode of V23 is limited to approximately +30V with respect to earth by the diode V35 in conjunction with the resistor chain R187–R188 across the +250V supply.

24. With SWE in the ON position and relay RLA operated, the positive waveform is fed to the grid of the cathode follower stage V24 to produce a positive-going rectangular waveform at the output socket SKQ (*fig.* 7). With SWE in the OFF position and relay RLA operated or with relay RLA released a steady d.c. potential, produced by the divider network R192–R193 across the −250V supply, is fed to the grid of V24, thus cutting off the valve and producing zero voltage output at socket SKQ. The FAULT lamp LP1 is illuminated

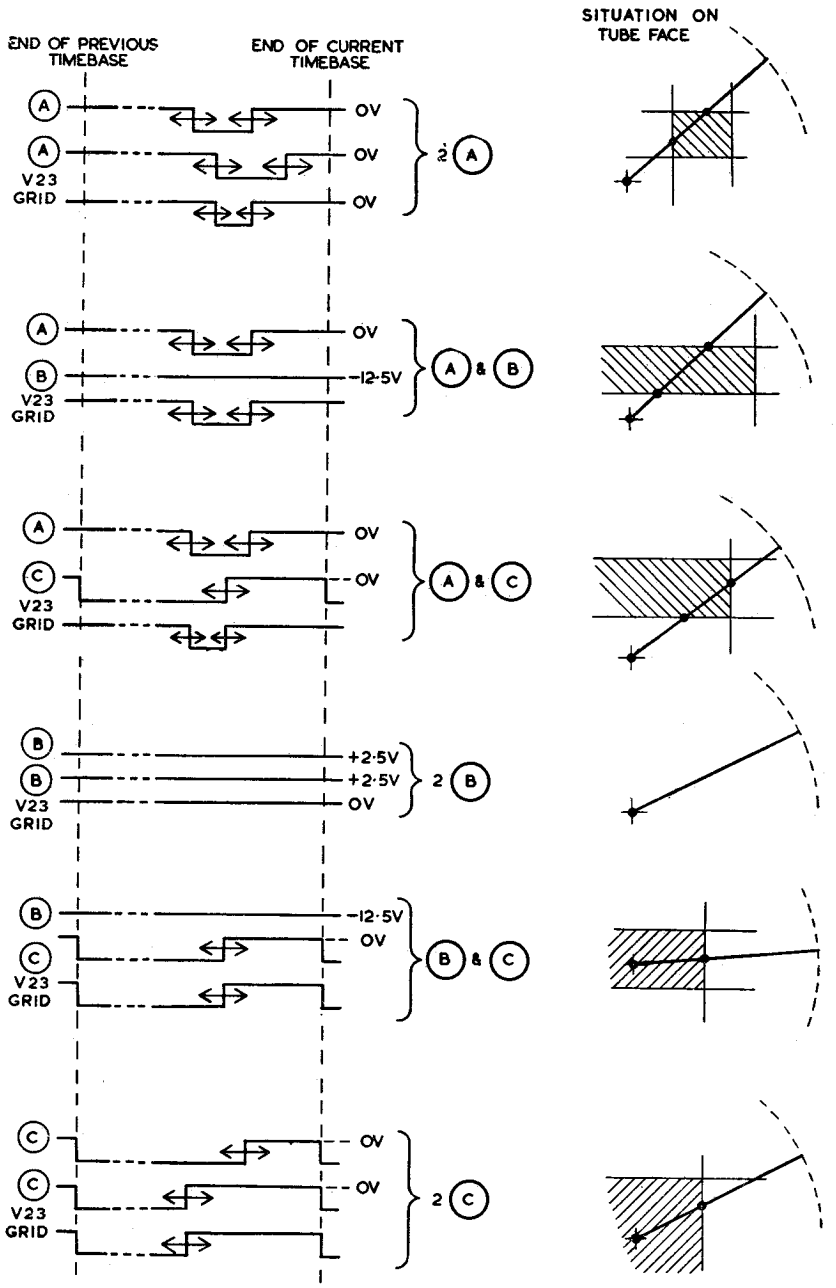


Fig. 6. Final waveform production

when SWE is operated to the OFF position, thereby serving as a visual warning to guard against SWE being left in this position.

SECRET

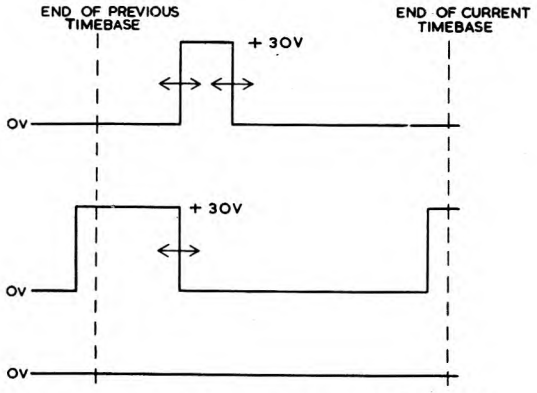


Fig. 7. Possible outputs at V24 cathode

25. The output from V24 is developed across the termination in the area switching panel; R190 provides a cathode load for V24 should the connection from SKQ be broken.

Multimeter readings

26. With the multimeter Type 100 connected to socket SKA via a plug-to-socket adaptor, and with SWA–SWD operated to their ADJUST positions and RV1–RV8 correctly adjusted, the readings obtained in multimeter switch positions A–D should be 0·4 ±0·05 under all d.c. input conditions. The valve stages checked at multimeter positions A–D are V3a, V8b, V14b and V19a respectively.

Monitoring points

27. Test sockets are provided for monitoring purposes at various points in the circuit. The waveforms existing at these points are illustrated in fig. 9.

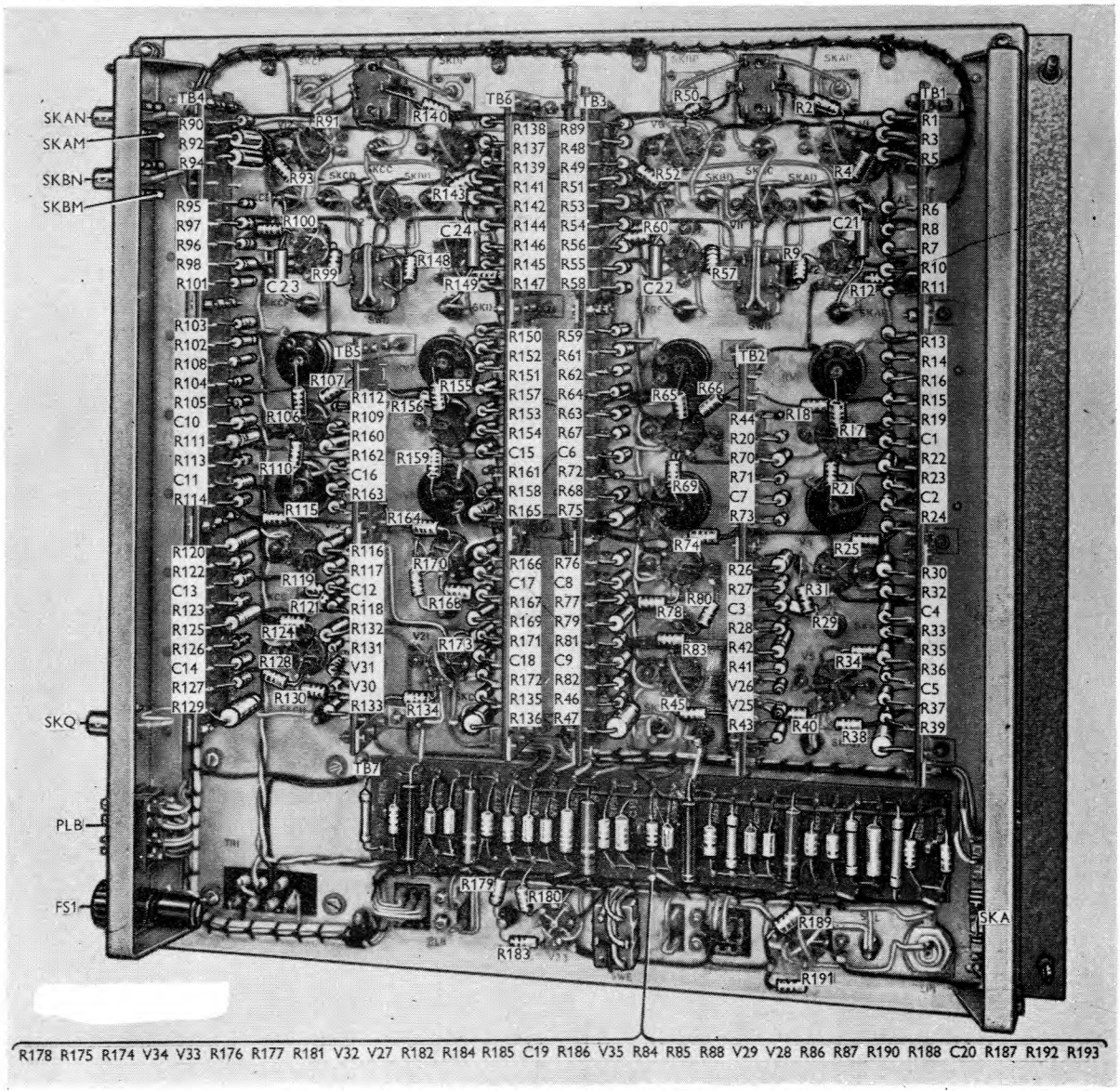


Fig. 8. Pulse generator (rectangle) M11: rear view

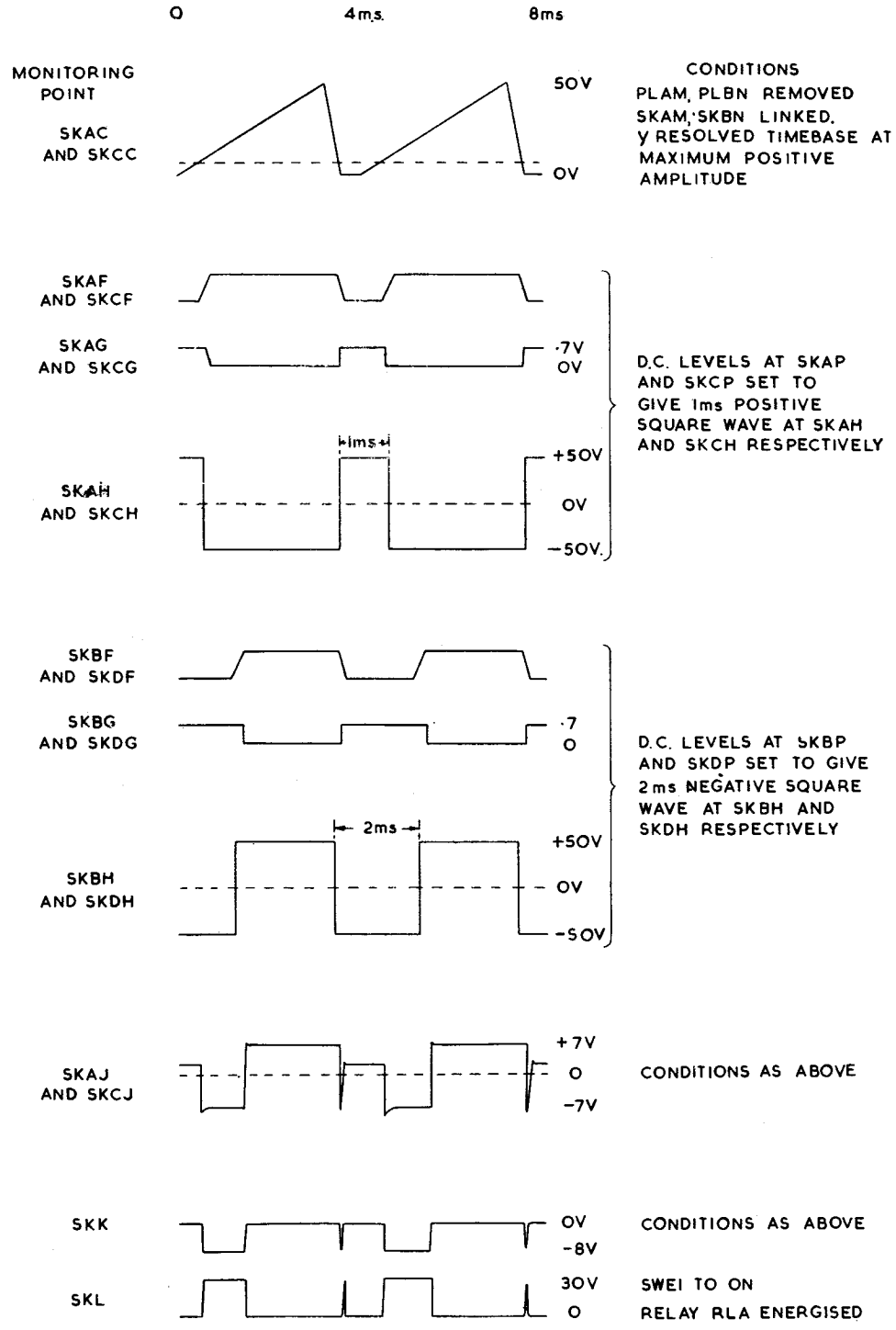


Fig. 9. Waveforms at monitoring points

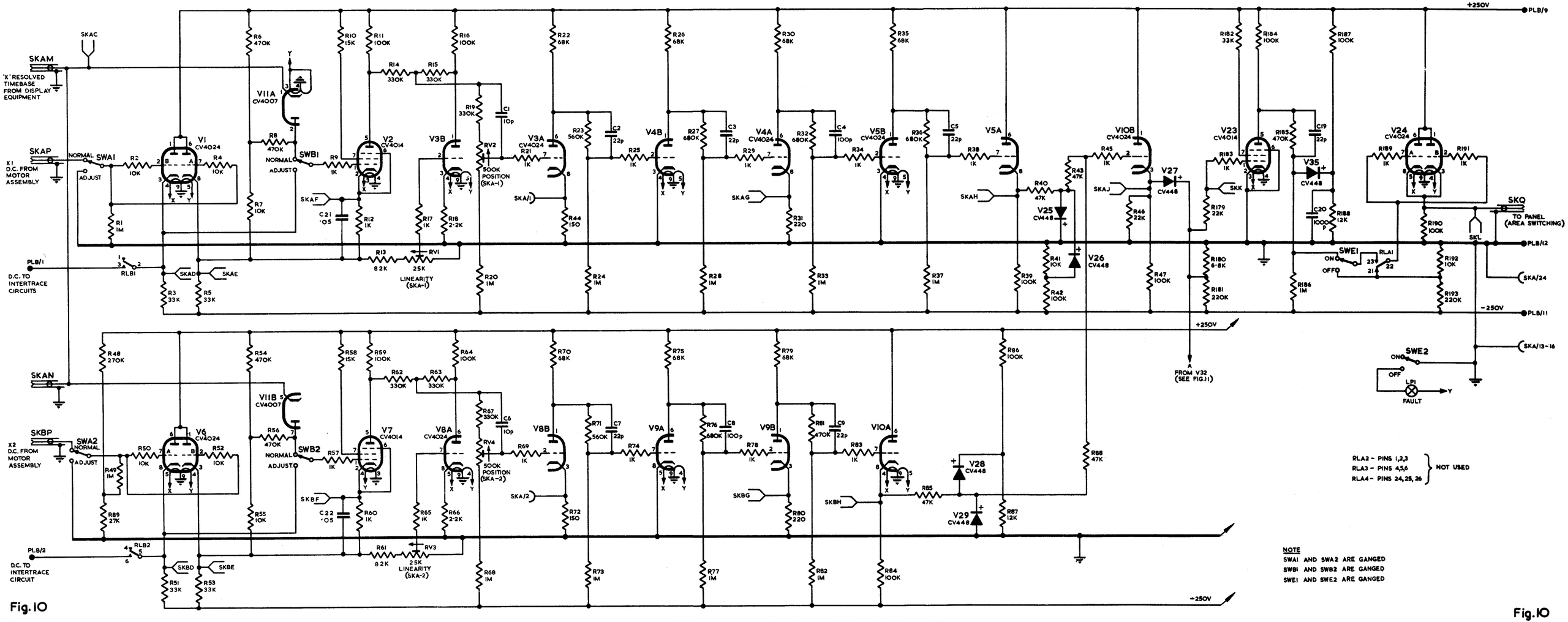
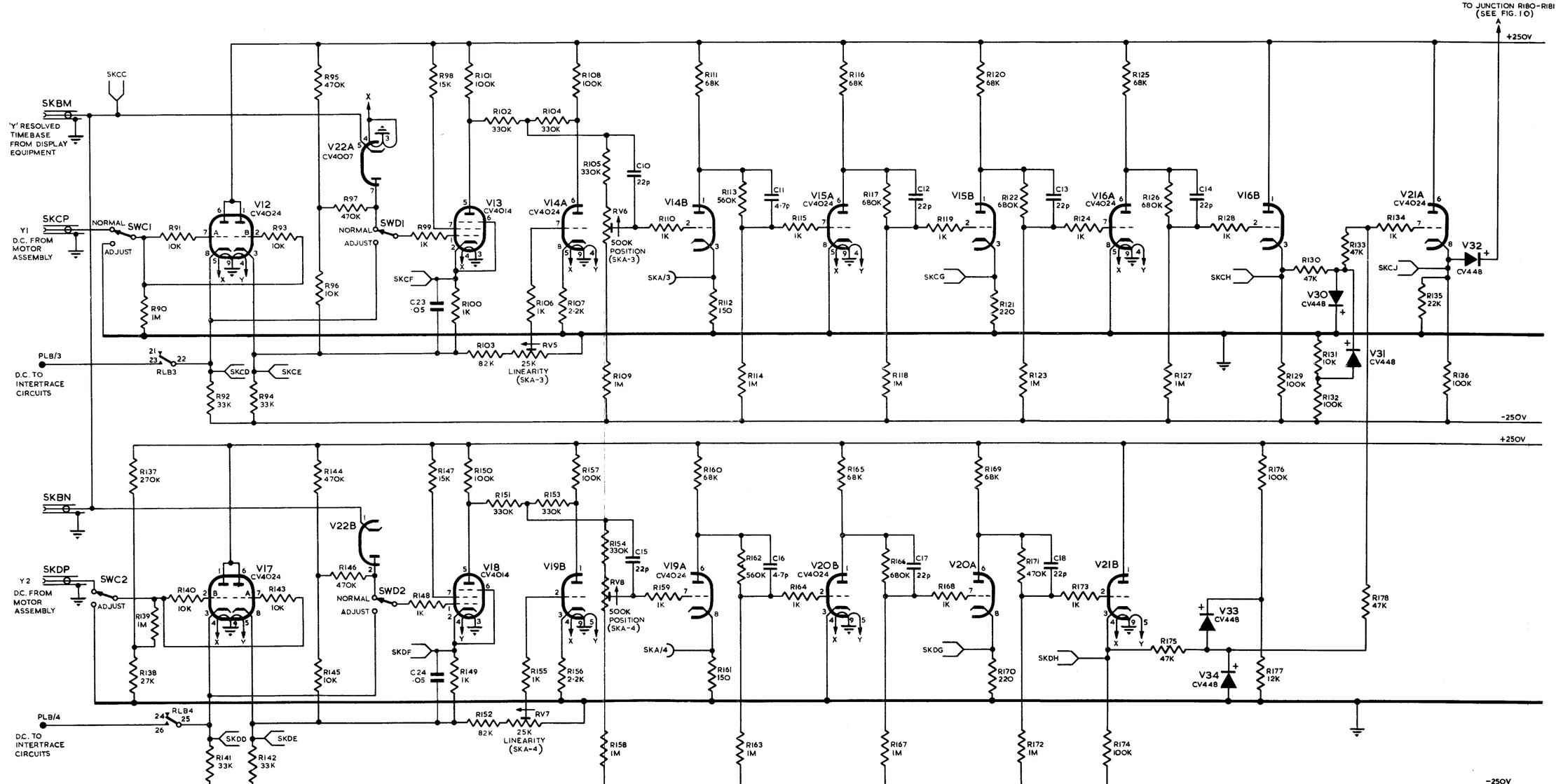
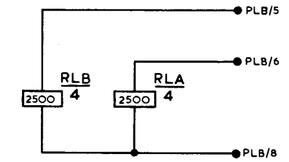


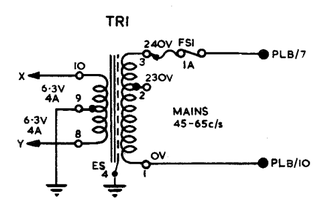
Fig.10

Pulse generator (rectangle) M11: circuit-part A

Fig.10







NOTE
SWC1 AND SWC2 ARE GANGED
SWD1 AND SWD2 ARE GANGED

Fig.11

Pulse generator (rectangle) M11: circuit-part B

Fig.11

Chapter 3

MOTOR ASSEMBLY M1

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

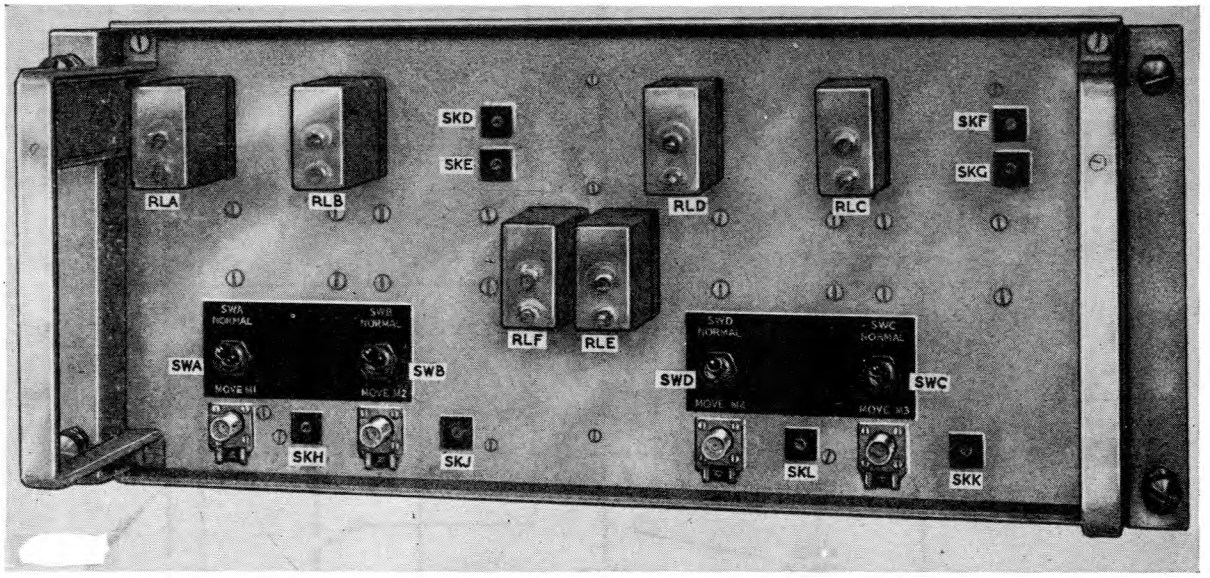


Fig. 1. Motor assembly M1 : front

Introduction

1. This assembly (*fig.* 1) is used to set the d.c. potential at which the resolved timebase for the p.p.i. displays on the radar operator's display console suite is gated so that the doppler compensation rectangle waveforms can be generated. The displayed rectangles can be set to any position or size on the display by the manually operated joystick which normally controls the motor assemblies. Three motor assemblies are used, one assembly for each rectangle. One assembly is located in frame 1 of the doppler cabinet, the other two are in frame 2.

2. Each assembly has four miniature two-phase motors which have built-in reduction gearboxes, the output shaft of each gearbox drives a cam and a potentiometer. The potentiometers set the d.c. gating potentials. The motors are reversible, and supplied with two 500c/s inputs. One 500c/s supply can lead or lag the other by 90 degrees and is variable in amplitude, according to the position of the joystick (*Chap.* 4). This voltage is produced by the motor controller (*Chap.* 4) to provide the necessary speed variation and direction of rotation of the motors when compared with the fixed reference 500c/s (nominal) generated by the reference signal generator M2 (*Sect.* 3, *Chap.* 11).

3. Two motors on each assembly are associated with the X axis and two with the Y axis. One motor in each axis controls the position potentiometer and the other controls the size potentiometer.

System description

4. A simplified block diagram of the motor assembly and its control system is shown in fig. 2. The control circuit for only one axis, the X, has been shown but this description is equally true of the Y axis. In the complete system the joystick also produces d.c. control voltages for the Y axis, i.e. a total of four 500c/s inputs to the X and Y move and size motors.

5. The 500c/s sine wave generated by the reference signal generator is fed to the motor controller where it is amplified to produce four outputs. Two of these outputs are of fixed amplitude and phase, and fed to the motor assemblies via relay contacts in the electronic joystick switch (*Chap.* 5) so that, with the joystick operated to produce a d.c. control voltage in excess of 6V in either direction for X or Y axes, and with the button at the top of the joystick or any RESET switch operated, the fixed 500c/s supply is available for the motor assemblies. The amplitude and phase of the variable 500c/s outputs from the motor controller are controlled by the d.c. from the joystick, and these two outputs are fed directly to the motor assemblies, provided all RESET switches are unoperated. If any reset switch is operated, all four 500c/s inputs to the motor assemblies are of fixed phase and amplitude.

6. With all four 500c/s supplies available to each motor assembly, selection of the rectangle to be adjusted must be made by one of the MOVE/SIZE or RESET keys on the radar operator's control desk ; these keys are interconnected so that the position or size of only one rectangle can be controlled by the joystick at a time and then only if all RESET keys are unoperated. The 500c/s supplies are fed to the pairs of move or size motors on a particular motor assembly via the contacts of a pair of move or size relays which, when closed, route the 500c/s supplies to the windings of the selected motors. The motors will then rotate in a direction and at a velocity determined by the joystick position.

7. As the motor turns it drives, through a reduction gearbox, the wiper arm of a potentiometer. It will continue to drive the potentiometer until the button on the top of the joystick is released ; there is no feedback path to cancel the demand.

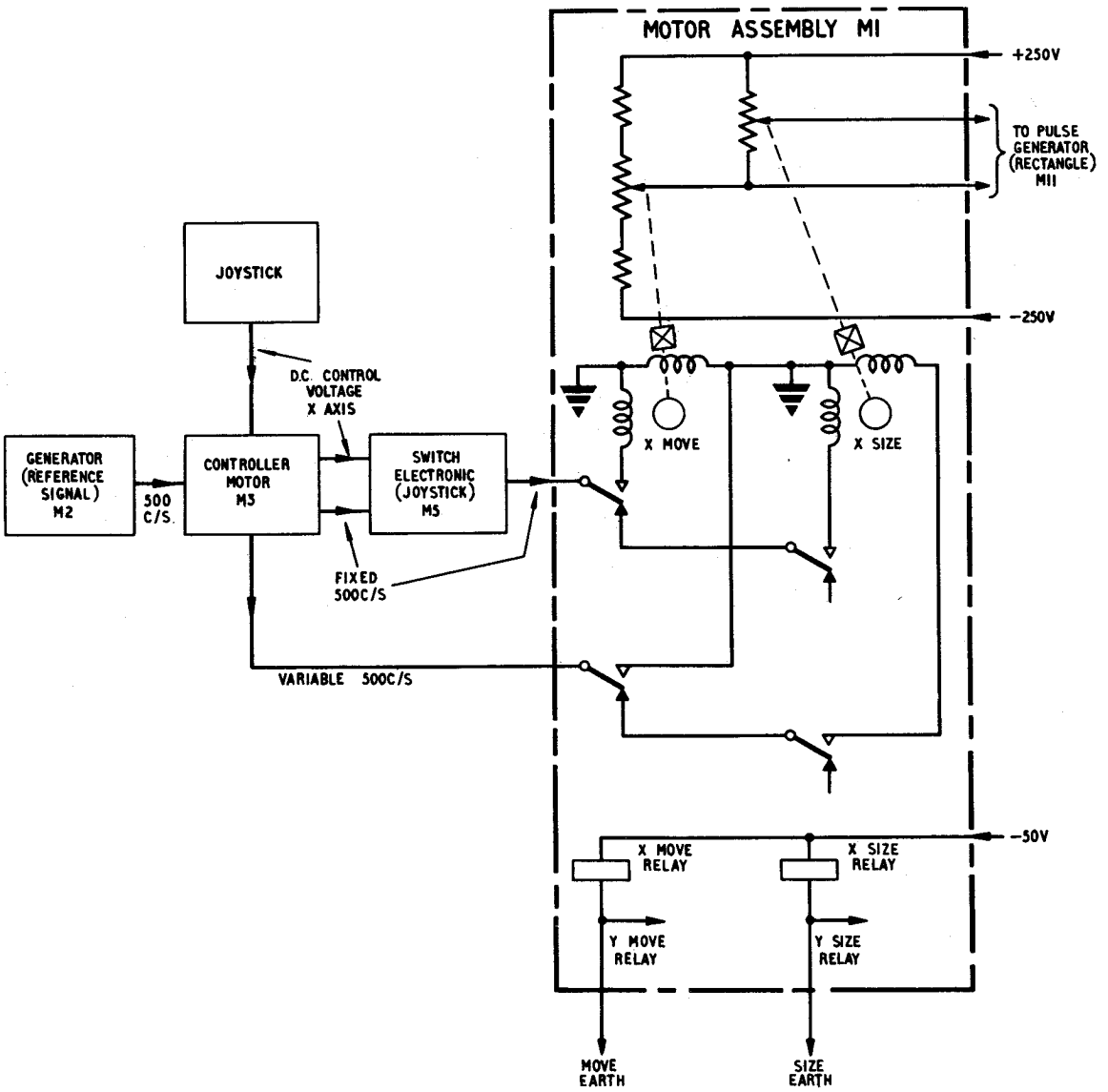


Fig. 2. Motor control circuit : block diagram

8. The move potentiometer is in a resistance chain connected between +250V and −250V supplies in the unit. The size potentiometer is also in a resistance chain, the potential across this chain being the difference between the +250V and the potential of the wiper arm of the move potentiometer.

9. The potentials of the two slider arms are fed into separate clipping stages in the rectangle generator (*Chap.* 2) where they are used to determine the level at which the resolved X (or Y) timebase level is clipped. The potential of the size potentiometer wiper arm is always positive with respect to the move potentiometer wiper arm.

10. Circuits (not shown in *fig.* 2) in the assembly enable the motors to be electrically damped, and controlled manually during servicing. Rectangle movement, under the control of a local joystick and a REMOTE/LOCAL switch in the motor controller, enable the trigger circuits in the electronic joystick unit to be set up. Selection of the motor to be used is made by MOVE/NORMAL switches on the motor assembly. The RESET switches on the radar operator's console allow rectangles to be reset by means of cam-operated microswitches on the motor assembly, to predetermined positions and sizes independently of the position of the joystick.

Performance characteristics

Inputs

11. (1) Fixed 500c/s supply at an amplitude of 50V peak-to-peak at PLB/1 and PLB/4.
(2) Variable 500c/s supply, variable in amplitude up to 48V peak-to-peak, and lagging or leading 90 deg. (±22.5 deg.) with respect to the fixed supply in (1) at PLB/3 and PLB/6.
(3) −50V d.c. This is used as a damping and braking voltage and is applied to the motors when they are being operated in both the normal and the reset condition.
(4) +250V d.c. from the +250V regulator in the top of frame 1.
(5) −250V d.c. from the −250V regulator in the power cabinet.
(6) −50V d.c. supply at PLB/8 from the bulk power supply.

Outputs

12. (1) Two d.c. (move) voltages at SKM (X axis) and SKP (Y axis) not exceeding ±60V.
(2) Two d.c. (size) voltages at SKN (X axis) and SKQ (Y axis) not exceeding +55V when output (1) is at a maximum.

Circuit description

13. Motors M1 and M3 (*fig.* 5) are concerned with the movement of the displayed rectangle, whilst motors M2 and M4 control the size of the rectangle.

14. A key switch on the radar operator's control desk selects whether the move or size motors shall turn. When this key is set to MOVE an earth is connected to SKC/6. Provided the MOVE/NORMAL switches (SWA and SWC) are set to NORMAL, relays RLA and RLC will be energized and contacts RLA1 and RLA2 will connect the X fixed and X variable 500c/s supply to the move motor M1. Contacts RLC1 and RLC2 will similarly connect the 500c/s supply to move motor M3 and contacts RLA3 and RLC3 connect the −50V d.c. damping supply from SKC/2 and SKC/5 to the fixed voltage winding of motors M1 and M3 respectively. These motors will rotate in a direction depending upon the phase difference between the fixed and variable supplies and drive the potentiometers' sliders of RV1 and RV3 causing their d.c. outputs to change. Since the sliders supply a d.c. to one end of the chain in which RV2 and RV4 are connected (the other end is at +250V) the outputs from the sliders will change proportionately. This will result in movement of the rectangle without a change in size.

15. If the MOVE/SIZE key, on the operator's control desk, is put in the SIZE position, an earth will be made to SKC/9, providing SWB and SWD are in NORMAL position, and energize the relay RLB and RLD. Contacts RLB1 and RLB2 will connect the X fixed and variable 500c/s supply to M2. Contacts RLD1 and RLD2 will similarly connect the Y 500c/s supply to size motor M4 and contacts RLB3 and RLD3 connect the −50V d.c. damping supply from SKC/2 and SKC/5 to the fixed voltage winding of motors M2 and M4 respectively. These motors drive the sliders of potentiometers RV2 and RV4. The d.c. output levels of RV2 and RV4 will depend primarily upon the relative position of the slider arms of the potentiometers, but the maximum d.c. level is set by the position of its associated move potentiometer.

16. The diodes V1 and V2 are used as catching diodes because the potentiometer sliders of RV1 and RV3 are capable of being rotated continuously. There will, therefore, be a point at which the slider is between the two ends of the potentiometer resistance winding, when the slider is effectively open-circuited. Since the size potentiometer chains derive their potential from the sliders of RV1 and RV2, the size potentiometer outputs would approach +250V, and overload the input stage of the respective pulse generator M11. The diodes V1 and V2 overcome this condition by conducting when the slider is open-circuited and maintain the lower ends of the chains R5, RV2 and R6, and R11, RV4 and R12 at potential of approximately +60V until the slider arms make contact with the resistance windings again.

17. The MOVE/NORMAL switches (SWA to SWD) are for servicing purposes, and are used in conjunction with a local control joystick on the motor controller. When any of the MOVE/NORMAL switches are set to MOVE, an earth is connected to the fault lamp on the motor controller, and the lamp lights. Local joystick control is also made to the motor associated with the switch so that the required servicing or checks can be made.

18. Any rectangle may be returned to a predetermined position and size by operating the appropriate RESET key on the radar operator's control desk. Operation of this key completes the earth to relays RLE and RLF in any position of the MOVE/NORMAL switches.

19. In the energized position the contacts of RLF connect the −50V d.c. damping supply at SKC/2, 5, 8 and 11 directly to the fixed voltage windings of motors M1, M3, M2 and M4 respectively. When RLE energizes,

motor control is removed from the MOVE/NORMAL switches and transferred to the microswitches. In this condition an earth from SKC/6 is made to RLA via SWE (when the cam follower is bearing on the normal cam diameter) and the relay contact RLE1 makes, causing RLA to energize.

20. When RLA energizes contact RLA1 changes over allowing a fixed 500c/s from the motor controller (available due to RESET switch being operated) to supply the fixed supply winding of motor M1. RLA2 changes over and the variable 500c/s supply from the motor controller is made to the other winding of the motor.

21. Motor M1 will rotate until the shoulder of the cam (*Para.* 23) changes over the microswitch contacts, interrupting the earth line to RLA, which de-energizes and its contacts disconnect the supplies to M1. Because the microswitch SWE is changed over, RLB (providing the cam follower has not operated SWF) is energized via RLE2 and SWF. The windings of M2 are therefore energized by the supplies formerly made to M1. M2 rotates until the cam interrupts the earth to RLB via SWF.

Motor drive assembly

22. The four, motor drive assemblies (*fig.* 3) in each unit are separately removable as complete sub-assemblies. Each sub-assembly is mounted on a U type bracket. The motor and gearbox forming an integral part, are mounted on the outside of one cheek, and the potentiometer the outside of the opposite cheek. Each sub-assembly is secured to the underside of the motor assembly chassis by nuts and bolts clamping the bottom of the U bracket. Electrical connections to each sub-assembly are by soldered connections to the motors and potentiometers from the main cableform.

23. The gearbox output shaft is offset from the centre of the motor due to the gear train, and is coupled by an Oldham coupling to the potentiometer spindle,

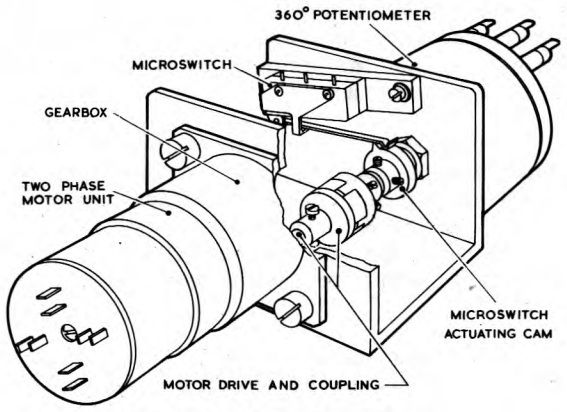


Fig.3 Motor drive assembly

upon which is mounted a cam. The two engaging faces of the coupling are sandwiched between a floating disc with recesses cut in it. The coupling has hollow bushes into which the motor and potentiometer drive shafts fit. The bushes are axially drilled and tapped and socket-headed screws are used to clamp the shafts and bushes together.

Cam setting

24. When the rectangle is in the selected position on the display and is of the desired size, the appropriate motor assembly M1 for that rectangle should be switched off. The socket-headed screws securing all four cams to the four potentiometer shafts should be slackened off, *care being taken not to move the position of the potentiometer shafts.* The cams should then be rotated until the cam followers are riding on the crest of the cam shoulders, and the microswitches are operated. The socket-headed screw of each cam should then be tightened ensuring that the cams remain at this setting.

25. To check that the setting is correct, operate the RESET key on the control desk and switch the motor assembly on. The motors in the assembly should not move, and the rectangle remain in its original position and size.

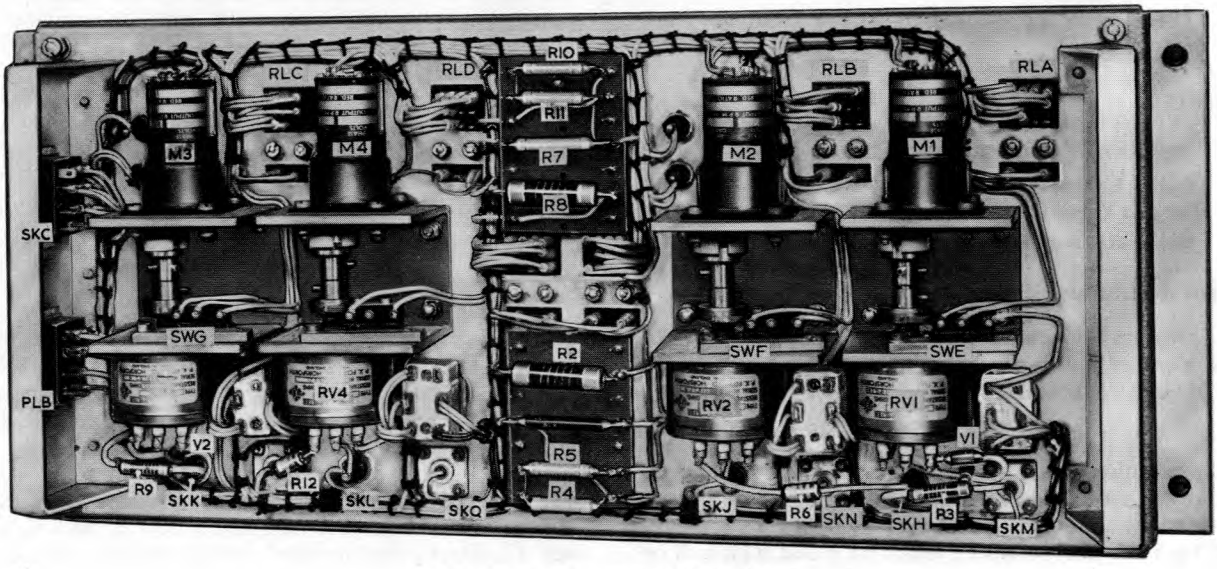


Fig. 4 Motor assembly M1: rear

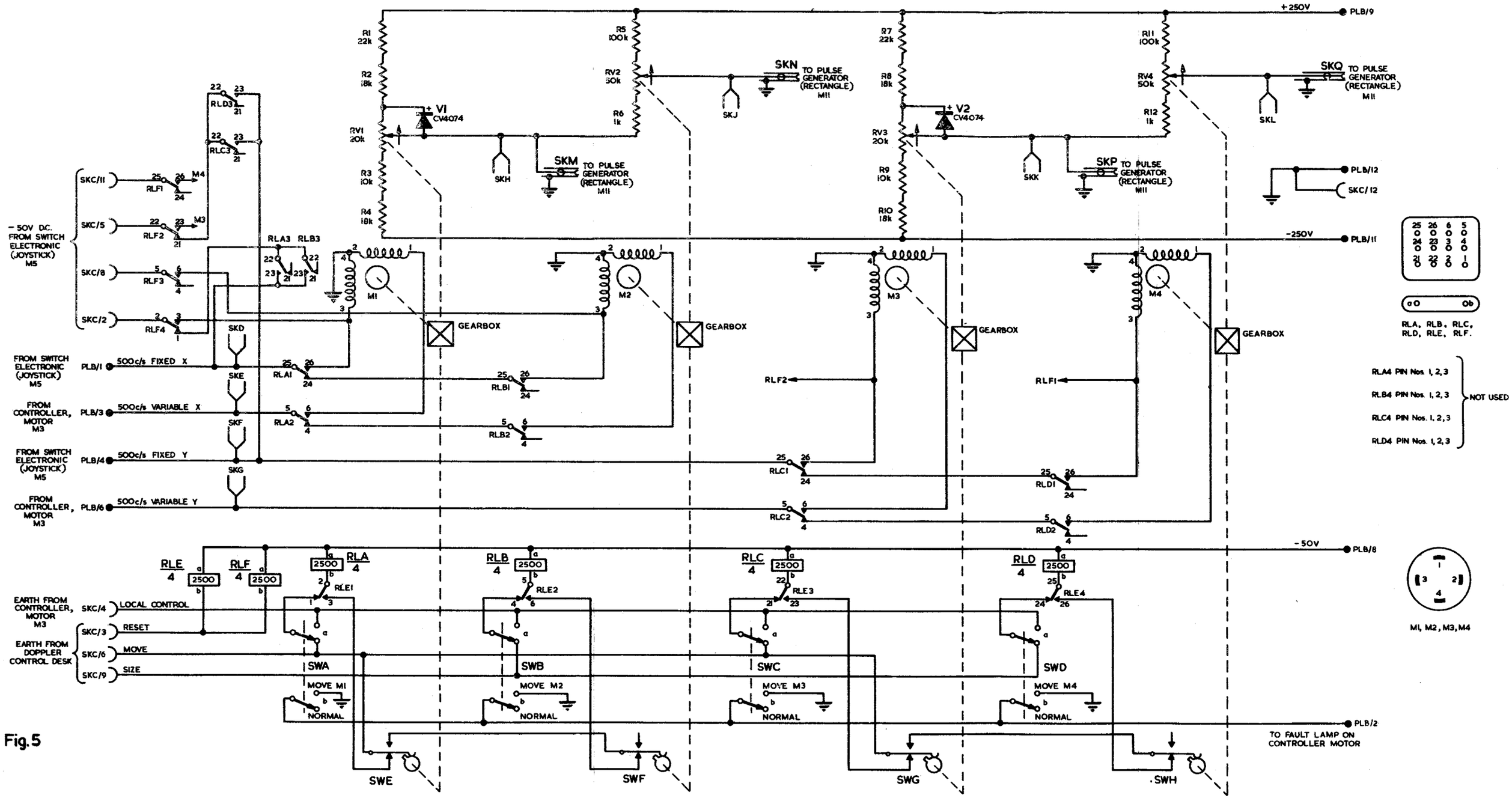


Fig.5

C.B.H. 3819 - Wt. 8895 - Dd. 7049 - 65 - 1/64

Motor assembly M1 : circuit

Fig 5

Chapter 4

CONTROLLER, MOTOR, M3

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

Introduction

1. The controller, motor, M3 (*fig.* 1 *and* 4) receives a 500 c/s input from the reference signal generator (*Sect.* 3, *Chap.* 11) and from it produces four 500 c/s outputs. These outputs drive the X and Y move and size motors (*Chap.* 3) associated with the adjustment of rectangle position and size.

2. Two outputs, of fixed amplitude and phase, are fed to the move and size motors via the electronic switch unit (*Chap.* 5) and two outputs, of variable amplitude and phase, are fed to the motors direct. The variable outputs are in quadrature with the fixed outputs.

3. The phase and amplitude of the variable outputs, and consequently the position and size of the displayed rectangles, are controlled by one or other of the following :—

(1) Variable d.c. voltages derived from a joystick control and associated MOVE/SIZE keys on the control desk (*remote control*).

(2) Fixed d.c. voltages switched by operation of a RESET key on the control desk. The selected rectangle moves to a predetermined position and size (*remote control*).

(3) Variable d.c. voltages derived from a LOCAL JOYSTICK potentiometer mounted on the unit in

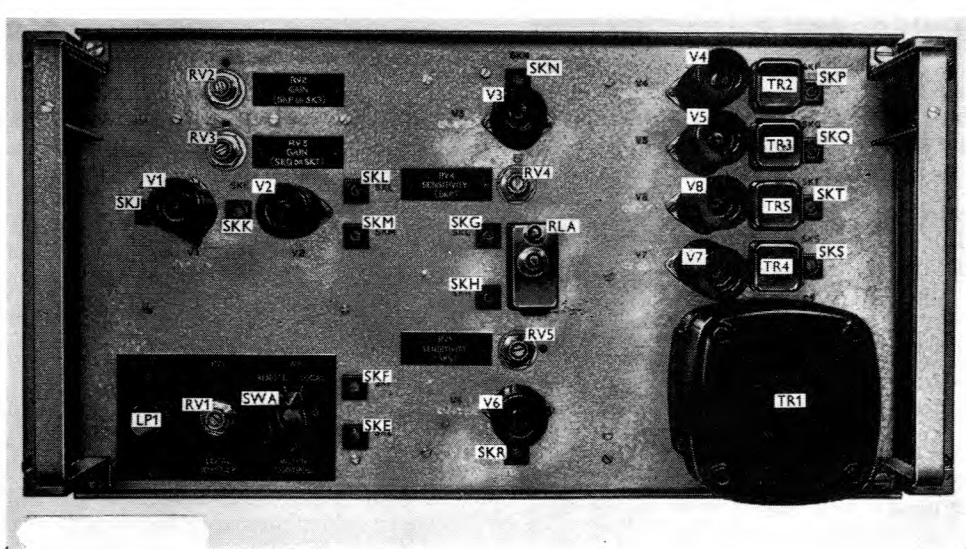


Fig. 1. Controller, motor, M3 : front view

conjunction with MOVE/NORMAL switches located on the move and size motor assemblies (*local control*).

4. A switch on the unit selects either LOCAL or REMOTE control. When set to LOCAL, the unit fault lamp is lit, as is the doppler cabinet fault lamp. The unit fault lamp is also lit if any of the MOVE/NORMAL switches on the motor assemblies are set to MOVE.

5. The unit is fitted in frame 1 of the doppler cabinet.

Performance characteristics

Inputs

6. The unit accepts the following inputs :—

(1) The X axis d.c. control voltage, of up to 50V positive or negative according to the setting of the joystick, is received at PLB/2.

(2) The Y axis d.c. control voltage, of up to 50V positive or negative according to the setting of the joystick, is received at PLB/5.

(3) The main 500 c/s input from the reference signal generator at a level of not less than 1V, is received at PLB/6.

Outputs

7. The unit provides the following outputs :—

(1) The X fixed 500 c/s output to the electronic joystick switch at SKC/1 is at a level of 50V peak-to-peak and is in phase with the input at PLB/6.

(2) The Y fixed 500 c/s output at SKC/4 is the same as that at SKC/1 and is also fed to the electronic joystick switch.

(3) The X variable 500 c/s output at SKC/3 is at a level not greater than 48V peak-to-peak and at a phase of $+90°$ or $-90° \pm 22\frac{1}{2}°$ with respect to the input at PLB/6. This output feeds three motor assemblies.

(4) The Y variable 500 c/s output at SKC/6 is similar to that at SKC/3 and also feeds three motor assemblies.

(5) A control d.c. voltage for the X axis trigger circuits is fed to the electronic joystick switch from SKC/2. This voltage lies between the limits of 50V positive or negative.

(6) A control d.c. voltage for the Y axis trigger circuits is fed to the electronic joystick switch from SKC/5. This voltage lies between the same limits as that from SKC/2.

Control functions

8. With the REMOTE/LOCAL switch on the unit in the LOCAL position the following connections are made :—

(1) The remote earth on PLB/3 is disconnected from the MOVE/SIZE and RESET switches on the control desk.

(2) SKC/7 provides an earth for the MOVE/NORMAL switches in the motor assemblies.

(3) PLD/3 provides an earth for relay RLE in the electronic joystick switch unit.

(4) PLD/2 connects an earth to the fault relay for frame 1.

9. When a rectangle is being moved to a preset position under the control of a RESET switch the following circuits are completed :

(1) An earth is received at SKC/10 from the operated RESET switch to operate relay RLA.

(2) An earth is connected to the intertrace equipment from PLD/1 by contacts of relay RLA.

10. Operation of any MOVE/NORMAL switch in a motor assembly to MOVE causes an earth to be fed in at SKC/9 to light the unit FAULT lamp.

Brief system description

11. Movement of display rectangles and changes to their size are effected by motor-driven potentiometers in the motor assemblies. The direction and speed of rotation of the move and size motors is determined by the motor controller under the control of d.c. voltages produced either remotely by the joystick control on the centre control desk panel (*Sect.* 8) or locally in the motor controller.

12. The motor control system is shown in simplified form in fig. 2. The basic supply for the rectangle control system is the 500 c/s input to the motor controller from the reference signal generator. This supply is amplified in the controller to provide fixed and variable 500 c/s inputs for the X and Y move and size motors.

13. The variable 500 c/s supply is phase modulated by a d.c. control voltage so that it either lags or leads the fixed supply by 90° (according to the polarity of the control voltage) and is modulated in amplitude according to the control voltage level. The variable supply is connected directly to the move and size motors whereas the fixed supply is switched by relays in the electronic joystick switch unit : the relays are controlled by Schmidt trigger circuits which are themselves under the control of the d.c. voltages used for phase modulation.

14. Under normal operating conditions, the LOCAL/REMOTE switch is in the REMOTE position and, with no control switches operated, all relays are released. The 500 c/s inputs are disconnected from the motors and the rectangles on the display remain in the positions set by the last operation of the controls. The system is therefore ready for remote adjustment of the rectangles by means of the joystick control or of the RESET switches.

15. Manual control of the rectangles is obtained by first selecting the rectangle for adjustment. The appropriate MOVE/SIZE switch is operated, the joystick moved and the button on the top of the joystick is depressed. D.C. voltages taken from the joystick control the phase modulators and are also connected to Schmidt trigger circuits by relay contacts in the electronic switch, the relay on the electronic joystick switch unit being energized via the joystick

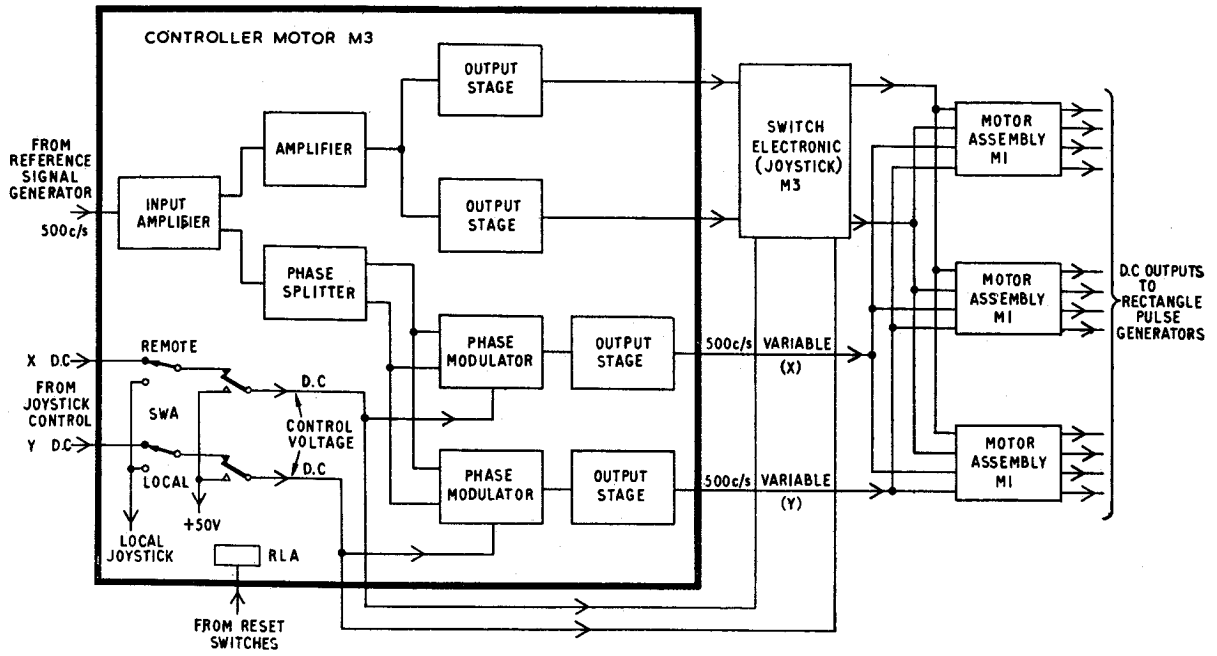


Fig. 2. Motor control system

push-button switch. Fixed and variable 500 c/s supplies are thus made available to all three move and size motor assemblies but the selected relays, MOVE or SIZE, are operated only on the motor assembly for the rectangle to be adjusted.

16. The position of the rectangle is indicated by dot corner markers on the display, the intertrace circuits having been made operative by the MOVE/SIZE switch. D.C. outputs from the motor-driven potentiometers are used to gate resolved timebase waveforms in the rectangle pulse generator (*Chap.* 2) to produce rectangular switching waveforms. When the rectangle is in the required position the joystick button is released and the joystick is returned to the central position. The motors, and hence the rectangles, cease to move.

17. Alternatively, rectangles may be set to a predetermined position and size by means of RESET switches on the control desk. Circuit action is similar to that described in the previous paragraph except that the phase and amplitude of the variable 500 c/s outputs from the controller are determined by the fixed d.c. potential derived from a potential divider network in the unit. The rectangle to be adjusted is selected by the RESET switch. The circuit conditions required for rectangle re-setting are made by relays operated by the RESET switch. The latter switch also energizes the relay connecting the d.c. inputs to the Schmidt trigger circuits and operates the intertrace circuits.

18. The selected rectangle is moved to a position determined by cam-operated microswitches in the motor assembly, the 500 c/s supplies being removed from the motor when the preset position is reached. The action is sequential, the rectangles being first moved and then adjusted to the required size.

19. Local control of rectangles is obtained by setting the REMOTE/LOCAL switch on the controller to LOCAL. The phase and amplitude of the variable 500 c/s output from the controller is then determined by the LOCAL JOYSTICK potentiometer. The relay controlling the d.c. inputs to the Schmidt trigger circuits is operated by the switch. Each of the motors on the motor assemblies may be moved individually by operation of one of the MOVE/NORMAL switches to the MOVE position. This facility is used when setting-up the Schmidt trigger circuits in the electronic joystick switch unit.

Circuit description (*fig.* 6)

20. The 6·3V a.c. heater supply for V1 to V8 is obtained from transformer TR1 which is supplied with 50 c/s mains from PLB/7, via FS1, and PLB/10. The other power supplies are +250V, applied at PLB/9 and PLB/12 (earth) and −250V, at PLB/11 and PLB/12 (earth). The −50V supply for relay RLA is applied at PLB/8. All these supplies are received from, or via, the +250V regulator unit at the top of frame 1 of the cabinet. Additional inputs of +50V and −50V are received at PLB/4 and PLB/1 respectively from a separate power unit at the bottom of frame 1 : this power unit also provides the supplies for the joystick on the control desk.

Input amplifier

21. The 500 c/s input is received at PLB/6 and applied, via C1 and R7, to the grid of the triode amplifier stage V1b. Two outputs are taken from the anode of V1b via the sliders of potentiometers RV2 and RV3 which are designated GAIN (SKP OR SKS) and GAIN (SKQ OR SKT) respectively.

22. The output from the slider of RV2 is at a lower level than that from the slider of RV3 and is used in the production of the variable 500 c/s outputs at SKC/3 and SKC/6. The output from the slider of RV3 is used in the production of the fixed 500 c/s outputs at SKC/1 and SKC/4. RV2 is set so that with RLA operated the outputs at SKC/3 and SKC/6 are at a level of +45V peak-to-peak as monitored at SKP and SKS. RV3 is set so that the outputs at SKC/1 and SKC/4, as monitored at SKQ and SKT, are at a level of 50V peak-to-peak.

Fixed 500 c/s amplifiers

23. The output from the slider of RV3 is further amplified by the triode stage V1a before application to the grids of the tuned driver stages V5 and V8. The two pentodes with their associated circuits produce outputs at the secondaries of TR3, for the X axis motors, and of TR5 for the Y axis motors. The primaries of the transformers are flatly tuned by C13 and C21 respectively.

Variable 500 c/s amplifiers

24. The output from the slider of RV2 is coupled via the components C2, R14 and C4, R15 to the grid of V2b in the phase-splitting stage V2. These components form phase-shift networks which, together with the couplings between the antiphase outputs of V2 anodes and the balanced modulator stages, provide a phase shift of approximately 90° with respect to the fixed 500 c/s outputs.

Balanced modulators and output stages

25. The two balanced modulator stages, V3 and V6, are identical and therefore only the action of V3 will be described here. The inputs to the two grids of V3 are equal in amplitude but opposite in phase. If the d.c. control input to V3b, via R24, is equal to that to V3a, i.e. earth potential, the output from V3 anode is theoretically zero. In practice, however, the output under these conditions is a 1 kc/s signal at low level. If the d.c. control level at V3b grid is changed in a positive or negative direction (*para.* 28) there will also be a 500 c/s output from the anode, the phase of the output relative to the fixed 500 c/s output being dependent on the polarity of V3b grid.

26. The output from V3 anode is applied to the grid of the tuned driver stage formed by V4 and its associated circuit. The tuning of TR2 by C12 is very wide-band and does not eliminate the 1 kc/s component from the output. This 1 kc/s output will not drive the motors in the motor assembly.

27. The SENSITIVITY (SKP) control RV4 is set so that maximum output amplitude at SKP is obtained only when the control voltage is at a maximum. Any reduction of control voltage will thus result in an immediate decrease of output amplitude. The SENSITIVITY (SKS) control RV5 is similarly set for the output at SKS.

REMOTE/LOCAL and RESET switching

28. A simplified schematic of REMOTE/LOCAL and RESET switching circuits is given in fig. 3. REMOTE/LOCAL switching is controlled by SWA and RESET switching by RLA. In the REMOTE position of SWA, with the reset relay RLA released, the two balanced modulators are controlled by the d.c. potentials received at PLB/2 and PLB/5 from two 50K potentiometers. These potentiometers are located in the joystick on the control desk and are connected across the +50V and −50V supplies received at PLB/4 and PLB/1. Further contacts of SWA extend a remote earth to the MOVE/SIZE and RESET switches on the control desk via PLB/3 so that control of rectangles is vested in the control desk on the console.

29. If any RESET switch on the control desk is operated RLA will be energized. Contacts RLA1 and RLA2 change over, so that the balanced modulators V3 and V6 are controlled by a fixed −50V potential with respect to earth produced by the potential divider network R5, R6, R66, R67 across the +250V and −250V supplies. Contacts

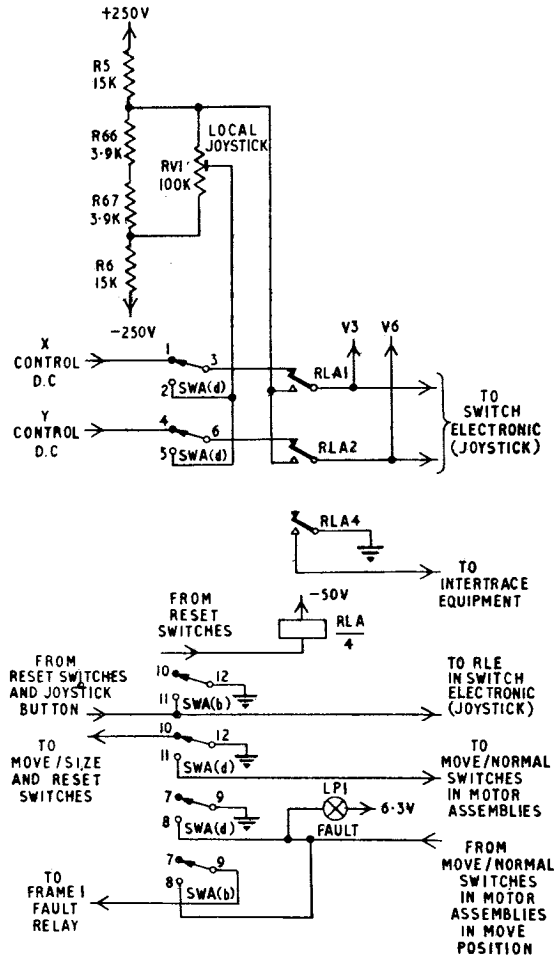


Fig. 3. REMOTE/LOCAL and RESET switching

RLA4 change over to extend an earth to the inter-trace equipment so that dot corner markers are produced on the monitor display.

30. For setting-up purposes SWA is set to the LOCAL position so that the balanced modulators are controlled by the d.c. potential produced by the LOCAL JOYSTICK potentiometer RV1, connected in the potential divider network R5, R6, R66, R67. This control potential for the balanced modulators may be continuously varied between +50V and −50V with respect to earth. Under these circumstances the potential at the slider of RV1 controls both modulators.

31. In this condition, the rectangles can only be controlled by operation of local controls on the unit and on the motor assemblies. An earth is therefore extended via PLD/3 to the electronic joystick switch and the unit and the cabinet FAULT lamps are lit. A control earth is extended via SKC/7 to the MOVE/NORMAL switches in the motor assemblies, this earth being removed from PLB/3 so that the MOVE/SIZE and RESET switches are inoperative.

The X and Y axis control d.c. potentials are fed out of the unit for use in the electronic switch unit, so that the control d.c. for the balanced modulators is also fed to the Schmidt trigger circuits associated with the fixed 500 c/s supplies for the same motors.

32. Resistors R1 to R4 are interconnected between the X and Y joystick inputs and the +50V and −50V supplies at PLB/4 and PLB/1. These resistors, in conjunction with the 50K potentiometers in the joystick control, produce a control d.c. characteristic which is non-linear. The characteristic is such that fine control of voltage is given for small movements of the joystick from the centre position, with a more coarse control when the joystick is moved towards the extreme position.

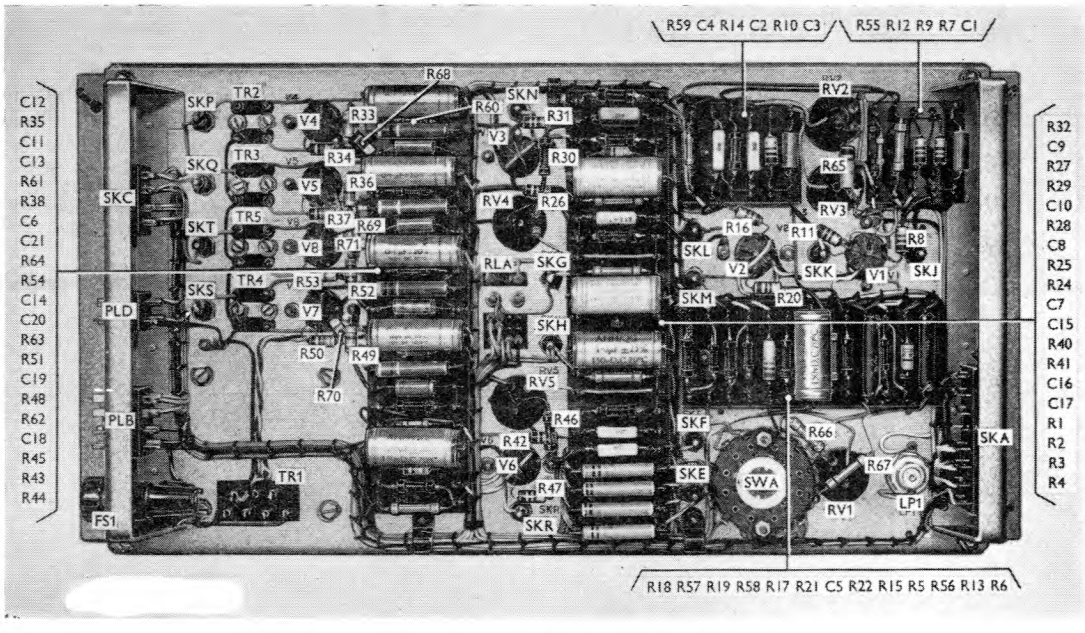


Fig. 4. Controller, motor, M3 : rear view

Monitor points

33. Monitor points SKE and SKF provide a means of checking the +50V and −50V joystick supplies. SKG and SKH are used to check the control d.c. potentials for the balanced modulators. All these test points are normally checked with a multimeter Type 1 or equivalent instrument.

34. Monitor points SKJ to SKT may be checked using a suitable oscilloscope. The idealized monitor point waveforms in fig. 5 are those which should be obtained with SWA set to local, the LOCAL JOYSTICK RV1 turned fully anti-clockwise and with RV2 to RV5 correctly adjusted.

Test readings

35. With the multimeter Type 100 connected to SKA via the plug-to-socket adaptor and with RV1 set to its mid-position the readings obtained should be as indicated in Table 1.

TABLE 1

Multimeter readings

Multimeter switch position	Stage monitored	Measured across resistor	Reading	Tolerance
A	V1b	R55	0·6	±0·12
B	V1a	R56	0·5	±0·1
C	V2b	R57	0·4	±0·08
D	V2a	R58	0·4	±0·08
E	V3	R59	0·53	±0·1
F	V4	R60	0·5	±0·1
G	V5	R61	0·5	±0·1
H	V6	R62	0·53	±0·1
J	V7	R63	0·5	±0·1
K	V8	R64	0·5	±0·1

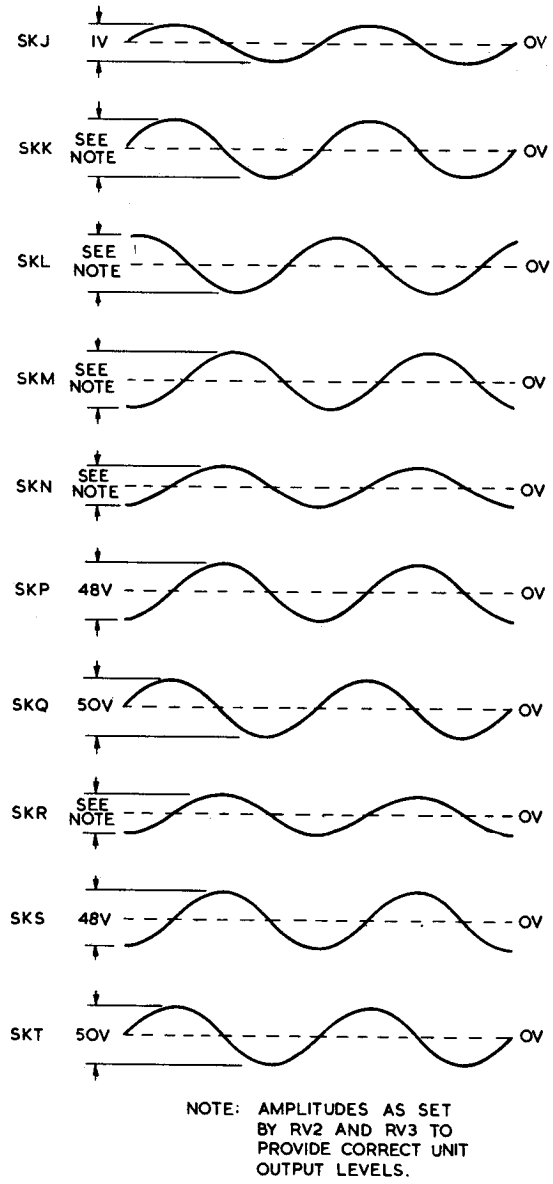


Fig. 5. Monitor point idealized waveforms

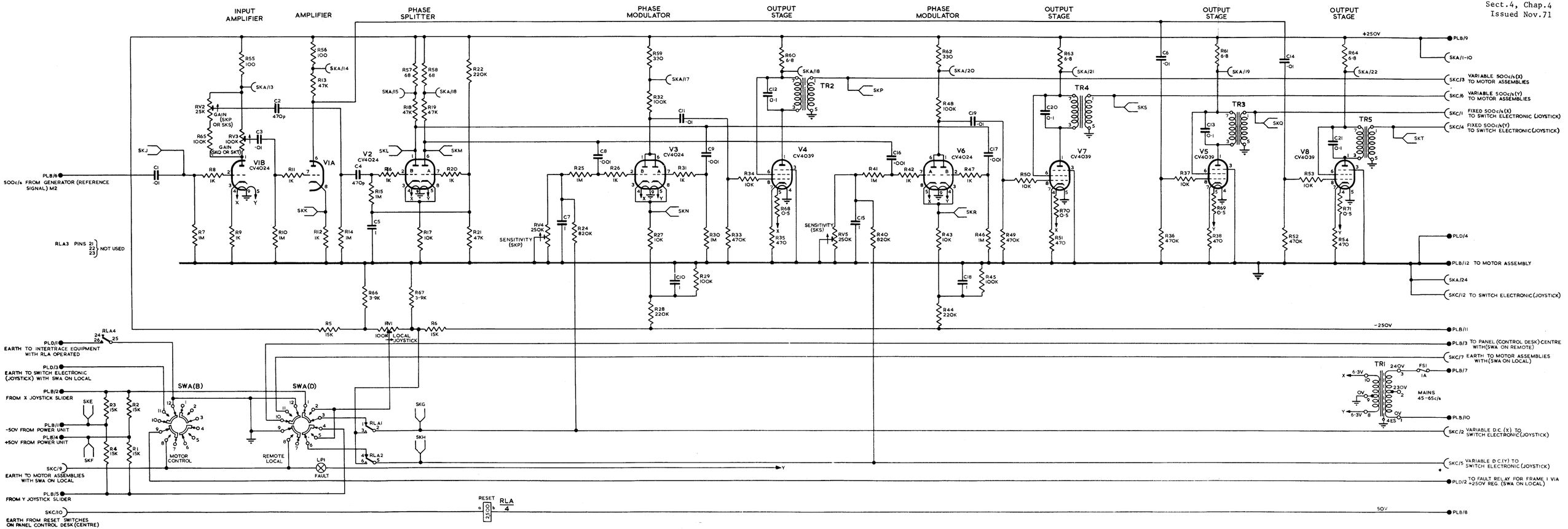


Fig.6 Wt.9110. R.C.1646

Controller, motor, M3: circuit

Fig.6

Chapter 5

SWITCH ELECTRONIC (JOYSTICK) M5

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

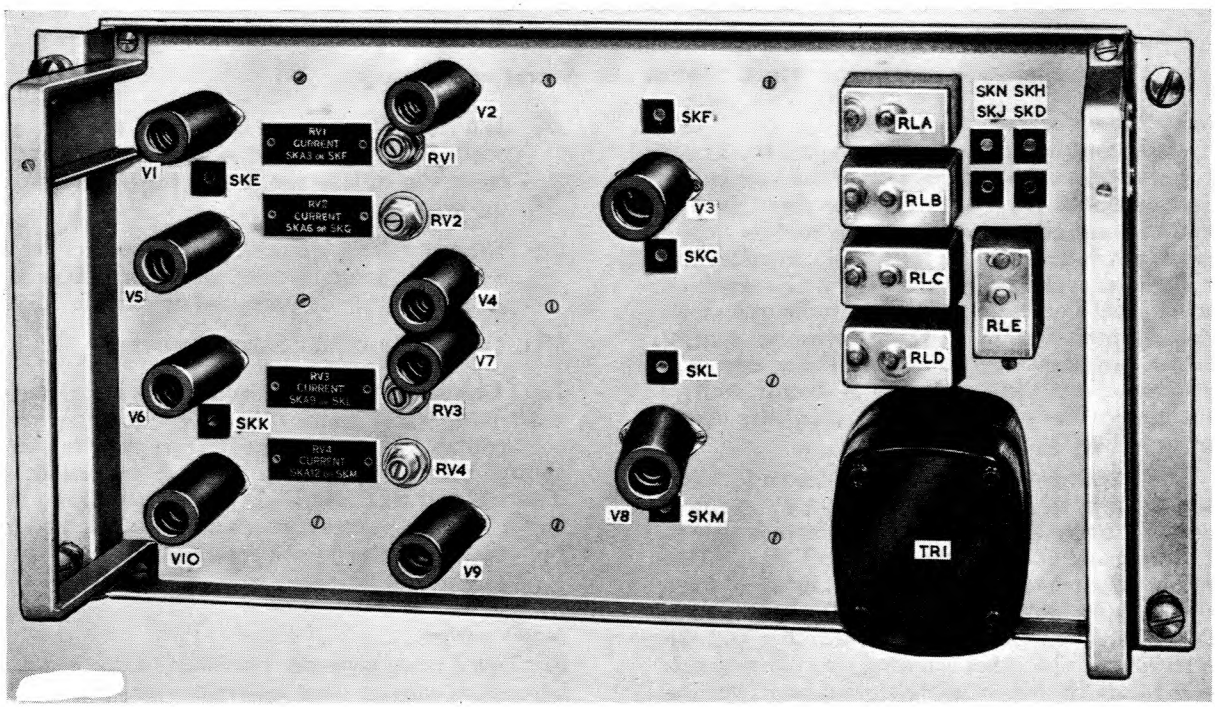


Fig. 1. Switch electronic (joystick) M5 : front

Introduction

1. The purpose of this unit (*fig.* 1) is to create dead zones in the manually operated joystick which is used to position, and determine the size of, three rectangles displayed on the radar operator's console suite, depending upon the position of the MOVE/SIZE key (*Chap.* 3). The dead zones are along the X and Y axis of joystick movement. The switch electronic joystick withholds the fixed 500c/s supply to the motor assemblies until the joystick movement produces a control voltage which is in excess of ±6V (*fig.* 2). The function of this unit is the same whether the joystick is used to position, or determine the size of, the rectangles. Only the positioning system will be described here, the complete system for positioning and sizing the rectangles is described in Section 1 Chapter 5.

2. Dead zones are necessary because the motors associated with rectangle movement are sensitive to inputs in the order of millivolts. If there were no dead zones it would be difficult to position the rectangles in one axis, as the deflection motor in the other axis would tend to rotate as well, causing the rectangle to wander from the direction demanded by the joystick.

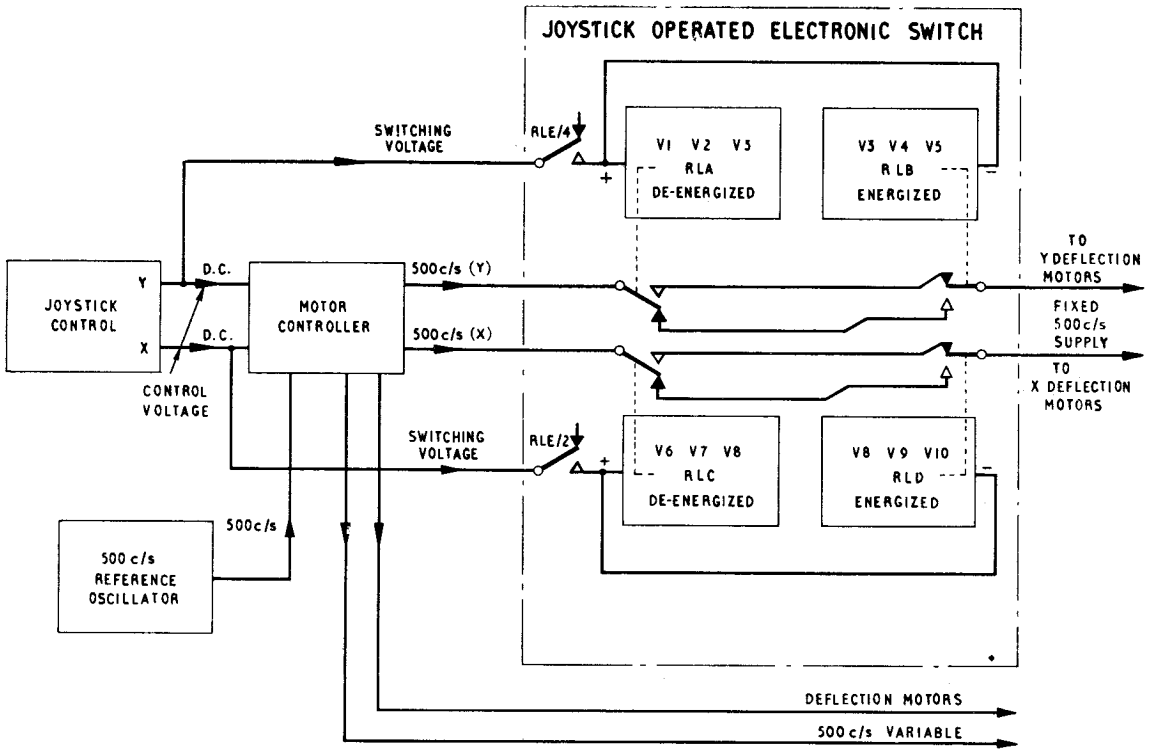


Fig. 2. Switch unit control system

Brief description of system

3. Movement of the display rectangles is effected by motor-driven potentiometers which are in the motor assembly M1 (*Chap.* 3). The direction and speed of rotation of the two-phase motors in the assembly is determined by the motor controller and by the d.c. voltages produced by the joystick control (on the centre console of the radar operator's console suite, *Sect.* 8). The overriding control which determines whether or not the motors will turn (and move the rectangles) is determined by the action of the switch unit, assuming the MOVE/SIZE key is set to MOVE.

4. The motor switching system is shown in block diagram form in fig. 2. There are two identical motors in the system, one to move the rectangle in the X axis and one to move it in the Y axis. One winding of each motor is supplied with a fixed 500c/s supply provided by the 500c/s reference oscillator and fed via the motor controller and the switch unit. The other winding of each motor is also fed from the 500c/s reference oscillator, but the phase and amplitude of this supply is modified in the motor controller by the d.c. voltages fed in from the joystick.

5. The presence or absence of the fixed 500c/s fed to the motors via the switch unit determines whether or not the motors (and therefore the rectangles) will move. The variable 500c/s determines the direction and rate at which the motors, and the rectangles, will move. In this chapter we are concerned with the switching function.

6. The motors are switched individually in the switch unit. For each motor the following conditions have to be satisfied before the fixed 500c/s supply is applied to it.

(1) The joystick displacement, in the X or Y axis, must be sufficient to provide ± 6V d.c.

(2) The button switch on the top of the joystick control must be pressed so the d.c. voltages are made available to the X or Y trigger circuits in the switch unit.

(3) The two relays, controlling the contacts in the fixed 500c/s supply line, must both be in the same state, i.e. de-energized or energized.

(4) The MOVE/SIZE key is set to MOVE.

7. The switch unit consists of two main parts, relay RLE whose contacts make the joystick voltages available to four identical trigger circuits which control valve-operated relays (RLA and RLB for Y inputs and RLC and RLD for X inputs), and the two fixed 500c/s supply lines which are switched by the contacts of the valve-operated relays.

Performance characteristics

Joystick voltages

8. Two d.c. voltages are produced by the joystick when it is moved from its central position. The polarity of these voltages depends upon the quadrant in which the joystick is moved, and they have maximum values, corresponding to maximum movement, of 50V. Maximum movement to the left will produce -50V in the X output and zero output in the Y. Maximum movement ahead (due north) will produce $+50$V in the Y output and zero in the X. The resolved voltages are fed into the switch unit via PLB, pole 2 receiving the Y outputs and pole 5 the X outputs.

Switched 500c/s fixed supply

9. The fixed 500c/s enters the unit from the motor control unit on PLB/1 and PLB/4. The amplitude is constant at about 50V. The input at PLB/1 is switched out to the motor assembly, when relays RLA and RLB are in the same state, and is made

available at SKC/1 to the Y deflection motor on the motor assembly. Similarly, the X motor is supplied when the input at PLB/4 is fed out, via contacts of RLC and RLD, at SKC/4.

Circuit description

Trigger stages

10. The d.c. joystick output voltages are connected to the trigger circuits when the button switch on the top of the joystick completes the −50V supply to RLE (*fig.* 4). Contact RLE4 connects the Y joystick voltage to trigger stages V1 and V5, and contact RLE2 connects the X voltage to V6 and V10.

11. There are four identical trigger circuits of the Schmitt type. One circuit (V1 and V2) will be described, the other three operate in the same manner.

12. V1 and V2 cathodes are connected together and taken to the −250V line via R7. Since the grid of V2 can be set at any potential between approximately +80V and −80V with respect to earth by adjustment of RV1, it is possible to determine whether or not V2 shall conduct.

13. When RV1 is set fully clockwise, V2 grid will be below earth potential and V2 cut off. Cathode follower V1 will conduct since its grid is at earth potential via R5. In this condition an input of the order of −80V would be necessary to reverse the conduction state of the two valves.

14. If RV1 is set fully counter-clockwise, V2 grid is taken above earth potential and the valve current increases the cathode potential due to both valves conducting. Due to this the cathode potential rises above V1 grid potential and V1 is cut off. The circuit remains in this condition until a positive d.c. input from the joystick greater than about +80V is applied.

15. Intermediate settings of RV1 will reduce the joystick input necessary to reverse the conduction state. This setting determines the dead zone on the displays. RV1 in this particular instance is adjusted so that V1 is initially cut off, and so that a positive d.c. voltage of +6V from the joystick will cause V1 to conduct and V2 to cut off. In trigger stage V5, V4, RV2 is adjusted so that V5 is normally conducting.

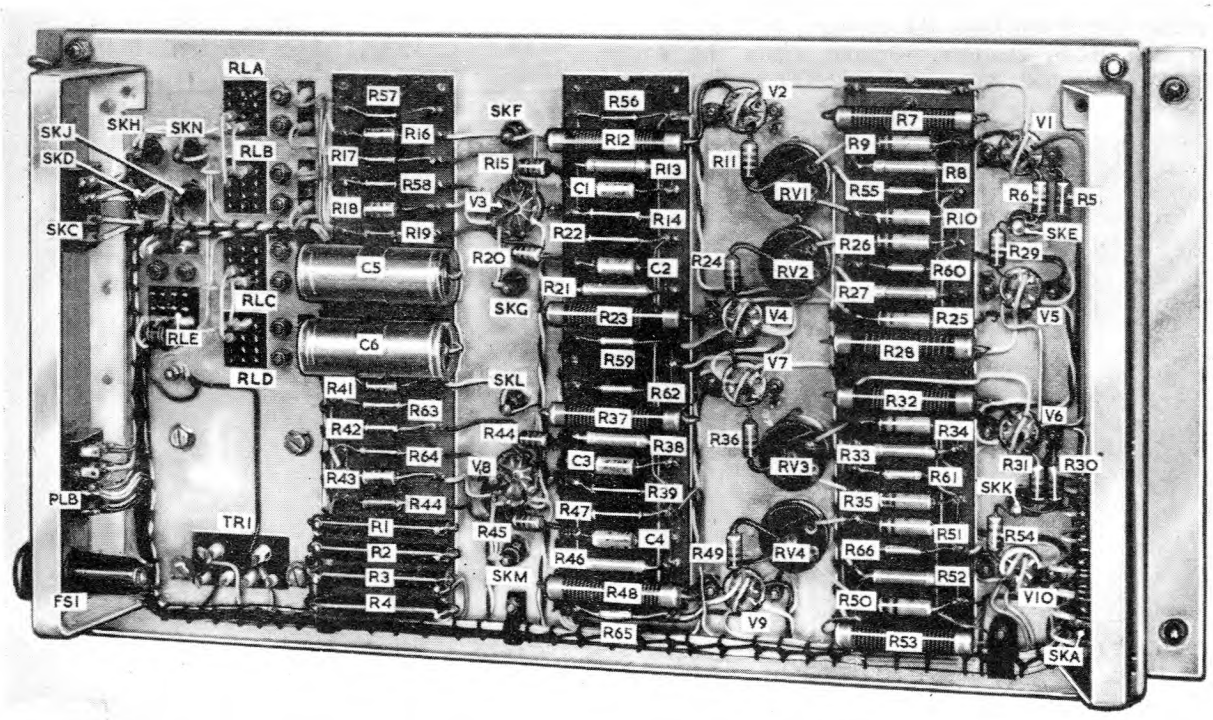
16. For X voltage inputs V6 is cut off and V10 is normally conducting.

Note . . .

When setting up these circuits it is important to adjust the ADJ CURRENT *controls* slowly *to enable the cathode potentials to keep in step with those on the relays.* Ambiguous results will be obtained if the controls are turned too quickly.

Relay stage

17. The four relay stages are fed from the outputs of the four Schmitt trigger circuits. All the stages are identical.



(C49735)

Fig. 3. Switch unit: underside view

18. Considering V3B, the grid is d.c. coupled to V2 which acts as an amplifier. C1 is connected across R13 to accentuate the switching action of V2. When V2 is conducting, the anode potential will be low, hence the grid of V3B, connected in the potential divider chain between V2 anode and the −250V line will be at or below earth potential. In this condition V3B is cut off.

19. When V2 is cut off (due to a joystick input causing V1 to conduct) the V2 anode potential is high, consequently the V3B grid potential will be above earth potential, and V3B will conduct. The resulting anode current will energize RLA, whose contact RLA4, in the fixed 500c/s supply line to the deflection motor, will close.

20. Due to the setting of RV2, the other Schmitt trigger circuit in the Y channel will allow V3A to conduct. RLB will therefore be energized, and its contacts, also in the fixed 500c/s supply line to the deflection motor, will close, completing the motor supply circuit. The corresponding trigger stages and the relays RLC, RLD in the X channel operate in a similar manner.

Fixed 500c/s switching

21. The fixed 500c/s supply to the Y rectangle deflection motor is applied through SKC1 to the motor assembly when contacts RLB2 and RLA4, connected in series, are in the same position.

22. Initially when the unit is switched on, and there is no joystick voltage input, RLA remains in its unenergized condition, but RLB is energized. Thus the supply to the motor is normally disconnected. When a positive d.c. voltage is switched into the unit, sufficient in amplitude to overcome the backlash of the Schmitt trigger circuit, V3B is triggered into conduction, RLA4 changes over and the supply to the Y motor is completed. If a negative d.c. is fed from the joystick, RLB is de-energized, RLB2 changes over and, again, the Y motor is supplied with its fixed 500c/s supply. The X motor is supplied in a similar way via contacts RLC4 and RLD2. All the circuits will revert to their initial state when joystick voltages are removed or fall below ±6V, or when the button switch on the top of the joystick is released.

23. The purpose of C5 and C6 is to prevent the motor d.c. damping voltage being fed back from SKC to PLB.

Monitoring points

24. Twelve metering points are provided to enable the functioning of the unit to be checked by means of a plug-to-socket adapter and a multimeter Type 100. The readings are given in Table 1.

TABLE 1

Multimeter readings

Multi-meter switch	Monitoring Points	Readings	
Position	(Valves)	RV1–RV4 Clockwise	RV1–RV4 Counter clockwise
A	V1	0·6 ± 0·12	
B	V2		0·34 ± 0·7
C	V3B	0·48 ± 0·1	Less than 0·1
D	V5		0·6 ± 0·12
E	V4	0·34 ± 0·07	
F	V3A	Less than 0·1	0·48 ± 0·1
G	V6	0·6 ± 0·12	
H	V7		0·34 ± 0·07
J	V8B	0·48 ± 0·1	Less than 0·1
K	V10		0·6 ± 0·12
L	V9	0·34 ± 0·07	
M	V8A	Less than 0·1	0·48 ± 0·1

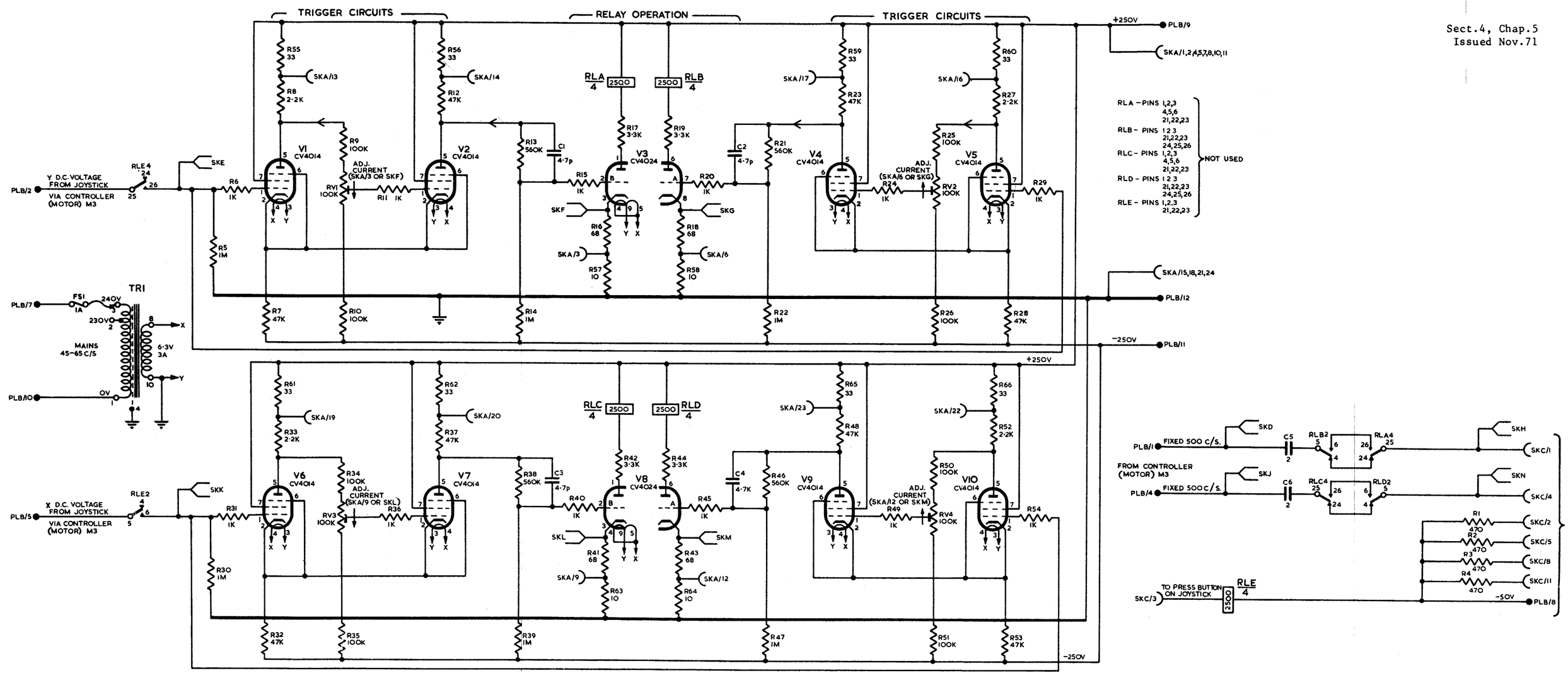


Fig. 4

Switch, electronic (joystick) M5: circuit

Chapter 6

PULSE GENERATOR (SWITCHING) M7

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

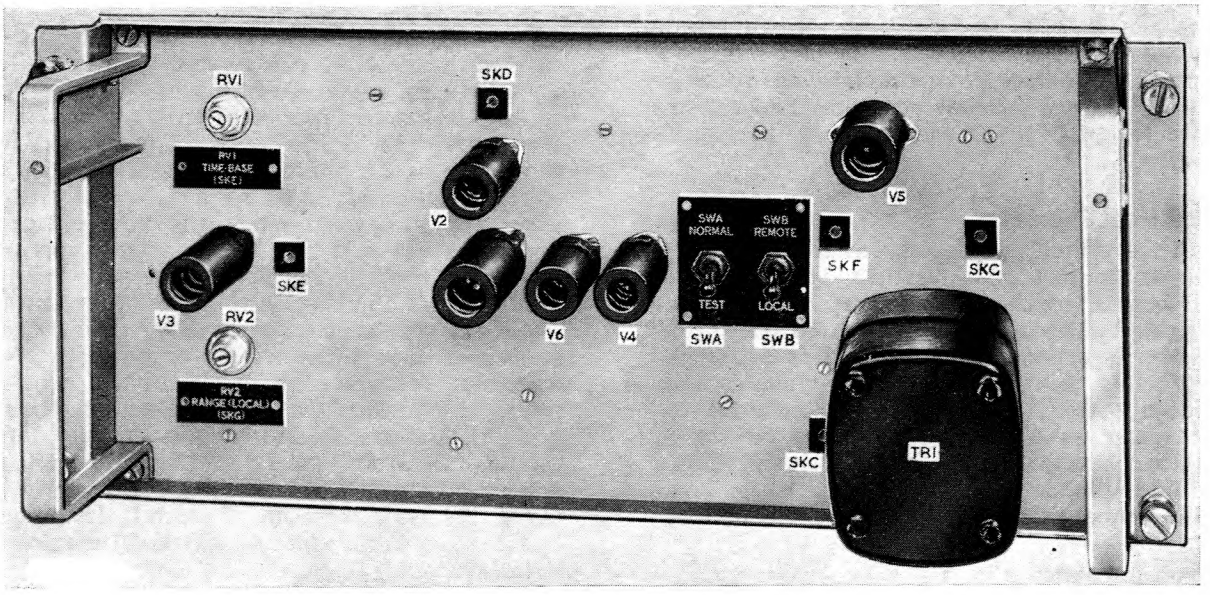


Fig. 1. Pulse generator (switching) M7: front view

Introduction

◀1.▶ The pulse generator (*fig.* 1) is used in two applications, one being in the Doppler cabinet, the other in the video cabinet (*Sect.* 5). In both applications the units produce positive pulse outputs (which are adjustable in duration) from a synchronized input. This input is the 0 microseconds positive-going pulse, generated in the p.r.f. system.

2. In the Doppler cabinet, the pulse generator is used to produce positive pulses approximately ◀500▶ μs long (40 nautical miles). One output is fed to the area switching panel (*Chap.* 7) to define the 40 nautical miles circle on the p.p.i. displays, and another, to produce the selection waveform for video switches 1 and 2 (*Sect.* 5, *Chap.* 5).

3. In the video cabinet, one output is taken to the reverse sweep generator (*Sect.* 5, *Chap.* 7) and a second output to video switch 3 (*Sect.* 5, *Chap.* 5). The output pulse from the video switch is about ◀2·4▶ milliseconds in duration, the trailing edge operating the reverse swept gain circuits.

Operating characteristics

Inputs

◀4. From the p.r.f. system 0 microseconds positive-going pulses of not less than 15V amplitude are fed to SKH on the pulse generator. The pulse width is 4μs nominal.▶

Outputs (Doppler cabinet)

5. The positive pulse outputs at the paralleled output sockets SKJ and SKK should be between 27 and 35 volts. The pulse width, when the unit is used in the Doppler cabinet, is set by RV2, ADJ. RANGE (LOCAL) potentiometer to produce, in conjunction with the area switching panel, the 40 nautical mile marker circle on the p.p.i. displays and a switching waveform of the appropriate duration.

Outputs (video cabinet)

6. The outputs of the unit are made available at SKJ and SKK, and are between 27 and 35 volts in amplitude. The pulse width in this case is adjusted by RV2 to operate the reverse swept gain circuits and to produce a switching waveform of the appropriate duration. The trailing edge of the pulse generator output pulse triggers the reverse swept gain generator in the video cabinet so that it operates at a range of◀200▶nautical miles.

Range control

7. In either application the duration of the waveform may be controlled either by the ADJ. RANGE (LOCAL) potentiometer RV2 on the unit with SWB in position LOCAL or by an external range potentiometer (not used in either of these applications) connected to PLB/1–3 with SWB in the REMOTE position.

Brief circuit description

8. The required rectangular waveform is derived from the output of a Sanatron type oscillator. This output, which is in the form of a negative-going sawtooth waveform, is converted to a square-wave by the action of the two following d.c. amplifiers before being passed to an output cathode follower stage. The mark-to-space ratio of the rectangular waveform is governed by the setting of the d.c. bias to the first of the two amplifier stages and its amplitude by a limiting circuit at the input to the cathode follower output stage.

Circuit description

9. Heater voltages for the valves are supplied from TR1, the a.c. 240V primary supply for the transformer being received at PLB/7 and PLB/10.

10. The −250V supply from the cabinet appears across PLB/11 (−250V) and PLB/12 (earth). The +250V supply from the +250V voltage regulator appears across PLB/9 (+250V) and PLB/12 (earth).

Sanatron oscillator

11. The input pulse is differentiated by the short time constant circuit C1, R2 after which the resultant positive spikes are removed by the conduction of V6a and the remaining negative spikes are passed to the grid of V1a by V6b (*fig.* 2). The diode V2b limits the negative excursions of V1a grid to approximately −8V so that V1a remains just cut-off during the timing period.

12. The output from the anode of V1a is applied as a positive suppressor trigger to the oscillator V3, the suppressor of which is held at a nominal voltage of approximately −10V by a tapping on the potential divider R41, R5, R6 and R9.

13. Capacitor C4 is connected in a Miller circuit between anode and control grid of V3, the anode potential of V3 being caught by diode V2a at approximately 190V in order to effect a reduction in fly-back time. The standing bias on the control grid of V3 is set by the ADJ. TIME BASE potentiometer RV1; this sets the point at which the run down action is terminated, and thus determines the timing of the fly-back which is normally adjusted to occur approximately 300μs before the next input timing pulse.

14. The negative-going sawtooth output is taken from the anode of V3 at the junction of R16 and R17 and applied to the first d.c. amplifier stage via R21. This output is developed across the resistor chain R19, R20 between anode and earth with a monitoring point at SKE: The amplitude of the waveform at this point should be approximately 3V.

D.C. amplifiers

15. The standing bias on the grid of V1b may be derived either from a potentiometer RV2 with the LOCAL/REMOTE switch SWB in the LOCAL position or from an external potentiometer when SWB is in the REMOTE position. In the latter position of the switch the fixed portion of the external potentiometer is connected via PLB/1 and PLB/3 and the slider via PLB/2. In either case the potential applied to V1b grid may be set between approximately 68V and 210V negative with respect to earth. The grid base of V1b is such that the valve is conducting hard when no sawtooth waveform is applied to its grid. However, when the negative sawtooth waveform reaches a point determined by the setting of RV2 or of the external potentiometer, its grid potential continues to be driven negative until the valve is cut off (*fig.* 2). An amplified positive-going sawtooth output is therefore developed at V1b anode, the commencement of which is determined by the setting of the ADJ. RANGE (LOCAL) or external potentiometers.

16. The second d.c. amplifier stage V4 operates in the same manner except that the bias on the grid of V4 is fixed as determined by the divider chain R26, R27 and R28. The potential developed at the anode of V4 now approximates to a rectangular waveform. The waveform at the cathode of V4 can be monitored at SKF.

Output stage

17. The output stage uses a double triode valve V5 connected as a cathode follower with the two halves of the valve connected in parallel. The inputs to the grids of◀V5▶are manually selected by the operation of the NORMAL/TEST switch SWA.

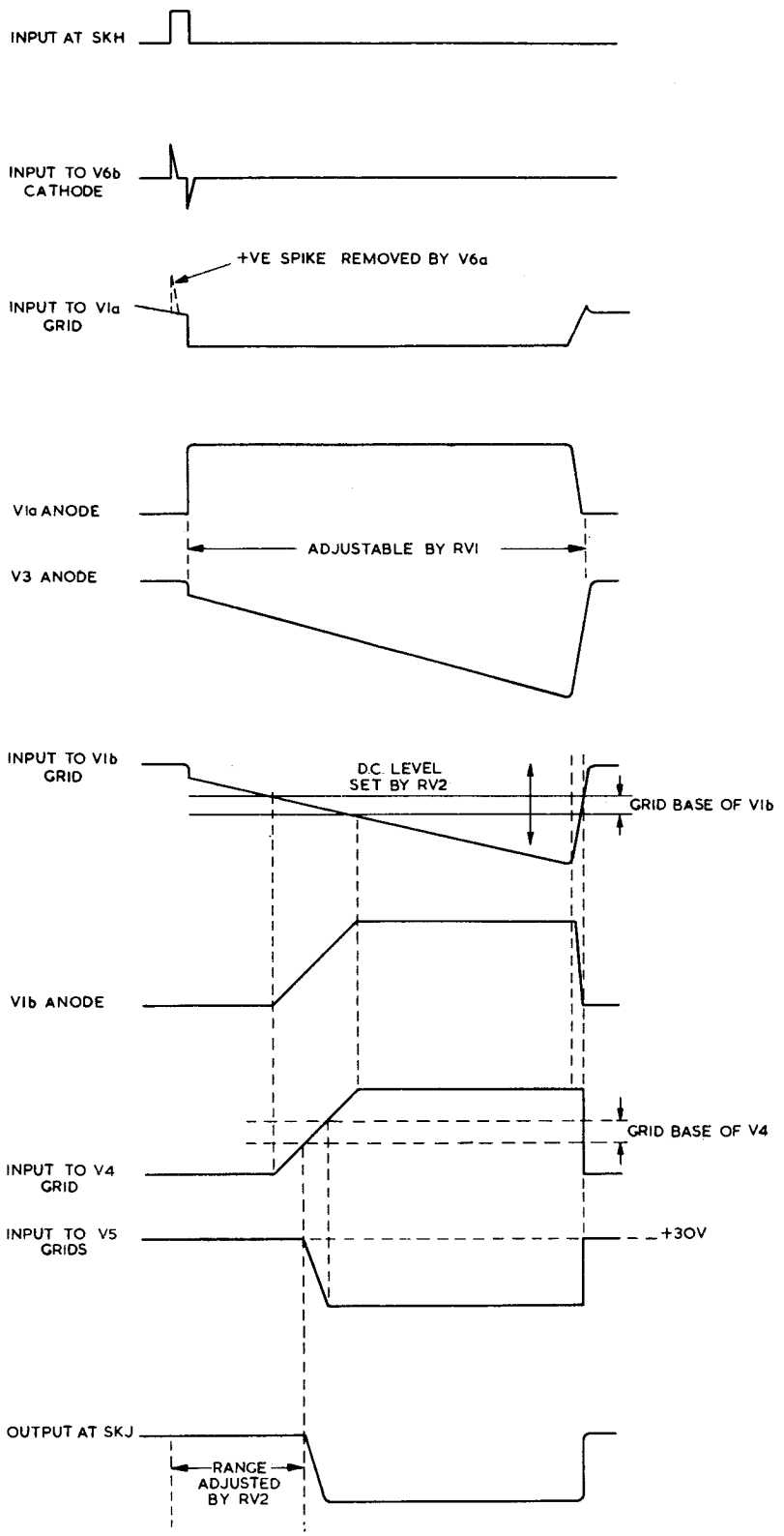


Fig. 2. Pulse generator M7: waveforms

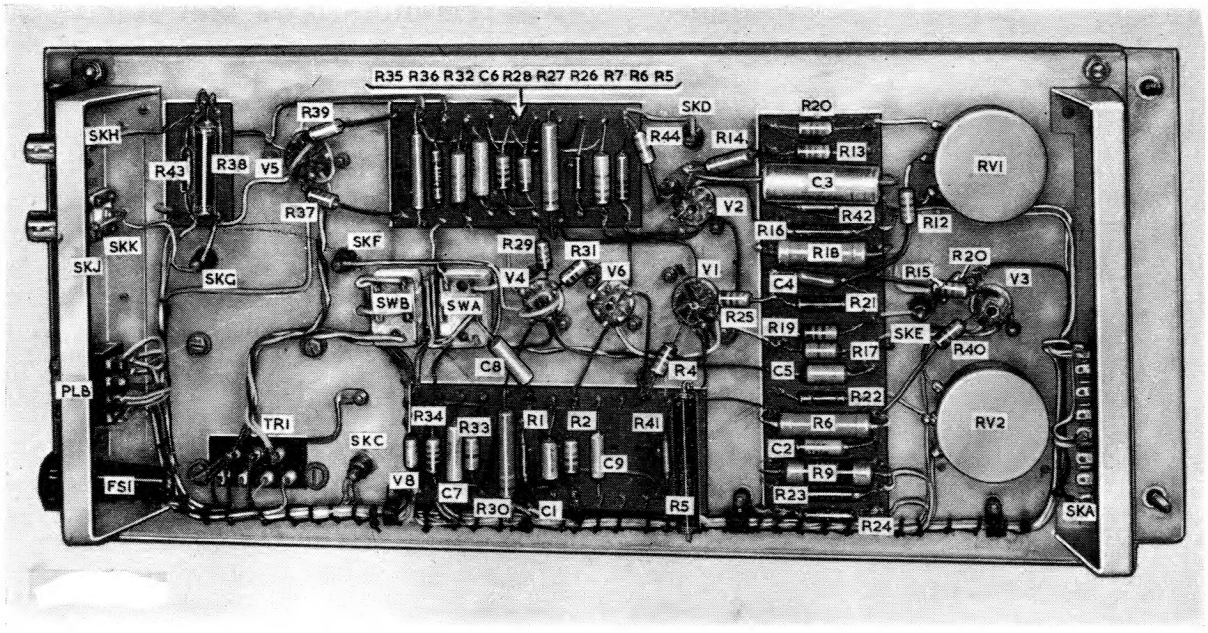


Fig. 3. Pulse generator M7: rear view

In the TEST position of the switch the grids are returned to the mid-point of the potential divider network R35, R36 across the +250V supply and the input from the anode of V4 is disconnected. In this position of the switch the voltage test level measured at test socket SKG will lie between +27V and +35V.

18. In the NORMAL position of SWA the inputs to the grids of V5 are obtained from the anode of V4, the input being limited at approximately +30V by the action of the diode V8 and its associated potential divider network. The amplitude of the rectangular waveform observed at SKG will lie between +27V and +35V under these conditions.

Test readings

19. With the multimeter 100 connected to socket SKA via a plug to socket adapter the readings obtained should be as indicated in Table 1.

Monitoring points

20. Test sockets, SKC–SKG, are provided which may be used for monitoring purposes. The waveforms existing at these points are illustrated in Fig. 4.

TABLE 1

Multimeter readings

SKA pole	Multimeter switch position	Measured across resistor	Reading	Tolerance
13	A	R41	0·61	±0·1
2	B	R43	0·62	±0·1
15	C	R42	0·27	±0·05

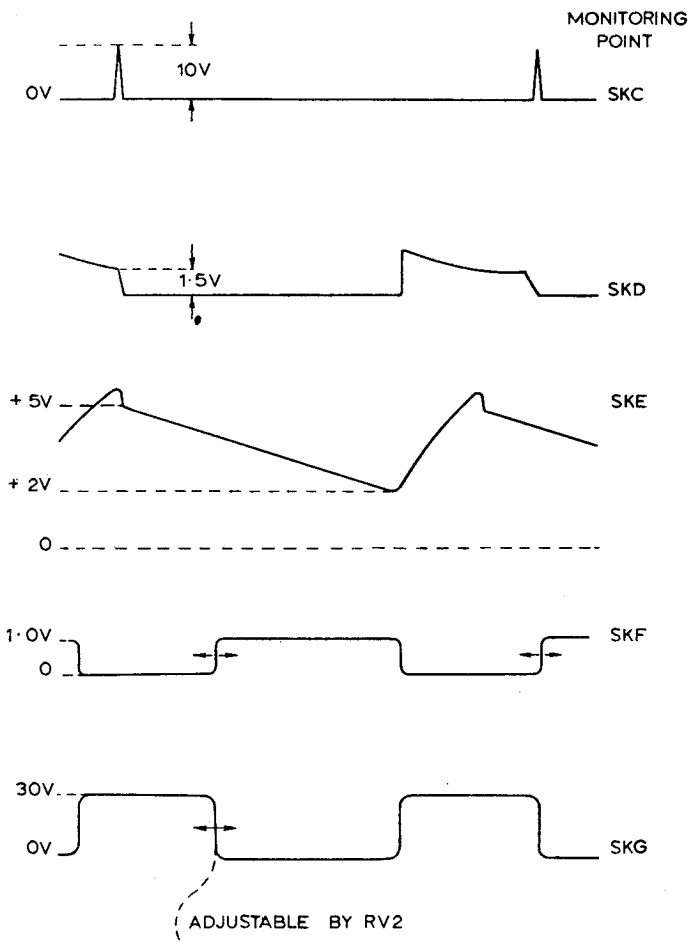


Fig. 4. Pulse generator M7: waveforms at monitoring points

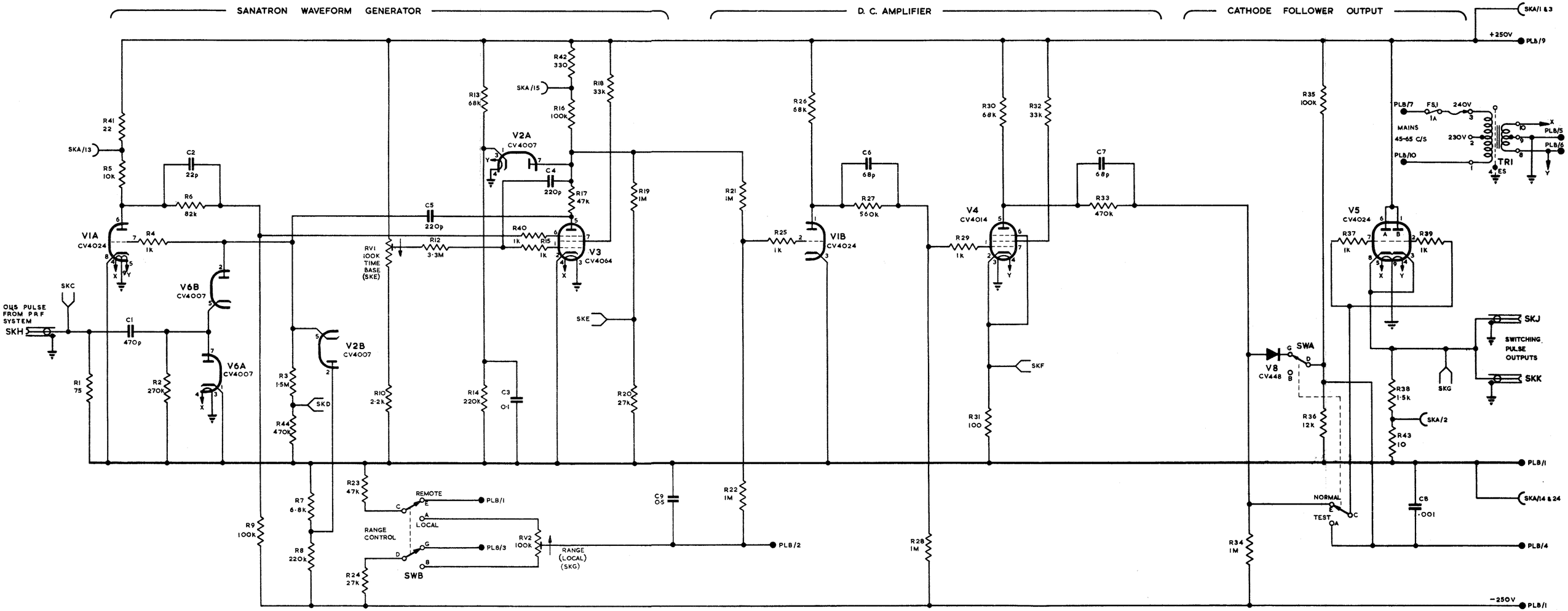


Fig.5

Pulse generator (switching) M7: circuit

Fig.5

Chapter 7

PANEL (AREA SWITCHING) M1

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

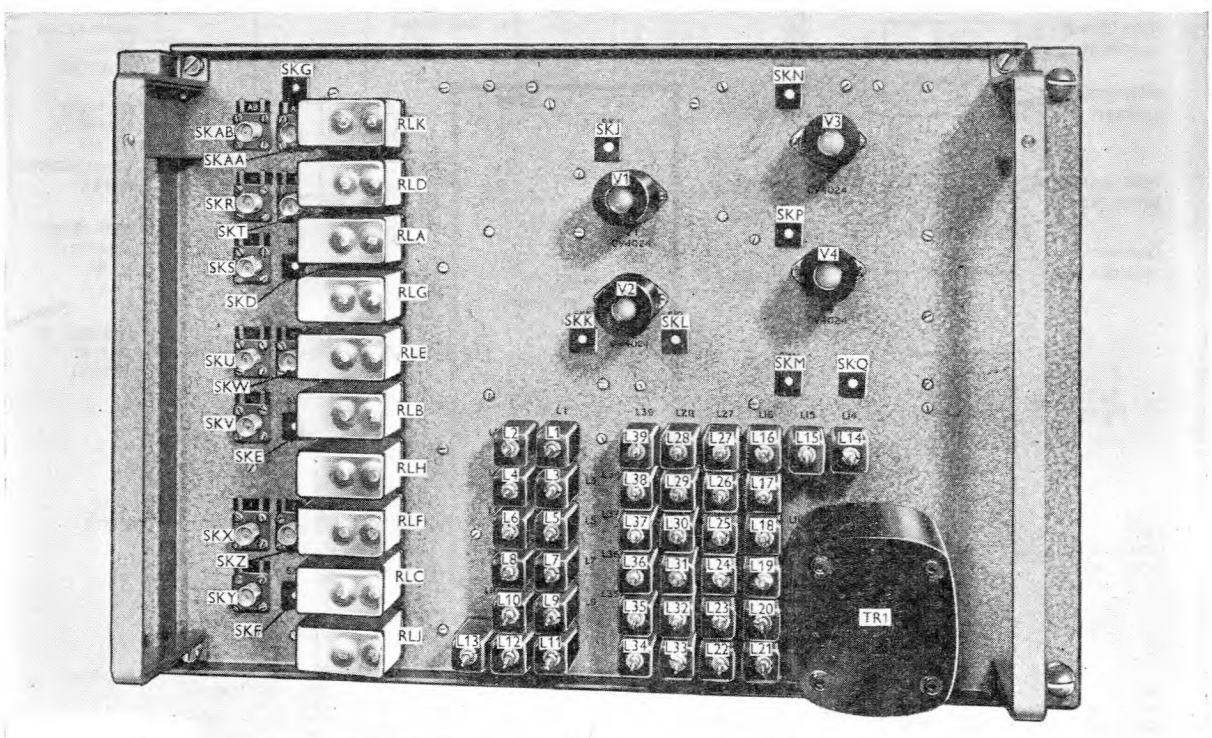


Fig. 1. Panel (area switching) M1: front view

Introduction

1. The panel (area switching) M1 (*fig.* 1 and 9) has two functions related to the Doppler compensation and video switching system. The first of these functions is the generation of the switching waveform for the electronic video switch (*Sect.* 5, *Chap.* 5) associated with the fully-processed video output from the system. The switching waveform is a selected combination of switching waveforms for the circle and the three rectangles. It may be used to operate the video switch over the whole of the circle or rectangle area or it may be used to gate the clutter-switching waveforms (from two clutter-operated switch units) so that the video is clutter-switched within the appropriate areas. The second function is the generation of marker pulses which are fed to the monitor display. These markers indicate the boundaries of the circle and of the three rectangles on the display.

2. The LOCAL/USERS switches on the monitor console control the application of input waveforms from the rectangle pulse generators (*Chap.* 2) to the electronic reference frequency switches (*Chap.* 8) so that Doppler compensation is applied to the cancellation channels. The same switches also control the generation of markers and switching waveforms for the rectangles. Doppler compensation is effective and rectangle markers are displayed with the switches in either the LOCAL or the USERS position but video switching operates only with the switches in the USERS positions. These facilities may be controlled independently for each of the three rectangles. Video switching and marker generation for the circle is operative at all times, there being no switch to control these facilities.

3. Video switching and display marker waveform outputs are delayed by 26 microseconds to match the delays introduced in the clutter-operated switch units and in the signal channels.

4. Video in the circle and in the rectangular areas may be clutter-switched by the use of four CLUTTER SWITCHING controls on the display console. These controls are set to determine whether MTI video shall be displayed in the whole of the appropriate area or whether it shall be clutter switched. This facility applies only to the fully-processed video output.

5. The switching waveform and display marker generating circuits are so arranged that waveforms for rectangle 1 take precedence over those for rectangles 2 and 3 and waveforms for rectangle 2 over those for rectangle 3. A similar order of precedence is obtained in the electronic reference frequency switch for the application of Doppler compensation to the cancellation channels.

6. The unit is fitted in frame 1 of the Doppler cabinet.

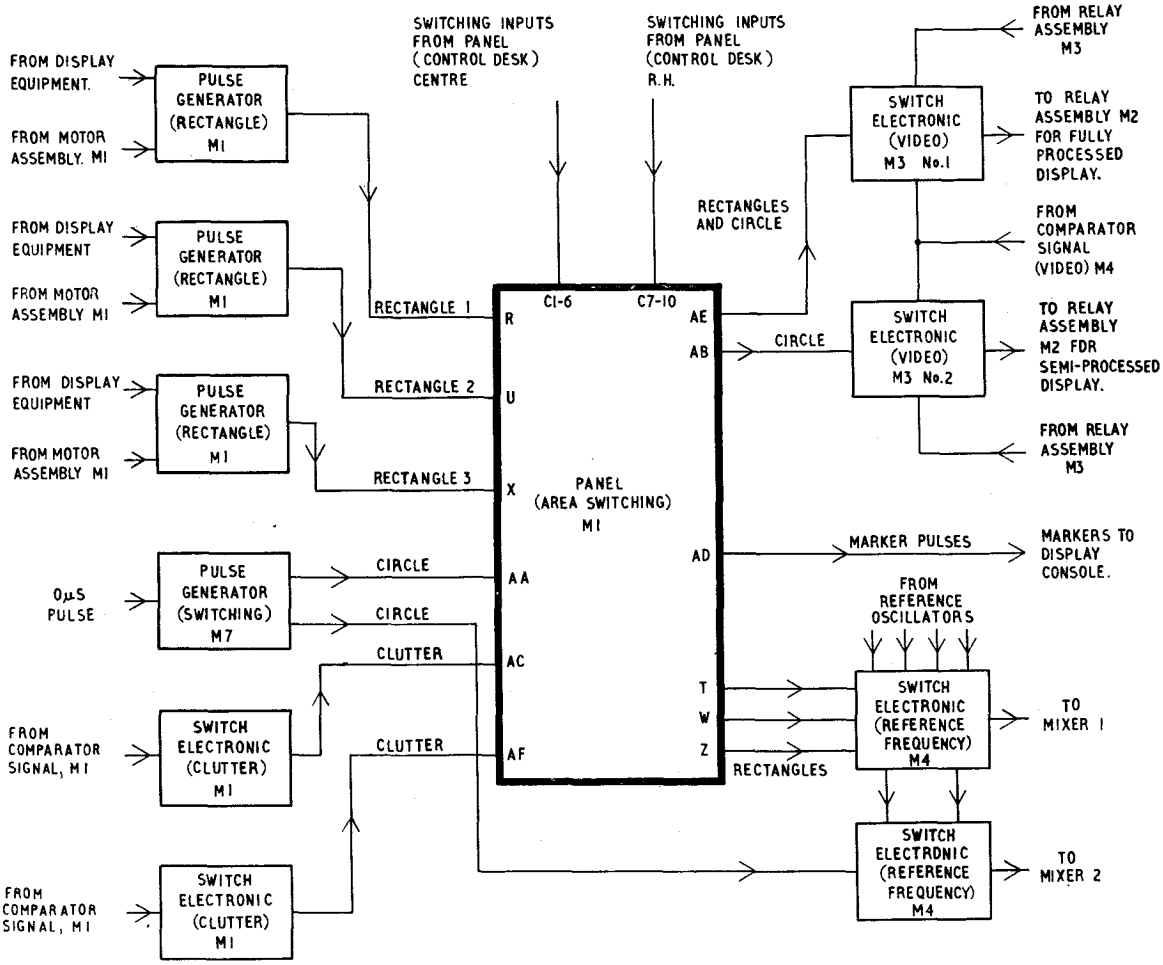


Fig. 2. Panel (area switching) M1: system diagram

Performance characteristics (*fig.* 2 *and* 3)

Inputs

7. Six inputs are received by the unit, one from each of the rectangle pulse generators at SKR, SKU and SKX, one from the circle switching pulse generator at SKAA and one from each of two clutter-operated switching units at SKAC and SKAF. Each of these inputs consists of rectangular waveforms with an amplitude of approximately 27V.

8. Should any of the previously mentioned switches be operated an earth will be received at the appropriate poles of SKC 1–10.

9. The inputs at SKR, SKU and SKX are not available until the appropriate LOCAL/USERS switches are operated since these switches also control the outputs from the rectangle pulse generators.

Outputs

10. A marker output at SKAD, consisting of narrow (approximately 2 microseconds) positive-going pulses with an amplitude of approximately 6V, is fed to the monitor display console. A circle marker output is always present but rectangle markers are only obtained when relays RLD, RLE and RLF are operated.

11. The switching waveform output at SKAE consists of variable width, positive-going rectangular waveforms with an amplitude of approximately 20V. A circle waveform output is present at all times but outputs for the rectangles are only produced when relays RLA, RLB and RLC are operated. These outputs are fed to video switch 1.

12. Switching waveform outputs, identical to those received at SKR, SKU and SKX are fed to the electronic reference frequency switch unit for the fully processed display from SKT, SKW and SKZ. These outputs are present only when relays RLD, RLE and RLF are operated.

13. The circle switching waveform input at SKAA is connected directly to SKAB whence it is fed to the video switch for the semi-processed display.

14. Direct connections are made from input sockets SKR, SKU and SKX to output sockets SKS, SKV and SKY respectively (*fig.* 11). These outputs are not used.

Brief circuit description (*fig.* 2 *and* 3)

Marker generation

15. With the panel in full operation, i.e. with all rectangles in use, relays RLA to RLF are all operated. The rectangular waveform inputs at SKR, SKU and SKX are applied to sockets SKT, SKW and SKZ and thence to the electronic reference frequency switch. These waveforms, with a precedence decided by the input divider network and diodes V15 and V16, are also applied to the marker generation circuits via differentiating circuits. Positive pulses are produced at the beginning of each rectangular waveform and negative pulses at the end of the waveform. After amplification (V1A) the pulses are applied to a full-wave rectifier circuit (V17, V18), the output from which consists of positive pulses to indicate the beginning and end of each of the input waveforms. These pulses are amplified (V1B, V2A) and fed to an open-circuit delay line in the cathode circuit of V2A.

16. The pulses are reflected from the delay line so that the output from the anode of V2A consists of a series of positive pulses each followed, after a delay of 26 microseconds, by a negative pulse. The output stage V2B is normally cut off but is made to conduct heavily by the positive pulse outputs from V2A which are received via a pulse stretching circuit (V20, V21). V2B continues to conduct until it is again cut off by the negative pulse received from V2A. The anode circuit of V2B is thereby caused to ring and a positive pulse is produced at the output socket SKAD.

Switching waveform generation

17. For the production of switching waveforms the input rectangular waveforms, in order of precedence, are amplified (V3A) and applied to a 26-microsecond delay line. The output from the delay line provides one input to an AND gate. The second input to the gate depends upon the operated conditions of relays RLG to RLK. Thus, for example, with RLA and RLG operated, the duration of the input to V3B will be decided by the overlap between the input at SKR and the delayed waveform at the AND gate. With only RLA operated the input to V3B consists of pulses representing the coincidence periods between the delayed input from SKR at the AND gate and the inputs at SKAC and SKAF, the latter inputs having already been delayed by 26 microseconds in the clutter switching and associated circuits. V3B and V4A are conventional amplifiers and are followed by a cathode follower stage V4B, the switching waveform output being taken from SKAE.

Circuit description

Power supplies

18. The heater voltages for the valves are supplied from TR1, the 240V a.c. supply for the transformer being received at PLB/7 and PLB/10 and applied to the transformer via fuse FS1. This supply is controlled by the main system switch which controls the mains supply to all units of the complete system.

19. The −50V supply is received at PLB/8, the −250V supply from the power cabinet across PLB/11 (−250V) and PLB/12 (earth) and the +250V supply from the +250V voltage regulator across PLB/9 (+250V) and PLB/12 (earth).

20. For the purpose of this description the unit may be considered as consisting of three parts, viz.:—

(1) The marker waveform generation circuits.
(2) The switching waveform generation circuits.
(3) The Doppler compensation output circuits.

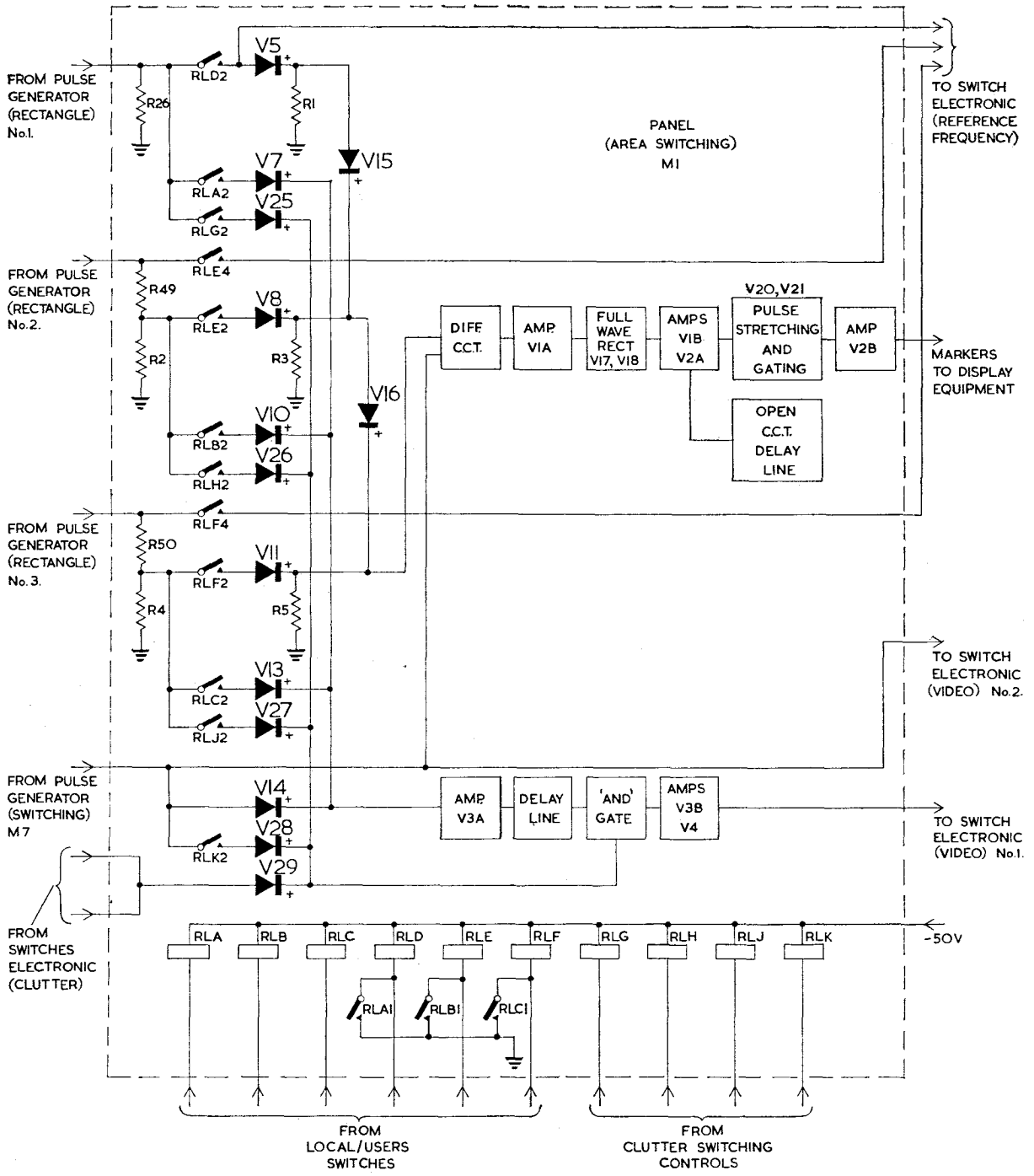


Fig. 3. Panel (area switching) M1: block diagram

Marker generation

21. The coils of relays RLD, RLE and RLF are connected between the −50V supply and sockets SKC/1, 2 and 3 respectively so that application of an earth to one or more of these sockets causes the appropriate relay, or relays, to be energized. Alternatively, the relays may be energized by the operation of relay contacts RLA1, RLB1 or RLC1.

22. With contacts RLD2 operative, the input at socket SKR (*fig.* 4), at an amplitude of about 27V is applied via diodes V5, V15 and V16 to the differentiating circuit C3, R6. After a very short period, C3 is charged and remains charged for the duration of the positive waveform input.

23. The input at socket SKU (*fig.* 4), also of approximately 27V amplitude, is connected to the divider chain R49 and R2 so that, with relay contacts RLE2 operated, the waveform amplitude fed via V8 and V16 to C3 from the junction of the resistors is approximately 18V. If an input is already present at SKR and contacts RLD2 are operated, no further action can take place because C3 is already charged to 27V and V8 will therefore not conduct. If, however, there is no input at SKR, or if contacts RLD2 are not operated, V8 will conduct and C3 will charge to approximately 18V via V16 (*fig.* 5).

24. The input at SKX is connected to a resistor chain R50 and R4, so that with contacts RLF2 operated, the waveform amplitude fed via V11 to C3 is approximately 9V (*fig.* 4).

25. When the leading edge of a waveform is applied to V5 the charging current in C3 produces a positive-going pulse across R6 but subsequent application of waveforms to V8 and V11 has no

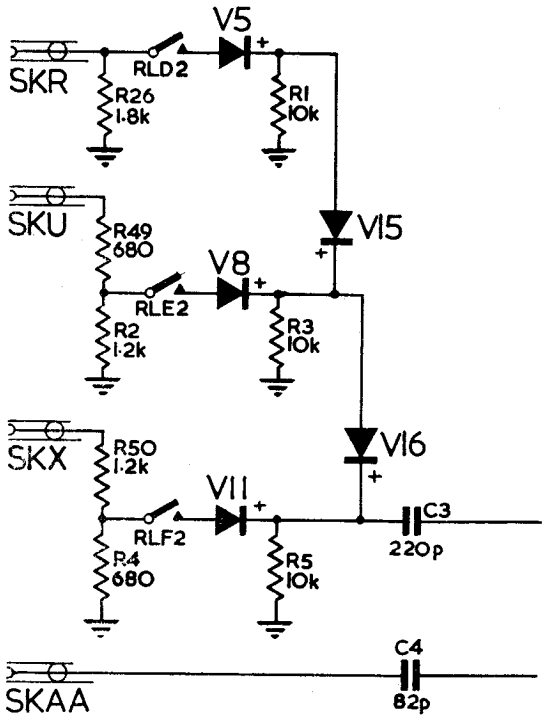
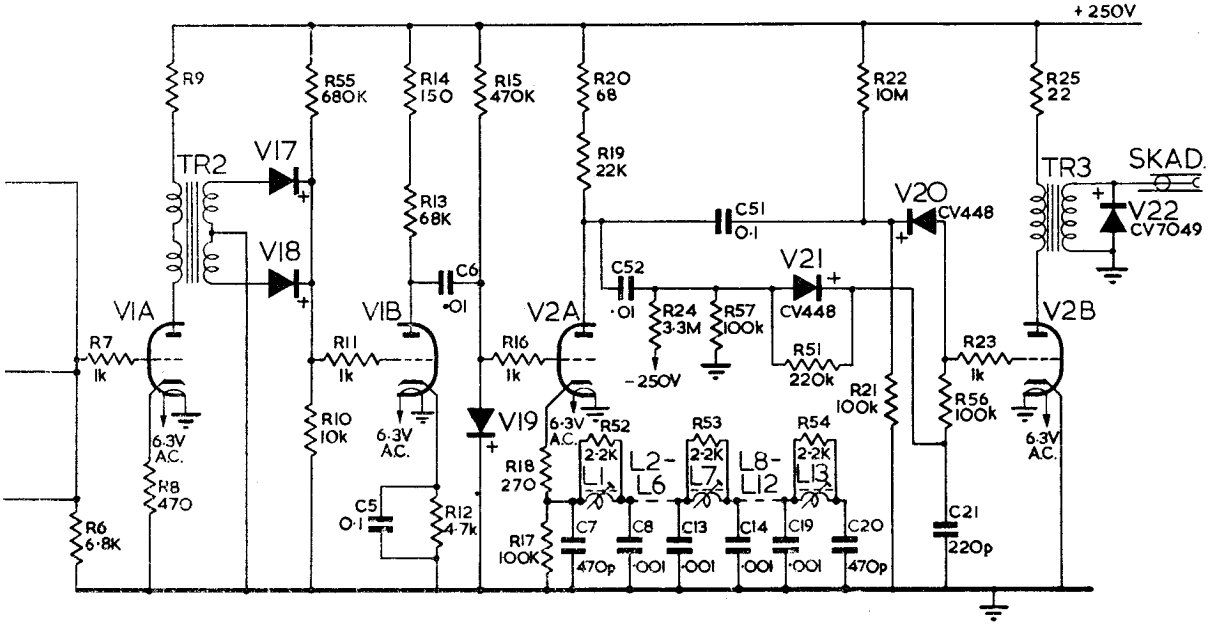


Fig. 4 (Part 1). Marker generation circuit



◀ **Fig. 4 (Part 2). Marker generation circuit** ▶

effect at R6; this also applies when the application of the leading edge of a waveform to V8 is followed by the application of the leading edge of a waveform to V11 (*fig.* 5). However, it will be seen from fig. 5 that, should the application of a waveform to V11 be followed by the application of a waveform to V8 or V5, or the application of a waveform at V8 be followed by the application of a waveform to V5, the charge across C3 will be increased accordingly and a further positive-going pulse, or pulses, will be developed across R6.

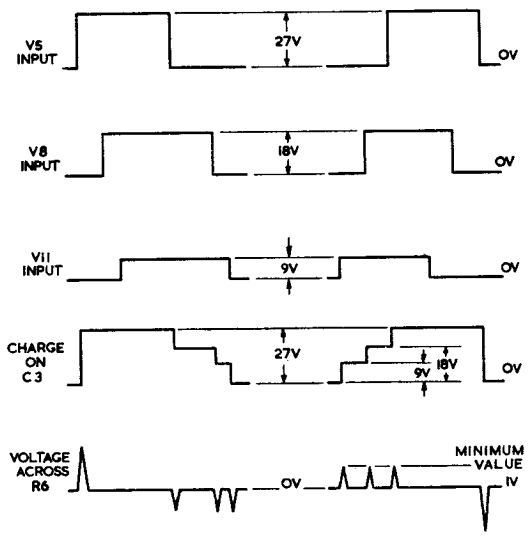


Fig. 5. Initial marker waveforms

26. At the trailing edges of input waveforms, negative-going pulses will appear across R6 except that no pulse will appear across R6 at the trailing edge of a waveform at V11 while waveforms still exist at V8 or V5, because the charge on C3 is maintained by either or both of these waveforms, and no pulse will appear across R6 at the trailing edge of a waveform at V8 while the waveform at V5 persists, because the charge on C3 is maintained by the waveform at V5. By these means, precedence is given to the waveform at SKR over those appearing at SKU and SKX, or to the waveform at SKU over that at SKX where overlapping of waveforms occurs.

27. The input at SKAA, which also consists of a rectangular waveform with an amplitude of approximately 27V, is applied directly to C4 (*fig.* 4) so that a positive-going pulse is produced across R6 at the leading edge of the waveform and a negative-going pulse at the trailing edge of the waveform; these pulses are independent of those produced by the charge and discharge of capacitor C3 and are produced regardless of any overlap of waveforms.

28. To explain the remainder of the marker generation circuits it is convenient to consider a single positive-going and a single negative-going pulse, as produced at the leading and trailing edges of a single rectangular waveform. Waveforms appropriate to various points in the circuit are given in fig. 6.

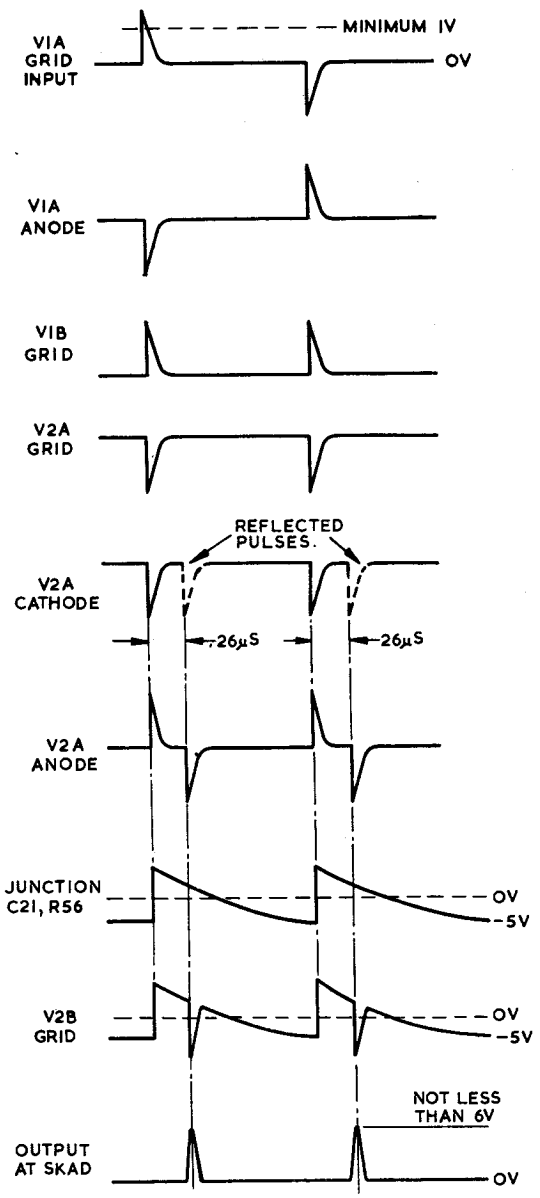


Fig. 6. Marker waveforms

29. The differentiated waveform produced across R6 (*fig.* 4) is applied to the grid of V1A whereupon negative- and positive-going pulses are developed across the primary winding of TR2. The secondary winding of TR2 is connected in push-pull to the diodes V17 and V18 so that positive-going pulses are fed to the grid of V1B. Negative-going pulses developed at the anode of V1B are coupled to the grid of V2A via C6 and limited to earth potential by the diode V19. Positive-going pulses are produced at the anode of V2A and negative-going pulses at its cathode, the latter being connected to the open-circuit delay line C7 to C20 and L1 to L13 so that the negative-going pulses are reflected back, in phase, from the end of the delay line and arrive at the cathode after a delay time of 26 microseconds. Since V2A grid is held at earth potential between input pulses the negative-going reflected pulses at the cathode produce negative-going pulses at the anode, the delay time between the original positive-going pulses and the negative-going pulses being 26 microseconds.

30. The output from the anode of V2A therefore consists of positive-going pulses, followed after a delay of 26 microseconds by negative-going pulses. Upon the arrival of a positive-going pulse at the anode of V21 the diode conducts and C21 is charged to a potential dependent on the pulse amplitude. V2B conducts and continues to conduct, though V21 is cut off as soon as the positive pulse ends. The pulse input to the grid of V2B is effectively stretched by the discharge time of C21, via R51 and R57, which is in the order of 700 microseconds. However, after 26 microseconds a negative pulse arrives at the cathode of V20 which was previously cut off by a potential of approximately +23V with respect to earth due to the divider network R21 and R22. As soon as V20 conducts due to the negative pulse, V2B is cut off sharply.

31. The output marker pulses are produced by V2B which has an anode load consisting of TR3 with its secondary winding shunted by the diode V22. This circuit rings when the valve is sharply cut off, but the polarity of the diode connection is such that negative half-cycles of oscillation are damped out. Marker pulses are produced which are delayed by 26 microseconds after the leading and trailing edges of the input waveforms, with an order of precedence determined by the input divider networks and their associated diodes. V2B is kept non-conducting between pulse sequences because V21 is cut off by the potential divider R24, R57, connected across the −250V supply.

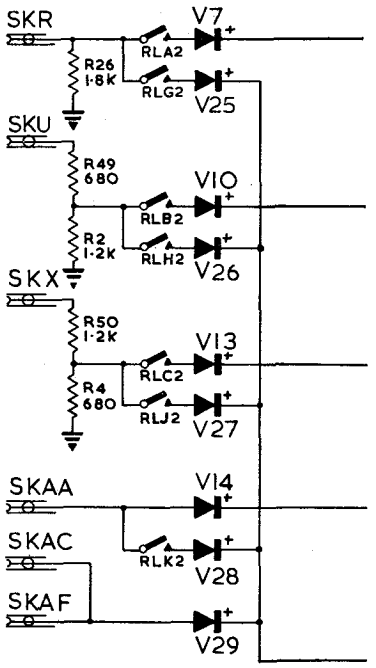


Fig. 7 (Part 1).
Switching waveform generation circuit

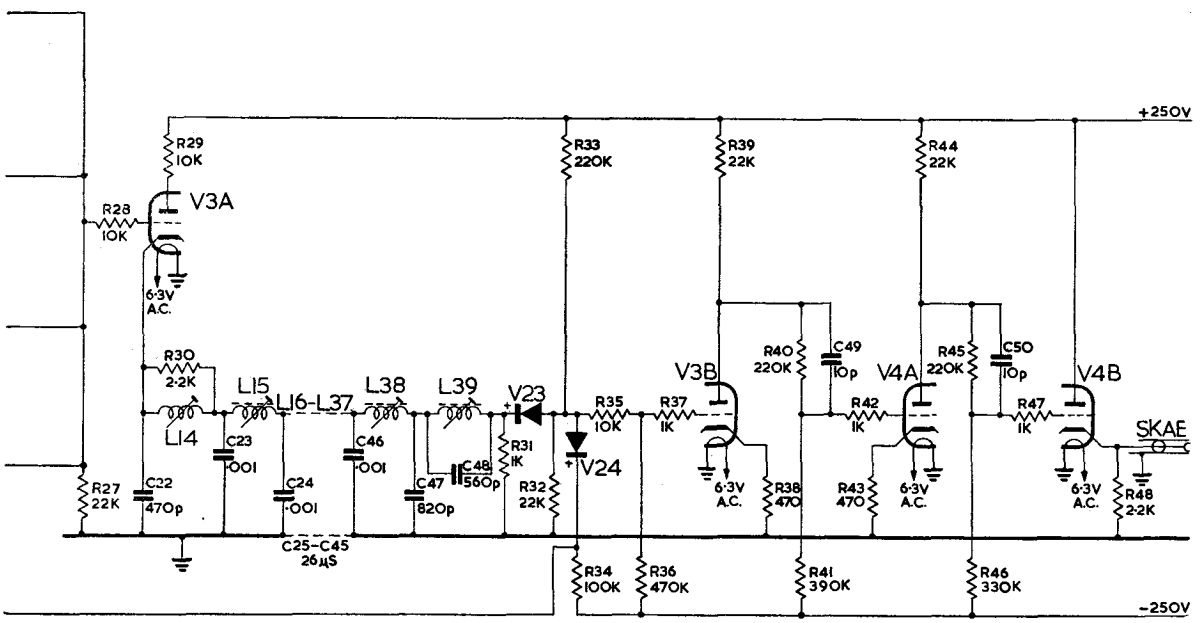


Fig. 7 (Part 2). Switching waveform generation circuit

Switching waveform generation

32. The coils of relays RLA to RLC and RLG to RLK are connected between the −50V supply and socket SKC poles 4 to 10 respectively, so that application of an earth to any one or more of these poles causes the appropriate relay, or relays, to be energized (*fig.* 11). The selected input waveforms are then applied via relay contacts RLA2, RLB2 or RLC2 (*fig.* 7) to the diodes V7, V10 and V13, the amplitudes of the waveforms being the same as those applied to V5, V8 and V11 (*para.* 22 *to* 24). In addition to these inputs, the waveform at SKAA is applied directly to V14.

33. Whenever an input is applied to any of the diodes a positive potential with respect to earth is produced across R27. With no input from any circuit the grid of V3A is at earth potential and the valve is already conducting so that an input of 9V or more at the grid is sufficient to drive it into full conduction (*fig.* 8). A positive-going waveform appears at the cathode during any period when an input is impressed on the grid. The cathode waveform is applied to the delay line, C22 to C48 and L14 to L39, and after a delay time of 26 microseconds arrives at the cathode of V23.

34. The switching waveform output is so arranged that it may either consist of rectangular waveforms coinciding (except for the 26 microsecond delay period) with any one or more of the inputs at SKR, SKU, SKX or SKAA, or of a number of rectangular waveforms appearing at the coincidence periods of the above inputs delayed by 26 microseconds and that at SKAC or SKAF. In the latter case relays RLG to RLK are unoperated but in the former instance the appropriate input is selected by operation of one or more of these relays. The required waveform is then fed via diodes V25 to V28 to the cathode of V24, this waveform overriding the waveforms received via V29 from SKAC or SKAF.

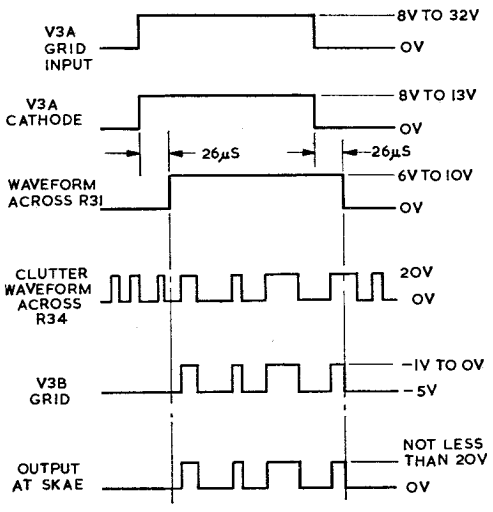


Fig. 8. Switching waveforms

35. In the quiescent condition, i.e. with no inputs to the cathodes of V23 and V24, the grid potential of V3B is determined by divider networks, including V23 and V24 which are both conducting, across the +250V and −250V supplies and is such that V3B is cut off. The common point of V23 and V24 is at approximately earth potential so that the grid is approximately 5V negative with respect to earth. With only one input, to the cathode of either V23 or V24, the grid of V3B remains at the same potential since the cathode of the diode to which no input is applied remains at earth potential.

36. During periods in which inputs to V23 and V24 coincide, both diodes are cut off so that the grid potential of V3B rises to that determined by the divider chains R32, R33, R35 and R36 and the valve conducts. A negative waveform is produced at V3B anode which is inverted by V4A to produce a positive waveform at V4B grid and hence a positive waveform at its cathode: this waveform is applied to socket SKAE as the switching waveform output of the unit.

Switching outputs for doppler compensation equipment

37. The full amplitude of the input waveforms at SKR, SKU and SKX is fed to the doppler compensation equipment via sockets SKT, SKW and SKZ respectively when relay contacts RLD2, RLE4 and RLF4 are operated. Separate relay contacts are used for the outputs at SKW and SKZ since the full amplitude of the input waveforms is required and this is not available at relay contacts RLE2 and RLF2.

Test readings

38. With the multimeter, Type 100, connected to socket SKA via the plug-to-socket adaptor and with relays RLA to RLF released the readings obtained should be as indicated in Table 1.

Monitoring points

39. Test sockets are provided at various points for use with a monitoring oscilloscope. The waveforms existing at these points are illustrated in *fig.* 10.

TABLE 1

Multimeter readings

Multimeter switch position	Stage monitored	Reading	Tolerance	
A	V1A	0·56	±0·11	20%
B	V1B	0·50	±0·10	
C	V2A	0·45	±0·09	
D	V2B	<0·1		

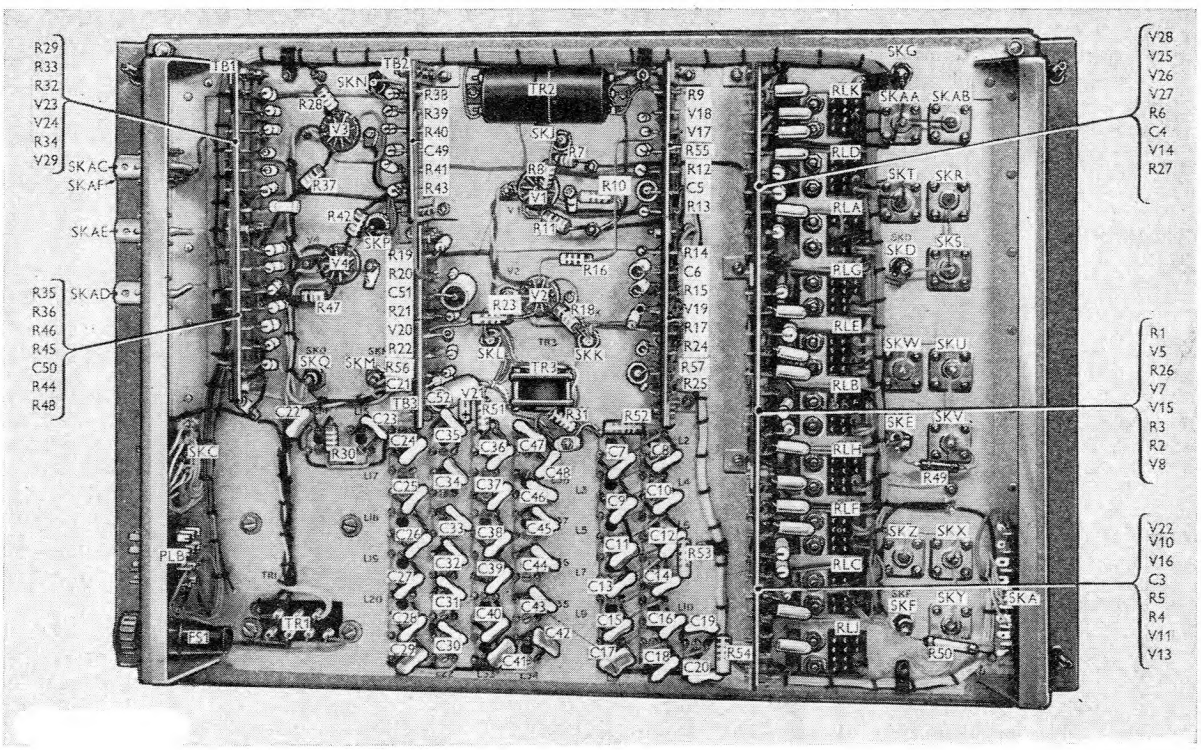


Fig. 9. Panel (area switching) M1: rear view

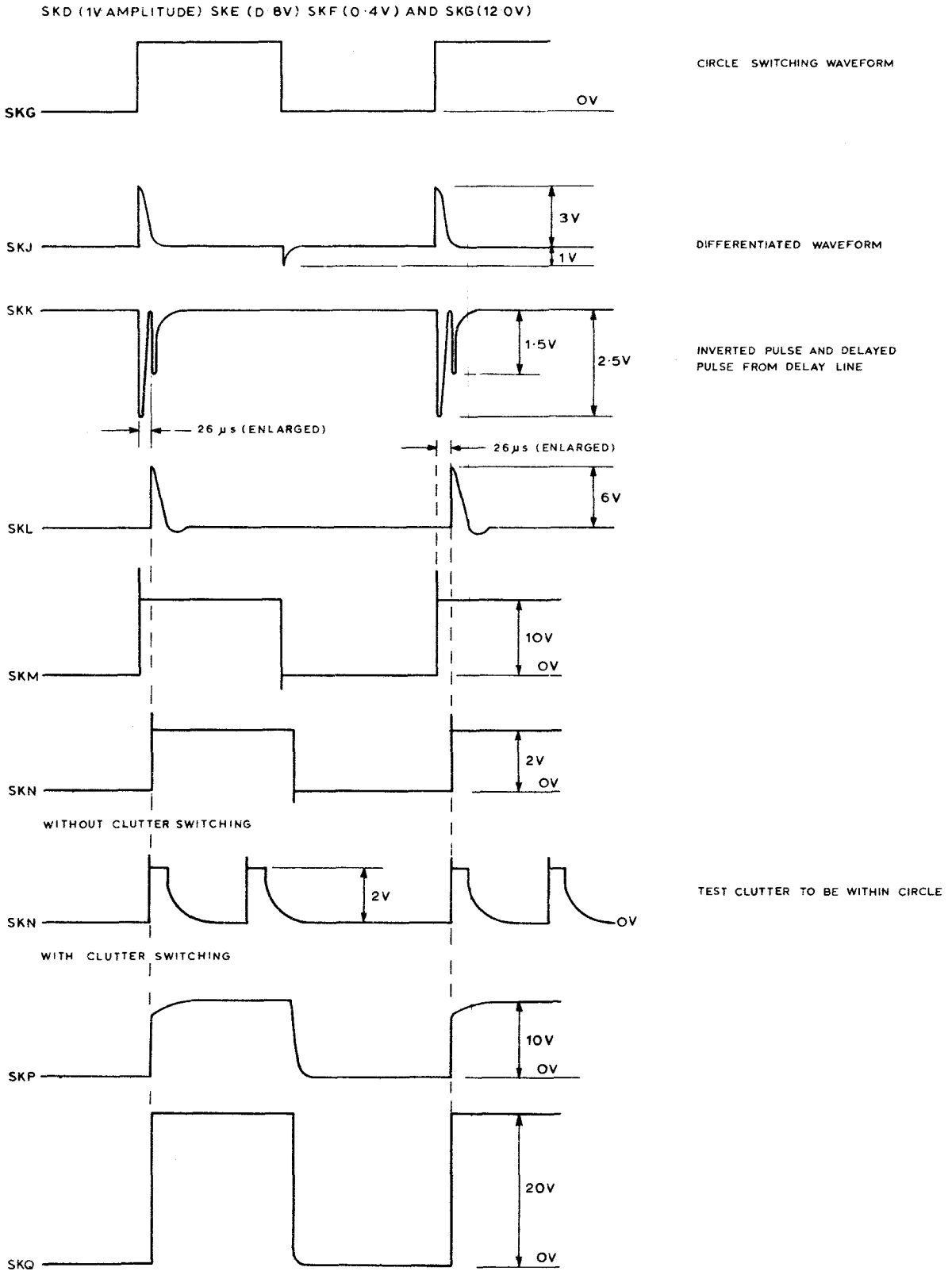


Fig.10 Waveforms at monitor points

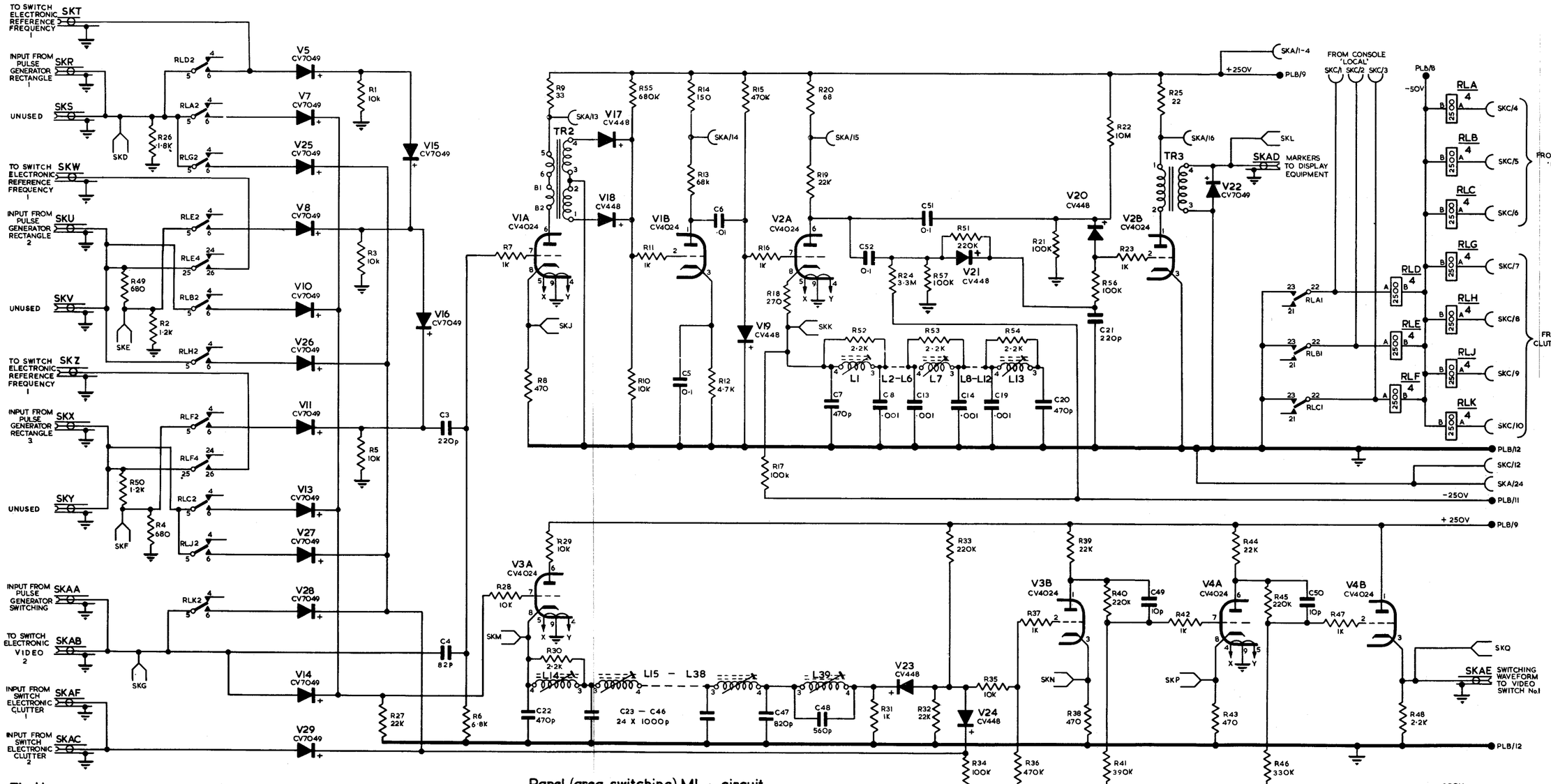


Fig.11.

Panel (area switching) M1 : circuit

Fig.11.

Chapter 8

SWITCH, ELECTRONIC (REF. FREQ.) M4

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

◀APPENDIX

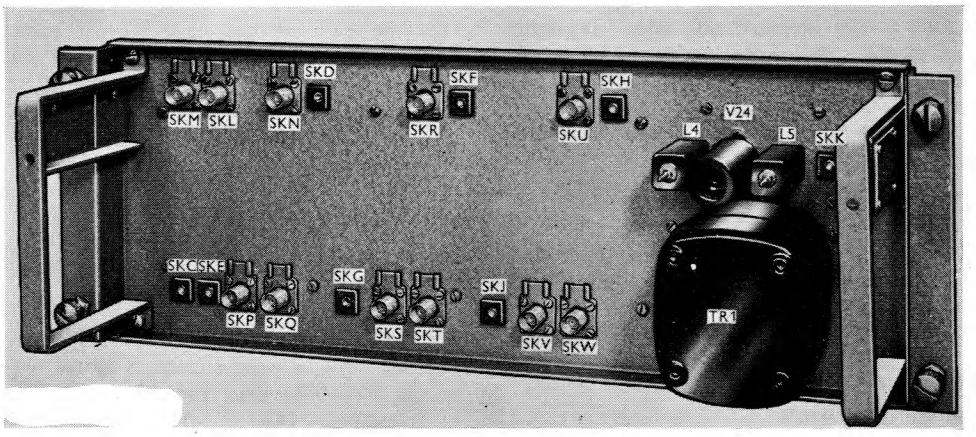


Fig. 1. Switch, electronic (ref. freq.) M4: front view

Introduction

1. There are two switches of this type (*fig.* 1); they are located in frame 3 of the Doppler cabinet. The purpose of these units (*fig.* 2) is to select, by means of switching waveforms, the doppler compensating signals which are used to change the frequency outputs of the mixer stages (*Sect.* 2, *Chap.* 16) feeding the cancellation channel demodulators (*Sect.* 1, *Chap.* 5). The switching waveforms are those used to produce the rectangles and circle on the display consoles.

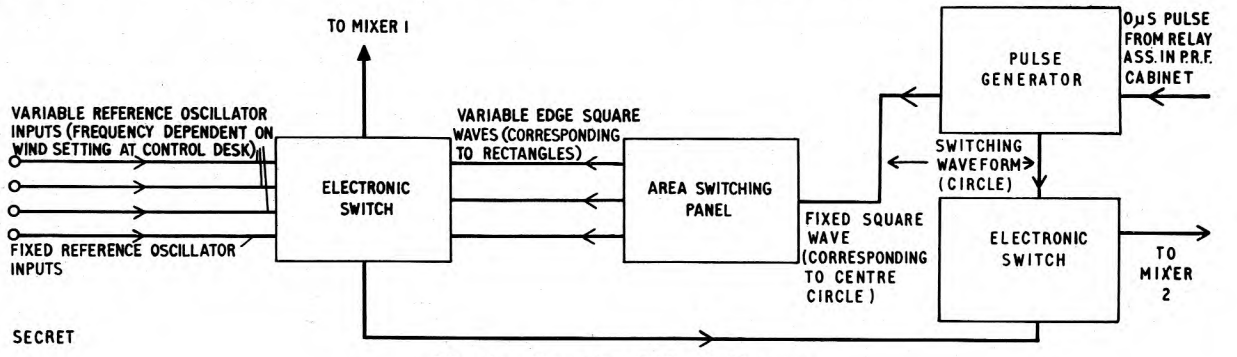


Fig. 2. Functional block diagram

2. The unit basically consists of three changeover switch sections connected in series feeding a tuned impedance matching stage. The switch sections are made up of a pair of diode switches. The switch sections, in the absence of switching waveforms, are d.c. biased so that an input appearing at SKL or SKM is passed through the unit to the output terminals SKX and SKY. When switching waveforms are applied, the Doppler compensating frequency is switched, whether or not they will appear at the output, will depend upon the state of the switching sections following the switched section.

3. The switches function together (*Sect.* 1, *Chap.* 5). The first switch is operated by three switching waveforms coming from the area switching panel. Each switching waveform is identified with a particular rectangle, which routes out a particular Doppler compensating frequency to the mixer stages.

4. In the absence of these three switching waveforms, a fixed compensating frequency applicable to the centre circle on the display is fed through the first switch unit and applied to the second unit.

5. The second switch unit uses only one switching section. This determines whether a fixed reference frequency, which will eliminate Doppler compensation, or the reference frequencies as selected by the first switch unit shall be applied to the mixer feeding channel A demodulator. Cancellation channel A always has the fixed reference frequency applied to it in the circle area whereas channel B has Doppler compensation applied to it where any rectangle overlaps the circle area. The reference frequencies applied to both cancellation channels are identical outside the circle area.

6. Most of the switching circuit components are mounted on a printed circuit board. This is secured to supports on the unit chassis by means of seven nuts. Circuit connections to chassis mounted components are made by fourteen leads. A screening cover is fitted over the board assembly.

Performance characteristics

Inputs (*rectangle switching*)

7. There are seven inputs to the unit. Four inputs are sinusoidal signals from four reference oscillators M3, in the Doppler cabinet. Three of these inputs corresponding to the Doppler compensation within the three rectangles, at SKP, SKS and SKV, are at a frequency of 5·25 Mc/s ± the doppler compensating frequency variation up to 500c/s, being set in manually by the radar operator adjusting the WIND SPEED and WIND DIRECTION controls at the Doppler control desk. The fourth input, corresponding to compensation within the centre circle at SKL, is at a fixed frequency of 5·25 Mc/s plus four times the pulse recurrence frequency.

8. The three switching inputs are accepted at sockets SKN, SKR and SKU and consist of positive-going rectangular switching waveforms of approximately 30V amplitude from the area switching panel M1 (*Chap.* 7). These switching waveforms determine which one of the four frequency inputs is selected.

Output (*rectangle switching*)

9. The output at SKX and SKY consists of the amplified signal selected by the diode switches from the four signal inputs. It is passed to one of the frequency mixer stages M1 in the i.f. cabinet.

Circuit description

10. Three identical pairs of diode switches, each pair controlled by a separate switching waveform, provide the means of selecting one of four Doppler compensating signals. The switch pairs are series-connected so that the signal passage in one pair is closed when a subsequent pair is open to its own input. The selected reference signal is amplified and passed to sockets SKX and SKY.

11. The following description refers to the first-mentioned application of the unit and the action of a typical switch pair, V2-V3-V4 and V6-V7-V8, will be considered.

Output due to input at SKL or SKM

12. With no switching waveform applied at SKN (*fig.* 3), the d.c. condition is that V4 is conducting since it is in series with R4 in the +250V line and R6 in the −250V line. This tends to produce a potential of approximately −100V at V4-V3-V2 junction which causes V2 to conduct, its anode being at approximately −4V set by the potential divider R2-R3. With V2 conducting the negative potential at the junction of the three diodes is reduced to approximately −6V, and V3 remains cut-off. V2 and V4 will therefore present a low impedance to the reference signal input at SKL, providing the signal amplitude is less than the d.c. potential on the diodes.

13. Capacitors C1 and C6 isolate the d.c. condition of the diode switch from the input socket SKL and the second switching stage, V9-V10-V11, respectively.

14. Similarly, with no switching inputs at SKR and SKU (*fig.* 6) the diodes V9 and V11 also V16 and V18 will present low impedances to the reference signal at SKL. Under these conditions the fixed reference frequency input will be fed (via the impedance matching transformer L4) to the grid of the tuned amplifier stage V24. Diode V23 functions as an amplitude limiter and the output from the anode of V24 is passed via SKY to the mixer unit.

15. With no switching input at SKN, the diodes V6 and V7 are non-conducting and present a high impedance to the reference signal input from SKP, whereas a relatively low impedance path for this input is offered through R10 to earth. The d.c. condition is that V8 is conducting, it being in series with R7 in the −250V line to hold its cathode (at junction V6-V7-V8) slightly below earth potential. Diode V6 is therefore cut-off by the positive voltage at its cathode derived from the potential divider R9-R10 across the +250V supply. Similarly, V7 is cut-off due to its anode being returned via R6 to the −250V line.

16. With no switching inputs at SKR and SKU the crystal diode switches V13-V14-V15 and V20-V21-V22 will be in a similar condition to the switch V6-V7-V8.

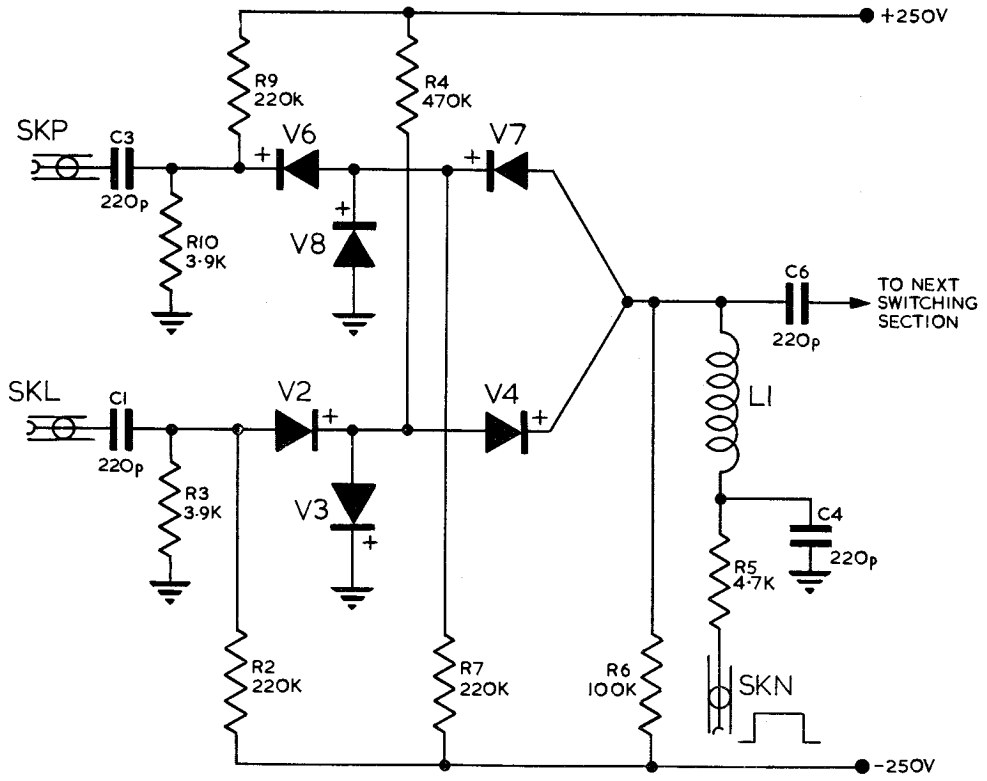


Fig. 3. Diode switch: simplified circuit

Switching action

17. The arrival of a positive-going switching waveform of approximately 30V amplitude at SKN (*fig.* 3) indicates the presence of a rectangle on the display, and causes diode V4 to be cut off. The junction V2-V4 immediately rises to earth potential due to the conduction of V3 so that V2, the anode potential of which is determined by the divider chain R2-R3 across the −250V supply, is also cut off. The anode of V7 is also made positive with respect to earth so that it conducts, the junction of V6 and V7 rises to above earth potential and V8 is cut off, thus causing V6 to conduct. The conditions of the two switches are therefore reversed so that the input at SKL is terminated by R3 whereas the input at SKP is fed via C6 to the next switching section and thence (in the absence of switching inputs at SKR and SKU) to the output stage V24.

18. With a switching input at SKR and no switching input at SKU, switch V13-V14-V15 will operate to connect the reference signal input at SKS to the output stage whereas switch V9-V10-V11 will be closed with the output from the first switch section terminated by R12.

19. Similarly, with a switching input at SKU, the input from SKV will be connected via switch V20-V21-V22 to the output stage with the output from the second switch section terminated by R21.

20. Thus, with overlapping rectangles, precedence will be preserved in the routing of Doppler information to the overlapping portions. If, for instance, rectangles two and three overlap, the Doppler vector for rectangle two only (reference input via SKS) will be routed to the mixer circuits. If all three rectangles mutually overlap, the Doppler vector for rectangle one only (reference input via SKV), will be passed to the mixer circuits.

21. The inputs from the area switching panel at SKN, SKR and SKU are decoupled by chokes L1, L2, L3 in conjunction with R5, R14, R23 and capacitors C4, C8 and C12.

Monitoring points

22. Metering sockets SKC, SKE, SKG, SKJ and SKK are provided for the checking of reference frequency inputs and output. Each monitoring point is connected to the common point of a diode, a 10 kilohm resistor and a 22 picofarad capacitor (e.g. V1, R1 and C2) to provide a d.c. output which may be checked with a multimeter 1 or similar instrument.

23. The switching waveforms fed in at SKN, SKR and SKU may be monitored by connecting an oscilloscope to test sockets SKD, SKF and SKH respectively. The waveforms to be expected at these points are indicated in Fig. 5.

24. The waveforms monitored at these test points on the first switch unit each correspond with one of the rectangular switching waveforms originating in one of the three pulse generators (rectangle) M11. They are positive-going square waves, of 30V amplitude, the leading and trailing edges of which vary in time as the p.p.i. trace rotates.

25. Fed to the second switch unit is only one switching waveform, from the pulse generator (switching) M7. This may be monitored at SKH. The waveform is a positive-going square wave of 30V amplitude. The duration of the waveform is determined by the setting of RV2, ADJ RANGE (LOCAL) potentiometer on the pulse generator M7 and is of the order of 480 μs.

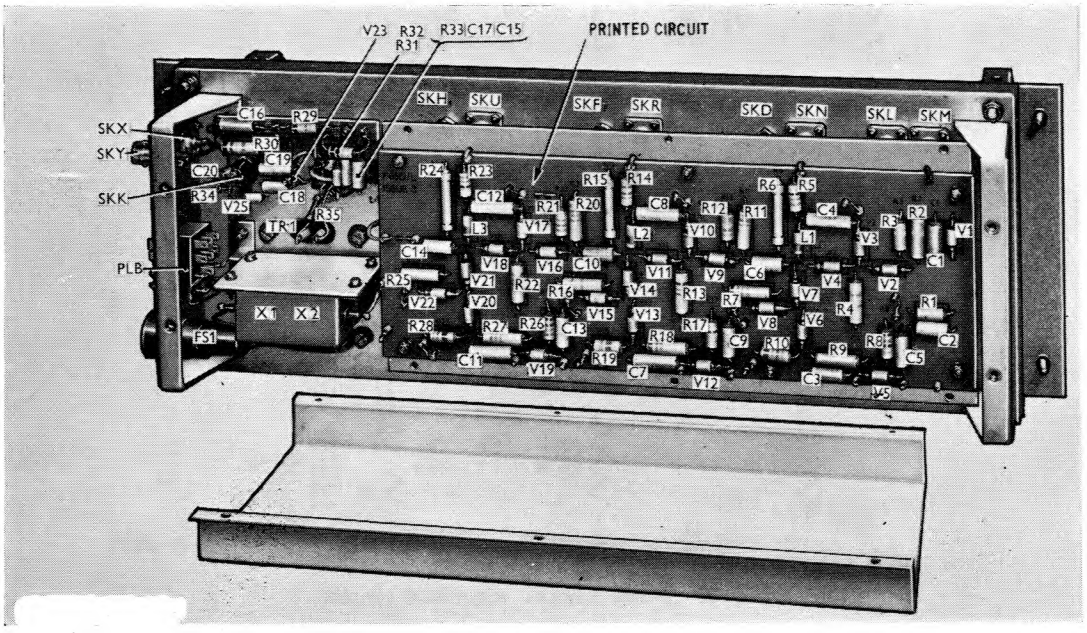


Fig. 4. Switch, electronic (ref. freq.) M4: rear view

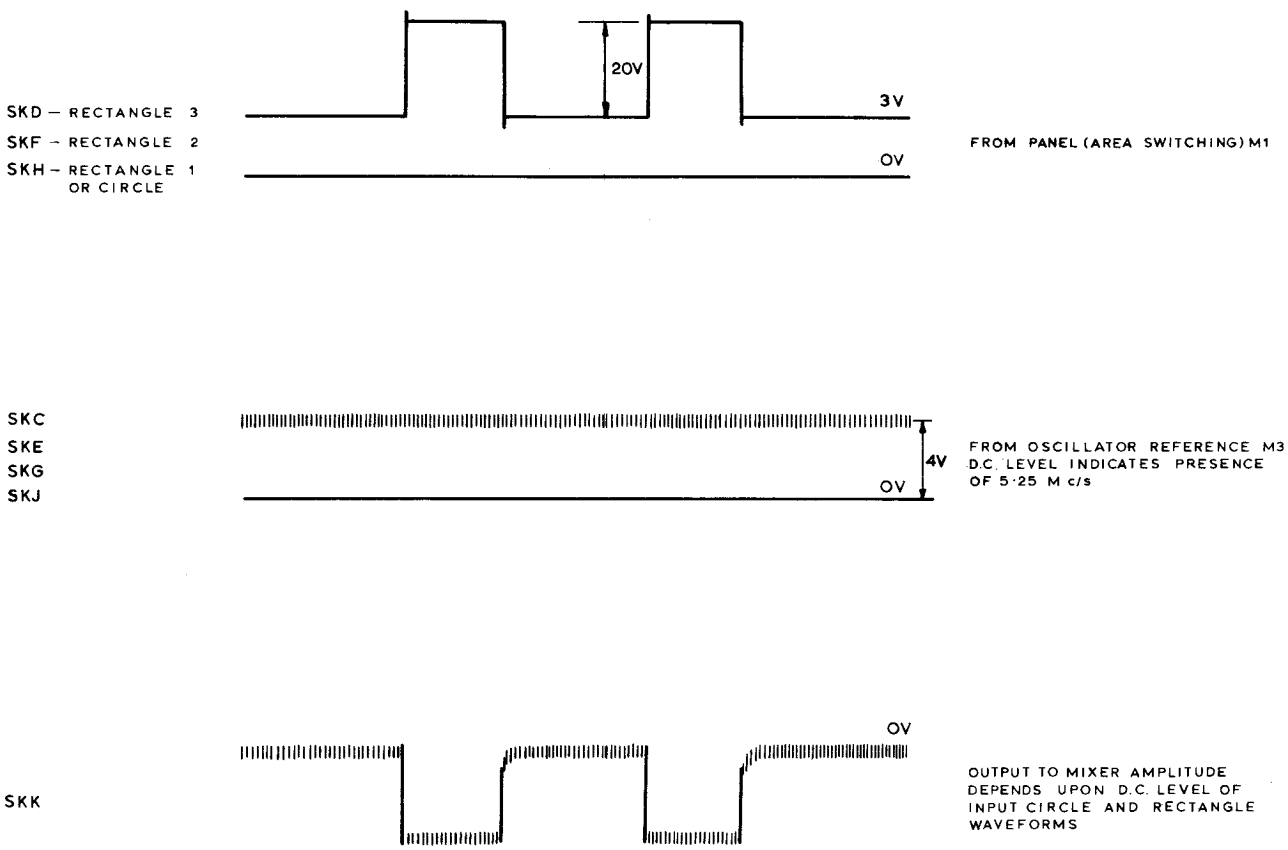


Fig.5 Waveforms at monitor points

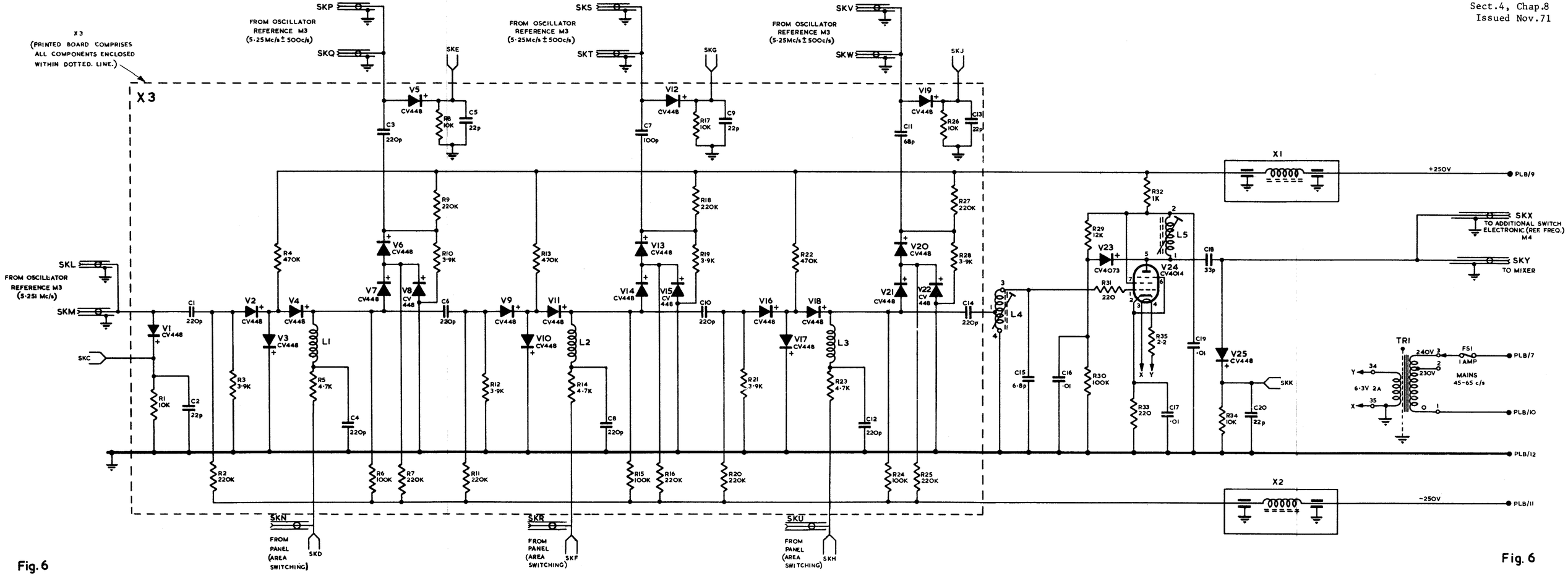


Fig. 6

Switch, electronic (ref. freq.) M4: circuit

Fig. 6

Appendix 1

RECOMMENDED METHODS OF SERVICING PRINTED WIRING BOARDS

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

Introduction

1. Printed wiring boards are made of a laminated material with a thin sheet of copper bonded to one side. The conductor pattern is formed by an etching process. Component leads are threaded through holes punched in the boards and the ends of the leads are normally bent over against ' pads ' on the copper conductors. The completed assembly is then soldered and a protective coating applied.

Tools and materials required for servicing

2. The following tools and materials should be available :—

(1) A small soldering iron with a bit diameter of approximately $\frac{3}{16}$ in. and a working temperature rather above the normal 250°C. A suitable tool is the Precision Iron, Model C240, 230–240 volts, 15 watts, with the No. 4 standard bit, made by A.N.T.E.X. Ltd., 3 Tower Hill, London, E.C.3.

(2) 22 SWG resin cored 60/40 solder. Additional flux must not be used.

(3) A pair of small side-cutters.

(4) A pair of small snipe-nosed instrument pliers.

(5) A small stiff-bristled brush such as the Post Office type brush, fitch, paint, No. 7, round.

(6) A small-bladed knife, e.g. a penknife.

(7) An epoxy resin repair kit, e.g. the Araldite two-tube pack.

Repair procedure

3. It is recommended that the board be removed from the equipment before servicing, in order to facilitate inspection of the underside after repair.

4. Care should be taken to avoid mechanical damage to the board. Where the protective coating has been applied to both the component and the copper side of the board, it will be necessary to apply a sideways force to the component, after freeing the leads, in order to release it from the coating lacquer.

5. Avoid excessive heating of the joint, as this will reduce the strength of the bonding adhesive and damage more than the necessary minimum area of protective varnish.

6. Mechanical damage to the copper foil is most likely to be caused by stress on the component leads from the component side of the board.

7. In those methods where the soldering iron is applied to the copper ' pad ', the following points should be noted :—

(1) It is not necessary to remove the protective varnish beforehand.

(2) The iron should only be applied to the pad for the absolute minimum of time necessary to melt the solder.

(3) Local repair of the damaged protective coating must be carried out immediately after the final soldering and cleaning operations, to prevent the ingress of moisture.

8. There are three recommended methods for the replacement of defective components, the suitability of each being determined by the circumstances.

Method 1

9. This is the recommended method for axial lead components, and certain others, when it is possible to leave a sufficient length of wire attached to the board.

(1) Clip off the leads close to the component (*fig.* 1*a*). In the case of certain non-axial lead components it may be necessary to break the component in the middle (*fig.* 1*b and* 1*c*). Remove the component.

(2) Straighten the wires left on the board, by bending away from the board, until they are perpendicular to it (*fig.* 1*d*).

(3) Bend semicircular hooks on the replacement component leads, to correspond with the spacing of the old component wires, slide on to the old leads and solder into position, ensuring that the component lies flat on the board (*fig.* 2*b*). For radial lead components, form the leads as fig. 1a and attach as shown in fig. 2c.

Note . . .

Where insulating spacers have been used to keep a component, such as a wirewound resistor, raised from the board, they should be retained as shown in fig. 2d to maintain adequate ventilation.

Method 2

10. This is the recommended procedure when it is desired to retain, as far as possible, the original appearance of the board. It is preferable, however, that it should not be used unless the importance of appearance overrides the obvious advantage of avoiding application of heat direct to the copper pads.

(1) Proceed as in method 1 until the old component leads are perpendicular to the board.

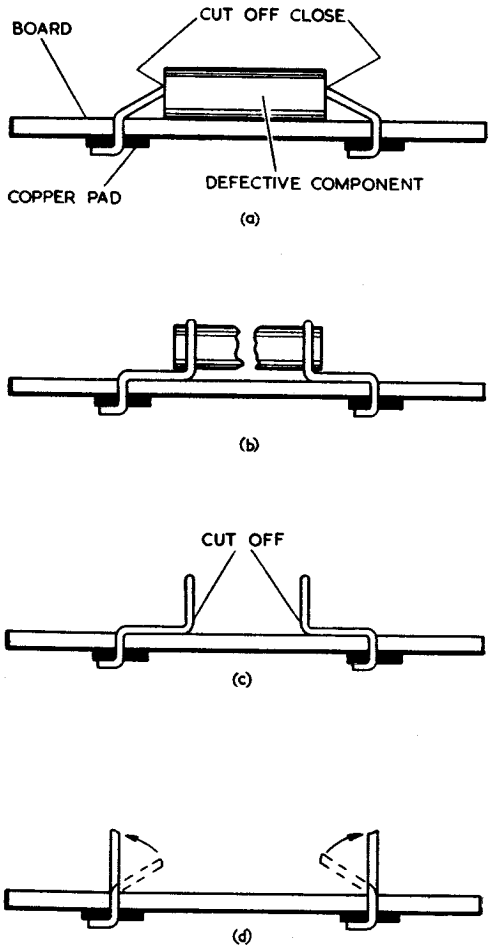


Fig. 1. Removing component : method 1

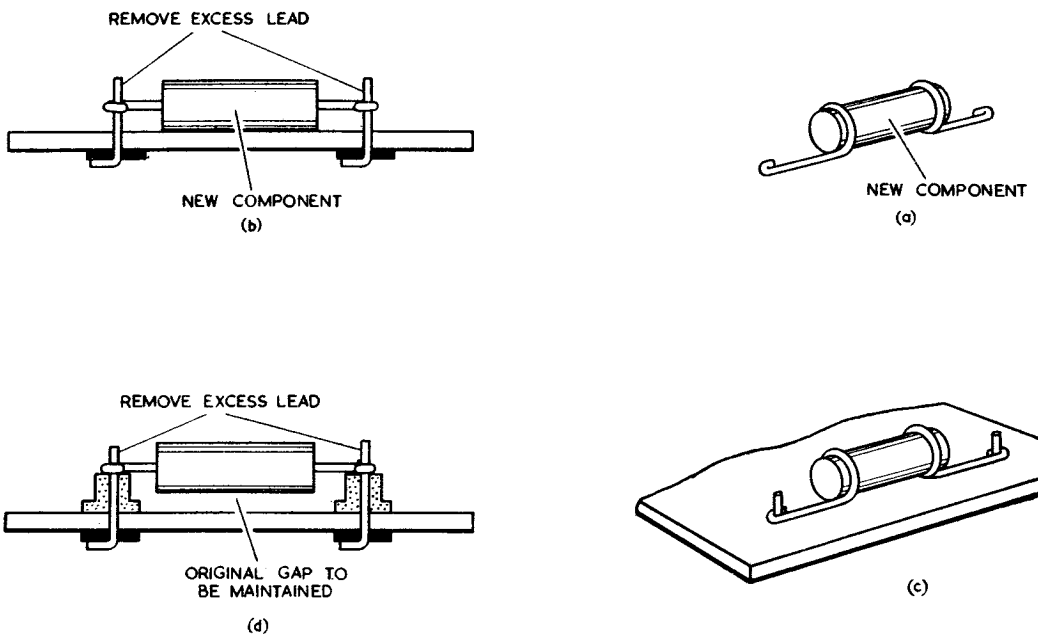


Fig. 2. Fitting new component : method 1

(2) Clip off the leads close to the component side of the board.

(3) Melt the soldered connection by the brief application of a hot iron and flick the board rapidly so that the lead stub is ejected, together with the solder in the hole. Check that no solder remains in the hole. Care should be taken to avoid physical damage to the board when flicking.

(4) Form the leads of the replacement components to the required shape (*fig.* 3*a*).

(5) Fit the component and, after ensuring that it is lying flat on the board, clench the lead ends by gripping with the pliers, $\frac{1}{8}$ in. from the board, and pressing sideways, not allowing the pliers to twist, so that the sides of both jaws remain parallel to the board throughout the movement (*fig.* 3*b*).

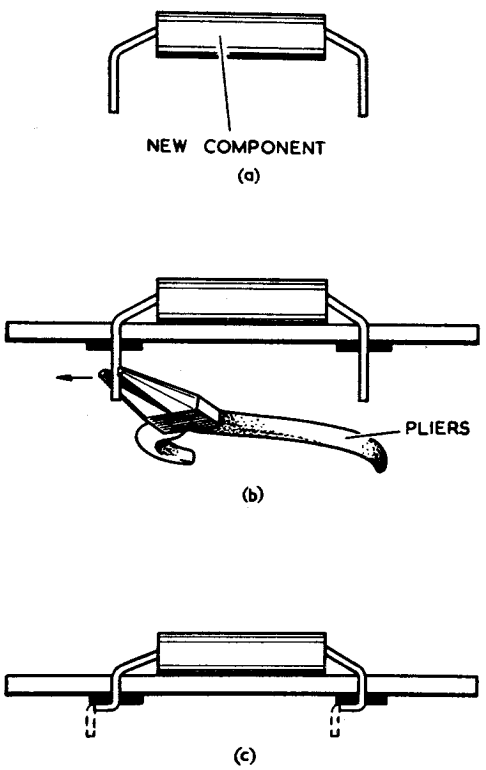


Fig. 3. Fitting new component . method 2

(6) Cut off leads at the edge of the pad between the two right-angle bends (*fig.* 3*c*).

(7) Resolder the joint using only resin-cored solder and a hot iron. The iron should be applied for the least possible time consistent with obtaining a good soldered joint.

(8) Remove the excess resin and any contaminant from around the joints by wiping with a degreasing solvent, e.g. trichlorethylene. Allow excess solvent to evaporate.

(9) Mix the components of the epoxy resin, according to the maker's instructions and apply to the areas from which varnish has been removed during soldering, taking care to overlap the old varnish. The new resin will cure at room temperature but, if it is desired to achieve a ' tack free ' state rapidly, the cure may be accelerated by raising the temperature of the board to 50°C.

Note . . .

Operations (8) *and* (9) *should follow* (7) *as rapidly as possible. If resealing is appreciably delayed, it is strongly recommended that the board be heated to* 50°C *and maintained at this temperature for one hour before resealing.*

Method 3

11. This method is recommended where access to the leads on the component side of the board is denied and where destruction of the component to gain access is impracticable.

(1) Apply a hot iron to the soldered connections, one at a time, and as soon as the solder has melted, remove as much excess as possible with the stiff brush.

(2) With the excess solder removed, apply the soldering iron to the clenched component lead end and, as the solder melts, introduce the blade of the small penknife under the clenched end, removing the soldering iron immediately this is achieved. Straighten the clenched end by twisting the knife in such a manner that the thin edge remains both on the board and touching the lead where it leaves the hole (*fig.* 4).

(3) After repeating operation (2) on all the leads of the component, carefully examine the leads where they enter the board, to ensure that

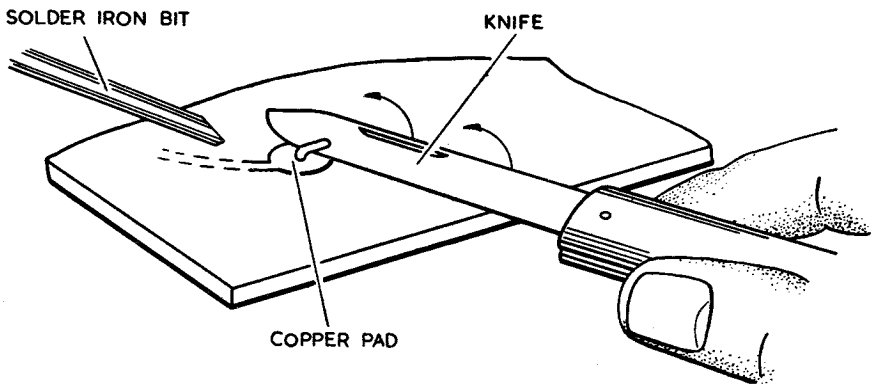


Fig. 4. Removing component : method 3

they are not still attached to the pads. In those cases where they are attached they must be freed by re-applying the iron to the wire and, after the solder has melted, moving the wire to and fro in the hole until the solder has set.

(4) When all the leads are freed the component may be withdrawn and a new one inserted, pre-forming the leads where necessary.

(5) After insertion the ends are clenched, trimmed and soldered and the board resealed as in para. 10 (8) and (9).

Note 1 . . .

Certain components, such as valve bases, may be fitted with tags which it is impracticable to clench over because of risk of damage to the board. Where these components have to be replaced, operation (2) *is omitted during the removal and, correspondingly, the re-clenching operation is not carried out when fitting the new component.*

Note 2 . . .

In operation (2) *the knife must not be inserted without first melting the solder, or damage to the copper pad may result. Similarly in* (4) *the component must not be withdrawn until all the leads are freed as in* (3).

Test and inspection

Note . . .

At no time, either while locating a faulty component or while testing following a repair, should any lead be attached to the copper side of the board.

12. Repairs should be inspected for dry joints. When methods 2 or 3 have been used the amount and shape of solder should be similar to the original connections on the board, and it should be possible to see the outline of the component leads.

13. Repairs should be inspected to ensure that all varnish displaced during the servicing operations has been made good and that a sufficient overlap of varnish has been allowed to effect a complete seal.

Chapter 9

OSCILLATOR (REFERENCE) M3

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

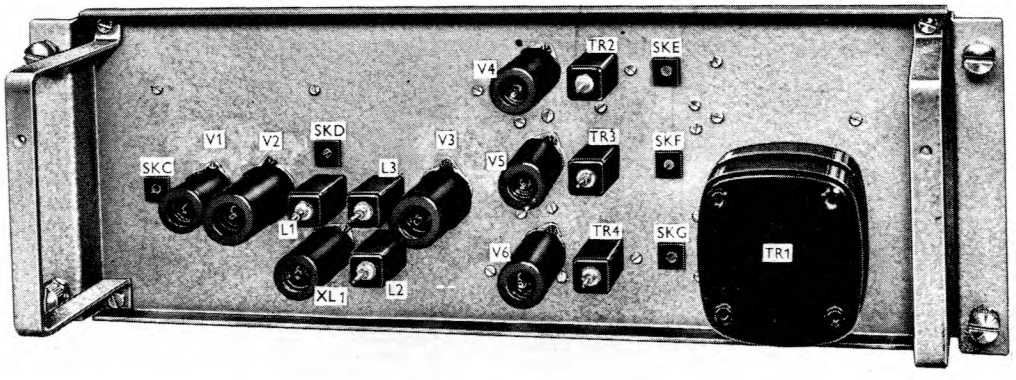


Fig. 1. Oscillator (reference) M3 : front view

Introduction

1. Four oscillator (reference) M3 units (*fig.* 1 and 3) are used in the signal processing system, all of them being mounted in frame 3 of the doppler cabinet. One of the oscillators is of fixed frequency, producing an output at 5·251 Mc/s. The remaining three oscillators produce outputs at 5·25 Mc/s, variable by up to ±500 c/s.

2. The purpose of the reference oscillators is to provide doppler compensated reference frequencies to the mixer circuits where they are used for the cancellation of moving clutter in the three rectangular areas. The use of three variable frequency oscillators enables three values of doppler compensation to be used successively, each in a different rectangle.

Performance characteristics

Input

3. When the unit is used as a variable frequency oscillator, the input at SKH consists of a d.c. voltage fluctuating between maximum limits of $\pm 2 \cdot 5$V. This input is derived from the control, electrical frequency M1 (*Chap.* 11) associated with the particular reference oscillator. In the fixed frequency application of the unit, SKH is fitted with a 75-ohm termination.

Outputs

4. Three identical outputs are provided by the unit from sockets SKJ, SKK and SKL, consisting in the case of the variable frequency oscillators of a sine wave at 5·25 Mc/s, variable from the nominal by ± 500 c/s, and in the case of the fixed frequency oscillator of a sine wave at 5·251 Mc/s. The output amplitude in all cases is $5\text{V} \pm 1\text{V}$ peak into an impedance of 75 ohms. The output from SKL is not used in the present application of the unit.

Brief circuit description

5. A functional schematic diagram is given in fig. 2. The circuit consists basically of a crystal controlled oscillator, V3, operating at 5·251 or 5·25 Mc/s, depending on the application. The required ± 500 c/s variation of the oscillator frequency is achieved by the use of a reactance valve V2, connected in parallel with the oscillator inductance. Control of the reactance of V2 is effected by a d.c. potential fluctuating between $\pm 2 \cdot 5$V, derived from the control, electrical frequency M1. To obtain the fixed frequency condition required by one of the four reference oscillators used in the system, the d.c. control voltage is replaced by a 75-ohm termination.

6. The unit produces three outputs at the crystal frequency from three buffer amplifier stages. In the variable frequency application of the unit one of these outputs is not used ; of the remaining two, one is fed to the switch, electronic (reference frequency) M4 (*Chap.* 8) associated with the particular oscillator, where it is selected for application to the appropriate rectangle. The remaining output is fed back to the associated control, electrical frequency, where it is used for frequency stabilizing purposes.

Circuit description (*fig.* 4)

Power supplies

7. The +250V h.t. supply required by the unit enters at PLB/9 and PLB/12 (earth), and is filtered by the network X1 to prevent feedback of r.f. to the h.t. line. The 6·3V heater supply required by V1 to V6 is supplied from the secondary winding of TR1, the primary of which receives a 45–65 c/s a.c. mains input from PLB/7 (via FS1), and PLB/10.

Oscillator circuit

8. The oscillator, comprising V3 and its associated circuit, is basically a crystal controlled Hartley oscillator. The shunt capacitance of the crystal, XL1, is tuned out by the parallel-connected inductance L1, and the crystal is coupled to the oscillator inductance L3, via C7. An anti-parasitic circuit, formed by R17, C9 and L2, is included in the oscillatory circuit, tuning to the crystal frequency being effected by the dust-iron core of L2. In the event of the oscillator attempting to operate at the wrong frequency, the impedance of the tuned circuit L2 and C9 will decrease, thereby damping L3 and preventing the circuit from oscillating.

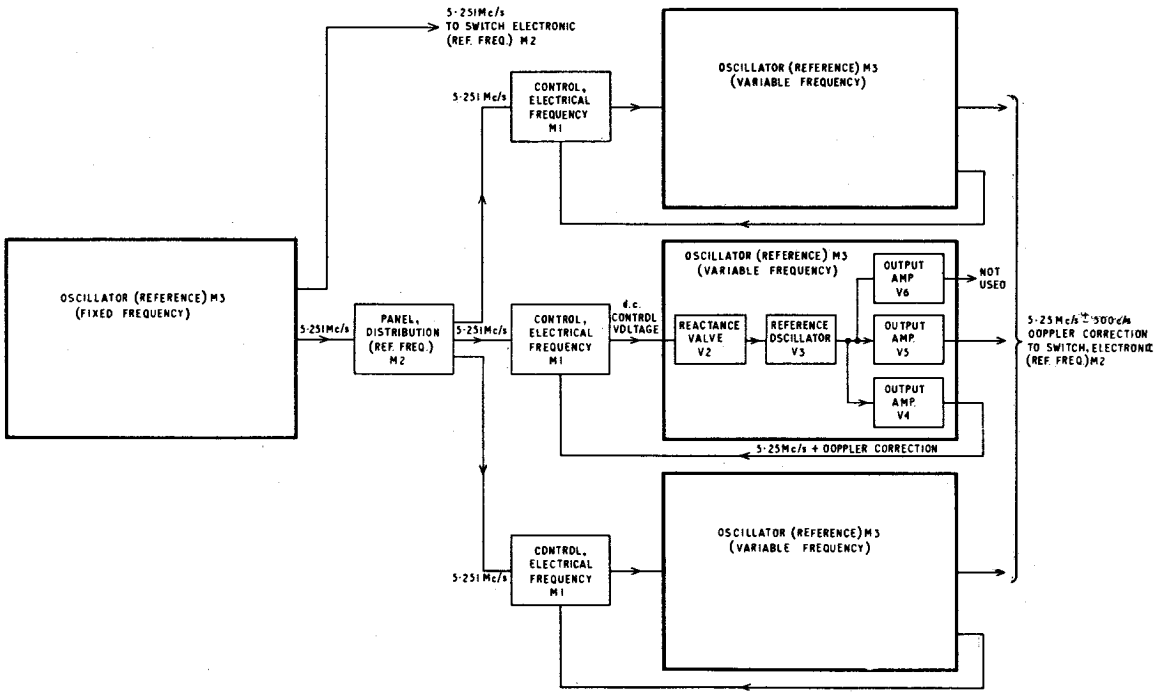


Fig. 2. Functional schematic

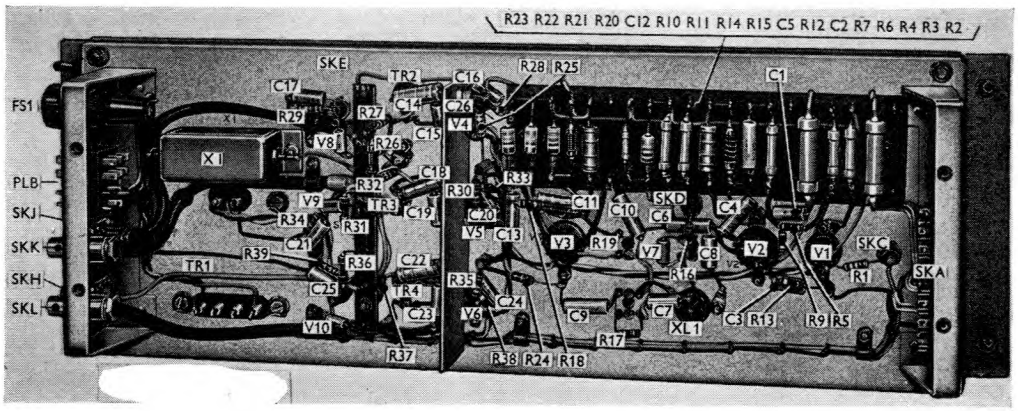


Fig. 3. Oscillator (reference) M3 : rear view

Variable reactance circuit

9. The required variation of oscillator frequency is obtained by the use of a variable reactance circuit, comprising V2 connected in parallel with the oscillator inductance L3. V2 is a variable-mu pentode, connected in such a way that when an alternating voltage is applied between anode and cathode, the resultant anode current is in quadrature with the anode-cathode voltage. Under these circumstances the valve behaves like an inductive reactance, the equivalent inductance being given by the equation $L = \frac{C1 \times R7}{G_m}$. C2 is a blocking capacitor and its value is too large to affect the phase shift network formed by C1 and R7.

10. Variation of the mutual conductance of V2, and hence the equivalent inductance of the circuit, is effected by the d.c. control voltage fed in at SKH from the associated control, electrical frequency. The reactance circuit is capable of accepting an input control voltage the maximum fluctuation of which is $\pm 3{\cdot}5$V. These limits are determined in the positive direction by V1, which is biased at approximately $+3{\cdot}5$V by the divider network R2, R3, and in the negative direction by the grid base of V2, which cuts off at approximately $-3{\cdot}5$V. In practice however, the controlling voltage has a maximum variation of $\pm 2{\cdot}5$V, and this variation in terms of oscillator frequency represents a frequency variation of ± 500 c/s. In the case of the fixed frequency reference oscillator, SKH is terminated in 75 ohms.

Output stages

11. The output from the anode of V3 is fed via C13 to the grids of the three buffer amplifier output stages, V4, V5 and V6. The output, attenuated by R18, is also applied as negative feedback to the grid of V3. Since the three output stages are identical in operation, only the stage associated with V4 will be described.

12. The output of V4 is developed across the primary of TR2 which, with C15, forms a tuned circuit at 5·25 Mc/s. The secondary of TR2 produces an output at an impedance of 75 ohms and this is routed to SKJ, at which the final amplitude is approximately 10V peak-to-peak. A detector circuit comprising V8, C17 and R29 provides facilities at SKE for monitoring the level of the output signal.

13. Similar outputs to that at SKJ are obtained at SKK and SKL, these outputs being produced by the amplifier stages V5 and V6 respectively.

Multimeter readings

14. With the multimeter type 100 connected to SKA via a plug-to-socket adaptor, the readings obtained should be as given in Table 1.

Monitoring points

15. Test sockets are provided at SKC to SKG for use with a monitoring oscilloscope or meter. The voltages obtainable at these points are shown in Table 2.

TABLE 1

Multimeter readings

Multimeter switch position	Stage monitored	Measured across	Reading	Tolerance
A	V2	R10	0·60	±0·10
B	V3	R20	0·36	±0·10
C	V4	R26	0·40	±0·08
D	V5	R31	0·40	±0·08
E	V6	R36	0·40	±0·08

TABLE 2

Monitor point voltages

Monitor socket	Reading	Tolerance	Remarks
SKC	±2·5V	—	Dependent upon instantaneous input voltage.
SKD	Minimum μA	—	Dependent upon tuning of L2 and L3.
SKE	5V	±1V	
SKF	5V	±1V	
SKG	5V	±1V	

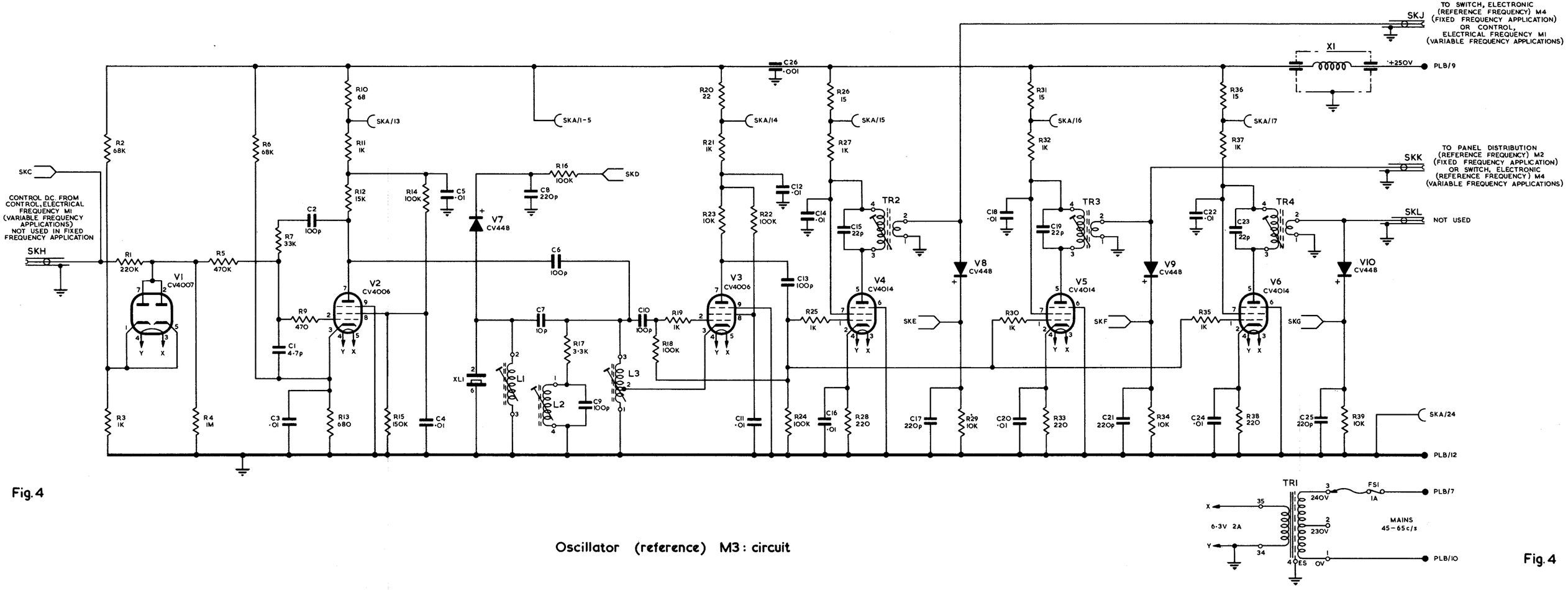


Fig.4

Oscillator (reference) M3 : circuit

Fig.4

Chapter 10

PANEL DISTRIBUTION (REFERENCE FREQUENCY) M2

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

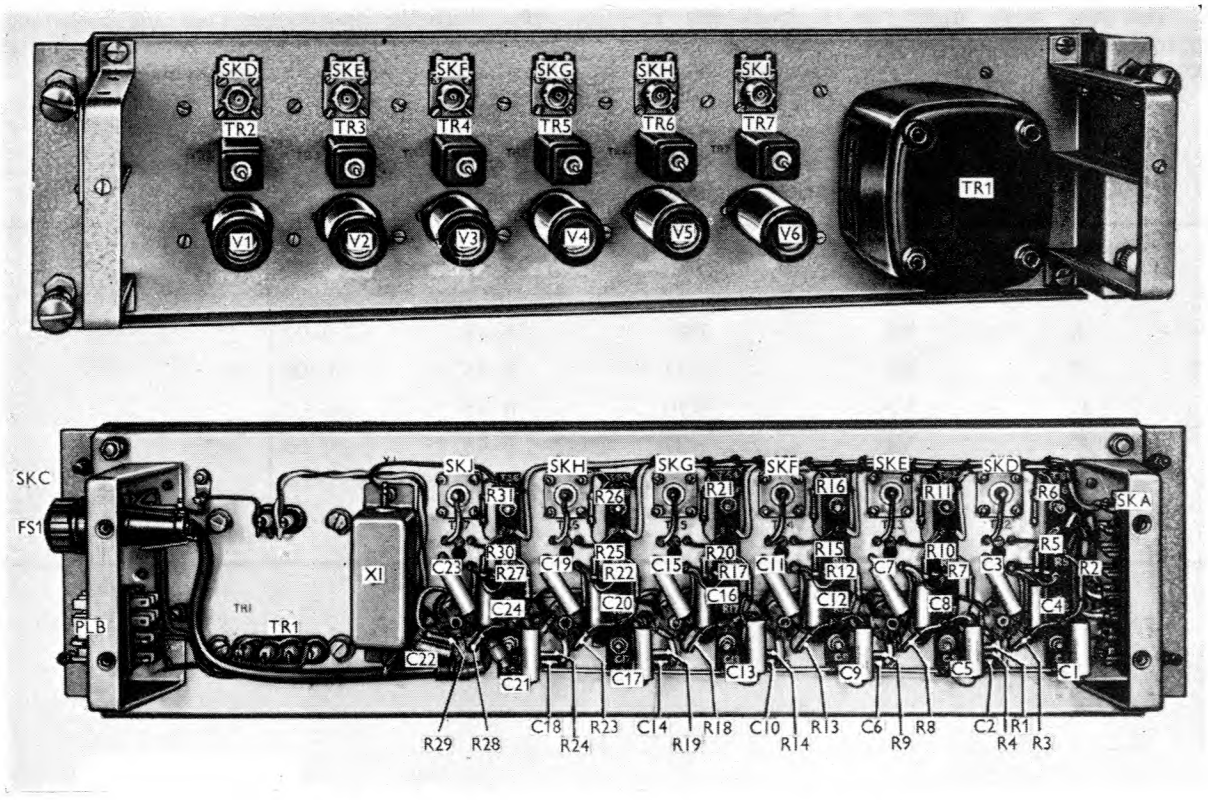


Fig. 1. Panel, distribution (ref. freq.) M2 : front and rear views

Introduction

1. From a c.w. input at 5·251 Mc/s supplied by the fixed reference oscillator M3, the distribution panel (reference frequency) M2 provides six independent c.w. outputs by means of six tuned buffer amplifier stages. The panel is mounted in frame 3 of the doppler cabinet.

2. Three outputs are applied to the three frequency control panels M1, and are used in frequency discriminator circuits which form part of feedback loops from the variable frequency oscillator units in the doppler compensation system (*Sect.* 1, *Chap.* 5).

3. Two outputs are applied to the two frequency mixer stages feeding the cancellation channel demodulators (*Sect.* 1, *Chap.* 3). A sixth output from the distribution panel is not used.

Performance characteristics

4. The panel receives a 5·251 Mc/s c.w. input at socket SKC, the level being 0·5V r.m.s., from the fixed reference oscillator M3 (*Chap.* 9). Six identical c.w. outputs at this same frequency are provided, of which those from sockets SKD, SKE and SKF are fed to each of the three frequency control panels M1, and those from SKG and SKH to each of two frequency mixer stages M1 ; the sixth output, from SKJ, is not used. Each stage has a gain of unity at 5·251 Mc/s, with a bandwidth of 125 kc/s at 3dB points.

Circuit description

5. Heater voltages for the valves are supplied from TR1, the 240V a.c. primary supply for the transformer being received via the 1 ampere fuse FS1 from plug PLB poles 7 and 10. The supply is controlled by the main system switch which controls the mains supply to all units of the complete system.

6. The +250V supply from the +250V voltage regulator appears across PLB poles 9 (+250V) and 12 (earth).

7. The sine wave input, at a frequency of approximately 5·251 Mc/s, is brought in at socket SKC and from there it is fed via capacitors C1, C5, C9, C13, C17 and C21 to six separate single buffer amplifier stages. The input is terminated in 75 ohms by R1. The six buffer stages are identical and therefore only the stage associated with V1 will be described.

8. The input is fed via C1 and the grid stopper resistor R3 to the grid of V1, R2 being a grid leak. The output in the anode circuit is developed across the primary of TR2 which is tuned for maximum output by C3 and by adjustment of the transformer core. An unbalanced output is taken from the secondary of TR2 via socket SKD. The component values in the circuit are such that the stage gain is approximately unity and a bandwidth of 125 kc/s is obtained between 3dB points under normal operating conditions.

9. Identical outputs to that at SKD are obtained at sockets SKE, SKF, SKG, SKH and SKJ. Decoupling is provided for the +250V supply by the filter unit X1, and for individual anode circuits by 1kΩ resistors and ·01μF capacitors in the anode circuits.

Multimeter readings

10. With the multimeter Type 100 connected to socket SKA via the plug-to-socket adaptor the meter readings should be as indicated in Table 1.

TABLE I

Multimeter readings

Multimeter switch position	Valve monitored	Measured across resistor	Meter reading	Tolerance
A	V1	R6	0·45	±0·09
B	V2	R11	0·45	±0·09
C	V3	R16	0·45	±0·09
D	V4	R21	0·45	±0·09
E	V5	R26	0·45	±0·09
F	V6	R31	0·45	±0·09

(20 per cent)

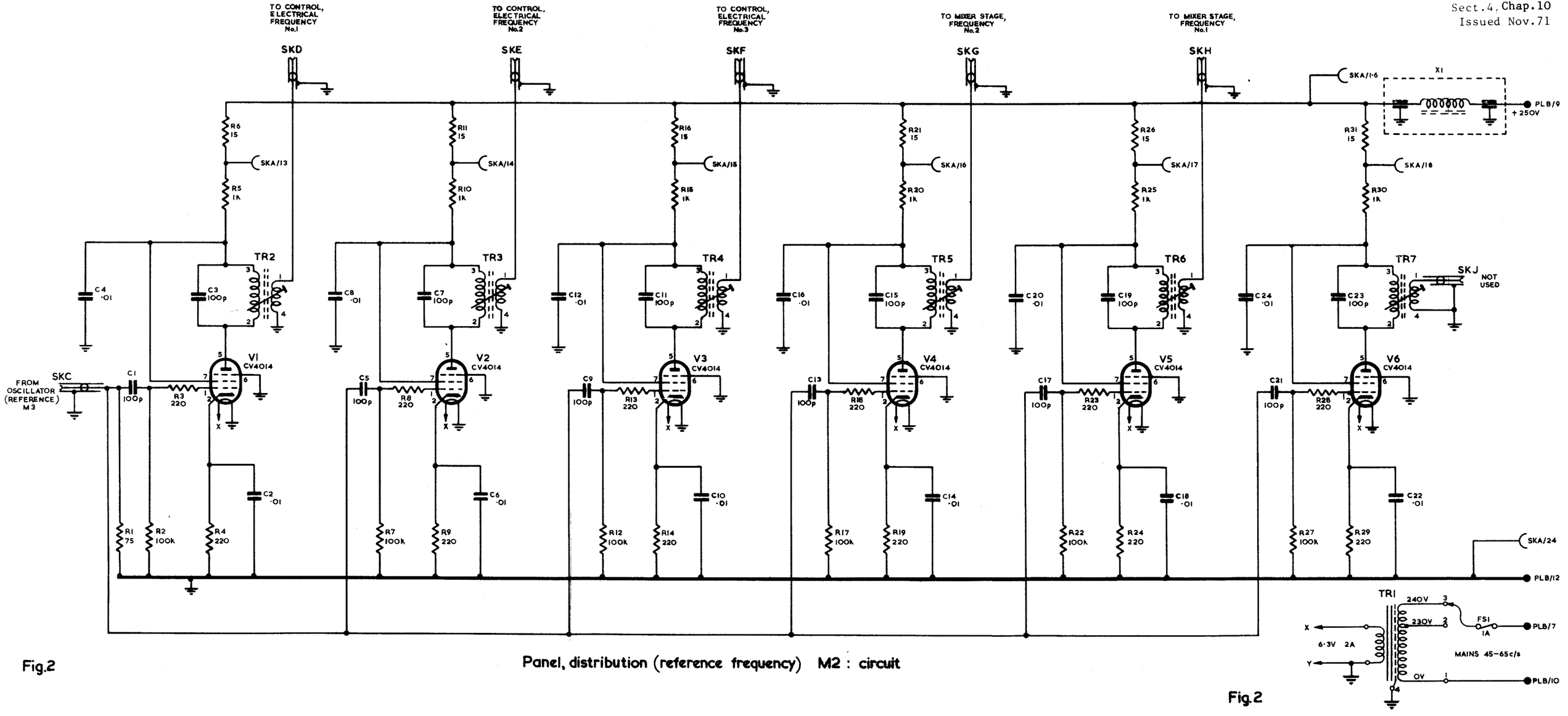


Fig.2

Panel, distribution (reference frequency) M2 : circuit

Fig.2

Chapter 11

CONTROL, ELECTRICAL FREQUENCY M1

LIST OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

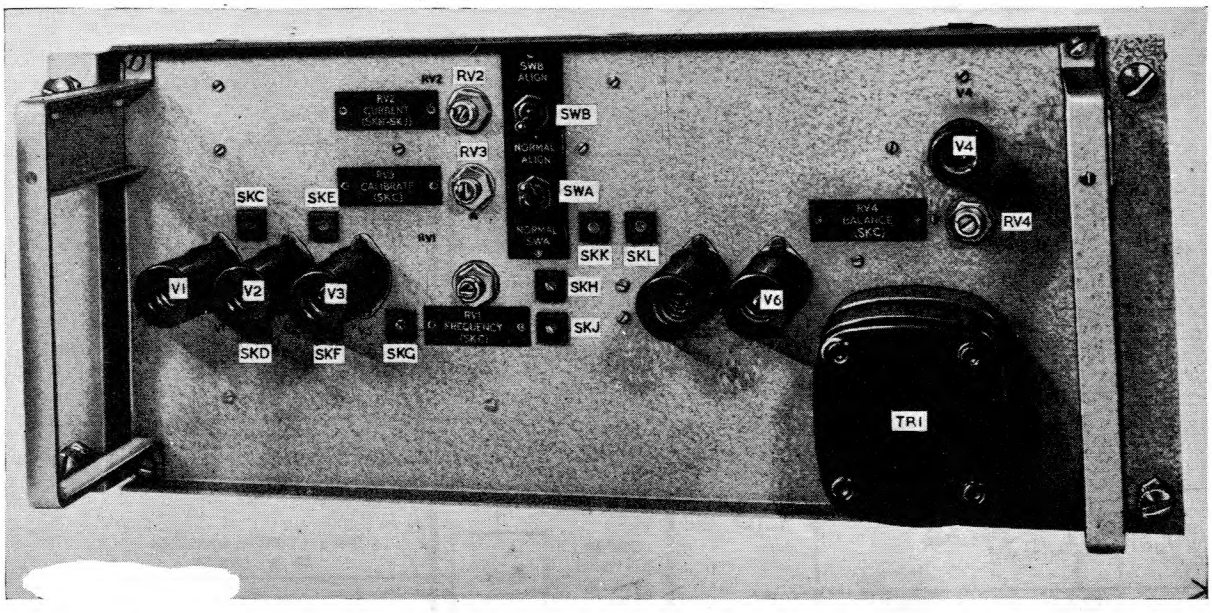


Fig. 1. Control, electrical frequency M1 : front view

Introduction

1. The purpose of the frequency control unit M1 (*figs.* 1 *and* 4) is to produce the d.c. output required to control the frequency of a variable frequency oscillator (*Chap.* 9). Three such units are provided, each associated with one of three frequency oscillators, so that three variable frequencies are available for use in the coherent demodulator (*Sect.* 2, *Chap.* 10) for each cancellation channel. The output from each variable frequency oscillator is selected for use in the appropriate cancellation channel by electronic reference frequency switches (*Chap.* 8) which are themselves controlled by rectangle switching waveforms. By this means the appropriate frequency, incorporating doppler compensation, is applied to the cancellation circuits during the period when the timebase sweep is crossing the rectangle area.

2. The d.c. output from the unit is controlled initially according to the amplitude and phase of the 500c/s input received from a wind speed and direction control unit on the console suite. A second means of control is that in which the unit forms part of a feedback loop so that the required frequency difference between the output of the variable frequency oscillator and that of an identical oscillator with a fixed reference frequency output is maintained. The feedback loop compensates any tendency in either or both oscillators to drift in frequency due to temperature variation or other discrepancies in oscillator performance.

3. A functional block schematic of the system, showing one control unit and one variable oscillator is shown in fig. 2. The rotor of an electrical resolver (*Sect.* 7, *Chap.* 3), which is driven at aerial rotational speed, is fed with a nominal 500c/s supply from the reference signal generator M2 (*Sect.* 3, *Chap.* 11). The output from the stator windings of the resolver is 500c/s (nominal) resolved for aerial rotation and is fed to three wind speed and direction control units on the radar operator's console. The angle of the rotor in the magslip of the wind speed and direction control unit is manually adjusted by a WIND DIRECTION control and the amplitude of the resolved output from the magslip by the WIND SPEED control in order to set up the required doppler compensation.

4. The output from each control unit is used for a separate rectangle area and is applied to the phase-sensitive rectifier circuit in the appropriate electrical frequency control unit. The d.c. output from this circuit controls the frequency of the variable frequency oscillator. The nominal frequency of the oscillator is 5·25 Mc/s, and the output frequency is controlled within the limits of plus and minus 2 × p.r.f. (about 500c/s), requiring a controlling d.c. input of between plus and minus 2·5V.

5. The reference frequency used in subsequent coherent demodulator circuits consists of a nominal frequency of 13·5 Mc/s modified by the doppler correction frequency, the latter being obtained by mixing the output of the variable frequency oscillators with the nominal 5·251 Mc/s (5·25 Mc/s plus 4 × p.r.f.) output from the fixed reference frequency oscillator. It is therefore necessary to provide compensation for frequency drift in both the oscillators so that the correct frequency relationship, according to the amount of doppler compensation in use, exists under all conditions.

6. Frequency stability is achieved by mixing a feedback output from the variable frequency oscillator with the output from the fixed oscillator. The resultant beat frequency is used to produce a d.c. output from a frequency discriminator circuit, the d.c. output being in opposition to any change of frequency in the variable oscillator and thus constituting a form of negative feedback. With no

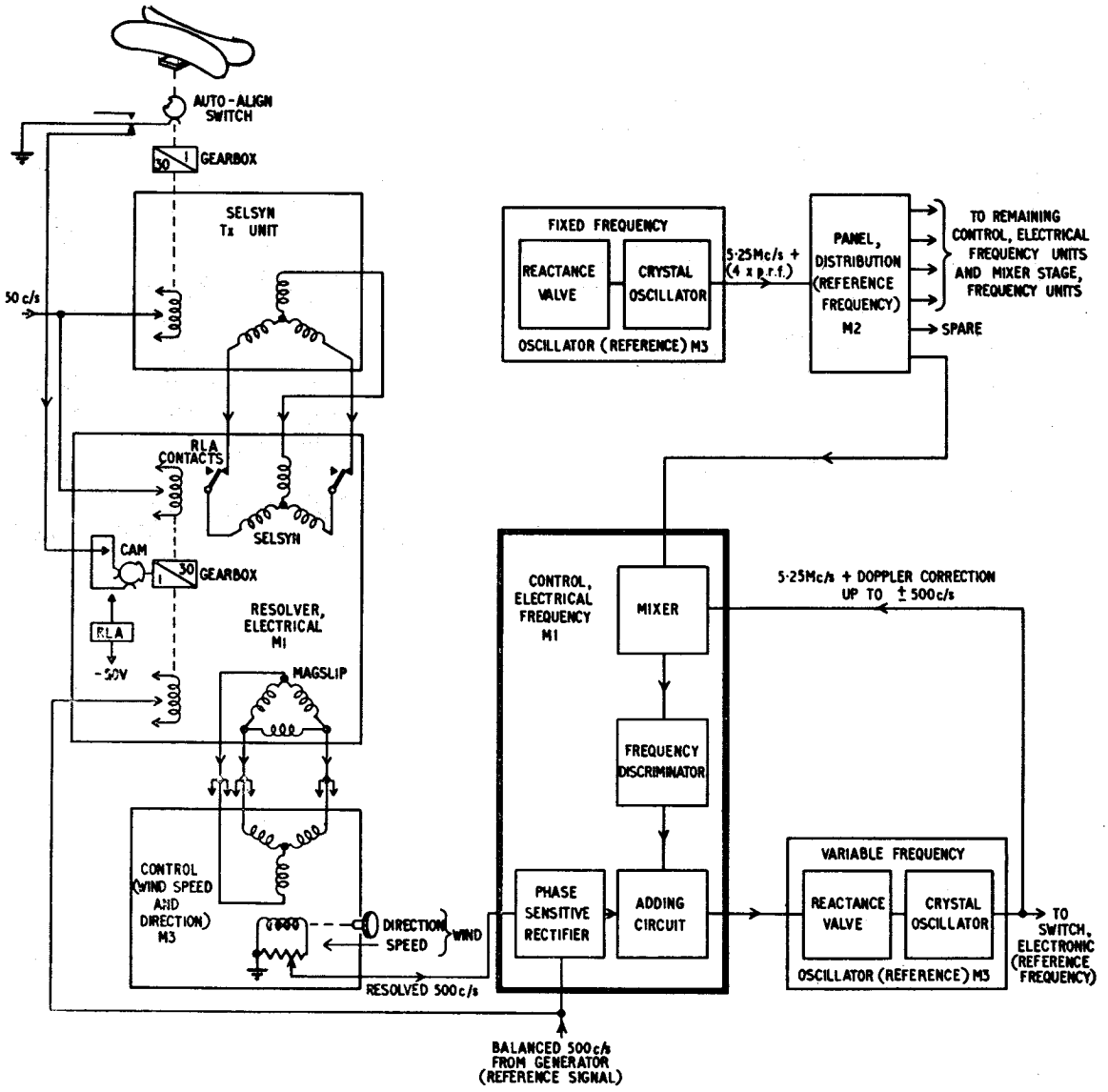


Fig. 2. Functional block schematic

output from the phase-sensitive rectifier circuit (i.e. with no doppler correction) the difference frequency between the fixed and variable oscillators is 4 × p.r.f. (nominally 1 kc/s corresponding to the fourth blind speed) and this difference is maintained should either oscillator drift in frequency. Similarly, the appropriate frequency difference is maintained, in the range 500–1500c/s, according to the degrees of doppler compensation.

7. The three control units, for rectangles 1, 2 and 3, are mounted in the fourth, sixth and eighth positions respectively from the top of frame 3 in the doppler cabinet, each control unit being associated with the reference oscillator immediately beneath it.

Performance characteristics

Inputs

8. A balanced 500c/s input of fixed phase and with an amplitude of 100V peak-to-peak is received across PLB/1 and PLB/3 from the reference signal generator M2 in the cancellation cabinet.

9. An unbalanced, resolved 500c/s input with a maximum amplitude of 36V peak is received at PLB/2 from the appropriate wind speed and direction control unit in the radar operator's console suite.

10. An input at a nominal frequency of 5·25 Mc/s, varying by up to 500c/s about the nominal frequency, is received at socket SKM from the variable frequency oscillator M3. This input has an amplitude of 5V peak.

11. An input at a nominal frequency of 5·251 Mc/s with an amplitude of 5V peak is received at socket SKN from the fixed reference frequency oscillator M3 via the reference frequency distribution panel M2.

Output

12. The output to the variable reference frequency oscillator controlled by the unit is taken from SKP and is a d.c. voltage fluctuating between maximum limits of plus and minus 2·5V.

Brief circuit description

13. The fixed and resolved 500c/s inputs (*fig.* 2) are applied to a phase-sensitive rectifier circuit which produces a d.c. potential of amplitude and polarity according to the phase and amplitude relationship between the two inputs.

14. A further d.c. potential is produced in a frequency discriminator circuit which forms part of a feedback loop from the output of the variable frequency oscillator. The inputs from fixed and variable frequency oscillators are mixed and the difference frequency is selected by a filter circuit for amplification. After amplification the positive half-cycles are clipped to provide an input of negative half-cycles to a long-tailed pair, the anti-phase anode outputs from which are substantiallv square. The square waves are differentiated a. rectified in a full-wave rectifier circuit to provide a mean potential proportional to the number of pulses per second.

15. The outputs from the phase-sensitive rectifier and frequency discriminator circuits are added in a resistive network and amplified in two d.c. coupled long-tailed pairs to produce the controlling d.c. output required for frequency modulation of the variable reference frequency oscillator.

Circuit description

16. Heater voltages for the valves are supplied from TR1, the 240V a.c. primary supply for the transformer being received via FS1 at PLB/7 and PLB/10. The 240V a.c. supply is controlled by the main system switch which controls the mains supply to all units of the complete system.

17. The −250V supply from the power cabinet appears across PLB/11 (−250V) and PLB/12 (earth) and the +250V supply from the +250V regulator across PLB/9 (+250V) and PLB/12 (earth).

Phase-sensitive rectifier

18. The unbalanced input at PLB/2 has its amplitude and phase determined by a magslip resolver in the radar operator's console suite, the rotor of the

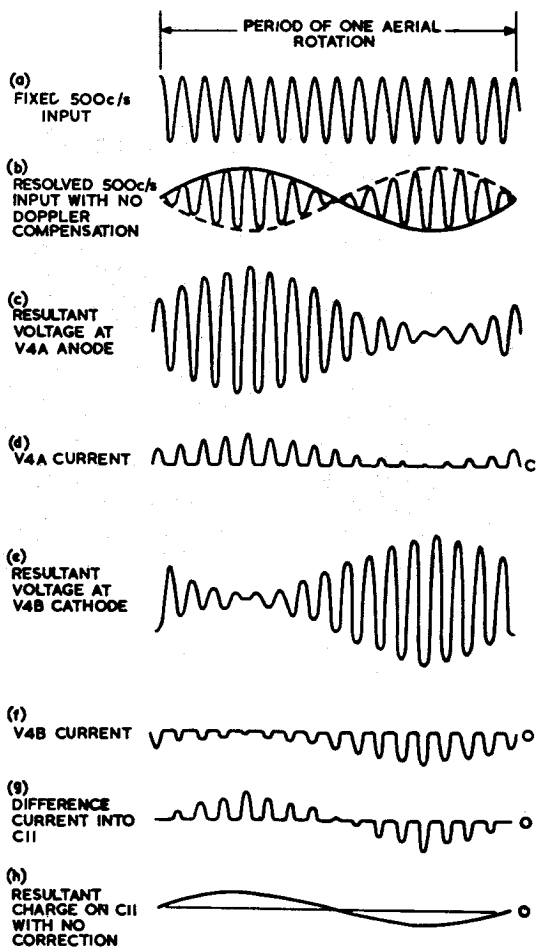


Fig. 3. Theoretical waveforms

magslip being manually set to apply correction for wind direction and a potentiometer, across the output from the rotor, for wind speed. The unbalanced 500c/s input is therefore resolved for aerial rotation, its phase and amplitude being set so that the appropriate doppler correction frequency can be applied. The balanced 500c/s input, with fixed amplitude and phase, is received at PLB/1 and PLB/3. The waveforms are illustrated in fig. 3(a) and (b).

19. The balanced 500c/s input is applied across the resistor chain R18, R24, R26, R27 so that current flows through the resistor chain for half a cycle from R18 to R27 and in the reverse direction for the other half cycle. With no input at PLB/2, i.e. with the WIND SPEED potentiometer set to zero, the diodes V4a and V4b conduct, when PLB/1 is positive and PLB/3 negative, and are cut off when the polarity is reversed. Under these circumstances PLB/2 is at earth potential and the slider of RV4 is also at earth potential since R28, RV4 and R29 form a completely balanced circuit. No current therefore flows in the circuit R30, RV3, R25, RV2, R21.

20. When doppler compensation is applied a nominal 500c/s unbalanced input appears between PLB/2 and earth (PLB/4). This input is either in phase or anti-phase to the balanced 500c/s input according to the instantaneous aerial position. The currents in the circuit, R18, etc., now become unbalanced so that the potential at the anode of V4a, with respect to earth, is half the sum of the input voltages at PLB/1 and PLB/2, R18 and R24 having equal values. Similarly the potential at the cathode of V4b is half the sum of the input voltages at PLB/3 and PLB/2. At any instant, one half of the balanced input aids the unbalanced input whereas the other half of the balanced input opposes the unbalanced input so that, with a resolved, unbalanced input, the voltage waveforms at V4a anode and V4b cathode are as at (c) and (e) in Fig. 3.

21. Current flows in V4a and V4b as before, but, under the new circumstances, the valve currents are unbalanced (*fig.* 4 (*d*) *and* (*f*)). Therefore, although a value of current, equal to that of the valve conducting at the lower level, flows in the circuit V4b, R28, RV4, R29, V4a there will also be a difference current from the valve conducting at the higher level. This difference current will flow from the slider of RV4 via R30, RV3, R25, part of RV2 and R21 to earth. If the difference current flows from V4a the potential developed between RV3 slider and earth will be such as to charge C11 positively, whereas a difference current from V4b is in the reverse direction and tends to charge C11 negatively (*fig.* 4 (*g*)). The mean potential on C11 due to the phase-sensitive rectifier circuit takes the form shown in Fig. 4(h).

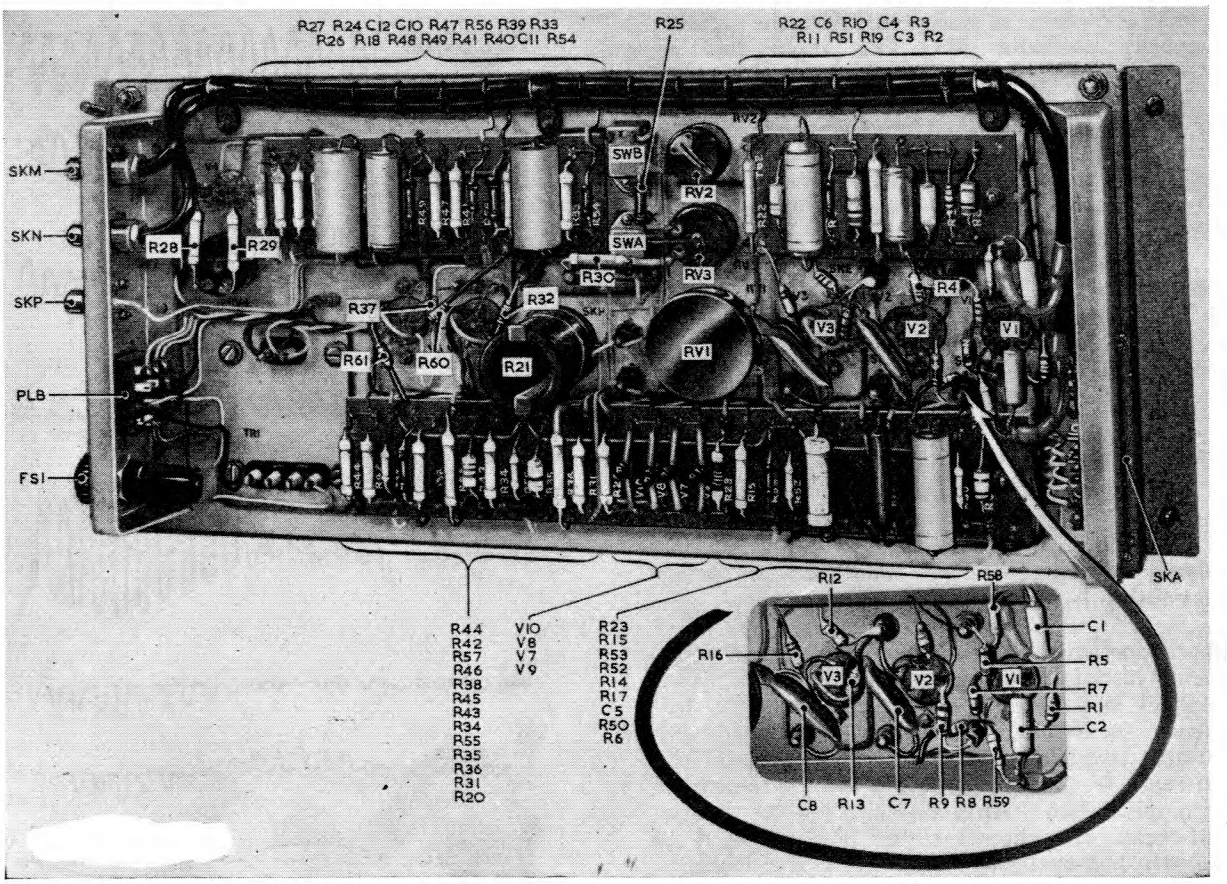


Fig. 4. Control, electrical frequency MI : rear view

Low frequency discriminator circuit

22. The variable and fixed reference oscillator frequencies are received at sockets SKM and SKN respectively and are terminated in 75 ohms by resistors R58 and R59. From these inputs, which are equal in level, a d.c. potential proportional to the frequency difference between the two inputs is produced. The circuit consists of a square-law mixer, the audio frequency output from which is amplified and applied to a full-wave rectifier circuit.

23. The two inputs are developed across R58 and R59 which can be considered as series-connected via earth. The algebraic sum of the inputs is applied across V1a, strapped as a diode, and across R1, R2. V1a current is proportional to the square of the combined inputs so that square-law mixing takes place, the products of mixing including the difference frequency between the two inputs. The higher frequencies are eliminated in the network R3, C3, since C3 has a very low impedance at frequencies of 5 Mc/s and above, leaving the low frequencies, in the range 500–1500c/s, to be amplified by the conventional amplifier stages V1b and V2a.

24. Positive half-cycles of the output from V2a anode are clipped by V2b to provide an input of negative-going half-cycles to the long-tailed pair V3. The FREQUENCY (SKG) control RV1 is set in conjunction with RV2, CURRENT (SKH–SKJ) so that with a current of 250 microamperes through R23, the beat frequency (the difference in frequency between variable and fixed reference oscillators) at test socket SKC is 1 kc/s.

25. The anodes of V3a and V3b produce anti-phase outputs which are substantially square waves. Negative inputs at V3a grid drive the cathode of both halves of the valve negative resulting in the anode of V3a going positive and that of V3b negative. The anode waveforms are fed, via the differentiating capacitors C7 and C8, to the full-wave bridge rectifier V7 to V10. Positive and negative pulses produced at the beginning and end of the anode waveforms are differentiated and rectified to produce positive-going inputs to the rectifier load R23, the negative-going pulses being inverted in the rectification process. A negative potential for the grid of V3b is obtained from the divider network R21, R22, RV2 across the −250V supply.

Combination of d.c. voltages

26. The outputs from the full-wave rectifier and phase-sensitive rectifier circuits are combined in the network R21, R20, R23, R31, R25 and part of RV2. With no output from the phase-sensitive rectifier, or with SWB set to ALIGN, the lower end of R30 is at earth potential. A potential will, however, be developed across R23 so that current flows in the path R31, RV3, R30, R21 and R20 to produce a potential at the slider of RV3 to charge C11 positively with respect to earth.

27. With an output from the phase-sensitive rectifier circuit, current flows from the slider of RV4 according to the two potentials produced and hence the potential at the slider of RV3 is the resultant of the two potentials. The output from the bridge rectifier opposes that from RV4 slider in that an increase in the more positive or less negative direction from RV4 slider causes RV3 slider potential, and therefore the output from SKP, to change in the same direction. The output from the variable frequency oscillator is thus increased in frequency and therefore the beat frequency is decreased. The frequency of positive pulses from the bridge rectifier is decreased so that the mean potential across R23 falls. Conversely, a negative output from RV4 slider decreases the oscillator frequency and increases the beat frequency. The potential across R23 therefore increases so that the bridge rectifier output opposes the decrease in oscillator frequency.

28. The CALIBRATE (SKC) control RV3 is set so that the current swing through R23, as measured between sockets SKH and SKJ, is 250 microamperes.

29. The BALANCE (SKC) control RV4 is set so that the current swing is balanced equally about 250 microamperes, i.e. with minimum and maximum readings of 125 and 375 microamperes respectively.

30. The time constant of C11 and its associated circuits is long and therefore its charge at any instant corresponds to the integrated sum of the outputs of the bridge rectifier and phase-sensitive rectifier circuits.

D.C. amplifiers

31. The potential across C11 is amplified by two d.c. coupled, long-tailed pairs V5 and V6, the cathodes of which are returned to potential dividers across the −250V supply to provide greater gain and power handling. The grids of V6a and V6b are returned to the −250V supply to maintain the grids at near earth potential.

32. The output from the unit is taken from the anode of V6a via the filter network C10, C12 and R48 and socket SKP to the associated variable reference frequency oscillator. SKP is returned to the junction of R47, R49 in a divider network across +250V and −250V supplies in order to provide a mean d.c. output level of zero volts ; this

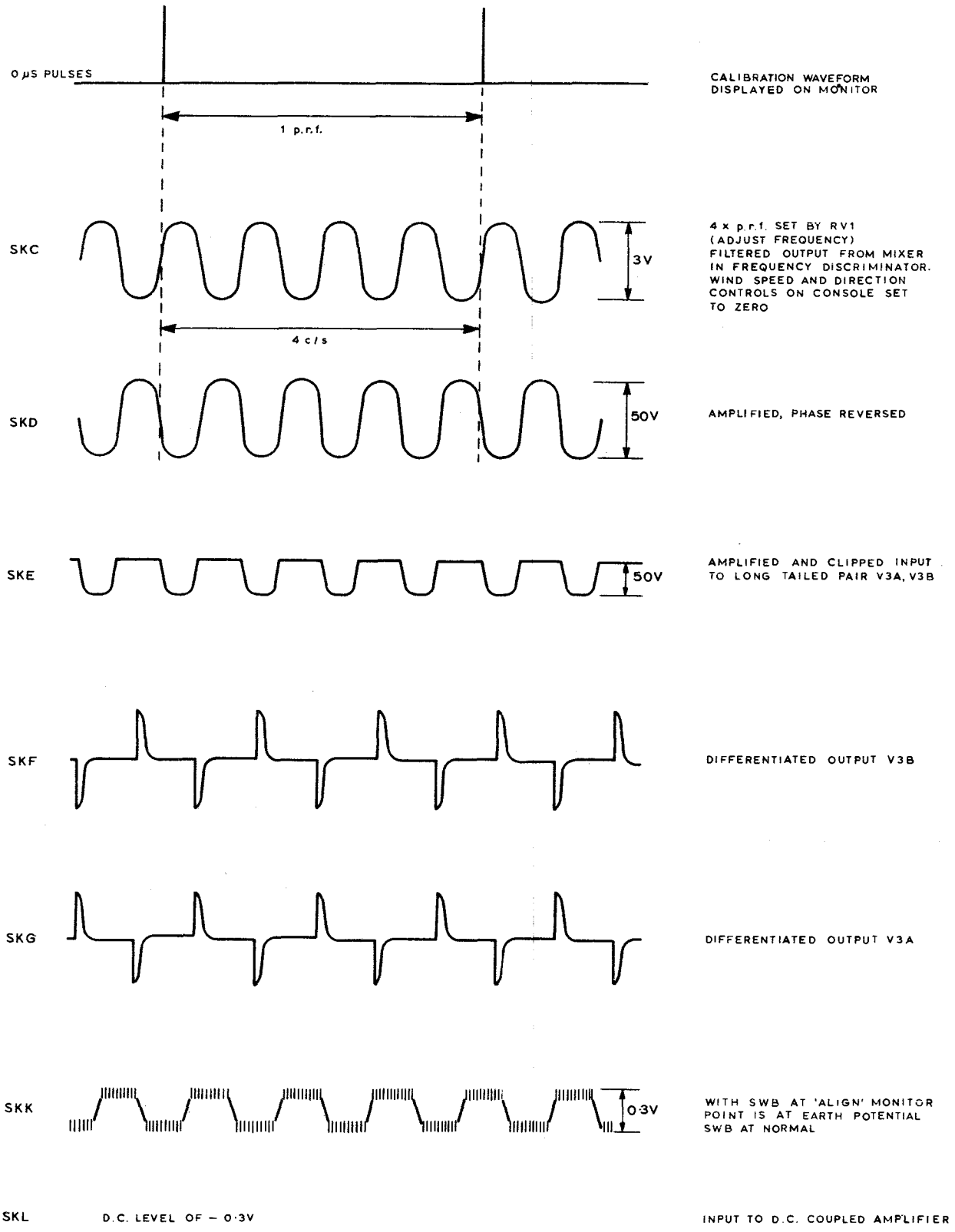


Fig.5 Waveforms at monitor points

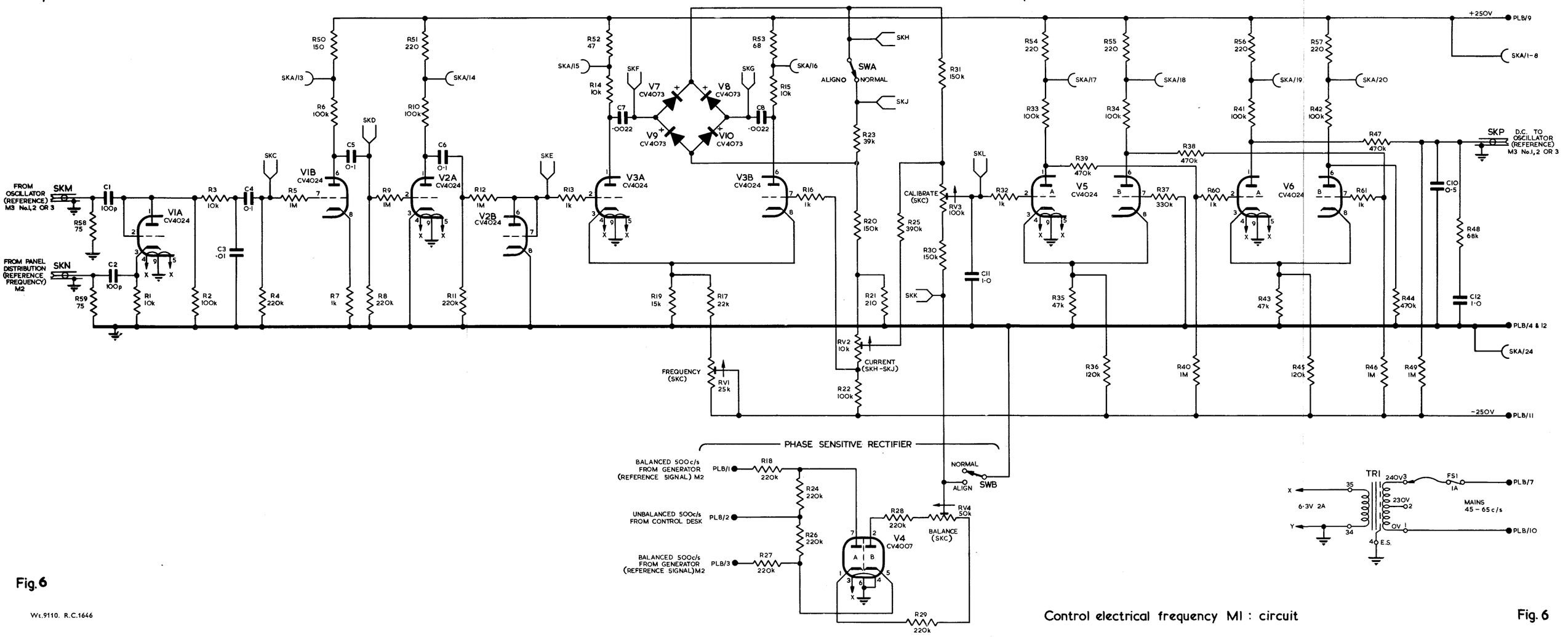


Fig. 6

Wt.9110. R.C.1646

Control electrical frequency MI : circuit

Fig. 6

Chapter 12

POWER SUPPLY (±50V)

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

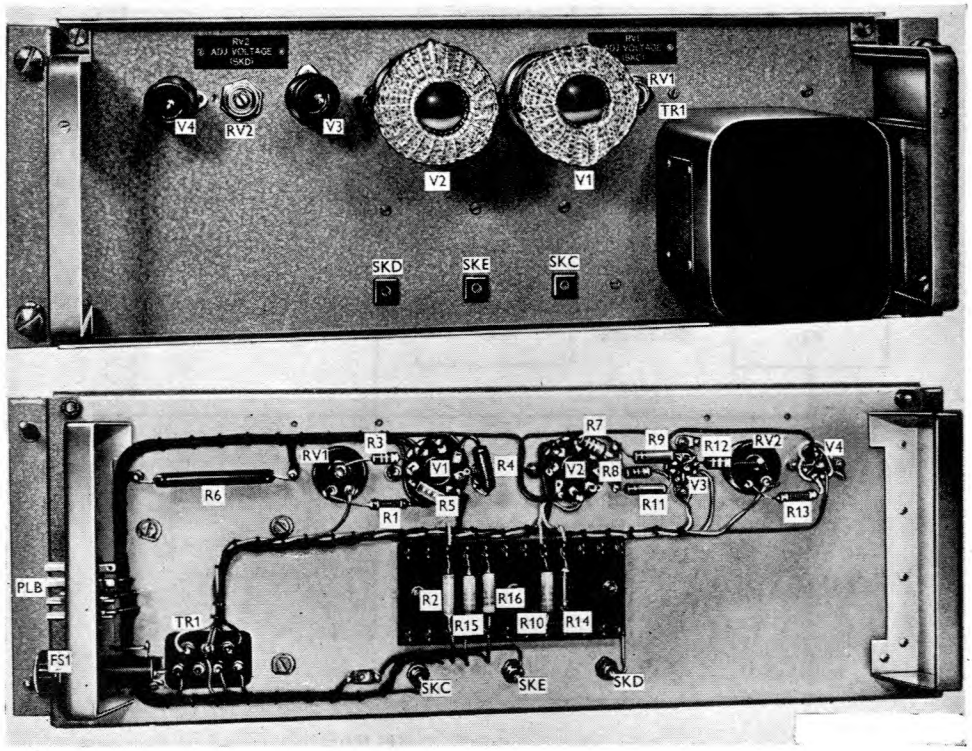


Fig. 1. Power supply (±50V): front and rear views

Introduction

1. The purpose of the power supply (±50V) (*fig.* 1) is to provide stabilized outputs at +50V and −50V for the joystick control on the monitor console. The unit is located in frame 1 of the doppler cabinet.

2. The +50V and −50V outputs are derived (*fig.* 2) from the +250V and −250V supplies provided by the regulator, voltage (+250V) M2. The +50V is taken from a cathode follower stage connected across the +250V supply with provision for output voltage adjustment. The −50V is provided from the −250V supply by a shunt regulator stage whose output is fixed by a control valve. Facilities are provided for adjusting the output voltage. Monitoring sockets are provided for measuring the output voltages.

Performance characteristics

Inputs

3. The unit requires the following inputs:

(1) 240V 50 c/s single-phase a.c. at 0·2A fused by FS1 at PLB/7 and PLB/10.

(2) +250V at 100mA at PLB/9.

(3) −250V at 100mA at PLB/11.

Outputs

4. The unit delivers the following outputs:

(1) +50V ±5V at 50mA with a peak ripple not greater than 20mV at PLB/5.

(2) −50V ± 5V at 50mA with a peak ripple not greater than 20mV at PLB/6.

Circuit description (*fig.* 4)

+50V supply

5. This supply is derived from the +250V input to the unit. Valve V1 is a cathode follower, the output of which remains constant and is a function of the grid voltage. The grid voltage is set by the ADJ. VOLTAGE (SKC) control RV1 which is adjusted to give +50V ±5V measured at SKC with a multimeter Type 1.

−50V supply

6. This supply is derived from the −250V input to the unit. The −50V output is taken from the cathode of V2, the valve operating as a shunt regulator maintaining constant current in, and thus constant voltage drop across, R6. V2 is controlled by V3 whose grid receives output variations from the potentiometer chain V4, R13, RV2 and R14. The stabilizer V4 provides a reference potential, and allows the possible output variations to be passed to the grid of V3 with minimum attenuation.

7. Variations at the grid of V3 appear in opposite sign at the anode and are passed to the grid of V2 via R8. This input to V2 alters the impedance of the valve and thus the voltage drop across it, thereby tending to maintain a constant voltage drop across R6. The output voltage is set by the VOLTAGE (SKD) control RV2 to give −50V ±5V measured at SKD with a multimeter Type 1.

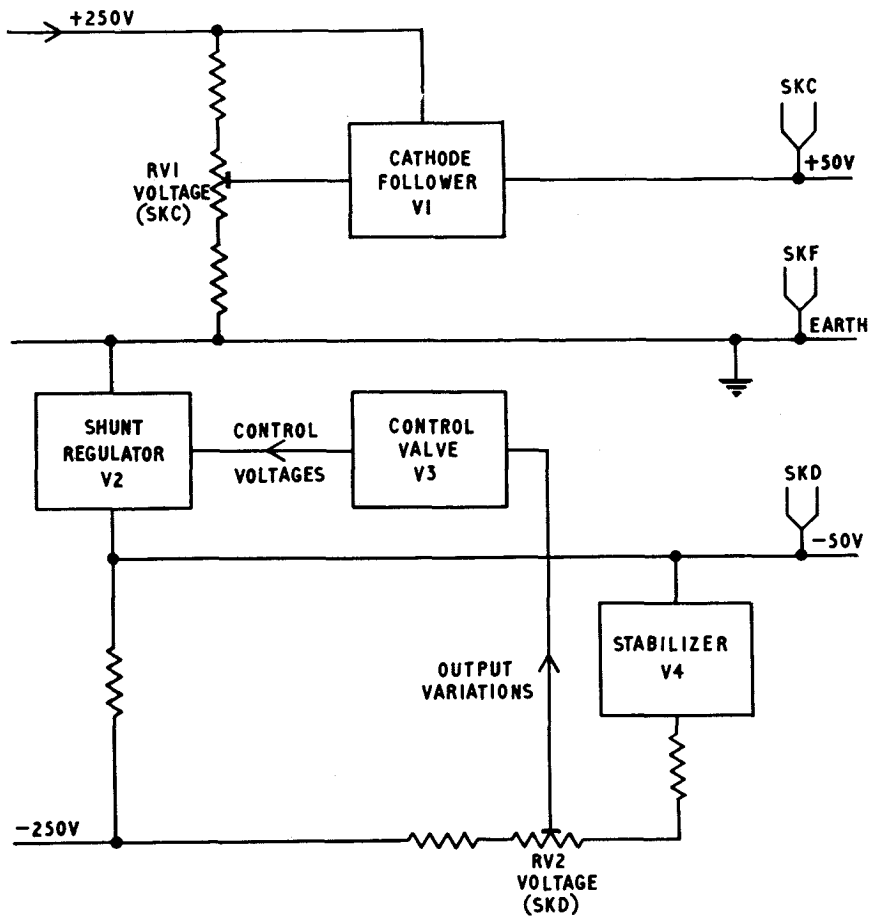


Fig. 2. Power supply (±50V): block schematic

Heater supplies

8. The valve heaters are supplied from transformer TR1. The mains supply is taken to the primary of the transformer via PLB/7, PLB/10 and FS1. The secondary is held at about −125V to preserve the cathode/heater insulation of V3 (V3 cathode is at −200V). The heaters of V1 and V2 are also tied at this potential although their cathode/heater breakdown voltage is greater than 250V. The reason for this is that the transformer fitted has a single secondary winding.

Distribution

9. Fig. 3 shows the distribution of the ±50V supplies to the controller motor M3, the doppler distribution cabinet and the joystick control in the centre control desk.

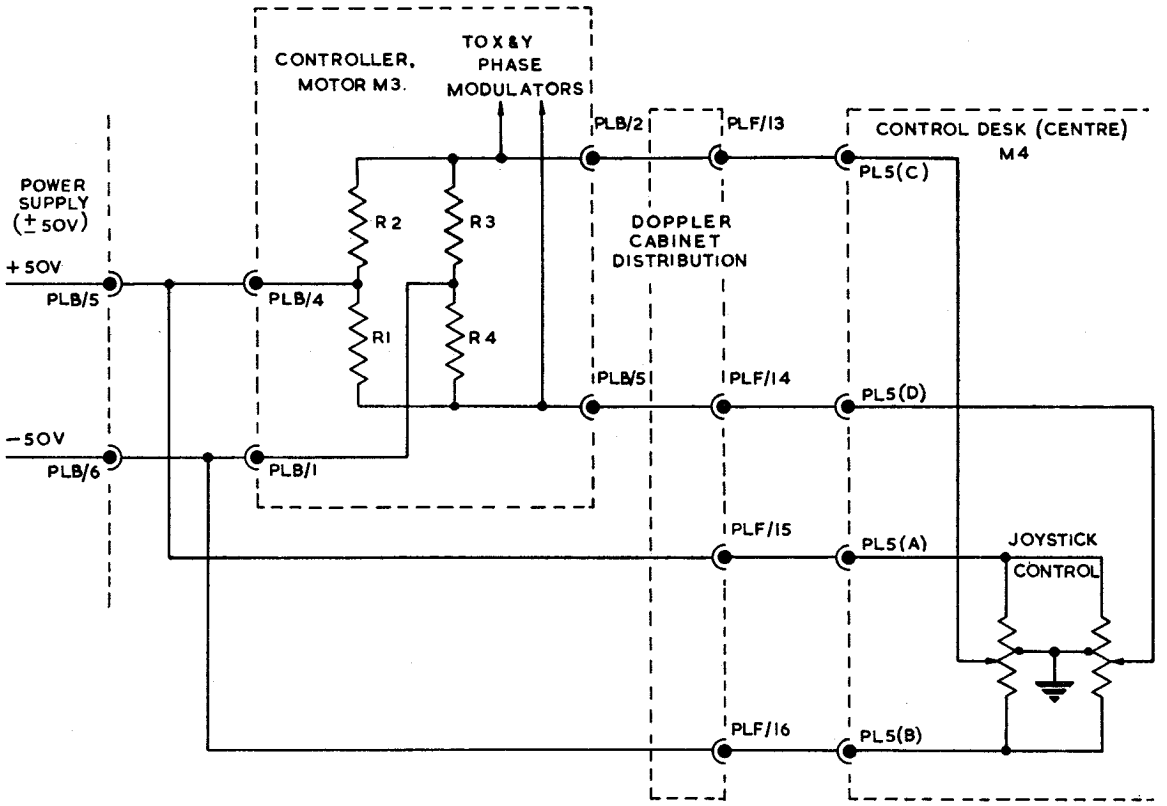


Fig. 3. Power supply (±50V): distribution

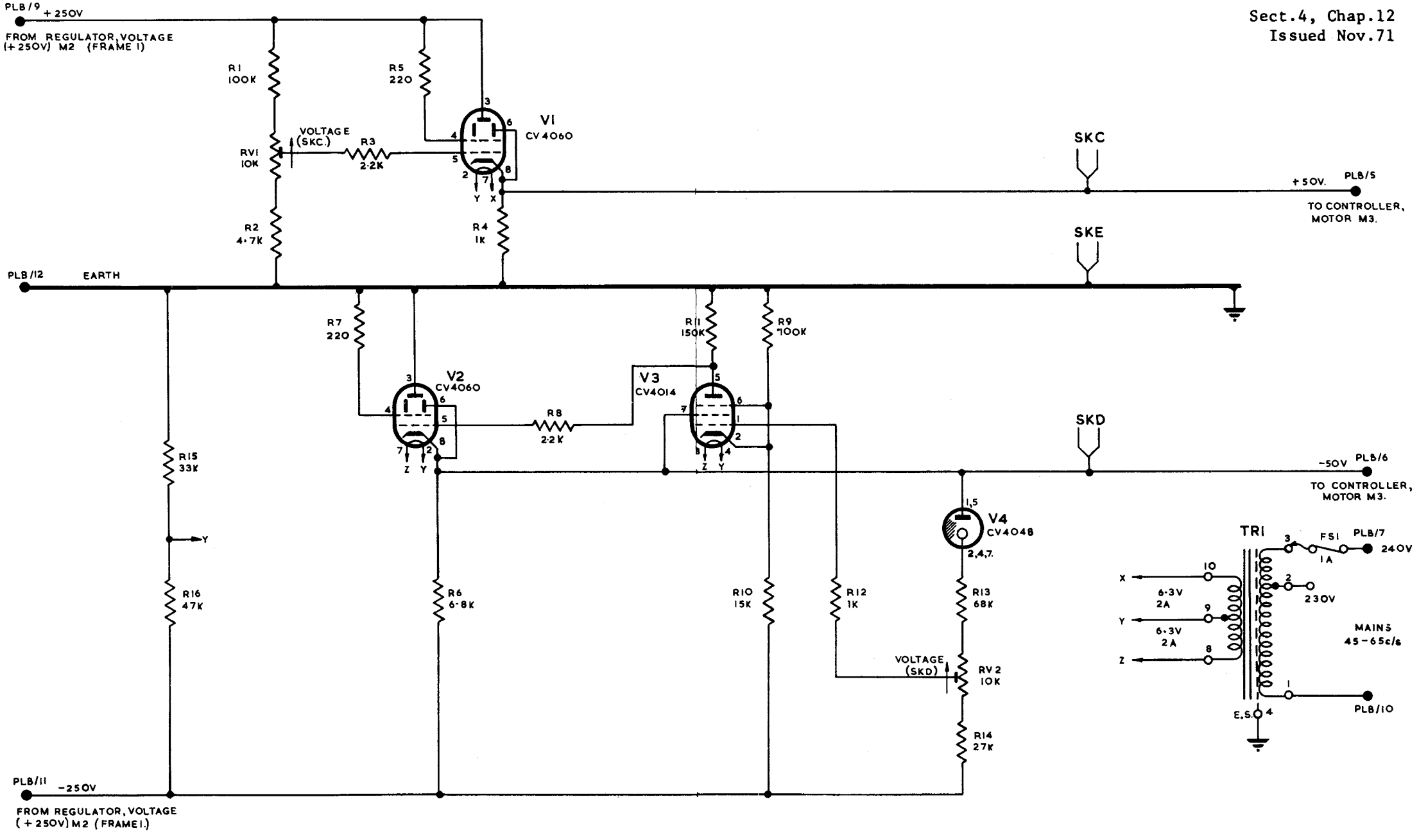


Fig.4

Power Supply (± 50V): circuit

Fig.4

51476-(M.F.P.)