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**116B-0610-1**

# DECCA LORAN C/A TYPE ADL21 RECEIVER ARI. 23180 AND ASSOCIATED TEST EQUIPMENT

## GENERAL AND TECHNICAL INFORMATION

BY COMMAND OF THE DEFENCE COUNCIL

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Ministry of Defence

FOR USE IN THE
ROYAL AIR FORCE

(Prepared by the Ministry of Technology)

Issued Apr. 67

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## LIST OF ASSOCIATED PUBLICATIONS

*Air Navigation — Manual of Radio Aids* *A.P.*1234*C*

◀*Decca Loran C/A Type ADL*21 *receiver ARI.*23180 *and associated test equipment: servicing diagrams manual* *A.P.*116*B*-0610-10▶

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# PART 1

# GENERAL INFORMATION

## LEADING PARTICULARS

*Function* ... ... ... *The ARI.23180 is an airborne radio installation employing the Decca Loran Type ADL21 receiver which provides position-fix information derived from the transmissions from any of the currently available chains of Loran C or Loran A stations.*

*In the Loran C mode, signals are acquired manually, but thereafter, master and slave signals are tracked automatically. Loran A operation is manual.*

*Display* ... ... ... ... ... *A five-digit numerical display provides a direct read out, in microseconds, of the time differences applicable to the selected transmissions. In the Loran C mode, the read-out may be switched to display time difference for either one of two selected master/slave pairs, or to alternate automatically between the two readings* ⋈.

*A cathode ray tube (CRT) display is provided for signal acquisition and Loran A interpretation.*

*Frequency*

*Loran C*: ... ... ... ... ... ... ... ... ... ... 100 *kc/s*

*Loran A*: ... ... ... ... ... ... ... ... ... ... 1850 *kc/s*
1900 *kc/s*
1950 *kc/s*

*Bandwith*

*Loran C*: ... ... ... ... ... *Switch selected, 20 kc/s to 3dB points*
*or 6 kc/s to 3dB points*

*Loran A*: ... ... ... ... 40 *kc/s to 3dB points*

*Sensitivity*

*Loran C*: ... ... ... ... *The system will continue to track (at the 3rd cycle) down to 1μV into the antenna amplifier.*

*Loran A*: ... ... ... ... *20μV r.m.s. (measured at the peak of the pulse) to provide a useful deflection on the CRT.*

*Signal/Noise tolerance*

*Loran C*: ... ... ... ... *Third cycle signal tracking will continue with signal/white noise conditions as poor as 1/10.*

*Loran A*: ... ... ... ... *Satisfactory operation will continue at signal/noise ratio of 3/1.*

*Normal operating range*

*Loran C*: ... ... ... ... ... 1200 *n.m. over sea water (ground wave)*
900 *n.m. over land (ground wave)*
2500 *n.m. using skywave.*

*Loran A*: ... ... ... ... ... 700 *n.m. over sea water (ground wave)*
150 *n.m. over land (ground wave)*
1500 *n.m. using skywave*

*Probable accuracy*

*Loran C*: ... ... ... ... ... 200-400 *yd. in good cover (ground wave)*
½-1 *n.m. at range of* 1000 *n.m.*
10-20 *n.m. when using skywave.*

*Loran A*: ... ... ... ... .. 1-5 *n.m. in good cover (ground wave)*
30-50 *n.m. when using skywave.*

*Antenna* ... ... ... ... ... *Normally a suppressed plate which forms part of the aircraft skin and is unique to each aircraft type.*

*Power supplies* ... ... ... ... ... ... ... 115*V*, 400 *c/s, single phase*
28*V, d.c. negative earth*

*Power consumption*

*a.c.* ... ... ... ... ... ... ... ... ... *Normal power is* 45*W*
*Maximum power during oven warm-up period is* 55*W.*

*d.c.* ... ... ... ... ... *Varying with lighting demand, mode of operation, etc. but not exceeding* ◀2*A*▶.

*Units of equipment*

| | |
|---|---|
| *Receiver, Loran (Decca Type* 1831) ... ... ... ... ... | 5826-99-955-8336 |
| *Indicator, Loran (CRT Controller) (Decca Type* 1832) ... ... | 5826-99-955-8337 |
| *Indicator, Digital Display (Read-out Unit) (Decca Type* 1833) ... | 5826-99-955-8338 |
| *Amplifier, Antenna (Decca Type* 1953) ... ... ... ... | 5826-99-955-8339 |

*Dimensions and weights*

| | *Width (in)* | *Depth (in)* | *Height (in)* | *Weight (lb)* |
|---|---|---|---|---|
| *Receiver* ... ... ... ... | 10·250 | 22·215 | 7·750 | 39 |
| *CRT Unit* ... ... ... ... | 5·750 | 13·750 | 6·000 | 8 |
| *Read-out Unit* ... ... ... ... | 5·750 | 5·469 | 2·625 | 2 |
| *Antenna Amplifier* ... ... ... | 3·875 | 6·438 | 3·875 | 1·5 |

**Note.**—*These are maximum dimensions (i.e. over knobs, handles or other projections).*

*Special test equipment*

| | |
|---|---|
| ◀*Test Set, Loran (Decca Type* 1863) ... ... ... ... ... | 6625-99-107-1415 |
| *Signal processing box (Decca Type* 1958) ... ... ... ... | 5826-99-107-7566 |
| *Module test set (Decca Type* 1959) ... ... ... ... ... | 5826-99-195-0870▶ |

# Chapter 1

# GENERAL PRINCIPLES OF LORAN C AND LORAN A

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### Loran C

**1.** Loran C (Loran with phase-matching or cycle-matching) is so termed to distinguish it from the original Loran system, now generally termed Loran A (see, for example, A.P. 1234C, Vol. 3, Sect. 7, Chap. 3). The system stems from efforts to improve the range and accuracy of Loran. Between 1946 and 1951, an experimental system operating on 180 kc/s and 200 kc/s was developed: this was named CYCLAN (Cycle-matching air navigation). In 1952 the basis of the current system was established, employing a 100 kc/s carrier frequency and using both time and phase measurement. This was initially referred to as CYTAC (Cycle-matching tatical navigational system). CYTAC was under field evaluation from 1955 to 1957 after which the system was renamed Loran C.

**2.** The system is similar to Loran A in principle, being a pulse technique hyperbolic position fixing aid, but it differs in three important respects: —

(1) A single transmission channel is used based on carrier frequency of 100 kc/s (Loran A uses a group of channels in the band 1800 kc/s to 1950 kc/s).

(2) A multiple pulse coded transmission sequence is used.

(3) Both pulse and phase-matching techniques are employed in the receiver.

These changes result in considerably improved range and higher accuracy and permit the use of automatic tracking of signals with continuous or cyclic readout of the time differences. Automatic acquisition of signals, also, is possible with Loran C but this places some restriction on operating range and the facility is not included in the present receiver.

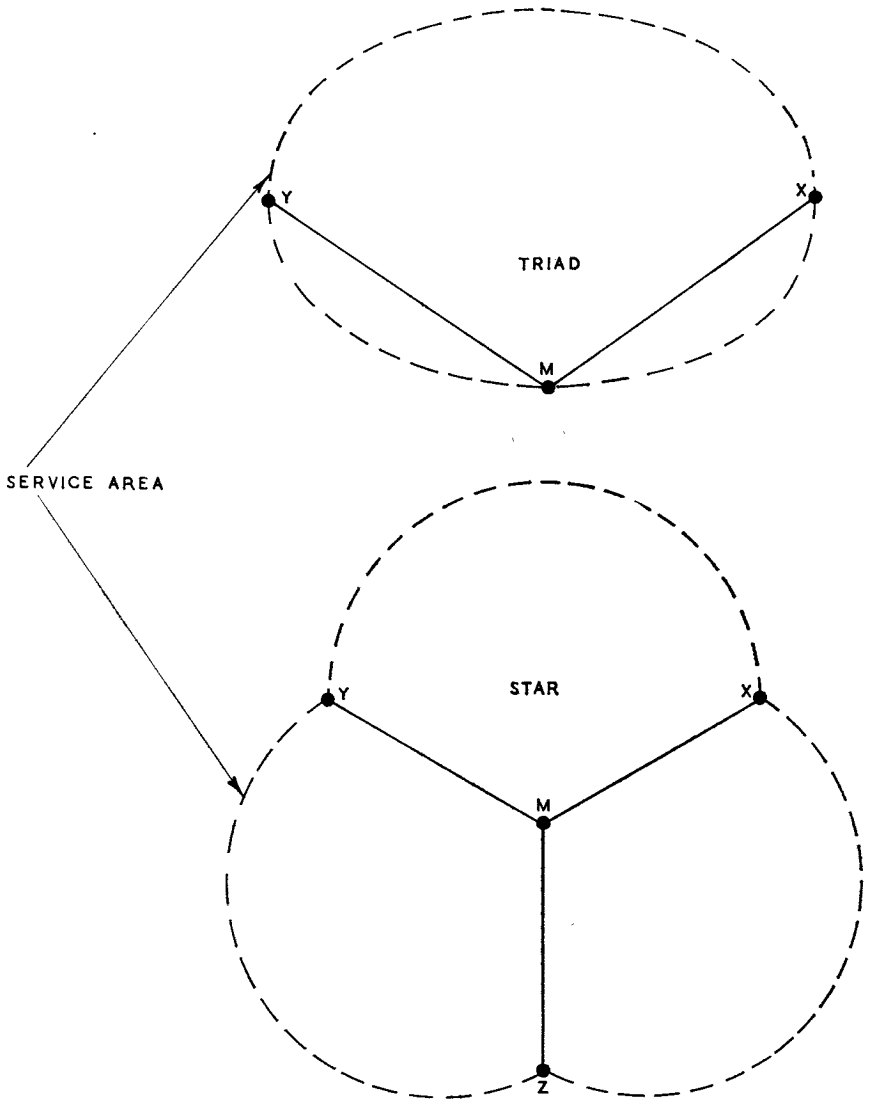


**Fig. 1. Loran system configurations**

## Principle of operation

**3.** Fig. 1 illustrates two Loran system configurations. Three to five land-based pulse transmitting stations comprise a Loran C chain and consist of a master (M) and two, three or four slave stations (X, Y, Z and W). When two slave stations are employed the chain is called a triad. When three or four slaves are used, it is known as a star. The precisely timed pulse transmissions from all stations are made on a time shared basis, utilizing the common carrier frequency of 100 kc/s. The transmissions occupy a spectrum of 20 kc/s, 99% of the radiated energy lying within the band 90 kc/s to 110 kc/s.

**4.** The transmissions propagated from the master station are received at a slave station and at the receiving set in the service area. The slave station delays by a precise time interval known as the coding delay and then transmits its own signal.

**5.** Figure 2 illustrates time relationships between transmitted signals. A receiver in the service area will receive the pulses from the slave station delayed in time from the master by an amount depending upon both the location of the receiver and the coding delay indicated in fig. 2. Since the receiver is at a constant time difference with respect to the two stations, the time difference between the reception of pulses from them establishes hyperbolic contours with the two stations as foci. A second slave station performing the same function as the first slave also generates a family of hyperbolic contours. The receiver establishes the difference in time of the two slave signals relative to the master thus creating two hyperbolic contours, the intersection of which defines the location of the receiver.

**6.** The Loran transmitted pulse (fig. 3) is approximately 300$\mu$S in duration and rises to greater than 90% of its maximum amplitude within 70$\mu$S. At about 30$\mu$S, from the com-

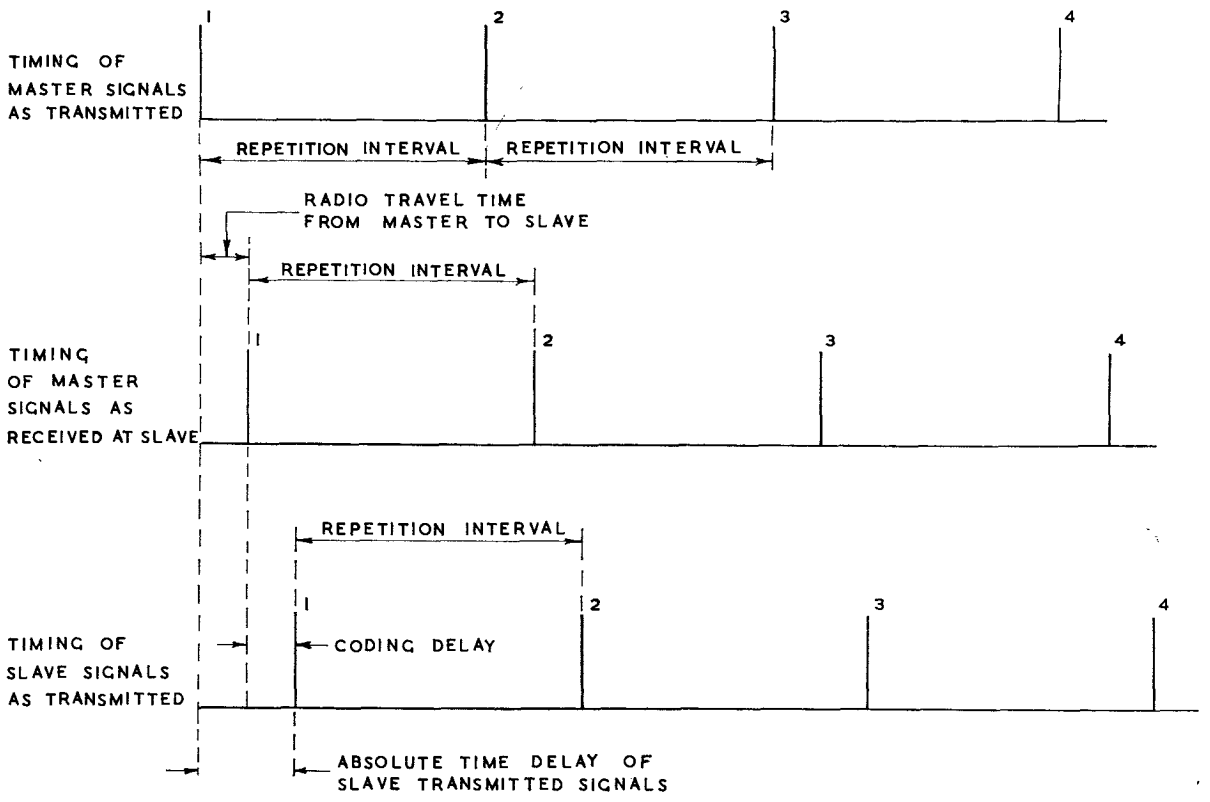


**Fig. 2. Time relationship of transmitted signals**

mencement of the pulse the signal amplitude is approximately 60% of the peak amplitude. This point is chosen as the latest point at which measurements in the receiver (phase sampling) can be made, before contamination from the first hop sky waves can occur. Normal or ground wave Loran signal measurements are thus referred to a point 30$\mu$S from the start of the signal.

**7.** The low basic frequency of the system allows the ground wave propagational path to follow the curvature of the earth. The same transmissions reflect off the ionosphere and the sky waves thus formed, depending upon the height of the ionosphere and the distance of the user from the transmitting station, appear at the receiver some time after the reception of the ground wave signals. However, the sampling of a given pulse in the receiver occurs before the earliest possible arrival time of the skywave. This enables positional accuracy of the order of 0·1$\mu$S to be obtained continuously within the groundwave coverage area. This accuracy is obtained through the use of coherent detection techniques for measuring the phase of the received pulse and techniques for determining the fixed reference point on the leading edge of the pulse irrespective of pulse amplitude.

**8.** Figure 4 illustrates the multipulse time sharing. The coding delays at the slave stations are so arranged that a receiver placed anywhere within the service area will always receive the master transmissions first, followed in order by the X, Y and Z slaves. The master station transmits a burst of eight pulses each approximately 300$\mu$S long spaced 1mS apart (followed by a ninth pulse 2mS later, which is used for identification and fault signalling). The X slave is the next to transmit, followed in turn by the Y and then the Z slave if incorporated in the chain. (A fourth slave, the W slave, may also be incorporated). Each slave sends eight pulses. The time which elapses between the initiating pulse transmission from the master station and the next initiating pulse transmission from the same station is known as the repetition interval.

**9.** Since the whole of the Loran C system operates on a single 100 kc/s carrier frequency, identification of a particular chain must be provided by some means other than r.f. channel selection. This identification is achieved by the use of 48 different pulse repetition rates. All the stations in a particular chain use the same pulse repetition rate but a different rate must be used for each chain. The 48 pulse repetition rates are

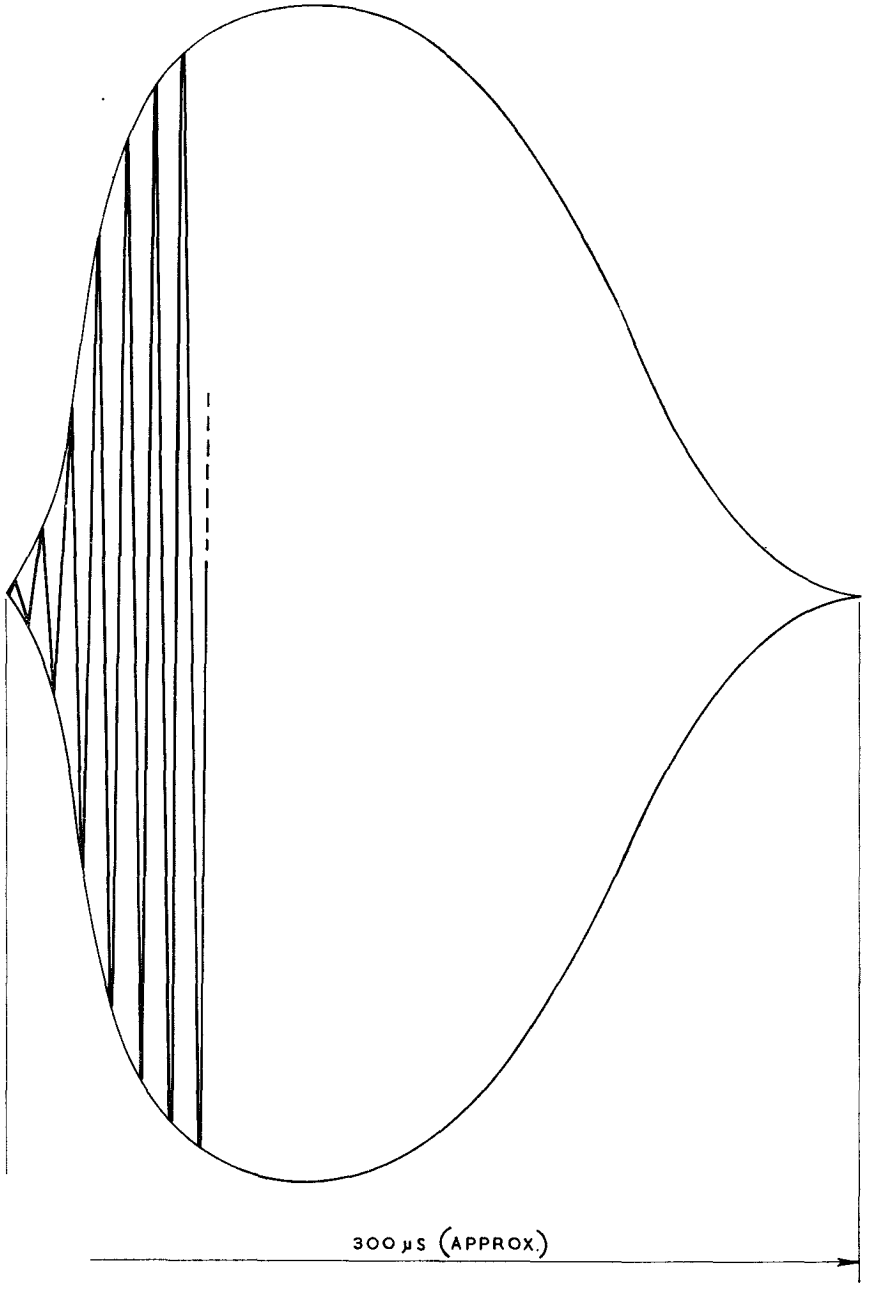


**Fig. 3. Typical Loran C pulse shape**

selected from six basic rates designated by letters H, L, S, SH, SL & SS. These designations correspond with group repetition intervals of 30,000, 40,000, 50,000, 60,000, 80,000 and 100,000$\mu$S. In addition for each of these basic rates there are eight specific rates, 0, 1, 2, 3, 4, 5, 6 and 7. To obtain the repetition rate, 0, 100, 200, 300, 400, 500, 600 or 700$\mu$S is subtracted from the basic rate according to whether the specific rate code is 0 to 7 respectively, each digit representing 100$\mu$S.

**10.** In order to provide both an automatic search capability and some measures of skywave rejection, the pulses are phase coded. The phase of the r.f. carrier relative to the pulse envelope is given one of two values. When the first half cycle of the carrier is positive going the coding is said to be positive. When the first half cycle of the carrier is negative going the coding is negative. The r.f. within the envelope of the negative phase coded pulse is 180° out of phase with the r.f. of a positive coded pulse. These phase definitions are illustrated in fig. 5.

**11.** The phase-coding of master and slave stations is given in Table 2. The master transmits alternately two types of coding, M1 and M2

respectively. Similarly the slaves all transmit a phase code identical to each other but use two coding patterns S1 and S2. Thus one repetition interval will consist of M1, S1 (X), S1 (Y), S1 (Z) followed in the next repetition interval by M2, S2 (X), S2 (Y), S2 (Z). The whole sequence then repeats. On a four-slave chain, Slave W precedes X.

12. The generation of a Loran pattern by the transmissions from a master and slave station is shown in fig 6 with a typical baseline length of 1200 km and to clarify this description the upper half of the hyperbolic pattern is annotated with the master/slave time differences in μs that would exist were the pulses transmitted simultaneously. The time difference would then be zero on the baseline bisector, rising to -4000μs (master advance on slave) on the master baseline extension and to +4000μs (slave advance on master) on the slave baseline extension. A total range of time difference of 8000μs is thus represented by this pattern.

13. If an absolute time delay (fig 2) of more than 4000μs is introduced into the slave transmission the master pulse will always be received before the slave pulse. The lower half of fig 6 indicates the actual pattern numbering that would be used with a cooling delay of 46,000μs (absolute time delay being 50,000μs). The interpolated figures show the 100μs intervals which are usually adopted for Loran C charts and the 50μs sub-divisions that may also be used. The 100μs intervals each represent 15 km on the baseline. The appropriate time-delay readout of the receiver is directly referred to the chart to establish the aircraft position on a hyperbola within that pattern. The readout corresponding with the second slave transmission is similarly referred to the pattern generated by that slave in conjunction with the master and the fix is unambiguously established by the intersection of the two hyperbolae so defined.

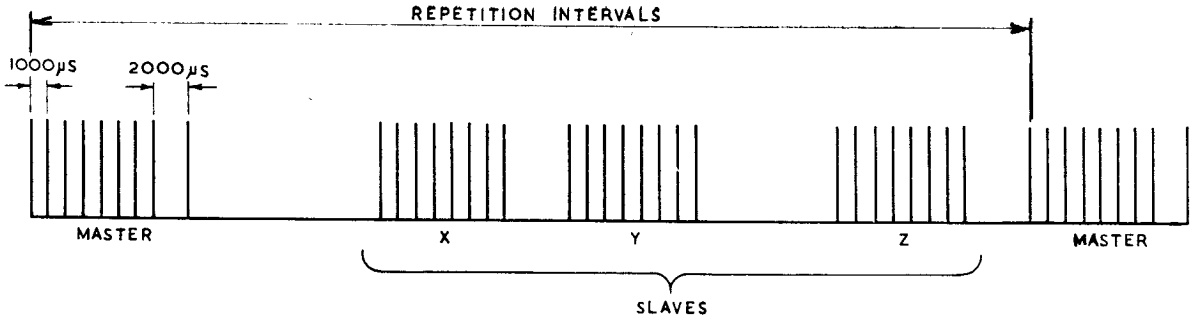


Fig.4 Loran C: multipulse time sharing

Basic measurement techniques

14. The primary stage in time measurements on Loran C is similar to that of Loran A. Gates (in the present instance, groups of gates) are aligned with the received pulse groups to establish the coarse time measurement. The second stage, known as 'indexing' consists of aligning the gates, derived from the output of an internal 100 kHz pulse generator, with the 3rd cycle of the received master and slave pulses (ie at the 30ms sampling point defined in para 6). The accurate time measurements are then made by automatic counting of the 100 kHz pulse train between master and slave gating points. The time difference is then read directly in microseconds on the Read-out Unit display.

LORAN A

15. Loran A is fundamentally similar to Loran C but it operates from 1850 kHz to 1950 kHz with only basic pulse time measurement. The signals are transmitted on one of three frequencies in that band, coded by channel number, and on one of three basic pulse recurrence rates (Table 3). The latter are further augmented by 8 specific recurrence rates 0 to 7 which have the same significance as with Loran C (para 9), the digits 0 to 7 representing successive reductions in recurrence interval of 0 to 700μs in 100μs decrements. For example 2S6 represents transmissions on 1850 kHz with a recurrence frequency of 20 Hz (50,000μs interval) less 600μs or an actual interval of 49,400μs.

16. Individual measurements must be made on each Master:Slave pair of transmissions to obtain a fix and the automatic tracking facility cannot be employed. The received signals are identified on the double-trace oscilloscope display of the receiver and the time measurement, in the present receiver, is effected by first aligning two gate waveforms (termed 'pedestals') with the two displayed pulses and then adjusting the display to bring both gated pulses into visual coincidence. The time difference may then be read directly in microseconds from the digital readout of the receiver. This operation must then be repeated for the master and the second slave to obtain a position fix.

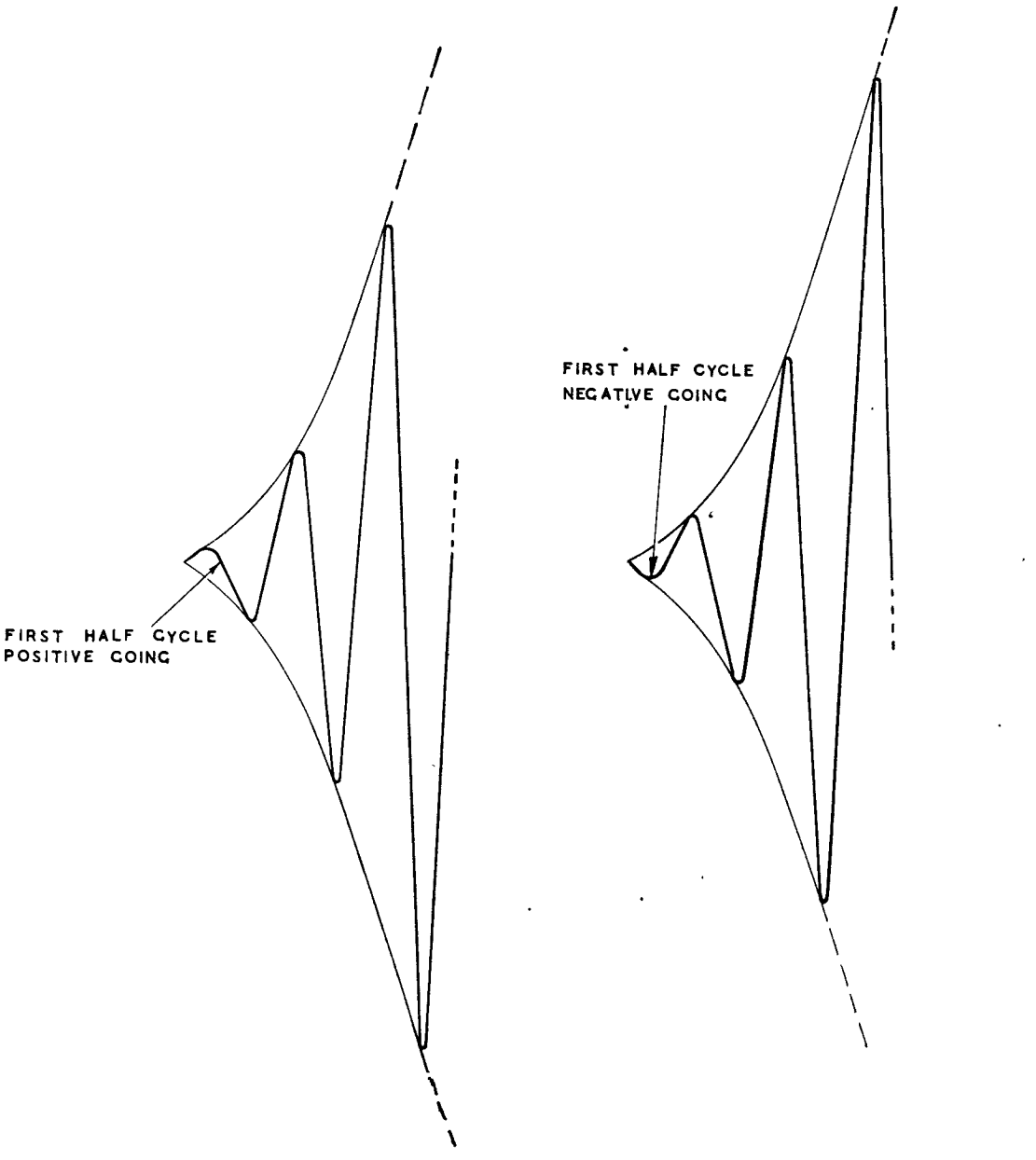


Fig.5 Loran C: phase definition

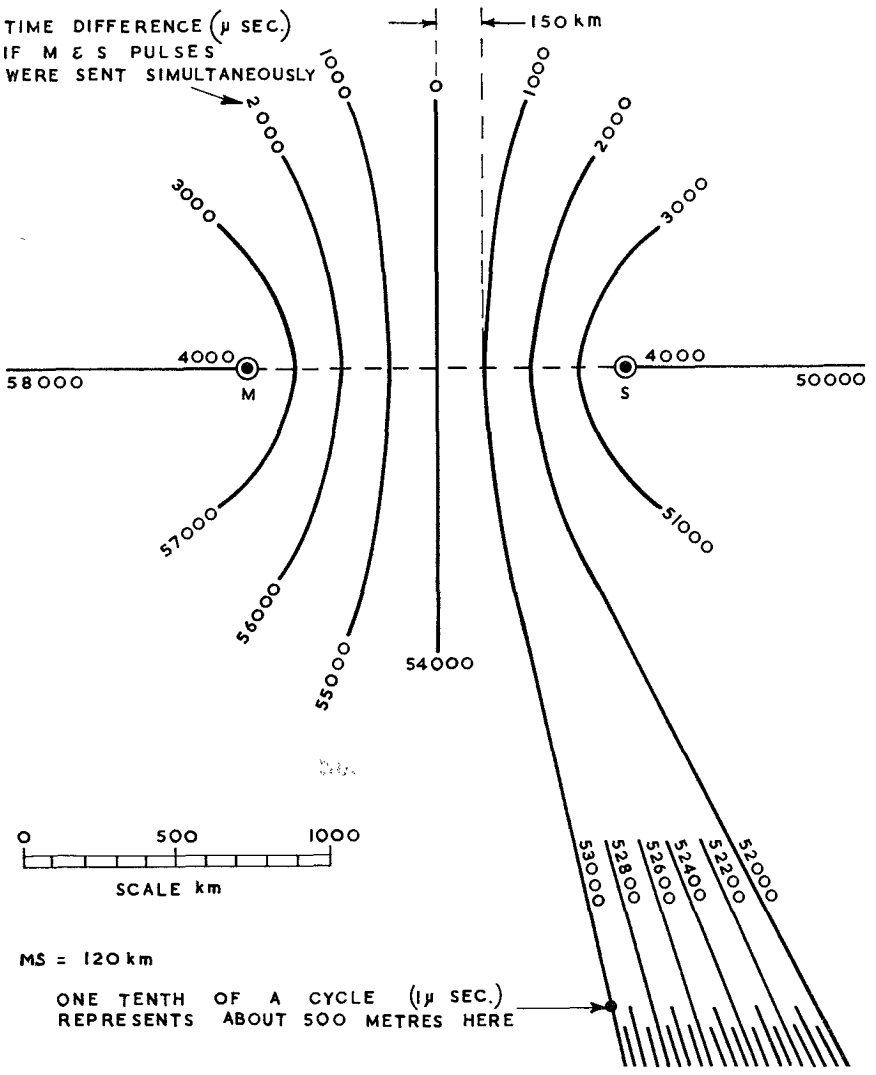


**Fig. 6. Typical Loran C pattern numbering**

## TABLE 1

**Loran C: Pulse repetition rates**

| Specific rate selection | Pulse repetition rates (Microseconds) | | | | | |
|---|---|---|---|---|---|---|
| | Basic rate selection | | | | | |
| | SS | SL | SH | S | L | H |
| 0 | 100,000 | 80,000 | 60,000 | 50,000 | 40,000 | 30,000 |
| 1 | 99,900 | 79,900 | 59,900 | 49,900 | 39,900 | 29,900 |
| 2 | 99,800 | 79,800 | 59,800 | 49,800 | 39,800 | 29,800 |
| 3 | 99,700 | 79,700 | 59,700 | 49,700 | 39,700 | 29,700 |
| 4 | 99,600 | 79,600 | 59,600 | 49,600 | 39,600 | 29,600 |
| 5 | 99,500 | 79,500 | 59,500 | 49,500 | 39,500 | 29,500 |
| 6 | 99,400 | 79,400 | 59,400 | 49,400 | 39,400 | 29,400 |
| 7 | 99,300 | 79,300 | 59,300 | 49,300 | 39,300 | 29,300 |

**TABLE 2**

**Loran C: Phase coding of transmissions**

| Interval | Master | Slave X, Y, Z All identical |
|---|---|---|
| 1 | M1 + + − − + − + − | S1 + + + + + − − + |
| 2 | M2 + − − + + + + + | S2 + − + − + + − − |
| 3 | M1 + + − − + − + − | S1 + + + + + − − + |
| 4 | M2 + − − + + + + + | S2 + − + − + + − − |
| 5 | All master signals repeat as interval 1, 3, etc. for odd intervals and as interval 2, 4 etc. for even intervals. | All slaves repeat as interval 1, 3, etc. for odd intervals and as interval 2, 4, for even intervals. |

**TABLE 3**

**Loran A: Frequency and basic rate coding**

| Code | Frequency | Interval |
|---|---|---|
| CHANNEL 1 | 1950 kc/s | |
| CHANNEL 2 | 1850 kc/s | |
| CHANNEL 3 | 1900 kc/s | |
| P.R.F. S | 20 c/s | 50,000 $\mu$S |
| P.R.F. L | 25 c/s | 40,000 $\mu$S |
| P.R.F. H | 33⅓ c/s | 30,000 $\mu$S |

# Chapter 2

# GENERAL AND FUNCTIONAL DESCRIPTION OF ARI.

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### Units of Equipment

**1.** ARI.23180 comprises four major units:—

(1) Receiver, Decca Type 1831 (Receiver, Loran 5826-99-955-8336)

(2) CRT Unit, Decca Type 1832 (Indicator, Loran 5826-99-955-8337)

(3) Read-out Unit, Decca Type 1833 (Indicator, Digital Display 5826-99-955-8338)

(4) Aerial Amplifier, Decca Type 1953 (Amplifier, Antenna 5826-99-955-8339)

### Brief Description of units

**2.** The Aerial Amplifier Type 1953 is a two-valve unit mounted adjacent to the aerial. The primary function of this unit is to isolate the aerial which represents a high impedance source, from the necessarily long and high capacitance feeder to the receiver. The amplifier provides a useful gain of the order of 6. Essential features are a low capacitance, high resistance input, low noise factor and low output impedance, the absence of phase distortion within the frequency bands 70-130 kc/s (Loran C) and 1·8 Mc/s to approximately 2·5 Mc/s (Loran A) and good linearity up to inputs greatly in excess of normal operating level. These characteristics ensure a high signal to noise ratio with minimum phase error within the Loran frequency bands, and permit operation in the presence of high level signals at other frequencies without appreciable harmonic or cross-modulation interference appearing on the wanted signal.

**3.** The Receiver Type 1831 incorporates all the circuitry necessary for the processing of the received Loran C and Loran A signals, together with the power supply circuits for the receiver and the other three units. There are no operator controls on the receiver, thus it may be mounted remote from the control/display units.

**4.** The CRT Unit Type 1832 houses the cathode ray tube and all the controls necessary for an operator to adjust the display. The function of the unit is to provide a visual display of the received Loran signals together with their selected comparison or tracking gates. A meter on this unit enables the index channel, the a.g.c. channel and the a.f.c. channel sampling voltages to be verified.

**5.** The Read-out Unit Type 1833 indicates the time difference in microseconds between the master pulses and selected slave pulses. This measurement is displayed on a five-digit read-out. Also on this unit are the alarm lights, a dimmer

control for the display, and switches to select the basic mode of operation and chain pulse-repetition rate. The switch to the right of the display selects display of slave 'A' or slave 'B' measurement, or automatic display of slave 'A' and slave 'B' measurements alternately. These identities 'A' and 'B' are used throughout the receiver as either measuring channel may be operationally used for any one of the X, Y, Z and/or W slave inputs.

**Outline of operation** (fig. 1, 2)

**6.** The following paragraphs describe the functional operation of the ADL21 equipment. Reference should be made to the functional block diagram (fig. 2). This description follows the primary (Loran C) function of the installation. Changes in the mode of operation for Loran A use are outlined in para. 22.

**7.** A radio-frequency amplifier accepts the low-level input signal from the aerial amplifier and amplifies it to a level suitable for the signal sampling process, and for the oscilloscope display in the c.r.t. unit, Type 1832. The r.f. amplifier output is controlled by two a.g.c. detectors which maintain the signal level during tracking of the pulsed signals at 0·4 volts and, where the received signals are extremely weak, limit the r.m.s. signal-plus-noise output level to less than 10 volts to avoid non-linearities associated with overdriving the amplifier or gating circuits which follow. The specified output of the r.f. amplifier is maintained over an input range of 2 microvolts to approximately 0·5 volts. A manual gain control is used to adjust the gain prior to acquisition when time-gated samples of each signal level are not available to the a.g.c. loops.

**8.** Two types of filtering are accomplished within the r.f. amplifier: —

(1) Bandpass filtering around the 100 kc/s carrier frequency is manually switched, with 3 dB bandwidths of either 30 or 6 kc/s. The former is sufficiently wide to avoid distortion of the leading edge of the pulse during tracking, while the latter provides improved signal-to-noise to assist signal acquisition.

(2) A notch filter is provided to reject interfering signals. This is tuned manually over a range of 72 to 125 kc/s using the c.r.t. display to measure their effect.

**9.** The output of the r.f. amplifier is presented, via a 90° phase shift circuit and a manually-adjustable Y gain control, on the Y-axis of the c.r.t. display. This display, when properly synchronised by other circuits and controls, enables manual signal acquisition and monitors signal tracking after acquisition.

**10.** A phase-code generator (the coder) uses timing signals developed in the master and slave divider chains (para. 13) to position a flip-flop to the binary states corresponding to the phase-codes of the transmitted signals (Chap. 1, Table 2). This coding, as described in Chap. 1, is intended to permit rejection of multi-hop skywave contamination and consists of 180-degree phase reversals of the transmitted carrier. These are removed prior to signal sampling and integration by applying the coder output to a pair of phase decoding gates which select either the real or inverted phase of the r.f. amplifier output according to the state of the output flip-flop in the phase-code generator.

**11.** The filtered and decoded r.f. signal is applied to three sets of three sampling and filtering channels: —

(1) The a.f.c. channels detect phase deviations in each of the three signals and provide the appropriate control voltages for phase-locking three local oscillators to the filtered signals received from the three transmitters.

(2) The a.g.c. channels detect amplitude deviations in each of the three signals and provide the appropriate automatic gain control waveforms for adjusting r.f. amplifier gain sequentially to the level of each of the received signals.

(3) The index channels measure the phase relation between the signal sampling point and the envelope of the appropriate received pulse. This measurement enables resolution of the 10-microsecond ambiguity otherwise associated with the 100 kc/s phase measurement in the a.f.c. channel, and permits adjustment of the signal sampling point sufficiently early on in the pulse to avoid skywave contamination (i.e. normally at the 3rd cycle).

**12.** Filtering of the time difference measurements on the incoming signals is accomplished by phase-locking separate oscillators to each of the three signals. These oscillators employ crystals in a temperature-controlled environment to provide long-term frequency stability of the order of 5 parts in $10^7$. To avoid "cross-talk" between the three channels, the oscillators operate on different harmonics of 100 kc/s, viz. 5·0, 4·8 and 4·5 Mc/s. Analogue frequency division by 50, 48 and 45, respectively, then converts each to the required 100 kc/s carrier frequency.

**13.** The 100 kc/s outputs of the frequency dividers are then applied to separate decade dividers which count the pulse-repetition interval and are automatically reset at a count corresponding to the manually selected pulse repetition rate for the desired chain. The three oscillator-divider systems are referred to as Master, A and B clocks. The current logic of each decade divider is decoded to provide five time-related trigger signals.

(1) 1 mS tracking gate pulses: these control the phase decoding of the received signals via the coder (para. 10) and are also applied via

the coder, to the c.r.t. to provide visual indication of gate alignment with the incoming signals during acquisition.

(2) 5 microsecond pulse: this opens the gates which sample the incoming signal in the a.f.c., a.g.c. and index channels described above.

(3) 1 mS read pulses: these connect a time-shared d.c. amplifier between master and slave transmissions, to update stored analogue outputs of the three channels according to the latest information available from the input stores. Phase errors which might result from unbalance or drift are eliminated by use of a time-shared amplifier as the same phase offset occurs in the master and both slave oscillator channels, and the time-difference measurement is thus unaffected.

(4) A trigger applied to the c.r.t. sweep generator.

(5) A digitizing trigger: this defines the phase of each clock to the decade counters which provide the output time-difference readings.

**14.** The stored output of each a.f.c. channel gated by the 1mS pulse is applied to a variable-capacitance diode to pull the frequency of the corresponding local oscillator until the 5 microsecond sampling gate generated by its divider chain is centered about the zero crossover of the incoming r.f. signal, completing the phase-locking loop.

**15.** The a.g.c. channels operate in a similar manner using the same 5 microsecond gating pulses, except that the r.f. input is shifted 90 degrees, so that, when the a.f.c. loop has phase-locked the local oscillator establishing automatic tracking, the output of the a.g.c. channel will be at maximum and thus it will be proportional to the amplitude of the r.f. amplifier output. The stored outputs of the three a.g.c. channels are combined to form a time-shared gain control waveform which is applied to the r.f. amplifier to control the input levels to the sampling gates for each of the three signals.

**16.** The index channels again operate in a similar manner gated by the same 5 microsecond pulses but the input r.f. signal passes through the index derivation/mixer circuit so that the waveform may be adjusted to have a zero crossover at any desired point on the r.f. pulse. This derivation is illustrated in fig. 1. The 90° shifted signal, used as an input to the a.g.c. channel, is delayed 10 microseconds and added to a selected portion of the undelayed signal in an r.f. mixing circuit. As shown in fig. 1, the signals then cancel each other and provide an amplitude null at a point 30 microseconds after the start of the pulse ( the required "3rd cycle" sampling point). Should the sampling point be set less than 30$\mu$S, a positive output is obtained whilst if it occurs more than 30$\mu$S after the start of the pulse the output is negative.

**17.** The stored outputs of the three index channels are routed to the d.c. voltmeter on the panel of the c.r.t. unit (as are the a.f.c. and a.g.c. channel outputs). A meter selector switch selects a.f.c., a.g.c. or index channels for display. Positioning the function switch to M, A or B selects the signal to be monitored. Additionally, the three index channels are connected via a nand gate to an alarm warning light so that an indexing fault in any channel gives rise to an alarm lamp indication. Similar alarm provision is made for the a.f.c. and a.g.c. channel outputs.

**18.** The index channel output, unlike the a.f.c. and a.g.c. outputs, is not part of a closed-loop servo system but is under the control of the operator, who is required to position the sampling gate on the proper portion of the received signal pulse. When the a.f.c. channel has established lock-on of the local oscillator, the polarity of the index channel output displayed on the meter indicates the direction of error in the sampling point position with respect to the correct 30$\mu$S point. The operator corrects this in 10 microsecond steps to obtain a null indication (zero meter reading). The sampling point is changed in 10$\mu$S steps by a process termed "slewing" in which the triggering of the 4 decade divider chain of the affected channel is stepped 1 cycle at a time with respect to the applied 100 kc/s input from the associated oscillator/divider system. Manual slew control in this manner has the advantage under poor signal-to-noise conditions when third cycle sampling is impracticable, that providing the c.r.t. display indicates tolerable skywave contamination later into the pulse, all three station sampling triggers may be jumped in 10 microsecond steps toward the peak of the pulse to increase the signal level in the sample.

**19.** Each of the three divider chains is capable of being manually slewed by the operator at three different rates. As indicated in para. 18, the operator may insert or blank input pulses one at a time to slew the dividers 10 microseconds in either direction. For signal acquisition when the equipment is first turned on, however, much more rapid slew is required to synchronize the entire four-decade counter to the incoming signal. For this purpose, switches are provided which select either a 50 c/s or 500 c/s signal from the divider, and these are used to slew the clock in either direction. With the coarse slew switch on the c.r.t. unit in the LEFT position, the 500 c/s signal blanks one input pulse every 2 microseconds. This slows the clock which is producing the triggers so that the signals drift to the left on the c.r.t. display at a rate which will traverse the maximum Loran repetition interval (100 milliseconds) in twenty seconds.

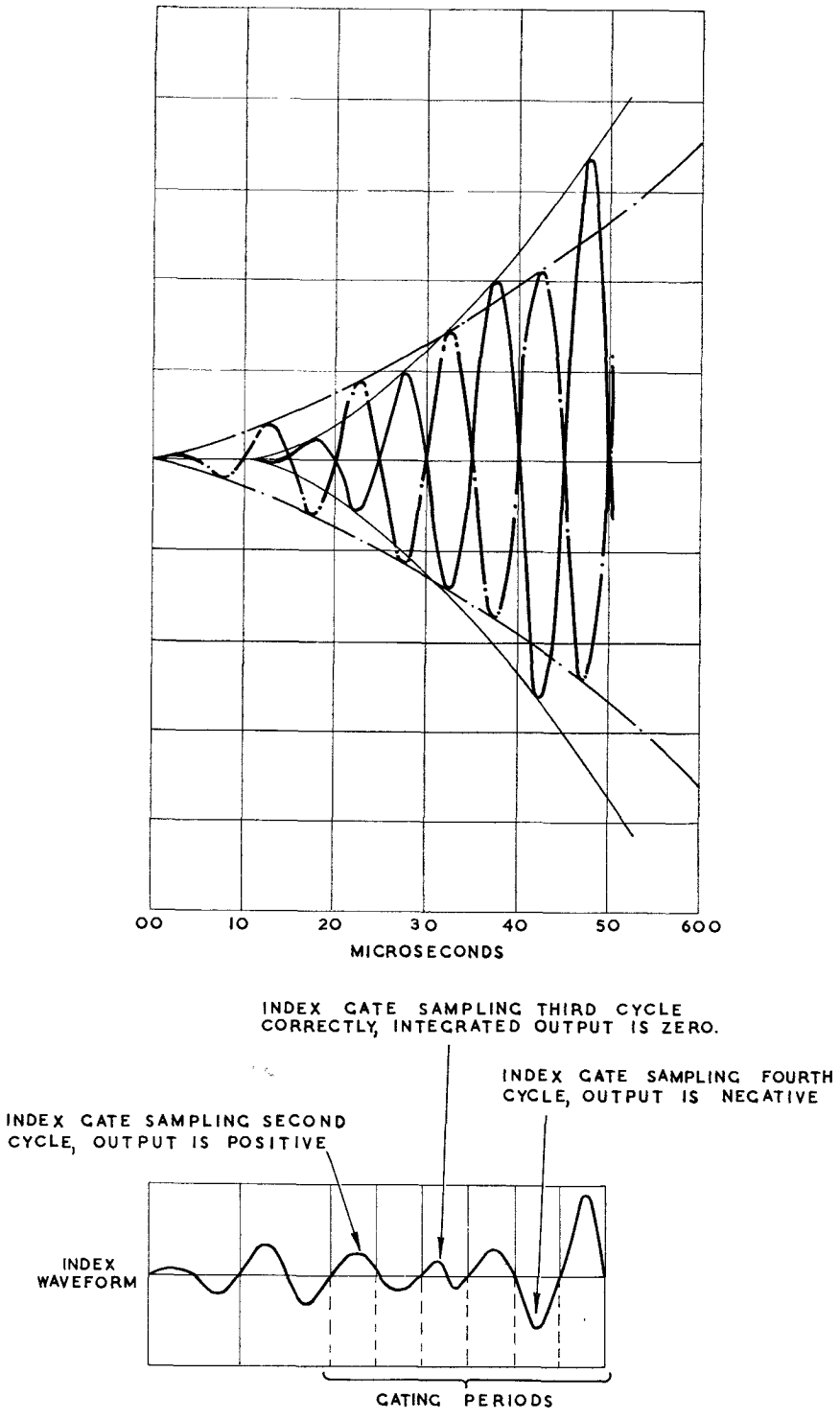


**Fig. 1. Index derivation and gating**

**20.** When the pulse group corresponding to the channel being slewed has reached the left edge of the sweep, and the first pulse has just started to re-appear at the right, the operator increases sweep speed to correspond to a 10 millisecond trace length (which contains the pulse group), and operates the MEDIUM slew to right. In this position, the 50 c/s signal adds one input pulse every 20 milliseconds. This speeds up the clock which is producing the triggers so that the signals drift to the right on the c.r.t. display at a rate of 500 microseconds per second. When the first pulse of the desired group appears at the left edge of the trace, slew is stopped, the sweep rate is increased to 150 microseconds trace-length (one pulse-length) and the 10 microsecond jump is used

to position the sampling trigger on the third r.f. cycle as verified by both the c.r.t. display and the metered output of the index channel. Once a signal has been so acquired by its respective oscillator-divider combination, it will be tracked by its a.f.c. sampling and integration channel which controls local oscillator frequency to maintain the clock in synchronism with the received signal.

**21.** When the three clocks are synchronized with their respective signals, in other words when the receiver is tracking all three signals, the time measurements are made by comparing the phase of the A and B slave clocks with that of the master clock. To this end each divider chain develops a digitizing trigger once each clock interval (PRR): the trigger has a fixed time relation to the sampling pulse controlling its phase. 10 megacycle clock pulses derived by doubling the master oscillator frequency are gated into a binary-coded decimal counter, the length of the gate being the time-difference between the master digitizing trigger and the selected slave trigger. The resulting count of the BCD counter is decoded and displayed on five decimal projection indicators. This single display is shared between the two slave signals. The operator may select A slave, B slave or both alternately, on an automatic time-cycling basis. The rate of display updating is internally adjustable.

**Loran A operation**

**22.** For LORAN-A operation, the same local oscillator and decade divider chains are used. The received pulses, after amplification and filtering in a separate r.f. amplifier, are presented to the c.r.t. along with master and slave timing pedestals decoded from their respective divider chains. The operator then manually slews the two clocks to synchronize each with its respective signal, and, as before, the output counters measure and display the phase difference between the master and slave clocks as a time difference. This operation is then repeated for the second slave. The three sampling and filtering channels described above for LORAN C are not used during LORAN A operation.

Printed for Her Majesty's Stationery Office by Ezra Sidebotham Ltd., Wigan.
270354/D.461039 200 8/67 Gp.483

# Chapter 3

# INSTALLATION AND OPERATION

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## LIST OF ILLUSTRATIONS



## UNITS OF EQUIPMENT

**1.** ARI.23180 comprises the four major units listed in Table 1 and illustrated in Fig. 1 to 4. Fig. 6 illustrates the unit interconnections. Details of inter-unit cables, together with Part Numbers for the associated cable-end plugs or sockets are listed in Tables 2 to 10.

**2.** In addition to the four major units of Table 1, an antenna is required. This is normally of the suppressed plate type which is specifically designed for each aircraft type to be fitted.

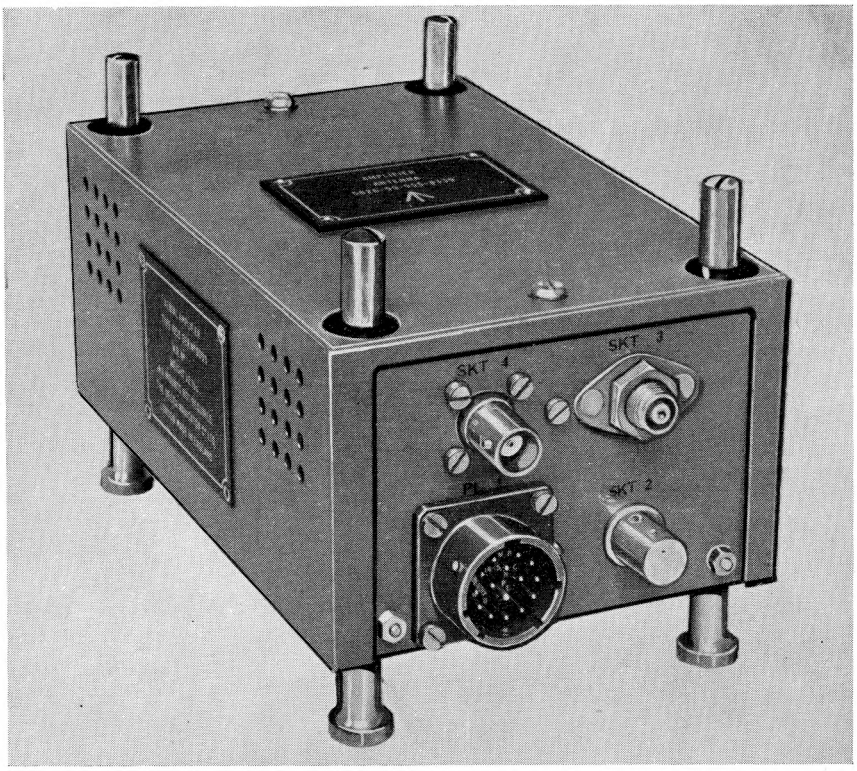


**Fig. 1. Antenna amplifier Type 1953**

## MOUNTING AND LOCATION OF UNITS

**3.** In general, a large degree of flexibility exists in the siting of units, subject only to the limitations noted in the following paragraphs. On all units, plug or socket connectors are of differing types or have differing orientations to prevent insertion of a cable connector into the wrong receptacle.

### Antenna

**4.** The suppressed plate antenna is a construction of synthetic resin bonded, laminated glass fibre with an embedded wire mesh antenna element. Due the the wide variation in airframes and available locations, antennae vary considerably in shape; only general information is therefore given in this Air Publication.

**5.** The location of the antenna, as indicated in para. 4, is physically restricted by considerations of aircraft construction and existing obstructions, but electrically the controlling factors are that it should be as far as possible either below or above the longitudinal electrical centre of the aircraft, which

**TABLE 1**

**ARI.23180. Dimensions and weights**

| | Dimensions (inches) | | | Weight |
|---|---|---|---|---|
| | Width | Depth | Height | (lb.) |
| Receiver Unit, Type 1831<br>5826-99-955-8336 | 10·250 | 22·215 | 7·750 | 39 |
| CRT Unit, Type 1832<br>5826-99-955-8337 | 5·750 | 13·750 | 6·0 | 8 |
| Read-out Unit, Type 1833<br>5826-99-955-8338 | 5·750 | 5·500 | 2·625 | 2 |
| Antenna Amplifier Type 1953<br>5826-99-955-8339 | 6·438 | 3·875 | 3·875 | 1·5 |

Maximum dimensions are quoted (i.e. over knobs, handles or other projections).

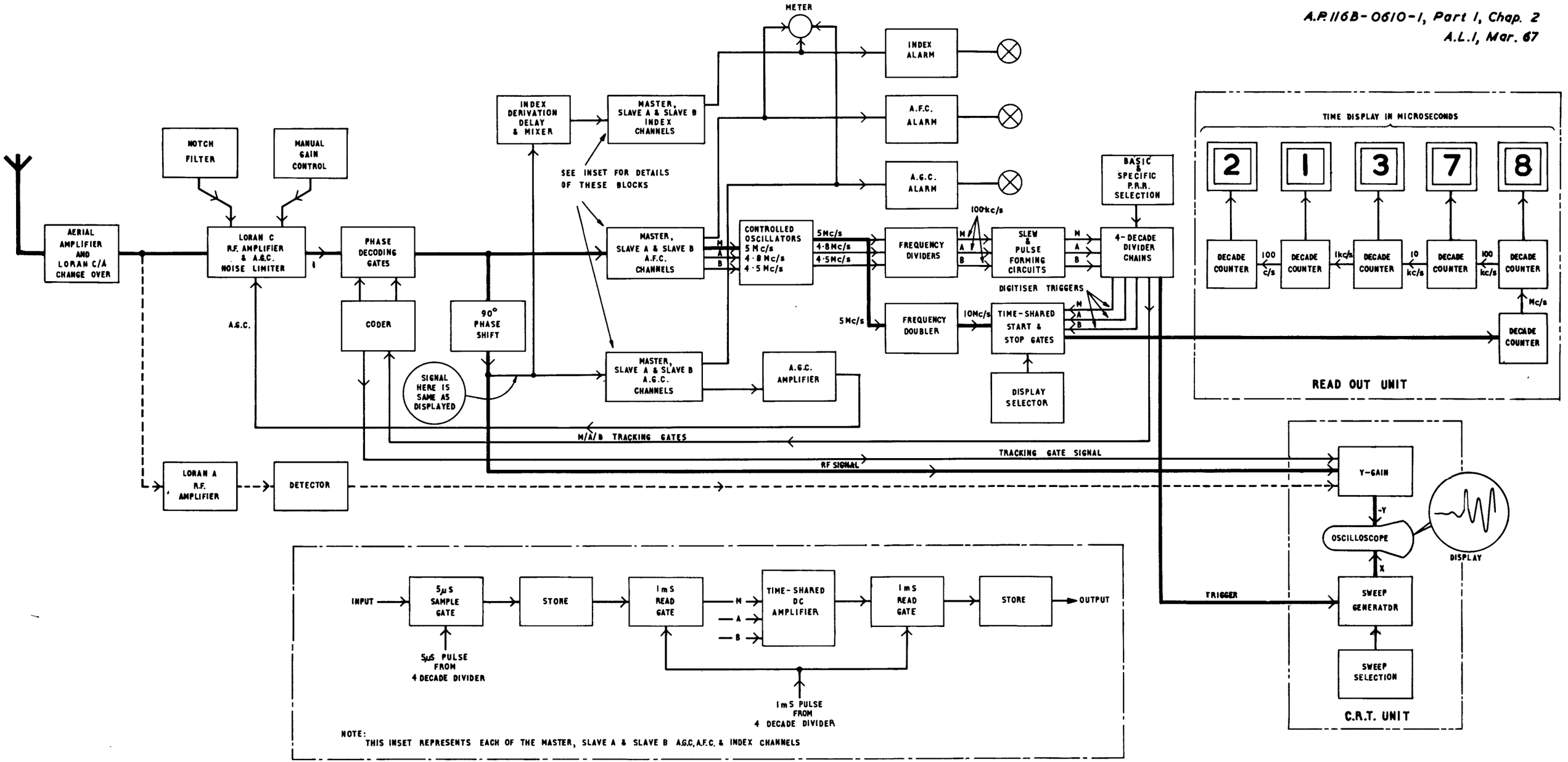


Fig. 2

Block diagram of ARI. 23180 (LORAN C/A)

Fig. 2

is analagous to a ground plane, and that it should be positioned where the minimum static due, for example, to impact of charged precipitation is experienced. It is normally necessary to employ static dischargers at selected points on the aircraft to minimise radio noise due to the uncontrolled discharge of accumulated static electricity which would otherwise occur at wing tips, extremities of tail surfaces, jet effluxes etc. The location of such dischargers is peculiar to the aircraft configuration. Note that the indiscriminate attachment of such dischargers can produce the opposite effect to that intended (i.e. an increase in static noise on radio equipment in the aircraft).

**6.** Electrical connections to the antenna are made to a hexagonal stud moulded into the antenna. Where possible, two such studs are preferred to provide separate attachments for the r.f. feeder cable (Connector No. 10) and the test signal cable (Connector No. 11). Thus the test signal (which originates in the Test Set and passes via receiver SKT. 8, SKT 5, Connector No. 5, antenna amplifier PL1, SKT. 4 and Connector No. 11) is injected into the antenna at a point which will provide test facilities to the complete installation, including antenna connections.

**Antenna Amplifier. Decca Type 1953** (fig. 1)

**7.** The antenna amplifier is secured by four 10-32 UNF captive screws. Anti-vibration mounts are not required and the mounting attitude is unrestricted. The antenna amplifier is mounted so that the length of the screened feeder from the antenna (Connector No. 10) does not exceed 18 inches, with an additional 6 inches of the insulated inner conductor protruding beyond the screen.

**8.** The outer screen of Connector No. 10 is bonded to the airframe at the antenna end only. At the amplifier end, the feeder screen is connected to the shell of the coaxial plug/socket (SKT 3) which is isolated from the amplifier case. The amplifier case is bonded to the airframe by a bonding tail secured beneath one of the cover retaining screws. The inner conductor of the test lead to the antenna (Connector No. 11) is connected via a series capacitor to the antenna. The

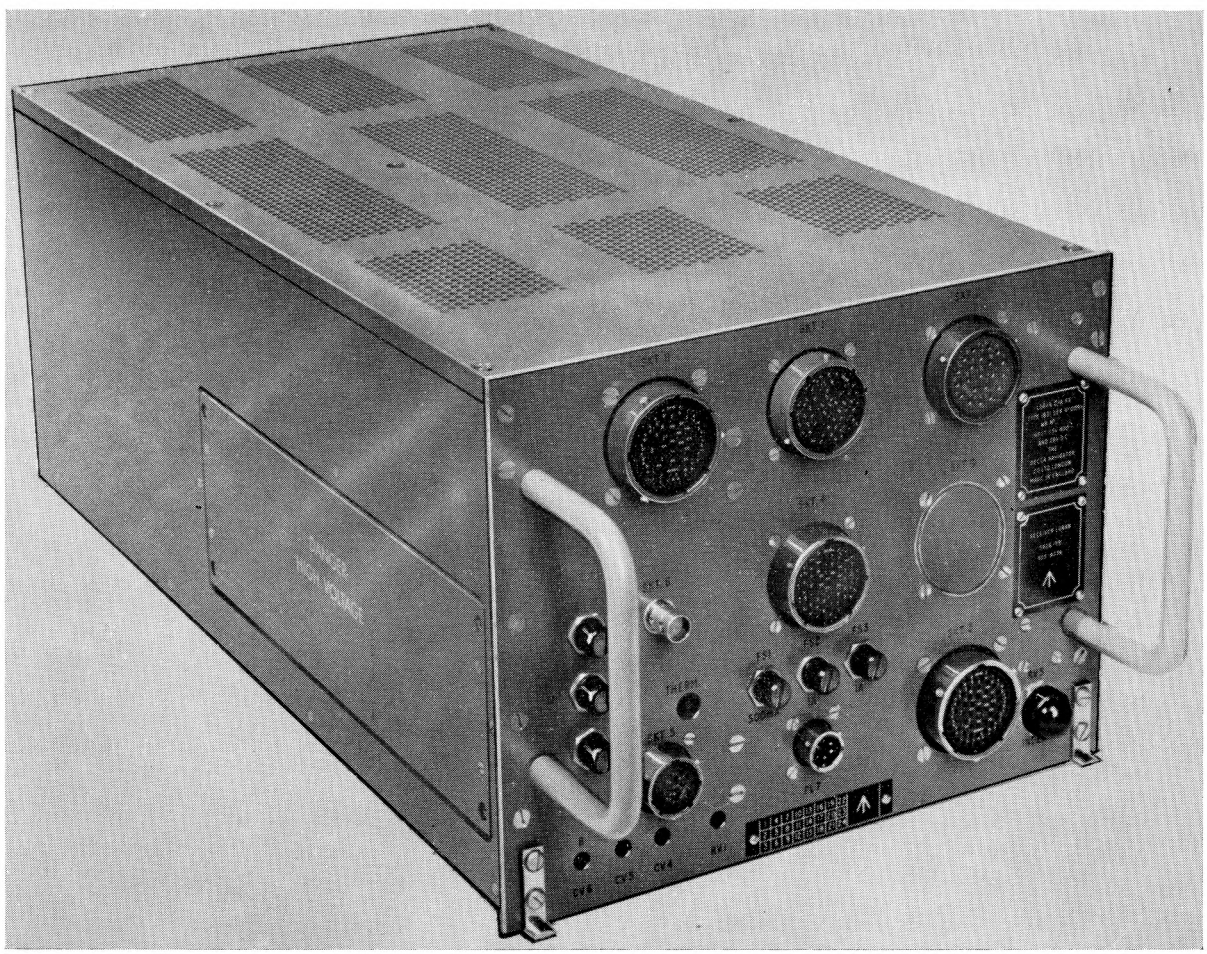

**Fig. 2. Receiver Type 1831**

outer screen of Connector No. 11 is left unconnected at the antenna end. Connectors No. 10 and 11 must not be interrupted by additional plug/socket connectors; where is it necessary to pass through a pressure bulkhead, a pressure bung is used.

**Receiver. Decca Type 1831** (fig. 2)

**9.** The Loran receiver in a 1 ATR (long) case, is secured to its mounting rack by two locking devices at the front and by two dowels on the rack which enter dowel receptacles at the rear of the unit. The receiver must be sited within the pressurized area of the aircraft. Neither anti-vibration mounts, nor forced cooling is required. Cooling is by natural convection and sufficient space must be allowed to permit a free flow of air through the holes in top and bottom of the receiver case.

**10.** All installation connections are made via plugs or sockets on the front panel of the receiver. The front panel also carries fuses, a test plug for connecting a test set and pre-set controls which are required only during ground test and adjustment procedures.

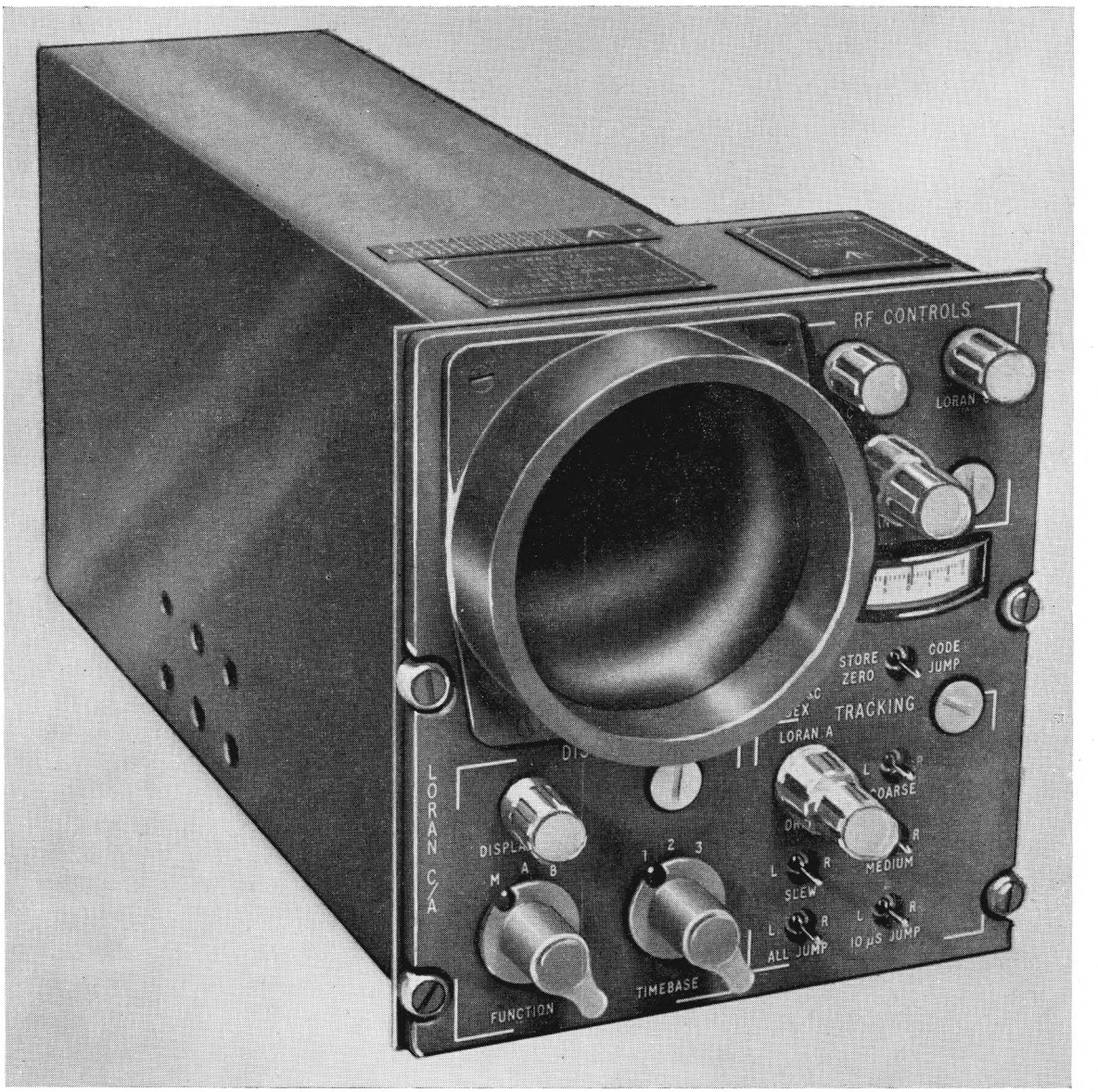


**Fig. 3. CRT Unit Type 1832**

**Cathode Ray Tube (CRT) Unit. Decca Type 1832** (fig. 3)

**11.** The CRT unit is sited so that it may be viewed and operated by the navigator or other crew member as required. Mounting attitude is otherwise unrestricted. Anti-vibration mounts are not required. The front panel conforms to the recommendations of ARINC specification No. 306, but the front-to-rear dimension exceeds the ARINC maximum. Rear support (e.g. a back-plate) must be provided to hold the unit by means of the two dowels on the rear of the unit. Electrical connections are to two plugs, of different sizes, on the stepped rear face of the unit. Note that the two cables (Connectors No. 1 and 2) between the CRT unit and the receiver should not be longer than 25 feet. During test and adjustment, access is required at the left hand side (viewed from the front) of the CRT unit, without disconnecting electrical connections.

**Read-out Unit. Decca Type 1833** (fig. 4)

**12.** As with the CRT unit (para. 11) this unit must be easily viewed and operated by the navigator (or other crew member as required). The unit conforms to ARINC specification No. 306. Mounting attitude is unrestricted and anti-vibration mounts are not required.

## INTER-UNIT CABLES

**13.** The interconnections for ARI.23180 are shown in Fig. 6. Connectors are numbered 1 to 7 inclusive and 10 and 11 (i.e. Connectors No. 8 and 9 are omitted). Details of these connectors are listed in Tables 2 to 10. Unless otherwise stated, screening braids of all connectors must be connected to the shell of the plug or socket, at both ends of the connector.

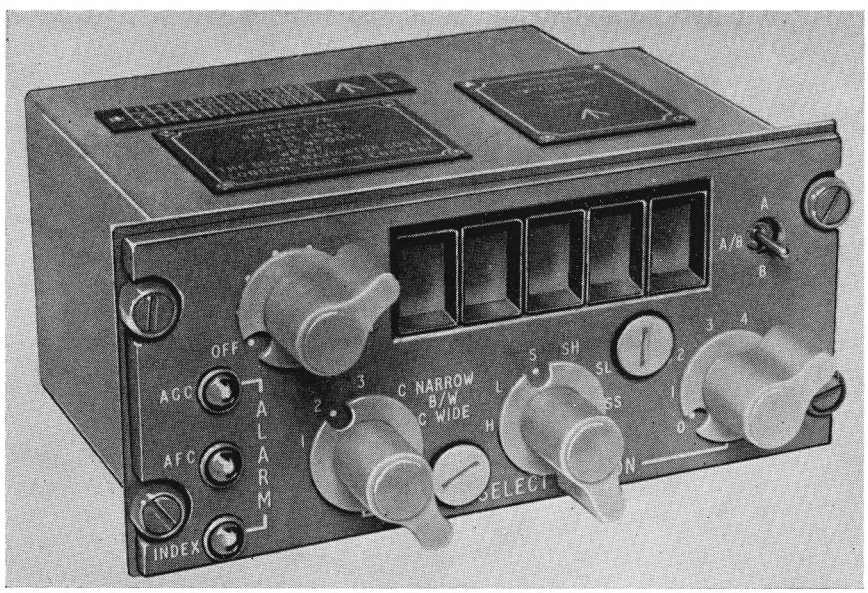


**Fig. 4. Read-out Unit Type 1833**

## TABLE 2

### Connector No. 1. Receiver to CRT unit

Cable Type : 50 × Minyvin 22

Terminations : (a) Receiver SKT1: — MS3126F-22-55PX

(b) CRT Unit PL1
ITT Cannon Electric DD50S with junction shell DD20964 (round clamp)
or DD19678-4 (straight clamp).
Male screw lock assemblies D20420-12.

Maximum length : 25 ft.

| Receiver SKT1 | CRT Unit PL1 | Receiver SKT1 | CRT Unit PL1 |
|---|---|---|---|
| A | 1 | c | 26 |
| B | 2 | d | 27 |
| C | 3 | e | 28 |
| D | 4 | f | 29 |
| E | 5 | g | 30 |
| F | 6 | h | 31 |
| G | 7 | i | 32 |
| H | 8 | j | 33 |
| J | 9 | k | 34 |
| K | 10 | m | 35 |
| L | 11 | n | 36 |
| M | 12 | p | 37 |
| N | 13 | q | 38 |
| P | 14 | r | 39 |
| R | 15 | s | 40 |
| S | 16 | t | 41 |
| T | 17 | u | 42 |
| U | 18 | v | 43 |
| V | 19 | w | 44 |
| W | 20 | x | 45 |
| X | 21 | y | 46 |
| Y | 22 | z | 47 |
| Z | 23 | AA | 48 |
| a | 24 | BB | 49 |
| b | 25 | CC | 50 |

## TABLE 3

### Connector No. 2. Receiver to CRT unit

Cable Type : 13 × Minyvin 20
2 × Nyvin 20
2 × Unimedten No. 1

Terminations : (a) Receiver SKT2: — MS3126F-22-21P

(b) CRT Unit PL2
ITT Cannon Electric DBM17 W2S with high tension inserts, DM51155 (for pins A1, A2).
Junction shell DB20962 (round clamp) or DB24659 (deep straight clamp)
Male screw lock assemblies D20419-16

Maximum length : 25 ft.

| Receiver SKT2 | CRT Unit PL2 | Wire Type | Function |
|---|---|---|---|
| A | A1 | Unimedten No. 1 | 1kV |
| B | 1 | Minyvin 20 | |
| G | 2 | ,, | 6·3V |
| C | 3 | ,, | |
| R | 4 | ,, | |
| S | 5 | ,, | −24V |
| D | 6 | ,, | |
| L | 7 | ,, | +52V |
| E | 8 | ,, | |
| X | 9 | ,, | |
| H | 10 | Nyvin 20 | −580V |
| F | 11 | ,, | −500V |
| V | 12 | Minyvin 20 | |
| M | 13 | ,, | |
| P | 14 | ,, | |
| J | 15 | ,, | |
| N | A2 | Unimedten No. 1 | 2kV |

## TABLE 4

**Connector No. 3. Receiver to read-out unit**

Cable Type : 61 × Minyvin 22

Terminations : (a) Receiver SKT3: — MS3126F-24-61P

(b) Read-out Unit PL1: — RS3126F-24-61S

| Receiver SKT3 | Read-out Unit PL1 | Receiver SKT3 | Read-out Unit PL1 |
|---|---|---|---|
| A | A | i | i |
| B | B | j | j |
| C | C | k | k |
| D | D | m | m |
| E | E | n | n |
| F | F | p | p |
| G | G | q | q |
| H | H | r | r |
| J | J | s | s |
| K | K | t | t |
| L | L | u | u |
| M | M | v | v |
| N | N | w | w |
| P | P | x | x |
| R | R | y | y |
| S | S | z | z |
| T | T | AA | AA |
| U | U | BB | BB |
| V | V | CC | CC |
| W | W | DD | DD |
| X | X | EE | EE |
| Y | Y | FF | FF |
| Z | Z | GG | GG |
| a | a | HH | HH |
| b | b | JJ | JJ |
| c | c | KK | KK |
| d | d | LL | LL |
| e | e | MM | MM |
| f | f | NN | NN |
| g | g | PP | PP |
| h | h | | |

## TABLE 5

### Connector No. 4. Receiver to Read-out unit

Cable Type : 55 × Minyvin 22

Terminations : (a) Receiver SKT4: — MS3126F-22-55P

(b) Read-out Unit PL2: — MS3126F-22-55S.

| Receiver SKT4 | Read-out Unit PL2 | Receiver SKT4 | Read-out Unit PL2 |
|---|---|---|---|
| A | A | f | f |
| B | B | g | g |
| C | C | h | h |
| D | D | i | i |
| E | E | j | j |
| F | F | k | k |
| G | G | m | m |
| H | H | n | n |
| J | J | p | p |
| K | K | q | q |
| L | L | r | r |
| M | M | s | s |
| N | N | t | t |
| P | P | u | u |
| R | R | v | v |
| S | S | w | w |
| T | T | x | x |
| U | U | y | y |
| V | V | z | z |
| W | W | AA | AA |
| X | X | BB | BB |
| Y | Y | CC | CC |
| Z | Z | DD | DD |
| a | a | EE | EE |
| b | b | FF | FF |
| c | c | GG | GG |
| d | d | HH | HH |
| e | e | | |

## TABLE 6

**Connector No. 5. Receiver to antenna amplifier**

Cable Type : 9 × Minyvinmetsheath 22
(or 9 × Minyvin 22, collectively screened and sheathed).

Terminations : (a) Receiver SKT5: — MS3126F-14-15P

(b) Antenna amplifier PL1: — MS3126F-14-15S

| Receiver SKT5 | Antenna Amplifier PL1 | Function |
|---|---|---|
| A | A | 160V + |
| B | B | 28V (Heater) |
| C | C | Test signal |
| D | D | 28V test |
| E | E | Earth |
| L | L | Earth |
| M | M | |
| N | N | |
| R | R | 28V (Loran C/A switching) |

## TABLE 7

**Connector No. 6. Receiver to antenna amplifier**

Cable Type : 1 × Transradio MC02E (or Duradio 68 — see Note 2)

Terminations : (a) Receiver SKT6: — Amphenol 31-224 (Note 2)

(b) Antenna Amplifier SKT2: — Amphenol 31-224 (Note 2)

| Receiver SKT6 | Antenna Amplifier SKT2 |
|---|---|
| 1 | 1 |
| 2 | 2 |

**Notes...**

1. *The screening braid must be earthed to the plug shell at both ends.*
2. *If Duradio 68 is used, the washer and clamp gasket of the cable-end plugs should be replaced by:* —

Washer 31GB-0114

Clamp Gasket 31-1051-02

## TABLE 8

**Connector No. 7. Power supply to receiver**

Cable Type : 4 × Nyvin 22 (or Minyvin 22)

Terminations : (a) Power Supply (via fuses or circuit breakers): — Open ends, Fittings as required.

(b) Receiver PL7: — MS3126F-10-6S

| Power Supply | Receiver PL7 |
|---|---|
| 115V 400 c/s Line | A |
| 115V 400 c/s Neutral | B |
| 28V d.c. return (earth) | C |
| 28V d.c. +ve | E |

## TABLE 9

**Connector No. 10. Antenna to antenna amplifier**

Maximum length : 18″ screened feeder (plus 6″ unscreened *)

Cable Type : T 3283 (B.I.C.C)

Terminations : (a) Antenna:

Inner conductor: 2BA eyelet tag (e.g. AMP lug) to antenna terminal.

Outer screen: 2BA Z tag (or similar) to airframe

(b) Antenna Amplifier SKT3 P.E.T. 101

* Outer screen must be stripped back 6″ from antenna terminal to avoid the risk of short circuit due to condensation in the feeder.

Earth screen to airframe at antenna end only.

## TABLE 10

**Connector No. 11. Antenna amplifier to antenna**

Cable Type : T 3283 (B.I.C.C.)

Terminations : (a) Antenna Amplifier SKT4
ITT Cannon Electric UG-260A/U

(b) Antenna

Outer screen: Not connected

Inner conductor: via a series-connected 2·7pF capacitor (Erie Type NPO.AD) to the antenna terminal.

**Note . . .**

*Outer screen must be stripped back approximately 6″ from the antenna terminal to avoid the risk of short circuit due to condensation: this screen is left un-connected at the antenna end.*

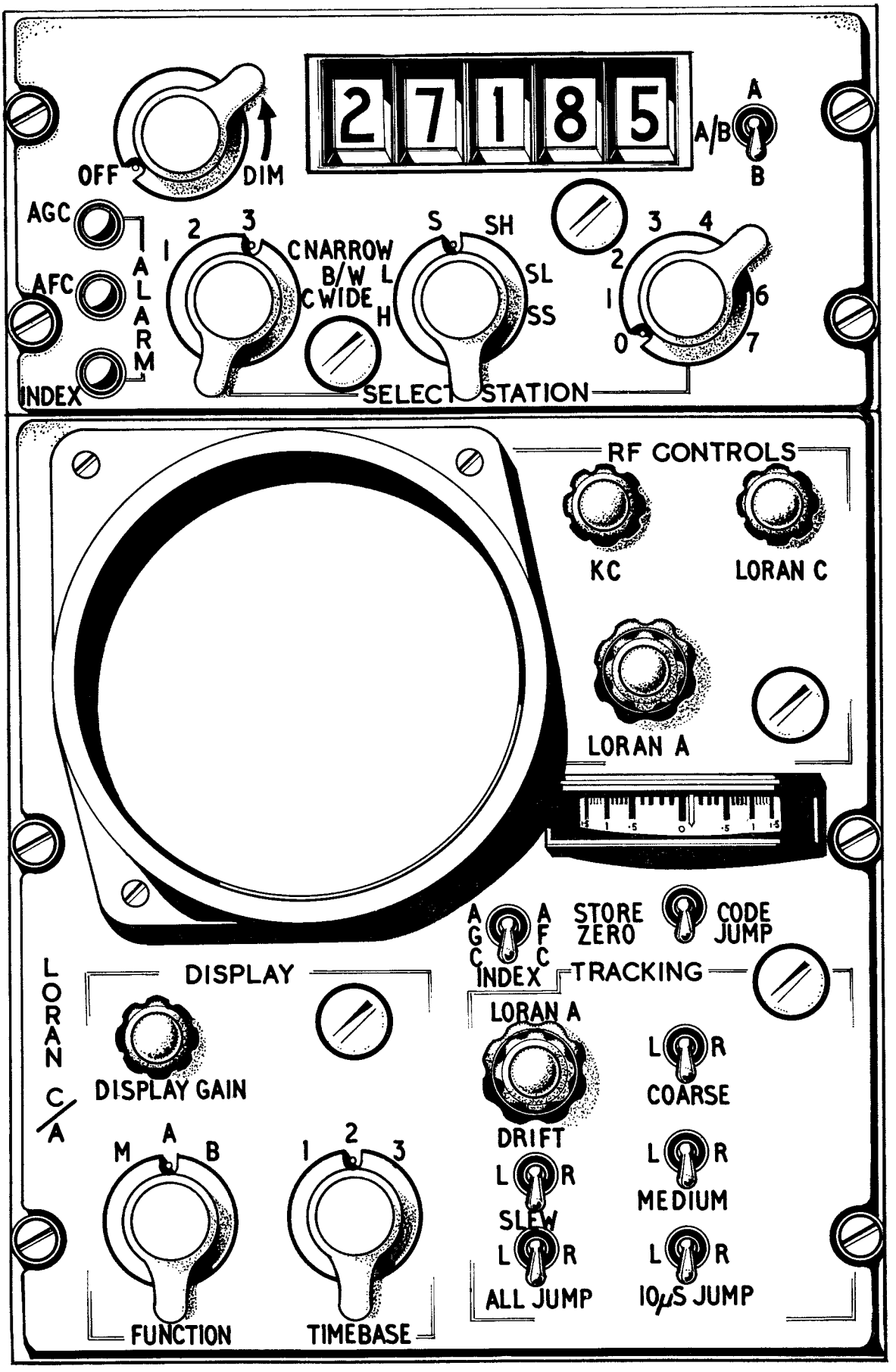


Fig. 5. ARI.23180. Operating controls

## OPERATION

**14.** All operating controls for ARI.23180 are carried either on the Read-out Unit or the CRT Unit. The functions of these controls are described in the following paragraphs (fig. 5).

### Control Functions. Read-out unit

**15.** (1) OFF/DIM. This control combines the functions of main on/off switch and panel lamp dimmer.

(2) A, A/B, B—selects time difference displayed on Read-out Unit. In position A, master-to-slave A time difference is displayed at 1 second intervals. In position B, master-to-slave B time difference is displayed. In position A/B the display alternates between A and B readings at approximately 1 second intervals.

(3) SELECT STATION. The first (i.e. left-hand) of these three switches selects the frequency (1=1950 kc/s; 2=1850 kc/s; 3=1900 kc/s, C=100 kc/s) and the bandwidth for Loran-C operation (C Narrow=6 kc/s; C Wide=20kc/s). The second and third switches select basic and specific pulse recurrence rate (p.r.r.) respectively and are common to both Loran-A and Loran-C (see Chap. 1, para. 9 and 15).

(4) A.G.C. ALARM—illuminated when a.g.c. falls below a pre-set level. This indicates a possibility of incorrect functioning due to poor signal/noise ratio, but does not necessarily mean tracking has ceased. This lamp may also light if a very strong signal is present.

(5) A.F.C. ALARM—Due to Doppler effect, the a.f.c. will vary with changes of aircraft velocity and, under extreme conditions, may not be able to cope with aircraft acceleration. The lamp lights when the a.f.c. exceeds a pre-set value indicating a possibility of incorrect functioning.

(6) INDEX ALARM—If the Loran-C pulse is incorrectly indexed, the meter pointer will be displaced. When this approaches full scale deflection, either way, the lamp is illuminated indicating either that the sampling point has slipped a cycle or that indexing was not correctly set up initially. Note that with no signal present, the index meter indicates zero (central) and the light is out.

**Notes...**

(i) *The alarm lamps may be illuminated by incorrect operation of either M, A or B channels. The channel concerned may be identified by operating the* FUNCTION *switch (CRT Unit) and observing the meter indications.*

(ii) *The alarm lamps have no significance in the Loran-A mode.*

### Control Functions. CRT Unit

**16.** (1) FUNCTION

M — selects master as timebase trigger: displays master index, a.g.c. or a.f.c. on meter; applies slew control to master.

A — as above, for A Slave.

B — as above, for B Slave (Loran-C mode only).

(2) TIME BASE

(a) In the Loran-C mode: —

(i) Displays all signals of selected chain.

(ii) Displays eight (slave) or nine (master) pulses of station selected by FUNCTION switch.

(iii) Displays eight pulses, superimposed to appear as one pulse, with individual cycles visible.

**Note...**

*Tracking gates are visible in all three positions; do not confuse these with received signals.*

(b) In the Loran-A mode: —

(i) Displays double timebase, all signals and pedestals.

(ii) Displays double timebase, but only signals within pedestals.

(iii) Superimposes signals on one timebase.

(3) DISPLAY GAIN—controls amplitude of c.r.t. display (in Loran-C mode only) by acting on input to Y amplifier. The receiver gain is unaffected.

(4) R.F. CONTROLS–LORAN A. Of these concentric gain controls, the smaller knob controls master amplitude and the larger knob controls slave amplitude.

(5) RF CONTROLS–LORAN-C. The Loran-C r.f. gain control should be at maximum (fully clockwise) except when acquiring signals.

(6) RF CONTROLS–KC. This is a notch filter control tuneable between 72 kc/s (counter-clockwise) and 125 kc/s (clockwise). It should be fully clockwise or fully counter-clockwise except when required (e.g. when an interfering signal is present—see para. 23).

(7) AGC/INDEX/AFC—Selects meter display (in conjunction with the FUNCTION switch). In general, any meter indication within the limits of half scale deflection either side of the centre zero is acceptable. When the meter approaches full-scale deflection, the appropriate alarm lamp is illuminated. When A.G.C. is selected, full left deflection indicates zero signal, full right deflection indicates a very strong signal.

(8) STORE ZERO/CODE JUMP — Spring loaded to central, 'off' position.

(a) STORE ZERO — Index, a.g.c. and a.f.c. circuits have long time-constants and faster operation is sometimes possible if the stores are 'zeroed' manually.

(i) INDEX. If lock is obtained on a cycle high in the pulse, the index meter will be deflected hard right. If third cycle is now selected, some time will elapse before the meter centralises. Zeroing the store will centralise the meter much faster, to indicate selection of the third cycle.

(ii) A.G.C. If a very strong signal is put into the gates (e.g. R.F. gain control set too high), the a.g.c. circuits may be overloaded, reducing the receiver gain to the point where the a.f.c. circuits will not lock. Reducing R.F. gain and switching to STORE ZERO (with AGC/INDEX/AFC to AGC) will restore lock. Similarly the STORE ZERO facility may be useful when switching from a very strong slave signal to a very weak signal.

(iii) A.F.C. As in (ii) above, the sudden acquisition of a very strong signal may overload the a.f.c. circuits which then acquire a bias, indicated by a hard left, or hard right, meter indication. Although such a bias will decay eventually, switching to AFC and STORE ZERO will save time.

**Note...**

*Only the store selected by* AGC/INDEX/AFC *switch for the station* (M, A *or* B) *selected by the* FUNCTION *switch is zeroed.*

(b) CODE JUMP—Setting this switch briefly to CODE JUMP changes the phase coding applied to Loran-C signals.

(9) LORAN-A DRIFT. These concentric controls are used to stop Loran-A signals drifting along the time base. The smaller knob controls the master oscillator and the larger knob controls the slave oscillator.

(10) SLEW L-R. Drifts Loran-A slave signal very slowly to left or right for accurate alignment with the master signal. This switch, together with the other tracking switches (items 11 to 14 below) are spring-loaded to the central 'off' position.

(11) COARSE L-R. Drifts selected signal rapidly to left or right.

(12) MEDIUM L-R — drifts selected signal slowly to the left or right.

(13) 10$\mu$S JUMP — jumps selected signal in 10$\mu$S steps (= 1 cycle steps for Loran-C) to the left or right.

(14) ALL JUMP — as (13) above except that all signals are jumped in 10$\mu$S steps.

**Note . . .**

*Toggles of switches* (7), (8) *and* (10) *to* (14) *are spring-loaded to centre and have left/right movement.*

**Pre-set Controls. CRT Unit**

**17.** At the left-hand side of the CRT unit (viewed from the front) are pre-set controls for brilliance, focus and astigmatism. Separate controls are provided so that these qualities may be separately set up for TIMEBASE 1 and TIMEBASE 2/3.

**Operating. Loran-C**

**18.** Switch on and select required chain. The digital read-out will appear almost immediately but approximately 10 minutes will be required for the crystal oven to attain operating temperature.

**19.** Set control positions:—

(1) FUNCTION — M

(2) TIMEBASE — 1

(3) DISPLAY GAIN — Fully clockwise

(4) R.F. CONTROLS. LORAN-C — Turn down to the point where the receiver is not overloaded (as evidenced by 'flat-topping' of noise or signal pulses.

(5) R.F. CONTROLS. KC — Fully clockwise or fully counter-clockwise.

(6) AGC/INDEX/AFC—A.G.C. — INDEX

(7) L.H. SELECT STATION — C NARROW

*Master Acquisition*

**20.** Look for the master signal on c.r.t. (a nine-pulse signal with ninth pulse offset by twice the spacing between the other eight). If master signal is not present proceed from para. 22. If master is present, then: —

(1) Use tracking controls COARSE and MEDIUM, to drift master signal to left of trace so that the first pulse coincides with the start of the timebase.

(2) Check that the three sets of eight gates, appearing as blocks of short vertical 'blips' above the timebase, do not overlap or are too close together (this is easier to see if DISPLAY GAIN is temporarily reduced to zero). If they are too close: —

(a) Set FUNCTION switch to A, read-out A, A/B, B switch to A and use COARSE and MEDIUM tracking switches to set read-out to approximate estimated time difference for A slave.

(b) Set FUNCTION to B, read-out A, A/B, B switch to B and set approximate time difference for B slave.

(c) Return FUNCTION to M.

(3) Set TIMEBASE to 2 and observe a single block of eight gates. Align signal pulses with gates using MEDIUM tracking switch.

(4) Set TIMEBASE to 3 and observe a single pulse and gate. Align gate on third cycle, using 10μS JUMP switch. If pulse has appearance of two interlaced sine waves, operate CODE JUMP once and pulse should return to normal.

Note...

If pulse is still abnormal:

(a) Slave has been misinterpreted as Master, or

(b) the eight pulses are not aligned with the gates (e.g. only seven pulses in), or

(c) gates are still overlapping.

Slave acquisition

21. Having acquired master, select the two slaves which are within range and which give position lines with the best angle of cut. Note the approximate time differences expected, then:

(1) Set TIMEBASE to 1 and both FUNCTION and A, A/B, B to A. Operate COARSE and MEDIUM tracking to set one of these readings on the Read-out Unit.

(2) Set TIMEBASE to 3. The selected A slave pulses now appears approximately aligned with the gates. Proceed for A slave as for master acquisition, para. 20(3) and (4).

(3) Set FUNCTION and A, A/B, B to B and repeat (1) and (2) above, for B slave.

(4) Set RF CONTROLS-LORAN C to maximum (fully clockwise) and set left hand SELECT STATION (Read-out Unit) to C WIDE. Check meter deflection (AGC/INDEX/AFC switch still at INDEX). If third cycle has been correctly selected, meter pointer is central; if second cycle has been selected, pointer drifts to left or if fourth cycle, pointer drifts to right.

Note...

There is a long time-constant in the Index system and, with weak signals, a few minutes may elaps before a reliable meter indication is displayed. If the pointer is hard left, or hard right, set STORE ZERO/CODE JUMP to STORE ZERO for 10. The pointer will centralise and, on the switch being released, will give a quicker indication of whether or not the correct cycle has been selected.

(5) Check A.F.C. on meter. For an aircraft on the ground, the pointer should be central and steady; in flight, pointer may show a constant deflection either way.

master signals

. If the master signals are not visible, there may still be sufficient gnal to maintain lock and tracking, but in this case it will be necessary lock in initially to a slave signal. (This is necessary over most of e UK for example). It will usually be known which slave is the one sible from a consideration of the ranges and the expected time differences r this slave should be worked out as accurately as possible, then:

(1) Set FUNCTION to A and, using COARSE and MEDIUM, drift the slave signal pulses to the left of the timebase.

(2) Set FUNCTION to M and, with A read-out selected on the Read-out Unit, operate COARSE and MEDIUM to display the estimated time difference.

(3) Check that the gates are not overlapping, (para.20(2)) but note that only the B gate need be moved; neither M nor A should be altered.

(4) Lock in the A slave as in para.20(3) and (4).

(5) Re-check time difference set in for A and reset if necessary by setting FUNCTION to M and using tracking switches.

(6) Set TIMEBASE to 3 and FUNCTION to M. It may now be possible to see some signal (try setting left-hand SELECT STATION to C NARROW), and if so, set the gate into the strongest part of the pulse. This enables the a.g.c. and a.f.c. circuits to acquire, but will not place the gate on the right cycle. Since the third cycle is almost inevitably buried in the noise the only guide to acquiring the third cycle is the index meter.

(7) The index meter will not be to the right and the pulse should be jumped through the gate by operating 10μS JUMP to the right, one cycle at a time, until the index meter reads centrally. Use STORE ZERO to obtain a quicker reading (see Note to para.21(4)). If the aircraft is on the ground, the best indication of satisfactory tracking is a more-or-less constant read-out (fluctuating over 1 or 2μS, but not drifting). The A.G.C. lamp will probably be on but this is no indication that tracking is not taking place.

(8) The third cycle may be so far down in noise that tracking on it is not possible and the effect will then be that, as the pulse is jumped through the gate, tracking is lost before the correct time-difference reading (appropriate to master and slave being on the same cycle) is attained. In this case, leave the master gate on a cycle on which tracking is maintained, and jump the slave pulse further into the slave gate, using 10μS JUMP until the correct reading is restored.

(9) A second slave may now be chosen and acquired, remembering that if M and A are now tracking on the fourth or fifth cycles, third cycle indexing on B will not give the correct time difference read-out.

Use of notch filter

23. If interference due to another transmitter is seen on the c.r.t. display (usually a coherent pattern instead of random noise) it may be possible to eliminate this by use of the notch filter (RF CONTROL - KC). Tune KC carefully through the frequency range and set to the position of minimum interference but, if possible, avoid leaving it in the 100 kc/s position where receiver operation may be adversely affected.

Operating Loran-A

24. When operating in the Loran-A mode:

(1) Manually realign the received pulses each time a time difference reading is taken.

(2) Leave the A/A/B/B switch on the Read-out Unit in position A.

(3) The ALARM lamps have no significance.

25. To obtain a position line (time difference reading):

(1) Switch on and allow 15 min for the ovens to warm up. Set SELECT STATION switches for the desired Loran-A pair: left-hand switch - channel frequency; centre switch - basic rate; right-hand switch - specific rate.

(2) Set FUNCTION to M, TIMEBASE to 1 and adjust r.f. gain control LORAN A to obtain a clear picture.

(3) Operate tracking COARSE and MEDIUM so that one pulse is obtained on each trace, with the bottom pulse to the right of the top pulse.

(4) Operate MEDIUM or 10μS JUMP to slew top pulse to left-hand edge of timebase, on to the pedestal.

(5) Set FUNCTION to A and operate MEDIUM to slew bottom pulse over bottom pedestal.

(6) Set TIMEBASE to 2 and operate TRACKING MEDIUM to slew M and A in turn (FUNCTION to M or A) until both are positioned left or central on pedestal, i.e. "strobe" the pulses.

(7) Set TIMEBASE to 3 and operate SLEW and/or 10μS JUMP to drift master and slave pulses into precise alignment. Adjust r.f. gain control LORAN A so that both pulses are of the same amplitude.

(8) Read the time difference displayed on the Read-out Unit.

Note...

If the signals drift steadily to right or left on the c.r.t., adjust LORAN A DRIFT controls to eliminate this drift. The small knob controls the master oscillator and the large controls the slave oscillator.

# PART 2

# TECHNICAL INFORMATION

# Chapter 1

# AERIAL AMPLIFIER TYPE 1953

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## LIST OF ILLUSTRATIONS



## Introduction

**1.** The aerial amplifier Type 1953 (amplifier antenna Ref. 5826-99-955-8339) is mounted adjacent to the Decca aerial; it has the primary function of isolating the aerial, which forms inherently a high impedance source, from the necessarily long and high capacitance feeder to the receiver.

## Circuit details

**2.** The amplifier comprises a single stage embodying two high-gm pentodes V1, V2 in parallel, resistance-capacity coupled from the aerial and transformer coupled to the receiver feeder line. The control grids are held at approximately 10·2 volts by connecting R3, the grid resistor to the junction of R4 and R5, a potential divider across the positive h.t. supply. The isolating capacitor C1 is included to prevent any change in this potential occurring in the event of low aerial leakage current. A d.c. return for the aerial is formed by R1, to avoid any static charges being built up on the aerial. The coaxial input cable is grounded to the aircraft skin immediately surrounding the plate aerial, and to the sub-chassis immediately adjacent to V1; the input socket is isolated from the amplifier baseplate and grounded only at that point. In this way, only the aerial signal voltage appears directly across the grid/cathode circuit of the two valves: local noise generated across any series impedance in the amplifier frame ground connection can only be fed into the grid/cathode circuit via R5 or R9. The ratios of these resistors to the r.f. impedance of the associated decoupling capacitors C2, C3 is such that negligible signal transfer occurs in practice.

**3.** The amplifier circuit is conventional, save for the use of carefully determined values of d.c. and r.f. feedback, provided by cathode degeneration, employing R9, C3 plus R6 and R12. The positive

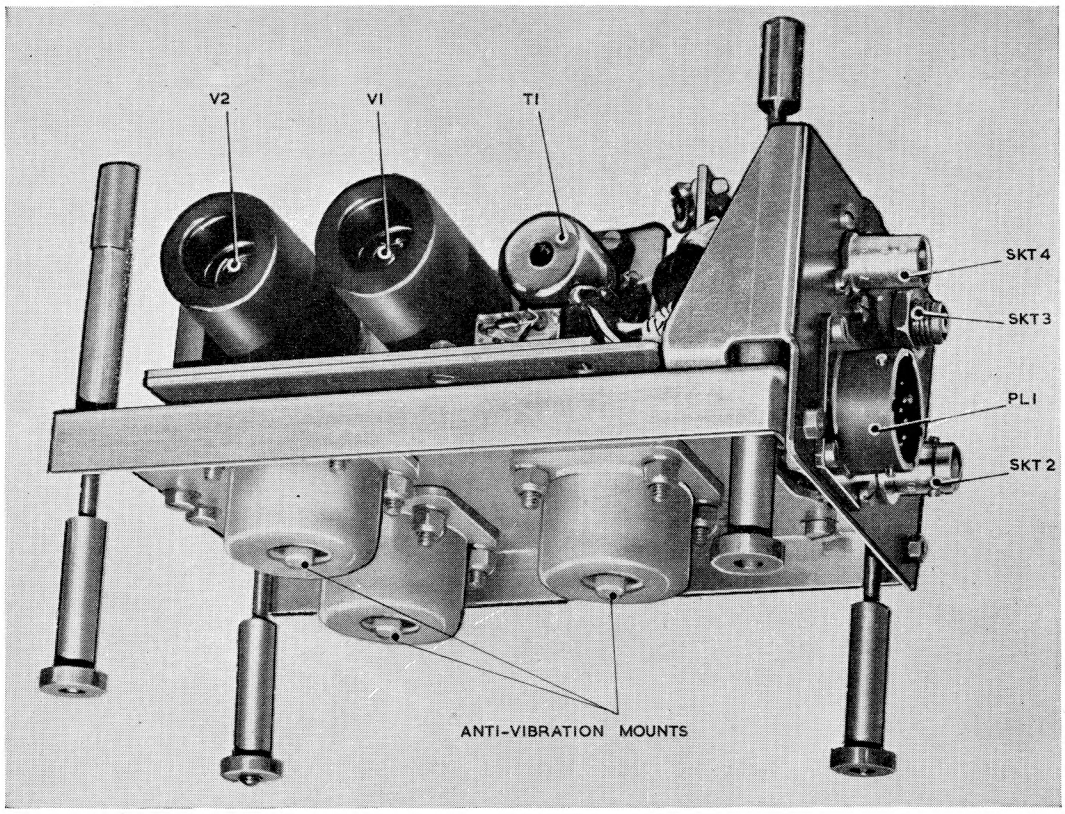



**Fig. 1. Component location (side view)**

control-grid bias, already mentioned, offsets the effect of the high cathode resistance on valve operating conditions and restores V1, V2 to the optimum point of their Vg. Ia curve. The combined feedback makes the amplifier less susceptible to changes in valve characteristic and also provides valuable current-limiting protection in the event of abnormal operation; for example, when a large positive input pulse drives the valves into grid current. The amount of r.f. feedback has been chosen so that the grid and anode overload points coincide at the same input level: the amplifier is then substantially linear up to 1V r.m.s. input. The input capacitance is reduced to between 25 and 30pF total at this optimum feedback level.

**4.** Coupling from the relatively high impedance anode circuit to the feeder lines is provided by ferrite-cored transformer which are brought into circuit by relay contact RLA.1. With Loran C operation selected at the c.r.t. unit RLA remains de-energized, T2 primary winding is then connected in circuit by the normally closed contact RLA.1; the normally closed contact of RLA.2 provides a short circuit to the Loran A transformer secondary winding (T1), T2, which has a turns ratio of 6:1, is designed to be used between 70-130 kc/s. With Loran A operation selected on the c.r.t. unit, relay RLA operates, T1 primary winding is selected by the normally open contact of RLA.1 and T2 secondary winding is shorted by the normally open contact of RLA.2. T1 has a turns ratio of 6:1 and is designed to be used between 1·8-2·5 Mc/s. The 100 ohm secondary load R13 is included to stabilize the phase characteristic of the unit, and it renders the amplifier substantially independent of output loading conditions. With the effective anode load of 10 K thus provided, the stage gain is 60 and the overall amplifier voltage gain is of the order of 6.

**5.** Provision is made for use in both 'dorsal' and 'ventral' aerials, these being defined as those normally above and below the electrical centre of the aircraft respectively. For 'dorsal' operation, the 180° phase change introduced by the single amplifier stage is taken out in the transformer, whilst for 'ventral' operation, reversal of the transformer secondary connections retains this phase change, compensating for the 180° reversal in received signals, inherent when the aerial is below the aircraft's electrical centre. The amplifier baseplate and case, which are bonded to the aircraft frame, are connected also to one side of the transformer secondary winding.

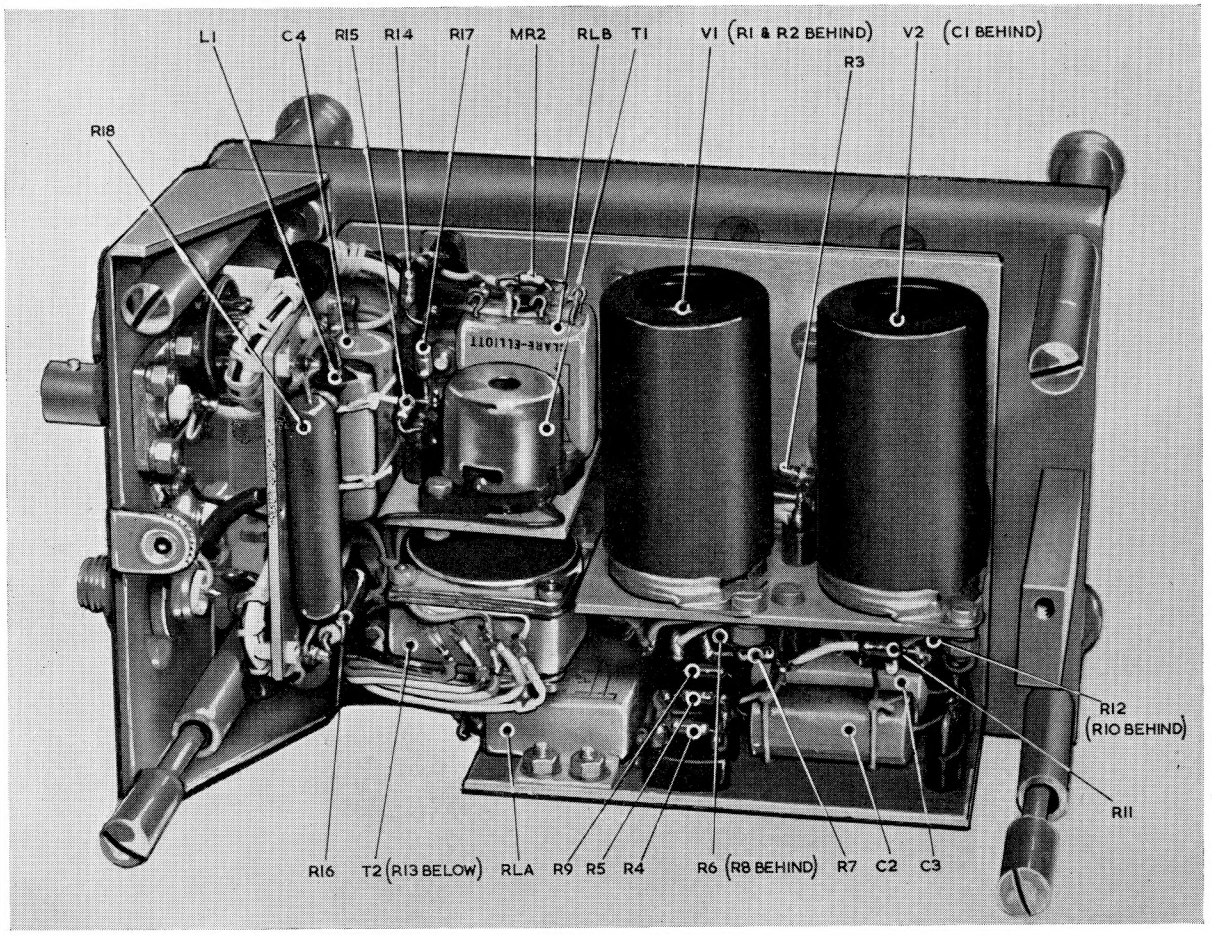


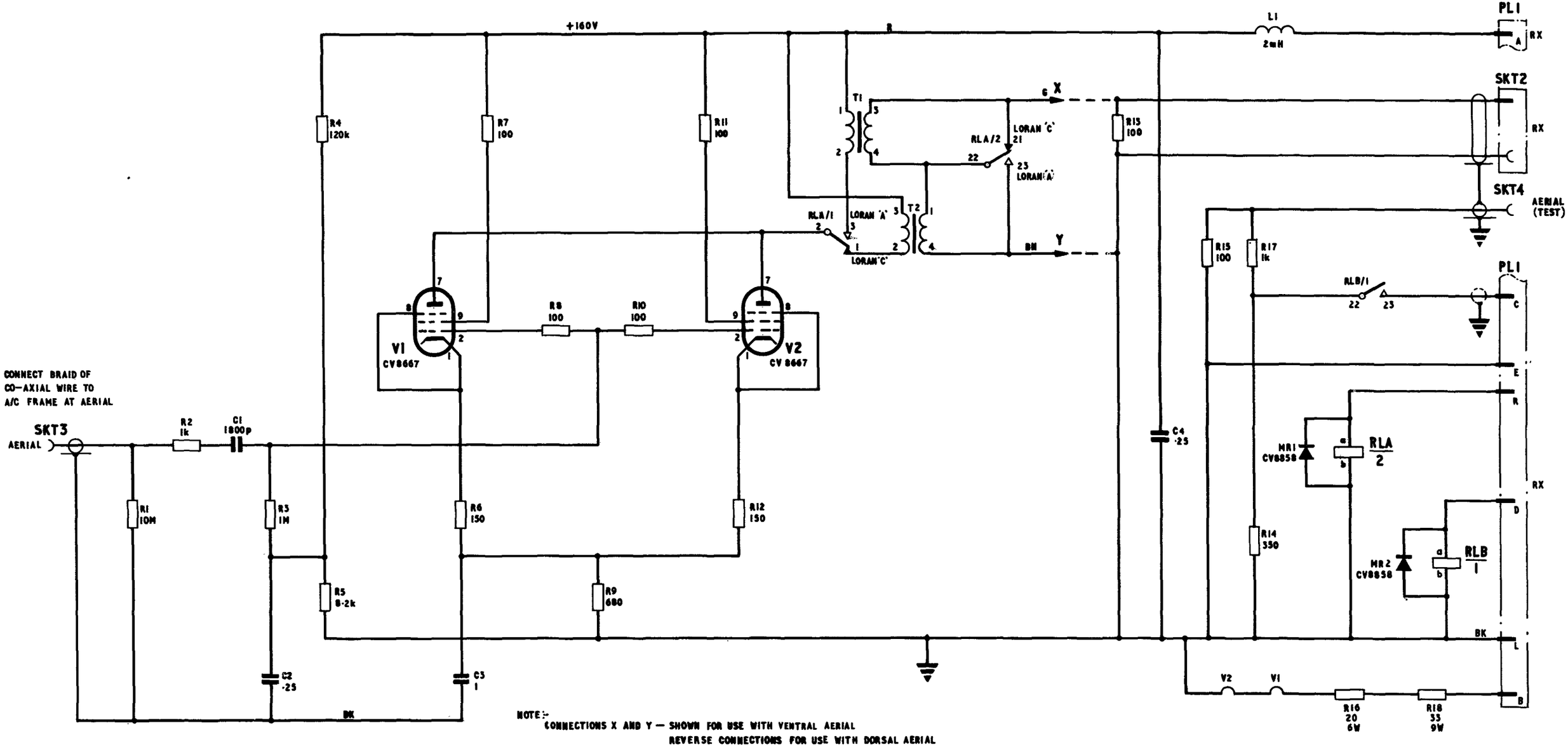

**Fig. 2. Component location (top view)**

**6.** Power supplies drawn from the power unit of the receiver are:

16 to 18 mA at +160V (nominal h.t.)
and 0·3A at 28V, heater supply.

The latter supplies the two 6·3 volt heaters in series, excess voltage being dropped in a 53 ohm series resistance comprising R16 and R18.

**7.** Relay RLB is operated when the first line test set (Test set, Loran 6625-99-107-1415) is used to verify the correct operation of the complete ADL21 receiver. RLB.1 will close, connecting the test signal applied to pole C of PL1 across R14 and across the potential divider network R15 and R17. The output from this 10:1 voltage divider is then coupled via the aerial (test) socket SK4 to the test stud on the aerial. Signal can then be taken from the main stud on the aerial to the aerial amplifier input circuit as in the normal condition of operation; the aerial amplifier output will then be coupled to the receiver in the normal way.




Aerial amplifier Type 1953 : circuit

Fig.3
S.P. 546852

# Chapter 2

# RECEIVER, LORAN (DECCA TYPE 1831)

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## LIST OF TABLES



## LIST OF ILLUSTRATIONS



**Note**—*Fig.* 5 *to* 34 *will be found in A.P.* 116*B*-0610-10.

## Introduction

**1.** The receiver unit (Receiver Loran Ref. 5826-99-955-8336) has been designed to process Loran C/A master and slave signals in order to present the read-out unit with a time difference measurement corresponding to the aircraft's position. Except for ancillary circuitry, the circuits within the receiver are on plug-in printed circuit boards, the operation of which are separately described in this chapter. The board titles, reference letters and numbers are listed, in the order they appear in the chapter, in Table 1. Connections from the various circuits within the receiver to the aerial amplifier, c.r.t. unit and read-out unit are made via sockets on the receiver front panel. Where connections are to be made between the read-out unit and the c.r.t. unit, these are also made via the receiver unit to minimize the number of inter-unit connections. Socket 8 on the front panel is provided to enable functional checks to be carried out when using the first line test set.

**2.** There are no operator controls on the receiver unit, permitting it to be located in the aircraft in an out of the way location, but preset controls that are accessible on or through the front panel (fig. 1) are provided as follows:—

(1) The INDEX control RV5 selects the cycle of the received pulse on which the index meter will read zero when the receiver is locked into the signal.

(2) The oven temperature control RV1.

(3) The master, slave A and slave B crystal oscillator trimmers CV4, CV5 and CV6.

Three supply fuses are provided, there being one fuse in each primary feed to the mains transformers T1 and T2, and one fuse in the 28V supply line to the panel lamps. Internal views showing component location are given in fig. 2 and 3.

### *Terminology*

**3.** Terminology relating to signals used in the circuit description of this receiver is given below. the time relationship between waveforms can be seen from fig. 5.

| | |
|---|---|
| ±MTS | An 8 mS master time shared pulse occuring once per selected pulse repetition rate. |

**TABLE 1**

**Board Reference Numbers**

| Reference Letter | Title | Reference Number |
|---|---|---|
| X | Loran C r.f. strip | 5826-99-956-5922 |
| U | Loran A r.f. strip | 5826-99-956-5920 |
| T | Coder | 5826-99-956-5906 |
| H | Index | 5826-99-956-5914 |
| K | A.F.C. | 5826-99-956-5916 |
| FW | A.G.C. | 5826-99-956-5908 |
| J | Oscillators and dividers | 5826-99-956-5918 |
| HH | Variable capacity diodes | 5826-99-956-5876 |
| JJ | Crystal oven and drive | 5826-99-956-5874 |
| KK | Tagboard | 5826-99-956-5968 |
| L | Slew circuits | 5826-99-956-5900 |
| M | Master pedestal generator | 5826-99-956-5904 |
| FN | Master pedestal generator | 5826-99-956-5902 |
| P and (R) | Slave pedestal generator | 5826-99-956-5879 |
| Q and (S) | Slave pedestal generator | 5826-99-956-5878 |
| E | 10 Mc/s counter and readout | 5826-99-956-5912 |
| F | Counter | 5826-99-956-5910 |
| G and (MM) | Counter | 5826-99-956-5882 |
| Y | Power supply ±12V −24V ±6·6V | 5826-99-956-5967 |
| Z | Power supply receiver unit | 5826-99-956-5924 |
| FF | Supply filter | 5826-99-956-5875 |
| EE | Power supply c.r.t. unit and aerial amplifier h.t. | 5826-99-956-5923 |

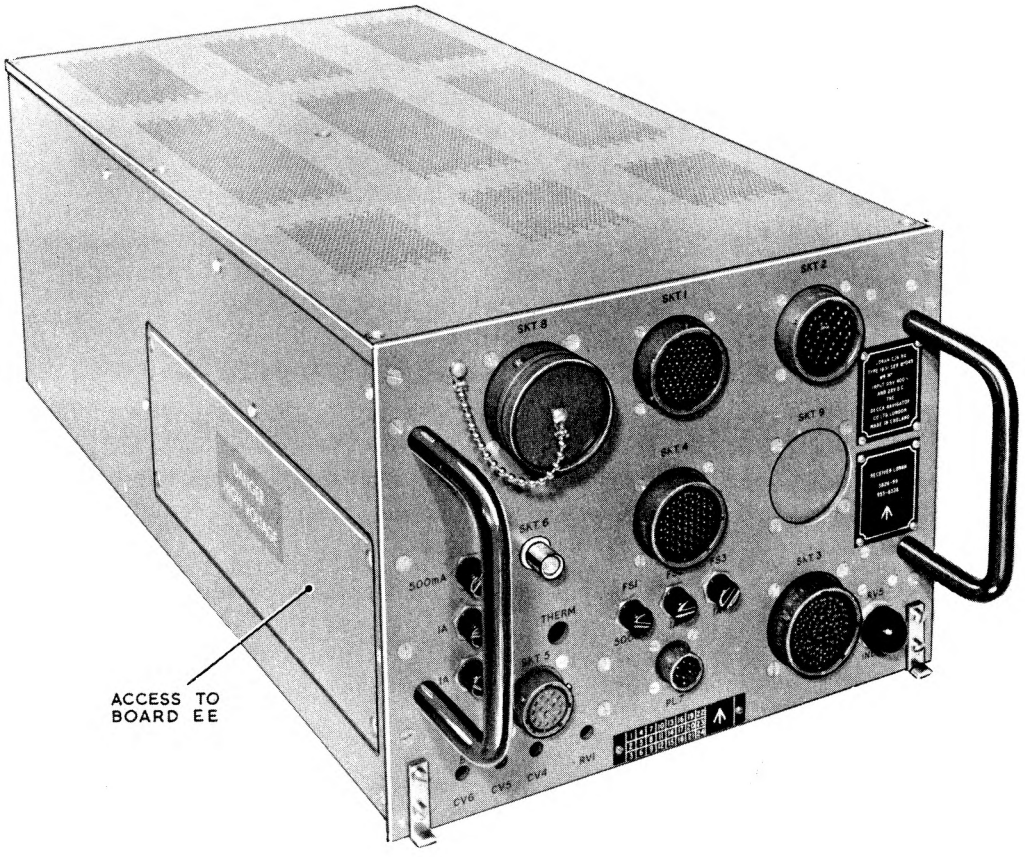


Fig.1 Receiver, general view

| | |
|---|---|
| ±ATS | An 8ms slave A time shared pulse occurring once per selected pulse repetition rate. |
| ±BTS | An 8ms slave B time shared pulse occurring once per selected pulse repetition rate. |

+MTS, +ATS and +BTS are coincident in time with -MTS, -ATS and -BTS but a phase inversion is applied to the pulses.

| | |
|---|---|
| MST, AST and BST | These are master, slave A or slave B 10µs scope triggers and arrive 15µs after their master, slave A or slave B time-sharing periods. |
| Tracking gates | These eight pulses are 4.5µs long and are derived from the master, slave A and slave B tracking gates that are supplied by K, Q and S boards. |

| | |
|---|---|
| 1ms gates | These 1ms pulses are derived from the respective master, slave A or slave B decade dividers. The pulses read the AFC, AGC and INDEX store voltages. |
| Digitiser trigger | These pulses, which are of 1μs duration, are derived from the master, slave A and slave B dividers respectively; their function is to start and stop the read-out unit counters. These pulses have a 45μs lead on the first tracking gate pulse of each of the master, slave A and slave B groups. |
| Master and Slave full rate Pedestal | This is a 3μs pulse occurring once per pulse repetition rate. They are used to reset the pedestal generators and coder bistables. The pulse is coincident with the start of MTS. The slave A pedestal will therefore be coincident with the start of ATS. |
| ½ INT. PED | This is a 100μs pulse occurring 4ms after the start of MTS, this being half of the 8ms MTS period; the main functions of the pulse being to time-share the gain of the Loran A rf strip and to switch the trace on the crt unit. |
| 100 kHz clock | These are 100 kHz square wave signals that are produced by the crystal oscillator circuit (board J). These are the signal sources for the master, slave A and slave B decade dividers. |

Loran C rf strip (board X)

4. There are effectively four separate circuits on this board (fig 15):

100 kHz rf signal amplifier
Phase decoder
AGC noise limiter
Index derivation.

The received Loran C signal arriving at T1 from the aerial amplifier is fed to notch filter T2, C1 and MR1 which normally eliminates coherent pattern interference from the crt trace. It is tunable from 78 to 123 kHz. At its 3dB rejection points it has a bandwidth of 5½ kHz and at its 20dB rejection points a bandwidth of 1 kHz. Frequency is adjusted by changing the reverse bias on variable-capacity diode MR1. RV1 provides this bias and is on the front panel of the crt unit designated KC. The signal from the notch filter is fed to a current-sharing amplifier of constant input impedance. With low agc the base voltage on VT2 becomes more positive, so the emitter potential rises to cut off VT1. The current from the choke-coupled stage is then routed via VT2 through isolator VT3 to tuned load T3, C7 and R7. This reshapes the signal pulse before passing it to the next stage. Another choke-coupled stage feeds a second current-sharing amplifier VT4/VT5, this stage being almost the same as the first. The tuned circuit in the collector of VT6 supplies one of two choke-coupled stages via contact RLA/1. L3 and C13 provide a narrow-band characteristic and L4 and C17 provide a wide-band characteristic. For the use of these bandwidth filters see Pt.1, Chap.2, para 8.

5. Two further stages of amplification using current-sharing amplifiers are used, the first, VT7/VT8, being the bandwidth control amplifier, the second, VT11/VT12, being the driver circuit for the decoding stage. The signal is decoded by VT13 and VT14. Decoding means the phase correction of a transmitted signal whereby the leading edge of each pulse after correct decoding is positive-going. Further details are in Pt.1, Chap.1, para 10 and 11.

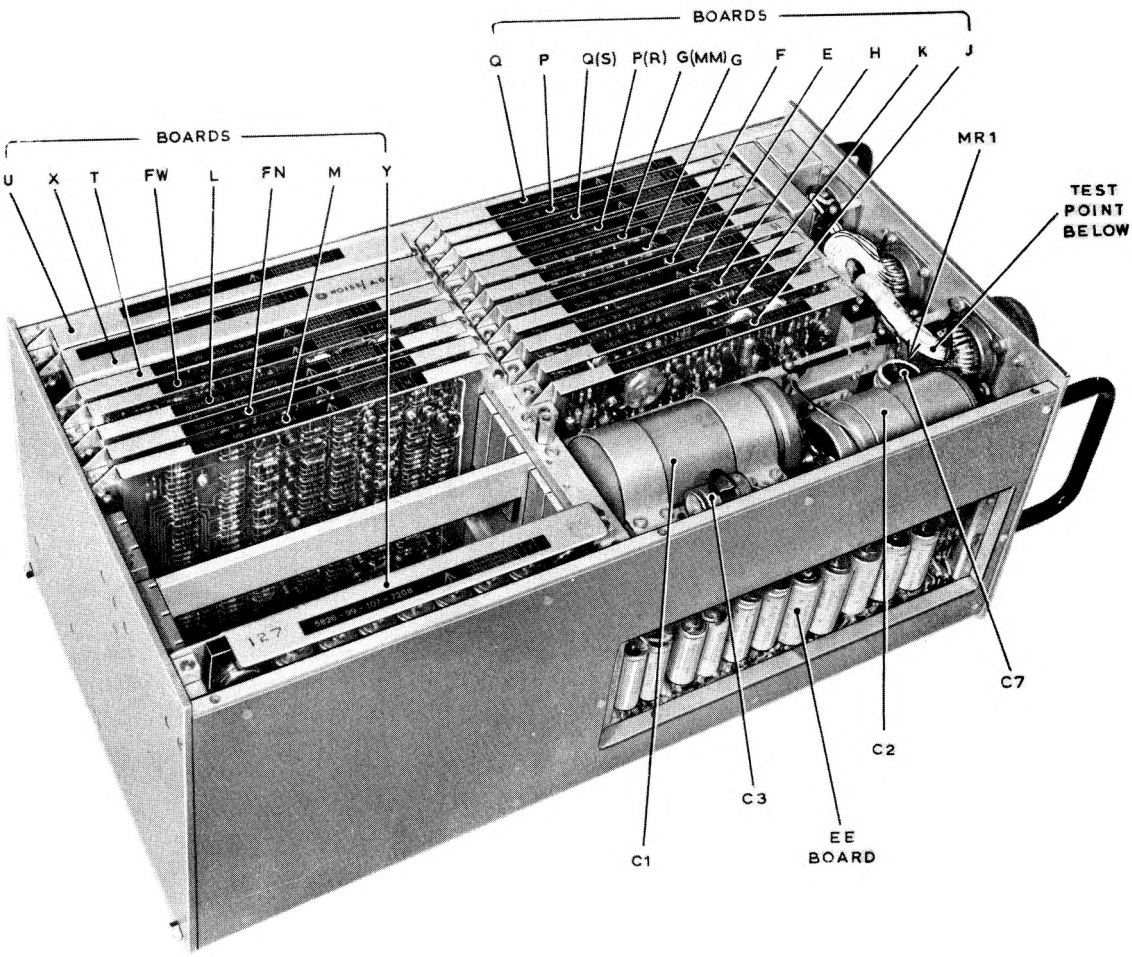


Fig.2 Receiver top view, case removed

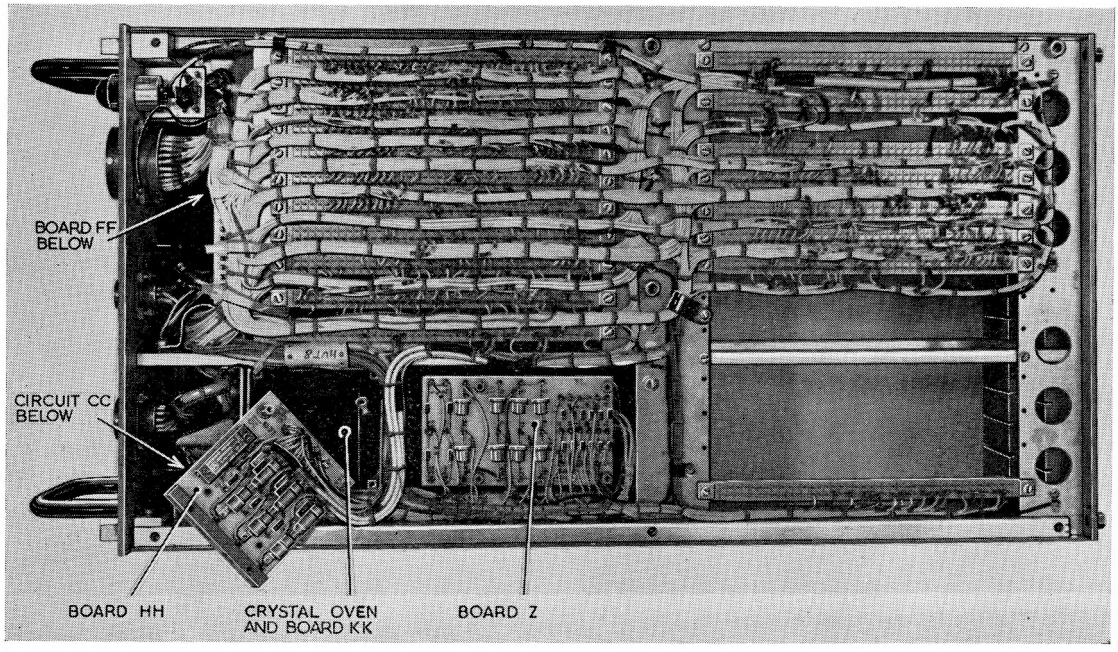


**Fig. 3 Receiver underside view, case removed**

Where the first cycle of an incoming pulse is already positive going, VT14 is switched on by a coding pulse from the decoding circuit board T; no phase inversion will take place. If the first cycle of the incoming pulse is negative going then the coding pulse switches on VT13 providing a 180° phase inversion, If the group of received pulses do not correspond to the coding applied to VT13 and VT14, then the resultant output pulses will be of incorrect polarity; this would normally be due to incorrect acquisition of the signal. The decoded output from T7 is coupled via the tuned current-sharing amplifier VT15 and VT16 and VT17 to the output transformer T10. The zener diodes MR18 and MR19, across the primary winding of the output transformer T10, limit the primary voltage swing to approximately 10 volts. The transformer is used to couple the output a.f.c. waveforms to the a.f.c. determining and time-sharing circuits (board K) and to feed the 90° phase shift circuit. This phase shift represents a $2\frac{1}{2}\mu$S delay and ensures that the a.f.c. channel, which is undelayed, has locked before a.g.c. and indexing is carried out.

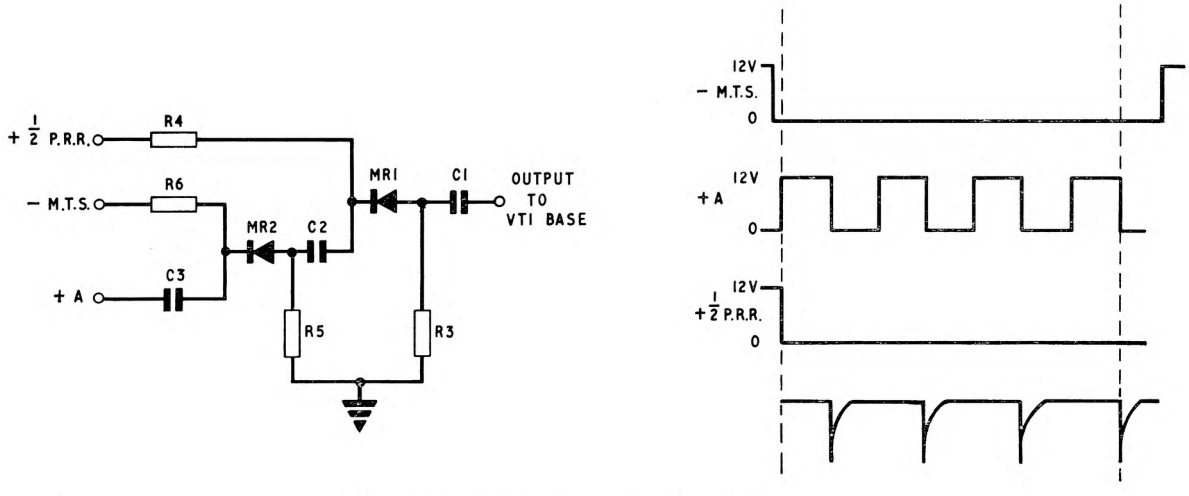


**Fig. 4 Part of coder gate circuit, board T**

*Index derivation*

**6.** The index waveform is produced by adding a delayed signal to an undelayed signal of lower gain; the crossover point of the two pulse envelopes then occurs at the third cycle within the r.f. pulse. Further details are given in Pt. 1, Chap. 2, para. 16. The signal at the emitter of the buffer stage VT18 is coupled directly to the delay circuit L6, C46 and T8, and is coupled via transformer T9 to the a.g.c. determining and time-sharing circuit. Connected to another secondary winding on T9 is the resistive network used to control the amplitude of the undelayed signal, this preset control being on the front panel of the receiver unit. The preset signal, controlled by the setting of the INDEX control on the receiver front panel, is added to the delayed signal appearing at T8 secondary winding and is then amplified by V20. The index waveform is then fed via a buffer amplifier VT21 to the index circuit, Board H.

*Noise a.g.c. circuit*

**7.** The gain of the r.f. amplifier is a minimum until a time-shared a.g.c. pulse arrives at pin 23. This then removes the clamping effect on VT26 and allows the feedback voltage from the output to control the gain of the receiver. The r.f. signal from VT17, which is fed via the emitter follower VT22, is full-wave rectified by MR16/MR17 and smoothed by C41. An increase in output from the r.f. amplifier causes an increase in the negative voltage applied to VT25 base, turning on VT25. VT26 conduction is then reduced causing the a.g.c. voltage to go less positive; this reduces the overall gain of the r.f. amplifier. The time-shared a.g.c. voltages from Board FW (these being the mean voltages obtained during a 4·5$\mu$S sampling period) are fed to VT26 base circuit via MR11. This voltage, which can vary between +3 and +12 volts, overrides the noise a.g.c. circuit and thus provides an overall system a.g.c.

**Loran A r.f. strip (board U)**

**8.** The Loran A r.f. strip, Board U (fig. 16) consists of a superhet circuit which receives, amplifies and demodulates the Loran A master and slave signals that are fed from the aerial amplifier. The receiver has three channel centre frequencies, these being 1·95 Mc/s, 1·9 Mc/s and 1·85 Mc/s; the overall −3dB bandwidth being 40 kc/s. Station selection is achieved by connecting the appropriate local oscillator frequency to the mixer stage to provide a constant intermediate frequency of 500 kc/s. The r.f. strip has an overall gain of 100 dB and a differential gain control of 80 dB between master and slave levels. Separate gain controls are employed for the master and slave signals, the operation of which are time-shared by using a bistable switching circuit controlled by the $\frac{1}{2}$ interval pedestal and the c.r.t. unit timebase sweep pulses.

**9.** The output signal from the aerial amplifier is coupled to the tuned transformer T1; C3 provides the tuning and R3 and R4 in series with the primary of this transformer provide the correct impedance match to the aerial amplifier output circuit. One side of T1 secondary winding is decoupled to earth by C4; the input to VT3 base circuit is then taken from T1 secondary tapping to provide the correct matching to VT3 without affecting the tuning of the input circuit. The base bias for VT3 is provided by the potential divider R11 and R12. The r.f. amplifier comprises VT2 and VT3, VT2 being a common base connected stage, with VT3 in its emitter circuit providing the r.f. input signal. The transformer in the collector circuit of VT2 is tuned by C8 to 1·9 Mc/s. which is the centre frequency of the available transmitted signals. By connecting VT1 across VT2 and its collector load, an adjustment on the gain of the stage is made possible. This is achieved by the action of VT1 which, when made to conduct, shunts both VT2 and its load, thus reducing the output. The shunt is variable and is controlled by the LORAN A DRIFT controls: RV12 on receipt of the master pulses and RV13 on receipt of slave pulses.

**10.** The output to the next stage, which is a mixer, is taken from the secondary winding of T3. The mixer stage combines the local oscillator frequency with the received Loran A frequency to produce a pulse envelope frequency of 500 kc/s, this being the difference between the received frequency and the local oscillator frequency. A field-effect transistor (VT4) is used as the mixer because it has a wide dynamic range, enabling it to handle higher input signals. It also has a high input impedance, therefore minimizing the loading effect on the r.f. stage; the overall gain of the stage is unity. The tuned load in the drain circuit of VT4 is tuned to resonate at the difference frequency (500 kc/s) and the i.f. output, of which one side is decoupled to earth, is coupled to the first i.f. stage.

**11.** The local oscillator, mentioned above, is designed to operate at one of three frequencies depending on which Loran station has been selected; these frequencies are 2·35, 2·4 and 2·45 Mc/s. One of the three crystals is introduced into the base circuit of VT20 by applying a positive bias, via positions 1, 2 or 3 of the left-hand SELECT STATION switch on the read-out unit, to diodes MR1, MR2 or MR3 respectively. This positive bias causes the diode in series with the selected crystal to conduct, effectively connecting one end of the crystal to earth.

**12.** The operation of the oscillator is as follows. The crystal represents a series resonant circuit which, when at resonance, causes an r.f. current to flow through C10 and C11. Because the reactance of C11 is low in comparison with the impedance of T6, C11 effectively becomes the emitter load to VT20. A portion of the crystal current is amplified and fed via R24 to C11 where it is combined with the original crystal current to provide sufficient drive to maintain oscillation. The output to the mixer stage VT4 is taken from the 7:1 step down transformer T6.

**13.** VT5, VT6 and VT7 form the first i.f. amplifier and as the circuit is similar to the r.f. amplifier described in para. 9, the operation of the circuit is the same. The i.f. transformer T4 in the collector circuit of VT6 is tuned to the 500 kc/s i.f. frequency. The output from the secondary winding of this i.f. transformer, of which one side is decoupled to earth by C21, is coupled to a second identical i.f. stage. The second i.f. output is coupled to a fixed gain stage comprising VT11 and VT12, with VT12 amplifying the i.f. signal and injecting it into the emitter circuit of the common base connected stage VT11. The output, which is tuned to 500 kc/s by VT11 collector load, is coupled via a p.n.p. emitter follower stage to the detector MR4. A filter comprising L3, C33 and C36 is introduced to remove the 500 kc/s content of the half cycle 40$\mu$S pulses emanating from the detector MR4. The pulses are then coupled to the c.r.t. unit via C35 and the Loran station selector switch.

**14.** The gain control voltages that are applied to the r.f. and both i.f. stages are time-shared and are controlled by RV13 on receipt of the master Loran A pulse and by RV12 in receipt of the slave Loran A pulse. This time-sharing is controlled by a bistable circuit comprising VT17 and VT18, the inputs to which are the half interval pedestal from board M, and the timebase sweep start pulses from the c.r.t. unit sweep generator, board VA pin C.

**15.** Arrival of the $\frac{1}{2}$ interval pedestal resets the bistable circuit, which causes VT19 to cut off and allow the voltage on the wiper of RV12 to reach the base circuit of VT16; this condition occurs on receipt of the slave Loran A pulses. On receiving the c.r.t. timebase sweep start pulse, the bistable circuit changes state causing VT15 to cut off, which allows the voltage on the wiper of RV13 to reach the base circuit of VT16; this condition occurs on receipt of the master Loran A pulses. VT16 has an active load comprising VT14, MR5 and MR6, the effect of which is to provide an almost linear output at the collector of VT16 for an equal increment adjustment to either of the gain control potentiometers RV12 or RV13. The resistive effect of the load decreases with increase in current by the action of VT16 in controlling the base/emitter voltage of VT14. This is achieved by utilising a reduction in voltage at VT16 collector to reduce VT14 emitter voltage; the base/emitter voltage of VT14 is then increased due to the fact that the base of VT14 is at a fixed potential. The d.c. outputs from VT16 collector, which are time-shared gain control voltages, are coupled via the noise filter comprising L2, C30 and C32 to the r.f. and two i.f. stage gain control transistors.

**Coder circuit (board T)**

**16.** This circuit (fig. 17) provides the coder gates on board X (VT13 and VT14) with appropriately phased pulses to decode the master, slave A and slave B received pulses. Decoding, which means in effect phase reversal of the inverted pulses in any group of received pulses, is carried out by switching on one of the two transistors mentioned above (VT13 and VT14). Incorrect decoding usually implies that the wrong phase-code is being applied to the coder gates, i.e. the slave decoding pulses may be fed to the coder gates to decode the received master signals or group 1 pulses may be fed to decode group 2 signals. Operation of the CODE JUMP switch S12 will correct the latter condition. The phase code pulses are produced by gating together the outputs of two bistable circuits together with plus or minus MTS and plus or minus $\frac{1}{2}$ PRR. The pulses so produced, set the state of the coder gates in anticipation of the next received pulse.

*Circuit description*

**17.** Reference should be made to the circuit diagram fig. 17 and the logic diagram fig. 7. Three bistable circuits with associated emitter followers (VT10 to VT21) are connected in cascade, the input to the first one being controlled by the master, slave A and slave B tracking gate pulses. The bistables are reset by the master and slave full rate pedestal from boards FN and Q. The function of each bistable circuit is to divide by two the signal from the previous stage. The outputs from the first and last of these three bistable circuits are fed to 'and' gates, details of which are given later in paragraph 20. The bistable circuit VT2 and VT3 is triggered by −MTS once per pulse repetition rate. As a bistable circuit is effectively a frequency divider, then the resultant output of this bistable circuit occurs at half the repetition of the input signal, hence the pulse designation $\frac{1}{2}$ PRR ($\frac{1}{2}$ pulse repetition rate). The outputs from VT2 and VT3 collectors are also coupled to 'and' gates, further information on which is given in paragraph 20. Although this bistable circuit is normally triggered by −MTS pulses, it can also be triggered by depressing the code jump switch; this has the effect of changing the code of the pulses to suit the alternative group of received pulses, i.e. M2 pulse group instead of M1.

**18.** The function of VT23 and VT31 is to provide a composite signal to feed the c.r.t. unit, comprising the master, slave A and slave B tracking gates. VT23 is normally conducting and on receipt of a tracking gate pulse from either a master or slave group of pulses it will switch off; the collector voltage of VT23 will then rise and because VT31 is an emitter follower this voltage rise which is fed to its base will appear at its emitter. Therefore, for every pulse fed to VT23, whether master or slave, a corresponding pulse will appear at VT31 emitter. VT1 is an emitter follower to which are connected the outputs of

all the 'and' gates; as VT1 is normally on, the output of the emitter follower will then fall when an output appears from any of the 'and' gates.

**19.** VT8 and VT9 form the coder delay monostable circuit, the time constant of which provides a delay of approximately 150$\mu$S, i.e. sufficient time to allow the previous pulse fed to the coder circuit to take effect. The coder delay circuit is triggered by a negative pulse from the emitter follower VT1. After the 150$\mu$S delay period a negative pulse is fed to the coder bistable circuit VT5 and VT6, changing its state. By incorporating the inverters VT4 and VT7, a voltage of 24V is produced for controlling the code switching transistors VT13/VT14 on board X. The coder bistable circuit is reset, i.e. VT6 off and VT5 on, at the end of the −MTS pulse. The resultant outputs from the emitter followers VT4 and VT7 are of such a pattern as to effect a code change to the received signal when necessary.

**20.** The diode gates mentioned in para. 17, which are used in the derivation of the code change pulses, are shown in the logic diagram fig. 7. Fig. 4 shows just one pair of 'and' gates taken from fig. 6 coder gate circuit diagram. During the −MTS period, the voltage applied to MR2 is only just sufficient to bias it to the off condition. On receipt of the +A signal, the positive-going part of the pulse will bias off still further the diode MR2, but due to the signal being differentiated by C3/R6 the original bias state on MR2 will be returned before the +A signal starts to go less positive; C3 is then charged up to the +A potential (10 volts approximately). When the +A signal falls, the 10 volts on C3 will forward bias MR2 and produce a negative-going pulse at the junction of C2/R5/MR2. When the $+\frac{1}{2}$ PRR potential is approximately that of the −MTS potential, the process above repeats, this time adjusting the bias on MR1. A negative-going output pulse is then fed via C1 to the base of the emitter follower VT1. This same process is carried out on the other gating circuits, only different input signals are used. The appropriate coding pulses are thus obtained to suit master 1, master 2 or slave 1, slave 2 groups of pulses. Fig. 6 and 7 show the pairs of 'and' gates associated with the production of the coder pulses. Although a coding pulse is produced at the same time a pulse is received, the coder circuit will not effect a change to that pulse, due to the 150$\mu$S delay circuit VT8/VT9. The coding pulses have been so timed to effect a change, if necessary on the following received pulse. The last output coder gate pulse during any time-shared period is always used to set the coder transistors on Board X (VT13 and VT14) to positive signal phase.

**Index circuit (board H)**

**21.** To verify at which index cycle the equipment is functioning, the portions of master, slave A and slave B index waveforms that are coincident with their respective tracking gates are stored on capacitors. By using a time-sharing process, the voltage stored on each of the three capacitors are coupled separately to a d.c. amplifier. The output voltages from the d.c. amplifier which are also time-shared in order to separate them, are then coupled via the respective master, slave A or slave B Darlington pair emitter followers to the metering circuit. If the incorrect index cycle has been selected on the master, slave A or slave B signals, the resultant output from the d.c. amplifier for the relevant signal will be of sufficient amplitude to operate the appropriate index alarm lamp and will also cause the deflection of the index meter. Also mounted on this board is a circuit which removes the supplies from the crystal oven in the event of the oven overheating.

*Circuit description* (fig. 18)

**22.** The index waveform from the r.f. amplifier on board X is coupled to pin 7 of board H and is limited by MR13 to MR16. VT33, an emitter follower, then couples the signal via T4 to the master, slave A and slave B gating circuits. As the master, slave A and slave B channels are the same, only the master channel will be described.

**23.** When a 4·5 $\mu$S master tracking gate pulse is present between the base and collector of the gating transistor VT27, one side of the secondary winding of T4 will be connected, via VT27 and R2, to C1 for this 4·5$\mu$S period. The tracking gate pulses for operating the master, slave A and slave B gating circuits are provided by board K, board Q and board S respectively. VT45 is also supplied with the master tracking gate pulse, effectively connecting the other side of T4 secondary winding via R1 and R64 to the other side of C1. Because C1, R1 R2 and R64 form an integrating network, the mean level of the index waveform over the 4·5$\mu$S period is stored on C1, and provided the third cycle of this waveform, shown in Part 1, Chapter 2, fig. 1 is selected, the resultant charge on C1 will be zero. Store updating is carried out eight times during the −MTS period at the selected pulse repetition rate. The purpose of R65 and contact RLB1 across C1 is to reduce the store voltage to zero when STORE ZERO has been selected on the c.r.t. unit.

**24.** The slave A and slave B gating circuits function in the same way as the master circuit described above, except that the signal used will be the slave A and slave B tracking gates respectively. Due to the time-sharing process, the pulses sampled by these tracking gates will be those for slave A and slave B respectively.

**25.** A gating circuit comprising VT34, VT2, R58, R3 and T1 (secondary 1 winding) is used to read the voltage stored on capacitor C1, and a 1mS gating pulse derived from board FN is used to open this read gate. By applying this 1mS pulse to VT42, the transistor is switched on and current is passed through the primary and secondary windings of T1, switching on VT34 and VT2 allowing the stored voltage on C1 to be connected to the d.c. amplifier. At the same time an identical gating circuit comprising VT3 and VT4, for the master signal only, is switched on for the same

1mS period by T1 (secondary 2 winding). This enables the master voltage levels, from the d.c. amplifier, to be separated from the slave voltage levels.

**26.** The d.c. amplifier comprises three cascade connected long-tailed pair circuits. The inputs to the first of these three stages are coupled via emitter followers VT29A and VT29B. This is to maintain the balance of the circuit during temperature variations by providing low impedance drives for VT49A and VT49B. RV2 in the emitter circuit of VT49 is adjusted on test to provide an initial balanced output from the long-tailed pair. The three long-tailed pair circuits comprising VT49, VT31/VT32 and VT26/VT30 are required to provide an overall gain of 100, this being sufficient to give the required meter deflection when incorrectly indexed.

**27.** The gated output signal from the 1mS gate VT3/VT4 is coupled via a Darlington pair emitter follower VT6/VT7 to the FUNCTION switch S1/1 and then via the normally closed contacts of RL6/2 and RL7/2 to the index meter. If the receiver is locked to some cycle higher than the normal indexing third cycle, the output from the Darlington pair VT6/VT7 will be positive, and if some cycle below the index third cycle is selected, then the Darlington pair output will be negative. The transistor switch VT18/VT17 that operates the index alarm lamp requires a positive voltage on its base to operate it. This is obtained by VT8 being switched off when the first or second cycle has been used for indexing, causing VT8 collector potential to go positive. As soon as VT8 collector voltage goes sufficiently positive to overcome MR11 zener voltage, the transistor switch VT18/VT17 will operate. In order for the transistor switch to operate when some cycle higher than the third has been selected, i.e. VT7 output is positive, the values of R10 and R11 are selected such that a positive voltage at VT8 base forward biases the base-collector junction of VT8. This then connects the voltage on VT7 emitter to MR11 via MR1, and the transistor switch VT18/VT17 will again be switched on.

*Oven protection circuit*

**28.** This circuit is designed to protect the crystal circuitry under a possible oven overheat condition. Protection is achieved by placing a transistor within the oven and using its leakage current, which increases with increase in temperature, to energize relay (RLA). The temperature at which the relay will be energized (74°C) is set by the preset bias control RV5. Once operated, the normally open relay contact RLA/1 maintains the operation of the relay, and contact RLA/2 disconnects the supplies from the oven. To reset the oven, the equipment must be switched off and the oven allowed to cool down. Before using the equipment for normal service the cause of the fault should be ascertained. Relay switching is employed to prevent signal interaction in the long leads that would otherwise be required.

**A.F.C. circuit (board K)**

**29.** The function of this circuit is to provide the automatic tracking facility on Loran C operation. This is done by sampling with a 4·5μS gate the cross over point of the a.f.c. waveform, third cycle, from circuit board X. By using an integrating circuit the mean voltage of this sampled portion of a.f.c. waveform is stored on a capacitor and by using a 1mS read gate together with a d.c. amplifier, changes in stored voltage level on this capacitor are used to effect a change to the oscillator frequency until the store voltage has retumed to zero. The output from the d.c. amplifier is also coupled to the meter, and the AFC ALARM lamp via a transistor switch, R90 and contact RLA/1 reduce the voltage stored on C1 to zero when STORE ZERO is selected on the c.r.t. unit.

*Circuit description* (fig. 19)

**30.** This circuit is basically the same as that of circuit board H in operation; additional circuitry and circuit changes necessary for the correct functioning of this circuit are described below. The tracking gate triggers, derived from circuit board M which are 10μS wide pulses recurring eight times coincident with the 8 Loran C pulses every repetition rate, are used to trigger a monostable circuit comprising VT40/VT41. This monostable circuit is incorporated to reduce the duration of the tracking gate triggers to 4·5μS. The pulses are then amplified by VT42 and the outputs that are provided at secondary windings 1, 2 and 3 of T4 are coupled to the master AFC, INDEX and AGC 4·5μS sampling gates on circuit boards K, H and FW respectively. The equivalent circuits to VT40, VT41 and V42, which supply the slave A and slave B pulses are incorporated on circuit boards Q and S respectively; boards Q and S are identical boards. Although the d.c. amplifier on this circuit functions in the same way as the one on circuit Board H, it is only required to provide an overall gain of 50 instead of 100. Because it is possible to obtain an overall gain of 50 with just two long-tailed pair stages, a third stage is unnecessary. With just two long-tailed pair stages, the individual gain of each stage is higher, and because of this, additional temperature stability is provided by VT48, a temperature compensated constant current circuit in the emitter circuit of the first long-tailed pair.

**31.** The output circuit differs from that on circuit board H in the following respects. The voltage at the emitter of VT23 of the Darlington pair emitter follower is coupled via the phase advancing resistor capacitor network C14/R66 ▶◀ to the master frequency controlling variable

capacity diode mounted inside the oven. To ensure that the variable capacity diode is operated within its prescribed voltage range, a potential divider network is incorporated comprising R65, R66, R64 and R67. In the Loran C positions of the SELECT STATION switch S13, the output of the Darlington pair VT33/VT23 is divided down and coupled to the master variable capacity diode mounted in the oven. At the same time, output voltages are coupled to the slave A and slave B variable capacity diodes in the oscillator circuits from identical potential divider networks on the slave A and slave B channels respectively. With the SELECT STATION switch set to its Loran A positions, automatic frequency tracking is not carried out, but a preset voltage determined by the settings of RV11 and RV10 LORAN A DRIFT controls will be coupled to the master and slave A oscillator variable capacity diodes via R68 or R42 respectively.

**A.G.C. circuit (board FW)**

**32.** The circuits on this board are similar in operation to those on board K. The function of the circuit is to adjust the gain of the r.f. strip on board X to

received signal levels. This is done by gating and then integrating the third cycle of the a.g.c. waveform so that the mean voltage over the 4·5$\mu$S gating period is stored on a capacitor. The amplitude of this voltage, after gating, amplification and further gating is used to control the biasing and hence the gain of the transistors in the r.f. strip (board X). This is a time-shared process, where the gain of individual signals, master and slave, are separately adjusted.

33. A lost signal alarm is incorporated, designated AGC ALARM. ▶◀The output voltage that is monitored by the panel meter is taken from the output of the Darlington pair emitter followers (VT6/VT7 for master).

*Circuit description*

**34.** Reference should be made to the circuit diagram fig. 20. The principle of operation of this circuit is basically the same as that of board K, where differences occur they are detailed below. An a.g.c. delay circuit comprising MR23 and MR24 is introduced so that an input level to this circuit falling below approximately 0·5V causes these diodes to cease conducting, therefore no voltage will be stored on C1, this being the condition under which maximum gain of the r.f. strip on board X is produced. The diodes MR23 and MR24 are parallel-back-to-back connected to obtain a true integration of signal plus positive noise together with negative noise.

**35.** The 4·5$\mu$S gating circuits used to store the a.g.c. voltage are similar than those used on the a.f.c. circuit board K and as all three (master, slave A and slave B) gating circuits are the same, only the master one will be described. A 4·5$\mu$S master tracking gate pulse, obtained from board K, is applied between the emitter/base circuit of VT1/VT42, causing both transistors to conduct and so connect the sampled portion of the a.g.c. waveform to the integrator C1/R2. The stored voltage on C1 is read by the 1mS gate and coupled to a d.c. amplifier as it is on the index circuit, board H. The function of R6 and RLA/1 contact across C1 is to reduce the store voltage to zero when STORE ZERO has been selected on the c.r.t. unit.

**36.** The output circuits associated with the master, slave A and slave B channels incorporate gating circuits comprising VT47/MR14/MR17, VT48/MR16/MR18 and VT41/MR19/MR28; these are controlled by +MTS, +ATS and +BTS (time-shared) signals, so as to let the respective a.g.c. voltages through one at a time. Fig. 8 shows the output circuit in logic form.

**37.** When locking in the Loran C signals during the normal operating procedure, slave B tracking gates can be aligned to slave A received signals with no adverse effect, conversely the slave A tracking gates can be aligned with slave B received signals. Therefore the inhibit voltages applied to the gates are so arranged that the slave signals can follow the master in any order and still control the gates so that only the relevant a.g.c. voltage will be coupled to the output circuit, at any one time. The output circuit comprises a Darlington pair emitter follower VT52/VT5, with C28 acting as a store for the a.g.c. voltage until it is re-charged with the next a.g.c. voltage.

**Oscillator and divider circuits (boards J, ◀ HH, KK and oven JJ)▶**

**38.** The master, slave A and slave B crystal drive circuits together with the divider circuits necessary to produce an output of 100 kc/s from the M, A and B channels are incorporated on this circuit. The three different crystal frequencies were chosen (5·0, 4·8 and 4·5 Mc/s) to prevent interaction between the channels, although the crystal oscillator circuit for each frequency is exactly the same. To produce the required 100 kc/s output from each channel, different divider stages are used.

*Circuit description*

**39.** Reference should be made to the circuit diagrams fig. 21 and 22. As the three crystal oscillator circuits are identical, only the master one will be described. The crystal, which is mounted on circuit board JJ (para. 43), represents a series resonant circuit in the emitter of VT30, causing maximum gain of this stage at the crystal frequency (5 Mc/s). The basic oscillator frequency is controlled by the crystal used, but adjustment to this frequency is effected by applying a bias voltage from the a.f.c. circuit (board K) to control the capacitance of the variable capacitor diodes on circuit board ◀KK.▶With no a.f.c. bias applied to the variable capacity diodes the crystals are made to oscillate at their nominal frequencies by adjustment of the select-on-test capacitors C1,

C2 and C3 across these variable capacity diodes on circuit board HH. VT30 and VT31 form the basic crystal oscillator with VT31 driving the primary of T3 from its collector, the primary of T3 being tuned to 5 Mc/s by C48. One secondary winding of T3 is connected to the base circuit of VT30 to reasonate its emitter circuit and VT30 collector signal is fed back to VT31 base as positive feedback, the circuit then continues to oscillate at a controlled frequency. VT32 provides an automatic gain control by sampling the output voltage from another secondary winding on T3: VT32 will then alter the bias conditions of VT31, resulting in a change in T3 output. The output from this circuit will therefore reach a limiting value and remain there. C37 provides a long time constant on the a.g.c. circuit to prevent hunting or low frequency oscillations. Coupling to the next stage, which is a Darlington pair, is done by C36. The Darlington pair VT33/VT34 provides a low impedance source for the squarer stage VT35/VT36 and also provides a 5 Mc/s output to the 5 to 10 Mc/s multiplier circuit on board E via MR10.

**40.** The divide-by-two stage, which is a monostable circuit comprising VT37 and VT38, is triggered by the leading edge of a negative-going pulse from the squarer stage. This negative-going pulse is applied to the base of VT46, an emitter follower, which transfers the pulse to the base circuit of VT38, thus cutting it off. By using this emitter follower, VT37 switches off more quickly, resulting in a cleaner waveform and hence more reliable switching at this high frequency. VT38 collector will now go positive causing VT37 to conduct, thereby inhibiting the operation of the circuit to a further pulse until VT37 has cut off. The monostable circuit has a time constant of sufficient duration to respond only to every other 5 Mc/s pulse, therefore the output frequency from this monostable circuit will be 2·5 Mc/s. The output, which is taken from VT37 collector, is coupled via C41 to the next stage which is also a monostable circuit, only this time having a division ratio of five. The time constant of the VT39/VT40 monostable circuit is such that it will only respond to every fifth 2·5 Mc/s pulse, giving a 0·5 Mc/s output signal to the next stage. A similar divide-by-five stage VT41/VT42 is included to divide the frequency down to 100 kc/s. The output signal is then differentiated by C46/R99 and the negative-going pulses so produced are amplified and clipped by VT44. These pulses are then passed to the slew board (board L) via the emitter follower VT43 and diode MR14.

**41.** The frequency divider circuits associated with the slave A and slave B channels are basically the same as those described above, an emitter follower being required in the first divider stage of each channel for matching purposes and hence to assist the high speed operation of the circuit. The only differences between the monostable frequency dividing circuits are the division ratios, these being controlled by different value components.

**42.** The same power supply is used for each of the master, slave A and slave B circuits, but to prevent interaction between the oscillator and frequency divider sections, the supply is routed through MR5, R105 and MR15, R103 where the supply is separately decoupled for the oscillators and the frequency dividers respectively. Further decoupling is provided at the supply connections to each individual circuit to prevent any signal interaction between the circuits.

**Crystal oven and drive circuit JJ and tagboard KK**

**43.** This circuit embodies the master, slave A and slave B crystals 5·0, 4·8 and 4·5 Mc/s respectively, the oven heater circuit, the temperature controlling transistor and the oven overheat sensing transistor. These circuits provide a controlled temperature environment to ensure high stability from the crystal oscillators.

*Circuit description*

**44.** The drive circuits for the three crystals are mounted on circuit board J, (para. 39). The oven is heated by the power dissipated in four resistors in the collector circuit of VT2, and by VT2; the dissipation is controlled by the applied voltage at VT2 base. The oven controlling voltage is dependent upon oven temperature and is provided by the potential divider network R6/VT3 on tagboard KK, together with RV1 on board HH. VT3 is reverse biased and only the leakage current characteristic is used to control the oven temperature. While the oven is cold, the leakage current through VT3 is at a minimum. This causes the potential at the base of VT6—one of three transistors in a cascade emitter follower configuration—to go positive, which in turn causes the base of VT2 to go positive and therefore produce a high current condition in VT2. Because VT3 is heated by the oven, its leakage will be governed by the temperature of the oven. An increase in oven temperature causes an increase in VT3 leakage current, therefore VT3 resistance will be reduced causing VT6 base voltage to fall. Because the circuit is a cascade emitter follower, then VT4 emitter voltage will fall thus reducing the drive to VT2, and reducing the heat dissipation from the heater resistors. By adjusting RV1 (shown on board HH fig. 22), the circuit will just maintain the oven heat losses at the required pre-determined temperature, this being 63°C.

**Slew circuits, board L**

**45.** This circuit board contains the slew circuits, which are used to align the tracking gate pulses with the received signal pulses, as seen on the c.r.t. unit. Slewing, which means in effect raising

or lowering the 100 kc/s clock frequency, is achieved by adding or subtracting pulses from the 100 kc/s signals obtained from Board J. The slewed clock signal is then fed to the pedestal generator Board M/FN, P/Q and R/S where the correct pulse repetition rate for the master, slave A and slave B signals is generated, together with +MTS, −MTS, +ATS, −ATS, +BTS, −BTS, master and slave pedestals, tracking gates and other gating waveforms used throughout the receiver. Once these waveforms have been manually aligned, the a.f.c. circuit tracks them continuously and the slew board acts basically as an inverter between the master, slave A and slave B 100 kc/s clock signals and the pedestal generator, boards M, P and R respectively.

**46.** The facilities available on this board are as follows:—

(1) *Coarse slew left or right.* When in the left position, the appropriate 100 kc/s clock signal is slowed down by 500 pulses per second and in the right position, the 100 kc/s clock signal is increased by 500 pulses per second.

(2) *Medium slew, left or right.* When in the left position, the appropriate 100 kc/s signal is slowed down by 50 pulses per second and in the right position, the 100 kc/s clock signal is increased by 50 pulses per second.

(3) 10$\mu$S *Jump.* Once the tracking gates have been slewed into the received pulses, they can then be correctly aligned to the required cycle of the pulse in 10$\mu$S steps. This is achieved by adding, or subtracting if slew left has been selected, one pulse from the appropriate 100 kc/s pulse for each operation of the 10$\mu$S JUMP switch.

(4) *All Jump.* This switch enables the master, slave A and slave B tracking gates to be jumped 10$\mu$S simultaneously for each operation of the switch. In the absence of skywave contamination but with considerable noise, positive locking to the signal can be ensured by using this switch to jump the tracking gates to the higher amplitude cycles in the received pulse.

*Circuit description*

**47.** Reference should be made to the circuit diagram fig. 23 and the logic diagram fig. 9. As the master, slave A and slave B slewing circuits are the same, only the master circuit will be described. The output signal from the master 100 kc/s divider on Board J is differentiated and applied to a monostable circuit (VT1/VT2) with a 5$\mu$S time constant; because of this time constant, the monostable output will be a square wave at 100 kc/s. The output from the emitter follower VT3 is coupled to the master divider board FN, the collector circuit of VT7 and via MR6 to the base circuit of VT11. Assuming that no slew conditions are selected, the 100 kc/s square wave signal is applied to the inverter (VT11) base via R17, R21/C8 and R23/C10 as well as via MR6, R22/C9 and R24. Although there are two signal feeds to the base of the inverter VT11 on the unslewed operation of this circuit, only one of them need be considered as they are effectively in parallel. The slew signals are derived from one of three sources:—

(1) For coarse slewing, 500 c/s from board Q is used.

(2) For medium slewing, 50 c/s from board Q is used.

(3) For jumping the signal in 10$\mu$S steps, a single pulse from a monostable triggered by the 10$\mu$S jump or all jump switch is used.

**48.** With the coarse slew switch operated to the left position, the circuit functions as follows. VT21 is made to conduct by applying +12 volts to its base, thus pulling the voltage on the collector down to approximately −12 volts, making the voltage at the junction of R34 and R35 +1 volt. A 500 c/s square wave is differentiated by C13/R34/R35, and the negative pulses produced by differentiation are applied via MR7 to VT12 which shapes these pulses and inverts them. These pulses, which are now positive going, are used to trigger a 15$\mu$S monostable circuit VT13/VT14, the output of which is a train of 15$\mu$S pulses at a 500 c.p.s. rate. These are fed to the base of VT15 which, for the 15$\mu$S period cuts off, allowing its collector potential to rise, thus opening the gate comprising MR2/MR31/VT4. Initially VT4 is turned hard on but with M selected on the c.r.t. unit FUNCTION switch, the biasing arrangement for the differentiating circuit C36/R77/R8 is modified so that a short duration negative-going differentiated pulse fed via MR31 will switch off VT4 during the 15$\mu$S period that the diode MR2 is open, but it will only remain off for the duration of the short pulse. The short positive-going pulse produced at VT4 collector is used to trigger a 12$\mu$S monostable circuit VT5/VT6, the output of which, during the 12$\mu$S period, causes VT7 to conduct. This causes the 100 kc/s signal at the collector of VT7 to be grounded for 12$\mu$S, therefore eliminating one complete pulse. This slewed signal is inverted by VT11 and coupled via an emitter follower VT38 to the pedestal generator boards. The 100 kc/s signal cannot enter VT11 base via MR6, because, with slew left selected, VT10 is forward biased thus grounding that line.

**49.** The operation of this circuit under medium slew left conditions is the same as described above except that the 15$\mu$S monostable circuit is triggered by 50 c/s instead of 500 c/s. With the coarse slew or medium slew switch pressed to the right, pulses are added to the output of the 100 kc/s clock signal at a rate of 500 or 50 pulses per second respectively. The basic difference to the circuit in the slew right condition as compared with slew left is that VT10 is now non-conducting. MR5 and MR6 form a two input 'or' gate, where one input is a 100 kc/s square wave signal and

the other is a train of positive-going 0·6μS pulses, produced by differentiating the trailing edge of each 12μS pulse from the monostable circuit (VT5/VT6) and inverting them in VT8. Although these 0·6μS pulses appear at the rate of 500 or 50 per second, they arrive at the base of VT11 during the 5μS period that the 100 kc/s waveform is at 0 volts. This then causes VT11 to conduct 500 or 50 times per second more, depending on the slew rate selected. Fig. 10 shows the inverted waveform obtained at VT11 collector.

**50.** With 10μS jump left or right selected, the circuit configuration is as described above except that just one pulse is added or subtracted for each operation of the 10μS JUMP switch instead of 500 pulses or 50 pulses as is the case with the coarse or fine slew controls. The 20 mS delay monostable circuit VT42/VT41 is provided to allow the output circuitry feeding VT11 time to reach the correct state. The operation of the circuit on ALL JUMP is the same as that on 10μS JUMP described above, but instead of jumping just the master tracking gate, VT43 conducts, priming VT4, VT16 and VT27; causing the master, slave A and slave B tracking gates to be jumped. VT9 triggers the VT42/VT41 monostable circuits on ALL JUMP in exactly the same way as on 10μS JUMP.

**Master pedestal generator (board M)**

**51.** This board houses the master first and second decade dividers and also the circuitry for the generation of the following:—

(1) ½ interval pedestal—used on Loran A only.

(2) Loran A and Loran C digitiser triggers —used to start the readout unit counters.

(3) Master tracking gate trigger—used in the a.f.c. tracking circuit.

(4) Master scope trigger (MST)—used on the c.r.t. unit.

**52.** Fig. 24 shows the circuit of this board. The first decade divider is fed from the 100 kc/s slewed-clock signal which is derived from board L. Assuming that the divider has been reset to zero, i.e. VT2, VT4, VT6 and VT8 are switched on, then the first negative-going part of the 100 kc/s pulse will change the state of the first bistable circuit thus leaving VT1 in the ON state. Succeeding bistable circuits cannot change state until the output transistor of the bistable stage immediately preceding them is switched on. This occurs on the second 100 kc/s slewed-clock pulse, causing a fall in VT2 collector voltage which provides the next stage with a negative pulse. When VT2 is switched the negative pulse then changes the state of VT3/VT4 bistable circuit, turning on VT3.

**53.** Table 2 shows the complete decade-count, where 1 indicates the 'on' state of a transistor, e.g. the count of 0 is shown as 01, 01, 01, 01, where VT1, VT3, VT5 and VT7 are in the off state and VT2, VT4, VT6 and VT8 are in the on state. By resetting this circuit at the count of 10, what would normally have been a divide--by-16 circuit is converted to a divide-by-10. This resetting is achieved by using the count of 10 binary states. The collector potentials of VT4 and VT8 are fed to an 'and' gate VT9, and on the count of 10 when their collector potentials rise, +6 volts is fed to the base of VT9 causing it to conduct heavily. As the emitter of VT9 is grounded, then the collector will also become effectively grounded. This collector is connected by diodes to the collectors of VT4 and VT8 to reduce their potentials and so reset the bistable circuits. The collector potential of VT6 is also held down to prevent the negative pulse from VT4, due to its switching on, from changing the state of the VT5/VT6 bistable circuit. Every time the count of 10 is reached and the counter is reset, a negative pulse is fed to the second decade divider stage.

**TABLE 2**

**Divide by ten circuit binary arrangement**

| Count | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| 0 | 01 | 01 | 01 | 01 |
| 1 | 10 | 01 | 01 | 01 |
| 2 | 01 | 10 | 01 | 01 |
| 3 | 10 | 10 | 01 | 01 |
| 4 | 01 | 01 | 10 | 01 |
| 5 | 10 | 01 | 10 | 01 |
| 6 | 01 | 10 | 10 | 01 |
| 7 | 10 | 10 | 10 | 01 |
| 8 | 01 | 01 | 01 | 10 |
| 9 | 10 | 01 | 01 | 10 |
| 10 | 01 | 10 | 01 | 10 |

**54.** The second divider comprises VT11 to VT19 inclusive and operates in exactly the same way as the first. VT19 is the 'and' gate reset transistor which, on the count of ten of the second decade divider, lowers the collector potential of VT12, VT14, VT16 and VT18 via diodes thus resetting the divider to zero. Although VT11/VT12 and VT15/VT16 bistable circuits are already in their correct state at the count of 10, the applied negative pulse from VT19 prevents their changing state by the negative pulse from the preceding stage. This decade feedback line also supplies an 'and' gate VT25, which is also supplied with −MTS. The pulses from the decade reset line, which are 100μS pulses at 1 mS intervals, will only be passed through VT25 'and' gate during the −MTS period (8 mS duration).

**55.** There is an overriding reset line which resets each bistable stage of the first and second decades, this is controlled by the third and fourth decades on circuit board FN. From the count-of-five 'and' gate (MR21/MR20/MR72) on the first decade divider, 10$\mu$S pulses starting 50$\mu$S after −MTS at 100$\mu$S intervals are fed to the 'and' gate (MR122/MR119), producing for the duration of −MTS a set of eight 10$\mu$S pulses at 1 mS intervals; these are the master tracking gate triggers. From the count-of-2 'and' gate (MR18/MR22/MR28/MR29) the 1$\mu$S pulses at 100$\mu$S intervals appear 30$\mu$S before the master tracking gate triggers. The former pulses are fed to VT25, an 'and' gate; the two inputs to VT25 are −MTS and the second decade reset pulse. The output from VT25 and MR120 'and' gate is eight 10$\mu$S pulses occuring at 1 mS intervals. The scope trigger pulses are then provided by gating one of the 10$\mu$S pulses with the first decade count of 2 and then inverting this resultant pulse; this output is then coupled to the c.r.t. unit. To provide the digitiser trigger on Loran C operation the following inputs are coupled to the pair of gates comprising MR121, 123 and 127 and VT30: the eight 10$\mu$S pulses at 1 mS intervals from VT25 mentioned above, the 10 mS pulses from Board FN, derived from the third decade reset line to delete the last seven digitiser trigger pulses, and the decoded 0 count from the 'and' gate MR19/MR23/MR27/MR30; these pulses are used to start the counters in the readout unit on Loran C. On Loran A the digitiser trigger pulse is derived from VT20/21/22/23/24 and 0 or 5 output from the first decade, (see the logic diagram, fig. 11). The output from the gating circuit VT20 to VT24 without any additional gating is the $\frac{1}{2}$ interval pedestal used on Loran A only to control the c.r.t. trace.

◀**56.** Some diodes MR76 to MR118 are ▶ wired as gating circuits and are associated with the 'specific rate' selection process, the bias for the operation of most of these gates being provided by the SPECIFIC switch S9/1. Because the specific and basic rate selections are co-related, these being on the first and second, and third and fourth decades respectively, then the rate selection will be dealt with under the board FN description, para. 59.

**Master pedestal generator (board FN)**

**57.** This board houses the third and fourth decades and the decoding gating circuits for the derivation of the basic rate selection. Besides the basic rate selection, the following outputs are provided by this board:— +MTS, −MTS, a 1 mS gate once per PRR and the master pedestal. −MTS is an 8 mS pulse occurring once per pulse repetition rate. +MTS is the same, only an inversion of the above.

*Circuit description*

**58.** The circuit diagram for this board is shown in fig. 25 and the logic diagram is shown in fig. 11. VT6 to VT14 inclusive is what is termed the third decade and VT15 to VT22 inclusive is what is termed the fourth decade divider. The process of frequency division and means of resetting the divider is exactly the same as the first and second decades, described in para. 51 to 55 but the output to this third decade is a 1 kc/s signal derived from the output of the second decade divider.

**59.** Assuming a pulse repetition rate of S1 is selected, (i.e. 49·9 mS), then VT23 gate opens from 40 to 50 mS, VT24 gate opens from 9 to 10 mS and VT27 gate opens from 0·9 mS to 1 mS. The combined effect of these three gates being open turns off VT25. The positive pulse at VT25 collector is then gated with a 100 kc/s clock pulse at V26 base to produce the full rate pedestal. This pulse is then inverted by VT28 and differentiated and is used to reset to zero all the decades. Prior to inversion this pulse is also used to reset the coder bistable circuits on board T. Once the decade dividers reset, all the 'and' gates that were open to switch off VT25 close immediately, and as resetting occurs 5$\mu$S after the acquisition of the selected rate, a 5$\mu$S delay occurs before the first 100 kc/s pulse of the next pulse repetition rate is fed in. With the 'basic' rate switch set to S a fourth decade count of 4 or 5 will be decoded. If the specific switch is now set to 0, a fourth decade count of 5, together with a third decade and second decade count of 0 will be decoded. If the specific switch is now set to 1 to reduce the rate by 100$\mu$S, the fourth decade count of 4, together with a third decade count of 9 and a second decade count of 9 will be decoded. From the above description it can be seen that 0 is decoded from the second and third decade dividers only when the specific switch is set to rate 0 and a 9 is decoded with the specific switch at any other position.

**60.** As well as decoding the full rate pedestal as described above, a half rate pedestal is decoded to switch the traces on the c.r.t. unit. The decoding of the half rate pedestal is controlled by the settings of the basic and specific switches in the same way as the full rate pedestal, e.g. with a full rate of 49·9 mS as above, the count of 2 is decoded from the fourth decade together with the count of 4 from the third decade, the count of 9 from the second decade and the count of 5 from the first decade, producing a half rate of 24·95 mS.

*+MTS and −MTS derivation*

**61.** The −MTS output is an 8 mS pulse decoded from the third and fourth decades: see the logic diagram fig. 11. An inversion is effected on the −MTS signal by VT2 to obtain +MTS.

*1mS gate circuit*

**62.** The 1 mS gating pulses that are required by boards K, H and FW are provided from the emitter circuit of VT5. VT5 input is controlled primarily by the decoded 0 line from the third decade divider and the +MTS waveform, i.e. 1 mS gating signals will only appear from this circuit during the master time-sharing period.

**Slave pedestal generator (boards P and R)**

**63.** Circuit board P, which is identical to circuit board R, houses the circuitry associated with the slave A (board P) or slave B (board R) first and second decade dividers. Because identical circuitry has already been described on circuit board M, no additional description need be given. The circuit diagram is given on fig. 26.

**Slave pedestal generators (boards Q and S)**

**64.** Circuit board Q (fig.27) identical to board S, houses the circuitry associated with the Slave A (board Q) or slave B (board S) third and fourth decade dividers. Because the dividers, reset circuits and gating parts of this circuit are basically the same as those already described on circuit board FN (see fig. 11), no further description is necessary. Rate selection is carried out on exactly the same way as it is on circuit board FN.

**65.** The additional circuitry on this board comprising VT29, VT30 and VT31, is used to provide the 4·5$\mu$S gating pulses used on the AGC, INDEX and AFC boards (FW, H and K). VT29 and VT30 is a monostable circuit which is triggered by the tracking gate triggers derived from circuit board P. The purpose of this monostable circuit is to widen the differentiated tracking gate triggers that are applied to the input and so produce output pulses of 4·5$\mu$S duration. These pulses are coupled to the output transistor VT31, which transfers them to T4; the three secondary windings then provide the 4·5$\mu$S pulses to the AFC, INDEX and AGC circuits. Two additional outputs are taken from the decade divider stages on this circuit board; these are 500 c/s and 50 c/s and are coupled from slave 'A' board only to circuit board L to enable coarse and medium slewing of the 100 kc/s signals coming from Board J.

**10 Mc/s counter and readout circuit (board E)**

**66.** The function of this board is to gate the output of a 5 to 10 Mc/s multiplier signal, using first the master digitiser trigger signal to open the gate then the slave A or slave B digitiser trigger signal to close the gate. The 10 Mc/s pulses that pass through the gate during the open period are fed via the read-out unit counters to be presented as a time difference on the readout unit. Continuous readout of A or B can be selected, or by switching to A/B, the two time difference measurements will be displayed alternately at approximately 1 second intervals.

*Sequence of operation (fig.12)*

**67.** At the instant of switching of the clock astable circuit VT25 to VT28 and VT38, VT39, pulses are produced, which with the aid of a differentiating circuit and pulse widener circuits are widened to over 200 mS duration. These pulses are coupled via an inhibit ◄ gates VT54, VT53► (A, A/B B switch) to 'and' gates which permit one of the slave digitiser trigger pulses to be fed via an 'or' gate to the gate generator VT6 to VT11 (fig. 12). This same circuit configuration applies to either slave A or slave B digitiser trigger pulses, unless one specific condition has been selected, in which case the clock frequency is doubled and is fed to the gate of the selected slave only.

**68.** The negative pulses used to gate the digitiser triggers are coupled via a pulse shaping Schmitt trigger circuit to a 20$\mu$S monostable. The initiating pulse to the monostable circuit also resets the counters to zero and as an added precaution this reset pulse is applied to the gate generator to ensure that it is in a state whereby it can accept the master digitiser trigger pulses. After 20$\mu$S, which is sufficient time to ensure the counters are reset, the delay monostable circuit output pulse triggers the interrogate bistable circuit which, on changing state, switches off the master trigger inhibit transistor VT4. With VT4 switched off, the first master digitiser trigger pulse received will change the state of the gate generator and as this switches off the gating transistor VT7, 10 Mc/s pulses will then be fed to the read-out unit counters. After a period not greater than 100 mS a slave A or slave B digitiser pulse will be received and, as the digitiser trigger gates are open for at least 200 mS, the first slave pulse will be fed to the gate generator reset transistor thus changing its state and stopping the read-out unit counters. From this period until the next change of state of the clock (astable circuit), the time difference in microseconds will be displayed on the read-out unit. The slave digitiser trigger, in resetting the gate generator, changes the state of the bistable circuit VT1/VT2 which turns on VT4 and inhibits any further master digitiser trigger pulses until the end of the time difference display period.

*Circuit description*

**69.** Reference should be made to the logic diagram fig. 12, and to the circuit diagram fig. 28. The 10 Mc/s signal which is gated and used to drive the read-out unit counters is initially derived from the master 5 Mc/s oscillator. VT43 amplifies the 5 Mc/s signal, and the collector load T1 is tuned to accept the second harmonic of the signal (10 Mc/s). VT40 modifies its input waveform to produce a flat topped waveform, which is then fed to the pulse former circuit VT33 and VT34. The combination of VT33/VT34 together with VT40 effectively squares the waveform and, providing the clamp transistor VT35 is not switched on, this signal will be differentiated by C36/R87. VT36 then removes the negative-going input pulses derived from the differentiating circuit and, due to the inversion provided by VT36, negative-going differentiated 10 Mc/s pulses are fed to the read-out unit counters.

**70.** The slave display clock is a modified astable

circuit with a two speed switching rate (from once every second to twice every second). The modification referred to is that one resistor (R98 or R99) is used for base biasing to hold a transistor in the 'on' condition whilst another resistor R66 (or R66 and R88 in parallel for double speed switching) is used to discharge the 68 microfarad switching capacitor from the collector of the transistor that is switched on. Mixing diodes MR27/MR28 connect R66 to the switching capacitors to prevent interconnection of the transistor bases and to prevent shunting of R66 by the base bias resistors. High values of base bias resistors are used, feeding into Darlington pairs (VT26/VT38 and VT27/VT39) to provide extra gain. The other two diodes MR25 and MR26 are to protect the transistors from high reverse base-emitter voltage. The astable outputs are fed through emitter followers (VT25 and VT28) and then via 1 microfarad differentiating capacitors to a pulse widening circuit. The positive differentiated pulses are used to drive the circuit, which produces a 12 volt negative interrogate pulse of greater than 200 mS duration. This duration ensures that a combination of master digitiser trigger followed by slave digitiser trigger must be encompassed, taking into account the maximum delay of 100 mS for the master digitiser trigger to arrive.

**71.** Presentation on the read-out unit of slave A, slave B, or both displayed alternately (A/B), is selected by the slave display selector switch. In the A/B position both pulse widening circuits are operative (VT29 to VT32) and slave A and slave B times are displayed alternately. As well as increasing the speed of the display clock in positions A or B of the slave selector switch, VT53 or VT54 is switched on ◄ to clamp out the pulse on VT29 or VT32 base ►

By this means, the unwanted digitiser trigger pulse is gated to earth and the wanted digitiser trigger pulse is fed via the inverter stage VT9 to the gate generator. The interrogate pulse is simultaneously channelled to a Schmitt trigger circuit to sharpen the pulse, from where it is differentiated by C22/R36, clamped by MR14 and shaped by the reset amplifier VT17/VT18 to produce a 10 volt positive pulse of 3$\mu$S duration on the collector of VT18. This has the effect of earthing the digitiser reset line via the collector of VT12 for 3$\mu$S and thus resetting all read-outs to zero. The 3$\mu$S pulse on VT18 collector is differentiated by C19/R49, the negative pulse from which is used to trigger the gate opening monostable circuit VT19/VT20, providing a delay of 20$\mu$S to ensure complete resetting of the read-out. After this 20$\mu$S period, VT20 is turned on as the monostable circuit reverts to its stable state and the resultant negative pulse provided by the differentiating circuit C18/R46 is used to operate the interrogate bistable circuit VT1/VT2 which turns off VT3 and VT4, allowing the master pedestal to switch VT5.

**72.** The gate generator operation is as follows. The positive master digitiser trigger pulse is inverted by VT5 and fed via C8 to turn VT8 off and hence VT7 on by means of the bistable action of the circuit. The succeeding slave digitiser trigger pulse, inverted by VT9, is fed via C6 to turn VT7 off and hence VT8 on. As VT8 collector voltage decreases, VT6 is turned off and the resultant reduction in VT6 emitter voltage causes the interrogate bistable circuit VT1/VT2 to be reset, i.e. VT2 turned off. During the period that VT7 is conducting, VT10 and VT11 are both cut off and hence the gating transistor VT35 is turned off for this period, allowing the 10 Mc/s signal to be applied via the final output transistor VT36 to the read-out unit counters. Reset diode MR9, operated by the reset amplifier VT17, VT18 and VT12, is simply a safety precaution to ensure that the gate generator bistable circuit is in the correct condition for interrogation.

**Counter (board F)**

**73.** This board contains the 10 Mc/s and 1 Mc/s counters; the count is decoded on the 1 Mc/s counter but not on the 10 Mc/s. The 1 Mc/s counter is a conventional counter which resets to 0 at the count of 10. The binary state of each counter is decoded and used to control transistor switches which turn on the appropriate lamps in the readout unit. These are minature 6 volt 140 mA lamps which are mounted behind small condenser lenses. Between each lens and lamp there is a piece of film, there being one digit (designated 0 to 9) to each of the ten lamps in the indicator unit. The images from these films are focussed onto a common ground glass screen; thus when a lamp lights, the corresponding number will be displayed upon the screen. Because of the high switching rate involved with the 10 Mc/s counter, a different approach is employed in dividing the frequency. Instead of resetting the counter to 0 at the count of 10, the count of 2 sets the binary circuits as though the count of 8 has been received. Therefore after the tenth input pulse, the counter automatically counts 0.

*Circuit description*

**74.** Reference should be made to the logic diagram fig. 13 and the circuit diagram fig. 29. The 10 Mc/s counter comprises three diode gated bistable circuits followed by one R-S (reset/set) bistable circuit, the detailed operation of which is as follows:—

**TABLE 3**

**10 Mc/s Counter truth table**

| Count | VT20 | VT21 | VT28 & VT29 Gate circuit | VT22 | VT23 | VT24 | VT25 | VT26 | VT27 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | | 0 | 1 | 0 | 1 | 0 | 1 |
| 2 | 0 | 1 | | 0 | 1 | 0 | 1 | 1 | 0 |
| 3 | 1 | 0 | | 0 | 1 | 0 | 1 | 1 | 0 |
| 4 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 5 | 1 | 0 | | 1 | 0 | 0 | 1 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 7 | 1 | 0 | | 0 | 1 | 1 | 0 | 1 | 0 |
| 8 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 9 | 1 | 0 | | 1 | 0 | 1 | 0 | 1 | 0 |
| 10 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

**75.** The pulses from the first bistable circuit are coupled to the second via an inhibit gate comprising VT28/VT29. The first 10 Mc/s pulse changes the state of binary 1. The second pulse puts binary 1 back to its original condition which triggers the 'set' side of the R-S bistable circuit VT26/VT27. In this 'set' condition an inhibit voltage is removed from the gate comprising VT28/VT29. The third pulse changes the state of binary 1 again, and the fourth pulse, as well as changing binary 1 to its previous state, provides a positive pulse to the 'and' gate which is inverted and used to trigger binary 2. The binary stage continues to change state with the arrival of each pulse as shown in Table 3. Because at the second pulse the binary counters are effectively brought forward by 6 pulses, the count of 10 naturally resets the counter.

**76.** The 1 Mc/s counter circuit comprises 4 diode gated bistable circuits or binary stages, whereby the count is decoded by diode 'and' gates, the outputs of which are used to operate the numbered lamp switching transistors. Because the circuit uses four binary stages for its counting, the natural frequency division at the last binary stage would be 16. To make the circuit divide by ten, the count of ten is decoded by a diode gate comprising MR23/MR48, the output of which is used to turn on a reset transistor VT9; the counter then has the facility to divide by ten. The logic diagram fig. 13 shows the binary stages and the gate interconnections required to produce a particular count. VT30, in series with the lamp switching transistors VT10 to VT19, is controlled by the output from the gate generator circuit on board E and is switched off to stop large high frequency lamp currents being drawn during the counting periods. Similar inhibit circuits are incorporated in the circuits associated with the other digits.

**Counter (board G and MM)**

**77.** These two circuit boards are identical and completely interchangeable, and their purpose is to control the four higher order digits of the read-out unit. The decade divider circuits, the reset circuits and the gating circuits, used for decoding the state of the counters, are identical to those described in para. 76.

*Brief description*

**78.** Reference should be made to the logic diagram, fig. 14, and the circuit diagram fig. 30. This counter uses standard divide by 16 circuits which are reset at the count of 10 by internal circuitry. Two dividers are used to obtain the 3rd and 4th counter digits. By decoding each count and using the gated output to control a switching transistor, the appropriate lamp in the transistor collector circuit will be lit. The lamps associated with the other counters work in an identical manner to those described above.

**Power supply circuit (board Y)**

**79.** There are five separate power supply circuits on this board, the function of which is to provide smoothed stabilized supply voltages for the various circuits within the ARI.23180 installation.

Each printed circuit board is fitted with a power supply reservoir. To prevent a reservoir being discharged by loading conditions on another circuit board, the supplies to the boards from board Y are routed via diodes.

*Circuit description* (fig. 31)

**80.** Transistors VT1 and VT2 form a long-tailed pair with the base circuit of VT3 as the collector load of VT1. A preset percentage of the stabilized supply output voltage is measured by VT2 and compared with MR1 zener voltage by VT1. The difference between these two levels is used to control the current through VT3 and VT14, which in turn controls the output voltage. The capacitors C1/1 and C1/2 are provided to store the full wave rectified d.c. input to this circuit and thus prevent VT14 responding to the a.c. content of the rectified input.

**81.** In the event of a reduction in loading on this supply, the output will tend to increase, causing VT2 to conduct more heavily. With VT1 emitter voltage now slightly higher, the current through VT1 will be reduced and therefore the current through VT3 and VT14 will be reduced so that the output voltage returns to its previous level. If a short circuit should occur across the output of these power supplies, the control transistors are protected due to the zener diode MR1 being maintained by the output side of the control circuit. The zener diode maintaining voltage would be removed in the event of a short circuit, causing VT1 and hence VT3 and VT14 to be switched off; this condition would remain until the fault had been cleared. The potentiometer RV1 is adjusted on test and is set so that the maximum current available from the circuit is approximately twice the normal working current. The resistor R16 is provided to give sufficient leakage in the base circuit of VT3 to re-start the circuit after a switched off or shorted condition. The capacitor C3 provides a speed-up facility to the stabilizing action of the circuit. The output from each of the supplies is routed via diodes so that the 'b' lines, which are held up by large capacitors in the event of a supply interruption, do not discharge into the normal lines.

**82.** Apart from the inclusion of additional store capacitors on the input circuit, the stabiliser circuit that provides the +6V supplies is identical in operation to the +12V stabilizer circuits described above. The circuit that provides the −12V supplies comprising VT7, VT8 and VT16, functions in the same way as those described above, but because less stabilization is required, the transistor between the long-tailed pair and the series current controlling transistor shown in the above circuits has been omitted.

**83.** The −24V supply line on this circuit is produced by adding a −12V supply line to the existing −12V line. This additional 12V supply is governed by the combined working voltage of the zener diodes MR10 and MR11 in the base circuit of VT11. The zener maintaining current is taken via R13 and the zener voltage is then used to control the output of VT11; this will be approximately 0·5V below the combined zener working voltage (13·6V).

**84.** VT10 together with MR12 and MR13 functions in the same way as the circuit incorporating VT11 described above, but to provide a +6·6V and −6·6V supply, the output lines are balanced either side of earth by incorporating the potential divider R10 and R11 and earthing the junction of these two resistors. The capacitors C15 and C12 are to provide high frequency stability to the circuit and the capacitors C11/1, C11/2 and C11/3 store the unstabilized +15V supply derived from the full wave bridge rectifier on circuit board Z.

**Power supply circuit (board Z)**

**85.** The six full wave bridge rectifiers on this circuit (fig. 31) provide all the supplies used in the receiver unit.

**Supply filter circuit (board FF)**

**86.** This circuit (fig. 31) is incorporated in the primary feed to transformers T1 and T2 to smooth any transients that may occur on the 115V 400 c/s aircraft supply. The supply to this filter is coupled by relay contacts RLA/1 and RLA/2; relay RLA being energized by the OFF/DIM switch S3 on the read-out unit. Smoothing is carried out by two L.F. filters in each supply line, these being L1/C1 and L2/C2 in the neutral line, and L3/C3 and L4/C4 in the live supply line. The filtered output is then coupled via two fuses to the primary windings of T1 and T2.

**87.** A similar filter circuit comprising L5/C5 and L6/C6 is used to smooth the 28V d.c. supply before it is connected to the aerial amplifier valve heaters, the mains supply relay and the panel lamps. The 28V supply is also connected to the read-out unit via SKT3/r.

**Decoupling circuit CC**

**Note . . .**

*This circuit is not contained on a board but is attached to tags which are fitted to the side of the receiver chassis.*

**88.** There are six separate L.C. filters on this circuit board (fig. 31), the purpose of which is to decouple all the supplies and signals coupled to the aerial amplifier. C6/L6 and C5/L5 filter the balanced line through which a test signal is coupled from the test set Type 1863 to the aerial amplifier. When switching from Loran C to Loran A operation, a 28V supply is coupled via the filter C4/L4 to energize a relay in the aerial amplifier. C3 and L3 filter the 160V valve h.t. supply and C2 and L2 filter the 28V d.c. valve heater supply. Finally C1/L1 is used to filter the 28V supply that is coupled to the aerial amplifier under test conditions.

**Power supply circuit (board EE)**

**89.** The h.t. supplies used in the c.r.t. unit and the aerial amplifier are provided by this circuit. Two of the supplies, the +54V and the +160V, are conventional, whereby the a.c. inputs are full wave rectified and coupled to $\pi$ network R.C. filters. Another supply is derived by voltage doubling the 190V a.c. supply with MR10, MR11 and C4, C5; the resultant output from this circuit being −530V d.c. The 82V a.c. supply is full wave rectified, smoothed and stabilized by the 82V zener diode MR9, and this output voltage is added to the −530V supply in the correct polarity to provide a −612V d.c. supply. The 390V a.c. supply is coupled to a voltage quadrupler circuit comprising MR12 to MR15 and C6 to C9 to produce the c.r.t. unit 1·95kV e.h.t. supply. An output of 1kV is derived from the first voltage doubler section of this circuit, and a further output, which is coupled to the test socket SKT8 is provided by a 60:1 potential divider comprising R5 to R8 which is connected across the 1·95kV output.

*Interconnections*

**90.** The receiver unit interconnections are shown in three parts, A, B and C on fig. 32, 33 and 34 respectively.

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# Chapter 3

# INDICATOR, LORAN

# (C.R.T. CONTROLLER DECCA TYPE 1832)

# 5826-99-955-8337

## LIST OF CONTENTS



## LIST OF ILLUSTRATIONS



### Circuit description

**1.** The function of the c.r.t. controller also known as the (Indicator Loran 5826-99-955-8337 or Decca Type 1832) is to provide visual display of the received Loran A or Loran C signals, together with their selected comparison or tracking gates for the purpose of signal acquisition. The unit houses the cathode ray tube together with all the controls necessary for the operator to adjust the display, and a meter which, in conjunction with the function switch, is used to verify the receiver's a.g.c. and a.f.c. channel sampling voltages to ensure correct operation of the equipment.

**2.** The circuits associated with timebase generation and switching, X and Y gain amplification and c.r.t. brilliance are incorporated on one or more of four printed circuit boards; the boards are as follows:—

(1) Board VA. Panel Electronic Circuit 5826-99-956-5925

(2) Board VB. Panel Electronic Circuit 5826-99-956-5926.

(3) Board VC. Panel Electronic Circuit 5826-99-956-5927.

(4) Board VE. Panel Electronic Circuit 5826-99-956-5928.

Each of the four printed circuit boards are removable and, to prevent incorrect insertion of a board into the wrong socket, coded keys are

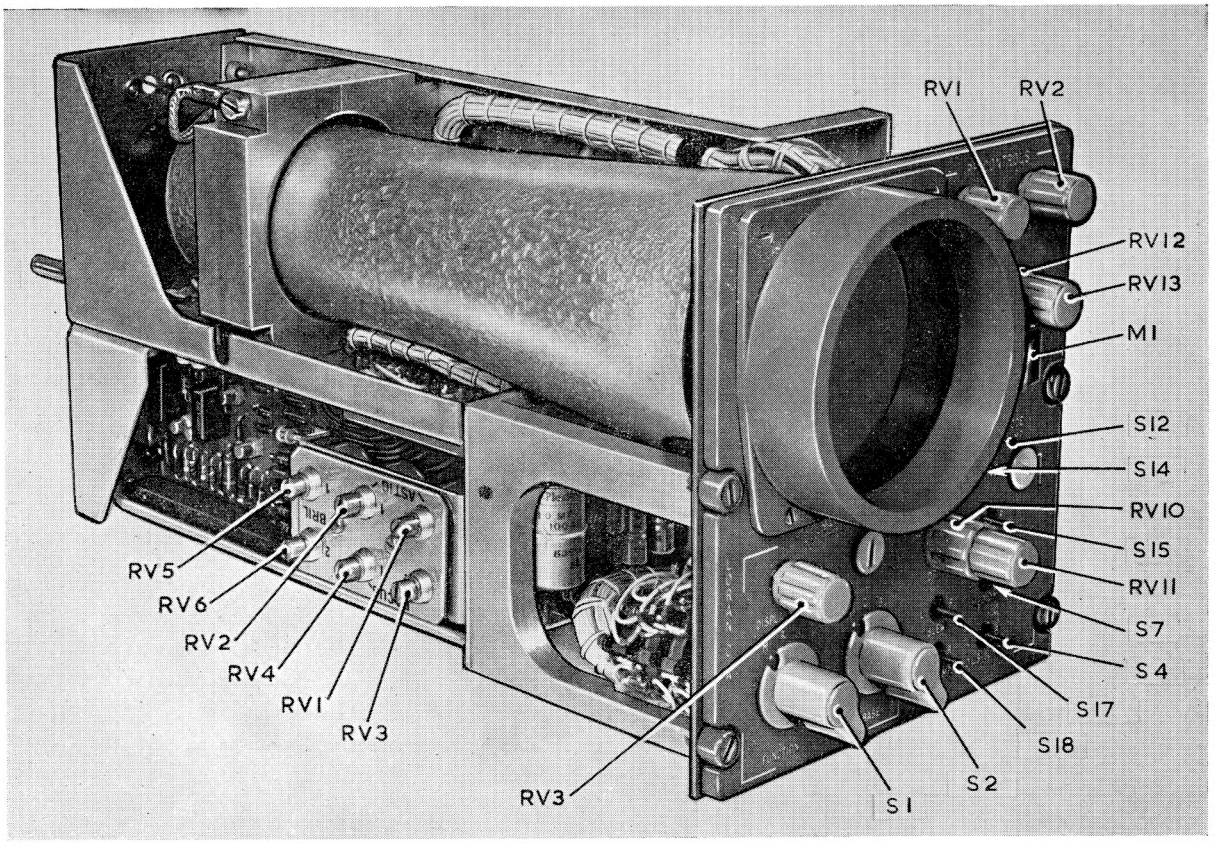


**Fig. 1. Indicator Loran: location of controls**

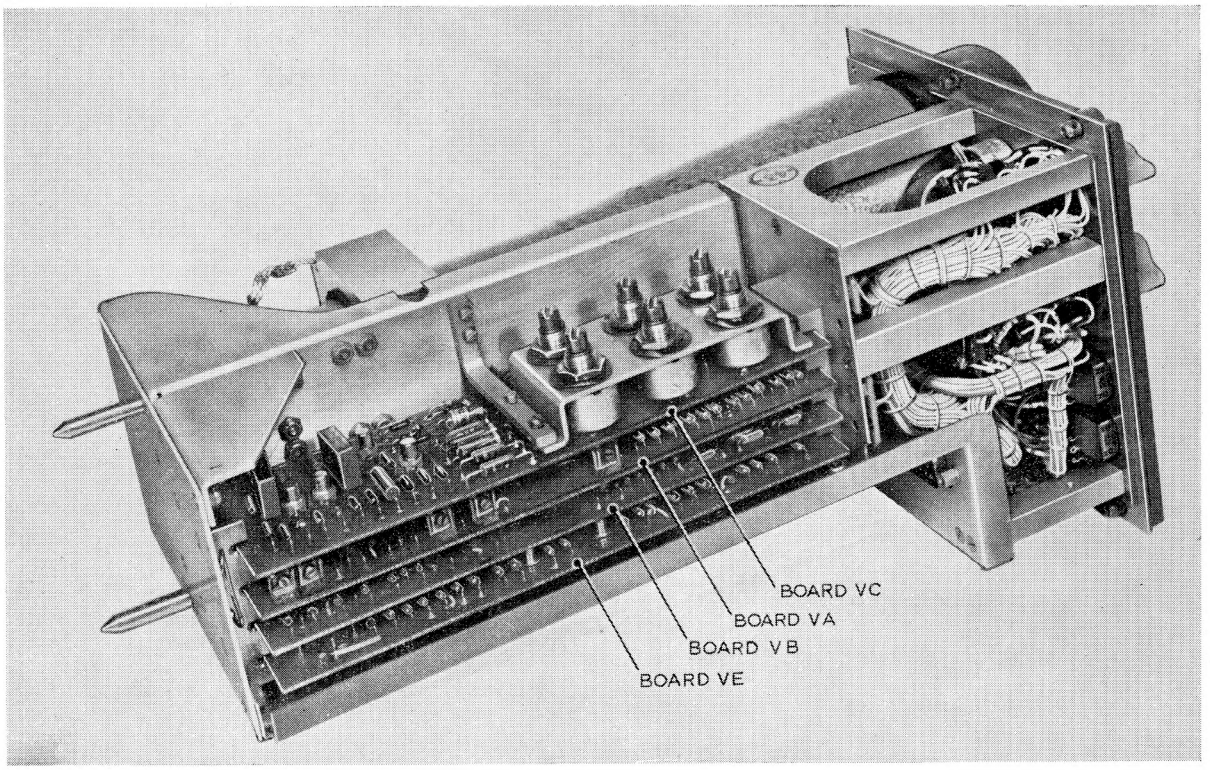


**Fig. 2. Indicator Loran: location of boards**

fitted to the sockets: the key in each socket being in a different position.

3. The function of the c.r.t. controller in the Loran A and the Loran C modes of operation is shown in logic form in fig.4. The circuit diagrams of the boards are given functionally in fig.5 and 6 and individually in fig.7 to 10.

CIRCUIT DESCRIPTION (fig.5)

Board VA

4. This board comprises the circuitry providing the beam switching facility on Loran A operation, the sweep generation and the X and Y axis amplification.

Y amplifier

5. The Y axis amplifier comprises VT5, VT6 and VT7 and has three inputs:

(1) The received Loran C signal from the unity gain, wide-band amplifier VT39, VT38, the amplitude of which is controlled by DISPLAY GAIN, RV3.

(2) The received Loran A pulses, the amplitude of these being adjustable by the LORAN A RF CONTROLS, 2V12 and 13.

(3) A stepped input level controlled by the alternator binary VT9/VT10.

6. VT7 in the emitter circuit of the long-tailed pair VT5/VT6 is a constant current device, by which changes in base to emitter voltage due to temperature change are counter-acted by an equivalent change across MR15 in the base circuit of VT7. RV7 adjusts the Y gain, and RV8 and RV9 control the Y1 and Y2 shifts respectively on Loran A TIMBASE positions 1 and 2.

Beam switching

7. With LORAN A operation selected, the alternator binary VT9/VT10 is operative. This provides a beam-switching facility when observing the Loran A signal. When A - MTS (master time shared) pulse is fed to the VT9 side of the alternator binary, VT9 collector voltage rises to a maximum causing VT6 collector voltage to fall and VT5 collector voltage to rise. This brings the c.r.t. trace just above the centre of the tube face. When the alternator binary changes state due to the arrival of the inverted $\frac{1}{2}$-interval pedestal from VT37, VT9 collector voltage falls reduding the gain of VT6 and increasing the gain of VT5. The c.r.t. trace is then moved to just below the tube centre line. The speed at which these two traces are presented in conjunction with the persistence of the tube produces what appears to be a continuous double trace. The double trace facility is not used on Loran C. The marker pulses are introduced on these two traces by briefly switching VT8 with the Loran A marker pulses.

X amplifier

8. VT11, VT12 and VT13 form the temperature-compensated X amplifier, VT12 being a temperature-controlled constant current dev ice to provide stability and balance. RV10 provides X shift, and RV11 adjusts X gain.

Sweep generator

9. VT14 to VT21 form the sweep generator. VT14 is a temperature-compensated circuit which, once the sweep rate has been selected, becomes a constant current device. The tracking gate inputs, which are eight 4.5µS pulses at 1mS intervals, would normally arrive via C27/R80 (fig.10) but during a sweep period, with VT22 on board VE conducting, the signal is gated out.

10. The sawtooth generator for Loran C operation is first considered. With TIMEBASE switch S2 in position 1 the generator is initiated by a negative-going leading edge of the first tracking gate pulse (fig.3). This changes the state of the bistable stage VT20/VT21, turning VT20 off. VT20 collector voltage go positive as will VT19 emitter. This then turns off VT15, allowing the selected capacitors on tag-board R (depending on the timebase selected) to charge, and as a safety factor VT22 is also turned on, inhibiting any further input pulses. The charge rate is controlled by the current flow through VT14 and the time base switch setting.

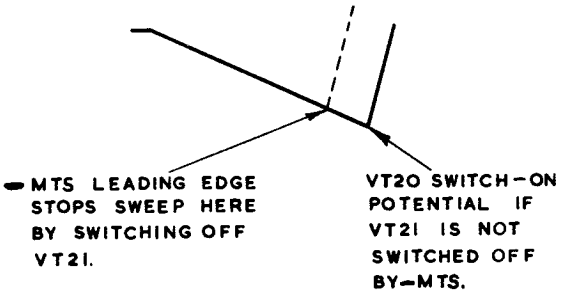


Fig.3 Sweep generator switching

The selected capacitor continues to charge until VT17 emitter voltage rises to approximately -5V; at this point, VT18 is turned on which pulls the base voltage of VT20 in the bistable circuit up to approximately -5V. If the start of the - MTS (master time shared) pulse has not already switched off VT21 in the bistable, VT20 switches on and returns it to its original state. The sawtooth output to X amplifier VT11/VT13 is taken from the divider R62/R63 via emitter follower VT16. The divider provides the correct voltage swing for the X amplifier.

11. With TIMEBASE at position 2 on Loran C operation, the sawtooth generator is started by -MST, -AST or -BST ('scope triggers) and is stopped by the arrival of the -MTS pulse at VT21. The timebase speed is

determined by the selected capacitor on tagboard R and by the selected VT14 emitter resistor. In positions 2 and 3 of TIMEBASE VT14 emitter is routed to a selected resistor on VE board. In position 1 of TIMEBASE VT14 emitter is routed to a resistor in the read-out unit (Chap.4), selected from a bank of resistors associated with the basic rate switching.

12. With TIMEBASE at position 3, the sawtooth generator is initiated by MST, AST or BST triggers and is stopped by its natural preset switching voltage (para.10).

Loran A sawtooth generator switching (boards VA and VB)

13. Because Loran A operation is displayed on two traces for the first and second timebase positions, two sweep waveforms must be produced. The -MTS pulse initiates the start of the first trace (top trace) which is stopped by the inverted leading edge of the ½-interval pedestal which also trips the alternator binary to displace the 'scope display. This inverted ½-interval pedestal pulse is derived from the two-input emitter follower VT36. The trailing edge of the non-inverted ½-interval pedestal occurring 100μs later, then initiates the second sweep, and the trailing edge of the -MTS pulse derived from MR37 and VT36 stops the second sweep and resets the alternator binary, thus returning the 'scope trace to its high position. The duration of this pulse is 100μs to enable flyback and beam displacement to take place before starting the next trace.

Loran A timebase switching

14. On Loran A operation, only one of the eight internally generated tracking gate triggers is required, therefore the master and slave single sweep binaries have been incorporated. The master single sweep bistable VT23/24 is switched to provide an output to OR gate VT25 by the -MTS pulse and is switched back to its original state after 20μs by the first master 'scope trigger. Because VT24 is now in the off position, the other seven tracking gate triggers have no effect. This circuit is not used for Loran C operation.

15. In position 1 of TIMEBASE the single pulse from the master single sweep bistable VT23/24 is fed via OR gate VT25 AND gate VT22 which controls the sweep binary VT20/21. The slave single sweep bistable comprises VT27/VT28, and is controlled as for the master single sweep binary. This circuit is not used for Loran C operation.

Loran A marker pulse generation (boards VE and VB)

16. The only way in which a Loran A master pulse can be distinguished from a slave pulse is by comparing the master to slave and slave to master time differences. The ambiguity is overcome when the operatore ensures that the pulse on the bottom trace is to the right of the pulse on the top trace (TIMEBASE at position 1). The pulse on the bottom trace must then be the slave because a slave pulse follows the master by more than half the pulse repetition rate. Appearing on both c.r.t. traces at position 1 of TIMEBASE are 1.5ms marker pulses; once the received pulses and the marker pulses are aligned, the master and slave pulses are each set up to an accuracy of 1.5ms.

17. By switching to position 2 of the TIMEBASE switch, which is a sweep speed of 1.8mS, two 150μS marker pulses, upper and lower, are presented on the trace; these are triggered by the -MTS and -ATS pulses respectively. The received pulses, because they are at present only accurate to 1.5mS may be anywhere along their respective traces; by operating S15 or S7, the COARSE and MEDIUM SLEW switches, these pulses can be aligned on top of the markers to increase the master to slave pulse alignment accuracy to within 150μS.

18. At position 3 of the TIMEBASE switch, no marker pulses are used, but because the alternator binary does not function in this position, the master and slave pulses can be superimposed on the same sweep trace along the centre of the tube, this time operating S7 or S4 the MEDIUM SLEW and 10μS JUMP switches. By using the Loran A r.f. gain controls on the front panel, the master and slave pulses can be adjusted to the same amplitude; the smaller knob (RV13) controls the amplitude of the master pulse and the larger knob (RV12) controls the amplitude of the slave pulse. The 1.5ms and 150μs marker pulses are produced by monostables VT32/VT33 and VT34/VT35 respectively. These are on board VE and are triggered by marker binary VT29/VT30 on board VB. The MST and AST pulses occur in groups of eight and are applied to the marker binary via OR gate MR9/MR10/VT31. The marker binary changes state on the trailing edge of the first pulse in the MST or AST groups, simultaneously triggering the monostables to generate the marker pulses. The marker binary is returned to its former state by the leading edge of the next available time-shared pulse which is applied via OR gate MR39/MR40. The final seven pulses of the MST or AST Group are thus of no consequence.

**19.** Although both marker monostable circuits are triggered simultaneously, the output from only one at a time is used, this being determined by the TIMEBASE switch settings. (For example the slowest timebase speed incorporates the 1·5mS marker, and timebase position 2 incorporates the 150$\mu$S marker).

**Bright-up circuit (board VC)**

**20.** The purpose of this circuit is to switch the grid bias on the oscilloscope tube so that the trace can be seen during the sweep periods. During the trace flyback period the grid of the c.r.t. is biased back to −80V with respect to cathode; this voltage represents the difference between the supplies which are fed to pin T and pin H of board VC (fig. 10). This −80V state is selected by the bistable stage VT3/VT4 which is controlled by the start and stop sweep bistable circuit VT20/VT21 on board VA. With VT21 in the off state (flyback period) VT2 will also be in the off state. The collector voltage on VT3 will go less negative and so bias off VT1 which will in turn bias off VT2. With VT1 and VT2 effectively open circuit, the voltage at RV5 or RV6 wiper is determined by the resistor network R8, R9, RV5 and RV6, thus producing the −80V no brilliance condition.

**21.** During the sweep period, the bistable stage VT3 and VT4 changes state and VT1 and VT2 are switched on, the potential applied to R9, RV5 and RV6 is that of the zener diode MR3 (5V) plus the collector to emitter voltages of VT1 and VT2. Thus the total voltage applied to the brilliance control potentiometers is approximately 5·3V below the c.r.t. cathode potential, this voltage controls the brilliance of the trace.

**22.** RV5 and RV6 are incorporated to compensate for the reduced brilliance usually obtained when switched to a higher time base speed, a preset voltage is then obtained which, when applied to the grid of the c.r.t. provides adequate illumination for all three timebase switch positions. It is also necessary to make adjustments for change of focus with change of sweep speed; this is catered for by RV3 and RV4. Similarly, to compensate for change of astigmatism RV1 and RV2 are incorporated. The zener diode MR4 in conjunction with MR3 provides the 12V supply to the bistable stage VT3/VT4.

**Ancillary components**

**23.** The function of the front panel tracking controls are described in Part 2. Chapter 2 together with the circuit description of board L, with the exception of the LORAN A DRIFT control which is described in Part 2, Chapter 2, together with board U description.

**24.** The function of the front panel RF CONTROLS are described together with their associated circuitry on either board X or board U. The KC and LORAN C controls are associated with board X and the LORAN A control is associated with board U.

**25.** The AGC/INDEX/AFC switch is used in conjunction with the FUNCTION switch to select the sampling voltage to be displayed on the meter. In the STORE ZERO position of the STORE ZERO/CODE JUMP switch, the a.g.c., a.f.c. and index stores on circuit board FW, K and H respectively are discharged. In the code jump position of this switch, the phase coding applied to Loran C signals is changed.

*Relay switching*

**26.** Indirect relay switching is used to prevent pulse radiation, which would result if direct switching by the LORAN A/C switch (left-hand SELECT STATION switch on read-out unit) were employed.

*Front panel illumination*

**27.** There are three panel lamps on the c.r.t. unit, the purpose of which is to illuminate the panel engraving. This is achieved by using a sprayed perspex front panel and by positioning the lamps within the thickness of the panel such that the inside of the perspex becomes the light path. The brilliance of illumination is controlled by the OFF/DIM switch on the read-out unit. There is one lamp for the R.F. CONTROLS, one for the DISPLAY controls and one for the TRACKING controls.

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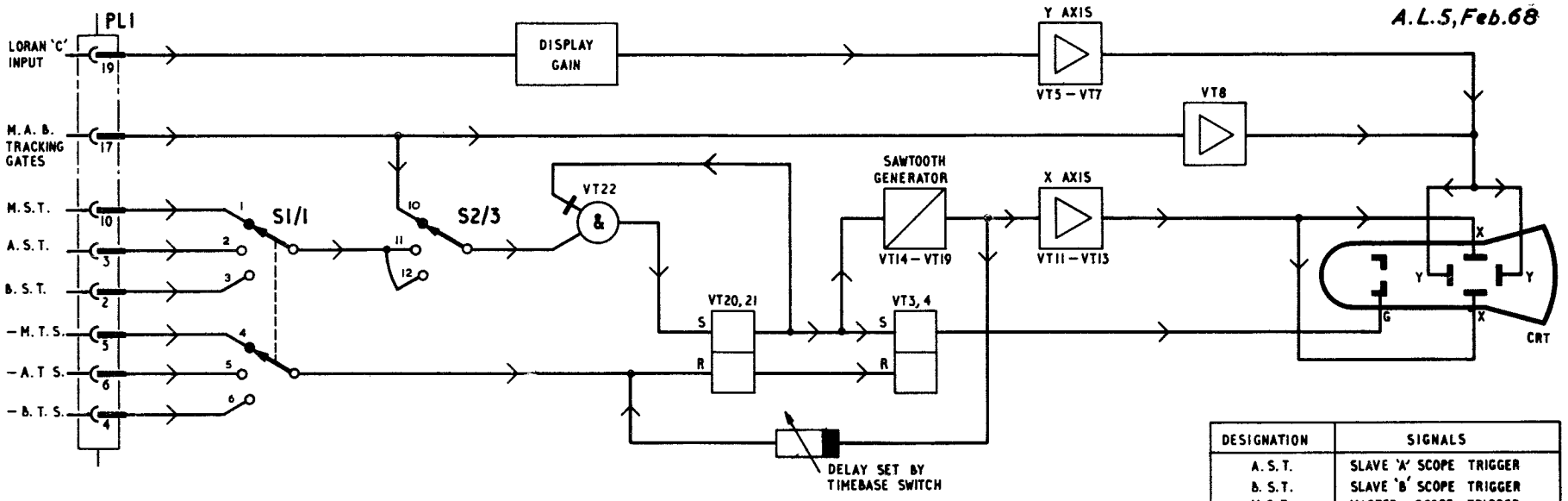
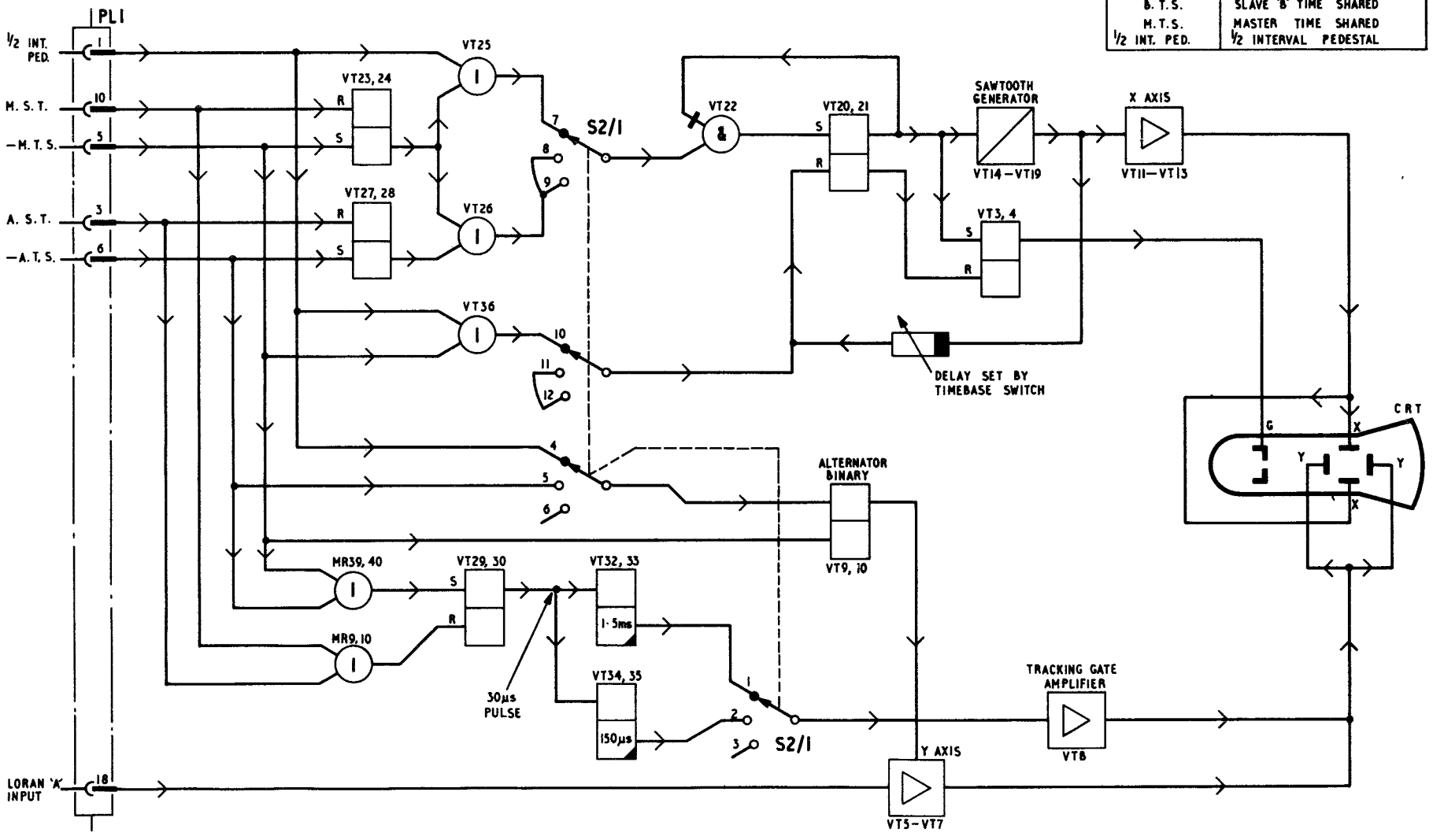


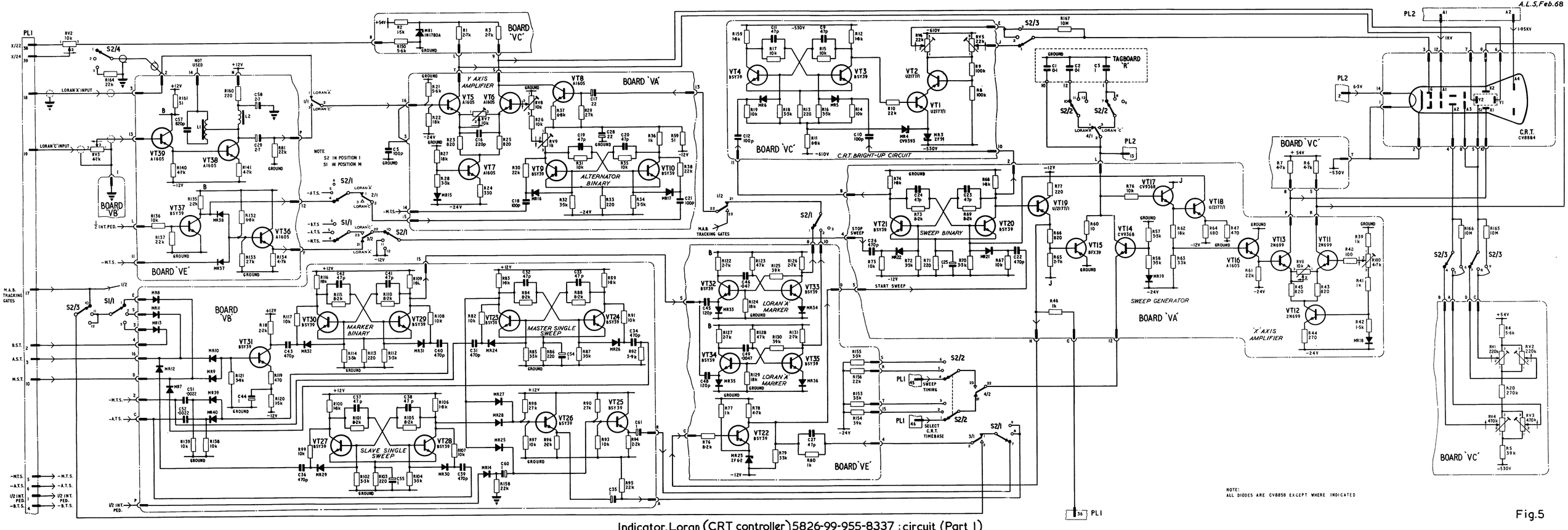

Loran 'C' mode

| DESIGNATION | SIGNALS |
|---|---|
| A. S. T. | SLAVE 'A' SCOPE TRIGGER |
| B. S. T. | SLAVE 'B' SCOPE TRIGGER |
| M. S. T. | MASTER SCOPE TRIGGER |
| A. T. S. | SLAVE 'A' TIME SHARED |
| B. T. S. | SLAVE 'B' TIME SHARED |
| M. T. S. | MASTER TIME SHARED |
| ½ INT. PED. | ½ INTERVAL PEDESTAL |




Loran 'A' mode

Indicator, Loran (CRT controller) 5826-99-955-8337 : logic diagram Fig.4




Indicator, Loran (CRT controller) 5826-99-955-8337 : circuit (Part 1)

Fig.5

PL1 34 35 28 37 32 49 48 31 26 40 44 11 12 13 14 15 16 PL1 7 8 9 42 33 44 PL2 4

TAGBOARD 'H'

MR41 Y218 MR39 Y218 MR43 Y218 MR42 Y218 MR47 Y218 MR44 Y218 MR50 Y218 MR49 Y218 MR48 Y218

21 5 2 12 26 19 16 18 23 17 7

S15 COARSE S7 MEDIUM S4 10μs JUMP S18 ALL JUMP

M1 INDEX/A.G.C./A.F.C. METER

TAGBOARD 'H' 22 6/2 21 7/2

S1/1 (A.G.C.) S1/2 (A.F.C.) S1/1 (INDEX) S1/2 (A.F.C.) S1/2

NOTE: SWITCH 1 IS THE FUNCTION SWITCH

ILP1 ILP2 ILP3 PANEL LAMPS

PL2 6 +12V 12 −12V 9 GROUND

PL1 8 +28V S14 INDEX A.G.C. A.F.C.

RL6/2 RL7/2 MR4 CV8858 MR5 CV8858

PL1 43 GROUND 21 +28V SWITCHED

RL1/2 RL2/1 RL3/2 RL4/2 MR2 IN4002

TAGBOARD 'H' R169 1M

PL2 5 −26V

TAGBOARD 'R' R47 51 C4 22 GROUND

PL1 50 −24V 20

S17 SLEW

RV10 1k LORAN 'A' DRIFT RV11 1k R146 470 R148 3-3k R147 3-3k R145 470 B

N H A I +12V GROUND R161 51 −12V

R149 56k −24V 16 M RV1 100k NOTCH FILTER (KC) GROUND

BOARD 'VE'

F T I +12V −12V GROUND

BOARD 'VB'

R168 560 E J 9 A +12V −12V GROU'D

−24V 1

BOARD 'VA'

M 2 H T GROUND +54V −610V −530V

BOARD 'VC'

PL1 RV13 1k LORAN 'A' 30 U/5

RV12 1k LORAN 'A' 29 U/4

GROUND

S12/2 S12/1

STORE ZERO CODE JUMP STORE ZERO CODE JUMP

23 T/31 22 T/30 24 A.G.C. STOR 6/1 25 A.F.C. STORE 7/1 27 INDEX STORE

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ISSUE 1 Prepared by the Ministry of Technology

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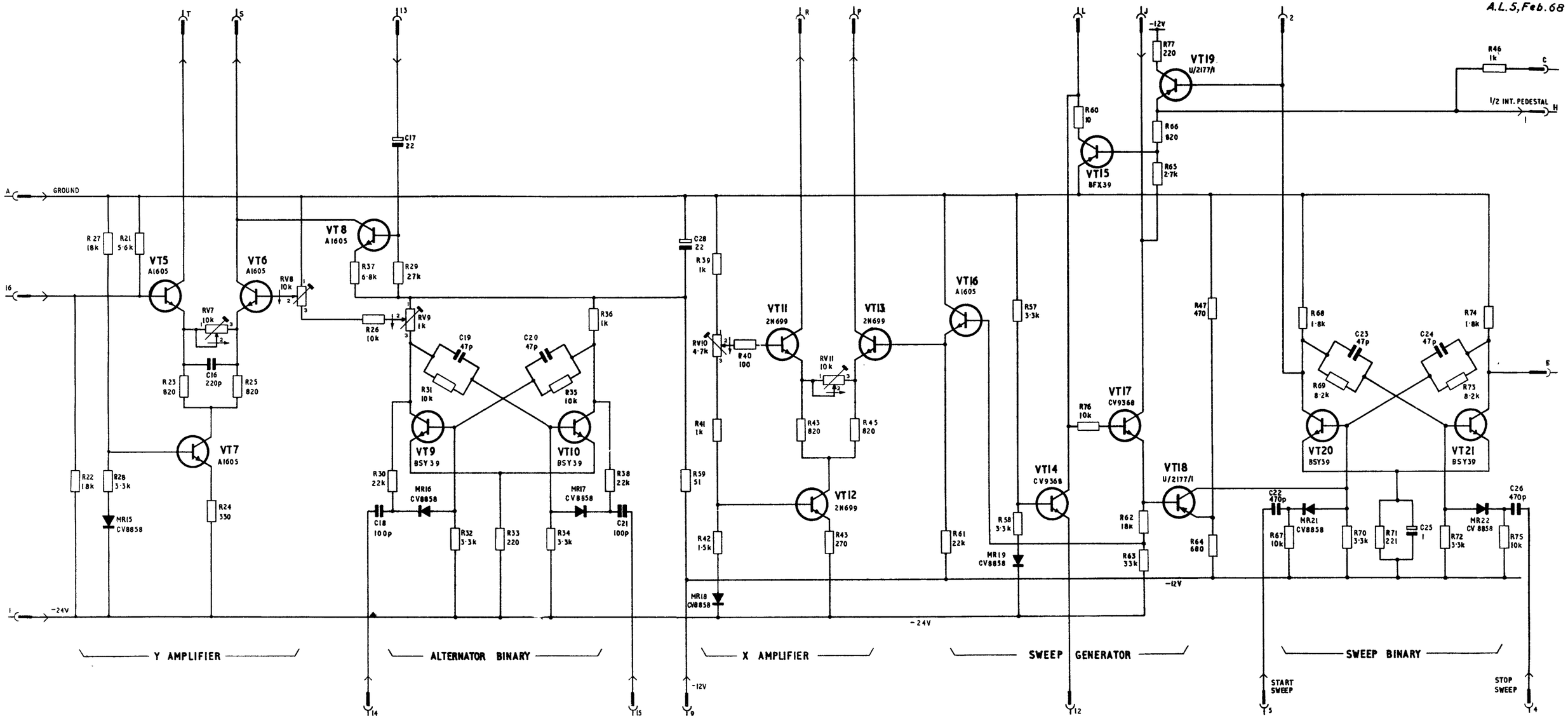
Indicator, Loran (C R T controller) 5826-99-955-8337 : circuit (Part 2)

Fig.6

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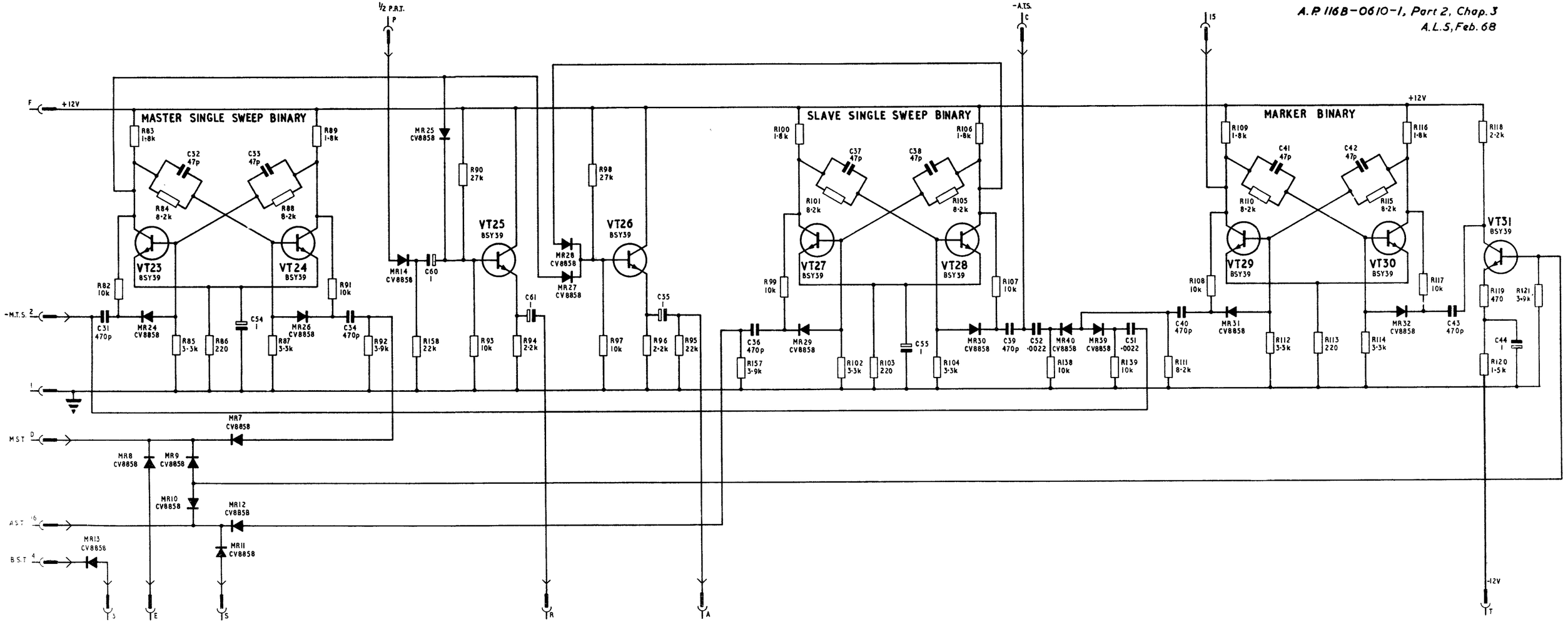
CRT controller board 'VA' : circuit
(Indicator Loran 5826-99-955-8337)

Fig.7




CRT controller board 'VB': circuit
(Indicator Logan-5826-99-955-8337)

Fig.8

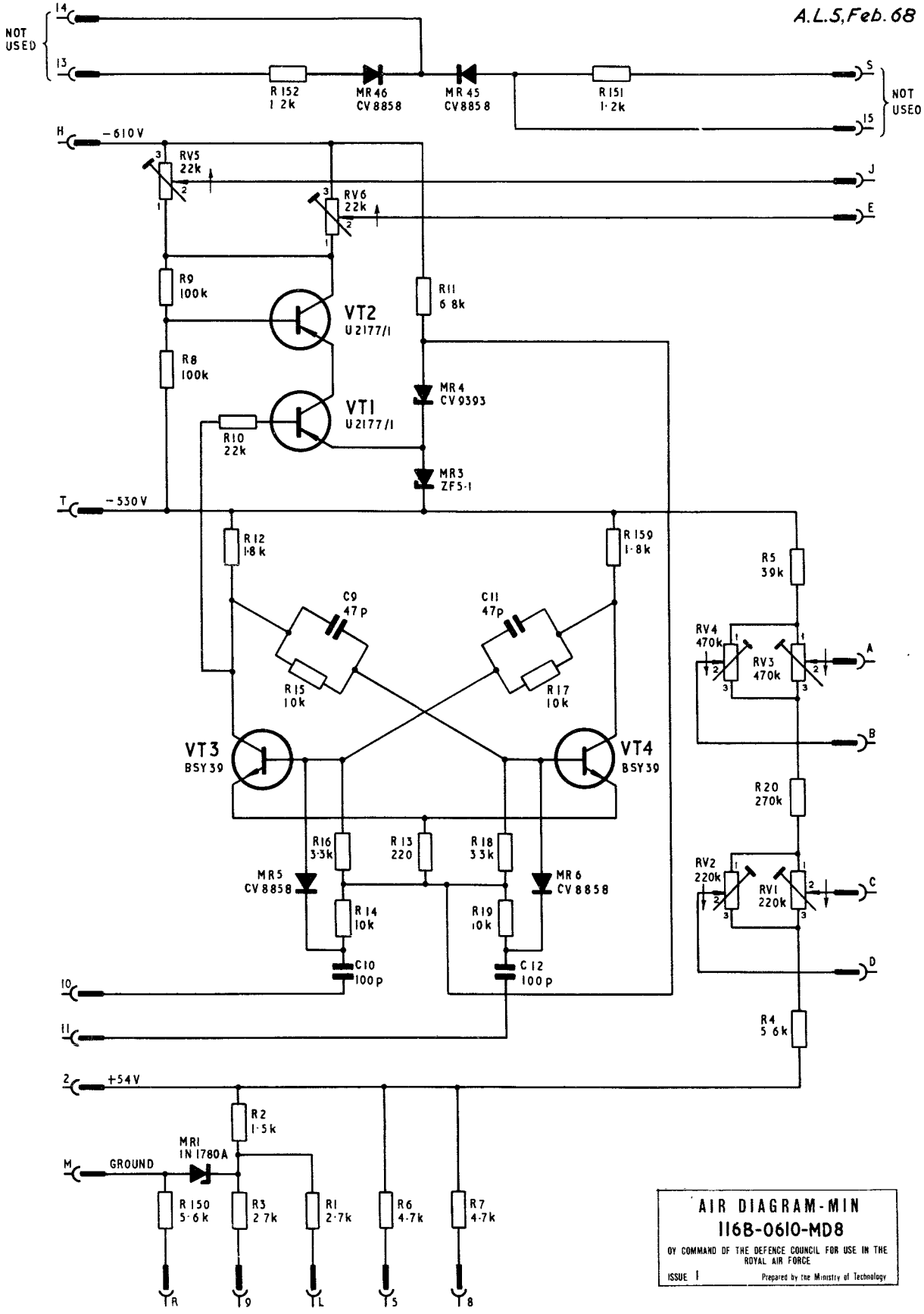
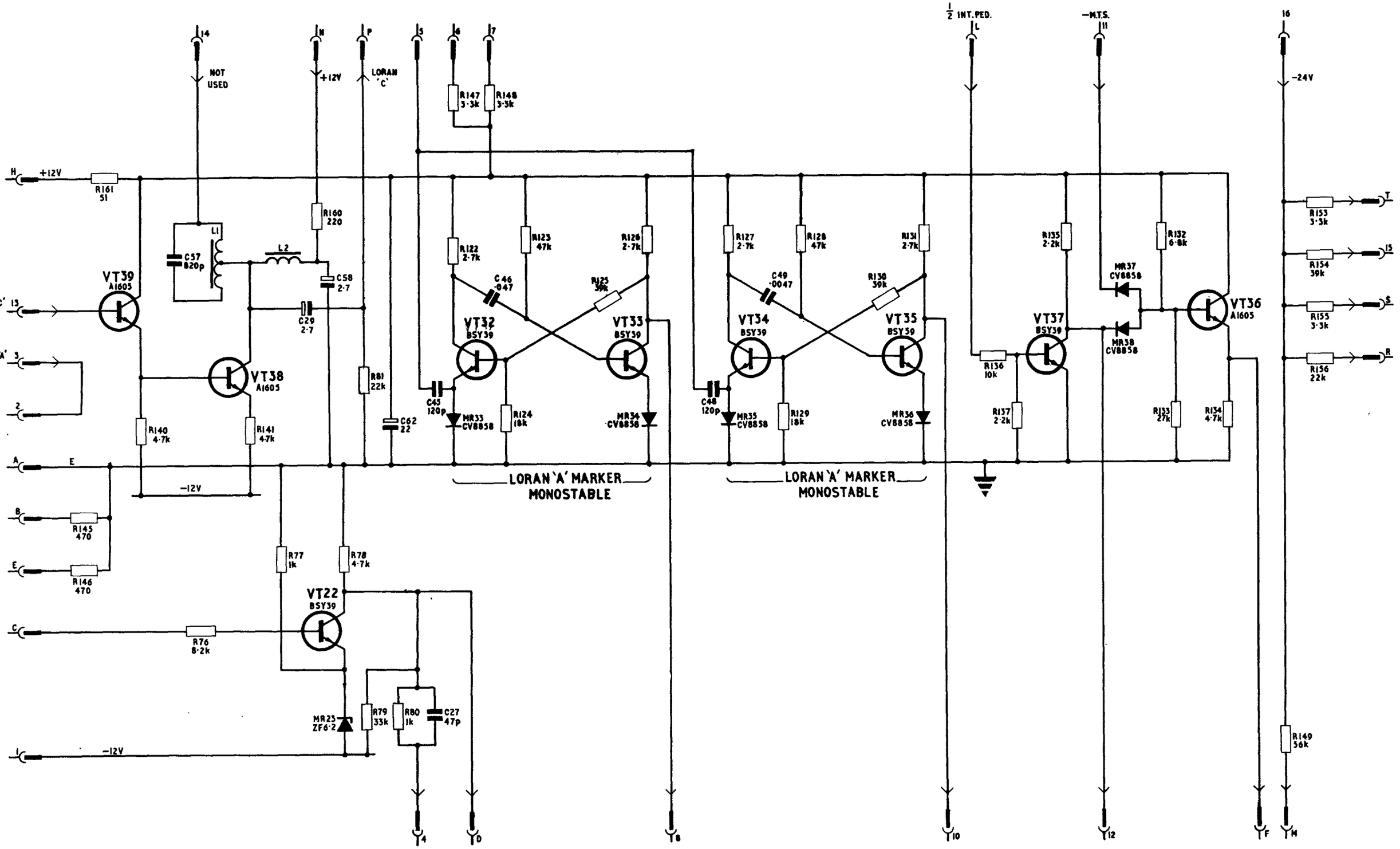



Fig.9. CRT controller board 'VC': circuit (Indicator, Loran 5826-99-955-8337)




C R T controller board 'V E': circuit
(Indicator, Loran 5826-99-955-8337)

Fig.10

# Chapter 4

# INDICATOR, DIGITAL DISPLAY (READ-OUT UNIT DECCA TYPE 1833)

## LIST OF CONTENTS



## LIST OF ILLUSTRATIONS



## INTRODUCTION

**1.** The indicator, digital display or read-out unit Decca Type 1833 (5826-99-955-8338) displays in digital form, the time difference in microseconds between the master pulse and the selected slave pulse. The displays and panel controls comprise:—

1. Five-digit numerical display with associated counter display selector switch, S10 selecting A, A/B (alternating pattern A and pattern B) or B read-out.

2. SELECT STATION switches.

   (a) S13: Loran A 1, 2 and 3, Loran C NARROW and WIDE bandwidth.

   (b) S11: Basic rates H, L, S, SH, SL and SS.

   (c) S9: Specific rates 1 to 9 inclusive.

3. Three alarm lamps (AGC, AFC and INDEX).

4. S3: Combined panel illumination and off switch.

The function of each item is described in Part 1, Chapter 3, para. 15.

## INDICATOR LAMPS

**2.** The read-out indicators each embody ten lamps controlled by the decade counters situated on circuit boards F, G and MM in the Type 1831 receiver unit. The read-out indicators, from right to left, display units, tens, hundreds, thousands and ten thousands of microseconds. Board F controls the units read-out, board G controls the tens and hundreds read-out, and board MM, which is exactly the same as board G, controls the thousands and ten thousands read-out. The supply to each read-out is 15 volts which is filtered by the choke L1 and C1, and coupled via individual 68 ohm resistors to each read-out indicator.

**3.** The A.G.C. ALARM lamp is switched on by a transistor on circuit board FW in the receiver unit when the a.g.c. voltage is outside the normal operating range. The A.F.C. ALARM lamp is switched on by a transistor on circuit board K in the receiver unit when the a.f.c. voltage is outside the normal operating range. The INDEX ALARM lamp is switched on by a transistor situated on circuit board H in the receiver unit; the lamp is lit when the incorrect index point is selected. All three lamps are provided with a +12 volt supply derived from circuit board Y pole 19.

**4.** The two lamps ILP1 and ILP2 illuminate the lettering on the perspex front panel at a brilliance determined by the setting of the dimmer switch S3/2 which also controls the panel illumination of the c.r.t. unit Type 1832. R1, R2, R3, R4, R5 and R6 are connected in series across S3/2 and as the switch is turned progressively clockwise, the panel lamp (ILP1, ILP2) circuit series resistance is reduced, resulting in an increase in panel illumination.

## SWITCH OPERATION

### Loran C/A station selector switch S13

**5.** This switch selects either the Loran C or Loran A mode of operation.

(1) In the first 3 positions (Loran A) of S13/1, R21 is short-circuited and the drift control voltage on RV11 of the c.r.t. unit is connected to the master crystal oscillator control circuit on board K. The crystal frequency is then controlled manually. In the next two positions of the switch, the direct connection from the wiper of RV11 to the crystal oscillator circuit is removed; automatic frequency control will then take place. The sixth position of the switch (fig. 3) is not used.

(2) S13/2 functions in exactly the same way as S13/1 except that the slave A channel is the one that can be controlled manually. With S13 set to the Loran C positions, automatic tracking is carried out.

(3) In the Loran A positions of S13/3, a 28V d.c. supply energizes RLA in the aerial amplifier, to select the correct anode load (T1 primary winding) for Loran A operation. In the Loran C positions of S13/3 the aerial amplifier relay is released, connecting T2 in circuit ready for Loran C operation. Also energized in the Loran C positions of this switch are the relays RL1, 2, 3 and 4 on the c.r.t. unit. These select circuits necessary for Loran C operation. In the Loran A position of this switch all c.r.t. unit relays are released making the circuit operative only to Loran A signals.

(4) S13/4 connects +12 volts to the selected crystal of the local oscillator circuit on board U in the Loran A positions of this switch i.e. positions 1, 2 and 3. In the first Loran C position, RLA in the Loran C r.f. strip, board X is energized, selecting the coupling circuit that gives narrow band operation. In the second Loran C switch position RLA is released and the wide-band coupling circuit is introduced into circuit.

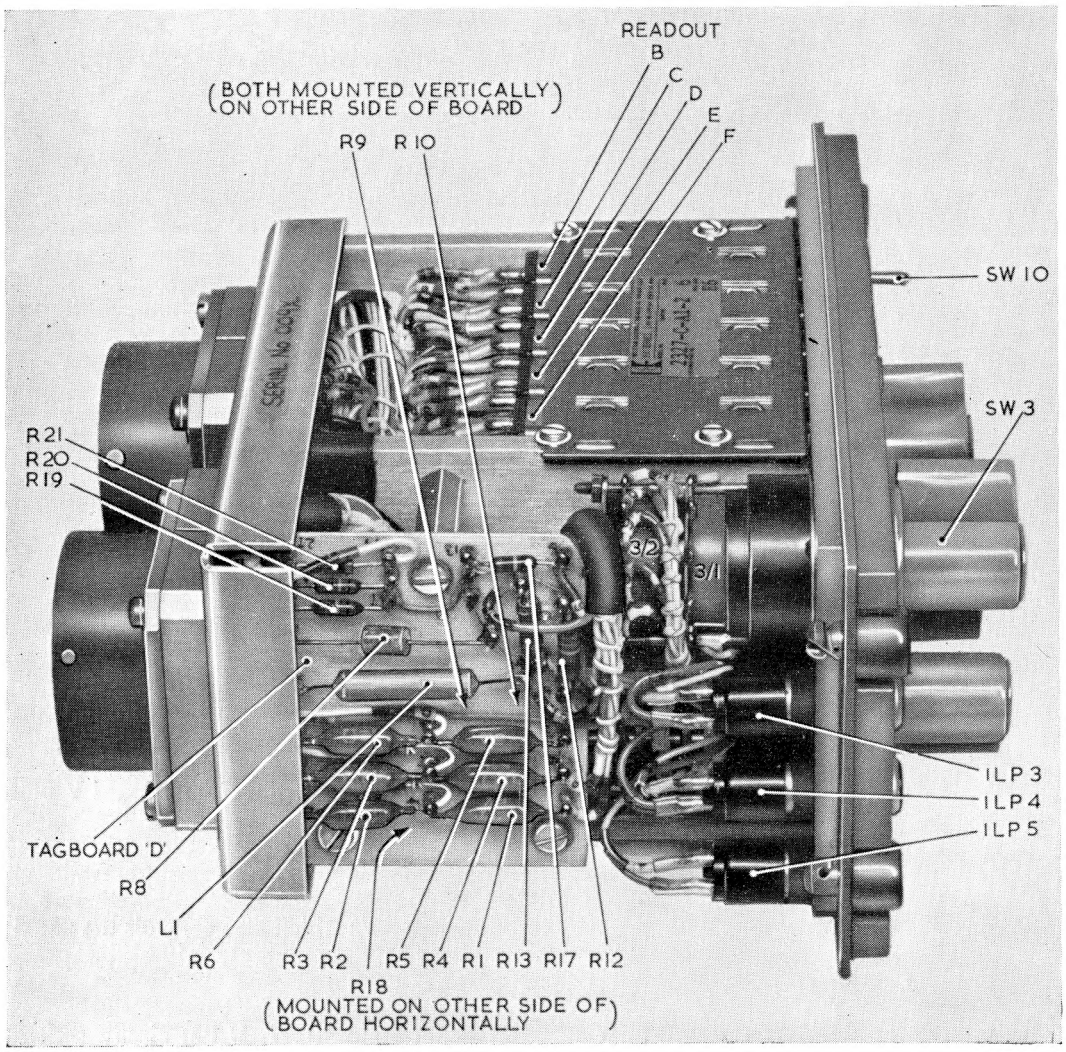



**Fig. 1. Read-out unit: top view**

(5) S13/5 selects the half rate master digitizer trigger for Loran A operation and the full rate master digitizer trigger for Loran C operation.

(6) S13/6 is not used.

**Basic rate selector switch S11**

**6.** This switch selects the 'basic' pulse repetition rate.

(1) Switch banks S11/1 and S11/2 are used to route +6 volts to the master and slave fourth decade divider gating circuits but although these two switch banks serve a similar purpose, they are not used simultaneously, S11/1 is used when the specific rate switch, S9, is set to position 0 and S11/2 is used at all other positions of the specific rate switch. The purpose of this 6 volt supply is to prime the selected gates of the fourth master and slave decade dividers.

(2) Switch banks S11/3 and S11/4 provide the master third decade dividers with a +6 volts priming voltage. As with S11/1 and S11/2, these switch banks are not used simultaneously; S11/3 is operative at position 0 of the specific rate swich and S11/4 is operative at all other positions of the switch. When the binary states of these third decade dividers are at a count corresponding to the selected rate position of S11, an output will be coupled via pole 24 of board FN to pole 22 of board M. Details of the function and operation of the master and slave decade dividers and associated gating circuits are given with the descriptions of circuit boards M, FN, P, Q, R and S (Chapter 2).

(3) With the c.r.t. unit TIMEBASE switch set to position 1 and with Loran A selected on the read-out unit, S11/5 selects the resistor required to operate the c.r.t. timebase at a speed corresponding to the selected pulse repetition rate.

(4) With Loran C selected on the read-out unit and with the c.r.t. unit timebase switch set to position 1, S11/6 selects the resistor required to operate the c.r.t. time base at a speed corresponding to the selected pulse repetition rate.

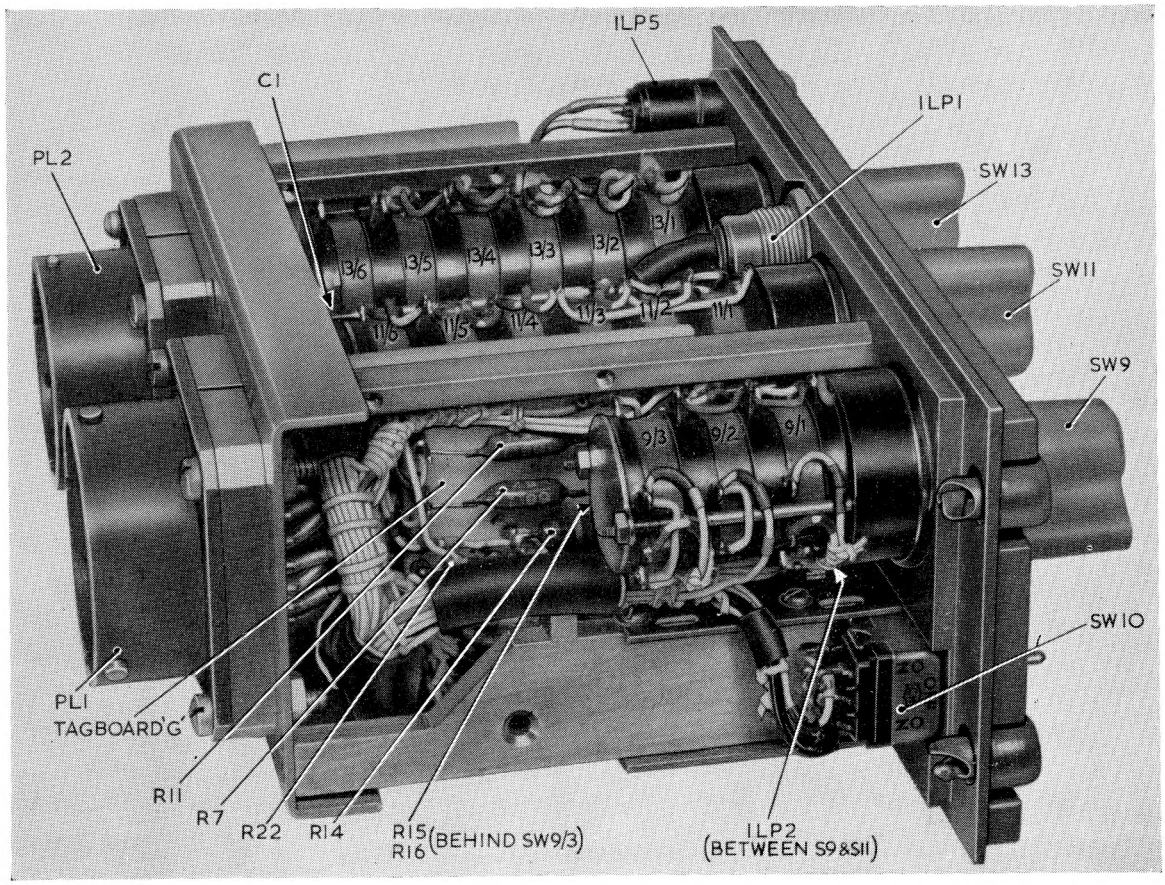



**Fig. 2. Read-out unit: underside view**

**Specific rate selector switch S9**

**7.** The switch S9 is associated with the selection of the pulse repetition specific rate.

(1) Switch S9/1 routes a +6 volt supply to the master divider second decade gating circuits (board M), so that when the binary counter is in the state corresponding to the selected position of this switch, a positive output will be present at pole 27 of board M. The slave A and slave B second decade divider gating circuits are also supplied with +6 volts via S9/1 for the same purpose.

(2) Switch S9/2 connects S11/1 in circuit at switch position 1 (rate 0) and also provides +6 volts to the master and slave third decade divider gating circuits that provide an output at the third decade count of 0. At positions 2 to 8 (rates 1 to 7) of S9/2, S11/2 is connected in circuit and the +6 volt supply is coupled to the gating circuits that provide an output at the third decade count of 9 on the master and both slave third decade dividers.

(3) Switch S9/3 supplies the first decade gates of the master decade divider circuit with +6 volts. When the binary states of the divider are at the count corresponding to the selected rate of S9/3, a +6 volt output will be coupled to the half rate master digitizer trigger circuitry. This switch is used only on the master divider first decade.

**Read-out selector A, A/B, B (S10)**

**8.** S10 is used to select the required display on the read-out unit.

(1) S10/1 primes the gating circuits on circuit board E to accept either the slave A or slave B digitizer trigger or, with the switch in the A/B position, both slave digitizer triggers will be accepted alternately at 1 second intervals.

(2) S10/2 modifies the speed of the astable circuit comprising VT26 to VT28 and VT38 to VT39 on circuit board E. With A or B selected this astable circuit functions at twice its normal frequency, but because A only or B only will be presented on the read-out unit, the read-out presentation still occurs at 1 second intervals.

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272866/D.547919 220 7/68 Gp.483

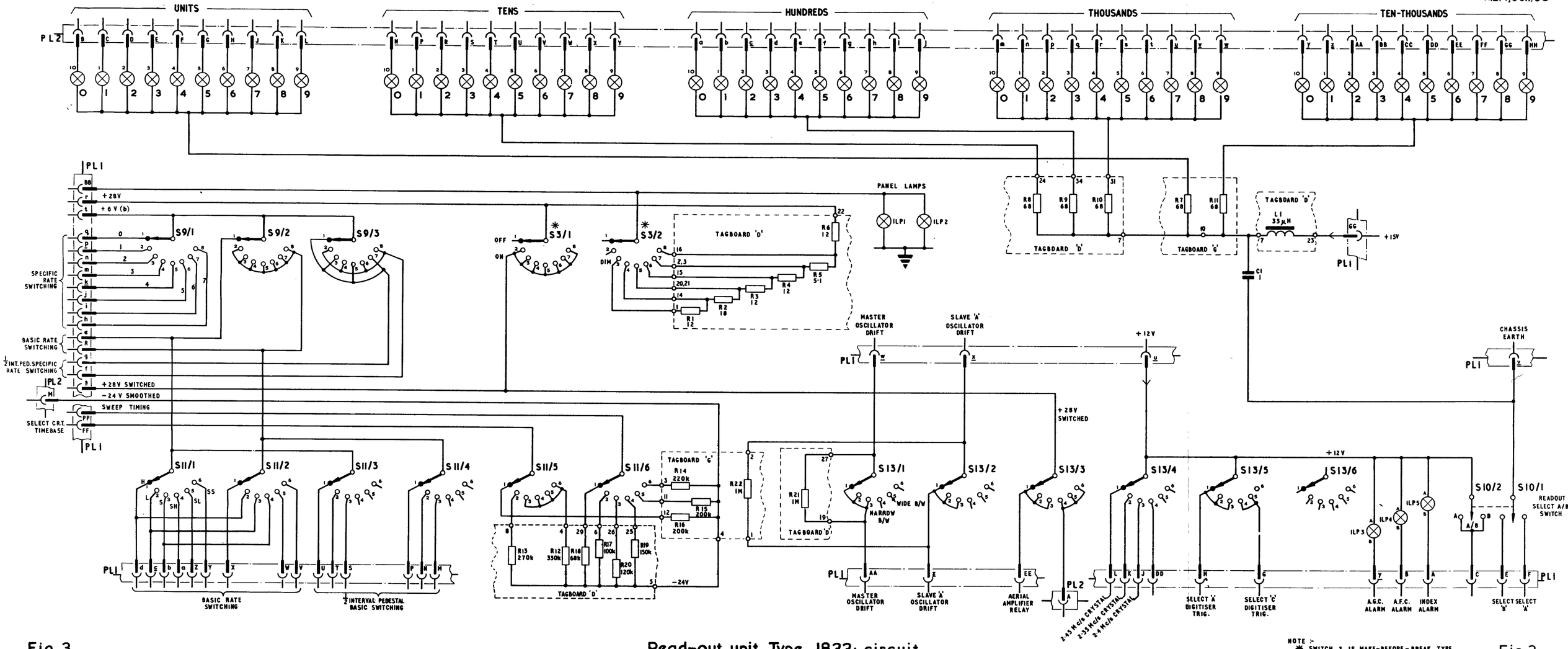


Fig. 3

## Read-out unit Type 1833: circuit

NOTE :-
* SWITCH 3 IS MAKE-BEFORE-BREAK TYPE

Fig. 3

# PART 3

# SERVICING AND FAULT DIAGNOSIS

# Chapter 1

# FIRST LINE TEST SET TYPE 1863

## LIST OF CONTENTS



## LIST OF ILLUSTRATIONS



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(to be found in A.P.116B-0610-10)



## INTRODUCTION

**1.** The first line test set Type 1863 (Test Set, Loran, 10S/6625-99-107-1415) is a portable piece of test equipment used to check the performance of ARI.23180 and in the event of unsatisfactory performance, to diagnose which of the four units of this installation is faulty. Although it is primarily for testing the ARI.23180, it can also be used to test any other Loran C/A installation. In addition to simulating a transmitted Loran C or A signal and providing signals to simulate those generated in the receiver unit Type 1831 (Receiver Loran 5826-99-955-8336), the test set also provides a reference for the receiver unit oscillator frequencies and the oven temperature. The first line test set is also intended to comprise one of two units to form the 2nd/3rd line test set.

**2.** Produced within the test set are the various signals required by the ARI.23180 equipment for normal operational use. Received signals are simulated by the test set to test the aerial amplifier. the receiver unit and the c.r.t. unit, and these signals are time-shared to provide a known reading on the readout unit digital display to verify its operation. The test set is able to monitor important voltages within the 1831 receiver unit and also to monitor its own internal voltages, thus providing a self-test facility.

### Summary of tests

**3.** This test set provides the facility to check the receiver voltages and oven temperatures, and by providing the Loran signals as mentioned above it can be used for the following:

(1) To carry out a full Loran C signal acquisition procedure, which with the aid of the Fault Check Table (Chapter 2, Table 1), can be used to isolate any unit which may be faulty.

(2) To check the pulse repetition rate selection circuitry on the receiver unit by providing the different rates.

(3) To check the operation of the receiver in simulated flight towards and away from the transmitters.

(4) To carry out a full signal acquisition procedure on Loran A operation.

## GENERAL DESCRIPTION

**4.** The 1863 equipment embodies seven plug-in printed circuit boards together with a mains transformer, a rectifier sub-panel and an oven unit. These units are mounted within a frame containing the front panel, behind which are two tray-shaped side plates mounted at 90° from the panel at each end. Supporting the rear of these plates are two cross members to form a rigid construction. The lower cross member is fitted with two receptacles having internal spring-loaded bearing plates to ensure case interchangeability. These receptacles mate with spigots within the case so that the whole assembly remains rigid even during transportation.

The R.A.E. case used for this test set is size 15S, Type number WTA/186215/3/AT to specification number RAE/RSP. 1966. With the test set inserted in the case, the whole unit including the lid becomes airtight, but pressure release screws are fitted both to the lid and the case to ensure case pressure equalization during air transit.

**5.** The seven plug-in printed circuit boards are coated with a special lacquer that does not affect normal soldering practice when replacing a component. The lacquer adds to the mechanical strength of the boards as well as providing a moisture-proof seal and greatly increasing the tracking resistance between components. Attached to each printed circuit board by screws is a metal plate: this serves to locate the board and also provides electrostatic screening between one board and the next.

### Front panel

**6.** Mounted on the front panel are all the controls necessary for testing the ARI.23180 up to first line stage. Signal and supply plugs and sockets that are required for testing the installation are also on the front panel, together with a meter to give a voltage level checking facility.

### Switches

**7.** The test set houses the following operator controls:

(1) The POWER SOURCE switch has five positions, the positions of which are as follows:

OFF

The 115V and 28V supplies are disconnected from the test set.

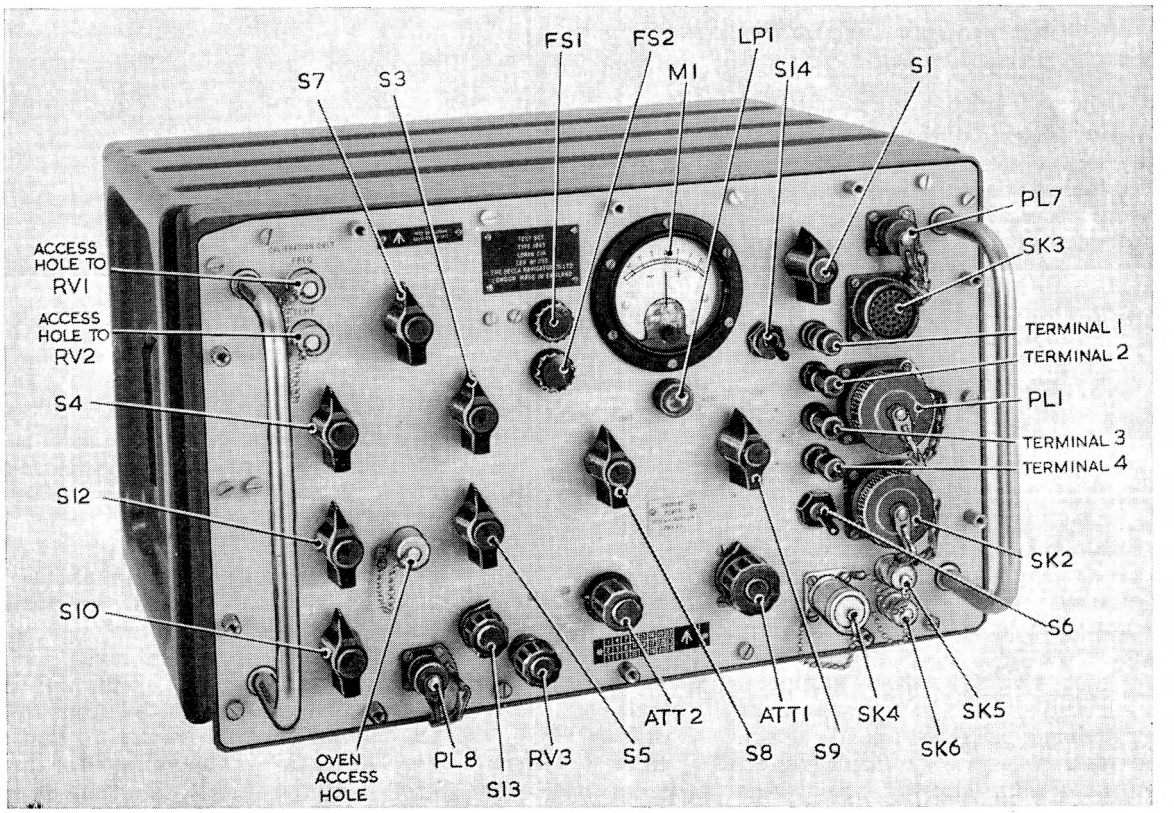


**Fig. 1. General arrangement**

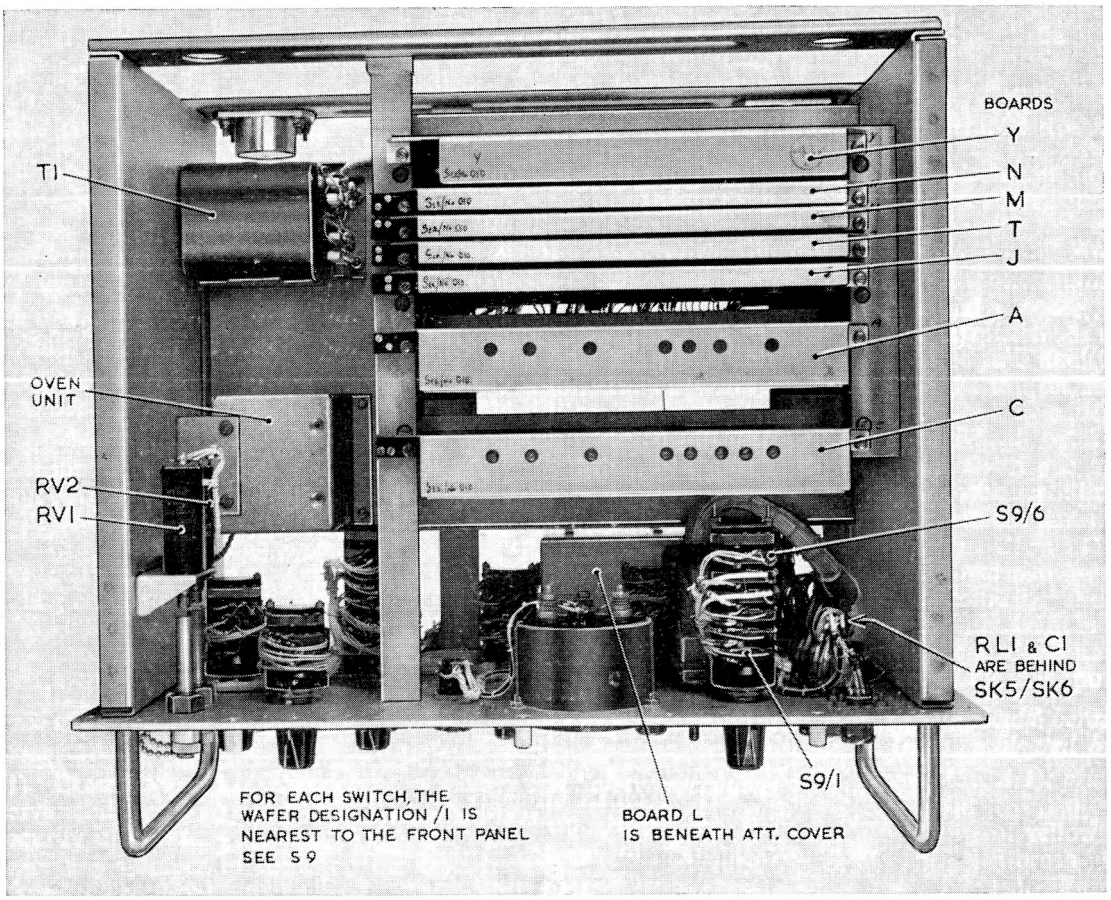


**Fig. 2. Top view (cover removed)**

1831 1
The supplies from the Type 1833 receiver unit are coupled via connector 1 to drive the test set. A test signal is provided by the set via pins G and H of plug 1, and the aerial amplifier test relay is energized.

1831 2
The supplies are connected as at position 1 but the aerial test relay is de-energized and the signal is removed from plug 1 pins G and H.

EXT 1
The power supplies required for the test set are derived from an external source via plug 7. In this position the test set functions normally but is usually used for verifying its own oven temperature.

EXT 2
The supply is connected via plug 7 as above, but the equipment is only used in this position when used in conjunction with its complement, the 1958 unit for the purpose of second or third line testing.

(2) The VOLTS CHECK switch is used in conjunction with the METER FUNCTION switch. The positions of the METER FUNCTION switch are as follows:—

1832
This position permits circuit testing of some of the 1832 c.r.t. unit spring-loaded toggle switches together with their associated supply cable.

115 ac
The meter monitors the 115V supply to the test set.

1831
At this position, the VOLTS CHECK switch is introduced into circuit to measure the receiver unit generated voltages; the white engraving on the VOLTS CHECK switch is applicable.

1863
The VOLTS CHECK switch is introduced to measure the voltages within the test set; these voltages are engraved in green around the VOLTS CHECK switch.

TEMP
In this position the meter monitors the voltage across the temperature comparator connected to the PROBE outlet on the test set (socket 8), the meter reading is dependent upon the temperature of the oven and the setting of the temperature ZERO control.

AFC
At positions M, A or B of this switch section, the voltage on the a.f.c. stores for master, slave A and slave B in the 1831 receiver unit are monitored respectively. With the receiver functioning correctly the meter should

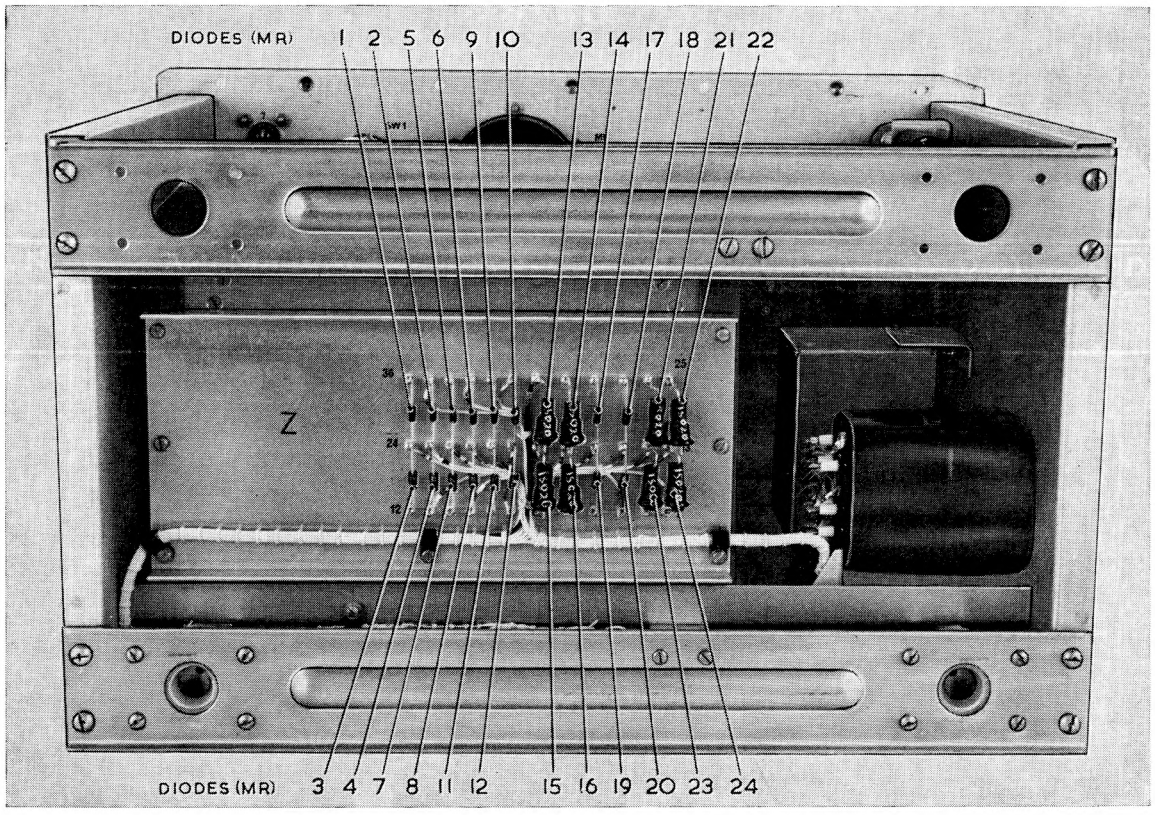


**Fig. 3. Rear view (cover removed)**

read zero ± 1 division (meter f.s.d. is 4V d.c. in each direction).

INDEX

The voltage on the slave A index store in the 1831 receiver unit is monitored. If the receiver is functioning correctly on the index cycle, the meter should read zero ± 4 divisions (meter f.s.d. is 4V d.c. in each direction).

AGC

At positions M, A or B of this switch section, the voltage on the a.g.c. stores for master, slave A and slave B in the 1831 receiver unit are monitored. With the receiver functioning correctly and with a test set input of −67dB + dB equivalent of aerial (see Part 3, Chap. 2, Table 2) the meter should read zero ± 5 divisions (meter f.s.d. is 4V d.c. in each direction).

(3) ATTENUATOR 1 is a stepped control (0 to −100dB in 20dB steps) and ATTENUATOR 2 is a variable control (0 to −30B), both of which are used to control the output of the internally generated signal from connector 4, and plug 1 pins G and H: the attenuators are connected in series.

(4) The SIGNAL SELECT switch has six positions: these are as follows:—

A1

Loran A frequency 1950 kc/s

A2

Loran A frequency 1850 kc/s

A3

Loran A frequency 1900 kc/s

C

Loran C signals are selected in this position.

−

Minus 12V is applied to the 1831 receiver unit index and a.f.c. d.c. amplifiers.

+

Plus 12V is applied to the 1831 receiver unit index and a.f.c. d.c. amplifiers.

(5) The FREQ control is used to adjust the frequency of the 5 Mc/s internal reference oscillator: this control is used for calibration only.

(6) The TEMP control is used to adjust the temperature of the test set oven to 63·0°C. The control is only adjusted during monthly calibration against an accurate thermometer.

(7) The SPECIFIC RATE switch in conjunction with the BASIC RATE switch selects the appropriate gates on the counter boards to provide the required repetition rate.

(8) The SLAVE SETTING switch has 9 positions. In the OFF position, only the master signal is presented to the ARI.23180 equipment. At position 1, master, slave A and B pulses are coupled to the equipment; the time interval between the master pulse and the slave A pulse is 10,000μS and the time difference between the master A pulse and slave B pulse is 20,000μS. For each successive position of this switch, there is an additional 10,000μS between master and slave A, and master and slave B pulses.

(9) The CODING switch has three positions:

OFF

No coding is applied to the internally generated Loran C signal, therefore all pulses within the Loran C waveform envelope will be positive at plug 1, pin G and at the left hand pin of socket 4.

BELLY

Coding is applied to the Loran C pulse groups. The first pulse in each pulse group is negative code and subsequent pulses in these pulse groups will be inverted from their normal codes both for interval 1 and interval 2 pulse groups, e.g. master 1, master 2, slave A1, slave A2 and slave B1, slave B2 pulse groups. The first half cycle of the first envelope in each pulse group is negative at pin G of plug 1 and on the left hand pin of socket 4.

DORSAL

Coding is applied to the Loran C pulse groups, but this time the coding at pin G of plug 1 and at the left hand pin of socket 4 is the normal code.

(10) The VELOCITY CHECK switch simulates three received signal conditions: these are as follows:

ZERO

100 kc/s output signal is provided by the test set to simulate a stationary aircraft.

MINUS

The output signal from the test set simulates a closing speed between all three transmitters and the aircraft of 800 knots.

PLUS

The output signal from the test set simulates the three transmitters moving away from the aircraft at 800 knots.

(11) The COMPARATOR control is a three position switch used to zero the meter reading for the purpose of making temperature comparison checks on the 1831 receiver oven. The control becomes operative with the METER FUNCTION switch set to TEMP. At the OFF position the test set meter does not read, but position 1 is the coarse position for preliminary meter zero setting and position 2 is the fine adjustment position.

(12) The ZERO control is used to position the meter reading at zero when the METER FUNCTION switch is set to TEMP and with the test set oven temperature correctly set.

(13) The EXT METER switch is operated by a spring-loaded toggle. The switch is normally in the off position but, when pressed, it connects an external meter (CT498A) in circuit.

(14) The LAMP ON/OFF switch connects 28V to terminal 4 on the test set panel for the purpose of supplying a lead lamp. The earth return for the lead lamp would be on terminal 3.

**Plugs and sockets**

**8.** Eight plug/sockets are mounted on the test set panel, the purposes of which are as follows:—

(1) Plug 1 receives all test voltages for first line testing and appropriate signals for second/third line testing. The simulated Loran C signal is coupled to the ARI.23180 equipment via pins G and H.

(2) Socket 2 provides all the signals required to test an 1832 c.r.t. unit.

(3) Socket 3 is used during second line testing and is used to couple the test set to the 1958 second line test set.

(4) Socket 4 supplies the test signal direct to the receiver unit (1831) to eliminate a possible faulty aerial amplifier.

(5) An output of 5 Mc/s is provided at socket 5 for monitoring the test set internal oscillator.

(6) An output of 100 kc/s is provided at socket 6 for monitoring the test set internal decade dividers.

(7) Plug 7 is used to connect the test set to the external power supply.

(8) Plug 8 is used to make connection to the probe (thermistor) when verifying oven temperature.

**Miscellaneous items**

**9.** There are four terminals fitted to the front panel of the test set. Terminals 1 and 2 are for the external meter (positive on pin 1 for positive voltage measurement) and terminals 3 and 4 are for supplying a 28V lead lamp. Terminal 3 is earth.

**10.** Illumination of the lamp situated beneath the meter indicates that the supply is connected to the test set either from the 1831 receiver unit or from an external source, and also indicates that the POWER SOURCE switch is not set to OFF.

**11.** Two fuses are incorporated, one of which is in the 115V supply line to the test set and the other is in the 28V supply line.

**12.** The meter has a 250-0-250$\mu$A movement and is scaled 16-0-16 and 32-0-32 divisions. This scale is multiplied or divided to correspond to the voltage being monitored by the test set; the scaling for the particular voltage being measured is given under the heading 'Voltage Tests', Part 3, Chap. 2, para. 3.

## CIRCUIT DESCRIPTION

**13.** In order to simulate a Loran C or Loran A transmission, this test set incorporates four crystals, three of which are for Loran A operation and the fourth is used on Loran C. By dividing down the 5 Mc/s crystal frequency to 100 kc/s the Loran C pulse frequency is produced. The correct time intervals of these pulses are controlled by a master pedestal generator, which is in effect a four decade frequency divider, boards TM and TN. From this four decade divider are produced the full rate pedestal, this being a function of the pulse repetition rate selected, and the master, slave

A and slave B time sharing periods. Master and slave A time-sharing periods are used on Loran A and all time sharing periods are used on Loran C operation. Generation of the Loran C pulse is carried out on board TC and the encoding waveforms which control the phase polarity of the pulses within the pulse envelope, are generated on board T. The Loran A pulses, which are generated by board TA, are envelope modulated pulses at the selected Loran A frequency, i.e. 1850 kc/s, 1950 kc/s or 1900 kc/s and occur 50$\mu$s after the start of MTS and 50$\mu$S after ATS; there is only one slave required on Loran A operation. An output attenuator is incorporated to adjust the level of the signals and an emitter follower output is incorporated to provide a low output impedance. As well as providing the Loran A or Loran C pulses, this test set provides tracking gates to enable the c.r.t. unit Type 1832 to be tested on its own. The test set is designed to run off the aircraft supply, this being connected when the test set is coupled to the receiver unit Type 1831 by the test lead 5826-99-195-8851 (53 ABE).

**Oscillator and frequency divider circuits, board TJ 5926-99-194-5220**

14. This circuit board houses the crystal controlled oscillator and frequency divider circuits which provide the 100 kc/s frequency. Also incorporated on this board are the following circuits:—

(1) Squarer shaper
Used to shape the 100 kc/s output of these frequency dividers before coupling them to the main decade dividers, board TM, and to provide the 100 kc/s clock pulse waveform.

(2) Time-sharing generators
These are switching stages controlled by MTS, ATS and BTS signals decoded from board TN and TM. The function of the circuits is to provide positive and negative polarity low impedance time-sharing signals.

(3) 'Scope trigger generators
This circuit provides the master, slave A and slave B 'scope triggers on three lines from a common generated line.

(4) Fixed velocity circuit
This comprises a potential divider which supplies the receiver a.f.c. circuit with a fixed voltage representing a fixed aircraft velocity. A similar circuit is provided to provide a minus velocity check.

(5) AGC, AFC, INDEX reference circuit
This is also a resistive network, used to provide a reference voltage to the test set metering circuit.

(6) The oven overheat control circuit.

(7) The resistor networks associated with the test set BASIC RATE switch, used to provide the correct ARI.23180 c.r.t. timebase speed.

(8) The mains supply meter rectifiers.

(9) All the meter multipliers for the various positions of the VOLTS CHECK switch S9.

**15.** The crystal oscillator used in this test set is identical to the one in the ARI.23180 installation and is described in detail in Pt. 2, Chap. 2, para. 39. The frequency divider comprising VT6 to VT16 is also the same as the one in the receiver unit and is described in Pt. 2, Chap. 2, para. 40.

**16.** The squarer shaper circuit comprising VT18 to VT19 is a monostable circuit having a 5$\mu$S time constant; because this monostable circuit is triggered by 100 kc/s pulses, the output signal will be a 100 kc/s square wave. An emitter follower stage is coupled to each side of the monostable circuit. VT20 output provides the input to the master pedestal generator, board TM, and VT17. VT21 is purely an inverter stage used to provide the tracking gates from the tracking gate triggers.

**17.** VT22 and VT27 provide the plus and minus MTS, ATS and BTS waveforms and, as the three circuits are similar, only the master one need be described. On receipt of the decoded MTS signal from the pedestal generator board TN, VT22, which is an inverter stage, will conduct and so produce a −MTS signal at its collector. By using a further inverter stage VT23, the +MTS signal is produced. It is necessary to reproduce the +MTS signal as the decoded MTS signal is inherently spiky. These spikes are removed by the smoothing circuit R23.3/C22.1 and further precautions are taken to remove the spikes by incorporating the threshold circuit MR22.1, MR22.2 and R22.2. This prevents the inverter stages responding to low level pulses.

**18.** For the generation of the master, slave A and slave B 'scope triggers three 'nand' gates are used; these are VT29/VT30, VT31/VT32 and VT33/VT34. A composite signal comprising the master, slave A and slave B 'scope triggers is coupled to VT28 where the signals are inverted and coupled to each of the 'nand' gates. Also applied to the 'nand' gates is a master, slave A or slave B time-shared waveform. The resulting output from each gate in turn will be a group of eight 'scope triggers, coincident with MTS, ATS and BTS respectively. These pulses are identical to those produced in the receiver unit and are used when running the c.r.t. unit from the test set.

**19.** The resistive network comprising R0.51 and R0.23 to R0.26 together with RV2 and RV3 provides the variable capacity diodes in the crystal oscillator circuit with a fixed d.c. bias. By selecting the MINUS position of the velocity check switch a speed of 800 knots towards the transmitter is simulated, and by selecting the PLUS position, an aircraft speed of 800 knots away from the transmitter is simulated. With the VELOCITY CHECK switch set to the ZERO position, the resistor network R0.22, R0.38 and RV1 is introduced into circuit. The voltage on the wiper of RV1 is adjusted to approximately 3V and is applied to the crystal oscillator; this simulates a stationary aircraft.

**20.** When using the METER FUNCTION switch to measure the a.f.c., a.g.c or index store voltages on the receiver, the voltage reference network R0.21, MR0.6 together with RV1 and R0.50 is connected to the negative side of the test set meter. The voltage on the wiper of RV1 is adjusted to exactly 6V, therefore, providing the a.g.c., a.f.c. and index

store voltages in the receiver are correct, (i.e. giving 6V), then the test set meter will read zero. The oven protection circuit comprising RLA, RV4, R0.35 and R0.36 is identical in operation to the one fitted to the AR1.23180 receiver unit and the description of this is given in Pt. 2, Chap. 2, para. 28.

**Crystal oven circuit, board F**

**21.** The oven is heated by the power dissipated in the three resistors in the collector circuit of VT2, and by VT2; the power dissipated is controlled by the applied voltage at VT2 base. The oven controlling voltage is dependent upon oven temperature and is provided by the potential divider network R4/VT3 together with the temperature setting control RV2. VT3 is reverse biased and only the leakage current characteristic is used to control the oven temperature. While the oven is cold, the leakage through VT3 is at a minimum. This causes the potential at the base of VT6 (one of three transistors in a cascade emitter follower configuration) to go positive, which in turn causes the base of VT2 to go positive and therefore produce a high current condition in VT2. Because VT3 is heated by the oven, its leakage will be governed by the temperature of the oven. An increase in oven temperature causes an increase in VT3 leakage current, therefore VT3 resistance will be reduced, causing VT6 base voltage to fall. As the circuit is a cascade emitter follower, then VT4 emitter voltage will fall thus reducing the drive to VT2, and reducing the heat dissipation from the heater resistors. By adjusting RV2, the circuit will just maintain the oven heat losses at the required pre-determined temperature, this being 63°C.

**22.** The operation of the oven overheat sensing transistor VT1 is described in Pt. 2, Chap. 2, para. 28, and the operation of the crystal oscillator is described with board TJ circuit description, para. 14. The zener diode MR2 provides a stable voltage reference for the plus and minus velocity check.

**Encoder circuit, board T 5826-99-194-5223**

**23.** This circuit comprises three divide-by-two bistable circuits, the outputs of the first and second are gated together with $\pm\frac{1}{2}$ PRR and $\pm$ MTS to provide coding triggers. These trigger a bistable circuit which in turn control the encoding transistors VT14 and VT15 on board TC to provide the appropriate code on master or slave pulse groups. Details of the master and slave pulse groups transmitted by a Loran C station are given in Pt. 1, Chap. 1, Table 2. The circuit used to encode the simulated Loran C pulses is identical to board T in the receiver unit and the detailed description of it is given in Pt. 2, Chap. 2, para. 17 to 20.

**Master pedestal generator, board TM 5826-99-194-5221**

**24.** This circuit contains the first and second decades of the master pedestal generator. The circuit details are the same as those already described for board M of the receiver unit in Pt. 2, Chap. 2, para. 51 to 56 inclusive. Divergencies from these details are as follows:

(1) The 100 kc/s input signal is derived from the frequency dividers on board TJ.

(2) The Loran A full rate pedestal is produced by gating together MTS or ATS with the 100$\mu$S reset pulses from the master pedestal second decade. This gating is done by the resistor network R73/R74, and inversion is carried out by VT25. This 100$\mu$S signal output is applied to a three input 'and' gate together with a lmS reset pulse from the third decade and the first decade count of 5. An output occurring 50$\mu$S after the start of MTS and ATS is this produced which, after differentuation by C38/R79 is coupled to the base of the inverter stage VT26. During the receiver unit d.c. amplifier tests, with the test set SIGNAL SELECT switch set to AMP TEST + or −, on Loran C, an inhibit voltage is supplied to VT26 base circuit. Therefore, in the Loran A mode, a short negative-going differentiated pulse is produced, which is then used to trigger the 50$\mu$S monostable circuit VT1/VT2 on board TA that initiates the Loran A pulse.

(3) Smoothing has been incorporated in the base circuits of VT20 and VT23 to prevent these stages responding to the small pulses inherent in the diode decoding process.

**Master pedestal generator, board TN 5826-99-194-5222**

**25.** This board houses the third and fourth decades of the master pedestal generator together with the decoding and gating circuits for the basic rate selection. The operation of the circuits are basically the same as those already described in Pt. 2, Chap. 2, para. 57 to 60, any differences to the basic circuit are detailed below:

(1) To provide the ninth tracking gate pulse, or master recognition pulse as it is referred, a lmS pulse is decoded from the third decade of the master pedestal generator, board TN. This decoded pulse occurs 9mS after the start of MTS and is provided by the 'nand' gate MR128 to MR133. By decoding the fourth decade count of 0, as is done here, and gating it with the third decade count of 9, then only one lmS pulse will be decoded from this line per pulse repetition rate.

(2) The 8mS MTS (master time shared) pulse at pin 1 of board TN is produced by gating the output from VT12 together with the outputs from VT15, VT17, VT19 and VT20. This 8mS output pulse commences immediately after the decades have reset on reaching their selected pulse repetition rate, and it ceases when VT12 switches on and VT13 switches off after 8mS due to the normal bistable counting action of the circuit. (See Pt. 2, Chap. 2, para. 52, Table 2).

(3) In order to provide slave A and slave B time-shared pulses, 8mS pulses are decoded from the third decade of the pedestal generator

every 10mS. The decoded 8mS pulses are applied to MR126 and MR127. During these pulses, the diodes are reverse biased and the outputs at pins 4 and 5 of Board TN are dependent upon the position of the SLAVE SETTING switch S5, i.e. at the OFF position the 8mS pulses are grounded. At all other positions of S5 the 8mS pulses are grounded by the decoding diodes MR55 to MR96 until the basic and specific rates selected by S3 and S4 respectively have been reached by the pedestal generator bistable stages. During the first 10mS of the pedestal generating period, MTS is produced as mentioned in (2) above. Providing the SLAVE SETTING switch (S5) is set to position 1, then the ATS pulse will be produced 10mS later. This is produced by gating together the 8mS pulse from MR126 with the 10mS pulse on pin AS of Board TN, arriving at MTS plus 10mS. The BTS pulse is produced by gating together the 8mS pulse at MR127/MR134 with the 10mS pulse at pin AJ of Board TN, arriving at MTS plus 20mS. For each position of the SLAVE SETTING switch progressing in a clockwise direction, an additional 10mS is introduced between the MTS pulses and the ATS pulses, up to a maximum duration of 80mS. This controlled time difference is provided by gating the initial 8mS time sharing pulse from MR126 with the 10mS pulses occuring at pin AS or AJ to AH inclusive, depending upon the position of the SLAVE SETTING switch. BTS pulses occur at ATS + 10mS for all positions of the SLAVE SETTING switch S5, i.e. when ATS is gated with the pulses on pin AK of Board TN (MTS +30mS), then BTS will be gated with the pulses on pin AL (MTS +40mS).

**Note . . .**

*The positions at which the* SLAVE SETTING *switch can be used are determined by the 'basic rate' selected, see Pt.* 3, *Chap.* 2, *Table* 3.

(4) The MTS output together with the ATS and BTS outputs mentioned above are coupled to the plus and minus MTS, ATS and BTS generators on Board TJ in the Loran C mode of operation. When operating on Loran A mode, the BTS input to Board TJ is removed by the SIGNAL SELECT switch S7 as only master and one slave are required.

(5) Derivation of the full rate pedestal on this circuit is carried out in a slightly different manner to the method used on Board FN of the receiver unit. Instead of gating the count of 1 to 10 on the fourth decade of the master pedestal generator, as is done on Board M, the gating pulse is taken from the wiper of S3/1 or S3/2 via MR62 or MR66 depending on which specific rate has been selected. This modification is necessary owing to the inclusion of the SLAVE SETTING switch on the 10mS decoding lines, counts 2 to 10 to provide ATS and BTS. The function of the SPECIFIC switch wafer S4/2 is to provide +6V to either R59 or R60. This voltage which is coupled to R60 at the specific rate 0 position and R59 at specific rates 1 to 8, is normally grounded by the decoding diodes MR57 to MR96 via MR56 and S3/2 or MR59 and S3/1. Once the selected rate has been reached, the voltage at R59 or R60 depending on the SPECIFIC switch setting will be +6V for 10mS. This voltage will then be coupled via MR62 or MR66 to the threshold circuit MR78 and MR99 and then to VT23. This pulse provides one of the three inputs required for the generation of the full rate pedestal. The threshold circuit is introduced to prevent VT23 responding to the small pulses produced in the diode decoding of the basic rate. An example of this rate selection process is given in Pt. 2, Chap. 2, para. 59.

**Loran C pulse generator, board TC**

**26.** The circuitry on this board is associated with the production of Loran C pulses for the purpose of carrying out functional tests on the ARI.23180 installation. A monostable circuit controls the transistors that provide the appropriate rise and decay characteristics of the pulse envelope. An encoder circuit then applies the correct phase relation to the 100 kc/s signal within the pulse envelope to correspond to the phasing of a normal Loran C transmitted pulse group. After phase encoding the signal is passed through two tuned pulse forming stages to the emitter follower output circuit.

*Circuit description*

**27.** VT1 and VT2 act as a pulse limiting stage and is used to provide the ninth pulse on the master pulse group; the input to this stage is decoded from the pedestal generator, board TN. The master, slave A and slave B tracking gates, derived from board T, together with the ninth or 'master recognition' pulse from board TN are coupled to the pulse width monostable circuit comprising VT3 and VT4.

**28.** VT7 is a current generator, the function of which is to provide a standing current in one primary winding of T1 via MR5, VT6 and VT8; this standing current is controlled by the setting of RV2 in the base circuit of VT7. A super-regenerative oscillator, VT9, is incorporated in the primary circuit of T1, but it is not operational until the VT3/VT4 monostable circuit has been triggered. The winding of T1 which has the standing current passing through it also has a switched damping circuit across it comprising VT10 and RV4; the main function of this circuit is to control the rate at which the simulated Loran C pulses will decay.

**29.** The circuit functions in the following sequence: on receipt of a master, slave A or slave B tracking gate pulse from board T, and the ninth 'master recognition' pulses from board TN the monostable circuit VT3/VT4 changes state, i.e. VT3 on and VT4 off. In this condition, the emitter follower VT5 which was normally conducting is turned off, producing a negative 50$\mu$S pulse

at its emitter. This pulse is used to switch off VT6, thus eliminating the standing current in T1 primary, and is also used to switch off VT11, which in turn switches off VT10, removing the shunt from T1 primary. The sudden collapse of flux due to the cessation of T1 primary standing current, causes the transformer to ring; this initial flux collapse represents the start of the simulated Loran C pulse. The super-regenerative action of VT9 increases the amplitude of this oscillation in T1 at a rate determined by the setting of RV3 PULSE RISE CONTROL, and at a frequency determined by the tuning components C12/C22, this frequency being 100 kc/s. The output from the secondary of T1 is coupled to the decoding circuit via the Darlington pair emitter follower VT12 and VT13.

**30.** Approximately 50$\mu$S after the pulse rise, the monostable circuit reverts to its original state, i.e. VT3 off and VT4 on. VT3 in switching off switches on VT5 which provides a positive pulse to turn on VT11. The base potential of VT10 will go less positive due to the action of VT11, and VT10 will be turned on; this then introduces the decay control RV4 to the primary of T1 so that a controlled exponential pulse decay is obtained. Approximately 50$\mu$S after the monostable circuit resets, this timing being determined by the time constant R18 and C8, the base of VT6 will go positive causing VT6 to conduct and restore the standing current in the primary of T1 ready for the next pulse.

*Signal encoding*

**31.** The Darlington pair emitter follower VT12/VT13 couples the simulated Loran C pulse to the primary winding of T2. The secondary winding of this transformer is equally split and coupled to the collectors of the transistor switches VT14 and VT15. Either VT14 or VT15 will be conducting depending on the state of the encoder bistable circuit on board T. With VT14 conducting, pin 4 of T2 is effectively earthed, providing a phase inversion to the Loran C pulse envelope at the centre tap of T2; this state is termed negative code. Positive code pulses are produced by earthing the other side of T2 secondary, achieved by switching on VT15.

**32.** The first tuned pulse shaping stage, to which the centre tapped output of the encoder is connected, comprises VT16, VT17 and T3. VT16 is a common base stage with VT17 acting as the input to this stage. T3 in the collector load of VT16 is tuned by C20/C29 to 100 kc/s and, by adjustment of RV5, an adjustment is effected on the operating bandwidth of this tuned load. The output from the secondary winding of T3 is coupled to an identical stage comprising VT19, VT20 and T4. By adjusting the bandwidth of each of these two tuned stages with RV5 and RV8, and by adjusting the respective stage gains with RV6 or RV7, the Loran C pulse envelope can be formed so that it represents a true transmitted pulse. An emitter follower VT18 finally couples this pulse to the output of the test set.

**Loran A pulse generator, board TA 5826-99-194-5218**

**33.** The function of this board is to provide a Loran A master and slave pulse so that the Loran A operation of the receiver in the ARI.23180 installation can be verified. Also incorporated on this board is a metering circuit for standardizing the receiver oven temperature.

**34.** VT1 and VT2 forms a monostable circuit which, when triggered by the decoded master and slave full rate pedestal, provides a 50$\mu$S pulse. This square wave pulse is coupled to the pulse shaping tined circuit T1/C3·2 via VT3. The Loran A pulse is then produced by modulating the crystal frequency with the 50$\mu$S pulse. This is achieved by coupling the 50$\mu$S pulse to a circuit which is tuned to 1900 kc/s, and coupling VT5 to the other side of this tuned circuit. During the period that a pulse is present at C1, VT11 which was previously inhibiting the operation of VT5 is switched off, and VT5 is switched on and off at the oscillator frequency; the resultant signal at VT6 due to VT5 switching on and off will be the crystal frequency modulated by the 50$\mu$S pulse.

*Crystal oscillator*

**35.** The crystal oscillator is designed to operate at one of three frequencies depending on which Loran station is to be simulated by the test set: these frequencies are 1850 kc/s, 1950 kc/s and 1900 kc/s. One of the three crystals is introduced into the base circuit of VT4 by applying a positive bias, via positions A1, A2 or A3 of the SIGNAL SELECT switch, to MR4.9, MR4.5, or MR4.4 respectively. This positive bias causes the diode in series with the selected crystal to conduct, effectively connecting one end of that crystal to earth.

**36.** The operation of the oscillator is as follows: the crystal represents a series resonant circuit which, when at resonance, causes an r.f. current to flow through C4.4, C4.6 and C4.7. Because the reactance of C11 is low compared with the impedance of L2 at this frequency, C4.7 effectively becomes the emitter load to VT14. A portion of the crystal current is amplified and coupled from the emitter of VT4 to C4.7, where it is combined with the original crystal current to provide sufficient drive to maintain oscillation. The output from this oscillator stage is taken from the emitter of VT4 via C5.2 to the modulator switching transistor VT5 and to the collector of VT11, an inhibit transistor controlled by the state of the 50$\mu$S monostable circuit.

**37.** The Loran A pulse from the emitter follower VT6 is coupled to the 1900 kc/si.f. stage comprising VT8, VT9 and T2; VT8 is a common base connected stage and VT9 is used to inject the signal into VT8 emitter circuit. VT10, an emitter follower, then couples the signal to the switched output circuit. With Loran C selected on the SIGNAL SELECT switch, contact RLA1 changes over and connects the Loran C signal that is applied to pin 27 of this board to the test set attenuator

circuit. With Loran A selected, the signal at the emitter of VT10 is connected to the attenuator. A second output from VT10 emitter follower is coupled to socket 2 pin U via the 2:1 potential divider network R10.5/R10.6. This output provides a Loran A signal for testing the 1832 c.r.t. controller.

*Temperature probe circuit*

**38.** This circuit provides a means of measuring the ARI.23180 receiver oven temperature. The thermocouple probe is initially inserted into the test set oven and the TEMP control is adjusted to provide zero panel meter reading. As the test set oven is preset to run at 63°C ± 0·1° the probe circuit is then standardized at this temperature. On inserting the probe into the receiver oven it should then only be necessary to make slight adjustments to the receiver oven temperature control RV1 to obtain a zero test set meter reading.

**39.** VT12 and VT13 comprises a long-tailed pair voltmeter circuit where the meter is connected between the collectors of the two transistors. Provided the temperature of the oven into which the probe is inserted is correctly set, the base bias of VT13, controlled by the potential divider network R0.3, R0.2, RV3 TEMP control and the probe, will be the same as the voltage provided by the reference potential divider R12.3/R12.4; this results in a zero panel meter reading. The probe is a negative temperature coefficient thermocouple, therefore if the temperature of the oven under test is high, the resistance of the probe will reduce, thus reducing the base bias on VT13. This reduction in base bias causes VT13 collector voltage to increase giving a positive meter reading. Should the temperature of the oven under test be low, then the meter reading will be negative. Two meter sensitivity positions are provided for this test, these being coarse and fine (engraved 1 and 2 respectively). Initial calibration is carried out at position 1 and when satisfied that the meter reading is near zero, position 2 can be selected.

**Power supply circuit, board TY5826-99-194-5224**

**40.** The stabilized supply requirements for all the circuitry within the test set are provided by this board. Details of these are given in Pt. 2, Chap. 2, para.79 to 84, this being an identical set of stablizer circuits.

**Attenuator amplifier circuit, board L**

**41.** The circuit diagram of this amplifier is shown on the test set inter-connection diagram Fig. 10.53 Attenuator 2 in conjunction with R0.1 is a resistive divider providing up to 30dB signal attenuation; the input signal to this attenuator is the selected Loran A or Loran C signal from board TA. VT1 and VT2 forms a Darlington pair emitter follower, providing a low impedance output signal to the switched attenuator (ATTENUATOR 1). This 0 to 100dB attenuator provides a coarse adjustment to the output of the amplifier prior to coupling the signal to the output transformer T2. One of the two secondary windings of T2 is coupled via SK4 to the aerial amplfier unit and the other secondary winding is coupled via the normally open contacts RLA/1 and RLA/2 and PL1 to the receiver unit. At the 1831 '1' position of the POWER SOURCE switch RLA is energized and the test signal from T2 is connected via pins G and H of PL1 to the receiver unit. At the 1831 '2' position of this switch RLA is de-energized and the test signal is removed from pins G and H of PL1. The test signal will be present at SK4, therefore the ARI.23180 equipment can be tested as though signals were being received normally.

# Chapter 2

# FIRST LINE SERVICING

## LIST OF CONTENTS



## LIST OF TABLES



## LIST OF ASSOCIATED ILLUSTRATIONS

*Note:—These illustrations appear as fig. 67 in A.P.116B-0610-10*



### Introduction

**1.** The ARI.23180 (Decca Type ADL 21) comprises four units, these being the aerial amplifier Type 1953, the receiver unit Type 1831, the c.r.t. unit Type 1832 and the read-out unit Type 1833. By using the first line test set Type 1863, each of these units can be made to function as though under normal receiving conditions, thus enabling any faulty unit to be isolated. The procedure detailed in this chapter is directed to the quick localization of faults in the aircraft installation. Where the cause lies in the equipment, the checks described should give a positive indication of which unit is at fault; the unit should then be replaced to restore the installation to the serviceable state.

### Test Equipment

**2.** The first line test. Decca Loran Type 1863 Ref. 6625-99-107-1415 includes the following items:—

(1) Decca Type 53ABB Signal Test Lead 5826-99-195-8848

(2) Decca Type 53ABC Power Supply Lead 5826-99-195-8849

(3) Decca Type 53ABD 5 Mc/s Output Lead 5826-99-194-3331

(4) Decca Type 53ABE 21 foot Test Lead 5826-99-195-8850

(5) Decca Type 53ABW 1832 Test Lead 5826-99-195-8851

On each lead there is a sleeve which is marked with the relevant Decca type number.

Additional items that are supplied are a temperature test probe 6685-99-194-6576 and an 1831 receiver oscillator adjusting key Decca Type 53AAU, 5826-99-195-4837. Additional items that may be required are a multimeter set Type CT498A (5QP/1057049) for verifying test set meter readings where necessary, an external power supply capable of providing 115V at 400 c/s 500 mA single phase and 28V d.c. 200 mA for use during calibration of the test set, e.g. six-monthly check, and finally a Thermometer, Mercury Type 10AF/81 for initially setting and standardizing the test set oven. This standardizing test must be carried out at once monthly intervals.

**Caution . . .**

1. *A thermometer containing mercury must not be taken on an aircraft.*

2. *Front panel sockets not in use must have their protective cover fitted.*

### Voltage Checks

**3.** (1) Connect the test set connector 1 (61-pole connector) to the receiver test socket SKT8 (see Fig. 1) by means of the appropriate test lead (Decca Type 53ABE, forming part of the test set) and switch on the ARI.23180 by turning the OFF/DIM switch on the read-out

unit clockwise. Note that as the switch is turned clockwise the ARI.23180 panel lamp brightness increases.

(2) Set the POWER SOURCE switch to 1831 position 1 and ensure that the indicator lamp situated beneath the test set panel meter lights.

(3) Set the test set METER FUNCTION switch to 115 a.c. to measure the supply voltage. Ensure that the panel meter reads between 109V and 118V, the meter full scale voltage will be 160V when taking this measurement and the meter pointer will move to the left.

(4) Set the METER FUNCTION switch to 1863 and the VOLTS CHECK switch to +28 (green engraving), to measure the d.c. supply voltage. The meter should read within the limits 25.5V to 28.5V. If this voltage measurement is found to be near its limit, recheck the voltage using the CT498A multimeter connected to terminals 1 and 2 (positive to terminal 1 to measure positive voltage): the multimeter will read when the EXT. METER switch is pressed upwards.

(5) Set the VOLTS CHECK switch to each green engraved position in turn and note the panel meter readings.

| VOLTS CHECK *switch position (green engraving or dot)* | *Meter f.s.d.* | *Tolerance* |
|---|---|---|
| + 6 | 16V | ±0.8V |
| −12 | 16V | ±0.8V |
| +12 | 16V | ±0.8V |
| −26 | 32V | ±1.6V |
| +15 | 32V | ±1.6V |
| +26 | 32V | ±1.6V |

(6) Set the METER FUNCTION switch to 1831 and the VOLTS CHECK switch to each of the 12 positions in turn. The switch position together with the panel meter full scale reading is given below. (The meter moves right for positive and left for negative).

| VOLTS CHECK *switch position (white engraving)* | *Meter f.s.d.* | *Remarks* |
|---|---|---|
| −530 | 1600V | These voltages cannot be checked using the multimeter. |
| 1·9K | 8kV | |
| +6 | 16V | |
| −12 | 16V | |
| +12 | 16V | |
| −26 | 32V | |
| +15 | 32V | |
| −6·6 | 16V | |
| +6·6 | 16V | |
| +160 | 320V | These voltages cannot be checked using the multimeter. |
| −610 | 1600V | |
| +54 | 160V | |

A tolerance of ±15% is allowed for each of these voltages, but if any appear to be near their limits, check them using the CT498 multimeter connected to terminals 1 and 2. Switch off the ARI.23180 installation and remove the test lead.

**Standardizing the Test Set Oven**

**4.** Once monthly the test set oven must be referenced against an accurate thermometer: this must not be done in the aircraft. Referencing is carried out as follows:

(1) Connect the test set to an external supply having outputs of 28V at 200mA and 115V 400 c/s at 500mA. Connections should be made to the following pins of plug 7 on the test-set:—

| *Pin* | *Function* |
|---|---|
| A | 115V line |
| B | 115V neutral |
| C | 28V neutral and earth |
| E | 28V positive |

With these connections made, the test set POWER SOURCE switch must be set to EXT 1 and be left running for an hour to allow the oven temperature to stabilize.

**Note . . .**

1. *When setting the oven temperature, the ambient temperature must be between* 15 *to* 20°*C.*

2. *The test set power source may be supplied to plug* 1 *from an* 1831 *receiver unit if one is available, away from the aircraft.*

(2) Remove the knurled cap over the OVEN access hole in the front panel and insert the thermometer, mercury, Type 10AF/81 into the hole. After the equipment has been on for 1 hour, note the temperature and if necessary, make adjustments to the TEMP control until a temperature of 63°C ± 0.1 °C is obtained. After any adjustment to the oven TEMP control allow a further 10 minutes before reading the temperature. Now that the test set oven is standardized, the ARI.23180 oven temperature can be verified.

**Checking the ARI.23180 oven temperature**

**5.** Connect the test set plug 1 to the receiver unit (1831) test socket SK8 by means of the 61-way cable Decca Type 53ABE, and switch on the ARI.23180 by turning the read-out unit OFF/DIM

switch clockwise. Set the test set POWER SOURCE switch to 1831 position 1; the test set is now on. Temperature checking can be carried out as follows:—

(1) Set the test set METER FUNCTION switch to TEMP. Connect the probe to connector 8 of the test set and insert the probe into the hole marked OVEN on the front panel. 40 minutes must then be allowed for the oven temperature to stabilize.

(2) Set the COMPARATOR switch to position 1 (coarse zero setting) and adjust the ZERO control to obtain a zero reading on the panel meter (centre scale).

(3) Set the COMPARATOR switch to position 2 (fine zero setting) and re-zero the meter using the ZERO control; the test set meter is now calibrated at the correct oven temperature.

(4) Transfer the probe from the test set oven to the 1831 receiver oven recess marked THERM and after 15 minutes note the meter reading. The meter should read zero $\pm 5$ divisions: a reading outside this limit indicates that the oven temperatures has been incorrectly set. When the receiver oven has been on for one hour, the test set meter should read within $\pm 2$ divisions.

(5) If the above tolerances are not achieved after the full warming-up period, insert the screwdriver end of the tool provided into RV1 on the receiver unit and turn the control clockwise to reduce the temperature of the oven, or counter-clockwise to increase it. After each small adjustment, 10 minutes must be allowed for the oven temperature to stabilize. When the test set meter reads zero, the oven is correctly set.

**Operational fault reports**

**6.** The symptoms observed during first line checks in many instances give a guide to the nature of the fault: these symptoms may subsequently be of considerable assistance when a detailed bench check is made on the rejected unit(s). Faulty operation of the ARI.23180 installation may be evident during a ground check, when the appropriate fault checks in Table 1 may be applied, or during operation in flight. In this second case, the following details should, if possible, be obtained:—

(1) Nature of fault or reported failure.

(2) Mode of operation and pulse repetition rate, and if on Loran A operation—frequency selected.

(3) Time of failure(s) if on master or just one slave only.

(4) Duration of failure(s) if intermittent.

From these conditions it is possible to assess the probability of an external cause of failure, such as transmission breakdown or interference with reception by abnormal electrical noise conditions. The serviceability of the suspect transmitting station for the period(s) of the fault should be checked.

**Initial checks**

**7.** When available information on the fault has been obtained, the installation should be checked with the test set in accordance with the procedure laid down in para. 21 and 22 to 26 inclusive. Operation of the installation should be checked both on Loran C and Loran A.

**8.** Where no fault condition can be found to exist in the installation, despite an operational defect report, any decision on the replacement of units must be made on:—

(1) The adequacy and reliability of the initial defect report.

(2) The nature of the reported failure.

(3) The possibility of aircraft-generated noise.

(4) The possibility of abnormal reception conditions (e.g. electrical storm, exceptionally high static level): this may be confirmed by checks for any simultaneous failure reported on other radio equipment.

**9.** The following procedure has the primary object of locating the faulty unit in order that a serviceable replacement may be fitted. Only in the case of an installation fault (i.e. socket or cable connection fault) is it intended that an in situ repair should be made. Installation inter-connecting data against which cable connections may be checked are shown in Pt. 1, Chap. 3, Tables 2 to 10 inclusive. To identify the precise nature of the fault, test set checks should be made. To assist in later unit servicing, the findings should be recorded on the unserviceability report of the faulty unit when it is returned for repair.

**10.** Para. 21 to 26 details test set readings and display behaviour to be expected on a normal serviceable receiver, and para. 17 to 20 inclusive details the method by which one unit of the installation can be isolated from another. In order to pinpoint a faulty unit, the fault check table is written in the same order in which functional tests are carried out (para. 21 to 24). If a fault is apparent during these functional tests, compare the symptom with those listed in Table 1; against this symptom the fault action is given.

**11.** To effect fault diagnosis the test set is capable of providing signals of the shape, repetition rate and signal strength to simulate Loran A and Loran C transmissions. During testing, the test set is powered by the internal supplies of the ARI.23180, therefore connector 1 must be connected to the 1831 receiver unit plug 1. (Fig. 1).

**Preliminary adjustments, (Loran C)**

**12.** For the purpose of first line testing, rate SH1 is specified, i.e. position SH on the BASIC switch and position 1 on the SPECIFIC switch. In areas where transmissions from rate SH1 stations may be received, test set checks should be made at some other rate which is not locally received (subject to the limitations of Table 3).

**13.** With the test set POWER SOURCE switch set to position 1, the test set simulated signals will be coupled via pins G and H of connector 1 and via the receiver unit to the test stud on the aerial. Under these conditions the ARI.23180 equipment can be operated as though a signal is being normally received.

**14.** Set the controls as follows:—

(1) Test Set

| *Control* | *Position* |
|---|---|
| SIGNAL SELECT | C |
| BASIC RATE | SH |
| SPECIFIC RATE | 1 |
| SLAVE SETTING | See Table 3 |
| CODING | BELLY OR DORSAL (for ventral or dorsal as appropriate). |
| VELOCITY CHECK | ZERO |
| ATTENUATOR 1 | Set for signal level of 5$\mu$V at aerial amplifier. (See Table 2). |

**Note . . .**

*The attenuator readings must be added to give the total attenuation in dB.*

(2) Read-out Unit

| *Control* | *Position* |
|---|---|
| LEFT-HAND SELECT STATION | C WIDE |
| CENTRE SELECT STATION | SH |
| RIGHT-HAND SELECT STATION | 1 |

(3) CRT Unit

| *Control* | *Position* |
|---|---|
| FUNCTION | M |
| TIMEBASE | 1 |
| KC | Fully clockwise |

**15.** Adjust the R.F. CONTROLS LORAN C and DISPLAY GAIN (c.r.t. unit) switch until the r.f. pulses are present on the c.r.t. unit at an amplitude of approximately 1 cm. Ensure that the general appearance of the c.r.t. trace is normal (width, noise, etc.) and that it is clearly visible. Set the c.r.t. unit TIMEBASE switch to position 2 and ensure that the trace is clearly visible, then return the switch to position 1.

**16.** Proceed to lock-in the simulated signal with the tracking gates as follows:—

(1) With the c.r.t. unit function switch set to M, A and B in turn, operate the COARSE tracking switch until the tracking gates are separated from each other and from the signal pulses. Reset the function switch to M.

(2) Operate the COARSE and MEDIUM tracking switches to align the first eight of the nine master r.f. pulses with the eight tracking gates at the beginning (left-hand edge) of the timebase.

(3) Set the TIMEBASE switch to 2 and align the master r.f. pulses with the gates using the MEDIUM tracking switch.

(4) Set the TIMEBASE switch to 3 and observe a single pulse and gate. Align the gate on the index (third) cycle of the pulse, using the 10$\mu$S JUMP switch. If the pulse has the appearance of two interlaced signals, operate the CODE JUMP switch once and the pulse should revert to normal appearance.

(5) Repeat operations (2) and (4) for the two slave channels (FUNCTION switch to A and B in turn). Remember that the slave signals have only eight pulses instead of the nine for master. Reset the FUNCTION switch to M.

(6) Set the r.f. gain control LORAN C to maximum (fully clockwise).

(7) Set the AGC/INDEX/AFC switch to INDEX and check the meter deflection. If the index cycle has been correctly selected, the meter should indicate zero $\pm 2$ divisions. If the cycle before the index cycle has been selected, the pointer will drift to the left or if the cycle after the indexing cycle is selected, the pointer will drift to the right.

(8) Operate the 10$\mu$S JUMP switch to left and/or right and check that INDEX ALARM lamp (Read-out Unit) is on when second or fourth cycles are selected. Operate the 10$\mu$S JUMP switch to select the third cycle, using the STORE ZERO switch as necessary.

**Note . . .**

*The* ALARM *lamp should be out and the c.r.t. unit meter pointer should read zero* $\pm 2$ *divisions.*

(9) Set the FUNCTION switch to A and B in turn and repeat sub-para. (7) and (8). Check the time differences indicated on the Read-out Unit (Table 3).

**17.** If there are no signals on the c.r.t. display, proceed to locate the fault as follows:—

(1) Set the test set POWER SOURCE switch to 1831 position 2, to disconnect the signal from pins G and H of connector 1.

(2) Remove SKT6 on the receiver unit (1831) and in its place connect the signal lead from socket 4 of the test set, see Fig. 2. Set the attenuators to 100dB. If the signals appear on the c.r.t. unit the fault is in the aerial amplifier. If there is still no signal, the fault may be either in the 1831 receiver unit or in the 1832 c.r.t. unit. To prove which unit is faulty it is necessary to run the c.r.t. unit from the test set signals.

(3) Remove the test signal cable from the receiver SKT6. Remove the plug from SKT1 of the receiver unit and couple it to the lead from socket 2 on the test set (see Fig. 3). Appropriate 'scope triggers, tracking gates and signals are generated so that, if the c.r.t. unit is working, the signals will appear on the c.r.t.

(4) The high voltage supplied to the c.r.t. unit comes directly from the receiver unit. Therefore if the voltage checks given in para. 3(5) are correct, then it is assumed that the c.r.t. unit is faulty if no display is obtained.

(5) If on replacing the c.r.t. unit there is still no display, the fault will most probably be in the interconnecting cable.

**18.** With the receiver unit set to the same pulse repetition rate as that produced by the test set, the c.r.t. signals displayed should be stationary. If the signals are not stationary, another pair of rates must be selected, and if the fault is still apparent, then the receiver unit must be faulty. If the fault is on one rate only, then it is likely to be in the read-out unit. A read-out unit indicator lamp having apparently failed can be checked by first changing the read-out unit to see if the number lights up. If it does, the read-out unit is at fault, but if the indicator lamp does not light, the fault is in the receiver unit or the interconnecting cables.

**19.** To isolate a faulty indicator in the read-out unit, two indicators can be interchanged. This is done by pressing in two adjacent indicators together and then releasing them; the units can then be withdrawn from the front of the read-out unit. Interchange the two indicators and press them into the read-out unit until they lock in position. If the fault still occurs on the indicator that was previously faulty then it must be replaced.

**20.** If the fault has not yet been discovered, carry out a complete functional test, first for Loran C operation as laid down in para. 16 to 21 inclusive. If a fault is apparent, note the symptom and study the Fault Check Table (Table 1) to ascertain the cause.

**Loran C functional tests**

**21.** For the Loran C functional tests proceed as follows:—

(1) Check that the control positions are set as listed in para 14(1), (2) and (3).

(2) AGC checks:

(a) Set the AGC/INDEX/AFC switch (c.r.t. unit) to A.G.C. Set the FUNCTION switch to M, A and B in turn and check that the meter on the c.r.t. unit indicates $-7 \pm 4$ divisions to the left.

(b) Increase the test set r.f. output to $-67$ + aerial capacity dB (Table 2) and check that the a.g.c. readings for M, A and B are $-4 \pm 4$ divisions on the c.r.t. unit meter.

(c) Increase the test set r.f. output to $-55$ + aerial capacity dB (Table 2) and check that the a.g.c. readings for M, A and B are $0 \pm 4$ divisions.

(d) Return signal level to $-87$ + aerial capacity dB.

(3) Set the FUNCTION switch to M and operate the tracking 10$\mu$S JUMP switch to jump the gates out of the pulse. Set the AGC/INDEX/AFC switch to AGC and check that the meter pointer is fully left and that the AGC ALARM lamp is on. Set the AGC/INDEX/AFC switch to INDEX and check that the meter indicates zero $\pm 4$ divisions. Return the gate to the index cycle using the tracking the MEDIUM and 10$\mu$S JUMP switches.

(4) Repeat (3) with the FUNCTION switch set to A and B.

(5) Set the FUNCTION switch to M and set the AGC/INDEX/AFC switch successively to INDEX and AFC. Check that in both positions of this switch, the meter indicates zero $\pm 4$ divisions. When checking the INDEX set the test set METER FUNCTION switch to INDEX A and check that the test set meter indicates zero $\pm 4$ divisions.

(6) Repeat (5) with the FUNCTION switch set to A and B in turn.

(7) Set the STORE ZERO/CODE JUMP switch to STORE ZERO and repeat checks (5) and (6). Check that with the AGC/INDEX/AFC switch set to AGC, the meter (on the c.r.t. unit) indicates between 14 and 17 divisions to the left.

(8) Check that the r.f. gain control LORAN C is still set to maximum and that the gates are still on the index cycle. With the FUNCTION switch set to M, A and B in turn, set the STORE ZERO/CODE JUMP switch momentarily to CODE JUMP and check that the c.r.t. displays interlaced signals. Again, select CODE JUMP momentarily and check that the c.r.t. display returns to normal.

(9) Set the AGC/INDEX/AFC switch to AFC and set the FUNCTION switch to M. Set the METER FUNCTION switch (test set) to AFC M and check that the test set meter indicates zero $\pm 4$ divisions.

(10) Repeat (9) with the FUNCTION switch set to A and B and the test set METER FUNCTION switch to AFC A and AFC B in turn.

(11) Check that the DISPLAY GAIN control varies the amplitude of the c.r.t. display. Restore the DISPLAY GAIN control to its former position (fully clockwise).

(12) Rotate the notch filter control (RF CONTROLS-KC) and note that this has an effect on the latter part of the displayed pulse shape. Restore the notch control to fully clockwise position.

(13) Press the ALL JUMP switch to the left and check that tracking is now on one cycle after the index cycle. Pause for 30 seconds and check that the displayed read-out is unchanged. Press the ALL JUMP switch to right, pause for at least two seconds and press it right again and check that tracking is on one cycle before the index cycle. After a further 30 seconds, check that the displayed read-out is unchanged. Press the ALL JUMP switch to the left to return to the index cycle.

(14) Set the left-hand SELECT STATION switch (Read-out Unit) to C NARROW and ensure that the signal is still present (smaller and shifted to the right). Return to C WIDE.

(15) Velocity check:

(a) Set the test set VELOCITY CHECK switch to MINUS. At the c.r.t. unit, set the FUNCTION switch to M and the AGC/INDEX/AFC switch to AFC. After one minute,

check that c.r.t. unit meter indicates between 7 and 15 divisions right.

(b) Repeat (a) with the c.r.t. unit FUNCTION switch to A and B in turn (the one minute delay is not required here).

(c) Return the test set VELOCITY CHECK switch to ZERO and allow one minute for the test set to recover. Check that the receiver is still on index cycle.

(d) Set the VELOCITY CHECK switch to PLUS and repeat (a) and (b): the c.r.t. unit meter should indicate between 7 and 15 divisions to the left.

(e) Return the VELOCITY CHECK switch to ZERO.

(16) Set the read-out unit centre SELECT STATION switch to SS and the right-hand switch to 0 (no adjustments to the test set are required here). To check the lights for all numbers of each digit of the read-out display proceed as follows:

(a) To check 10,000$\mu$S digits depress and hold the COARSE SLEW switch.

(b) To check the 1000$\mu$S digits momentarily depress the COARSE SLEW switch to display each digit.

(c) To check the 100$\mu$S digits momentarily depress the MEDIUM SLEW switch to display each digit.

(d) To check the 10$\mu$S digits operate the 10$\mu$S JUMP switch to display each digit.

(e) The 1$\mu$S digit is tested by setting the LH SELECT STATION switch to position 3, centre SELECT STATION switch to S and off-setting the LORAN A DRIFT control slightly.

**Loran A, Functional Tests**

**22.** For the purpose of first line testing using Loran A signals, rate IL2 is specified. In areas where transmissions from rate IL2 stations may be received, test set checks should be made at some other rate which is not locally received (subject to the limitations in Table 4).

**23.** Remove connector 6 from the receiver SKT6 and connect the test lead Decca Type 53ABB between the test set SK4 and the receiver SK6. The test lead that was connected between the receiver SK8 and the test set SK1 on Loran C tests must remain connected for Loran A tests.

**24.** Set the controls as follows:

(1) Tests Set

| *Control* | *Position* |
|---|---|
| POWER SOURCE | 1831/2 |
| SIGNAL SELECT | A1 |
| BASIC RATE | L |
| SPECIFIC RATE | 2 |
| SLAVE SETTING | 1 (see Table 4) |
| CODING | BELLY or DORSAL as appropriate |
| VELOCITY CHECK | ZERO |
| ATTENUATOR 1 | −80dB |
| ATTENUATOR 2 | −14dB |

(2) Read-out Unit

| *Control* | Position |
|---|---|
| Left-hand SELECT STATION | 1 |
| Centre SELECT STATION | L |
| Right-hand SELECT STATION | 2 |
| A, A/B, B | A |

(3) C.R.T. Unit

| *Control* | *Position* |
|---|---|
| FUNCTION | M |
| TIMEBASE | 1 |
| RF CONTROLS, LORAN A | As necessary to obtain a clear picture. |

(4) Operate the tracking COARSE and MEDIUM switches so that one pulse is obtained on each trace on the c.r.t. with the bottom pulse to the right of the top pulse.

(5) Operate the tracking COARSE or MEDIUM switch to slew the top pulse to the left edge of the timebase, on to the pedestal.

(6) Set the FUNCTION switch to A and operate the tracking COARSE or MEDIUM switch to slew the lower pedestal under the lower pulse.

(7) Set the TIMEBASE switch to 2 and operate the tracking MEDIUM switch to slew M and A in turn (FUNCTION switch to M and A) until both are positioned left on the pedestals.

(8) Set the TIMEBASE switch to 3 and operate the 10$\mu$S JUMP switch and/or LORAN A SLEW switch to drift the master and slave pulses into precise alignment. It is necessary to adjust the RF CONTROLS, LORAN A so that both pulses are of the same amplitude.

(9) Note the displayed time difference (see Table 4).

**Note . . .**

*If the signals drift steadily to the right or left on the c.r.t. display, adjust the* LORAN A DRIFT *controls to eliminate this effect. The larger knob controls the slave oscillator and the smaller knob controls the master oscillator.*

**25.** Ensure that the appearance of the c.r.t. unit traces are normal (width, brightness, etc.) and that all parts of the setting-up procedure detailed in para. 24. above can be performed satisfactorily. If a fault seems to be apparent, note the fault and study the Fault Check Table to ascertain the cause.

**26.** Ensure that the displayed time difference read-out corresponds with that selected on the test set (Table 4). Select 2L2 on the read-out unit SELECT STATION switches and A2L2 on the test set; the receiver should remain correctly tuned and the read-out unit should indicate the same time-difference. Select 3L2 on the read-out unit and A3L2 on the test set; the read-out reading should remain unchanged.

## TABLE 1

### Fault check table for first line servicing

This table covers faults arising during Loran C or Loran A functional tests given in para. 21 to para. 24 inclusive.

| Fault indication | Action |
|---|---|
| No panel illumination on any unit when switching on. | (1) Check FS3 on the receiver unit.<br>(2) Measure the 28V d.c. supply using the test set. If there is no reading, the fault is probably due to a faulty cable connection. If 28V is indicated on the test set, then the fault is in the read-out unit. |
| No panel illumination on just one unit when switching on. | (1) Check the lamps on that unit.<br>(2) Carry out cable continuity test and check earth bonding.<br>(3) If the fault is not yet discovered, replace the unit that has the fault. |
| No reading on any read-out unit digit. | (1) Check FS1 and FS2 on the receiver unit.<br>(2) Check the +15V supply using the test set. If the supply is present, then the fault is either in the read-out unit or in the supply cable to the read-out. If there is no supply present, the fault is in the receiver unit. |
| No reading on one indicator of the read-out unit. | (1) This would most likely be caused by a fault in the read-out unit, therefore it should be changed.<br>(2) If the fault still persists, change the receiver unit. |
| Failure of any number to come up on any indicator of the read-out unit. | Interchange the suspect indicator with its adjacent one. If the fault has moved with the unit then one of the lamps in the unit has blown. If the fault is in the same position as before it is caused by:—<br>(a) A faulty cable connection.<br>(b) A fault in the receiver unit control circuitry.<br>(c) A fault in the read-out unit. |
| No c.r.t. unit displayed trace. | (1) Check the fuses.<br>(2) Measure the voltage using the test set.<br>(3) Couple the test set signal directly to the receiver unit to eliminate a possibly faulty aerial amplifier, see para. 17(1) & (2).<br>(4) Couple the test set signal directly to the c.r.t. unit as described in para. 17(3) & (4). If the display is satisfactory then the fault lies in the receiver unit or the interconnecting cables. If there is still no display, then the fault is probably in the c.r.t. unit. |
| Correct pulse repetition rates cannot be acquired. | (1) Carry out cable continuity tests.<br>(2) If the fault still persists it must either be in the read-out unit switching circuitry or in the receiver unit. |
| Incorrect meter reading on initial a.g.c. checks, see para. 21(2) sub. paras. (a), (b) and (c). | (1) Connect the test set signal directly to the receiver unit as described in para. 17(1) & (2) to eliminate a possible faulty aerial amplifier.<br>(2) If the fault still persists, then the c.r.t. unit is less likely to be the cause of the trouble than the receiver unit. |
| 10$\mu$S and MEDIUM TRACKING switches have no effect when acquiring signals, see para. 21(3). | (1) Set the test set METER FUNCTION switch to 1832 and check that there is a test set meter deflection on operation of each of the tracking switches. If there is not, change the c.r.t. unit.<br>(2) Carry out a cable continuity test.<br>(3) If the fault still persists then it must be in the receiver unit. |

**TABLE 1** (*cont.*)

| Fault Indication | Action |
|---|---|
| Impossible to lock the M, A or B pulses when acquiring signals, see para. 21(3) and (4). | Replace the receiver unit. |
| Incorrect meter readings when checking the AGC, AFC and INDEX stores after locking the signals. See para. 21(5), (6), (7), (9) and (10). | With the test set connected to the receiver, measure the store voltages by setting the METER FUNCTION switch to the AGC, INDEX and AFC positions in turn. If all readings are zero $\pm 4$ divisions then the c.r.t. unit is at fault. If just one or two readings are faulty then the receiver unit is faulty. |
| CODE JUMP switch has no effect when observing the display. See para. 21(8). | Set the test meter function switch to 1832 and operate the code jump switch. If a meter deflection is obtained on the test set, then the fault is in the interconnecting cable or the receiver unit. If there is no test set meter deflection, then the c.r.t. unit is faulty. |
| Display gain control has no effect. See para. 21(11). | Simulate the receiver unit by connecting the test set signals directly to the c.r.t. unit (see para. 17) via connector No. 2. If the DISPLAY GAIN control still has no effect, then the c.r.t. unit is faulty. |
| RF CONTROL KC has no effect when observing the Loran C pulse envelope. See para. 21(12). | Connect the test set signals directly to the c.r.t. unit. If the RF CONTROL KC still does not function, then the fault is in the c.r.t. unit. If this control does function when directly coupled to the test set then the fault is in the $-24$V supply circuit in the receiver unit or in the interconnecting cables. |
| Incorrect functioning of ALL JUMP switch. See para. 21(13). | With the test set connected to the c.r.t. unit via connector 2 as detailed in para. 17, set the METER FUNCTION switch to 1832. The ALL JUMP switch is working satisfactorily if, on operation of the switch to the right and left position, full scale deflection on the test set meter is obtained. If the switch is found to be satisfactory then the fault will lie in either the interconnecting cable or the receiver unit. |
| Displayed read-out changes after operation of ALL JUMP switch. | Replace the receiver unit. |
| Signal remains unchanged or disappears when checking the bandwidth. See para. 21(14). | (1) If the signal is unchanged, the relay on board X is probably not operating, therefore check the interconnecting cable and, if the fault is still not cured, replace the receiver unit.<br>(2) In the event of the fault still persisting then it must be in the read-out switching. Change the read-out unit.<br>(3) If the signal disappears then the fault is most probably in board X of the receiver unit. |
| Incorrect meter readings when carrying out the velocity check. See para. 21(15). | A faulty meter on the c.r.t. unit would have been ruled out on a previous check, therefore the fault will probably be in either the interconnecting cables or the receiver unit. |
| Malfunction of any TRACKING switch other than SLEW and CODE JUMP when checking the read-out unit lamps. See para. 21(6). | With the test set coupled directly to the c.r.t. unit by connector 2 as detailed in para. 17, and with the test set METER FUNCTION switch set to 1832, operate each tracking switch in turn. For each operation of a switch, a test set meter deflection should be obtained. If all switches are satisfactory, then the interconnecting cable or the receiver unit is at fault. |
| No pulses presented on c.r.t. unit when acquiring Loran A signals. See para. 24(4). | Couple the test set directly to the c.r.t. unit with connector 2; with the test set controls adjusted as detailed in para. 17, the Loran A pulse envelope should be presented on the c.r.t. unit. If there is still no signal available when using the test set, then the fault is in the interconnecting cable or the receiver unit. |

**TABLE 1** (*cont.*)

| Fault Indication | Action |
|---|---|
| No pedestal available. See para. 24(5). | Check the interconnecting cables and if the fault still persists then replace the receiver unit. |
| No double trace on c.r.t. unit. | Couple the c.r.t. unit to the test set as detailed in para. 17. If there is still no double trace, replace the c.r.t. unit, If the double trace appears on connecting the test set, then the fault is either in the interconnecting cable or in the receiver unit. |
| Trace on c.r.t. unit not central or still double at timebase position 2. See para. 24(7). | Check the c.r.t. unit using the test set as detailed in para. 17. If c.r.t. functions satisfactorily on the test set, then the fault is in the interconnecting cable or the receiver unit. |
| RF CONTROLS LORAN A have no effect when setting amplitude of Loran A pulse. See para. 24(8). | Couple the test set directly to the c.r.t. unit as detailed in para. 17. If the LORAN A controls still have no effect, replace the c.r.t. unit. If the controls function satisfactorily then the fault is in either the interconnecting cable or the receiver unit. |
| Drift cannot be corrected with LORAN A DRIFT control. See para. 24(9). | (1) Ensure that the SIGNAL SELECT, BASIC RATE, SPECIFIC RATE and SLAVE SETTING switches are correctly set.<br>(2) Observe the reading on the read-out unit before and after adjustment of the LORAN A DRIFT control. If there is no change then the fault is either on the c.r.t. unit DRIFT control or the interconnecting cables. If the read-out reading changes, then the fault is probably in the receiver unit oscillator circuit. |

**TABLE 2**
**dB equivalent of aerial capacity**
(For test set attenuator settings)

| Aerial Capacity (pF) | dB Equivalent |
|---|---|
| 16 | 17 |
| 20 | 18·5 |
| 25 | 20 |
| 32 | 22·5 |
| 40 | 24 |
| 50 | 25·5 |
| 63 | 27·5 |
| 79 | 29·5 |
| 100 | 31·5 |
| 126 | 33 |
| 158 | 35 |
| 199 | 37·5 |
| 251 | 39·5 |
| 316 | 41·5 |

**Notes . . .**

(1) *The output from the test set is injected into the aircraft aerial via the following route:— Test Set SKT1—Test set connector—Receiver SKT8—Receiver SKT5—Connector No. 5—Aerial Amplifier PL1—Aerial Amplifier SKT4—Connector No. 11—2·7pF capacitor—Aerial.*

(2) *To inject a signal of known level at the aerial it is necessary to know the aerial capacity and, from Table 2, an equivalent figure in dB is obtained.*

(3) *The signal level required for first line testing is 5μV at the aerial amplifier input. The required attenuator setting to achieve this is calculated by means of the formula:*

$$-87 + dB \text{ equivalent of aerial capacity.}$$

*Thus if the aerial capacity of the aerial under test is 63pF the equivalent dB figure (from the table) is 27·5 and the required attenuator setting is −87+27·5 or −59·5dB. In this case, test set* ATTENUATOR 1 *is set to −40dB and* ATTENUATOR 2 *(continuously variable from 0 to −30dB) is set to −19·5dB.*

## TABLE 3

**Rate settings and displayed read-out, Loran C**
(For checks using 1st line test set)

| SLAVE SETTING (Test Set) | BASIC RATE Test Set and Read-out Unit | READ-OUT (in $\mu$S) A | B |
|---|---|---|---|
| 1 | H, L, S, SH, SL, SS | 10000 | 20000 |
| 2 | L, S, SH, SL, SS | 20000 | 30000 |
| 3 | S, SH, SL, SS | 30000 | 40000 |
| 4 | SH, SL, SS | 40000 | 50000 |
| 5 | SL, SS | 50000 | 60000 |
| 6 | SL, SS | 60000 | 70000 |
| 7 | SS | 70000 | 80000 |
| 8 | SS | 80000 | 90000 |

**Notes . . .**

(1) SPECIFIC *rate switch has no effect on read-out when using the 1st line test set for Loran C checks.*

(2) *Combinations of* SLAVE SETTING *and* BASIC RATE, *other than those listed, will not give a satisfactory read-out.*

## TABLE 4

**Rate settings and displayed read-out, Loran A**
(For checks using 1st line test set)

| *Test Set* SLAVE SETTING | BASIC RATE | *Test Set and Read-out Unit* SPECIFIC RATE (Read-out in $\mu$S) 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | H | 5000 | 4950 | 4900 | 4850 | 4800 | 4750 | 4700 | 4650 |
| 1 | L | 10000 | 9950 | 9900 | 9850 | 9800 | 9750 | 9700 | 9650 |
| 1 | S | 15000 | 14950 | 14900 | 14850 | 14800 | 14750 | 14700 | 14650 |
| 2 | S | 5000 | 4950 | 4900 | 4850 | 4800 | 4750 | 4700 | 4650 |
| 3 | S | 5000 | 5050 | 5100 | 5150 | 5200 | 5250 | 5300 | 5350 |

**Note . . .**

*Combinations of* SLAVE SETTING, BASIC RATE *and* SPECIFIC RATE, *other than those listed, will not give a satisfactory read-out.*

# Chapter 5

# SECOND LINE SERVICING: INDICATOR, LORAN (DECCA CRT CONTROLLER TYPE 1832)

## LIST OF CONTENTS



## LIST OF TABLES



## LIST OF ASSOCIATED ILLUSTRATIONS

(to be found in A.P.116B-0610-1



## GENERAL INFORMATION

**1.** The procedure detailed in this chapter is directed to the diagnosis and, where possible, the repair of faults in the C.R.T. Controller of the Loran ARI.23180 installation. Faulty operation of a C.R.T. Controller may become apparent during a ground check or during operation in flight. In the latter case the following details should be obtained: —

(1) Nature of fault or reported failure.

(2) Duration of failure(s) if intermittent.

(3) Mode of operation at which the fault was evident.

**2.** Reference to any available information on the nature of the operational failure will assist in the quick location of the fault. Where such information indicates that the fault is of an intermittent nature, a prolonged run of the unit may be necessary to enable the fault to be repeated. In some instances, failure may not recur until the equipment has stabilized at full operating temperature.

**3.** When no fault condition can be found in the unit, despite an operational defect report, a decision on the serviceability of the unit must be made on the following considerations:—

(1) The adequacy and reliability of the initial defect report.

(2) The nature of the reported failure.

(3) The likelihood of a cable fault in the installation.

(4) The possibility of a supply failure.

### Test equipment

**4.** The following items of test equipment are required to carry out the functional checks on the C.R.T. Controller of the Loran ARI.23180.

(1) Oscilloscope set (CT536) 10S/6625-99-952-2040 or Hewlett Packard oscilloscope Type 108A 10S/6625-99-194-9182.

(2) Multimeter set (CT498A) 5QP/1057049.

(3) Wrench, hexagon (Allen) 0·050 in. across flats 10AG/5826-99-195-4837.

(4) Power supply unit 10K/9561998.

(5) Receiver Loran Type 1831, 10D/5826-99-955-8336 (part of bench rig).

(6) Indicator digital Type 1833, 5826-99-955-8338 (part of bench rig).

(7) Aerial amplifier unit Type 1953, 10U/5826-99-955-8339 (part of bench rig).

(8) Test set, Loran Type 1863 10S/6625-99-107-1415 together with the following cable assemblies: Decca Type 53ABC 5826-99-195-8849, Decca Type 53ABD 5826-99-194-3331 and Decca Type 53ABE 5826-99-195-8850.

(9) Extension electronic circuit panels:
Decca Type 1864G 10AD/5826-99-195-0495 (for board VA).
Decca Type 1864H 10AD/5826-99-195-0498 (for board VB).
Decca Type 1864L 10AD/5826-99-195-0501 (for board VC).
Decca Type 1864M 10AD/5826-99-195-0499 (for board VE).

(10) C.R.T. test graticule.

**Procedure**

**5.** The second line check and fault location procedure comprises a mechanical inspection of the C.R.T. controller followed upon satisfactory completion, by a functional test routine. If the unit passes satisfactorily through these checks it may be assumed serviceable.

**6.** Unless a unit has a self-evident fault, it should be subjected to the complete test procedure. Where a fault indication is obtained, its sympton should be compared with those given in the fault check table (Table 2) and the appropriate action should be taken. Where the fault is caused by only a partial failure, it is best found by using an oscilloscope in conjunction with the signal flow block diagram fig. 10.66. A complete check of the unit should be made when the fault has been rectified.

**7.** Most faults in the C.R.T. controller will necessitate the replacement of a faulty sub-assembly. Servicing procedure should however include the overall cleaning of the unit, specifically the cleaning of the plug and socket contacts.

**8.** The second line servicing of the C.R.T. controller is restricted to the routine servicing outlined in para. 5 and the replacement of certain sub-assemblies found faulty after mechanical and/or functional inspection para. 9 to 21 inclusive. The replaceable sub-assemblies are the plug-in printed circuit boards and the cathode ray tube.

**Mechanical inspection**

**9.** A thorough examination of the C.R.T. controller should be made before power is applied and before functional tests are made. Check: —

(1) General assembly conforms to the current modification state.

(2) Piece parts, plating, etc. show no signs of damage, rust or corrosion.

(3) All components and cableforms are secure, show no signs of overheating or damage.

(4) All wiring is free from damage to insulation and not too close to resistors.

(5) Components are secure on printed circuit boards and are not squashed.

(6) All soldered connections are neat and mechanically sound.

(7) All fixing screws are correctly seated and secured with varnish, unless otherwise locked.

(8) Sub-assembly plugs and sockets are clean, undamaged and all pins are free to move individually.

(9) External plugs and sockets are clean, undamaged and all pins are free to move individually.

(10) Engraved figures and letters are legible.

(11) All applicable modifications have been incorporated on all sub-assemblies and the modification states are recorded on modification labels.

**10.** The following functional tests should be carried out to ensure correct operation of the C.R.T. controller. All checks are performed with the controller in the test bench rig, and the cover of the unit removed for visual checking when necessary. Unless stated otherwise, all tests should be carried out with supplies of 28V d.c. and 115V, 400 c/s and at an ambient temperature not exceeding 55°C.

**Switching on**

**11.** Ensure that the equipment is properly earthed. Connect the controller to the test rig as shown in Part 3, Chapter 4, fig. 3 and connect just the 28V d.c. supply. Rotate the read-out unit OFF/DIM switch fully clockwise and ensure that the panel lamps are lit. Then connect the 115V 400 c/s supply.

## FUNCTIONAL TESTS

**12.** Fit the test graticule into the hood of the cathode ray tube and set the C.R.T. controller and test set controls as follows: —

(1) 1832 C.R.T. Controller.

| *Control.* | *Position.* |
|---|---|
| TIMEBASE. | 2 |
| FUNCTION. | M |
| DISPLAY GAIN | Fully clockwise |
| KC and LORAN C r.f. controls | Fully clockwise |

(2) 1863 Test Set.

| *Control.* | *Position.* |
|---|---|
| SIGNAL SELECT | C |
| BASIC RATE | SS |
| SPECIFIC RATE | O |
| SLAVE SETTING | 2 |
| POWER SOURCE | 1831-1 |

**13.** The trace length should be 4·5 cm ± 10%, symmetrical and horizontally displaced about the tube centre line within ± 0·2 cm. If the trace

appearance is not correct then adjustment can be affected by the following controls: —

RV8 — This controls the trace position on the 'Y' axis.

RV10 — This controls the trace position on the 'X' axis.

RV11 — This control varies the trace length.

**Note . . .**

*For the location of these controls see the note following para.* 15.

**14.** On the C.R.T. controller set the TIMEBASE switch to 1. Rotate the read-out unit centre SELECT STATION (basic rate) control through all its positions and note that the trace length is not less than 4·0 cm. at any position. Repeat this test with the FUNCTION switch set to position A and B. With the test set and read-out unit set to each basic rate position in turn, ensure that all three sets of positive tracking gates are displayed at each position.

**15.** Set the test set SIGNAL SELECT switch to A1 and the BASIC RATE switch to H. On the read-out unit, set the left hand SELECT STATION control to 1 and select rate HO. Ensure that a two line display exists on the c.r.t. which is not less than 4 cm. long and which is equally spaced about the centre-line by 1 cm. ± 0·2 cm. On each line of the display there should be a high marker pedestal greater than 0·4 cm. high. Repeat these checks with the read-out unit set to rates S and L. The trace length is controlled by RV11 as mentioned in para. 13, but the positions of the two traces are controlled separately as follows: —

RV7 controls the 'Y' axis position of the upper trace.

RV9 controls the 'Y' axis position of the lower trace.

**Note . . .**

*Controls RV7 to RV11 are mounted on board A (Part 2, Chap. 3, fig. 2). Viewed from the underside and from rear to front, the controls are arranged: RV7 and RV8, RV9 and RV11, RV10.*

**16.** With the basic rate on the read-out unit reset to H, set the C.R.T. controller TIMEBASE switch to position 2 and check that a two line display exists that is 4·5 cm. long ± 10%, and equally spaced about the centre line by 1 cm. ± 0·2 cm. Two marker pedestals should be displayed on the screen, one at the start of each trace. Repeat this check with the read-out set to rates S and L in turn.

**17.** With the basic rate reset to H once more on the read-out unit set the C.R.T. controller TIMEBASE switch to position 3. A single trace 4·5 cm. long ± 0·5 cm. positioned within 0·2 cm. about the tube centre line should be obtained.

**18.** Set the test set SIGNAL SELECT switch to C, the read-out left hand SELECT STATION control to C. WIDE and set the C.R.T. controller TIMEBASE switch to position 2. A single trace should appear along the tube centre line and should be 4·5 cm. ± 10%. All eight positive tracking gates should be displayed and should be 0·5 cm. high. Repeat this check with the FUNCTION switch set to A and B.

**19.** Set the C.R.T. controller TIMEBASE switch to position 3. A single trace positioned on the tube centre line should be displayed and should be 4·5 cm. ± 10% long. Positioned on this trace should be one positive tracking gate greater than 0·5 cm. high. Repeat this test with the FUNCTION switch set to A and B.

**20.** Ensure that there is no breaking or unwanted modulation of the trace in any of the positions tested above and also check that the brightness, focus and astigmatism is satisfactory on all timebase functions.

**Note . . .**

*The brightness* (BRIL), FOCUS *and astigmatism* (ASTIG) *controls are mounted on a panel located at the left of the unit (Part* 2, *Chap.* 3, *fig.* 1).

**21.** Carry out a complete setting up procedure for Loran C and Loran A operation as detailed in Part 3, Chapter 4, para. 15 to 19 and para. 52 to 54 to check the operation of each switch on the C.R.T. controller. It is possible to verify the operation of the COARSE, MEDIUM and 10$\mu$S JUMP switches, the ALL JUMP switch and the CODE JUMP position of the STORE ZERO/CODE JUMP switch. This is done as follows: couple the cable that supplies PL1 of the C.R.T. unit to SK2 of the test set then, with the test set METER FUNCTION switch set to 1832, the meter should read full scale on operation of the C.R.T. controller switches mentioned previously.

**22.** The circuitry allied to each printed circuit board is shown in Table 1. A list of fault symptoms and the appropriate fault action is given in Table 2.

**Note . . .**

*If it is necessary to change board VA, then the Y shift and Y gain controls may require adjustment, see para.* 12 *to* 15.

## TABLE 1

**Circuit board functions of C.R.T. Controller Type 1832.**

| Board | Function |
|---|---|
| VA | Sweep generator.<br>X Output amplifier.<br>Y Output amplifier.<br>Alternator binary (Loran A).<br>Tracking gate amplifier. |
| VB | Master single sweep binary.<br>Slave single sweep binary.<br>Master binary.<br>Master single sweep and ½ PRT 'or' gate.<br>Master single sweep and Slave single sweep 'or' gate. |
| | Scope trigger Invertor. |
| VC | Bright-up binary.<br>Bright-up output stages.<br>Pre-set BRIL, ASTIG and FOCUS controls.<br>Components for + 24V stabilized line. |
| VE | Loran A timebase 2 and 3 pedestal monostables.<br>Master and ½ PRT inverted 'or' gate.<br>Loran C indicator bandwidth switching.<br>Sweep trigger gate circuit.<br>Several timing resistors. |

## TABLE 2

**Fault check table**

| Symptom | Fault and fault action |
|---|---|
| (1) No oscilloscope trace at any position of TIMEBASE switch. | This could mean that the bright-up binary circuit has failed, therefore change board VC.<br>Turn the BRILL 1 control fully clockwise, if there is still no trace then the timebase circuit may be faulty, change board VA or if necessary board VE. |
| (2) Dim trace not affected by BRILL 1 or BRILL 2 controls. | Cathode ray tube probably faulty. Replace the tube. |
| (3) Bright spot only. | This is most likely to be a timebase fault. Replace board VC; if the fault still persists then replace board VA and if necessary then VE. |
| (4) Bright spot at start of trace on timebase 2 and 3 only. | The bright-up binary circuit is probably at fault. Change VC board. |
| (5) Trace appears but with no tracking gates or pedestals. | Tracking gate amplifier is most likely faulty on board VA. Replace the board. |
| (6) Trace with only one pedestal on Loran A operation. | The gating circuitry on board VE is possibly faulty or the marker monostable on board VB is faulty. Change VE board or if fault still persists, change board VB. |
| (7) No Loran A or C signals. | The Y gain amplifier is possibly faulty. Change VA board. If the fault persists on Loran C only, then the ancillary relay is at fault. |
| (8) No double trace on Loran A at timebase 1 or 2. | The alternator binary is possibly faulty. Change board VA. Alternatively the triggers to this binary are not present. Change VE board. |
| (9) Tracking gates not evenly displaced across tube face in timebase position 2. | Sawtooth generator non-linear. Change board VA. |
| (10) Amplitude of Loran A and Loran C signals greatly reduced. | If the gain reduction is on one axis only on the tube then the X or Y amplifier is faulty. Change VA board. If the gain reduction is on both axis then the tube life has possibly expired. Replace the tube. |
| (11) Other symptoms. | If the fault cannot be cured by replacing the tube or any of the circuit boards, then it must be assumed that it lies in the ancillary circuitry on the C.R.T. controller. |

# Chapter 6

# SECOND LINE SERVICING: INDICATOR DIGITAL DISPLAY (DECCA TYPE 1833)

## LIST OF CONTENTS



## LIST OF ILLUSTRATIONS



## GENERAL INFORMATION

**1.** The procedure detailed in this chapter is directed to the diagnosis and, where possible, the repair of faults in the indicator digital display (read-out unit) of the Loran ARI.23180 installation. Faulty operation of a read-out unit may become apparent during a ground check or during operation in flight. In the latter case the following details should be obtained: —

(1) Nature of fault or reported failure.

(2) Duration of failure(s) if intermittent.

(3) Mode of operation and pulse repetition rate at which the fault was evident.

**2.** Reference to any available information on the nature of the operational failure will assist in the quick location of the fault. Where such information indicates that the fault is of an intermittent nature, a prolonged run of the unit may be necessary to enable the fault to be repeated.

**3.** When no fault condition can be found in the unit, despite an operational defect report, a decision on the serviceability of the unit must be made on the following considerations: —

(1) The adequacy and reliability of the initial defect report.

(2) The nature of the reported failure.

(3) The likelihood of a cable fault in the installation.

(4) The possibility of a supply failure.

### Test equipment

**4.** The following items of test equipment are required to carry out the functional checks on the read-out unit of the Loran ARI.23180.

(1) Multimeter set (CT498A) 5QP/1057049.

(2) Power supply unit 10K/9561998.

(3) Receiver Loran Type 1831, 10D/5826-99-955-8336 (Part of bench rig).

(4) Indicator Loran Type 1832, 10Q/5826-99-955-8337 (Part of bench rig).

(5) Indicator digital Type 1833, 5826-99-955-8338. (Part of bench rig).

(6) Aerial amplifier unit Type 1953, 10U/5826-99-955-8339. (Part of bench rig).

(7) Test set, Loran Type 1863 10S/6625-99-107-1415 together with the following cable assemblies: Decca Type 53ABB 5826-99-195-8848, Decca Type 53ABC 5826-99-195-8849, Decca Type 53ABD 5826-99-194-3331 and Decca Type 53ABE 5826-99-195-8850.

(8) Cable assembly, set electrical Type 1864 5826-99-107-7566 comprising the following cables, Decca Type 53 ABH 5826-99-195-0577; Decca Type 53 ABJ 5826-99-195-0578, Decca Type 53 ABK 5816-99-195-0579. Decca Type 53 ABL 5826-99-195-0580. Decca Type 53ABM 5826-99-195-0581. Decca Type 53 ABN 5826-99-195-0583. Decca Type 53 ABP 5826-99-195-0582.

(9) Extractor readout Decca Type 53/1987, 10AG/5826-99-222-9115.

(10) Stop watch 6B/9101001.

**Procedure**

**5.** The second line check and fault location procedure comprises a mechanical inspection of the read-out unit, followed upon satisfactory completion, by a functional test routine. If the unit passes satisfactorily through these checks it may be assumed serviceable. Unless a unit has a self-evident fault, it should be subjected to the complete test procedure. A complete check of the unit should then be made when the fault has been rectified.

**6.** Most faults in the read-out unit will necessitate the replacement of a faulty sub-assembly. Servicing procedure should however include the overall cleaning of the unit, specifically the cleaning of the plug and socket contacts and lamp sockets.

**7.** The second line servicing of the read-out unit is restricted to the routine servicing outlined in para. 5 and the replacement of certain sub-assemblies and lamps found faulty after mechanical and/or functional inspection. The replaceable sub-assemblies are the units which house the ten lamps for each digit of the display.

**Mechanical inspection**

**8.** A thorough examination of the read-out unit should be made before power is applied and before functional tests are made. Check:—

(1) General assembly conforms to the current modification state.

(2) Piece parts, plating, etc. show no signs of damage, rust or corrosion.

(3) All components and cableforms are secure, show no signs of overheating or damage.

(4) All wiring is free from damage to insulation and not too close to resistors.

(5) All soldered connections are neat and mechanically sound.

(6) All fixing screws are correctly seated and secured with varnish, unless otherwise locked.

(7) External plugs and sockets are clean, undamaged and all pins are free to move individually.

(8) Engraved figures and letters are legible.

(9) All applicable modifications have been incorporated on all sub-assemblies and the modification states are recorded on modification labels.

## FUNCTIONAL TESTS

**9.** The following functional tests should be carried out to ensure correct operation of the read-out unit. All checks are performed with the read-out in the test bench rig, and the cover of the unit removed for visual checking when necessary. Unless stated otherwise, all tests should be carried out with supplies of 28V d.c. and 115V, 400 c/s and at an ambient temperature not exceeding 55°C.

**Initial checks**

**10.** Ensure that the equipment is properly earthed. Connect the read-out unit to the test rig as shown in Part 3, Chapter 4, fig. 3 and connect just the 28V d.c. supply. Rotate the read-out unit OFF/DIM switch fully clockwise and ensure that the panel lamps are lit. Then connect the 115V 400 c/s supply. If any of the panel lamps should be found faulty, they can be unscrewed from the front panel with a large bladed screwdriver or a coin. The bulb is then inserted into the sleeve part of this holder.

**OFF/DIM switch**

**11.** To check the OFF/DIM switch, rotate the switch progressively counter-clockwise and note that the panel illuminating lamps become dimmer with each position of the switch.

**SELECT STATION switch**

**12.** Verify the operation of the SELECT STATION switches as follows:

(1) Set the left hand SELECT STATION control to C WIDE.

(2) Set the other SELECT STATION controls to SH and O.

(3) Set the c.r.t. controller FUNCTION switch to M and the TIMEBASE switch to 1.

(4) With the test set SIGNAL SELECT switch at C and the basic and specific rates set to SH.O the trace of the c.r.t. controller should cease drifting.

(5) Repeat this test with the read-out and test set controls set to SL and SS and all position of the specific rate switch (0 to 7).

**13.** Continue the test on the SELECT STATION switches as follows:

(1) Set the left hand SELECT STATION control to 1 and select rate HO on the basic and specific rate switches.

(2) Set the test set SIGNAL SELECT switch to A1 and select rate HO; with the same rate selected on the test set as is selected on the read-out unit the c.r.t. trace should cease to drift.

(3) Repeat this test with the read-out and test set controls set to 1.H.O, 2.H.O, 3.H.O, 3.L.O and 3.S.O; a stationary trace should be observed at each position.

**14.** To ensure the C NARROW position of the left hand SELECT STATION switch is satisfactory, lock in the receiver as detailed in Part 3, Chapter 4, para. 15 to 19. Observe the pulse shape when switched to timebase position 3, in particular the leading edge. Switch the read-out control to C NARROW;

the rise time of the pulse displayed should appear delayed.

### A, A/B, B Switch test

**15.** With the read-out A, A/B, B switch set to A/B the time taken for five A and five B readings sould be between 17 and 24 seconds. Set the switch to A; the time taken for 10 successive readings should be 5·6 to 8·2 seconds. Repeat this test with the switch at B; the same time limit applies as for position A.

### Read-out display lamp test

**16.** To test each lamp of the digital displays within the read-out unit, set the centre SELECT STATION switch to SS and the RH SELECT STATION switch to O. Operate the COARSE, MEDIUM and 10$\mu$S JUMP switches to check the lamps for each digit of the read-out unit for equal illumination as follows:

(1) To check 10,000$\mu$S digits, depress and hold the COARSE SLEW switch.

(2) To check the 1000$\mu$S digits, momentarily depress the COARSE SLEW switch to display each digit.

(3) To check the 100$\mu$S digit, momentarily depress the MEDIUM SLEW switch to display each digit.

(4) The 10$\mu$S digit can be checked by operating the 10$\mu$S JUMP switch to display each digit.

(5) The 1$\mu$S digit is tested by setting the LH SELECT STATION switch to position 3, the centre SELECT STATION switch to S and offsetting the LORAN ADRIFT control slightly.

### Display lamp replacement

**17.** To change a faulty lamp within one of the digital indicator units, depress the unit with the rubber tool provided and withdraw it from the read-out unit. The bulbs can be removed by placing a pin or some other pointed object beneath the bulb flange and gently levering out the bulb.

**18.** The bulbs relevant to each digit of the indicator unit are shown in fig. 1, the spare bulb

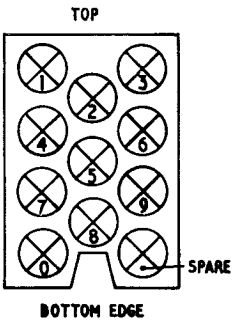


**Fig. 1. Indicator bulb arrangement**

being the one at the lower right hand side viewed from the rear. It is possible that one or more digits of an indicator may appear faulty even though the bulbs are good, if this is the case then the bulb contacts should be cleaned. To replace the indicator unit simply press the unit (manufacturers label uppermost) into the read-out unit using the tool provided. A click should be heard; the tool can then be removed.

### Alarm lamp test and replacement

**19.** All three alarm lamps can be tested simultaneously by setting the OFF/DIM switch to OFF, waiting a couple of minutes and then resetting the switch to the 'on' position (clockwise). All three lamps should initially come on although they may only remain on for about one second. To replace a faulty lamp unit, remove the plugs from the rear of the read-out unit and remove the rear cover. Remove the small socket from the rear of the suspect lamp and slide off the rubber sleeve that holds the lamp unit against the front panel — the lamp unit can then be withdrawn through the front panel. When replacing the new lamp unit, ensure that the rubber sleeve is as far onto the lamp as it will go, or the lamp will be loose in the panel. Replace the lamp socket and then replace the rear cover.

**20.** In the foregoing tests, if the fault condition could not be cured by changing lamps, then the unit should be sent to the third line test department together with details of the fault.

# Chapter 7

# SECOND LINE SERVICING: AMPLIFIER, ANTENNA (DECCA TYPE 1953)

## LIST OF CONTENTS



## LIST OF ILLUSTRATIONS



## GENERAL INFORMATION

**1.** The procedure detailed in this chapter is directed to the diagnosis and, where possible, the repair of faults in the aerial amplifier of the Loran ARI.23180. Faulty operation of an amplifier may become apparent during a ground check or during operation in flight. In the latter case the following details should be obtained: —

(1) Nature of fault or reported failure.

(2) Duration of failure(s) if intermittent.

**2.** Reference to any available information on the nature of the operational failure will assist in the quick location of the fault. Where such information indicates that the fault is of an intermittent nature, a prolonged run of the unit may be necessary to enable the fault to be repeated. In some instances, failure may not recur until the equipment has stabilized at full operating temperature.

**3.** When no fault condition can be found in the unit, despite an operational defect report, a decision on the serviceability of the unit must be made on the following considerations: —

(1) The adequacy and reliability of the initial defect report.

(2) The nature of the reported failure.

(3) The likelihood of a cable fault in the installation.

(4) The possibility of a supply failure.

### Test equipment

**4.** The following items of test equipment are required to carry out the functional tests on the aerial amplifier of the Loran ARI. 23180.

(1) Oscilloscope set (CT536) 10S/6625-99-952-2040 or Hewlett Packard oscilloscope Type 108A 10S/6625-99-194-9182.

(2) Multimeter set (CT498A) 5QP/1057049.

(3) Signal generator set (CT452A) 10S/9008337.

(4) Receiver Loran Type 1831, 10D/5826-99-955-8336 (part of test rig).

(5) Indicator Loran Type 1832, 10Q/5826-99-955-8337 (part of test rig).

(6) Indicator digital Type 1833, 5826-99-955-8338 (part of test rig).

(7) Aerial amplifier unit Type 1953, 10U/5826-99-955-8339 (part of test rig).

(8) Cable assembly, set electrical Type 1864, 5826-99-107-7566 comprising the following cables, Decca Type 53 ABH 5826-99-195-0577, Decca Type 53 ABJ 5826-99-195-0578

Decca Type 53 ABK 5816-99-195-0579. Decca Type 53 ABL 5826-99-195-0580. Decca Type 53 ABM 5826-99-195-0581. Decca Type 53 ABN 5826-99-195-0583. Decca Type 53 ABP 5826-99-195-0582.

**Procedure**

**5.** The second line check and fault location procedure comprises a mechanical inspection of the aerial amplifier unit, followed upon satisfactory completion, by a functional test routine. If the unit passes satisfactorily through these checks it may be assumed serviceable.

**6.** A fault in the aerial amplifier will normally necessitate the replacement of a faulty valve. Servicing procedure should however include the overall cleaning of the unit, paying particular attention to valve pins and their bases and external plugs and sockets.

**Mechanical inspection**

7. A thorough examination of the aerial amplifier should be made before power is applied and before functional tests are made. Check: —

(1) General assembly conforms to the current modification state.

(2) Piece parts, plating etc. show no signs of damage, rust or corrosion.

(3) All components and cableforms are secure, show no signs of overheating or damage.

(4) All wiring is free from damage to insulation and not too close to resistors.

(5) All soldered connections are neat and mechanically sound.

(6) The three anti-vibration mountings are undamaged and are free to move in all directions.

(7) All fixing screws are correctly seated and secured with varnish, unless otherwise locked.

(8) Valves are correctly inserted.

(9) External plugs and sockets are clean, undamaged and all pins are free to move individually.

(10) Engraved figures and letters are legible.

(11) All applicable modifications have been incorporated on all sub-assemblies and the modification states are recorded on modification labels.

## FUNCTIONAL TESTS

**8.** The following functional tests should be carried out to ensure correct operation of the receiver unit. All checks are performed with the aerial amplifier in the test bench rig, and the cover of the unit removed for visual checking when necessary. Unless stated otherwise, all tests should be carried out with supplies of 28V d.c. and 115V, 400 c/s to the test rig and at an ambient temperature not exceeding 55°C.

**Initial checks**

**9.** Ensure that the equipment is properly earthed. Connect the aerial amplifier to the test rig as shown in fig. 1 then connect the 115V 400 c/s supply.

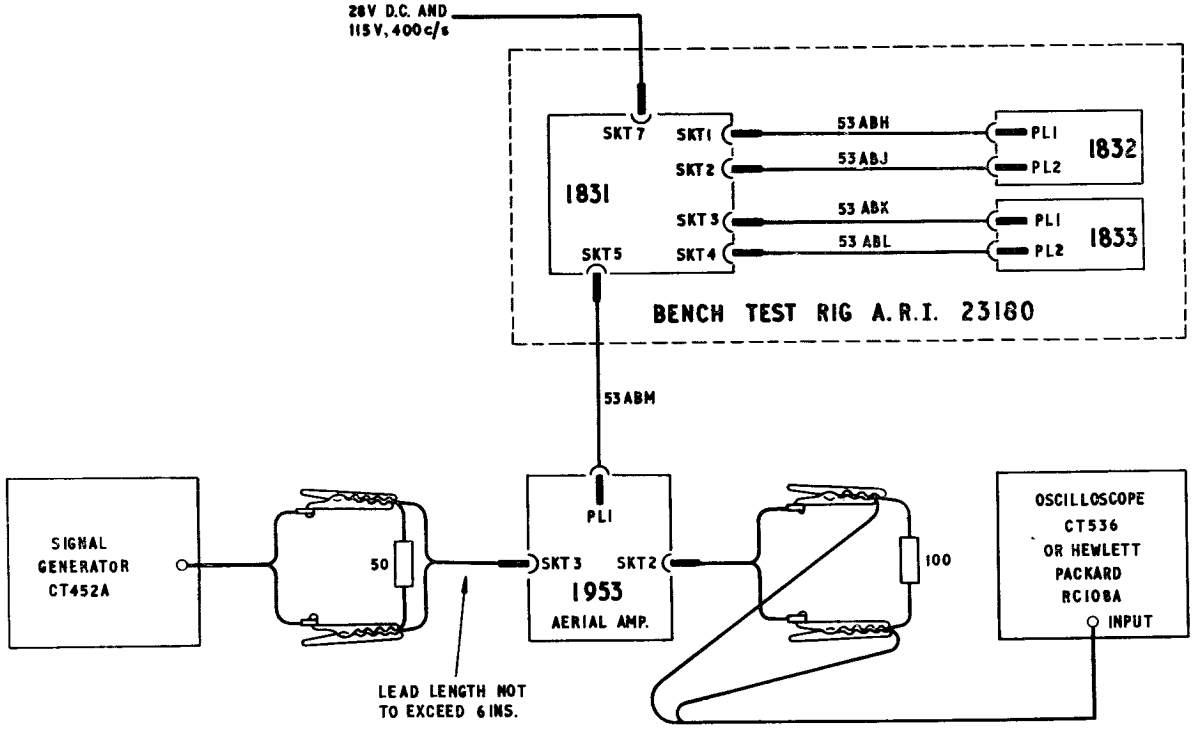


**Fig. 1. Test connections**

**Voltage tests**

**10.** Check the following operating voltages within the aerial amplifier using the multimeter:

| *Test Point* | *Voltage* |
|---|---|
| Between junction of L1/C4 (HT line) and earth | 160V ± 10V |
| Between junction of R6/R12 and earth | 10·8V ± 1V |
| Between junction of R4/R5 and earth | 10·2V ± 1V |
| Between junction of R6/R9 and cathode of V1 | 1·25V ± 0·25V |
| Between junction of R6/R9 and cathode of V2 | 1·25V ± 0·25V |

**Note . . .**

*If one of the last two valve readings is lower than the other by more than 20%, then a valve change and possible valve selection may be necessary.*

**Amplifier gain**

**11.** Connect up the equipment as shown in Fig. 1 and, as the input impedance of the aerial amplifier is high, terminate the signal generator output with the correct value load (50 ohm). Connect a 100 ohm-load across the output of the aerial amplifier and then proceed as follows: —

(1) Set the read-out unit SELECT STATION switch to C WIDE and turn the OFF/DIM switch clockwise. With the signal generator set to 100 kc/s, correctly terminated, and coupled directly to the oscilloscope, adjust the generator output attenuators so that a 1 cm display is produced on the oscilloscope with the sensitivity controls set to 300 mV/cm.

(2) Couple this known signal level to the aerial amplifier input (SK3) and transfer the oscilloscope probe to the aerial amplifier output (SK2) 'male' connection. With the oscilloscope sensitivity control set to 3V/cm the display amplitude should be 1·5 cm indicating a gain of 15. A tolerance of 25% is permitted on this gain figure. If the gain falls below this limit then valve replacement will be necessary.

**Input impedance**

**12.** With the aerial amplifier connected as in para. 11, insert a 270pF capacitor in series with the signal feed from the signal generator; this capacitor must be inserted at the aerial amplifier end of the lead. Repeat para. 11(1) and (2); if the aerial amplifier output is less than 75% of the output obtained in para. 11(2), a low input impedance fault is indicated.

**Bandwidth**

**13.** Remove the 270 pF capacitor and reconnect the signal generator set to 100 kc/s directly to the aerial amplifier. Note the aerial amplifier output amplitude on the c.r.t. and then increase the generator output by 3dB. Sweep the signal generator frequency to 10 kc/s and note that the amplitude of the c.r.t. deflection is greater than the initial amplitude obtained at 100 kc/s. Swing the generator frequency above 100 kc/s until the initial 100 kc/s c.r.t. deflection is obtained; the signal generator should indicate at least 420 kc/s. If these bandwidth figures cannot be obtained, then the fault is most likely to be in the ancillary aerial amplifier components and it must therefore be returned to the third line service bay. Repeat this test for Loran A frequencies with the read-out unit-left-hand SELECT STATION switch set to 1 and with the signal generator centre frequency of 1·9 Mc/s; the corresponding frequencies for the −3dB points should be above 1·3 Mc/s and below 2·3 Mc/s.

**Distortion test**

**14.** With the left hand SELECT STATION switch set to 1, set the signal generator to 1·9 Mc/s at 0·5V r.m.s. output. Observe the aerial amplifier output signal on the oscilloscope; there should be no visible signs of distortion.

Printed for H M.S.O by Christchurch Times Ltd , Christchurch.
(6973) 713045 220 7/69 483/1