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Colin Hinson

In the village of Blunham, Bedfordshire.

PUBLICATIONS
L. 5
R.A.F. LOCKING

AIR PUBLICATION
115 K-1201-1
Issued August 69

Mk.5 AUTONOMOUS DISPLAY (Plessey Type TDS5)

BASIC DISPLAY

GENERAL, TECHNICAL AND SERVICING INFORMATION

BY COMMAND OF THE DEFENCE COUNCIL

J. Durrant

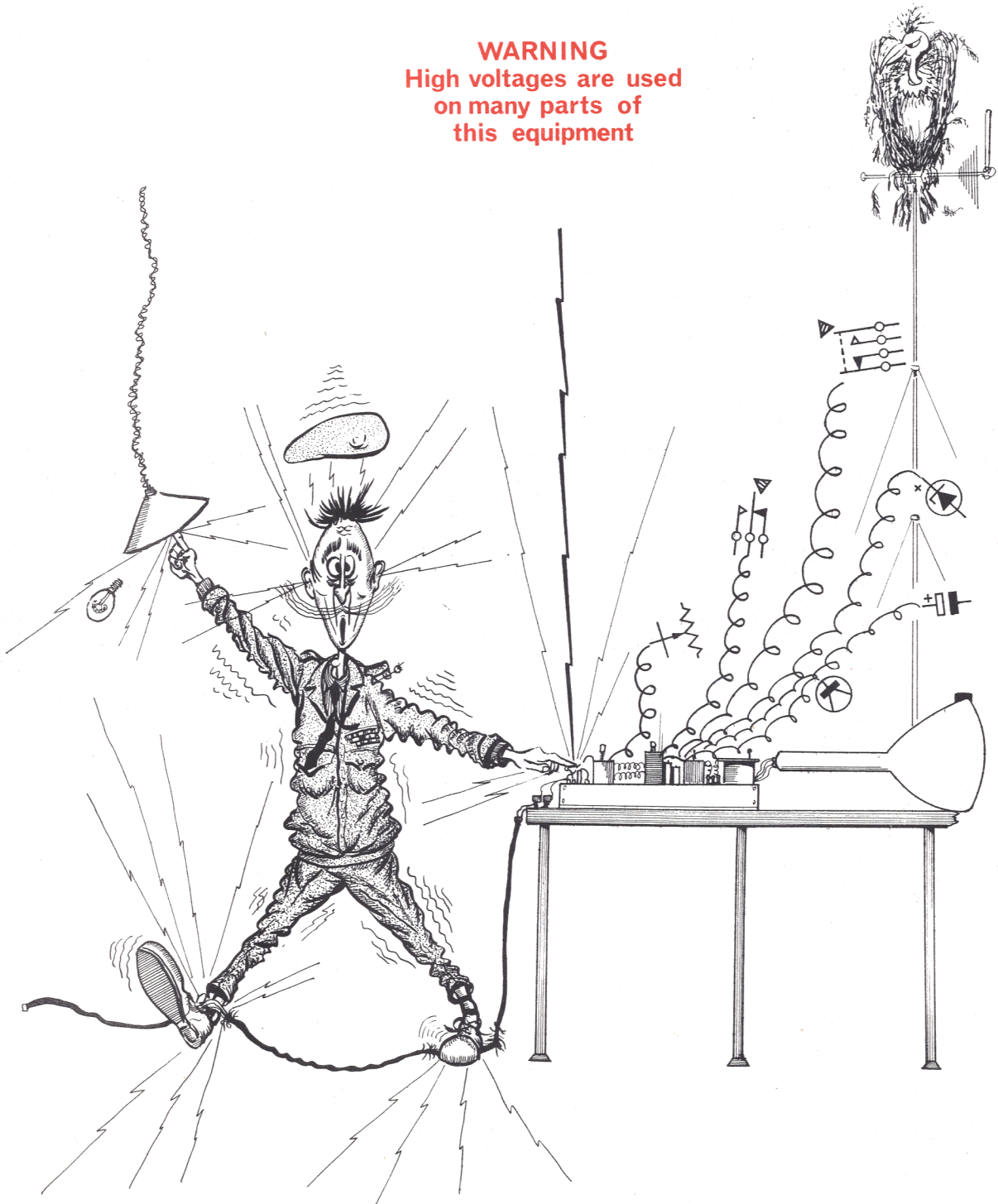
(Ministry of Defence)

FOR USE IN THE
ROYAL AIR FORCE

(Prepared by the Ministry of Technology)

DANGER ! HIGH VOLTAGE

WARNING
High voltages are used
on many parts of
this equipment



PREFACE

A. P. 115K-1201-1 relates to the basic Mk. 5 display; for some applications of the display supplementary information units are published. Each supplementary information unit is a coded publication in its own right, but for convenience it is issued for gathering in the same binder as A. P. 115K-1201-1.

In general, each supplementary information unit provides:-

- (1) A description of the display as tailored for that application in terms of the variants of units and Panels, Electronic Circuit, with block diagram.
- (2) Details of any preset controls whose settings are non-standard.
- (3) Internal wiring diagrams.
- (4) Table of units and plug-in boards fitted, quoting equipment and publication references, and modification state.
- (5) Technical information on any special-to-application units or panels fitted in, or attached to, the display which are not described in A. P. 115K-1201-1.
- (6) Servicing information peculiar to the application, with list of approved general and special-to-type test equipment.

The A. P. 115K-1201 to -1299 series of publications will supersede the commercial handbooks on the Mk. 5 displays.

NOTE TO READERS

The subject matter of this publication may be affected by Defence Council Instructions, Servicing schedules (-4 and -5), or 'General Orders and Modifications' leaflets in this A. P., in the associated publications listed below, or even in some others. If possible, Amendment Lists are issued to correct this publication accordingly, but it is not always practicable to do so. When an Instruction, Servicing schedule, or leaflet contradicts any portion of this publication, the Instruction, Servicing schedule, or leaflet is to be taken as the overriding authority.

The inclusion of references to items of equipment does not constitute authority for demanding the items.

Each leaf, except the original issue of preliminaries, bears the date of issue and the number of the Amendment List with which it was issued. New or amended technical information on new leaves which are inserted when this publication is amended will be indicated by filled triangles thus: ◀ xxxxxx ▶ . When information is simply removed, a pair of triangles will appear in its place thus: ▶ ◀

LIST OF ASSOCIATED PUBLICATIONS

Mk.5 autonomous HRI Display in SJCC	A. P. 115K-1202-1
◀ Mk.5 autonomous HRI Display in ADRS	A. P. 115K-1203-1
Mk.5 autonomous PPI Display in TGRI (AT) 23214 (S259 Radar System)	A. P. 115K-1204-1
Mk.5 autonomous PPI Display in FGRI 23154 and TGRI (AT) 26038/1 and /2 (AR-1)	A. P. 115K-1205-1
Mk.5 display in Radar Type 89 system	A. P. 115K-1206-1
Mk.5 autonomous HRI Displays in Bishop's Court	A. P. 115K-1207-1
Mk.5 displays in GL161 systems	A. P. 115K-1208-1 ■

CONTENTS

Title Sheet
Amendment Record Sheet
High Voltage Warning
Preface
Note to Readers
List of Associated Publications
Contents Sheet

LIST OF CHAPTERS

PART 1 - GENERAL INFORMATION

- Chap.1 Introduction
2 System principles
3 General description
4 Circuit techniques

PART 2 - TECHNICAL INFORMATION

SECTION 1 - UNITS

- Chap.1 Power Unit 11600
2 EHT Power Unit 11601
3 Deflection Coil Drive Amplifier 12502
4 Viewing unit control panel
5 Viewing unit junction unit
6 Cooling system
7 Deflection Coil Assembly 11702A
8 Character Drive Unit 12500
9 Deflection Coil Drive Amplifier 12505
10 Power Unit 11605

PART 2, SECTION 1 (contd.)

- Chap.11 Power Unit 11606
- 12 Viewing Unit Junction Unit 12795/A (21in)
- 13 Deflection Coil Assembly 11703A
- 14 Cooling system (21in)
- 15 Focus Control Panel 12701

SECTION 2 - PLUG-IN BOARDS

- Chap.1 Timing boards (MJE series)
- 2 Deflection boards (MRG and MRH series)
- 3 Deflection boards (MRK series)
- 4 Video boards (MFD series)
- 5 Sampling gate generator boards
- 6 P. W. boards (MUE series)
- 7 P. W. boards (MQR series)
- 8 P. W. boards (NUJ series)
- 9 Category selection boards (MJS series)
- 10 Video boards (MFK series)
- 11 Deflection boards (MRM series)

PART 3 - SERVICING INFORMATION

SECTION 1 - DISPLAY SERVICING

- Chap.1 Maintenance techniques
- 2 Display accuracy test (HRI)
- 3 Display accuracy test (PPI)
- 4 Display setting-up procedure (HRI)
- 5 Display setting-up procedure (PPI)
- 6 CRT replacement
- 7 Maintenance of cooling system
- 8 CRT replacement (21in)
- 9 Maintenance of cooling system (21in)

PART 3 (contd.)

SECTION 2 - UNIT TESTING AND SETTING-UP PROCEDURES

- Chap.1 Power Unit 11600
- 2 EHT Power Unit 11601
- 3 Deflection Coil Drive Amplifier 12502
- 4 Power Unit 11605
- 5 Power Unit 11606
- 6 Deflection Coil Drive Amplifier 12505

SECTION 3 - PLUG-IN BOARD TEST PROCEDURES

- Chap.1 Timing boards (MJE series)
- 2 Deflection boards (MRG and MRH series)
- 3 Deflection boards (MRK series)
- 4 Video boards (MFD series)
- 5 Sampling gate generator boards
- 6 P. W. boards (NUE series)
- 7 P. W. boards (NQP series)
- 8 P. W. boards (NUJ series)
- 9 Category selection boards (MJS series)
- 10 Video boards (MFK series)
- 11 Deflection boards (MRM series)

GENERAL INFORMATION

Chapter 1

INTRODUCTION

LIST OF CONTENTS

	Para.
General	1
General assembly	4
Printed wiring (plug-in) boards	12

LIST OF ILLUSTRATIONS

	Fig.
Mk. 5 Autonomous Display (12in)	1
Mk. 5 Autonomous Display (21in)	2

GENERAL

1. The Mk. 5 Autonomous Display (Plessey Type TDS5) is a self-contained fixed coil display unit whose role and character is a function of the plug-in boards fitted. Depending upon the type and configuration of the plug-in boards, it can provide h. r. i. or p. p. i. presentation and can have synthetic marks and symbols.
2. The purpose of this publication is to describe the basic display unit, to provide information on basic units and plug-in boards fitted and to distinguish between type variants of basic units and boards.
3. The display unit has several Service applications. In general, it is associated with, or forms an integral part of, a larger system or equipment, and its application therein will be described in the publication on the larger system or equipment. Certain information specific to a particular application (e. g. non-standard panels, re-designed or modified units or boards, list of boards fitted, particular servicing information, etc.) is published in coded information units in the number series A. P. 115K-1202, 1203, etc. ; such information units are supplementary to this publication for a particular application and are intended to be gathered in the same cover as this handbook.

GENERAL ASSEMBLY

4. The 12in display unit (see Fig.1) consists of a viewing unit fitted to a wedge-shaped mount which also carries the operator's control panel; the viewing unit and mount are located on a floor-standing console or desk. The viewing unit houses the c. r. t. and the majority of the electronic circuits. Fitted to the rear of the viewing unit is a removable junction unit which provides all connections between the viewing unit and the mount and console units.

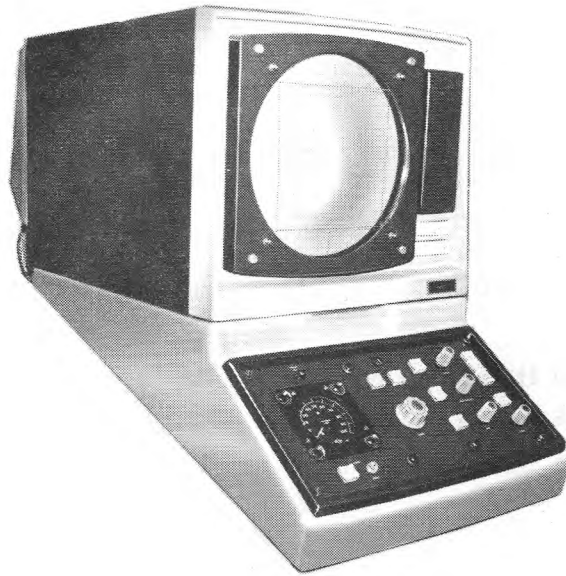


Fig.1 Mk.5 Autonomous display

5. The 21in viewing unit (see Fig.2) is designed to be fitted below, and provides the mounting for the horizontal table top. The whole assembly is free-standing and is at a convenient height for the standing operators. The viewing unit is built up on a main structure frame which supports and houses various sub-units.

6. Each display unit contains its own power supplies and all the circuits necessary for the presentation of radar information, calibration marks and strobe (height line on h. r. i.; bearing marker on p. p. i.). All circuits are semiconductor devices with the exception of the rectifiers in the e. h. t. power unit and the c. r. t.

7. The heat generated within the unit is removed by means of an internal heat exchanger system.

8. The viewing unit contains a medium or long-persistence c. r. t. fitted with a suitably coloured implosion screen; the type of c. r. t. fitted can vary between applications of the display.

9. The viewing unit control panel controls are as follows:-
- (1) Panel illumination control (2 controls on 21in viewing unit).
 - (2) Focus control.
 - (3) X and Y centring controls (not present on 21in viewing unit).
 - (4) Video channel gain controls (4 controls).
 - (5) Range marker brightness (two separate controls engraved with the marker interval).
 - (6) Radar trace brightness
 - (7) Video limiter control.
 - (8) Push-button switches for off, on and standby conditions.
 - (9) Four range selector push-buttons (in some applications these push-buttons are not fitted).

However, in some applications additional controls may be fitted which are not listed.

10. The operator's control panel may be mounted on the viewing unit mount or on the desk top of the console and accommodates controls that relate to the display unit function. These vary with each application and are described in the appropriate system publication or in the coded information unit for a particular application of the display.

11. The display is capable of operating in an ambient temperature range of -10°C to $+35^{\circ}\text{C}$.

PRINTED WIRING (PLUG-IN) BOARDS

12. The flexible nature of the autonomous display system enables a number of different types of presentation to be produced. The particular type of display is determined by the types of printed wiring boards fitted in the viewing unit. These printed boards are divided into main categories according to their function, i. e. deflection boards, timing boards, etc. Each category of board is identified by the first three letters of a four-letter designation or code. The four-letter code has the significance: (example, timing board MJEZ) M = size, J = function, E = type, Z = basic board. Thus the first three letters of all timing boards will be MJE and those of Y deflection boards MRG or MRH. For each category a basic board is produced which carries all the transistors and a majority of the electronic components; at this stage the board is identified by using Z

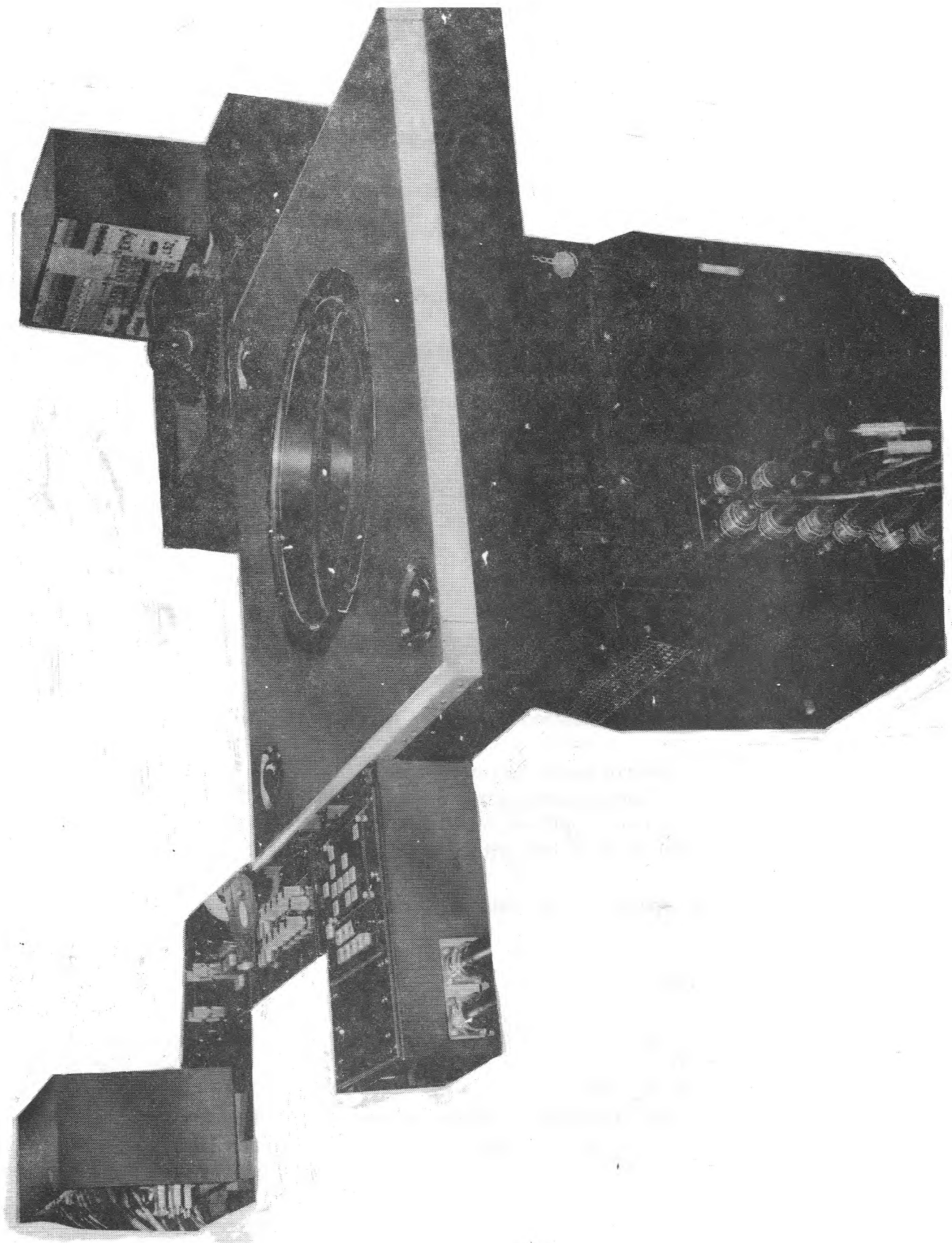


Fig.2

Mr. 5 Autonomous display (0111)

as its fourth letter. The board is then tailored by the fitting of links and particular components, to form part of a specific display. Depending upon the parameters required for that particular presentation, the appropriate values are then allocated to those components for which no values are shown on the circuit diagram. After a board has been tailored in this manner, its final identification letter is changed from Z to some other letter. All printed wiring boards carry a type number for identification.

13. In general a p. p. i. display will require 'M' boards as follows:-

- (1) Timing board.
- (2) Two identical deflection boards.
- (3) Video board.

In addition up to five 'N' boards may be fitted to provide symbol multiplexing if required.

14. A h. r. i. display will, in general, require 'M' boards as follows:-

- (1) Timing board.
- (2) X and Y deflection boards of different types.
- (3) Video board.

In addition, up to five 'N' boards, housed in a Gate Generator Unit, may be fitted.

CHAPTER 2

SYSTEM PRINCIPLES

LIST OF CONTENTS

	Para.
<u>SYSTEM PRINCIPLES</u>	
INTRODUCTION	1
PPI DISPLAY (RADIUS SCAN)	
Basic requirements	3
Practical arrangements	8
Scan control voltage demodulators	13
PPI DISPLAY (DIAMETER SCAN)	
Practical arrangements	23
Scan control voltage demodulators	24
HRI DISPLAY	
Basic requirements	27
Practical arrangements	30
SYSTEM TIMING	
Introduction	32
Timebase generators	34
Synthetic markers	36
THE INTERSCAN SYSTEM	
Introduction	37
Interscan timing	40
Range and bearing marker	41
THE FASTSCAN SYSTEM	
Introduction	50
Fastscan timing	53
Fastscan deflection waveforms	55
ELECTRONIC SWITCHES AND GATE CIRCUITS	
Electronic switches	60
Gate circuits	62
Switch waveforms	64
Gate waveforms	65
Inhibitors	67
BRILLIANCE, VIDEO AND CALIBRATION CIRCUITS	
Brilliance circuits	68
Video circuits	71
Calibration circuits	72

LIST OF ILLUSTRATIONS

				Fig.
Principles of radius scan production	1
Principles of diameter scan production	2
Principles of h. r. i. scan production	3
Principles of interscan production	4
Principles of fastscan production	5

SYSTEM PRINCIPLES

INTRODUCTION

1. The Mk.5 Autonomous Display (Plessey Type TDS5) system consists of a series of radar displays designed to cover a wide range of user requirements. Three basic types of presentation are available: a normal p.p.i. display for use with a single radar, a cartwheel scan consisting of two diametrically opposed radial scans for use with back-to-back aerial systems and a height/range display for use with nodding-type heightfinder radars.

2. All systems are based on interscan techniques, which use fixed deflection coils to produce both the basic scan and the markers. In the following paragraphs the various techniques of the interscan system are explained in general terms.

PPI DISPLAY (RADIUS SCAN)

Basic requirements

3. The four deflection coils are symmetrically arranged about the neck of the c.r.t. in such a position that corresponding currents produce deflection to the north, south, east and west respectively. If equal current are passed through all four coils, the fields due to opposed pairs will cancel and the spot will remain stationary in a central position.

4. Push-pull deflection in a northerly direction is obtained by increasing the current in the north coil and reducing the current in the south by a corresponding amount. For simplicity of explanation, the currents in the south and west coils can be neglected on the assumption that changes in current in them will be equal and opposite to those of the north and east coils, and that their presence merely serves to double the deflection for a given change in current.

5. Linear traces in a northward or eastward direction can be obtained by a linear increase of the current in the appropriate coil. To obtain a linear trace in a north-easterly direction equal linearly rising currents in both the

north and east coils are required, but in this case the rate of increase must be less than it was before if the actual rate of scan is to remain the same. By varying the rates of rise of the currents applied to the north and east coils, the spot can be made to scan on any bearing between 0° and 90° . If rates of fall as well as rates of rise are admitted, this can be extended to bearings between 0 and 360° . If the resultant spot velocity is to remain the same on all bearings, a certain relationship must be maintained between the two deflection rates. If the trace is to rotate at a constant angular velocity, the component velocities northwards and eastwards must vary to a definite law.

6. A velocity V in a direction making an angle θ with the N-S line (i.e. at a bearing of θ°) can be resolved into component velocities of $V\cos\theta$ in a northerly direction and $V\sin\theta$ in an easterly direction. Allowing for changes of sign this applies over the whole 360° . Conversely a northwards velocity of $V\cos\theta$ will combine with an eastwards velocity of $V\sin\theta$ to give a velocity V on a bearing of θ° . It therefore follows that the law to be followed by the component spot velocities (paragraph 5) and consequently the current in the coils, is one of direct proportion to $\cos\theta$ in the case of the north coil and $\sin\theta$ in the case of the east coil, where θ is the bearing of the rotating aerial to which the trace is synchronised.

7. Thus the current waveform required for the north coil is a linear sawtooth, modulated so that the rate of rise of each successive excursion is proportional to the cosine of the aerial bearing; that required for the east coil is a linear sawtooth with its rate of rise proportional to the sine of the aerial bearing. The currents in the south and west coils must of course have their rates of change modulated by the minus cosine and minus sine respectively.

Practical arrangements

8. To modulate a sawtooth waveform in accordance with the sine and cosine of the aerial bearing, it is first necessary to obtain a pair of control voltages whose amplitudes vary according to these quantities. These voltages are generated by means of a synchro-resolver and a pair of demodulator circuits.

9. The rotor of the synchro is turned in 1:1 synchronism with the radar aerial and fed with an a.c. supply with a frequency in the range of 250Hz to 1kHz. The two stators of the synchro, which are arranged at right angles to each other, resolve the rotor input into two components, one amplitude-modulated according to the sine and the other according to the cosine of the angular position of the rotor. Outputs are taken from the stators of the synchro and separately demodulated to give a pair of voltages which are proportional to sine and cosine of the aerial bearing and therefore rise and fall in a sinu-

soidal manner at a frequency of one cycle per aerial revolution with a phase difference of 90° between them (Fig.1). These voltages are known as scan control voltages.

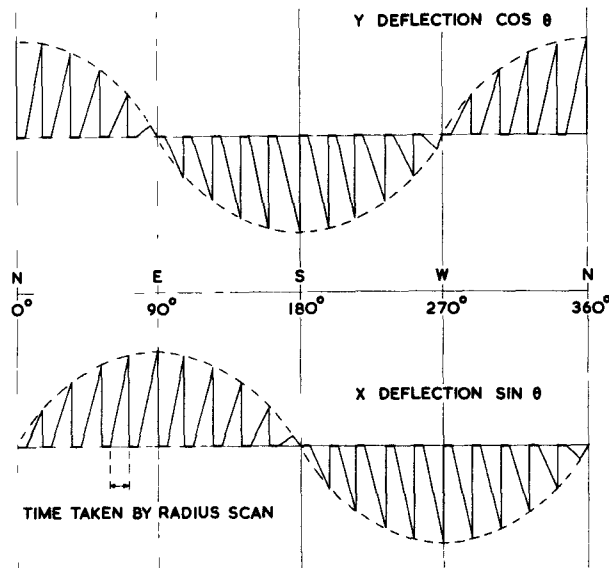


Fig.1 Principles of radius scan production

10. Each of the scan control voltages is fed to an integrator circuit which is called a timebase generator. The timebase generator is capable of being switched so that it responds only to the scan control voltage for a certain period of time in each radar repetition period, this period being arranged to correspond to the required scan duration. During this period the output of the timebase generator rises or falls from a predetermined level at a rate proportional to the scan control voltage, and in a direction determined by the polarity of this voltage. Two such timebase generators are employed in the system, one receiving the sine scan control voltage and the other the cosine scan control voltage. The outputs from these circuits provide the X and Y deflection levels for the c.r.t. The output voltage waveforms from these circuits correspond exactly to the current waveforms required for the north and east deflection coils.

11. Since a push-pull deflection system is employed, the output from each timebase generator is fed to a paraphase amplifier which provides the necessary opposed pair of waveforms for each deflection axis. Each paraphase amplifier operates in conjunction with a pair of deflector coil drive amplifiers which transform the voltage waveforms into current waveforms through the coils.

12. When a linear sawtooth current flows through the inductance of a deflection coil, it gives rise to a stepped voltage waveform across the coil with a step-amplitude proportional to the rate of rise of current. Since the deflector coils used are sectionalized and each section is fitted with parallel

damping resistors, the stepped voltage waveform will produce a stepped current waveform in the resistors. Unless arrangements are made to provide the additional current thus required, distortion of the output waveform will result. The additional current is provided by the addition of a suitable step voltage to the output of the timebase generators which will in turn provide a stepped voltage at the input of the coil drive amplifiers, thus providing the additional current. The step is normally produced by including suitable components in the input circuit of the paraphase amplifier.

Scan control voltage demodulators

13. The type of presentation is largely determined by the scan control voltages to the timebase circuits.
14. The demodulator circuits used in this system are of the 'sample-and-store' type, i.e. they are capable of two modes of operation. In the 'sample' mode the output of the demodulator assumes a level proportional to the input and stores this level during the 'store' mode. In practice the sampling period is of very short duration, usually not more than $100\mu\text{s}$.
15. The switching of the demodulator circuits between the two modes of operation is effected by reversing the polarity of a level applied to a gate control input.
16. With a p.p.i. display (radius scan) the switching is effected by a train of positive-going short-duration pulses referred to as the sampler gate waveform. Each positive pulse switches the circuit to the 'sample' mode. The timing of the positive-going pulses is made to coincide with the positive peaks of the carrier sine wave fed to the aerial synchro resolver. Under these conditions the output of the demodulator circuit will be a stepped waveform in which the level of the consecutive steps corresponds to the levels of the consecutive peaks of the input modulated carrier waveform.
17. Since the demodulator circuit, when in the 'store' mode, is in fact an integrator circuit with a zero rate control input, it is possible to cause the output to vary by varying the rate control input. This technique is in fact used to produce a demodulator output more closely resembling the modulation envelope. If a correctly chosen rate control voltage is applied during the 'store' mode, the output can be caused to move towards the level it should have during the next sampling period.
18. To achieve an ideal sine wave output, i.e. to achieve ideal rate prediction, it is necessary to apply the complement of the demodulator output to the rate prediction input.

19. In the case of the sine demodulator the required rate prediction voltage will be a cosine waveform and this can be obtained by using the output of the cosine demodulator. In the case of the cosine demodulator the required voltage is a minus sine waveform and this can be obtained by inverting the output of the sine demodulator.

20. Thus, the resulting configuration will consist of an integrator (the sine demodulator) feeding an inverter circuit, the output of which is fed to a second integrator (the cosine demodulator). The loop is completed by feeding the output of the cosine demodulator to the rate control input of the sine demodulator. These conditions of course obtain only when the demodulator circuits are in the 'store' mode. If the loop gain around this circuit is adjusted to near unity, the combination will self-oscillate and the outputs from the two integrator circuits will be sine waves with a phase difference of 90° .

21. Thus, the demodulation system for a p.p.i. display may be considered as an oscillator which produces one cycle of output per aerial rotation, the output level of which is amplitude-corrected to the modulation envelope at every positive peak of the carrier waveform by switching the circuit to the 'sample' mode.

PPI DISPLAY (DIAMETER SCAN)

22. The cartwheel or diameter scan is used when two radars are used with their aerials mounted back-to-back on a common turning unit. In this type of presentation, radial traces are painted alternately on opposed bearings, giving the effect of a rotating diameter instead of a radius (Fig.2). The video from each aerial is painted on its corresponding trace.

Practical arrangements

23. The arrangements used in the production of a cartwheel display correspond to those described for a p.p.i. display (paragraphs 8 to 12).

Scan control voltage demodulators

24. To produce the scan control voltages for the cartwheel or diameter scan the same demodulator circuits are used as for the radius scan (paragraphs 13 to 20), but in this application no prediction is used.

25. The repetition rate of the sampler pulses applied to the gate input of the demodulator circuits is arranged to be twice the carrier frequency, so that sampling occurs on both the positive and negative peaks of the carrier waveform. Thus, the outputs from the demodulators will be alternately positive and negative for the periods between sampler pulses, the positive levels being proportional to the positive peaks of the modulated input, and the negative levels pro

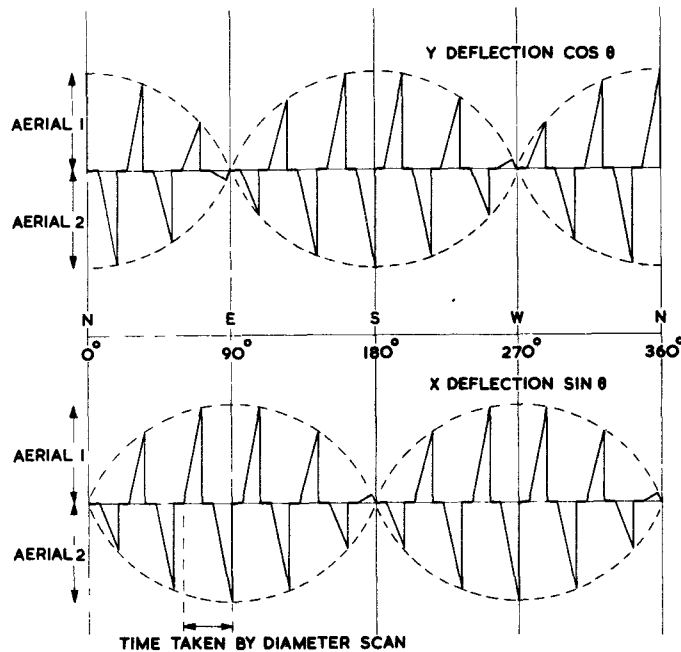


Fig.2 Principles of diameter scan production

26. When these levels are applied to the timebase generators, the combined deflection waveforms produced will cause successive radius scans to be painted 180° apart on the c.r.t.

HRI DISPLAY

Basic requirements

27. The height/range indicator (h.r.i.) provides a display which covers the vertical section swept by the beam of a nodding-type heightfinder radar.

28. The simplest method of producing this type of display would be to gear a synchro resolver to the elevation sweep of the aerial and feed the rotor with a carrier sine wave in the same way as for a p.p.i.-type display. The outputs from the stators could then be demodulated in the normal way and the resulting scan control voltages used to control the timebase generator. The appearance of the trace on the c.r.t. would then resemble a sector of a p.p.i. trace, the angle swept corresponding to the angle through which the heightfinder aerial is sweeping. In this type of presentation the origin of the trace is off-centred to the lower left-hand corner of the c.r.t.

29. The type of display thus produced would not be very satisfactory for a number of reasons. The angle swept by the trace on the c.r.t. would be exactly the same as that swept by the radar aerial, and since this is usually between 20° and 30° only, the full area of the c.r.t. would not be used. It is also desirable in a height/range display that facilities should exist for expanding the range axis without expanding the height axis; this is not possible with the simple display described. A further desirable feature is that slant range should be measureable from left to right across the c.r.t. and that points of equal slant range should occur along the same vertical line.

Practical arrangements

30. To satisfy the above requirements a distorted type of display is used. In this display the left-to-right component of the c.r.t. spot velocity is maintained constant and the vertical component is made proportional to the sine of the angle of elevation of the heightfinder aerial. These results are obtained by feeding a constant value of scan control voltage to the X timebase generator, and a voltage proportional to the sine of the aerial elevation to the Y timebase generator (Fig. 3). As will be seen, one aerial demodulator only is required.

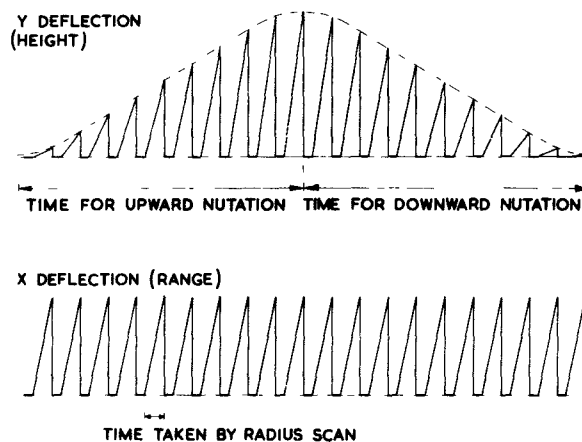


Fig. 3 Principles of h.r.i. scan production

31. With this type of display an angular expansion of two to four times is obtained; on the longest range scale an elevation sweep of approximately 30° covers about 80° on the c.r.t. Slant range is measureable directly from left to right across the c.r.t. and height is measureable vertically from the base line. This type of display also enables the range scale to be varied while the height scale is maintained constant.

SYSTEM TIMING

Introduction

32. In the Autonomous Display system the period of time between two successive radar trigger pulses is divided into two discrete time periods. The first of these, the 'scan regime', is the period of time during which the spot is actually painting on the c.r.t. and the second, the 'shift regime', is a period of preparation for the 'scan regime' in which the deflection currents may settle down to the value required to commence the next scan. These periods and others within the system are initiated and terminated by a series of timing 'pulses'. (The word pulse is used to define either a short-duration pulse or the transient edge of a rectangular waveform.) The scan regime is initiated by the radar trigger pulse and terminated by either the scan-end pulse or the mainscan-end pulse, according to whether an interscan or fastscan system is being used (paragraph 36). The 'shift regime' is initiated by the scan-end pulse and terminated by the following radar trigger pulse.

33. The radar repetition period is the time interval between two radar trigger pulses, but it is more convenient to consider a display repetition period which commences with the shift regime, since each display period will then consist of a period of preparation (shift regime) followed by the actual scanning period (scan regime).

Timebase generators

34. The timebase generators used in the system have three inputs referred to as the 'rate-control' input, the 'shift' input and the 'gate' input, and have one output. The circuit is capable of two modes of operation: the 'shift' mode and the 'scan' mode. In the 'shift' mode the level at the output is proportional to the level being applied to the shift input; in the 'scan' mode the level at the output changes from the level it has during the 'shift' mode at a rate proportional to the scan control voltage (and in a direction determined by its polarity). The mode in which the timebase generator operates is determined by the polarity of the voltage applied to the 'gate' input; if this is negative, the scan mode is assumed and if positive, the 'shift' mode. The gate level normally moves between the levels of -5V and +5V, and this waveform is referred to as the timebase gate waveform.

35. It will be seen from the above that during the 'shift' mode, the spot on the c.r.t. will remain stationary and by suitable adjustment of the levels applied to the shift, inputs can be made to occupy any required position on the c.r.t. screen.

Synthetic markers

36. To obtain synthetic markers on the display, two alternative systems are available; these are referred to as the 'interscan' system and the 'fastscan' system, and they are described separately in the following paragraphs.

THE INTERSCAN SYSTEM

Introduction

37. The interscan system is used when the time required to paint the marker is in excess of approximately $250\mu\text{s}$ and is in fact comparable with the time required to paint the normal p.p.i. trace. These conditions obtain when a measuring marker capable of measuring up to the full range of the system is required. When using the interscan system the normal traces displaying the radar video etc. are referred to as mainscans and the markers as interscans. Interscan markers usually take the form of straight lines and are used for measuring range and relative bearing, for displaying the outputs of c.r.d.f. stations and indicating runway approach lines, etc.

38. To produce an interscan marker, the mainscan scan control and shift voltages are disconnected every so often from the timebase generators for the whole of one display repetition period. In their place are connected suitable scan control and shift voltages for the required marker. The origin of the marker can be placed in any required position on the c.r.t. by applying suitable interscan shift voltages (Fig.4). The bearing of the marker can be predetermined by applying suitably proportional scan control voltages.

39. To display a marker without apparent flicker it is necessary to paint it not less than 16 times per second, i.e. it is necessary to disconnect the mainscan control voltages and replace them with the interscan control voltages at least 16 times per second. Thus, with a radar p.r.f. of 480p.p.s. it would be necessary to replace one mainscan in every 30 with the interscan.

Interscan timing

40. To time the interscan periods correctly with respect to the mainscan periods, it is necessary to produce an 'interscan start' pulse. This pulse is coincident in time with the scan-end pulse and occurs when it is desired to switch the system to interscan conditions. The pulse is produced by counting down scan-end pulses.

Range and bearing marker

41. A particular form of marker often provided takes the form of a range and bearing line. This is a straight-line marker, the length of which may be accurately adjusted by means of a calibrated range control, and the

bearing about its origin accurately set by means of a calibrated bearing control. In addition, the origin of the line may be made either to coincide with the origin of the p.p.i. picture or to be off-centred to any part of the c.r.t. screen.

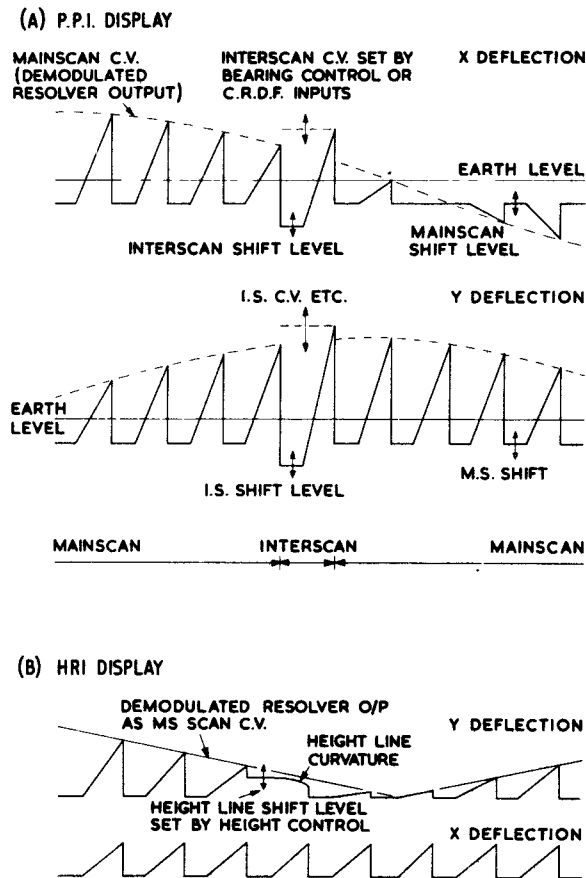


Fig.4 Principles of interscan production

42. To ensure the bearing accuracy of such a marker, a precision sine/cosine potentiometer is used to derive the scan control voltages. The spindle of this potentiometer is geared to an operator's bearing control and the sine and cosine voltages are taken from the appropriate sliders.

43. Measurement of range is achieved by making the length of the marker line variable. In practice the c.r.t. spot is caused to scan a full-length line but is brightened only for a period of time determined by the setting of the range control.

44. The brightened length of marker line is determined by an interscan knock-off pulse. This pulse is generated during interscan periods only; its timing is determined by the setting of the range control.

45. When an interscan is used to provide a c.r.d.f. line, the origin of the line is set to coincide with the geographical location of the c.r.d.f. station and the bearing is determined by the positional information derived by the c.r.d.f. equipment. In practice, scan control voltages are derived from the bearing outputs of the station.

46. In the case of runway markers, facilities are provided to position the marker in any one of a number of preset positions. These positions normally correspond to the number of runways available on the airfield and the one in use is indicated by the marker.

47. On the h.r.i. display the interscan marker takes the form of a height line. This marker is a horizontal line painted from left to right across the c.r.t. The line is capable of movement in a vertical plane only and this movement is controlled by the height/range operator from a calibrated height potentiometer, the output from this potentiometer being fed as a shift voltage to the Y timebase generator during interscan periods.

48. The height line can be arranged to have a downward curvature of increasing magnitude towards its right-hand end, to compensate for the earth's curvature.

49. To assist the h.r.i. operator in locating the required target, the length of the height line is controlled from an associated p.p.i. display. Setting the range control on the p.p.i. to the range of a given target adjusts the length of the height line to correspond to that range.

THE FASTSCAN SYSTEM

Introduction

50. The fastscan system provides an alternative method of producing synthetic markers on the c.r.t. It is normally used when the number of markers required is such that if the interscan system were used, an excessive number of mainscaans would need to be suppressed, thus resulting in deterioration of definition and resolution. The fastscan system may also be used when the markers are such that only a short period of time, i.e. up to $250\mu\text{s}$, is required to paint them.

51. The type of marker produced by the fastscan system includes short vectors and various characteristically shaped symbols, i.e. circles, ellipses, squares, triangles, etc.

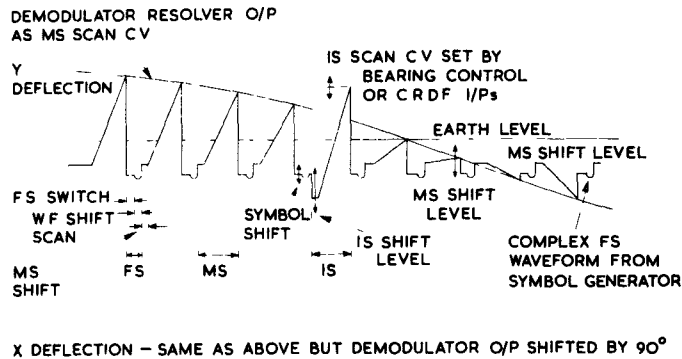


Fig.5 Principles of fastscan production

52. The essential difference between the interscan and fastscan systems is that an interscan marker is painted in a period of time made available by suppressing a mainscan, but a fastscan marker is painted in the interval between the end of one mainscan and the commencement of the next. The deflection waveforms are shown in Fig.5; these waveforms apply to a system with a continuous fastscan and an intermittent interscan.

Fastscan timing

53. For the purpose of a fastscan system a further sub-division of the radar repetition is required in addition to that already defined. The repetition period is first divided into two parts referred to as the mainscan (MS) period and the fastscan (FS) period. Each of these periods is then further divided into a shift regime and a scan regime. Thus a complete display period will comprise a mainscan shift regime, a mainscan scan regime, a fastscan shift regime and a fastscan scan regime. Since the radar trigger times the start of the mainscan scan regime, the mainscan shift regime will occur at the end of the radar repetition period.

54. The timing pulses for a fastscan system comprise the radar trigger, the MS end pulse, the FS start pulse and the FS end pulse. The mainscan scan regime occurs between the radar trigger and the MS end pulse, the fastscan shift regime between the MS end pulse and the FS start pulse, the FS scan regime between the FS start pulse and the FS end pulse and the mainscan shift regime between the FS end pulse and the next radar trigger.

Fastscan deflection waveforms

55. During the fastscan period the action of the mainscan timebase

generators are inhibited, and the fastscan shift and deflection waveforms are used in their place. The fastscan markers are positioned by means of a pair of fastscan shift voltages which are fed to the deflection amplifiers in the appropriate periods.

56. If the fastscan markers are symbol shapes, a symbol generator is switched on for the duration of the fastscan scan regime and the outputs, comprising the X and Y symbol deflection waveforms, are fed to the deflection amplifiers. The symbol generator is normally capable of producing up to four different shapes of symbol and the shape required is determined by feeding a selector signal to one of four selector inputs.

57. It is possible to have any number of symbols of up to four on the display, each symbol being positioned independently of the others. If more than one symbol is required, they are painted sequentially in succeeding fastscan periods.

58. The requirement that each symbol must be painted at least 16 times per second to prevent apparent flicker applies equally to fastscan symbols.

59. Positioning voltages for the symbols may be either generated within the display, or fed in from a remote point.

ELECTRONIC SWITCHES AND GATE CIRCUITS

Electronic switches

60. In order to connect scan control voltages to timebase generators, shift and deflection voltages to deflection amplifiers etc., for the required periods, use is made of electronic switches. These are fast-acting devices consisting of a number of identical elements. Each such element has an input terminal, an output terminal and a switching terminal. When a level of -5V is applied to the switching terminal, the level applied to the input is made available at the output terminal. When the switching level is changed to +5V, the device becomes an open circuit between the input and output terminals.

61. To produce a multi-way switch, a number of these elements have their output terminals commoned and the various levels to be switched are applied to the separate input terminals. To obtain a particular output, a level of -5V would be applied to the required element and +5V to all other elements. The action of the switch, therefore, may be programmed by varying the levels applied to the switching circuits.

Gate circuits

62. Certain of the circuits used in the system are capable of two distinct modes of operation and selection of the required mode is performed by means

of a gate circuit. Examples of this type of circuit are the timebase generators and the scan control voltage demodulator circuits. These circuits operate on the polarity of the level applied to a gate terminal or terminals; thus a positive level at a particular terminal causes one mode of operation and a negative level the alternative mode. The levels normally used are either -5V and +5V or -2V and +2V.

63. In addition to the above type of gate circuit, logical AND and OR gates are also used.

Switch waveforms

64. The electronic switches used in the system are operated by a series of standard rectangular waveforms referred to as switch waveforms. The waveforms alternate between the levels of +5V and -5V. Switch waveforms are normally defined by their function; in fact a mainscan switch waveform is at a level of -5V for the whole of the mainscan period and at a level of +5V at all other times. Switch waveforms are normally used to switch the system between MS and IS or MS and FS conditions.

Gate waveforms

65. Gate waveforms are somewhat similar to switch waveforms and are used to control gate circuits. They consist of rectangular waveforms moving between levels of either $\pm 5V$ or $\pm 2V$. Gate waveforms are usually used to define a sub-division of a period, i.e. a scan regime or a shift regime. A gate waveform is usually defined by its function; thus a timebase or scan gate would switch the timebase generator circuits to the scan mode of operation.

66.1 A special gate waveform (as regards timing) is the aerial sampler gate waveform which switches the scan control voltage demodulators to the 'sample' mode of operation.

Inhibitors

67. The inhibitor is a device, usually a diode, fitted to a circuit to prevent it operating under certain conditions. It is normally operated by a switch-type waveform and renders the circuit inoperative so long as this waveform is negative.

BRILLIANCE, VIDEO AND CALIBRATION CIRCUITS

Brilliance circuits

68. The function of the brilliance circuits is to provide individual control of the various elements of the c.r.t. picture. The circuits comprise a gated brilliance amplifier with a switched input.

69. The inputs to the brilliance amplifier comprise the mainscan brilliance control voltage and either the interscan or the fastscan control voltage. These voltages are obtained from the sliders of the operator's controls. The control voltages are fed to the amplifier via a two-way single-pole electronic switch, operated by either the MS/IS or MS/FS switch waveforms.

70. The gating circuit of the amplifier is controlled by a brilliance gate waveform which ensures that the c.r.t. is brightened only during the required periods. This gate waveform is generated from the various pulses previously mentioned. The output from the brilliance amplifier is fed to the c.r.t. grid.

Video circuits

71. The video circuits comprise a video amplifier with up to six input channels. Each input channel may be switched on or off independently as required and has independent gain control facilities. The output from the video amplifier is fed to the c.r.t. cathode.

Calibration circuits

72. The system incorporates a built-in calibrator which is capable of producing two trains of calibration pulses at differing intervals, e.g. 5-mile and 10-mile intervals. The actual calibration intervals vary between applications.

73. The calibrator circuits are controlled by a calibration gate waveform generated from the basic timing pulses and generates calibration markers during the mainscan scan regime only.

CHAPTER 3

GENERAL DESCRIPTION

LIST OF CONTENTS

	Para.
MECHANICAL DESCRIPTION OF 12in VIEWING UNIT	
Introduction	1
Main assembly	4
Power unit	8
EHT power unit	11
Deflection coil drive amplifier assembly	13
Board box and printed wiring boards (4 M-type boards)	15
Control panel	20
Character drive unit type 12500	24
Junction unit type 12792/A	25
Cathode ray tube	26
Deflection coil	27
Cooling system	28
Space heaters	32
Desiccator	33
Overload cut-outs	34
MECHANICAL DESCRIPTION OF 21in VIEWING UNIT	
Introduction	35
Main assembly	38
Power unit	41
EHT power unit	42
Deflection coil drive amplifier assembly	44
Board box and printed wiring boards	46
Control panel (Types 11057, 11066 and 11060)	47
Control panel type 12701	48
Character drive unit	49
Junction unit type 12795/A	50
Cathode ray tube assembly	53
Focus and deflection coil assemblies	56
Cooling system	58
Space heaters	62
ELECTRICAL DESCRIPTION OF 12in AND 21in VIEWING UNITS	
Outline of operation (Fig. 5)	63
Viewing unit sub-assemblies	67
Power supply circuits	69
The temperature control system	77

	Para.
The printed wiring boards	80
Interscan timing board (MJE)	83
Category selection board (MJS)	92
Deflection boards MRG, MRH and MRK	97
Video board (MFD)	117
Deflection drive amplifiers types 12502 and 12505	123
Character drive unit type 12500	126
Viewing unit mount	130
Viewing unit control panel	131
Operator's control panel	137
Radar display control panel	138

LIST OF ILLUSTRATIONS

	Fig.
12in viewing unit: front view	1
12in viewing unit: top view	2
12in viewing unit: rear view	3
12in viewing unit: right-hand view	4
21in viewing unit:	5
21in viewing unit: (covers removed)	6
21in viewing unit: detail of interior	7
21in viewing unit: detail of interior	8
Mk. 5 autonomous display: simplified block diagram	9

MECHANICAL DESCRIPTION OF 12in VIEWING UNIT

INTRODUCTION

1. The display unit consists of a viewing unit fitted to a wedge-shaped mount which also carries the operator's control panel; the viewing unit and mount are located on a floor-standing console. The viewing unit houses the cathode ray tube and the majority of the electronic circuits. Fitted to the rear of the viewing unit is a removable junction unit which provides all connections between the viewing unit and the mount and console units.

2. The viewing unit consists of a main assembly which supports and contains various sub-units. The sub-units can be removed for servicing by disconnecting the appropriate terminal strips and releasing the securing bolts. It is not advised that the power units and deflection drive amplifier assemblies be operated out of the viewing unit out of contact with their cold plates unless adequate provision is made for their cooling.

3. In the following paragraphs the main viewing unit assembly will be described first, followed by the various sub-assemblies.

MAIN ASSEMBLY

4. The viewing unit is constructed on a front casting and a base plate to which a framework is attached to support the sub-assemblies. The front panel of fibreglass is

attached to the casting. The tube mount and the implosion screen are secured to the main casting, offset to the left of the front panel; the viewing unit control panel is secured to the rear of the casting, on the right-hand side of the tube. The controls are accessible through two openings in the front panel. The OFF/STANDBY/ON switch and the range selector push-buttons are always exposed to view; the rest of the controls are concealed by a hinged door. The implosion screen covering the c. r. t. face is engraved with a compass rose and edge-lit by four lamps (the cursor illumination lamps).

5. The air duct of rectangular cross-section is fitted to the base plate under the neck of the c. r. t. This duct is closed at the front by an angled plate and an air inlet is provided at this end through the base plate. The space between the front of the duct and the front panel is occupied by a Mu-metal screen surrounding the tube. The Mu-metal screen is not a supporting member and is not under stress. The chassis is divided into three sections by two vertical panels fitted one on each side of the air duct, and held in position at the top by two shaped bars secured to the front casting and a bracing member at the rear of the assembly.

6. The viewing unit is fitted with a fibreglass case, located in position by four dowel studs and locked on by two spring-loaded bolts operated by a handle at the front of the unit. A top cover is fitted to this case and secured by four Dzus fasteners. The monitoring points and test switches required for servicing are accessible with this top cover removed. The viewing unit is removed from the case by pulling forward the locking handle on the underside of the unit at the front; the case remains attached to the table top mount.

7. After the case has been fitted, the junction pack is fitted to the back of the viewing unit and secured by a single quick-release screw.

POWER UNIT (FIG. 4)

8. The power unit is constructed on a back plate which, having considerable mass, acts as a heat sink. The mains transformer, the high current rectifiers, the series regulator transistors, smoothing chokes, large capacitors and a high temperature cut-out are mounted directly onto the back plate. A framework attached to the back plate supports two printed circuit boards, a capacitor, four overload cut-outs and six terminal strips.

9. The printed wiring boards carry all the small electronic components of the power unit. Certain transistors are wired to the printed boards and fitted in clips attached to the back plate. These clips are designed to ensure that the transistors are in good thermal contact with the back plate.

10. The power unit is attached to the power unit cold plate by four captive screws and two loose screws. External connections to the power unit are made via six terminal strips. Whilst the power unit cableform is long enough to permit the unit to be operated outside the viewing unit, it is unwise to operate the unit for long periods detached from its cold plate.

EHT POWER UNIT (FIG. 4)

11. The e. h. t. unit is assembled on a heavy back plate which acts as a heat sink for the two power transistors used in the unit. The two power transistors and a printed resistor are secured to the back plate. The e. h. t. transformer, high voltage rectifiers and e. h. t. smoothing circuit are contained in a sealed can which is secured to the back plate. Certain small components are mounted on a printed wiring board and this, together with the remaining components, is mounted on a small frame fitted between the top of the e. h. t. can and the back plate. Connections to the unit are made via a terminal strip and the e. h. t. voltage output is taken via a special high voltage lead.

12. The e. h. t. unit is fitted to the same cold plate as the power unit and is held in position by three captive screws.

DEFLECTION-COIL DRIVE-AMPLIFIER ASSEMBLY (FIG. 2)

13. This assembly comprises a metal transistor mounting block and a printed wiring board, supported on this block but spaced from it by two brackets. The two output transistors of each amplifier and eight printed resistors are fitted to the mounting block, which has considerable mass and acts as a heat sink. The other electronic components are fitted to the printed wiring board.

14. The complete assembly is fitted to a cold plate mounted over the neck of the c. r. t. and held in position by six screws. Connections to the assembly are made via two terminal strips.

BOARD BOX AND PRINTED WIRING BOARDS (4 M-TYPE BOARDS)

15. The left-hand chassis section (viewed from the front) is occupied by the board box assembly in which the plug-in printed wiring boards are fitted (Fig. 4). The board box is open at the top and printed circuit edge connections are fitted to the bottom plate (two for each board). Each board is secured in position by two clamps operated by turnscrews at the top of the unit. The boards are cooled by a light mineral oil which circulates through channels in two sides of the box. This section of the box is known as the board box cold plate.

16. The base of the board box containing the printed circuit edge connectors is a part of the 'connector plate and board connector assembly' (Fig. 4). The three multi-way plugs, through which the external connections are made, are mounted flush with

the rear of the viewing unit (Fig. 3). The complete assembly can be removed for servicing by disconnecting four terminal strips and removing eight screws, without disconnecting the board box cold plate, which remains in position.

17. The printed wiring boards are made of fibreglass and carry printed wiring on both sides of the board. Components are fitted to one side of the board only. Connections from the circuitry on the board are taken to a series of gold-plated edge connectors on the bottom edge of the board. These connectors mate with sockets fitted to a connector plate at the bottom of the board box. The transistors on the board are fitted in metal clamps which make contact with the board box cold plate.

18. The boards are fitted vertically in the board box and held in position by a pair of clamps on the top corner of each board.

19. Each board carries a number of monitor points, test switches and preset potentiometers mounted on a strip attached to the top edge of the board. This strip also carries a handle to facilitate easy removal of the board. The test and setting-up facilities on the boards are accessible via a removable panel in the top of the viewing unit cover.

CONTROL PANEL (FIG. 1)

20. The viewing unit control panel is constructed on a metal front plate and a framework attached to this plate supports two components mounting plates. All controls are mounted on the front plate. An engraved perspex panel is fitted to the front.

21. The component panels carry relays, a thermal delay switch, a thermal cut-out and various smaller components.

22. The viewing unit control panel is fitted to the rear face of the viewing unit front casting and secured by four captive screws. The release and reset buttons of the thermal cut-out are accessible through the removable top panel of the viewing unit cover.

23. The front of the control panel is covered by a hinged fibreglass cover on the front of the viewing unit.

CHARACTER DRIVE UNIT TYPE 12500

24. This unit contains two identical push-pull amplifiers, one for the X deflection and one for the Y deflection. It is engineered as a rectangular box (approx. 2.75in x 3.5in x 6in) which is secured within the viewing unit by means of four bolts. The major part of the circuitry housed in this unit is carried on two printed circuit boards.

JUNCTION UNIT TYPE 12792/A

25. The junction unit interconnects between various groups of circuit, within the viewing unit, between the display and external items of equipment and between the

viewing unit and radar control panel. The unit has two fixed 50-way sockets and one fixed 14-way socket which mate with corresponding plugs on the rear of the 12in labelled plan radar display. External connections to the unit are achieved by a total of nine connectors, all easily removable, located at the rear of this assembly.

CATHODE RAY TUBE

26. The centre section of the chassis contains the neck of the 12in c. r. t. The deflection coil assembly, which also contains the focusing magnets, is fitted round the neck of the c. r. t. and secured to the top of the air duct. The heat sink for the deflection coil drive assembly is secured to the two vertical panels above the deflection coils and forms a horizontal platform for the amplifier assembly. The coolant circulates through a channel in this heat sink.

DEFLECTION COIL

27. The deflection coil is encapsulated in epoxy resin and the connections are made by taper pin sockets on a terminal strip. The focus magnet is a circular permanent magnet mounted directly behind the deflection coil. Focusing is achieved by adjusting the position of the magnet along the axis of the tube by means of an annular slot. Two beam-centring magnets are fitted to the rear of the deflection coil assembly, each consisting of a ring with three lugs. The combined field strength can be adjusted by rotating one magnet with respect to the other, and the direction in which the combined field lies can be set by rotating both magnets together. These magnets and the focus magnet act together to centre and focus the spot with zero deflection field.

COOLING SYSTEM

28. The coolant is a light mineral oil and is circulated through the cold plates and heat exchangers by a small electric pump operated from the mains supply (Fig. 4). The pump operates continuously as long as the display is at STANDBY or ON. The coolant flows from the pump through the board box cold plate, the power unit cold plate, the deflection coil drive amplifiers heat sink, the heat exchanger and back to the pump.

29. The heat absorbed by the coolant is extracted by the heat exchanger and transferred to the cooling air drawn over the heat exchanger by the cooling fan. The heat exchanger is a coiled tube, finned inside and out (Fig. 3). The coolant flows over the inner fins and the cooling air is drawn over the outer fins, through an air intake at the front underside of the unit and exhausted through two vents at the rear. The cooling air is isolated from the interior of the viewing unit.

30. The mains supply to the cooling fan passes through a thermostat fitted to the outlet block of the heat exchanger. This thermostat opens if its temperature falls to 0°C and stops the cooling fan to prevent overcooling in conditions of low ambient temperature. A second thermostat opens if its temperature rises to 85°C and interrupts the mains supply to the power unit, thus switching off the display. This temperature will be reached only if the cooling system fails or a fault develops in the deflection coil drive amplifier assembly.

31. The right-hand of the two vertical panels is the power unit's cold plate and contains a channel through which the coolant circulates. The power unit, the e. h. t. unit and the symbol multiplexer sub-unit (when incorporated) are secured to this cold plate on the right-hand side of the viewing unit (Fig. 4). The pump unit used to circulate the cooling oil is secured to the base plate in this section, between the viewing unit control panel and the e. h. t. unit (Fig. 2).

SPACE HEATERS

32. Two space heaters are fitted to the viewing unit base plate; one under the power unit and one under the board box. When the display is switched off at the viewing unit control panel, these heaters are connected in series across the main supply.

DESICCATOR

33. The viewing unit case is designed to be airtight with the cover in position. A desiccator is fitted to the Mu-metal screen of the c. r. t. behind the front casting to absorb any moisture sealed in the unit. The desiccant will change colour from blue to pink as its moisture content increases. The desiccator must be replaced when the desiccant turns pink.

OVERLOAD CUT-OUTS

34. An overload cut-out is fitted to the viewing unit control panel and four cut-outs are fitted to the power unit; fuses are not used. These cut-outs are fitted with mechanical release and reset buttons which are accessible from the top of the unit after removing the top cover. These cut-outs should not be reset until the cause of tripping is ascertained.

MECHANICAL DESCRIPTION OF 21in VIEWING UNIT

INTRODUCTION

35. The viewing unit is designed to be fitted below and provide the mounting for the horizontal table top. The whole assembly is free-standing and is at a convenient height for the standing operators.

36. The viewing unit is built-up on a main structure frame which supports and houses various sub-units. The sub-units can be removed for servicing by disconnecting the appropriate terminal strips and releasing the securing bolts. It is not advised that the power units and deflection drive amplifier units be operated out of the viewing unit out of contact with their cold plates unless adequate provision is made for their cooling.

37. During the initial setting-up procedure, the orientation of the display with respect to the viewing unit framework may be set to one of several positions to meet local operating requirements. For reference purposes in the following description, that face of the viewing unit which carries the heat exchangers is identified as the west face. In the following paragraphs the main viewing unit assembly will be described first, followed by the various sub-assemblies.

MAIN ASSEMBLY

38. The basic frame consists of a top plate and a bottom plate, linked together by four vertical corner struts. The top plate has a circular cut-away area to accommodate the vertically mounted c.r.t., which is supported via a rubber mask, fitted to the periphery of the c.r.t. face. The mask is seated in a circular, curved section support ring secured to the top plate. At the centre of the base plate, a vertical horn-shaped framework surrounds the c.r.t. and provides a mounting for the Mu-metal screen panels. The framework also supports the deflection and focus coil assemblies. The four outer faces of the unit are enclosed by non-removable top plates and removable covers, each secured by six quick-release fasteners.

39. Removal of the west face cover exposes the two air ducts, each containing a heat exchanger. A small electric motor, driving two centrifugal fans, supplies cooling air to both ducts. When fitted, the cover so extends the ducts, that air is drawn in from, and exhausted to, the outside of the viewing unit.

40. Removal of the east face cover gives access to the three power units, and the character drive unit and final deflection amplifiers become accessible. These units are mounted on two cold-plates, situated one above the other. The lower plate carries the main, auxiliary and e.h.t. power units, together with the character drive unit. The upper plate carries the two final deflection amplifiers.

POWER UNIT

41. The main power unit is constructed with a back plate which provides an effective heat sink. The back plate is mounted in close contact with the viewing unit cold-plate. The power unit mains transformer, high current rectifiers, series regulator transistors, smoothing chokes and all heat generating components, are mounted directly onto the back plate.

EHT POWER UNIT

42. The e.h.t. unit is likewise constructed with a back plate, to provide an effective heat sink for the two power transistors used in the unit. The e.h.t. transformer, high voltage rectifiers and e.h.t. smoothing circuit, are contained in a sealed oil-filled can, secured to the back plate. Connections to the unit are made via a taper-pin socket, with the e.h.t. voltage output taken via a special high voltage lead direct to the c.r.t. final anode terminal.

43. The heat generating components of the auxiliary power unit are also mounted on a back plate, which is in close contact with the cold plate. Five taper-pin sockets accommodate the external connections to this unit, and are easily accessible from the front.

DEFLECTION COIL DRIVE AMPLIFIER ASSEMBLY

44. Just above the character drive unit and e. h. t. unit, are the deflection coil drive assemblies. These assemblies each comprise a metal transistor mounting block and a paxolin printed wiring board, supported on this block, but separated by spaces. The four output and two driving transistors of each amplifier, together with 12 printed resistors, are fitted to the mounting block, which has considerable mass to form a heat sink. The other electronic components are fitted to the printed wiring board. Connections to each assembly are made via two taper-pin sockets. Both deflection coil drive assemblies are mounted on a common cold-plate. All cold-plates used in the viewing unit are hollow channelled structures, connected to external inlet and outlet pipes, through which flows the coolant.

45. On removal of the north face cover, access is obtained to the pump assembly for the deflection drive amplifier cold-plate, the board box (containing four vertically mounted M type printed wiring boards) and the focus control panel.

BOARD BOX AND PRINTED WIRING BOARDS

46. The board box is identical to that employed in the 12in viewing unit, housing the same M type boards (see paras. 15 to 19).

CONTROL PANEL (TYPES 11057, 11066 AND 11060)

47. The operator's control panel contains the majority of controls required by the operator to select the various radar display functions available. The panel is constructed in the form of a rectangular box (approx. 13in \times 6in \times 5.5in) and is mounted in the Master Allocator Controller's Comms. Pedestal Assembly Type 60083. The 11 potentiometer controls are mounted on a perspex panel which is illuminated by panel lamps.

CONTROL PANEL TYPE 12701

48. This panel is located under the east side cover of the 21in viewing unit and is mounted across the top of this chassis section. The complete assembly measures approx. 17in \times 4in \times 2in, and is secured to the viewing unit frame by four screws. All potentiometers are preset except RV5 and RV6.

CHARACTER DRIVE UNIT

49. The character drive unit takes the form of a three-sided box, with two printed wiring boards forming the two sides, and a heat sink forming the connecting base. All components are mounted on the inside faces of the boards. The unit is located to the left of the e. h. t. power unit and is fixed to the same cold-plate that carries the power units.

JUNCTION UNIT TYPE 12795/A

50. The junction unit interconnects between various groups of circuits within the viewing unit, between the display and external items of equipment and between the viewing unit and the control panels.

51. The interconnections between viewing unit and junction unit are carried by four 50-way Burndy Hyfen connectors. External connections to the junction unit are achieved by 14 removable plugs and sockets.

52. The junction unit is located immediately behind the south face panel of the viewing unit, but holes cut in the panel allow engagement of the system interconnection cables with the 14 junction box plugs and sockets. After removal of the viewing unit panel, access to the interior of the junction box is obtained by releasing six Dzus fasteners.

CATHODE RAY TUBE ASSEMBLY

53. The focus coil assembly, which also contains the astigmatic correction and alignment coils, is located below the deflection coil assembly.

54. The beam-centring magnets are fitted around the neck of the c. r. t. and the combined field strength of the magnets may be adjusted by rotating one magnet with respect to the other.

55. The c. r. t. is supported by the rubber flange fitted around its flare, and is held against upward motion by the implosion screen. The screen is edge-lit by four lamps.

FOCUS AND DEFLECTION COIL ASSEMBLIES

56. Mounted across the top of this chassis section is the focus control panel, consisting of a metal plate on which are mounted the controls necessary to obtain correct beam alignment and electrical focusing of the c. r. t.

57. Access to the deflection and focus coil assemblies is obtained by removal of the Mu-metal panel sections on the north and south faces of the inner frame. The main and secondary deflection coils are in one assembly, encapsulated to ensure rigidity. A laminated plate, mounted horizontally within the inner frame and secured

to it, supports the deflection coil and its adjustment assembly. The latter consists of an adjustable clamp of insulating material, fitted around the deflection coil and secured to the mounting shelf. When the clamp is released, the deflection coil can be moved freely along the neck of the c. r. t. The Tufnol bolts which engage with vertical threaded holes in the mounting shelf, clear the inner diameter of the clamp and abut against the base of the deflection coil assembly. The screws are used to adjust the height of the coil assembly. The height is set such that the top of the assembly is firmly in contact with the flare of the c. r. t. and the clamp is then tightened. Situated to the right of the clamp locking screw is the metal screw which provides limited rotation of the deflection coil assembly for fine adjustment of orientation.

COOLING SYSTEM

58. The heat generation of the viewing unit necessitates two similar but distinct cooling systems. The coolant used in the system is a light mineral oil (Shell Turbine No.1), which is circulated through a series of cold-plates by a pump driven by an integral 230V electrical motor. The heat absorbed by the coolant is extracted by a heat exchanger and transferred to cooling air drawn over the heat exchanger by double centrifugal fans. The heat exchanger is a coiled tube, finned inside and out, with the coolant flowing over the inner fins and the cooling air drawn over the outer. The heat exchangers are mounted vertically, and cool air is drawn in at the top of the trunk and exhausted at the bottom.

59. The main cooling system circulates from the south face pump around the power unit's cold-plate, the heat exchanger and the board box. The subsidiary cooling system circulates from the north face pump around the final deflection amplifier cold-plate, the second heat exchanger and back to the pump.

60. On removal of the south face side cover, the second coolant pump, situated to the right of the junction unit, becomes accessible. This pump is identical with the other pump assembly, but is part of a separate cooling system.

61. The power supply to the pumps and fans of both systems is connected while the display is at 'standby' or 'on'. Each heat exchanger has fitted to its outlet mounting block, a gravinette thermostat to interrupt the supply to the fan if the coolant temperature falls to 0°C. This is to prevent over-cooling while operating at low ambient temperature. A third thermostat, fitted to the power unit's cold-plate, trips the incoming mains supply to the display if the temperature rises to 83°C. This condition could arise if a cooling system fails, or the final deflection amplifiers develop a fault.

SPACE HEATERS

62. Two space heaters are fitted to the centre of the viewing unit base plate, directly under the c. r. t. base. When the display is switched off, these heaters are connected in series across the mains supply, thereby preventing condensation within the unit.

ELECTRICAL DESCRIPTION OF 12in AND 21in VIEWING UNITS

OUTLINE OF OPERATION (FIG.5)

63. Switch and gate waveforms are produced in the timing board from the radar trigger and are fed to the video and deflection boards; the excitation voltage for the synchro resolver is also produced in the timing board (in some applications, however, this excitation is derived from an external source).

64. The video board provides the complex video waveform to the c. r. t. grid and the complex brilliance waveform to the c. r. t. cathode. The video waveform is a combination of radar videos and calibration markers produced in the video board; the brilliance waveform blanks the c. r. t. during appropriate periods. Control voltages for the brilliance and video circuits in the video board are provided from the viewing unit control panel and the operator's control panel.

65. The deflection boards contain the aerial demodulator, timebase generator, shift switching and deflection combining circuits used in the generation of the deflection waveforms; these waveforms are fed to the deflection coil drive amplifier.

66. In the deflection coil drive amplifier four separate but identical amplifiers are provided to drive the four deflection coils.

VIEWING UNIT SUB-ASSEMBLIES

67. The circuits of the viewing unit may be divided into a number of groups:-

- (1) Power supply circuits
- (2) The temperature control system.
- (3) The printed wiring boards.
- (4) The deflection drive amplifiers.
- (5) Character drive unit type 12500 (LRD only).
- (6) Viewing unit control panel.
- (7) Radar display control panel.

68. Each of these groups is described under a separate heading in the following paragraphs.

POWER SUPPLY CIRCUITS

69. Two separate power supply units are fitted in the 12in viewing unit (both LRD and HRI), one type 11600 and the other type 11601. These power units are controlled from the OFF/STANDBY/ON switch on the viewing unit control panel.

70. Power Unit Type 11600 operates from a single-phase a.c. supply in the range 200/250V. With the exception of the h.t. and e.h.t. supplies for the c.r.t., this power unit supplies all the power requirements of the viewing unit and its associated control panel.

71. Power Unit Type 11601 operates from an unstabilised 22V d.c. supply obtained from the Power Unit Type 11600. This supply becomes available when the ON switch on the viewing unit control panel is operated. A thermal delay is incorporated to ensure that this power unit does not become operative until the c.r.t. heaters have attained working temperature. The outputs from this unit comprise a 15kV e.h.t. supply and a stabilised 320V supply for the first anode of the c.r.t.

72. In addition to the E.H.T. Power Unit Type 11601, the 21in viewing unit also employs Power Units Type 11605 and 11606.

73. Power Unit Type 11606 operates from a 200/250V r.m.s. single-phase 45-65Hz supply. With the exception of the supplies required by the deflection drive amplifiers, the focus coil and the c.r.t., it provides all the power supplies required for the 21in viewing unit. The fan in the board box and main P.U. cooling system is supplied with 200V a.c. from tappings on the primary of the P.U. mains transformer.

74. Power Unit Type 11605 produces a 22V supply for the deflection drive amplifiers. It also produces a regulated current supply for the focus coil from the stabilised but unregulated 18V supply received from the Power Unit Type 11606. The fan and pump in the final deflection cooling system are supplied with 200V a.c. from tappings on the primary of the P.U. mains transformer.

75. The 12in viewing unit employs a mechanically adjusted permanent magnet focusing system, but a fine adjustment of focus is provided by variation of the e.h.t. voltage within a limited range. This facility is controlled by a potentiometer mounted on the viewing unit control panel.

76. The 21in viewing unit employs an electro-mechanical focusing system using a focus coil. The fine adjustment of focus is provided by the focus potentiometer on the Viewing Unit Control Panel Type 11066 varying the focus coil current. Coarse adjustment is similarly provided by the preset coarse potentiometer on the Power Unit 11605. Various alignment, astigmatism and centring controls together with their associated test switches are provided on Control Panel Type 12701/A.

THE TEMPERATURE CONTROL SYSTEM

77. Cooling of the 21in viewing unit is achieved by two separate systems, each using a separate pump and heat exchanger. The main system coolant circulates from the pump, round the power unit's cold plate, through the heat exchanger to the board

box and back to the pump. The subsidiary system circulates from the pump, around the deflection drive amplifier cold plate, through the second heat exchanger and back to the pump. Each heat exchanger itself is cooled by a small electric fan. A low temperature (0°C) thermostat is fitted in the air flow of each heat exchanger and when operated interrupts the main supply to the associated fan. A second high temperature thermostat (65°C) is fitted to the back plate of the Power Unit 11606 and is connected in series with the 83°C thermostat on the cold plate of the deflection drive amplifier cooling system. Operation of either thermostat interrupts the mains supply to relay RLA in the control unit. The relay de-energises and interrupts the mains and SW supply to the viewing unit.

78. Cooling of the 12in viewing unit (both LRD and HRI) is similar to the above, but employs only a single system. The coolant flows from the pump, through the board box cold plate, the power unit cold plate, the deflection drive amplifier cold plate, through the heat exchanger and back to the pump.

79. Both the above cooling systems are operative when either the STANDBY or ON switch on the relevant viewing unit control panel is in the operated position.

THE PRINTED WIRINGBOARDS

80. The printed wiring boards carry the majority of the display circuits (excluding the power supplies). Four such boards are fitted as follows:-

- (1) One timing board or category selection board.
- (2) One X and one Y deflection board.
- (3) One video board.

81. The general functions of the circuits contained on these boards and the inter-connections between boards are described in the following paragraphs. Detailed technical descriptions are contained in Part 2, Section 2.

82. One of two differing types of timing board is fitted to the viewing unit, according to whether an interscan or fastscan system is being used. For convenience both boards are described in the following paragraphs.

Interscan timing board (MJE)

83. The circuits of this board generate various switch and gate waveforms and provide an excitation voltage for the aerial synchro resolver.

84. The circuits performing the first of the above functions derive a series of timing pulses from the radar trigger, and subsequently use these to produce the gate waveforms. The pulses derived are the 'scan-end' pulse, the 'IS start' pulse and the 'IS knock-off' pulse.

85. The MS/IS switch waveforms and the MS/IS switch waveforms (shift) are generated from the IS start pulse and the scan-end pulse. The first of these pairs of waveforms is fed to both the deflection and video boards and the second to the deflection board only. The only difference between these pairs of waveforms is that the latter pair may be replaced by two fixed levels corresponding to mainscan conditions.

86. The calibration and brilliance gate waveform is generated from the radar trigger and scan-end pulse for mainscan periods, and the radar trigger and IS knock-off pulse for interscan periods. Both waveforms are fed as a single train to the video board only.

87. The timebase gate waveform is generated from the radar trigger and the scan-end pulses, and is fed to the deflection boards.

88. The circuits generating the aerial synchro supply operates differently according to whether a radius of diameter scan is being produced.

89. If a radius scan is being used, the circuits produce a 400Hz sine wave for feeding to the aerial synchro, together with a sampler gate waveform, the pulses of which coincide with the positive peaks of the sine wave only. The sampler gate waveform is fed to the deflection boards.

90. If a diameter scan is being used, the circuits utilize the radar trigger pulses to generate a sine wave at the radar repetition frequency for feeding to the aerial synchro together with a sampler gate waveform whose pulses coincide with both the positive and negative peaks of the sine wave.

91. When an h. r. i. system is used it employs a radius scan, but the internal 400Hz sine wave is not used in some applications.

Category selection board (MJS)

92. This board accepts the following timing pulses - MS start, MS end, FS start, FS end, track label/symbol marker bit, and the console address supervisory bit. All these inputs are positive-going. From these inputs the board generates the following waveforms:-

- (1) Mainscan switch waveform.
- (2) Character switch waveform.
- (3) Symbol switch waveform.
- (4) Symbol waveforms.
- (5) Composite brilliance gate waveform.

93. The MS switch waveform is produced by the MS switch bistable from the MS and FS end pulses.

94. The character switch waveform is produced by gating the bistable output (para. 93) with the track marker bit.

95. The symbol switch waveform is produced, and the symbol generator initiated by gating the bistable output with the inverted track marker bit.

96. The FS start pulse is gated with the console address supervisory bit. Either the gate output or the MS start pulse is used to set the brilliance gate bistable (the bistable is reset by the MS or FS end pulse). The bistable output is gated with the tube protection waveform to produce the composite brilliance gate waveform.

Deflection boards (MRG, MRH and MRK)

97. Two deflection boards are fitted to the viewing unit, one handling the X deflection and the other the Y deflection.

98. Each board carries one aerial demodulator circuit, one timebase generator and scan switching circuit, one shift switching circuit, one deflection combining amplifier and one symbol drive amplifier. Thus it will be seen that each board carries all the necessary deflection circuits for one axis of the c. r. t.

99. In general, the following description refers to the circuits of one board only, since the two boards are identical for p. p. i. type displays. The exceptions are where certain circuits on the two boards are interconnected and the specific case of the h. r. i. display (see para. 114).

100. According to whether a diameter or radius scan is being produced, different methods of using the demodulator circuits obtain.

101. When a diameter scan is being produced, the demodulator circuits on the two boards are used independently. Each circuit receives its particular modulated component from the aerial synchro and both receive the sampler gate waveform; its output is the scan control voltage for one axis of the c. r. t.

102. When a radius scan is being produced, the demodulator circuits on the two boards are coupled to form the oscillator-type demodulator referred to in Chap. 2. Each demodulator receives the same inputs as in para. 101 and produces the same output.

103. The MS scan control voltage and the appropriate IS scan control voltage are fed to a switching circuit controlled by the MS/IS switch waveforms, which selects one or other for feeding to the timebase generator circuit.

104. If the interscan marker is in the form of a range and bearing marker the IS scan control voltages are the outputs from the sliders of a sine/cosine potentiometer-

operated by the operator's bearing control. The scan control voltages thus determine the bearing of the marker. The bearing of runway markers and harbour leading line markers are set in a similar way. If the interscan marker is being used as a c. r. d. f. line, the IS scan control voltages are derived from the outputs of the c. r. d. f. station.

105. If the interscan marker is in the form of a height line on a height/range display, the scan control voltage for both MS and IS on the X board will be a fixed d. c. level. On the Y board, however, the MS scan control voltage will come from the aerial synchro and the IS scan control voltage will be an attenuated version of the output from the X timebase generator. This latter will produce a downward curvature of the height line which corresponds to the earth's curvature.

106. The timebase generator circuit is identical to that described in Chap. 2 of this section. For a p. p. i. type display the shift input terminal is connected to earth level, but in certain other applications a variable shift level is used. The action of the timebase generator circuit is controlled by the timebase gate waveform from the timing board. The output from the timebase generator forms one input to the deflection combining amplifier (para. 111).

107. To programme the various shift levels (MS and IS/FS) into their correct display periods, a shift switching circuit is used. The switch is capable of receiving three inputs: MS shift, IS shift, and FS shift. As the MS shift input is usually earthed, the IS and FS inputs are used as required.

108. For an interscan system the switch is operated by the MS/IS switch waveforms (shift) from the timing board. For a centred interscan marker, i. e. one whose origin is coincident with that of the mainscan, the switch waveform is held permanently in the mainscan condition. This is achieved by replacing the switch waveforms with levels corresponding to mainscan conditions, i. e. locking the switch waveform generator at 'MS'.

109. For a fastscan system the MS/FS switch waveform from the timing board is used to control the switch circuit.

110. The output from the shift switch circuit is fed to the deflection combining amplifier.

111. The deflection combining amplifier generates a push-pull pair of complex deflection drive waveforms from a total of four inputs. These inputs comprise the 'scan waveform' output from the timebase generator circuit, the output from the shift switching circuit and both a picture centring control voltage from the viewing unit control panel and a radar shift control voltage from the operator's control panel. The radar shift voltage is switch-selected at the operator's control panel.

112. The circuit comprises a summing amplifier followed by a unit gain inverting amplifier whose push-pull output waveforms are fed to the coil drive amplifier assembly.

113. Range switching is achieved by switching the gain of the summing amplifier between four discrete values.

114. In a h.r.i. display certain variations are required for the deflection boards. The Y deflection board is exactly as described, but a much simpler board is used for the X deflection. This simpler deflection board carries timebase generator and combiner amplifier circuits only. The timebase generator receives a constant value of scan control input and therefore runs at a constant rate. The shift input to the timebase generator on the Y deflection board receives a variable shift level from the operator's height control potentiometer. This level determines the level of the height line above the base line.

115. Returning to the basic deflection boards, these also carry the circuits of a symbol drive amplifier, which is only used with a fastscan system. The amplifier receives as input the symbol deflection drive waveforms from the fastscan timing board. It produces as output a pair of push-pull symbol drive waveforms suitable for feeding out to the coil drive amplifiers. It should be appreciated that these push-pull outputs are for one deflection axis only, those for the second axis being produced on the second deflection board.

116. Thus, the outputs from the deflection board comprise the push-pull components of the complex deflection drive waveform for one deflection axis. These outputs are fed out to the coil drive amplifiers. Additionally, when a fastscan system is being used, the board produces also the push-pull symbol waveforms which are fed to the coil drive amplifiers.

Video board (MFD)

117. The video board carries the circuits of a video amplifier system, a brilliance control system and a calibration generator.

118. The function of the video amplifier is to combine up to six radar videos for onward transmission to the c.r.t. and to blank the c.r.t. during appropriate periods.

119. The amplifier is provided with up to six separate input channels; each channel is capable of being switched off and is provided with independent gain control. Four of the channels are used for radar videos and the remaining two for calibration markers. The amplifier also contains circuits for blanking the video during the interscan or fastscan periods. The output from the amplifier is fed to the c.r.t. cathode.

120. The brilliance circuits comprise a switching circuit feeding a gated brilliance amplifier. The inputs to the switching circuit consist of the mainscan brilliance control voltage and either an interscan brilliance or a fastscan brilliance control voltage. The switch is controlled either by the MS/IS switch waveforms or by the MS/FS switch waveforms.

according to which system is being used. The output from the switch is the correct brilliance control voltage in each display period.

121. The output from the switch circuit is fed to the gated amplifier. The function of the gating circuit is to blank the c. r. t. during all shift regimes, and also in accordance with the output of an octagonal blanking circuit. The octagonal blanking circuit restricts the usable part of the c. r. t. face to an octagonal-shaped area within the circular periphery.

122. The outputs from the brilliance circuit are fed to the grid of the c. r. t.

DEFLECTION DRIVE AMPLIFIERS TYPES 12502 and 12505

123. In the 12in Mk. 5 viewing unit, one Deflection Drive Amplifier Type 12502 provides four identical amplifier channels, one for each section of the mainscan deflection coil assembly. Two Deflection Drive Amplifiers Type 12505 are used to provide the larger deflection coil drive current required by the 21in video unit. Each amplifier has two identical channels, each of a similar circuit configuration to those of the Amplifier Type 12502.

124. The mainscan deflection waveforms are applied during mainscan and the symbol waveforms during the fastscan periods. The amplifiers act as current convertors, and drive through the relevant deflection coil, a current proportional to the input voltage.

125. The first stages of the Amplifier 12502 operate from a +12V regulated supply, and the final stage from a high current 20V (nominal) unregulated supply. Both supplies are derived from the Power Unit 11600. The first stages of the Amplifier Type 12505 also operate from the +12V regulated supply derived from the Power Unit 11606 but the 20V (nominal) supply to the final stages is derived from the auxiliary Power Unit 11605.

CHARACTER DRIVE UNIT TYPE 12500

126. This unit used only in the LRD viewing units, accepts the character scan waveforms superimposed on the minor shift level routed from the character generator cabinet. It will be noted that the minor shift is a series of d. c. levels that position from left to right the sequential characters in a character group (the X channel only).

127. The unit contains two push-pull amplifiers, one for the X and one for the Y deflection. Each amplifier contains an inhibit circuit to which the character switch waveform is applied from the category selection board.

128. During the fastscan period, if a track label bit is input, the character switch waveform is negative-going and therefore enables the presentation of character deflection waveform inputs. In the mainscan period the character switch waveform is positive-going (+6V) and therefore inhibits the presentation of the e. d. d. character deflection waveforms.

129. To accept the short duration deflection pulses which make up the character shape, a separate low inductance deflection coil is provided for character deflection.

VIEWING UNIT MOUNT

130. The viewing unit mount, fitted to the 12-inch viewing unit only, is a wedge-shaped assembly which supports the viewing unit at the optimum angle for a seated operator. It also provides an angled mounting for the operator's control panel, and houses termination strips for all cabling to the display. The mains transformer for the operator's control panel illumination is also housed within the mount.

VIEWING UNIT CONTROL PANEL

131. The Control Panel Type 11211 on the 12in display is located behind the hinged flap on the front of the viewing unit. The panel contains a set of four range-selection push-button switches, various picture element and c. r. t. controls and three push-button power supply control switches.

132. The Control Panel Type 11066 for the 21in display is located in the Master Allocation Controller's Comms., Pedestal Assembly Type 60083. This panel also contains a set of four range-selection push-button switches, various picture element and c. r. t. controls and three push-button power supply control switches.

133. The four range-selection switches control, via relays, the gain of the range amplifiers on the X and Y deflection boards contained in both the 12in and 21in viewing units.

134. Six gain control potentiometers control the gains of the various input channels of the video amplifiers, again, on both types of viewing unit.

135. Other potentiometers on the 12in Viewing Unit Control Panel Type 11211 are the X and Y centre controls, radar brilliance, focus, video limiter and the panel lights dimmer control.

136. The other potentiometers on the 21in Viewing Unit Control Panel Type 11066 are the fine focus, radar brilliance, video limiter controls and a dimmer control for the panel and plotting table lamps. The 21in viewing unit employs electro-magnetic focusing with the focus coil supplied by the Power Supply and Focus Drive Unit Type 11605. The various alignment, astigmatism, gain and centring controls are contained on Control Panel Type 12701. This panel also contains the various test/run switches associated with these controls, and is located under the north side cover of the 21in viewing unit, mounted horizontally across the top of this chassis section.

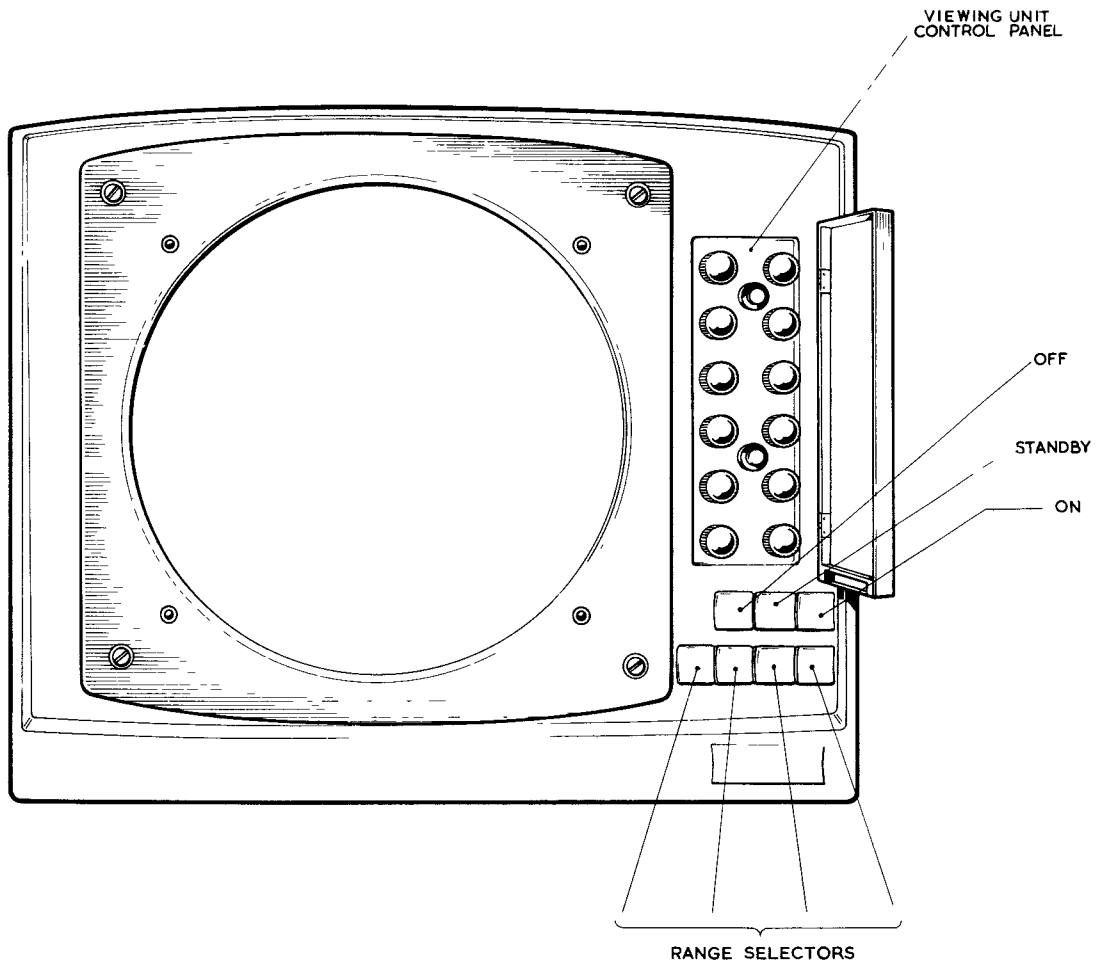
OPERATOR'S CONTROL PANEL

137. The operator's control panel provides control facilities for the radar video, range markers and the range and bearing line. The last facility may also be used as a c.r.d.f. line in some applications. The type of operator's control panel fitted will depend on the particular application of the viewing unit.

RADAR DISPLAY CONTROL PANEL

138. This control panel used with both the 12in and 21in viewing units is required to carry out the following functions:-

- (1) From the e.c.c.m. console radar video outputs, to select the required video and route it to the video PWB in the viewing unit.
- (2) To select the required auxiliary video for channel 4, i.e. one of the video maps 1 to 4, the S.I.F. gates from the character generator cabinet, or the 10^0 angle marks from the m.g.t. cabinet.
- (3) To select one of the two display system channels.
- (4) To provide various brilliance and shift controls which are used to control the radar picture presentation.
- (5) To provide the dimming facility for the panel lights. This is achieved by an eight position switch selecting various voltage tappings from a step-down mains transformer.



12 inch viewing unit: front view

A.L. 32. NOV. 71.

Fig. 1

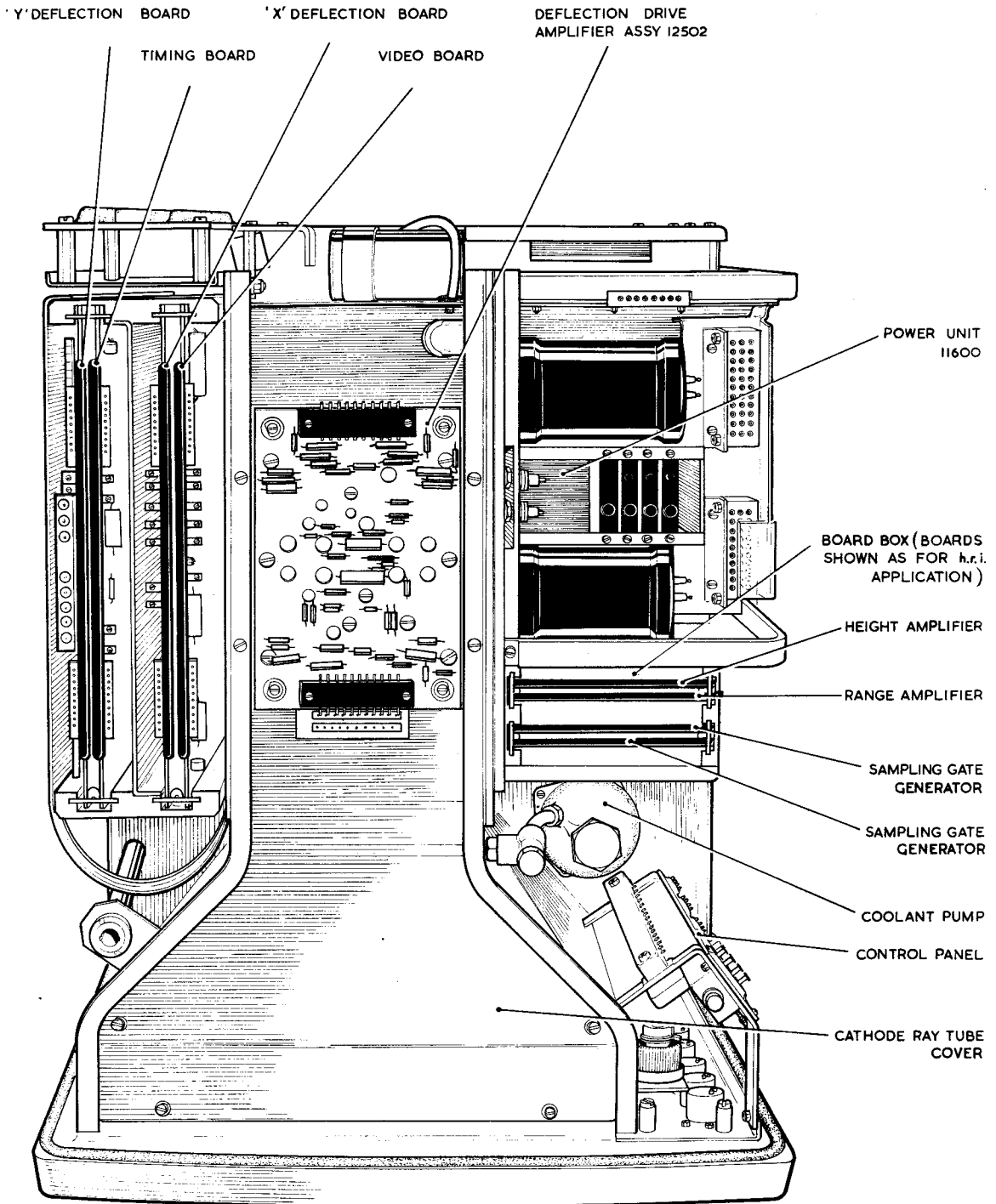
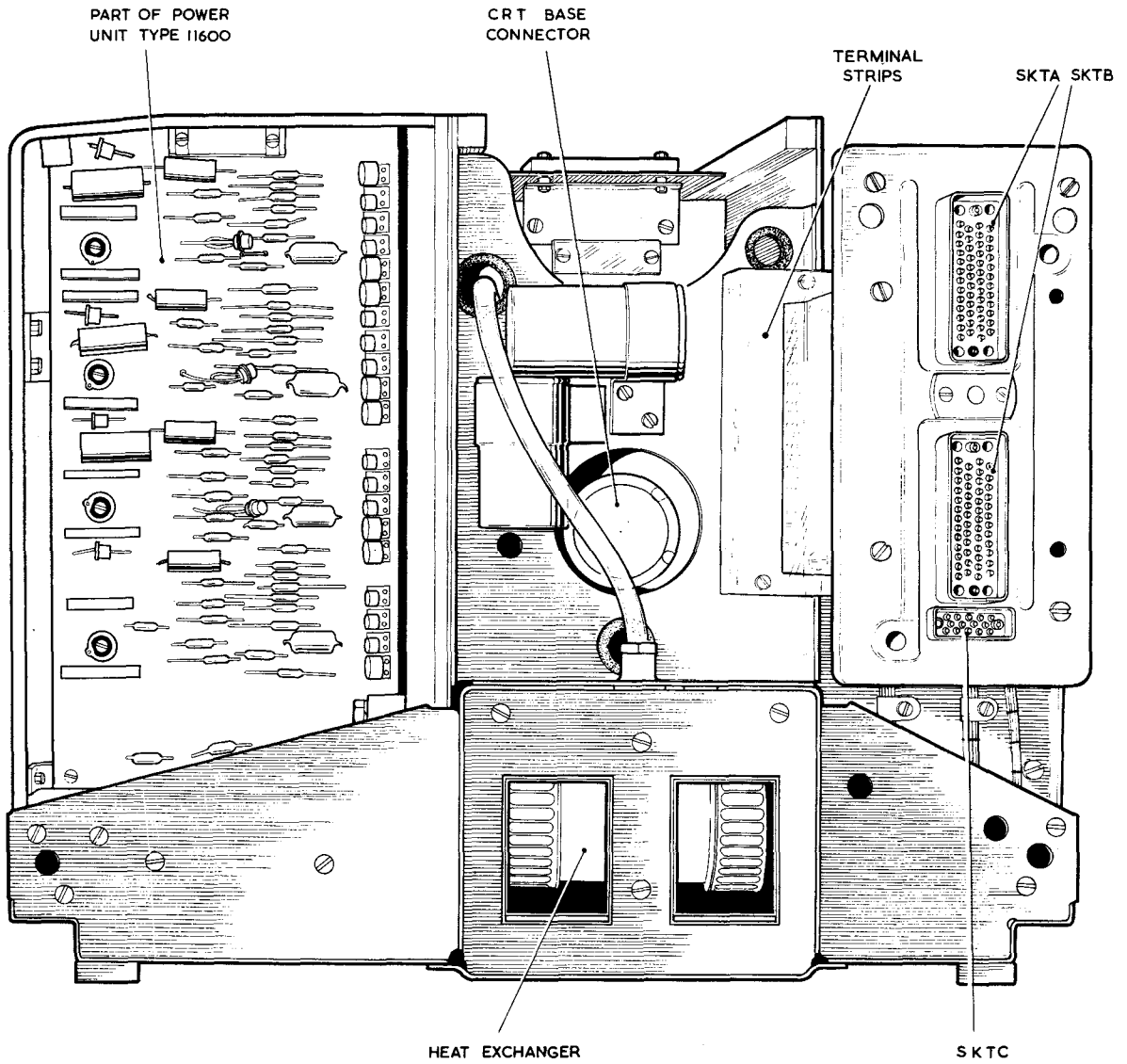
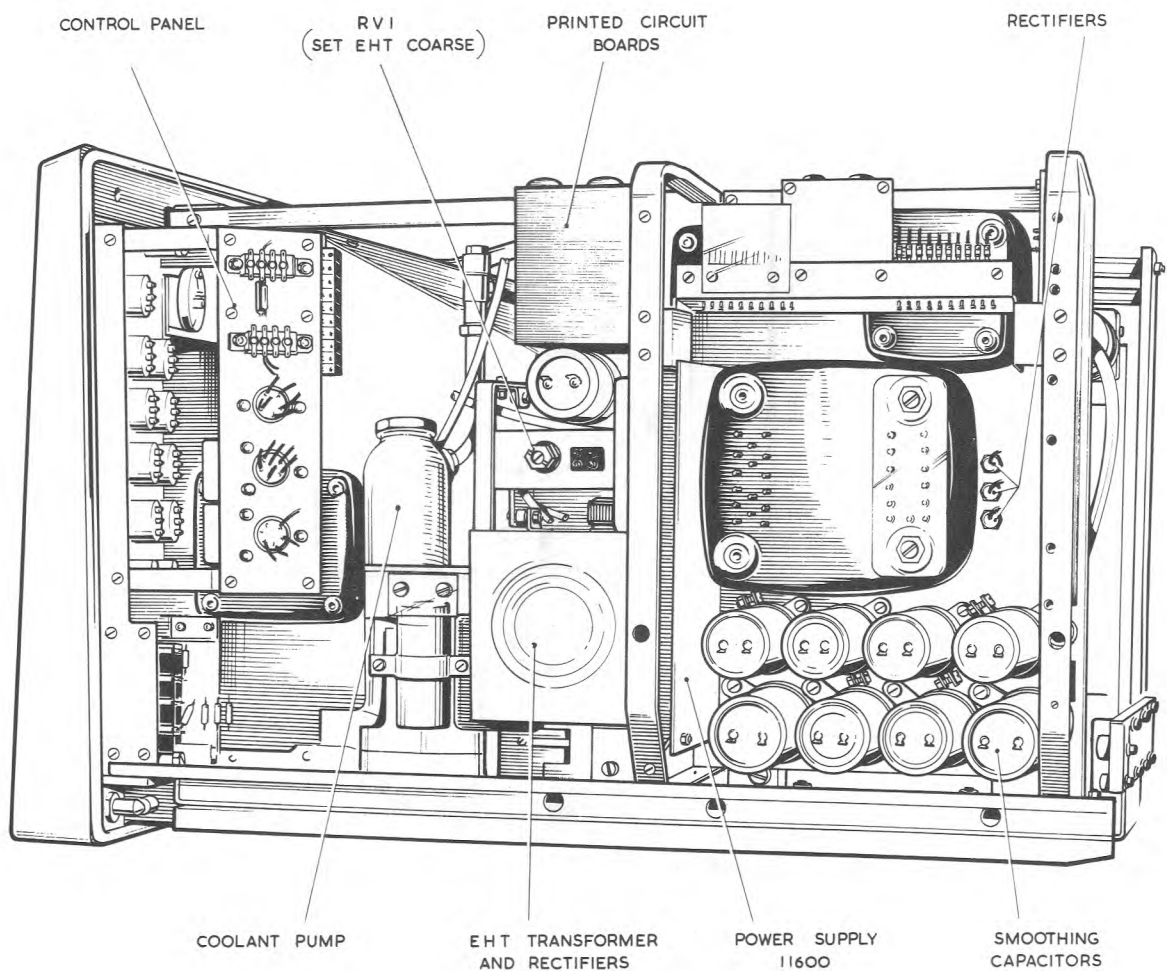


FIG. 2

A.L. 32. NOV. 71.



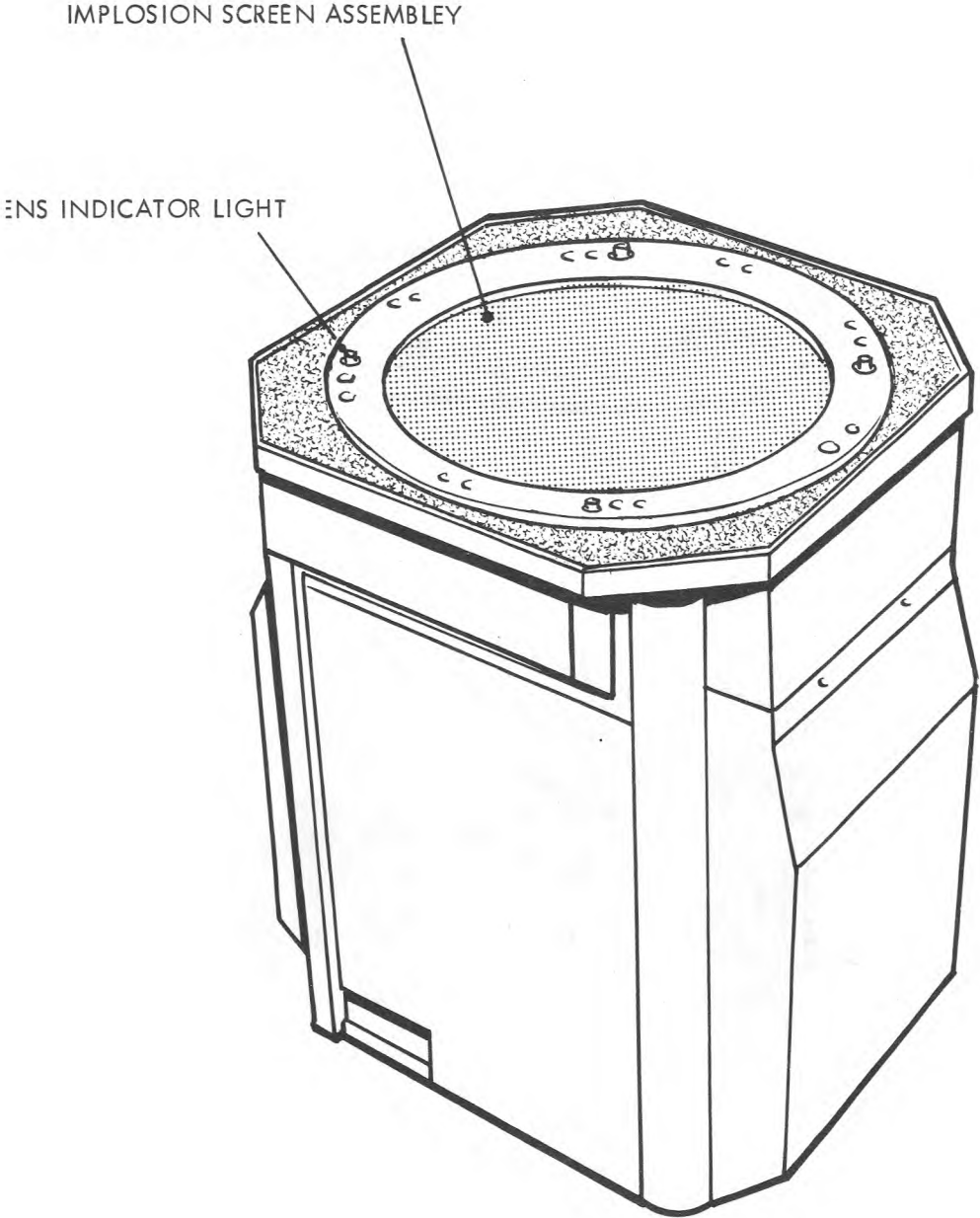
12 inch viewing unit: rear view



12 inch viewing unit : right-hand view

Fig. 4.

A.L. 32. NOV. 71.



A.L.32 NOV. 71

21in Viewing Unit

Fig. 5

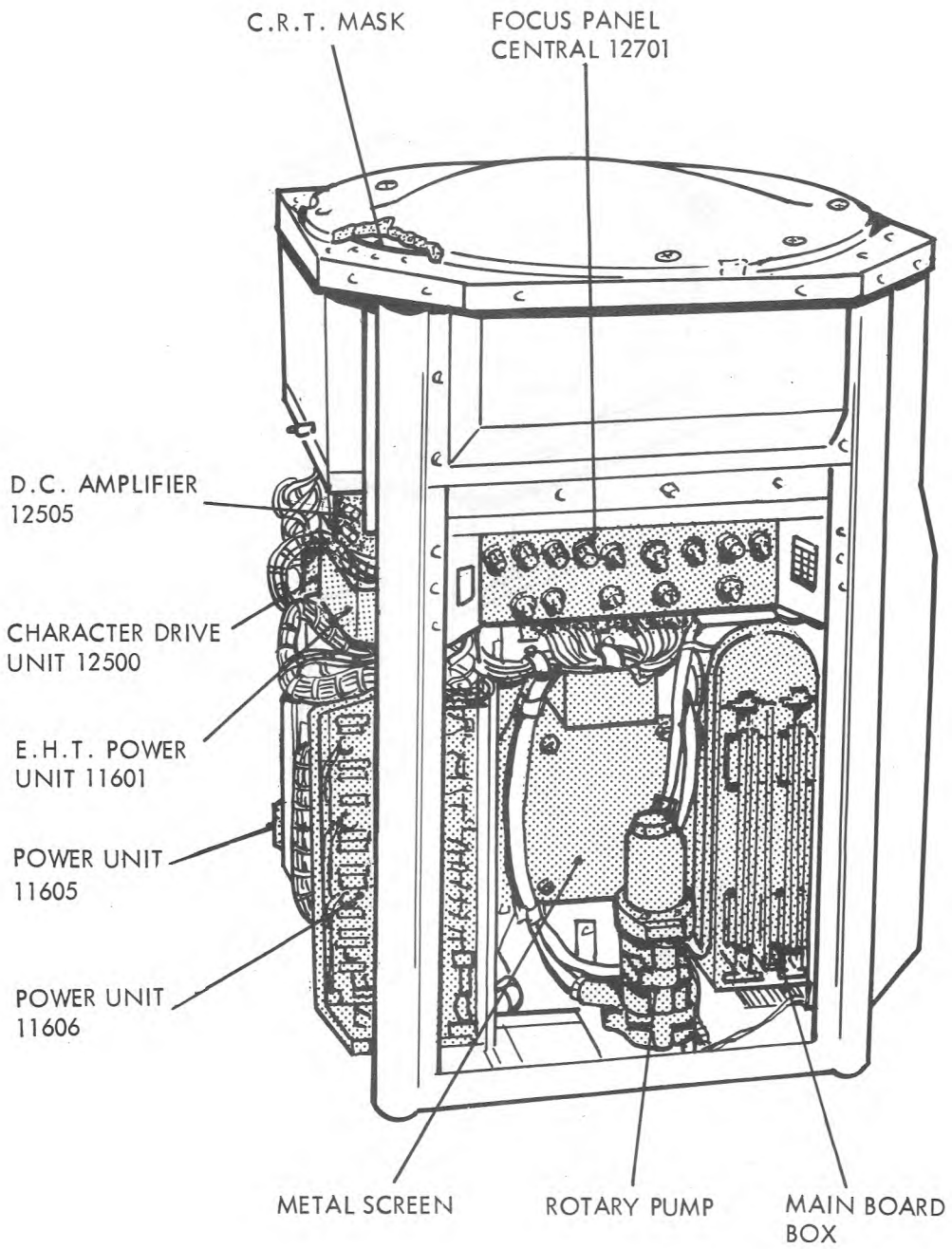
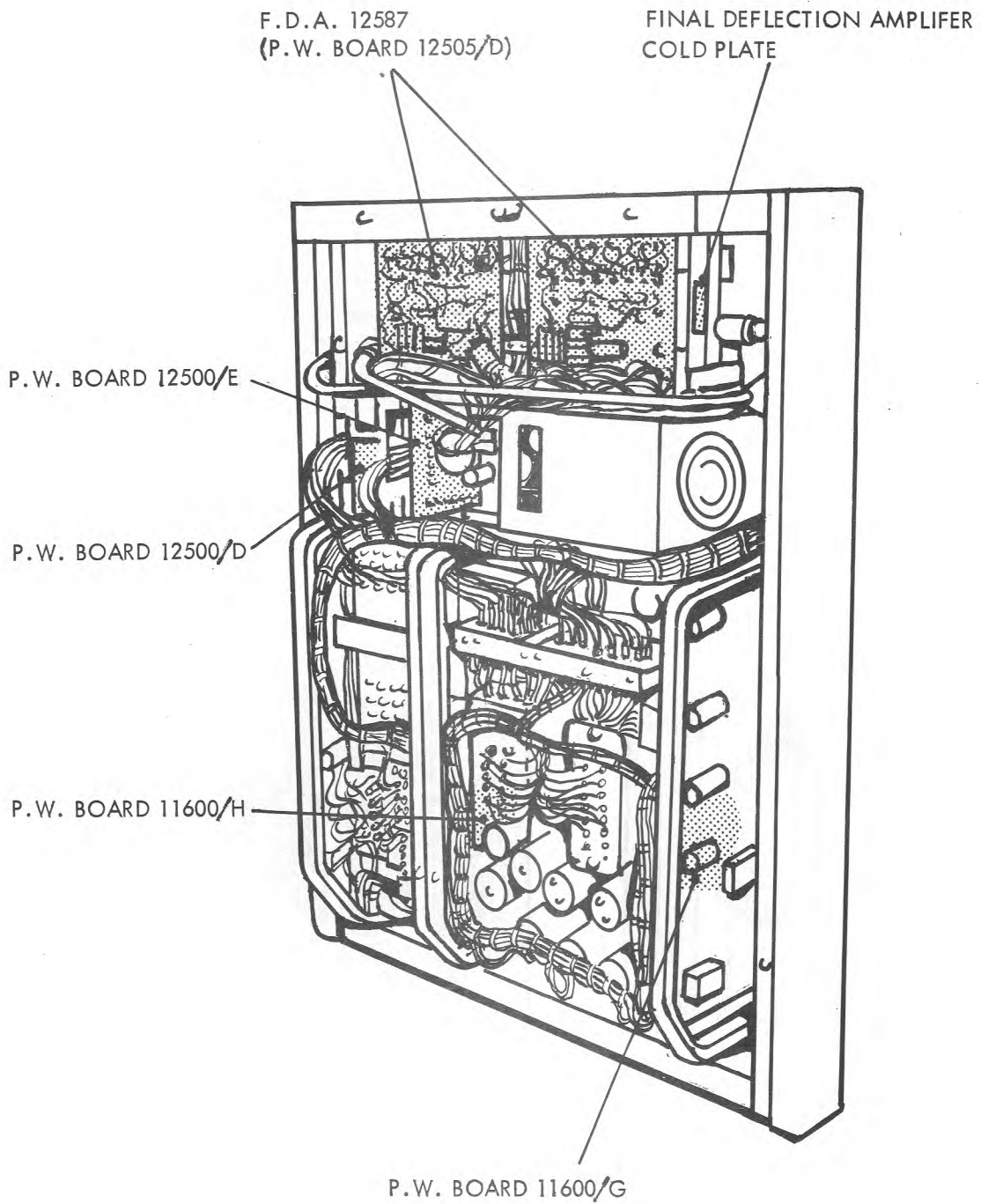
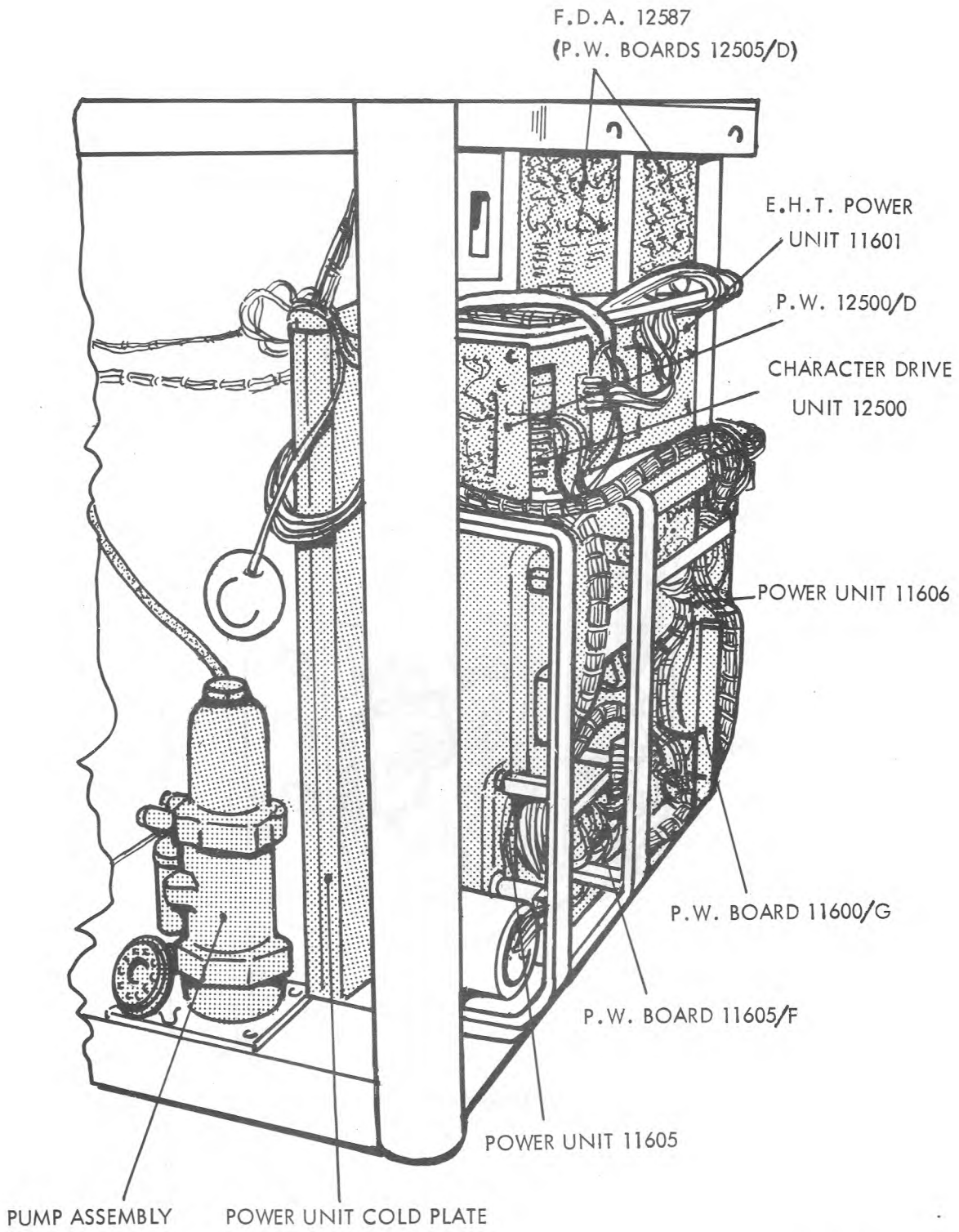


Fig. 6

21in Viewing Unit (Covers removed)

A.L.32 NOV. 71





PUMP ASSEMBLY

POWER UNIT COLD PLATE

F.D.A. 12587
(P.W. BOARDS 12505/D)

E.H.T. POWER
UNIT 11601

P.W. 12500/D

CHARACTER DRIVE
UNIT 12500

POWER UNIT 11606

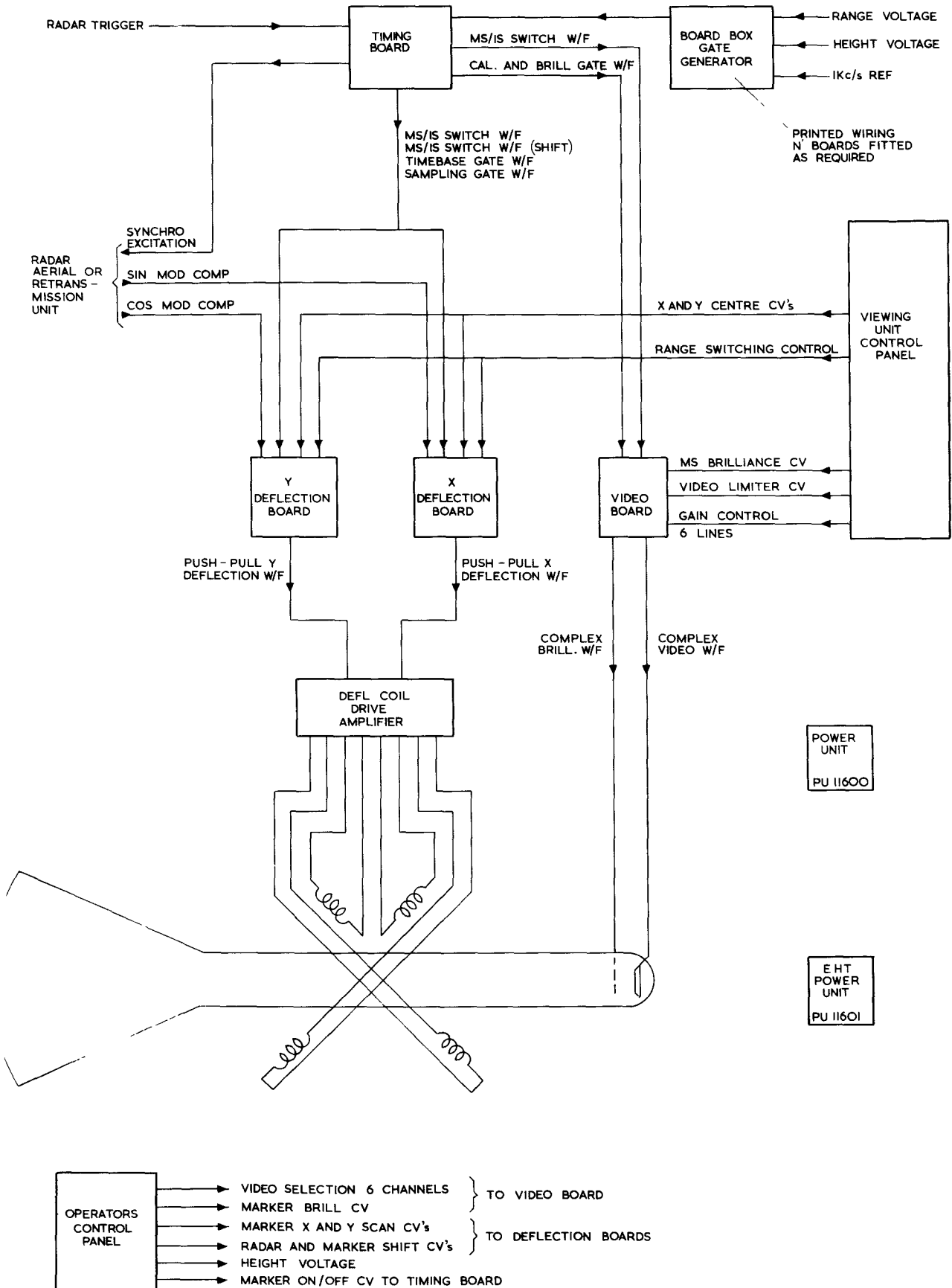
P.W. BOARD 11600/G

P.W. BOARD 11605/F

POWER UNIT 11605

Fig. 8

21in Viewing Unit - Detail of Interior



Mk.5 autonomous display: simplified block diagram

CHAPTER 4

CIRCUIT TECHNIQUES

	Para.
INTRODUCTION	1
OPERATIONAL AMPLIFIER	4
OPERATIONAL INTEGRATOR... ..	10
SHIFTING INTEGRATOR	11
OPERATIONAL DIFFERENTIATOR	19
CURRENT CONVERTER	20
TRANSISTOR PAIRS	21
ELECTRONIC SWITCH	34
ELECTRONIC GATE OR INHIBITOR	46
BISTABLE CIRCUITS	50
MONOSTABLE CIRCUITS	54
ASTABLE CIRCUITS	58
ZENER DIODES	59

LIST OF ILLUSTRATIONS

	Fig.
Basic feedback amplifier	1
Operational amplifier	2
Summing amplifier	3
Operational integrator	4
Shifting integrator	5
Operational differentiator	6
Current converter	7
Transistor pairs	8
Complementary transistor pairs	9
Complementary transistor emitter-follower	10
Current follower (1)	11
Current follower (2)	12
Transistor long-tailed pair	13
Series-operated transistors	14
Electronic switch... ..	15
Electronic switch (3-way)	16
Electronic gate or inhibitor	17
Basic bistable element	18
Monostable element	19
Astable element	20

INTRODUCTION

1. This chapter explains in general terms the electronic circuits which are commonly encountered in the Mk.5 Autonomous Display.
2. It will be appreciated that the degree of accuracy required in display systems is considerably greater than in most parts of a radar transmitter/receiver, since the eye is capable of detecting quite small distortions and discrepancies of shape on the screen, and any results obtained with the use of markers must be correct within quite fine tolerances.
3. The required degree of accuracy is obtained by the use of circuits whose behaviour is governed almost entirely by passive elements, usually resistors and capacitors, and as little as possible by the active amplifying elements.

OPERATIONAL AMPLIFIER

4. This is the simplest of circuits whose characteristics conform to paragraph 3; in this case the circuit has a stable voltage gain determined almost entirely by the values of two resistors.
5. The action of the device may be understood by considering first the behaviour of an amplifier with heavy negative feedback (Fig.1).
6. In the diagram, the triangle represents a high-gain inverting amplifier. Earths are included, but in later diagrams they are often omitted for convenience.
7. The feedback applied to this amplifier is derived in shunt with the output impedance and applied in shunt with the input. This results in the device having low input and output impedances and a 'transfer' impedance (the relationship between output voltage and input current) almost exactly equal to the value of the feedback resistor. The higher the transfer impedance of the amplifier without feedback, the more exact is this equality with feedback applied.
8. In the operational amplifier the circuit just described is voltage-fed via a relatively high-value resistor (Fig.2). Since the input impedance of the amplifier with feedback is low compared with R_{in} , to all intents and purposes all the input voltage is developed across the input resistor. Thus the input current is V_{in}/R_{in} and the over-all voltage gain is $-R_{fb}/R_{in}$.
9. Since the centre-point of the device is a low-impedance, low-voltage point and therefore may be said to be a virtual earth, it may be used for mixing several inputs applied via individual input resistors (Fig.3). The

value of each input resistor determines the over-all gain accorded to the corresponding input voltage. Such a device is usually referred to as a 'summing amplifier'.

OPERATIONAL INTEGRATOR

10. The operational integrator is obtained by replacing the feedback resistor with a capacitor. In this arrangement (Fig.4), the feedback stabilizes the relationship between input current and rate-of-change of output voltage. The relationship is directly derived from the property of the capacitor itself: $dV_{out}/dt = I_{in}/C$. Hence, if the device is voltage-fed via an input resistor, $dV_{out}/dt = V_{in}/CR$. Thus the output voltage changes at a rate determined by the input voltage and the time-constant formed by C and R.

SHIFTING INTEGRATOR

11. This circuit is a combination of the operational amplifier and the operational integrator and is often used in demodulation, timebase generation and other similar applications where the required output is, say, a sawtooth (or other integral) starting from a particular level. There are two input voltages: one to determine the starting level and one to determine the rate-of-change of the output voltage.

12. In the arrangement shown (Fig.5) the first amplifier is non-inverting and has a low-impedance output, while the second amplifier is inverting. When the switch is closed, the two amplifiers are connected in cascade; the whole arrangement functions as an operational amplifier, and the output instantaneously assumes a level determined by the 'shift' control input. The effect of the 'scan' control input is overridden by the low output impedance of the first amplifier, and the feedback capacitor, connected between two low-impedance points, is effectively charged to the value of the output voltage. This state of the circuit is referred to as the 'shift' condition.

13. When the switch is opened, no sudden change occurs, since the p.d. across the feedback capacitor momentarily holds the output constant. The 'scan' control input now becomes effective, and determines the rate at which the output changes.

14. In practice the change of condition of the circuit is accomplished by a gate circuit operated by a pair of opposed gate waveforms.

15. This arrangement may be used also to demodulate the output of an aerial synchro resolver. In this application the waveform to be demodulated is connected to the shift input and the scan control input is earthed. The switch is arranged to be closed for short periods coincident with the positive peaks of the resolver input waveform. During the period when the switch is closed the arrangement functions as an operational amplifier and the output assumes a level proportional to the peak of the input at that instant. When the switch opens, since there is no scan control input, the circuit acts as a store and maintains the output level it assumed during the period when the switch was closed. When the switch next closes, the output rises or falls to the level dictated by the input now present. Thus, the waveform at the output will be a reproduction of the modulation envelope of the input, varying in small steps.

16. If the modulation of the input is a linear function, the application of a small scan control input of the correct polarity will cause the output to move slowly during the period when the switch is open; careful adjustment of the scan control input causes the output to move at a rate and in a direction such that it assumes the next expected output just as the switch closes again. This technique is known as 'rate prediction' and gives rise to a smoothly varying output; it is normally employed on h.r.i. displays.

17. In normal p.p.i. systems the modulation varies according to the sine or cosine of the aerial's bearing. If a form of rate prediction is desired, the scan control input must vary according to the cosine or -sine respectively.

18. In cartwheel p.p.i. system, where alternate scans are painted 180° apart, it may be said that the positive half-cycles of the sine wave fed to the resolver produce the bearing information of one aerial, and the negative half-cycles the bearing information of the other. The gate waveform applied to the demodulator therefore is made to close the switch for small instants coincident with both positive and negative peaks of the resolver input, thus giving rise to an output which changes polarity every time the switch closes. Thus this output contains bearing information on one axis for both aerials. In this application the sampling frequency is twice the p.r.f. of each radar transmitter and the scan input is zero.

OPERATIONAL DIFFERENTIATOR

19. This circuit is the inverse of the integrator (Fig.6). The input current is CdB_{in}/dt and the output voltage is $CRdV_{in}/dt$. Such a circuit as shown is unstable, but it may be used with the addition of a resistor shunted across the capacitor so that the whole device operates as an operational amplifier with a differentiated component added to the output waveform.

CURRENT CONVERTER

20. A variant of the operational amplifier is employed sometimes where stabilized 'transfer admittance' (relationship between input voltage and output current) is required, as is often the case when driving reactive loads such as deflection coil assemblies. Here the feedback is derived in series with the output (Fig.7), and the transfer admittance is $R_{fb}/R_{in}R_g$. Typical resistor values are quoted as an indication of their comparative orders. (It should be noted that in this configuration, the two-terminal output impedance is considerably increased compared with the device without feedback, a situation obviously required to obtain an output determined by input voltage only and not by the nature of the load.)

TRANSISTOR PAIRS

21. Many circuits within this equipment employ pairs of transistors which are so closely interconnected that in many cases they may be regarded as one transistor with certain required characteristics more nearly approaching the ideal. Such pairs, therefore, may yield much higher current and voltage gains, and closer current or voltage following, or lower output impedance than would be the case if a single transistor were used. It should be noted, however, that in order to obtain a desired improvement of one characteristic, another characteristic is sacrificed, and that a type of pair is selected for any given application so that the sacrificed characteristic has least import in the circuit's operation.

22. The pairs shown in Fig.8a and 8b are employed where high current gain and low output impedances are required. The properties of these formations differ from those of a single transistor mainly in their very high current gain. In Fig.8a the stabilised relationship is input voltage to emitter voltage and this emitter voltage follows the input voltage separated by twice V_{be} (approximately 0.6V). The dotted resistor is sometimes included to stabilize the current from changes in temperature in cases where the source impedance at the input is high.

23. Fig. 9 shows an arrangement of complementary transistors (p.n.p. - n.p.n.). Fig. 9b is simply an inverted form of Fig. 9a. These pairs behave in a very similar manner to those of Fig. 8a but the output voltage is separated from the input voltage by only V_{be} (0.3V). The pairs are also much less conscious of temperature change. In both Fig. 9a and 9b arrangements the internal feedback (which is shunt-derived and series-applied) stabilizes the relationship between input voltage and emitter voltage.

24. Fig.10 shows another emitter-follower arrangement employing complementary transistors. Circuit values are included to indicate their comparative order and to show the exact symmetry which the circuit demands. Application of an input voltage causes no change in the p.d. between two transistor bases, since both bases are driven in the same direction through equal excursions dependent on the equal ratios R1:R5 and R3:R6. Thus it follows that, provided that the load impedance is large compared with the output impedance of the circuit, the common emitter current remains constant and the output voltage assumes the mid-point potential between the two bases, which is the level applied to the input. The arrangement is excellent for a number of reasons; voltage follow is much more exact, since it is without the normal V_{be} separation of the ordinary emitter-follower, and the output level is unaffected by temperature changes, since a change in V_{be} of one transistor tends to be cancelled by a similar change in the other.

25. Fig.11 shows a current-follow device in which the input and output currents are to all intents and purposes equal. In a normal single transistor common-base stage, the collector current is smaller than the emitter current by an amount equal to the base current; in this arrangement the base current of the first transistor is fed to the emitter of the second, and therefore appears almost intact in the output. This is the common-base configuration of the arrangement shown in Fig.8b, which is virtually the same device in common-emitter configuration.

26. In Fig.12 two arrangements of another transistor pair are shown, one using similar transistors and the other using complementary transistors. The arrangement gives input and output impedances of a common-emitter stage at middle frequencies, while at frequencies nearer the upper operating limits of the transistors employed, the arrangement gives input impedances of the common-emitter configuration and the high output impedances of the common-base configuration. The insertion of a resistor (not shown) between emitters permits emitter current, and therefore output current, to be defined for a given input voltage. The use of similar transistors in this application demands the addition of a bias resistor which determines the current to be shared by the two emitters; in fact, this arrangement is a disguised short-tailed or long-tailed pair.

27. A short or long-tailed pair is normally drawn in the manner shown in Fig.13a. The current drawn through the common impedance in the emitter circuit (the 'tail') splits between the two transistors according to the different voltages applied to the bases. Provided that both transistors are conducting, an increase of current drawn by one transistor will be matched by a corresponding decrease of current drawn by the other transistor. This change is determined by the difference between the applied inputs, and the arrangement performs as a 'differential' amplifier.

28. The 'length' of a tail implies both the magnitude of the common emitter impedance and the p.d. across it, which of necessity are inter-related and defined by the supply voltage available and the current required. Ideally the emitters should receive a constant-current supply, so that an identical change on the levels at both bases causes no change to either collector potential. Very effective current feeding is obtained by inserting a further transistor in the 'tail' (Fig.13b); this has the advantage of enabling the emitters to be fed with a comparatively large current at high impedance without the necessity of a large voltage supply and consequent high power consumption.

29. An important aspect of the long-tailed pair is its temperature stability; changes in temperature affect equally the V_{be} of each transistor, giving rise to a state which may be likened to a push-push input, thus causing the division of 'tail' current between transistors to remain unchanged.

30. This device is employed in a variety of applications: it may be used in comparator circuits to detect the difference between two signals, or to compare one input against a steady reference potential. Most amplifiers actually compare the input with earth level, so that this arrangement is frequently employed as an input stage with earth level applied to the reference input, especially in d.c.-coupled amplifiers where temperature stability is important. Another advantage is that the device provides opposed outputs, one from each collector, and thus may be used as a phase-splitter, or (using one or other output) an inverting or non-inverting amplifier.

31. The output levels corresponding to zero input (or zero differential input) may be set by means of either a small input applied to the reference input or by a small potentiometer connected between the two emitters as shown in Fig.13b.

32. The circuits in Fig.13 have been considered only in terms of small voltage inputs. By applying larger inputs, the circuit can be made to change rapidly from a state where one transistor is taking all the available current to a state where the other transistor draws all the current, giving a step voltage output of defined amplitude. This application may be employed when comparing a run-down with a reference potential; as the run-down passes through the reference level, the conditions of the transistor change over to produce a step coincident in time with the instant the input assumes the reference level.

33. The arrangement shown in Fig.14 comprises an emitter-fed (Fig.14a) and a base-fed (Fig.14b) pair in which the output voltage is applied across the

equal series-connected resistors so that half appears across each transistor. Since both transistors draw (to all intents and purposes) identical collector currents, each transistor will also dissipate internally half of the total power applied.

ELECTRONIC SWITCH

34. The electronic switch employed in a number of places in this equipment performs at high speed the function of a single-pole, two-way or multi-way switch. It is operated by a series of related switch waveforms, each of which alternates between $-5V$ ('on') and $+5V$ ('off'); these waveforms are related by arranging that one, and only one, is 'on' at any one time.

35. The diagram (Fig.15) shows the arrangements of a switch; only one 'way' is shown in detail.

36. Each 'way' of the switch comprises a $2.6mA$ constant-current transistor, a switching transistor (to which the switch waveform is applied) and a pair of diodes. In addition there is one $1.3mA$ constant-current transistor forming the pole.

37. When a given 'way' is 'on', the switching transistor is cut off and the $2.6mA$ divides equally between the two diodes, half flowing to the 'pole' transistor and half to the low-impedance signal input. Since the diodes carry equal current and are oppositely connected, the level at the signal input is passed to the output.

38. When the 'way' is 'off' (which means that one of the other ways is now 'on'), the $2.6mA$ is diverted to the switching transistor and both diodes are cut off, while the 'pole' transistor draws its $1.3mA$ from the 'on' way.

39. The additional diode in series with the switching transistor emitter protects this transistor against excessive back-bias.

40. It should be noted that in the arrangement of Fig.15 at least two 'ways' must be employed. If only one way is required, the signal input of the second is earthed. Failure to earth this input would result in the output being driven towards $-6V$ (the potential on the base of the 'on' way constant-current transistor).

41. Another arrangement is shown in Fig.16 which is similarly operated by a series of related switch waveforms. The circuit takes the form of a number of 'ways', each comprising a pair of similar transistors, one acting as a switching transistor and the other as a signal-transmitting stage. The pole is formed by a resistor common to all 'ways'.

42. When a given way is 'on', the switching transistor is cut off by a negative switching level applied to its base, and the current flowing in the signal stage is determined by the level of the signal input and the impedance of the resistor in the emitter circuit. The output therefore consists of an inverted version of the input at an amplitude dependent on the magnitudes of the emitter resistor and the common 'pole' resistor.

43. When the way is 'off' (which means that one of the other ways is 'on'), the base of the switching transistor is driven positive, causing the switching transistor to conduct and pull the emitter of the signal stage positive by almost the same amount, thus cutting off that stage.

44. It can be seen that a given way can have a gain factor greater or less than unity if required, and that the output is both inverted and at a different operating level.

45. The arrangement bears close comparison, from the angle of circuit configuration only, with the transistor pairs described in para. 26 to 32. The switch circuit just described depends for its action on having a comparatively short 'tail' in order that the signal stage may act as an amplifier.

ELECTRONIC GATE OR INHIBITOR

46. The electronic gate or inhibitor performs at high speed the function of a single-pole one-way switch, i.e. a simple on/off switch. Fig. 17a, b and c show three simple gate circuits, each of which is operated by a pair of opposed gate waveforms, which in this equipment normally alternate between the levels of +2V and -2V.

47. The simplest arrangement is shown in Fig. 17a. Four switching diodes are employed and the applied opposed waveforms supply both the forward current for the 'on' condition (transmit) and the reverse bias for the 'off' condition (inhibit). Theoretically, in the 'on' condition all diodes draw equal current, and since each pair of diodes is oppositely connected between input and output, the output level will assume the level of the signal input.

48. In the arrangement shown in Fig. 17b the 'on' condition obtains when the gate waveform is such that MR1 and 2 are reversed-biased and MR3 and 4 draw current through the resistors linked to positive and negative potentials. The device is 'off' when the gate waveform pairs reverse their polarity; MR3 and MR4 are then cut off by gate waveform potentials applied via MR1 and MR2 respectively.

49. Fig. 17c is a logical development of Fig. 17b, the diodes having been replaced by transistors and the necessary supply voltages and bias resistors added. This arrangement has much less loading effect on the gate waveforms and is considerably faster in action. Attention is drawn to the fact that the circuit is that of Fig. 10 with the addition of the two gating transistors.

BISTABLE CIRCUITS

50. The basic arrangement of a bistable is shown in Fig. 18. This device is employed to generate a rectangular waveform whose leading and trailing edges coincide in time with the application of two trigger pulses.

51. The resistors of this circuit are so chosen that when one transistor is conducting its collector is 'bottomed' and so holds the base of the other transistor well below cut-off. Since d.c. coupling is employed, the circuit is stable in this condition. A trigger pulse which causes the other transistor to conduct will initiate a rapid changeover, positive cross-feedback occurring so long as both transistors are conducting. A second stable state is then reached with the other transistor conducting and the first cut off. It will be observed that a pulse applied at 'trigger 1' or 'trigger 2' will be effective only if it is of the correct polarity to cause changeover.

52. The rectangular output waveforms are complementary and therefore may usefully be employed as switch or gate waveforms. The two fixed d.c. potentials between which these outputs alternate are defined accurately; the positive level is held at the potential determined by the steady current in a potential divider network and the negative level is held at the base potential of the related transistor, which in turn is determined by the steady current flowing in the other potential divider network.

53. Several refinements may be added. Emitter-followers are often used to provide low-impedance outputs, and capacitors are connected across the collector-base resistors to accelerate changeover. Another refinement consists of applying the triggers to the two inputs, each through a separate gating diode controlled by the associated output; this ensures that the trigger input to the conducting transistor is inhibited. If the triggers are inhibited in the manner just described, the circuit may be used as a divide-by-two device; in this application a common trigger pulse train is fed to both inputs, and alternate pulses act as trigger and reset trigger.

MONOSTABLE CIRCUITS

54. The monostable circuit consists basically of a bistable in which one of the feedback resistors (or resistor/capacitor) is replaced with a capacitor (Fig. 19). The stable condition is that in which the right-hand transistor in

the diagram is conducting and the left-hand transistor is cut off by virtue of its base potential being held well below cut-off. In this condition the capacitor is charged to the p.d. across the base bias resistor.

55. The application of a positive trigger pulse, of sufficient amplitude to cause the first transistor to commence conduction, results in an accelerated changeover of the transistors' respective conditions, with the base potential of the right-hand transistor well below cut-off. This state is unstable however, since the coupling capacitor will commence to discharge, causing the base potential to rise comparatively slowly until a point is reached when the right-hand transistor commences to conduct. At this point the positive loop feedback rapidly returns the circuit to its stable condition.

56. The time taken for the circuit to reset itself is determined by the timing components (C and R) according to the normal laws governing the behaviour of CR networks.

57. Monostable circuits such as this are very often employed as elements in electronic delay circuits. In this use, the recovery interval is adjusted to equal the required time delay, and the 'reset' or trailing edge of the output waveform becomes the new timing edge; this edge may be used direct, or differentiated to trigger a pulse generator, the output of which becomes the new delayed pulse.

ASTABLE CIRCUITS

58. The basic astable circuit comprises a bistable circuit in which both feedback resistors have been replaced with capacitors (Fig. 20). Thus the circuit has no stable condition and alternates continually between two states. According to the values of CR time-constants employed, the output may be a square wave or a waveform with a wide mark-space ratio.

ZENER DIODES

59. Zener diodes are used in a variety of applications, all of which utilize the typical Zener characteristic. This comprises a well-defined discontinuity in the relationship of reverse voltage to reverse current, beyond which the current increases sharply with increase of voltage and yields very low slope resistances.

60. The most common use of Zener diodes is in deriving reasonably stable reference voltages against which other potentials are compared, as in voltage regulators.

61. Another use of Zener diodes is in voltage limiters; the diodes are used singly or connected back-to-back according to the required limits. (It will be noted that with forward bias the Zener diode will behave as a normal diode).

62. One of the problems associated with transistor circuits is that signal-to-supply voltage ratios may be very high. Such ratios demand unusually efficient decoupling to ensure that the supply line is pulse-free, which in turn necessitates the use of large capacitors. By replacing these capacitors with suitable Zener diodes steadily biased to conditions of low-slope impedance, identical decoupling efficiency may be obtained with considerable saving in both space and cost.

63. Zener diodes are used also where two points at different potentials are required to be d.c. -coupled without attenuation of a signal transmitted from one to the other. Here the diode acts as a low-resistance transmission element while maintaining the difference in potential between the two points. In assessing the d.c. conditions of two networks linked to one another in this way, it is helpful to regard the diode as a simple battery.

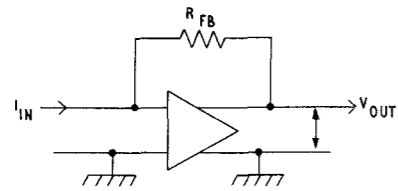


FIG.1 BASIC FEEDBACK AMPLIFIER

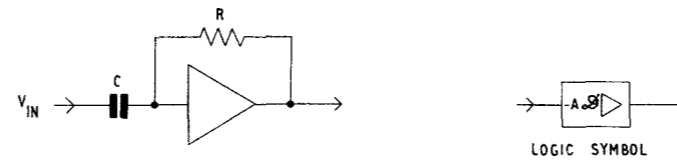


FIG 6 OPERATIONAL DIFFERENTIATOR

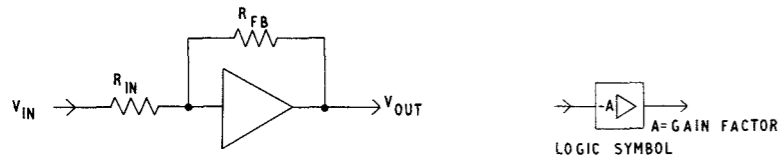


FIG. 2 OPERATIONAL AMPLIFIER

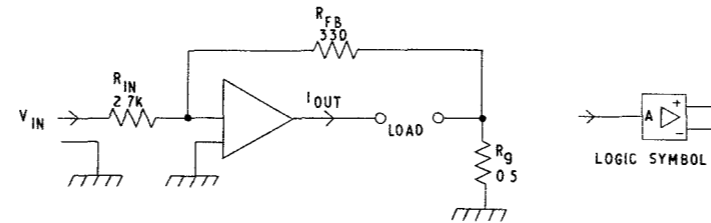


FIG 7 CURRENT CONVERTER

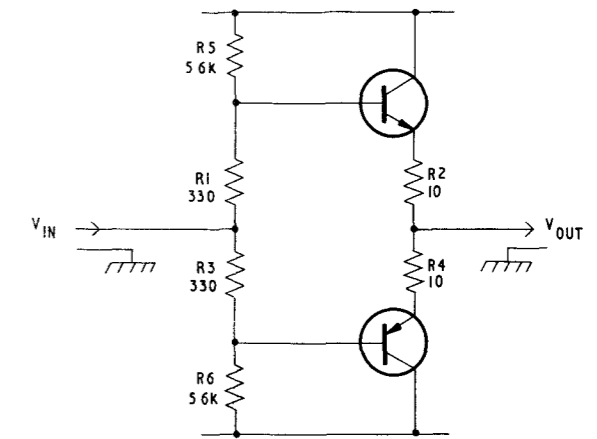


FIG 10 COMPLEMENTARY TRANSISTOR EMITTER FOLLOWER

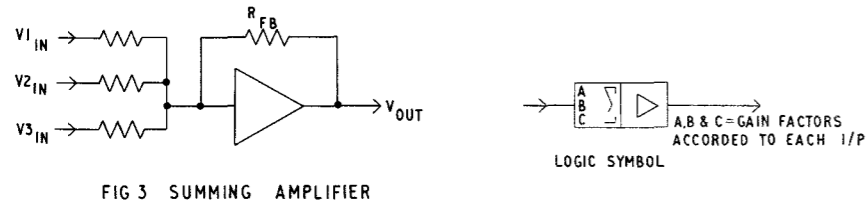


FIG 3 SUMMING AMPLIFIER

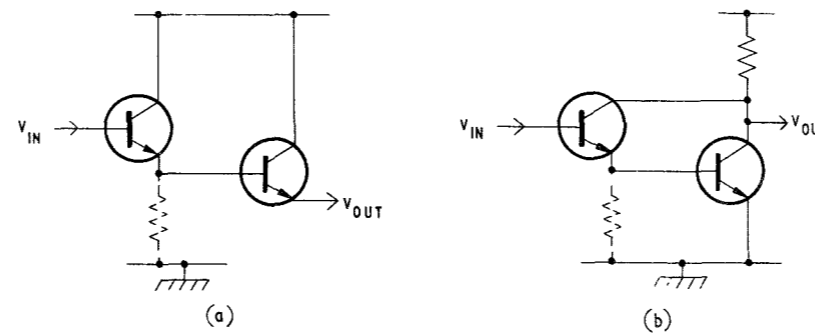


FIG 8 TRANSISTOR PAIRS

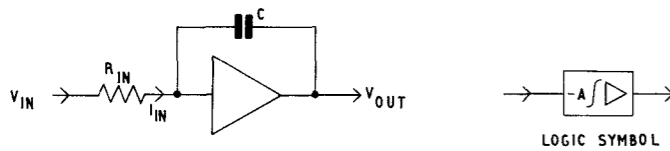


FIG.4 OPERATIONAL INTEGRATOR

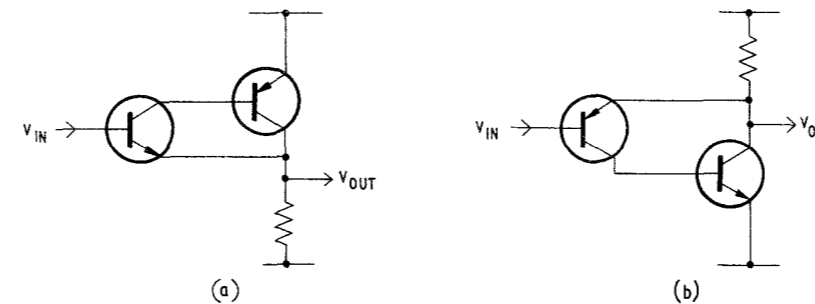


FIG.9 COMPLEMENTARY TRANSISTOR PAIRS

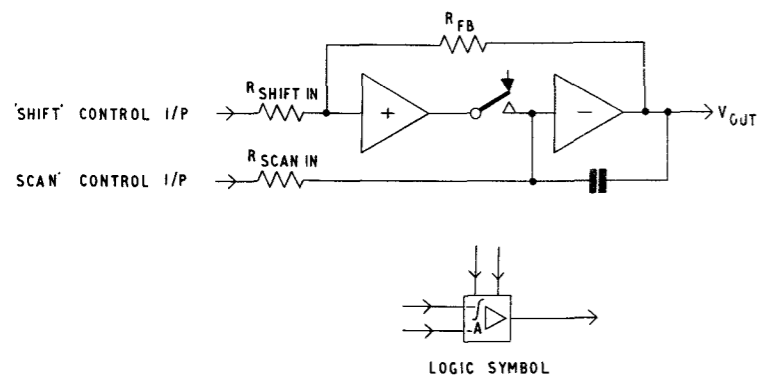


FIG 5 SHIFTING INTEGRATOR

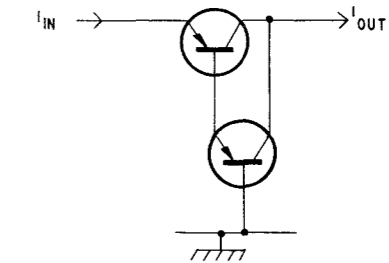


FIG 11 CURRENT FOLLOWER (1)

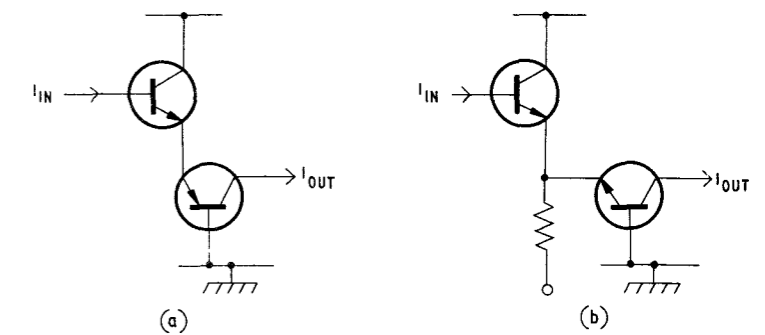


FIG 12 CURRENT FOLLOWER (2)

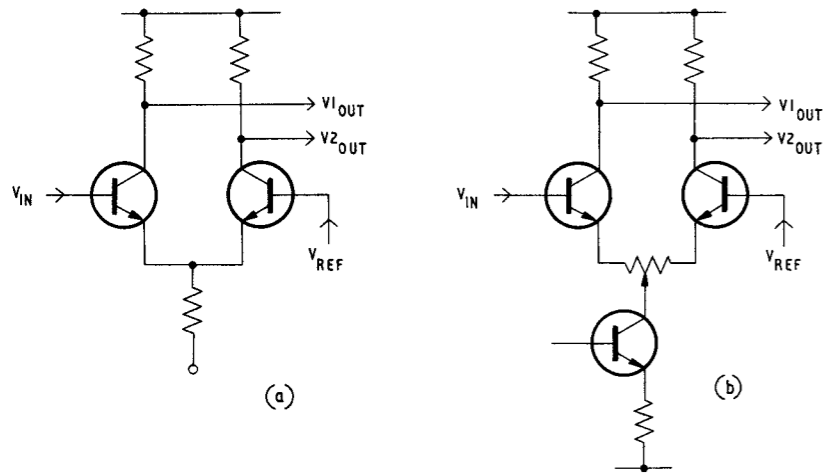


FIG 13 TRANSISTOR LONG-TAILED PAIR

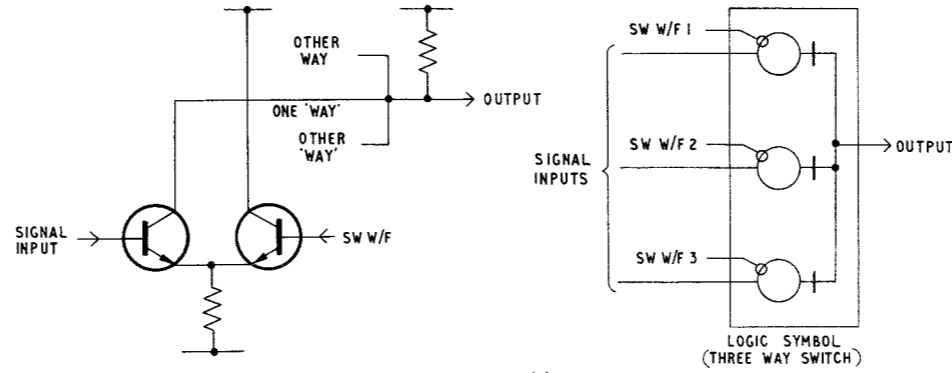


FIG 16 ELECTRONIC SWITCH (2)

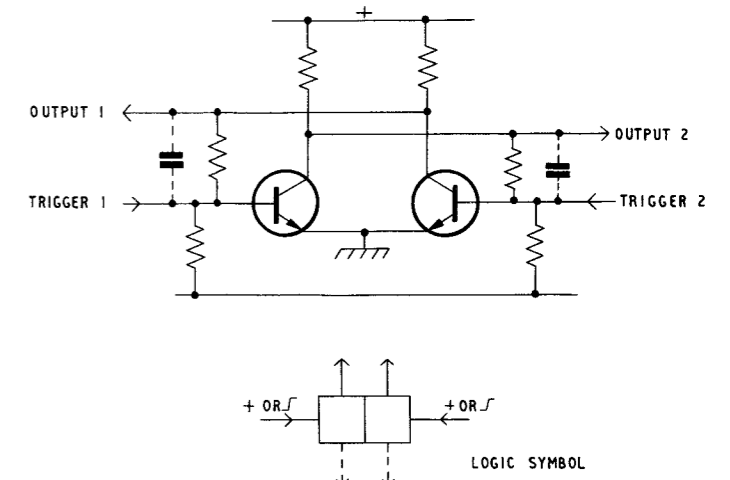


FIG 18 BASIC BI-STABLE ELEMENT

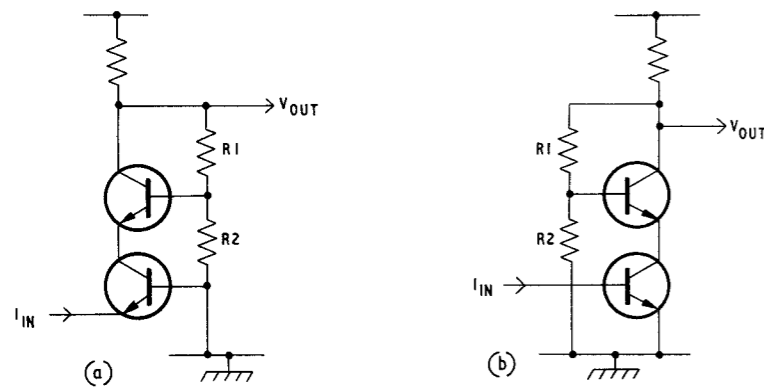


FIG 14 SERIES OPERATED TRANSISTORS

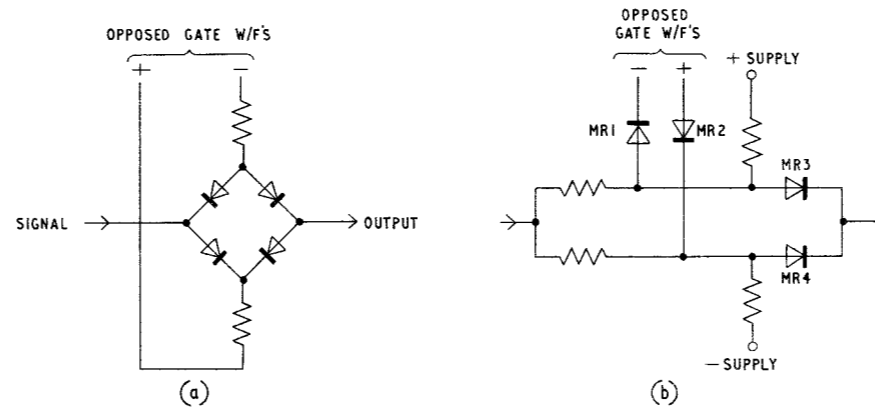


FIG 17 ELECTRONIC GATE OR INHIBITOR

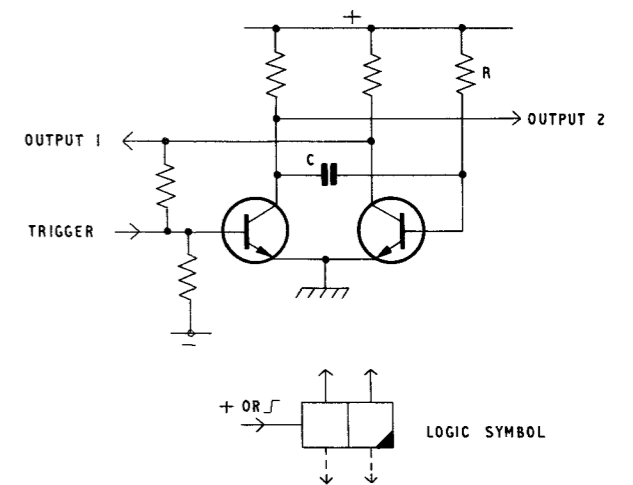


FIG 19 MONOSTABLE ELEMENT

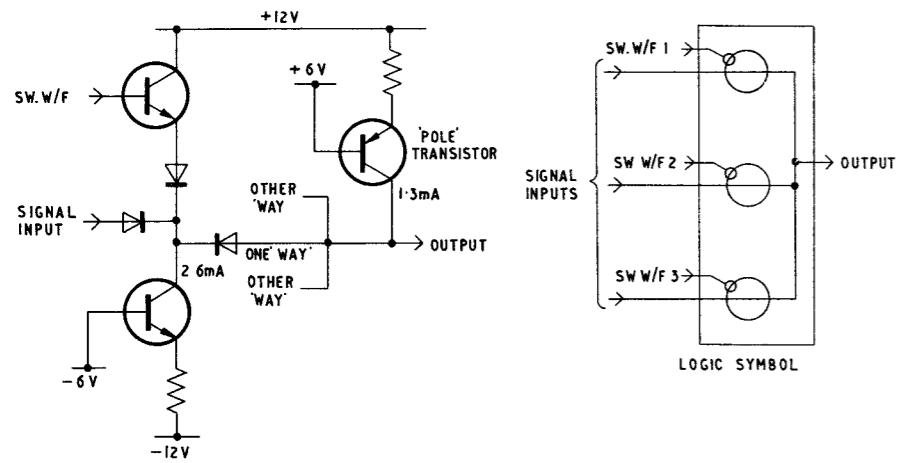


FIG 15 ELECTRONIC SWITCH (1)

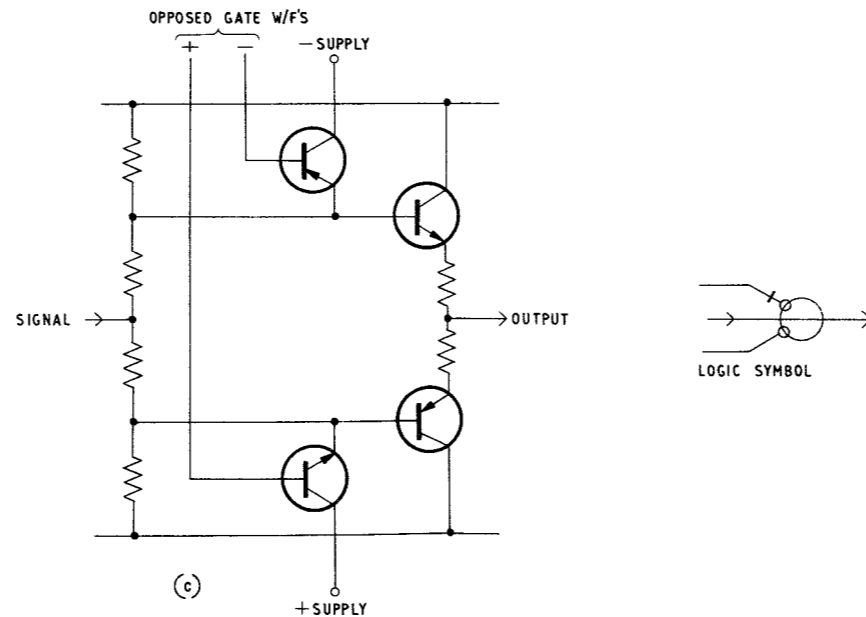


FIG 20 ASTABLE ELEMENT

TECHNICAL INFORMATION

UNITS

CHAPTER 1

POWER UNIT 11600

LIST OF CONTENTS

	Para.
INTRODUCTION	1
CIRCUIT DESCRIPTION	
Mains supply circuits	8
Unregulated supplies	12
The stabilised supply	16
Regulated supplies	17

LIST OF ILLUSTRATIONS

	Fig.
Power Unit 11600: component location	1
Power Unit 11600: stabiliser board	2
Power Unit 11600: rectifier board	3
Power Unit 11600: circuit Part A	4
Power Unit 11600: circuit Part B	5
Power Unit 11600: circuit Part C	6

INTRODUCTION (Fig.1)

1. The power unit operates from a 200-250V r.m.s, single-phase, 45-55Hz supply and provides all the power supplies required by the viewing unit. The tapings of the mains transformer are adjusted to the nominal supply voltage and the unit provides the following supplies:-

- (1) 6.3V r.m.s. at 2A maximum.
- (2) +100V d.c. stabilised at 100mA maximum.
- (3) +12V d.c. regulated at 1A maximum.
- (4) +6V d.c. regulated at 1A maximum.
- (5) -6V d.c. regulated at 1A maximum.

- (6) -12V d.c. regulated at 1A maximum.
- (7) 24V d.c. unregulated at 1A maximum (floating).
- (8) +15V d.c. unregulated at 2.5A maximum.
- (9) -15V d.c. unregulated at 4.5A maximum.

The common line is isolated from the chassis earth and must not be earthed to the metal work at any point in the viewing unit; it is connected via the signal earth line to earth at one point only at either the radar transmitter or the central equipment rack.

2. The regulated supplies are protected against overloads by transistor-operated overload circuits. The stabilised 100V supply is not protected against overloads except by its comparatively high output impedance. Overload cut-outs are fitted to the mains supply line and to the three unregulated supplies. These four cut-outs are fitted with mechanical release and reset buttons.

3. A thermostat (cut-out X1) is fitted to the power unit back-plate which operates at a temperature of 65°C and interrupts the supply to the solenoid of the main circuit breaker on the control panel. This switches off the display. The power unit back-plate will reach this temperature only if a fault develops in the cooling system, or if the power unit is not properly secured to the power unit cold-plate.

4. The larger components of the power unit circuit are mounted on an aluminium back-plate; this plate serves as a high thermal capacity heat sink, and it is in physical contact with a cold-plate when fitted in the viewing unit.

5. The components mounted on the back-plate include two chokes (L1 and L2), a cut-out (X1) between these chokes, mains transformer T1 and eight electrolytic capacitors (C11 to C18). Further components are mounted on brackets secured to the back-plate; these are four cut-outs (X2 to X5) and six 10-way taper pin terminal strips (TSA to TSF) through which the external connections are taken.

6. Two printed wiring boards are secured to opposite edges of the back-plate and at right angles to it. These are the rectifier board and the stabiliser board. An 8-way test point connector is positioned along the top edge of the stabiliser board and this is easily accessible within the viewing unit.

7. Two guard bars, one at either side of the power unit, enable the unit to be placed in any position on the bench without damaging the components. The right-hand guard bar is engraved with the functions of the preset controls mounted on the adjacent stabiliser board.

CIRCUIT DESCRIPTION

Mains supply circuits (Fig.4)

8. The power unit terminal strips A and B are used to distribute the mains supply within the viewing unit. The circuits external to the power unit differ between displays and will not be described in this chapter. The connections to the power unit transformer are made through terminal strip F and the transformer tapings are set to correspond with the nominal supply voltage by two links from F9 (line) and F10 (neutral).

9. The mains supply enters the unit via A7 (line) and A9 (neutral). The circuit from A7 is fed out of the unit via B7, through the main circuit breaker, back into the unit via B6 and then via the mains overload cut-out X2 to F9.

10. The overload cut-out X2 is rated at 2.5A and is operated by a heater strip only. This introduces a slight time lag and the cut-out does not operate on transient current surges. (The cut-out is fitted with an electromagnetic release coil, but this is not used.) The cut-out can be released and reset by two push-buttons on the outside of the unit. The thermostat X1 has a pair of normally-closed contacts which open at a temperature of 65°C and close automatically when the temperature falls again. The thermostat is in thermal contact with the power unit back-plate. The effect of either the mains overload cut-out or the thermostat contact's opening is to release the main circuit breaker and switch off the display.

11. The coolant pump and cooling fan operate from a 225V r.m.s. supply. The 225V supply is obtained from the -5V and 230V taps on the power unit transformer and fed to the pump via A3 and A5, and to the fan via B3 and B5.

Unregulated supplies (Fig.1)

12. The power supplies have separate secondary windings on the power unit transformer. A 6.3V a.c. supply is connected to terminals E8 and E9; C10 is connected across this supply to suppress transients. This supply is used for the c.r.t. heater and the viewing unit lighting circuits.

13. The 24V d.c. supply is rectified by the bridge rectifier circuit employing silicon diodes MR26 to MR29 and reservoir C17. C5 is connected across the supply side of the rectifiers to protect them from transients on the mains supply. The heater strip of the 2A overload cut-out X4 is connected between the rectifier and C17, and its magnetic release coil is in

series with the supply on the output side of C17. The heater strip operates the cut-out in the event of a large overload. The coil is connected after C17 so that pulses of short duration do not operate the cut-out. The cut-out carries two buttons which can be released or reset. This supply is used by the e.h.t. unit.

14. The +15V d.c. supply is rectified by the bridge rectifier employing silicon diodes MR30 to MR33 and smoothed by L2 and C18. R6 limits the voltage developed across L2 by rapid change of load current and C7 limits the amplitude of the transient voltage developed across the rectifiers. The heater strip of the 4A overload cut-out X5 is connected between the rectifier and the smoothing circuit, and the magnetic release coil is connected on the supply side of the smoothing circuit. This prevents the magnetic release operating on surges when the load current changes. This supply is used on viewing units fitted with a character drive unit and is not required on autonomous displays.

15. The -15V d.c. supply is rectified by the bridge rectifier circuit employing silicon diodes MR22 to MR25 and smoothed by L1 and C16. R5 limits the voltage developed across the choke by rapid changes of load current. The rectifiers are protected against voltage and current transients by C8 R3 C9, connected across the mains side of the rectifier bridge. The heater strip of an 8A overload cut-out is connected between the rectifier and the smoothing circuit and its magnetic release coil is connected on the supply side of the smoothing circuit. This prevents the cut-out operating on surges when the load changes. This supply is used by the deflection coil final drive amplifiers.

The stabilised supply (Fig.1)

16. The +100V d.c. stabilised supply is rectified by the full-wave rectifier circuit employing silicon diodes MR17 and MR18 and reservoir C15. The supply is stabilised at a nominal 100V by the Zener diodes MR19 and MR20 and series resistors R1 and R2. A stabilised supply at a nominal +18V is derived from this 100V supply by Zener diode MR21 and series resistor R4. This 18V supply is required by the regulator of the +12V regulated supply and is not a power unit output. The +100V supply is required by the output stages of the video board.

Regulated supplies (Fig.5 and 6)

17. The four regulated supplies employ similar circuits and only the circuit of the +12V supply will be described in detail (Fig.6).

18. The +12V supply is rectified by the bridge rectifier circuit employing silicon diodes MR1 to MR4 and reservoir C11. The rectifiers are protected against voltage transients by C1 connected across the supply side of the rectifiers.

19. The voltage across C11 is applied to a voltage regulator consisting of a series transistor whose impedance is controlled by a voltage comparator. The comparator compares a preset fraction of the output voltage with a fixed reference voltage (5.6V nominal) and adjusts the impedance of the series transistor to maintain a constant output voltage. A protection circuit is provided to limit the current drawn from the supply to a safe value.

20. TR1 is the series transistor and its base current is controlled by the voltage comparator and amplifier employing TR5, TR6, TR7, and TR2. TR3 is used in the overload protection circuit.

21. Zener diode MR34 provides a stable reference voltage having a value in the range of $5.6V \pm 5\%$. The temperature coefficient of a Zener diode varies with the current through it. Potentiometer RV2 is adjusted during manufacture to set the Zener current to the optimum value for the individual diode and should not be adjusted in service unless the diode is replaced.

22. The double transistor TR7 is connected as a long-tailed pair and used as a voltage comparator. The reference voltage is applied to base TR7a and a preset fraction of the output voltage, obtained from the potential dividing network R18, RV3, R19 is applied to base TR7b. The exact fraction of the output voltage applied to base TR7b is preset by adjusting potentiometer RV3. The output of the comparator stage is amplified by the long-tailed pair TR5/TR6 and the emitter-follower TR2. The emitter current of TR2 flows into the base of the series transistor TR1 and controls its collector/emitter impedance. Potentiometer RV3 is adjusted during servicing to set the output voltage.

23. The overload protection transistor TR3 is cut off during normal operation of the regulator. The base/emitter voltage of TR3 is the algebraic sum of the fraction of the output voltage across RV1 and the voltage developed across R9 due to the load current; the two voltages are of opposing polarities, and if the load current exceeds the full rated load, the voltage across R9 will exceed that across RV1 and TR3 will be turned on. The collector voltage of TR3 then falls towards the +12V output line and takes the base of TR2 with it. The emitter of TR2 follows its base and the base/emitter voltage of TR1 approaches zero, which raises its impedance and lowers the output voltage. The resulting fall in load current turns off TR3, so that the process continues only until the overload is removed. The effect of this circuit is to limit the current to a constant value and allow the voltage to fall if the rated output is exceeded. The current at which the overload circuit operates is set by adjusting potentiometer RV1.

24. The positive and negative supplies are interconnected through the external circuits and if the positive 12V supply fails, the negative supplies will try to drive current back into the regulator; diode MR35 is fitted to prevent this. MR35 is normally back-biased and has no effect, but if a negative voltage is applied to the +12V line, it conducts and connects this line to the common earth line and protects the transistors from damage.

25. The other regulated supplies employ similar circuits, except that the component values are different, and the power supply for the second long-tailed pair is different in each case, as follows:-

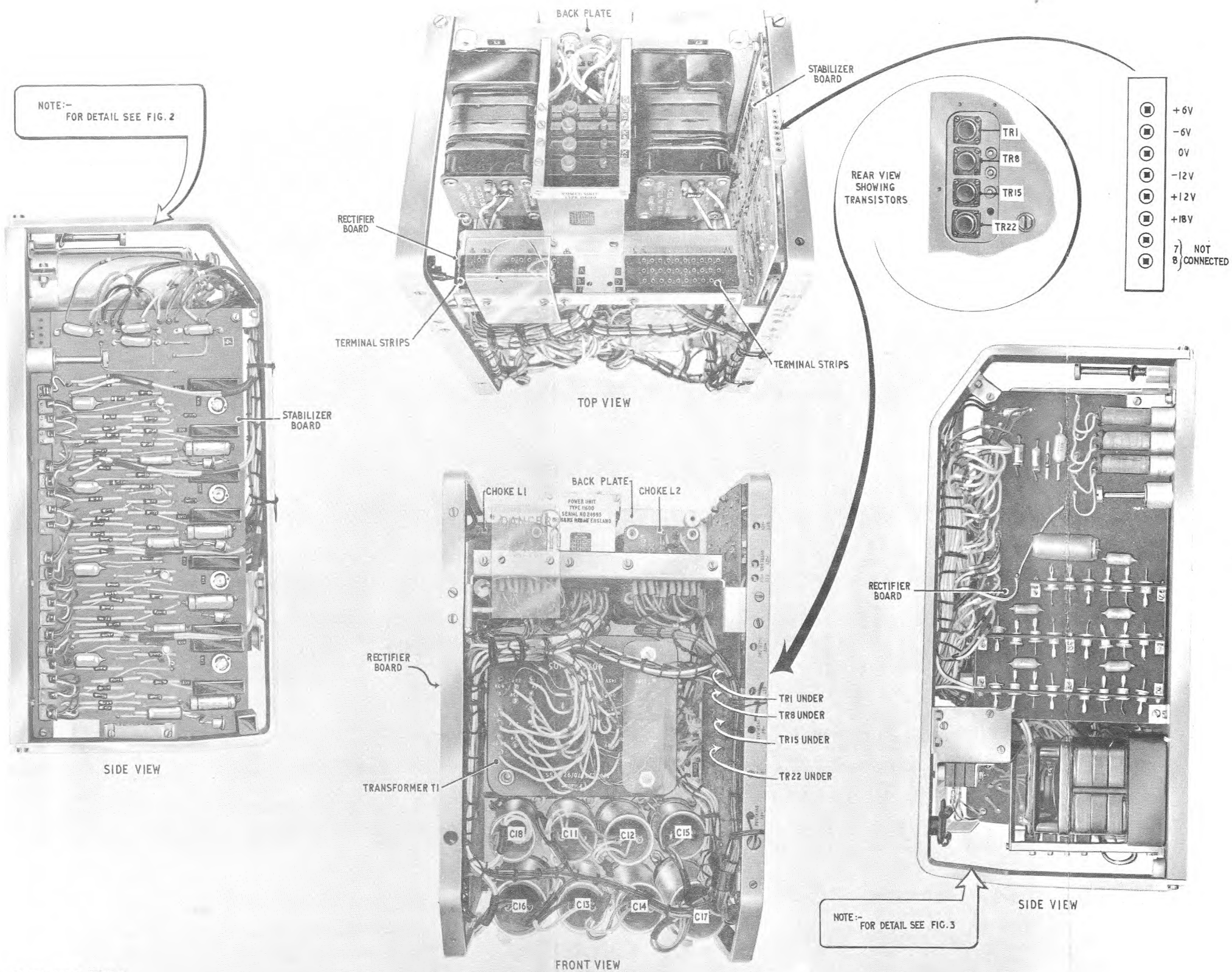
- (1) +12V regulator +18V stabilised supply.
- (2) -12V regulator +6V regulated supply.
- (3) +6V regulator +12V regulated supply.
- (4) -6V regulator +6V regulated supply.

It is apparent from this that the regulators are interdependent and a failure of one supply may affect the others.

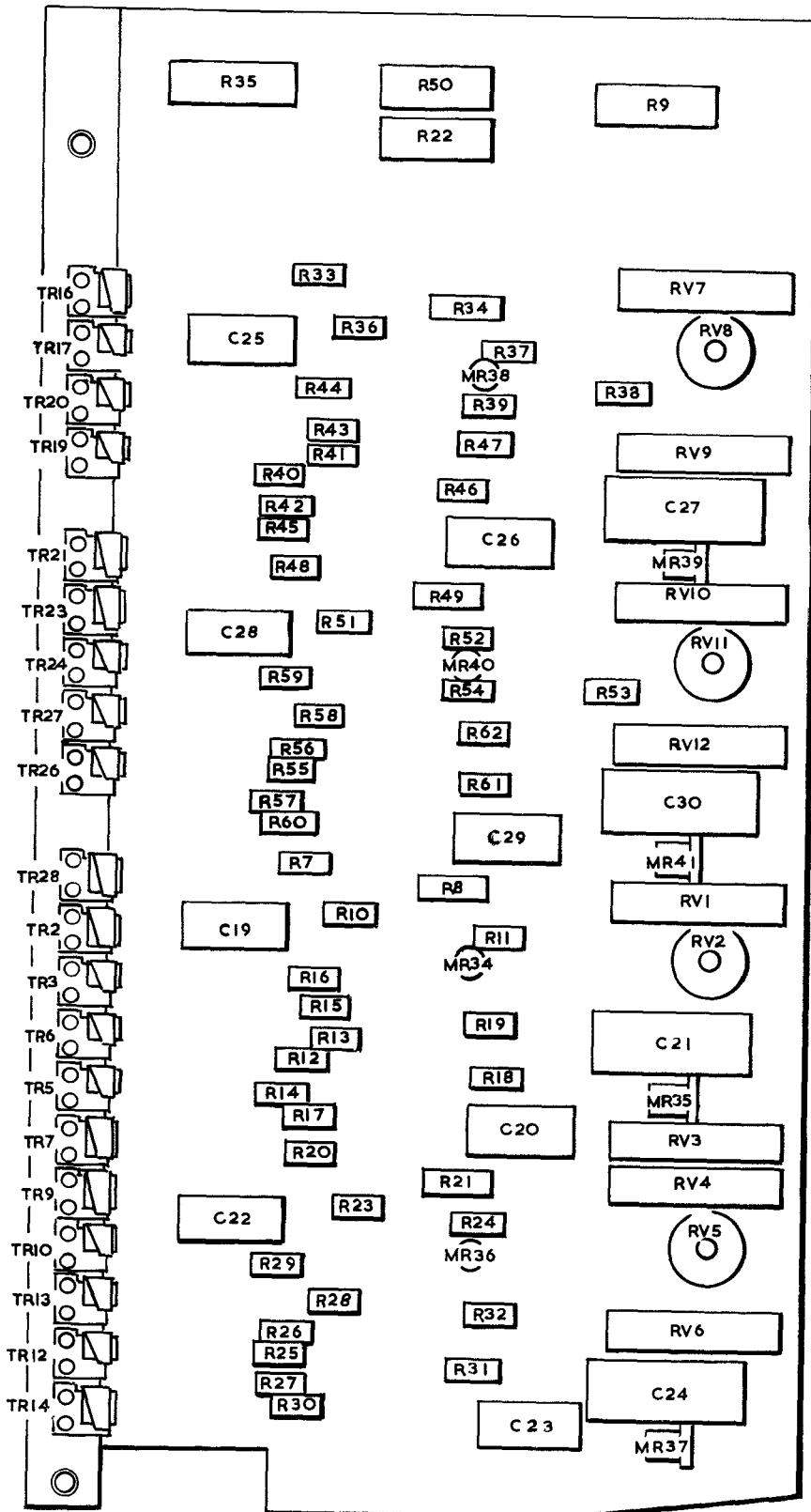
Monitoring points

26. The test point connector on the top edge of the stabiliser board (paragraph 6) carries test points 1 to 8, test point 1 being nearest the cold-plate. The following supplies can be monitored on the test points:-

Test point 1	+6V	Test point 5	+12V
2	-6V	6	+18V
3	0V	7	Not used
4	-12V	8	Not used

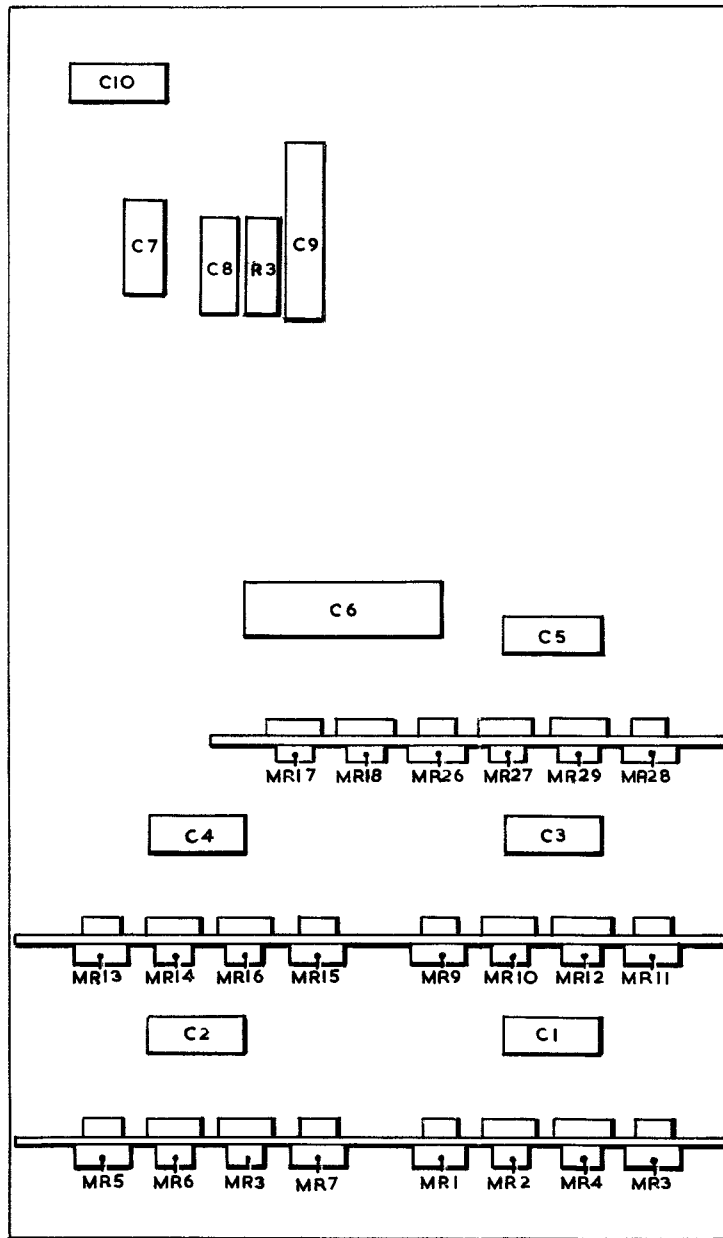


C/DD1/11600/G ISSUE 5
B/DD1/11600/H ISSUE 5



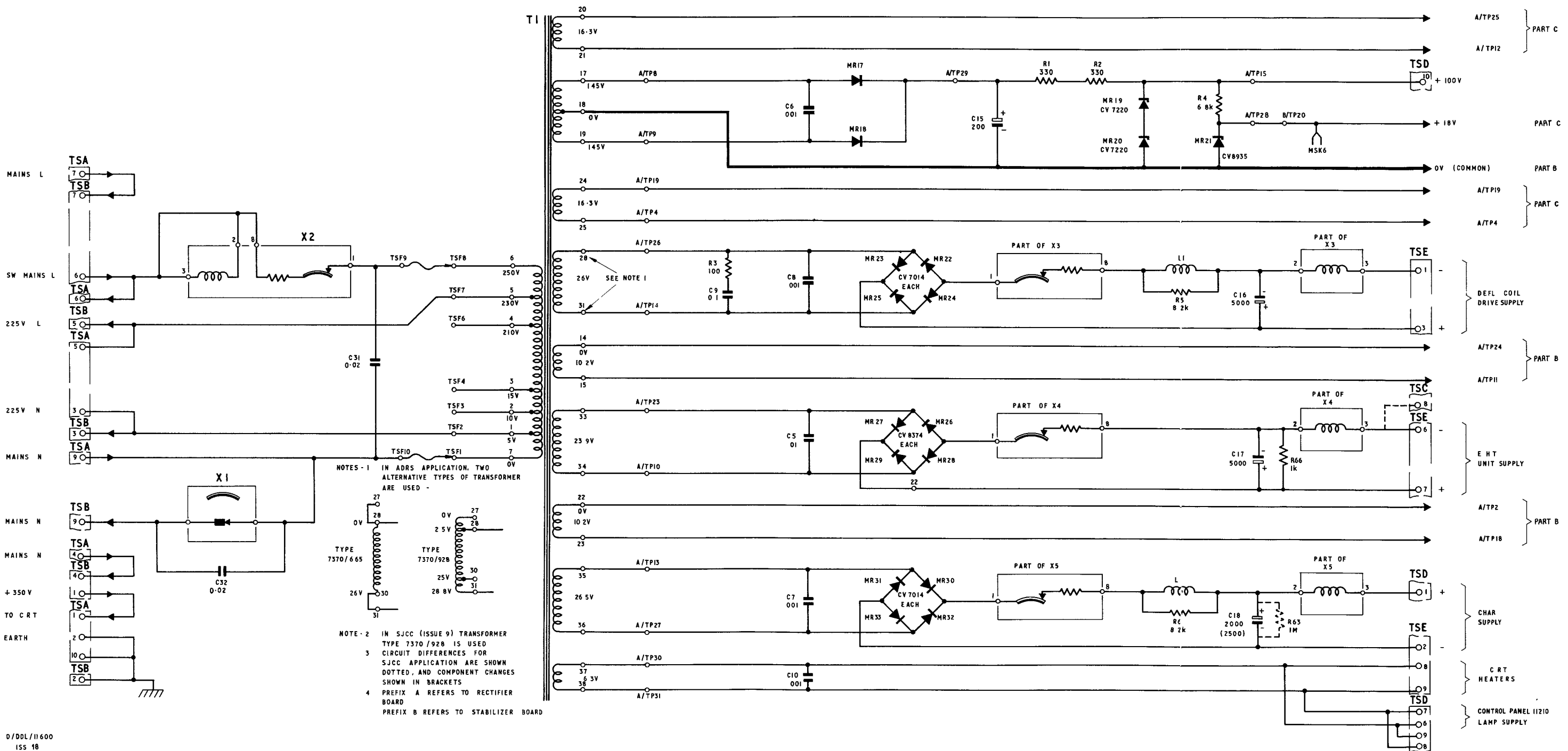
C/DDL/11600/G
ISSUE 5

Fig.2 Power unit 11600: stabiliser board



B/DD/11600/H
ISSUE 5

Fig.3 Power unit 11600: rectifier board



NOTES - 1 IN ADRS APPLICATION, TWO ALTERNATIVE TYPES OF TRANSFORMER ARE USED -

TYPE 7370/665	TYPE 7370/928
0V 27	0V 27
2.5V 28	2.5V 28
25V 30	25V 30
26V 31	28.8V 31

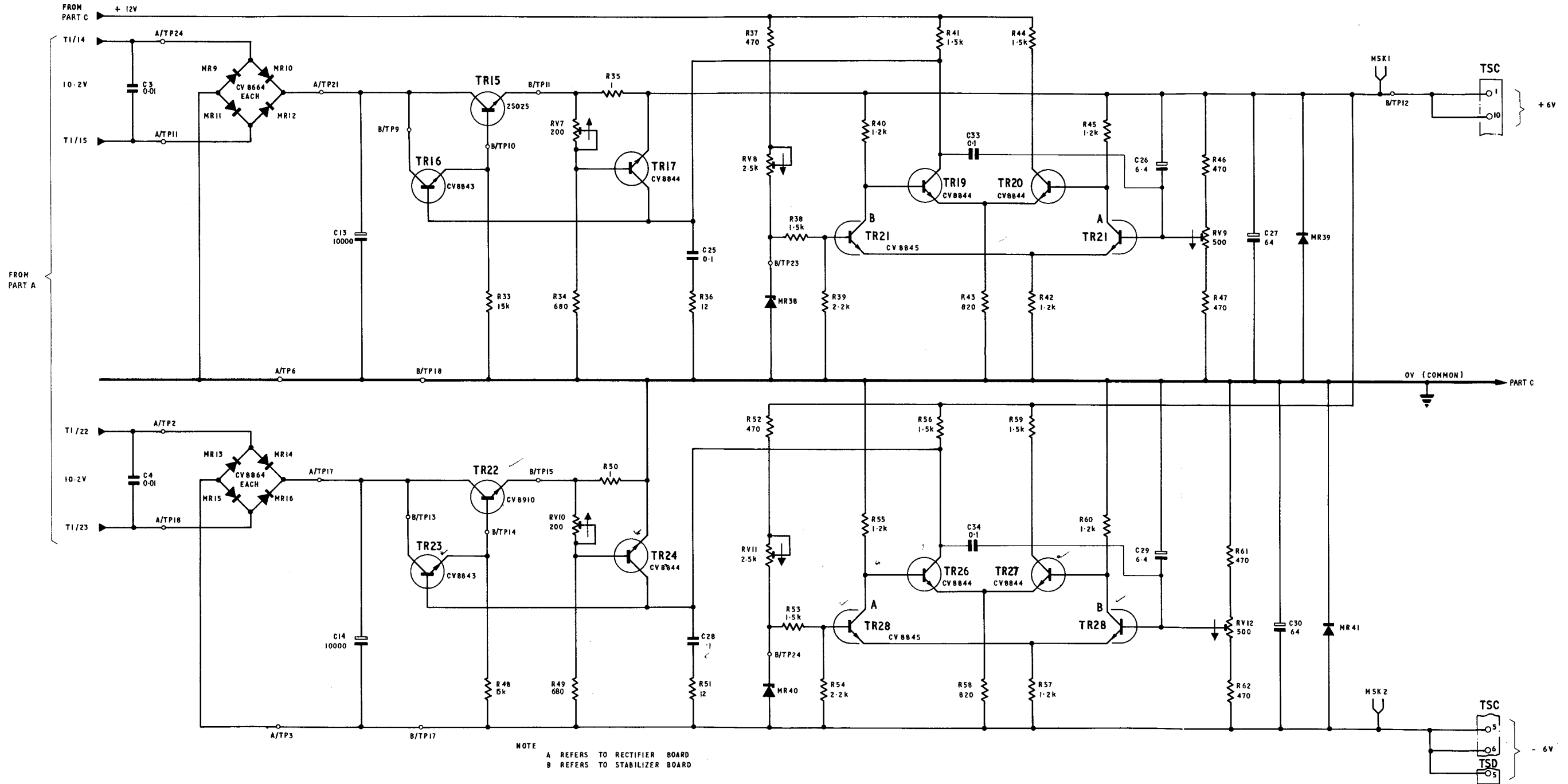
NOTE - 2 IN SJCC (ISSUE 9) TRANSFORMER TYPE 7370/928 IS USED

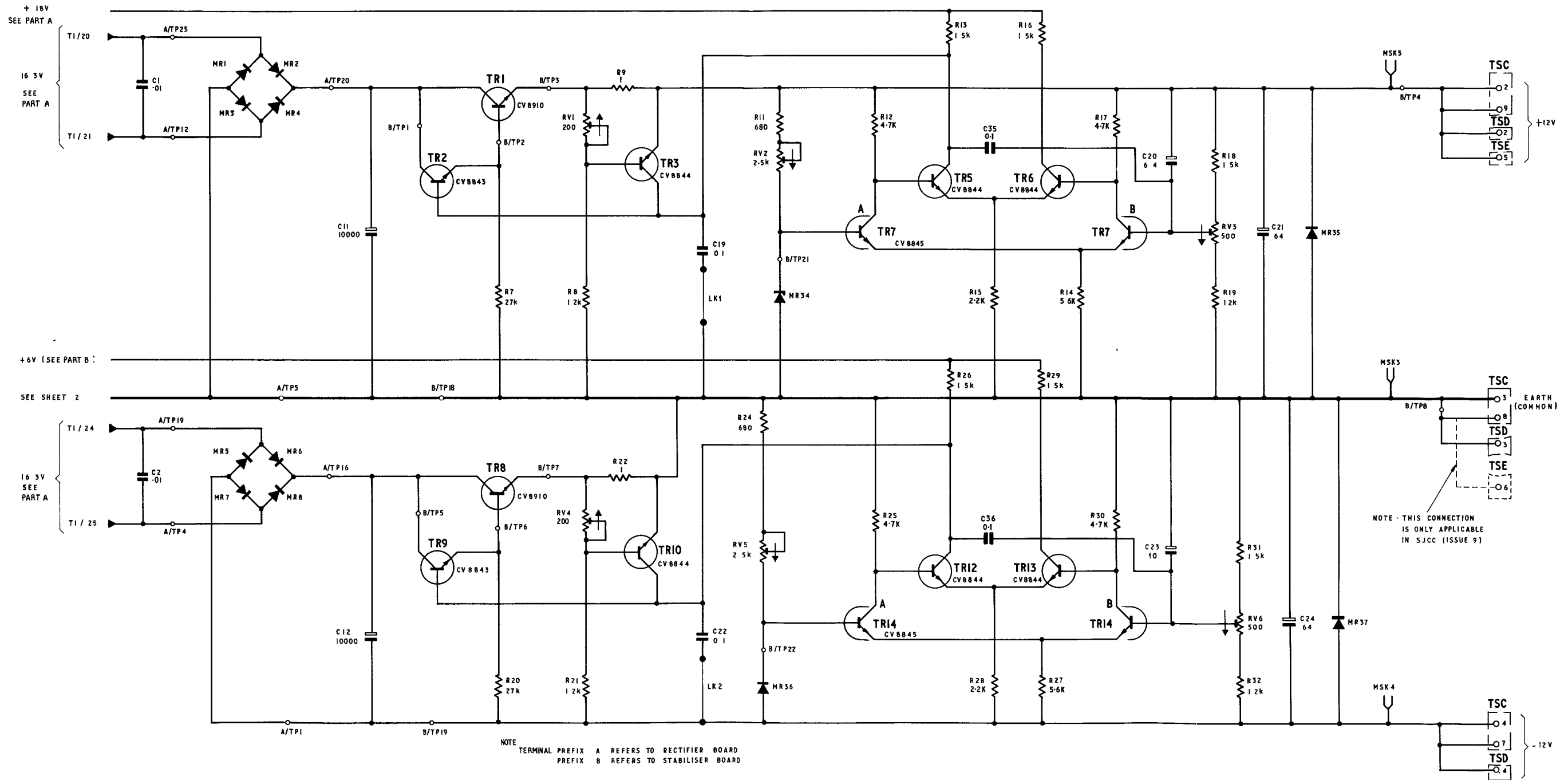
3 CIRCUIT DIFFERENCES FOR SJCC APPLICATION ARE SHOWN DOTTED, AND COMPONENT CHANGES SHOWN IN BRACKETS

4 PREFIX A REFERS TO RECTIFIER BOARD
PREFIX B REFERS TO STABILIZER BOARD

Power unit 11600 : circuit Part A

Fig.4





NOTE - THIS CONNECTION IS ONLY APPLICABLE IN SJCC (ISSUE 9)

D/DDI/11600
 1SS 18

Power unit 11600 : circuit Part C

A.L. 29, July 71

Fig. 6

Chapter 2

EHT POWER UNIT 11601

LIST OF CONTENTS

	Para.
INTRODUCTION	1
CIRCUIT DESCRIPTION	
Oscillator	7
320V supply	9
Regulator	10
Protection circuit	14

LIST OF ILLUSTRATIONS

	Fig.
EHT Power Unit 11601: component location	1
EHT Power Unit 11601: circuit	2

INTRODUCTION (Fig. 1)

1. The EHT power unit operates from a +24V d.c. supply obtained from Power Unit 11600. It provides a +15kV EHT supply for the final anode of the CRT and a +320V supply for the first anode.

2. The circuit used is a d.c./d.c. converter comprising oscillator and rectifier circuits. The d.c. input to the circuit (the supply to the oscillator) is controlled by a voltage regulator circuit, containing a comparator and amplifier, which compares a fraction of the EHT voltage with a preset reference voltage and adjusts the oscillator supply voltage to maintain the voltage output at a constant value.

3. The EHT transformer forms a part of the oscillatory circuit and has two output windings. The EHT winding is connected to a voltage-doubling rectifier circuit employing two thermionic diodes and an RC smoothing circuit. The second winding provides the 320V supply, and this is rectified by a silicon diode with a reservoir capacitor but no smoothing circuit.

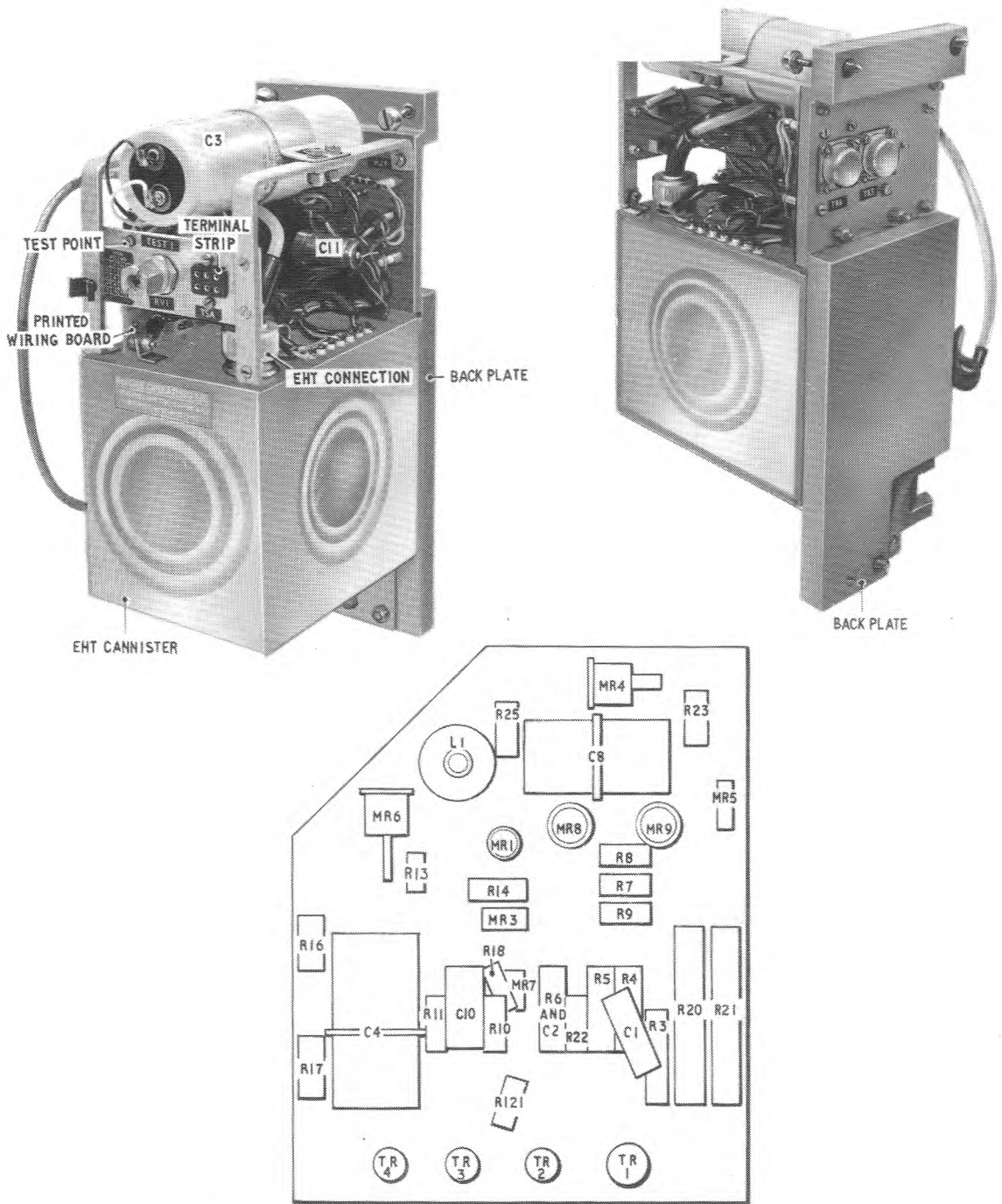


Fig.1 E.H.T. Power Unit 11601: component location

4. The components of the EHT power unit are mounted on an aluminium back-plate, which serves as a high thermal capacity heat sink. Three captive screws secure the power unit to the viewing unit, the back-plate then being in physical contact with a cold-plate.

5. The EHT canister is mounted on the lower part of the back-plate. This canister is vacuum oil-filled; it contains the transformer T1, rectifier valves V1 and V2 and associated smoothing components. Connection to the

CRT second anode is made via a fly-lead integral with the canister and connections from the canister to other power unit components are made via insulated feed-through tags.

6. The remainder of the components, including those on a printed wiring board, are mounted on the upper part of the back-plate. Two right-angles bars protect these components when the power unit is removed for bench servicing. A bracket attached to these bars carries the preset potentiometer RV1 (provided with a spindle lock), the Test Point 1 socket and a 6-way taper pin terminal strip TSA. External connections are made via the terminal strip TSA.

CIRCUIT DESCRIPTION (Fig. 2)

Oscillator

7. TR6 is operated as a class-C sinewave oscillator at a frequency of 10kHz. The amplitude of the collector voltage waveform is determined by the collector/emitter supply voltage, i.e. the p.d. across C3. This p.d. is in turn controlled by the voltage regulator circuit containing TR1 to TR5. Diode MR6 and inductor L1 prevent the maximum reverse base/emitter voltage being exceeded on negative half-cycles.

8. The amplitude of the oscillatory waveform at the collector of TR6 is of the order of 40V peak-to-peak and may be monitored at Test Point 1. The voltage on the EHT winding is approximately 7.5kV peak-to-peak, and this is rectified by two thermionic diodes connected in a voltage-doubling circuit and smoothed by the RC filter contained within the EHT canister. The EHT connector is a flying lead with a connector cap to fit the CRT anode terminal.

320V supply

9. The 350V supply is half-wave rectified by diode MR4, C4 being the reservoir capacitor. MR8 and MR9 (160V Zener diodes) in conjunction with R23 stabilize the d.c. output at 320V.

Regulator

10. The collector supply for the first three transistors of the voltage regulator is stabilized at a nominal 10V by Zener diode MR3.

11. The double transistor TR1 is connected as a long-tailed pair and

used as a voltage comparator. The base of TR1b is connected to a reference supply of 5.6V (nominal) provided by Zener diode MR1. The potential at TR1a base is set by a potential divider consisting of two 200Mohm resistors in the EHT canister together with R21 and R3, connected between the EHT line and the slider of RV1. Potentiometer RV1 is a part of a low-resistance potential divider (R7 RV1 R8) connected across the reference supply. The comparator compares a small fixed fraction of the EHT voltage (across R3) with about $\frac{3}{4}$ of the reference supply voltage (between the slider of RV1 and TR1b base). RV1 is used to set the EHT to its nominal value of 15kV, and a fine control of the EHT voltage is provided by a 'focus control voltage' obtained from the focus control on the viewing unit control panel and applied to TSA4.

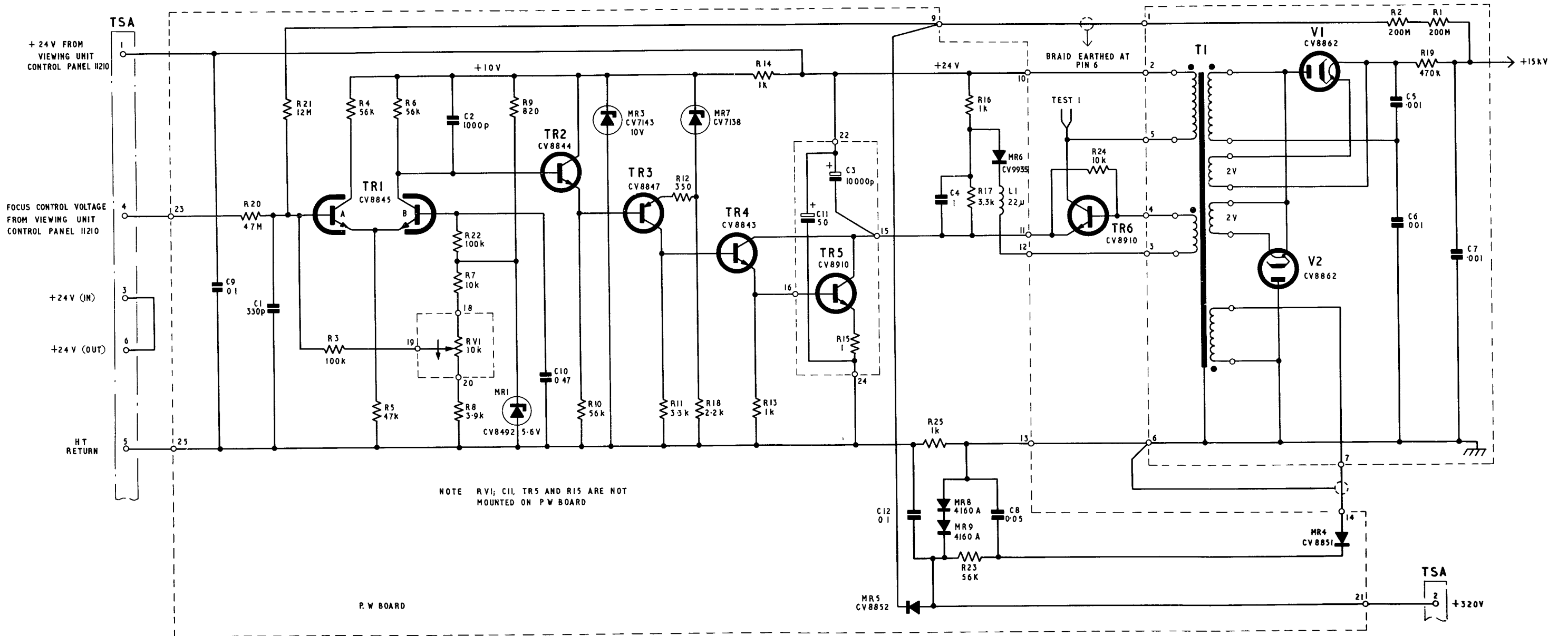
12. EHT control voltage is added via TSA4 and R20 to the voltage fed back via R1-2 and R21 to one input of the voltage comparator TR1. Variation of this voltage between $\pm 12V$ swings the EHT through approximately $\pm 1kV$. In some cases the input to TSA4 is controlled manually to adjust the focus; in other cases this voltage is fixed.

13. The output of the comparator stage is taken from the collector of TR1b and amplified by the emitter-follower TR2, the common emitter TR3 and the transistor pair TR4/TR5. The emitter of TR3 is held at a nominal 3.3V below the 10V line, by the Zener diode MR7, to improve the stability of the amplifier. The transistor pair acts as a common-emitter stage with high gain. The collector load of TR4, and TR5 (R16 and R17) is connected across C3. The voltage on C3 is therefore determined by the input to the comparator at TR1a base. C3 supplies the current pulses required by the oscillator TR6.

Protection circuit

14. The voltage at the junction R2/MR5 is of the order of 400V with the unit operating correctly. In these circumstances diode MR5 is back-biased and does not affect the operation of the comparator. However, the EHT cannot build up to its correct voltage until the heaters of the two rectifier diodes are at their operating temperature. During the warming-up period diode MR5 conducts and provides an input to the comparator consisting of a fixed fraction of the 320V supply voltage. This input holds the oscillatory voltage and the collector current of TR4/5 to safe levels until the diodes warm up and the EHT input takes control. If MR5 were omitted from the circuit, the input to the comparator on first switching on would be so low that the current through TR4/TR5 might rise to a value which would destroy the transistors.

15. The diode MR5 also protects the unit if a fault condition occurs which causes the EHT voltage at the junction R2/MR5 to fall below that of the 320V supply. The diode conducts as soon as the voltage falls below that of the 320V supply and clamps the junction R2/MR5 to the 320V line, thus stabilizing the EHT at a lower than normal voltage.



B/DDI/11601/B ISSUE 19

MODS INCORPORATED: A 4584
A 4834

EHT POWER UNIT 11601 CIRCUIT

FIG 2

FIG 2

Chapter 3

DEFLECTION COIL DRIVE AMPLIFIER 12502 (5840-99-948-8879)

LIST OF CONTENTS

	<i>Para.</i>
Introduction	1
Circuit Description	6
<i>Temperature cut-out</i>	13

LIST OF ILLUSTRATIONS

	<i>Fig.</i>
Deflection coil drive amplifier: general view ...	1
Deflection coil drive amplifier 12502: component layout	2
Deflection coil drive amplifier 12502: circuit	3



Fig.1 Deflection coil drive amplifier: general view

INTRODUCTI _

1. The deflection coil drive amplifier assembly comprises four identical feedback amplifiers, one for each section of the deflection coil assembly. The amplifiers each have two input terminals. The combined scan and shift waveform (known as the deflection drive waveform) is applied to the main input in all displays. The second input is used only with a fastscan system and accepts the symbol waveform.
2. Each deflection coil drive amplifier operates as a current converter and drives through the relevant deflection coil a current proportional to its input voltage.
3. The early stages of the amplifier operate from the +12V regulated supply and the final stage operates from the unregulated high-current -15V supply. These supplies are provided by Power Unit 11600.
4. The amplifier unit consists of a printed wiring board secured to an aluminium heat sink by brackets and spacing pillars. Eight chassis-mounted transistors are attached to the underside of the heat sink; holes in the printed wiring board provide access to the pillar nuts securing these transistors. Wire-ended transistors are attached to the top surface of the heat sink by retaining clips. All the remaining components are mounted on the top surface of the printed wiring board. External connections to the amplifier circuits are made via the two 10-way taper pin terminal strips TSA and TSB, mounted one at each end of the board.
5. When fitted in the viewing unit the heat sink is in physical contact with a cold plate cooled by the display cooling system. Six screws along the outer edges of the unit are used to secure the unit in position; these screws are accessible through holes in the printed wiring board.

CIRCUIT DESCRIPTION

6. The assembly contains four amplifiers which supply the four deflection coils XA, XB, YA and YB respectively. Since the amplifiers are identical, only that connected to coil XA is described.
7. The amplifier is connected as a combining amplifier with three input resistors and a common feedback resistor. The feedback voltage is developed across a 0.5-ohm feedback resistor in series with the deflection coil and is proportional to output current. This arrangement gives the amplifier a high output impedance, and stabilizes the relationship between input voltage and output current.

8. Double transistor TR1 is connected as a long-tailed pair with the second input at earth level. The output of this pair is amplified by emitter-follower TR2, common-emitter stage TR3 and composite transistor pair TR4/5. C1 and R60 are connected between the base of TR2 and earth to stabilize the amplifier by limiting the high-frequency response. The emitter load of TR1 is returned to a stabilized level of -8.2V. This level is stabilized by Zener diode MR9 and is common to all four circuits.

9. The composite transistor acts as a common-emitter stage with high current gain. Resistor R14 provides local negative feedback and increases the output impedance. Resistor R12 is fitted to provide a path for the reverse base current leakage of TR5 which occurs during the flyback periods.

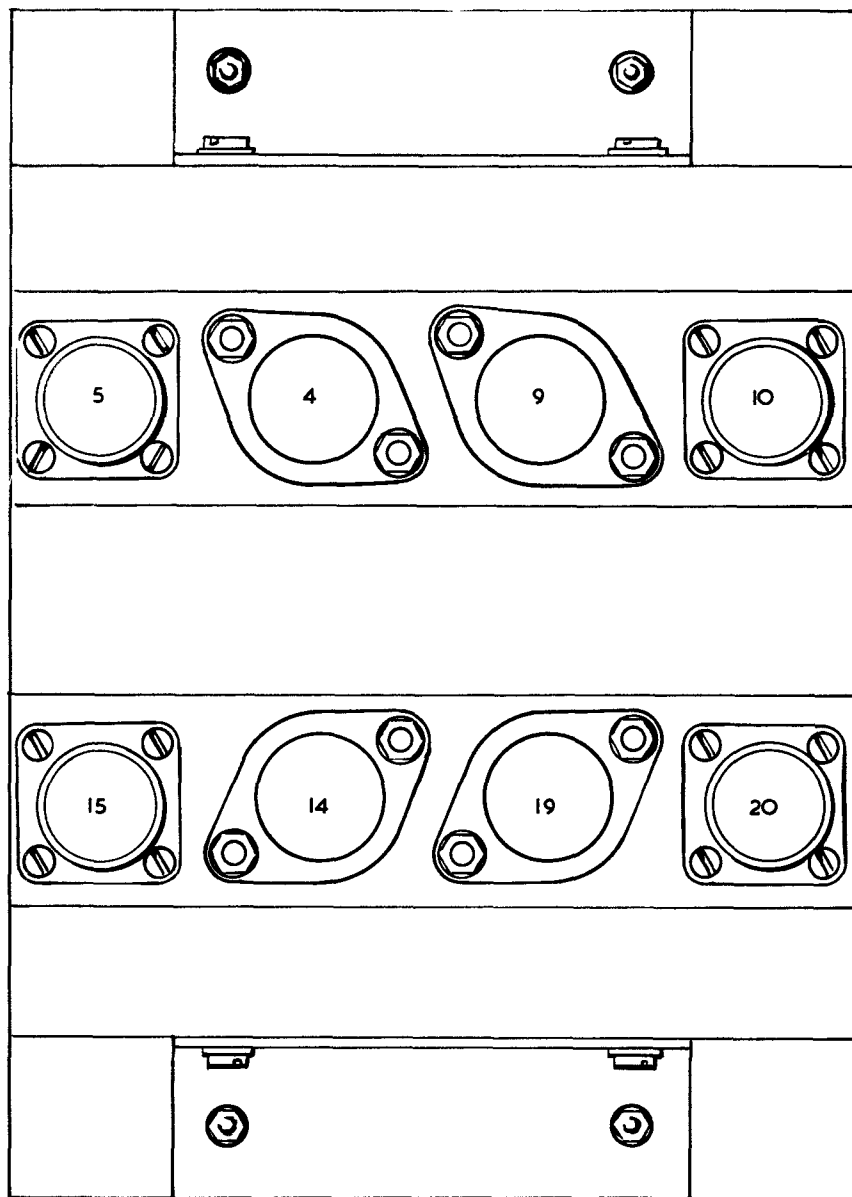
10. Three inputs are added at the input of the amplifier: the scan and shift waveform applied to R1, the symbol waveform applied to R2, and a d.c. level applied to R3. The voltage developed across R13, through which the deflection coil current flows, causes feedback current to flow via R4 to the centre point of the summing junction.

11. The d.c. input is used to set the deflection-coil current to 1.2A in the absence of a signal. The deflection coil current moves between the limits 0.250A to 2.05A to scan the full diameter of the screen. The sum of the currents in the two deflection coils on the same axis is maintained constant at 2A. The d.c. input is obtained from the regulated +12V supply and is set by potentiometer RV1.

12. The transient voltages developed across the deflection-coil during flyback periods are limited by two Zener diodes MR10 and MR11, connected across the output terminals. These diodes are necessary to protect the output transistors against current overload.

Temperature cut-out

13. The deflection coil drive amplifier assembly when fitted in its position in the viewing unit, makes a tight thermal connection to a cold plate; an integral part of this heat sink is a thermostat which operates when the temperature of the sink rises above 83°C and causes the d.c. supplies of the viewing unit to be switched off. This will occur only when either the viewing unit cooling system is faulty or when a failure occurs in the deflection drive amplifier. The deflection coil drive amplifier therefore should not be operated when out of the viewing unit unless adequate provision is made for dissipating the heat generated.

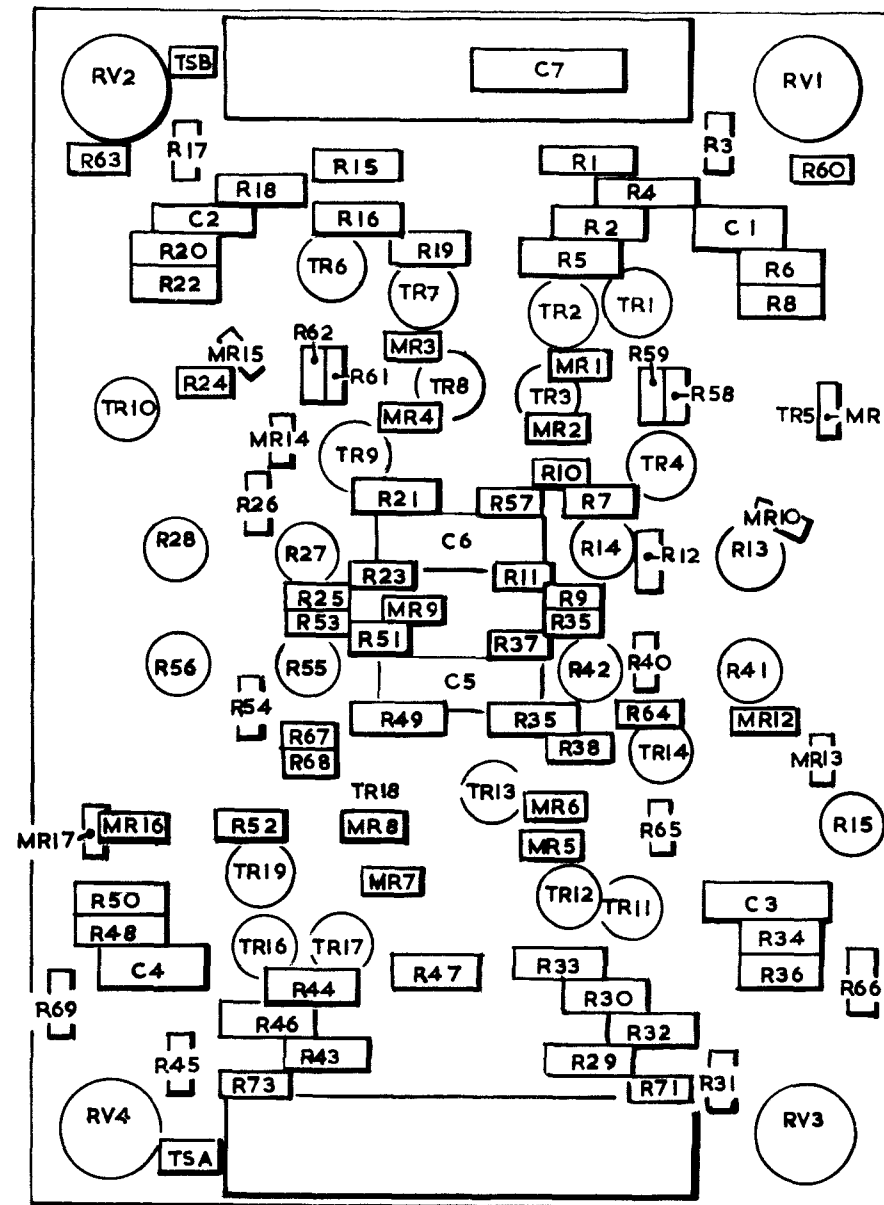


TOP VIEW
(HEAT SINK)

C/PDL/12502/A
ISSUE 11

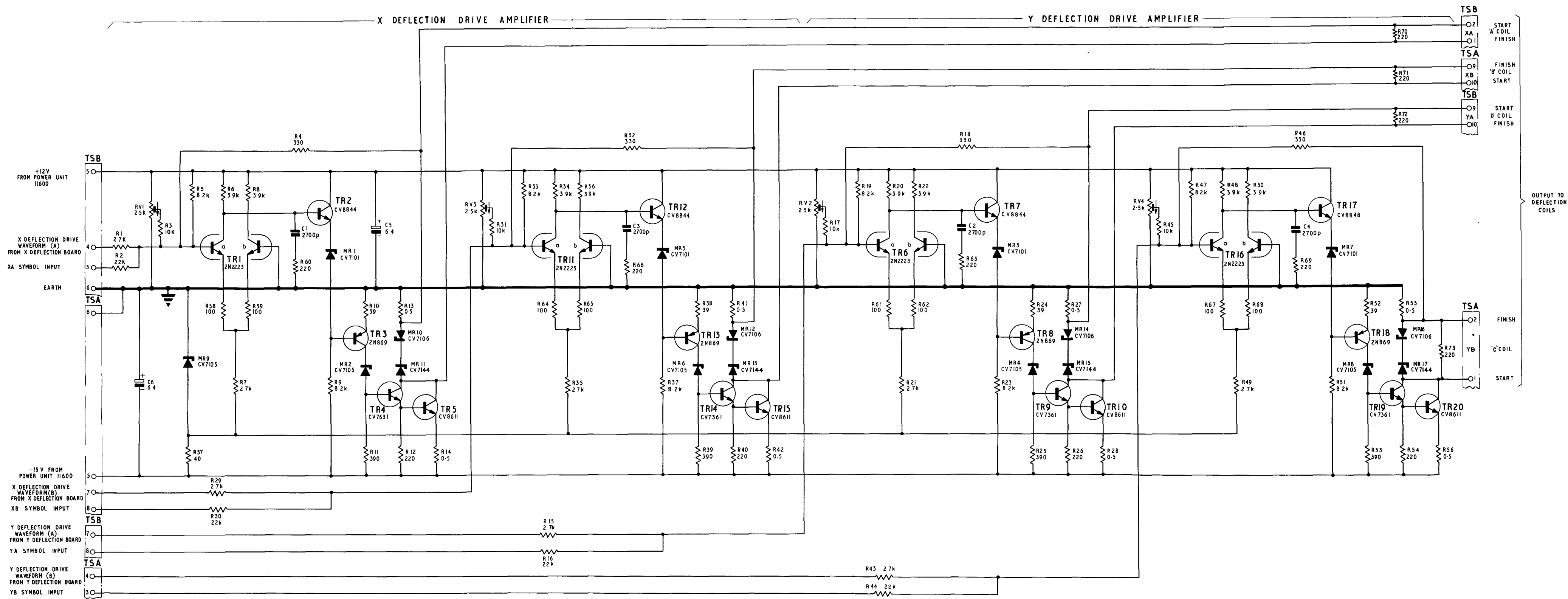
NOTE:
THE FOLLOWING COMPONENTS
ARE MOUNTED ON THE HEAT SINK,
WITH ACCESS TO THEM VIA HOLES
IN THE P.W. BOARD

- TR. 6, 7, 2, 1,
8, 3,
18, 13,
16, 17, 12, 11,
- R. 28, 27, 14, 13,
56, 55, 42, 41,



B/DD/12562/D
ISSUE 8

BOTTOM VIEW
(P.W. BOARD)



B/DDL/12502/7 MOD STRIKE 1
 A.L.30. Aug 71.

Deflection coil drive amplifier 12502:circuit

Fig. 3

Chapter 4

VIEWING UNIT CONTROL PANEL

LIST OF CONTENTS

	Para.
General description	1
Circuit description	
X and Y centre controls	3
Video and calibration marks	4
Brilliance and focus	7
OFF, STANDBY and ON switches	9

LIST OF ILLUSTRATIONS

	Fig.
Viewing unit control panel 11200: component location	1
Viewing unit control panel 11200: circuit diagram	2

LIST OF APPENDICES

	App.
Viewing unit control panel 11057	1
Viewing unit control panel 11066	2
Viewing unit control panel 11210/R/A	3
Viewing unit control panel 11210/T/A	4
Viewing unit control panel 11211/A	5
Viewing unit control panel 11211/B	6
Viewing unit control panel 11211/D	7
Viewing unit control panel 687/00018/004	8
Viewing unit control panel 687/00018/008	9

GENERAL DESCRIPTION

1. The viewing unit control panel is mounted to the right of the display screen and contains display controls required by the operator. Most of the controls are mounted behind a hinged flap. The panel also contains an overload cut-out, main circuit breaker, e. h. t. thermal delay, e. h. t. on-off relay and two terminal strips, TSA and TSB.
2. The Viewing Unit Control Panel 11200 is a basic panel and has variations that

arise from different component values and controls applied to different purposes (hence labelled differently). This chapter describes the 11200 panel; appendices to the chapter describe differences between this basic panel and its derivation (in some applications of the display the viewing unit control panel differs so widely from the 11200 panel that simple comparison is not possible, and the panel variant is described fully in the appropriate supplement to this publication).

CIRCUIT DESCRIPTION

X and Y centre controls

3. These potentiometer controls are connected between the +12V supply entering the panel on terminal TSB33 and -12V on TSB37. The X centre control voltage from the wiper of RV1 (X CENTRE) leaves the panel on TSB5 and is fed to the X deflection board (MRKZ). Similarly, the Y centre control voltage from the wiper of RV2 (Y CENTRE) leaves on TSB6 and is fed to the Y deflection board (MRGZ).

Video and calibration marks

4. Four potentiometer controls are provided, each controlling the gain of a video channel; each potentiometer is connected between the +12V and -12V supplies. These are RV3 to RV6, controlling video channels 1 to 4. The outputs from the potentiometer sliders are the video control voltages, and these are fed out on terminals TSB1, 21, 2 and 22 to the video board (MFDZ).

5. Potentiometer RV11 (LIMITER) is connected between the +12V and -12V supplies. The output from the slider determines the level at which video limiting occurs; this is the video limiting control voltage which is fed to the limiting circuit on the video board (MFDZ) via TSB7.

6. Two control potentiometers enable the operator to set the gain of the range marker channels (video channels 5 and 6). These are RV7 (FINE MARKS GAIN) and RV8 (COARSE MARKS GAIN). The potentiometers are connected between the +12V and -12V supply lines, and the wiper outputs are fed to board MFDZ via TSB3 and TSB23.

Brilliance and focus

7. The brilliance control is a potentiometer RV9 (RADAR BRILL) connected between +12V line and earth. The output from the wiper is the MS brilliance control voltage; this leaves the panel on terminal TSB4 and is fed to the video board (MFDZ).

8. The focus control voltage is obtained from RV10 (FOCUS) connected between +12V and -12V. The wiper output is fed via TSB24 to the e. h. t. power unit.

OFF, STANDBY and ON switches

9. These push-buttons operate single-pole changeover switches biased to one position.

10. The mains supply enters the viewing unit control panel at terminals TSA1 (line) and TSA3 (neutral). When the viewing unit is switched off (i.e. when OFF switch SA is operated) the following circuit path exists across the mains supply: TSA1, cut-out X1 (this cut-out operates at 3.5A overload), normally-closed contacts of switch SA (the OFF switch), RLA/2 (the main circuit breaker), TSA7 through the space heater to TSA8, TSA9 through the space heater to TSA10, RLA/1, lamps ILP1 and ILP2 (the OFF switch lamps), RLA/3 to TSA3. The space heaters are operating, the OFF button is lit at full brilliance and the other panel lights are unlit.

11. When standby switch SB (STANDBY) is operated the mains are applied to the solenoid of main circuit breaker RLA which operates and locks on via contacts RLA/2. The mains supply is available at TSA2 and is fed out to the viewing unit power unit. A 6.3V a.c. supply from the power unit is fed into the viewing unit control panel at TSB14 (line) and TSB16 (neutral), and a -24V d.c. supply from the power unit is fed in at TSB40. The 6.3V a.c. input is applied to thermal delay X2, and to lamp circuits in the panel through a dimmer control RV12 (LIGHTS). The internal lamps of the range selector switch which is operated will also be connected across the 6.3V a.c. supply in series with a 27-ohm resistor and will be lit at reduced brilliance unless a particular range is selected. The circuit conditions are therefore as follows:-

- (1) STANDBY push-button lamps are lit at full brilliance.
- (2) ON and OFF push-buttons are lit at reduced brilliance; range selector lamps are at reduced brilliance except that one may be at full brilliance if selected.
- (3) All other lights are lit at a brilliance set by the LIGHTS control.
- (4) The space heaters and e.h.t. power unit are off.

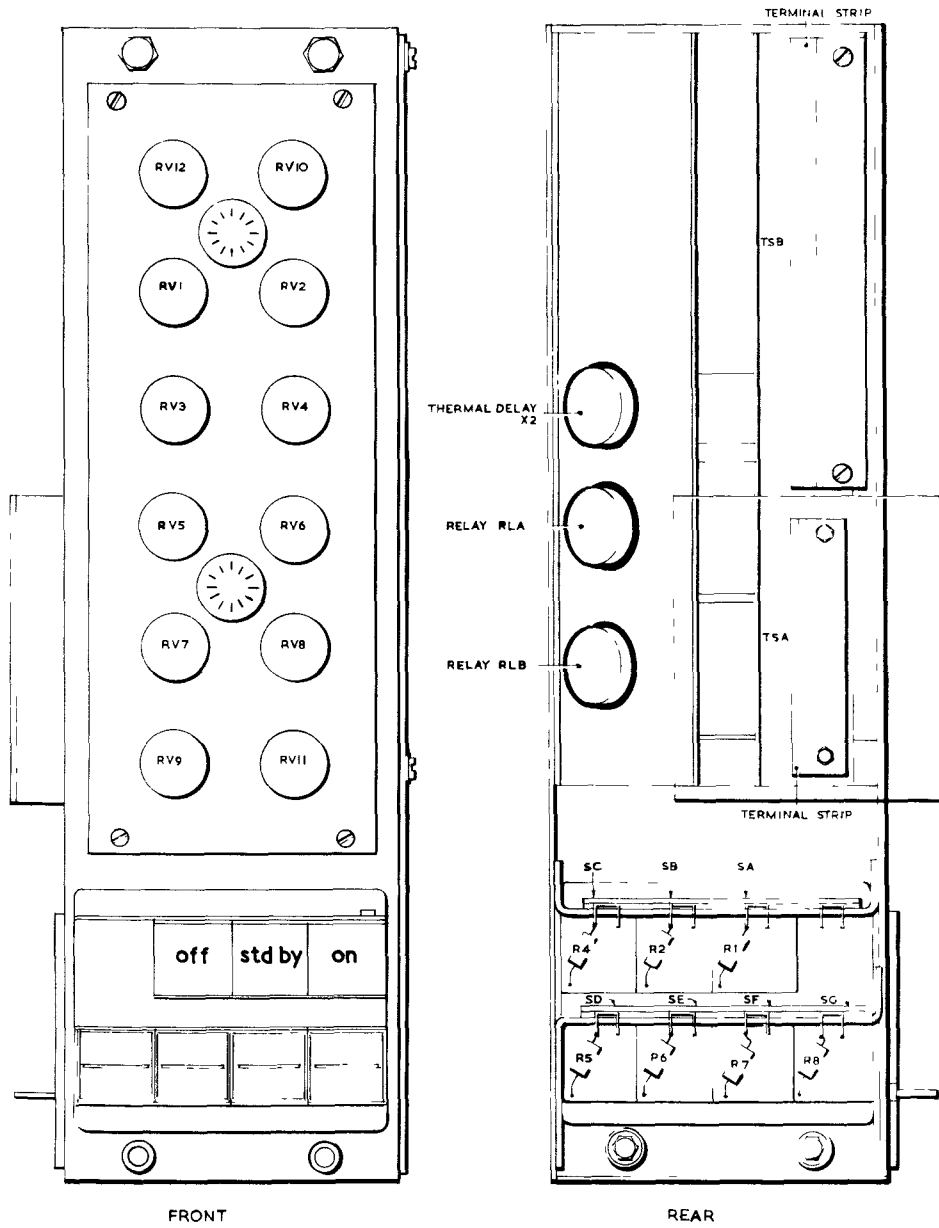
12. The STANDBY switch must be operated before operating the switch SC (ON) has any effect. When the ON switch is operated the mains are applied to the solenoid of e.h.t. relay RLB which locks on via contacts RLB/1. Contacts RLB/2 connect the -24V supply to thermal delay X2; this thermal delay operates 30 seconds after the STANDBY button is operated and it connects the -24V supply to the e.h.t. power unit via TSB39. Contacts RLB/3 connect a 27-ohm resistor (R2) in series with the STANDBY switch lamps and short resistor R4, illuminating the ON switch at full brilliance. The circuit conditions therefore are as follows:-

- (1) The e.h.t. power unit is connected to its power supply.
- (2) The ON push-button and a range selector push-button (if a range is selected) are illuminated at full brilliance.
- (3) The STANDBY and OFF buttons are lit at reduced brilliance.
- (4) The panel lights are lit at a brilliance set by the LIGHTS control.

Range selection

13. A bank of four push-button switches SD, SE, SF and SG is provided for range selection; a release locking bar ensures that only one switch is locked in the operated position at any time. Two sets of contacts are fitted to each push-button. Each push-button is engraved with its corresponding range; in the basic panel these are 50nM, 100nM, 150nM and 200nM.

14. The +12V d.c. regulated supply from the power unit enters the panel at TSB33. When a range selector switch is operated this +12V supply is applied to the corresponding relays on the X and Y deflection boards via terminals TSB27, TSB8, TSB28 or TSB30. A second set of contacts on each switch shorts out a 27-ohm resistor in series with its own lamps when the switch is operated, lighting them at full brilliance.

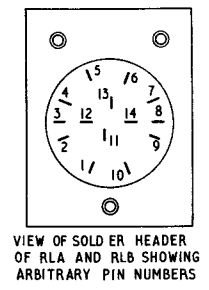
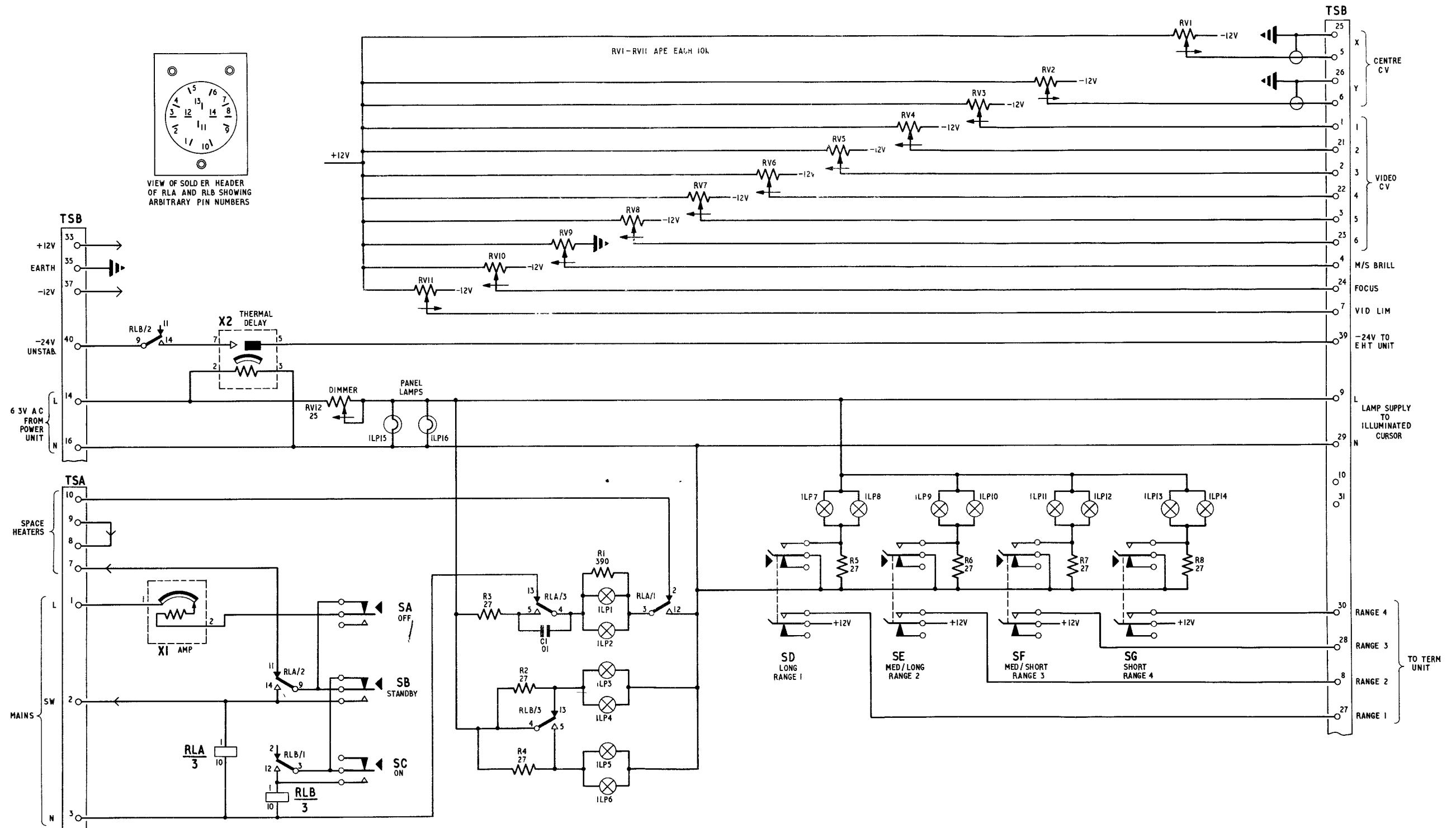


D/DDL/11200/A
ISSUE 12

A.L 32, Nov 71

Viewing unit control panel 11200 component location

Fig 1



B/DDL/11200/B
ISSUE 9
A.L.32, NOV 71

Viewing unit control panel 11200: circuit diagram

Fig.2

A. P. 115K, 1201-1, Part 2, Sect. 1
Chap. 4, App. 1
A. L. 32, Nov. 71

Appendix 1

VIEWING UNIT CONTROL PANEL TYPE 11057

This viewing unit control panel is used in the G. L. 161 application of the Mk. 5 Display. It differs widely from the basic 11200 panel and is fully described in the supplement for G. L. 161 (A. P. 115K, 1208-1, Part 2, Chap. 1).

A. P.115K-1201-1, Part 2, Sect.1
Chap. 4, App. 2
A. L. 32, Nov. 71

Appendix 2

VIEWING UNIT CONTROL PANEL TYPE 11066

This viewing unit control panel is used in the G. L.161 application of the Mk. 5 Display. It differs widely from the basic 11200 panel and is fully described in the supplement for G. L.161 (A. P.115K-1208-1, Part 2, Chap.2).

Appendix 3

VIEWING UNIT CONTROL PANEL TYPE 11210/R/A
(5840-99-955-3594)
(Mod. Strike 2)

This viewing unit control panel differs from the basic 11200 panel only in the engraving of the controls. The control labels are given below.

Control	Engraving	Control	Engraving
RV1	X CENTRE	SA	OFF
RV2	Y CENTRE	SB	STD. BY
RV3	VIDEO 1	SC	ON
RV4	VIDEO 2	SD	75
RV5	VIDEO 3	SE	30
RV6	VIDEO 4	SF	15
RV7	MARKS 2n. m.	SG	7.5
RV8	MARKS 20n. m.		
RV9	RADAR BRILL		
RV10	FOCUS		
RV11	LIMITER		
RV12	LIGHTS		

Appendix 4

VIEWING UNIT CONTROL PANEL TYPE 11210/T/A
(5840-99-955-3596)
(Mod. Strike 2)

This control panel differs from the basic 11200 panel only in the engraving on the controls. The control labels are given below.

Control	Engraving	Control	Engraving
RV1	X CENTRE	SA	OFF
RV2	Y CENTRE	SB	STD. BY
RV3	VIDEO 1	SC	ON
RV4	VIDEO 2	SD	100
RV5	VIDEO 3	SE	50
RV6	VIDEO 4	SF	25
RV7	MARKS 4n. m.	SG	12.5
RV8	MARKS 20n. m.		
RV9	RADAR BRILL		
RV10	FOCUS		
RV11	LIMITER		
RV12	LIGHTS		

Appendix 5

VIEWING UNIT CONTROL PANEL TYPE 11211/A

This control panel differs from the basic 11200 panel only in the engraving on the controls. The control labels are given below.

Control	Engraving	Control	Engraving
RV1	X CENTRE	SA	OFF
RV2	Y CENTRE	SB	STD. BY
RV3	VIDEO 1	SC	ON
RV4	VIDEO 2	SD	SHORT
RV5	AUX. VID	SE	MED. SHORT
RV6	IFF	SF	MED. LONG
RV7	10m	SG	LONG
RV8	50m		
RV9	RADAR BRILL		
RV10	FOCUS		
RV11	LIMITER		
RV12	LIGHTS		

Appendix 6

VIEWING UNIT CONTROL PANEL TYPE 11211/B

This control panel differs from the basic 11200 panel only in the engraving on the controls. The control labels are given below.

Control	Engraving	Control	Engraving
RV1	X CENTRE	SA	OFF
RV2	Y CENTRE	SB	STD. BY
RV3	LIN	SC	ON
RV4	LOG	SD	SHORT
RV5	ELEVATED MARKS	SE	MED. SHORT
RV6	VID. 4	SF	MED. LONG
RV7	10m	SG	LONG
RV8	50m		
RV9	RADAR BRILL		
RV10	FOCUS		
RV11	LIMITER		
RV12	LIGHTS		

A. P.115K-1201-1, Part 2, Sect. 1
Chap. 4, App. 7
A. L. 32, Nov. 71

Appendix 7

VIEWING UNIT CONTROL PANEL TYPE 11211/D

(Mod. Strike 1)

This viewing unit control panel is used in ADRS applications of the Mk. 5 Display. It differs widely from the basic 11200 panel and is fully described in the supplement for ADRS (A. P.115K,1203-1, Part 2, Chap. 3).

At the time of writing the panel has not been allocated a NATO Cat. No.

A. P. 115K, 1201-1, Part 2, Sect. 1
Chap. 4, App. 8
A. L. 32, Nov. 71

Appendix 8

VIEWING UNIT CONTROL PANEL TYPE 687/00018/004
(5840-99-222-1045)
(Mod. Strike 0)

This viewing unit control panel is used in the SJCC application of the Mk. 5 Display. It is widely different from the basic 11200 panel and is fully described in the supplement for SJCC (A. P. 115K-1202-1, Part 2, Chap. 3).

Appendix 9

VIEWING UNIT CONTROL PANEL TYPE 687/00018/008
(5840-99-115-2251)
(Mod. Strike 0)

This viewing unit control panel differs from the basic 11200 panel only in the engraving on the panel controls. The control labels are given below.

Control	Engraving	Control	Engraving
RV1	X CENTRE	SA	OFF
RV2	Y CENTRE	SB	STD. BY
RV3	VIDEO 1	SC	ON
RV4	VIDEO 2	SD	256
RV5	VIDEO 3	SE	128
RV6	VIDEO 4	SF	64
RV7	MARKS 10d. m.	SG	32
RV8	MARKS 50d. m.		
RV9	RADAR BRILL		
RV10	FOCUS		
RV11	LIMITER		
RV12	LIGHTS		

Chapter 5

VIEWING UNIT JUNCTION UNIT

LIST OF CONTENTS

	Para.
General description	1
Circuit description	
Viewing unit junction unit circuits	3
Connections between viewing unit circuits	4
External connections	5
Power supply connections	6
Relays	7
Aerial synchro drive transformer	10

ILLUSTRATIONS

	Fig.
Viewing unit junction unit: general view	1
Viewing unit junction unit 687/00407/004: circuit	2
Viewing unit junction unit 12790/Q/A: circuit	3
Viewing unit junction unit 12790/J/A: circuit	4
Viewing unit junction unit 12790/A: circuit	5
Viewing unit junction unit 687/00407/013: circuit	6
Viewing unit junction unit 687/00407/014: circuit	7
Viewing unit junction unit 12792/A: circuit	8
Viewing unit junction unit 12792/C: circuit	9

GENERAL DESCRIPTION

1. The viewing unit junction unit is mounted at the rear of the viewing unit. The interconnections between the various groups of circuits within the viewing unit, and between the viewing unit and external circuits (i. e. circuits in the mount or console, or the circuits of equipment external to the display) are taken through this junction unit.
2. The junction unit carries two 50-way sockets and a 14-way socket which mate with plugs on the rear of the viewing unit; the sockets are designated A, B and C. In addition two 60-way taper pin terminal blocks TSA and TSB are housed within the unit, together with the four relays RLA, RLB, RLC and RLD.

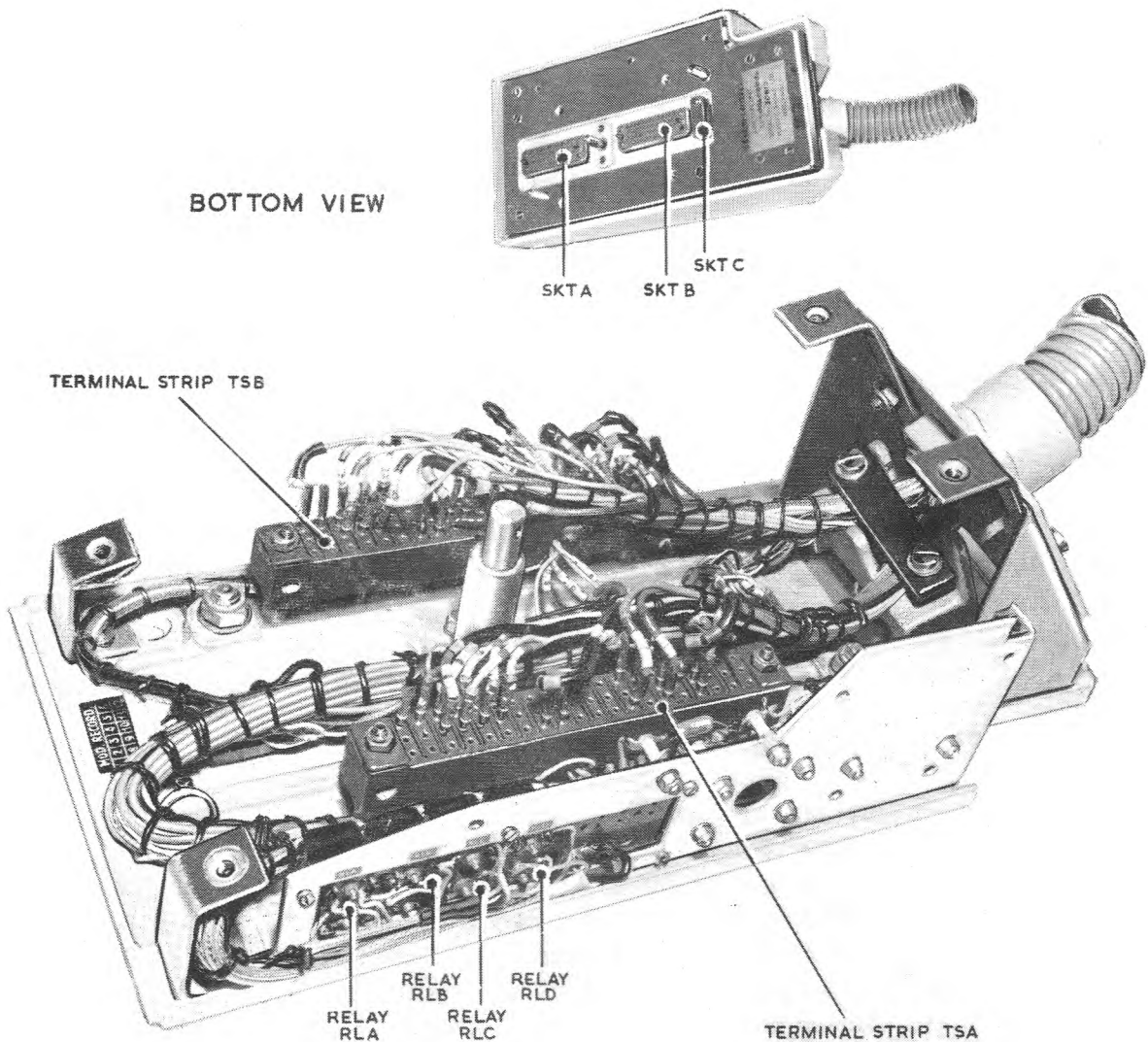


Fig.1. Viewing unit junction unit; general view

CIRCUIT DESCRIPTION

Viewing unit junction unit circuits

3. The circuits of junction unit variants are given in Figs. 2 to 9, as well as being shown on the interconnections diagrams in the first chapter of the supplementary publication for each application (A. P.115K-1202-1 for SJCC, A. P.115K,1203-1 for ADRS, etc.).

Connections between viewing unit circuits

4. The inputs and outputs of the groups of circuits within the viewing unit are connected to pins on the fifty-way plugs on the rear of the viewing unit. In the junction unit the corresponding socket connections are taken to terminals on the terminal blocks TSA and TSB. Interconnections between the viewing unit circuits are made by links between the terminals.

External connections

5. Connections from the viewing unit to external circuits (i. e. circuits in the mount, including the operator's control panel, the console or in equipment external to the display) are made via the junction unit sockets. These connections may be routed via the terminal blocks TSA and TSB, or may be made from the external equipment directly to the three sockets.

Power supply connections

6. The mains input connections to the viewing unit are made via plug and socket C. Mains are distributed to the control panel and other equipment via this plug and socket.

Relays

7. Four relays (RLA, RLB, RLC and RLD) are fitted in the junction unit. The function of these relays depends upon whether the display is used in the h. r. i. or p. p. i. role, and they are not necessarily all used in a particular installation. Refer to the supplements for details of the relay functions.

8. In an h. r. i. display RLD is the check vernier relay; it is energized when the CHECK VERNIER push-button switch is operated, and in this condition its contacts disconnect the output from the HEIGHT potentiometer to the Y deflection board replacing this with earth level and setting the height line to zero. Relay RLC is the video blanking relay and it is energized by a video blanking signal from the aerial when it reaches the bottom of its sweep; in the energized condition contacts RLC/2 disconnect the radar video signal from the video amplifier (contacts RLC/1 are part of the rate prediction circuit). Relays RLA and RLB also are part of the rate prediction circuit, and their purpose is to feed a rate prediction voltage (either +6V or -6V depending on whether the aerial is undergoing an upward or downward sweep) to the demodulators.

9. In the p. p. i. display relays RLA, RLB and RLC provide range and bearing line/c. r. d. f. line changeover facilities for the interscan marker. Relay RLD is controlled by the VID MAP selector push-button on the operator's control panel and selects the appropriate video map presentation for feeding to the video amplifier.

Aerial synchro drive transformer

10. ◀ This transformer is normally fitted to p.p.i. and h.r.i. displays. ▶ It is located in the junction unit and is driven by the power amplifier located on the timing board (MJE). The transformer outputs are fed to the radar head via terminal block TSA.

11. Each p.p.i. display has its own synchro excitation supply generator and sampling gate generator. The outputs from these are brought to separate terminals on the terminal blocks, and similarly the inputs to the demodulator circuits are also connected to terminals on the terminal blocks.

12. When a single display is used the terminals connected to the sampling gate must be linked to the terminals connected to the demodulator circuits.

13. When a number of displays are used the synchro supply and sampling gate from one display only is used to control all the displays. The selected synchro supply and sampling gate may be obtained from any of the displays, selection being either manual or automatic from a switch on or near the displays.

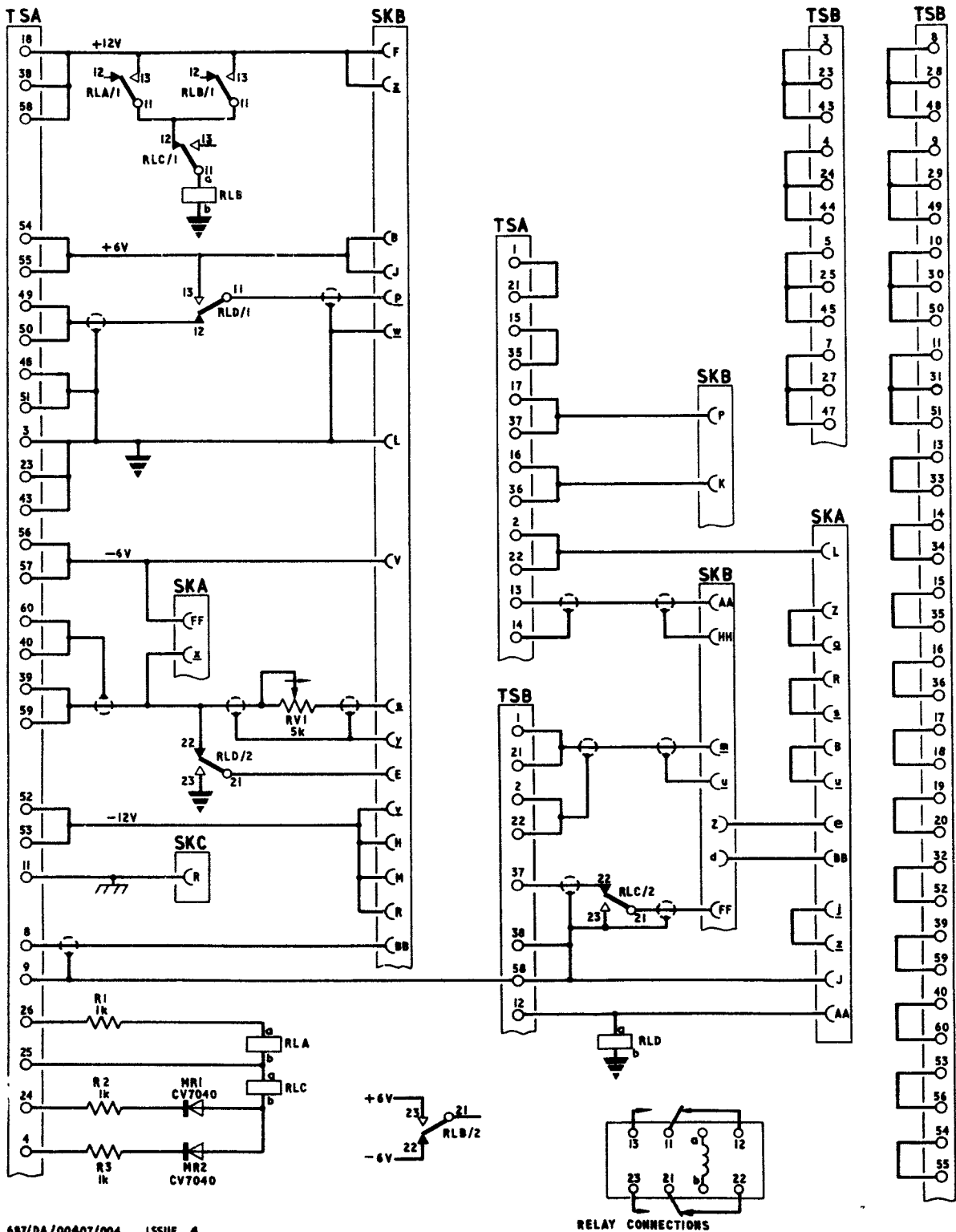


Fig.2 Viewing unit junction unit 687/00407/004: circuit

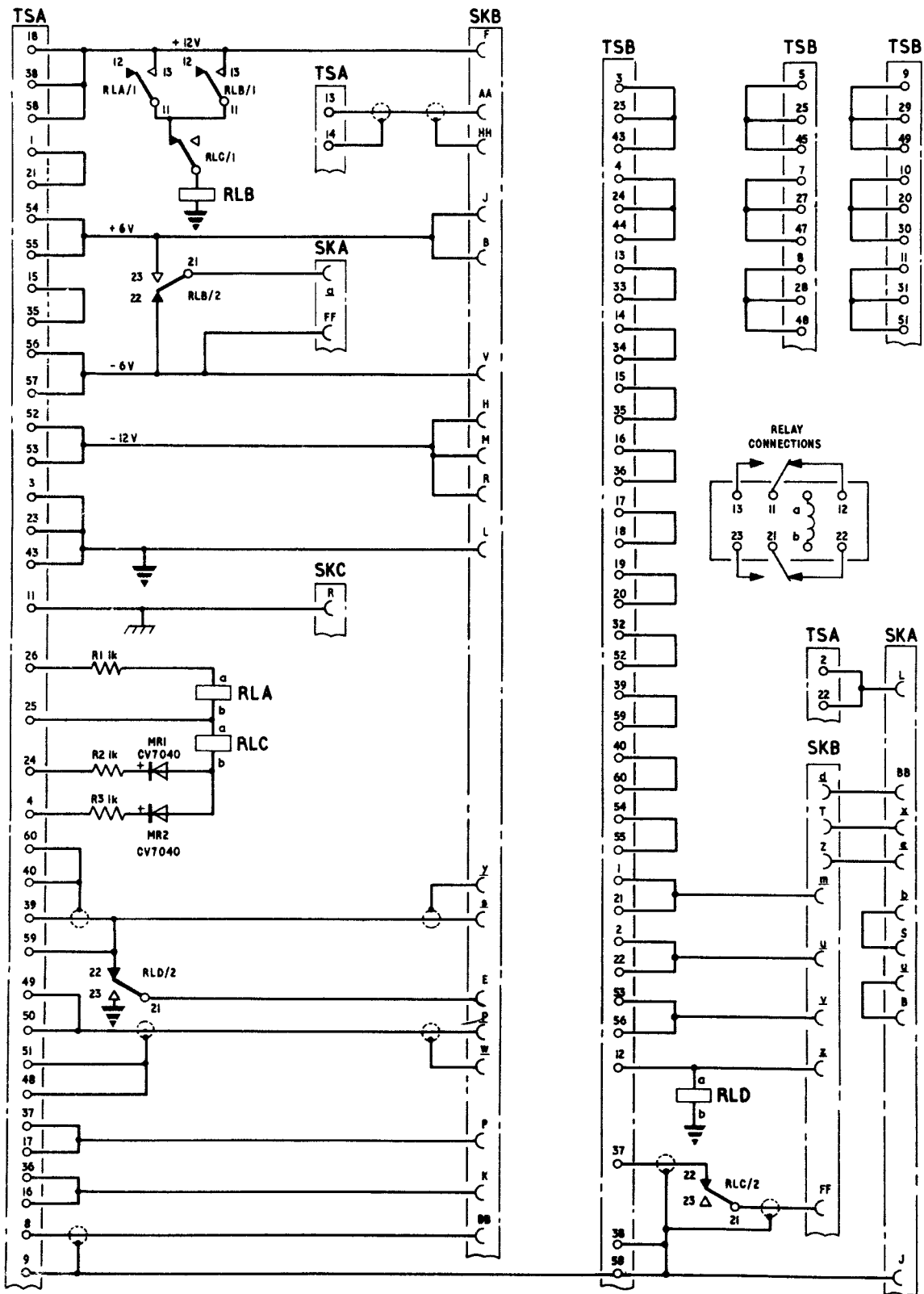


Fig. 3 Viewing unit junction unit 12790/Q/A: circuit

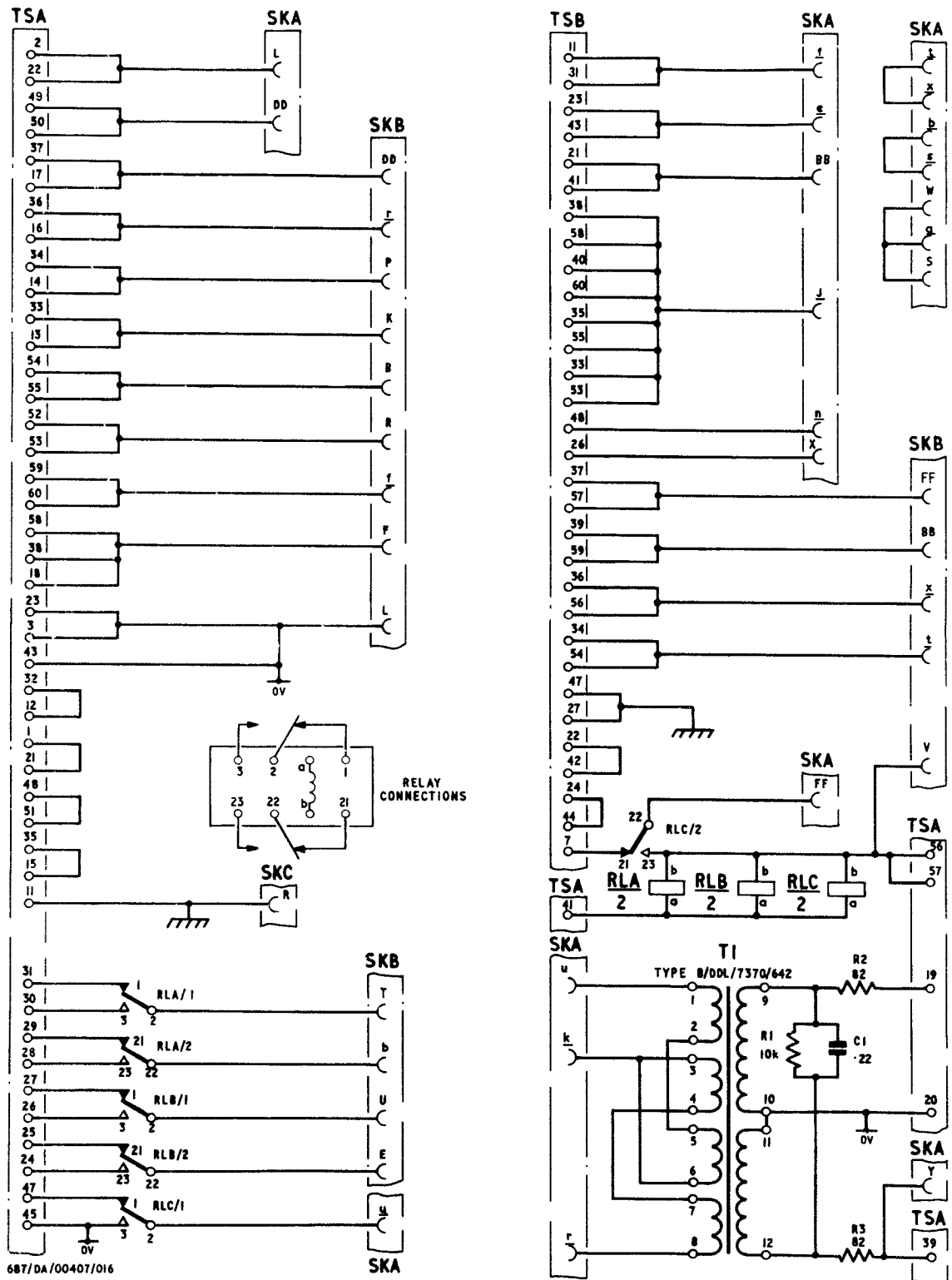
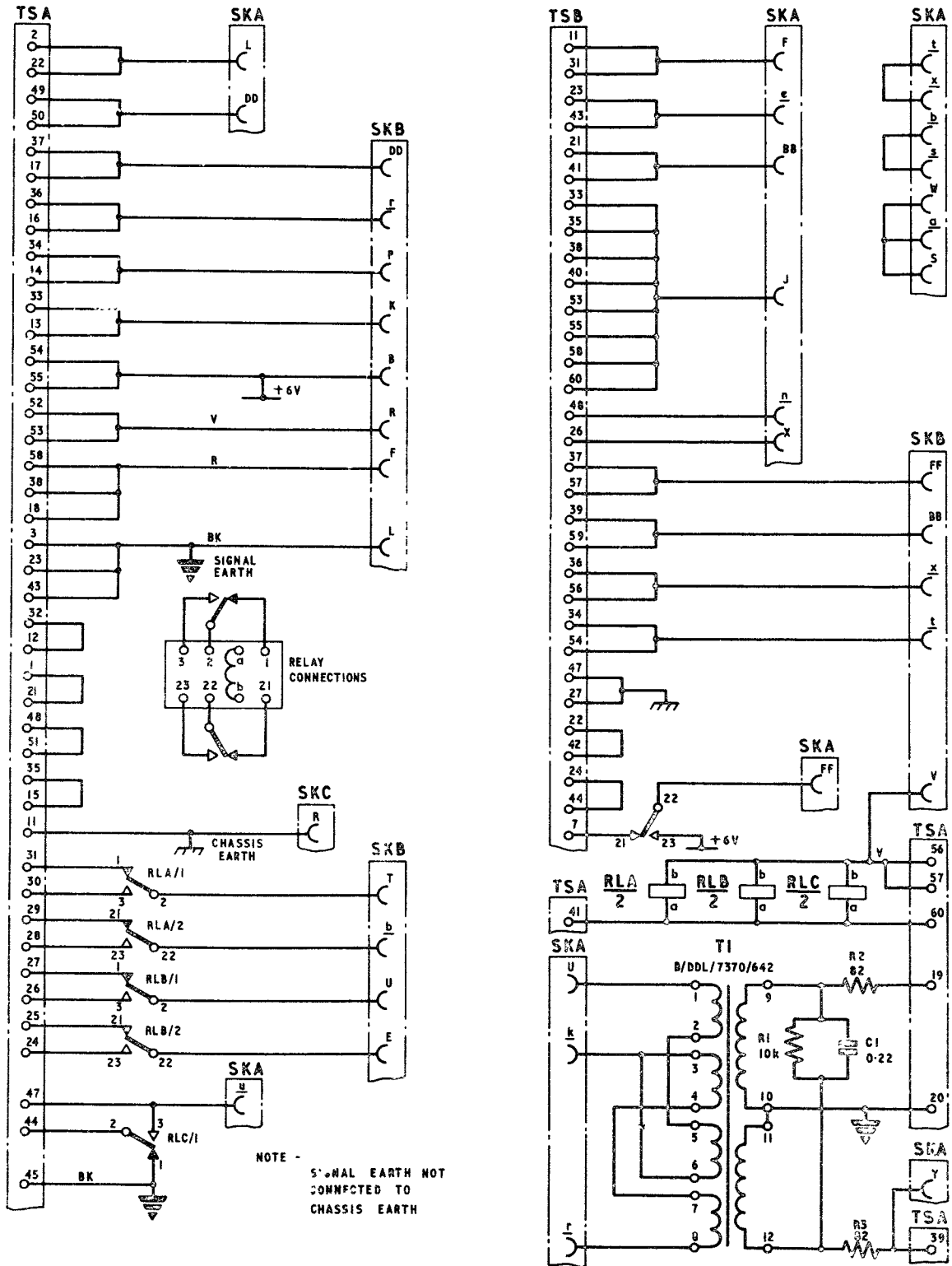


Fig. 5 Viewing unit junction unit 12790/A: circuit



697/DA/00407/013

Fig. 6 Viewing unit junction unit 687/00407/013: circuit

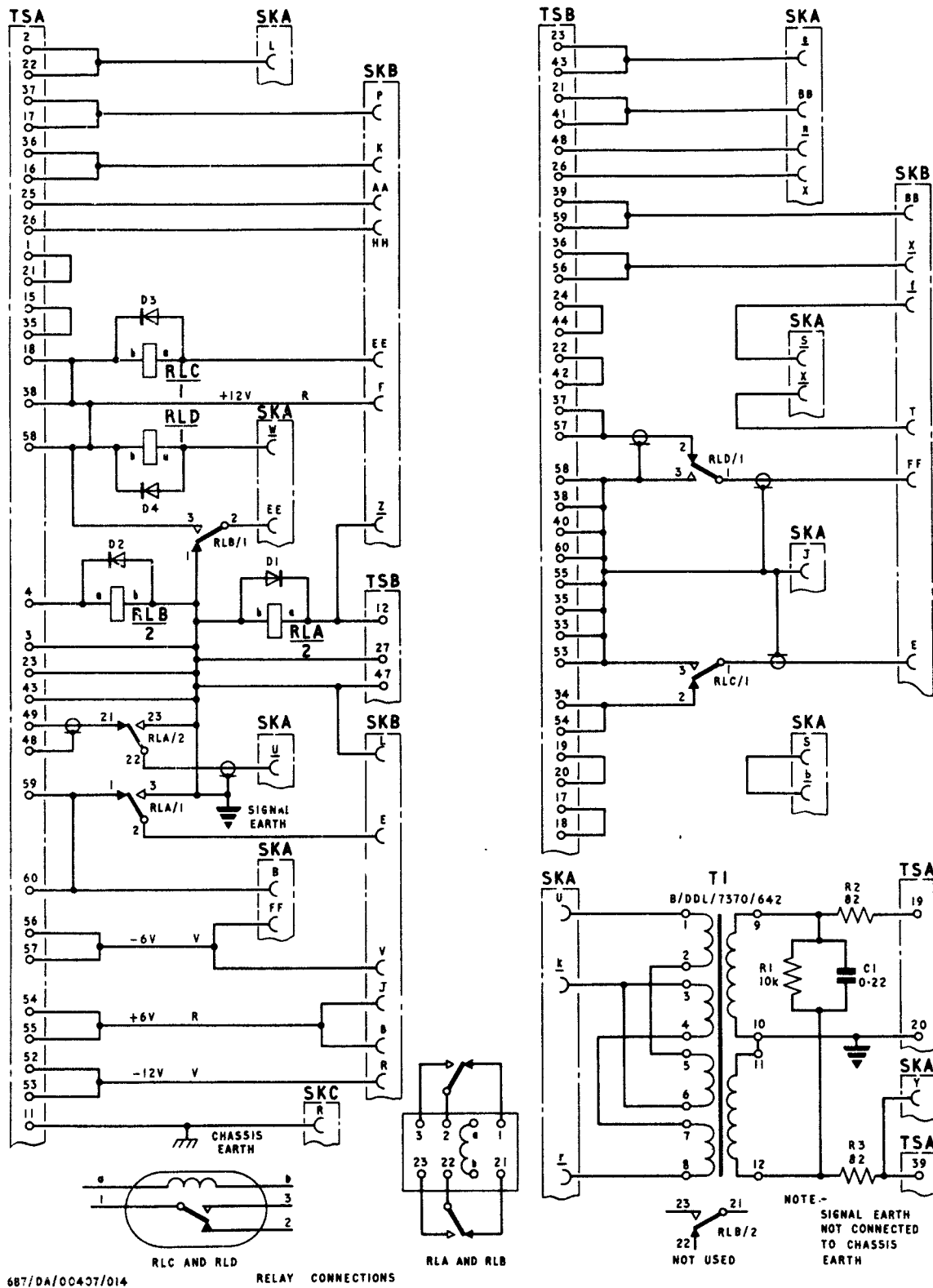


Fig. 7 Viewing unit junction unit 687/00407/014: circuit

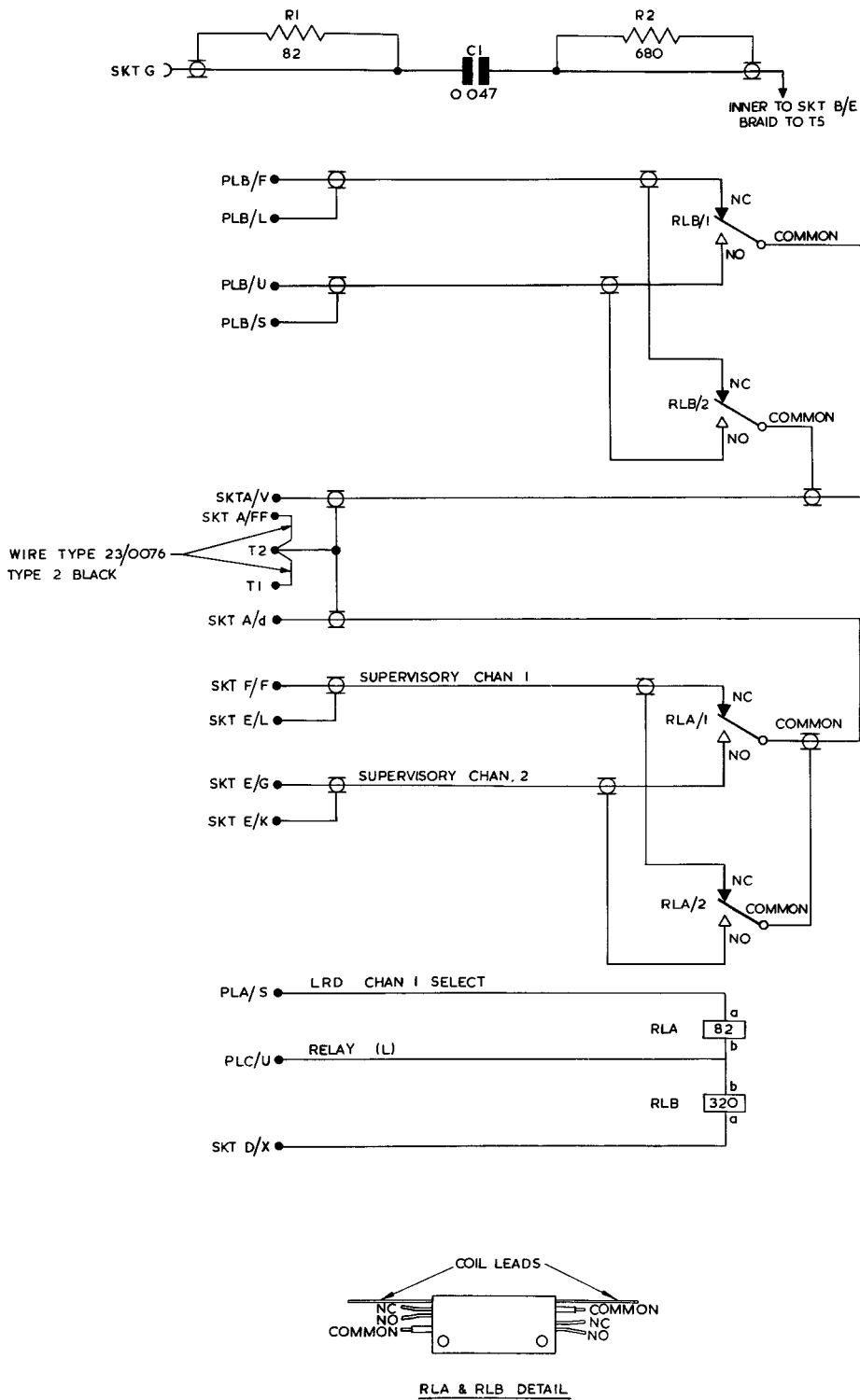
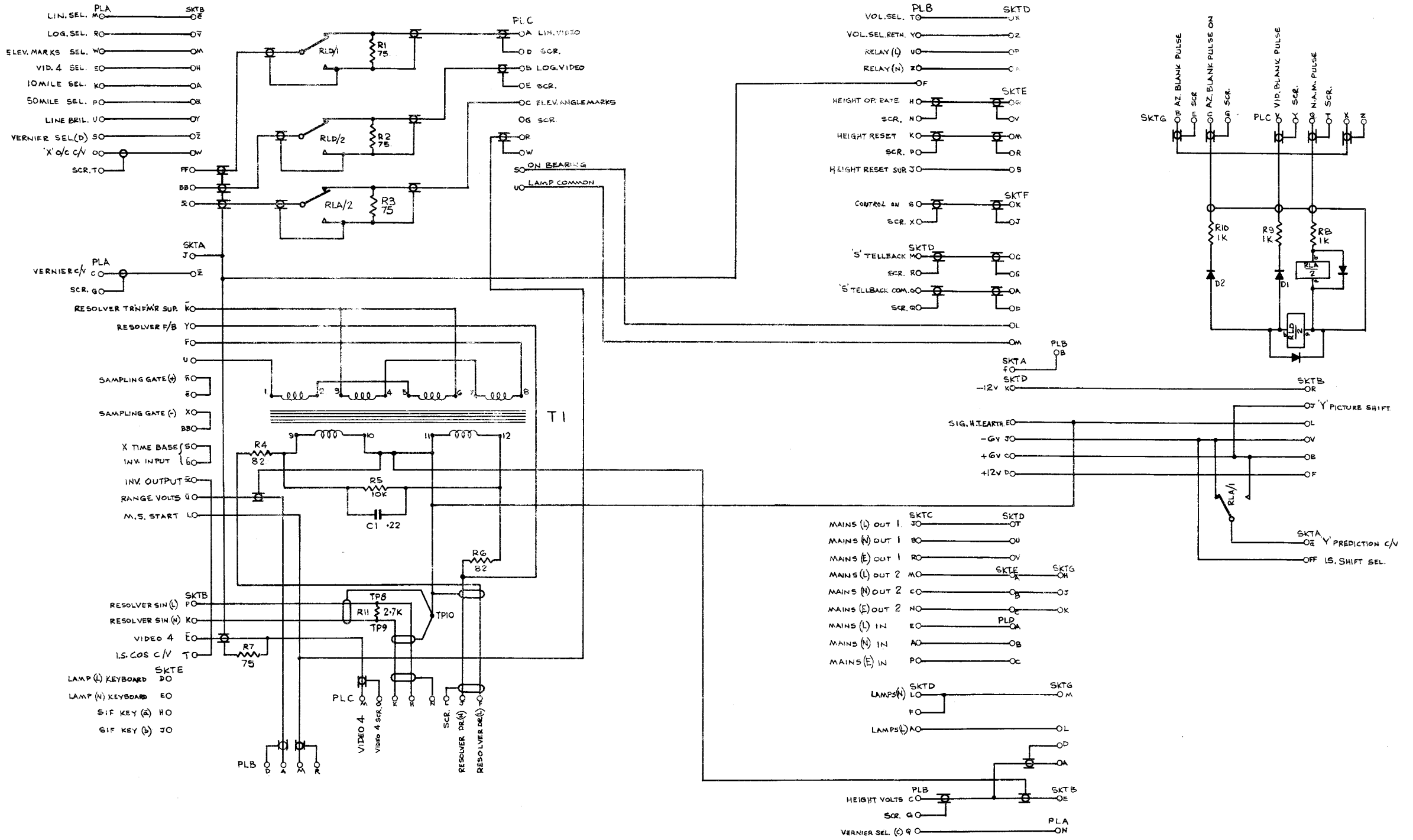


FIG. 8

JUNCTION UNIT TYPE 12792/A

FIG. 8



Chapter 6

COOLING SYSTEM

LIST OF CONTENTS

	Para.
Introduction	1
Heat exchanger 11950A	3
Pump 12551/C	6
Electrical circuit	7

LIST OF ILLUSTRATIONS

	Fig.
Elements of the cooling system	1
Heat exchanger 11950A: detail	2
Cooling system: electrical circuit	3
Pump assembly 12551	4

Introduction (Fig. 1)

1. The Mk.5 12in viewing unit employs a cooling system which maintains an operating temperature in the range 10°C to 40°C for an ambient temperature of 0°C to 35°C. Cold plates (to which are attached the heat-generating elements of the viewing unit) and a liquid-to-air heat exchanger are connected in a closed circuit and a light mineral oil is circulated through them. The general oil temperature is 8°C to 15°C above ambient.

2. The elements of the system are:-

- (1) Heat exchanger 11950A (Cooler, liquid, 5840-99-948-9043).
- (2) Pump assembly 12551/C (Pump, rotary, 5840-99-948-9059).
- (3) Power unit cold plate.
- (4) Board box cold plate.
- (5) Deflection coil drive amplifier cold plate.

Caution . . .

The power units and deflection coil drive amplifier must not be operated out of the display unless some arrangement is made for cooling.

Heat exchanger 11950A (Fig. 2)

3. The heat exchanger consists of an enclosed, coiled tube and a fan. The circulating oil flows over fins on the inside of the tube and cooling air is drawn over fins on the outside. The oil flow rate varies between 9 and 15 gall/hr, depending upon oil viscosity with temperature. The temperature of the oil leaving the heat exchanger coil is 6^oC cooler than that of the incoming oil.

4. The fan is a capacitance start-and-run induction motor driving two sets of paddles. It is rated at 50 cu.ft./min of air transfer. The amount of heat transferred to the air depends upon the relative temperatures of the viewing unit and the surrounding air, and can be the equivalent of 250W.

5. The heat exchanger fan and coil are mounted together in an air duct at the bottom rear of the viewing unit. The air path to the heat exchanger coil is from the front underside of the viewing unit and through a duct under the deflection coil support platform; the air then passes through the coil and fan and is exhausted through two vents in the rear of the viewing unit.

Caution . . .

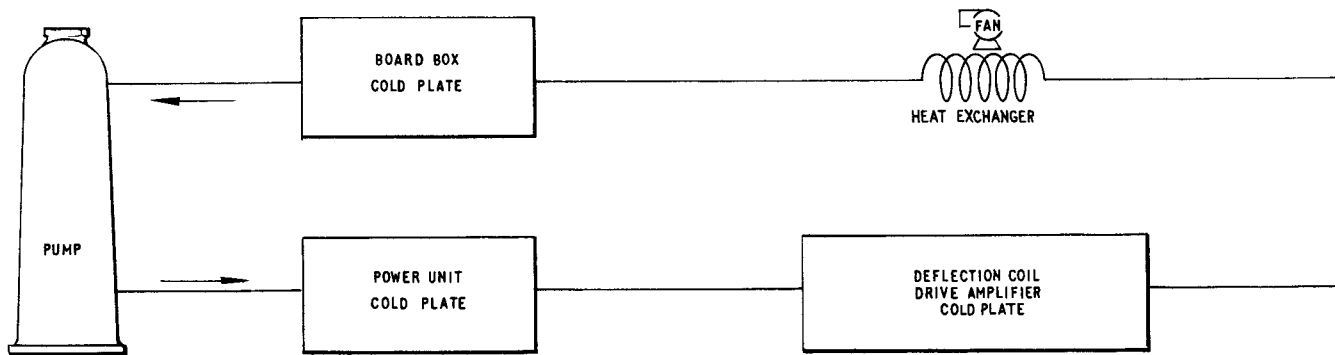
The intake and exhaust ports must be kept clear of obstructions.

◀ Pump 12551/C (Fig. 4) ▶

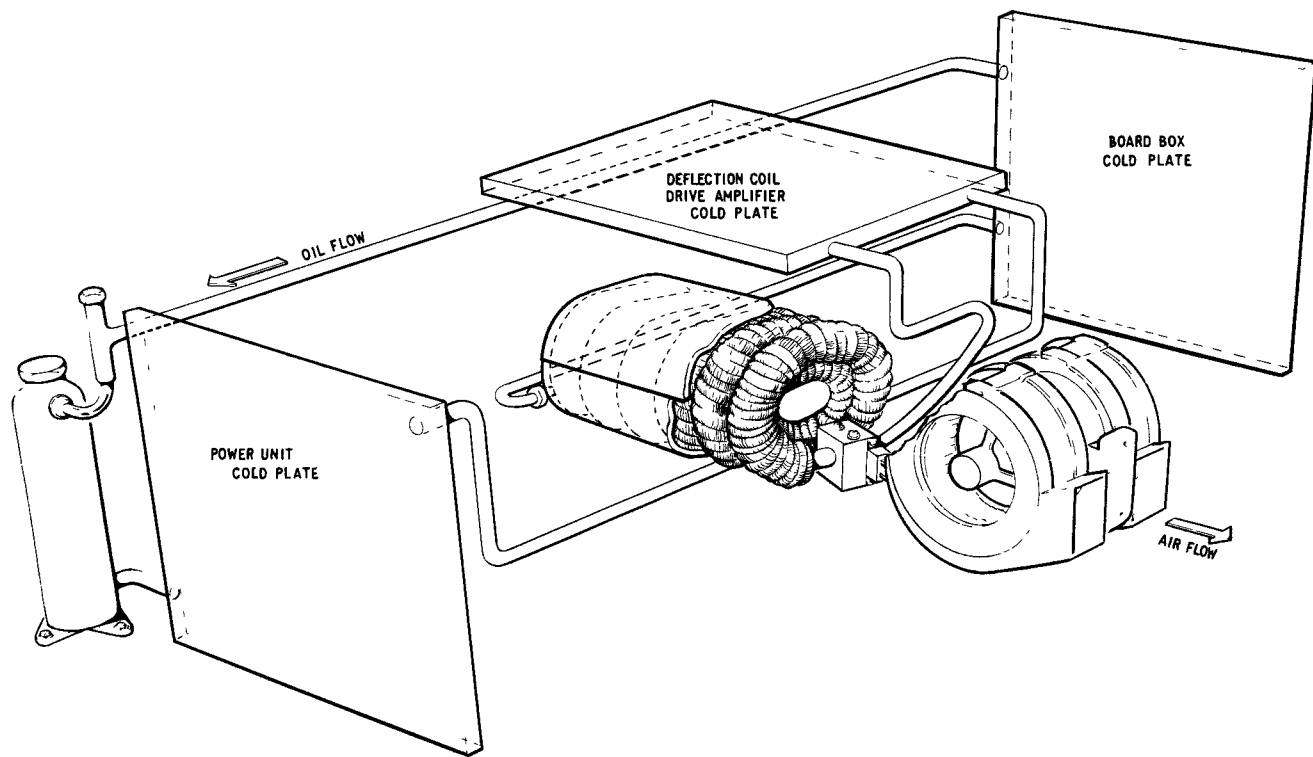
6. The pump is an integral unit consisting of a capacitance start-and-run induction motor whose rotor shaft is extended in the form of a screw pump. The rotor and screw are immersed in the circulating oil. An expansion unit is incorporated at the base of the pump to allow for variation in the volume of oil with pressure and temperature. The normal pressure developed across the pump at 15^oC ambient air temperature is 12 lb/in²; this condition gives a flow rate of 12 gall/hr.

Electrical circuit (Fig. 3)

7. The pump is supplied with 225V a. c. from tappings on transformer T1 in the Power Unit 11600; this supply is available when either the STANDBY or the ON push-button on the viewing unit control panel is pressed. The neutral line to the main contactor RLA is taken through two high-temperature cut-outs as follows:-



(a) SCHEMATIC



(b) SIMPLIFIED LAYOUT

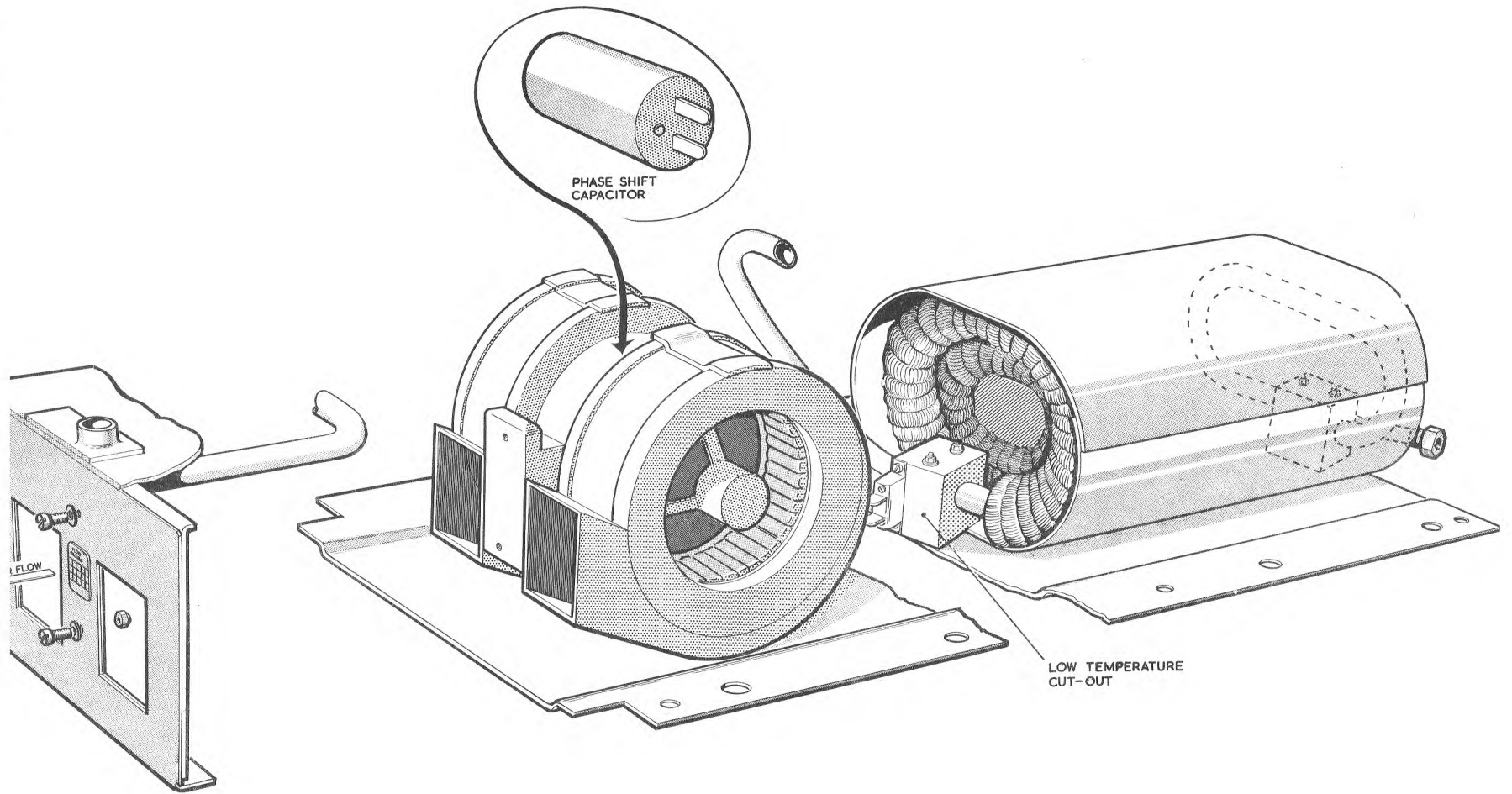


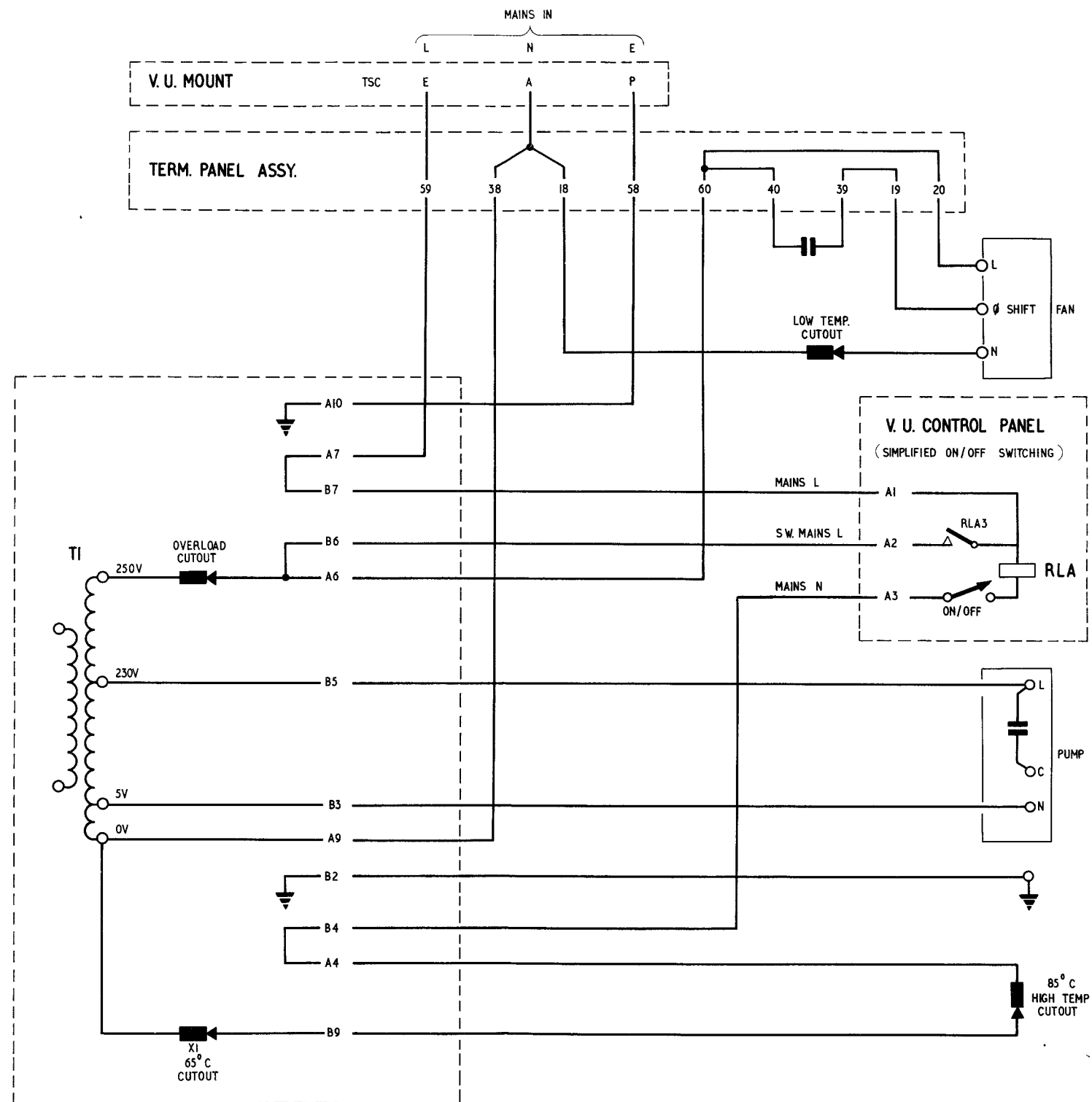
Fig.2

Fig.2 Heat exchanger 11950A: detail

- (1) X1 (75°C) on the power unit cold plate (Gravinette TCS3150/75°C).
- (2) High temp. (83°C) cut-out on the underside of the deflection coil drive amplifier cold plate (Gravinette TCS3150/83°C).

If either of these cut-outs opens under high-temperature conditions the neutral line to RLA is broken and the viewing unit switched off.

8. The fan is supplied from the switched mains and is operative when either the STANDBY or the ON push-button is pressed. A low-temperature (0°C) cut-out, located in the heat exchanger air stream, is connected in the neutral line of the fan supply; this cut-out opens at 0°C and below, and interrupts the fan supply to allow the viewing unit to reach the correct operating temperature in low ambient temperatures.



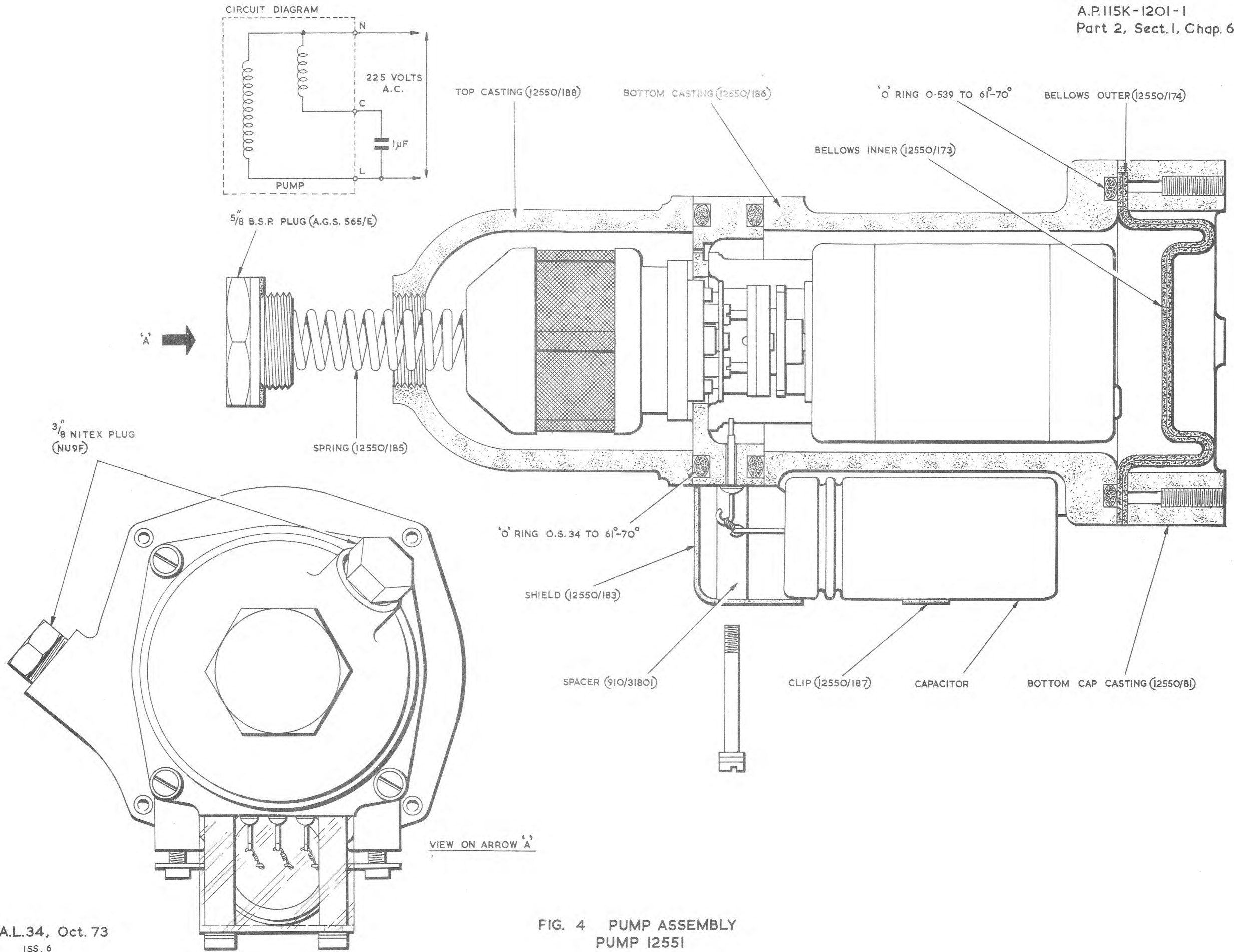


FIG. 4 PUMP ASSEMBLY
PUMP 12551

CHAPTER 7

DEFLECTION COIL ASSEMBLY 11702A

(5840-99-948-9055)

1. The deflection Coil Assembly 11702A is used on 12in Mk. 5 displays. The assembly incorporates main coils for mainscan deflection and auxiliary digit coils for the small deflections required in writing characters in labelled plan applications of the display. The assembly of coils is encapsulated into a single unit to which a focusing magnet assembly is attached. No servicing should be attempted by Service personnel other than measurement at external terminals (Table 1).
2. The four deflection coils are wound on Permalloy cores (Figure 1) and the coil connections taken to a terminal block within the coil encapsulation. A 220ohm damping resistor is connected across each coil (within the encapsulation, and in addition to the 220ohm resistors across the drive output from the drive amplifier).
3. The four digit coils are also wound on a Permalloy core with connections taken to the terminal block. The finish of each coil is commoned and a single connection taken out. A 100ohm damping resistor is connected across each coil (Figure 2); the coil, with the four resistors, is enclosed within a Tufnol tube. This tube sub-assembly is bonded to the main deflection coil. The complete assembly is then encapsulated to form the deflection coil unit.
4. The focusing magnet assembly is attached to the end of the deflection coil encapsulation. This assembly, enclosed by an aluminium casing, consists of an annular permanent magnet fitted with two pole pieces. The effective gap between the pole pieces can be varied by means of a soft iron tube which slides through the apertures in the magnet and the rear pole piece (Figure 1c). Movement of the focus adjustment control varies the position of this tube, and hence the focus of the c. r. t.
5. Two ferrite-impregnated, plastic, beam centring magnets are mounted on the rear lips of the focusing magnet assembly casing and produce a small correcting field in the grid region of the c. r. t. beam. These are annular magnets whose external field configuration is changed by rotating the magnets with respect to each other.

Note: The beam centring magnets must always be mounted in the

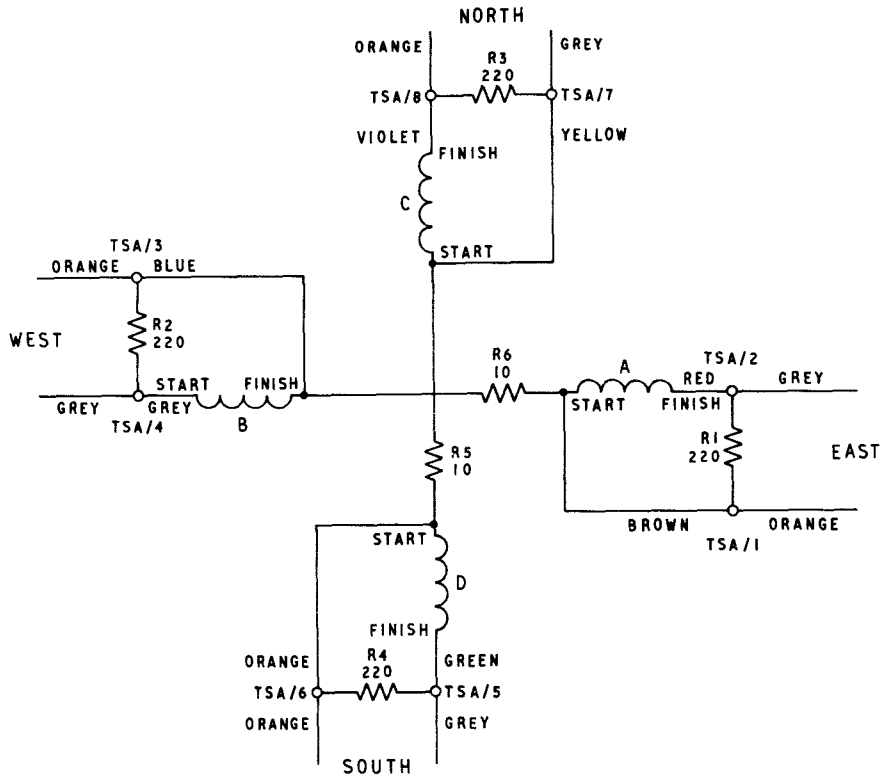
correct relative position; correct polarity is indicated by the notches on the adjusting lugs facing each other.

6. The procedure for adjusting the mechanical focusing control and beam centring magnets is given in Part 3, Sect. 1, Chap. 6. In general this should be necessary only on replacement of the c. r. t.

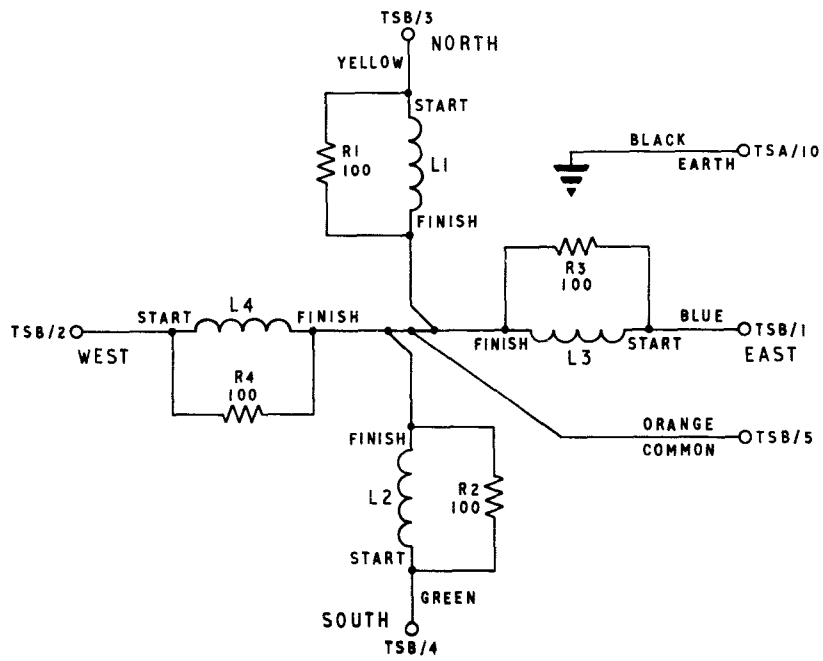
TABLE 1
Test data

	R (ohms)	L (μ H)
Deflection coil	0.75 nominal	195 \pm 5%
Digit coil	0.1 nominal	9.5 \pm 10%

Note: These parameters measured on Marconi Bridge TF868B at 10kHz.



(a) DEFLECTION COILS



(b) DIGIT COILS

Chapter 8

CHARACTER DRIVE UNIT TYPE 12500

LIST OF CONTENTS

	Para.
Introduction	1
Detailed description	5
The inhibiting action	12

LIST OF ILLUSTRATIONS

	Fig.
Character drive unit type 12500: circuit diagram	1

INTRODUCTION

1. Characters are drawn on the c. r. t. in a series of $1\mu s$ discrete scans, the most complicated characters requiring fifteen of these scans. In order to present these very fast scans, a separate low-inductance deflection coil is provided specially for characters. The unit with which this description is concerned generates the necessary drive current for this coil assembly.
2. The unit accepts character scan waveforms superimposed on the minor shift levels routed from board LRYB in position 3D of the Electronic Cabinet Type 11826 (the character generator). These waveforms are, of course, only produced by the cabinet during fastscan periods.
3. The unit contains two push-pull amplifier channels, one for the X deflection and one for the Y deflection. Each amplifier channel contains a switch circuit to which, except during fastscan periods, a separate input is applied to inhibit the generation of character deflection waveforms.
4. The unit comprises a rectangular box, approximately $2\frac{3}{4}$ in \times $3\frac{1}{2}$ in \times 6in, which is secured within the viewing unit by means of four bolts. A great part of the circuitry housed in this unit is carried on two small printed wiring boards.

DETAILED DESCRIPTION

5. Since the two amplifier channels are identical, only one is described, i. e.

that handling the Y deflection waveform and shown on sheet 2 of the circuit diagram.

6. TR14 and TR15 comprise a long-tailed differential amplifier with the neutral input applied as reference input to TR16 base and the character deflection input applied to TR14 base; this input varying between the limits of $\pm 4V$. TR15 acts as a high impedance constant current source, supplying the 'tail' current to the differential amplifier.

7. With both differential inputs earthed, RV5, connected into the emitter circuit of this stage, enables the tail current to be divided equally between both transistors so that their collector potentials are identical. With the normal inputs then applied, the outputs at TR14 and TR16 collectors are truly complementary.

8. TR14 collector level is emitter-followed by TR18, passed via Zener diode MR5 to change the voltage level (MR5 providing a very low a. c. /d. c. impedance), and thence to a composite output pair TR23, TR24.

9. The gain of the output stage TR23, TR24 is determined by the total resistance accorded to the composite resistor in TR23 emitter circuit, and can be varied by means of three-position switch SA. Rotating this switch from its open-circuit position through terminal 2 to terminal 1 varies the gain factor by 1, 2 and 3 respectively, the standing coil currents being 0.2A, 0.4A and 0.6A respectively. In this system, the switch should remain at position 1, giving maximum gain.

10. The output, derived from TR24 emitter, is fed to one end of the centre-tapped Y deflection coil, this centre-tap being connected to the negative 19V coil supply. The other end of this coil is driven from a similar series of stages which are themselves driven from the opposed output at TR16 collector.

11. The current in one section of the coil, therefore, decreases as the current in the other section increases, and vice versa, so that a true push-pull deflection of the c. r. t. beam is obtained.

The inhibiting action

12. The action of the amplifier may be inhibited by the application of a +6V level to TR17 and TR21 circuits. For the amplifier to function, this switch input is held at -6V. In this condition, TR17 is heavily bottomed and its collector is, therefore, at near-earth potential. TR15 base level is determined by the potential divider network R37, R38 at approximately -6V. TR5, therefore, conducts, supplying tail current to the differential amplifier determined by the setting of RV6 in its emitter, this potentiometer being adjusted so that the outputs at test points 9 and 10 are both -3V.

13. Under the same conditions, TR21 base is held at approximately -8V, TR21 is cut-off so that no current is supplied to either TR19 or TR20, and the levels at TR14 and TR16 are determined solely by the currents drawn by their own collectors.

14. When the switch input assumes its +6V level, TR17 is cut-off causing TR15 to be cut-off. No tail current is, therefore, available for the differential stage; the

inputs applied to TR14 and TR16 bases can, therefore, have no effect on their collector levels. Normally, the reduction of the tail current to zero would cause TR14 and TR16 collector levels to rise to +12V. However, in this state, TR21 is bottomed, applying -6V to the bottom of TR19, TR20 emitter networks, and careful adjustment of RV7 and RV8 in these networks sets the emitter currents (and, therefore, sets the collector currents) at values which just equal the current supplied by TR14 and TR16 respectively in normal conditions. Thus, either TR14 and TR16 are both conducting and TR19, TR20 are both cut-off or vice versa, and the levels at their commoned collectors when the amplifier is inhibited are equal to the levels obtained in normal conditions with zero input applied to the amplifier.

Chapter 9

DEFLECTION COIL DRIVE AMPLIFIER 12505

LIST OF CONTENTS

	Para.
Introduction	1
Mechanical description	3
Circuit description	4

LIST OF ILLUSTRATIONS

	Fig.
Circuit of deflection coil drive amplifier type 12505	1

INTRODUCTION

1. This deflection drive amplifier assembly used in the 21in viewing unit comprises two identical feedback amplifiers, one for each of the deflection coils used on one axis. The amplifiers each have three input terminals. The combined scan and major shift waveform is applied to the main input from deflection board MRMC. The second input, used during the fastscan period accepts the symbol waveform. The remaining input accepts a centring voltage.
2. Each deflection coil drive amplifier provides a deflection coil current, the amplitude of which is proportional to the input voltage.

MECHANICAL DESCRIPTION

3. Transistors TR4, TR5 and TR6, and TR10, TR11, TR12 and Zener diodes MR6 and MR11 are bolted onto the metal mounting block which acts as a heat sink, and is in turn bolted to a cold plate. Printed resistors R18, R19, R21-R24, R41-R42 and R44-R47 are also fitted to this block. All other transistors are mounted in small clips which are in close thermal contact with the mounting block, and are situated under the paxolin P. W. B. which is held off by four spacers. Electrical connection is achieved by two 10-way taper pin termination blocks, which provide easy monitoring points for servicing purposes.

CIRCUIT DESCRIPTION

4. The assembly contains two amplifiers which supply the two deflection coils

Xa and Xb (or Ya and Yb). Since the amplifiers are identical, only that connected to coil Xa is described.

5. The amplifier comprising TR1-TR6 is connected as a combining amplifier with three input resistors and a common feedback resistor. The feedback voltage is developed across a 0.25ohms (two 0.5ohms in parallel) feedback resistor in series with the deflection coil and is proportional to output current. This arrangement provides an amplifier with a high output impedance.

6. TR1 is a double transistor differential amplifier whose signal input is limited by MR1, MR2 to within +0.7V and whose reference input is at earth level. The output from the differential amplifier is applied to emitter-follower TR2 and thence via coupling Zener diode MR4 to the common emitter stage TR3. TR3 drives the composite output stage, transistors TR4-TR6, via another Zener diode coupler MR5.

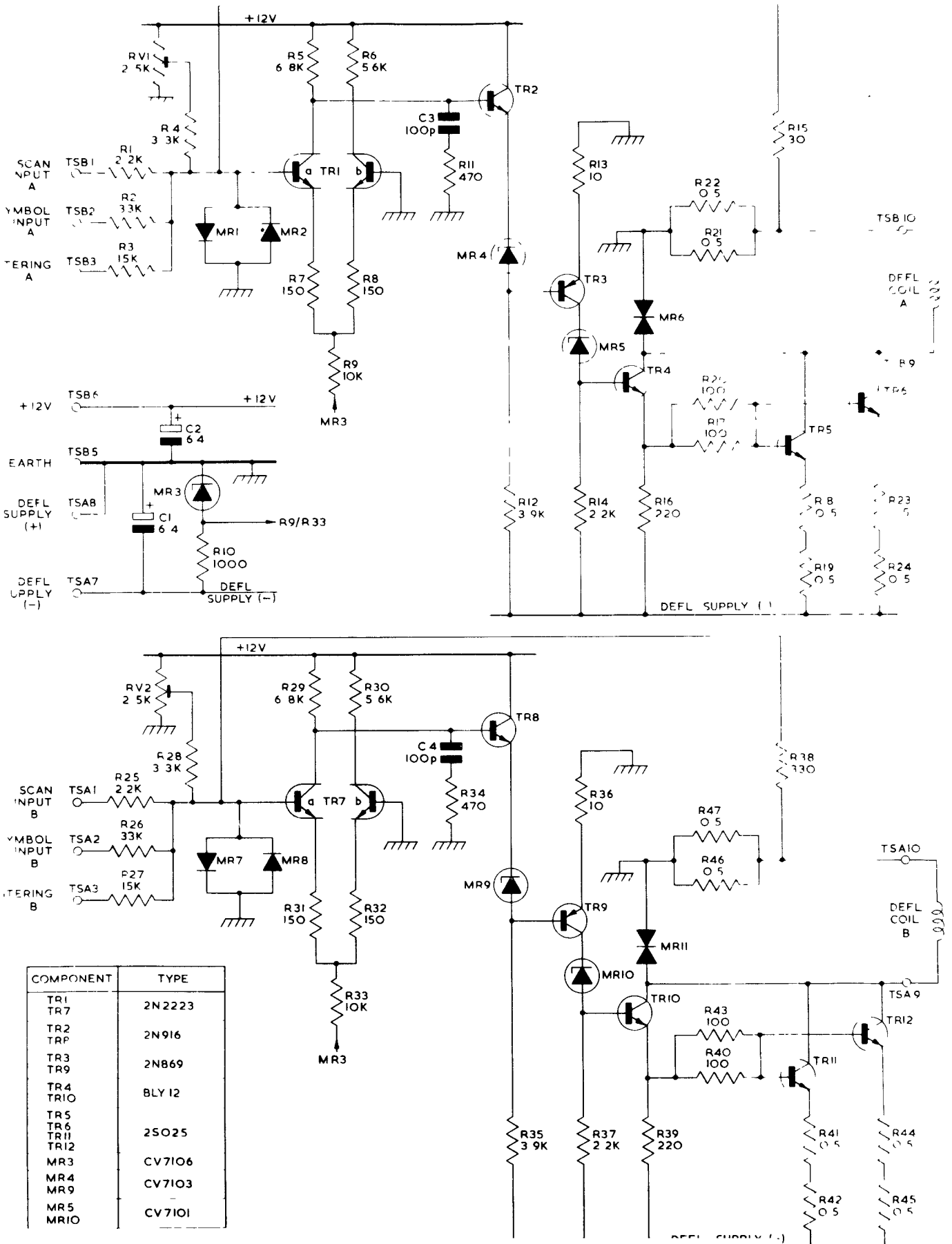
7. Excepting the individual 1ohm emitter resistors (two 0.5ohm in series), whose function is to provide local negative feedback, TR5-TR6 are connected in parallel. The composite transistor acts as a common emitter with high current gain. R16 is fitted to provide a path for the reverse base currents of TR5-TR6 which occur during the fly-back periods.

8. Three inputs are added at the centre-point of the amplifier; the scan and shift waveform applied to R1, the symbol waveform applied to R2, and a d. c. centring level applied to R3. The voltage developed across the parallel resistors R21, R22, through which the deflection coil current flows, is fed back via R15 to the centre point.

9. RV1 is used to adjust the current through the deflection coil to a steady value of 2.5A with two inputs earthed and the centring input open-circuit.

10. The transient voltages developed across the deflection coil during the flyback periods are limited by Zener diode MR6 to protect the output transistors.

11. MR3 is a 15V Zener diode and is connected across the -22V supply in series with 1k resistor R10. This network produces a stabilised -15V supply for the long-tailed pairs. C2 and C1 are decoupling capacitors connected across the supply input.



Chapter 10

POWER UNIT 11605

LIST OF CONTENTS

	Para.
Introduction	1
Mechanical construction	4
Circuit description	
-22V supply	5
Focus coil stabilised current supply	6

LIST OF ILLUSTRATIONS

	Fig.
Power supplies and focus drive unit type 11605	1

INTRODUCTION

1. This unit generates a -22V supply for the deflection coil drive amplifiers. It also receives the stabilised -18V from the Main Power Unit Type 11606 and produces from this a regulated current supply for the focus coil. In addition, the mains supply input to this unit is distributed to the final deflection cooling system.

2. Main supplies are brought to the unit and the live supply is passed out to a test switch on the focus control panel. From there it is returned to the primary of the HT transformer T1 via a low temperature thermal cut-out X1.

3. A 225V supply is tapped from the primary of the HT transformer T1 and fed via B5, B3 to the fan, and C3,C5 to the pump assembly of the final deflection cooling system.

MECHANICAL CONSTRUCTION

4. This power unit is situated behind the south side cover of the 21in viewing unit. All the heat generating components are mounted on a back plate which is in close thermal contact with the power unit cold plate. Five taper pin sockets accommodate the external connections to this unit and are easily accessible from the front.

CIRCUIT DESCRIPTION

-22V supply

5. Connected in series with the primary of the HT transformer is a 2A indirectly heated thermal cut-out. The output from the secondary of the HT transformer is applied across bridge rectifier MR1-MR4. R13 and C7 protect the transformer against transients, should the 15A thermo-magnetic cut-out X2 open. This cut-out has a directly heated bi-metal strip set to trip at 15A and is connected in series with the a. c. input to the bridge rectifier. A solenoid in the cut-out and connected in series with the d. c. output from the bridge trips the bi-metal should the output read 15A. The d. c. output from MR1-MR4 is smoothed by LC filter L1 and C1-C2, and is fed to the X and Y deflection coil drive amplifiers (12505).

Focus coil stabilised current supply

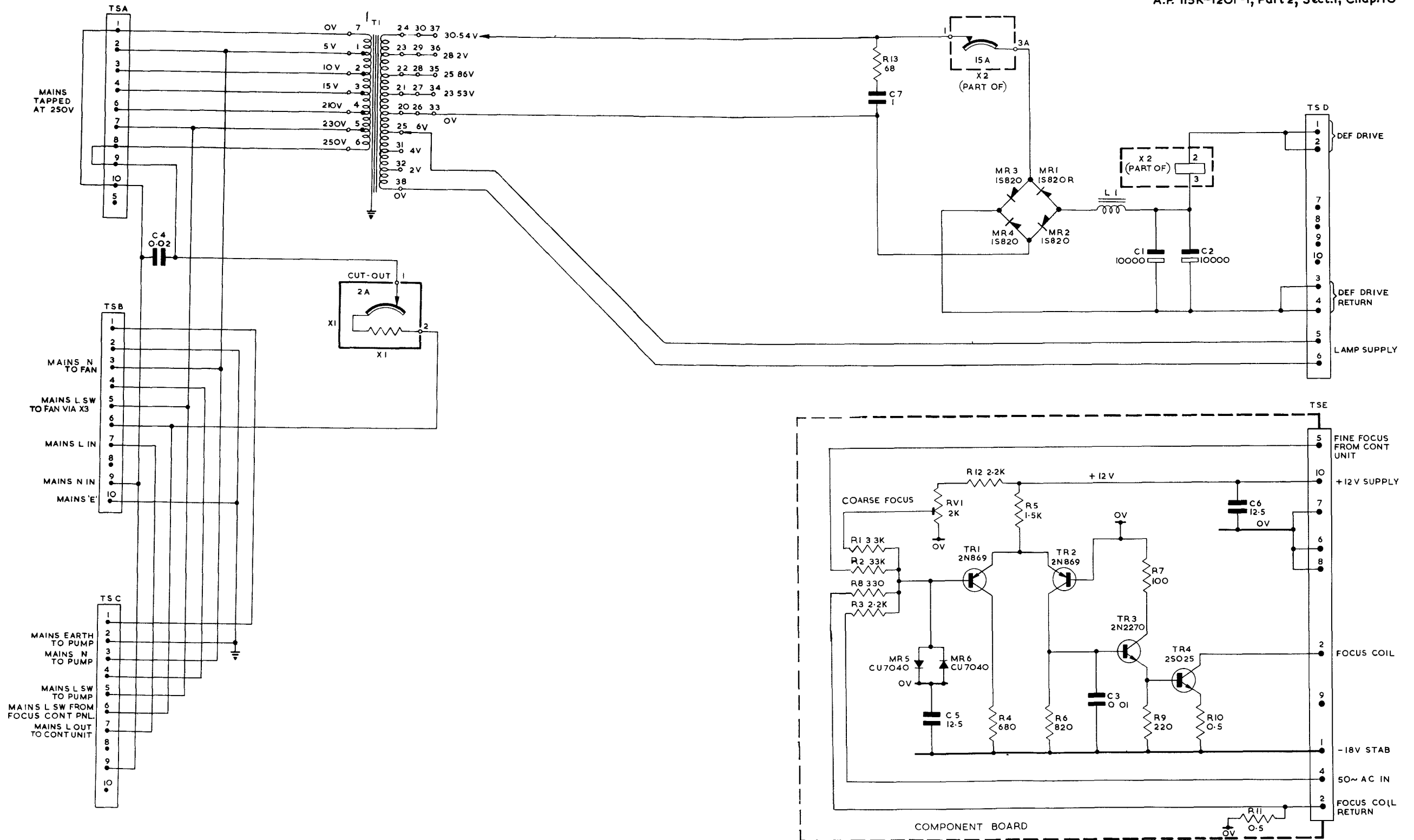
6. Transistors TR1-TR4 comprise the feedback amplifier whose function is to stabilise the current supplies to the focus coil. Voltages from the fine and coarse focus potentiometers are applied to the centre point of this amplifier to set the focus coil current.

7. TR1 base is the centre point of the amplifier, R8 the feedback resistor, and R1, R2 and R3 input resistors. Differential amplifier TR1-TR2 compares the centre point with earth potential and an output from TR2 collector is passed via emitter-follower TR3 to the base electrode of the series element TR4.

8. Diodes MR5-MR6 limit the voltage at the centre point of the amplifier to within 0.7V of earth potential.

9. One end of the focus coil is connected to the -18V rail via TR4 and a 0.5ohm resistor (R10) and the other end to the earth rail via a 0.5ohm resistor (R11). An increase in the focus coil current causes the potential at TR4 emitter to rise and the potential at the junction R8 and R11 to fall. The latter fall is translated by the stabiliser amplifier to a fall of potential at TR4 base. The potential across TR4 emitter-base junction thus moves in a direction causing a reduction of focus coil current.

10. The coarse focus control, RV1, is applied to the centre point via R1. A fine focus control, mounted on the control panel, is applied to the centre point via TSE5 and R2. A 50Hz signal, used when aligning the axis of the focus coil, may be switched to the centre point via TSE4 and R3.



6. The right-hand bracket is drilled to permit screwdriver access to a number of presets mounted on the printed wiring board behind; the metal of the bracket is engraved to provide identification of each potentiometer. The right-hand bracket also has attached to it a monitor block carrying eight test points for the power unit system.
7. A cross-member of the framework holds six taper pin blocks labelled A to F which are used for the interconnection of the power unit to the viewing unit assembly.
8. A metal stand attached to the back plate holds the four cut-outs labelled X2, X3, X4 and X5; the thermostat X1 is located below the stand but attached to the back plate.
9. The power unit is permanently wired into the viewing unit assembly by a cable-form so that for detailed servicing it would be necessary to remove the entire unit from the viewing unit and provide a dummy load as detailed in the unit test procedures.

CIRCUIT DESCRIPTION

10. The power units operate from a 200V-250V r. m. s. single-phase, 45Hz-65Hz supply and provide all the power supplies required by the viewing units. The tappings of the mains transformer are adjusted to the normal supply voltages and the units provide the following supplies:-

- (1) 6.3V r. m. s. at 2A maximum.
- (2) +100V d. c. stabilised at 100mA maximum.
- (3) +12V d. c. stabilised at 1A maximum.
- (4) +6V d. c. stabilised at 1A maximum.
- (5) -6V d. c. stabilised at 1A maximum.
- (6) -12V d. c. stabilised at 1A maximum.
- (7) 22V (nominal) d. c. unstabilised at 1A maximum (floating) (EHT. P. U.).
- (8) +19V d. c. unstabilised at 2.5V maximum (floating) (character drive amplifier).
- (9) -15V d. c. stabilised at 1A maximum (Power Unit Type 11606 only) (focus coil supply to 11605).
- (10) -18V d. c. unstabilised at 4.5A maximum (Power Unit Type 11600 only) (main deflection amplifier).

The common line is isolated from the chassis earth and must not be earthed to the metal work at any point in the viewing unit.

11. The stabilised supplies are protected against overloads by transistor-operated overload circuits. The stabilised 100V supply is not protected against overloads except by its comparatively high output impedance. Overload cut-outs are fitted to the mains supply line and the three unstabilised supplies. These four cut-outs are fitted with mechanical release and reset buttons.

12. A thermostat is fitted to the power unit back plate which operates at a temperature of 65°C and interrupts the relay supply of the main circuit breaker on the viewing unit control panel. This switches off the display. The power unit back plate will only reach this temperature if a fault develops in the cooling system or the power unit is not properly secured to the power unit cold plate.

Mains supply circuits

13. The power unit terminal strips A and B are used to distribute the mains supply within the viewing unit assembly. The mains supply is controlled from the viewing unit control panel and the reader is referred to the detail for on/off switching described there. The connections to the power unit transformer are made through terminal strip F and the transformer tappings are set to correspond with the nominal supply voltage by two links from F9 (line) and F10 (neutral).

14. At the 12in viewing unit, the mains supply enters the unit via A7 (line) and A9 (neutral). The circuit from A7 is fed out of the unit via B7, through the main circuit-breaker and relay contacts in the viewing unit control panel and back into the unit via B6 (switched mains L); then via the mains overload cut-out X2, terminal strip F pins 7 and 8 to the transformer primary winding. At the 21in viewing unit the mains L line is routed direct to the control unit and enters the viewing unit as mains L switched. The neutral line enters at A9 and is fed via the power unit 65°C cut-out X1, B9 and 83°C cut-out X2 on the deflection amplifier cold plate, B4 and A4, as the neutral supply to the Viewing Unit Control Panel Type 11606.

15. The overload cut-out X2 is rated at 2.5A and is operated by a heater strip only. This introduces a slight time delay and the cut-out does not operate on transient current surges. (The cut-out is fitted with an electro-magnetic release coil, but this is not connected.) The cut-out can be released and reset by two push-buttons fitted on the top of the unit. In the event of an overload activating the cut-out, the reset button must be pressed to restore the mains supply.

16. The thermostat X1 has a pair of normally-closed contacts which open at a temperature of 65°C and close automatically when the temperature falls again. The thermostat is in thermal contact with the power unit back plate and any rise in

temperature above 65°C causes the contacts to open-circuit which has the effect of releasing the main circuit-breaker relay on the viewing unit control panel. This relay cannot be energised and the mains supply restored until the contacts of X1 have returned to the closed position.

17. The coolant pumps and fans in both viewing units operate from a 225V r. m. s. supply. The 225V supply is obtained from the 5V and 230Vappings on the power unit transformer and fed to the pump via A3 and A5, and to the fan via B3 and B5. Power Unit Type 11606 supplies the mains for the main cooling system in the 21in viewing unit (there being two cooling systems in this unit).

Unstabilised supplies

18. The power supplies have separate secondary windings on the power unit transformer. A 6.3V a. c. supply is connected to terminals E8 and E9; C10 is connected across this supply to suppress transients. This supply is used for the c. r. t. heater and the viewing unit lighting circuits.

19. The 24V unstabilised d. c. supply is rectified by the bridge rectifier circuit employing silicon diodes MR26 to MR29 and reservoir C17. C5 is connected across the supply side of the rectifiers to protect them from transients on the mains supply. The heater strip of the 2A overload cut-out X4 is connected between the rectifier and C17, and its magnetic release coil is in series with the supply on the output side of C17. The heater strip operates the cut-out in the event of a large overload. The coil is connected after C17 so that pulses of short duration do not operate the cut-out. The cut-out carries two buttons which can be released or reset. This supply is used by the e. h. t. unit and is available on E7 +ve and E6 -ve.

20. The +15V unstabilised d. c. supply is rectified by the bridge rectifier employing silicon diode MR30 to MR33 and smoothed by L2 and C18. R6 limits the voltage developed across L2 by rapid change of load current and C7 limits the amplitude of the transient voltage developed across the rectifiers. The heater strip of the 4A overload cut-out X5 is connected between the rectifier and the smoothing circuit, and the magnetic release coil is connected on the supply side of the smoothing circuit. This prevents the magnetic release operating on surges when the load current changes. This supply is used for the character drive amplifier unit and is available on D1 (+ve) and E2 (-ve).

21. The nominal -15V unstabilised 4.5A d. c. supply is rectified by the bridge rectifier circuit employing silicon diodes MR22 to MR25 and smoothed by L1 and C16. R5 limits the voltage developed across the choke by rapid changes of load current. The rectifiers are protected against voltage and current transients by C8, R3, C9 connected across the mains side of the rectifier bridge. The heater strip of an 8A overload cut-out is connected between the rectifier and the smoothing circuit and its magnetic release coil is connected on the supply side of the smoothing circuit. This prevents the cut-out operating on surges when the load changes. This supply is used

by the final deflection drive amplifiers in the 12in viewing unit (supplied by Power Unit Type 11600) and is available on E3 (+ve earth) and E1 (-ve).

The stabilised supplies

22. The -18V d. c. stabilised supply (Power Unit Type 11606) is supplied from the bridge rectifier circuit described in paragraph 21, but connected across C16, are resistors R63 and R64 and Zener diode MR42. From this and the +12V supplies are derived the focus coil current (via a voltage regulator circuit in Power Unit Type 11605).

23. The +100V d. c. stabilised supply is rectified by the full-wave rectifier circuit employing silicon diodes MR17-MR18 and reservoir C15. The supply is stabilised at a nominal 100V by the Zener diodes MR19-MR26 and series resistors R1-R2. A stabilised supply at a nominal +18V is derived from this 100V supply by Zener diode MR21 and series resistor R4. This 18V supply on pin 20 (TP6) is required by the long-tailed pair of the +12V stabiliser supply and is not a power unit output. The +100V supply is required by the final stages of the video board and is available on D10 (+ve) and D3 earth common (TP3).

24. The four other stabilised supplies in this unit employ similar circuits, therefore, only the circuit of the +12V supply will be described in detail.

25. The +12V supply is rectified by the bridge rectifier circuit employing silicon diodes MR1-MR4 and reservoir C11. The rectifiers are protected against voltage transients by C1 connected across the supply side of the rectifiers.

26. The voltage across C11 is applied to a voltage stabiliser consisting of a series transistor whose impedance is controlled by a voltage comparator. The comparator compares a preset fraction of the output voltage with a fixed reference voltage (5.6V) and adjusts the impedance of the series transistor to maintain a constant output voltage. A protection circuit is provided to limit the current drawn from the supply to a safe value.

27. TR1 is the series transistor and its base current is controlled by the voltage comparator and amplifier employing TR5, TR6, TR7, TR2. TR3 is used in the over-load protection circuit.

28. Zener diode MR34 provides a stable reference voltage having a value in the range of 5.6V +5%. The temperature coefficient of a Zener diode varies with the current through it. Potentiometer RV2 is adjusted during manufacture to set the Zener current to the optimum value for the individual diode and should not be adjusted unless the diode is replaced.

29. The double transistor TR7 is connected as a long-tailed pair and used as a voltage comparator. The reference voltage is applied to the base of TR7a and a

preset fraction of the output voltage, obtained from the potential dividing network R18, RV3, R19, is applied to the base of TR7b. The exact fraction of the output voltage applied to the base of TR7b is preset by adjusting potentiometer RV3 SET +12V. The output of the comparator stage is amplified by the long-tailed pair TR5/TR6 and the emitter-follower TR2. The emitter current of TR2 flows into the base of the series transistor TR1 and controls its collector/emitter impedance. Potentiometer RV3 is adjusted during servicing to set the output voltage.

30. The overload protection transistor TR3 is cut off during normal operation of the stabiliser. The base/emitter voltage of TR3 is the algebraic sum of the fraction of the output voltage across RV1 and the voltage developed across R9 due to the load current, the two voltages are of opposing polarities, and if the load current exceeds the full rated load, the voltage across R9 will exceed that across RV1 and TR3 will be turned on. The collector voltage of TR3 then falls towards the +12V output line and takes the base of TR2 with it. The emitter of TR2 follows its base as the base/emitter voltage of TR1 approaches zero, which raises its impedance and lowers the output voltage. The resulting fall in load current turns off TR3, so that the process continues only until the overload is removed. The effect of this circuit is to limit the current to a constant value and allow the voltage to fall if the rated output is exceeded. The current at which the overload circuit operates is set by adjusting potentiometer RV1, +12V OVERLOAD. The +12V supply is available on E5, C2/C9 +ve (TP5) and D3/D8 -ve (earth).

31. The positive and negative supplies are interconnected through the external circuits contained in the printed wiring boards, and if the positive 12V supply fails, the negative supplies will try to drive current back into the regulator; diode MR35 is fitted to prevent this. MR35 is normally back-biased and has no effect, but if a negative voltage is applied to the +12V line, it conducts and connects this line to the common earth line and protects the transistors from damage.

32. The other three stabilised supplies employ similar circuits, except that the component values are different, and the power supply for the second long-tailed pair is different in each case, as follows:-

(1)	+12V stabilised	+18V stabilised supply
(2)	-12V stabilised	+6V stabilised supply
(3)	+6V stabilised	+12V stabilised supply
(4)	-6V stabilised	+6V stabilised supply

It is apparent from this that the stabilisers are interdependent and a failure of one supply may affect the other.

33. The corresponding supply output pins, potentiometers and test points are as follows:-

- (1) -12V available on C3/C8 earth and C4/C7 and D4 -ve (TP4)
RV4 -12V OVERLOAD; RV6 SET -12V
- (2) +6V available on C1/C10 +ve (TP1) and C3/C8 earth; RV7 +6V OVER-
LOAD; RV9 SET +6V.
- (3) -6V available on C3/C8 earth and C5/C6 and D5 -ve (TP2) RV10-64
OVERLOAD; RV12 SET -6V.

Fig. 1 Circuit for Power Unit 11606

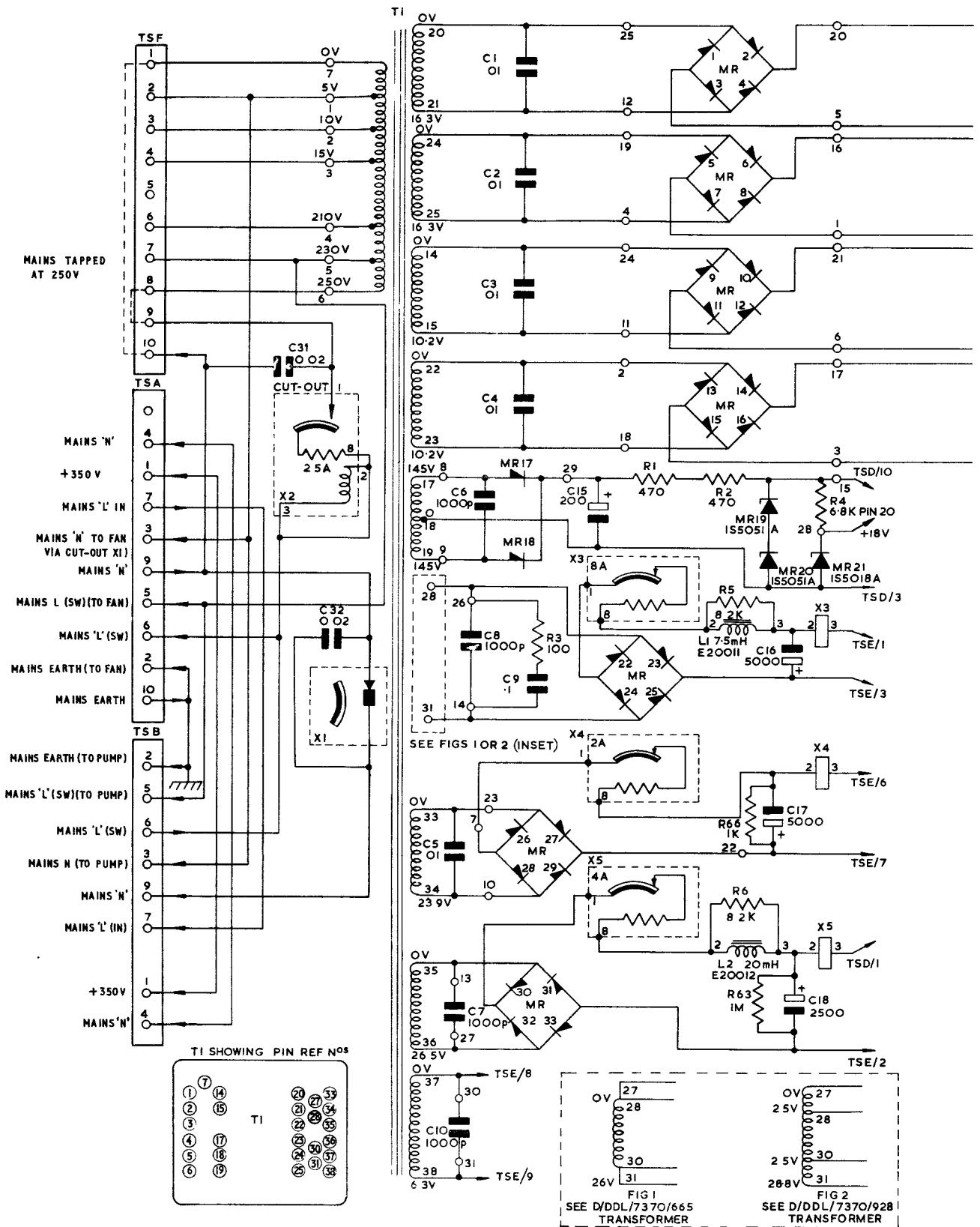
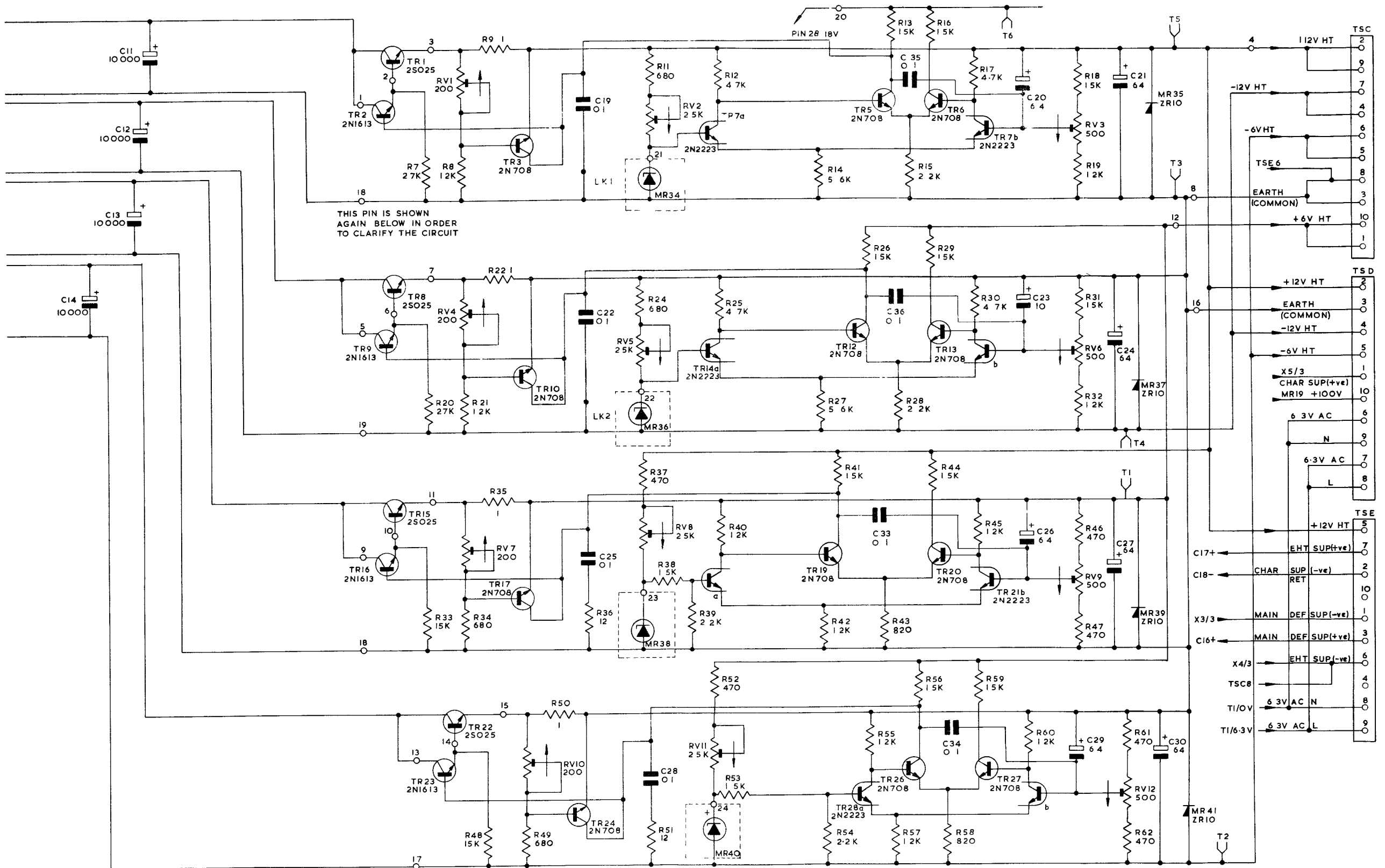


Fig. 1

Circuit for power unit 11606

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Circuit for power unit 11606

Chapter 12

VIEWING UNIT JUNCTION UNIT 12795/A (21in)

LIST OF CONTENTS

	Para.
Introduction	1
Mechanical construction	3
Circuit description	4
Line distribution	12

LIST OF ILLUSTRATIONS

	Fig.
21in viewing unit junction connections type 12795/A	1-4

INTRODUCTION

1. The junction unit interconnects between various groups of circuits within the viewing unit, between the display and external items of equipment and between the viewing unit and the control panels.
2. The interconnections between viewing unit and junction unit are carried by four 50-way Burndy Hyfen connectors. External connections to the junction unit are achieved by 15 removable plugs and sockets.

MECHANICAL CONSTRUCTION

3. The junction unit comprises five main sub-assemblies. These are as follows:-
 - (1) Two unitor panels, each containing two 50-way Burndy Hyfen connectors, SKTA to SKTD which mate with corresponding connectors in the viewing unit. The unitor panels also contain Dzus fasteners by which the complete junction panel is held in position.
 - (2) One relay bracket assembly containing the three relays RLA to RLC.
 - (3) One connector panel assembly carrying five plugs PLA to PLE, and ten sockets SKTE to SKTP, which mate with external cables.

- (4) One case assembly, constructed of 16 s.w.g. mild steel, which encases the complete junction unit. Access to the interior for servicing purposes is achieved by six Dzus fasteners which are released by a quarter turn. The internal cable loom is of sufficient length to allow withdrawal of the connector panel from the cover.

CIRCUIT DESCRIPTION

4. Relays RLA and RLB are the channel selection relays for the console address supervisory bit and are connected between pin S of PLA and pin U of PLD. Pin U feeds the relay live (switch) supply to one side of the relays and pin S the neutral. The neutral line is switched by the channel selection switches at the radar control panel.
5. When the Deputy Defence Commander only is operating at the 21in viewing unit, relay contact RLA/1 selects the DDC console address supervisory bit from either channel 1 or channel 2 as the output to the viewing unit. The supervisory bit 'enables' the production of the brilliance gates by the category selection board MJSB, hence the viewing unit will respond to the data addressed to the DDC only.
6. When the CCF and/or the CC (SAM) are also operating from the 21in viewing unit, the appropriate cable(s) is (are) transferred from the CCF and/or the CC (SAM) position(s) to the duplicate keyboard(s) at the viewing unit.
7. The CC (SAM) channel 1 and 2 console address supervisory bits are thus fed as the alternative inputs to contacts RLA/2 and similarly the CCF, channel 1 and 2 supervisory bits are fed to RLB/1. Changeover of the relay contacts simultaneously selects either channel 1 or channel 2 of all three inputs.
8. The three selected inputs are fed via the OR gate MR1, MR2 and MR3 and are combined as the output to the category selection board.
9. The 21in viewing unit will thus also present all l. r. d. data addressed to either of the additional addresses.
10. Relay RLC is associated with the i. f. f. video channel, and when energised switches through to the video board the i. f. f. video fed into the junction unit on socket SKTJ. When de-energised, relay RLC connects the input circuit of the i. f. f. video channel to signal earth.
11. At the MJR and ACC sites relay RLC is held permanently in the energised state, receiving its supply from Power Unit Assembly Type 60147/A via the Radar Control Panel Type 11057.

LINE DISTRIBUTION

12. The 240V mains supply is fed via plug PLE to TSB and is then distributed to the following points:-

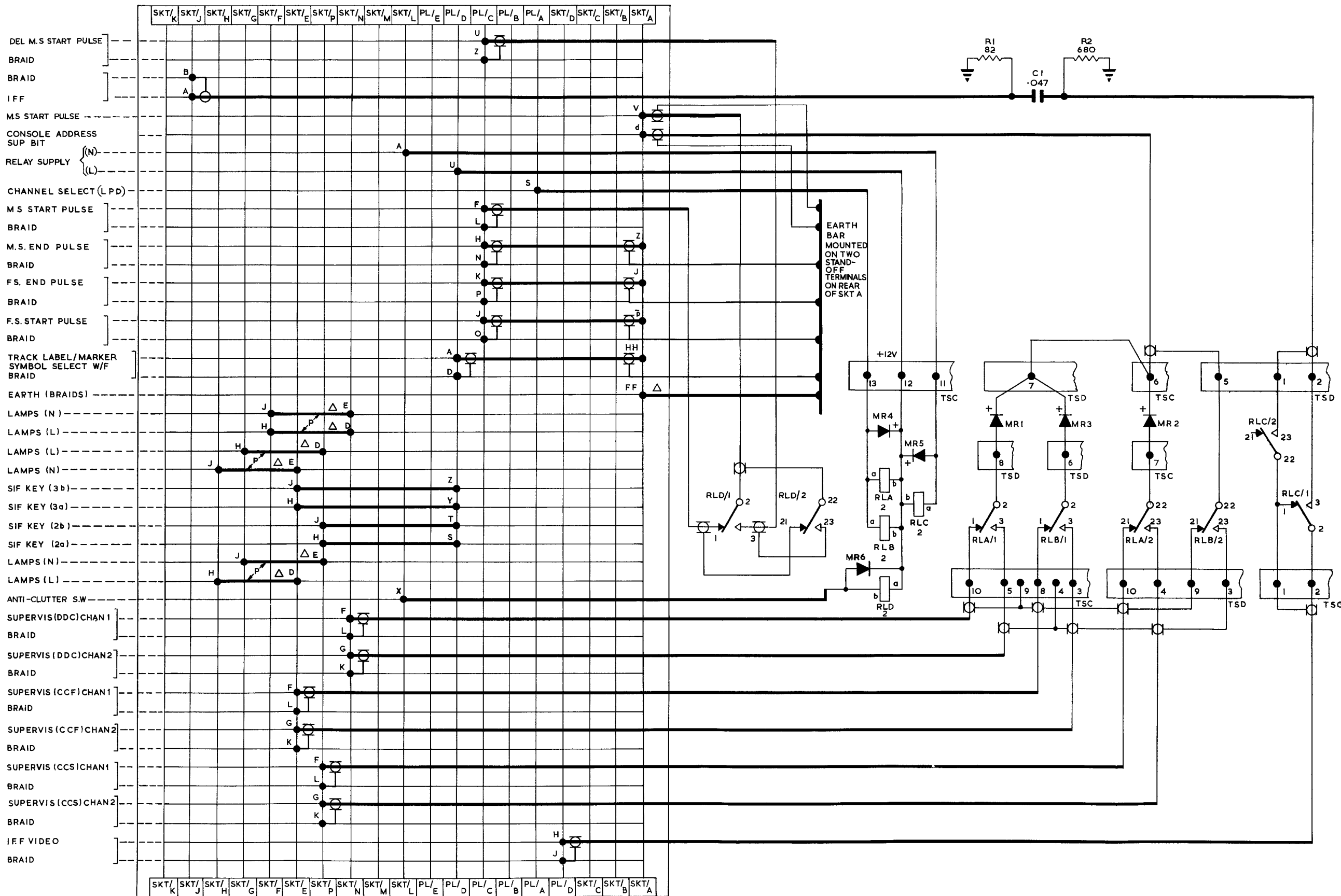
- (1) Socket SKTC into the viewing unit.
- (2) Socket SKTN out to the keyboard unit (11064) No.1.
- (3) Socket SKTP out to the keyboard unit No.2.
- (4) Socket SKTE out to the keyboard unit No. 3.
- (5) Socket SKTL out to the Radar Control Panel Type 11057.

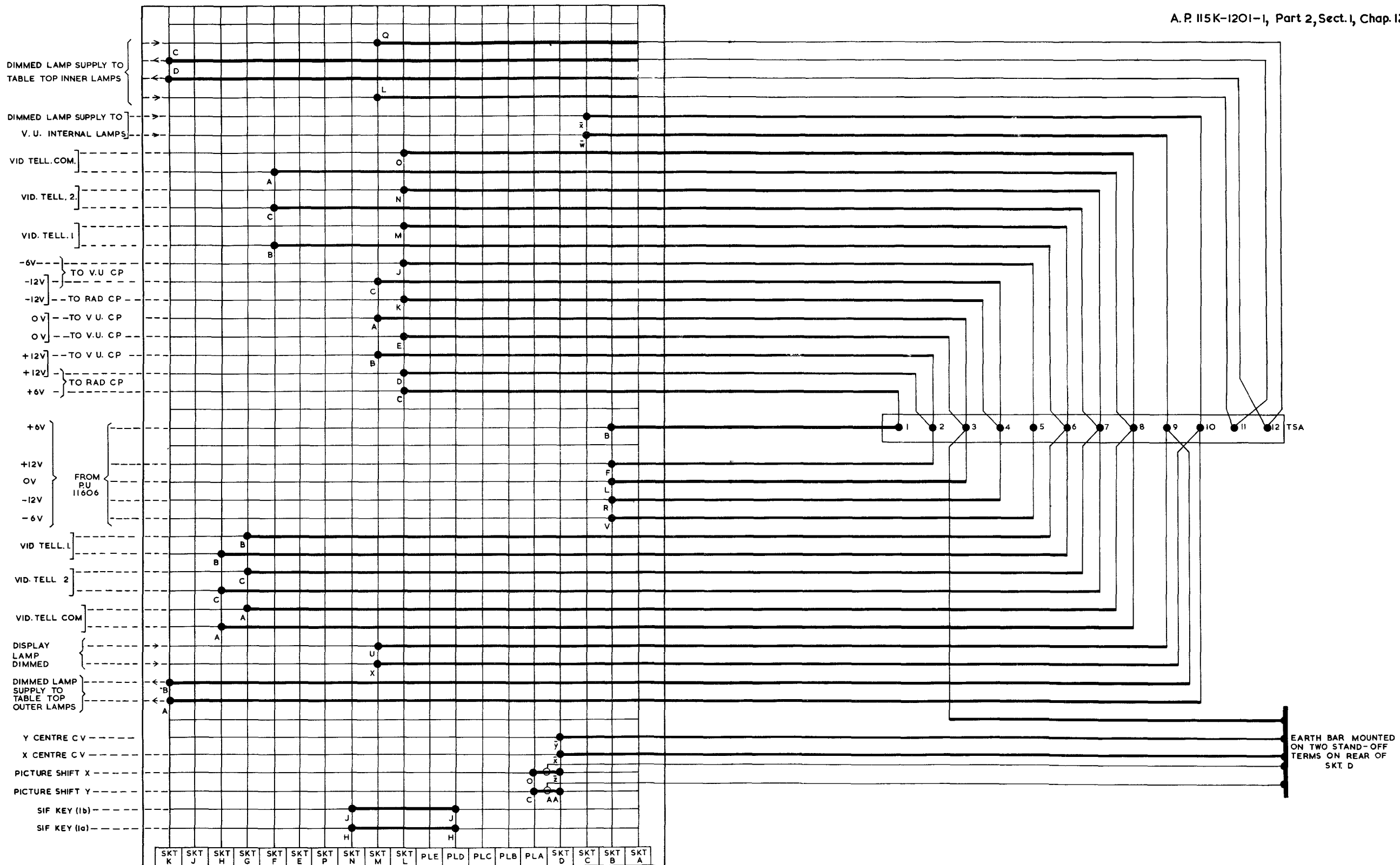
13. The mains are fed out via socket SKTM to the viewing unit OFF/STANDBY/ON switch in the Viewing Unit Control Panel Type 11066.

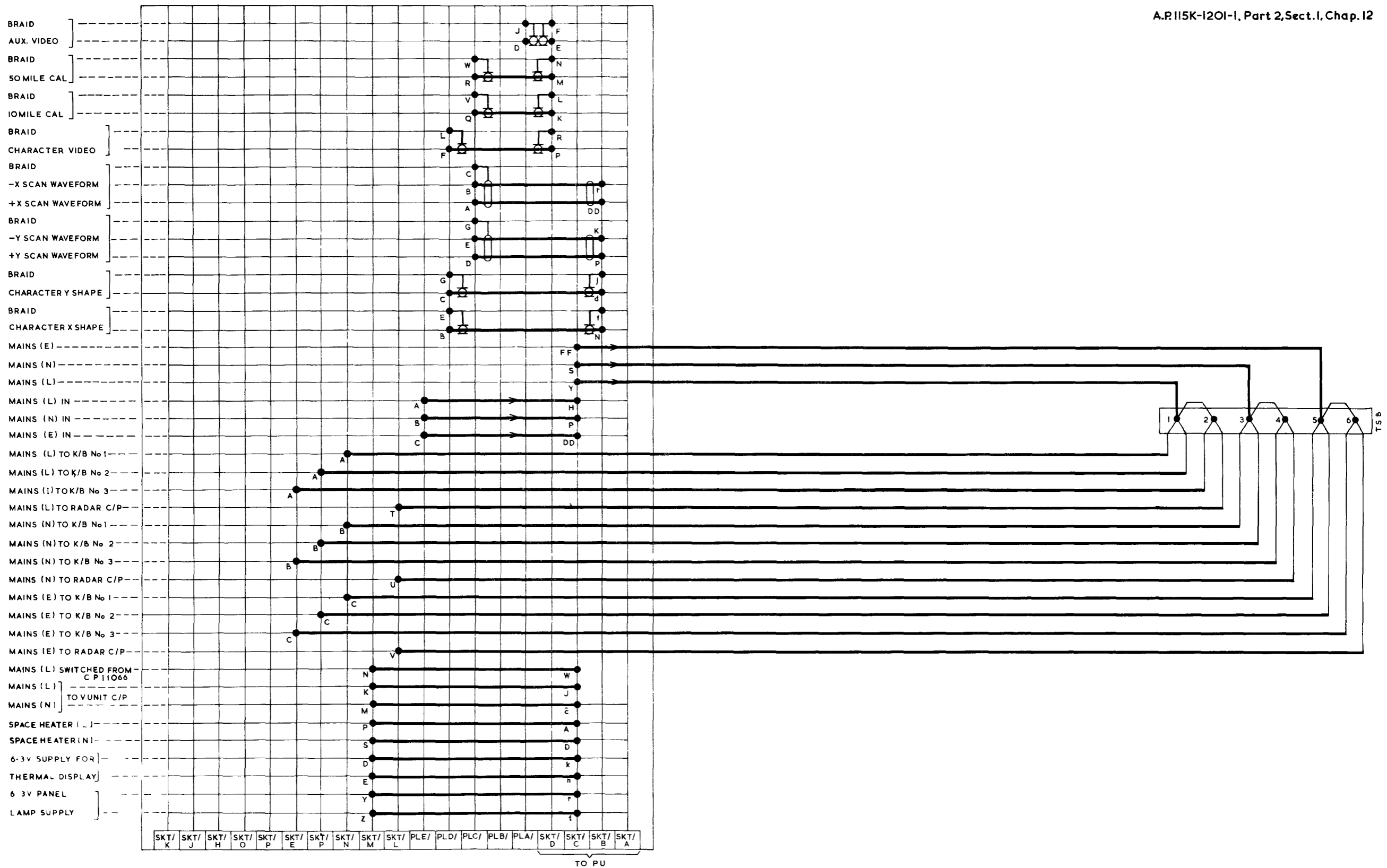
14. The d. c. supplies from the viewing unit main power unit are fed to TSA from where they are distributed to both the Radar Control Panel Type 11057 and the Viewing Unit Control Panel Type 11066. TSA also handles the video tellback lines from the computer controlled by the video selector switch on the radar control panel.

15. The lamp supplies fed out for the internal lamps and Table Top Type 12853/F are both routed from socket SKTC to TSA from where they are distributed to sockets SKTM and SKTK respectively.

16. All other signal lines are interconnected between the input and output connectors only.

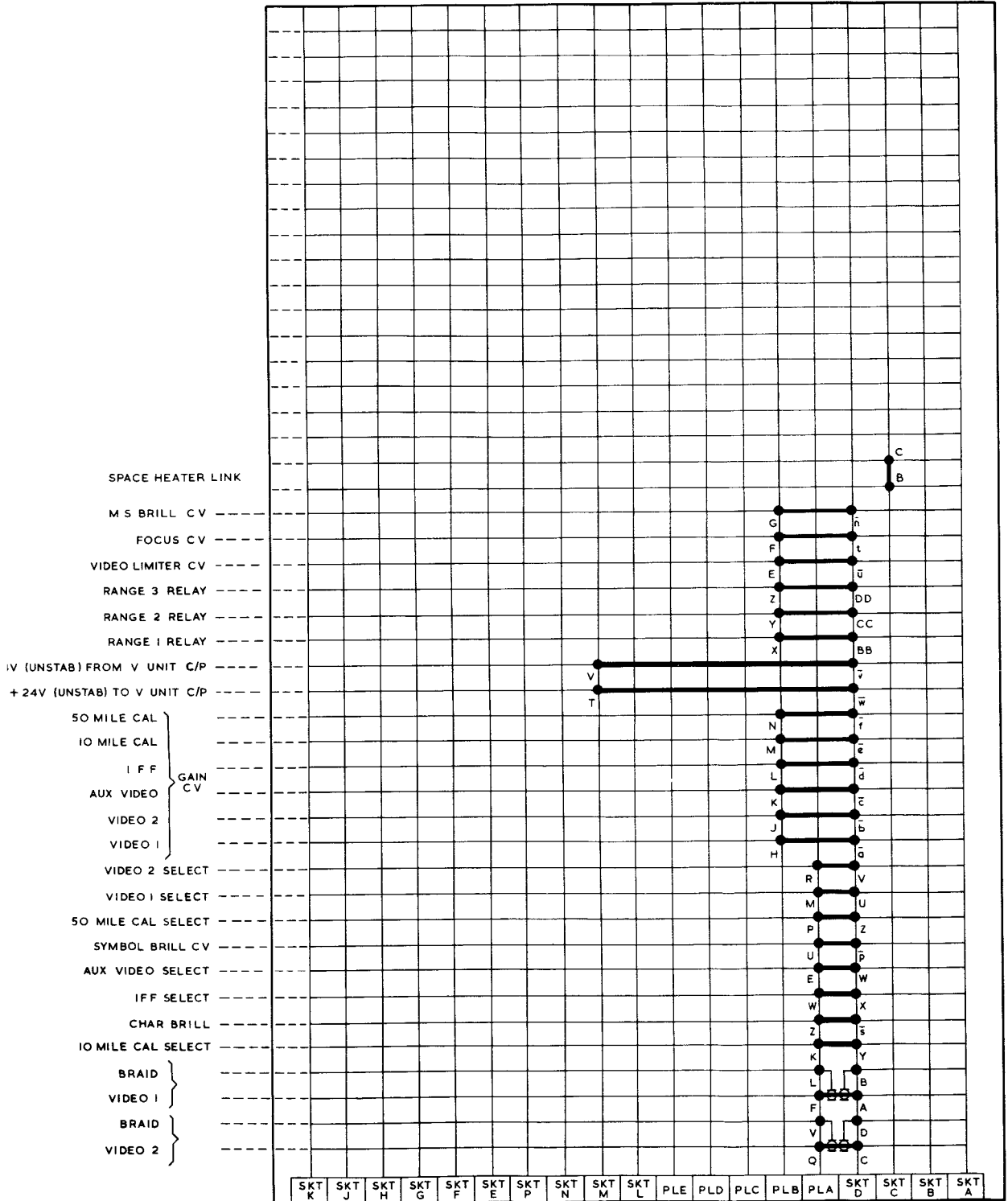






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A.P115K-1201-1, Part 2, Sect.1, Chap.12



Chapter 13

DEFLECTION COIL ASSEMBLY 11703A

LIST OF CONTENTS

	Para.
General	1
Mechanical details	2
Electrical details	4
Test data	5

LIST OF ILLUSTRATIONS

	Fig.
Deflection coil assembly 11703A: assembly	1
Deflection coil assembly 11703A: circuit	2

GENERAL

1. The Deflection Coil Assembly 11703A is used on 21in Mk. 5 displays. The assembly incorporates main coils for mainscan deflection and auxiliary digit coils for the small deflections required in writing characters in labelled plan applications of the display. The assembly of coils is encapsulated into a single unit to which a focusing coil assembly is attached. No servicing should be attempted by service personnel other than measurement at external terminals (see para. 5).

MECHANICAL DETAILS

2. The four deflection coils are wound on ferrox-cube cores (Fig. 1) and the coil connections taken to a terminal block within the coil encapsulation. Damping resistors are connected across all of the sections of the coils within the encapsulation, and in addition resistors are connected across the drive output from the drive amplifier.

3. The four digit coils are also wound on a ferrox-cube core with connections taken to the terminal block. The finish of each coil is commoned and a connection is taken out. The coil is enclosed within a Tufnol tube, which is bonded to the main deflection coil. The complete assembly is then encapsulated to form the deflection coil unit.

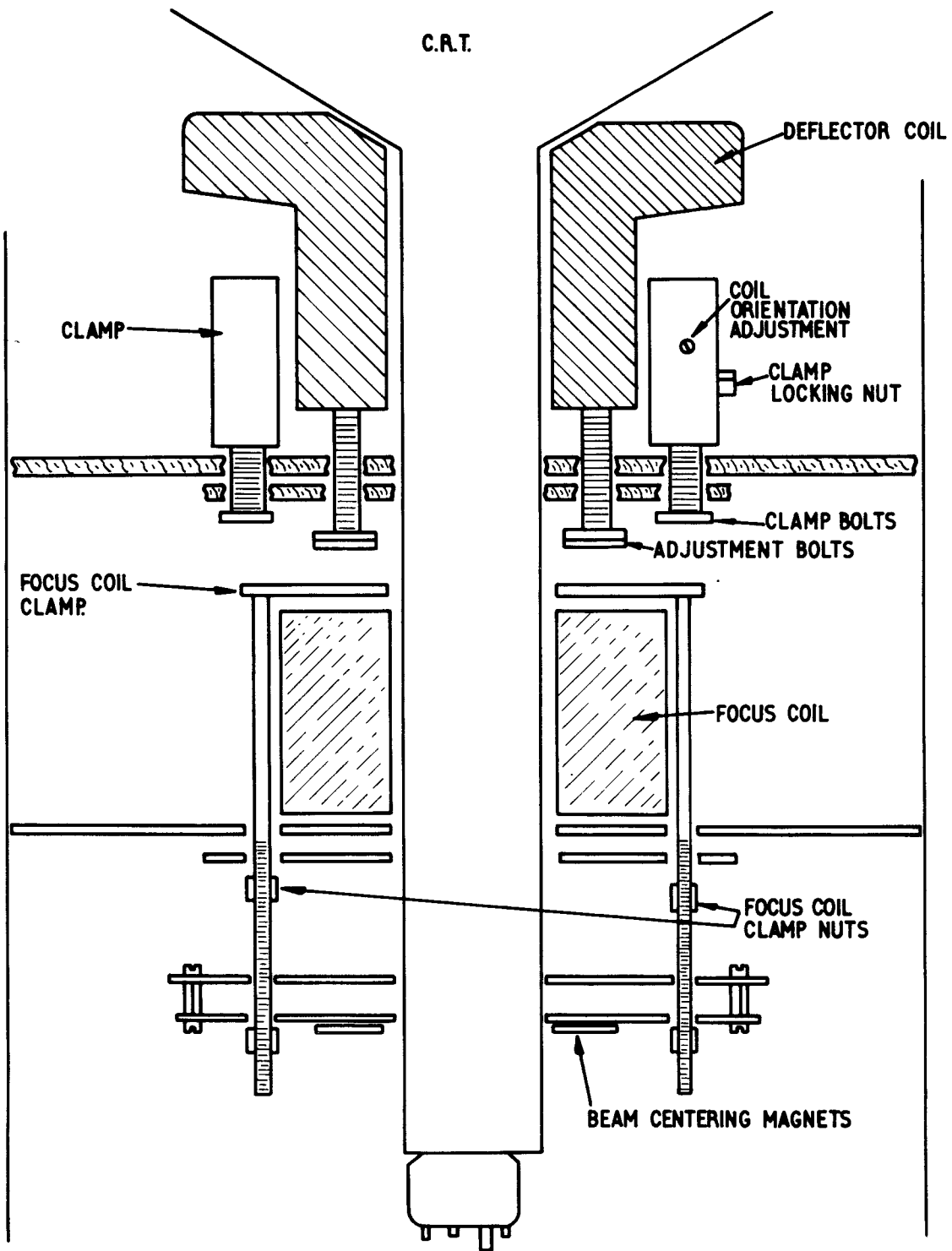
ELECTRICAL DETAILS

4. The 21in viewing unit employs an electro-mechanical focusing system using a

focus coil. The fine adjustment of focus is provided by the focus potentiometer on the Viewing Unit Control Panel Type 11066 varying the focus coil current. Coarse adjustment is similarly provided by the preset coarse potentiometer on the Power Unit 11605.

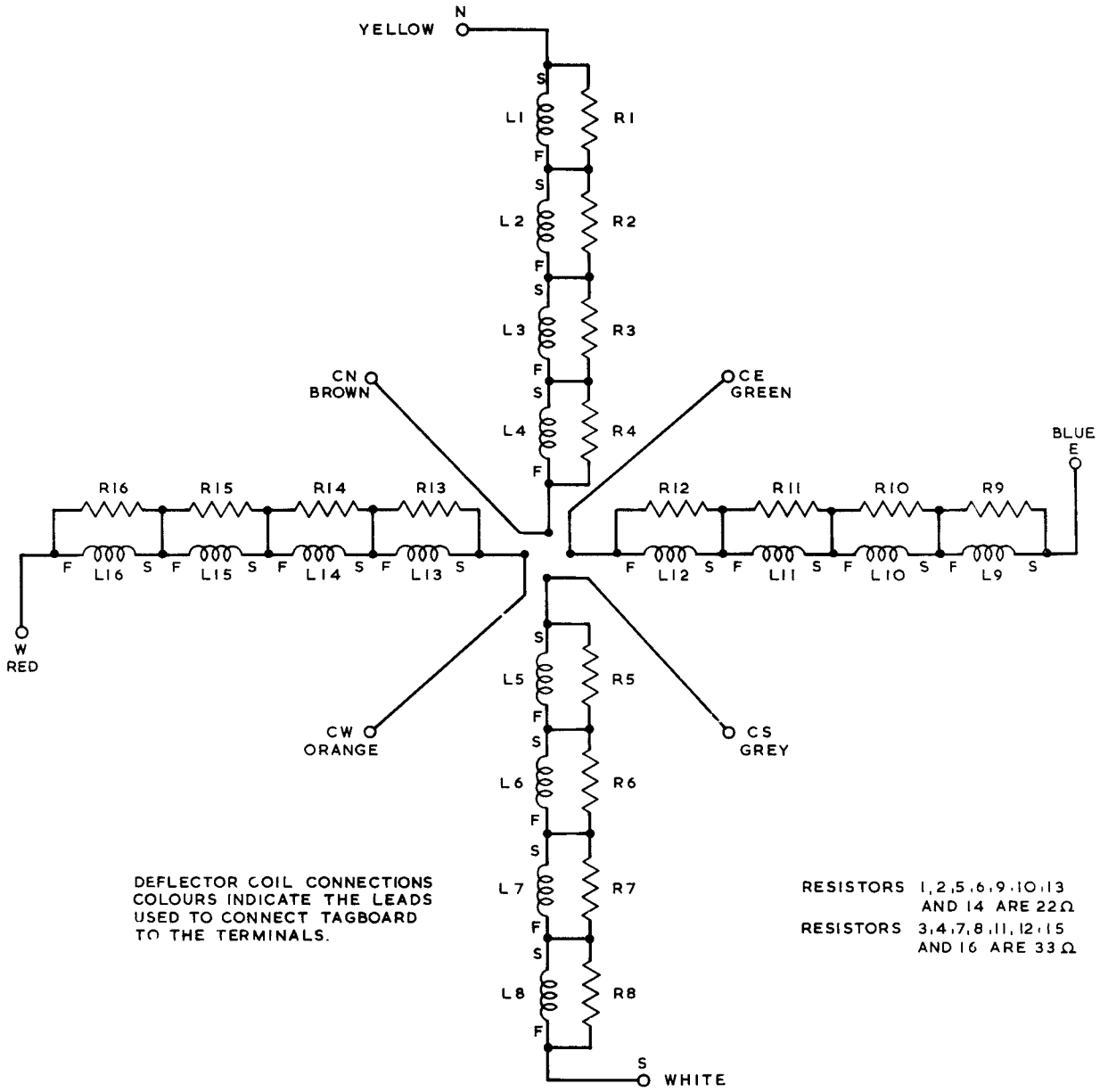
TEST DATA

5. The deflection coil inductors, measured between opposite poles (N to S or E to W) with CE linked to CW and CN linked to CS, is $290\mu\text{H}$. All readings $\pm 5\%$ measured at 1kHz. The digit coil inductance, measured between any pole and its common connection, is $9.5\mu\text{H} \approx 10\%$ measured at 10kHz.

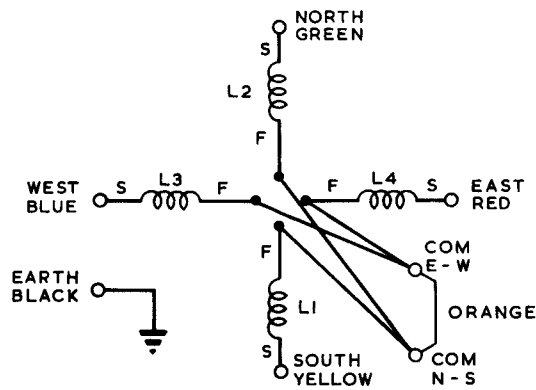


Deflection coil assembly 11703A: assembly

Fig. 1



(a) DEFLECTION COILS



(b) DIGIT COILS

Chapter 14

COOLING SYSTEM (21in)

LIST OF CONTENTS

	Para.
Introduction	1
Heat exchanger 11950A	3
Pump 12551/C	6
Electrical circuit.	7

LIST OF ILLUSTRATIONS

	Fig.
Main cooling system (board box and main power unit)	1
Subsidiary cooling system (final deflection amplifier)	2
Cooling system: electrical circuit	3

Introduction (Figs.1 and 2)

1. The Mk. 5 21in viewing unit employs two separate cooling systems each using a pump and heat exchanger. Cold plates (to which are attached the heat generating elements of the viewing unit) and a liquid-to-air heat exchanger are connected in a closed circuit and a light mineral oil is circulated through them. The main cooling system (Fig.1) circulates the coolant from the pump, round the power unit's cold plate, through the heat exchanger to the board box and back to the pump. The subsidiary system circulates from the pump, around the deflection drive amplifier cold plate, through the second heat exchanger and back to the pump.

2. The elements of the main cooling system are:-

- (1) Heat exchanger 11950A (cooler, liquid, 5840-99-948-9043).
- (2) Pump assembly 12551/C (pump, rotary, 5840-99-948-9059).
- (3) Power unit cold plate.
- (4) Board box cold plate.

The elements of the subsidiary system are:-

- (1) Heat exchanger 11950A (cooler, liquid, 5840-99-948-9043).
- (2) Pump assembly 12551/C (pump, rotary, 5840-99-948-9059).
- (3) Final deflection drive amplifier cold plate.

Caution

The power units and deflection coil drive amplifier must not be operated out of the display unless some arrangement is made for cooling.

Heat exchanger 11950A

3. The heat exchanger consists of an enclosed, coiled tube and a fan. The circulating oil flows over the fins on the inside of the tube and cooling air is drawn over the fins on the outside. The oil flow rate varies between 9 and 15gall/hr, depending upon oil viscosity with temperature. The temperature of the oil leaving the heat exchanger coil is 6°C cooler than that of the incoming oil. This unit is illustrated in Part 2, Sect.1, Chap.6, Fig.2.

4. The fan is a capacitance start-and-run induction motor driving two sets of paddles. The phase shift capacitor C1 is mounted on a central bracket at the rear of the viewing unit. The motor is rated at 50ft³/min of air transfer. The amount of heat transferred to the air depends upon the relative temperature of the viewing unit and the surrounding air, and can be the equivalent of 250W.

5. The heat exchangers are exposed by removing the west face cover of the viewing unit, thus exposing two air ducts each containing a heat exchanger. A small electric motor, driving two centrifugal fans, supplies cooling air to both ducts. When fitted, the cover so extends the ducts, that air is drawn in from, and exhausted to, the outside of the viewing unit.

Pump 12551/C

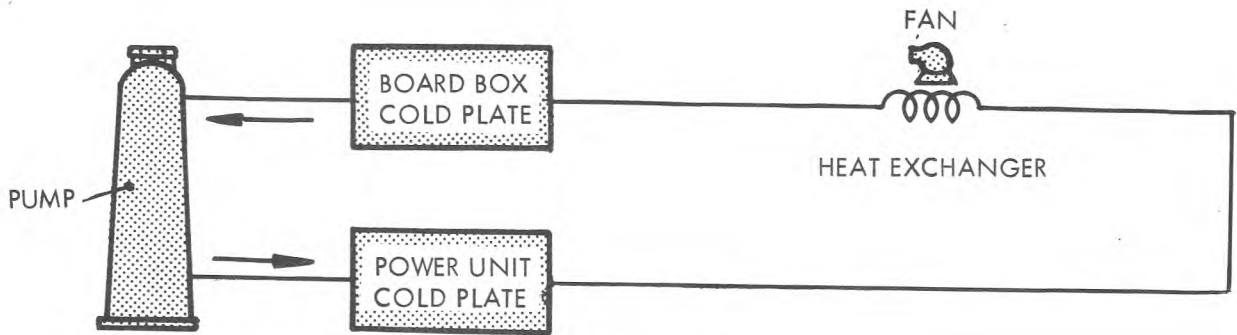
6. The pumps in both the main and subsidiary cooling systems are identical. Each pump is an integral unit consisting of a capacitance start-and-run induction motor, whose rotor shaft is extended in the form of a screw pump. The rotor and screw are immersed in the circulating oil. An expansion unit is incorporated at the base of the pump to allow for variation in the volume of oil with pressure and temperature. The normal pressure developed across the pump at 15°C ambient temperature is 12lb/in²; this condition gives a flow rate of 12gall/hr.

Electrical circuit (Fig. 3)

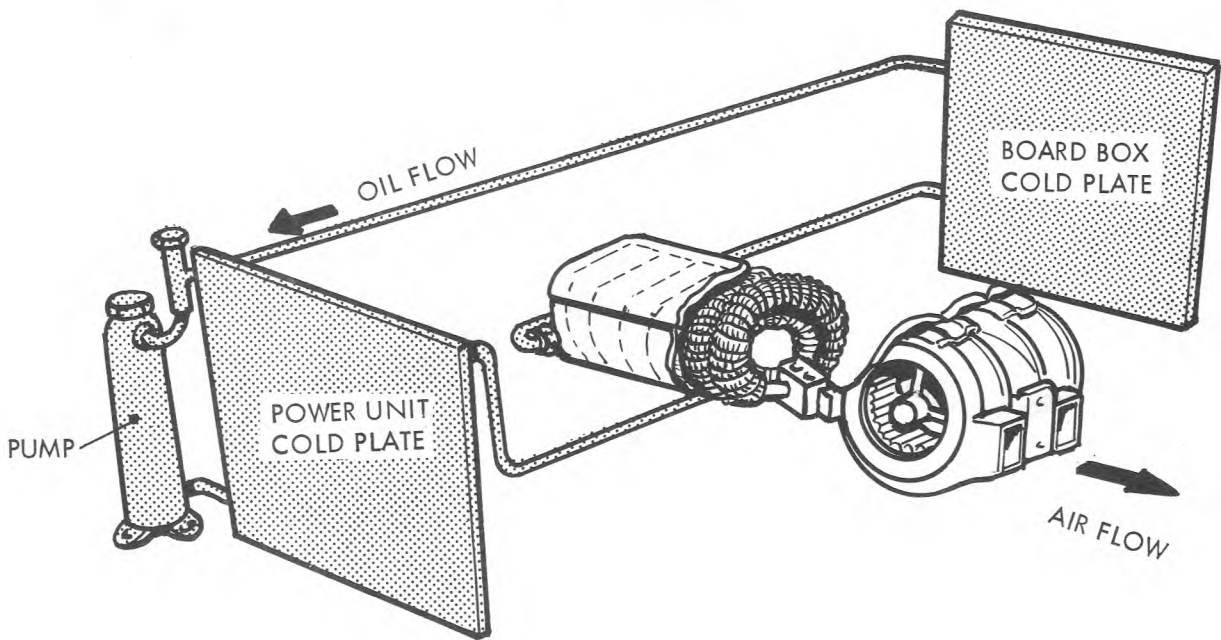
7. The coolant pump and fan for the board box and main power unit cooling system operate from a 225V r. m. s. supply. The 225V supply is obtained from the 5V and 230V tappings on the power unit (11606) transformer T1 and fed to the pump via B3 and B5 and to the fan via A3 and A5. This supply is available when either the

STANDBY or the ON push-button on the viewing unit control panel is pressed. The neutral line to the main contactor RLA is taken through two high-temperature cut-outs X1 (65°C) and X2 (83°C) either of which opens under high-temperature conditions, breaking the neutral line to RLA and switching the viewing unit off. A low-temperature (0°C) cut-out, located in the heat exchanger air stream, is connected in the neutral line of the fan supply to allow the viewing unit to reach the correct temperature in low ambient temperature.

8. Power Supply 11605 supplies a 225V r. m. s. supply from primary of HT transformer T1, to the fan and coolant pump of the final deflection cooling system. This supply is available when either the STANDBY or the ON push-button on the viewing unit control panel is pressed. The 225V supply is fed via B3 and B5 to the fan and C3, C5 to the coolant pump. A low-temperature (0°C) cut-out located in the heat exchanger air stream, is connected in the supply to the fan as for the main power unit cooling system, its action being identical to that stated before.



(A) SCHEMATIC



(B) SIMPLIFIED LAYOUT

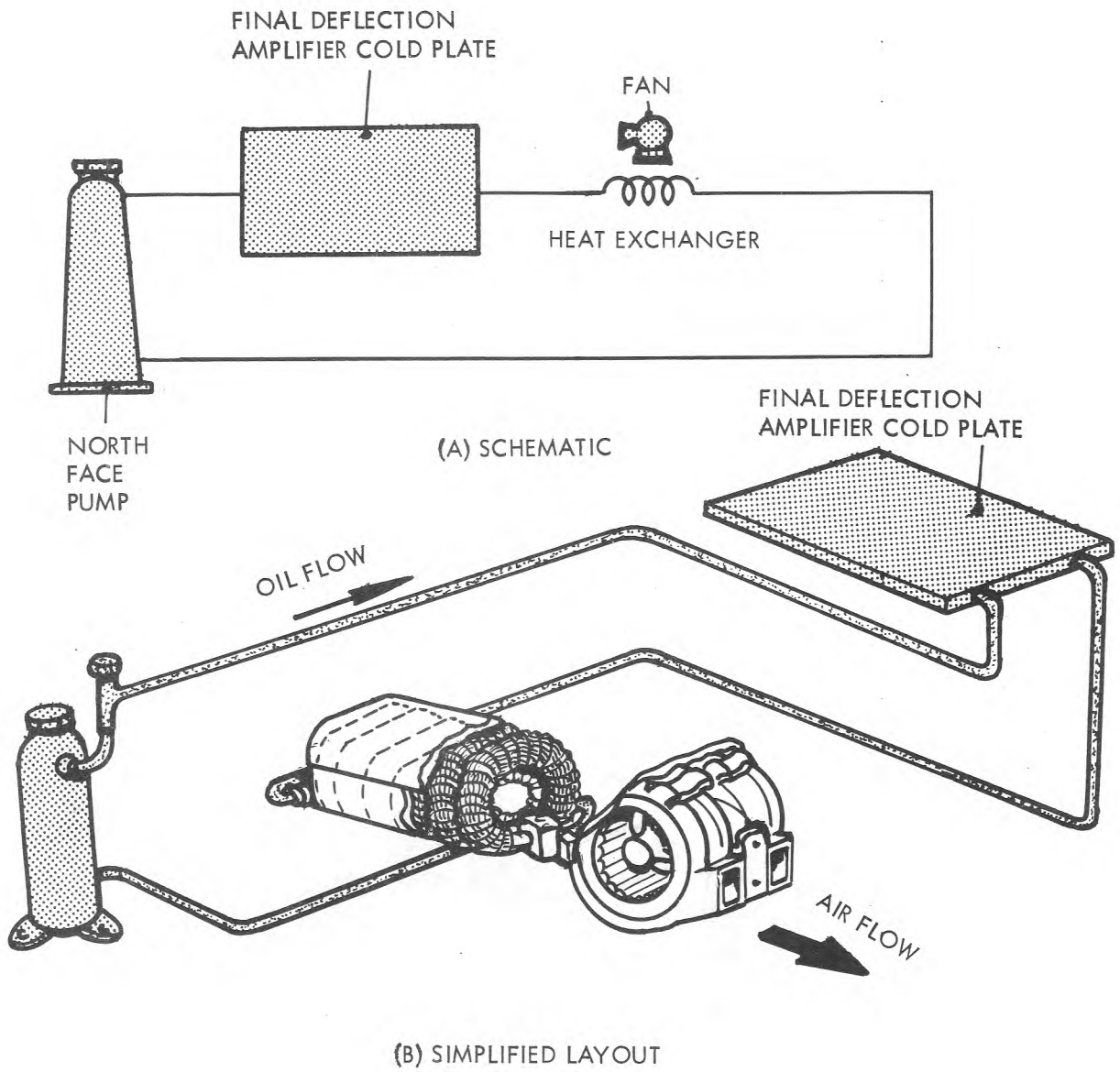
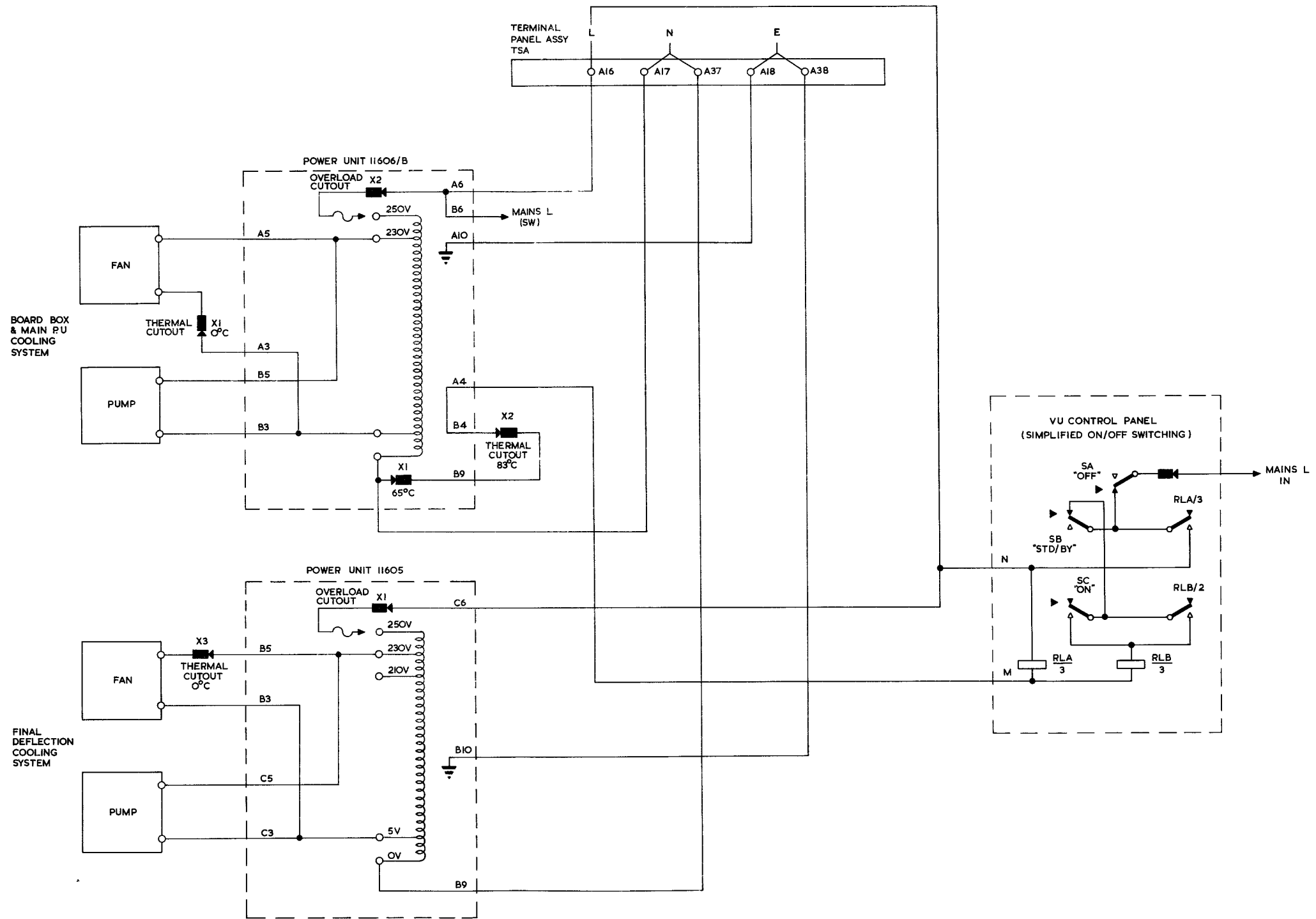


Fig. 2

Subsidiary Cooling System (Final Deflection Amplifier)

A.L.32 NOV, 71



Chapter 15

FOCUS CONTROL PANEL 12701

LIST OF CONTENTS

	Para.
Introduction	1
Description	2

LIST OF ILLUSTRATIONS

	Fig.
Focus control panel circuit diagram	1

INTRODUCTION

1. This panel contains the alignment, astigmatism and centring controls for the focus coil in the 21in viewing unit.

DESCRIPTION

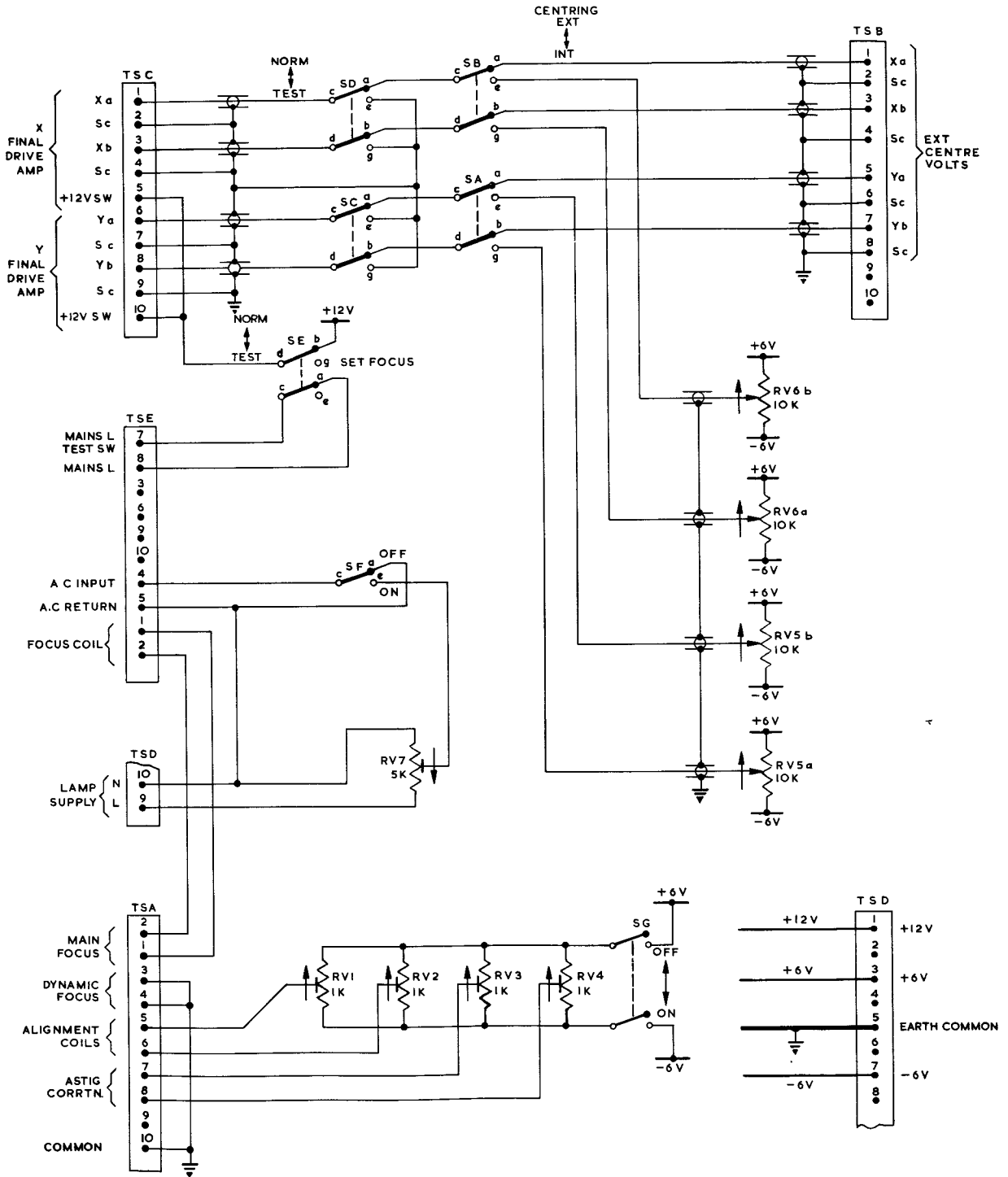
2. The panel is located under the east side cover of the 21in viewing unit, mounted across the top of this chassis section. The complete assembly measures approximately 17in × 4in × 2in and is secured to the viewing unit frame by four screws. All potentiometers are preset controls except RV5 and RV6, which are knob controls. External connections are made via taper pin blocks TSA to TSE which are secured below this panel.

3. The functions of the controls and switches are given below:-

RV1 and RV2	X/Y alignment
RV3 and RV4	X/Y astigmatism
RV5 and RV6	Internal centring
RV7	A. C. gain
SA and SB	X/Y INT/EXT centring
SC and SD	X/Y normal/test

SE	Set focus normal/test
SF	A. C. ON/OFF
SG	Align/astig ON/OFF

4. All the potentiometers with the exception of RV7 (A. C. GAIN) are connected between the $\pm 6V$ supply fed in from Power Unit Type 11606 via TSD.
5. To set up the focus coil, switch SE is set to the TEST position and switch SF to the ON position. SE interrupts the supplies to the final deflection coil drive amplifiers, one pole interrupting the +12V supply and the other pole the mains supply to the Power Unit 11605. SF applies a 50Hz signal, controllable in amplitude to a maximum of 6.3V by RV7, to the centre point of the focus coil current stabiliser amplifier (located in Power Unit Type 11605), thus periodically varying the focus coil current above and below the focused value.
6. The effect of this periodic variation of focus current is to paint on the c. r. t. face an unfocused lobe within which can be seen a focused spot. RV3 and RV4 are adjusted to make the lobe circular and RV1 and RV2 to move the spot to the centre of the lobe.
7. When SA and SB are in the INT position RV5a-b and RV6a-b supply the picture centring voltages to the deflection coil drive amplifier. SC and SD, in the test position, earth these inputs for test purposes. The EXT centring facility is not used in the GL161 21in displays.
8. Switch SG in the OFF position disconnects the two alignment and the two astigmatism coils during the focus setting-up procedure.



A.L.32, NOV. 71

Focus control panel 12701

Fig. 1

**UNIT SERVICING AND
SETTING - UP PROCEDURES**

Chapter 1

TIMING BOARDS (MJE SERIES)

LIST OF CONTENTS

	Para.
INTRODUCTION	1
OUTLINE OF OPERATION	
Switch and gate generating circuits	8
Radar trigger	9
Scan timing circuit	11
Delay unit	16
Gate waveform generators	18
MS/IS switch waveform generator	22
Aerial syncho supply and sampling gate generator	28
Sampling gate waveform generator	29
Synchro supply circuit	30
CIRCUIT DESCRIPTION	
Switch and gate generating circuits	
Radar trigger	34
Scan timing circuit	36
Delay unit	44
Gate waveform generators	46
MS/IS switch waveform generator	48
Aerial synchro supply and sampling gate generator	
Sampling gate waveform generator	51
Synchro supply circuit	53
Additional circuits	
Protection against supply failure	61
FS switch waveform	62

LIST OF ILLUSTRATIONS

	Fig.
Switch and gate waveform generator:	
functional diagram	1
Switch and gate waveform generator:	
idealized waveforms	2

ILLUSTRATIONS (Contd.)

	Fig.
Aerial synchro supply and sampling gate: functional diagram	3
Timing board MJEZ (12002): component layout	4
Timing board MJEZ (12002): waveforms	5
Timing board MJEZ (12002): circuit (Part A)	6
Timing board MJEZ (12002): circuit (Part B)	7
Timing board MJEZ (12002): circuit (Part C)	8

LIST OF APPENDICES

	App.
Timing board MJEC (12025A)	1
Timing board MJEG (12137)	2
Timing board MJEJ (12198)	3

INTRODUCTION

1. Timing board MJEZ is the basic timing board used in autonomous displays which employ the interscan system. The board generates all the switch and gate waveforms required by the display unit and also the drive supply for the aerial bearing synchro resolver. Trigger pulses derived from the associated radar installation are applied to the board to initiate the action of the timing circuits, so that the switch and gate waveforms are synchronous with the firing of the radar transmitter. In the case of a diameter-scan presentation, the board requires two radar trigger pulse trains, one from each of the two alternately-firing radar transmitters.

2. The circuit may be considered in two main sections:-

(1) The switch and gate generating circuit.

(2) The aerial synchro supply and sampling gate generator.

The aerial synchro supply and sampling gate generator provides the 'synchro excitation supply' and a pair of opposed 'sampling gate waveforms' synchronized with this supply and require to control the synchro demodulators in deflection boards. The switch and gate generating circuit generates an opposed pair of 'timebase gate waveforms', a 'brilliance and calibration gate waveform', a 'MS switch waveform', an 'IS switch waveform', a 'MS switch (shift) waveform' and an 'IS switch (shift) waveform'.

3. The board also carries a resistive link which is entirely independent of the other sections and which is used to feed a bias-off level to the unused fastscan sections of electronic switches in deflection and video boards.

4. Functional diagrams show the switch and gate generating circuit (Fig.1) and the aerial synchro supply and sampling gate generator (Fig.3). Links are provided (Fig.3) to select the circuit configuration suitable for either a radius-type presentation or a diameter-type presentation. In the following description both configurations of the circuit are described. For the h.r.i. application the circuit is connected in its radius scan configuration.

5. Associated with Fig.1 is the waveform diagram (Fig.2) showing idealized waveforms to aid explanation.

6. When studying these diagrams and circuit outline, the following points are relevant:-

- (1) As a general rule the circuits of the board generate timing 'edges' rather than timing 'pulses'; nevertheless, these edges will be referred to as pulses.
- (2) In the waveform diagrams the significant timing edges are drawn in bolder line.
- (3) The various elements of the board are annotated to show the direction of the output edge or pulse and to show the polarities required as trigger inputs. As examples, in the functional diagram of the switch and gate generating circuits the 'MS comparator' produces a negative-going pulse output (denoted \lrcorner) and the 'Delay 2' element is triggered by a positive-going edge (denoted \llcorner).

7. For information relating to the principle of timing and for detailed descriptions of the most commonly occurring circuits, refer to Part 1, Chap.2 and 4. For details of variants of the basic board refer to the appendices following this chapter.

OUTLINE OF OPERATION

Switch and gate generating circuits (Fig.1 and 2)

8. The operation of this circuit is shown in simplified form in the functional diagram (Fig.1). The circuit is considered in four groups: a scan

timing circuit, a delay unit, a gate waveform generator, a MS/IS switch waveform generator; they are discussed in this order below.

Radar trigger

9. The display is synchronized with the radar transmitters by the 'radar trigger A' and 'radar trigger B' pulses which enter on E15 and E16 respectively. In radius scan application the A trigger only is received. In diameter scan application both A and B triggers are received: the A trigger from the forward radar and the B trigger from the backward radar.

10. The triggers are combined in an OR gate to obtain a single trigger pulse train which is applied via an inverter both to the delay unit and the scan timing circuit.

Scan timing circuit

11. The scan timing circuit generates from the inverted radar trigger the following pulses:-

- (1) The 'scan-end pulse', which determines the end of both MS and IS scan regimes (and therefore the start of MS and IS shift regimes).
- (2) The 'IS knock-off pulse' which determines the instant at which the interscan ends.

12. The inverted radar trigger pulse applied to the sweep generator gate bistable (TR24-25 TR2) initiates the action of the scan timing circuit. The 'positive' output of the gate bistable inhibits the action of the sweep generator (TR30-33) until the radar trigger is applied. The radar trigger pulse causes the gate bistable to change state and the sweep generator is permitted to commence producing an output voltage which rises linearly with time; this output is applied to the MS voltage comparator (TR37-41). (The inverted radar trigger is also applied as 'end' trigger to the sweep gate bistable to ensure that the bistable is set to the correct condition when the display is first switched on.)

13. The MS comparator compares the sweep output with a preset d.c. voltage and at the instant the two are equal, it produces as an output the 'scan-end pulse'. Since the magnitude of this d.c. voltage determines the length of the scan regime, and since this in turn bears a direct relationship with the maximum display range, it follows that this voltage is preset according to the maximum range requirement of a given display. In display units in which it is required to switch the scan regime, the preset voltage is derived from a number of external preset potentiometers each receiving the bottom-set supply voltage.

14. The 'scan-end pulse' is applied to a gate waveform generator, discussed later, and an end-trigger to the sweep gate bistable. The positive output of the sweep gate bistable now inhibits the action of the sweep generator, causing its output to fall to the quiescent level from which all sweeps commence. The next-occurring inverted radar trigger pulse will again start-trigger the sweep gate bistable and the cycle described above is repeated.

15. The output of the sweep generator is applied also to a second voltage comparator circuit (TR3 TR42-46 TR53) which contains an inhibit circuit and is referred to as the IS comparator. The inhibit terminal of this comparator receives as control input a waveform known as the 'IS switch waveform', the derivation of which is discussed later. The effect of this input is to permit the action of the comparator in IS periods only. In this comparator the sweep voltage is compared with the 'IS range control voltage' and produces (in IS periods only) an output at the instant the two are equal; this output is called the 'IS knock-off pulse' and is used subsequently to brilliance-blank the IS line at the range corresponding to the level of the IS range control voltage.

Delay unit

16. The delay unit generates from the radar trigger the following pulses:

- (1) A 'timebase start pulse' used in the production of a 'timebase gate waveform' discussed later.
- (2) A 'calibration and brilliance start pulse' used in the production of a 'calibration and brilliance gate waveform' discussed later.

The unit comprises two electronic delay circuits connected in series; the first (Delay 1 - TR1, TR61-62) is triggered by the radar trigger pulse and generates the delayed 'timebase start pulse'; the second (Delay 2 - TR63-65) is triggered by the output of the first and generates the further-delayed 'calibration and brilliance start pulse'.

17. The radar trigger pulse applied to the autonomous display occurs some 1 to $5\mu\text{s}$ before radar zero time (which is the instant at which the radar transmitter fires). The delays are adjusted so that the timebase is started $0.75\mu\text{s}$ before radar zero time and calibration and brilliance brightening occurs coincident with radar zero time. The prior triggering of the timebase $0.75\mu\text{s}$ in advance of radar zero time is necessary to allow for the inherent delay of the deflection coil current at the start of each scan.

Gate waveform generators

18. The gate generating circuits produce the following waveforms:-

- (1) A pair of opposed 'timebase gate waveforms' used in deflection boards to control the operation of timebase circuits.
- (2) The 'calibration and brilliance gate waveform' used in other boards to time the calibration range marker pulse-train and the brightening of the trace.

19. The timebase gate generator comprises a bistable circuit (TR28-29) which is start-triggered by the 'timebase start pulse' and end-triggered by the 'scan-end pulse'. The rectangular waveform at the positive output operates between the levels of $\pm 2V$, the positive level defining scan regimes and the negative level the shift regimes.

20. The calibration and brilliance gate waveform generator circuit (TR26-27, 52) is also a bistable circuit, but with the addition of an OR gate element (MR5-6) to which two alternative end triggers are applied. The bistable is start-triggered by the 'calibration and brilliance start pulse' and end-triggered coincident with the 'scan-end pulse' (by the trailing edge of the negative sweep gate waveform) or the 'IS knock-off pulse'. In MS periods the 'scan-end pulse' will be the operative trigger, but in IS periods the 'IS knock-off pulse' will be operative, since this pulse occurs prior to the 'scan-end pulse' (except in the rare case where the range set into the IS range control equals the maximum range of the display and the two pulses are produced simultaneously and are equally effective). In certain units the maximum display range is less than the scaling of the IS range control, in which case the scan-end pulse often terminates the brilliance gate in IS regimes.

21. The positive output of the bistable comprises the 'calibration and brilliance gate waveform', which moves between levels of $\pm 5V$. This waveform is fed from the board via F21 to separate brilliance and calibration circuits which are gated into action whenever the waveform assumes its negative level.

MS/IS switch waveform generator

22. The MS/IS switching circuits generate two pairs of opposed switch waveforms as follows:-

- (1) The 'MS switch waveform' (scan or shift).
- (2) The 'IS switch waveform' (scan or shift).

These determine the frequency with which a mainscan is suppressed and replaced by an interscan. The factors which determine the choice of mainscan/interscan ratio are outlined in Part 1, Chap. 2; it is sufficient to say here that one of these factors may be the p.r.f. of the associated radar(s) and therefore the ratio can vary from display to display. In the circuit the mainscan/interscan ratio is determined by an IS timer which, together with two bistable elements and an inhibitor, forms the MS/IS switch group.

23. The MS/IS switch waveforms control the action of electronic switches in circuits concerned with the generation of shift waveforms and scan waveforms. Two independent pairs of switch waveforms are generated; one pair is fed to the scan circuits and the other to the shift circuits. The pair fed to the shift circuits may be replaced by steady levels which produce MS conditions in these shift circuits during both MS and IS periods, resulting in the interscan having the same electrical origin on the c.r.t. as the mainscan. This 'IS centre/off-centre' facility is provided as an operator's control.

24. The IS timer (TR34-36) comprises a beginning element which is triggered coincident with the production of a 'scan-end pulse' by the positive-going trailing edge of the 'sweep gate waveform' and produces simultaneously a negative-going edge output. This output is the 'IS start pulse' and is used to trigger the two switch bistables (TR47-48 and TR49-50). The timer takes a preset interval of between 15 and 100 display periods before it resets (depending upon the required MS/IS ratio); thus the positive-going edges of the sweep gate waveform which occur during this interval are ineffective. The first edge which occurs after the timer resets will trigger the timer again and the cycle of events is repeated. In essence the IS timer acts as a time-dependent inhibitor connected in the start-trigger inputs of the two switch bistables.

25. The bistable element generating the 'MS' and 'IS' switch waveform (scan) (TR47-48) is start-triggered by the 'IS start pulse' and end-triggered by a negative-going edge, from the sweep gate generator, coincident with the production of the next 'scan-end pulse'. The positive output moves between the levels of $\pm 5V$, assuming $-5V$ during IS periods and $+5V$ during MS periods and is referred to as the 'IS switch waveform (scan)'. This waveform is applied as control input to the inhibited IS voltage comparator (paragraph 15) and is fed from the board via F10 to the deflection boards where it switches 'scan' circuits between IS and MS modes. The negative output is the inverse of the 'IS switch waveform (scan)' and constitutes the 'MS switch waveform (scan)' fed from the board via F5 to 'scan' circuits on the deflection boards.

26. Bistable TR49-50 generates the 'MS' and 'IS' switch waveforms (shift)'; it is start-triggered and end-triggered by the same pulse as bistable TR47-48. However, the start-trigger is routed via inhibitor element TR4 MR8 which is controlled by the 'line shift on/off control voltage'. This control voltage is derived from an operator's control and fed to this board via E3. When this control input is positive the inhibitor transmits the start-trigger and the bistable operates normally, producing outputs identical to the switch waveforms described in the previous paragraph. When the control input is negative, the start trigger is inhibited and the bistable remains in its reset condition; the bistable output is then held steady at levels corresponding to MS conditions. The bistable outputs are fed from the board via F6 and F11.

27. The start and end-triggers applied to the MS/IS switch waveform bistables do not occur simultaneously, since the slight delay introduced in the IS timer makes the 'IS start pulse' the decisive and overriding trigger pulse of the two.

Aerial synchro supply and sampling gate generator (Fig. 3)

28. The function of this group is to generate a sinusoidal synchro supply and a pair of opposed trains of sampler pulses whose pulses coincide with the peaks of this synchro supply. In a diameter-scan presentation, it is further required that:-

- (1) The synchro supply and sampling pulses be synchronized with the associated radar transmitters.
- (2) The sampling pulse train p.r.f. be twice that of the synchro supply, so that the pulses coincide with both positive and negative peaks of the supply.

But in radius-scan or h.r.i. presentations, the sampling pulse train p.r.f. must be equal to that of the synchro supply, so that the pulses coincide with positive peaks only; this permits special demodulation techniques to be employed (Chap. 2) and the circuits need not be synchronized with the radar transmitter.

Sampling gate waveform generator

29. The sampling gate waveform generator monostable (TR8-10, TR67-68) is triggered by either the leading edge of the 'sweep generator gate waveform' (diameter-scan) or the output of a free-running 400Hz square-wave generator TR6-7 (radius-scan). The monostable produces a pair of opposed trains of pulses of duration adjustable from $30\mu\text{s}$ or $80\mu\text{s}$; in the diameter-scan case, these pulses coincide with the 'A' and the 'B' radar triggers. These pulses are fed to the deflection boards via E9 and E10.

Synchro supply circuit

30. The synchro supply circuit is triggered by either the 'B' radar trigger (diameter-scan) or by the 400Hz square-wave (radius-scan) (paragraph 29). The appropriate trigger is applied to a delay circuit (beginning element TR11-13), the output of which triggers a monostable element TR14-16. The delay circuit is adjusted to obtain coincidence between sampler pulses and the peaks of the synchro supply waveform. The monostable has an adjustable mark-space ratio which is adjusted to produce a square-wave. This square-wave is converted into a sinewave by a filter network which removes all frequencies above the fundamental. The frequency of this fundamental is radar p.r.f. for diameter-scan display or 400Hz for radius-scan display.

31. The sinewave output from the filter network is applied to power amplifier TR55-60, which generates a pair of push-pull outputs balanced about earth. These outputs constitute the 'synchro supply' fed to the aerial synchro. The output transformer is located on the associated junction unit.

32. The synchro supply is amplitude-stabilized at 35V peak-to-peak by a negative-feedback loop comprising rectifying circuit TR51b MR60-61 and d.c. amplifier TR19-22 TR51a. The inverted output from the power amplifier is rectified and the resultant d.c. is amplified and applied to monostable TR14-16 as a d.c. supply voltage.

33. Since the 'B' radar trigger (diameter-scan) is positive-going and the required triggering edge of the 400Hz square-wave (radius-scan) is negative-going, they must be applied to the delay circuit via different input points which are sensitive to the opposite trigger polarities. This is arranged by linking K-M or K-L, as applicable, at the input to the delay circuit.

CIRCUIT DESCRIPTION

Switch and gate generating circuits

Radar trigger (Fig. 6)

34. Radar trigger 'A' enters the board at terminal E15 (Fig.6); it is applied via an attenuating network C1, R1, R2 to limiter circuit MR1, MR2 which limits the peak level to +6V. Radar trigger 'B' enters the board at E16 and passes through a similar circuit. Both triggers are then combined by MR66, MR67, these diodes preventing interaction between the two trigger

circuits. Radar trigger 'B', in addition to being combined with radar trigger 'A', is also applied through link G-J (diameter-scan) to the synchro supply circuit.

35. The combined radar trigger pulses are d.c.-restored by MR54 and inverted by trigger amplifier, common-emitter stage TR1. The inverted pulses are applied:-

- (1) To the scan timing circuit (TR24-25, Fig.7).
- (2) To the delay unit (TR62).

Scan timing circuit (Fig.7)

36. The sweep generator gate circuit (Fig.7) is start-triggered by the inverted radar pulses, which are differentiated by network C66, R188, C26 and applied to TR24 base via MR27. TR24 and TR25 are connected as a bistable and their collectors alternate between levels of $\pm 5V$. The negative-going end-trigger is applied to the reset input point (C28-R8 junction) via MR3 and the inverted radar pulses also are applied to this point via MR4; thus, if the bistable assumes its 'on' condition when the equipment is first switched on, the first-occurring radar pulse will act as end-trigger. MR29 R79 form part of the reset input circuit and have the effect of inhibiting this input when the bistable is in its 'off' condition. Emitter-follower TR2 feeds the output at TR25 collector to the IS timer (TR34-36) and, via network R100-101, to the sweep generator (TR33) as control input. An output from the sweep generator gate is taken from TR24 collector to the synchro supply circuits (TR47-48, TR49-50).

37. The sweep generator employs a 'bootstrap' circuit and generates a sawtooth waveform. C37 is the charging capacitor and its charging current is the collector current of TR30, drawn through resistive charging network R102 R18 RV5. TR30 forms a conventional constant-current source of a relatively crude nature. The sweep generator is inoperative when the output of the gate bistable is positive, with TR30 collector current drawn entirely by the 'bottomed' TR33, so that there is zero charge in C37. When the gate bistable goes negative ($-5V$), TR33 cuts off and the collector current of TR30 commences to charge C37 via the resistive charging network. The potential change across C37 is applied to emitter-follower stage TR31-32, whose output is applied to the MS comparator circuit and as feedback via MR36 to the top of the resistive charging network. This feedback maintains an almost constant voltage across the charging network which in turn gives rise to an almost constant charging current. The potential across C37, and therefore the output potential, thus rises linearly. When the gate bistable goes positive ($+5V$) TR33 bottoms and C37 discharges rapidly through the low impedance of this transistor.

38. The composite emitter-follower pair TR31-32 presents a very high input impedance, and thus draws very little current from the charging capacitor. MR37-38 compensate for changes in V_{be} in TR31-32 which occur with changes in temperature. Zener diode MR36, connected in the feedback path, enables the total change in output level to be applied to the top of the charging network while at the same time maintaining the necessary potential difference between these two points (4.7V).

39. The sweep generator output rises linearly from a quiescent level of -6V, starting $0.75\mu s$ before radar zero time. Subsequent circuits arrange that the sweep gate bistable is reset as this output approaches earth level. The time taken for the output to reach earth level defines the interval of scanning on the c.r.t. and therefore must be made equivalent to the time corresponding to the maximum range requirement of a specific display. Since the constant charging current is always the same, the value of C37 determines the rate of rise and therefore the interval under discussion, and must be selected according to the required maximum display range. RV5 permits fine adjustments to be made.

40. The MS comparator circuit (Fig.7) comprises the two common-emitter pairs (TR37-38, TR39-40) connected as a long-tailed pair which acts as an overdriven differential amplifier, with the sweep output applied to one input (TR37 base) and a preset d.c. reference potential (derived from a 'bottom set' circuit as described in paragraph 43) applied to the other (TR40 base) via R121. C41, C81 accelerate the changeover as parity is reached and then hold the circuit steady for a short interval until after the sweep output has been driven negative with respect to the d.c. reference potential. The positive-going edge output from TR40 collector is amplified by TR41 and differentiated by network C42, R7 to give a negative-going narrow pulse output, the leading edge of which coincides with the instant parity is reached; this pulse is the 'scan-end pulse'.

41. The IS comparator circuit (Fig.7) is very similar to the MS comparator, but with the addition of an inhibitor in the output circuit. TR3, TR42, TR43, TR53 form two common-emitter pairs connected as a long-tailed pair with TR46 as the constant-current 'tail', the whole acting as an overdriven differential amplifier. The sweep generator output is applied to the TR3 base and the 'IS range control voltage' to the TR53 base as reference potential. The output produced at TR3 and TR42 collectors is fed via R149 to the base of inhibiting transistor TR45, which also receives the overriding 'IS switch waveform (scan)' via R128 and MR52. In MS periods this switch waveform is at a level of +5V, holding TR45 firmly bottomed. At the start of IS periods the switch level changes to -5V which

back-biases MR52 but leaves TR45 bottomed by the positive level from TR3 and TR42 collectors. When parity is reached, TR3 and TR42 collectors go negative, cutting off TR45; the positive-going edge produced on the TR45 collector is passed to the base of overdriven amplifier TR44 via network R125 and C60, the purpose of C60 being to preserve the rise-time. Amplifier TR44 is an inverting amplifier; the output is differentiated by C44 and R10 to produce the 'IS knock-off pulse'. At the end of IS periods, the switch waveform once more bottoms TR45 for the duration of the subsequent MS periods.

42. The 'starting' potential of the sweep generator output is the bottoming potential of the TR33 collector (paragraph 37), which will vary very slightly with temperature changes. To maintain the accuracy of the IS range control calibration it is necessary to vary the scaling of potential across this control in sympathy with the variations of the sweep output. This is achieved by a bottom-set circuit which supplies the negative level to the IS control. This negative level is obtained from the collector of TR5, which has an identical temperature coefficient to TR33 and whose d.c. bias conditions can be made to correspond exactly to those of TR33 by means of preset RV2. Zener diode MR9 stabilizes the voltage on RV2 slider.

43. A preset fraction of this bottom-set potential is applied also to the reference input of the MS comparator so that the instant of 'scan-end' is stabilized against temperature changes. This fraction is derived from the slider of RV1 connected in series with R197 in the collector circuit of TR5. Network RV1 R197 is removed in some displays and replaced by an external circuit.

Delay unit (Fig. 6)

44. The first delay circuit in the delay unit (Fig. 6) comprises TR1, TR61-62. TR1 forms a common-emitter trigger amplifier with a small positive bias (0.2V) on its emitter which holds the stage cut off during quiescent periods and provides a threshold to the incoming combined radar triggers. MR54 provides d.c. restoration for these pulses at TR1 base, ensuring that the negative period of the pulse corresponds to 0V. (The trigger amplifier stage is shown as an inverter in the functional diagram.) The inverted output is fed as start-trigger to the sweep gate generator and the monostable formed by TR61-62. Here C3, C103-104 are selected to obtain a recovery time approximately equal to that required by the specific delay and RV12 enables this interval to be set at an exact value (normally in the range 1-4 μ s). Opposed outputs are taken from the two collectors of TR61 and TR62, the positive-going edge via link R-S as trigger to the second delay circuit and the negative-going edge via link B-C as start-trigger to the timebase gate generator. In applications where there is no requirement for delay, the circuit may be bypassed; the second delay circuit then employs the positive-going radar pulses as trigger via link

W-S and the gate generator employs the negative-going inverted radar pulses as trigger via link A-C.

45. The second delay circuit (Fig.6) comprises an inverting amplifier (TR63) and a monostable (TR64-65) which are almost identical with those used in the first delay circuit. In this circuit the recovery time is set at $0.75\mu s$. Only one output is required, that producing the negative-going delayed edge, which is fed as start-trigger to the calibration and brilliance gate generator.

Gate waveform generators (Fig.6)

46. The calibration and brilliance gate generator (Fig.6) comprises a bistable (TR26-27) whose 'positive' output is fed out via emitter-follower TR52. The bistable is start-triggered by the output from delay 2 circuit and end-triggered by one or other of the outputs from the MS or IS comparators. The negative-going start-trigger is differentiated by C31 and R83 and applied to TR26 base via MR32 to cut off TR26 and to initiate the changeover. MR32 inhibits the start trigger when TR26 is already cut off. The alternative negative-going end-triggers are applied via separate diodes (MR5-6) to common resistor R9 and thence via differentiating network C32, R89 and MR33 to the TR27 base. MR5 and MR6 prevent interaction between the two end-triggers and MR33 inhibits these triggers when TR27 is already cut off. The 'positive' output at TR52 emitter, fed from the board on F21, moves between the levels of +5V and -5V, the negative level representing the 'calibration and brilliance on' condition.

47. The timebase gate generator (Fig.6) comprises TR28-29, which form a bistable circuit start-triggered by the negative-going 'timebase start pulse' and end-triggered by the negative-going 'scan-end pulse'. Both the positive and negative outputs are used, constituting the '-' and '+' timebase gate waveforms, which move between the levels of $\pm 2V$; these waveforms are fed out of the board on F2 and F4 respectively. MR34, MR35 inhibit one or other of the triggers, depending upon the state of the bistable. The collector and emitter potentials of this bistable are closely defined by Zener diodes MR12-13.

MS/IS switch waveform generator (Fig.7)

48. The IS timer, which forms part of the MS/IS switch circuit (Fig.7) comprises a circuit very similar to the first delay circuit described above, with TR34 as the trigger stage and TR35-36 as the monostable. The circuit is triggered by the first-occurring trailing edge of the 'sweep gate waveform'

after the monostable resets. The recovery time is comparatively long and may be of the order 0.02 seconds. Since many trigger edges occur during this interval (paragraph 24), an additional diode (MR40) is incorporated to inhibit these trigger edges from TR36 base; this diode constitutes the only significant difference between the two delay circuits.

49. The output at the TR35 collector, which goes negative as the monostable is triggered, is referred to as the 'IS start pulse' and is applied as start-trigger to the two switch waveform generators.

50. Both switch waveform generators (TR47-48 and TR49-50) (Fig.7) comprise standard bistable circuits with the addition of self-inhibiting diodes at their trigger inputs. The two generators are identical, producing pairs of opposed outputs moving between $\pm 5V$. Both bistables receive the same start-triggers and end-triggers, but the start-trigger applied to bistable TR49-50 is fed via R204 and an inhibitor circuit TR4 MR8 controlled by the 'line shift on/off control voltage' (E3). When this voltage is +6V, MR8 conducts and causes the start-trigger to be attenuated sufficiently (by R204 and the low impedance of TR4 emitter) to prevent triggering. When this voltage is -6V, MR8 is reverse-biased and the full trigger pulse is effective.

Aerial synchro supply and sampling gate generator

Sampling gate waveform generator (Fig.8)

51. The 400Hz square-wave generator comprises TR6-7 arranged as a conventional astable circuit (as described in Part 1, Chap.4). The output is taken from the TR7 collector and applied, when link E-F is fitted, to trigger inputs on the sampling gate generator and delay circuit TR11-13 via links H-J and K-L.

52. The sampling gate generator is triggered by either the output of the square-wave generator (link E-F) or the sweep gate generator (link D-F). The circuit comprises trigger stage TR8, monostable TR9-10 and emitter-follower stages TR67 and TR68. The supplies for both trigger and monostable stages are derived from the network consisting of Zener diodes MR10-11, R158 and R156, the Zeners being employed both as decoupling and stabilizing elements. TR8 is connected in common-base configuration and receives the negative-going trigger edge on its emitter via differentiating network C10, R27, C73, R28, with MR16 providing d.c. restoration. R24 and R28 keep TR8 cut off during quiescent conditions, thus providing a threshold level which the trigger input must exceed. The monostable is similar to that employed in the timing circuit (paragraph 48), except that its component values are changed to obtain a comparatively short recovery interval (30-80 μs); preset control RV8 enables this interval to be adjusted.

Synchro supply circuit (Fig.8)

53. The variable delay circuit (Fig.8) comprises a monostable TR12-13 (the recovery time of which is adjusted by means of selected R36 and preset RV3) and its trigger stage TR11. TR11 may be connected either as a common-base stage by fitting link M-Y or as a common-emitter stage by fitting link L-Y; thus in diameter-scan applications, positive pulses from the delay circuit (Fig.6) are linked via G-J and K-M to the base of TR11 connected in its common-emitter configuration, while in radius-scan applications negative pulses from the 400Hz generator are linked via H-J and K-L to the emitter of TR11 connected in its common-base configuration. In quiescent conditions MR19, connected between TR11 base and emitter in the network R34, R38-39, takes a small current and the resultant p.d. across it and the sense of its connection causes TR11 to be cut off by a negative base-emitter bias of approximately 0.3V. Trigger pulses applied to either base or emitter must therefore back-off this small current before TR11 commences to conduct. The diode thus provides both a threshold level and a d.c. restoration path in both circuit configurations. The output taken from TR12 collector is applied as trigger to square-wave generator TR14-16.

54. TR14-16 (Fig.8) form a monostable and its trigger stage, the recovery time being adjustable by specially selected R46 and preset RV4 to obtain the required 1:1 mark-space ratio.

55. The negative output from monostable TR14-16 is applied to low-pass filter network L2-4, C22, C53-54, C65 which passes only the fundamental frequency component to provide a sinewave output suitable for application to the synchro drive power amplifier. Most of the components of the filter are specially selected to suit the frequency employed in a specific display.

56. The synchro drive power amplifier (Fig.8) comprises TR55-60 together with a transformer on the associated junction unit, the whole forming an operational amplifier which provides a balanced output. Resistor R56 and specially selected R57 form the feedback resistor and RV9 the input impedance, thus enabling the gain of the amplifier to be adjusted. The input stage is formed by TR55-56 connected as a long-tailed pair and acting as a phase-splitter. The opposed outputs are then emitter-followed (TR57 and TR58) and applied to common-emitter stages (TR59 and TR60) which drive the centre-tapped output transformer. Feedback is shunt-derived from the secondary winding of this transformer via E11.

57. C23 provides a d.c. block between RV9 and the input circuit (Fig.8); since this capacitor requires a d.c. bias (provided by R153 connected to -12V), C67 is connected in the opposite sense to block this bias from the amplifier input. Current-sharing by the two long-tailed pair transistors is determined by two resistive potential divider networks connected one to each base and may be balanced by preset RV10. High-frequency stability is maintained by a top-cut network and a phase-shifting network; top-cut is provided by C68 connected between the opposed outputs of the phase-splitter, and phase-shifting by C69 connected in the feedback circuit.

58. The balanced output of the power amplifier is stabilized at 35V peak-to-peak by feeding a d.c. voltage proportional to this output as amplitude-control input to monostable TR14-16. This feedback loop (Fig.8) comprises a rectifier and a d.c. amplifier. The operation of the feedback loop circuits is given in paragraphs 59 and 60.

59. The power amplifier output at E11 is applied to preset attenuating network R151-152, RV7, is rectified by MR61 (which removes negative half-cycles) and is thence fed via emitter-follower TR51b and MR60 to reservoir and smoothing network R71, C20, L1, C19.

60. The positive d.c. output from the smoothing network is applied to highly stable d.c. amplifier TR22 (a double transistor), TR51a, TR19-21. TR22 is connected as a long-tailed pair and forms a differential amplifier, the reference input being a fixed fraction of the +6V supply fed via emitter-follower TR51a. The non-inverted output from the differential amplifier is amplified by another long-tailed pair TR20-21, the reference input being the full +6V supply. The inverted output of this pair is fed via emitter-follower TR19 and applied as the positive d.c. supply to monostable TR14-16. The amplitude of the square-wave produced by this monostable is proportional to this supply voltage; thus, if the synchro excitation supply exceeds the nominal amplitude, the supply voltage is reduced and vice versa. In practice RV7 and RV9 are adjusted in conjunction with one another to obtain a d.c. supply voltage of +5V (which means that the d.c. amplifier operates in the centre of its range) and thus obtain the correct output voltage.

Additional circuits

Protection against supply failure (Fig.6)

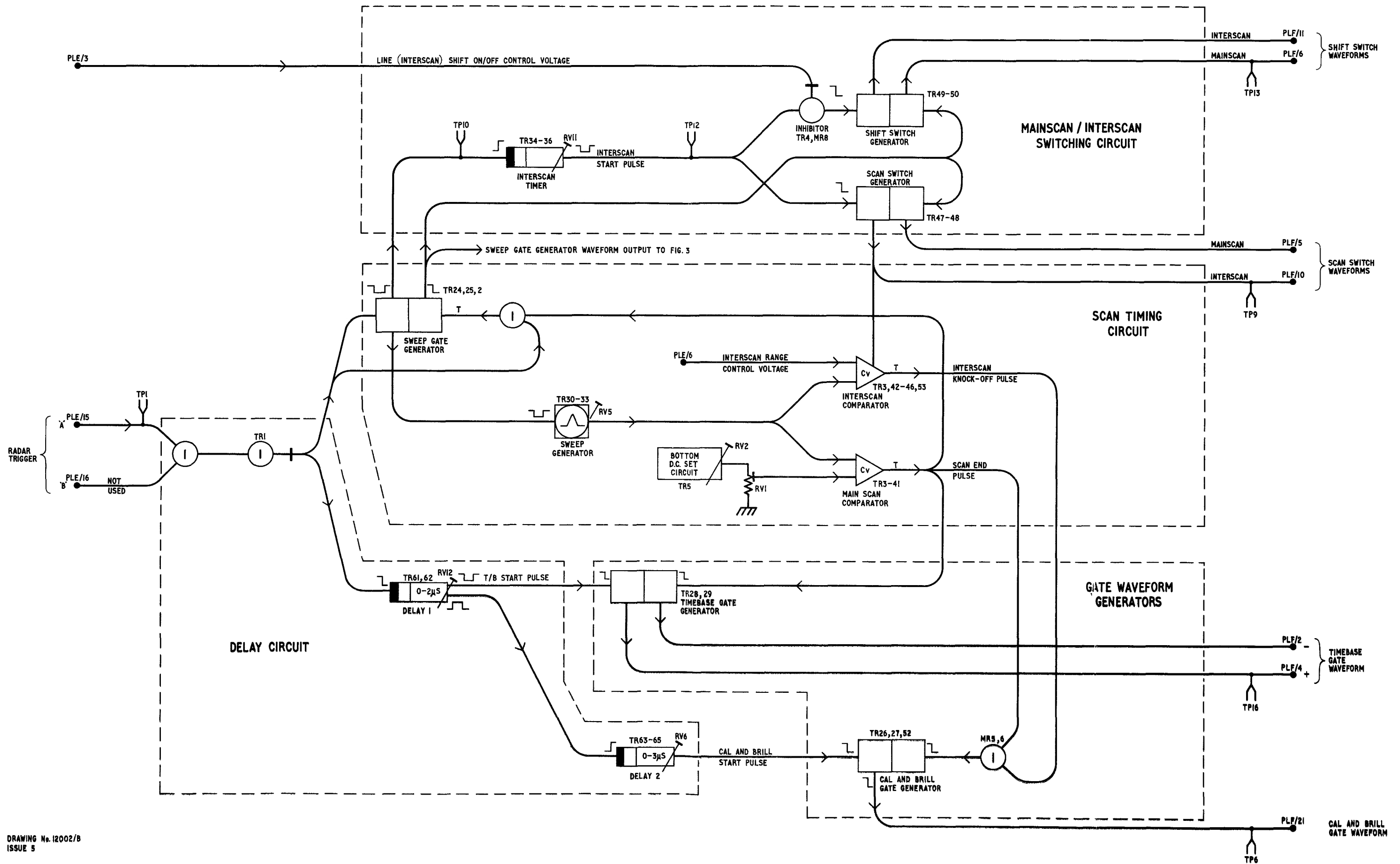
61. The four d.c. lines supplying the 6V and 12V to the board are heavily interconnected through the board's circuits. MR55-58 (Fig.6) are employed to protect the circuits from damage which would otherwise result if one of these supplies failed, since in their absence, that supply line would be driven in reverse polarity by the other supplies. In the normal condition all these diodes are back-biased, but should the +12V supply fail, the +12V line will be driven towards earth until it is arrested at earth by the action

of MR55. Similarly MR56, MR57 and MR58 arrest the -12V, +6V and -6V lines at earth. C61-64 provide the usual decoupling of supply line transients to earth.

FS switch waveform

62. Since this board is employed solely in interscan systems, but is associated with other boards which may be employed in interscan and fast-scan systems, a special positive d.c. level is derived for feeding to fastscan switch 'ways' on these other boards to hold those ways securely 'off'.

This level is derived from the +6V supply via R201 and F12 and is referred to as the 'FS switch waveform'.

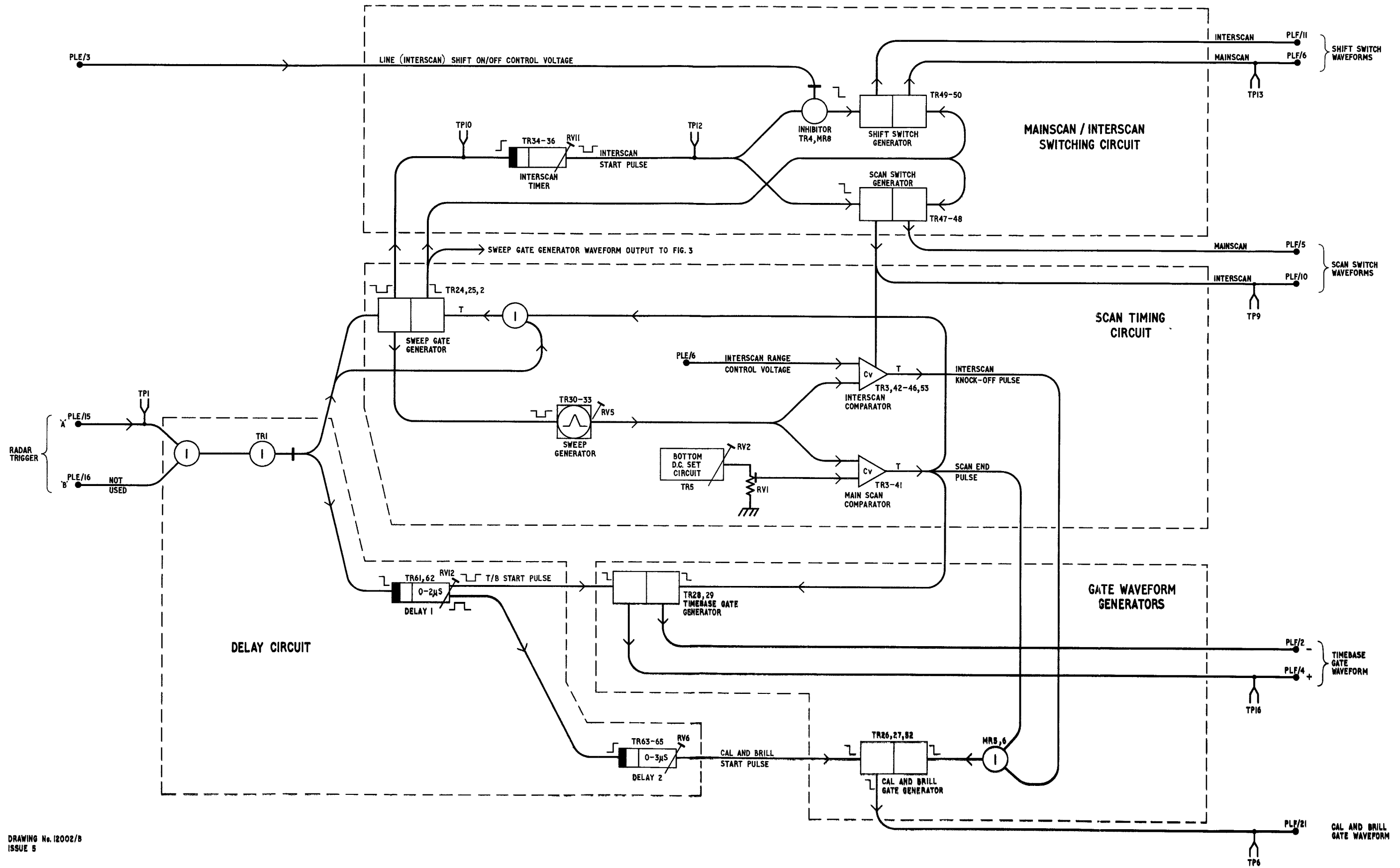


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A.L. 5, Mar. 70

Switch and gate waveform generator: functional diagram

Fig. 1

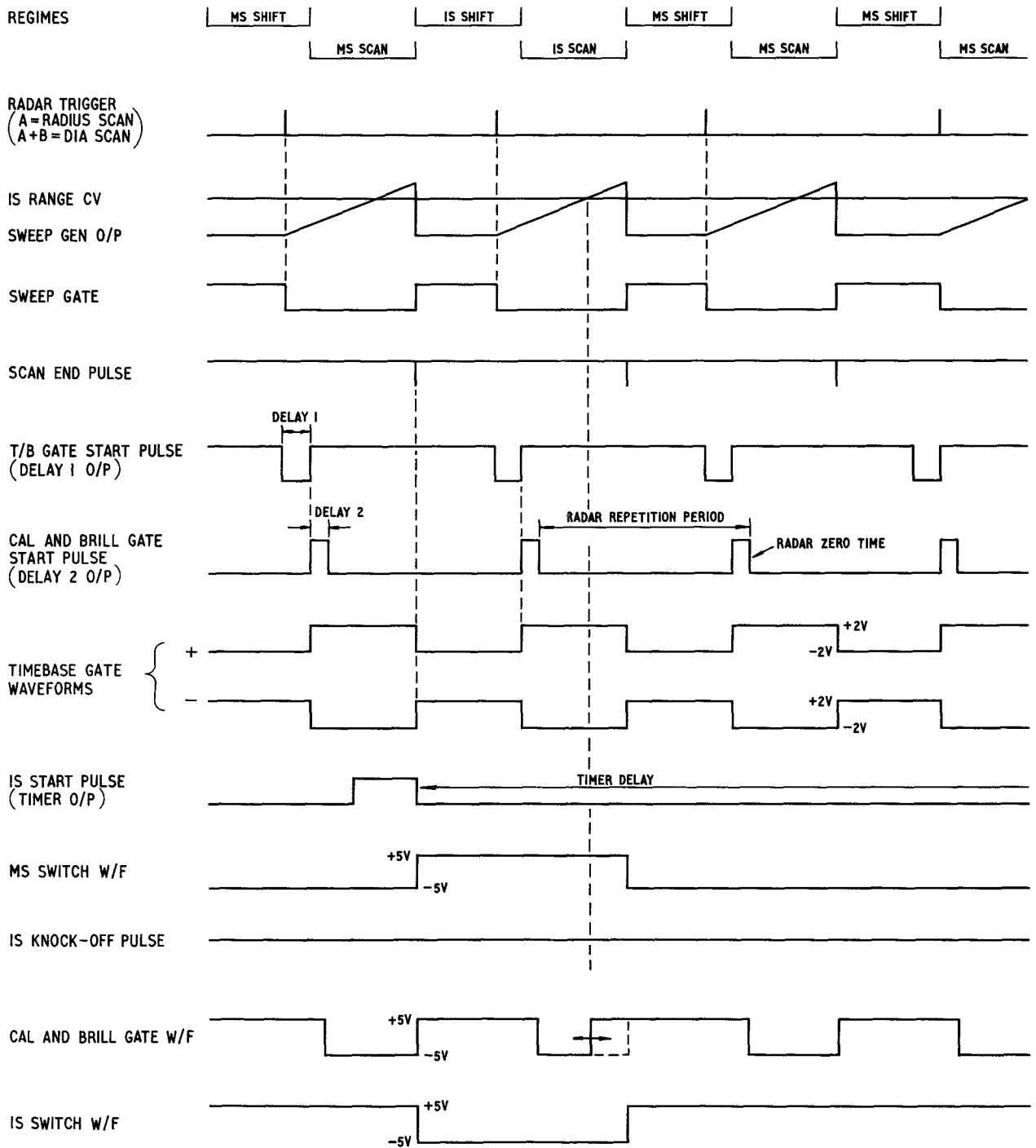


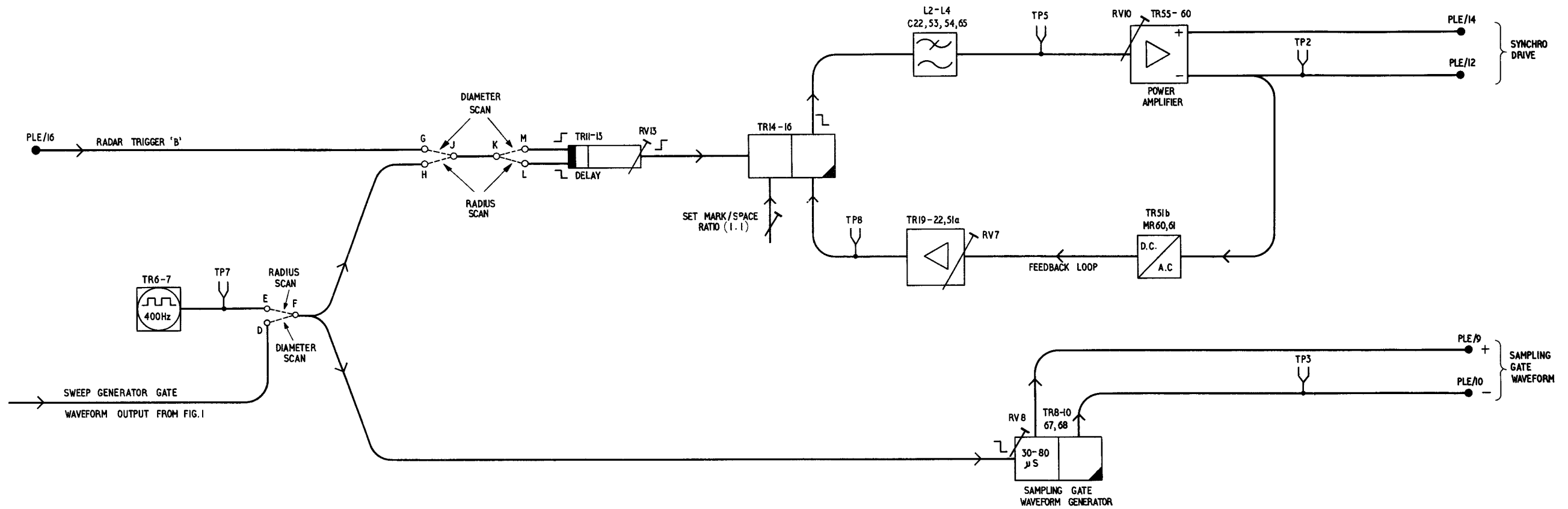
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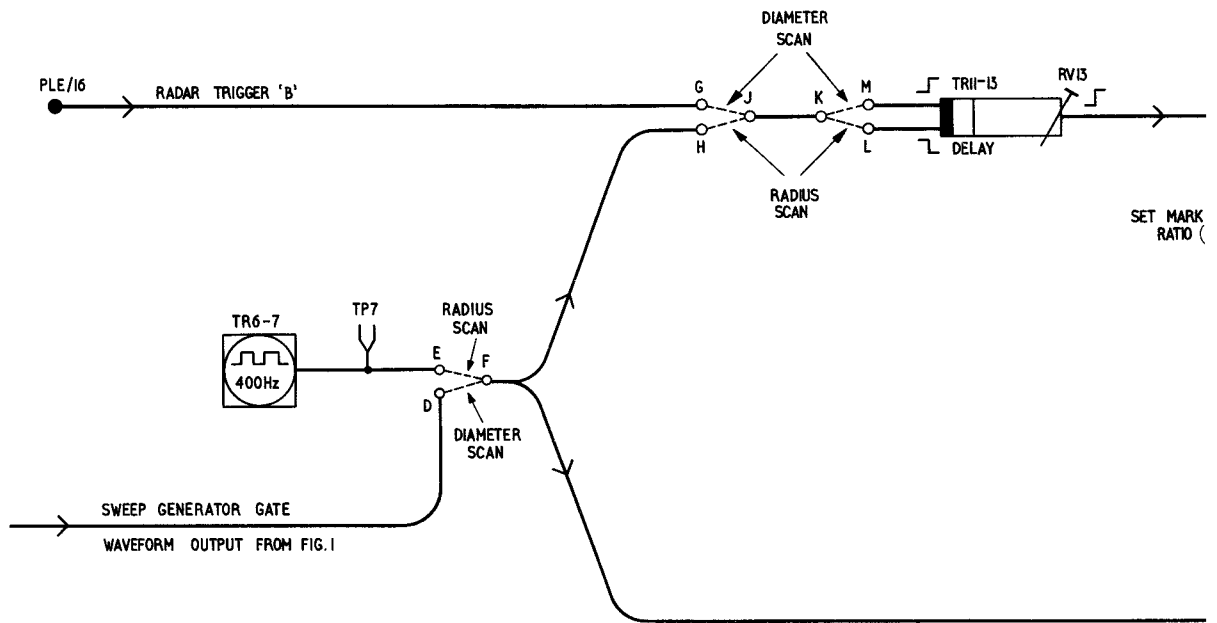
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Switch and gate waveform generator: functional diagram

Fig. 1



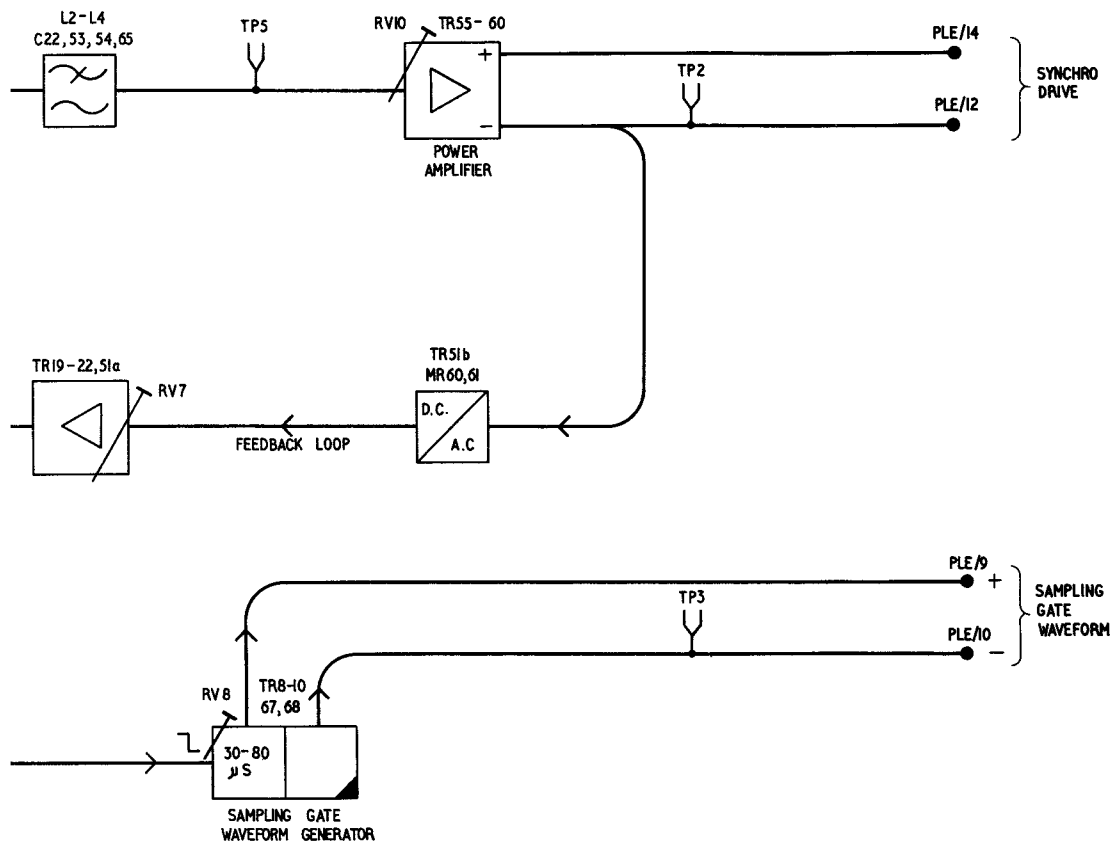




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ISSUE 5

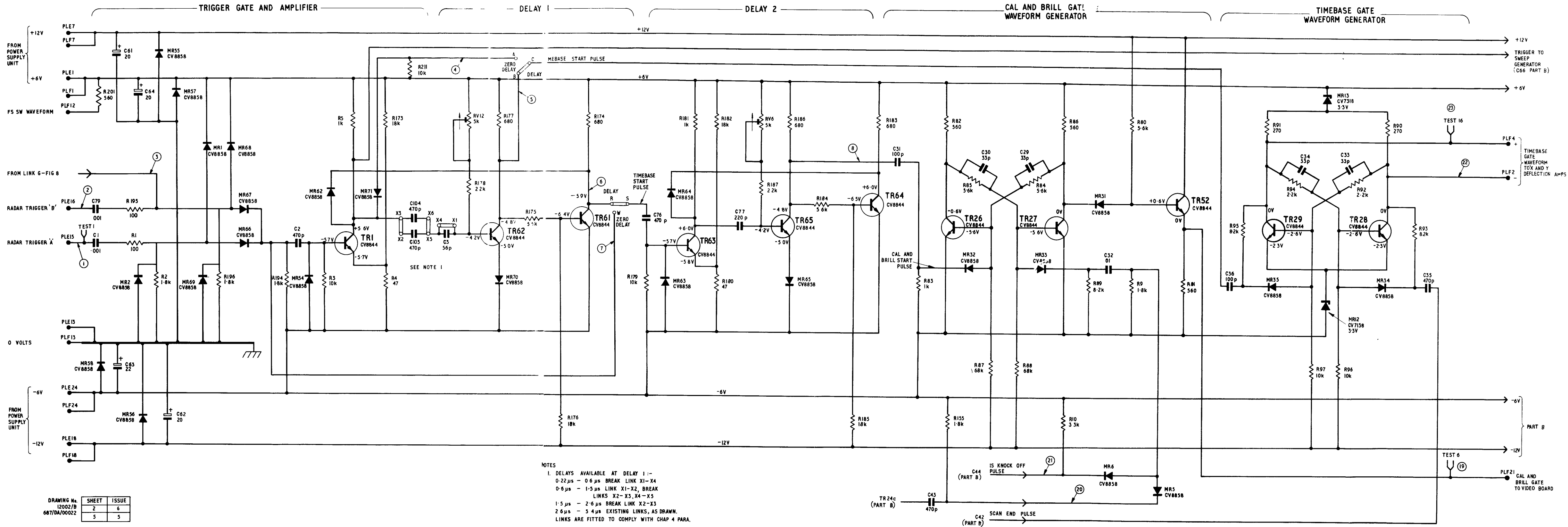
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Aerial synchro suppl



functional diagram

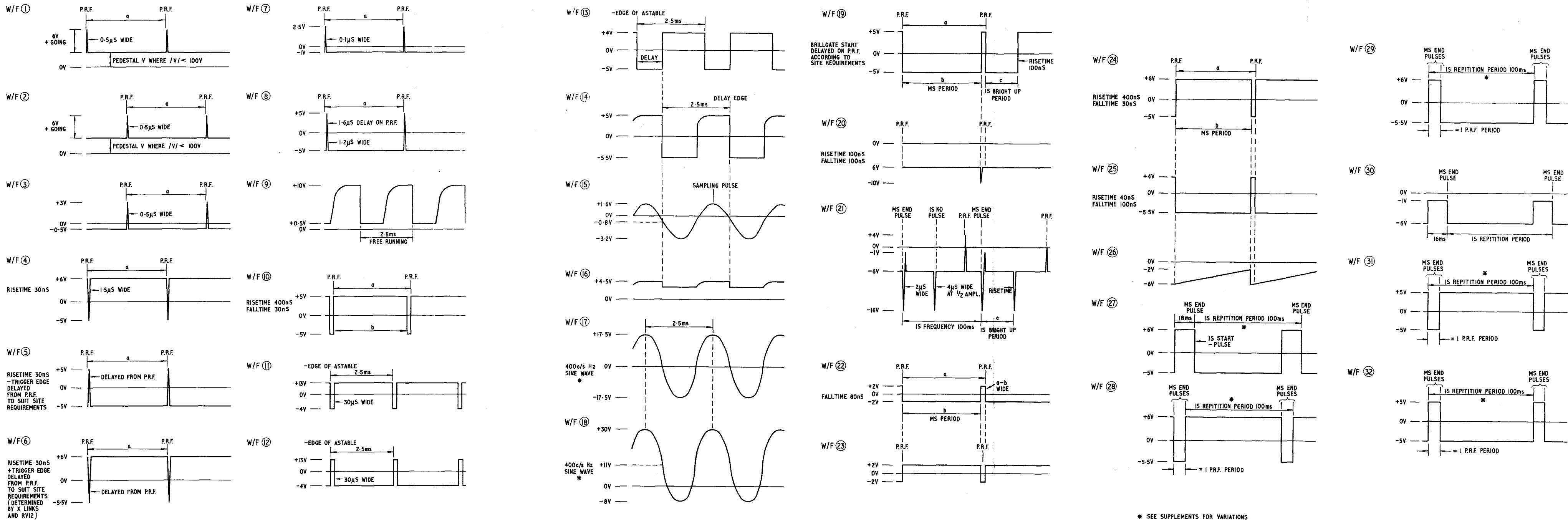
Fig. 3

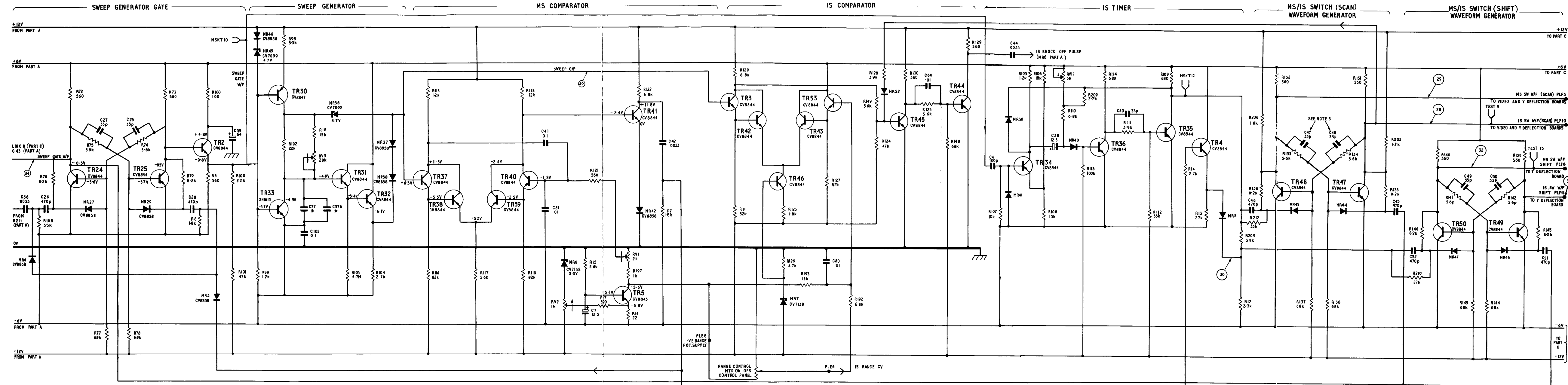


NOTES
 1. DELAYS AVAILABLE AT DELAY 1 :-
 0.22 μ s - 0.6 μ s BREAK LINK X1-X4
 0.6 μ s - 1.5 μ s LINK X1-X2, BREAK LINKS X2-X3, X4-X5
 1.5 μ s - 2.6 μ s BREAK LINK X2-X3
 2.6 μ s - 5.4 μ s EXISTING LINKS, AS DRAWN. LINKS ARE FITTED TO COMPLY WITH CHAP 4 PARA.
 2. ENCIRCLED NUMBERS REFER TO WAVEFORMS (SEE FIG)

DRAWING No.	SHEET	ISSUE
12002/B	2	6
687/DA/00022	5	5

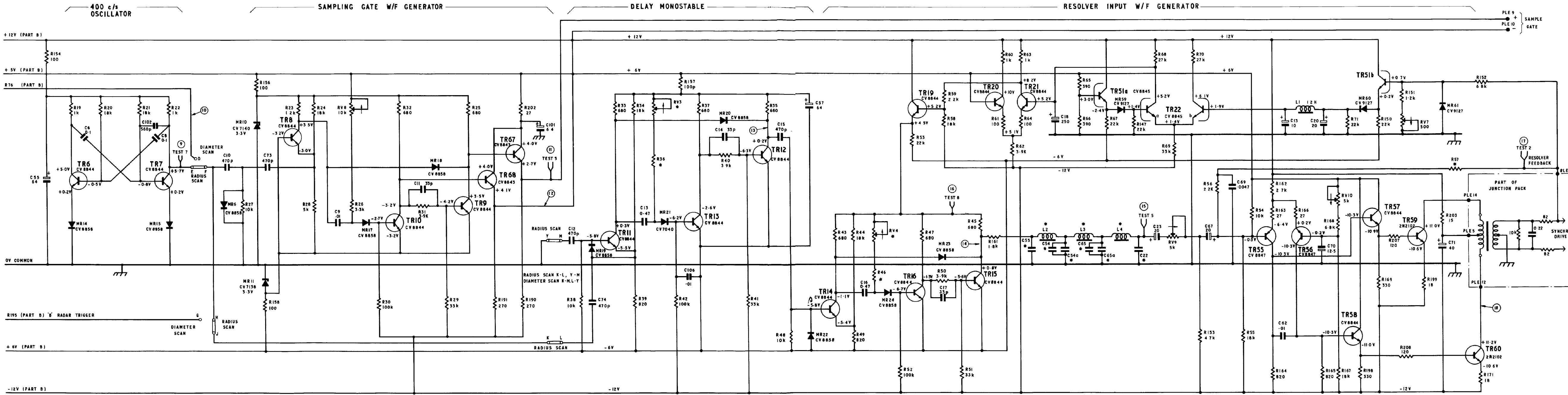
Timing board MJEZ (12002) : circuit - (Part A)





- NOTES
- ENCIRCLED NUMBERS REFER TO WAVEFORMS (SEE FIG 5)
 - FOR DETAILS OF COMPONENTS MARKED THIS * SEE SPECIAL TO VARIANT COMPONENTS LISTS
 - CAPACITORS C47 AND C48 REMOVED BY MOD A.2365 (MOD STRIKE 5).

DRAWING No.	SHEET	ISSUE
12002/B 6877/DA/00022	5	5
	6	4
	7	4



NOTES - 1 ENCIRCLED NUMBERS REFER TO WAVEFORMS (SEE FIG)
 2 FOR DETAILS OF COMPONENTS MARKED THUS * SEE SPECIAL TO VARIANT COMPONENT LISTS

DRAWING No	SHEET	ISSUE
12002 / B 667/DA/00022	3	9
	4	7
	5	5

Timing board MJEZ (12002) : circuit - (Part C)

Appendix 1

TIMING BOARD MJEC (12025A)
5840-99-956-5098

Mod. Strike-off No. 2

The timing board MJEC is a variant of the basic timing board MJEC (12002) with component values to give a mainscan gate length corresponding to a maximum range of 240 nautical miles.

SPECIFIC COMPONENTS LIST

Component	Value
R36	1.5kohm
R46	2.7kohm
R57	12kohm
RV3, RV4	5kohm
C22	0.1 μ F
C37	0.25 μ F
C37A	0.02 μ F
C53	0.1 μ F
C54, C54A	0.1 μ F
C65, C65A	0.1 μ F
L2-L4	Type 'A' coil (Decca B/DDL/7370/AE)

Appendix 2

TIMING BOARD MJEG (12137)
5840-99-953-5056

Mod. Strike-off No. 3

The timing board MJEG is a variant of the basic timing board MJEZ (12002) with component values to give a mainscan gate length corresponding to a maximum range of 75 nautical miles.

SPECIFIC COMPONENTS LIST

Component	Value
R36	1.5kohm
R46	2.7kohm
R57	12kohm
RV3, RV4	5kohm
C22	0.1 μ F
C37	0.085 μ F
C53	0.1 μ F
C54, C54A	0.1 μ F
C65, C65A	0.1 μ F
L2-L4	Type 'A' coil (Decca B/DDDL/7370/AE)

Appendix 3

TIMING BOARD MJEJ (12198)
5840-99-955-3597

Mod. Strike-off No. 4

The timing board MJEJ is a variant of the basic timing board MJEZ (12002) with component values to give a mainscan gate length corresponding to a maximum range of 100 nautical miles.

SPECIFIC COMPONENTS LIST

Component	Value
R36	1.5kohm
R46	2.7kohm
R57	12kohm
RV3, RV4	5kohm
C22	0.1 μ F
C37	0.115 μ F
C53, C54	0.1 μ F
C65, C65A	0.1 μ F
L2-L4	Type 'A' coil (Decca B/DDDL/7370/AE)

Appendix 4

TIMING BOARD MJEL (12462)

The timing board MJEL is a variant of the basic timing board MJEZ (12002) with component values to give a mainscan gate length corresponding to a maximum range of 300 miles*.

(*NATO mile = 2000yd).

SPECIFIC COMPONENTS LIST

Component	Value
R36	1.5kohm
R46	2.7kohm
R57	12kohm
RV3, RV4	5kohm
C22	0.1 μ F
C37	0.25 μ F
C37A	0.09 μ F
C53	0.1 μ F
C54, C54A	0.1 μ F
C65, C65A	0.1 μ F
L2 - L4	Type 'A' coil (Decca B/DDDL/7370/AE)

Chapter 2

DEFLECTION BOARDS (MRG AND MRH SERIES)

LIST OF CONTENTS

	Para.
General	1
OUTLINE OF OPERATION	4
Demodulation of aerial resolver outputs	6
IS scan control voltage	13
Composite scan control voltage	15
Timebase generation	16
Switch shift control voltage generation	21
Deflection drive waveform generation	24
Symbol generation	27
CIRCUIT DESCRIPTION	
Demodulation of aerial resolver outputs	28
IS scan control voltage	37
Composite scan control voltage	38
Timebase generation	39
Switch shift control voltage generation	47
Deflection drive waveform generation	51
Protection against supply failure	57

LIST OF ILLUSTRATIONS

	Fig.
Deflection board MRGZ (12003): functional diagram	1
Deflection board MRGZ (12003): component location	2
Deflection board MRGZ (12003): waveforms	3
Deflection board MRGZ (12003): waveforms (variations for HRI applications)	4
Deflection board MRGZ (12003): circuit (Part A)	5
Deflection board MRGZ (12003): circuit (Part B)	6
Deflection board MRGZ (12003): circuit (Part C)	7

LIST OF APPENDICES

	App.
Deflection board MRGX 	1
Deflection board MRHG 	2
Deflection board MRGE 	3
Deflection board MRGL 	4
Deflection board MRGC 	5
Deflection board MRGR 	6

General

1. The board variants in the MRG and MRH families carry deflection circuits for all types of Mk.5 display (X and Y for p.p.i. s. and X only for h.r.i. s.). All the variant in these series are based on the MRGZ board and differ only in the scaling of the expansion circuits. Details of variants in Service use are given in appendices to this chapter.

2. The board generates a pair of opposed composite deflection waveforms suitable for application to a pair of complementary current-converter amplifiers forming part of the deflection coil drive amplifier assembly. This pair of waveforms, together with a second pair of opposed waveforms generated within a second deflection board and feeding the remaining current-converter amplifiers in the amplifier board, control spot velocity and position on the screen at all times.

3. The term 'all types' in para.1 embraces not only the different types of radar picture displayed, but also the two types of system techniques which may be employed. Thus the board may be tailored to suit a 'fastscan' (FS) or 'interscan' (IS) system displaying either a radius-scan p.p.i. a diameter-scan p.p.i. or an h.r.i. In the following description the action of the circuits are described for all these uses, the term 'IS/FS' will be used to denote periods and functions other than mainscan (MS) periods and functions.

OUTLINE OF OPERATION

4. The following outline should be read in close conjunction with the functional diagram (fig. 1) and the waveforms (figs. 3 and 4).

5. In its 'X' role the board mates with viewing unit edge-connector sockets C and D, and in its 'Y' role with sockets H and G. Since the connecting pins on the board take the letter of the socket with which they mate, these pins are annotated on the functional diagram (fig. 1) and circuits (fig. 5, 6 and 7) with both of the possible appropriate letters.

Demodulation of aerial resolver outputs

6. The board receives as inputs on pins C/G2 and C/G3 a pair of

opposed and balanced sinewaves derived from the aerial resolver and, depending on the role of the board, modulated according to either the sine or cosine of the aerial's bearing (X and Y roles respectively in p.p.i. operation) or the sine of the aerial's elevation (Y role in h.r.i. operation).

7. To produce a single sinewave suitable for demodulation from the opposed pair, and to cancel completely any noise which may be induced between the resolver and this board, one sinewave is inverted and added to the other. The inversion is performed by the operational amplifier (o.a.) TR1-2 and the summation at the input of the demodulator circuit TR3-16, with both sinewaves accorded equal gain factors (0.1) through their respective paths.

8. The demodulator circuit TR3-16 comprises a shifting integrator controlled by an opposed pair of sampling gate waveforms, which consists of relatively narrow pulses coincident with the peaks of the resolver outputs, so that demodulation is phase sensitive. Thus the peaks of the combined sinewave are sampled by the gate pulses and the sampled levels are stored between pulses. Two further inputs may be applied to the demodulator dependent upon the type of display; a rate prediction voltage (C/G 12) which is applied as a scan control input to cause the demodulator output to vary in the time between sampling pulses and/or a vernier control voltage (C/G 11) which is applied as an auxiliary shift input. Both these auxiliary inputs are accorded very little gain.

9. Rate prediction is employed in radius-scan p.p.i. systems and in h.r.i. systems to cause the demodulator output to move between sampling pulses towards a level corresponding to the output level at the next sampling instant. In the radius-scan p.p.i. system, this prediction voltage is derived from the output of the demodulator in the other deflection board; in Y boards it is fed direct to the scan input but in X boards via the inverter (operational amplifier) TR45-46 to the scan input. When the board is employed in h.r.i. systems in the Y deflection role, the rate prediction input is derived from the positive and negative 6V supplies, the polarity being switched according to whether the aerial is sweeping up or down. Thus in both of these types of system the demodulator output consists of a d.c. level changing smoothly and slowly with the aerial rotation or nutation.

10. In the diameter-scan p.p.i. rate prediction is unnecessary since the resolver drive and sampling pulses are synchronised with the radar trigger, and the rate prediction input is consequently earthed. In this type of display the output of the demodulator reverses polarity every display period to

generate alternate scans spaced 180 deg. apart.

11. The vernier correction input (para. 8) is used in h. r. i. displays for certain vernier correction procedures and is derived from an operator's control. When the CHECK VERNIER switch on the operation control panel is operated the height control voltage is replaced by earth level, setting the height line to zero height. The vernier correction input from the VERNIER potentiometer on the operator's control panel can then be adjusted to align the zero degree angle with the height line.

12. The output of the demodulator circuit is used to control the generation of the MS scan deflection waveform; it is therefore referred to as the 'MS scan control voltage' and fed to the scan control input of a timebase circuit in MS periods.

IS scan control voltage

13. The IS scan control voltage, fed to the board on C/G4, comprises either a d. c. level (p. p. i. systems) or a linear voltage sweep (h. r. i. systems). In p. p. i. systems the control voltage is derived from a sine/cosine potentiometer and determines the X or Y component of scan for the bearing and range line. In h. r. i. systems the control voltage determines the downward curvature of the height line, representing the earth's curvature; the voltage is obtained from the timebase generator on the X deflection board, and is fed through the rotor inverter circuit on the Y deflection board before passing to the operational amplifier TR17-18 (para. 14). In FS systems the scan control voltage input is earthed, since the FS scanning circuits are not located on this board.

14. The IS scan control voltage is fed to the inverting operational amplifier TR17-18 the gain factor of which is preset according to whether the system is p. p. i. or h. r. i. The output of the amplifier is applied to the timebase circuit in IS periods.

Composite scan control voltage

15. The selection of the MS and IS scan control voltages (for application to the timebase circuit) in their appropriate periods is accomplished by a two element electronic switch (TR19-23) operated by a pair of opposed switch waveforms, one an MS switch waveform and the other an IS switch waveform.

Timebase generation

16. Timebase generation is accomplished by the shifting-integrator circuit TR24-39. The composite scan control voltage is applied to the scan input, either earth (p. p. i.) or -6V (h. r. i.) is applied to the shift

input, and an opposed pair of gate waveforms (the '+ve' and '-ve' timebase gate waveforms') control the selection between shift and scan modes. The scan mode obtains during the whole of both MS and IS scan regimes while the shift mode obtains in the intervals between (i. e. in MS and IS shift regimes, fig. 3).

17. Thus in shift regimes the timebase circuit output is steady at earth level (p.p.i.) or at a level determined by the -6V shift input (h.r.i.), and in scan regimes the output is a voltage which starts at the level reached in the previous shift regime and moves in a direction and at a rate dependent upon the polarity and magnitude of the scan input.

18. In p.p.i. systems the output in scan regimes varies linearly to provide constant-velocity, straight-line mainscaans and interscaans. In h.r.i. systems while the output in MS regimes is also linear, the output in IS regimes is hyperbolic to provide the slight downward curvature on the height line: this hyperbolic curve is produced by applying a linear voltage sweep (sawtooth function) to the scan input (see para. 13).

19. A potential of -6V is applied as shift input to the timebase circuits in h.r.i. applications since in this type of display it is necessary to off-centre the trace origin to the lower left of the c.r.t. to make the most efficient use of the total screen area.

20. The output from the timebase circuit is the 'scan-waveform' and is applied to the summing operation amplifier TR54-57.

Switched shift control voltage generation

21. MS and IS/FS shift potentials are applied to an electronic switch (TR49-53 TR65-66) which selects them in their appropriate periods for feeding to summing operational amplifier TR54-57 where they are added to the composite scan waveform produced by the timebase circuit. The output of the switch is the 'switched shift control voltage'.

22. The IS and FS shift control voltages (derived from operator's controls via C/G5 or C/G17) are inverted by the unity gain operational amplifiers TR47-48 and TR70, TR67 respectively before being applied to the switch. Zero level is used as the MS shift control and this is applied directly to the switch.

23. In practice the electronic switch has three 'ways', but for any given application of the board only two ways are used, the MS way and either the IS or FS way. The operative ways are controlled by the opposed 'MS' and

'IS/FS switch waveforms'. When a centred IS condition is required (a condition where the interscan origin coincides with the mainscan origin) these switch waveforms are d. c. levels such that the MS way is held 'on' and the IS way is held 'off'.

Deflection drive waveform generation

24. The output circuit of the board comprises two operational amplifiers (o. a.'s) connected in tandem, the first (TR54-57) being a summing o. a. with four preset switchable gain factors (to give the four range scales required by the display) and the second (TR60-63) being an inverting o. a. with a unity gain factor. The first o. a. output, in addition to providing the input to the second o. a., also constitutes the 'A' output deflection drive waveform, while the second o. a. output constitutes the 'B' deflection drive waveform. It will be seen therefore that the 'A' and 'B' outputs are opposed, the 'B' output being an inverted version of the 'A' output.

25. Four inputs are applied to the first amplifier; the scan waveform, the switched shift control voltage, the centre shift voltage and the picture shift voltage. The centre shift voltage is derived from the X CENTRE control (PLD22) or the Y CENTRE control (PLH22); both of these controls are located on the viewing unit control panel. The picture shift voltage (PLG/C8) is one of two levels, the selection being made by the RADAR SHIFT push-button switch on the operator's control panel. When the RADAR SHIFT switch is not operated the picture shift voltage is at earth potential, and centred conditions are provided as required by a p. p. i. display. When the RADAR SHIFT switch is operated the picture shift voltage is obtained from the SHIFT potentiometer control on the operator's control panel; these conditions are selected when the off-centre mode of operation is required.

26. The opposed deflection drive waveforms, fed out of the board on D/H20 and D/H17, are routed to the deflection coil drive amplifier assembly for conversion into current waveforms suitable for driving the c. r. t. deflection coils.

Symbol generation

27. The generation of the basic X and Y waveforms used finally to scan the required shape of symbol on the c. r. t. is accomplished externally to this board. The board does contain, however, a phase-splitting circuit used to generate a pair of opposed waveforms from one or other of the basic waveforms. The basic waveform is applied via C/G6, split by the circuit TR64 and the opposed outputs (the 'A' and 'B' symbol outputs) are fed from the board via D/H21 and D/H19 respectively. These outputs are fed to the deflection coil drive amplifier assembly, where they are added to the deflection drive waveforms outputs (para. 24).

CIRCUIT DESCRIPTION (Figs. 5, 6, 7)

Demodulation of aerial resolver outputs (Fig. 5)

28. A pair of opposed resolver waveforms are fed to the summing shift inputs of the aerial demodulation shifting integrator, one directly and the other via inverting o.a. TR1-2, with equal gain accorded to each so that the noise component is cancelled (see para. 6-8).

29. Operational amplifier TR1-2 comprises a double-transistor differential amplifier TR1 feeding a common-emitter output stage TR2 with R1 and R6 acting as input and feedback resistors respectively; earth level is used as reference input to the differential amplifier. MR1-2 limit the voltage excursion at the amplifier centre-point to within $\pm 0.3V$ of earth level. Preset RV1 is used in conjunction with the test switch SA to balance the amplifier, i.e. to obtain a zero-out for zero-in condition. To ensure stability the circuit C1, R7 provides top-cut and C41 reduces the gain of the amplifier greatly at frequencies well above the normal input frequency. Zener diode MR3 both provides d.c. stabilisation for TR2 and a low-impedance to a.c. in the emitter circuit, enabling this stage to have a high gain factor.

30. The demodulator circuit comprises the shifting integrator TR3-16, which has three main summing shift input points and a single scan input point.

31. R9 and R10 form the input resistors for the two resolver outputs, and R181-182, R80 form an attenuator and input impedance for the vernier correction voltage input. RV4 and R27 form the feedback resistor for the circuit in its 'shift' condition and C4 forms the feedback capacitor for the circuit in its 'scan' condition. The non-inverting amplifier is formed by TR3-6 and TR9-10, the 'switch' by TR7-8, and the inverting amplifier by TR11-16.

32. In the non-inverting amplifier, TR3 is a differential amplifier with earth level as reference input to TR3b base. The inverted output from TR3a collector is passed through the emitter follower TR4, inverted by the common-emitter stage TR5 and then fed via emitter follower TR6 and the electronic switch TR7-8 to the complementary pair of emitter followers TR9-10.

33. MR4-5 limit the voltage excursion at the shift-mode centre-point to within $\pm 0.3V$ with respect to earth. Preset potentiometer RV2 enables the amplifier to be balanced until the amplifier gives zero output when the

input is zero.

34. To ensure that, during scan modes, the non-inverting amplifier is not driven into a state from which it cannot rapidly recover the negative sampling gate waveform is applied to the common emitters of TR3 via MR6, causing them to be driven to +2V which is sufficient to cut off both sections.

35. In the inverting amplifier TR 1 is a differential amplifier with the reference input (earth level) to TR11b base. The non-inverted output from TR11b collector is taken through the emitter follower TR12, inverted by the common emitter amplifier TR13 and fed via emitter follower TR14 to the complementary pair of emitter followers TR15-16.

36. Preset potentiometer RV6 enables the amplifier to be balanced until the amplifier gives zero output when the input is zero. Stability is ensured by two CR top-cut networks which reduce the high frequency gain; these are C5 and R33 shunting TR11b collector load, and C6 and R37 shunting TR13 collector load.

IS scan control voltage (Fig. 5)

37. The interscan scan control voltage fed to the board on C/G4 is applied to o. a. TR17-18, which is almost identical to o. a. TR1-2 previously described (para. 29). RV20 R48 form the input resistance; network R168-169 R210 applies a '+' d. c. input in h. r. i. application so that the linear sweep (para. 13) at this point starts at 0V. Setting-up facilities identical to those for o. a. TR1-2 are provided. In FS systems, earth level is fed as input to this amplifier since the symbol waveforms are generated outside this board. In h. r. i. applications, relay RLD is energized from the CHECK VERNIER switch on the operator's control panel and earths the input to the amplifier to remove the curvature from the displayed height line.

Composite scan control voltage (Fig. 4)

38. Selection of MS and IS/FS scan control voltages in their appropriate periods is accomplished by the single-pole, two-way electronic switch formed by TR19-23 MR14-15. Waveforms fed as control inputs to the two 'ways' of the switch are the opposed MS and IS/FS switch waveforms, which alternate between levels of +5V. The diode pairs MR14 and MR15 are alternately switched on and off by the applied switch waveforms. The 'off' pair inhibit the scan control input, while the 'on' pair produce an output load current proportional to the difference between the input current and the constant current stages TR20 or TR21 and TR22. The composite scan control waveform as produced by the circuit is applied to the scan control input of t

Timebase generation (Fig. 7)

39. The timebase generator circuit comprises TR24-39 acting as shifting integrator. The voltage applied to the shift input resistor R60 consists of either earth level or -6V (para.16), and the feedback impedance by parallel connected R68 and C11. The scan input impedance, fed with the composite scan control voltage, consists of preset RV8 and R59; C10 forms the feedback capacitor. TR24-27 TR30-31 form the non-inverting amplifier, TR32-39 the inverting amplifier, and TR28-29 the switch between the two. The switch is controlled by the opposed '+' and '-' timebase gate waveforms which alternate between levels of $\pm 2V$ (see fig. 3).

40. In the non-inverting amplifier, TR24 is a differential amplifier. The inverted output from TR24a collector is fed through the emitter follower TR25, inverted by the common-emitter amplifier TR26 and then taken via the emitter follower TR27 and the electronic switch TR28-29 to the complementary pairs of emitter followers TR30-31.

41. Diodes MR17-18 limit the voltage excursion at TR24a base to $\pm 0.3V$ with respect to earth. Preset potentiometer RV9 provides a fine adjustment at the shift control input which determines the d. c. level at the output of TR38/TR39, thus fixing the d. c. starting point of the scan waveform output from TR38-39.

42. To ensure that, during scan modes, the non-inverting amplifier is not driven into a state from which it cannot recover rapidly, the positive timebase gate waveform is applied to the common emitters of TR24 via MR 19, causing them to be driven to +2V which is sufficient to cut off both sections.

43. The first stage of the inverting amplifier comprises a differential amplifier TR32 with negative feedback applied separately to its two emitters, via separate common emitter inverter stages (TR33-34), from its two collectors. This arrangement compensates for changes of circuit parameters with temperature.

44. The inverted output from the emitter of TR33 is emitter-followed by TR35, and applied via R90 to the emitter of the common-base stage TR36. The output from TR36 collector is fed via the emitter-follower TR37 to the final stage comprising the complementary emitter followers TR38-39.

45. The output waveform therefore comprises MS and IS/FS scans in their appropriate regimes added to a constant level corresponding to the 'basic' picture shift voltage, the scanning peaks being $\pm 4V$. This output is fed to one of the summing inputs of o. a. TR54-57.

46. Switch SH enables earth level to be fed to the scan input for setting up purposes (so that RV10 may be preset to obtain a stationary output with zero scan input).

Switched shift control voltage generation (Fig. 6)

47. IS and FS shift control voltages are brought into the board on C/G5 and C/G17 respectively and passed via separate identical operational amplifiers (TR47-48 and TR67 TR70; each with gain factors of -0.6) to two ways of an electronic switch; a third way of this switch is fed with earth level which comprises the MS shift control voltage.

48. Operational amplifier TR47-48 comprises the double-transistor differential amplifier TR47 feeding a common-emitter stage TR48; R197 is the input resistor, R106 the feedback resistor and earth level is used as a reference input to TR47b base. The voltage excursion at the amplifier centre-point is limited to within $\pm 0.3V$ of earth level by diodes MR23-24. The preset control RV11 is used in conjunction with the test switch SD to balance the amplifier, i. e. to obtain a zero output for zero input condition. To ensure stability the circuit C12, R105 provides top-cut and C40 greatly reduces the amplifier gain at frequencies well above the normal input frequency. Zener diode MR45 provides d. c. stabilisation for TR48 and a low impedance to a. c. in the emitter circuit, enabling this stage to have a high gain factor.

49. The operational amplifier TR70, 67 is identical to the circuit TR47-48 described in para. 48.

50. The three 'ways' of the electronic switch are formed by TR52-53, TR50-51 and TR65-66, and the 'pole' by TR49. Only two ways are employed in any specific application of the board, depending on whether the system is fastscan or interscan. The opposed MS and IS/FS switch waveforms (shift), which alternate between the levels of $\pm 5V$, are fed as control inputs to the two ways employed. The operation of the circuit is identical to that described in para. 38. The switched shift control waveform produced by the circuit is applied to one of the four summing inputs of operational amplifier TR54-57.

Deflection drive waveform generation (Fig. 7)

51. Summing operational amplifier TR54-57 forms the first of the two output amplifiers; it adds at its input the switched shift control

voltages, the output of the timebase circuit, and the picture shift and centre control d. c. levels; its output is the 'A' deflection drive and the input to a second input operational amplifier (TR60-63).

52. Input impedances of TR54-57 are formed by R113, C15, R112a, RV17, R114 and R115. The feedback impedance is formed by R120 alone when the shortest range is selected, and by R120 in parallel with R119, R118 or R117 as the range is progressively lengthened; these connections are made by contacts on relays RLC, RLB and RLA, which are operated by the range switch on the operator's control panel.

53. The high-gain differential amplifier TR54 uses earth level as reference input against which the centre-point potential is compared. The non-inverted collector output is passed via emitter-follower TR55 and common-emitter stage TR56 to the output emitter-follower stage TR57. Switch SE is used with preset control RV13 to balance the amplifier. MR35-36 limit the voltage excursion at the centre-point to within $\pm 0.3V$ of earth. Circuits C51 R171 and C18 R135 provide top-cut and improve stability.

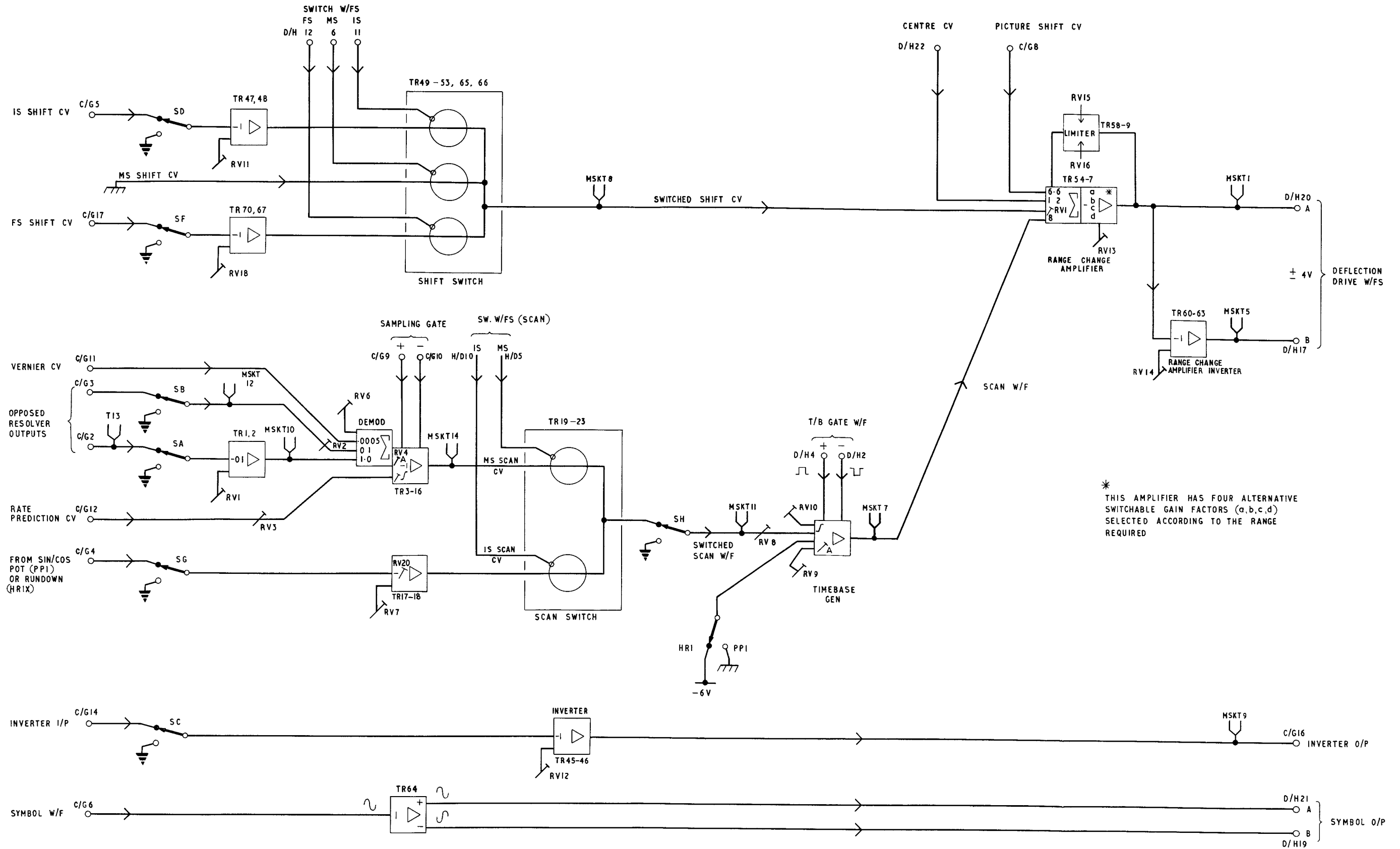
54. TR58-59, RV15-16, R121-126 and MR39-40 form a circuit which limits the amplifier output (and therefore the output of operational amplifier TR60-63) to within $\pm 4V$. The circuit effectively shunts the feedback network with a low impedance as the limiting levels are reached, thus greatly reducing the amplifier gain outside these levels. The transistors act as emitter-followers, with their bases connected to intermediate points of a potential divider network connected between $\pm 6V$ and 'centre-tapped' to the amplifier output. The slider potentials of RV15-16 determine the two base potentials which are adjusted to produce limiting levels of $+4V$ and $-4V$ at the amplifier output. The sense of connection of the two diodes which separately connect the emitters to the amplifier centre-point is such that they are back-biased when the amplifier is at zero.

55. With the amplifier working normally, the waveforms on the bases and emitters of TR58-59 are slightly attenuated versions of the amplifier output superimposed on the d. c. biases obtained from the potential divider network. As the output moves towards its limits, the reverse bias on one or other of the diodes MR39-40 diminishes until, when the limit is reached, one or other of the diodes commences to conduct, thus applying heavy negative feedback to the centre-point and quickly arresting the output excursion.

56. A second inverting operational amplifier comprising TR60-63 provides the 'B' deflection drive waveform. The input and output resistances, R137 and R148, are equal and the amplifier gain is unity. Earth level is used as the reference input to TR60b base. The non-inverted collection output from TR60 is fed by emitter-follower TR61 to the common-emitter amplifier TR62. This amplifier gives an output to the output emitter-follower TR63 which is an inverted version of the input. Diodes MR37-38 limit the voltage excursion at TR60 input to $\pm 0.3V$ with respect to earth. Top-cut is provided by the circuits C52, R170 and C22 R146, improving the stability of the amplifier.

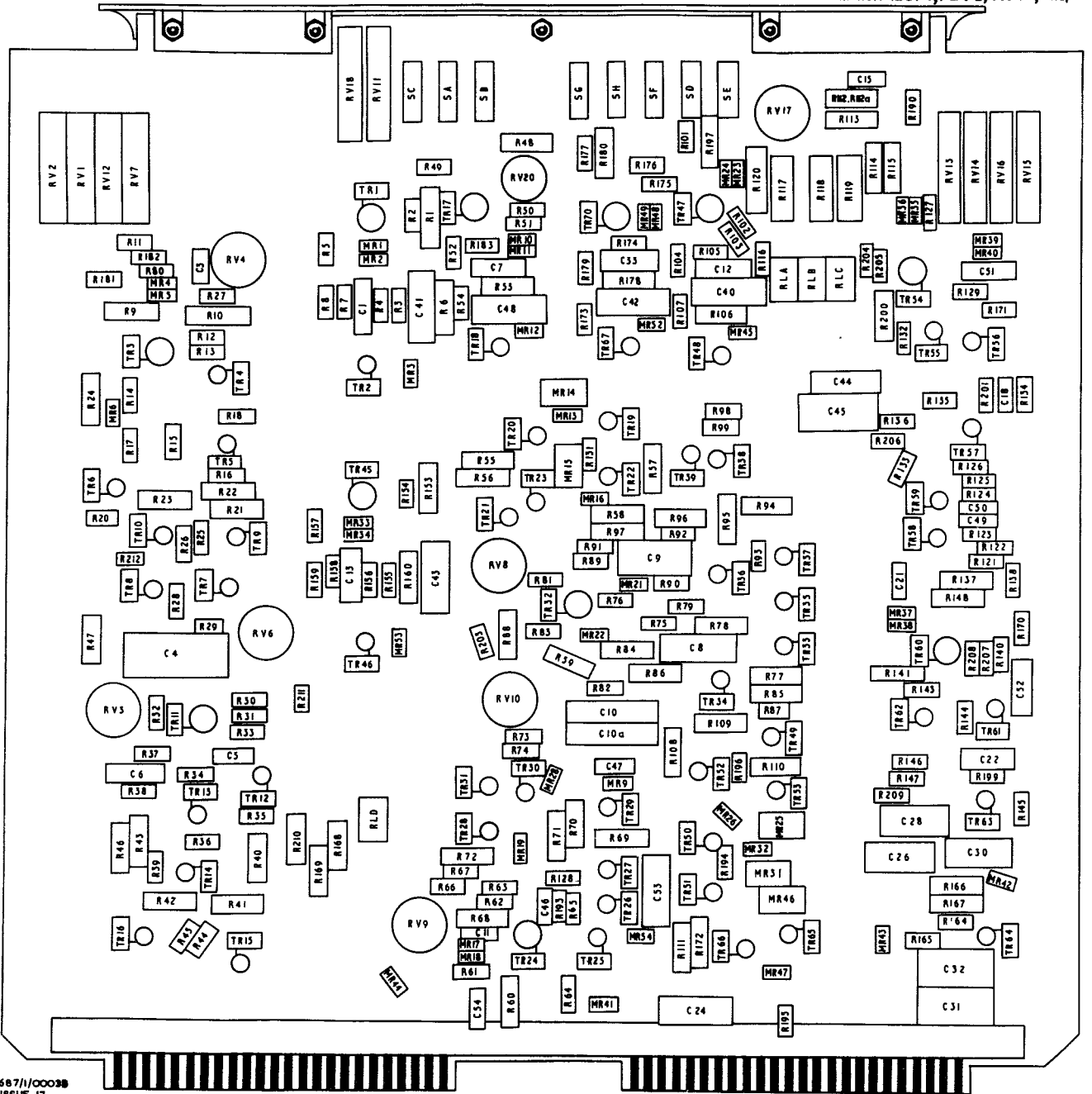
Protection against supply failure

57. The four d. c. lines supplying the 6V and 12V to the board are heavily interconnected through the board's circuits. MR41-44 are employed to protect the circuits from damage which would otherwise result if one of these supplies fails since, in their absence, that supply line would be driven into reverse polarity by the other supplies. In the normal condition all these diodes are back-biased but, should the +12V supply fail, the +12V line will be driven towards earth until it is arrested at +6V by the action of MR41. Similarly MR43 arrests the +6V line at earth, MR42 arrests the -12V at -6V, and MR44 arrests the -6V line at earth. C23-30 provide the usual decoupling of supply line transients to earth.



* THIS AMPLIFIER HAS FOUR ALTERNATIVE SWITCHABLE GAIN FACTORS (a,b,c,d) SELECTED ACCORDING TO THE RANGE REQUIRED

Deflection board MRGZ (12003) : functional diagram

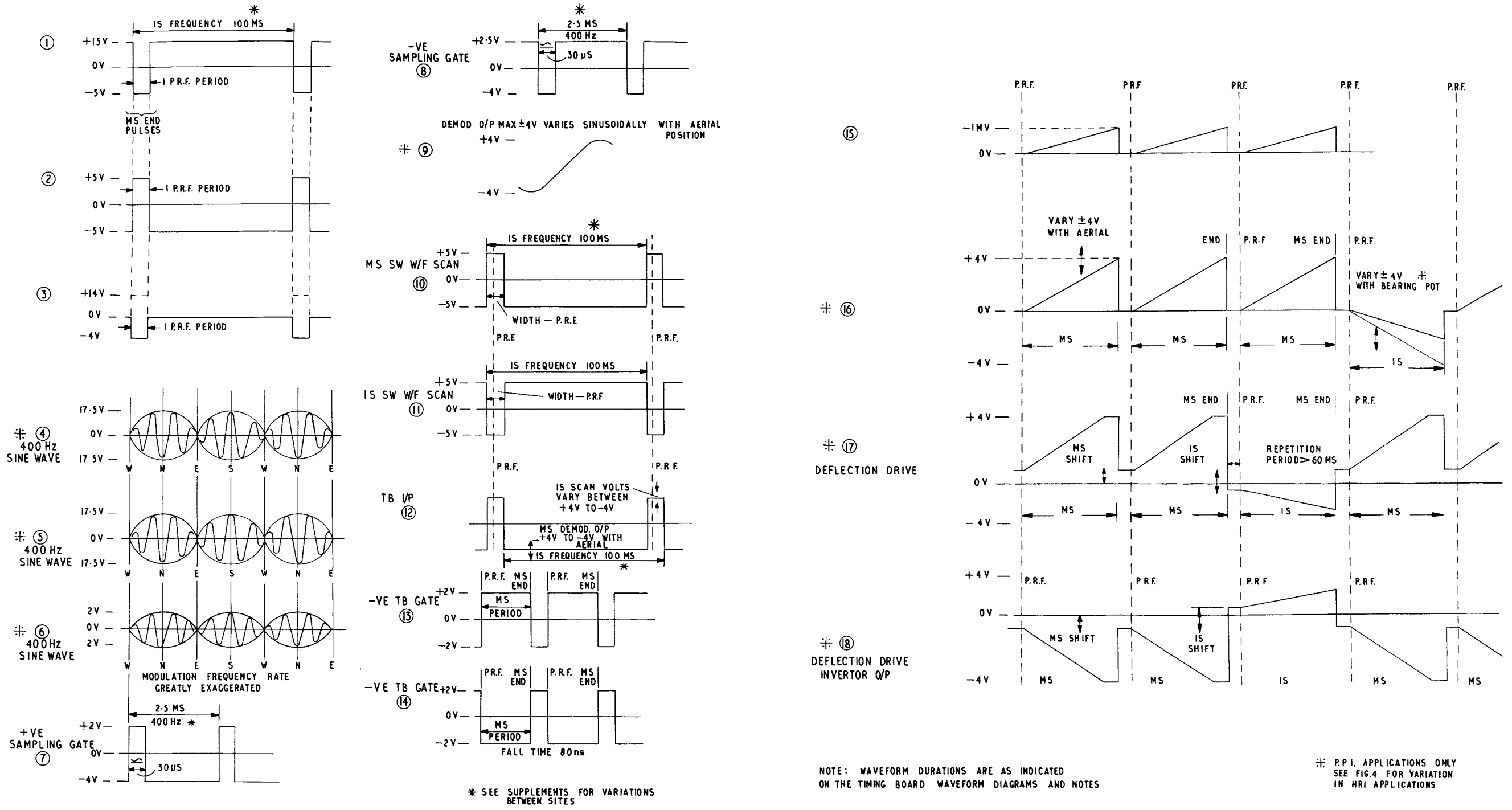


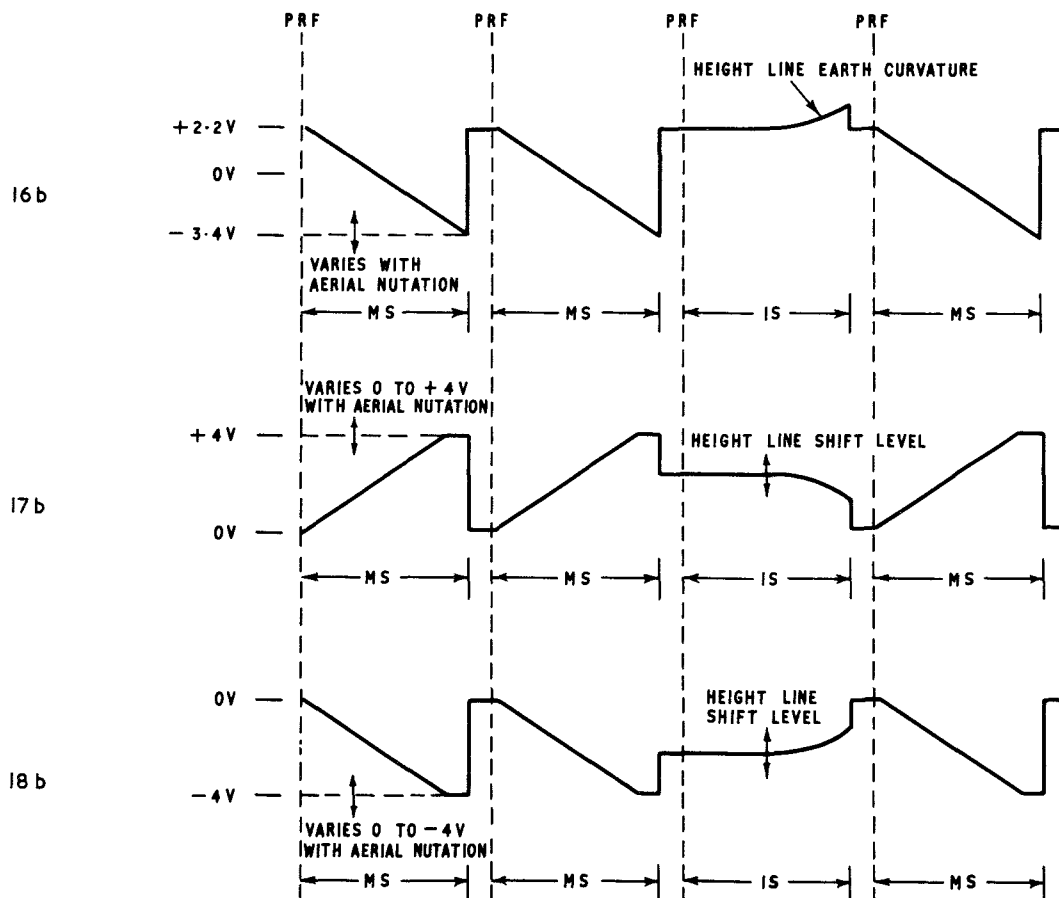
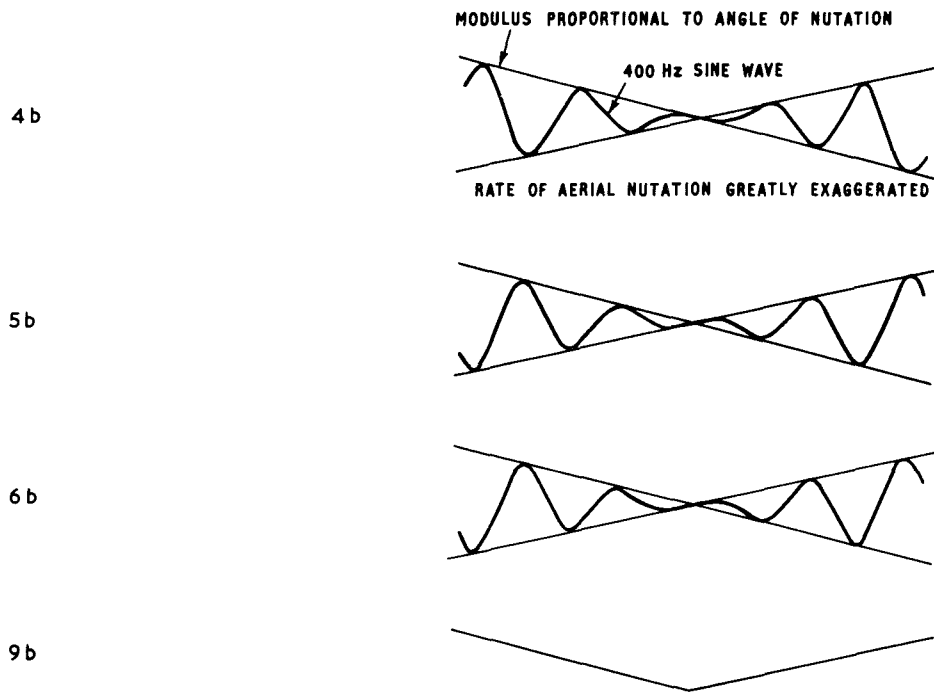
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ISSUE 17

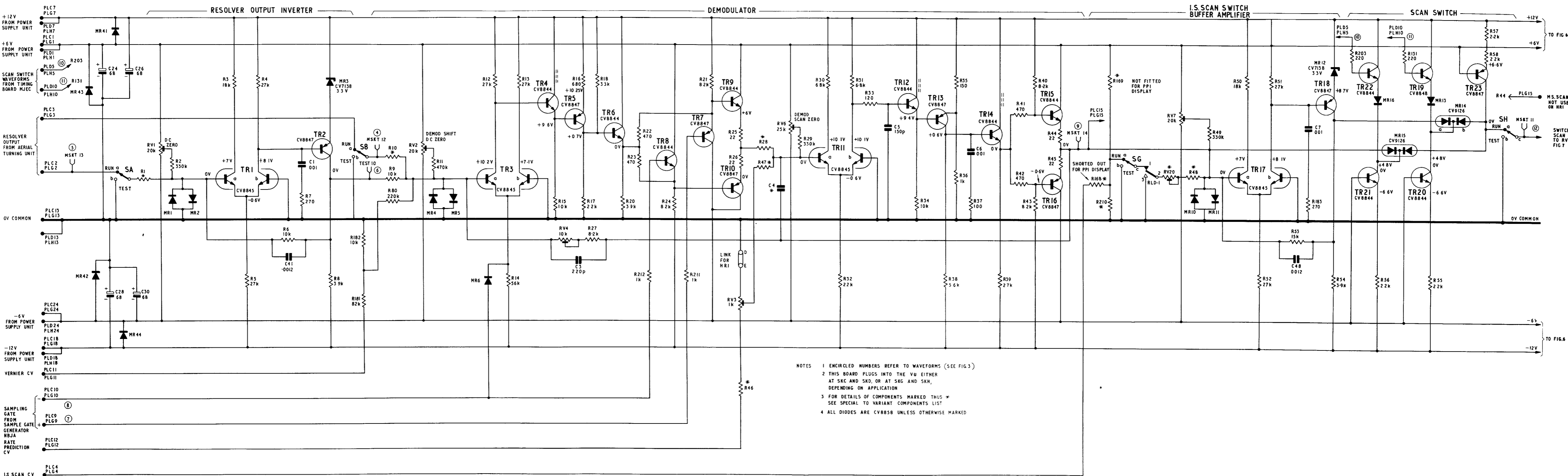
A.L.18, Aug. 70

Deflection board MRGZ (12003): component location

Fig. 2





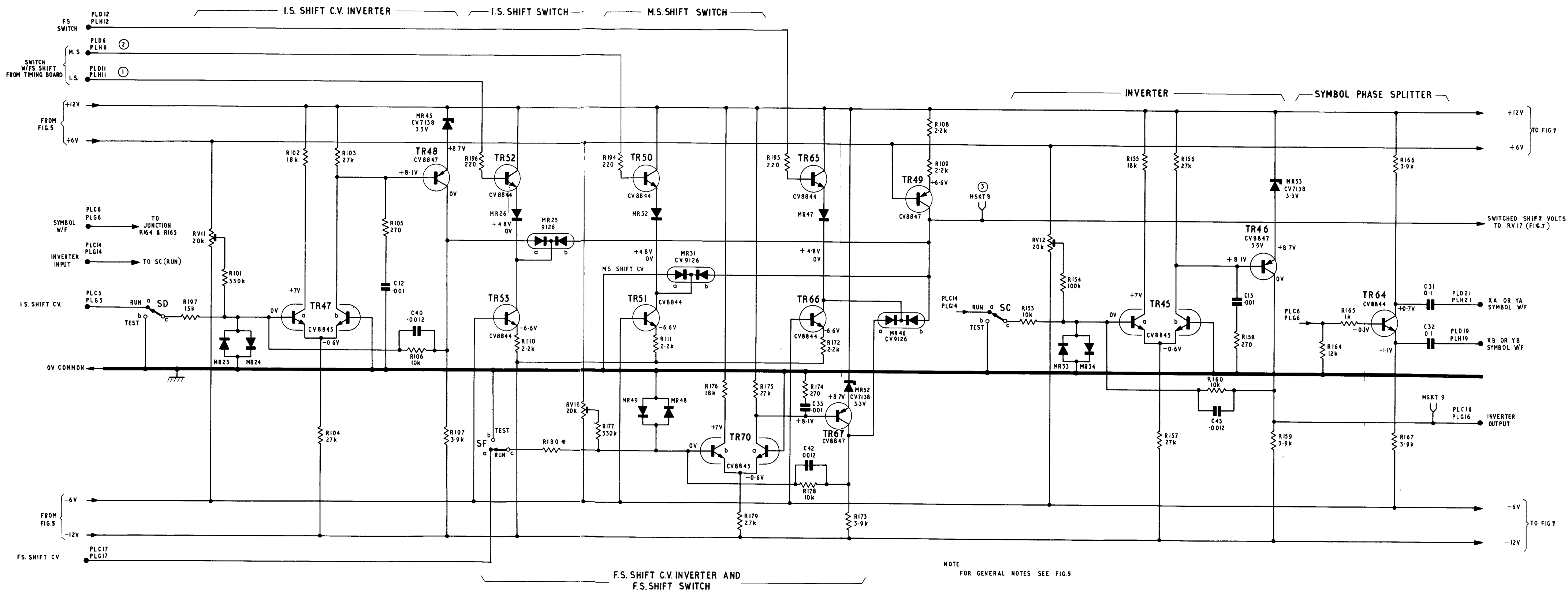


- NOTES
- 1 ENCIRCLED NUMBERS REFER TO WAVEFORMS (SEE FIG 3)
 - 2 THIS BOARD PLUGS INTO THE VU EITHER AT SKC AND SKD, OR AT SKG AND SKH, DEPENDING ON APPLICATION
 - 3 FOR DETAILS OF COMPONENTS MARKED WITH * SEE SPECIAL TO VARIANT COMPONENTS LIST
 - 4 ALL DIODES ARE CV8858 UNLESS OTHERWISE MARKED

Deflection board MRGZ (12003): circuit (Part A)

B/DDI/2003/B
687/DA/0003B

SHEET	3	4	5	6
ISSUE	4	7	5	6



NOTE
FOR GENERAL NOTES SEE FIG.5

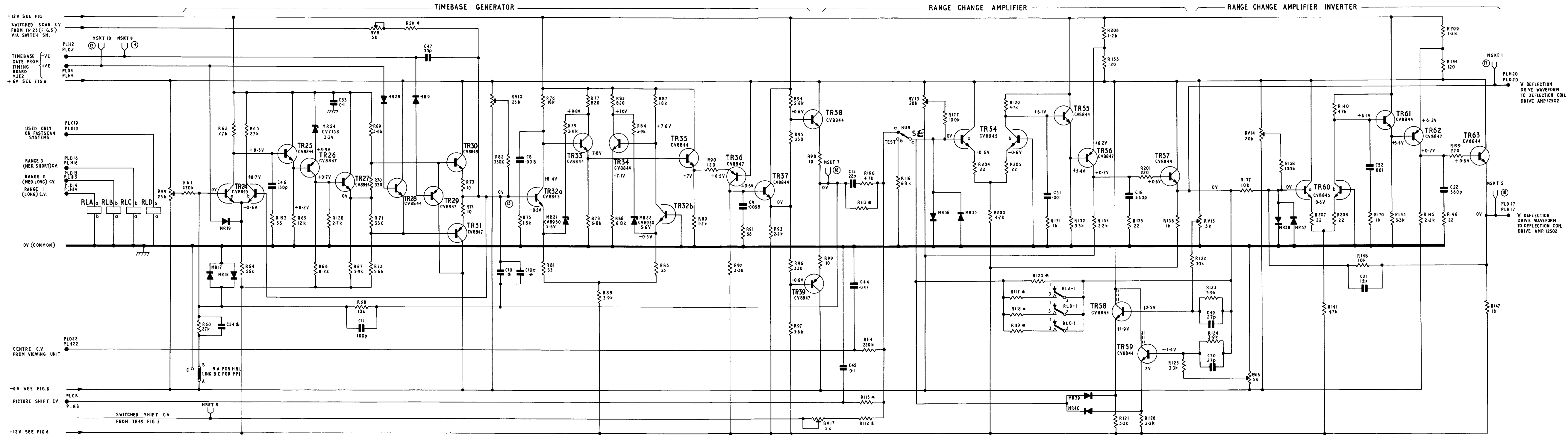
B/DDL/12003/B
687/DA/00038

SHEET	3	7	8
ISSUE	4	5	7

AL 19 Aug.70

Deflection board MRGZ (12003) : circuit (Part B)

Fig. 6



NOTE: FOR GENERAL NOTES SEE FIG. 5

B/DL/12003/B
687/DA/00038
SHEET 5 6 8
ISSUE 5 6 7
AL. 19, Aug. 70

Deflection board MRGZ (12003): circuit (Part C)

Fig. 7

APPENDIX 1

DEFLECTION BOARD MRGX

(687/00038/004)

5840-99-222-1046

(Incorporating modifications up to Mod. Strike-off No. 5)

1. The deflection board MRGX is a variant of the basic board MRGZ and is used to scale the height expansion in HRI displays for heights up to 128 000ft.

2. Other than the components fitted to give the correct expansion scale, this board also differs from the basic in that the rotor amplifier (TR45, 46) is used in this application (SJCC) to change the scaling of the height c.v. The circuit configuration of the rotor amplifier is unchanged but the values of R153 and R160 are changed to 22k ohms to give a different input impedance.

3. In addition R60 (in TR24a base circuit) is changed from 22k ohms to 27k ohms.

TABLE 1

SPECIFIC COMPONENTS LIST

Component	Value	Component	Value	Component	Value
R1	18k	R115	220k	RV20	10k
R10	18k	R117	-		
R28	1k	R118	-	C4	470n
R46	22k	R119	-	C10	20n
R47	68k	R120	10k	C10a	20n
R48	12k	R153	22k		
R59	3.9k	R160	22k		
R73	10	R168	3.9k		
R74	10	R169	8.2k		
R112	5.6k	R180	27k		
R113	12k	R210	470		

APPENDIX 2

DEFLECTION BOARD MRHG

(678/00038/012)

5840-99-223-0218

(Incorporating modifications up to Mod. Strike-off No. 7)

1. The deflection board MRHG is a variant of the basic board MRGZ and is used in HRI displays to provide a height scale up to 100 000ft. The circuit configuration is unchanged from the basic board and the specific components are only concerned with scaling to produce the correct vertical expansion.

TABLE 1

SPECIFIC COMPONENTS LIST

Component	Value	Component	Value	Component	Value
R1	18k*	R115	68k	C4	470n
R10	18k*	R117	-	C10	20n
R28	1k	R118	-	C10a	-
R46	22k	R119	-		
R47	68k	R120	10k		
R48	12k	R168	3.9k		
R59	9.1k	R169	8.2k		
R73	** 10	R180	100k		
R74	** 10	R210	470		
R112	5.6k				
R113	12k	RV20	5k		

* Tolerance $\pm 0.1\%$

**This value may be 47

APPENDIX 3

DEFLECTION BOARD MRGE

(687/00038/033)

5840-99-953-5055

(Incorporating modifications up to Mod. Strike-off No.4)

1. The deflection board MRGE is a variant of the basic board MRGZ and is used in p.p.i. displays to provide ranges of 7.5, 15, 30 and 75 nautical miles. The circuit configuration is unchanged from the basic board and the specific components fitted are only concerned with range scaling.

TABLE 1

SPECIFIC COMPONENTS LIST

Component	Value	Component	Value	Component	Value
R1	100k	R115	15k	C4	470n
R10	100k	R117	11.1k	C10	100n
R28	1k	R118	33.3k	C10a	-
R46	56k	R119	100k		
R47	10k	R120	100k		
R48	18k	R168	2.2k		
R59	6.8k	R169	-		
R73	10	R180	15k		
R74	10	R210	-		
R112	10k				
R113	15k	RV20	5k		

APPENDIX 4

DEFLECTION BOARD MRGL

(687/00038/039)

5840-99-955-3595

(Incorporating modifications up to Mod. Strike-off No.4)

1. The deflection board MRGL is a variant of the basic board MRGZ and is used in p.p.i. displays to provide ranges of 12.5, 25, 50 and 100 nautical miles. The circuit configuration is unchanged from the basic board and the specific components fitted are only concerned with range scaling.

TABLE 1

SPECIFIC COMPONENTS LIST

Component	Value	Component	Value	Component	Value
R1	100k	R115	15k	C4	470n
R10	100k	R117	14.3k	C10	150n
R28	1k	R118	33.3k	C10a	-
R46	56k	R119	100k		
R47	10k	R120	100k		
R48	18k	R168	2.2k		
R59	6.8k	R169	-		
R73	10	R180	15k		
R74	10	R210	-		
R112	10k				
R113	12k	RV20	5k		

APPENDIX 5

DEFLECTION BOARD MRGC
(687/00038/031)

5840-99-948-8645

(Incorporating modifications up to Mod. Strike-off No. 3)

1. The deflection board MRGC is a variant of the basic board MRGZ and is used in p.p.i. displays to provide ranges of 32, 64, 128 and 256 data miles. The circuit configuration is unchanged from the basic board and the specific components fitted are only concerned with range scaling.

TABLE 1

SPECIFIC COMPONENTS LIST

Component	Value	Component	Value	Component	Value
R1	100k	R115	15k	C4	470n
R10	100k	R117	14.3k	C10	220n
R28	1k	R118	33.3k	C10a	-
R46	56k	R119	100k		
R47	10k	R120	100k		
R48	18k	R168	2.2k		
R59	12k	R169	-		
R73	10	R180	15k		
R74	10	R210	-		
R112	10k				
R113	12k	RV20	5k		

APPENDIX 6

DEFLECTION BOARD MRGR
(687/00038/044)

5840-99-115-2250

(Incorporating modifications up to Mod. Strike-off No. 3)

1. The deflection board MRGR is a variant of the basic board MRGZ and is used in HRI displays to provide height scales up to 100 000ft. The circuit configuration is unchanged from the basic board and the specific components fitted are only concerned with height scaling.

TABLE 1

SPECIFIC COMPONENTS LIST

Component	Value	Component	Value	Component	Value
R1	50k	R115	68k	C4	470n
R10	50k	R117	-	C10	33n
R28	1k	R118	-	C10a	-
R46	22k	R119	-		
R47	68k	R120	10k		
R48	12k	R168	3.9k		
R59	6.8k	R169	8.2k		
R73	10	R180	15k		
R74	10	R210	470		
R112	5.6k				
R113	12k	RV20	10k		

APPENDIX 7

DEFLECTION BOARD MRGQ
(687/00038/043)

(Incorporating modifications up to Mod Strike-off No.4)

1. The deflection board MRGQ is a variant of the basic board MRGZ and is used in HRI displays to provide height scales up to 100 000ft. The circuit configuration is unchanged from the basic board and the specific components fitted are only concerned with height scaling.

TABLE 1

SPECIFIC COMPONENT LIST

Component	Value	Component	Value	Component	Value
R1	50k	R115	220k	C4	470n
R10	50k	R117	-	C10	33n
R28	1k	R118	-	C10a	-
R46	22k	R119	-		
R47	68k	R120	10k		
R48	12k	R168	3.9k		
R59	6.8k	R169	8.2k		
R73	10	R180	15k		
R74	10	R210	470		
R112	56k				
R113	10k	RV20	5k		

Chapter 3

DEFLECTION BOARDS (MRK SERIES)

LIST OF CONTENTS

	Para.
Introduction	1
OUTLINE OF OPERATION	
Introduction	4
Timebase generation... ..	6
Deflection drive waveform generation... ..	9
CIRCUIT DESCRIPTION	
Timebase generation... ..	12
Deflection drive waveform generation... ..	19
Protection against supply failure	26

LIST OF ILLUSTRATIONS

	Fig.
Deflection board MRKZ (12013): functional diagram	1
Deflection board MRKZ (12013): idealized waveforms	2
Deflection board MRKZ (12013): component location	3
Deflection board MRKZ (12013): circuit waveforms...	4
Deflection board MRKZ (12013): circuit	5
(to be issued later)	

AL 11

LIST OF APPENDICES

	App.
Deflection board MRKC	1

Introduction

1. Deflection board MRKZ (12013) forms the basic X deflection board in all height-range autonomous displays; variants of the board arise from different range requirements. Details of the board variants are given in appendices to this chapter.

2. The board generates a pair of opposed deflection drive waveforms suitable for application to a pair of complementary current-converter amplifiers forming part of the deflection coil drive amplifier assembly; these waveforms determine the components of spot position and velocity in the X axis.

3. The output waveforms, together with a pair of opposed Y deflection drive waveforms generated within the Y deflection board and feeding the remaining current-converter amplifiers of the assembly, control spot position and velocity on the screen at all times.

OUTLINE OF OPERATION

Introduction

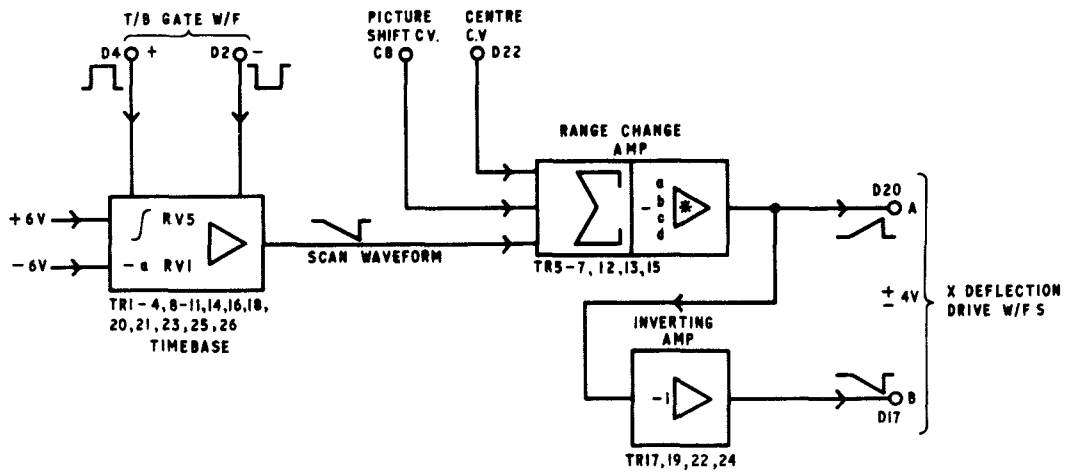
4. One of the requirements of the height-range display is that the horizontal component of spot velocity is constant, providing an X axis which represents time, i.e. radar range. Another requirement is for a constant shift component of X deflection such that deflection commences from the left of the screen. These requirements apply equally to both mainscan and interscan functions and therefore the same drive waveform is used in both MS and IS periods.

5. Since the scan and shift control voltages used to generate the deflection drive waveform remain unaltered during both the scan and shift regimes, it is not necessary to provide scan or shift MS/IS switching. Demodulation and rate prediction circuits are not required since the deflection waveform is constant in amplitude. Thus board MRKZ is similar to board MRGZ except that circuits concerned with demodulation, rate prediction, MS/IS switching and symbol generation are omitted.

Timebase generation

6. The scan waveform is generated by a shifting-integrator circuit. A potential of -6V is applied as the shift control input to the circuit, +6V is applied as the scan control input and an opposed pair of gate waveforms (the +ve and -ve timebase gate waveforms) control the selection between shift and scan modes. The scan mode obtains during the whole of both MS and IS scan regimes whilst the shift mode obtains in the intervals between (i.e. during MS and IS shift regimes).

7. In shift regimes the timebase circuit output (the scan waveform) is steady at a level determined by the -6V shift control input; this is necessary to off-centre the trace origin to the lower left of the c.r.t. to make the most efficient use of screen area. In scan regimes the scan waveform is a



* THIS AMP HAS FOUR ALTERNATIVE SWITCHABLE GAIN FACTORS (a b c d) SELECTED ACCORDING TO RANGE REQUIRED.

B/DDL/12013/B
SHEET 1 ISSUE 2

FIG.1 FUNCTIONAL DIAGRAM

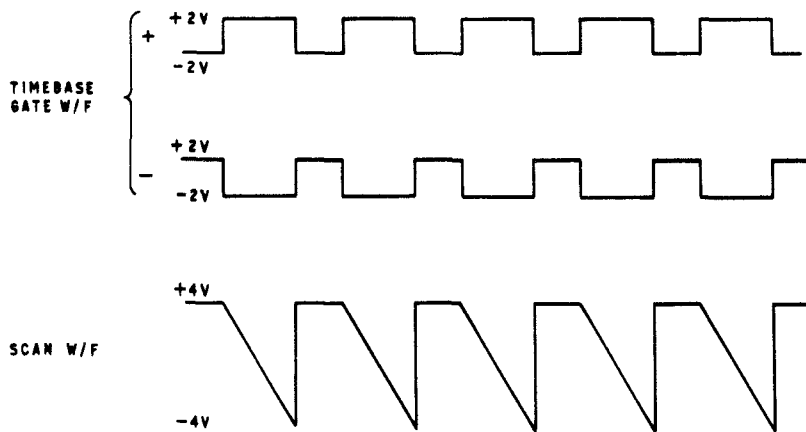


FIG.2 IDEALIZED WAVEFORMS

negative-going sawtooth of constant amplitude with a positive base level.

8. The scan waveform output from the timebase circuit is applied to a summing operational amplifier TR5, 12-13, 15.

Deflection drive waveform generation

9. The output circuit of board MRKZ comprises two operational amplifiers connected in cascade; the first (TR5, 12-13, 15) is a summing amplifier with four preset switchable gain factors which provide the four range scales required by the display, and the second (TR17, 19, 22, 24) is an inverting amplifier with a unity gain factor. The first operational amplifier output is the 'A' output deflection drive waveform; this output is also used to provide an input to the second operational amplifier. The output from the second amplifier is 'B' deflection drive waveform which is an inverted version of the 'A' output.

10. Three inputs are applied to the first amplifier; these are the scan waveform, the X centre shift voltage and the picture shift voltage. The X centre shift voltage is derived from the X CENTRE potentiometer control on the viewing unit control panel. The picture shift voltage is one of two levels, the selection being made by the RADAR SHIFT push-button switch on the operator's control panel. When the RADAR SHIFT push-button is not operated, the picture shift voltage is at earth potential and provides centred conditions; when RADAR SHIFT is operated, the picture shift voltage is derived from the SHIFT potentiometer control on the operator's control panel and this state is selected when off-centre conditions are required (i.e. for h.r.i. displays).

11. The opposed deflection drive waveforms, fed out of the board on PLD20 and PLD17, are routed to the deflection coil drive amplifier assembly for conversion into current waveforms suitable for driving the c.r.t. deflection coils.

CIRCUIT DESCRIPTION (Fig. 5)

Timebase generation

12. The timebase generation circuit comprises TR1-4, 8-1, 14, 16, 18, 20-21, 23 and 25-26 operating as a shifting integrator. A potential of -6V is applied to the shift input resistance (comprising RV1 and R1) and the feedback resistor (R50). The scan control input is +6V and this is applied to input resistance RV5 and R38; C10 is the feedback capacitor. The non-inverting amplifier comprises TR1-4, 9 and 11, the inverting amplifier contains TR14, 16, 18, 20-21, 23 and 25-26 whilst TR8 and 10 form the switch between the

two. This switch is controlled by the opposed +ve and -ve timebase gate waveforms which alternate between levels of $\pm 2V$ (Fig. 4).

13. In the non-inverting amplifier TR1 is a differential amplifier. The inverted output from TR1a collector is fed through emitter-follower TR2, inverted by common-emitter amplifier TR3, then taken via emitter-follower TR4 and electronic switch TR8 and 10 to the complementary pair of emitter-followers TR9 and 11.

14. MR1-2 limit the voltage excursion at TR1a base to within $\pm 0.3V$ of earth. Preset potentiometer RV1 provides the shift control input which determines the d. c. level at the output of TR25-26, thus fixing the d. c. starting point of the scan waveform at PLC14.

15. To ensure that, during scan modes, the non-inverting amplifier is not driven into a state from which it cannot recover rapidly, the positive timebase gate waveform is applied to the common-emitters of TR1 via MR3; these will be driven to +2V which is sufficient to cut off both sections.

16. The first stage of the inverting amplifier comprises differential amplifier TR14. Negative feedback is applied to the two emitters of TR14 via separate common-emitter inverter stages (TR16, 18) and diodes (MR10, 12) from their two collectors. This arrangement compensates for changes of circuit parameters with temperature.

17. The inverted output from TR16 emitter is taken to emitter-follower TR20, then applied via R68 to the emitter of common-base stage TR21. The output from TR21 collector is fed via emitter-follower TR23 to the final stage comprising the complementary pair of emitter-followers TR25-26.

18. The output waveform from complementary emitter-followers comprises a scan waveform which is fed to the Y deflection board (MRGZ) via PLC14 where it is used to produce earth curvature correction, as well as to the range change amplifier via coupling network R7, C2, R3.

Deflection drive waveform generation

19. Two operational amplifiers (the range change amplifier and the range change amplifier inverter) comprise the two output amplifiers which provide the 'A' and 'B' deflection drive waveforms.

20. The range change amplifier (TR5-7, 12-13, 15) is the first of the two

output amplifiers. It is a summing operational amplifier and sums three inputs, i. e. the waveform from the timebase generator, the picture shift control voltage and the X centre control voltage.

21. Input impedances of the range change amplifier are R9, R6 and circuit R7, C2, R3. The feedback impedance is R17 when the shortest range is selected, and by R17 in parallel with R14, R13 or R12 as the range is progressively lengthened; the connections are made by relay contacts RLC1, RLB1 and RLA1 which are operated by the range switch on the viewing unit control panel.

22. High-gain differential amplifier TR5 uses earth level as the reference input against which the summing-junction potential is compared. The non-inverted collector output is passed via emitter-follower TR12 and common-emitter stage TR13 to output emitter-follower TR15. The 'A' deflection drive waveform and the input to the inverter circuit are obtained from TR15 emitter. Switch SA is used with RV2 preset control to balance the amplifier. Diodes MR5-6 limit the voltage excursion at the summing junction to within $\pm 0.3V$ of earth. Circuits C5, R30 and C8, R40 provide top-cut and improve stability.

23. Circuit TR6-7, RV3-4, R26, 29, 31-34 and MR7-8 limits the output of the range change amplifier (and consequently the output of inverter amplifier TR17, 19, 22, 24) to within $\pm 4V$. This circuit shunts the feedback network with a low impedance as the limiting levels are reached, greatly reducing amplifier gain outside these levels. Transistors TR6-7 operate as emitter-followers with their bases connected to intermediate points of a potential divider network connected between $\pm 6V$ and centre-tapped to the amplifier output. The slider potentials of RV3-4 determine the two base potentials which are adjusted to limiting levels $+4V$ and $-4V$ with the amplifier output at zero. The sense of connection of the two diodes which separately connect the emitters to the amplifier centre-point is such that they are back-biased when the amplifier is at zero.

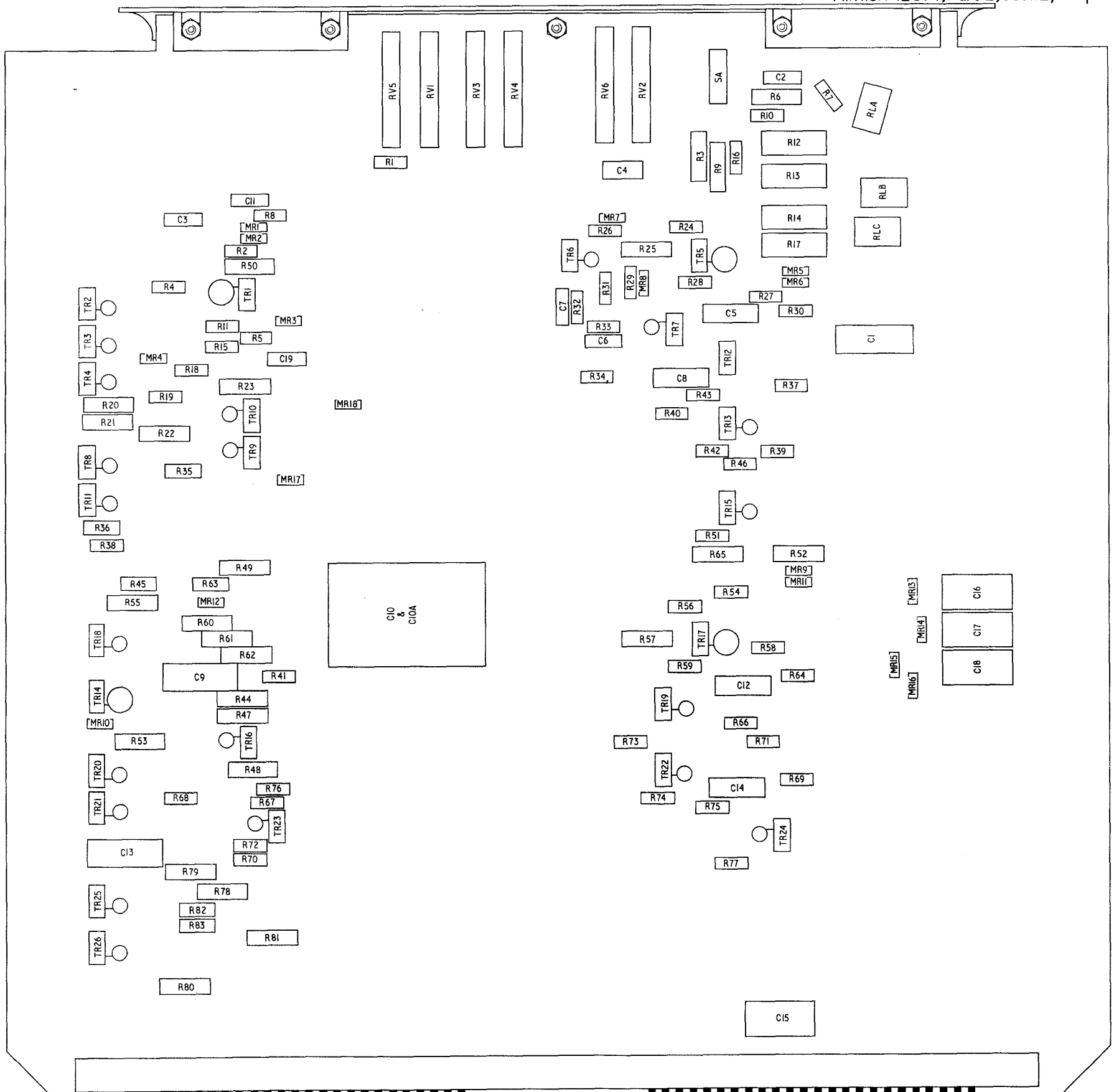
24. With the amplifier working normally, the waveforms on the bases and emitters of TR6-7 are slightly attenuated versions of the amplifier output superimposed on the d. c. biases obtained from the potential divider network. As the output moves towards its limits, the reverse bias on one or other of diodes MR7-8 diminishes until, when the limit is reached, one or other of the diodes starts to conduct, applying heavy negative feedback to the centre-point and quickly arresting the output excursion.

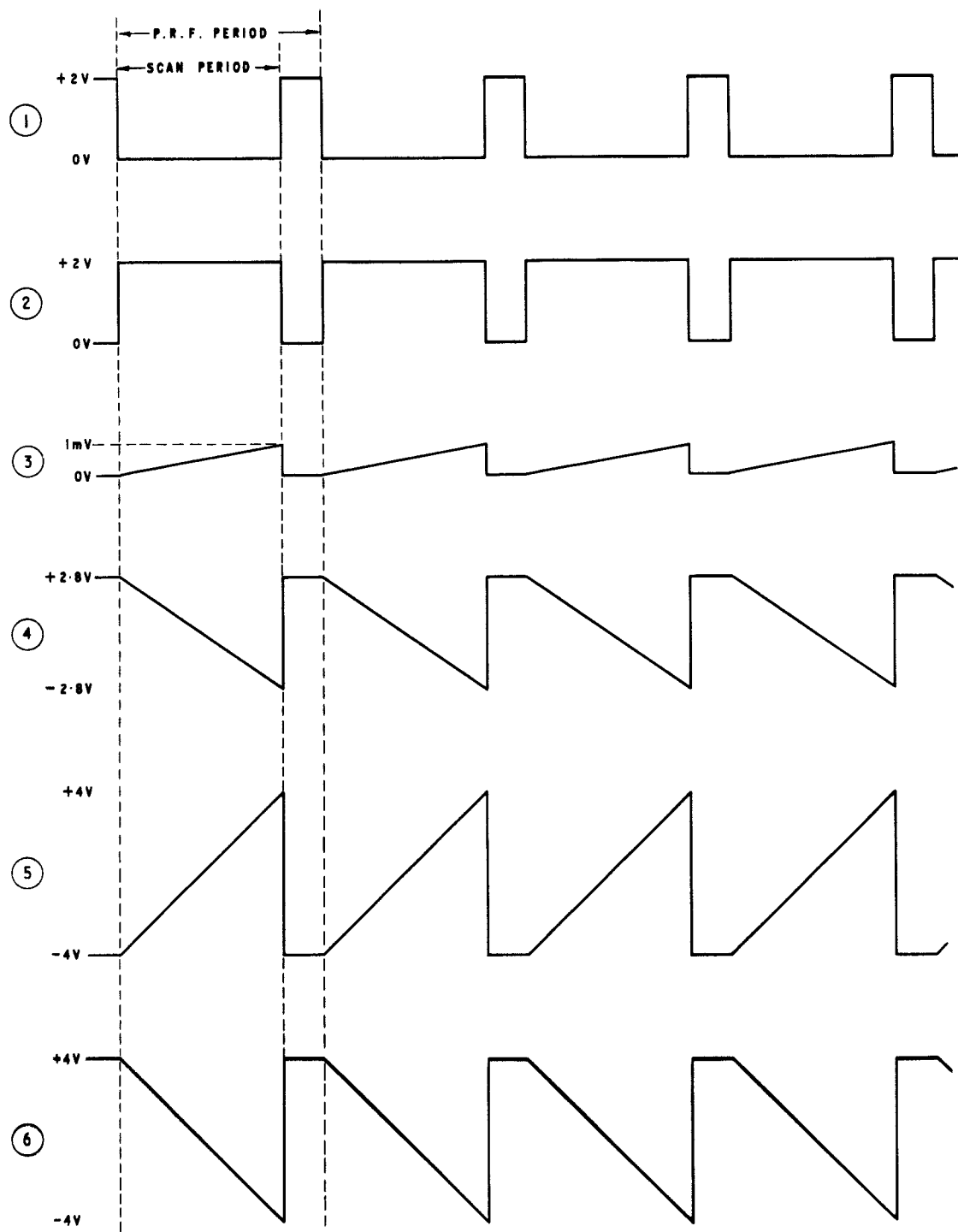
25. The range change amplifier inverter is an operational amplifier comprising TR17, 19, 22 and 24, and it provides the 'B' deflection drive waveform. Input and output resistances R52 and R65 are equal and the amplifier has a unity gain factor. Earth level provides the reference input to TR17b base. The non-inverted output from TR17b collector is fed via

emitter-follower TR19 to common-emitter amplifier TR22. This amplifier provides inversion and drives output emitter-follower TR24 which provides the 'B' deflection drive waveform. Diodes MR9 and 11 limit the voltage excursion at TR17 input to $\pm 0.3V$ with respect to earth. Top-cut is provided by C12, R64 and C14, R69, improving the stability of the amplifier.

Protection against supply failure

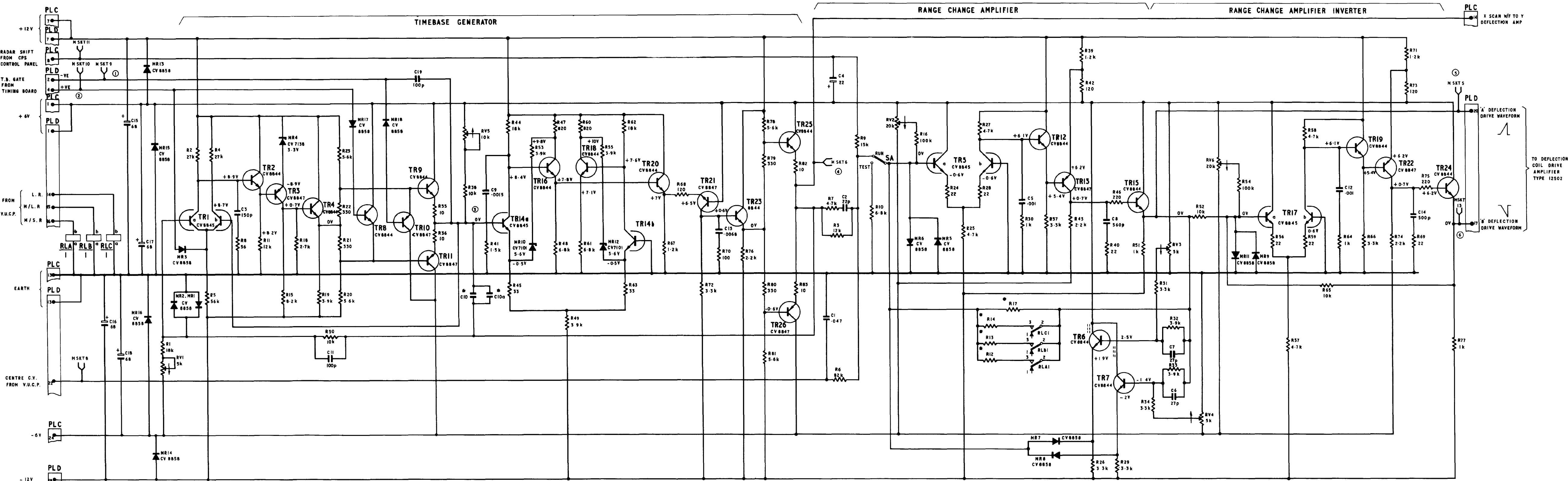
26. The circuits on the board are protected from damage which would result from failure of one or other of the power supplies by protective diodes MR13-16. These diodes are normally back-biased, but each diode would conduct if the associated power supply should fail. If the +12V supply failed, the +12V line would fall towards earth until arrested at +6V by the action of MR13. Similarly MR15 arrests the +6V line at earth level, MR14 arrests the -12V line at -6V and MR16 arrests the -6V line at earth. Capacitors C15-18 ensure that supply line transients are decoupled to earth.





Deflection board MPK7 (2012) circuit waveforms

Fig.4



ENCIRCLED NUMBERS INDICATE POINTS WHOSE WAVEFORM IS GIVEN IN FIG. 4

* COMPONENTS ARE FITTED ONLY ON SPECIFIC BOARD

Deflection board MRKZ (12013) : circuit

Fig. 5

Appendix 1

DEFLECTION BOARD MRKC
(687/00678/020, formerly 12015A)

5840-99-222-5094

Incorporating modifications up to Mod. Strike 1

1. Deflection board MRKC is a variant of the MRKZ family and is used to generate X deflection waveforms in h.r.i. applications of the Mk. 5 display with a range of 240 miles; it differs from the basic board only in the change of component values necessary to achieve the correct range and sawtooth slope.

TABLE 1

Specific components list

Component	Value
R12	14.3kohms
R13	33.3kohms
R14	100kohms
R17	100kohms
C10	0.2 μ F

Appendix 2

DEFLECTION BOARD MRKF (12463)

Deflection board MRKF is a variant of the MRKZ family and is used to generate X deflection waveforms in h. r. i. applications of the Mk.5 display with a range of 300 miles* (*NATO Mile - 2000yd) it differs from the basic board only in the change of component values necessary to achieve the correct range and sawtooth slope.

TABLE 1

Specific components list

Component	Value
R12	14.3kohm
R13	33.3kohm
R14	100kohm
R17	100kohm
C10	0.2 μ F
C10a	0.1 μ F

CHAPTER 4

VIDEO BOARDS (MFD SERIES)

LIST OF CONTENTS

	Para.
General	1
OUTLINE OF OPERATION	
Video channel	8
Brilliance channel	13
Calibration marker generator	18
CIRCUIT DESCRIPTION	
Video channel	24
Brilliance channel	39
Calibration marker generator	46
Protection circuits	54

LIST OF ILLUSTRATIONS

	Fig.
Video board MFDZ (12005): functional diagram	1
Video board MFDZ (12005): component location	2
Video board MFDZ (12005): waveforms	3
Video board MFDZ (12005): circuit (Part A)... ..	4
Video board MFDZ (12005): circuit (Part B)... ..	5

LIST OF APPENDICES

	App.
Video board MFDB (12029)	1
Video board MFDR (687/1/00419/002)	2
Video board MFDD (12139)	3
Video board MFDF (12214)	4
Video board MFDH (12277)	5

General

1. Video board MFDZ is the basic modulation board for all types of autonomous displays. For details of variants of the basic board refer to appendices following this chapter.

2. The board generates:-

- (1) A complex video waveform suitable for application to the cathode of the c. r. t.
- (2) A complex brilliance waveform suitable for application to the grid of the c. r. t.
- (3) Two sets of range calibration marker pulses which form components of the complex video waveform, one set (the 'No. 2 calibration markers') marking ranges at definite multiples of the other ('No. 1 calibration markers').

3. The board's circuits therefore are divided into three main groups, each concerned with the generation of one of the waveforms described in para. 2; these groups are the 'video channel', the 'brilliance channel' and the 'calibration generator'.

4. The complex video waveform is a combination of up to four radar videos and two sets of calibration markers superimposed upon a 'no video' level in MS scan regimes, and a 'just black' level in IS or FS scan regimes and all shift regimes.

5. The complex brilliance waveform consists of levels proportional to MS and either IS or FS brilliance control voltages in their appropriate scan regimes and a 'blacker-than-black' level during all shift regime.

6. A special octagonal blanking circuit (forming part of the brilliance channel) ensures that when the spot sweeps outside the periphery of the c. r. t. face, the complex video and brilliance waveforms revert to 'just black' and 'blacker-than-black' levels respectively.

7. The board may be used in both interscan and fastscan systems. The term 'IS/FS' is used to denote periods or functions other than mainscan periods and functions.

OUTLINE OF OPERATION (Fig. 1)

Video channel

8. The four video inputs are applied (via A2-5) to four separate amplifiers (TR1-2, TR5, TR6-8, TR9-11 and TR12-14) each provided with indivi-

dual gain control (B20-23) and inhibit control (A11-12, A14-15) inputs. Gain and inhibiting control voltages for these inputs are derived from associated controls located on the viewing unit or operator's control panel. The outputs of those amplifiers not inhibited are then combined, amplified (TR3-4) and applied to one input of a differential mixing amplifier (TR16-17).

9. The two sets of range calibration pulses are amplified by separate amplifiers (TR18-19 and TR20-21) each provided with individual gain control (B19 B17) and inhibit control (A16-17) inputs. Gain and inhibiting controls are located on the viewing unit or operator's control panel. The outputs of these amplifiers are combined and applied to the other input of the differential mixing amplifier.

10. The output of the mixing amplifier constitutes mixed video superimposed on an internally-generated d. c. level (adjusted by RV5) corresponding to 'no video' brightness of the mainscan; this output is referred to as the 'MS video waveform'.

11. The MS video waveform is subsequently subjected to two processes: the first, performed by video blanking circuit TR24-25 TR30-31, suppresses the waveform in IS/FS display periods, replacing it with a d. c. level derived from RV8 which corresponds to 'just black' on the c. r. t.; the second process is performed by video gate circuit TR34 which inhibits the output of the blanking circuit in all shift regimes (MS and IS/FS) and in all intervals during which the spot sweeps outside the periphery of the c. r. t. The blanking circuit comprises a 2-way electronic switch controlled by the opposed 'MS' and 'IS/FS switch waveforms' derived from the timing board. The action of the video gate is controlled by a 'brilliance blanking waveform' generated in the brilliance channel.

12. The output from the video gate circuit is amplified (TR26-27) and passed via a limiting circuit (TR35) to the final amplifier (TR28-29). The level at which limiting occurs is determined by a video limit control voltage entering the board at B11 derived from the LIMITER control located on the viewing unit control panel. The negative-going output of the final amplifier is the 'complex video waveform' and is applied to the c. r. t. cathode via B2.

Brilliance channel

13. The complex brilliance waveform applied to the c. r. t. grid is made up of three component signals which are combined and amplified by summing amplifier TR49-52.

14. The first component is a d.c. level which, since it is applied continuously, affects the trace equally at all times. This level is referred to as the 'overall brilliance level' and is derived from a preset potentiometer RV11.

15. The second component, the 'switched brilliance control voltage', consists of a waveform which alternates between the MS and IS/FS brilliance control levels so that each appears during its appropriate periods. The MS and IS/FS brilliance control voltages, derived via B8, A10, A9 from potentiometers located on the viewing unit and operator's control panels are processed by electronic switch TR36-39, TR42-43 which is in turn controlled by the MS and IS/FS switch waveforms. The switch has three 'ways', one each for MS, IS and FS; in IS systems the FS way is permanently held off and vice versa.

16. The third component, the 'brilliance blanking waveform', consists of a 'calibration and brilliance gate waveform' and an octagonal blanking waveform which are combined in an OR gate (MR28-29). The calibration and brilliance gate waveform, generated in the associated timing board, alternates between the levels $\pm 5V$; the positive level obtains during shift regimes and causes the c.r.t. to be brillianced-blanked whilst the negative level obtains during scan regimes and removes the brilliance inhibition. The octagonal blanking waveform moves between the same two levels, the positive level obtaining whenever the spot moves outside the periphery of the c.r.t. This waveform is generated by octagonal blanking circuit TR44-46 TR48, which determines spot position from the values of two pairs of X and Y scan drive waveforms applied as inputs; the output changes from negative to positive level at the instant spot deflection exceeds the value required to traverse the screen.

17. In interscan systems the calibration and brilliance gate waveform may change from its negative level to its positive level at any instant during the IS scan regime, depending upon the setting of the IS range control (see Chap.1). This arrangement ensures that the trace is brilliance-blanked at the required range.

Calibration marker generator

18. The calibration range markers are derived from a gated oscillator TR54, TR68 which is controlled by the calibration and brilliance gate waveform so that the oscillator runs during the period that the trace is brightened in both MS and IS periods.

19. The output of the oscillator controls a Schmitt trigger squarer (TR55-57) which produces a rectangular waveform having the same frequency and a preset mark/space ratio. The positive-going edges of this waveform trigger pulse generator TR63-65 whose output is fed two ways:-

- (1) Direct to the video 5 amplifier as 'No.1 calibration markers'.
- (2) Via inhibitor TR66-67 to the video 6 amplifier as 'No.2 calibration markers'.

The inhibitor is controlled by a divider circuit (TR58-62) which is also triggered by positive-going edges of the squarer output.

20. In quiescent conditions the output of the divider is negative and causes inhibition; this changes to a positive level immediately after receipt of either every seventh trigger edge (if the display is calibrated in nautical miles) or every ninth trigger edge (if the display is calibrated in kilometres) for a period of 1.5 calibration oscillator cycles, thus permitting the inhibitor to transmit every eighth or tenth pulse of the pulse generator.

21. By setting the mark/space ratio of the squarer output, the pulses are phased accurately so that they are correctly positioned on the c.r.t. relative to zero range. The trigger inputs of both the divider and the pulse generator contain a common circuit (not shown on the schematic) which suppresses the first trigger edge produced after the oscillator is gated into action, thereby preventing the production of a marker pulse at zero range.

22. Since the production of range marker pulses is controlled by the calibration and brilliance gate waveform, range markers are produced in both IS/FS and MS scan regimes. However, the action of the video gate in the video channel ensures that these markers are not displayed in IS/FS scan regimes.

23. The standard calibration-marker intervals are 5 and 40 nautical miles, or 5 and 50 kilometres. Range markers are provided at other intervals to users' requirements by changing the oscillator frequency and the frequency divider ratio.

CIRCUIT DESCRIPTION

Video channel (Fig.4)

24. The four video signals pass through individual amplifiers to common amplifier TR3/TR4 and follow a common path from that point. The four input amplifiers are identical and only that associated with video 1 input will be described in detail.

25. The video 1 input signal is applied to input amplifier TR1/TR2 through an attenuator R9/R10 with an attenuation factor of 30:1 (this factor may be altered for non-standard displays). The video 1 amplifier is a long-tailed pair (TR1/TR2) with a gain control transistor (TR5) connected in the tail. The second input of the amplifier (to TR2 base) is near earth level; its exact d. c. level is set by RV1 to balance the opposed outputs from the halves of the amplifier.
26. The gain of the amplifier is controlled by the video 1 gain control on the viewing unit control panel, which applies a voltage in the range -12V to +12V to the base of TR5 via PLB23 and R15. This control voltage sets the collector current to the input amplifier. The amplifier is working with very small collector currents, and over the working range the gain of the amplifier is almost proportional to the collector current. The amplifier is switched off (inhibited) by applying -12V to the video 1 selector input via PLA11 from the video 1 ON/OFF switch on the viewing unit control panel. This -12V cuts off TR5 and reduces the amplifier collector current to zero.
27. Collector load resistors R2 and R3 are common to the four video input amplifiers and the combined video signals developed across them are applied to common amplifier TR3/TR4.
28. The common amplifier is the long-tailed pair TR3/TR4. The video signals are applied in anti-phase to the two bases and a single-ended output is taken from the collector of TR4 to one input of mixing amplifier TR16/TR17.
29. Video inputs 5 and 6 are the range-marker pulses from the calibration marker generator. These signals pass through individual amplifiers to the second input of mixing amplifier TR16/TR17. The two input amplifiers are identical and only that associated with video 5 input is described.
30. The video 5 input amplifier is the common-emitter stage TR19. The d. c. level at the base of this transistor is set by gain control transistor TR18, which is connected as an emitter-follower. The calibration marker pulses are positive-going with an amplitude of 5V and these are applied to the base of TR19 via C12. The amplifier is switched off (inhibited) by applying -12V to video 5 selector input PLA16 from the range marker (Cal.1) ON/OFF switch on the operator's control panel. This sets the base of TR19 not less than -5V negative with respect to its emitter, which is at earth level and the transistor does not conduct during the pulses.
31. The selector input is disconnected to switch on the amplifier and the gain of the amplifier is then controlled by the range marker (Cal.1) brilliance control on the viewing unit control panel. The brilliance control applies a voltage in the range -12V to +12V to PLB19, which sets the base of TR19 within the range 0 to -5V, and pulses appear at the collector with

an amplitude proportional to the algebraic sum of the pulse amplitude and the d. c. level of the base (i. e. TR19 conducts when the pulse amplitude exceeds the voltage on the base). Collector load R57 is common to video input amplifiers 5 and 6. The combined range-marker signals developed across R57 are applied to the second input of the mixing amplifier through C11.

32. Mixing amplifier TR16/TR17 is a long-tailed pair. Combined video signals 1 to 4 are applied to the base of TR16 and combined video signals 5 and 6 are applied to the base of TR17. The output is taken from the collector of TR16 through capacitor C53 to the video blanking circuit. A d. c. level is added to the video signal at the base of TR17 from RV5; this level is adjusted to set the black level (zero signal level) at the c. r. t. grid to the correct voltage (approximately +95V).

33. The video blanking circuit is a two-way electronic switch with an OR gate at the switching terminal of one of the 'ways'. The first way, consisting of TR24-25 with the MS switch waveform as control input, transmits the mixed video superimposed on 'on-video' level in MS periods. The second way consists of TR30-31 with either the IS or FS switch waveform as control input (applied via OR gate MR14-15); this way transmits the 'just-black' level derived from the slider of preset RV8 in either IS or FS periods. The output from the switch circuit is an inverted form of the inputs, amplified slightly. Capacitor C15 is included to increase high-frequency response in the first way of the switch. Diode MR3 protects the base-emitter junction of TR31 from excessive back-bias switching transients.

34. The switch output, developed across common load R74, is applied directly but with a change of level to TR26 base via Zener diode MR12. The input of the video pre-amplifier (TR26 base) is connected to video gate circuit TR34, MR16.

35. The video gate circuit (TR34, MR16) is controlled by the brilliance blanking waveform generated in the brilliance channel. This waveform moves between $\pm 5V$; when it is at -5V, TR34 and MR16 are cut off and TR26 amplifies the video normally, but when it is at +5V, TR34 is bottomed, MR16 conducts, TR26 is cut off and the video is suppressed.

36. TR26-27 are connected as a long-tailed pair and a single-ended output is taken from the collector of TR27 and applied to the base of emitter-follower TR28.

37. The video at TR28 base is limited by MR17 to the level at TR35

emitter. This level is varied over the range 0 to +6V as the level at B11 (derived from the video limiter control) is varied from -12V to +12V.

38. The final video amplifier comprises emitter-follower TR28 and twin transistor TR29 connected as a cascode (composite common-emitter + common-base) amplifier to limit the voltage developed across each section to a safe value. The clipped video is applied to the lower section via TR28. The black level voltage at the c.r.t. cathode is of the order of +95V with respect to signal earth. The exact level is set by post-limiter gain control RV7 and allows for variations in the c.r.t. grid base.

Brilliance channel (Fig. 5)

39. The MS and IS/FS brilliance control voltages derived from control potentiometers are applied to MS/IS/FS brilliance switch TR36-39, 42-43. In this 3-way switch only two of the ways are used in any given application of the board, and it is similar to the switch employed in the video blanking circuit. The switch is controlled by the opposed MS and IS/FS switch waveforms, the unused way (in the absence of a switch waveform) being automatically switched off by an internal bias network (R125-126 in the IS 'way' and R115-116 in the FS 'way'). The inverted and slightly amplified output of the switch common-load R4 is the 'switched brilliance C.V.' and it is applied to one input of the brilliance amplifier.

40. In the octagonal blanking circuit the four scan waveforms enter the board at A19-22 and are fed via a diode mixing circuit and a level setting network to the base of emitter-follower TR44. The standing level at this base is adjustable by preset RV10. The output of TR44 operates the over-driven long-tailed pair TR45-46, whose output is shifted in level by MR27, inverted by TR48 and fed to the OR gate (MR28-29).

41. When all the inputs to this circuit are around zero, TR44 base is at about +3V, TR45 conducts, TR46 is cut off and TR48 is bottomed so that the level fed out from TR48 collector is around -5V. When any input becomes sufficiently negative to bring TR44 base to about zero level, TR45 cuts off, TR46 conducts, TR48 cuts off sharply and the output changes rapidly to around +5V; this level is passed to the OR gate and blanks the trace. The exact input level at which changeover occurs is set by RV10, which therefore determines the position on the screen at which blanking takes place (normally just inside the edge).

42. R130 and R131 give the frame created by the blanking an octagonal shape. When the spot is scanning towards a cardinal point on the screen, only one of the diodes in the mixer is conducting as blanking level is reached, and therefore around this trace-bearing the blanking will take place at a constant level of X and Y deflection giving a horizontal or vertical edge. Around a half-cardinal point R130 and R131 allow two diodes to conduct

simultaneously, and the voltage at TR44 base depends on the average of the inputs to these two. Blanking therefore takes place at a constant average level of X and Y deflection and this gives an edge with a 45° slope in the neighbourhood of the half-cardinal points.

43. In addition to the octagonal blanking waveform the OR gate (MR28-29) receives the calibration and brilliance gate waveform, which also moves between levels of $\pm 5V$. The output of the gate is positive when one or both inputs is positive, and this level causes the c.r.t. to be brilliance-blanked. The output is the 'brilliance blanking waveform' and is fed:-

- (1) To the video gate circuit in the video channel.
- (2) To one of the inputs of the brilliance amplifier.

44. The brilliance amplifier (TR49-52) is a summing operational amplifier with three inputs:-

- (1) The switched brilliance control voltage.
- (2) An overall brilliance level of 0 to -12V.
- (3) The brilliance blanking waveform.

The switched brilliance control voltage is applied via series-connected input network R140-141, the brilliance blanking waveform is applied to the junction of these two resistors, and the overall brilliance level which is derived from preset RV11 is applied via R142. R149 is the feedback resistor; parallel-connected C27 provides increased feedback during transient voltage changes and thus reduces overshoot as the brilliance waveform goes negative. RV11 sets the overall brilliance of the c.r.t. which is of the order of +5V with respect to signal earth.

45. The brilliance amplifier consists of a long-tailed pair (TR49-50), an emitter-follower (TR51) and a base-fed output pair (TR52a TR52b). The long-tailed pair forms a differential amplifier with earth level applied as reference input; the non-inverted output from TR50 collector is applied to TR51 base via Zener diode MR30, which maintains a constant d.c. potential difference between these two points.

Calibration marker generator (Fig. 5)

46. The calibration oscillator is LC-tuned and employs transistor TR54 in a modified Hartley circuit. Gating transistor TR53 is connected as an emitter-follower and its emitter current flows through oscillator coil L3. The calibrator gate waveform is applied to the base of TR53. This gate waveform is at +5V during shift regimes and establishes a steady current through MR36, R158 and L3. The low impedance of TR53 emitter circuit effectively damps the tuned circuit and no oscillation takes place. The gate waveform changes abruptly to a level of -5V at the commencement of the scan regime, cutting off the emitter current of TR53, which removes the damping and causes the oscillatory circuit to ring. TR54 maintains the oscillation until the gate waveform reverts to +5V and the circuit resets. MR36 protects the base-emitter junction of TR53 against positive peaks of the oscillatory voltage.

47. The sinewave is applied through emitter-follower TR68 to Schmitt trigger stage TR55-56, which produces a rectangular output waveform having the same frequency as the sinewave but an adjustable mark/space ratio. The circuit may be regarded as an overdriven long-tailed pair with positive feedback incorporated to accelerate changeover, with the sinewave applied to one base and a d.c. potential derived from the slider of RV13 applied to the other base. Varying the setting of RV13 varies the points on the sinewave at which changeover takes place, thus varying the mark/space ratio of the output. This facility is provided for timing the negative-going edge of the output accurately, so that the first range marker may be correctly positioned on the c.r.t.

48. The output of the Schmitt trigger is inverted by TR57 and applied to the diode pump of the frequency divider via C41 and to the calibration pulse generator via C44. C40 is charged from the positive 5V gate waveform during the shift regimes, and this positive level applied to its base bottoms TR57. The first negative half-cycle at the output of the Schmitt trigger discharges C40 and the remaining cycles in the burst appear at the collector of TR57. The first negative half-cycle (at zero range) is not transmitted by TR57.

49. The pulse generator is a monostable multivibrator incorporating TR63, TR64. TR64 is 'on' in the stable state. The positive-going edge of the input squarewave is differentiated and used to trigger the monostable, which provides a positive-going pulse of 5V amplitude and 0.2 μ s duration. This calibration pulse is applied through emitter-follower TR65 to video input 5, and through an inhibitor to video channel 6.

50. A fraction of the output waveform at the collector of TR57 is tapped off by preset RV14 and applied to the diode pump circuit (MR40, C42) of the frequency divider. A positive-going current pulse flows into C42 during

each cycle of the squarewave and the voltage across C42 is applied to unity-gain pair TR58-59. This voltage change is fed back through MR39 to the other side of MR40 to ensure that both sides of MR40 are at the same level and the staircase waveform rises in steps of equal amplitude.

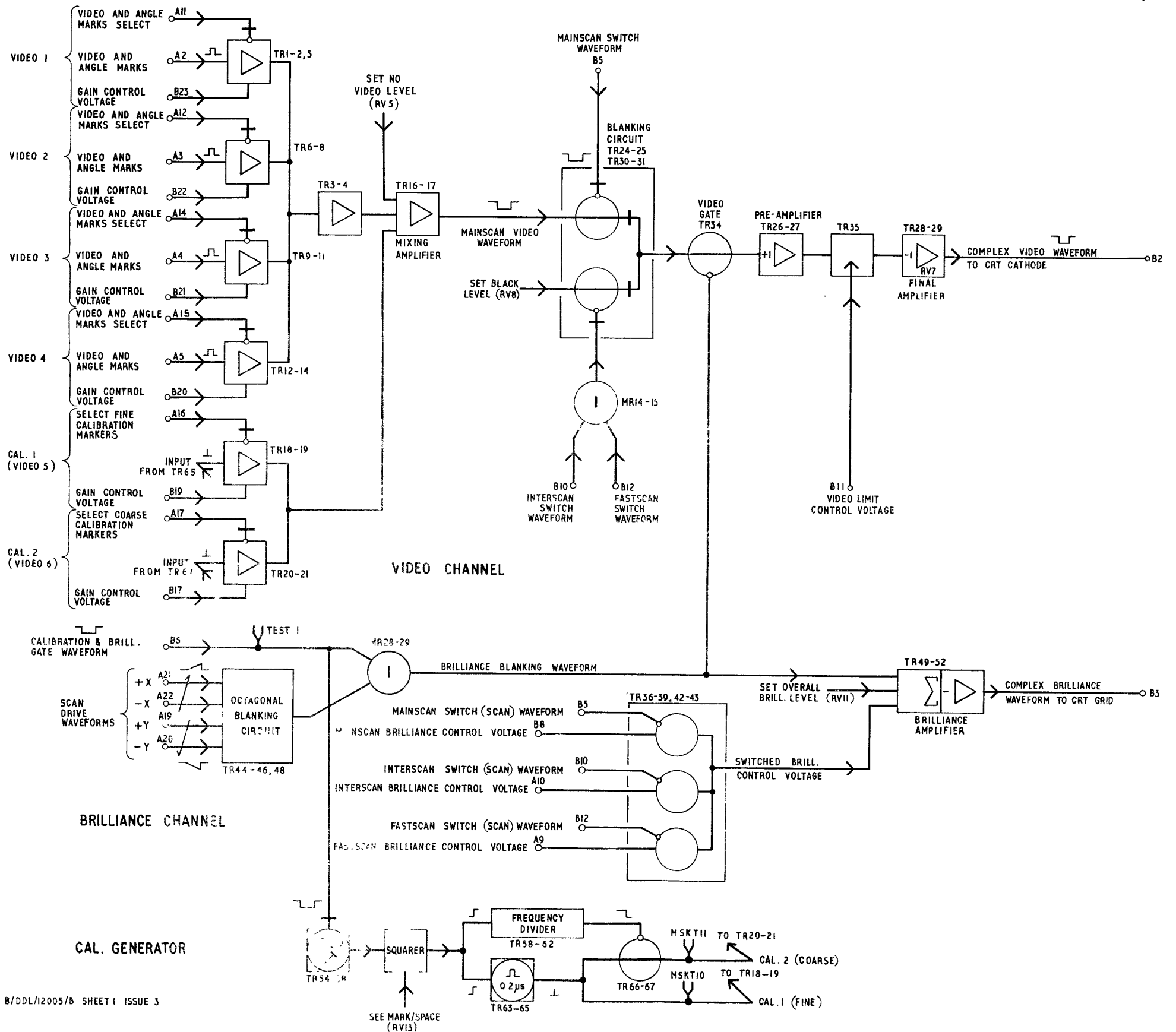
51. The staircase waveform is applied through Zener diode MR41 and diode MR42 to a monostable multivibrator TR60-61. The stable state of this monostable is with TR61 on and its collector at earth level. The circuit is adjusted by RV14 so that a staircase waveform of either 7 or 9 steps, according to the range scales fitted, has sufficient amplitude to trigger the monostable. The monostable provides a positive output pulse with a duration of 1.5 calibrator oscillator cycles. The trigger level can be set to other numbers of steps for special requirements.

52. The output of the monostable is applied to TR62, which is cut off by the monostable in its stable state. The collector of TR62 is connected to inhibitor TR66. TR66 is bottomed by the positive collector voltage of TR62, and the calibration pulses from the pulse generator are bypassed to earth and do not pass to TR67. The positive-going output pulse from the frequency divider monostable bottoms TR62 and its collector voltage falls to earth level. This cuts off TR66 and allows the eighth or tenth pulse to pass through TR67 to video 6 input.

53. Switching TR62 collector to earth level also discharges the staircase capacitor through MR43 and the circuit starts to count from the tenth or eleventh pulse. At the end of the scan regime, the cal. gate waveform changes to 5V and this, applied through MR44 to the base of TR62, bottoms TR62 and discharges the staircase capacitor if a part count has been made.

Protection circuits (Fig.4)

54. The board operates from four regulated power supplies, provided by the power unit (+12V, +6V, -12V, -6V). These supplies are interconnected through the circuits and if a supply fails, the supplies of opposite polarity may attempt to drive a reverse current through certain transistors. A protection circuit is included to prevent this happening, consisting of MR31-34 and C28-31. The diodes are each back-biased by their respective power supply. If a supply fails and reverse voltage appears on the line, the diode connected to it conducts and either earths the line (6V supplies) or holds it at 6V (12V supplies). The capacitors prevent the diodes from conducting on transients during normal operation and provide additional decoupling to isolate the boards from the power supply transients.

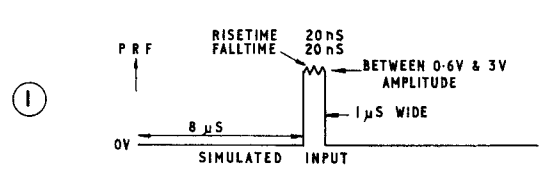


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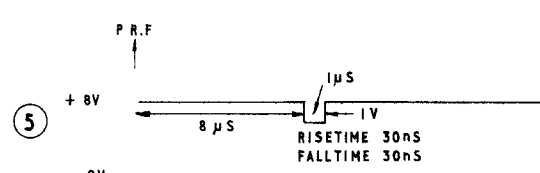
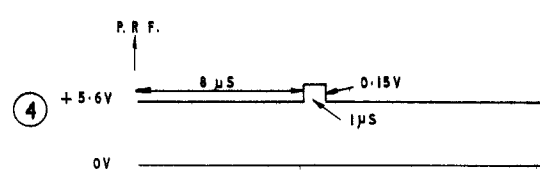
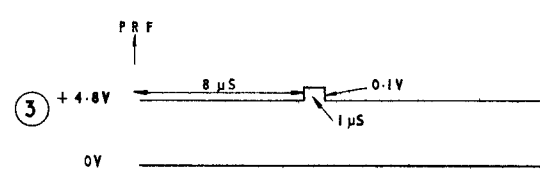
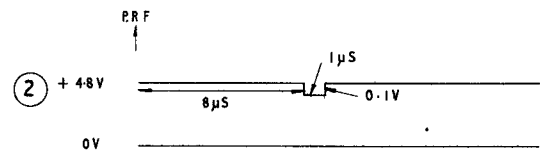
A.L. 13, June '70

Video board MFDZ (12005): functional diagram

Fig.1

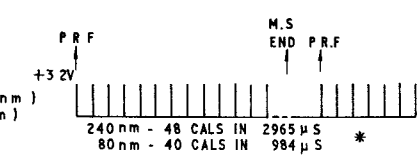


NOTE - REMAINING VIDEO SIGNAL WAVEFORMS TAKEN WITH VIDEO 1, 2, 3 & 4 GAIN CONTROLS ADJUSTED TO OBTAIN 30V SIGNAL ON CRT CATHODE (LIMITER SET FULLY ANTI-CLOCKWISE)



* SEE SUPPLEMENTS FOR VARIATIONS

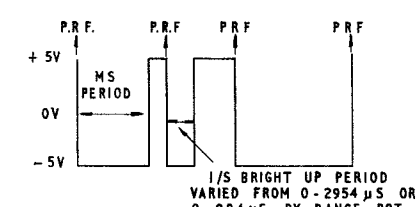
⑥ FINE CAL MARKERS
250 ns WIDTH AT HALF AMPLITUDE
SPACED 61.8 μs APART (5 nm)
SPACED 24.7 μs APART (2 nm) *



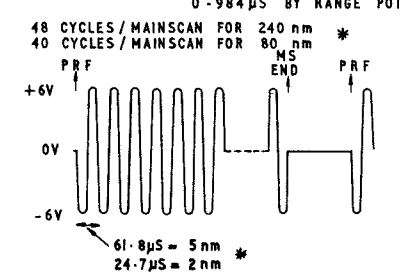
⑦ COARSE CAL MARKERS
250 ns WIDTH AT HALF AMPLITUDE
SPACED 246 μs OR 123 μs APART *



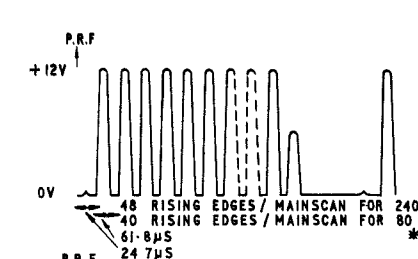
⑧ BRILLIANCE GATE (START DELAYED 3 μs FROM P.R.F.)



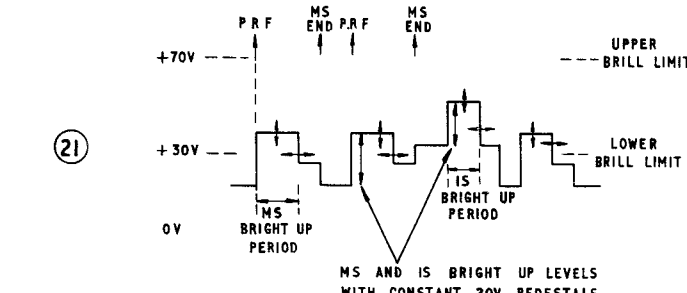
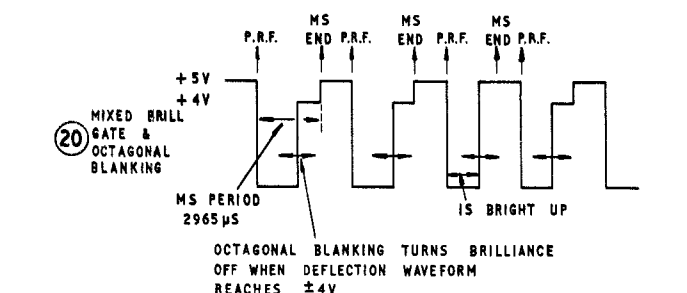
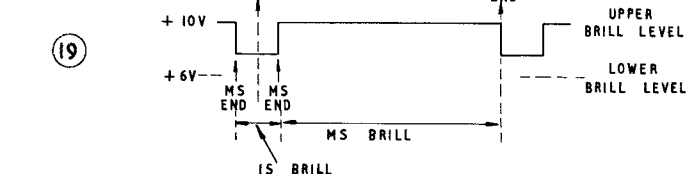
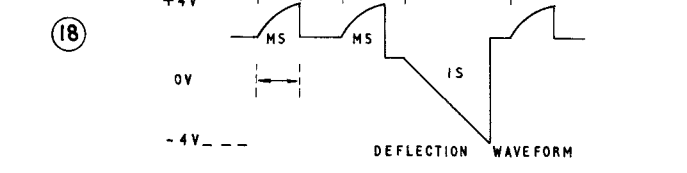
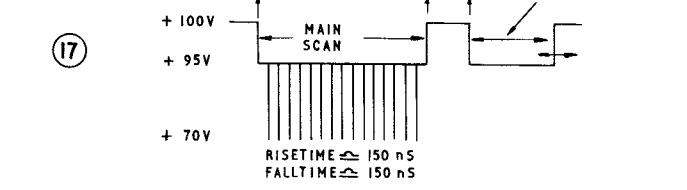
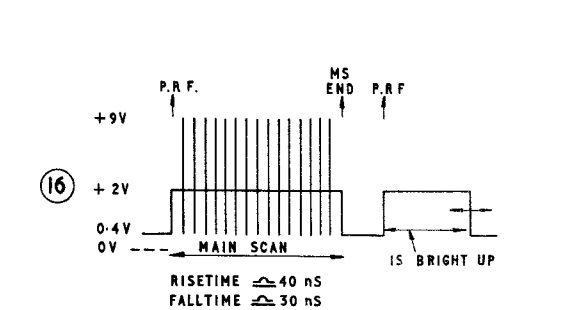
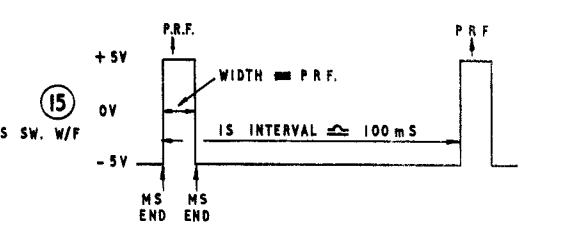
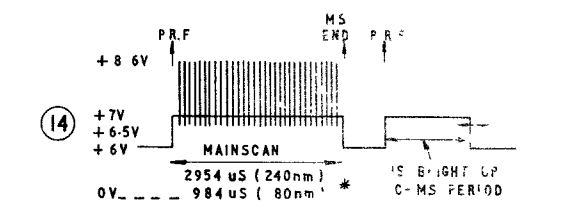
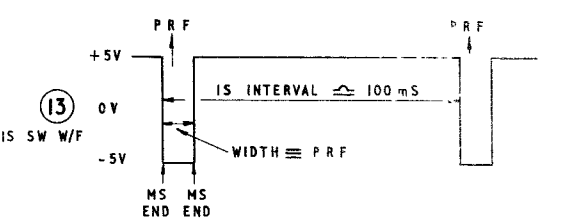
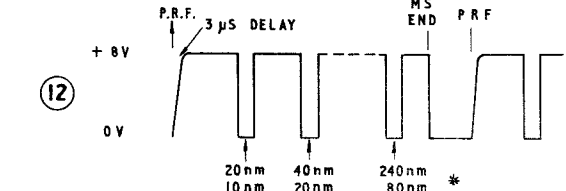
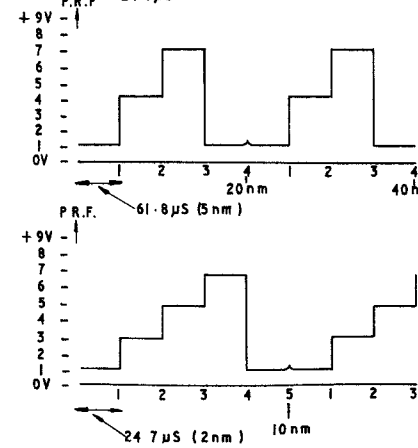
⑨ START DELAYED 3 μs FROM P.R.F.

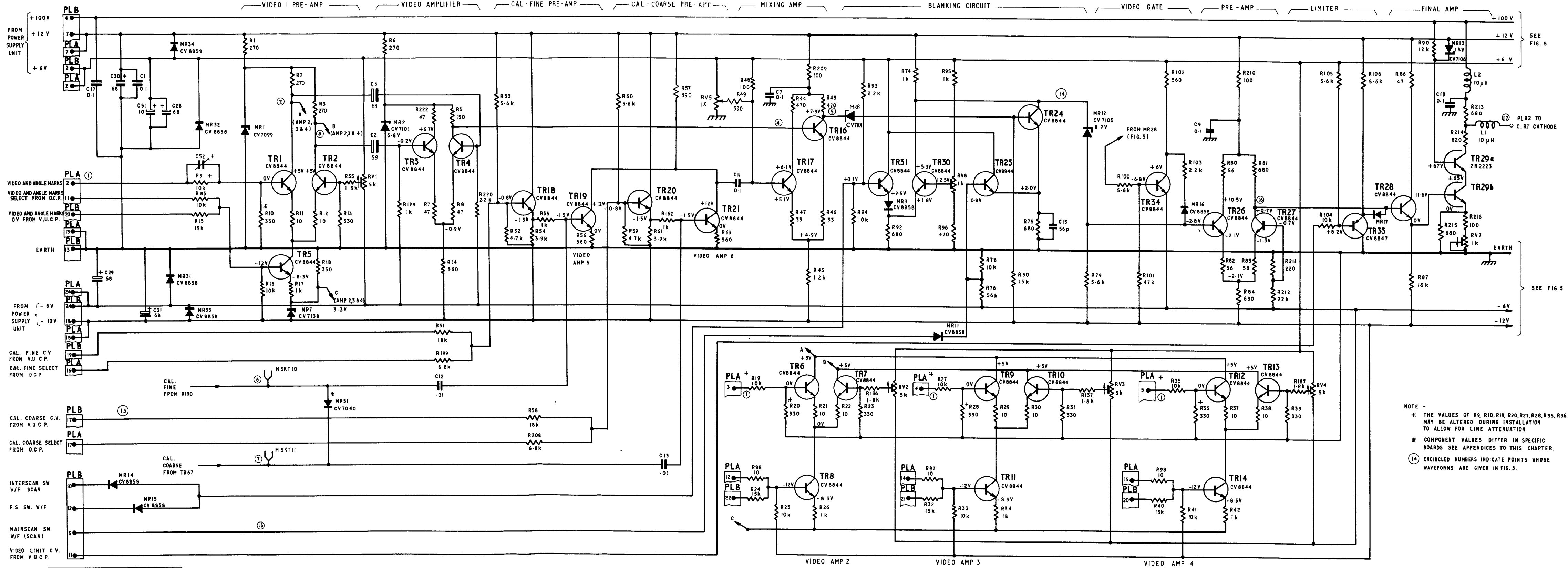


⑩



⑪

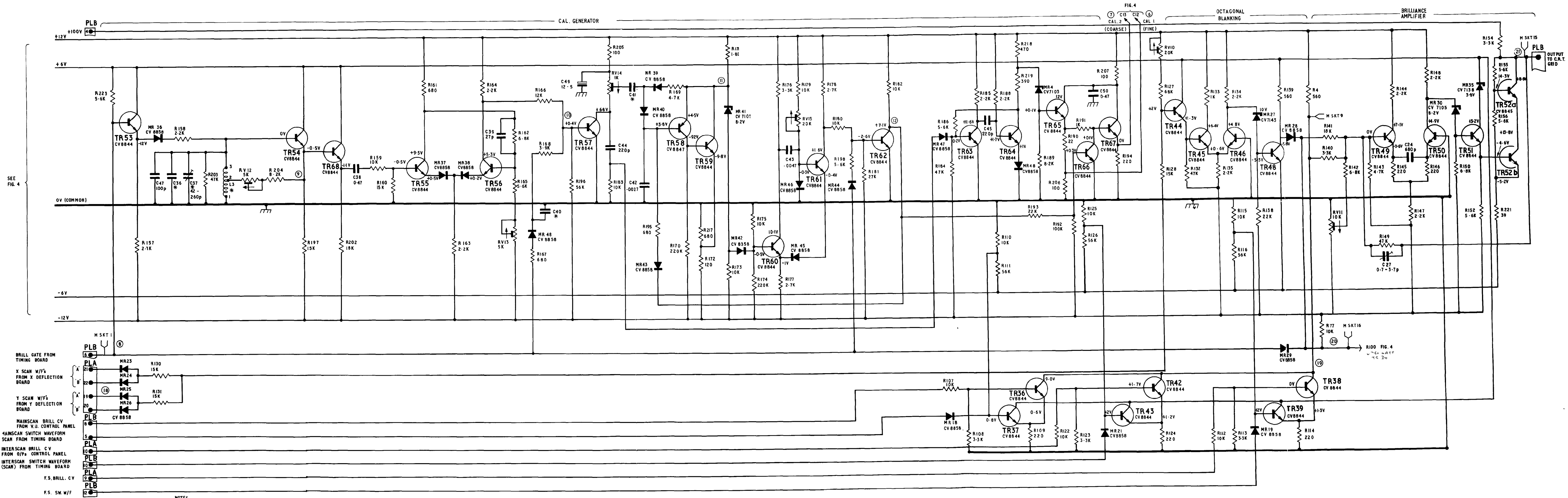




NOTE -
 * THE VALUES OF R9, R10, R19, R20, R27, R28, R35, R36 MAY BE ALTERED DURING INSTALLATION TO ALLOW FOR LINE ATTENUATION
 * COMPONENT VALUES DIFFER IN SPECIFIC BOARDS SEE APPENDICES TO THIS CHAPTER.
 (14) ENCIRCLED NUMBERS INDICATE POINTS WHOSE WAVEFORMS ARE GIVEN IN FIG.3.

B/DDL/12005/B	SHEET	2	3	4	5
	ISSUE	8	5	5	3

MODS INCORPORATED:- A3914



SEE FIG. 4

- BRILL GATE FROM TIMING BOARD
- X SCAN W/F's FROM X DEFLECTION BOARD
- Y SCAN W/F's FROM Y DEFLECTION BOARD
- MAINSCAN BRILL CV FROM V.U. CONTROL PANEL
- MAINSCAN SWITCH WAVEFORM SCAN FROM TIMING BOARD
- INTERSCAN BRILL CV FROM O/P CONTROL PANEL
- INTERSCAN SWITCH WAVEFORM (SCAN) FROM TIMING BOARD
- F.S. BRILL. CV
- F.S. SW. W/F

NOTES
 * COMPONENT VALUE DIFFERS IN SPECIFIC BOARDS. SEE APPENDICES TO THIS CHAPTER.
 (18) ENCIRCLED NUMBERS INDICATE POINTS WHOSE WAVEFORMS ARE GIVEN IN FIG. 3

B/DL/2005/B	SHEET	6	7	8	9	10
	ISSUE	3	6	3	3	7

Video board MFDZ (12005): circuit (Part B)

Fig. 5

Appendix 1

VIDEO BOARD MFDB (12029)

5840-99-956-5095

Incorporating modifications up to Mod. Strike 5

1. Video board MFDB is a variant of the MFDZ basic board, and it is tailored to provide calibration marker intervals at 5 and 40 data miles.

TABLE 1

Specific components list

Component	Value
C36	2200pF
C40	0.01 μ F
C41	390pF
C47	220pF
L3	Coil LNM

Appendix 2

VIDEO BOARD MFDR

(687/1/00419/002)

5840-99-222-1047

Incorporating modifications up to Mod. Strike 5

1. Video board MFDR is a variant of the MFDZ basic board, and it is tailored to provide calibration marker intervals at 4 and 64 data miles.

TABLE 1

Specific components list

Component	Value
C36	0.0012 μ F
C40	0.0047 μ F
C41	390pF
C47	150pF
L3	Coil LNM

Appendix 3

VIDEO BOARD MFDD (12139)
5840-99-953-5057

Mod. Strike 6

Video board MFDD is a variant of the basic MFDZ board. It provides the facilities given by the basic board and supplies calibration markers at 2 and 10 nautical miles.

SPECIFIC COMPONENTS LIST

Component	Type
C36	820pF
C40	4700pF
C41	680pF
C47	Open circuit
L3	Decca A/DDDL/7370/AB

Appendix 4

VIDEO BOARD MFDF (12214)

5840-99-955-3593

Mod. Strike 6

Video board MFDF is a variant of the basic board MFDZ. It provides the facilities given by the basic board and supplies calibration markers at 5 to 20 nautical miles.

SPECIFIC COMPONENTS LIST

Component	Type
C36	2200pF
C40	0.01 μ F
C41	1000pF
C47	220pF
L3	Decca A/DDI/7370/AA

Appendix 5

VIDEO BOARD MFDH (12277)
5840-99-948-6907

Mod. Strike 6

Video board MFDH is a variant of the basic MFDZ board. It provides the facilities given by the basic board and supplies calibration pulses at 10 and 50 data miles.

SPECIFIC COMPONENTS LIST

Component	Type
R204	5.6kohms
C36	0.01 μ F
C47	Selected on test (if fitted)
C40a	0.0047 μ F
C40b	0.01 μ F
C41	680pF
C42	0.0015 μ F
C43	0.01 μ F
L3	Plessey A/DDL/7370/AA

Chapter 5

SAMPLING GATE GENERATOR BOARDS

NBJA (12442) (5840-99-955-3885)

NBJB (12443) (5840-99-955-3882)

LIST OF CONTENTS

	Para.
Introduction	1
BOARD NBJB	
Circuit	
Schmidt trigger	4
Delay monostable	8
BOARD NBJA	
Circuit description	
Sample monostable	12
Protection against power supply failure	19

LIST OF ILLUSTRATIONS

	Fig.
Sampling gate generator boards; functional diagram	1
Sampling gate generator boards (NBJB and NBJA): idealized waveforms	2
Sampling gate generator board NBJB (12443): component layout	3
Sampling gate generator board NBJA (12242): component location	4
Sampling gate generator board NBJB (12443): circuit... ..	5
Sampling gate generator board NBJA (12442): circuit... ..	6

INTRODUCTION (Fig. 1)

1. The sampling gate generator (comprising boards NBJB and NBJA) is used in h. r. i. applications and provides sampling gate waveforms to the Y deflection board for use in the demodulator circuit. These waveforms consist

of complementary positive and negative pulses coincident with the peaks of the sinewave input.

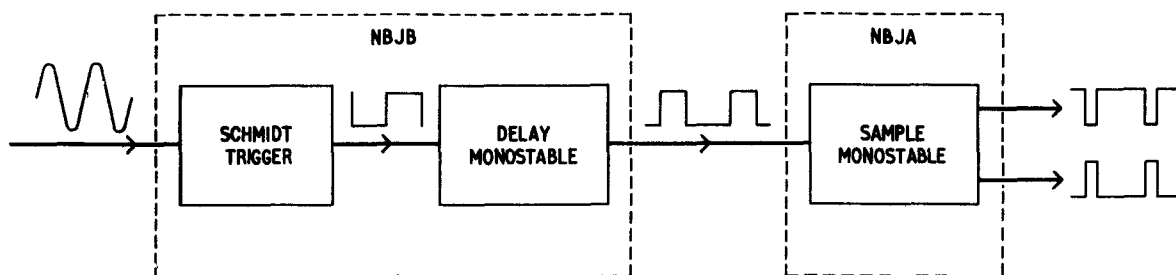


Fig. 1 Sampling gate generator boards: functional diagram

2. The input to the sampling gate generator is the synchro resolver drive waveform. This is normally a 400Hz sinewave produced by the synchro excitation supply circuits on the timing board, although in some applications a 1kHz sinewave obtained from an external source is used instead.

3. Boards NBJB and NBJA are connected in cascade. The sinewave input is taken to NBJB which contains a Schmidt trigger circuit and a delay monostable. The output is taken to the input of board NBJA which contains a sample monostable and provides the complementary pulse outputs.

BOARD NBJB

CIRCUIT DESCRIPTION (Fig. 2 and 5)

Schmidt trigger

4. The sinewave input enters the board at PLB24 and passes to the base of TR1 via R1. High gain differential amplifier TR1 to 2 operates as a Schmidt trigger circuit, producing a square-wave at TR2 collector; RV1 determines the voltage at which the circuit changes state and it is adjusted so that the change occurs when the input sinewave passes through 0V.

5. When the sinewave moves towards earth from its negative peak, then TR1 is cut off with its collector voltage about +12V (which assists the threshold potential of TR2 base via R4, R8 and RV1) and TR2 is bottomed with its collector voltage about -10V. As the sinewave approaches earth level TR1 begins to conduct, TR2 is driven towards cut-off and the threshold potential at TR2 base reverts to earth level. When the sinewave becomes

positive and moves towards its positive peak TR1 conducts heavily with the collector at -10V, drawing TR2 base slightly negative and TR2 cuts off; its collector potential is then about +12V. Capacitor C1 improves the high frequency response, reducing the time taken for the circuit to change state.

6. Thus TR2 collector potential changes from about -10V to +12V when the input sinewave moves in a positive direction, and similarly it will change from +12V to -10V when the input moves in a negative direction. These voltage changes are passed to the base of TR3, consequently TR3 collector is at a potential of about +12V when TR2 collector is -10V and TR3 collector is about earth level when TR2 collector is +12V.

7. The square waveform from TR3 collector passes to the differentiating network comprising C2, R11 and D3. The positive-going pulses are coincident with the rising edge of the input waveform and these are immediately suppressed by D3; the negative-going pulses coincide with the falling edge and are fed to TR4 emitter via C3.

Delay monostable

8. TR4 forms an input circuit for the monostable comprising TR5 and TR6. In the quiescent state TR4 is cut off by emitter bias from potential divider network R13 and R14, TR5 is cut off and TR6 is conducting.

9. The negative-going pulse to the emitter brings TR4 into conduction and its collector falls from about +6V to -6V. This fall is passed to the base of TR6 via C4, cutting off TR6; diode D5 prevents the full reverse voltage being applied to the emitter-base junction of TR6. The potential at TR6 collector rises to about +5V bringing the base of TR5 to about -3V; ~~TR5~~ TR5 bottoms with its collector voltage falling to about -6V, causing D4 to conduct and clamp TR4 collector to -6V. AL 26

10. Capacitor C4 charges via RV2 and R19 until TR6 base potential rises sufficiently to allow TR6 to conduct and return the monostable to its original condition. Time constant C4, RV2 and R19 determines the time duration of the unstable state.

11. The waveform at TR6 collector is a rectangular wave with its positive-going edge coincident with the instant the input sinewave is at earth potential and moving in a positive direction, and its negative-going edge adjusted by RV2 to be coincident with the positive peak of the sinewave input. This waveform is routed out of the board via PLB21 and fed to the input of board NBJA.

BOARD NBJA

CIRCUIT DESCRIPTION (Fig. 2 and 6)

Sample monostable

12. The rectangular wave from board NBJB (paragraph 11) enters NBJA at PLA24 and passes to differentiating network C1, R1 and D1. The positive-going pulses, coincident with the rising edge of the input waveform, are immediately suppressed by diode D1, whilst the negative-going pulses, coincident with the falling edge of the waveform and the positive peak of the sine-wave input to NBJB, are passed to TR1 emitter via C2.

13. TR1 forms the input circuit for monostable TR2 and TR3, and TR4 and TR5 are complementary emitter-follower output stages. In the quiescent state TR1 is cut off by emitter bias from potential divider R5 and R6, the base being held at -3.3V; TR2 is cut off and TR3 is conducting.

14. The negative-going pulses to the emitter brings TR1 into conduction and the collector voltage falls from about +2.7V to -2.7V. This fall is passed to the base of TR3 via C3, cutting off TR3. The voltage at TR3 collector rises to about +3V bringing the base of TR2 more positive than its emitter; TR2 bottoms with its collector potential about -3V causing D4 to conduct and clamp TR1 collector to -3V.

15. The monostable is now in its unstable state with TR2 collector potential appearing at TR4 base, resulting in a potential of about -3V at TR4 emitter. Similarly the collector potential of TR3 appearing at TR5 base results in an emitter voltage of +3V at TR5.

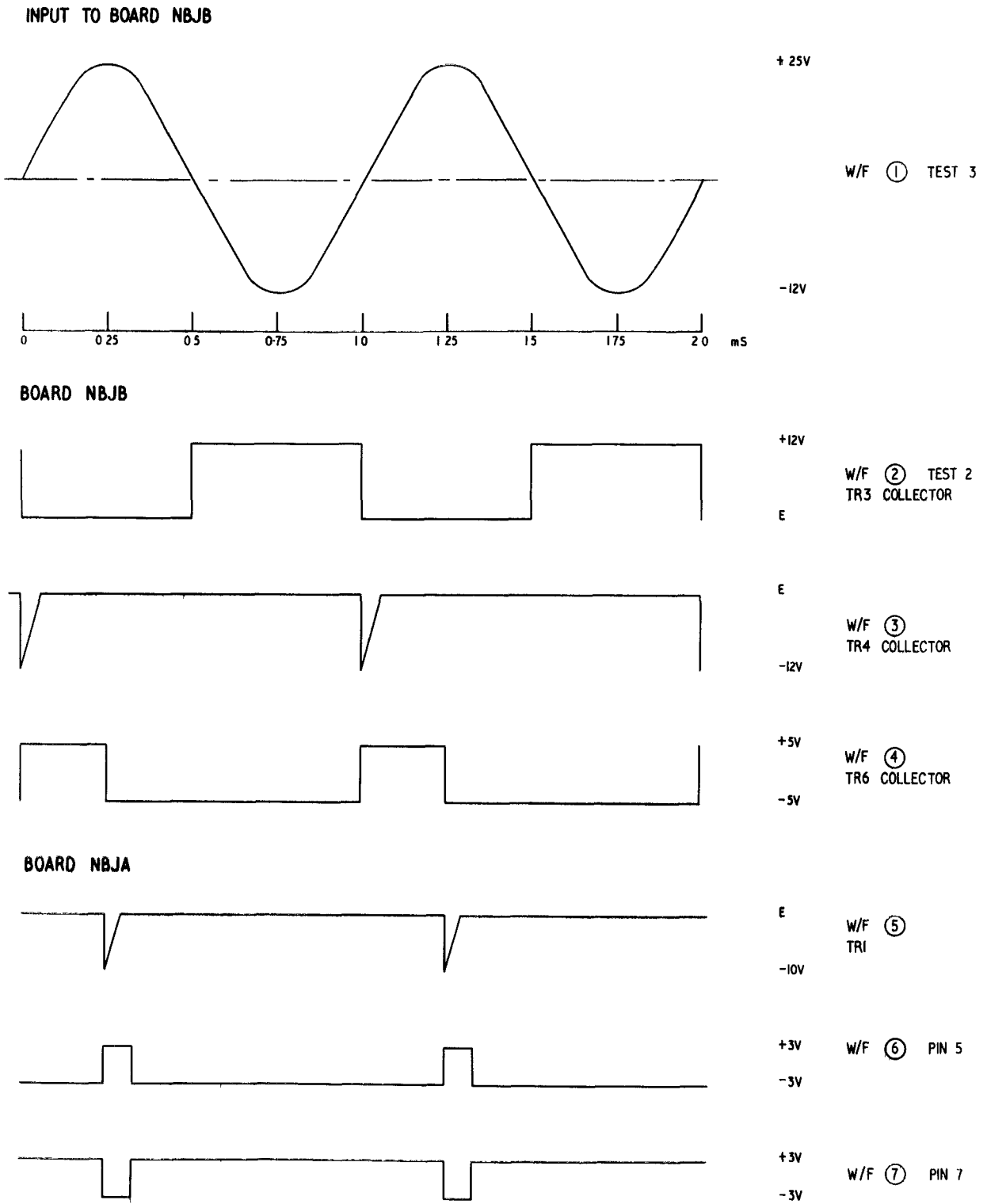
16. Capacitor C3 charges via RV1 and R10 until the potential at TR3 base rises sufficiently to allow TR3 to conduct and return the monostable to its original condition. Time constant C3, RV1 and R10 determines the time duration that the monostable is in its unstable state.

17. Thus TR4 emitter attains a level of -3V in the unstable state of the monostable and +3V in the stable state; this comprises the negative sampling gate waveform. Similarly TR5 emitter attains a level of +3V in the unstable state and -3V in the stable state; therefore this waveform is complementary to the waveform from TR4 emitter and comprises the positive sampling gate waveform.

18. The negative and positive sampling gate waveforms leave the board via PLA7 and PLA5 respectively and are routed to the demodulator circuits on the Y deflection board.

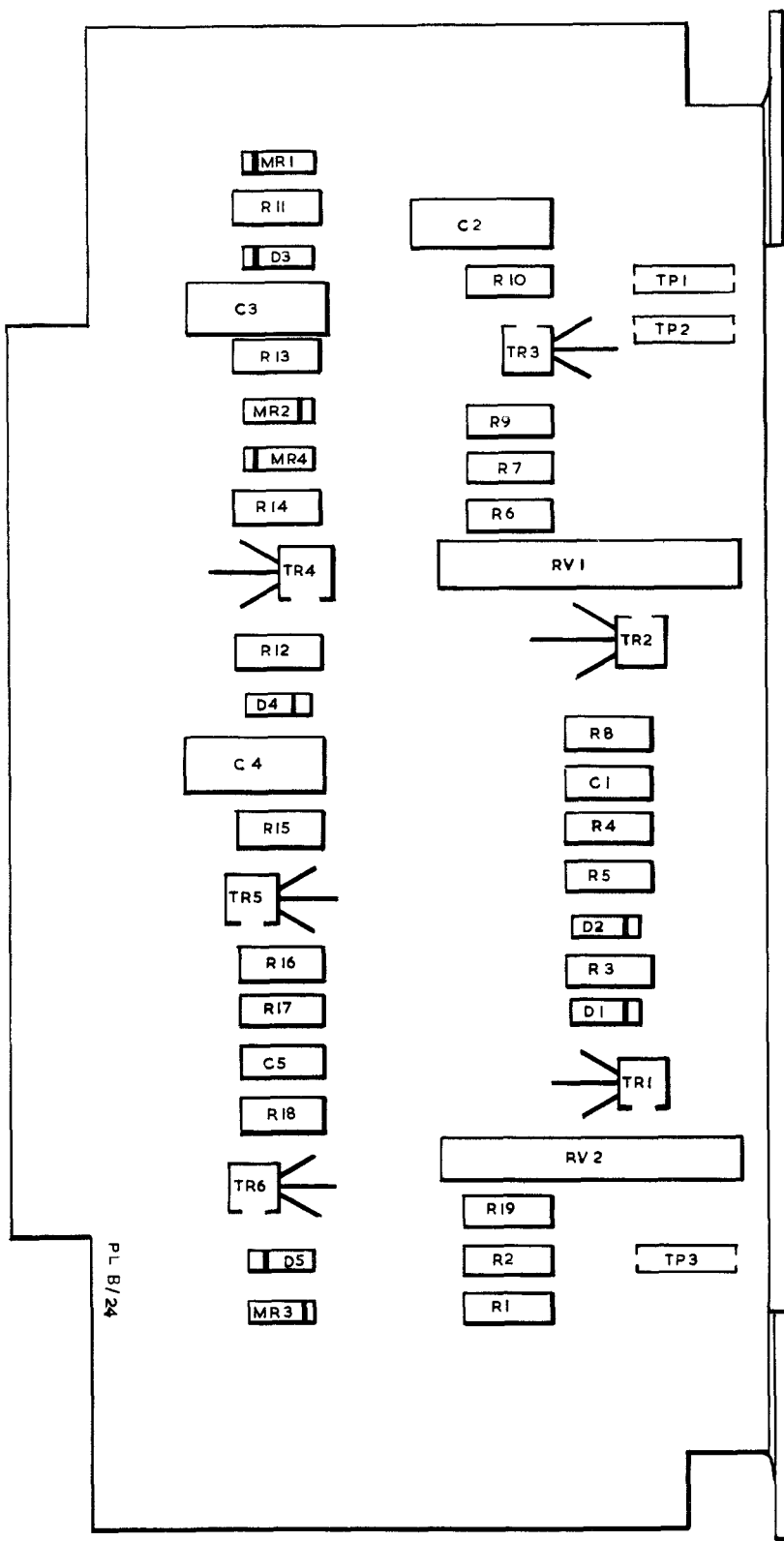
Protection against power supply failure

19. On both NBJA and NBJB boards the circuits are protected from power supply failure by diodes MR1 to MR4. These diodes prevent the line to a supply which has failed being driven into reverse polarity by the other supplies. Under normal conditions all diodes are back-biased, but should the +12V supply fail, the +12V line will be driven towards earth until it is arrested at +6V by MR1 conducting. Similarly MR2 and MR3 arrest the +6V and -6V lines at earth in the event of failure; MR4 arrests the -12V line at -6V.



Sampling gate generator boards (NBJA and NBJB)

Fig. 2

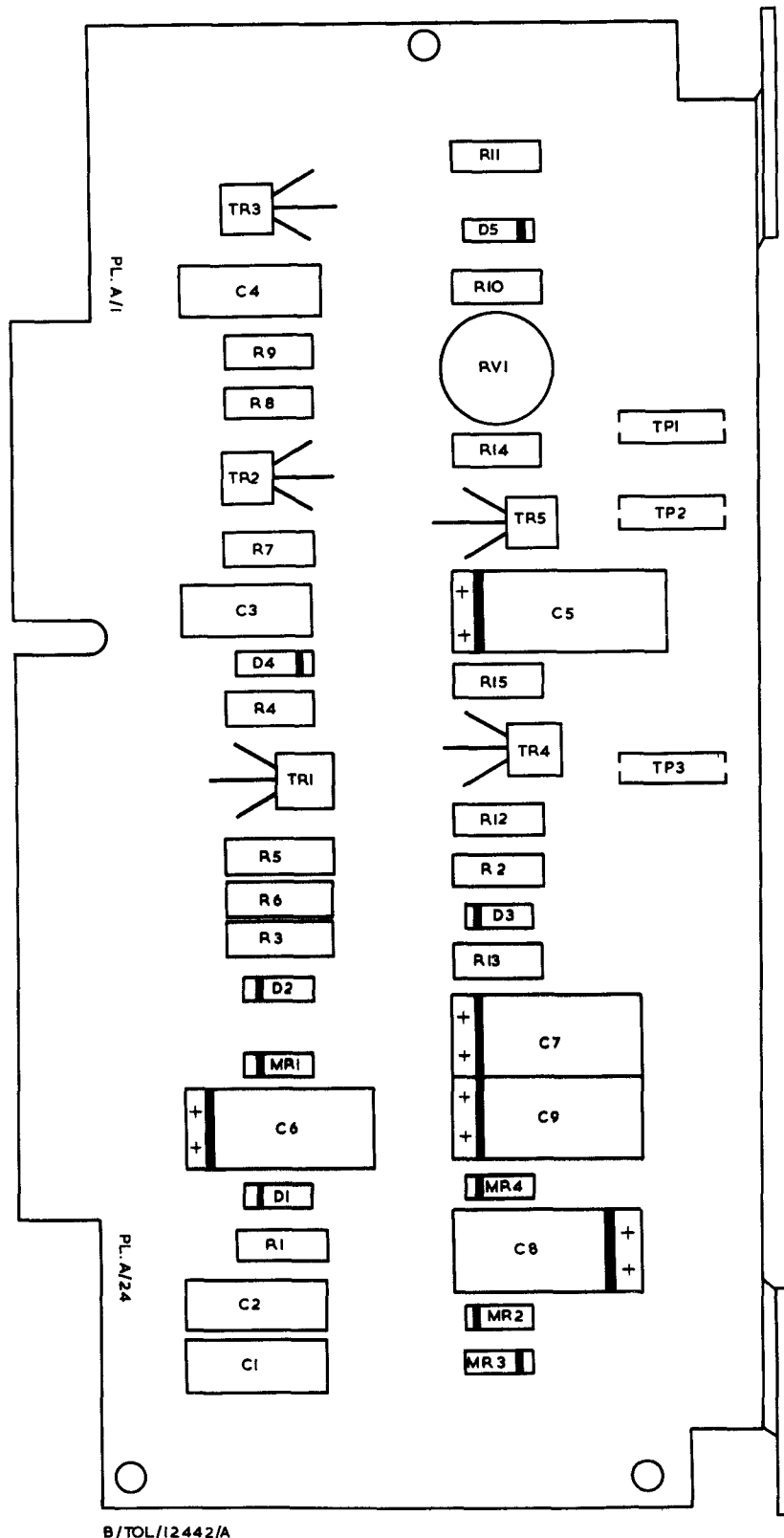


B/TOL/12443/A

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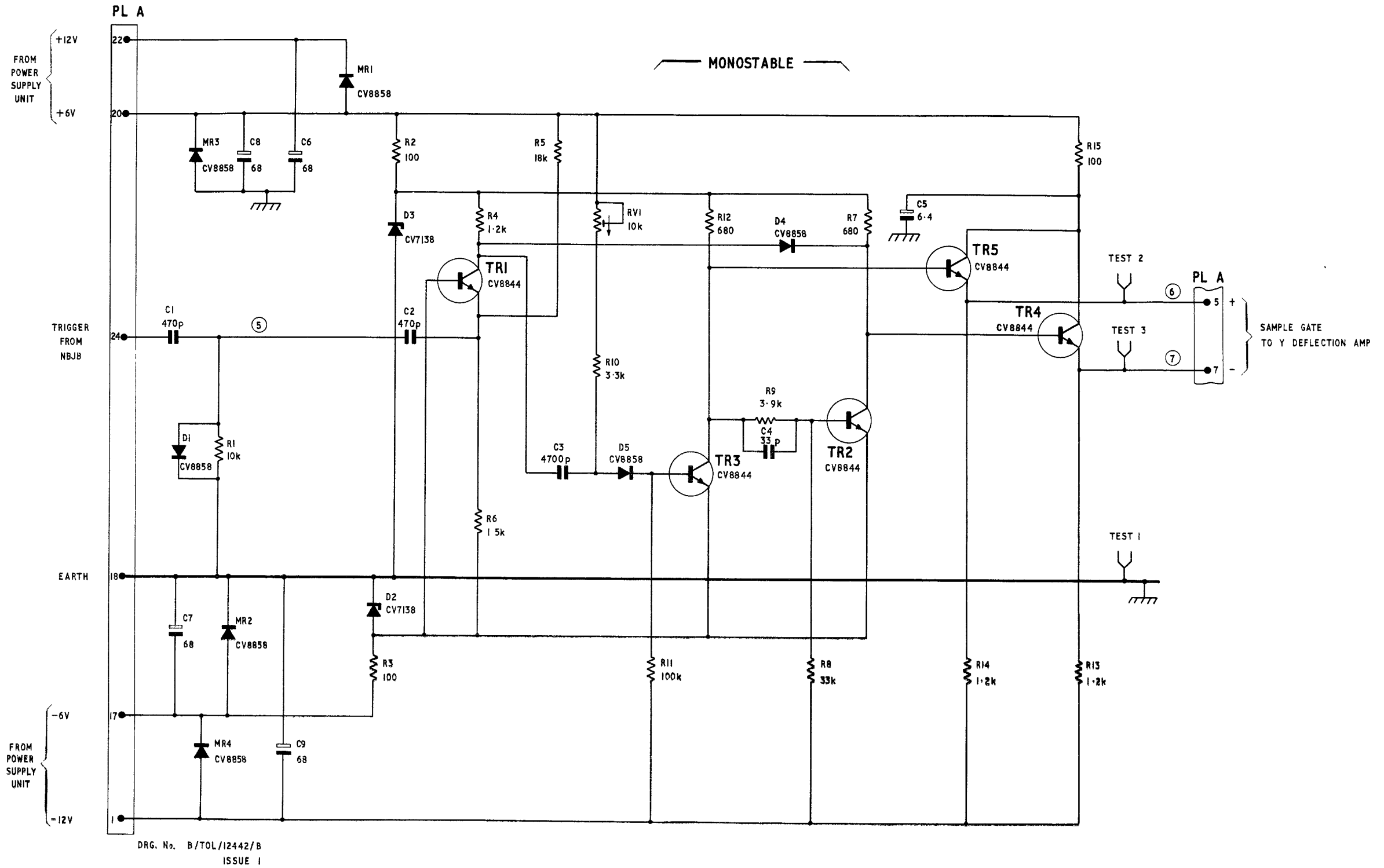
Sampling gate generator board NBJB (12443)
:component layout

Fig 3



B/TOL/12442/A

Sampling gate generator board NBJA (12442) :
component location



Sampling gate generator NBJA (I2442) ; circuit

Chapter 6

P. W. BOARDS NUE SERIES

CONTENTS

	Para.
Introduction	1
Circuit description	3

ILLUSTRATIONS

	Fig.
Scaling amplifier board NUEZ (12475): component location	1
Scaling amplifier board NUEZ (12475): circuit	2

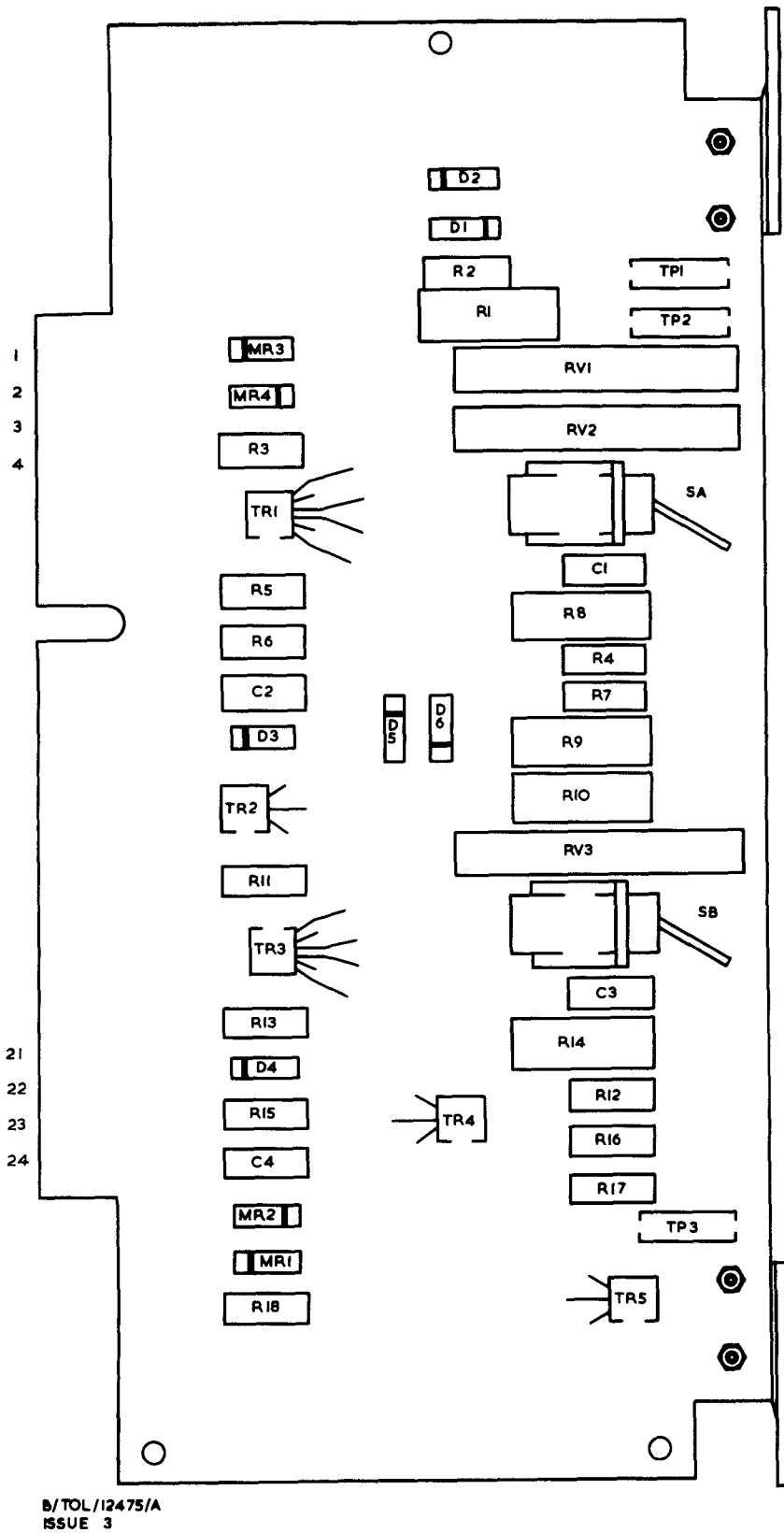
APPENDICES

	App.
Scaling amplifier board NUEA (12444)	1
Scaling amplifier board NUEC (12476)	2
Scaling amplifier board NUED (419/01572/001)	3
Scaling amplifier board NUEE (419/01572/002)	4

INTRODUCTION

1. Scaling amplifier board NUEZ is the basic height or range scaling board used in h. r. i. systems. The basic circuit comprises two operational amplifiers in cascade, each with its own feedback loop. The same basic circuit is used for all variants but to give the required gain different values are selected for components R1, R9 and RV2.

2. For details of variants of the basic board refer to the appendices following this chapter.

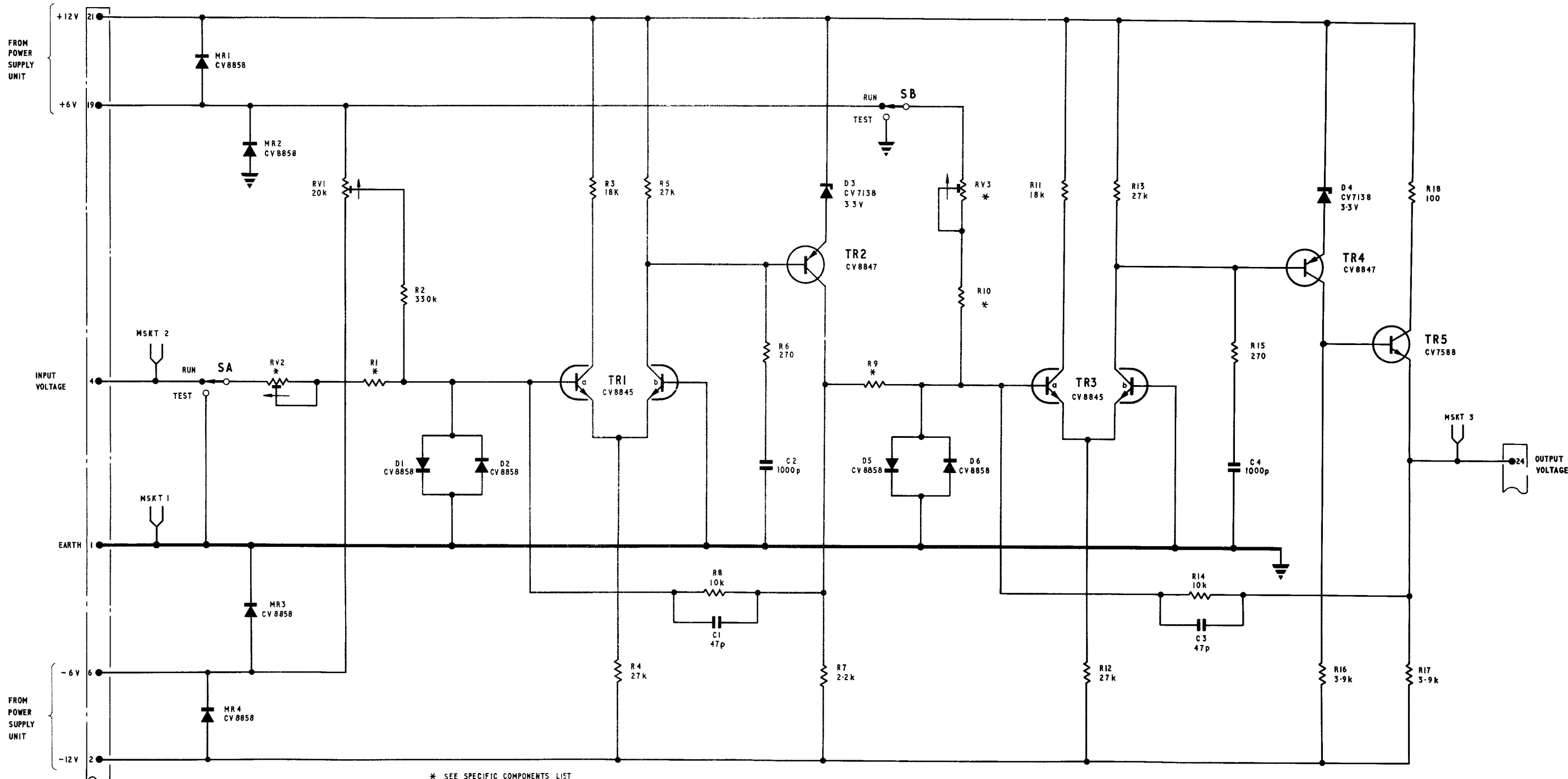


AL.26, Jan. 71 Scaling amplifier board NUEZ (12475): component location

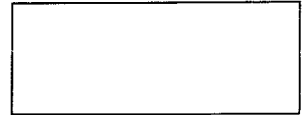
Fig.1

CIRCUIT DESCRIPTION (Fig. 2)

3. The input voltage enters the board on PLD4, and it is applied to long-tailed pair differential amplifier TR1 via test-run switch SA and input components RV2 and R1. Bias voltage to the base of TR1a is obtained from RV1 via R2. The potential excursions of TR1a base are limited to within $\pm 700\text{mV}$ by diodes D1 and D2. Preset control RV2 allows for small adjustments of amplifier gain whilst RV1 adjusts the balance of the long-tailed pair.
4. The potential at TR1b collector is an amplified, non-inverted version of the input voltage, and it is passed to the base of output drive transistor TR2. Circuit R6 and C2 prevents any tendency towards parasitic oscillation.
5. Over-all gain of the amplifier is determined by the ratio of feedback resistor R8 to the input resistance comprising R1 and RV2. Preset RV2 allows small adjustments of over-all gain to obtain the correct potential ratio between the input and the output at TR2 collector. Capacitor C1 shunts feedback resistor R8, improving the stability of the amplifier at the cut-off frequency.
6. The output from TR2 collector is passed to the second operational amplifier via R9. This second amplifier is similar to the first amplifier with the addition of an emitter-follower output stage (TR5). The output from TR5 emitter is fed out of the board via PLD24 and fed back to the amplifier input via feedback resistor R14. Selection of input resistor R9 determines the amplifier gain. The output of the amplifier can be offset negatively by putting switch SB to RUN and adjusting RV3.
7. Both of the operational amplifiers are of the inverting type, therefore the complete scaling amplifier is non-inverting.
8. The circuits on the board are protected from power supply failure by diodes MR1 to 4. These diodes prevent the line to a supply which has failed being driven in reverse polarity by the other supplies. In normal conditions all diodes are back-biased, but should the +12V supply fail the +12V line will be driven towards earth until it is arrested at +6V by MR1 conducting. Similarly MR2 and MR3 arrest the +6V and -6V lines at earth in the event of failure; MR4 arrests the -12V line at -6V.



* SEE SPECIFIC COMPONENTS LIST



B/TOL/12475/8 ISSUE 3

Scaling amplifier board NUEZ (12475) : circuit

Appendix 1

P.W. BOARD NUEA (12444)

5840-99-955-3884

P.W. board NUEA is a scaling amplifier and a variant of the basic board NUEZ (12475) with component values R1, R9 and RV2 selected to give the required gain. The amplifier output is -6V to 0V for an input of 0V to +50V.

SPECIFIC COMPONENTS LIST

Component	Value
R1	68kohm
R9	10kohm
R10	8.2kohm
RV2	20kohm
RV3	5kohm

Appendix 2

P.W. BOARD NUC (12476)

5840-99-955-3883

P.W. board NUC is a scaling amplifier. It is a variant of the basic board NUC (12475) with component values R1, R9 and RV2 selected to give the required gain. The amplifier output is -6V to +6V for an input of 0V to +6V.

SPECIFIC COMPONENTS LIST

Component	Value
R1	8.2kohm
R9	4.7kohm
R10	8.2kohm
RV2	5kohm
RV3	5kohm

Appendix 3

P.W. BOARD NUED (419/01572/001)

5840-99-222-7521

P.W. board NUED is a scaling amplifier. It is a variant of basic board NUEZ (12475) with component values R1, R9 and RV2 selected to give the required gain. The amplifier output is -6V to 0V for an input of -6V to +6V.

SPECIFIC COMPONENTS LIST

Component	Value
R1	8.2kohm
R9	20kohm
R10	15kohm
RV2	5kohm
RV3	10kohm

Appendix 4

P.W. BOARD NUEE (419/01572/002)

5840-99-223-0597

P.W. board NUEE is a scaling amplifier. It is a variant of basic board NUEZ (12475) with component values R1, R9 and RV2 selected to give the required gain. The amplifier output is -6V to +6V for an input of 0V to +6V.

SPECIFIC COMPONENTS LIST

Components	Value
R1	8.2kohm
R9	4.7kohm
R10a	10kohm
R10b	180kohm
RV2	1kohm
RV3	1kohm

Note....

R10a and R10b are connected in parallel in place of R10

Chapter 7

P. W. BOARDS NQP SERIES

NQPA 5840-99-223-0596
NQP B

CONTENTS

	Para.
Introduction	1
Rate prediction board NQPA (01623)	
Outline of operation	4
Circuit description	6
Differential detector board NQP B (01843)	
Outline of operation	12
Circuit description	15

ILLUSTRATIONS

	Fig.
Rate prediction board NQPA: theoretical waveforms ...	1
Rate prediction board NQPA: component location ...	2
Differential detector board NQP B: theoretical waveforms	3
Differential detector board NQP B: component location ...	4
Rate prediction board NQPA: circuit	5
Differential detector board NQP B: circuit	6

INTRODUCTION

1. The NQP series of boards are used in some h.r.i. applications to produce outputs that correspond with certain aerial conditions.
2. Rate prediction board NQPA senses the direction of nutation of the aerial and gives an output of +6V when the aerial sweeps upwards and -6V when it sweeps downwards. A second output of opposite polarity is available. In general, however, only one of the outputs is used and its function is to control the amplitude of the Y deflection scan drive waveform. This deflection waveform amplitude varies with the aerial resolver output which comprises a sinusoidal waveform varying in amplitude

with aerial elevation. Since the resolver waveform is sampled only during peaks, some control is necessary in the intervals between peaks when the Y deflection scan waveform must either rise or fall linearly.

3. Differential detector board NQPB senses the direction of aerial nutation and senses when the aerial elevation is zero degrees or below. When the aerial sweeps downwards an output from the board energizes a relay in the Viewing Unit Junction Unit which prevents the display of elevation markers. At aerial elevations of zero degrees and below a further output energizes a second relay in the Viewing Unit Junction Unit which disconnects the radar video from the display. This second relay is also energized via the circuits on board NQPB when a slew blanking signal is present.

RATE PREDICTION BOARD NQPA (01623)

Outline of operation

4. The triangular waveform from the demodulator is applied to the rate prediction board. This waveform rises positively during upward sweeps of the aerial and falls towards zero level during downward sweeps. It is filtered to remove ripple content and differentiated to give a waveform proportional to rate of change of amplitude before being applied to an integrated circuit amplifier. The polarity of the amplifier output controls the switching of a complementary symmetry transistor pair, and thus controls the polarity of the positive turn round gate 6V output terminal. In turn, this pair controls the switching of a second complementary transistor pair and the polarity of the negative turn round gate 6V output terminal.

5. The output from the negative turn round gate terminal is usually the only one used, but the positive turn round gate terminal output is available for certain applications.

Circuit description (Fig. 1 and 5)

6. The demodulated triangular waveform enters the board on terminals 10 and 1 (earth), ripples due to the synchro resolver excitation supply being removed by a filter comprising R2, R4, R5 and C2, C4, C5. The smoothed input is differentiated by C6 and R6 resulting in a current waveform which passes through zero level at the instant the demodulator output attains its maximum positive amplitude. The differentiated signal therefore changes polarity at the instant the heightfinder aerial changes its direction of nutation.

7. This differentiated waveform is applied to the input (pin 2) of a high gain integrated circuit amplifier (ML1). Capacitors C7 and C8 ensure that the amplifier has the required characteristics. A voltage from the preset potentiometer RV1 is applied to the amplifier non-inverting input (pin 3), and this is adjusted until the voltages at the output terminals of the board reverse polarity at the instant when the amplifier input passes through zero level.

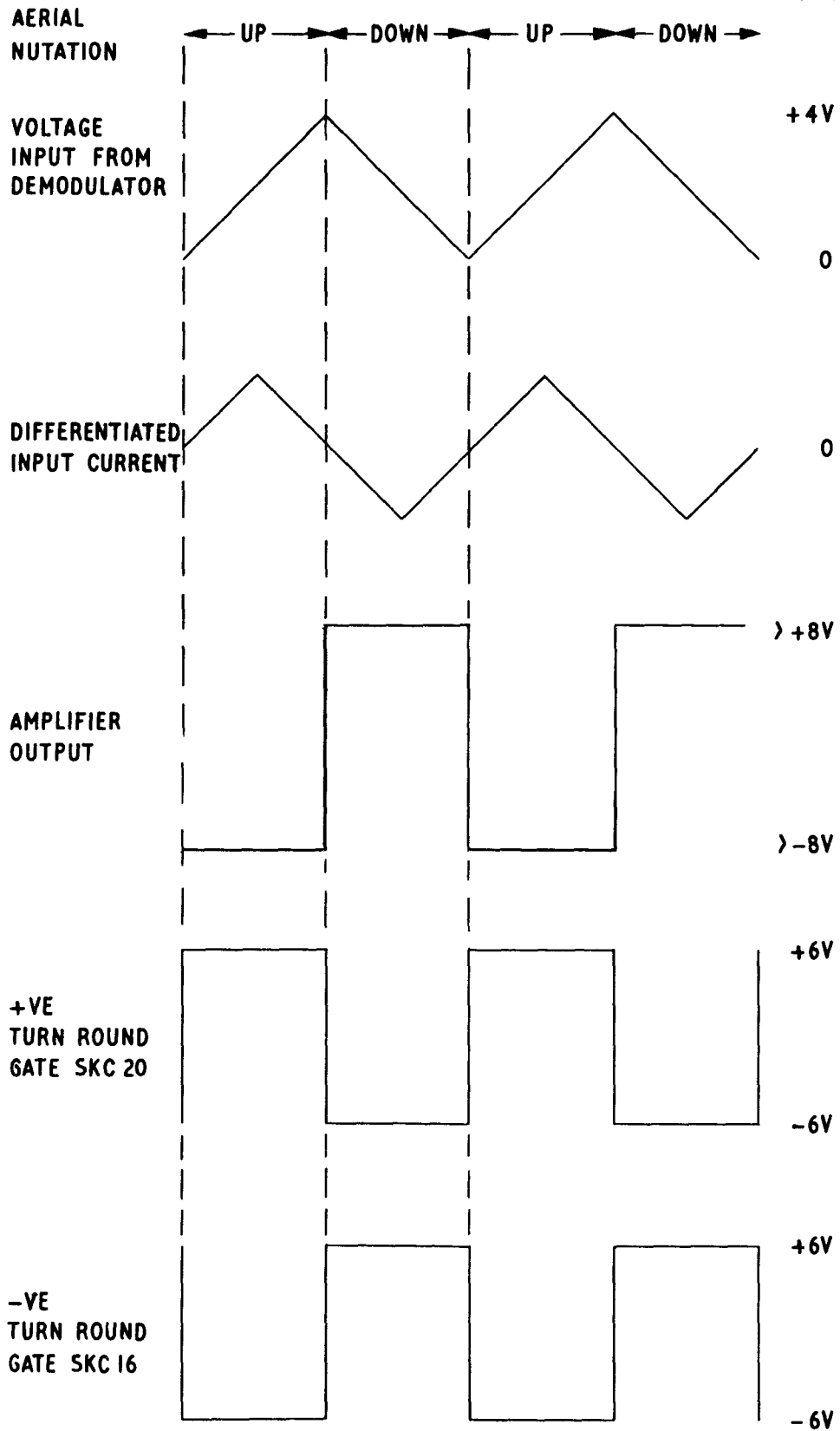


Fig. 1. Rate prediction board NQPA: theoretical waveforms

8. The output of the amplifier is approximately -8V when pin 2 of the amplifier is positive with respect to pin 3, and hard over to approximately +8V when pin 2 is negative with respect to pin 3. This output is fed via R9 and C9 (a low-pass filter preventing tendency towards parasitic oscillation) to the junction of R10 and R11, and provides base drive for transistors TR1 and TR2. These transistors are p-n-p and n-p-n types respectively and form the first complementary pair controlling the switching of the positive turn round gate (terminal 20) connected to the collector common lead.

9. When the aerial sweeps upwards the demodulator waveform at terminal 10 rises positively, the differentiated waveform to the input pin of the amplifier is positive and the amplifier output is -8V approximately. This negative output drives the first complementary pair of transistors and turns on TR1, thus switching the +6V emitter supply to the positive turn round gate (terminal 20) via R19. Transistor TR2 is cut off and therefore inoperative. The positive potential on the common collectors of TR1 and TR2 is applied to the junction of R13 and R14, driving the bases of TR3 and TR4. These transistors form a second complementary pair and control the switching of the negative turn round gate (terminal 16) connected to the collectors via R17. The positive potential on TR4 base brings this transistor into conduction, switching the -6V supply to the negative turn round gate (terminal 16). Transistor TR4 remains cut off by the positive potential on its base.

10. At the instant the aerial changes direction and starts its downward sweep the demodulator waveform starts its fall towards zero and the differentiated input to the amplifier changes polarity. The amplifier output swings to +8V approximately, TR1 is now cut off and TR2 turned on, i.e. the previous conditions are reversed. The -6V supply is now switched to the positive turn round gate (terminal 20). Similarly, the junction of R13, R14 is now negative, thus TR3 is turned on and TR4 cut off to switch the +6V supply to the negative turn round gate (terminal 16).

11. The polarities of both turn round gates are therefore reversed by a change in direction of aerial nutation.

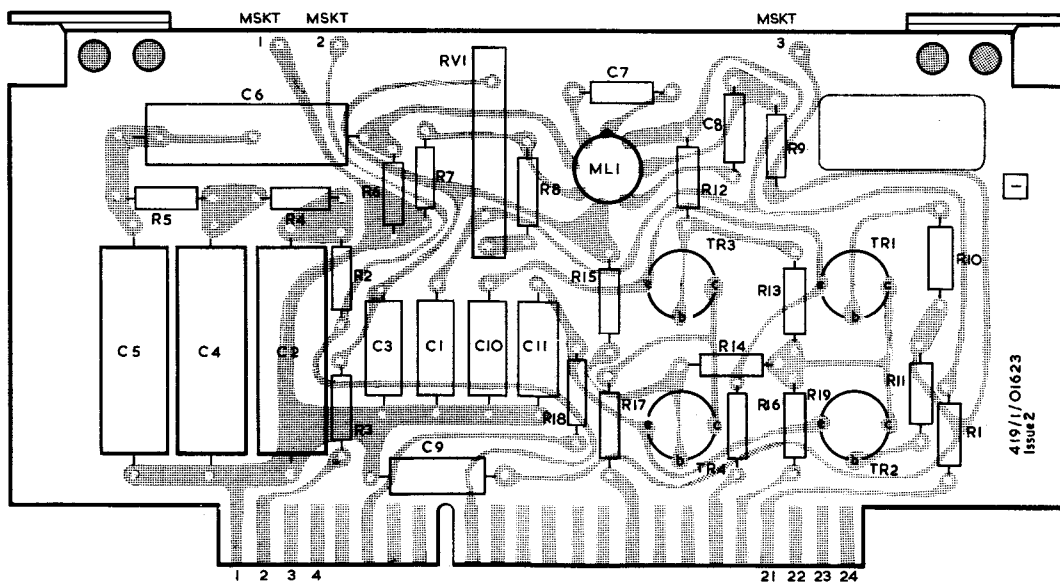


Fig. 2. Rate prediction board NQPA: component location

DIFFERENTIAL DETECTOR BOARD NQPB (01843)

Outline of operation

12. The input to the board is a triangular waveform from the demodulator which rises in a positive direction during upward sweeps of the aerial and falls during downward sweeps. This waveform is filtered to remove any ripple content and applied to two integrated circuit amplifiers.

13. Before entering the first amplifier the filtered waveform is differentiated to give an input proportional to the rate of change of demodulator waveform. The resulting amplifier output drives a transistor into conduction when the aerial sweeps downwards and cuts it off when it sweeps upwards. This transistor controls a relay in the Viewing Unit Junction Unit which inhibits elevation markers when it is energized.

14. The filtered waveform enters the second amplifier via a d.c. coupling network, and the amplifier output drives a transistor into conduction if the aerial is at or below zero degrees. The same transistor is also driven into conduction when a slew blanking input is present. A relay in the Viewing Unit Junction Unit is energized whenever the transistor conducts and the radar video is inhibited from the display.

Circuit description (Fig. 3 and 6)

15. The demodulated waveform is triangular and enters the board on terminals 10 and 1. Ripples due to the synchro resolver excitation supply are removed by the filter circuit R11, R15, R16 and C1, C2, C3. The smoothed input waveform is passed to the amplifier ML1 via the differentiating network C12 and R14 and to amplifier ML2 via the d.c. path R2 and link 1. Both ML1 and ML2 are high gain integrated circuit amplifiers.

16. The differentiated input to ML1 results in a current waveform which passes through zero level when the input triangular waveform attains its maximum positive amplitude. The differentiated signal therefore changes polarity at the instant the heightfinder aerial changes its direction of nutation. This input is fed to pin 2 of the amplifier and a reference voltage obtained from RV1 is fed to pin 3 via the network R17 and R18. Control RV1 is preset to give a zero output under static conditions, and capacitors C10 and C11 provide the desired amplifier characteristics.

17. The output of amplifier ML1 swings hard over to approximately -8V when pin 2 is positive with respect to pin 3, driving TR2 into the 'hard off' condition. Amplifier ML1 output remains at -8V as long as the input is positive. When the demodulated waveform input starts to fall pin 2 of ML1 is driven negative and the output swings hardover to +8V approximately, driving TR2 into conduction.

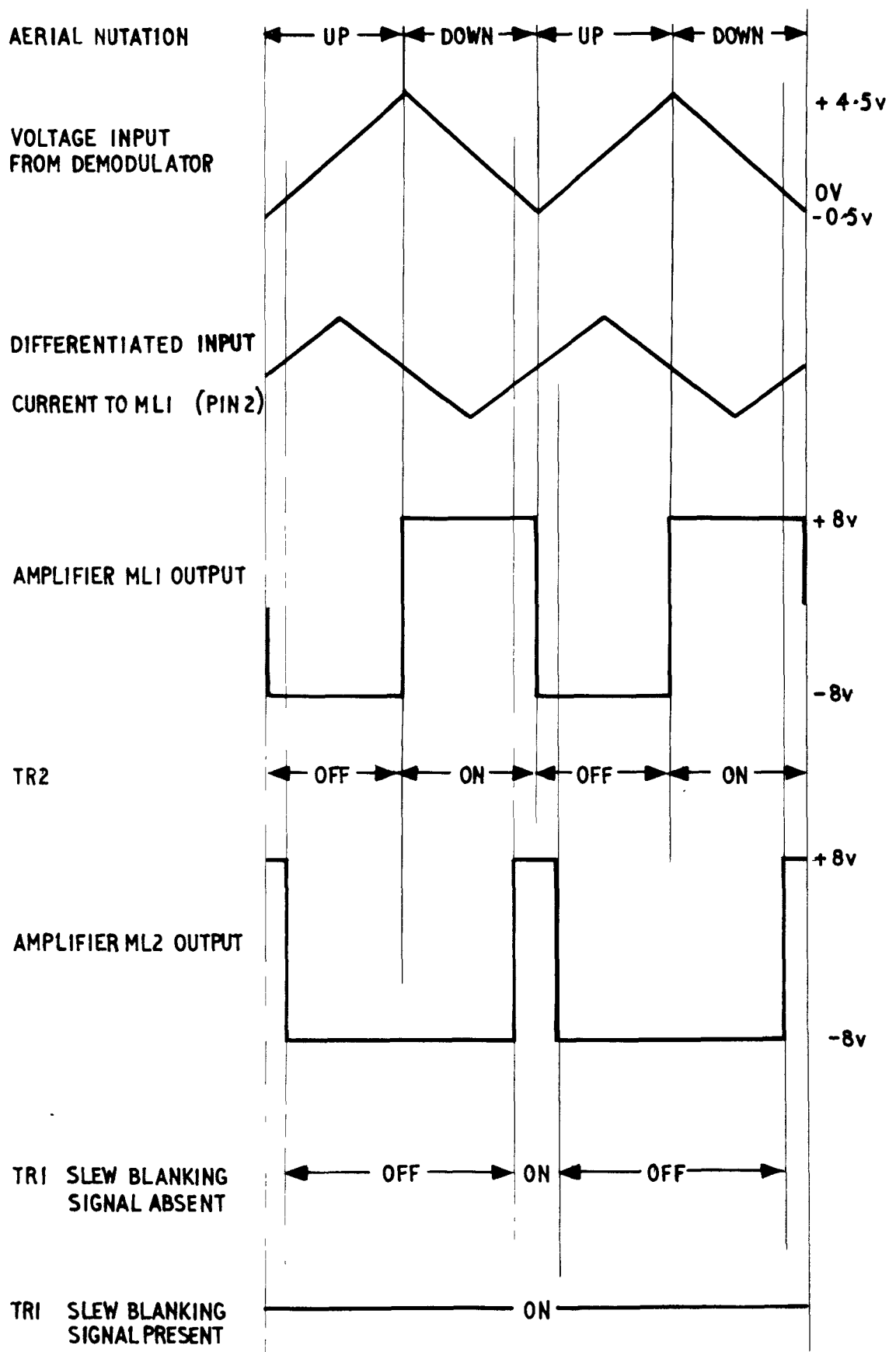


Fig. 3. Differential detector board NQPB: theoretical waveforms

12. If the computer output is the data to be displayed as a marker symbol, the track label/marker symbol bit will be a '0' and the inverter will produce a '1' input to the NAND gate. With the positive-going mainscan switch waveform also present, the NAND gate will produce a negative-going output which is then fed from the board as the symbol switch waveform and subsequently used by the video board MFKB.
13. The symbol switch waveform also triggers the symbol generator circuit which produces the symbol waveform. This is applied to a 90° phase shift network and fed out of the board in sine and cosine form. These waveforms are then routed to the X and Y deflection boards MRMC.
14. The brilliance gate waveform is produced in the following manner. The mainscan start pulse is routed from the m. g. t. cabinet and fed to an inverter stage, the output of which is used to set the brilliance gate bistable. The bistable remains in this state until the mainscan end pulse resets it. The resultant square waveform will be the mainscan brilliance gate waveform which forms part of the composite brilliance gate waveform.
15. The fastscan start pulse now enters the board from the m. g. t. cabinet and is applied via an inverter as one input of a NAND gate. If fastscan data is to be seen on the display, a console address supervisory bit will also be routed from the m. g. t. cabinet to this board. This bit will be applied as input to the second arm of the NAND gate. The resultant output is used to set the brilliance gate bistable for the fastscan period. At the end of this period, a fastscan end pulse is fed out by the m. g. t. cabinet and used to reset the brilliance gate bistable.
16. It will be seen that the brilliance gate waveform comprises two components, the mainscan brilliance waveform and/or the fastscan brilliance waveform. This composite waveform is applied to an AND gate, which receives a second input from the c. r. t. protection circuit.
17. The c. r. t. protection circuit comprises a NOR gate which receives two inputs each derived from a set of X and Y mainscan deflection waveforms. The first set are the inputs to the X and Y deflection boards and are fed to an OR gate which, if all waveforms are present, produces a negative output level which is fed as input to one side of the NOR gate.
18. The second set of deflection waveforms are tapped from the outputs of the four channels of the final coil deflection amplifiers, and are applied to an OR gate and rectifier circuit. A negative level output is produced and fed as the second input of the NOR gate. The resultant output from this NOR gate is used to enable the brilliance gate waveform NAND gate. Should either of these sets of waveforms fail the output of the brilliance NAND gate will be inhibited, thus presenting no picture on the tube face.

18. The d.c. input to ML2 follows the demodulated waveform input, and when pin 2 is driven more positive than pin 3 the amplifier output swings hard negative to approximately -8V. It will remain at this negative potential as long as the input is positive with respect to pin 3, but when the input is negative the amplifier output swings hard positive to approximately +8V.

19. Capacitors C4 and C7 provide the desired amplifier characteristics. Diodes D1 and D2 prevent the voltage excursions between pins 2 and 3 or ML2 from exceeding +700mV. Control RV2 provides a reference voltage to pin 3 and it is preset to give a zero output under static conditions.

20. The output from ML2 is passed to TR1 base via the network R6, C8, R5 and diode D4. The network R6, C8 is a low-pass filter which eliminates tendencies towards parasitic oscillation, R5 limits the base current of TR1 and D4 inhibits the negative-going waveform from reaching TR1 base. When the output waveform from ML2 is positive, however, D4 conducts and TR1 is turned hard on.

21. A second input is applied to TR1 base. This is a voltage which comes into the board on terminal 23 and is at +12V when the slew blanking signal is present and at 0V in the absence of slew blanking. With a 0V input diode D3 is non-conducting and in no way affects the input to TR1 base from amplifier ML2. However, with a +12V input to terminal 23 diode D3 conducts and TR1 is turned hard on.

22. The +12V and -12V supplies coming into the board via terminals 21 and 2 are decoupled by network R3, C5 and network R8, C6 before application to the circuits on the board.

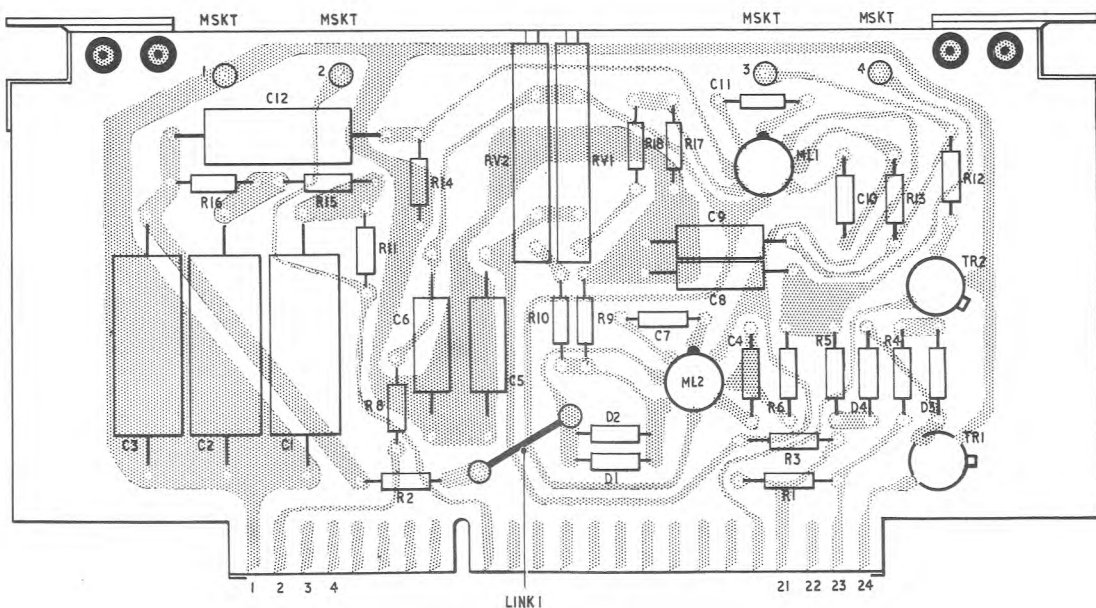
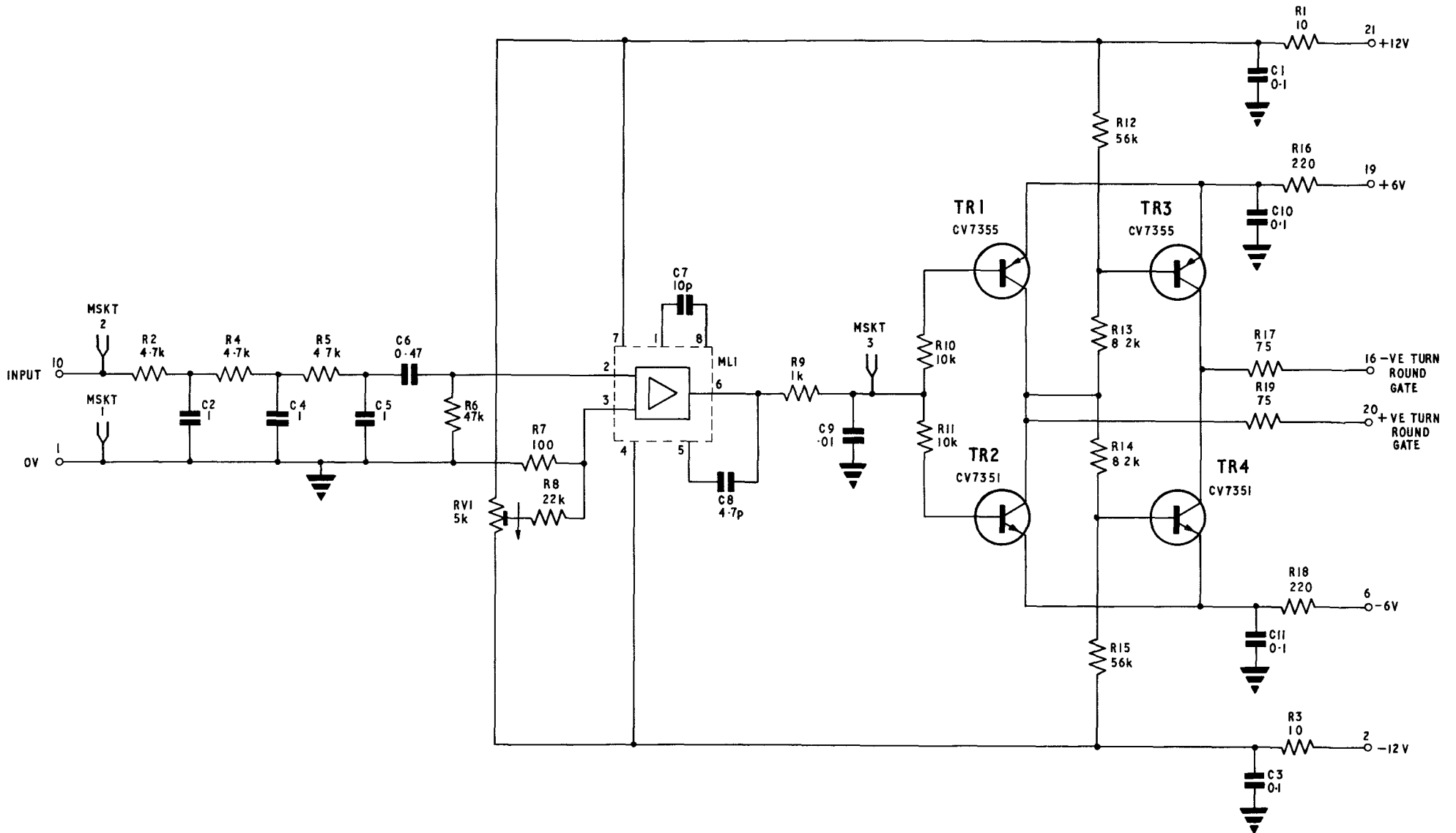


Fig. 4. Differential detector board NQP B: component location



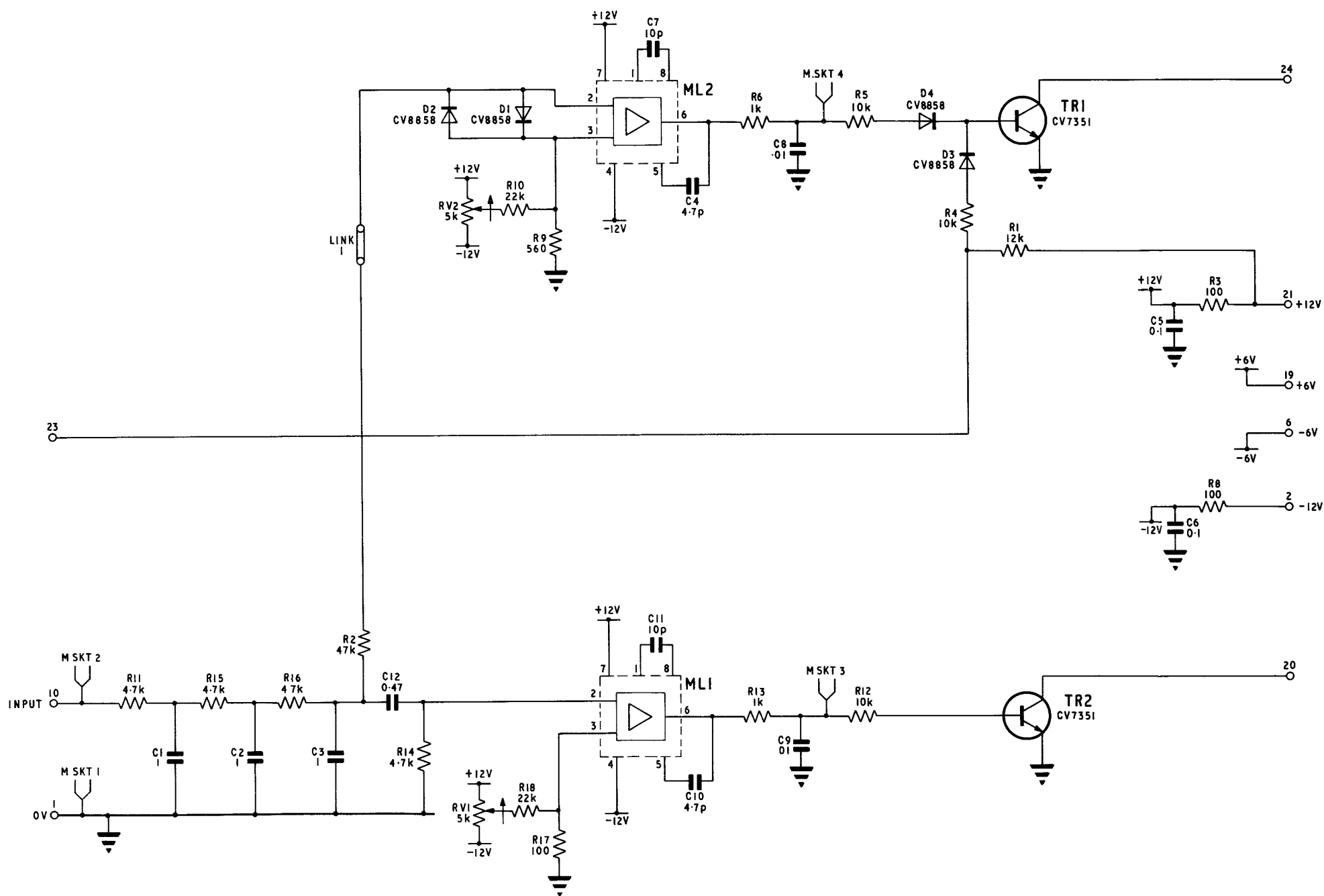


Fig. 6
A.L. 26, Jan. 71

Differential detector board NQPB:circuit

Fig. 6

Chapter 8

P. W. BOARD: NUJ SERIES

CONTENTS

	Para.
Introduction	1
Circuit description	3

ILLUSTRATIONS

	Fig.
P. W. board NUJZ: component location	1
P. W. board NUJZ: circuit	2

APPENDICES

	App.
P. W. board NUJC (419/01673/003)	1
P. W. board NUJD (419/01673/004)	2

INTRODUCTION

1. The NUJ series of P. W. boards are used for height scaling in h. r. i. systems. The basic circuit comprises an inverting operational amplifier with feedback loop. The same basic circuit is used for all variants, but to give the required gain different values are selected for components R1, R2, RV1 and RV2.

2. For details of variants of the basic board (NUJZ) refer to the appendices following this chapter.

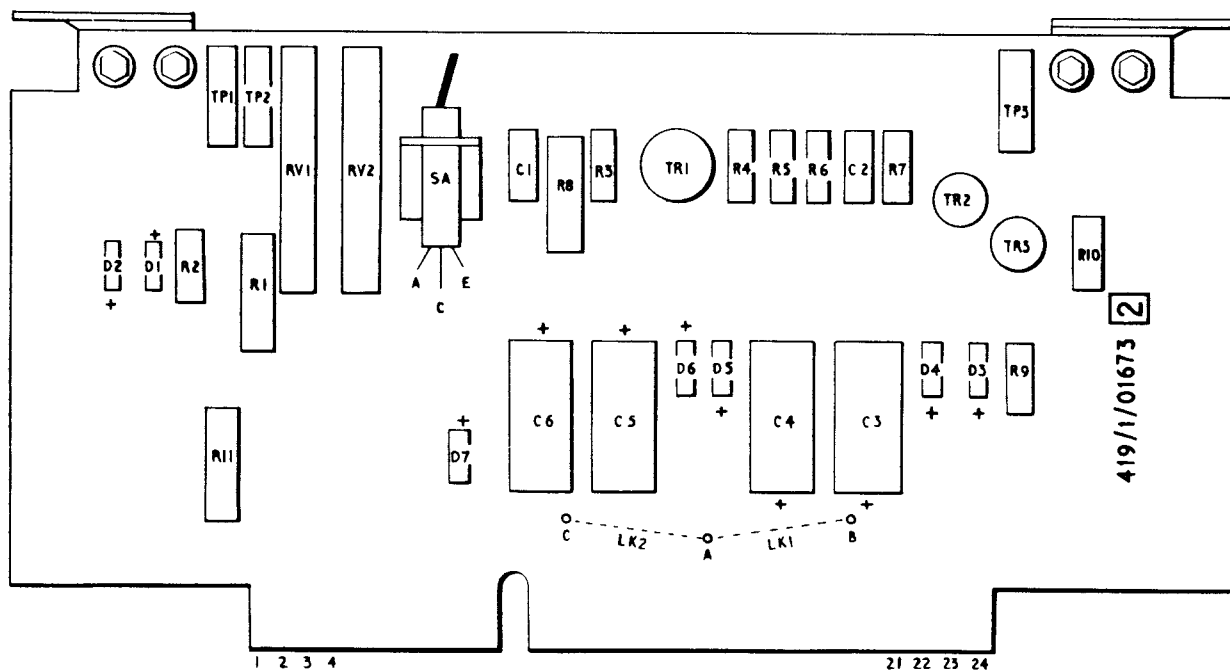
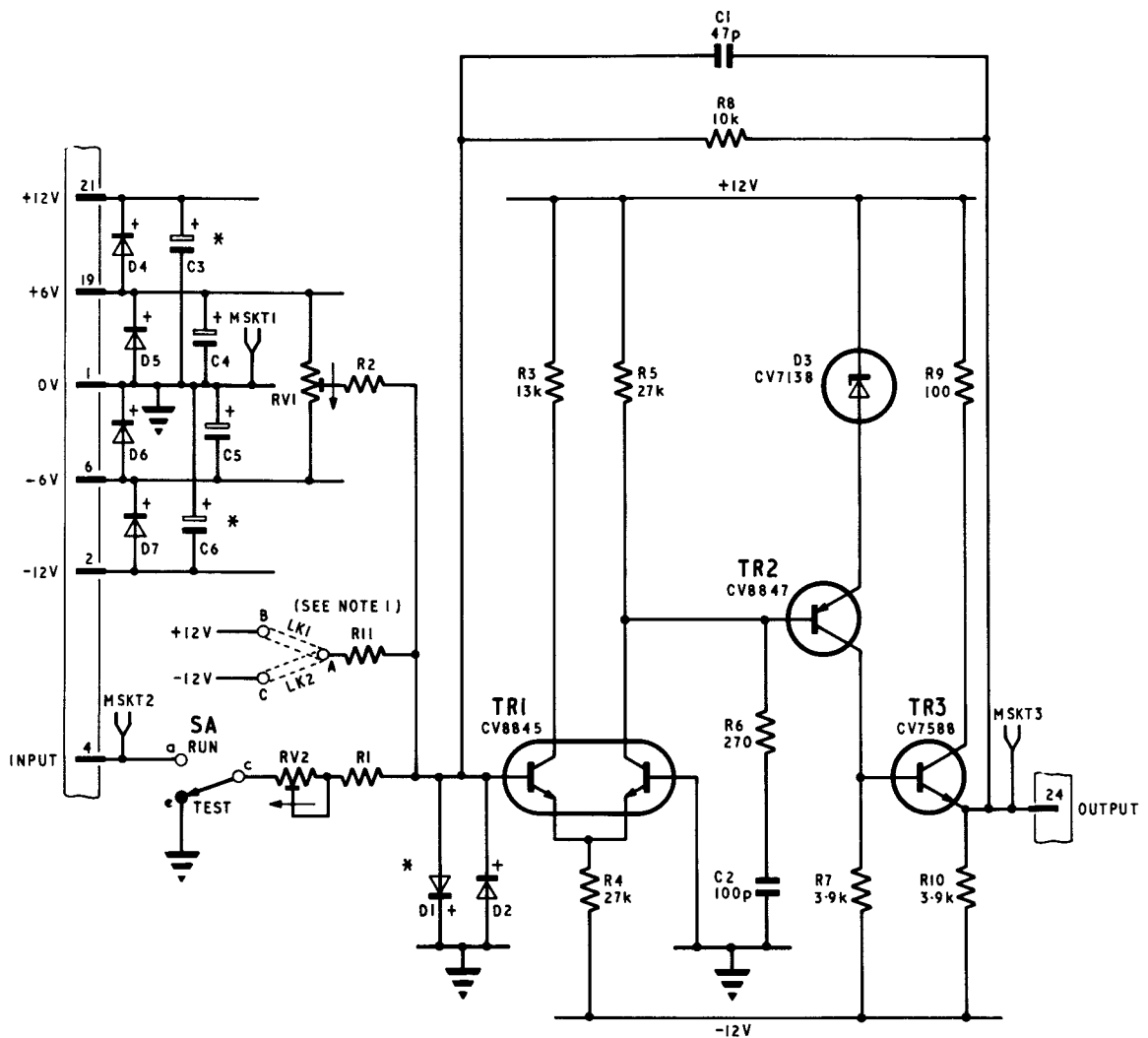


Fig. 1. P.W. board NUJZ: component location

CIRCUIT DESCRIPTION (Fig. 2)

3. The input voltage enters the board on terminal 4, and it is applied to the long-tailed pair differential amplifier TR1 via test-run switch SA and input components RV2 and R1. Bias voltage to the base of TR1a is obtained from RV1 via R2. The potential excursions of TR1a are limited to within $\pm 700\text{mV}$ by diodes D1 and D2. Preset control RV2 allows for small adjustments of amplifier gain whilst RV1 adjusts the balance of the long-tailed pair.
4. The potential at TR1b collector is an amplified, non-inverted version of the input voltage, and this is passed to the base of output drive transistor TR2. The circuit comprising R6 and C2 prevent any tendency towards parasitic oscillation.
5. Over-all gain of the amplifier is determined by the ratio of feedback resistor R8 to the input resistance comprising R1 and RV2. Preset RV2 allows small adjustments of over-all gain to obtain the correct potential ratio between the input and the output at TR3 emitter. Capacitor C1 shunts the feedback resistor .
6. The circuits on the board are protected from power supply failure by diodes D4 to 7. These diodes prevent the line to a supply which has failed being driven in reverse polarity by the other supplies. In normal conditions all diodes are back-biased, but should the +12V supply fail the +12V line will be driven towards earth until it is arrested at +6V by D4 conducting. Similarly D5 and D6 arrest the +6V and -6V lines at earth in the event of failure; D7 arrests the -12V line at -6V.



NOTES:-

- 1 LINKS AND R11 ARE SPECIFIC COMPONENTS WHICH ARE NOT USED IN SOME VARIANTS
- 2 * ALL DIODES EXCEPT D3 ARE CV8858
C3,C4,C5 AND C6 ARE ALL 68μF

Appendix 1

P. W. BOARD NUJC (419/01673/003)

5840-99-115-2249

P. W. board NUJC contains a scaling amplifier which is a variant of the basic scaling amplifier on board NUJZ, with component values R1, R2, RV1 and RV2 selected to give the required gain. The amplifier output is 0V to +6.3V for an input of 0V to -12V.

SPECIFIC COMPONENTS LIST

Component	Value
R1	18kohm
R2	470kohm
RV1	10kohm
RV2	2kohm

Appendix 2

P. W. BOARD NUJD (419/01673/004)

5840-99-115-2248

P. W. board NUJD contains a scaling amplifier which is a variant of the basic scaling amplifier on board NUJZ, with component values R1, R2, RV1 and RV2 selected to give the required gain. The amplifier output is 0V to -5V for an input of 0V to +6.3V.

SPECIFIC COMPONENTS LIST

Component	Value
R1	12kohm
R2	470kohm
RV1	10kohm
RV2	1kohm

Chapter 9

CATEGORY SELECTION BOARDS (MJS SERIES)

LIST OF CONTENTS

	Para.
Introduction	1
Mechanical construction	4
Outline of working	7
Detailed description	
Mainscan switch waveform generation	19
Character switch waveform generation	21
Pointer symbol generation	22
Brilliance gate waveform generation	30
CRT protection circuit	36
Transistor protection circuits	41

LIST OF ILLUSTRATIONS

	Fig.
Category selection board type 12458 MJSB	1-6

INTRODUCTION

1. The category selection board receives and decodes all the necessary timing pulses or d. c. levels to enable it to generate a series of switch and gate waveforms which remotely control the video and deflection boards and the character drive unit, which in turn provide the scan and bright-up signals as required for the displays.
2. Before a detailed study of this board is made, it is emphasised that the reader should already be familiar with the outline of working of both the m. g. t. cabinet and the character generator cabinet.
3. The board is situated in position No. 2 of the board box contained in both the 12in and 21in labelled plan displays.

MECHANICAL CONSTRUCTION

4. The printed wiring boards are made of fibreglass and carry printed wiring on both sides of the board. Components are fitted to one side of the board only. Connections from the circuitry on the board are taken to a series of gold-plated edge connectors

on the bottom edge of the board. These connectors mate with sockets fitted to a connector plate at the bottom of the board box. The transistors on the board are fitted in metal clamps and are cooled by the circulating air in the board box which in turn is cooled by the oil circulating in the board box walls.

5. The boards are fitted vertically in the board box and held in position by a pair of clamps on the top corner of each board.

6. Each board carries a number of monitor points, test switches and preset potentiometers mounted on a strip attached to the top edge of the board. This strip also carries a handle to facilitate easy removal of the board. The test and setting-up facilities on the boards are accessible via the removable panel forming the top of the viewing unit.

OUTLINE OF WORKING

7. The board accepts the incoming timing pulses from the m. g. t. cabinet, which are the mainscan start and end pulses, the fastscan start and end pulses, the track label/symbol marker bit and the console address supervisory bit.

8. From these incoming pulses, the board generates the following waveforms:-

- (1) Mainscan switch waveform.
- (2) Character switch waveform.
- (3) Symbol switch waveform.
- (4) Symbol generation waveforms.
- (5) Brilliance gate waveform.

9. The mainscan switch waveform is produced by a bistable circuit which is set by the incoming fastscan end pulse and reset by the mainscan end pulse. The pulses are fed from the m. g. t. cabinet. The switch waveform, which is negative-going during the mainscan period, is fed out to the video board MFKB. During the fastscan periods the switch waveform is positive-going and is used to enable two NAND gates.

10. The first NAND gate accepts as its second input the track label bit (positive-going). When both inputs are positive the NAND gate produces the negative-going character switch waveform. This is routed out of the board for subsequent use in both the video board and the character drive unit.

11. The track label/marker symbol bit, which is routed to this board from the m. g. t. cabinet, is used to initiate the production of symbol switch waveforms and the symbol deflection waveforms. This is arranged by feeding the incoming bit to an inverting circuit which then feeds the second NAND gate.

DETAILED DESCRIPTION

Mainscan switch waveform generation

19. The incoming positive-going mainscan end pulse is applied via pin F20 to TR11, where it is inverted and applied to the base of TR14. Transistor TR14 and TR13, together form a bistable which changes state on application of either the mainscan or fastscan end pulses. The fastscan end pulse is applied to the board via pin E22 to inverter stage TR12 and fed to the base of TR13.

20. The output of this bistable which is taken from TR14 collector, will switch from +6V for $170\mu\text{s}$ to -6V for approximately $3050\mu\text{s}$ on application of the mainscan end and the fastscan end pulses respectively. This switch waveform is fed as input to three places.

- (1) Out of the board on pin F10 for subsequent use in the video board.
- (2) Via R69 as input to the character switch waveform circuits.
- (3) Via R68 as input to the symbol circuits.

Character switch waveform generation

21. During fastscan periods, the mainscan switch waveform is at a positive level and is applied via R69 to TR21 base. A second input, the track marker bit, is also applied to TR21 base via R70. The complete circuit forms a NAND gate requiring both positive inputs to be present at TR21 base to effect a negative-going output at the collector. This output switches from a +6V to a -6V level and is referred to as the character switch waveform. This waveform is fed out of the board on pin F9, where it is subsequently used in the video board and character drive unit.

Point symbol generation

22. The symbol switch and deflection waveforms are generated when no track marker bit is applied to the board. It will be seen, therefore, that with no track marker bit applied, TR22 collector will be approximately +6V. This level will be applied to TR20 base via R75, acting as one arm of the NAND gate formed by R68, R75 and TR20. The second input is the mainscan switch waveform (the positive level) applied via R68.

23. The inverted output of TR20 collector is fed from the board on pins F12 and F3 as the symbol switch waveform for subsequent use in the video board MFDH. With TEST/RUN switch SB in the RUN position, the switch waveform is applied via diode D32 to TR23 base.

24. If the output of TR20 is at the positive level, current flowing through RV2 and R80 is divided between the base/collector and base/emitter junction of transistor TR23, flowing through coil L1 to earth. The value of the current is adjusted by RV2, which has the effect of controlling the amplitude of oscillations when initiated.

25. When the output of TR20 goes negative, TR23 is cut-off and the energy stored in the L1 will cause oscillation in the circuit, L1, C26, C27. The base/emitter current of TR24 maintains the oscillations.

26. The gated output at 28kHz is taken from both the emitter and collector of TR24. Normally, these would be 180° out of phase, but with coil L2 connected in TR24 collector, a 90° phase shift will be produced resulting in a sine and a cosine output.

27. The collector output of TR24 is applied via the double emitter-follower stage formed by TR25, TR27 to the board output pin F14, as the symbol cosine waveform, being available for monitoring purposes at TEST POINT 15.

28. Similarly, the emitter output (the symbol sine waveform) of TR24 is applied via double emitter-follower stage TR26, TR28 to pin F15, being available at TEST POINT 16 for monitoring purposes.

29. It will be noted that TR25 and TR27 are connected between the +12V supply and earth, while TR26 and TR28 are connected between ±6V. This is to allow for the fact that when TR24 is producing no oscillatory output, the collector/emitter potentials are at +6V and earth respectively.

Brilliance gate waveform generation

30. The action of the circuit will produce either the mainscan brilliance gate only, or a composite waveform comprising the mainscan gate and the fastscan gate when the console address supervisory bit is present.

31. The mainscan brilliance gate is formed in the following manner. The positive-going mainscan start pulse is fed into the board via pin F23 to the base of TR15. Transistor TR15 inverts the pulse and applies it via D26 to set the bistable formed by TR18 and TR19. Diode D26 forms one arm of the OR gate D26-D27.

32. The bistable remains in this state until the onset of the mainscan end pulse. This pulse is fed into the board on pin F20, is inverted by TR11, and applied via D18 to reset the bistable at the end of the mainscan period. Diode D18 forms one arm of the OR gate D18-D19. The duration of the mainscan period is determined by printed wiring board LJLE in the m. g. t. cabinet, and is 3050μs.

33. If fastscan data is to be displayed, this bistable will also require to be set for the duration of the fastscan period. The fastscan start pulse occurs 90μs after the mainscan end pulse and is applied to pin E21. The pulse is applied as input to TR16 base forming part of NAND gate circuit TR16 - TR17, D24-D25. The application of the fastscan pulse alone to this circuit will not set the bistable.

34. To do this, a positive-going console address supervisory bit (from the m. g. t. cabinet) is applied as the second input to this circuit via pin E23 to the base of TR17. The resultant output of the NAND gate is negative-going and is fed to the bistable, setting it for the start of the fastscan scan period. The bistable will remain set until the application of the fastscan end pulse (i. e. $80\mu\text{s}$).

35. The fastscan end pulse is applied via input pin E22 to the base of TR12, the inverted output of which is fed via D19 (of the OR gate D18-D19) to the base of TR19, resetting the bistable. The output is taken from TR18 collector and fed to the NAND gate formed by R29-R30 and TR10, the second input of which is brought from the tube protection circuit. If both inputs are present, the brilliance gate waveform is negative-going and is fed via pin F21 (TEST POINT 2) to the video board.

CRT protection circuit

36. In the event of failure of the mainscan deflection waveforms, the circuit protects the tube from possible burning by blanking the spot which would otherwise remain at the tube origin. This circuit comprises two channels, one accepting as input the deflection waveforms from the outputs of the final deflection amplifiers, and the other accepting the X and Y scan waveforms as fed in from the m. g. t. cabinet.

37. The four outputs of the final deflection amplifiers are fed via input pins F16, F17, F19 and F22, to the combined OR gate and rectifier circuit D5-8. Zener diodes D1-D4 drop the level of the incoming positive-going waveforms by 3.3V to produce a resultant +12V level at R1, with all waveforms present. Capacitor C1 charges to this level. TR1 conducts heavily, resulting in TR2 conducting heavily, producing a -6V level at TEST POINT 11 and R26. Resistor R26 forms one input of the NOR gate formed by R25-R26 and TR9.

38. The X and Y scan are applied to the OR gate formed by diodes D9-D12, resulting in a positive level of approximately +5V at the base of emitter-follower TR3. R11, RV1 and C2 form an integrating circuit with C2 charging slowly. With an approximate +6V level at TR4 base a +6V level will appear at TR4 collector, being limited to a most negative level of +6V by D13. Zener diode D14 reduces this level by 5.6V which is then applied via D15 to emitter-follower TR6. The resultant earth level at TR7 base produces a +6V level at TR7 collector. This is inverted by TR8 applying a -6V level to TEST POINT 7 and R25 (the second input of NOR gate 1). With both inputs at -6V, TR9 collector is at +6V feeding one input, via TEST/RUN switch SA to NAND gate 2 formed by R29-R30 and TR10. The network D5, C3 and R16 is a hold-off circuit which in the event of failure of the mainscan w/f inputs, delays the application of the brilliance blanking gate for some 20ns.

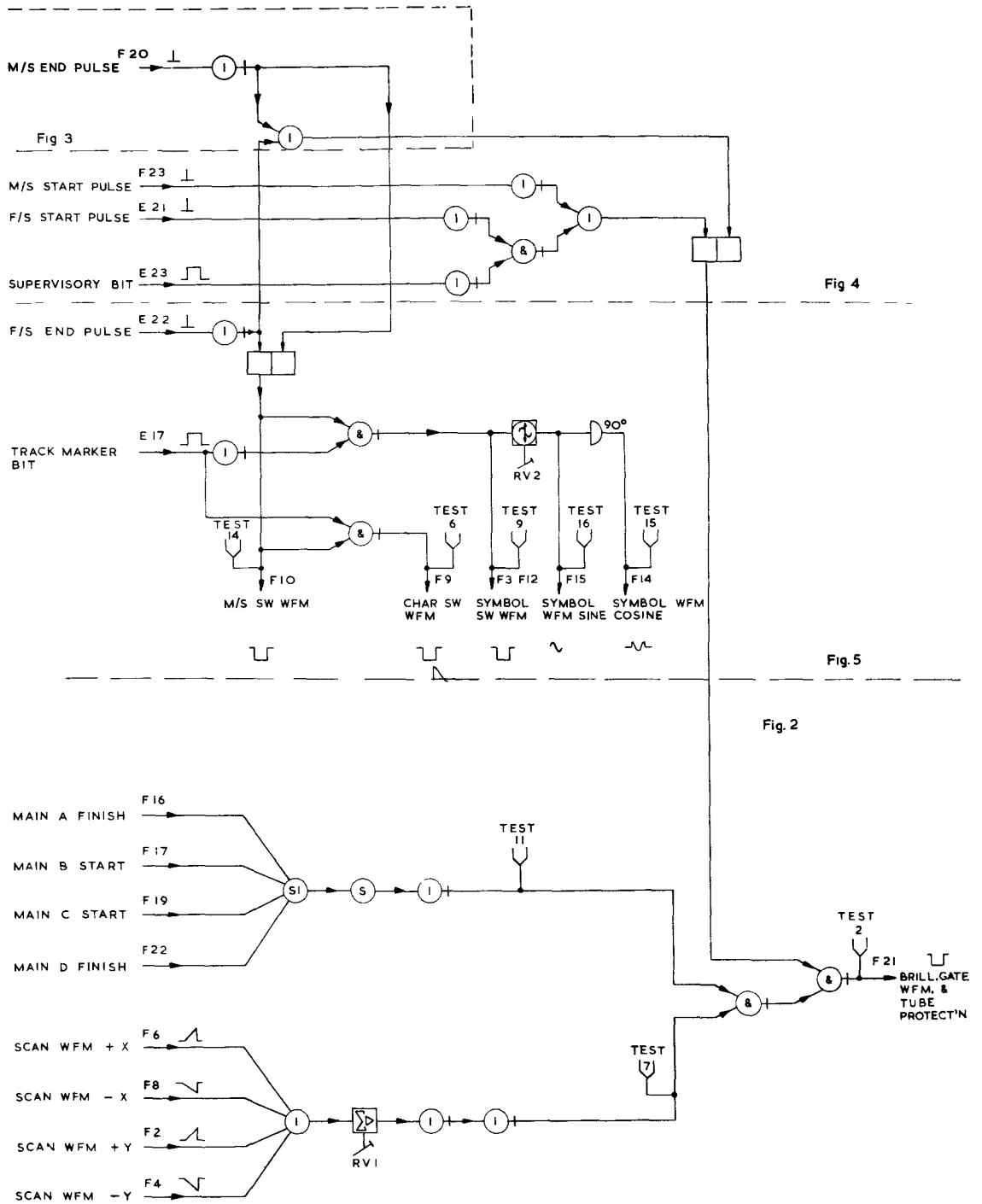
39. The second input to gate 2 is the brilliance gate waveform from TR18 collector, and when both inputs are at a positive level, the resultant output is negative at TEST POINT 2 and output pin F21. This waveform is applied to the brilliance channel of the video board.

40. If the composite mainscan waveform input fails, the c. r. t. will be blanked, but a condition could exist where only the mainscan component had failed and the fast-scan component was still present. The integrator circuit R11, RV1, C2 provides protection against this contingency. As the duration of the fastscan input is $170\mu\text{s}$ and the CR time of the integrating circuit is about 1ms, C2 will only charge to slightly above earth. TR4 collector will be at about +12V and a (positive) blanking waveform will be output from pin 21 to the c. r. t. brilliance circuits.

Transistor protection circuits

41. The board operates from four stabilised d. c. supplies provided by Power Unit Type 11600 in the 12in viewing unit and by Power Unit Type 11606 in the 21in viewing unit. These supplies are interconnected through the board circuits, and if a supply fails, the supply of the opposite polarity could attempt to drive a reverse current through certain transistors. A protection circuit is included to prevent this.

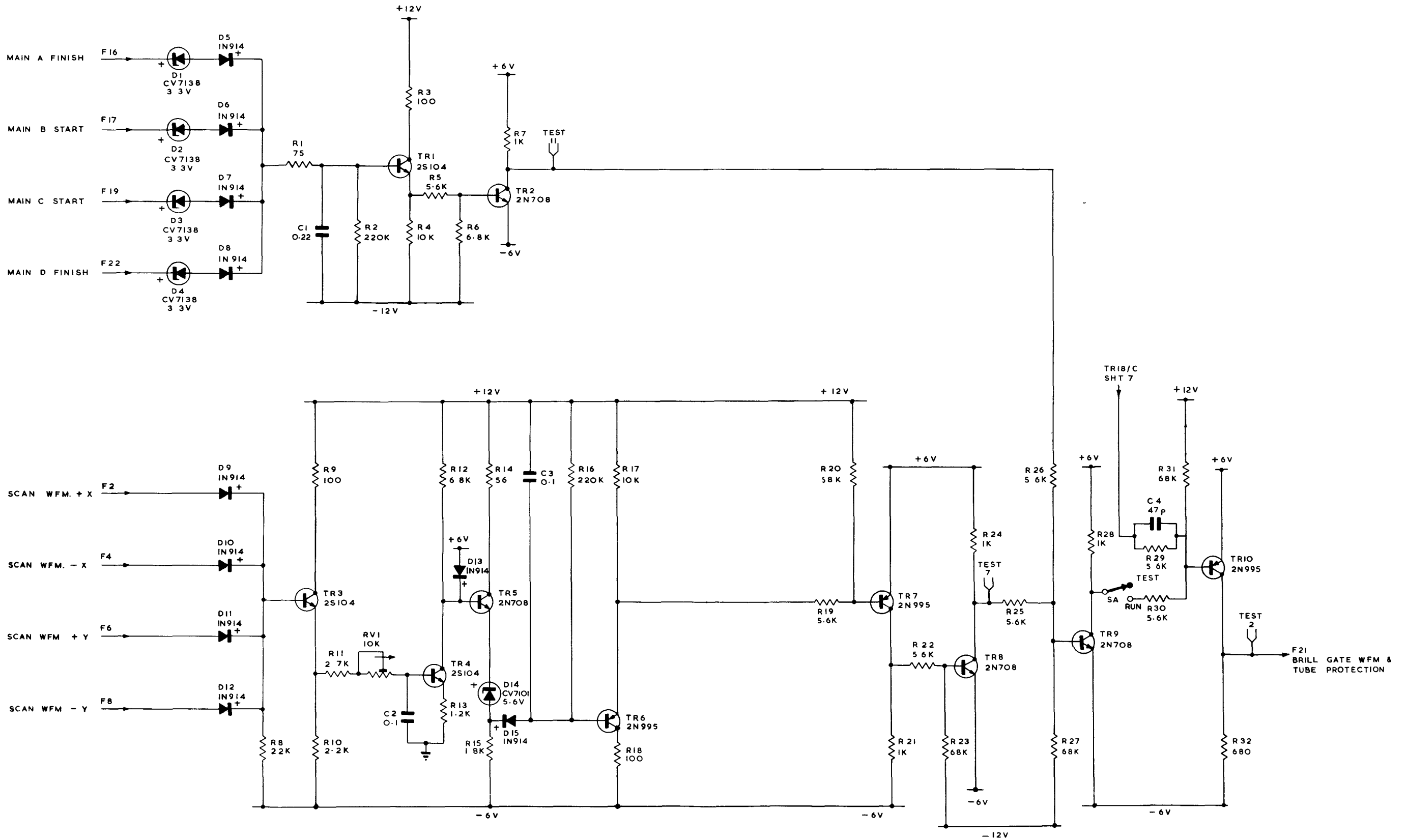
42. The circuit comprises diodes D28-D31 and capacitors C19-C22. The diodes are each back-biased by their respective power supply connected across each. If a supply fails and reverse voltage appears on the line, the diode connected to it conducts, and either earths the line (6V supplies), or holds it to the 6V level (12V supplies). The capacitors prevent the diodes conducting on transients during normal operation and provide additional decoupling to isolate the boards from the power supply transients.

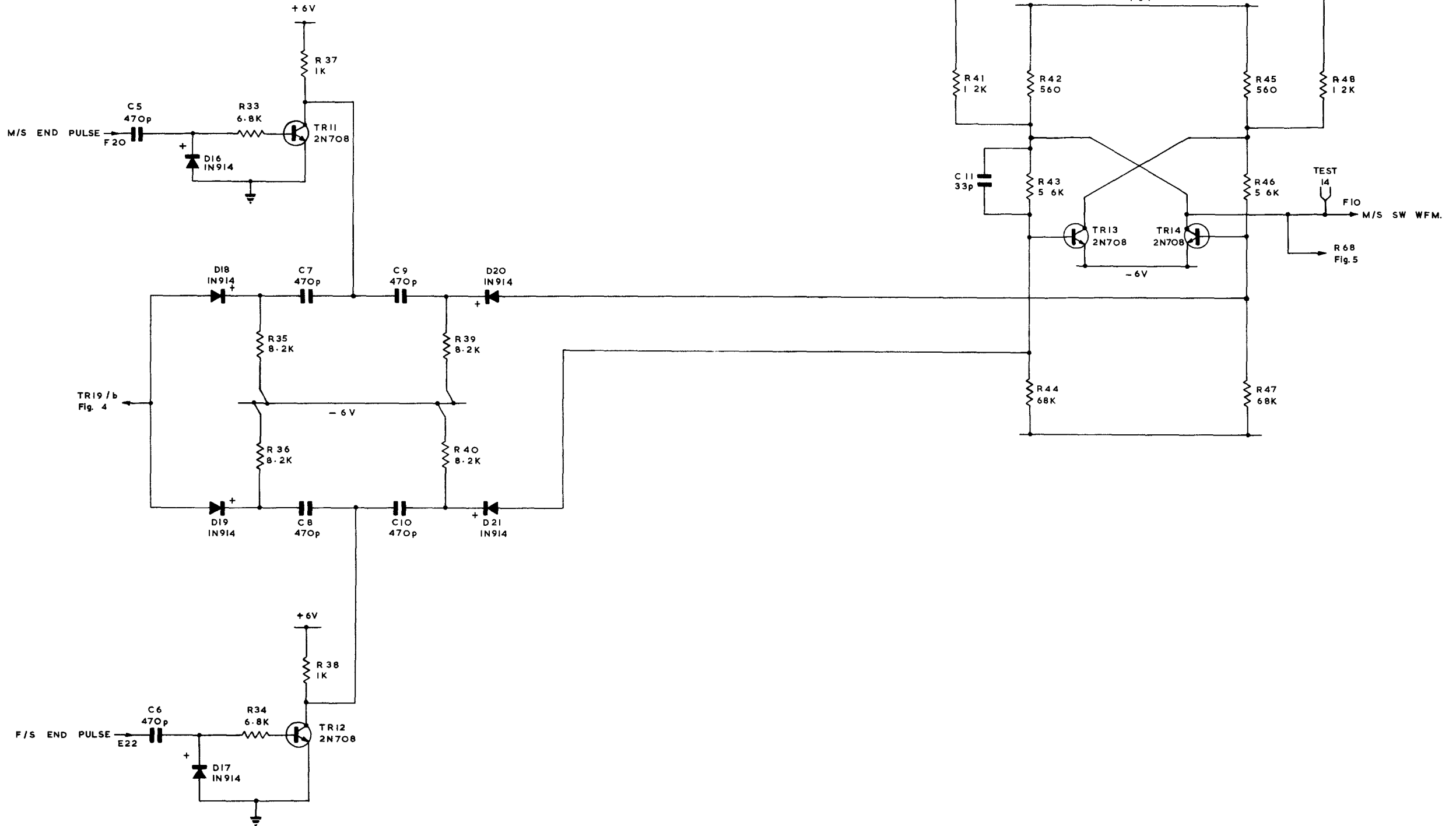


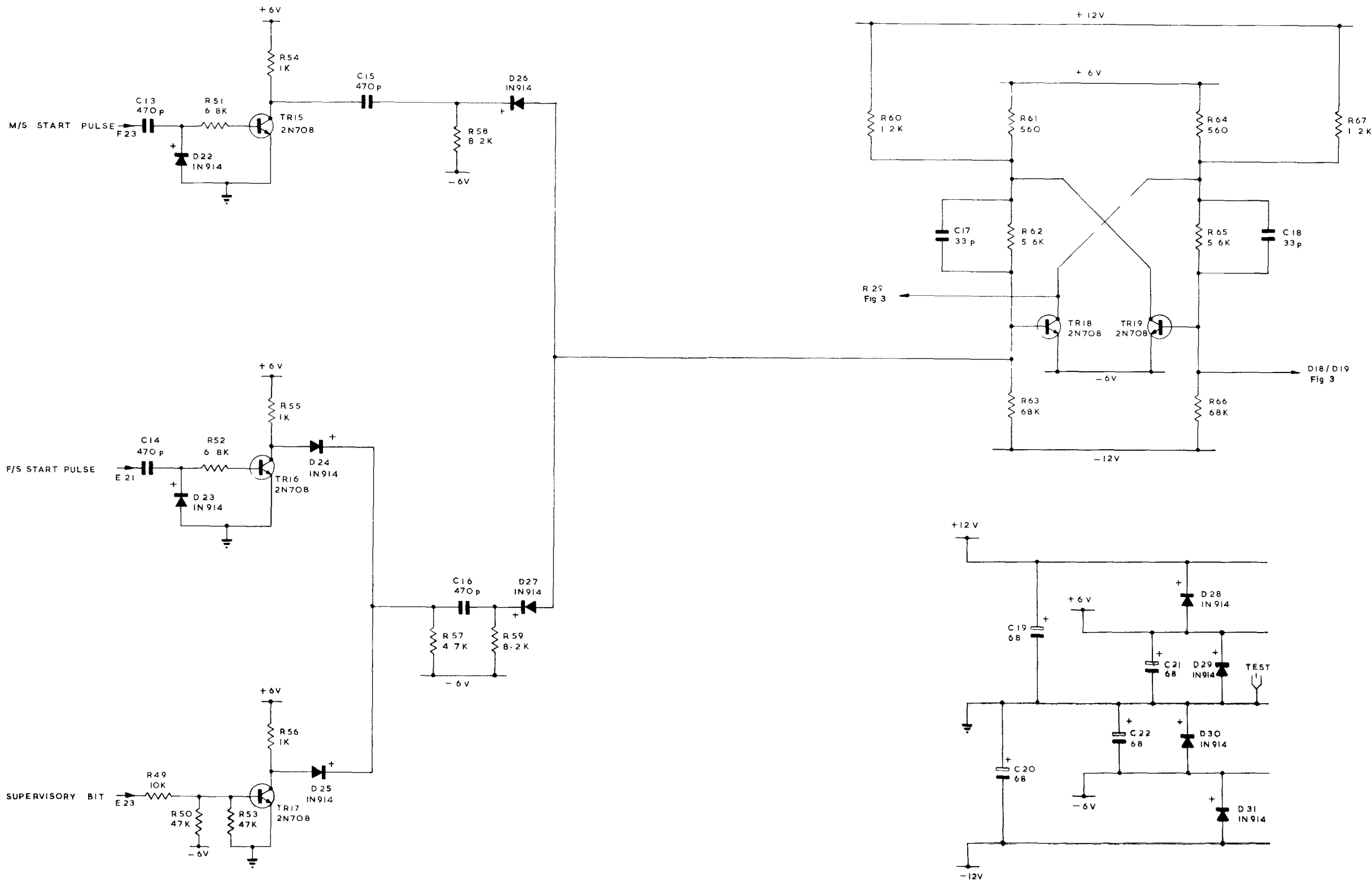
A.L.32, NOV. 71

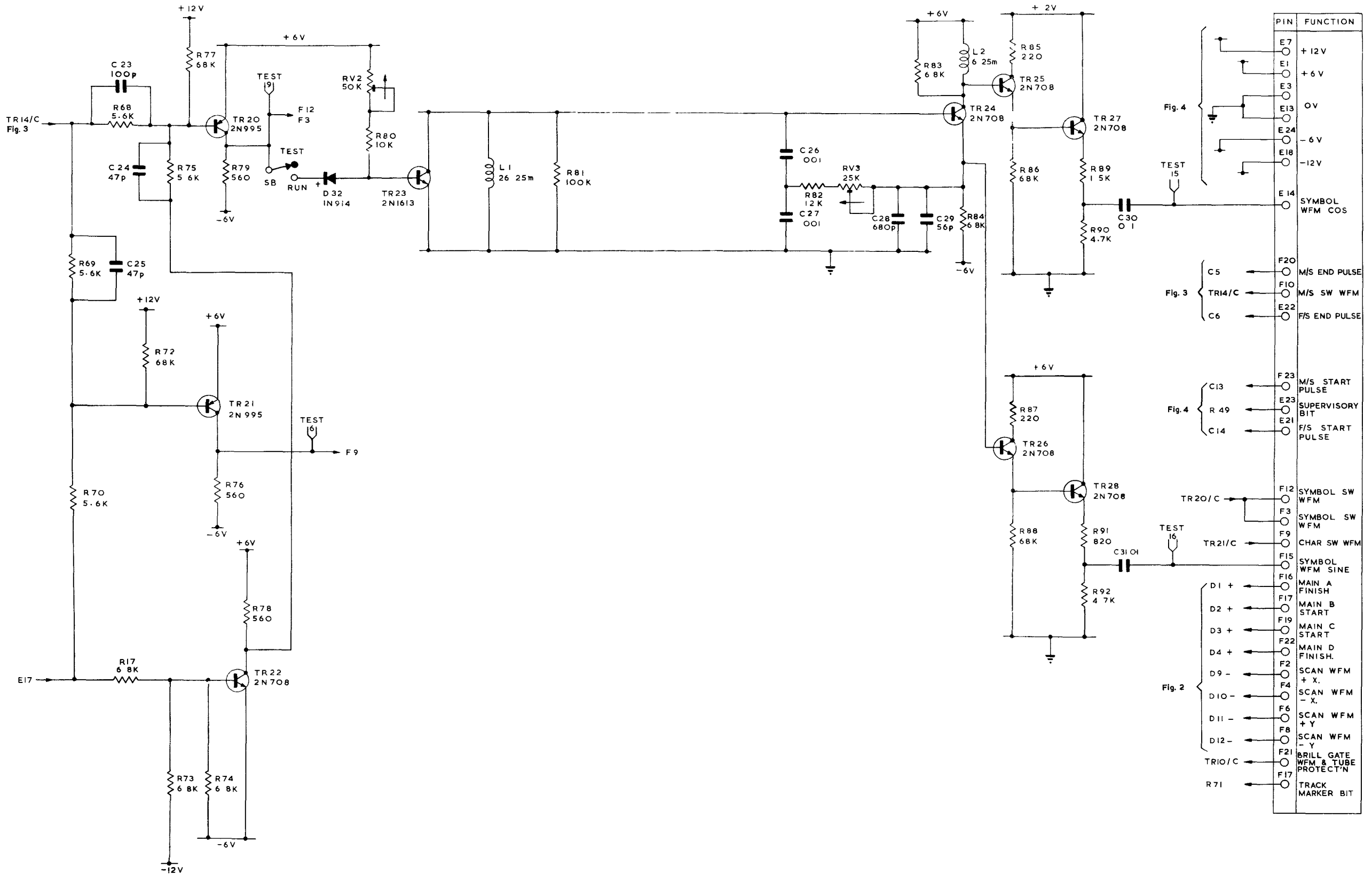
Category selection Type 12458

Fig. 1

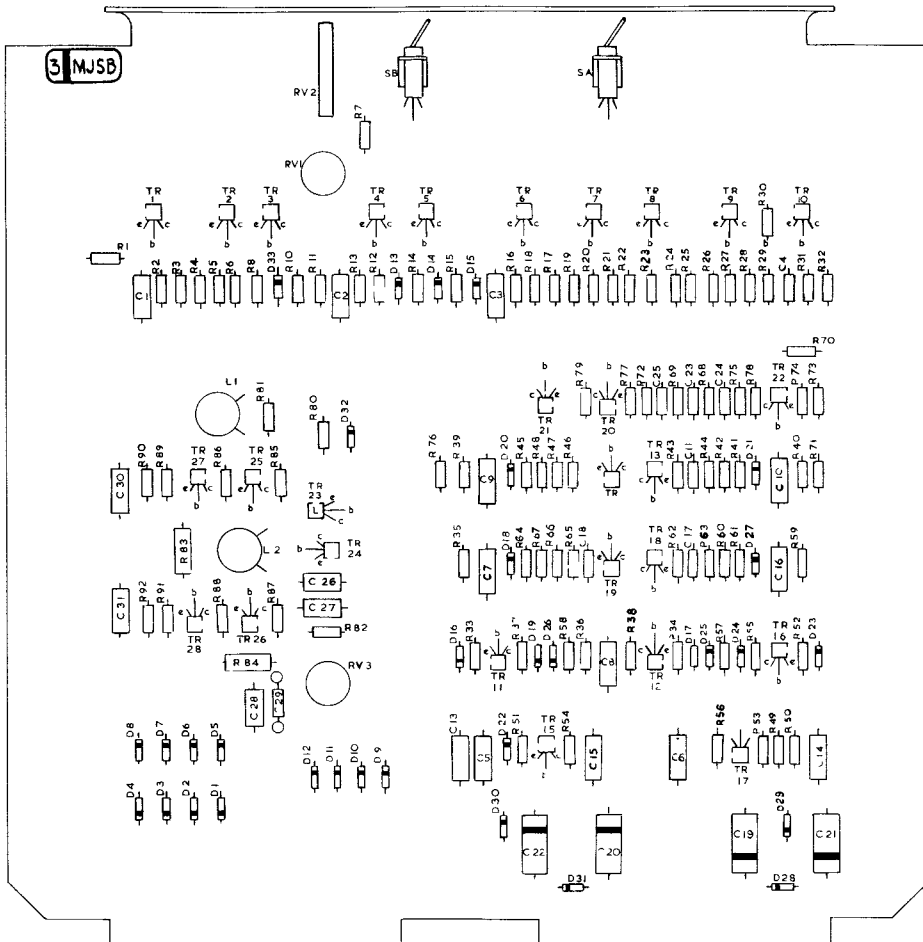








PIN	FUNCTION
E7	+ 12V
E1	+ 6V
E3	0V
E13	0V
E24	- 6V
E18	- 12V
E14	SYMBOL WFM COS
F20	M/S END PULSE
F10	M/S SW WFM
E22	F/S END PULSE
F23	M/S START PULSE
E23	SUPERVISORY BIT
E21	F/S START PULSE
F12	SYMBOL SW WFM
F3	SYMBOL SW WFM
F9	CHAR SW WFM
F15	SYMBOL WFM SINE
F16	MAIN A FINISH
F17	MAIN B START
F19	MAIN C START
F22	MAIN D FINISH.
F2	SCAN WFM + X.
F4	SCAN WFM - X.
F6	SCAN WFM + Y
F8	SCAN WFM - Y
F21	BRILL GATE WFM & TUBE PROTECT'N
F17	TRACK MARKER BIT



Chapter 10

VIDEO BOARDS (MFK SERIES)

LIST OF CONTENTS

	Para.
Introduction	1
Outline of working	7
Detailed description	
Video channels	19
Calibration channel	25
Character channel	28
Video electronic switch	29
The brilliance channel	35
Protection circuits	45

LIST OF ILLUSTRATIONS

	Fig.
Component layout on basic video board MFKB	1
Logic for video board type 12235 MFKB	2
Board type 12235 MFKB	3-8

INTRODUCTION

1. The information to be displayed on the viewing unit screen is brought into the unit from various parts of the system and appears at the inputs of a combined amplifier and brilliance controlling circuit contained in the printed wiring board MFKB.
2. This board is located in a board box in both the 12in and 21in labelled radar displays in position 4.
3. Before making a detailed study of the functioning of the board, it is essential that the reader is familiar with the working of the mainscan/fastscan system and the timing arrangements as described of the category selection board MJSB.
4. The board handles selected videos fed in on six channels. These videos are as listed below.

- Video 1) Both channels carry radar video as selected by the video selector switch on the Radar Control Panel Type 11057 (i. e. vertical and slant).
- Video 2)
- Video 3 This channel handles IFF video only.
- Video 4 This channel handles the auxiliary video as selected by the aux. video selector switch on Radar Control Panel Type 11057 (i. e. video maps 1 to 4, 10° angle marks and s. i. f. gate).
- Video 5 This channel accepts the combined 10 and 50 mile markers as selected on Control Panel Type 11057.
- Video 6 This channel accepts the coarse range marks (i. e. the 50 mile range marks) again selected on Control Panel Type 11057.

5. Character video and a. d. c. symbol level are also handled by the video channel of the board, being displayed during the fastscan period. The timing of this is determined by switching waveforms supplied by the category selection board.

6. The same switching waveforms control another set of electronic switches associated with the brilliance channel. The selected brilliance level output is then fed as one input to a brilliance amplifier, which is controlled by a brilliance gate waveform fed from the category selection board. This ensures that the tube is brightened during the selected video period.

OUTLINE OF WORKING

7. Each of the video inputs is taken to a separate amplifier which has its own video selector (on/off) switch and video gain control. The four amplifiers concerned share a common collector load, thus the output is mixed video, and the stage is known as the video mixer.

8. The mixed video signals are then fed to another amplifier where the level is set on which the signals will 'sit' when applied to the cathode of the c. r. t.

9. The calibration pulses are fed in to amplifiers similar to the four amplifiers that make up the main video mixer, where again separate selection and gain can be controlled before mixing, and the output of this stage combined with the output of the amplifier referred to in paragraph 55 above, so that the inputs to all six channels are mixed at this point.

10. The mixed videos thus produced are all displayed during the mainscan presentation and are therefore taken to the first way of the three-way electronic switch (video channel) which operates during the mainscan period.

11. A second 'way' receives character video, and the third 'way' receives symbol information, that is, the data required to be displayed during a fastscan period.

12. The output of all three 'ways' forms the common input to a final state of amplification which contains a limiting circuit, and which produces the waveform required to be applied to the cathode ray tube cathode in order to brilliance modulate the tube.
13. The grid of the cathode ray tube receives the waveform produced in the brilliance control circuits so that the tube is cut off when blanking is required. This waveform is produced as follows.
14. The brilliance amplifier has three inputs comprising the selected control voltage from the second group of electronic switches, the overall brilliance control voltage and the output from a two-way OR gate which passes either the brilliance gating waveform or the octagonal blanking waveform.
15. The overall brilliance control voltage is fed directly to one of three input resistors and sets the threshold level at the cathode ray tube grid by setting the lowest working input level at the amplifier.
16. The individual brilliance control voltages are derived from three potentiometers associated with mainscan, character and symbol presentation. The three controls feed into three electronic switches which are actuated by the appropriate switching waveform and pass the selected voltage on to a second input resistor in the amplifier during the period when a particular scan is to be displayed.
17. The two inputs to the OR gate associated with the third input resistor both affect the blanking of the tube. The brilliance gate waveform supplies a bright-up voltage during the periods when information is to be displayed and applies a blanking voltage between these periods, the waveform being produced by circuits in the category selection board. The octagonal blanking is required to effect edge blanking of the tube in order to prevent the 'halo' that would be produced if the duration of a bright-up waveform exceeded the duration of the visible trace. The octagonal blanking waveform is produced by a circuit contained within the board.
18. The three inputs are mixed in the brilliance amplifier which is an RR amplifier whose output controls the brilliance of the tube at its grid.

DETAILED DESCRIPTION

Video channels

19. The four circuits associated with videos 1 to 4 are similar, and therefore, for ease of description, only that associated with video 1 will be described.
20. Transistors TR1 and TR2 form a differential amplifier connected as a long-tail pair, with a constant current drive in the tail (TR5). The positive video signals

are applied as input to TR1 base via R9. The second input, which is applied to TR2 base, is a d. c. level derived from TR1 connected between the $\pm 6V$ supply. Potentiometer RV1 balances the circuit for equal collector currents with no input signal applied.

21. The gain of the amplifier is determined by controlling the 'tail' current which can also be cut-off when video has not been selected, and thus renders the circuit in-operative.

22. Transistor TR5 accepts two inputs, The first, which is the d. c. level set by the video 1 gain control on the Viewing Unit Control Panel Type 11211/A, controls the collector current of TR5, and thus the gain of TR1/TR2. The second is routed from the Radar Control Panel Type 11057, and is either 0V when video 1 is required or a -12V level when video 1 is to be inhibited.

23. The outputs of all four differential amplifiers are coupled together through common collector loads R2 and R3, and the two opposed outputs are applied as the two inputs to a second differential amplifier comprising TR3 and TR4. The output on TR4 collector is applied to a third differential amplifier TR16 and TR17, the second input of which is a d. c. level set by RV5. Potentiometer RV5 is adjusted to set the d. c. level of the c. r. t. to +95V.

24. The output is taken from TR16 collector and applied to the first way of the three-way electronic switch (video channel). This is formed by TR24 with TR25 accepting the mainscan switch waveform.

Calibration channel

25. This comprises transistors TR18 and TR19 (video 5) and TR20-TR21 (video 6). As both channels are identical, only that circuit associated with video channel 5 will be described.

26. The incoming cal. 1 signal (the combined 10/50 mile markers) is fed as input to TR18 base via PLA6. Transistor TR19 is connected as a constant current device in the emitter circuit, having as its inputs the d. c. level as adjusted by RV7 (10m marker) and/or the -12V inhibiting level as selected by the 10m push-button on the Radar Control Panel Type 11057.

27. The output of TR18 is developed across the common collector load R169 and fed as second input to the mainscan 'way' (TR24-TR25) of the three-way video electronic switch. The combined output of this 'way' is developed across the common collector load R74 and fed to TR26-TR27.

Character channel

28. The character video enters the board on PLA9 and is fed to the base of TR22. Transistors TR22 and TR23 are connected as a differential amplifier, the second input on TR23 base being a d. c. level set by RV9. This potentiometer is adjusted to set the d. c. level at the c. r. t. cathode to +95V. The output of this amplifier is fed to the second way of the video electronic switch.

Video electronic switch

29. The second way of this switch is formed by TR30 and TR31 with TR31 accepting the character switch waveform fed into the board on PLB9. The output of TR30 is developed across common collector load R74 and fed to TR26 and TR27.

30. The third way of this switch is formed by transistors TR32 and TR33 with the symbol video level applied to TR32 base. The symbol switch waveform is applied as input to TR33 base (the switching transistor). The output of TR32 is developed across the common collector load R74 and fed to TR26 and TR27.

31. The switch output is applied directly, but with a change of level to TR26 base, via Zener diode MR6. TR26 base is the input of the video pre-amplifier, and to this point is connected the video gate circuit TR34, MR11. The video gate receives as gating input the brilliance gate waveform from the OR gate in the brilliance channel.

32. Transistors TR26 and TR27 are connected as a long-tailed pair and a single-ended output is taken from the collector of TR27 and applied to the base of emitter-follower TR28.

33. The video at TR28 base is limited by MR12 to the level of TR35 base emitter. This level is varied over the level 0V to +6V as the level at PLB11, derived from the video limiter control on the Viewing Unit Control Panel Type 11211/A, is varied from -12V to +12V.

34. The final video amplifier comprises emitter-follower TR28 and twin transistor TR29 connected as a cascade (composite common-emitter + common base) amplifier to limit the voltage developed across each section to a safe value. The clipped video is applied to the lower section via TR28. The back level voltage at the c. r. t. cathode is of the order of +95V with respect to signal earth. The exact level is set by the post-limiter gain control TV7 and allows for variations in the c. r. t. grid base.

The brilliance channel

35. The mainscan, character and symbol brilliance control voltages derived from the control potentiometers (i. e. radar brill, on the the Viewing Unit Control Panel Type 11211/A and char. brill/symbol brill. on Radar Control Panel Type 11057) are applied to three ways of the brilliance channel electronic switch. This switch is a four-way switch, only three of which are used. The switch is controlled by the mainscan, character and symbol switch waveforms. The output of the switch (referred to as the switched brilliance control volts) is developed across common collector load R4 and is applied as one input of the brilliance amplifier TR49-TR52.

36. In the octagonal blanking circuit, the four scan waveforms enter the board at

PLA19-PLA22, and are fed via a diode mixing circuit MR18-MR21 and a level setting network to the base of emitter-follower TR44. The standing level at this base is adjustable by the preset RV10. The output of TR44 operates the overdriven long-tailed pair TR45-TR46, whose output is shifted in level by MR22, inverted by TR48 and fed to the OR gate MR23-MR24.

37. In addition to the octagonal blanking waveform, the OR gate receives the composite fastscan/mainscan brilliance gate waveform from the category selection board on PLB6. The output of the gate is positive when one or both inputs are positive, and this level causes the c. r. t. to be brilliance blanked. The output is referred to as the brilliance blanking waveform, and is fed:-

- (1) to the video gate circuit in the video channel.
- (2) to one of the inputs of the brilliance amplifier.

38. When all inputs to the octagonal blanking circuit are around zero, TR44 base is at about +3V. Transistor TR45 conducts, TR46 is cut-off and TR48 is bottomed, so that the level fed out from TR48 collector is approximately -5V. When any input becomes sufficiently negative to bring TR44 base to about zero level, TR45 cuts off, TR46 conducts, TR48 cuts off sharply and the output changes rapidly to around +5V; this level is passed to the OR gate and blanks the trace. The exact input level at which changeover takes place is set by RV10, which therefore determines the position on the screen at which blanking takes place (normally just inside the edge).

39. Resistors R130 and R131 give the frame created by the blanking an octagonal shape. When the spot is scanning towards a cardinal point on the screen, only one of the diodes in the mixer (MR18-MR21) is conducting as blanking level is reached, and therefore, around this trace-bearing, the blanking will take place at a constant level of X and Y deflection giving a horizontal or vertical edge. Around a half-cardinal point R130-R131 allow two diodes to conduct simultaneously, and the voltage at TR44 base depends on the average of the inputs to these two. Blanking therefore takes place at a constant average level of X and Y deflection, and this gives an edge with a 45° shape in the region of the half-cardinal points.

40. The brilliance amplifier is a summing operational amplifier with three inputs.

- (1) The switched brilliance control voltage controlled by the brilliance potentiometer on the control panels.
- (2) An overall brilliance level of 0V to -12V controlled by preset RV11.
- (3) The brilliance blanking waveform from brilliance gate circuit or the octagonal blanking circuit.

41. The switched brilliance control volts is applied via input resistor R140, the overall brilliance level is applied via input resistor R142 and the brilliance blanking

waveform is applied via input resistor R141. R149 is the feedback resistor having variable capacitor C20 connected in parallel to provide increased feedback during transient voltage changes, and this reduces overshoot as the brilliance waveform goes negative. Potentiometer RV11 sets the black level at the grid of the c. r. t.

42. The brilliance amplifier consists of a long-tailed pair (TR49-TR50), and emitter-follower (TR51) and a base fed output pair (TR52a, TR52b). The long-tailed pair forms a differential amplifier with earth level applied as reference to TR50 base. The non-inverted output from TR50 collector is applied to TR51 base via Zener diode MR25, which maintains a constant d. c. potential difference between these two points.

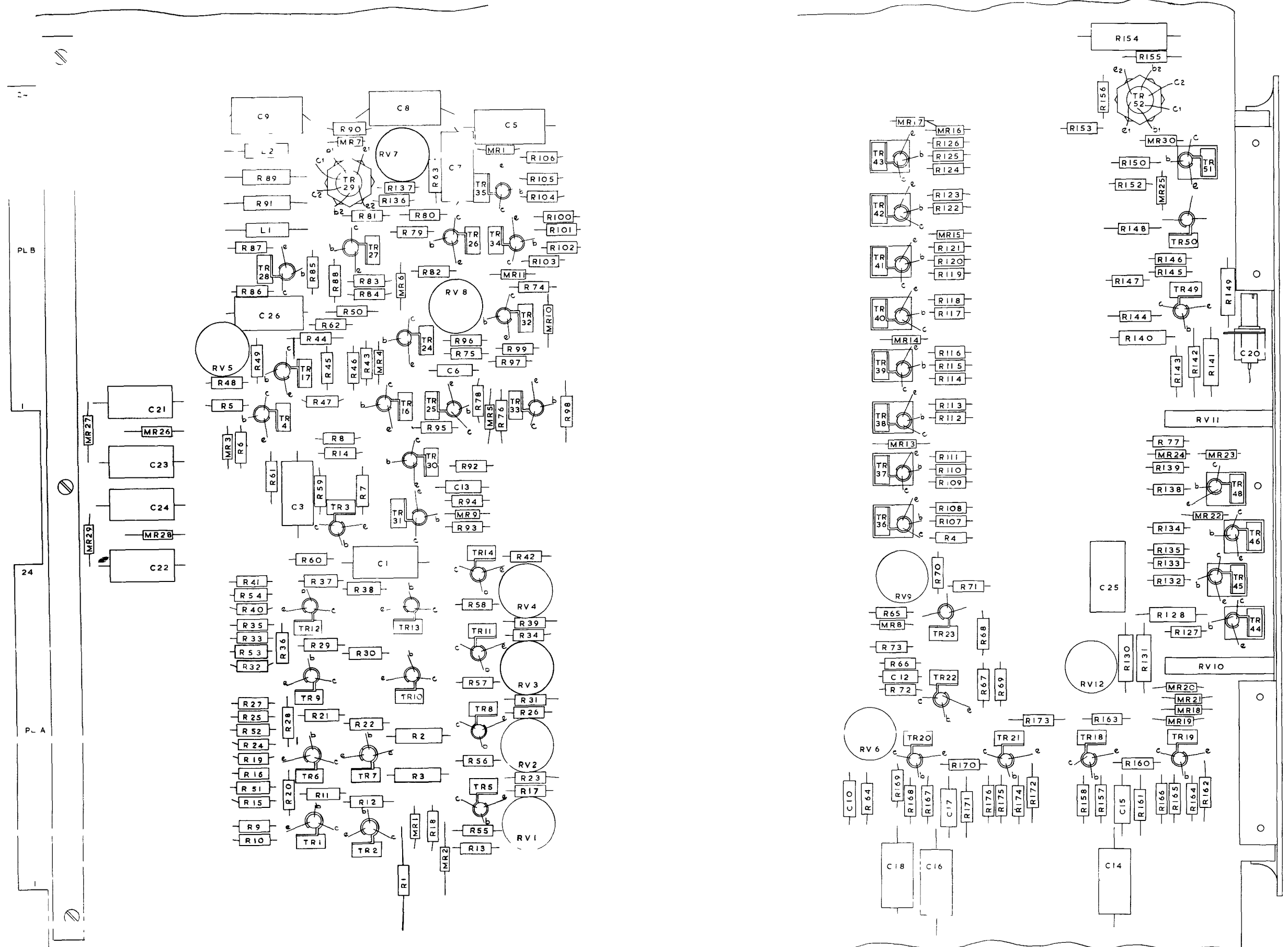
43. The output of TR51 is fed to the base fed output pair (TR52a-TR52b), which in turn applies the output voltage across the equal series connected resistors R155, R156. This ensures that each transistor will draw identical collector currents, thereby equally internally dissipating the total power across each transistor (i. e. half across each).

44. The output voltage is then fed out of the board PLB3 to the c. r. t. grid, this being monitored at TEST POINT 15.

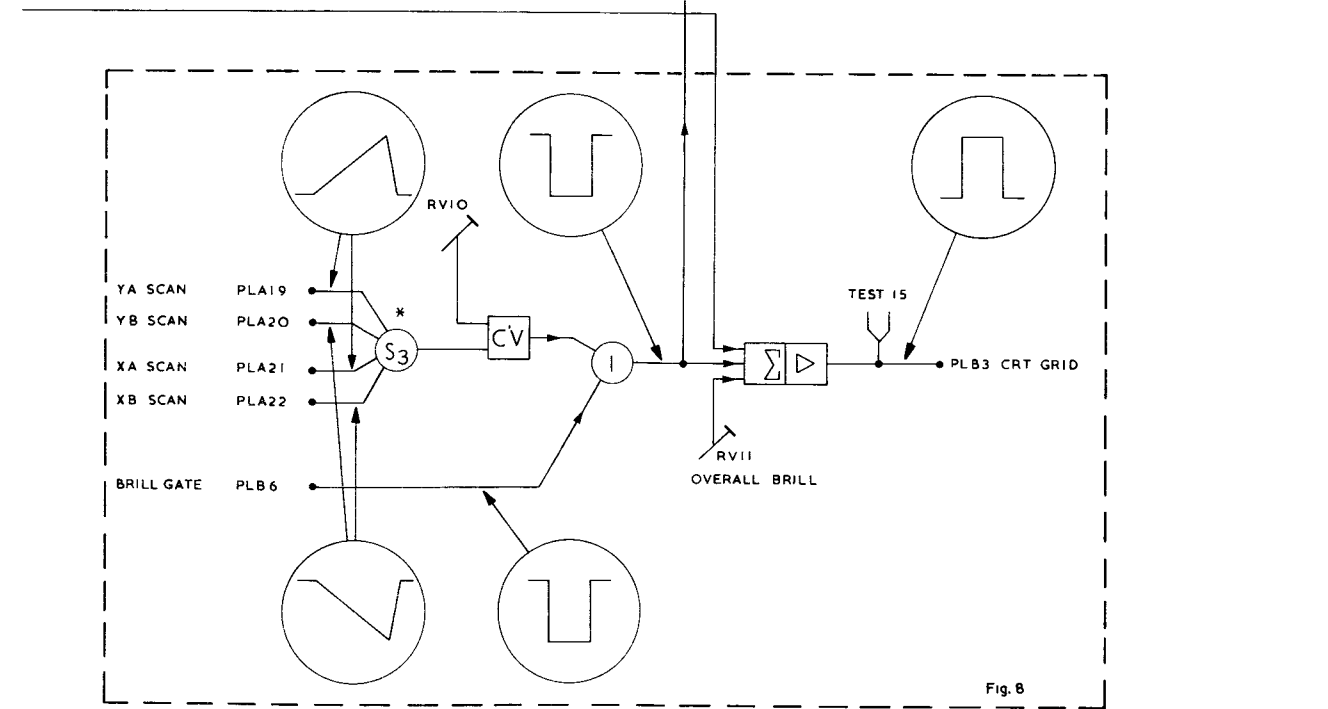
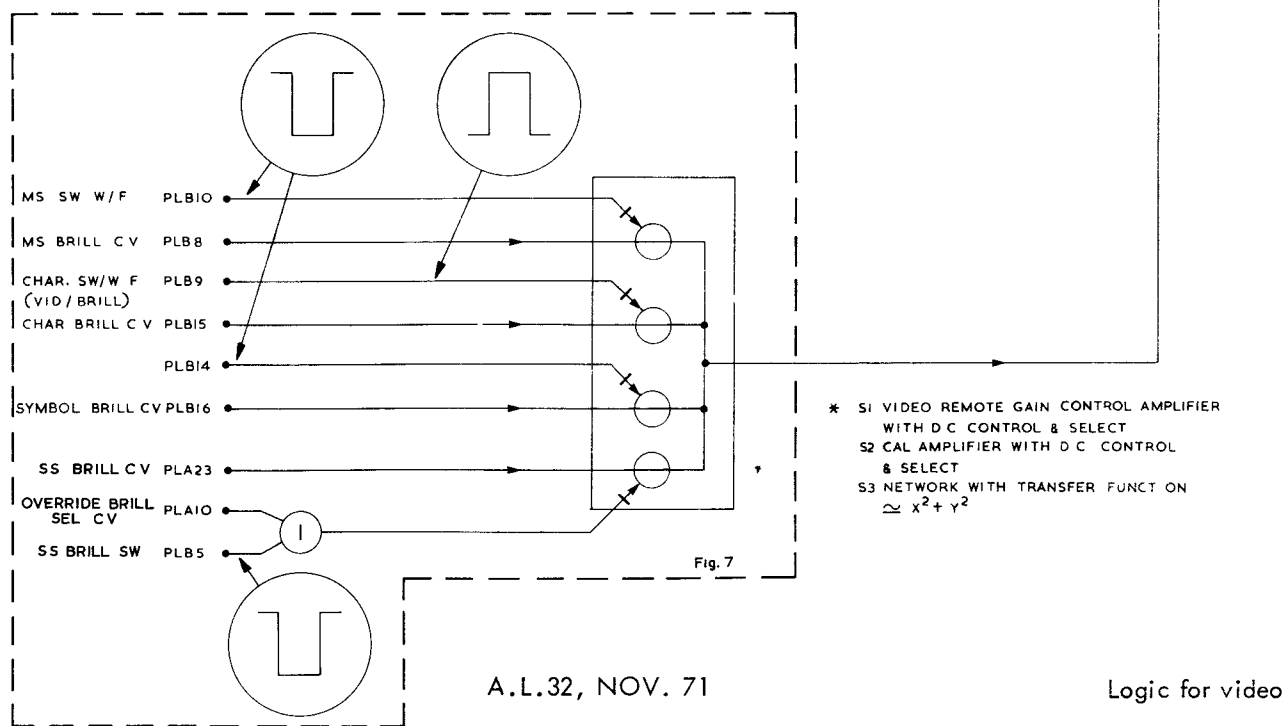
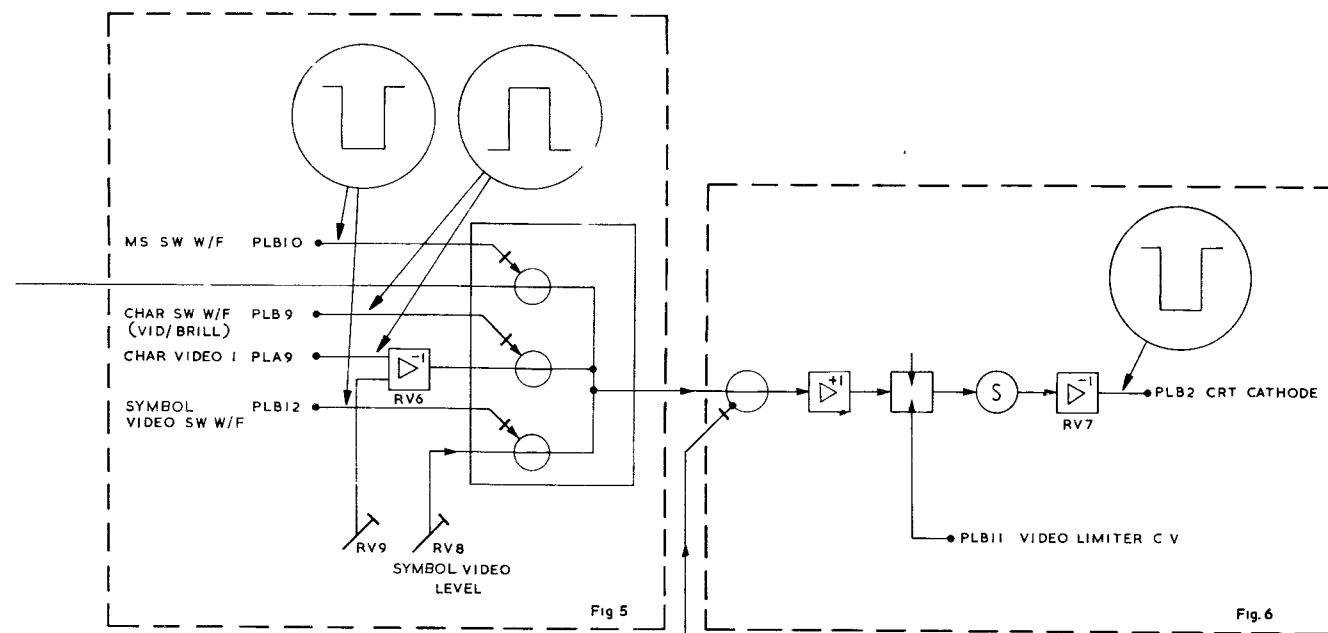
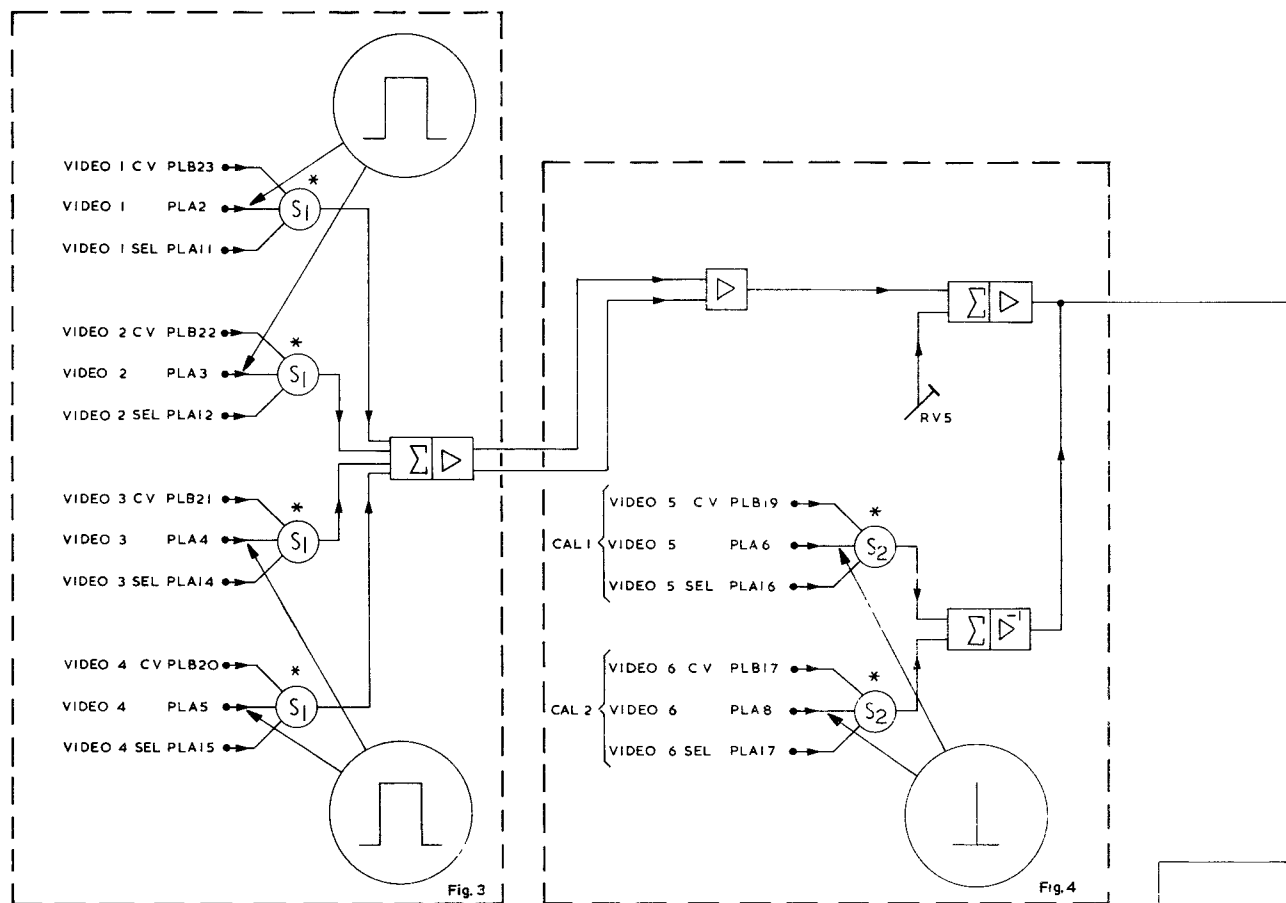
Protection circuits

45. The board operates from four stabilised d. c. supplies provided by Power Unit Type 11600 in the 12in viewing unit, and by Power Unit Type 11606 in the 21in viewing unit. These supplies are interconnected through the board circuits, and if a supply fails, the supplies of opposite polarity could attempt to drive a reverse current through certain transistors. A protection circuit is included to prevent this occurring.

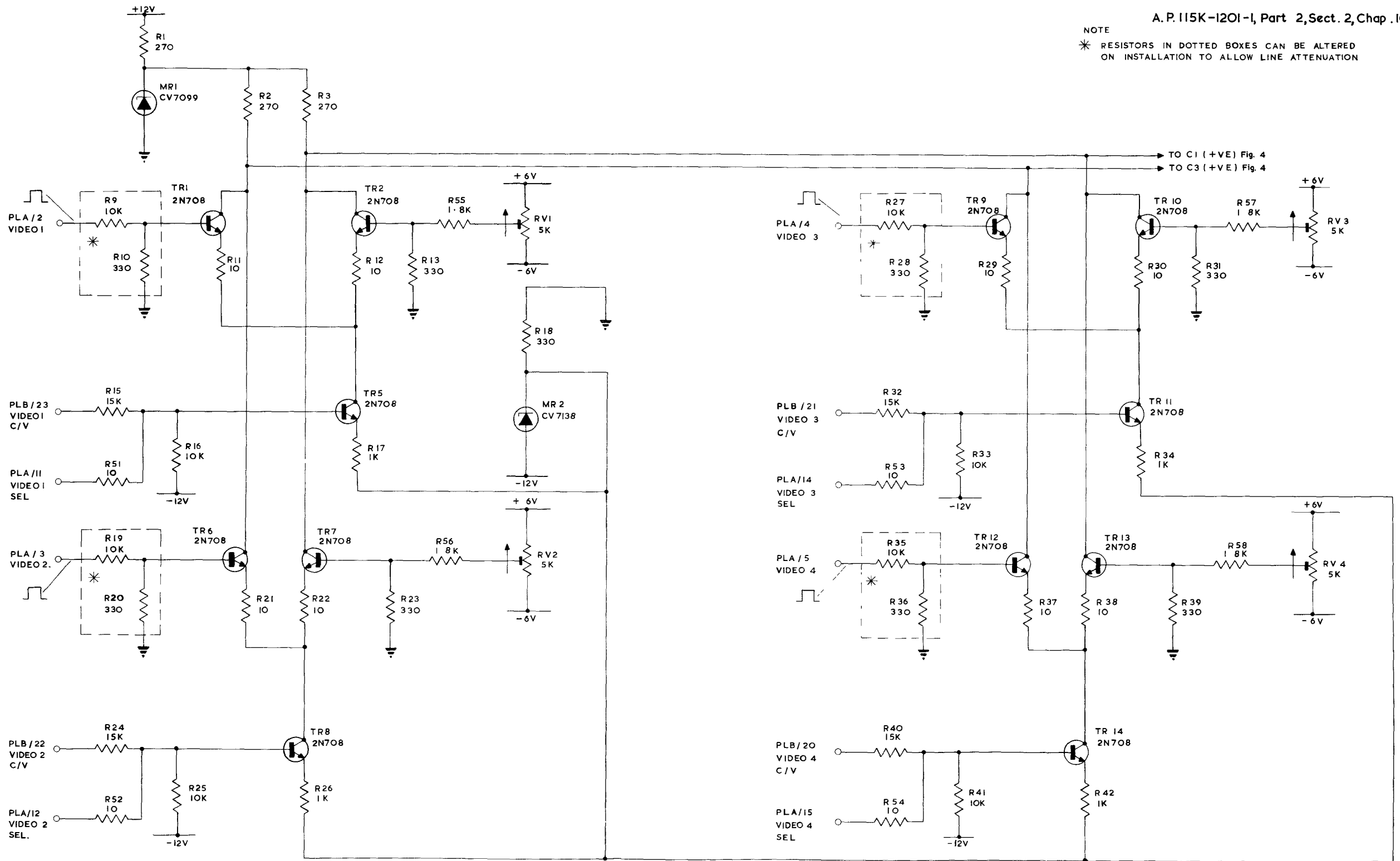
46. This circuit comprises diodes MR26-MR29 and capacitors C21-C24. The diodes are each back biased by their respective power supply connected across each. If a supply fails and reverse voltage appears on the line, the diode connected to it conducts, and either earths the line (6V supplies) or holds it at 6V (12V supplies). The capacitors prevent the diodes conducting on transients during normal operation and provide additional decoupling to isolate the boards from the power supply transients.

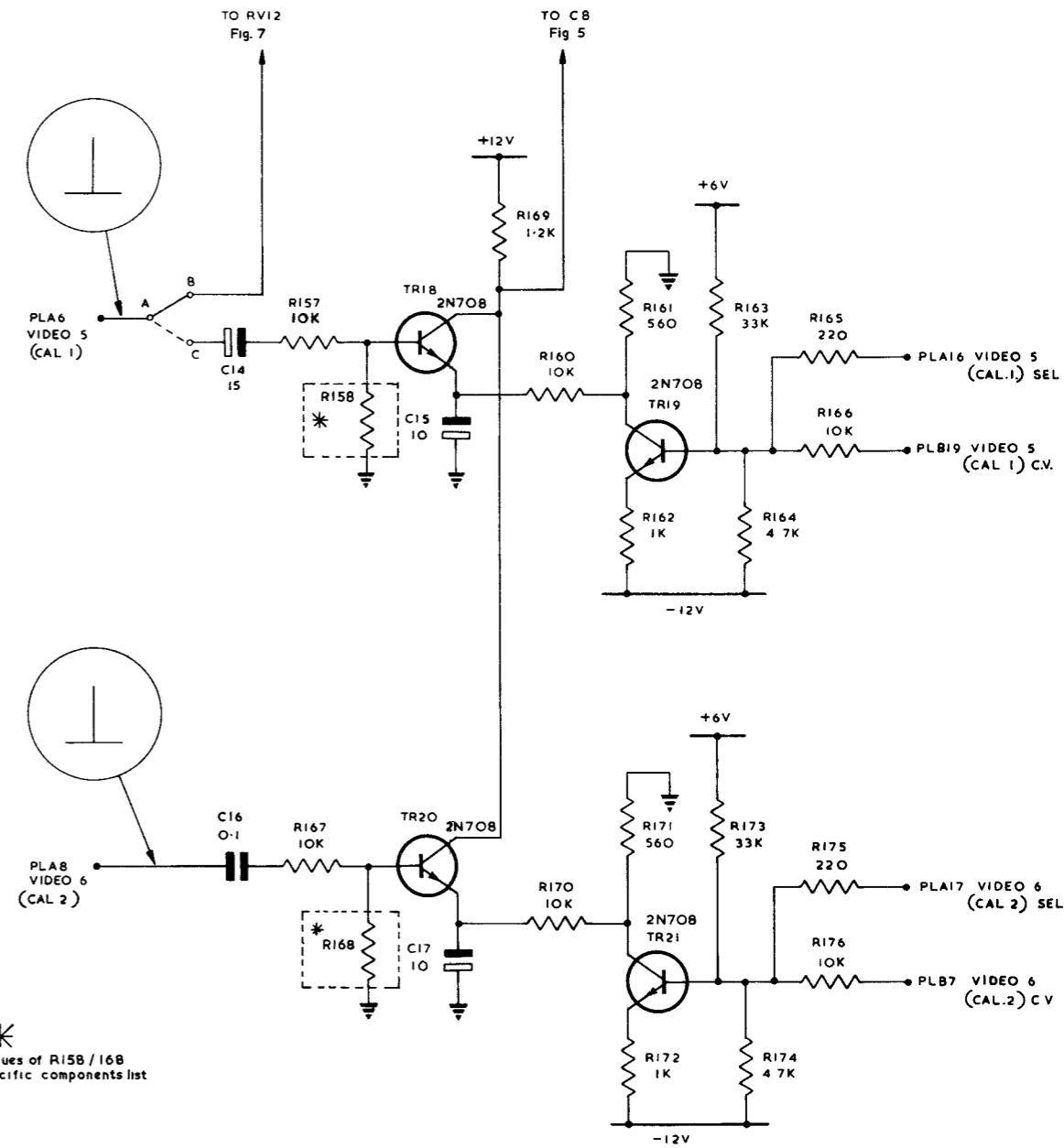
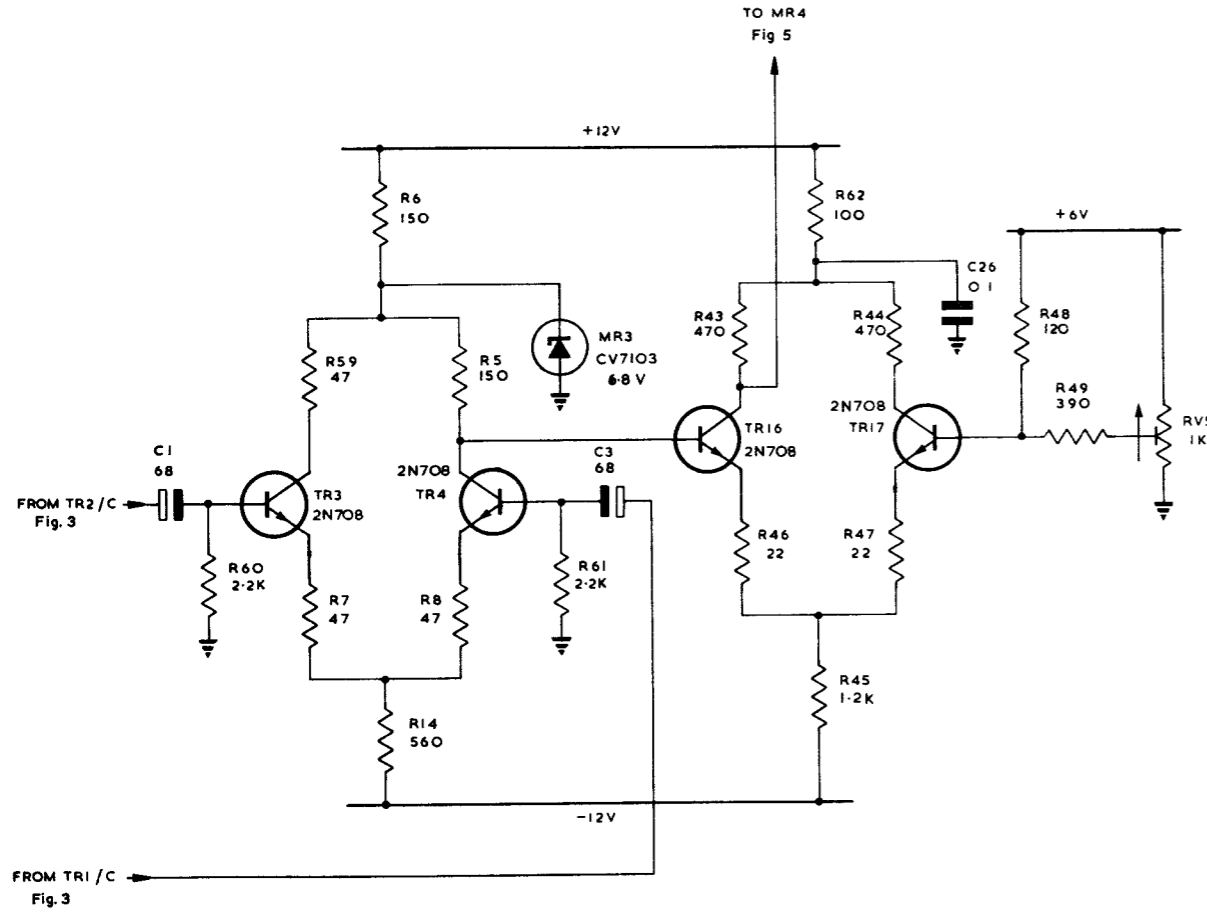


Component layout on video board Type 12235 MFKB

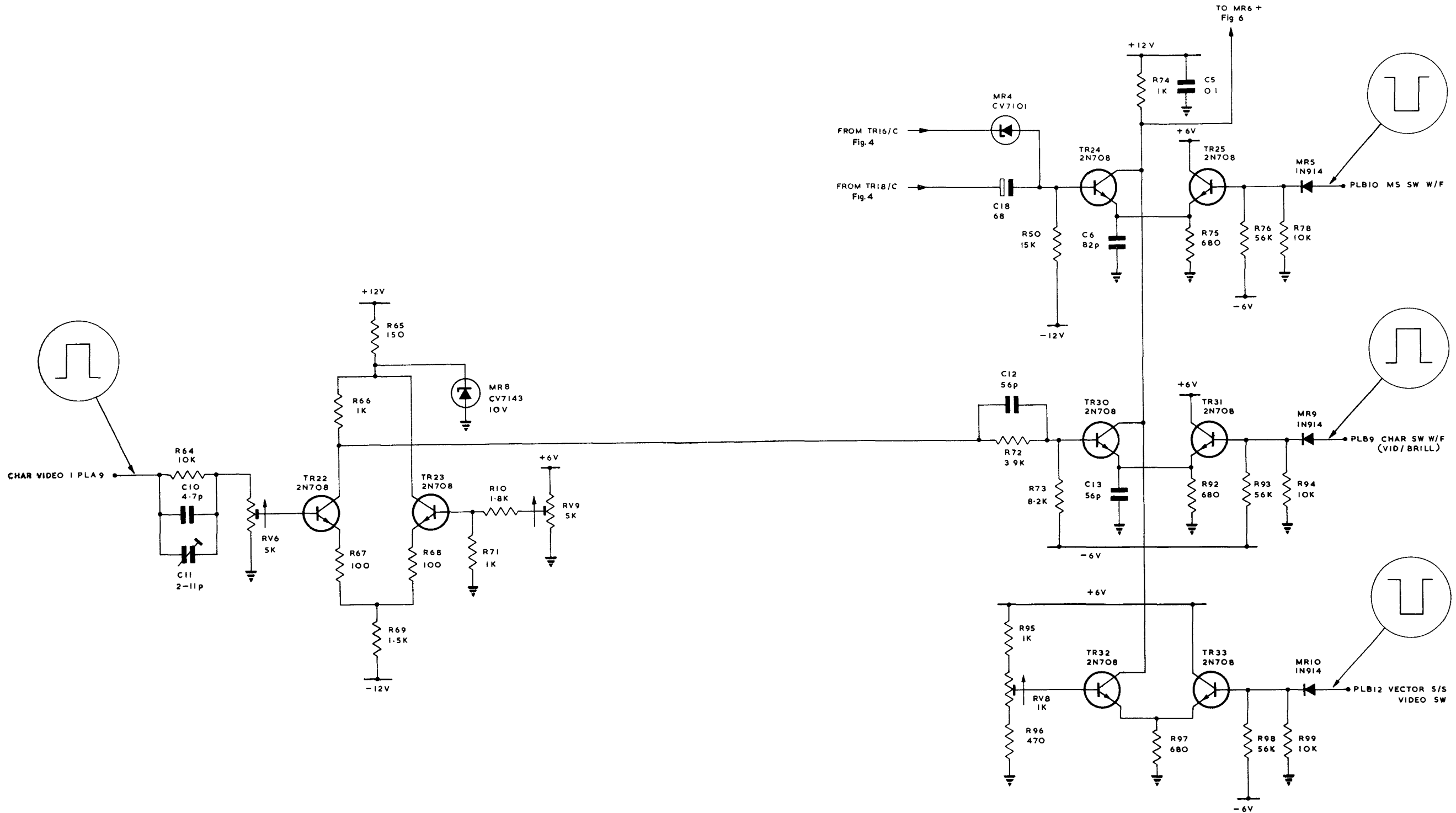


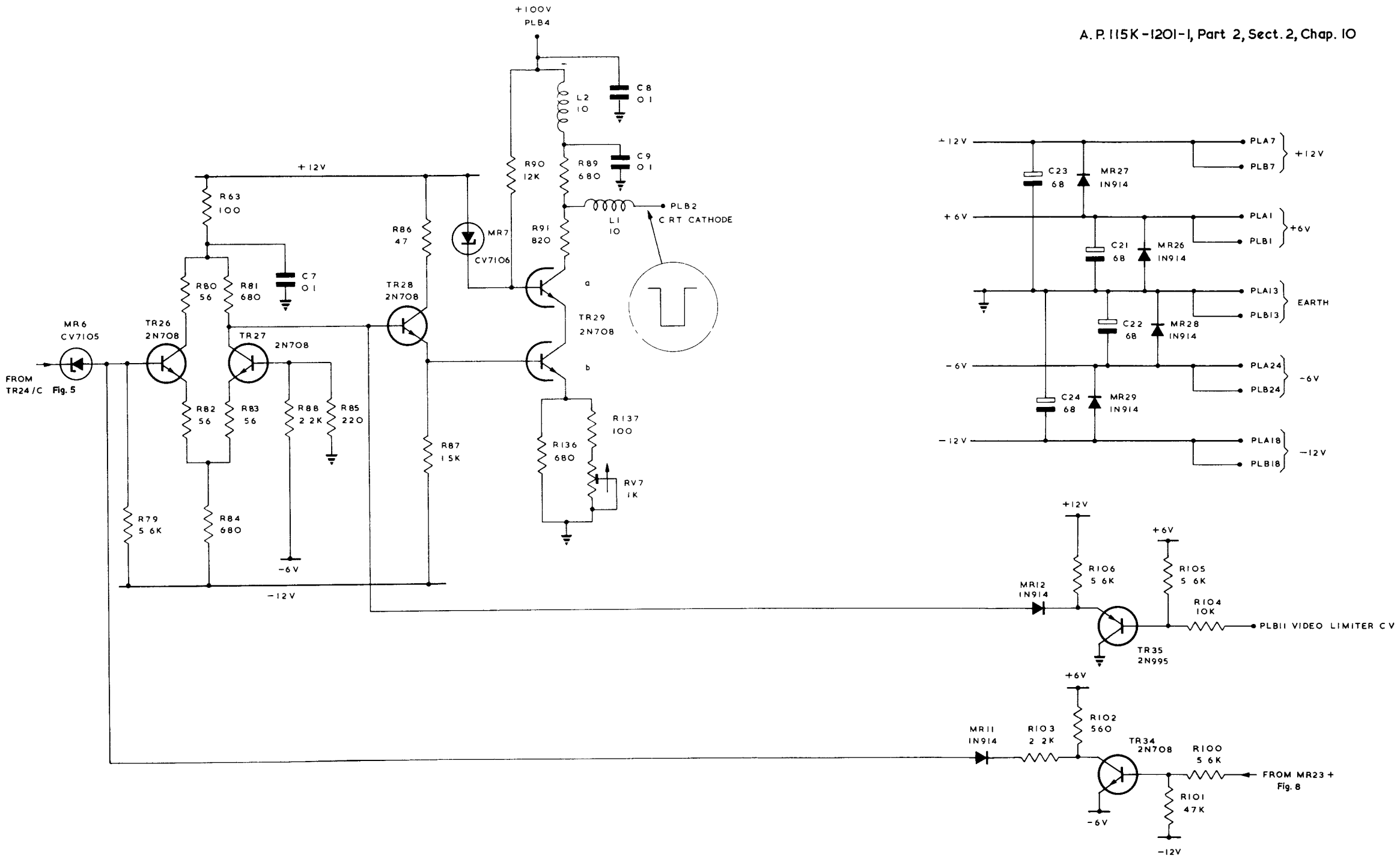
NOTE
 * RESISTORS IN DOTTED BOXES CAN BE ALTERED ON INSTALLATION TO ALLOW LINE ATTENUATION

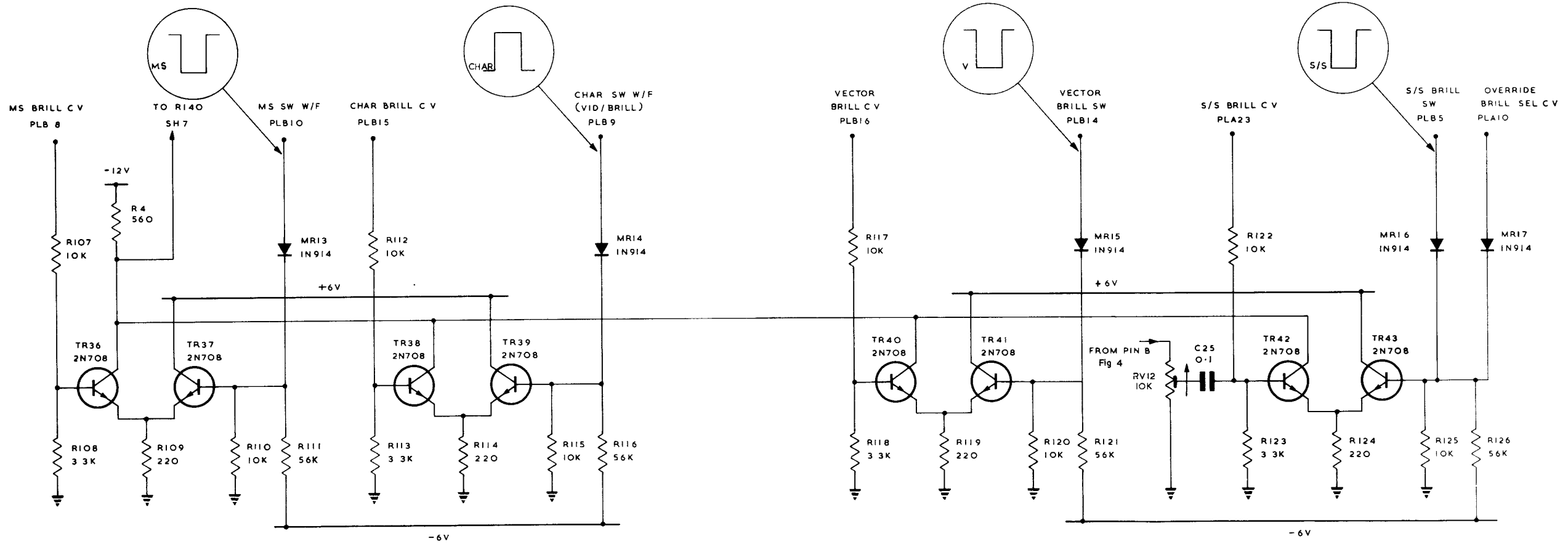


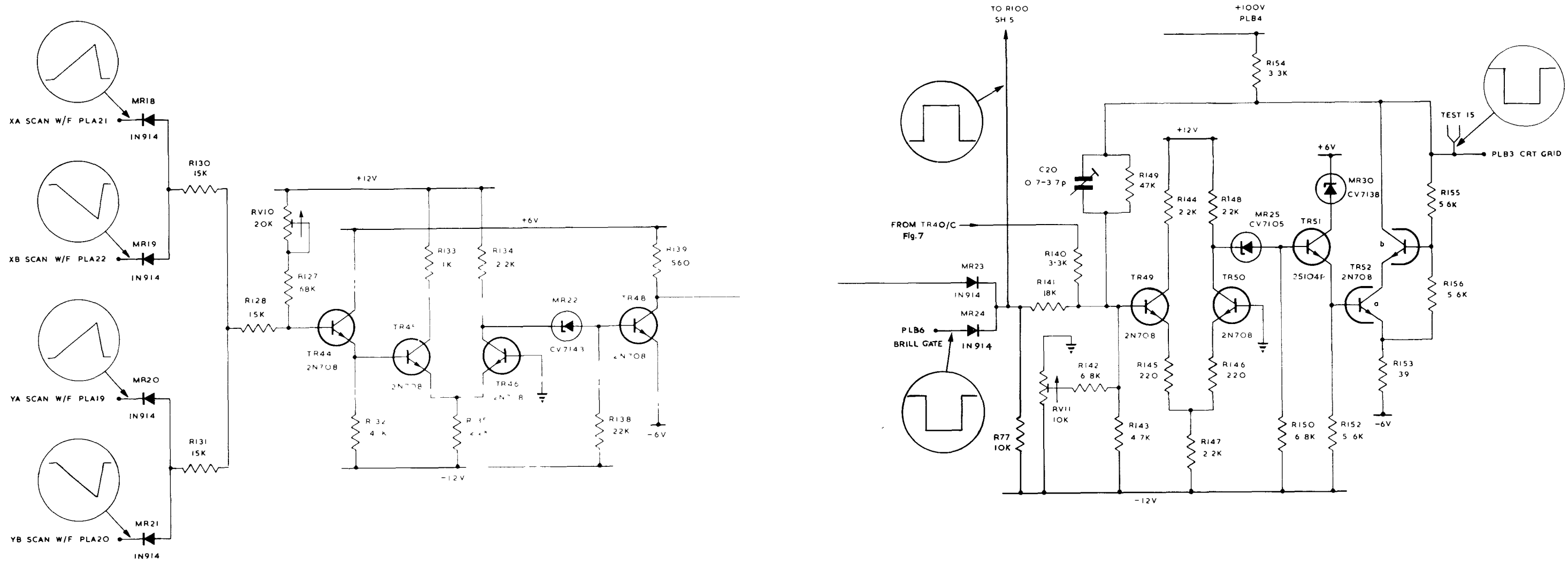


*
For values of R158/168
see specific components list









Chapter 11

DEFLECTION BOARDS (MRM SERIES)

LIST OF CONTENTS

	Para.
Introduction	1
Outline of operation	5
Detailed description	11
The range-change amplifier	18
Symbol channel... ..	25
Transistor protection circuit	27

LIST OF ILLUSTRATIONS

	Fig.
Deflection board layout MRMC 12439	1
Logic for deflection board MRMC (12439)	2
Deflection board type 12439 MRMC	3

INTRODUCTION

1. Two identical printed wiring boards of this type are used in each LRD viewing unit. One for the X deflection channel fitted into position No. 1 of the board box and the other for the Y deflection channel fitted into position No. 3 of the board box.
2. Each board contains the circuits necessary to produce the complex deflection voltage required to drive the final deflection drive amplifiers.
3. It should be noted that in its X deflection role, the board mates with the viewing unit printed circuit edge-connectors C and D, and in its Y deflection role, the board mates with the viewing unit printed circuit edge-connectors H and G. Since the connecting pins on the board take the letter of the socket with which they mate, these pins are annotated on the schematic and circuit diagrams with both of the possible appropriate letters thus: Pin 2C(G) or pin 8D(H), etc.
4. The board accepts five inputs as follows:-
 - (1) The mainscan deflection waveform or the positional control volts for the fastscan data, routed from the m. g. t. cabinet type 11825.

- (2) The inverted mainscan or positional control volts.
- (3) Picture centre control volts from the Viewing Unit Control Panel Type 11211 (not used with the 21in viewing unit).
- (4) Picture shift control volts from the Radar Display Control Panel Type 11057.
- (5) Symbol deflection waveform from the category selection board.

OUTLINE OF OPERATION

5. Two deflection boards MRMC are used in each viewing unit to process and mix the various X and Y scan and shift waveforms generated elsewhere in this system. The operation of each board is identical and that of the deflection circuits only are described.

6. During the mainscan scan periods, the X mainscan deflection waveforms are applied to the board, the negative phase being inverted and applied to a summation network which forms the input to a feedback amplifier. The second input to this feedback amplifier is the positive phase of the mainscan deflection waveform. This procedure is known as 'common mode rejection' and is used to minimise noise pick-up.

7. The amplifier output waveform together with the picture shift control volts and the centring control volts (12in only) are applied to a range-change amplifier, the gain of which is determined by the position of the range-change push-buttons on the relevant viewing unit control panel.

8. One output from the range amplifier is fed direct to a final deflection amplifier and is identified as 'scan A'. A second output is inverted by a feedback amplifier and fed to an identical final deflection amplifier. This output is identified as 'scan B'. The final deflection amplifiers are Type 12502 in the 12in l.r.d. and Type 12505 in the 21in l.r.d.

9. During fastscan periods, the fastscan positional control volts replace the mainscan deflection waveforms as the input to the same circuits. These control volts determine the positions at which the fastscan data will appear on the c.r.t. and are routed to the final deflection drive amplifiers for subsequent application to the main deflection coils.

10. One phase of the symbol waveform produced by the category selection board is fed to board MRMC. This input is applied to a phase-splitter which produces the push-pull A and B symbol waveforms. These outputs are added to the fastscan positional voltages at the final deflection amplifier.

DETAILED DESCRIPTION

11. The positive-going mainscan deflection waveform is applied via input pin C/G/2, R11 and TEST/RUN switch SA to the base of transistor TR3a. Diodes D4-D5 limit the base potential of TR3a to 0.7V. With switch SA in the TEST position, potentiometer RV2 connected across the $\pm 6V$ supply is set for a d.c. zero on TEST POINT 9.

12. The negative-going mainscan deflection waveform is applied via input pin C/G/3, TEST/RUN switch SA and R1 to the base of TR1a. Diodes D1-D2 limit the

base potential of TR1a to within 0.7V from earth. With switch SA in the TEST position, potentiometer RV1 is adjusted for a d. c. zero at TEST POINT 10.

13. TR1 is a double transistor connected as a differential amplifier with the reference input at earth level. The negative-going waveform is taken from TR1b collector, inverted by TR2 and applied as input via C3, R12 and switch SA to the base of TR3a. Feedback network C1, R8 is required to reduce the high frequency response of the amplifier.

14. It will now be seen that TR3a accepts the two mainscan waveforms which are in phase, but the noise pick-up on each waveform is 180° out of phase. This results in complete cancellation of noise pick-up, this procedure being referred to as 'common mode rejection'.

15. Transistor TR3 is also a double transistor connected as a differential amplifier, with the reference input at earth level. The positive-going output at TR3b collector is inverted by TR4. The output of TR4 is applied via the TEST/RUN switches SB and SC (in the RUN position) as one input to TR5a base, which also receives as inputs the picture control volts on pin D/H/22 and the picture shift control voltage on pin C/G/8.

16. With the 12in viewing unit the picture centre control volts are applied to TR5a base via three switched resistors R27-R29, each in turn paralleled with R26 by the three contacts RLA/1, RLB/1 and RLC/1. The relays are controlled by the push-button range switches on the viewing unit control panel. Each relay has a second set of contacts which connect parallel resistors in the feedback path of the range amplifier. With the MED/SHORT range selected, RLC is energised and contacts RLC/1 and RLC/2 close. RLC/2 parallels R51 with R48, doubling the amount of negative feedback in the range-change amplifier, thus halving the gain. It is necessary, however, to ensure that the picture origin remains at the same point. To achieve this, contact RLC/1 parallels R29 with R26, doubling the input centre control volts to TR5a base, thus counteracting the effect of the gain change as far as the picture origin is concerned. With the 21in viewing unit, input pin D/H/22 is connected to earth via Junction Unit Type 12795.

17. The picture shift control voltage is a d. c. shift level controlled by the X and Y shift potentiometers on Radar Control Panel Type 11057. These are connected between the ±6V supply. The shift control voltage is applied via pin C/G/8 and resistor R25, part of the summing network R25, R26.

The range-change amplifier

18. This circuit comprises the amplifier, formed by transistor TR5 to TR9 and the limiting network, formed by transistors TR10 and TR11. The summed inputs are applied to TR5a via TEST/RUN switch SC which, when in the TEST position, allows

the amplifier to be zeroed by adjusting potentiometer RV4 and thus removing any d. c. offset voltage.

19. This amplifier incorporates switched feedback resistors to give a variable gain factor. The input resistor R23 is constant at 12.5k and the feedback resistor R48 (100k) has successively smaller resistors switched across it, to give a combined R out/R in of 8, 4, 2 and 1. With R49 switched across R46, the amplifier is in the minimum gain or maximum range condition.

20. Besides gain changing facilities, this amplifier contains the summing networks described in the preceding paragraphs.

21. Transistor TR5 is a double transistor connected as a differential amplifier, feeding a second stage of emitter-follower TR7. TR6 increases the overall loop gain and TR8 is an inverter feeding a third emitter-follower TR9.

22. The limiting network associated with TR10, TR11 is inoperative until the range amplifier output approaches the positive and negative values set by RV5 and RV6. Diodes MR16, MR9 then conduct, the negative feedback is increased and the amplifier gain falls to zero. The circuit prevents the amplifier output exceeding $\pm 4V$ even in the shortest range.

23. The output of this amplifier is applied firstly to the final deflection amplifiers as the scan A output, and secondly to a similar amplifier (TR12 to TR15) on this board which produces the anti-phase version (i. e. the scan B output) for application to the other input of the final deflection amplifiers.

24. The action of the unity gain inverting amplifier (TR12-TR15) is similar to that of the amplifier TR5-TR9, but without the limiting network. The amplifier is zeroed by the adjustment of potentiometer RV7, with the TEST/RUN switch SC at the TEST position. The output of this stage is the scan B drive waveform which is 180° out of phase with the scan A drive waveform.

Symbol channel

25. One phase of the symbol scan waveform generated in the category selection board is applied via input pin C/G/6 to the base of phase splitter TR16. This transistor produces push-pull outputs which are fed out of the board on pins C/G/23 and C/G/22 to form the symbol A and B deflection waveforms for application to the final deflection coil amplifiers.

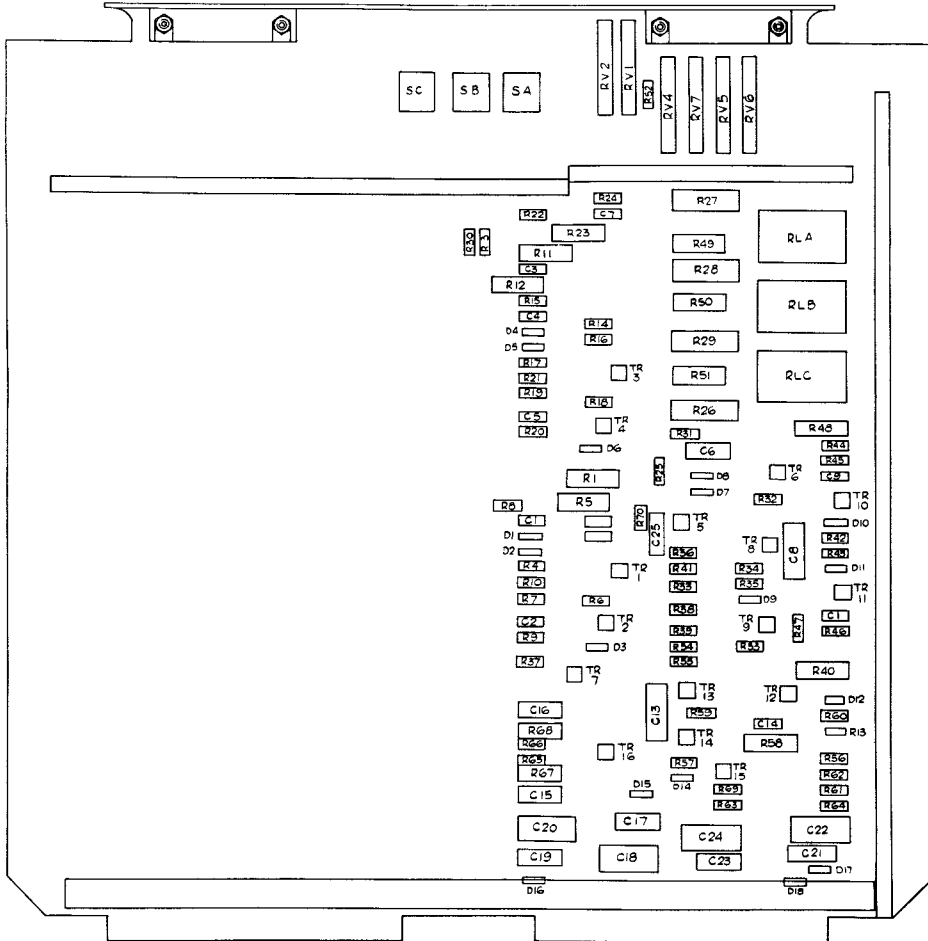
26. One deflection board handles the incoming sine component, and the other the cosine component.

Transistor protection circuit

27. Each board uses +12V and -12V, +6V and -6V stabilised d. c. supplies

provided by Power Unit Type 11600 in the 12in viewing unit and by the Power Unit Type 11606 in the 21in viewing unit. The opposite polarity supplies are interconnected through the board circuits, and if one power supply fails, the remaining supply could attempt to drive a reverse current through certain transistors. A protection circuit is included to prevent this.

28. This circuit comprises diodes D15-D18 and capacitors C17-C24. The diodes are 'reverse connected' between +12V and +6V, +6V and -0V, -6V and 0V and between -12V and -6V. With all supplies present, each diode is therefore back-biased. If a supply fails and reverse voltage appears on the line, the diode connected to it conducts and either earths the line (6V supply) or holds it to the 6V level (12V supplies). The capacitors prevent the diodes conducting on transients during normal operation and provide additional decoupling to isolate the boards from the power supply transients.



Deflection board layout MRMC (12439)

Fig.

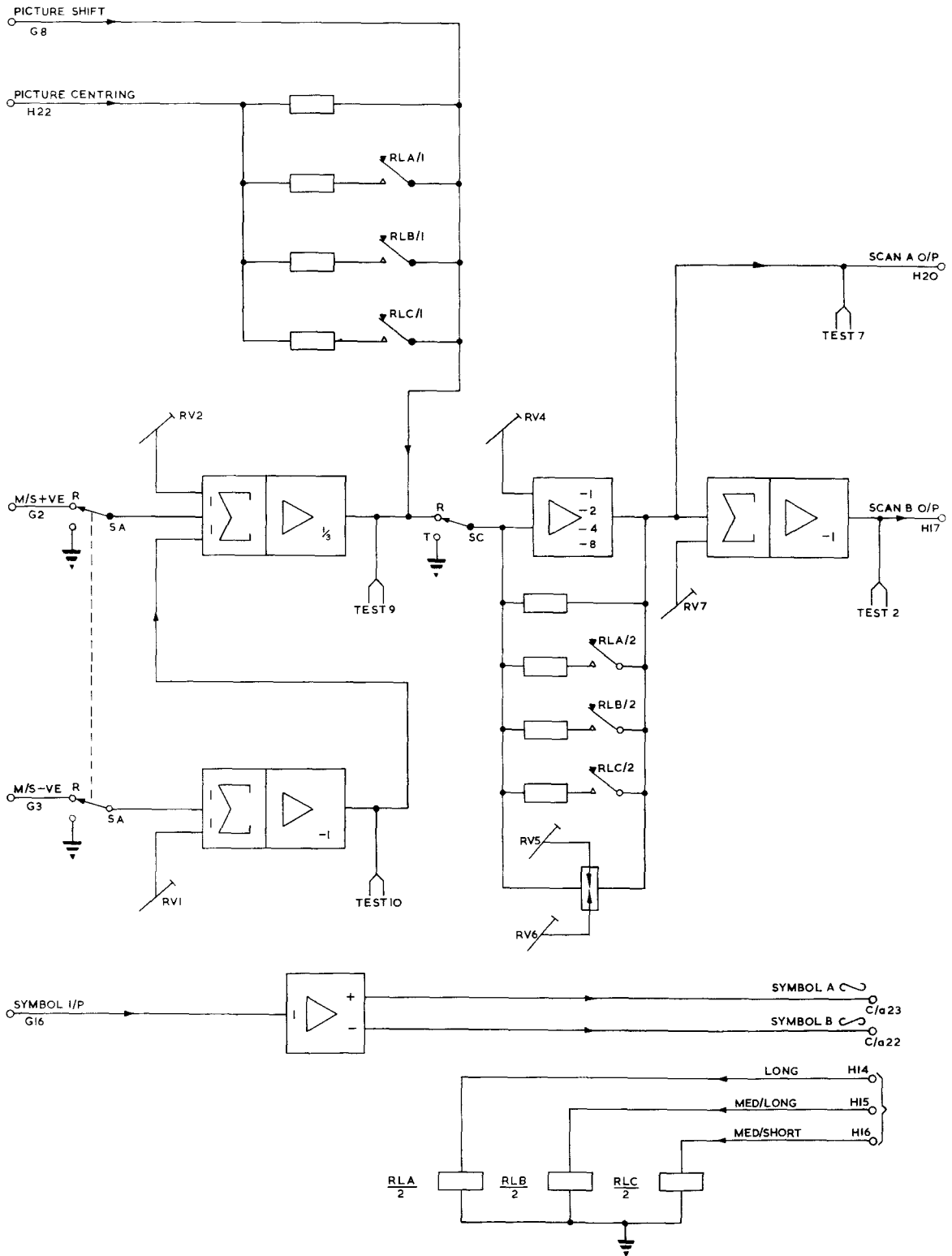
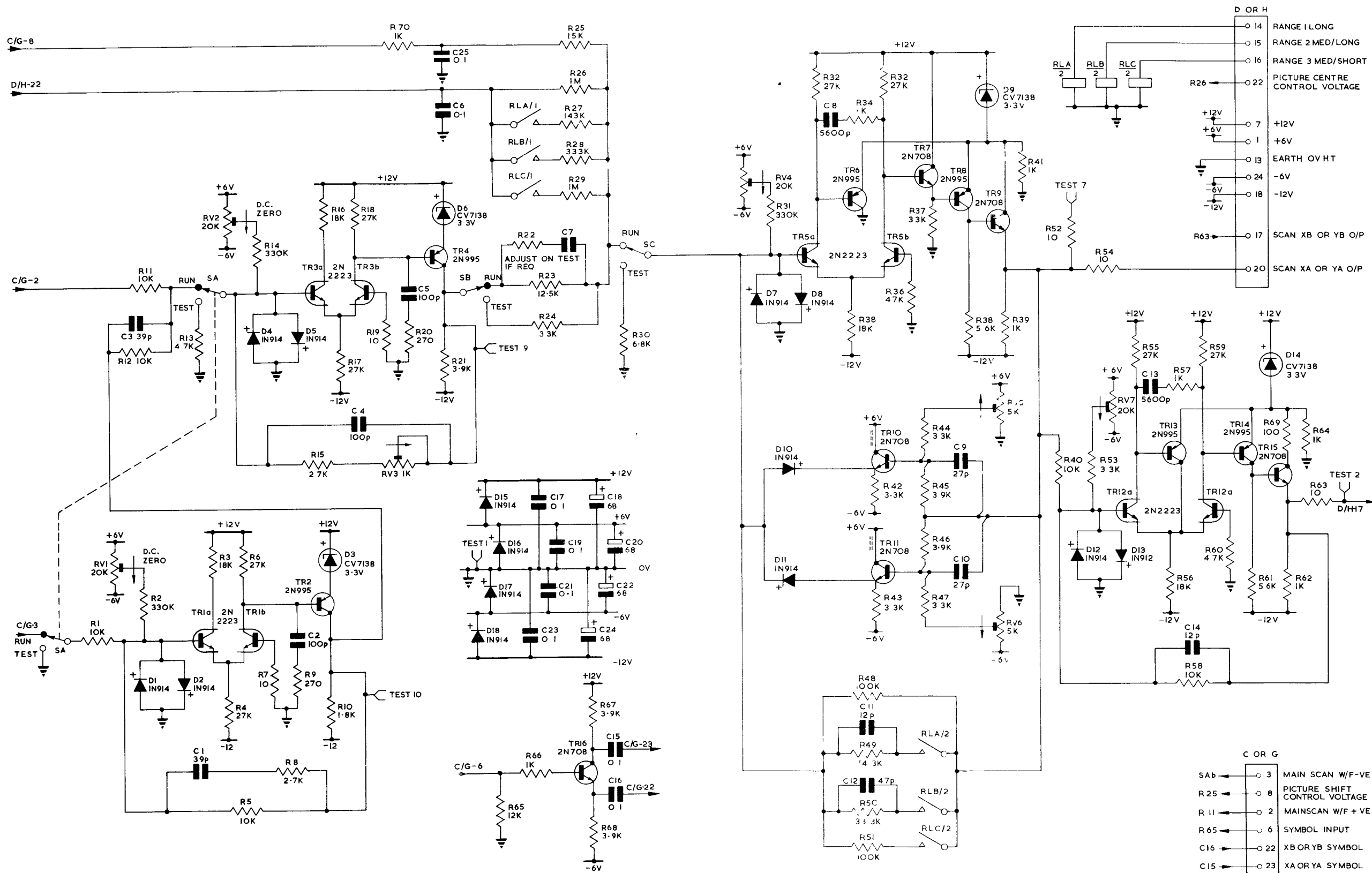


Fig. 2

Logic for deflection board MRMC (12439)

A.L.32, NOV. 71



- D OR H
- 14 RANGE 1 LONG
 - 15 RANGE 2 MED/LONG
 - 16 RANGE 3 MED/SHORT
 - 22 PICTURE CENTRE CONTROL VOLTAGE
 - 7 +12V
 - 1 +6V
 - 13 EARTH OV HT
 - 24 -6V
 - 18 -12V
 - 17 SCAN XB OR YB O/P
 - 20 SCAN XA OR YA O/P

- C OR G
- 3 MAIN SCAN W/F -VE
 - 8 PICTURE SHIFT CONTROL VOLTAGE
 - 2 MAINSCAN W/F +VE
 - 6 SYMBOL INPUT
 - 22 XB OR YB SYMBOL
 - 23 XA OR YA SYMBOL

SERVICING INFORMATION

DISPLAY SERVICING

CHAPTER 1

MAINTENANCE TECHNIQUE

LIST OF CONTENTS

	Para.
Introduction	1
Maintenance technique	2
Test equipment	10

Introduction

1. The servicing information in this and following chapters is applicable to a basic Mk.5 display and unrelated to environment. However, each display is tailored for its particular application and may be the subject of different servicing policies so that the servicing procedures are subject to local variation. For each application in which this publication is used a supplementary information unit is produced; this supplement either provides special-to-application servicing information, or indicates that the basic display procedures detailed in these chapters are appropriate. These chapters specify the test equipment required in terms of the parameters necessary for particular checks; the supplements list the common user and special-to-type test equipment available locally.

Maintenance technique

2. In previous comparative equipments of the type with which this manual is associated which employed valves throughout, a major part of the servicing and maintenance routine was concerned with adjustment of circuits to compensate for the change of valve characteristics with life, and the location and replacement of those valves approaching the end of their useful life in the equipment. In this equipment which employs transistors throughout (except for the e.h.t. rectifier) the situation is rather different, as the lifetime of transistors properly employed is such that they usually outlive the useful life of the equipment. Transistors are rather more susceptible to temperature changes than changes caused by ageing.

3. Maintenance of the equipment therefore falls into the following main categories:-

- (1) Routine checks to establish that the equipment is working to specification and therefore maintaining accuracy.
- (2) Occasional carrying-out of a setting-up procedure when accuracy requirements are not met (involving adjustments to preset controls).
- (3) Relatively rare conditions caused by a component failure which causes the equipment to be unserviceable and necessitates fault-finding.

4. Following from para.2, it is stressed that the equipment should have been running for at least sixty minutes before the categories in para.3 (1) and (2) are attempted.

5. Category (1) routine checks are listed in Chap. 2 and 3 of this section; they require no test equipment other than the viewing unit display itself. The operators and servicing engineers will gain sufficient familiarity with the presentation of the display (e.g. the range and bearing of permanent echoes) to quickly detect the occurrence of out-of-specification conditions.

6. Category (2) maintenance (the setting-up procedure) is contained in Chap.4. This procedure assumes that the equipment is serviceable. It is carried out when accuracy requirements are not met or after component replacement.

7. Category (3) maintenance will normally follow a fault condition and require a component to be replaced, in which case the relevant sub-assembly will be individually checked and set up to meet its own specifications before it is replaced in the viewing unit. Sub-assembly setting-up procedures are contained in Sect. 2 and 3.

8. Chap.6 describes the removal and replacement of the c.r.t. with the consequent adjustments to the deflection coil and focusing.

9. Chap.7 describes the maintenance of the cooling system.

Test equipment

10. The following items of test equipment are required for the setting-up procedures set out in Chap.3 and 4, and in Sect.2 and 3:-

- (1) Multimeter (accuracy $\pm 2\%$).
- (2) Double-beam oscilloscope, capable of measuring a rise time of $0.2\mu\text{s}$.
- (3) Electrostatic voltmeter, 0-18kV, (accuracy $\pm 2\%$).

- (4) Digital voltmeter (accuracy $\pm 0.02\%$).
- (5) Crystal controlled time interval/frequency counter (accuracy $\pm 0.002\%$)
- (6) Precision pulse generator.
- (7) Oscillator (not critical).
- (8) Servicing stalks for 12in and 6in. plug-in boards.

Note: No attempt should be made to set up the display circuits with test equipment whose performance is less than that mentioned above. In particular the P.U.11600 should not be adjusted without a digital voltmeter as maladjustment will affect the performance of the whole display.

CHAPTER 2

DISPLAY ACCURACY TEST (HRI)

LIST OF CONTENTS

	Para.
Introduction	1
Mainscan	4
Height line	9

LIST OF TABLES

	Table
Height accuracy table	1

Introduction

1. This chapter describes accuracy tests which may be undertaken on an HRI viewing unit when no other accuracy test, specific to the installation, is available. The tests do not require test equipment other than the display itself.

2. In general, display accuracy tests are specific to an installation and this information is provided in the appropriate supplement bound with this publication, or in the publication for the system with which the display is associated.

3. The tests require that the technician have facilities to control the aerial and height line, and for the injection of a 0° angle mark, either from the aerial or from an aerial simulator. The limits quoted in this chapter may not apply to all installations as the Mk.5 display can be adjusted or modified for higher orders of accuracy.

Mainscan

4. Switch on the viewing unit. Re-select the height line and video (including the angle and range calibration markers); rotate the mainscan brilliance fully counter-clockwise. Select centred conditions. Set the height-finder aerial nutating.

5. Set SA on the X deflection board to TEST. Set SE on the Y deflection board to TEST. Turn the brilliance control up until a spot is visible on the centre of the CRT. Alternately select the longest and shortest range scales and check that the spot does not noticeably 'jump'.
6. Set SE on the Y deflection board to RUN. Select the shortest range scale. Turn up the brilliance until a vertical trace is observed. Check that there is no deflection in the X axis.
7. Set SE on the Y deflection board to TEST and SA on the X deflection board to RUN. Observe that a horizontal trace is produced and that there is no deflection in the Y axis.
8. On the Y deflection board set SE to RUN and SH to TEST. Observe the horizontal trace and check that no Y deflection is present. Set all switches to RUN and reset the brilliance level as necessary.

Height line

9. Select elevation and range calibration markers; select the height line. Adjust their gain controls for optimum brilliance. Set SG on the Y deflection board to TEST.
10. Set the height line to maximum range. On the operator's control panel depress the CHECK VERNIER push-button and adjust the VERNIER control until the height line overlays the 0° mainscan (at the 0° angle mark if this can be displayed). De-select the CHECK VERNIER.
11. Using the height control, set the height meter to zero feet. Operate the CHECK VERNIER push-button a few times and check that the position of the height line on the CRT does not change as the switch is operated.
12. Adjust the height line so that it touches the range markers in turn; check that the range read-out coincides with the range marker in each case.
13. Mark the origin of the trace on the implosion screen. Set the height control to the maximum display height. Check that the height line is now $7\frac{1}{2}$ in. from the trace origin mark.
14. Adjust the height control so that the height line intersects the various angle markers. The expected height meter readings for the 40-mile range marker are given in Table 1; for displays which do not have a 40-mile range marker or angle markers as shown in the table, the expected height reading may be calculated from:-

$$\text{height} = \text{range} \times \sin \theta$$

where θ is the nutation angle and the height and range are in feet. A data mile is 6000 ft and a nautical mile is 6080 ft. The calculated height and indicated height should agree within $\pm 1\%$.

15. Set SG to RUN; this applies a downward curvature to the height line which represents the earth's curvature. Adjust the height control so that the height line intercepts the 0° mainscan at 40 nautical miles. Check that the height meter reads 1062 ft $\pm 2\%$. For displays calibrated in data miles, or which have no 40-miles marker, the height may be calculated from: -

$$\text{height} = 2/3 \text{ range}^2$$

where height is in feet and range is in nautical miles. For displays calibrated in data miles the formula becomes: -

$$\text{height} = 2/3 (0.985 \times \text{range})^2$$

16. Cause the heightfinder aerial to slew to various positions of azimuth from which known salient permanent echoes are returned. Adjust the tip of the height line to coincide with these echoes and check that the range 'readout' agrees with the actual ranges to within $\pm 0.5\%$ r.m.s. of actual range or $\pm 0.25\%$ r.m.s. of maximum display range, whichever is the greater.

17. This completes the display accuracy testing.

TABLE 1

Height accuracy table

Angle of elevation	Calculated heights	
	at 40 nautical miles	at 40 data miles
Degrees	Feet	Feet
1	4,244	4,200
2	8,488	8,376
$2\frac{1}{2}^*$	10,608	10,460
3	12,730	12,550
4	16,970	16,750
5	21,200	20,930

Angle of elevation	Calculated heights	
	at 40 nautical miles	at 40 data miles
Degrees	Feet	Feet
6	25,420	25,080
7	29,640	29,260
7½*	31,750	31,320
8	33,850	33,410
9	38,040	37,410
10	42,230	41,660

*Angles of elevation at which elevation markers are produced by Radar Type HF200 aerial.

CHAPTER 3

DISPLAY ACCURACY TEST (PPI)

LIST OF CONTENTS

	Para.
Introduction	1
The mainscan	4
The interscan	13

Introduction

1. This chapter describes an accuracy test which may be undertaken on PPI viewing units when no other accuracy test, specific to an installation, is available. The test requires no test equipment other than the display itself.
2. In general, display accuracy tests are specific to an installation and such information is provided in the appropriate supplement bound with this publication or as part of servicing information for the system with which the display is associated.
3. In the event of the viewing unit failing to meet the limits given in this chapter, the setting-up procedure given in Chap.4, in the appropriate supplement or in the system handbook must be undertaken. The limits given in this chapter are general for Mk.5 displays, but certain applications of the display may be tailored to conform to tighter margins of tolerance.

The mainscan

4. Switch on the viewing unit. De-select 'interscan' and 'videos' on the operator's control panel, rotate the mainscan brilliance fully anti-clockwise, and set SH on the X deflection board to 'test'. Turn up the brilliance until a vertical trace is observed. Select the shortest display range scale. Select 'centred' conditions.
5. Observe the vertical trace and check that no deflection in the X axis is present; X deflection will show most noticeably at the origin.

6. Set SH on the X deflection board to 'run' and SH on the Y deflection board to 'test'. Observe the horizontal trace and check that no deflection in the Y axis is present.

7. Set SH on the Y board to 'run'. Set SC on both X and Y boards to 'test'. Set SA and SB on the X board to 'test'. Repeat the observations of para.5. Select the longest range scale and check that the trace passes through the North and South compass rose marks; accuracy should be better than 0.5° . Select the shortest range scale.

8. Set SA and SB on the X board to 'run' and SA and SB on the Y board to 'test'. Repeat the observations of para.6. Select the longest range scale and check that the trace passes through the East and West compass rose marks; accuracy should be better than 0.5° .

9. Set SA and SB on the Y board to 'run'. Set SC on both X and Y boards to 'run'.

10. Increase the mainscan brilliance to obtain a reasonably bright picture. Check that the picture origin is centred on the centre graticule cross and that the picture is circular and of the correct size by observing that the range calibration ring corresponding to the maximum range of the display touches the inner-end of the 1° graticule marks round the entire c.r.t. perimeter. Check that the traces cease about 5n.m. beyond the display maximum range. Alternatively, select longest and shortest range scales; check that the picture origin does not noticeably 'jump'.

11. With the picture set at its longest range scale, select radar video and check the bearings of known salient permanent echoes (preferably one in each quadrant) against the indicated bearing of these echoes on the display. Accuracy should be better than $\pm 1.5^\circ$.

12. The test described above has checked the following features:-

- (1) The zeros, gains and symmetrical amplification of the various invertors, demodulators, timebase circuits and deflection amplifiers common to the mainscan, and the peak amplitude of the resolver drive waveform.
- (2) The orientation of the c.r.t. deflection coil.
- (3) The interval (or 'length') of the mainscan gate.
- (4) The orientation of the aerial resolver on the aerial shaft.

The interscan

13. Select 'interscan' and adjust line brilliance for suitable interscan

brightness. Select the centred condition of the interscan. Ensure that the origin of the interscan and mainscan coincide exactly. Adjust the interscan length so that it touches a range marker approximately $4/5$ of maximum range. Observe that the value indicated in the range indicator agrees with the range marker within 0.5%. Using the bearing control, rotate the interscan line around the origin in 30° steps and ensure that the interscan line continues to just touch the range marker.

14. Repeat the procedure of para.13 on all other ranges, using a range marker near the edge of the CRT.

15. Adjust the end of the interscan to coincide with permanent echoes of known range; check that the indicated ranges agree with the known ranges within $\pm 0.5\%$ r.m.s. of the actual range or 0.24% r.m.s. of the maximum display range, whichever is greater. Check that the indicated bearings agree within $\pm 0.5^\circ$ of the mainscan bearings obtained in para.11.

16. The tests in para.13 to 16 check:-

- (1) The zeros, gains and symmetrical amplification of interscan channels.
- (2) The scaling of the voltages across the range and bearing potentiometers.
- (3) The orientation of the bearing control with respect to the read-off scale.

CHAPTER 4

DISPLAY SETTING-UP PROCEDURE (HRI)

LIST OF CONTENTS

	Para.
INTRODUCTION	1
POWER SUPPLIES	2
Power Unit 11600	3
E.H.T. Power Unit 11601	5
TIMING BOARD MJE	13
Mainscan gate length	19
Sampling gate length	20
Synchro supply squarewave generation	21
Synchro supply circuits	22
X DEFLECTION BOARD MRK	26
Range change amplifier adjustment	27
Range change amplifier limiting adjustments	28
Timebase adjustments	29
Y DEFLECTION BOARD MRG & MRH	31
Modulator adjustments	32
Interscan control voltage adjustments	35
Timebase adjustments	36
Interscan buffer amplifier adjustments	37
Range change amplifier adjustments	38
Range change amplifier limiting adjustment	39
VIDEO BOARD MFD	41
Video channel balance adjustments	42
Range calibration adjustments	43
DEFLECTION COIL DRIVE AMPLIFIERS	49
FINAL SETTING-UP PROCEDURE	
Final deflection amplifier	53
X and Y deflection boards	56
Video board	62
Timing board	64

INTRODUCTION

1. The following procedure will be carried out on initial installation of the equipment in the operation's centre or when it is suspected that the performance has deteriorated outside the specified limits.

POWER SUPPLIES

2. It is assumed that the terminal strip TSF has been correctly linked so that the primary of the transformer is correctly tapped for the specified mains supply voltage. (Refer to power unit circuit for details).

Power Unit Type 11600

Test equipment:-
Digital voltmeter

3. First ensure that all the printed wiring boards are correctly fitted; ensure that the X2 cut-out on the power unit is actioned. Operate the STANDBY switch on the viewing unit control panel.

4. With a D.V.M. measure in turn the voltages with respect to Test 3 (0V) at the test points as follows:-

Test 1	+6V
Test 2	-6V
Test 4	-12V
Test 5	+12V

Press the OFF button on the viewing unit control panel.

Note: No attempt should be made to adjust the presets associated with the power unit except under the circumstances given in Chapter 1.

E.H.T. Power Unit 11601

Test equipment:-
Electrostatic Voltmeter 0-18kV

5. Set the focus control on the viewing unit control panel to the mid-position point, disconnect the final anode fly-lead from the c.r.t. and monitor the e.h.t. with an electrostatic voltmeter with respect to the chassis of the power unit.

6. Press the STANDBY and ON press buttons on the viewing unit control panel and note the reading on the voltmeter which should be 15kV.

7. Press the STANDBY and OFF press buttons in turn, remove the voltmeter connections and re-connect the c. r. t. final anode lead to the cap.
8. If it is necessary to adjust the e. h. t. voltage proceed as follows.
9. Switch off the mains supply to the equipment, remove the junction pack from the rear of the viewing unit after releasing the securing screw. Withdraw the viewing unit from its fibre glass cover and re-connect the junction pack to the viewing unit.
10. Re-connect the electrostatic voltmeter to the c. r. t. anode fly-lead and signal earth and switch on the mains supply. Press the STANDBY and ON press buttons and adjust RV1 on the e. h. t. unit for a reading of 15kV on the voltmeter, ensuring that the focus control is at its mid-position point.
11. Press the STANDBY and OFF press buttons and switch off the mains supply to the equipment. Remove the voltmeter and re-connect the c. r. t. final anode lead to the cap.
12. Remove the junction pack from the rear of the viewing unit and replace the fibre glass cover. Re-connect the junction pack and switch on the mains supply to the equipment.

TIMING BOARD MJE

Test equipment:-

 Servicing stalk
 Oscilloscope

13. Ensure that the aerial resolver, the radar trigger and the video signals are available and correctly connected to the junction panel.
14. Ensure that the display is switched. Remove the timing printed wiring board and insert the servicing bracket, finally place the timing board in the bracket.
15. Press the STANDBY button, and if a radar pre-trigger pulse is available proceed as follows. If no pre-pulse is available proceed as detailed in paragraph 17.

- 16.
- (1) Connect the oscilloscope trigger input to monitor point 1 on the timing board. Monitor the p. r. f. signal at MSKT1 on the Y1 channel. Connect the Y2 input to the collector of TR62 on the timing board.
 - (2) Set the oscilloscope vertical sensitivity to 5V/cm and the sweep speed to 1/us/cm and obtaining trigger from the monitor point 1 on the timing board.
 - (3) Note the relationship between the transmitter firing pulse on Y1 and the pulse at the collector of TR62.
 - (4) Adjust RV12 until the time interval between the trailing edge of the delay pulse at TR62 collector and the leading edge of the p. r. f. pulse corresponds to the pre-trigger time provided on site.

17. If the radar system associated with the display equipment has no pre-pulse trigger facilities the following links should be modified:-

- (1) Remove link B to C; Fit link A to C.
 - (2) Remove link R to S; Fit link S to W.
 - (3) Set the oscilloscope vertical sensitivity to 5V/cm and the sweep speed to 1/us/cm and obtaining trigger from the monitor point 1 on the timing board.
 - (4) Monitor TR65 collector and set the positive pulse width to a minimum with RV6.
- 18.
- (1) Connect the oscilloscope to monitor point 12 triggering from the same point. Set the vertical sensitivity to 5V/cm and the sweep speed to 100ms/cm.
 - (2) The squarewave output of the interscan timer will be displayed on the oscilloscope. Adjust RV11 for one cycle of the observed waveform to be 100ms duration.

Mainscan gate length

- 19.
- (1) Connect the oscilloscope to monitor point 16 triggering from monitor point 1.
 - (2) Set the vertical sensitivity to 5V/cm and the sweep speed to 500/us/cm.

- (3) The positive timebase gate waveform will be displayed on the oscilloscope. Using RV5 adjust the gate length according to the formula below:-
 - (a) Maximum display range (nautical miles) X 12.36/us.
 - (b) Maximum display range (data miles) X 12.2/us.
 - (c) Maximum display range (metres) X 6.69/us.

Sampling gate length

20.
 - (1) Connect the oscilloscope to monitor point 3 and obtain trigger from the same point.
 - (2) Set the oscilloscope for a negative trigger input and the vertical sensitivity to 5V/cm and the sweep speed to 10/us/cm.
 - (3) The negative sampling gate waveform will be displayed. Adjust RV8 for the negative excursion to be 30/us in duration.

Synchro supply squarewave generation

21.
 - (1) Connect the oscilloscope to the collector of TR16. Set the vertical sensitivity to 5V/cm and the sweep speed to 500/us/cm. Trigger from monitor point 3.
 - (2) The output of the squarewave generator will be displayed. Set the mark/space ratio to 1:1 by adjusting RV4.
 - (3) Set the oscilloscope trigger mode to internal and check the adjustment in (2) before switching the internal trigger mode alternately positive and negative, re-adjusting RV4 if necessary.

Synchro supply circuits

22.
 - (1) Set potentiometers RV7, RV9 and RV10 to their mid-positions. (Initial installation only.)
 - (2) Connect the oscilloscope to the junction of C71 R203, with internal trigger mode. Set the vertical sensitivity to 0.1V/cm and the sweep speed to 1ms/cm.

- (3) The oscilloscope is connected to the centre point of the synchro supply transformer. Balance the output of the resolver power amplifier by adjusting RV10 to minimise the ~~800~~ cycle component in the observed waveform.
- (4) Transfer the oscilloscope to monitor point 2. Set the vertical sensitivity to 10V/cm and adjust RV7 for the observed waveform to be 35V peak-to-peak in amplitude.

Note: It may be necessary to adjust RV9 to achieve this condition. If so adjust RV9 for a level slightly in excess and then re-adjust RV7.

23. Connect a voltmeter on the 10V d.c. range to monitor point 8 and adjust RV9 for a d.c. potential of 4.0V with respect to earth.

24. (1) Connect the oscilloscope to monitor point 3 and obtain trigger from the same point. Adjust the oscilloscope so that it is being triggered from the positive trailing edge of the negative going sampling gate.
- (2) Connect the oscilloscope to monitor point 2 with the vertical sensitivity set to 10V/cm and the sweep speed to 10ms/cm triggered as before.
- (3) Adjust the phasing control RV3 so that a peak or trough of the observed sine wave is coincident with the start of the trace.

25. This completes the setting-up procedure for the timing board, so press the OFF button on the viewing unit control panel, remove the board from the servicing bracket, withdraw the servicing bracket and insert the board in its normal position.

X DEFLECTION BOARD MRK

Test equipment:-

 Servicing stalk
 Oscilloscope

26. Ensure that the OFF button on the viewing unit control panel has been pressed, remove the X deflection boards, insert the servicing bracket and attach the board in the bracket. Finally press the STANDBY button.

Range change amplifier adjustment

27. (1) Set switch SA on the X deflection board to TEST. Connect the oscilloscope to monitor point 5 obtaining trigger from the monitor point 1 on the timing board.

- (2) Set the vertical sensitivity to 20mV/cm and adjust RV2 for the output to be 0V +10mV with respect to signal earth at monitor point 3 on the power unit.
- (3) Connect the oscilloscope to monitor point 13 and adjust RV6 for the output to be 0V +10mV with respect to signal earth at monitor point 3 on the power unit.
- (4) Set switch SA to the RUN position.

Range change amplifier limiting adjustments

28.
 - (1) Connect the oscilloscope to monitor point 5, obtaining trigger as before. Set the vertical sensitivity to 2V/cm and select the shortest range on the viewing unit control panel.
 - (2) The observed waveform should be a sawtooth. Adjust RV3 so that the onset of limiting occurs at -4V.
 - (3) Adjust RV4 so that the onset of limiting of the sawtooth occurs at +4V.
 - (4) Select the longest range.

Timebase adjustments

29.
 - (1) Connect the oscilloscope to monitor point 6 and obtaining trigger from monitor point 1 on the timing board.
 - (2) Set the vertical sensitivity to 2V/cm. Adjust RV1 so that the start of the negative going sawtooth waveform commences from a level of +2.8V.
 - (3) Adjust RV5 so that the sawtooth runs down to -2.8V in the interval given in the table of paragraph 19.

30. This completes the setting-up procedure for the X deflection board so press the OFF button on the viewing unit control panel, remove the oscilloscope connections and the board from the servicing bracket, withdraw the bracket and insert the board in its normal position.

Y DEFLECTION BOARD MRG & MRH

Test equipment:-

 Servicing stalk

 Oscilloscope

31. Ensure that the OFF button on the viewing unit control panel has been pressed, remove the Y deflection board, insert the servicing bracket and attach the board in the bracket. Finally press the STANDBY button.

Demodulator adjustments

32. (1) Set switches SA and SB on the Y deflection board to TEST.
- (2) Connect the oscilloscope to monitor point 10 obtaining trigger from monitor point 3 on the timing board. Set the vertical sensitivity to 5mV/cm and the sweep speed to 1ms/cm.
- (3) Adjust RV1 for the d.c. output level observed to be 0V \pm 10mV with respect to signal earth at monitor point 3 on the power unit.
- (4) Connect the oscilloscope to monitor point 14 and adjust RV2 for the d.c. output level observed during the 30/ μ s sampling pulse time to be 0V \pm 10mV with respect to signal earth at monitor point 3 on the power unit.
- (5) Adjust RV6 for a scan sawtooth of less than 10mV.
33. (1) Set switch SC to TEST and connect the oscilloscope to monitor point 9.
- (2) Adjust RV12 for the inverter output to be 0V \pm 10mV with respect to signal earth at monitor point 3 on the power unit.
- (3) Set switches SA, SB and SC to RUN.
34. (1) Connect the oscilloscope to monitor point 14 obtaining the trigger as before. Set the vertical sensitivity to 2V/cm.
- (2) With the aerial nutating through its greatest angle observe the output d.c. level which will be modulated in amplitude by the aerial movement. Adjust RV4 for the positive peak modulation to be +4V \pm 0.1V.

Interscan control voltage adjustments

35. (1) Set switch SD to the TEST position. On the operator's control panel press the LINE ON/OFF button to ON.
- (2) Connect the oscilloscope to the monitor point 8 obtaining trigger from monitor point 12 on the timing board. Set the vertical sensitivity to 5mV/cm.
- (3) Adjust RV11 for the output to be 0V \pm 10mV with reference to the d.c. level obtained during the mainscan period.
- (4) Set switch SD to the RUN position.

Timebase adjustments

36. (1) Connect the oscilloscope to monitor point 7 obtaining trigger from monitor point 1 on the timing board and switch SH to the TEST position.
- (2) With the vertical sensitivity set to 10mV/cm and the oscilloscope d.c. coupled adjust RV10 for a scan sawtooth of less than 10mV.
- (3) Set the vertical sensitivity to 1V/cm, and adjust RV9 for the output to be +2.8V with respect to signal earth at monitor point 3 on the power unit.
- (4) RV8 is adjusted later.
- (5) Set SH to the RUN position.

Interscan buffer amplifier adjustment

37. (1) Set switches SA, SB and SG to the TEST position, connect the oscilloscope to monitor point 11, and trigger from monitor point 12 on the timing board.
- (2) Set the vertical sensitivity to 10mV/cm and adjust RV7 for the output during the interscan period to be 0V \pm 10mV with respect to signal earth at monitor point 3 on the power unit.
- (3) Re-adjust RV2 for the output during the mainscan period to be 0V \pm 10mV with respect to signal earth at monitor point 3 on the power unit.

- (4) Set switches SA, SB and SG to RUN.

Range change amplifier adjustment

38.
 - (1) Set switch SE to the TEST position. Connect the oscilloscope to monitor point 1 and obtain trigger from the monitor point 1 on the timing board.
 - (2) Set the vertical sensitivity to 20mV/cm and adjust RV13 for the output to be 0V \pm 10mV with respect to signal earth at monitor point 3 on the power unit.
 - (3) Connect the oscilloscope to monitor point 5 and adjust RV14 for the output to be 0V \pm 10mV with respect to signal earth at monitor point 3 on the power unit.
 - (4) Set switch SE to the RUN position.

Range change amplifier limiting adjustment

39.
 - (1) Connect the oscilloscope to monitor point 1, obtain trigger as before. Set the vertical sensitivity to 2V/cm and select the shortest range on the viewing unit control panel.
 - (2) The observed waveform should be a sawtooth, the amplitude of which will be modulated by the aerial nutation. Adjust RV15 so that the onset of limiting of the sawtooth occurs at -4V. (It will be necessary to move the picture shift to achieve negative limiting.)
 - (3) Adjust RV16 so that the onset of limiting of the sawtooth occurs at +4V.
 - (4) Select the longest range.

40. This completes the setting-up procedure for the Y deflection board so press the OFF button on the viewing unit control panel, remove the oscilloscope connections and the board from the servicing bracket, withdraw the bracket and insert the board in its normal position.

VIDEO BOARD MFD

Test equipment:-

 Servicing stalk
 Oscilloscope
 Digital Voltmeter

41. Ensure that the OFF button on the viewing unit control panel has

been pressed, remove the video printed wiring board and insert the servicing bracket, and finally place the video board in the bracket. Press the STANDBY press button.

Video channel balance adjustments

42. (1) Connect the voltmeter set to its 10V d.c. range between the collectors of TR1 and 2.
- (2) Select video 1 on the operator's control panel ensuring that the calibration and elevation markers are at OFF and set all the gain controls fully clockwise on the viewing unit control panel.
- (3) Adjust RV1 to obtain $0V \pm 0.1V$ on the voltmeter.
- (4) Set video 1 to OFF and video 2 to ON; with the voltmeter connected as before adjust RV2 to obtain $0V \pm 0.1V$.
- (5) Repeat this procedure for video channel 3 (RV3 adjustment) and channel 4 (RV4 adjustment).

Range calibration adjustments

43. No attempt must be made to adjust the calibration marker generator unless the test equipment of the required accuracy is available; the procedure is detailed in Sect. 3, Chap. 4.
44. (1) Connect the oscilloscope to the base of TR54 obtaining trigger from monitor point 1 on the timing board. Set the vertical sensitivity to $2V/cm$ and the sweep speed to $200/\mu s/cm$.
- (2) Adjust RV12 to obtain a constant amplitude of the observed sinewave to within $\pm 5\%$.
45. (1) Connect the oscilloscope Y1 input to the collector of TR62 and the Y2 input to monitor point 10. (Fine marker generator output.)
- (2) Set the vertical sensitivity to $5V/cm$ and the sweep speed to $200/\mu s/cm$. Adjust RV15 to set the length of the observed negative gate pulses on the Y1 plate to lie between 1.2 and 1.5 times the fine calibration interval.

46. (1) Connect the oscilloscope Y1 input to monitor point 11. (Coarse marker generator output.)
- (2) Adjust RV14 to obtain the required division. There will be a range of movement of RV14 over which this is possible. Set the control to the centre of this range.
- (3) Disconnect the oscilloscope.
47. (1) Connect the oscilloscope to pin PBL 2 on the video board, set the vertical sensitivity to 10V/cm and the sweep to 1ms/cm obtaining trigger from the monitor point 1 on the timing board.
- (2) Set the 'coarse' range marks gain control on the viewing unit control panel fully clockwise and select the 'coarse' range markers on the operator's control panel.
- (3) Adjust RV7 on the video board for the amplitude of the coarse range markers to be 25V \pm 1V.
- (4) Adjust RV5 on the video board so that the mainscan level is at -5V \pm 1V with respect to the between mainscan level.
- (5) Adjust RV8 for an interscan level of -10V \pm 1V with respect to the between mainscan level.
- (6) Set RV11 fully anti-clockwise.
48. This completes the setting-up procedure for the video board. Press the OFF button on the viewing unit control panel, remove the board from the servicing bracket, withdraw the bracket and insert the board in its normal position.

DEFLECTION COIL DRIVE AMPLIFIER

Test equipment:-
Digital voltmeter

49. A real care must be exercised to avoid shorting the adjacent pins with the voltmeter probe. A sleeved probe should be used and when there is any doubt the viewing unit d.c. supplies should be switched off when connecting or removing the monitor probe.
50. (1) Press the STANDBY and OFF press-buttons on the viewing unit control panel.

- (2) Remove the X deflection board. Press the STANDBY button. Monitor the XA output of the final deflection amplifier at TS. B2 with a voltmeter set to the maximum sensitivity range.
 - (3) Adjust RV1 on the final deflection amplifier for the output level to be $-0.6V \pm 10mV$ with respect to signal earth at monitor point 3 on the power unit.
 - (4) Monitor the XB output of the final deflection amplifier at TS. A9 with a voltmeter set to the maximum sensitivity range.
 - (5) Adjust RV3 on the final deflection amplifier for the observed output level to be $-0.6V \pm 10mV$ with respect to signal earth at monitor point 3 on the power unit.
 - (6) Press the OFF button and replace the X deflection board.
51. (1) Remove the Y deflection board and repeat this adjustment for the Y channel, monitoring the YB output at TS. A2 and adjusting RV2 and the YA output at TS. B9 and adjusting RV4.
- (2) Replace the Y deflection board.
52. This completes the initial setting-up of the viewing unit.

FINAL SETTING-UP PROCEDURE

Final deflection amplifier

Test equipment:-

Digital voltmeter
Oscilloscope

53. (1) Remove both deflection boards and operate the STANDBY push-button on the viewing unit control panel.
- (2) Press the LINE ON/OFF button on the operator's control panel to OFF, and set both coarse and fine range and elevation marks to OFF.
- (3) Turn the RADAR BRILL. control on the viewing unit control panel fully anti-clockwise and press the ON button on the viewing unit control panel.

- (4) Turn the RADAR BRILL. control slowly clockwise until a spot is just visible on the centre of the c.r.t. face. Trip out X3 on the power unit and note any change of the spot position.
- (5) Reset cut-out X3. If any movement is apparent in the X direction adjust RV1 or RV3, or movement in the Y direction adjust RV2 or RV4 on the final deflection amplifier.

54. The actual potentiometer to be adjusted must be the one which increases the current in the coil. This may be checked by carefully observing the voltages at TS.A2, A9, TS.B2 and B9 on the final deflection amplifier to see that in each case the voltage does not become more positive than -0.6V d.c. as previously obtained. Switch the viewing unit to OFF.

55. Replace both deflection boards.

X and Y deflection boards

56.
 - (1) Switch the viewing unit to STANDBY and to ON. Ensure that all switches are in the RUN position. Select the longest range button on the viewing unit control panel and select RADAR SHIFT. Position the mainscan origin to the centre of the c.r.t.
 - (2) Set the SA switch on the X deflection board to the TEST position and alternately select the shortest and longest range button, note any positional change of the origin of the trace. Adjust RV1 on the X deflection board to remove any jump observed along the X axis.
57.
 - (1) Press the STANDBY and OFF button on the viewing unit control panel, remove the Y deflection board, insert the servicing bracket and attach the board in the bracket. Finally press the STANDBY and ON buttons on the viewing unit control panel.
 - (2) Select the shortest range button on the viewing unit control panel. Select RADAR SHIFT on the operator's control panel.
 - (3) Set the LINE ON/OFF to ON and adjust LINE BRILL. for the optimum level of brilliance.
58.
 - (1) Draw a square of $7\frac{1}{2}$ inch side on the implosion screen of the viewing unit and adjust the RADAR SHIFT controls so as to position the origin of the mainscan trace in the bottom left hand corner of the marked square.

- (2) Set the range control for a read-out equal to the maximum display range and the SA and SB switches on the Y deflection board to TEST.
 - (3) Connect the oscilloscope to monitor point 11 on the Y deflection board and set the vertical sensitivity to 50mV/cm obtaining trigger from monitor point 12 on the timing board MJE.
 - (4) Adjust RV7 on the Y deflection board for the base line of the sawtooth waveform during the interscan period to be the same level as the mainscan period.
 - (5) Set the SA and SB switches to RUN and the SG switch to TEST on the Y deflection board.
- 59.
- (1) Set the aerial nutating and select the longest range-scale button on the viewing unit.
 - (2) Select the elevation marks button on the operator's control panel and adjust the elevation markers gain control for optimum marker brilliance.
- 60.
- (1) Set the height control on the operator's control panel for a readout equal to the maximum display height and adjust RV17 on the Y deflection board so that the height line just overlays the top line of the 7½in square on the c. r. t. screen.
 - (2) Set the height control on the operator's control panel for a readout of 17 365 metres or 42 220ft as appropriate.
 - (3) Adjust RV8 on the Y deflection board for the height line to intersect the 10° mainscan at the 100km range marker point or at 40n. m. as appropriate.
 - (4) Set the SA and SB switches to TEST and the SG switch to RUN on the Y deflection board.
 - (5) Set the height control on the operator's control panel for a readout of 589 metres (or 1062ft).
 - (6) Adjust RV20 on the Y deflection board for the end of the height line to intersect the 0° mainscan at the 100km (or 40n. m.) marker point.

- (7) Repeat the procedure in paragraphs 58 and 59 until no further adjustment is necessary to satisfy both conditions.

61. Press the STANDBY and OFF buttons on the viewing unit control panel, remove the Y deflection board from the servicing bracket and replace it in its normal position.

Video board

62.
 - (1) Press the STANDBY and ON buttons on the viewing unit control panel, ensure that the LINE ON/OFF switch on the operator's control panel is set to ON and set RV11 (overall brilliance) on the video board fully anti-clockwise.
 - (2) Set the RADAR BRILL. control fully anti-clockwise and the LINE BRILL. control fully clockwise, and adjust RV11 on the video board for a just overbright interscan.
 - (3) Re-adjust the two brilliance controls for an optimum brilliance setting.
63. Adjust RV10 on the video board so that octagonal blanking occurs just outside the periphery of the c. r. t. Press the STANDBY and OFF buttons on the viewing unit control panel.

Timing board

64.
 - (1) Ensure that the STANDBY and OFF buttons on the viewing unit control panel have been pressed, remove the timing board, insert the servicing bracket and attach the board in the bracket. Finally press the STANDBY and ON buttons on the viewing unit control panel.
 - (2) Connect the oscilloscope to the junction of C37 and TR33 collector, set the vertical sensitivity to 1V/cm and the sweep speed to 1ms/cm obtaining trigger from monitor point 1 on the timing board.
 - (3) Adjust RV1 on the timing board for the positive peaks to occur at -2V d. c. $\pm 0.1V$.
65.
 - (1) Set the aerial accurately to an elevation of zero degrees and the height control on the operator's control panel for a read-out of zero metres.
 - (2) Select the longest range scale and adjust RV5 on the timing board for a mainscan length of approximately 5% longer than the maximum display range.

- (3) Set the range control on the operator's control panel for a readout of $1/5$ maximum range and adjust RV2 on the timing board so that the end of the interscan line just overlays the appropriate range marker.
 - (4) Set the range control for a read-out of $4/5$ maximum range and adjust RV5 on the timing board so that the end of the interscan line just overlays the appropriate marker.
 - (5) Repeat the procedure in sub-para. (1) to (4) but use the RADAR SHIFT facilities to centre each appropriate range before finally adjusting RV2 and RV5.
- 66.
- (1) Adjust RV1 on the timing board to set the mainscan length to the maximum display range.
 - (2) Press the STANDBY and OFF buttons on the viewing unit control panel, remove the timing board from the servicing bracket and replace the board in its normal position.
67. This now completes the display setting-up. Replace the top cover.

CHAPTER 5

DISPLAY SETTING-UP PROCEDURES (P.P.I.)

LIST OF CONTENTS

	Para.
INTRODUCTION	1
POWER SUPPLIES	2
Power Unit 11600	3
E.H.T. Power Unit 11601	5
TIMING BOARD MJE	13
Mainscan gate length	19
Sampling gate length	20
Synchro supply square-wave generation	21
Synchro supply circuits	22
X AND Y DEFLECTION BOARDS MRG	26
Demodulator adjustments	27
Interscan control voltage adjustments	30
Timebase adjustments... ..	31
Interscan buffer amplifier adjustment	32
Range change amplifier adjustment	33
Range change amplifier limiting adjustments	34
VIDEO BOARD MFD	37
Video channel balance adjustments	38
Range calibration adjustments	41
DEFLECTION COIL DRIVE AMPLIFIER	47
FINAL SETTING-UP PROCEDURE	
Final deflection amplifier	51
X and Y deflection boards	54
Video board	62
Timing board	64

INTRODUCTION

1. The following procedure will be carried out on initial installation of the equipment in the operations centre or when it is suspected that the performance has deteriorated outside the specified limits.

POWER SUPPLIES

2. It is assumed that the terminal strip TSF has been correctly linked so that the primary of the transformer is correctly tapped for the specified mains supply voltage. (Refer to power unit circuit for details.)

Power Unit 11600

Test equipment:-

Digital voltmeter

3. First ensure that all the system printed wiring boards are fitted correctly. Connect the mains supply through to the equipment and press the STANDBY switch on the viewing unit control panel.

4. With a voltmeter measure in turn the voltages at the following test points with respect to 0V (Test 3):-

Test 1	+6V
Test 2	-6V
Test 4	-12V
Test 5	+12V

Press the OFF button on the viewing unit control panel.

Note: No attempt should be made to adjust the presets associated with the power unit except under the circumstances given in Chapter 1.

E.H.T. Power Unit 11601

Test equipment:-

Electrostatic voltmeter 0-18kV

5. Set the focus control on the viewing unit control to mid-position. Disconnect the final anode connection and connect the electrostatic voltmeter between the e.h.t. flying lead and the power unit chassis.

6. Press the STANDBY and ON press-buttons on the viewing unit control panel and note the reading on the voltmeter, which should be 15kV.

7. Press the STANDBY and OFF press-buttons in turn, remove the voltmeter connections and reconnect the c.r.t. final anode lead to the cap.

8. If it is necessary to adjust the e.h.t. voltage, proceed as follows.

9. Switch off the mains supply to the equipment; remove the junction

pack from the rear of the viewing unit after releasing the securing screw. Withdraw the viewing unit from its fibreglass cover and reconnect the junction pack to the viewing unit.

10. Reconnect the electrostatic voltmeter as in paragraph 5 and switch on the mains supply. Press the STANDBY and ON press-buttons and adjust RV1 on the e.h.t. unit for a reading of 15kV on the voltmeter, ensuring that the focus control is in its mid-position.

11. Press the STANDBY and OFF press-buttons and switch off the mains supply to the equipment. Remove the voltmeter and reconnect the c.r.t. final anode lead to the cap.

12. Remove the junction pack from the rear of the viewing unit and replace it in the fibreglass cover. Reconnect the junction pack and switch on the mains supply to the equipment.

TIMING BOARD MJE

Test equipment:-

Oscilloscope

13. Ensure that the aerial resolver, the radar trigger and the video signals are available and correctly connected to the junction panel.

14. Ensure that the display is switched off. Remove the timing printed wiring board and insert the servicing bracket, then place the timing board in the bracket.

15. Press the STANDBY press-button and if a radar pre-trigger pulse is available, proceed as follows. If no pre-pulse is available proceed as detailed in paragraph 17.

16. (1) Connect the oscilloscope trigger input to monitor point 1 on the timing board. Connect the Y1 amplifier to MSKT1 on the timing board. Connect the Y2 input to the collector of TR62 on the timing board.

(2) Set the oscilloscope vertical sensitivity to 5V/cm and the sweep speed to $1\mu\text{s}/\text{cm}$; obtain trigger from monitor point 1 on the timing board MJE.

- (3) Note the relationship between the transmitter firing pulse on Y1 and the pulse at the collector of TR62.
- (4) Adjust RV12 until the delay between the trailing edge of the delayed pulse at TR62 collector and the leading edge of the p.r.f. pulse corresponds to the pre-trigger time provided on site.
- (5) Adjust RV6 (brilliance gate delay) to give a minimum of blanking of the trace origin consistent with no over-brightness at the early part of the trace.

17. If the radar system associated with the display equipment has no pre-pulse trigger facilities, the following links should be modified:-

- (1) Remove link B to C; fit link A to C.
- (2) Remove link R to S; fit link S to W.
- (3) Set the oscilloscope vertical sensitivity to 5V/cm and the sweep speed to $1\mu\text{s}/\text{cm}$; obtain trigger from monitor point 1 on the timing board MJE.
- (4) Monitor TR65 collector and set the positive pulse width to a minimum with RV6.

- 18.
- (1) Connect the oscilloscope to monitor point 12, triggering from the same point. Set the vertical sensitivity to 5V/cm and the sweep speed to 100ms/cm.
 - (2) The square-wave output of the interscan timer will be displayed on the oscilloscope. Adjust RV11 for one cycle of the observed waveform to have 100ms duration.

Mainscan gate length

- 19.
- (1) Connect the oscilloscope to monitor point 16, triggering from monitor point 1.
 - (2) Set the vertical sensitivity to 5V/cm and the sweep speed to $500\mu\text{s}/\text{cm}$.
 - (3) The positive timebase gate waveform will be displayed on the oscilloscope; adjust RV5 so that the gate duration is as follows:-
 - (a) Maximum display range (n.m.) x $12.36\mu\text{s}$.

(b) Maximum display range (d.m.) x $12.2\mu\text{s}$.

(c) Maximum display range (m) x $6.69\mu\text{s}$.

Sampling gate length

20. (1) Connect the oscilloscope to monitor point 3 and obtain trigger from the same point.
- (2) Set the oscilloscope for a negative trigger input; set the vertical sensitivity to $5\text{V}/\text{cm}$ and the sweep speed to $10\mu\text{s}/\text{cm}$.
- (3) The negative sampling gate waveform will be displayed. Adjust RV8 for the negative excursion to be $30\mu\text{s}$ in duration.

Synchro supply square-wave generation

21. (1) Connect the oscilloscope to the collector of TR16. Set the vertical sensitivity to $5\text{V}/\text{cm}$ and the sweep speed to $500\mu\text{s}/\text{cm}$. Trigger from monitor point 3.
- (2) The output of the square-wave generator will be displayed. Set the mark/space ratio to 1:1 by adjusting RV4.
- (3) Set the oscilloscope trigger mode to 'internal' and check the adjustment of step 2 by switching the internal trigger mode alternately positive and negative, readjusting RV4 if necessary.

Synchro supply circuits

22. (1) Set potentiometers RV7, RV9 and RV10 to their mid-positions (initial installation only).
- (2) Connect the oscilloscope to the junction of C17 R203 with internal trigger mode. Set the vertical sensitivity to $0.1\text{V}/\text{cm}$ and the sweep speed to $1\text{ms}/\text{cm}$.
- (3) The oscilloscope is connected to the centre point of the synchro supply transformer. Balance the output of the resolver power amplifier by adjusting RV10 to minimise the 800Hz component in the observed waveform.
- (4) Transfer the oscilloscope to monitor point 2. Set the vertical

sensitivity to 10V/cm and adjust RV7 for the observed waveform to be 35V peak-to-peak in amplitude.

Note: It may be necessary to adjust RV9 to achieve this condition. If so, adjust RV9 for a level slightly in excess and then readjust RV7.

23. Connect a voltmeter on the 10V d.c. range to monitor point 8 and adjust RV9 for a d.c. potential of 4V with respect to earth.
24. (1) Connect the oscilloscope to monitor point 3 and obtain trigger from the same point. Adjust the oscilloscope so that it is being triggered from the positive trailing edge of the negative-going sampling gate.
- (2) Connect the oscilloscope to monitor point 2 with the vertical sensitivity set to 10V/cm and the sweep speed to 10ms/cm, triggered as before.
- (3) Adjust the phasing control RV3 so that a peak or trough of the observed sinewave is coincident with the start of the trace.

25. This completes the setting-up procedure for the timing board. Press the OFF button on the viewing unit control panel, remove the board from the servicing bracket, withdraw the bracket and insert the board in its normal position.

X AND Y DEFLECTION BOARDS MRG

Test equipment:-

Oscilloscope

26. Ensure that the OFF button on the viewing unit control panel has been pressed, remove the Y deflection board, insert the servicing bracket and place the board in the bracket. Finally press the STANDBY button.

Demodulator adjustments

27. (1) Set switches SA and SB on both the X and Y deflection boards to TEST.
- (2) Connect the oscilloscope to monitor point 10, obtaining trigger from monitor point 3 on the timing board MJE. Set the vertical sensitivity to 5mV/cm and the sweep speed to 1ms/cm.
- (3) Adjust RV1 for the d.c. output to be 0V \pm 10mV with respect to signal earth.

- (4) Connect the oscilloscope to monitor point 14 and adjust RV2 for the d.c. output level observed during the $30\mu\text{s}$ sampling pulse time to be $0\text{V} \pm 10\text{mV}$.
 - (5) Adjust RV6 for a scan sawtooth of less than 10mV .
- 28.
- (1) Set switch SC to TEST and connect the oscilloscope to monitor point 9.
 - (2) Adjust RV12 for the inverter output to be 0V at $\pm 10\text{mV}$ with respect to signal earth at monitor point 3 on the power unit.
 - (3) Set switches SA, SB and SC on all boards to RUN.
- 29.
- (1) Connect the oscilloscope to monitor point 14, obtaining the trigger as before. Set the vertical sensitivity to $2\text{V}/\text{cm}$.
 - (2) With the aerial rotating, observe the output d.c. level which will be modulated in amplitude by the aerial rotation. Adjust RV4 for the peak modulation to be $\pm 4\text{V} \pm 0.1\text{V}$.

Interscan control voltage adjustments

- 30.
- (1) Set switch SD to the TEST position. On the operator's control panel press the LINE SHIFT button to ON.
 - (2) Connect the oscilloscope to monitor point 8, obtaining trigger from monitor point 12 on the timing board MJE. Set the vertical sensitivity to $5\text{mV}/\text{cm}$.
 - (3) Adjust RV11 for the output to be $0\text{V} \pm 10\text{mV}$ with reference to the d.c. level obtained during the mainscan period.
 - (4) Set switch SD to the RUN position.

Timebase adjustments

- 31.
- (1) Connect the oscilloscope to monitor point 7, obtaining trigger from monitor point 1 on the timing board MJE, and switch SH to the TEST position.
 - (2) With the vertical sensitivity set to $10\text{mV}/\text{cm}$ and the oscilloscope d.c.-coupled, adjust RV10 for a scan sawtooth of less than 10mV .

- (3) Set the vertical sensitivity to 5mV/cm and adjust RV9 for the output to be 0V with respect to signal earth at monitor point 3 on the power unit.
- (4) Set switch SH to the RUN position and adjust RV8 for the timebase to scan to $\pm 4V$ peak $\pm 0.1V$ in the mainscan period.

Interscan buffer amplifier adjustment

32. (1) Set switches SA, SB and SG to the TEST position. Connect the oscilloscope to monitor point 11 and trigger from monitor point 12 on the timing board MJE.
- (2) Set the vertical sensitivity to 10mV/cm and adjust RV7 for the output during the interscan period to be $0V \pm 10mV$ with respect to signal earth at monitor point 3 on the power unit.
- (3) Readjust RV2 for the output during the mainscan period to be $0V \pm 10mV$ with respect to signal earth at monitor point 3 on the power unit.
- (4) Set switches SA, SB and SG to RUN.

Range change amplifier adjustment

33. (1) Set switch SE to the TEST position. Connect the oscilloscope to monitor point 1 and obtain trigger from the monitor point 1 on the timing board MJE.
- (2) Set the vertical sensitivity to 20mV/cm and adjust RV13 for the output to be $0V \pm 10mV$ with respect to signal earth at monitor point 3 on the power unit.
- (3) Connect the oscilloscope to monitor point 5 and adjust RV14 for the output to be $0V \pm 10mV$ with respect to signal earth at monitor point 3 on the power unit.
- (4) Set switch SE to the RUN position.

Range change amplifier limiting adjustments

34. (1) Connect the oscilloscope to monitor point 1, obtaining trigger as before. Set the vertical sensitivity to 2V/cm and select the shortest range on the viewing unit control panel.
- (2) The observed waveform should be a sawtooth, the amplitude of which will be modulated by the aerial rotation. Adjust RV15 so that the onset of limiting of the sawtooth occurs at -4V.

(3) Adjust RV16 so that the onset of limiting of the sawtooth occurs at +4V.

(4) Press the longest-range button on the viewing unit control panel.

35. This completes the setting-up procedure for the Y deflection board. Press the OFF button on the viewing unit control panel, remove the oscilloscope connections and the board from the servicing bracket, withdraw the bracket and insert the board in its normal position.

36. Set up the second deflection board by repeating the procedure given in the previous paragraphs (26 to 35), substituting X for Y.

VIDEO BOARD MFD

Test equipment:-

Oscilloscope
Digital voltmeter

37. Ensure that the OFF button on the viewing unit control panel has been pressed, remove the video printed wiring board and insert the servicing bracket; then place the video board in the bracket. Press the STANDBY press-button.

Video channel balance adjustments

38. (1) Connect the voltmeter set to its 10V d.c. range between the collectors of TR1 and 2.

(2) Select Video 1 on the operator's control panel, ensuring the remaining videos are at OFF and all four video gain controls are fully clockwise on the viewing unit control panel.

(3) Adjust RV1 to obtain $0V \pm 0.1V$ on the voltmeter.

39. Set Video 1 to OFF and Video 2 to ON; with the voltmeter connected as before, adjust RV2 to obtain $0V \pm 0.1V$ on the voltmeter.

40. Repeat this procedure for video channel 3 (RV3 adjustment) and channel 4 (RV4 adjustment).

Range calibration adjustments

41. No attempt must be made to adjust the calibration marker generator unless test equipment of the required accuracy is available and the procedure is fully detailed in Section 3, Chapter 4.
42.
 - (1) Connect the oscilloscope to the base of TR54, obtaining trigger from monitor point 1 on the timing board MJE. Set the vertical sensitivity to 2V/cm and the sweep speed to 200 μ s/cm.
 - (2) Adjust RV12 to obtain a constant amplitude of the observed sinewave to within $\pm 5\%$.
43.
 - (1) Connect the oscilloscope Y1 input to the collector of TR62 and the Y2 input to monitor point 10 (fine marker generator output).
 - (2) Set the vertical sensitivity to 5V/cm and the sweep speed to 200 μ s/cm; adjust RV15 to set the length of the observed negative gate pulses on the Y1 plate to lie between 1.2 and 1.5 times the fine calibration interval.
44.
 - (1) Connect the oscilloscope Y1 input to monitor point 11 (coarse marker generator output).
 - (2) Adjust RV14 to obtain the required division. There will be a range of movement of RV14 over which this is possible. Set the control to the centre of this range.
 - (3) Disconnect the oscilloscope.
45.
 - (1) Connect the oscilloscope to pin PLB2 on the video board; set the vertical sensitivity to 10V/cm and the sweep speed to 1ms/cm, obtaining trigger from monitor point 1 on the timing board MJE.
 - (2) Set the 'coarse' range marks gain control on the viewing unit control panel fully clockwise and select the 'coarse' range markers on the operator's control panel.
 - (3) Adjust RV7 on the video board for the amplitude of the coarse range markers to be 25V ± 1 V (100V d.c. level with 25V negative-going signal).
 - (4) Adjust RV5 on the video board so that the mainscan level is at -5V ± 1 V with respect to the between-mainscan level ± 1 V (95V d.c. level).

- (5) Adjust RV8 for an interscan level of $-10V \pm 1V$ with respect to the between-mainscan level (90V d.c. level).
- (6) Set RV11 fully anti-clockwise.

46. This completes the setting-up procedure for the video board. Press the OFF button on the viewing unit control panel, remove the board from the servicing bracket, withdraw the bracket and insert the board in its normal position.

DEFLECTION COIL DRIVE AMPLIFIER

47. Real care must be exercised to avoid shorting the adjacent pins with the voltmeter probe. A sleeved probe should be used and when there is any doubt, the viewing unit d.c. supplies should be switched off when connecting or removing the monitor probe.

48.
 - (1) Press the STANDBY press-button on the viewing unit control panel.
 - (2) Remove the X deflection board. Monitor the XA output of the final deflection amplifier at TSB2 with a voltmeter set to the maximum sensitivity range.
 - (3) Adjust RV1 on the final deflection amplifier for the output level to be $-0.6V \pm 10mV$ with respect to signal earth at monitor point 3 on the power unit.
 - (4) Monitor the XB output of the final deflection amplifier at TSA9 with a voltmeter set to the maximum sensitivity range.
 - (5) Adjust RV3 on the final deflection amplifier for the observed output level to be $-0.6V \pm 10mV$ with respect to signal earth at monitor point 3 on the power unit.
 - (6) Replace the X deflection board.
49.
 - (1) Remove the Y deflection board and repeat this adjustment for the Y channel, monitoring the YA output at TSB9 and adjusting RV2 and the YB output at TSA2 and adjusting RV4.
 - (2) Replace the Y deflection board.

40. This completes the initial setting-up of the viewing unit.

FINAL SETTING-UP PROCEDURE

Final deflection amplifier

51. (1) Press the STANDBY button on the viewing unit control panel, set the SE switches on both deflection boards MRG to the TEST position and press the LINE ON/OFF button on the operator's control panel to OFF. Set both coarse and fine range marks to OFF.
- (2) Turn the RADAR BRILL. control on the viewing unit control panel fully anti-clockwise and press the ON button on the viewing unit control panel.
- (3) Turn the RADAR BRILL. control slowly clockwise until a spot is just visible on the centre of the c.r.t. face. Trip out X3 on the power unit and note any change of the spot position.
- (4) Reset output X3. If any movement is apparent in the X direction, adjust RV1 or RV3 on the final deflection amplifier; in the Y direction, adjust RV2 or RV4.

52. The actual potentiometer to be adjusted must be the one which increases the current in the coil. This may be checked by carefully observing the voltages at TSA2 and A9, TSB2 and B9 on the final deflection amplifier, to see that in each case the voltage does not become more positive than the -600mV d.c. originally set in paragraphs 48 and 49.

53. Set the SE switches on both deflection boards to RUN.

X and Y deflection boards

54. (1) Ensure that all switches are in the RUN position. Select the longest range button on the viewing unit control panel and, using the X and Y CENTRE controls, position the mainscan origin to the centre of the c.r.t.
- (2) Set the SE switch on the X deflection board to the TEST position and alternately select the shortest and longest range settings on the viewing unit control panel.
- (3) Note any positional change of the origin of the trace. Adjust RV13 on the X deflection board to remove any jump observed.
- (4) Set switch SE on the X deflection board to the RUN position.

55. Set the SE switch on the Y deflection board to the TEST position and repeat the procedure for the Y channel.
56. (1) Press the STANDBY and OFF buttons on the viewing unit control panel; remove the Y deflection board, insert the servicing bracket and place the board in the bracket. Finally press the STANDBY and ON buttons on the viewing unit control panel.
- (2) Select the longest range setting on the viewing unit control panel and RADAR SHIFT to OFF on the operator's control panel.
- (3) Select LINE SHIFT to OFF and adjust LINE BRILL. for the optimum level of brilliance.
- (4) With the aerial rotating at its standard speed, connect the oscilloscope d.c. -coupled to monitor point 14. Set the Y sensitivity to 50mV/cm and the sweep speed to 2ms/cm. As the demodulator passes through 0V, a step will be observed on the demodulator output.
- (5) Adjust RV3 on the Y deflection board to minimise the observed step.
57. (1) Observe the mainscan on the c.r.t. Adjust RV8 on the Y deflection board so that the longest range ring passes through the centre of the engraved figures on the implosion screen at the 0° and 180° cardinal points.
- (2) Press the STANDBY and OFF buttons on the viewing unit control panel, remove the Y deflection board from the servicing bracket and replace the board in its normal position.
58. Repeat the procedure in paragraphs 56 and 57 for the X deflection board and adjust RV8 on the X deflection board at the 90° and 270° cardinal points, but do not press the STANDBY and OFF buttons or remove the X deflection board from the servicing bracket.
59. (1) Set the BEARING control on the operator's control panel to 90° and the RANGE control so that the interscan line just touches a range ring at about 3/5 of maximum range.

Note: Accurate setting should be made by selecting the shortest range setting on the viewing unit control panel and off-centring the picture with the RADAR SHIFT controls.

- (2) Set the BEARING control to 270° and check that the interscan line overlays the selected range ring.

Note: Using the RADAR SHIFT controls and the shortest range setting as before.

- (3) If the interscan line does not overlay, adjust RV7 on the X deflection board to halve the observed error and repeat the procedure until no error is observed.

60.
 - (1) Set the BEARING control to 90° and the RANGE control for a graticule scale reading of maximum range.
 - (2) Press the shortest-range selection button on the viewing unit control panel and with the RADAR SHIFT controls, set the end of the interscan to the centre of the c.r.t. face.
 - (3) Adjust RV20 on the X deflection board for the length of the interscan to equal the mainscan length.
 - (4) Press the STANDBY and OFF buttons on the viewing unit control panel, remove the X deflection board from the servicing bracket and replace the board in its normal position.
61.
 - (1) Remove the Y deflection board, insert the servicing bracket and place the board in the bracket. Finally press the STANDBY and ON buttons on the viewing unit control panel.
 - (2) Repeat the procedure in paragraph 59 for the adjustment of RV7 but use bearing points of 0° and 180° .
 - (3) Repeat the procedure in paragraph 60 for the adjustment of RV20 but set the bearing to 0°

Video board

62.
 - (1) Set RV11 (overall brilliance) on the video board fully anti-clockwise; ensure that the LINE ON/OFF switch on the operator's control panel is set to ON.
 - (2) Set the RADAR BRILL. control fully anti-clockwise and the LINE BRILL. control fully clockwise, and adjust RV11 on the video board for a just over-bright interscan.

- (3) Readjust the two brilliance controls to an optimum brilliance setting.

63. Adjust RV10 on the video board so that octagonal blanking occurs just outside the periphery of the c.r.t. Press the STANDBY and OFF buttons on the viewing unit control panel.

Timing board

64.
 - (1) Ensure that the STANDBY and OFF buttons on the viewing unit control panel have been pressed, remove the timing board (MJE), insert the servicing bracket and place the board in the bracket. Finally press the STANDBY and ON buttons on the viewing unit control panel.
 - (2) Connect the oscilloscope to the junction of C37 and TR33 connector; set the vertical sensitivity to 1V/cm and sweep speed to 1ms/cm, obtaining trigger from monitor point 1 on the timing board.
 - (3) Adjust RV1 on the timing board for the positive peaks to occur at -2V d.c. $\pm 0.1V$.
 - (4) Adjust RV5 on the timing board for a timebase length of maximum range plus 5%.
65.
 - (1) Select the shortest range button on the viewing unit control panel.
 - (2) Set the RANGE control on the operator's control panel for a graticule scale reading of 1/5 of the maximum range and adjust RV2 on the timing board for the end of the interscan line to just overlay the appropriate range ring at a 0° bearing.
 - (3) With the RADAR SHIFT switch selected, adjust the Y off-centre control so that the range ring equivalent to 4/5 of maximum range appears in the centre of the c.r.t. face.
 - (4) Set the RANGE control until a graticule scale reading of 4/5 of the maximum range is indicated.
 - (5) Readjust RV5 on the timing board until the end of the interscan line coincides with the 4/5 range marker ring.

- (6) Repeat the procedure in this paragraph stages 1 to 5 until the adjustments of RV2 and RV5 are correct.
- 66.
- (1) Adjust the Y off-centre control so that the end of the mainscan is observed in the centre of the c.r.t. face.
 - (2) Adjust RV1 on the timing board to set the mainscan length to just touch the maximum range marker ring.
 - (3) Press the STANDBY and OFF buttons on the viewing unit control panel, remove the timing board from the servicing bracket and replace the board in its normal position.
67. This completes the display setting-up. Replace the top cover.

Chapter 6

CRT REPLACEMENT

LIST OF CONTENTS

	Para.
GENERAL	1
CRT REMOVAL	4
CRT REPLACEMENT	
Preliminary adjustment	7
Spot centring and focussing	10
Coil orientation	14

LIST OF ILLUSTRATIONS

	Fig.
Coil assembly: adjustment controls	1

GENERAL

1. The type of CRT fitted varies from one installation to another. In the 12-in displays used in all the systems covered by this manual (with its supplements), only one type of (small-spot) CRT is approved for replacement purposes. In some systems, a further, normal-spot-size CRT is approved as a second choice; the list overleaf shows which systems may use the alternative tube.

2. The CRT which is approved for replacement purposes in all the systems listed overleaf is a small-spot type with the following reference numbers:

Plessey Ref. 687/SG/01500/021

NATO Ref. 10CV/5960/99/118/3603

3. The CRT which is approved as a second choice for replacement purposes where acceptable is a normal-spot-size type with the following reference numbers:

Plessey Ref. 687/SG/01500/002

NATO Ref. 10CV/5960/99/027/5771

System Type	Display Type	Second Choice Acceptable
TGRI 23154 & TGRI (AT) 26038/1 & /2 (Type AR1 Radar, 75dm)	12600/N	Yes
As above, 100dm	12600/R	Yes
GL161 Systems 1 to 4 inc.	12600/Y	No
GL161 Systems 1 and 3	12608/C	No
SJCC	687/00017/009	No
TGRI (AT) 23214 (Type S259 Radar)	687/00017/014	Yes
Type 89 Radar (P.P.I. Display)	687/00017/014	No
Type 89 Radar (H.R.I. Display)	687/00017/025	No
FGRI 23100/3 (ADRS H.R.I. Displays)	687/00017/025	No

CRT REMOVAL

4. Switch off the display. Remove the junction unit from the rear of the viewing unit, taking care that the mating faces are kept parallel in doing so. Remove the viewing unit from its fibreglass case.
5. Remove the implosion screen. Remove the front and rear mu-metal screens fitted above the deflection coil assembly; the front screen may be removed directly and the rear screen slid onto the centre screen.
6. Remove the CRT anode connection and discharge the CRT by shorting the top cap to chassis. Remove the base connector. Ease the CRT forward and withdraw it (it is advisable to have someone at the front of the display to ensure that the CRT does not slide out suddenly).

CRT REPLACEMENT

Preliminary adjustments

7. Loosen the three platform securing screws (B, Fig. 1) and the two orientation screws (D, Fig. 1). Adjust the platform jacking screws and manipulate the platform to

obtain the condition of level platform (about 1/16in. clearance beneath), centrally positioned and in line with the sides of the chassis (Fig.1). Tighten, but do not secure, the platform securing screws.

8. Insert the new tube without any undue pressure. Connect the anode and base connectors. Reconnect the junction unit ensuring that the mating faces are kept parallel as the unit is pushed home. Switch on the display and check that the CRT is serviceable. Switch off the display. Replace the implosion screen.

9. Ensure that the CRT is held tightly by the Neoprene rubbering around the tube face periphery, allowing no movement of the CRT. Check that the deflection coils are tightly seated against the tube flare (avoid undue pressure). Tighten, but do not secure, the orientation screws (Fig. 1,D).

Spot centring and focussing

10. Turn the radar brilliance fully counter-clockwise. De-select radar videos and range markers. Set the focus control on the operator's control panel to mid position. Switch on the display. Trip X3 and adjust the radar brilliance to obtain a spot, exercising care to avoid excessive brilliance.

11. Adjust the beam centring magnets for optimum brilliance; these are independent annular magnets with adjusting lugs on the periphery, which are fitted at the rear of the focus magnet housing. Adjust the mechanical focus control for optimum focus; this control is a knurled knob which is slackened to allow movement in a slot in the focus magnet housing. Secure the mechanical focus control.

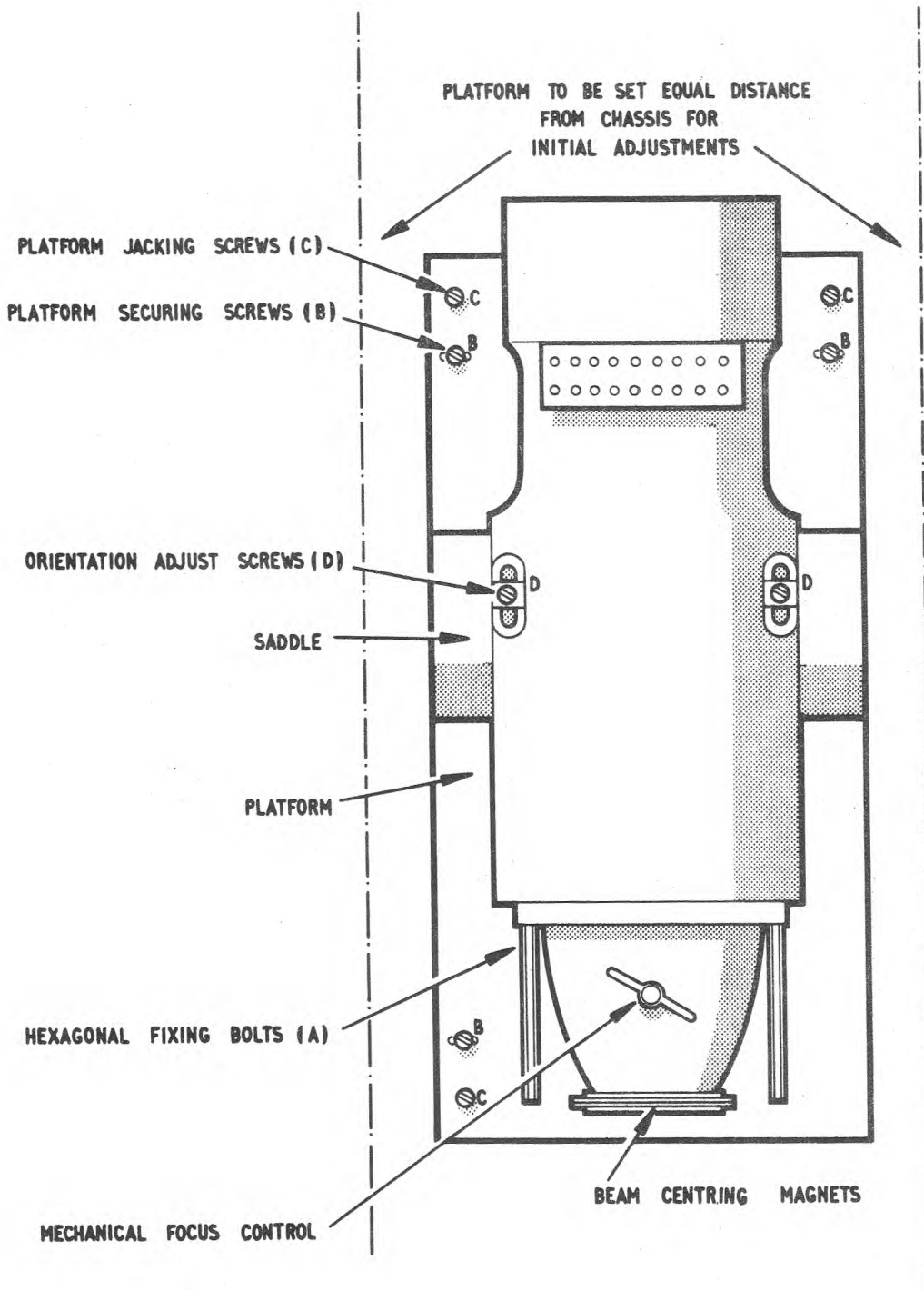
12. Loosen the two hexagonal bolts (Fig. 1,A) and orientate the magnet assembly to centre the spot. Tighten bolts (Fig. 1,A); this may move the spot slightly off centre but this is corrected later.

13. Slacken the platform securing screws (Fig. 1,B) and, with small adjustment of the platform alignment and of the platform jacking screws (Fig. 1,C), obtain exact coincidence of the centre spot with the engraved cross on the implosion screen; this adjustment is best carried out at the rear of the platform only, as adjustment of the platform front end could put breaking pressure on the tube neck near the flare. Secure all the platform securing screws.

Coil orientation

14. Reset X3. Set SA^E on the X deflection board to TEST. Increase brilliance until a vertical trace is presented. Rotate the deflection coil in its saddle by alternately slackening and tightening the orientation screws (Fig. 1,D) in opposition until the trace lies along the North/South line on the implosion screen.

15. If necessary repeat para. 8 to 11 to obtain simultaneously the optimum conditions of focussing, centre spot alignment and coil orientation.
16. Switch off the display. Remove the junction unit. Replace the mu-metal screens. Replace the viewing unit in its fibreglass cover and refit the junction unit.
17. Carry out display accuracy test, Chap. 2 or Chap. 3, as appropriate.



Chapter 7

MAINTENANCE OF THE COOLING SYSTEM

	Para.
Introduction	1
Topping-up sequence 'A'	7
Topping-up sequence 'B'	8

LIST OF ILLUSTRATIONS

	Fig.
Position of compression block and method of removal	1
Coolant filler adaptor	2
Pump assembly 12551	3

Introduction

1. The cooling system in the 12in viewing and the two similar systems in the 21in viewing unit require little or no maintenance. It is not anticipated that the coolant, Aeroshell Turbing Oil No.1 (34D/1625 oil SP4 grade 1005) will require replacement within the useful life of the equipment. The pump motor is lubricated by the coolant in which it is submerged. The fan induction motor has seal-packed bearings, which do not require maintenance.

2. The system is vacuum-tested at the factory. Gross defects that occur at a later date will be made very evident by repeated tripping of the high-temperature thermal cut-out.

3. From time to time it may be necessary to top up the system with coolant, as the most carefully sealed system will evaporate to some extent. The coolant needs to be topped up if, when the display is switched on, and then off again, the section of clear polythene tubing, forming part of the oil loop, shows an air bubble in excess of 5cm (2in). Topping up may be regarded as complete if an air bubble of 1.27cm (0.5in) or less is achieved.

4. Depending on the viewing unit model, one of two topping-up sequences described below should be followed and strictly adhered to. Sequence 'A' should be followed when the viewing unit is fitted with a special compression bracket; this is a hump shaped metal plate secured to the underside of the viewing unit by two of the four screws securing the pump body to the bottom casting. Sequence 'B' should be followed when this bracket is not fitted; in this case a special tool known as a 'compression block' is required.

Caution

The material forming the outside under-surface of the pump bellows can be damaged by contact with the coolant oil. Exercise care to avoid spillage and MOP UP ANY SPILLED OIL AS SOON AS POSSIBLE.

5. The filling procedure can be simplified by the use of a filler adaptor. This can be connected in place of the plug on the pump top. The coolant is added to the adaptor until it shows in the tube and time allowed for air bubbles to pass up through the adaptor as new coolant is drawn into the system (the pump must be switched ON meanwhile). Do not overfill the adaptor, and ensure that no coolant spills on the outside of the pump body when the adaptor is removed. The adaptor is not supplied as a special tool; if required it can be manufactured locally from the details given in Fig. 2.

6. If the adaptor in para. 5 is not used it will be found helpful to leave the filter retaining spring (exposed when the filler plug is removed) in position during the filling operation; this tends to break up bubbles and assists the egress of air from the system.

Topping-up sequence 'A'

7. This sequence uses the compression bracket fitted to the underside of the viewing unit:-

- (1) Switch off the incoming mains supply.
- (2) Disconnect and remove the e. h. t. unit and insulate the bared ends of the disconnected leads.
- (3) Remove the fore and aft screws retaining the pump body to the bottom casting; this frees the compression plate at the bottom of the pump and also the compression bracket under the casting. Rotate the bar attached to the compression plate until it is free to move upwards in the slot in the pump body.
- (4) Replace the compression bracket so that it is now upside-down with respect to its initial position, fit the two retaining screws and tighten these so that the hump on the bracket passes through the hole in the bottom casting and bears on the compression plate so that it rises up the slot. The screws should be fully tightened so that the compression plate constricts the oil bellows.

- (5) Switch on the mains supply and SWITCH ON THE PUMP.
- (6) Taking care not to touch the exposed terminals at the rear of the viewing unit control panel, remove the filler plug at the top of the pump and top up with coolant to a point just short of overflowing. If the filler adaptor is being used, substitute it for the filler plug and top up until coolant is just visible in the adaptor tube.
- (7) Continue to top up until the coolant is free of air bubbles.
- (8) Replace the filler plug, making sure that the filter retaining ring and filler-plug washer are in position. If the filler adaptor is being used it must be removed with care to avoid spilling coolant on the outside of the pump. Wrap a piece of absorbent rag around the pump body to catch any surplus oil when the adaptor is removed.
- (9) Switch off the pump and the mains supply.
- (10) Remove the two screws mentioned in sub-para (2), thus releasing the compression plate and compression bracket, and permitting the oil bellows to expand. Rotate the compression-plate bar to its original position, fit the compression bracket in its original position and replace the two screws.
- (11) Mop up any spilled oil and replace the e. h. t. unit.

Topping-up sequence 'B'

8. This sequence requires the use of a special tool referred to as the 'compression block', and is employed when there is no compression bracket fitted to the underside of the viewing unit (Fig. 1).

- (1) Switch off the incoming mains supply.
- (2) Disconnect and remove the four-symbol multiplexer unit, where fitted, and insulate the bared ends of the disconnected leads.
- (3) Disconnect and remove the e. h. t. unit and insulate the bared ends of the disconnected leads.
- (4) Free the compression plate at the bottom of the pump, by removing the fore and aft screw of the four screws in the

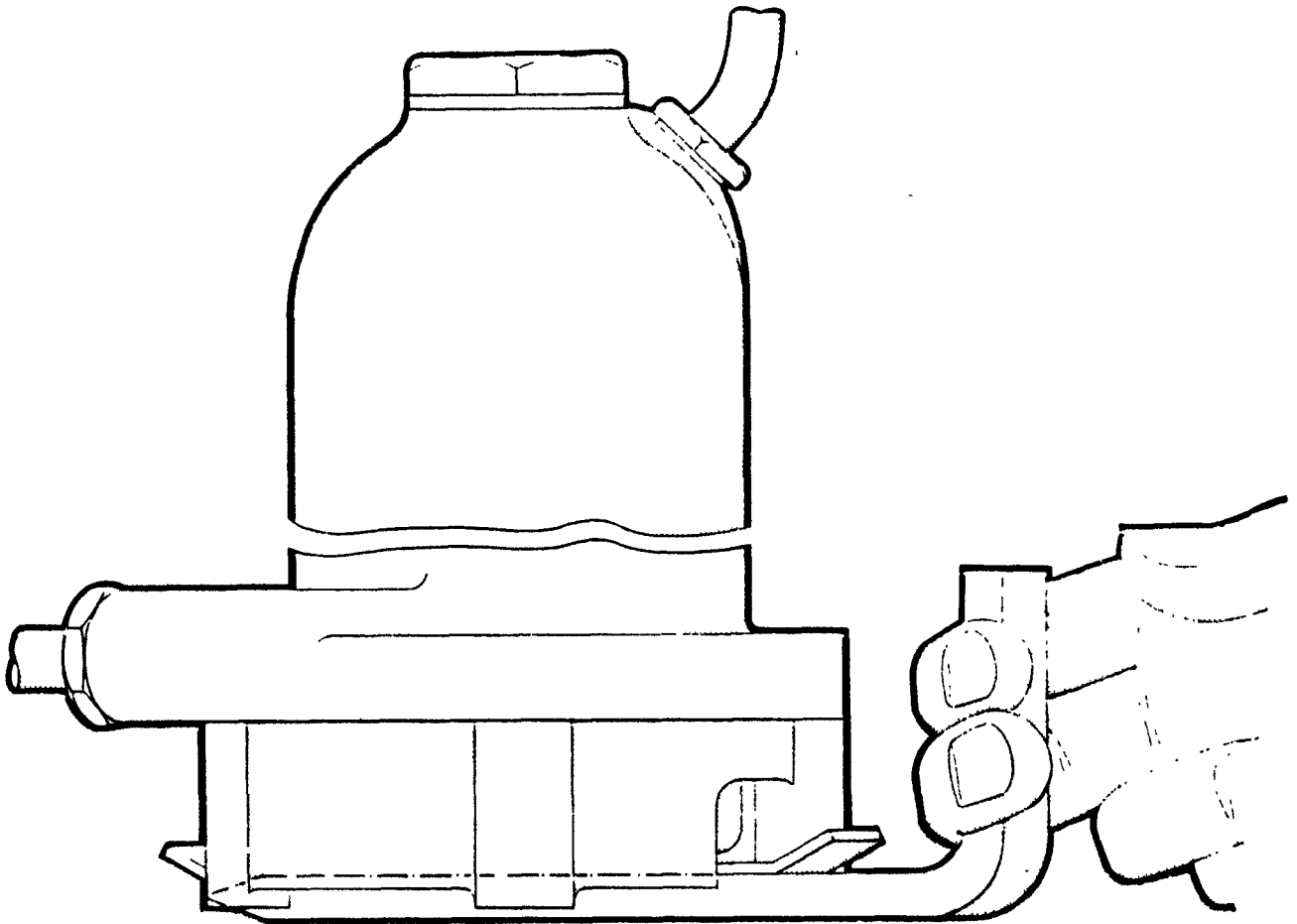
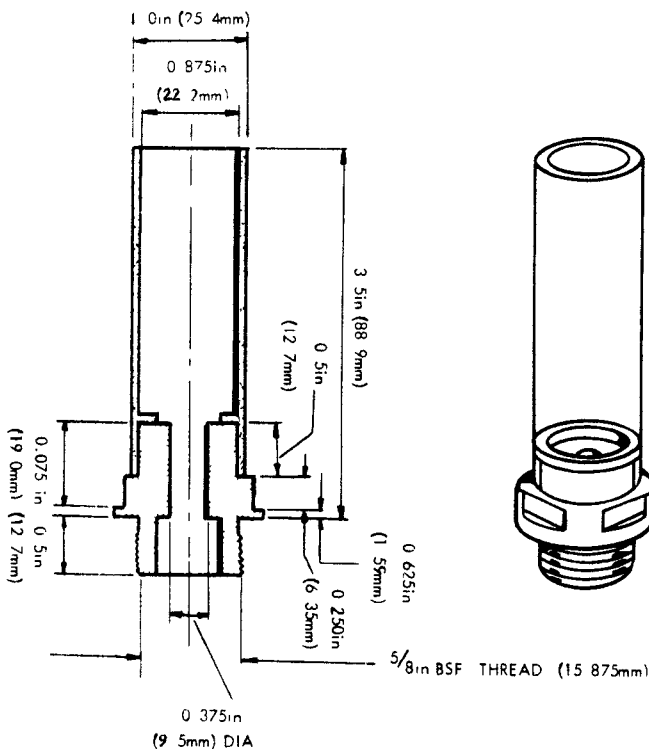


Fig. 1 Position of compression block and method of removal

bottom casting, and rotate through a few degrees in a clockwise direction the bar attached to this plate, until it is free to move up and down in the slot in the bottom of the casting.

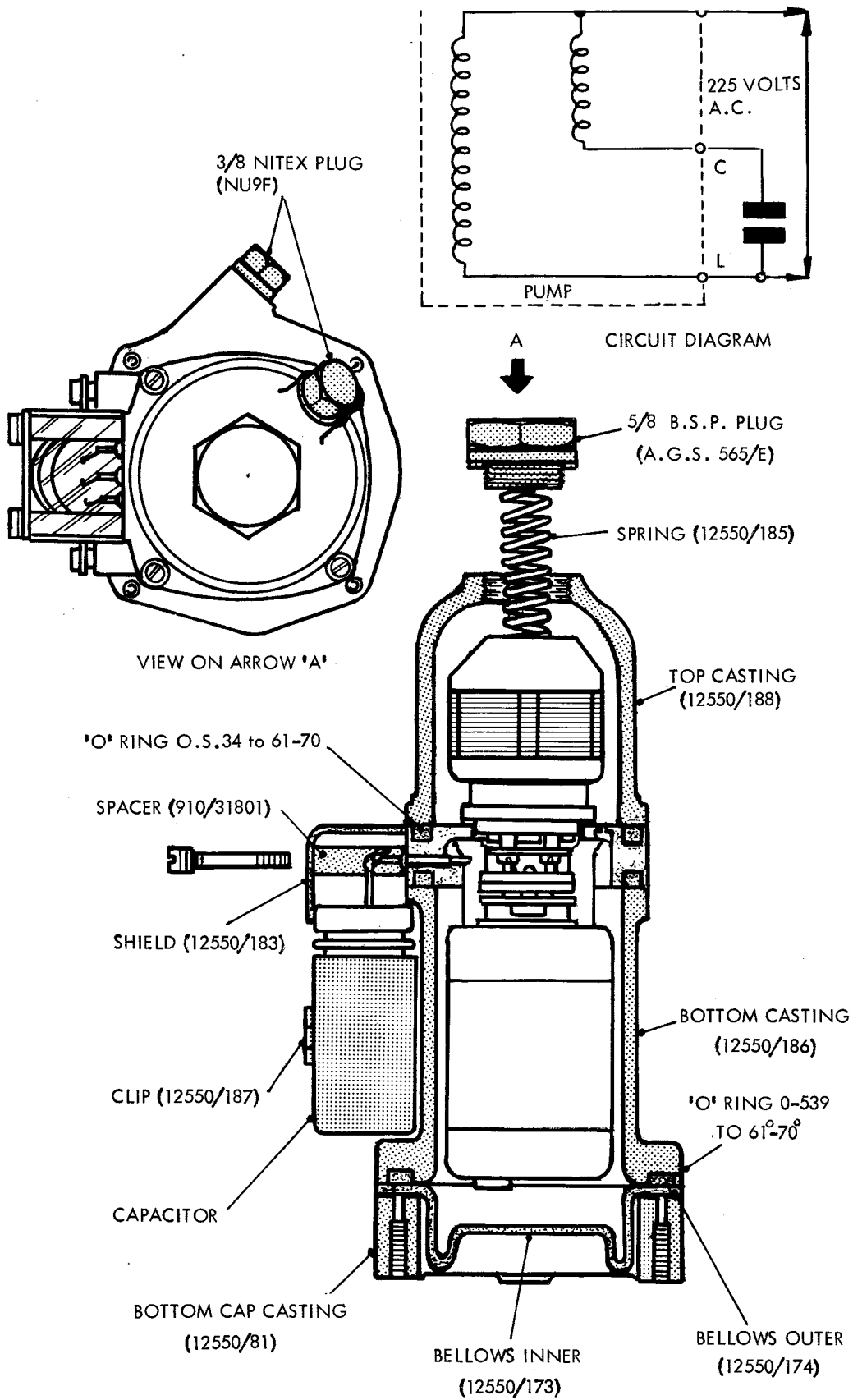
- (5) Push the special tool (Compression Block Decca A/DDDL/12550/198 Issue 2) under the compression plate bar so that this bar moves upwards in the slot and the compression plate constricts the oil bellows.
- (6) Switch on the mains supply and SWITCH ON THE PUMP by operating the STANDBY button on the control panel.
- (7) Taking care not to touch the exposed terminals on the rear of the viewing unit control panel, remove the filling plug at the top of the pump and top up with coolant to a point just short of overflowing. If the adaptor (Fig. 2) is being used substitute it for the filling plug and top up until coolant is visible in the adaptor tub

- (8) Continue to top up until the coolant is free of air bubbles.
- (9) Replace the filling plug making sure that the filter-retaining spring and filling-plug washer are in position. If the filler adaptor is being used it must be removed with care to avoid spilling coolant on the outside of the pump. Wrap a piece of absorbent rag around the pump body before removing the adaptor to catch any surplus coolant when the adaptor is removed.
- (10) Switch off the pump and the mains supply.
- (11) Remove the special tool.
- (12) Rotate the compression-plate bar to its original position and replace the two screws in the bottom casting.
- (13) Replace the e. h. t. and multiplexer units.
- (14) Mop up any spilled oil.



NOTE NOT TO SCALE

Fig. 2 Oil Filler Adaptor



Chapter 8

CRT REPLACEMENT (21in)

LIST OF CONTENTS

	Para.
CRT removal	1
CRT replacement	
Preliminary adjustments	6
Focus setting-up procedure	10
Deflection coil alignment	19

CRT REMOVAL

1. Switch off and disconnect the mains supplies to the equipment. Remove all covers from the underside of the four rolling ball control panels and table junction unit and remove the plugs connected to these units. Remove the east and west face side covers from the viewing unit.
2. Remove the four rolling ball control panels from the table top, then slacken all eight table-top retaining bolts and lift the table top from the viewing unit.
3. Unscrew and extract the cursor illumination lamps. Remove the implosion screen retaining bolts and lift the implosion screen off the pedestal. Remove the panels on either side of the Mu-metal screen, the cathode ray tube base connector and the final video amplifier.
4. Very carefully lift the tube out of the viewing unit and remove the rubber ring from the tube.
5. Slacken off the deflection coil locking bolt (horizontal Tufnol bolt), the deflection coil adjustment bolts (inner pair of Tufnol bolts) and the deflection coil assembly clamp bolts (outer pair of Tufnol bolts). The deflection coil should now be quite free to move.

CRT REPLACEMENT

Preliminary adjustments

6. Fit the rubber ring to the new tube and ensure it is seated evenly around the rim of the tube.

7. Insert the tube into the unit taking care that the long neck of the tube does not foul the deflection and focusing coil assemblies. Screw in the deflection coil adjustment bolts until the coil is felt to be pushed gently up against the flare of the tube. Tighten the deflection coil assembly clamp bolts and gently tighten the deflection coil locking bolt.

8. Slacken the focus coil clamp nuts and position the focus coil and the beam centring magnet assembly (immediately below the focus coil) centrally around the neck of the tube, ensuring that the notched lugs on the beam centring magnets are 180° apart.

9. Gently tighten the focus coil clamp nuts. Replace the implosion screen together with associated retaining bolts and cursor lamps; then the c. r. t. base connector and final video amplifier.

Focus setting-up procedure

10. Ensure all video channels are switched off and their gain controls set fully anti-clockwise. Trip all the cut-outs on Power Units 11605 and 11606 then set cut-out X1 on Unit 11605 and X2, X4 on Unit 11606.

11. Set all brilliance controls on the viewing unit control panel fully anti-clockwise. Press cut-out X4 on Unit 11606 and set deflection NORMAL/TEST switch to TEST and align OFF/ON switch to OFF on the focus control panel.

12. Press the STANDBY and ON buttons on the viewing unit control panel to switch on the e. h. t. Cautiously turn up the BRILLIANCE control until an unfocused spot appears on the tube. Adjust the beam centring magnets for the spot to be approximately at the centre of the tube.

13. Turn the BRILLIANCE control fully anti-clockwise and press the cut-out X3 on Unit 11606. Set align OFF/ON switch at focus control panel to ON.

14. Cautiously advance the BRILLIANCE control to obtain a spot then adjust the FOCUS control on the viewing unit control panel to optimum focus, which should occur at approximately mid-travel of the control. If this is not possible, set the FOCUS control to mid-travel and adjust RV1 on the focus coil amplifier situated in Unit 11605 until focus is achieved.

15. Set the astig X and Y potentiometers on the focus control panel to mid-travel and the a. c. ON/OFF switch to ON. Adjust the a. c. GAIN potentiometer for a de-focused spot of approximately 0.25in diameter. The spot may appear as a lobe; if so, that FOCUS control on the viewing unit control panel should be readjusted to make the centre of the lobe come into focus.

16. Adjust the alignment X and Y potentiometers on the focus control panel for the focused spot to occur within the unfocused area. Switch the a. c. ON/OFF switch off and adjust the astig X and Y potentiometers for a circular spot. Readjust the FOCUS control for focus.

17. Slacken the focus coil clamp nuts and adjust the positions of the focus coil for the focused spot to be at centre of the tube. Tighten the nuts.

18. Repeat the focusing procedure as necessary to achieve a centred focused spot on the tube. When exactly aligned, it should be possible to rotate the FOCUS control on the viewing unit control panel between its extremities and the spot should move in and out of focus without change of position. Set the deflection NORMAL/TEST switch on the focus control panel to NORMAL.

Deflection coil alignment

19. With the antenna turning, select SHORT range and advance the brightness control to bring up trace. Set the X and Y CENTRING switches on the focus control panel to INTERNAL. Position the origin of the mainscan at the tube centre using the X and Y centring controls.

20. Set switch SE on the X deflection board to TEST, and SG (alignment) switch on the focus control panel to OFF. Adjust the deflection coil aligning screw so that the trace passes through the 0° and 180° points on the azimuth scale.

21. Set switch SE on the X and Y deflection boards to RUN and TEST respectively. If necessary adjust the deflection coil orientation screw so that the trace passes through the 90° and 270° points on the azimuth scale. Lock the deflection coil in position by tightening the deflection coil clamp screw.

22. Replace the Mu-metal screen side plates, set switch SE on the Y deflection board to RUN and switch SG on the focus control panel to ON.

23. Upon completion of satisfactory alignment and focusing of the viewing unit, replace the table-top, four rolling ball panels and make associated connections.

24. If difficulty is experienced in alignment or focusing, refer to the procedures described in A. P.115B-0515-1, Cover 1, Sect. 1, Chap. 17.

PLUG - IN BOARDS

Chapter 1

POWER UNIT 11600

LIST OF CONTENTS

	Para.
Removal and replacement procedures	1
Test data	3

LIST OF TABLES

	Table
Test equipment	1
Dummy loads	2
Test data	3
Zener diode currents	4
Unstabilized power supply checks	5

REMOVAL AND REPLACEMENT PROCEDURES

Removal procedure

1. Unplug each taper pin connector from terminal blocks TSA to TSF. Loosen the six captive screws securing the power unit to the viewing unit cold plate. Withdraw the power unit from the main chassis (it may be necessary to unloose the cable looms on the main chassis).

Replacement procedure

2. Locate the power unit in position (on two dowel pins) on the viewing unit chassis and secure with the six captive screws. Insert the taper pin connectors into terminal blocks TSA to TSF; each taper pin lead is identified by sleeves bearing the block letter and pin number.

TEST DATA

Introduction

3. This chapter contains test data derived from Plessey Radar Ltd. Test Specification No. F.C.T.96.

4. Refer to Bench Test Procedures for test procedures with the board connected in the Printed Circuit and Power Unit Test Unit (687/1/01436), e.g. at L1.
5. Refer to A.P.115B-0514-1 and the Master Work Sheets for procedures using the Comprehensive Display Test Set Type 10060, e.g. at G.R.S.C.
6. Refer to the station list of approved test equipment for details of specific available test equipment.

TABLE 1

Test equipment

Comprehensive Display Test Set 10060
(or working display)

Oscilloscope CT536 or equivalent

Multimeter CT498 or equivalent

Digital voltmeter CT470D (set) or equivalent

Dummy loads (as given in Table 2)

TABLE 2

Dummy loads

Power supply	Load	Dummy load connections
+12V	0.9, 1.0, 1.4 and 1.5A	TSC2 to TSC8 (earth)
-12V	0.9, 1.0, 1.4 and 1.5A	TSC7 to TSC8 (earth)
+6V	0.9, 1.0, 1.4 and 1.5A	TSC10 and TSC3 (earth)
-6V	0.9, 1.0, 1.4 and 1.5A	TSC6 and TSC3 (earth)

Table 2 (Contd.)

Power supply	Load	Dummy load connections
EHT unit (-24V)	1.0A	TSE6 to TSE7
Deflection coil drive (-15V)	5.0A	TSE1 to TSE3
Character (15V)	2.5A	TSD1 to TSE2
Video (+100V)	50mA	TSD10 to TSC8 (0V common)

TABLE 3

Test data

Test	Function	Check for	Control
1	MSKT5 to MSKT3 (earth)	Using DVM: +12V $\pm 1\%$	RV3
2	MSKT4 to MSKT3 (earth)	-12V $\pm 1\%$	RV6
3	MSKT1 to MSKT3 (earth)	+6V $\pm 1\%$	RV9
4	MSKT2 to MSKT3 (earth)	-6V $\pm 1\%$	RV12
5	EHT unit supply TSE6 (-ve) to TSE7 (+ve)	Using multimeter: -26.9V $\pm 5\%$	
6	Deflection coil drive supply TSE1 (-ve) to TSE3 (+ve)	Using multimeter: 19.2V $\pm 5\%$	
7	Character supply TSD1 (+ve) to TSD2 (-ve)	Using multimeter: 19.2V $\pm 5\%$	
8	Volts across C15 A/TP29 to TSD3 (earth)	Using multimeter: 180V $\pm 5\%$	
9	+100V video supply TSD10 (+ve) to TSD3 (earth)	Using multimeter: 96.9V - 110.16V	
10	+18V supply MSKT6 (+ve) to MSK3 (earth)	Using multimeter: +18V $\pm 5\%$	

Table 3 (Contd.)

Test	Function	Check for	Control
11	CRT heaters TSE8 to TSE9	Using multimeter: 6.3V a.c. $\pm 5\%$	
12	Zener diode currents	Unsolder cathode lead and insert multimeter in series with diode, setting control for current specified in Table 4 (depending on type of Zener diode in circuit) to accuracy $\pm 1\%$	
		Note ... When RV2, RV5, RV8 or RV11 are adjusted Tests 1, 2, 3 or 4 should be repeated)	
	MR34 (+12V supply)		RV2
	MR36 (-12V supply)		RV5
	MR38 (+6V supply)		RV8
	MR40 (-6V supply)		RV11
13	Ripple voltages (with respect to MSKT3)		
	MSKT5 (+12V supply)	ripple less than 1mV peak-to-peak	
	MSKT4 (-12V supply)	ripple less than 1mV peak-to-peak	
	MSKT1 (+6V supply)	ripple less than 1mV peak-to-peak	
	MSKT2 (-6V supply)	ripple less than 1mV peak-to-peak	
14	Ripple voltages: between TSE1 and TSE3 (deflection coil drive supply)	less than 2V peak-to-peak	

Table 3 (Contd.)

Test	Function	Check for	Control
14	between TSE6 and TSE7 (EHT unit supply)	less than 2V peak-to-peak	
	between TSD1 and TSE2 (character supply)	less than 1.5V peak-to-peak	
	between TSD10 and TSD3 (+100V video supply)	less than 110mV	
15	Regulation: reduce loads on +12V, -12V, +6V and -6V stabilized power supplies in turn from 1.0A to 0.9A	with DVM: output voltage change to be not more than 1mV	
16	Stability: vary mains input voltage to stabilized supplies by $\pm 10\%$ of nominal	with DVM: output voltage of each supply to change by not more than $\pm 1mV$	
17	Stability: vary mains input voltage to unstabilized supplies by $\pm 10\%$ of nominal	with DVM: output voltage of each unstabilized supply to remain within the limits given in Table 5.	
18	Stability: vary mains input voltage to the +100V video supply by $\pm 10\%$ of nominal	with DVM: output to vary by not more than $\pm 4\%$ of nominal value as given in Test 9	
19	Regulation and ripple: increase loads on +12V, -12V, +6V and -6V stabilized supplies in turn from 1.0A to 1.4A	Adjust associated control for minimum ripple and steady output; increase load to 1.5A and check that output voltage decreases rapidly	

Table 3 (Contd.)

Test	Function	Check for	Control
14	between TSE6 and TSE7 (EHT unit supply)	less than 2V peak-to-peak	
	between TSD1 and TSE2 (character supply)	less than 1.5V peak-to-peak	
	between TSD10 and TSD3 (+100V video supply)	less than 110mV	
15	Regulation: reduce loads on +12V, -12V, +6V and -6V stabilized power supplies in turn from 1.0A to 0.9A	with DVM: output voltage change to be not more than 1mV	
16	Stability: vary mains input voltage to stabilized supplies by $\pm 10\%$ of nominal	with DVM: output voltage of each supply to change by not more than $\pm 1mV$	
17	Stability: vary mains input voltage to unstabilized supplies by $\pm 10\%$ of nominal	with DVM: output voltage of each unstabilized supply to remain within the limits given in Table 5.	
18	Stability: vary mains input voltage to the +100V video supply by $\pm 10\%$ of nominal	with DVM: output to vary by not more than $\pm 4\%$ of nominal value as given in Test 9	
19	Regulation and ripple: increase loads on +12V, -12V, +6V and -6V stabilized supplies in turn from 1.0A to 1.4A	Adjust associated control for minimum ripple and steady output; increase load to 1.5A and check that output voltage decreases rapidly	

Chapter 2

EHT POWER UNIT 11601

LIST OF CONTENTS

	Para.
Removal and replacement procedures	1
Test data	4

LIST OF TABLES

	Table
Test equipment	1
Test data	2

REMOVAL AND REPLACEMENT PROCEDURES

Removal procedure

1. Unplug the EHT connector from the anode cap on the side of the cathode-ray tube and remove each taper pin connector from terminal block TSA. Loosen the three captive screws securing the EHT power unit to the viewing unit cold plate and withdraw the power unit from the viewing unit chassis, taking care that the EHT connector and cable do not foul other components.

Replacement procedure

2. Place the EHT power unit in position in the viewing unit and secure it with the three captive screws. Insert the taper pin connectors into terminal block TSA; each taper pin lead is identified by sleeves bearing the block letter and pin number.

3. Fit the EHT connector on the anode cap of the cathode-ray tube.

TEST DATA

Introduction

4. This chapter contains test data derived from Plessey Radar Ltd. Test Specification No. F.C.T.371.
5. Refer to Bench Test Procedures for test procedures with the board connected in the Printed Circuit and Power Unit Test Unit (687/1/01436), e.g. at L1.
6. Refer to A.P.115B-0514-1 and the Master Work Sheets for procedures using the Comprehensive Display Test Set 10060, e.g. at G.R.S.C.
7. Refer to the station list of approved test equipment for details of specific available test equipment.

TABLE 1

Test equipment

Comprehensive Display Test Set 10060
Oscilloscope CT536 or equivalent
Multimeter CT498 or equivalent
Electrostatic voltmeter, 0-18kV (such as the Pye Scalamp)
Power supply capable of supplying 0 to +30V d.c. at 3A
Power supply capable of supplying -12V to +12V d.c. at 0.5A

TABLE 2

Test data

Test	Function	Check for	Control
1	EHT voltage output	Output voltage = +15kV for load current 200 μ A Current drawn from +24V d.c. supply to be 0.8 to 1.3A RV1 to be capable of varying EHT from less than 14kV to greater than 16kV	RV1
2	EHT regulation with load current variation	EHT output voltage to be less than 200V for load current variation 0 to 200 μ A	
3	Stability vary +24V d.c. input to TSA1 from +10% to -10%	EHT output voltage change to be less than 200V	
4	Ripple voltage	Connect 0.001 μ F capacitor to EHT output and a 2.2Mohm resistor between other end of capacitor and earth. Monitor ripple at junction between capacitor and resistor. Ripple must be less than 25V peak-to-peak.	
5	+350V d.c. line TSA2 to TSA5 (earth)	With multimeter on 2500V range: voltage measured to lie in range +298 to +352	
6	EHT voltage control	When voltage between TSA4 and TSA5 (earth) is varied between +12V and -12V, EHT voltage must vary by at least \pm 0.6kV from nominal	

Chapter 3

DEFLECTION COIL DRIVE AMPLIFIER 12502

LIST OF CONTENTS

	Para.
Removal and replacement procedures	1
Test data	3

LIST OF TABLES

	Table
Test equipment	1
Test data	2

LIST OF ILLUSTRATIONS

	Fig.
Output waveforms	1

REMOVAL AND REPLACEMENT PROCEDURES

Removal procedure

1. Unplug each taper pin connector from terminal block TSA and TSB on the amplifier printed wiring board. Remove the six screws (three along each of the longer sides, accessible through holes in the board) and lift the amplifier from the viewing unit.

Replacement procedure

2. Place the amplifier in position in the viewing unit and secure it with the six screws. Replace the taper pin connectors in terminal blocks TSA and TSB.

TEST DATA

Introduction

3. This chapter contains test data derived from Plessey Radar Ltd. Test Specification No. F.C.T.100.
4. Refer to the Bench Test Procedures for procedures with the unit connected to an otherwise serviceable display, e.g. at L1.
5. Refer to A.P.115D-0514-1 and the Master Work Sheets for procedures using the Comprehensive Display Test Set 10060, e.g. at G.R.S.C.
6. Refer to the station list of approved test equipment for details of specific available test equipment.
7. The deflection coil drive amplifier should not be operated when it is out of the viewing unit unless adequate provision is made for dissipating the heat generated.

TABLE 1

Test equipment

Comprehensive Display Test Set 10060 or working display
Oscilloscope CT536 or equivalent
Multimeter CT498 or equivalent

TABLE 2

Test Data

Test	Function	Check for	Control
1	Amplifier output TSA2	D.C. output voltage can be varied from more positive than -0.5V to more negative than -0.7V: set to -0.6V	RV4

Table 2 (Contd.)

Test	Function	Check for	Control
2	Amplifier output TSA9	as for Test 1	RV3
3	Amplifier output TSB2	as for Test 1	RV1
4	Amplifier output TSB9	as for Test 1	RV2
5	Amplifier output waveform TSA1	With complementary square-wave inputs (amplitude 3.75V \pm 0.25V peak-to-peak symmetrical about zero volts) fed to TSA4 and TSB7, check that the amplifier output waveform is as shown in Fig. 1.	
6	Amplifier output waveform TSB10	repeat Test 5	
7	Amplifier output waveform TSA10	With complementary square-wave inputs (amplitude 3.75V \pm 0.25V peak-to-peak symmetrical about zero volts) fed to TSB4 and TSA7, check that waveform is as shown in Fig. 1.	
8	Amplifier output waveform TSB1	repeat Test 7	

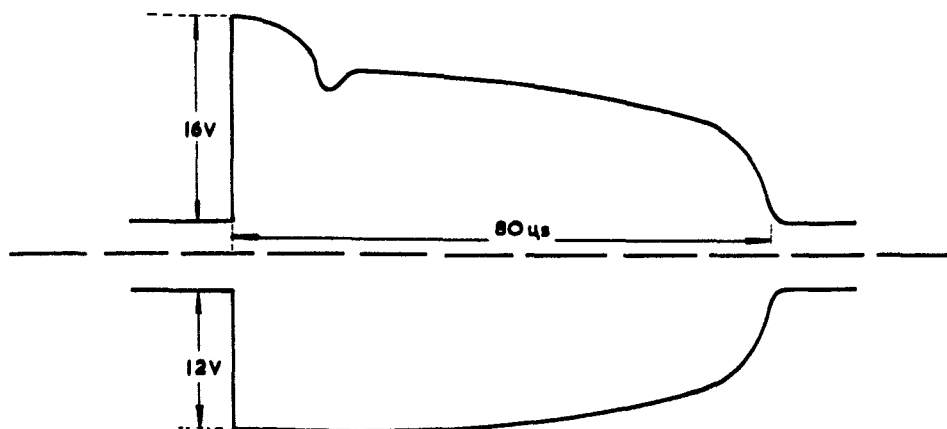


Fig. 1. Output waveforms

Chapter 4

POWER UNIT 11605

LIST OF CONTENTS

	Para.
Removal and replacement procedures	
Removal	1
Replacement	2
Test data	
Introduction	3

LIST OF TABLES

	Table
Test equipment	1
Dummy loads	2
Test data	3

REMOVAL AND REPLACEMENT PROCEDURES

Removal

1. Unplug each taper pin connector from the terminal block. Loosen the captive screws securing the power unit to the viewing unit. Withdraw the power unit from the main chassis (it may be necessary to loosen the cable looms on the main chassis).

Replacement

2. Locate the power unit in position on the viewing unit chasis and secure with the captive screws. Insert the taper pin connectors into the appropriate terminal blocks, each taper pin lead is identified by sleeves bearing the block letter and pin number.

TEST DATA

Introduction

3. This chapter contains test data derived from Plessey Radar, Test Specification No. FCT187.

4. Refer to Bench Test Procedures for test procedures with the board connected in the Printed Circuit and Power Unit Test Unit (687/1/01436), e. g. at L1.
5. Refer to A. P.115K,1210-1 and the Master Work Sheets for procedures using the Comprehensive Display Test Set Type 10060, e. g. at G. R. S. C.
6. Refer to the station list of approved test equipment for details of specific available test equipment.

TABLE 1
Test equipment

Comprehensive Display Test Set 10060 (or working display)
 Oscilloscope CT 536 or equivalent
 Two multimeters CT 498 or equivalent
 Two dummy loads (as given in Table 2)
 Power supply capable of supplying +12V d. c.
 Power supply capable of supplying -15V d. c.
 5k potentiometer (such as the Colvern CLV/RE) in series with 33k resistor (such as Electrosil CJ20)
 2.5k potentiometer (such as the Colvern CLV/RE) in series with 2.2k resistor (such as Electrosil CJ20)
 Variac 0V to 270V, 2A

TABLE 2
Dummy loads

	Power supply	Load	Dummy load connections
1.	-22V	10A variable resistor with series Avometer on 10A d. c. range.	(TSD1, TSD2) and (TSD3, TSD4). Note: TSD1 and TSD2, and TSD3 and TSD4, are to be paralleled.
2.	Focus coil drive	29ohm resistor 6W (27 ohm in series Avometer on 1A d. c. range.	TSE2 and TSE3.

TABLE 3
Test data

Test	Function	Check for	Control
1		<p>Connect mains L output of variac to TSC6. Connect mains N output of variac to TSB9. Connect mains E to TSB10. Connect mains L, N and E to variac. Check that cut-outs X1 and X2 are set to 'on'. Connect dummy load 1 (Table 2) Switch mains 'on' and adjust variac for 250V a. c. Adjust dummy load1 for 10A.</p>	
2	Supply voltage between TSD1 and TSD3.	22V \pm 0.6V d. c.	
3	Supply voltage between TSD1 and TSD3	<p>Polarity. TSD1 shall be negative w. r. t. TSD3.</p>	
4	Supply voltage between TSD1 and TSD3.	<p>Ripple. Using oscilloscope on TSD1 ripple shall be less than 1.3V peak-to-peak.</p>	
5	A. C.1A output between TSD5 and TSD6	Using Avometer on 10V a. c. range 6.3V \pm 5%.	
6		<p>Disconnect dummy load 1 (Table 2) Connect +12V power supply to TSE10. Connect TSE8 to earth (i. e. 0V of +12V and -15V power supplies. Connect -15V power supply to TSE1.</p>	
7		<p>Connect dummy load 2 (Table 2) Connect the 2.5k potentiometer and 2.2k resistor in series between +12V and earth (potentiometer at earth end), and connect the wiper of the potentiometer to TSE5. Set potentiometer to zero. Switch +12V and -15V power supplies 'on'.</p>	

TABLE 3 (continued)

Test	Function	Check for	Control
8		RV1 varying current through dummy load 2 (Table 2).	RV1
9		Current set to 300mA	RV1
10		External 2.5k potentiometer varying current through dummy load 2 (Table 2) from 300mA to greater than 380mA but not greater than 450mA.	
11		Current set to 350mA	External 2.5k pot.
12	Focus coil drive amplifier	+12V HT current 10.5mA \pm 1mA.	
13	Amplifier stability TSE2 and earth	Using oscilloscope. amplifier shall be stable, i. e. no HF oscillation.	
14		Connect TSD6 to TSE6 (earth). Connect the 5k potentiometer and 33k resistor in series between TSD5 and TSE7 (earth), with potentiometer at earth end, and connect the wiper of the potentiometer to TSE4. Monitor between TSE2 and earth with the oscilloscope.	
15	Output at TSE2	4V peak-to-peak.	External 5k pot.

Chapter 5

POWER UNIT 11606

LIST OF CONTENTS

	Para.
Removal and replacement procedures	
Removal procedure	1
Replacement procedure	2
Test data	
Introduction	3

LIST OF TABLES

	Table
Test equipment	1
Dummy loads	2
Test data	3
Zener diode currents	4
Unstabilised power supply checks	5

REMOVAL AND REPLACEMENT PROCEDURES

Removal procedure

1. Unplug each taper pin connector from terminal blocks TSA to TSF. Loosen the four captive screws and two other screws securing the power unit to the viewing unit cold plate. Withdraw the power unit from the viewing unit assembly (it may be necessary to loosen the cable looms on the main chassis).

Replacement procedure

2. Locate the power unit in position on the viewing unit chassis and secure with the four captive screws and the two additional screws. Insert the six taper pin connectors into terminal blocks TSA to TSF.

TEST DATA

Introduction

3. This chapter contains test data derived from Plessey Radar, Test Specification No. FCT183.

4. Refer to Bench Test Procedures for test procedures with the board connected in the Printed Circuit and Power Unit Test Unit (687/1/01436), e. g. at L1.
5. Refer to A. P.115K-1210-1 and the Master Work Sheets for procedures using the Comprehensive Display Test Set Type 10060, e. g. at G. R. S. C.
6. Refer to the station list of approved test equipment for details of specific available test equipment.

TABLE 1
Test equipment

Comprehensive Display Test Set 10060
 Oscilloscope CT 536 or equivalent
 Multimeter CT 498 or equivalent
 Digital voltmeter CT 470D (set) or equivalent
 Dummy loads (as given in Table 2)

TABLE 2
Dummy loads

Power supply	Load	Dummy load connections
+6V	0.9, 1.0, 1.4 and 1.5A	TSC1 to TSC8 (earth)
-6V	0.9, 1.0, 1.4 and 1.5A	TSC5 to TSC8 (earth)
+12V	0.9, 1.0, 1.4 and 1.5A	TSC2 to TSC8 (earth)
-12V	0.9, 1.0, 1.4 and 1.5A	TSC7 to TSC8 (earth)
Character (15V)	2.5A	TSD1 to TSE2
Deflection coil drive (-15V)	1A	TSE1 to TSE3
EHT unit (-24V)	1A	TSE6 to TSE7
Video (+100V)	50mA	TSD10 and TSC8 (0V common)

TABLE 3

Test data

Test	Function	Check for	Control
		Using d. v. m. :	
1	MSKT1 to MSKT3 (earth)	+6V $\pm 1\%$	RV9
2	MSKT2 to MSKT3 (earth)	-6V $\pm 1\%$	RV12
3	MSKT5 to MSKT3 (earth)	+12V $\pm 1\%$	RV3
4	MSKT4 to MSKT3 (earth)	-12V $\pm 1\%$	RV6
5	EHT unit supply TSE6 (-ve) to TSE7 (+ve)	Using multimeter: -26.9V $\pm 5\%$	
6	Deflection coil drive supply TSE1 (-ve) to TSE3 (+ve)	Using multimeter: 19.2V $\pm 5\%$	
7	Character supply TSD1 (+ve) to TSE2 (-ve)	Using multimeter: 19.2V $\pm 5\%$	
8	+100 video supply TSD10 (+ve) to TSC8 (earth)	Using multimeter: 96.9V -107.1V	
9	+18V supply MSKT6 (+ve) to MSKT3 (earth)	Using multimeter: +18V $\pm 5\%$	
10	Volts across C15 A/TP29 to TSD3 (earth)	Using multimeter: 180V $\pm 5\%$	
11	CRT heaters, TSE8 and TSE9	Using multimeter: 6.3V a. c. $\pm 5\%$	
12	Zener diode currents	Unsolder cathode lead and insert multimeter in series with diode, setting control for current specified in Table 4 (depending on type of Zener diode in circuit) to accuracy $\pm 1\%$	
		Note: When RV2, RV5, RV8 or RV11 are adjusted Tests 1, 2, 3, or 4 should be repeated.	

TABLE 3 (continued)

Test	Function	Check for	Control
	MR34 (+12V supply)		RV2
	MR36 (-12V supply)		RV5
	MR38 (+6V supply)		RV8
	MR40 (-6V supply)		RV11
13	Ripple voltages (with respect to MSKT3)		
	MSKT5 (+12V supply)	Ripple less than 1mV peak-to-peak.	
	MSKT4 (-12V supply)	Ripple less than 1mV peak-to-peak.	
	MSKT1 (+6V supply)	Ripple less than 1mV peak-to-peak.	
	MSKT2 (-6V supply)	Ripple less than 1mV peak-to-peak.	
14	Ripple voltages:	Using oscilloscope:	
	between TSE1 and TSE3 (deflection coil drive supply)	less than 200mV peak-to-peak.	
	between TSE6 and TSE7 (EHT unit supply)	less than 2V peak-to-peak.	
	between TSD1 and TSE2 (character supply)	less than 1.5V peak-to-peak.	
	between TSD10 and TSC8 (+100V video supply)	less than 110mV peak-to-peak.	
15	Regulation:	With d. v. m. :	
	reduce loads on +12V, -12V, +6V and -6V stabilised power supplies in turn from 1.0A to 0.9A.	output voltage change to be not more than 1mV.	
16	Stability:	With d. v. m. :	
	vary mains input voltage to stabilised supplies by $\pm 10\%$ of nominal.	output voltage of each supply to change by not more than ± 1 mV.	

TABLE 3 (continued)

Test	Function	Check for	Control
17	Stability: vary mains input voltage to unstabilised supplies by $\pm 10\%$ of nominal.	With d. v. m. output voltage of each unstabilised supply to remain within the limits given in Table 5.	
18	Stability: vary mains input voltage to the +100V video supply by $\pm 10\%$ of nominal.	With d. v. m. : output to vary by not more than $\pm 4\%$ of nominal value as given in Test 8.	
19	Regulation and ripple: increase loads on +12V -12V, +6V and -6V stabilised supplies in turn from 1. 0A to 1. 4A.	adjust associated control for minimum ripple and steady output; increase load to 1. 5A and check that output voltage decreases rapidly.	
	+12V supply MSKT5		RV1
	-12V supply MSKT4		RV4
	+6V supply MSKT1		RV7
	-6V supply MSKT2		RV10

TABLE 4
Zener diode currents

Zener diode	Current
SZT18	2. 9mA
SZT19	3. 2mA
SZT20	3. 6mA
SZT21	3. 9mA
SZT22	4. 4mA

TABLE 5

Unstabilised power supply checks

Monitor points	Output voltage for mains input voltage -10% from nominal	Output voltage for mains input voltage +10% from nominal
TSE6 and TSE7	Not less than -23.5V	Not greater than -30.5V
TSE1 and TSE3	Not less than +15.8V	Not greater than +20V
TSD1 and TSE2	Not less than +15.8V	Not greater than +21.5V

Chapter 6

DEFLECTION COIL DRIVE AMPLIFIER 12505

LIST OF CONTENTS

	Para.
Removal and replacement procedures	
Removal	1
Replacement	2
Test data	
Introduction	3

LIST OF TABLES

	Table
Test equipment	1
Test data	2

LIST OF ILLUSTRATIONS

	Fig.
Output waveforms	1

REMOVAL AND REPLACEMENT PROCEDURES

Removal

1. Unplug each taper pin connector from the terminal blocks. Loosen the captive screws securing the amplifier to the viewing unit. Withdraw the amplifier from the main chassis (it may be necessary to loosen the cable looms on the main chassis).

Replacement

2. Locate the amplifier in position on the viewing unit chassis and secure with the captive screws. Insert the taper pin connectors into the appropriate terminal blocks; each taper pin lead is identified by sleeves bearing the block letter and pin number.

TEST DATA

Introduction

3. This chapter contains test data derived from Plessey Radar Test Specification No. FCT361.
4. Refer to the Bench Test Procedures for procedures with the unit connected to an otherwise serviceable display, e. g, at L1.
5. Refer to AP115K-1210-1 and the Master Work Sheets for procedures using the Comprehensive Display Test Set 10060, e. g. at G. R. S. C.
6. Refer to the station list of approved test equipment for details of specific available test equipment.
7. The deflection coil drive amplifier should not be operated when it is out of the viewing unit unless adequate provision is made for dissipating the heat generated.

TABLE 1
Test equipment

Comprehensive Display Test Set 10060 or working display
Avometer Model 8.
Tektronix Oscilloscope Type 545A, with plug-in Unit Type H
21in Deflection Coil Type 11703
Power supply +12V stabilised and -22V unstabilised
A source of two adjustable complementary $\pm 4V$ peak square-waves at a frequency of less than 1kHz.
Heat sink

TABLE 2
Test data

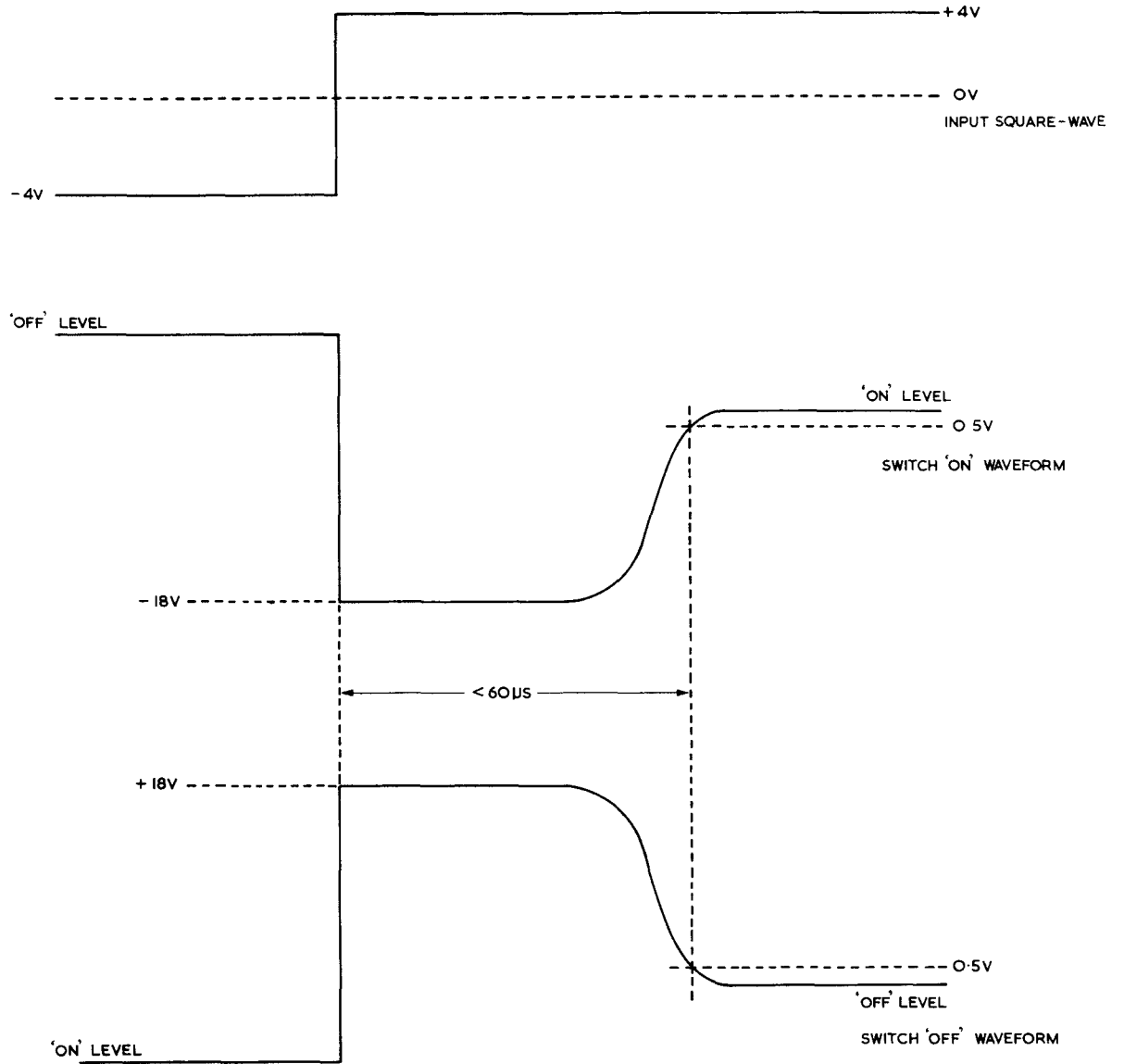
Test	Function	Check for	Control
1		Note: The deflection coil must be connected to the final drive amplifier before switching the power supplies on. The -22V supply must never be switched on while the +12V supply is off.	

TABLE 2 (continued)

Test	Function	Check for	Control
2		Connect +12V to TSB6. Connect earth to TSB5, TSA1 and TSB1. Connect -22V to TSA7. Connect -22V return (earthy) to TSA8. Connect the X-axis A coil of the Deflection Coil Type 11703 to TSB9 and TSB10. Connect the X-axis B coil to the Deflection Coil Type 11703 to TSA9 and TSA10. Place the final deflection amp- plifier on the heat sink. Turn RV1 and RV2 fully clockwise.	
3	Insulation between TR5, TR6, TR11 and TR12 collectors and chassis.	<u>No</u> continuity.	
4	Monitor TSA10 w. r. t. earth.	Use Avometer on 2.5V range (+ve to earth). Switch on d. c. supplies. Less than 0.1V. Note: A meter reading of greater than 1.5V indicates a fault condition which could destroy the output transistor if the power supplies are left on. Switch off d. c. supplies.	
5	Monitor TSB10 w. r. t. earth.	Use Avometer on 2.5V d. c. range. (+ve to earth). Switch on d. c. supplies. Less than 0.1V.	
6		Variation from less than 0.1V to more than 1.1V.	RV1
7		Voltage adjusted to 0.625V.	RV1

TABLE 2 (continued)

Test	Function	Check for	Control
8	Monitor TSA10 w. r. t. earth.	Use Avometer on 2.5V d. c. range (+ve to earth). Variation from less than 0.1V to more than 1.1V.	RV2
9		Voltage adjusted to 0.625V.	RV2
10	TR5 emitter resistors R18 and R19	Voltage across resistors 1.0V $\pm 2\%$.	
11	TR6 emitter resistors R23 and R24	1.0V $\pm 2\%$.	
12	TR11 emitter resistors R41 and R42	1.0V $\pm 2\%$.	
13	TR12 emitter resistors R44 and R45	1.0V $\pm 2\%$.	
14	+12V	Supply current 25mA ± 2 mA.	
15		Remove earth connections from TSA1 and TSB1. Connect the two complementary ± 4 V peak square-waves to TSA1 and TSB1 respectively, see Fig. 1. Monitor TSA10 with the oscilloscope and adjust the amplitude of the input square-waves to give an output square-wave of ± 0.6 V peak about a d. c. level of -0.625 V.	
	Monitor TSA9	(Using oscilloscope) switching transient recovers to 0.5V in less than $60\mu s$ (Fig. 1).	
16		Monitor TSB10 and adjust the amplitude of the input square-waves to give an output square-wave of ± 0.6 V peak about a d. c. level of -0.625 V.	
	Monitor TSB9	(Using oscilloscope) switching transient recovers to 0.5V in less than $60\mu s$ (Fig. 1).	



PLUG-IN BOARD
TEST PROCEDURES

Chapter 1

TIMING BOARDS
(MJE series)

Introduction

1. This chapter contains test data derived from Plessey Radar Limited Test Specification No. F. C. T. 116.
2. Refer to the Bench Test Procedures for procedures with the board connected to an otherwise serviceable display, e. g. at L1.
3. Refer to A. P. 115B-0514-1 and the Master Work Sheets for procedures using the Comprehensive Display Test Set Type 10060, e. g. at G. R. S. C.
4. Refer to the station list of approved test equipment for details of specific available test equipment.

Table 1

TEST EQUIPMENT

Test equipment required	Function
Comprehensive Display Test Set 10060 or Working Display	
Oscilloscope CT536 or equivalent	To measure rise times of 100ns
Multimeter CT498 or equivalent	General purpose voltage measurement.

- Note:
- (1) When checked on the comprehensive display test set the timing board links should be set for radius scan operation, i. e. links E-F, J-H, M-Y, K-L and R-S.
 - (2) When checked in a working p. p. i. display the link settings as in (1) apply.
 - (3) When checked in a working h. r. i. display the links should be set for h. r. i. operation.

Table 2

LIST OF TESTS

Test	Function	Check for	Control
1	Delay, TR62 coll. w. r. t. trigger (osc. trigger MSKT1)	Delays obtainable: 0.22 to 0.6 μ s (links X4-5, X5-6) 0.6 to 1.5 μ s (links X1-2, X5-6) 1.5 to 2.6 μ s (links X1-4, X4-5, X5-6) 2.6 to 5.4 μ s (links X1-4, X4-5, X5-6)	RV12
2	Delay negative edge TR65 coll. w. r. t. negative edge TR62 coll. (osc. trigger MSKT1).	Delay range of 0.5 μ s to 1.5 μ s obtainable.	RV6
3	Sawtooth TR31 base (osc. trigger MSKT1)	Positive peak at -2V Sweep durations: MJEC 2973 μ s MJEG 930 μ s MJEJ 1243 μ s	RV1 RV5
4	Timebase gate MSKT16 (osc. trigger MSKT1)	Amplitude: ± 1.75 V Rise time: \downarrow 350ns Fall time: \downarrow 350ns +ve durations: As for Test 3.	
5	Brilliance gate waveform MSKT6 (osc. trigger MSKT1)	Amplitude: ± 5 V Negative during mainscan period. Rise time: \downarrow 200ns Fall time: \downarrow 200ns Durations: As for Test 3.	
6	IS timer output MSKT12 (osc. trigger MSKT12)	Duration: 100ms Amplitude: $\downarrow \pm 5$ V	RV11
7	IS switch waveform scan MSKT9	Amplitude: $\downarrow \pm 5$ V Positive during mainscan Negative during interscan	
8	MS switch waveform scan PLF5 (osc. trigger MSKT12)	Amplitude: $\downarrow \pm 5$ V Negative during mainscan	
9	IS switch waveform shift PLF11 (osc. trigger MSKT12)	Amplitude: $\downarrow \pm 5$ V Positive during mainscan	

Table 2 (contd.)

Test	Function	Check for	Control
10	MSKT13 (osc. trigger MSKT12)	With +6V connected to PLE3: D. C. level: \dagger -5V. With -6V connected to PLE3: Gate waveform amplitude: \dagger \pm 5V. Negative during mainscan.	
11	Brilliance gate waveform MSKT6 (osc. trigger MSKT12)	Width variable from full period to zero in IS periods.	Range pot. (p. p. i.) External range control (h. r. i.)
12	Square waveform MSKT7 (osc. trigger MSKT7)	Amplitude approximately +12V period 2.5ms \pm 250 μ s	
13	Negative sampling gate waveform MSKT3 (osc. trigger MSKT3)	Negative-going waveform 30-60 μ s variable. Amplitude: \dagger 1.75V.	RV8
14	Positive sampling gate waveform PLE9 (osc. trigger MSKT3)	Inverse of Test 13 waveform.	
15	Squarewave TR13 collector (osc. trigger MSKT1)	Amplitude: \dagger +4V to -5V.	RV3 at mid-position
16	Squarewave TR16 collector	Amplitude 1V less than Test 15 d. c. voltage to \dagger -5V, mark/space ratio unity.	RV4
17	Balancing resolver power amplifier monitoring C71, R203 junction.	Minimum ripple.	RV10 (RV7 and RV9 to mid- position).
18	Resolver drive waveform MSKT2	Amplitude to be 35V peak-to-peak.	Set on high side with RV7 and reduce to 35V with RV9.

Table 2 (contd.)

Test	Function	Check for	Control
19	MSKT8	+4.5V d. c. (using multimeter)	RV9
20	Sampling gate pulse MSKT3 (osc. trigger MSKT3)	Note position of trailing edge for next test.	
21	Resolver drive waveform MSKT2 (osc. trigger MSKT3)	Set trailing edge to peak or trough of sinewave (Test 20)	RV3

Chapter 2

DEFLECTION BOARDS
(MRG and MRH series)

LIST OF TABLES

	Table
Test equipment required	1
List of tests	2
Test 8 for board variants	3

Introduction

1. This chapter contains test data derived from Plessey Radar Ltd. Test Specification No. F.C.T.125.
2. Refer to Bench Test Procedures for test procedure with the board connected in an otherwise serviceable display (e.g. at L1).
3. Refer to A.P.115B-0514-1 and Master Work Sheets for procedure using the Display Test Set Type 10060 (e.g. at G.R.S.C.).
4. Refer to station List of Approved Test Equipment for details of specific available test equipment.

Table 1

TEST EQUIPMENT REQUIRED

Test equipment	Recommended type
Display Test Set (or working display)	10060
Oscilloscope	CT536 or equivalent

Table 2

LIST OF TESTS

Test No.	Function	Switches at 'Test'	Check for	Control
1	Demod. inverting amp. o/p at MSKT10 (Osc. trig. MSKT3 on timing board)	SA (SA to RUN)	Zero level O/p inversely follows input at MSKT13 as resolver is turned (O/p ampt. is function of resolver type)	RV1
2	MS scan CV at MSKT14 (Osc. trig. MSKT3 on timing board)	SA and SB	Scan ampt. to be zero W/form level to be zero	RV6 RV2
3	MS scan CV at MSKT14 (Osc. trig. MSKT3 on timing board)		DC level varying with resolver rotation or aerial/simulator nuttation. Set limits of excursion to + and -4V	RV4
4	IS sw. buffer amp. o/p at TR18 collector (Osc. trig. MSKT3 on timing board)	SG (SG to RUN)	Amp o/p 0V wrt earth (P.P.I. boards only). See connections - Fig.1 1. Set PLC4 i/p to +6V; check that TR18 collector can be set to -4V. Set to -4V. 2. Set PLC4 i/p to -6V; check that TR18 collector is at +4V±5%	RV20
5	Sw. scan CV at MSKT11 (Osc. trig. MSKT3 on timing board)		See connections - Fig.1 1. Check CV varies with resolver position (or aerial or simulator angle) during interscan 2. Check CV varies with potentiometer setting during interscan	

Table 2 (contd.)

Test No.	Function	Switches at 'Test'	Check for	Control
6	Scan w/form at MSKT7 (Osc. trig. MSKT3 on timing board)	SH (SH to RUN)	See connections - Fig. 2	
			1. Check scan ampt. can be set to 0V	RV10
			2. (P.P.I. only). Check scan waveform level can be set to 0V	RV9
			3. (P.P.I. only). Check sawtooth ampt. varies with resolver position	
			4. (P.P.I. only). Check that sawtooth max. excursion can be limited at +4V and -4V	RV8
7	Def. drive waveform at MSKT1 (Osc. trig. MSKT3 on timing board) at MSKT5	SE	Set RV15 and RV16 fully clockwise	
			Check that waveform level can be set to 0V	RV13
			Check that waveform level can be set to 0V	RV14
8	Waveform at MSKT1		See connections - Fig. 3 See Table 3 With inputs as Col. 2, 3 and 4 check scan waveform ampt. as Col. 5	
9	Scan waveform at MSKT7 (Osc. trig. MSKT3 on timing board) at MSKT1 at MSKT1 at PLD20		Set resolver to obtain + and -4V scan ampt. at MSKT7	
			Set waveform to limit at +4V	RV16
			Set waveform to limit at -4V	RV15
			Check same as MSKT1	

Table 2 (contd.)

Test No.	Function	Switches at 'Test'	Check for	Control
10	Drive waveform at MSKT5 (Osc.trig.MSKT3 on timing board)		Check that waveform is the inverse of that at MSKT1	
	at PLD17		Check that waveform is same as at MSKT5	
11	Sw. shift volts at MSKT18 (Osc.trig.MSKT12 on timing board)	SD (SD to RUN)	Waveform to be at 0V See connections - Fig.1 1. For +6V at C5/G5 waveform to be $-4V \pm 5\%$ 2. For -6V at C5/G5 waveform to be $+4V \pm 5\%$	
12	FS shift CV inverter output at TR67 collector (Osc.trig.MSKT1 on timing board)	SF (SD to RUN)	Output can set to 0Vd.c. Connect i/p to PLC17/G17 - see Fig.1 1. For input at +6V check that output is $-4V \pm 5\%$ 2. For input at -6V check that output is $+4V \pm 5\%$	RV18
13	Inverter output at MSKT9 (Osc.trig.MSKT1 on timing board)	SC (SF to RUN)	Output can set to 0V Connect input to PLC14/G14 - see Fig.1 1. For input at +4V check that output is $-4V \pm 5\%$	RV12
	at PLC16		2. Check same as MSKT9	
	at MSKT9		3. For input at -4V check that output is $+4V \pm 5\%$	
	at PLC16		4. Check same as MSKT9	

Table 3

TEST 8 FOR BOARD VARIANTS

Board type	T/B gate length	Connect 12V to			Set W/F ampt. at MSKT7	Check W/F ampt. at MSKT1
		D14	D15	D16		
MRGC	2.96ms	✓			-0.0V	+0.5V±5%
	2.96ms		✓		-0.5V	+1.0V±5%
	2.96ms			✓	-0.5V	+2.0V±5%
	2.96ms	No connection			-0.5V	+4.0V±5%
MRGE	1.96ms	✓			-0.4V	+0.4V±5%
	1.96ms		✓		-0.4V	+1.0V±5%
	1.96ms			✓	-0.4V	+2.0V±5%
	1.96ms	No connection			-0.4V	+4.0V±5%
MRGL	1.40ms	✓			-0.5V	+0.5V±5%
	1.40ms		✓		-0.5V	+1.0V±5%
	1.40ms			✓	-0.5V	+2.0V±5%
	1.40ms	No connection			-0.5V	+4.0V±5%
MRGR		No connection			-2.0V	+2.0V±5%
MRGX		No connection			-2.5V	+2.0V±5%
MRHG		No connection			-2.0V	+2.0V±5%

Note: 12V not connected: Range 1 (long) selected
12V to PLD16: Range 2 (med.long) selected
12V to PLD15: Range 3 (med.short) selected
12V to PLD14: Range 4 (short) selected

Chapter 3

DEFLECTION BOARDS

(MRK series)

LIST OF TABLES

	Table
Test equipment required	1
List of tests	2
Tests 5 and 6 for board variants	3

Introduction

1. This chapter contains test data derived from Plessey Radar Ltd. Test Specification No. F.C.T.115.
2. Refer to Bench Test Procedures for test procedure with the board connected to an otherwise serviceable display (e.g. at L1).
3. Refer to A.P.115B-0514 and Master Work Sheets for procedures using the Display Test Set Type 10060 (e.g. at G.R.S.C.).
4. Refer to station List of Approved Test Equipment for details of specific available test equipment.

Table 1

TEST EQUIPMENT REQUIRED

Test equipment	Recommended type
Display Test Set (or working display)	10060
Oscilloscope	CT536 or equivalent

TABLE 2

LIST OF TESTS

Note: Tests 3 to 7 are carried out with switch SA to TEST, tests 5 to 7 with the circuit connected as shown in Fig.1. and tests 10 and 12 with connections shown in Fig.2.

Test	Function	Check for	Control
1	Negative-going sawtooth MSKT6	Start level can be varied +2.6V to +3.2V, set level to +2.8V	RV1
2	Negative-going sawtooth MSKT6	End of run-down can be varied -2V to -5V; set to -2.8V run-down duration to be: 2968 μ s when used with timing board MJEC for range 240d.m.	RV5
3	'A' defl. drive w/f MSKT5	0Vd.c.	RV6
4	'B' defl. drive w/f MSKT13	0Vd.c.	RV6
5	MSKT5	See Fig.1. With RV3 and RV4 fully counter-clockwise: -4V \pm 5% with pot slider at +0.5V +4V \pm 5% with pot slider at -0.5V	
6	MSKT6	Operate relays RLC, RLB and RLA and repeat Test 5 to obtain following results: +6V to PLD16 (operates RLC) \pm 2V \pm 5% +6V to PLD15 (operates RLB) \pm 1V \pm 5% +6V to PLD14 (operates RLA) \pm 0.5V \pm 5%	
7	MSKT13	Repeat Test 5 to obtain: +4V \pm 5% with pot slider at +0.5V -4V \pm 5% with pot slider at -0.5V	

Table 2 (contd.)

Test	Function	Check for	Control
8	Sawtooth w/f MSKT5	Inverse waveform to MSKT6, of much larger amplitude, RV3 limits w/f to +4V, RV4 limits w/f to -4V	RV3 RV4
9	Sawtooth w/f MSKT5	For board tested in viewing unit: Sawtooth baseline varies inversely with setting of X CENTRE (Viewing Unit Control Panel); longest range must be selected	X CENTRE
10	Sawtooth w/f MSKT5	For board separated from viewing unit: Connect pot slider to PLD22 and +6V to PLD14 (Fig. 2); sawtooth baseline varies inversely with setting of pot slider	
11	Sawtooth w/f MSKT5	For board tested in viewing unit: Sawtooth baseline varies inversely with setting of RADAR SHIFT (Operator's control panel); longest range must be selected	RADAR SHIFT
12	Sawtooth w/f MSKT5	For board separated from viewing unit: Connect pot slider to PLC8 and +6V to PLD14 (Fig. 2); sawtooth baseline varies inversely with setting of pot slider	

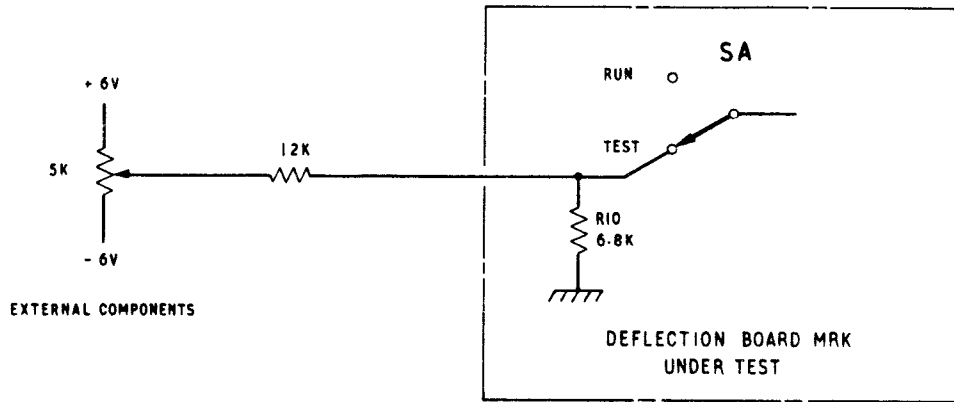


Fig. 1 Circuit connections for Tests 5-7

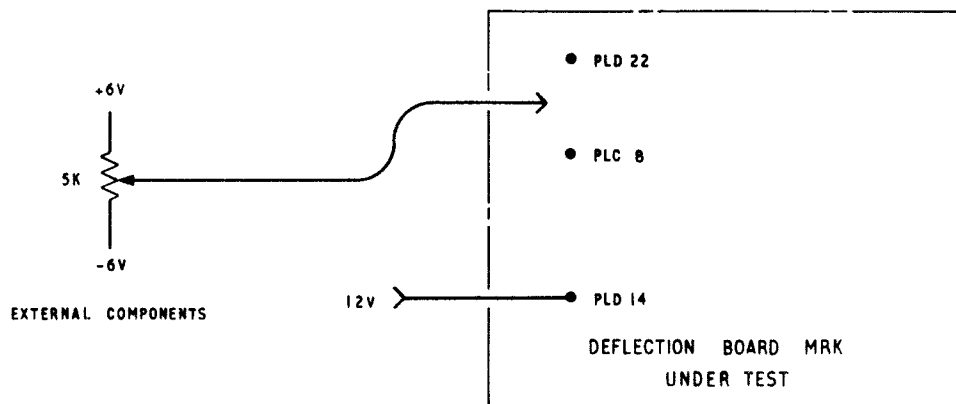


Fig. 2 Circuit connections for Tests 10 and 12

Table 3

TESTS 5 AND 6 FOR BOARD VARIANTS

Board type	Connect 12V to			Set d.c. level at TR5 base to	Measure at MSKT5	Measure at MSKT13
	D14	D15	D16			
MRKC	✓			+0.5V	-0.5V±5%	+0.5V±5%
		✓		+0.5V	-1.0V±5%	+1.0V±5%
			✓	+0.5V	-2.0V±5%	+2.0V±5%
		No connection		+0.5V	-4.0V±5%	+4.0V±5%
	✓			-0.5V	+0.5V±5%	-0.5V±5%
		✓		-0.5V	+1.0V±5%	-1.0V±5%
			✓	-0.5V	+2.0V±5%	-2.0V±5%
		No connection		-0.5V	+4.0V±5%	-4.0V±5%

Chapter 4

VIDEO BOARDS
(MFD series)

Introduction

1. This chapter contains test data derived from Plessey Radar Ltd Test Specification No. F. C. T. 105.
2. Refer to the Bench Test Procedures for procedures with the board connected to an otherwise serviceable display, e. g. at L1.
3. Refer to A. P. 115B-0514-1 and the Master Work Sheets for procedures using the Comprehensive Display Test Set Type 10060, e. g. G. R. S. C.
4. Refer to the station list of approved test equipment for details of specific available test equipment.

Table 1

TEST EQUIPMENT REQUIRED

Oscilloscope CT536 or equivalent
Multimeter CT498 or equivalent
Nagard Pulse Generator Type 5002/c, or equivalent, capable of providing a pulse of amplitude 200mV, p. r. f. 100Hz and length 1 μ s, 100 μ s, or 5ms.

Table 2

LIST OF TESTS

Test	Function	Check for	Control
1	TR1 and TR2 collector potentials	Equal potentials, using multimeter; (1) video 1 gain to max. , other gain controls to min. , video 2 only selected	RV1

Table 2 (Contd.)

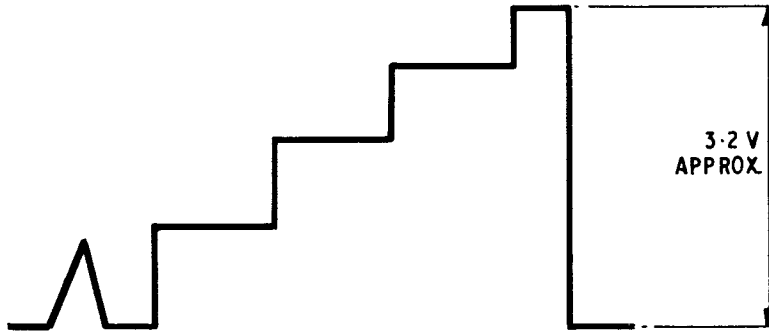
Test	Function	Check for	Control
		(2) video 2 gain to max. , other gain controls to min. , video 2 only selected	RV2
		(3) video 3 gain to max. , other gain controls to min. , video 3 only selected	RV3
		(4) video 4 gain to max. , other gain controls to min. , video 4 only selected	RV4
2	TR24 base potential	+2.5V w. r. t. earth	RV5
3	CRT cathode volts PLB2	RV7 fully counter-clockwise, adjust RV5 for +95V	RV5
4	Video channel check. CRT cathode w/f PLB2	With pulse amplitude 200mV, p. r. f. 100Hz and length 100 μ s connected to video 1 i/p (PLA2):- (1) when pulse width is reduced until PLB2 w/f falls to 0.707 of original o/p at 100 μ s, pulse width to be less than 200ns (2) when pulse width is 5ms droop to be less than 5% (3) when pulse width is 1 μ s no distortion to occur and overshoot to be less than 10% (4) video gain control reduces w/f to zero smoothly, video sel- ector inhibits the output	
5	Video channel check CRT cathode w/f PLB2	Repeat Test 4 for other video channels: Video 2 i/p PLA3	

Table 2 (Contd.)

Test	Function	Check for	Control
		Video 3 i/p PLA4	
		Video 4 i/p PLA5	
6	Junction of C36 and TR54 base	With all video selector switches OFF and gain controls fully counter-clockwise	RV12
		obtain max. amplitude oscillation (approx. 12V peak-to-peak)	
7	TR57 collector	Square wave, 12V peak-to-peak, equal mark-space ratio	RV13
8	TR58 base w/f	Staircase w/f with correct number of steps (see Fig. 1)	RV14
		Suppression of first staircase pulse	RV15
	Suppressor pulse TR62 collector	Pulse width = 1.5 x cal. interval	RV15
9	Fine cal. markers MSKT10	+ve pulse, 3.0V, 375ns	
	Coarse cal. markers MSKT11	+ve pulse, 3.0V, 375ns	
10	CRT cathode w/f PLB2	With 'fine' cal. markers selected and video gain to max: -ve pulse at least 25V amplitude With 'coarse' cal. markers selected and video gain to max: -ve pulse at least 25V amplitude.	

Table 2 (Contd.)

Test	Function	Check for	Control
11	CRT cathode w/f PLB2	With 'fine' and 'coarse' cal. markers selected: neither jitter nor double pulsing to occur	RV15
12	CRT grid potential PLB3	With radar brilliance control (V. U. control panel) and line brilliance control (Ops. control panel) at min: potential to vary between 0 and +25V	RV11
13	CRT grid potential PLB3	With radar brilliance control (V. U. C. P.) at max. , line brilliance control (O. C. P.) at min. and RV11 at min: at least +50V at PLB3 With line brilliance control (O. C. P.) at max. , radar brilliance control (V. U. C. P.) at min. and RV11 at min: at least +50V at PLB3	
14	CRT grid potential PLB3	Repeat Test 13 with RV11 at max: in each case obtain at least +75V at PLB3	



This waveform at TR58 base shows the calibrator staircase set to give a 5:1 divide ratio. Note that both the suppressed pulses at the beginning of the staircase and the spike at the top are counted as steps. The waveform below shows the coarse cal gating circuit at TR66 collector.

Set to $1\frac{1}{2}$ times cal. interval by means of RV15



Board Type	Calibrator Divide Ratio
MFDB	8:1
MFDC	10:1
MFDD	5:1
MFDR	4:1
MFDG	5:1
MFDH	4:1
MFDK	5:1
MFDP	5:1
MDFD	4:1

Fig. 1 Video boards: calibration staircase waveform

Chapter 5

SAMPLING GATE GENERATOR BOARDS
(NBJB and NBJA)

Introduction

1. This chapter contains test data derived from Plessey Radar Ltd Test Specifications Nos. F. C. T. 384 and 385.
2. Refer to the Bench Test Procedures for procedures with the board connected to an otherwise serviceable display, e. g. at L1.
3. Refer to A. P. 115B-0514-1 and the Master Work Sheets for procedures using the Comprehensive Display Test Set Type 10060, e. g. at G. R. S. C.
4. Refer to the station list of approved test equipment for details of specific available test equipment.

Table 1

TEST EQUIPMENT REQUIRED

Oscilloscope CT536 or equivalent.

Sine-wave oscillator - to give 10 to 25V peak-to-peak amplitude, at 1kHz.

Table 2

LIST OF TESTS: NBJB

Test	Function	Check for	Control
1	Schmidt trig. o/p MSKT2	With 25V peak-to-peak sine wave, 1kHz, applied between PLB24 and earth:	

Table 2 (Contd.)

Test	Function	Check for	Control
		-ve excursion to vary over range 475 to 575 μ s mark-space ratio unity	RV1
2	Schmidt trig. o/p	With 10V peak-to-peak sine wave, 1kHz, applied between PLB24 and earth: circuit must still trigger, amplitude of Schmidt trigger o/p to be 0 to 12V \pm 5%	
3	Delay monostable o/p w/f PLB21	With 25V peak-to-peak sine wave, 1kHz, applied between PLB24 and earth: reset time of monostable can be varied over range 170 to 250 μ s	RV2
4	Delay monostable o/p w/f PLB21	-ve edge of pulse to be co-incident with +ve peak of i/p w/f (MKST3, PLB24) pulse amplitude should be 5.0V \pm 5%	RV2

Table 3

LIST OF TESTS: NBJA

Test	Function	Check for	Control
1	+ve sampling gate MSKT2	+ve pulse, p. r. f. 1kHz, duration 150 μ s, amplitude 8V	
	-ve sampling gate MSKT3	Inverse of MSKT2 w/f	

Table 3 (Contd.)

Test	Funtion	Check for	Control
2	+ve sampling gate MSKT2	Sampling gate width 20 to 32 μ s, set to 30 μ s	RV1
3	+ve sampling gate MSKT2	Pulse amplitude +2.0V to -4.5V \pm 5%	
4	-ve sampling gate MSKT3	Pulse amplitude +2.0V to -4.5V \pm 5%	

Chapter 6

SCALING AMPLIFIER BOARDS
(NUE series)

Introduction

1. This chapter contains test data derived from Plessey Radar Limited Test Specifications Nos. F. C. T. 382, 383, 517 and 419/0152/2/002.
2. Refer to the Bench Test Procedures for procedures with the board connected to an otherwise serviceable display, e. g. at L1.
3. Refer to A. P. 115B-0514-1 and the Master Work Sheets for procedures using the Comprehensive Display Test Set Type 10060, e. g. at G. R. S. C.
4. Refer to the station list of approved test equipment for details of specific available test equipment.

Table 1

TEST EQUIPMENT REQUIRED

Test equipment	Type
Display Test Set (or working display) and Oscilloscope or Digital Voltmeter (and 1kohm series resistor)	10060 CT536 (or equivalent) CT470A (or equivalent)

Table 2

LIST OF TESTS

Note: When measuring with the digital voltmeter,
always insert a 1kohm resistor in series.

Test	Function	Switches at 'Test'	Check for	Control
1	Output volts MSKT3	SA, SB	0V \pm 100mV	RV1
2 NOT NUED	Output volts MSKT3	SA	Variation from -7V to -5V obtainable; set to -6.0V.	RV3
3 NUED ONLY	Output volts MSKT3	SA	With -3V applied between PLD4 and earth: Variation greater than \pm 0.4V obtainable; set to -3.0V.	RV3
4 NUEA ONLY	Output volts MSKT3		With +50V applied between PLD4 and earth: Variation \pm 300mV obtainable; set to 0V.	RV2
5 NUEZ, NUEC, NUEE	Output volts MSKT3		With +6.0V applied between PLD4 and earth: +6.0V \pm 100mV	RV2
6 NUED ONLY	Output volts MSKT3		With +6.0V applied between PLD4 and earth: Variation greater than \pm 0.4V obtainable; set to 0V \pm 100mV.	RV2
7 NUED ONLY	Output volts MSKT3		With -6.0V applied between PLD4 and earth: -6.0V \pm 10%.	

Table 3

BOARD VARIANT INPUT AND OUTPUT VOLTAGES

Variant	Input volts	Output volts
NUEZ	0 to +6.0	-6.0 to +6.0
NUEA	0 to +50	-6.0 to 0
NUEC	0 to +6.0	-6.0 to +6.0
NUED	-6.0 to +6.0	-6.0 to 0
NUEE	0 to +6.0	-6.0 to +6.0

Chapter 7

P.W. BOARDS NQP SERIES

Introduction

1. This chapter contains test data obtained from Plessey Radar Ltd. Test Specification No. F.C.T.419/01/01623 (for board NQPA) and from Test Specification No. 419/SD/01843 (for board NQPB).
2. Refer to the Bench Test Procedures for procedures with the board connected to an otherwise serviceable display, e.g. at L1.
3. Refer to A.P.115B-0514-1 and the Master Work Sheets for procedures using the Comprehensive Display Test Set Type 10060, e.g. at G.R.S.C.
4. Refer to the station list of approved test equipment for details of specific available test equipment.

TABLE 1

TEST EQUIPMENT REQUIRED

Comprehensive Display Test Set 10060

or

Working display

Oscilloscope CT536 or equivalent

TABLE 2

LIST OF TESTS FOR P.W. BOARD NQPA

TEST	FUNCTION	CHECK FOR	CONTROL
1	Integrated amp. ML1 o/p Test point MSKT3	RV1 fully counter-clockwise: not less than +8V RV1 fully clockwise: not less than -8V Set RV1 for best zero o/p (instability is possible due to nature of circuit)	RV1
2	+ve turn round gate Terminal 20	W/f amplitude excursions not less than +5V to -5V	
3	-ve turn round gate Terminal 16	W/f amplitude excursion not less than +5V to -5V	

TABLE 3

LIST OF TESTS FOR P.W. BOARD NQPB

TEST	FUNCTION	CHECK FOR	CONTROL
1	Integrated amp. ML1 o/p Test point MKST3	RV1 fully counter-clockwise: not less than +8V RV1 fully clockwise: not less than -8V Set RV1 for best zero o/p (instability is possible due to nature of circuit)	RV1
2	TR2 o/p Terminal 20	W/f amplitude excursion not less than +11.5V and not greater than +0.5V	

TABLE 3 (Contd.)

TEST		CONTROL
3	Integrated amp. ML2 o/p Test point MSKT4	RV2 fully counter-clockwise: not less than +8V RV2 fully clockwise: not less than -8V Set RV2 for best zero o/p (instability is possible due to nature of circuit)
4	TR1 o/p Terminal 24	W/f amplitude excursion not less than +11.5V and not greater than +0.5V

Chapter 8

P. W. BOARD NUJ SERIES

Introduction

1. This chapter contains test data obtained from Plessey Radar Ltd. Test Specification No. 419/SD/01673.
2. For procedures at G. R. S. C. refer to the Master Work Sheets.
3. Refer to the station list of approved test equipment for details of specific available test equipment.

TABLE 1

TEST EQUIPMENT REQUIRED

Oscilloscope CT536 or equivalent
Digital Voltmeter DM2020 or equivalent

TABLE 2

LIST OF TESTS FOR P. W. BOARDS NUJ SERIES

TEST	FUNCTION	CHECK FOR	CONTROL
1	Amplifier o/p voltage excursion MSKT3	Put SA to 'TEST' and measure with DVM With RV1 fully counter-clockwise: output not to exceed offset by more than -100mV With RV1 fully clockwise: output not to exceed offset by more than +100mV	RV1

TABLE 2 (Contd.)

TEST	FUNCTION	CHECK FOR	CONTROL
2	Adjusting amp. for specific offset MSKT3	Put SA to 'TEST' and measure with DVM Set RV1 for required offset (see TABLE 3)	RV1
3	Amplifier gain MSKT2 MSKT3	Apply a d.c. input voltage of 2V <u>+5mV</u> to terminal 4, measuring with DVM With DVM, measure o/p voltage at MSKT3 With RV2 fully counter-clockwise: note o/p voltage and calculate gain from $\text{Gain} = \frac{\text{Volts out} - \text{Offset}}{\text{Volts in}}$ With RV2 fully clockwise: note o/p voltage and calculate gain as above Ensure calculated gains are within limits specified in TABLE 3 and set RV2 to mid-travel	RV2

TABLE 3

CIRCUIT PARAMETERS

VARIANT TYPE	OFFSET	GAIN		RANGE OF RV1 ABOUT OFFSET
		MIN	MAX	
NUJA	-6V <u>+5mV</u>	0.53	0.64	<u>+100mV</u>
NUJB	0V <u>+5mV</u>	0.80	1.15	<u>+100mV</u>
NUJC	0V <u>+5mV</u>	0.52	0.53	<u>+100mV</u>
NUJD	0V <u>+5mV</u>	Must achieve gain of 0.794 i.e. $\frac{5}{6.3}$		<u>+100mV</u>

Chapter 9

CATEGORY SELECTION BOARDS
(MJS SERIES)

LIST OF CONTENTS

	Para.
Introduction	1

LIST OF TABLES

	Table
Test equipment required	1
Test data	2

INTRODUCTION

1. This chapter contains test data derived from Plessey Radar Test Specification No. FCT402.
2. Refer to the Bench Test Procedures for procedures with the board connected to an otherwise serviceable display, e. g. at L1.
3. Refer to A. P.115K-1210-1 and the Master Work Sheets for procedures using the Comprehensive Display Test Set Type 10060, e. g. G. R. S. C.
4. Refer to the station list of approved test equipment for details of specific available test equipment.

TABLE 1

Test equipment required

The following test equipment, or its equivalent, will be required in order to carry out the tests.

-
- Comprehensive Display Test Set 10060
 - Avometer Model 8
 - Tektronix Oscilloscope Type 531A with plug-in units Type H and Type CA
 - Power supplies: +6V, -6V, +12V, -12V stabilised

TABLE 1 (continued)

$2 \times 10\text{kohm}$ resistors CJ20
 P.R.F. source
 Pulse Generator Type 5002C
 Three separate pulses a, b and c successively delayed
 $100\mu\text{s}$ (see Fig.1)

TABLE 2

Test data

Test	Function	Check for	Control
1		<p>Connect a 10kohm load from F/14 to earth (0V H. T.) and from E/15 to earth.</p>	<p>Connect power supplies to the MJSB unit as follows:</p> <p>+6V to pin E/1 -6V to pin E/24 +12V to pin E/7 -12V to pin E/18 Common to pins E/3 and E/13.</p> <p>Switch SB to RUN Switch SA to TEST</p>
	Mainscan/fastscan logic circuit		
2			<p>See Fig.1 for waveform diagrams for the following inputs and outputs.</p> <p>Connect pulses:-</p> <p>(a) to F/20 (M/S end) (c) to E/22 (M/S end)</p> <p>Connect +6V to E/17 (Track marker bit).</p>

TABLE 2 (continued)

Test	Function	Check for	Control
3	Mainscan switch waveform at F/10 (MSKT14))	Measure amplitude of waveform (Fig.1d) (use oscilloscope triggered from waveform Fig.1a).	
4	Character switch waveform at F/9 (MSKT6)	Measure amplitude of waveform (Fig.1e) (use oscilloscope triggered from waveform Fig.1a).	
5	Symbol switch waveform at F/3 and F/12 (MSKT9).	Measure voltage level. (Use oscilloscope triggered from waveform Fig.1a).	
6		Remove +6V from E/17 and connect E/17 to 0V.	
	Character switch waveform at F/9 (MSKT6).	Check that amplitude of step level (Fig.1e) is greater than +5V (Use oscilloscope triggered from waveform Fig.1a).	
7	Symbol switch waveform at F/3 and F/12.	Measure amplitude of waveform (Fig.1f) (Use oscilloscope triggered from waveform Fig.1a).	
Symbol generator			
8		Maintain constant amplitude of sine and cosine waveforms throughout	RV3
9	Symbol waveform sine at F/15 (MSKT16)	Check that oscillation extends for correct duration (Fig.1g) (Use oscilloscope triggered from waveform Fig.1g).	

TABLE 2 (continued)

Test	Function	Check for	Control
10	Symbol waveform cosine at F/14 (MSKT15).	Check that oscillation extends for correct duration (Fig.1h). (Use oscilloscope triggered from waveform Fig.1g).	
11	Sine and cosine waveforms.	Check variation of peak-to-peak amplitude between 1.5V and 3.3V.	
12	Sine and cosine waveforms.	Measured frequency to be 40kHz \pm 5%.	
13	Sine and cosine waveforms.	Check that waveforms are switched off.	Switch SB to TEST.
Brilliance gate logic circuit			
14			Remove pulse Fig.1c from E/22. Connect pulse Fig.1b to F/23.
	Brilliance gate waveform.	Measure amplitude of waveform (Fig.1j). (Use oscilloscope triggered from waveform Fig.1a).	
15	Brilliance gate waveform.	Rise time must be greater than 150ns.	
16	Brilliance gate waveform.	Fall time to equal 400ns. (Use oscilloscope triggered from waveform Fig.1b).	
17	Brilliance gate waveform.	(Fit a double-beam Type CA unit in oscilloscope). Delay between 50% of leading edge of M/S start pulse, Fig.1b, and 10% down trailing edge of brilliance gate waveform Fig.1j, must be less than 150ns.	

TABLE 2 (continued)

Test	Function	Check for	Control
18			Fit Type H unit in oscilloscope trigger waveform Fig. 1a. Connect pulses Fig. 1b to E/21. Connect pulses Fig. 1c to E/22. Connect +6V to E/23 (supervisory bit).
19.	Brilliance gate waveform at MSKT2.	Measure amplitude of waveform (Fig. 1j).	
	Brilliance gate waveform.	A d. c. level greater than +5V (black condition).	Remove +6V from E/23 and connect E/23.
	Tube protection circuits		Remove pulse Fig. 1c from E/22. Connect pulse Fig. 1b to F/23. Connect F/16 to 0V. Switch SA to RUN.
20	MSKT11	Check that signal switches from greater than +4V (black) to greater than -5.5V (bright-up). Connect F/17 to 0V. Remove 0V from F/16.	+6V applied to F/17, F/19 and F/22 in turn.
21	MSKT11	Check that signal switches from greater than +4V to greater than -5.5V. Remove +6V from F/16.	Apply +6V to F/16.
22	MSKT7	Check that signal switches from greater than +4V to greater than -5.5V.	+6V applied to F/2, F/4, F/6 and F/8 in turn.

TABLE 2 (continued)

Test	Function	Check for	Control
			Connect +6V to F/19 and F/6.
23	Brilliance gate waveform at MSKT2	Waveform Fig. 1j.	
24	Brilliance gate waveform at MSKT2	D.C. level shall be greater than +5V.	Remove +6V from F/19.
			Reconnect +6V to F/19.
25	Brilliance gate waveform at MSKT2	D.C. level shall be greater than +5V.	Remove +6V from F/6.
26	Brilliance gate waveform at MSKT2.	Waveform Fig. 1j.	Switch SA to TEST.
27	Transistor TR4 base.	Adjust RV1 so that peak of integrated waveform Fig. 1i lies between 0V and +0.2V.	Connect waveform Fig. 1k to F/2, F/4, F/6 and F/8 in turn.
28	MSKT7	Check that d. c. level is greater than +4V.	Connect waveform Fig. 1k to F/2, F/4, F/6 and F/8 in turn.

Chapter 10

VIDEO BOARDS (MFK SERIES)

LIST OF CONTENTS

	Para.
Introduction	1

LIST OF TABLES

	Table
Test equipment required	1
Test data	2

INTRODUCTION

1. This chapter contains test data derived from Plessey Radar Test Specification No. FCT174.
2. Refer to the Bench Test Procedures for procedures with the board connected to an otherwise serviceable display, e. g. at L1.
3. Refer to A. P.115K-1210-1 and the Master Work Sheets for procedures using the Comprehensive Display Test Set Type 10060, e. g. G. R. S. C.
4. Refer to the station list of approved test equipment for details of specific available test equipment.

TABLE 1

Test equipment

Tektronix Oscilloscope with an L-Type plug-in unit and 10:1 probe
Avometer Model 8
Video Test Set Type I. T. E. D. 799
Nagard Pulse Generator Type 5002/C.

TABLE 2

Test data

Test	Function	Check for	Control
1			Switch BOARD SELECTOR to L/S.
2			Switch SUPPLIES to OFF.
3			Switch 100V to OFF.
4			Switch SCAN SELECT to '1' (M/S).
5			Switch BRILL GATE to '1' (ON).
6			Switch OCT. BLK to '1' (SA SCAN).
7			Switch VIDEO 1 SELECT to ON.
8			Switch VIDEO 2-6 SELECT switches to OFF.
9			Turn VIDEO 1 CON- TROL VOLTS poten- tiometers fully clockwise.
10			Turn VIDEO 2-6 CONTROL VOLTS potentiometers fully anti-clockwise.
11			Turn OCT. BLK. CONTROL VOLTS potentiometer fully anti-clockwise.
12			On MFKZ: turn RV7 fully anti-clockwise and all other potentio- meters to MID-TRAVEL.
13			Make link A-C, i. e. connect PLA/6 to C14.

TABLE 2 (continued)

Test	Function	Check for	Control
14			Temporarily mount 470ohms CJ20 in R158 and R168 positions (Harwin pins on the bases of TR18 and TR20 respectively).
15			Install the MFKZ in the video board test set.
16			Switch SUPPLIES to ON.
17	TR1 and TR2 collector voltages.	Use Avometer and adjust for 0V.	RV1
18			Set VIDEO 1 SELECT switch to OFF. Turn VIDEO 1 CONTROL VOLTS potentiometer fully anti-clockwise. Set VIDEO 2 SELECT switch to ON. Turn VIDEO 2 CONTROL VOLTS potentiometer fully clockwise.
	TR1 and TR2 collector voltages.	Use Avometer and adjust for 0V.	RV2
19			Set VIDEO 2 SELECT switch to OFF. Turn VIDEO 2 CONTROL VOLTS potentiometer fully anti-clockwise. Set VIDEO 3 SELECT switch to ON. Turn VIDEO 3 CONTROL VOLTS potentiometer fully clockwise.
	TR1 and TR2 collector voltages.	Use Avometer and adjust for 0V.	RV3

TABLE 2 (continue)

Test	Function	Check for	Control
20			Set VIDEO 3 SELECT switch to OFF. Turn VIDEO 3 CONTROL VOLTS potentiometer fully anti-clockwise. Set VIDEO 4 SELECT switch to ON. Turn VIDEO 4 CONTROL VOLTS potentiometer fully clockwise.
	TR1 and TR2 collector voltages.	Use Avometer and adjust for 0V.	RV4.
21			Set VIDEO 4 SELECT switch to OFF. Turn VIDEO 4 CONTROL VOLTS potentiometer fully anti-clockwise.
	TR24 base voltage.	Using the oscilloscope to monitor TR24 base, adjust voltage to +2.5V.	RV5
22	C.R.T. cathode socket.	Adjust for TR29 to just conduct in cathode. Level should be not less than +95V.	RV5.
23		Connect a positive 0.2V 100 μ s pulse to VIDEO 1 input socket.	Set VIDEO 1 SELECT switch to ON. Turn VIDEO 1 CONTROL VOLTS potentiometer fully clockwise.
24	C.R.T. cathode socket.	Connect the oscilloscope probe earth to the cathode socket solder tag.	
25	C.R.T. cathode socket.	Check that a negative pulse of amplitude greater than 10V is present.	

TABLE 2 (continued)

Test	Function	Check for	Control
26	C. R. T. cathode socket.	Check that the pulse can be reduced by approximately 50% of this total amplitude by adjustment.	RV7 (it may be necessary to re-adjust RV5 for the cathode level of +95V.
27			Set RV7 fully anti-clockwise. Re-adjust RV5 for +95V.
		Check that the pulse at the cathode disappears and the d. c. level rises to +100V.	Set BRILL. GATE switch to '2' (OFF).
28			Set BRILL GATE switch to '1' (ON). Set the OCT. BLK. potentiometer to the engraved dot (-4V at PLA/21 with the OCT. BLK. switch in position '1' (XA SCAN).
	TR48 collector.	Monitor with the Avometer and adjust the voltage to just switch to +4V.	
29	C. R. T. cathode.	Check that the pulse at the cathode disappears and that the d. c. level rises to +100V.	
30	C. R. T. cathode.	Check that in each position the pulse disappears and the d. c. level rises to +100V.	Set the OCT. BLK. switch to position '2' (XB SCAN), '3' (YA SCAN) and '4' (YB SCAN) in turn.

TABLE 2 (continued)

Test	Function	Check for	Control
		(It may be necessary to slightly re-adjust RV10).	
31	C.R. T. cathode.	Check that the pulse may be smoothly reduced in amplitude.	<p>Set the OCT. BLK. switch to position '1' (XA SCAN).</p> <p>Set the OCT. BLK. potentiometer fully anti-clockwise.</p> <p>Turn the VIDEO LIMIT potentiometer slowly clockwise.</p> <p>Set the VIDEO LIMIT potentiometer fully anti-clockwise.</p>
32	C.R. T. cathode.	Pulse should be greater than 10V amplitude.	<p>Set VIDEO 2-1 SELECT switches to ON.</p> <p>Turn VIDEO 2-4 CONTROL VOLTS potentiometer fully clockwise.</p>
33		Overshoot should be less than 10% of pulse amplitude.	
34	C.R. T. cathode pulse.	Check that droop is less than 10%.	<p>Increase input pulse width to 5ms.</p> <p>Reduce input pulse width to 100μs.</p>
35	C.R. T. cathode pulse.	Check that the pulse is reduced substantially to zero.	Rotate VIDEO 1 CONTROL VOLTS potentiometer anti-clockwise.
36			Set VIDEO 1 CONTROL VOLTS potentiometer fully clockwise.

TABLE 2 (continued)

Test	Function	Check for	Control
			Switch VIDEO 1 SELECT to ON.
	C.R.T. cathode pulse.	Check that the pulse is more than 3dB down compared with its amplitude at 100 μ s.	Reduce the width of the input pulse to 200ns.
38		Repeat tests 32 to 37 on video channel 2.	Connect the positive 0.2V 100 μ s pulse to VIDEO 2 input socket.
39		Repeat tests 32 to 37 on video channel 3	Connect the positive 0.2V 100 μ s pulse to VIDEO 3 input socket.
40		Repeat tests 32 to 37 on video channel 4.	Connect the positive 0.2V 100 μ s pulse to VIDEO 4 input socket.
41			Switch VIDEO 1-4 SELECT switches to OFF.
			Turn VIDEO 1-4 CONTROL VOLTS potentiometers fully anti-clockwise.
			Set VIDEO 5 SELECT switch to ON and turn VIDEO 5 CONTROL VOLTS potentiometer fully clockwise.
			Connect a positive 1V 2 μ s pulse to CAL. 1 input socket.
	Monitor at the c. r. t. cathode.	Check that a negative pulse of amplitude greater than 10V is present.	

TABLE 2 (continued)

Test	Function	Check for	Control
42	C. R. T. cathode.	Check that the output pulse is not more than 3dB down compared with its amplitude at $2\mu s$.	Reduce the input pulse width to 200ns.
43	C. R. T. cathode.	Check that the output pulse reduces substantially to zero.	Rotate the VIDEO 5 CONTROL VOLTS potentiometer anti-clockwise.
44			Set VIDEO 5 CONTROL VOLTS potentiometer fully clockwise.
	C. R. T. cathode.	Check that the output pulse is reduced substantially to zero.	Set the VIDEO 5 SELECT switch to the OFF position.
45		Repeat tests 41 to 44 on video channel 6.	Connect the positive 1V $2\mu s$ pulse to the CAL. 2 input socket.
46			Set the SCAN SELECTION switch to position '2' (CHARACTER SWITCH).
	Monitor at the C. R. T. cathode socket.	Cathode level to be at +95V.	Adjust RV9.
47			Set RV6 fully clockwise. Connect a positive 1V $10\mu s$ pulse to the CHARACTER input socket.
48	Monitor at the C. R. T. cathode.	Check that a negative pulse of amplitude greater than 20V is present.	
49	Output pulse.	Reduces substantially to zero.	Rotate RV6 anti-clockwise.

TABLE 2 (continued)

Test	Function	Check for	Control
50	Output pulse.	Overshoot should not be greater than 10% of the pulse amplitude.	Set RV6 fully clockwise.
51	Output pulse.	Check for 10% overshoot at 50% gain.	Adjust C11.
52	Output pulse.	Check that the output pulse is not reduced in amplitude. If the gain at 200ns is less than 10 μ s reduce the gain to 2/3 maximum and repeat.	Reduce the input pulse to 200ns.
53	Monitor at the C. R. T. cathode socket.	Cathode level to be at +95V	Set the SCAN SELECTOR switch to position '3' (VECTOR SLOW SCAN). Adjust RV8.
FUNCTIONAL TESTS - BRILLIANCE			
54	C. R. T. grid	Monitor at the c. r. t. grid socket with the oscilloscope. If necessary adjust C20 to stop any oscillations. Check that the voltage can be varied from 0V to at least +25V.	Set the SCAN SELECTOR switch to position '1' (M/S). Set BRILL-CONTROL VOLTS potentiometers 1 to 4 fully anti-clockwise. C20 RV11.

TABLE 2 (continued)

Test	Function	Check for	Control
55			Set RV11 for the grid potential to be just above 0V.
	C.R. T. grid.	Check that the grid potential rises to +50V or greater.	Turn the BRILL CONTROL VOLTS potentiometer (M/S) fully clockwise.
56	C.R. T. grid.	Grid potential to be +75V.	Adjust RV11.
57	C.R. T. grid.	Grid potential to be +50V.	Re- adjust RV11.
58	C.R. T. grid.	Check that the grid potential is reduced by approximately 20V to approximately +30V.	Set the BRILL GATE switch to position '2' (OFF).
59			Set the BRILL GATE switch to position '1' (ON).
	C.R. T. grid.	Check that the grid potential is reduced by approximately 20V to approximately +30V.	Set the OCT. BLK. CONTROL VOLTS potentiometer to the engraved dot (-4V at PLA/21 with the OCT. BLK. switch in position '1' (XA SCAN). Set the OCT. BLK. CONTROL VOLTS potentiometer fully anti-clockwise. Set the BRILL 1 CONTROL VOLTS potentiometer (M/S) fully anti-clockwise.
60			Set the SCAN SELECTOR switch to position '2' (CHARACTER SWITCH).

TABLE 2 (continued)

Test	Function	Check for	Control
	C. R. T. grid.	Check that the grid potential rises to +50V or greater.	Turn the BRILL 2 CONTROL VOLTS potentiometer (CHARACTER) fully clockwise.
61	C. R. T. grid.	Check that the grid potential is reduced to substantially 0V.	Turn the BRILL 2 CONTROL VOLTS potentiometer (CHARACTER) fully anti-clockwise.
62		Repeat tests 60 and 61 for the BRILL 3 CONTROL VOLTS potentiometer.	Set the SCAN SELECTOR switch to position '3' (VECTOR SLOW SCAN).
		Repeat tests 60 and 61 for the BRILL 4 CONTROL VOLTS potentiometer.	Set the SCAN SELECTOR switch to position '4' (SLOW SCAN).
			Remove the 470ohm resistors R158 and R168 from TR18 and TR20 bases.

Chapter 11

DEFLECTION BOARDS (MRM SERIES)

LIST OF CONTENTS

	Para.
Introduction	1

LIST OF TABLES

	Table
Test equipment required	1
Test data	2

INTRODUCTION

1. This chapter contains test data derived from Plessey Radar Test Specification No. FCT174.
2. Refer to Bench Test Procedures for test procedure with the board connected to an otherwise serviceable display, e. g. at L1.
3. Refer to A. P.115K-1210-1 and Master Work Sheets for procedure using the Display Test Set Type 10060, e. g. at G. R. S. C.
4. Refer to the station list of approved test equipment for details of specific available test equipment.

TABLE 1

Test equipment

Avometer Model 8
Tektronix Oscilloscope, Type 531A and plug-in unit Type H
Marconi Video Oscillator Type TF885A/1
Two 10k potentiometers
One 2.7k resistor Type NJ65

TABLE 2

Test data

Test	Function	Check for	Control
1			<p>Set RV5 and RV6 fully clockwise.</p> <p>Switch SA and SC to TEST.</p> <p>Switch SB to RUN.</p> <p>Switch on supplies and adjust:</p> <p>RV1 for 0V at TEST 10 RV2 for 0V at TEST 9 RV4 for 0V at TEST 7 RV7 for 0V at TEST 2</p>
		Connect 2.7k resistor between 0V and PLC/G/8.	Switch SC to RUN.
2	Monitor TEST 7	Connect +12V to PLD/H/16. Check output at TEST 7 is 0V +100mV.	
3	TEST 7	Repeat test 2 for PLD/H/15	
4	TEST	Repeat test 2 for PLD/H/14 Note: A slight difference may be found in the MAX. and MIN. values at TEST 7	Adjust RV4 for the difference to be a Minimum.
5		Connect a 10k potentiometer between +12V and -12V. Connect the wiper to PLD/H/22.	
	Monitor TEST 7	Note that this output is approximately -1.2V.	Set 10k potentiometer to +12V at PLD/H/22.
6		Check that output at TEST 7 remains the same.	Apply +12V to PLD/H/14, 15 and 16, in turn.
7	Monitor TEST 7	Repeat tests 6 and 7 with -12V at PLD/H/22. The output at TEST 7 should be approximately +1.2V.	

TABLE 2 (continued)

Test	Function	Check for	Control
8	Monitor TEST 2	Repeat tests 5, 6 and 7.	
9	Monitor TEST 7	Adjust 10k potentiometer for 0V at TEST 7 with +12V removed from PLD/H/14, 15 and 16.	
10		Connect a 10k potentiometer between +6V and -6V. Connect the wiper to PLC/G/8.	
	Monitor TEST 7	Adjust for +4V.	Set 10k.
11	TEST 7	Check that output is +2V.	Connect +12V to PLD/H/16.
12	TEST 7	Check that output is +1V.	Remove +12V from PLD/H/16 and connect to PLD/H/15.
13	TEST 7	Check that output is +0.5V.	Remove +12V from PLD/H/15 and connect to PLD/H/14.
14			Remove +12V from PLD/H/14. Remove potentiometer from PLC/G/8. Connect PLC/G/8 to EARTH via 2.7k resistor. Connect +12V to PLD/H/14. Connect +6V to PLC/G/2. Connect -6V to PLC/G/3. Switch SA to RUN.

TABLE 2 (continued)

Test	Function	Check for	Control
	TEST 7	Check that output is greater than +4.2V.	Adjust RV3 to Max.
15	TEST 7	Check that output is less than +3.4V.	Adjust RV3 for Min.
16	TEST 7	+4V.	Adjust RV3.
17	TEST 7	Check that output limits at approximately +7V.	Switch SB to TEST.
18	TEST 7	Output to be +4.5V.	Adjust RV6.
19			Switch SB to RUN. Connect +6V to PLC/G/3.
	TEST 7	Check output is -4V.	Connect -6V to PLC/G/2.
20	TEST 7	Repeat tests 17 and 18 adjusting RV5 for -4.5V.	RV5
21			Switch SB to RUN. Connect PLC/G/2 and PLC/G/3 together.
	TEST 7	Check that output is not greater than 0.1V peak-to-peak for all frequencies up to 50kHz.	Apply a 2V peak-to-peak 50Hz sine wave to PLC/G/2 and earth screen.
22			Remove +12V from PLD/H/14. Remove link between 2 and 3. Switch SB to RUN.
	TEST 2	Check output is 8V peak-to-peak.	Apply a 3V peak-to-peak 10kHz sine wave to PLC/G/3.
23	TEST 2	Check output amplitude does not fall below 5.66V at 300kHz.	Increase I/P frequency. Remove all connections.

TABLE 2 (continued)

Test	Function	Check for	Control
24	Output at PLC/G/23.	Check that the output is 3V peak-to-peak and 180 ^o out of phase with the input waveform.	Apply a 3V peak-to-peak 50kHz sine wave to PLC/G/6.
25	Output at PLC/G/22.	Check that the output is 3V peak-to-peak and in phase with the input waveform.	

SUPPLEMENTARY

INFORMATION UNITS

A. P. 115K-1205-1
Mk. 5 AUTONOMOUS PPI DISPLAY IN
FGRI. 23154 AND TGRI (AT). 26038/1 AND /2
(AR-1)

This publication is supplementary to A. P. 115K-1201-1 at AR-1 installations and is designed for gathering in the same binder.

CONTENTS

- Chapter 1. Mk. 5 Display with Radar Type AR-1
2. Operator's control panels (AR-1)
 3. Display servicing (AR-1)

INTRODUCTION

Mk. 5 display with AR-1

1. The AR-1 installation (FGRI. 23154 and TGRI(AT). 26038/1 & 2) is a surveillance radar with which up to four Mk. 5 p. p. i. displays may be associated. The AR 1 system is described in A. P. 115H-0604-1, including system aspects of the Mk. 5 displays. This publication (A. P. 115K-1205-1) is supplementary to A. P. 115K-1201-1 (Mk. 5 display - basic) and describes how the Mk. 5 display is tailored for use with the AR 1 radar.

2. Two variants of the Mk. 5 display are used with AR-1. These are:-

(1) 75 mile display Type 12852/A/A (Console, control indicator, 5840-99-953-4116).

(2) 100 mile display Type 12852/E/A (Console, control indicator, 5840-99-953-4115).

The make-up of these displays is given in Appendix 1 to this chapter.

3. Apart from differences in range and calibration markers both displays are essentially the same in function, and the outline description following relates to both displays.

Display features specific to AR-1

4. The 75 mile display has ranges of 7.5, 15, 30 and 75 nautical miles, and range calibration markers at 2 and 10 n. m. intervals. The 100 mile display has ranges of 12.5, 25, 50 and 100 n. m., and range calibration markers at 5 and 20 n. m. intervals.

5. The data presented consists of main video and background video together with range markers and one interscan line; also, when inputs are available, a video map (two channels, A or B), s. s. r. video and a c. r. d. f. line can be presented.

6. M. T. I. can be applied. For this purpose the main (or combined) video is composed, in any one p. r. f. period, of m. t. i. video out to the selected range followed by normal (uncancelled) video. Background video is unprocessed video that can be presented at a controlled intensity from zero to normal viewing level.

7. Selection of the presented data is made by controls on the Operator's Control Panel (Chap. 2).

8. Up to four autonomous displays can be used in a Radar Type AR-1 system. When multiple displays are used, synchro excitation voltage and sampling gate waveforms from one display only are employed. The control switch selecting from which particular display these waveforms are derived is the MASTER DISPLAY SELECTION switch located on the Radar Control Unit (R. C. U. 5864).

OUTLINE OF OPERATION

Introduction (Fig. 1)

9. In the text and block diagram the abbreviations MS and IS are used to denote mainscan and interscan respectively.

10. Interconnections diagrams are provided (Figs. 2 to 4).

11. For more detailed description of operation refer to A. P. 115K-1201-1, Part 1, Chap. 3.

Timing Board (MJE)

12. Various switch and gate waveforms are generated on this board. These are produced by the timing board circuits from a series of timing pulses derived from the radar trigger and (in the case of the 'interscan knock-off' pulse only) the interscan range control voltage.

13. Three timing pulses are derived. These are as follows:-

- (1) 'scan end' pulse
- (2) 'interscan start' pulse

and (3) 'interscan knock-off' pulse.

14. The 'scan end' pulse and the radar trigger are used to produce a time-base gate waveform; this waveform is fed to the deflection boards.

15. The 'interscan start' pulse produces the MS/IS switch waveform (shift), which is passed to both deflection boards, and the MS/IS switch waveform which is fed to both deflection boards and to the video board.

16. The 'scan end' pulse and 'interscan knock-off' pulse are fed to an OR gate to produce the 'calibration and brilliance end' pulse; this latter pulse,

together with the radar trigger, controls the calibration and brilliance gate generator circuit to obtain the calibration and brilliance gate waveform. In this way the calibration and brilliance gate waveform is produced from the radar trigger and 'scan end' pulse during mainscan periods, and from the radar trigger and 'interscan knock-off' pulse during interscan periods; these waveforms are fed as a single train to the video board.

17. A 400Hz aerial synchro excitation voltage is produced, along with positive and negative sampling gate waveforms. These are fed out of the display, and may be selected to provide synchro and sampling gates for the system (as described in para. 8).

Deflection boards (MRG)

18. Two identical deflection boards are fitted, one concerned with X deflection and the other with Y deflection.

19. Each board receives its associated modulated component from the aerial synchro (modulated as the sine of the aerial bearing for X deflection, and as the cosine of the aerial bearing for Y deflection) and both the positive and negative sampling gate waveforms. The output from each board is the scan control voltage for one axis of the c. r. t.

20. The aerial synchro input waveforms are fed to demodulator circuits on the deflection boards, and the demodulator circuits on each board are interconnected to form an oscillator-type demodulator (refer to A. P. 115K-1201-1, Part 1, Chap. 2 for a description of this circuit).

21. The MS scan control voltage (from the demodulator) and the IS scan control voltage (fed via an inverter from the sine/cosine potentiometer on the Operator's Control Panel) are passed to the scan switch circuit. This electronic switch is controlled by the MS/IS switch waveform and selects either the MS scan C. V. or IS scan C. V. to feed to the timebase generator. The output from the scan switch is the switched scan C. V. and this is fed to the timebase generator.

22. The timebase generator is a shifting integrator which produces a sawtooth during the MS or IS scan period. The circuit is controlled by the 'timebase gate' waveform and the sawtooth amplitude is determined by the switched scan C. V. The output is the timebase waveform, and this provides one input to the deflection combining amplifier.

23. The shift switch circuit programmes the MS and IS shift levels into their correct display periods. Zero voltage level, representing the MS shift potential, is fed into the circuit together with the IS shift control voltage (i. e. X or Y line shift from the Operator's Control Panel) which is applied to the

shift switch via an inverter. The shift switch is operated by the MS/IS switch waveform (shift) from the timing board. The output from the shift switch is applied to an input of the deflection combining amplifier.

24. The deflection combining amplifier generates a push-pull pair of complex deflection drive waveforms from a total of four inputs. These inputs comprise the timebase waveform, the shift switch circuit input, the X or Y radar shift voltage from the Operator's Control Panel and the X or Y centre shift voltage from the Viewing Unit Control Panel. The output waveform is inverted and the output waveform from the inverter is fed via the deflection coil drive amplifier to the deflection circuits.

Deflection circuits

25. The deflection circuits comprise the X and Y deflection coil drive amplifiers and the c. r. t. deflection coils.

26. The deflection coil drive amplifiers consist of four separate but identical amplifiers, two for X deflection and two for Y deflection. Each amplifier is fed with the complex deflection drive waveform from the associated deflection board, and provides the current drive for one c. r. t. deflection coil.

27. Four c. r. t. deflection coils are provided, two for X deflection and two for Y deflection, each coil being driven by one of the deflection coil drive amplifiers.

Video board (MFD)

28. The video board contains circuits concerned with video amplification brilliance control and calibration marker generation. The c. r. t. trace is blanked during appropriate periods: this includes octagonal blanking.

29. Two radar video signals are fed into the board. These are:-

- (1) background video, which is fed to the Video 1 channel, and
- (2) main video, fed to the Video 2 channel.

The gains of these video channels are controlled by the VIDEO 1 and VIDEO 2 controls on the Viewing Unit Control Panel.

30. The calibration marks generator, controlled by the 'calibration and brilliance gate' waveform from the timing board, produces coarse and fine

trains of marker pulses. Calibration marks appear at 2 n. m. and 10 n. m. intervals (75 n. m. displays) or 5 n. m. and 20 n. m. intervals (100 n. m. displays), and marker brilliance is adjusted by controls on the Viewing Unit Control Panel. Calibration marks and signal video are combined in the video mixer to produce the mixed video waveform.

31. The mixed video waveform together with a d. c. level (from the interscan level potentiometer RV8) and the MS/IS switch waveform (from the timing board) are fed to the video switch circuit. The video waveform is suppressed during interscan periods and replaced by the d. c. interscan level; the output from the video switch is inhibited when the spot sweeps outside the periphery of the c. r. t. screen

32. The output from the video switch is fed to the video gate along with the brilliance blanking waveform (para. 35) which controls the gate. The video gate output is fed to the c. r. t. cathode via a video amplifier; this is the complex video waveform. Blanking of the c. r. t. is provided in accordance with the octagonal blanking circuit output.

33. The brightness switch provides the switched brilliance control voltage. Two d. c. control voltages are taken to the electronic switch; these are the MS brilliance control voltage from the RADAR BRIL (RV9) control on the Viewing Unit Control Panel, and the IS brilliance control voltage from the LINE BRILLIANCE (RV7) control on the Operator's Control Panel. The MS/IS switch waveforms from the timing board are taken to the circuit to switch the output between two levels, one appropriate to mainscan deflection and the other to interscan deflection (this is the switched brilliance control voltage).

34. The X and Y timebase waveforms are taken to the octagonal blanking circuit, and the octagonal blanking waveform is produced from these when the voltage of the timebase waveform exceeds a certain level. This waveform alternates between two levels depending upon whether the spot is inside or outside the c. r. t. periphery.

35. The octagonal blanking waveform and the calibration and brilliance gate waveform (from the timing board) are combined in an OR gate; the combined output is the brilliance blanking waveform.

36. A preset potentiometer (RV11) provides the over-all brilliance level; this voltage is applied continuously, affecting the trace at all times.

37. The brilliance amplifier provides the complex brilliance waveform which is applied to the c. r. t. grid. This amplifier is fed with three inputs as follows:-

- (1) the over-all brilliance level (para. 33)

- (2) the switched brilliance control voltage (para. 33),
- and (3) the brilliance blanking waveform (para. 35)

Viewing unit junction unit

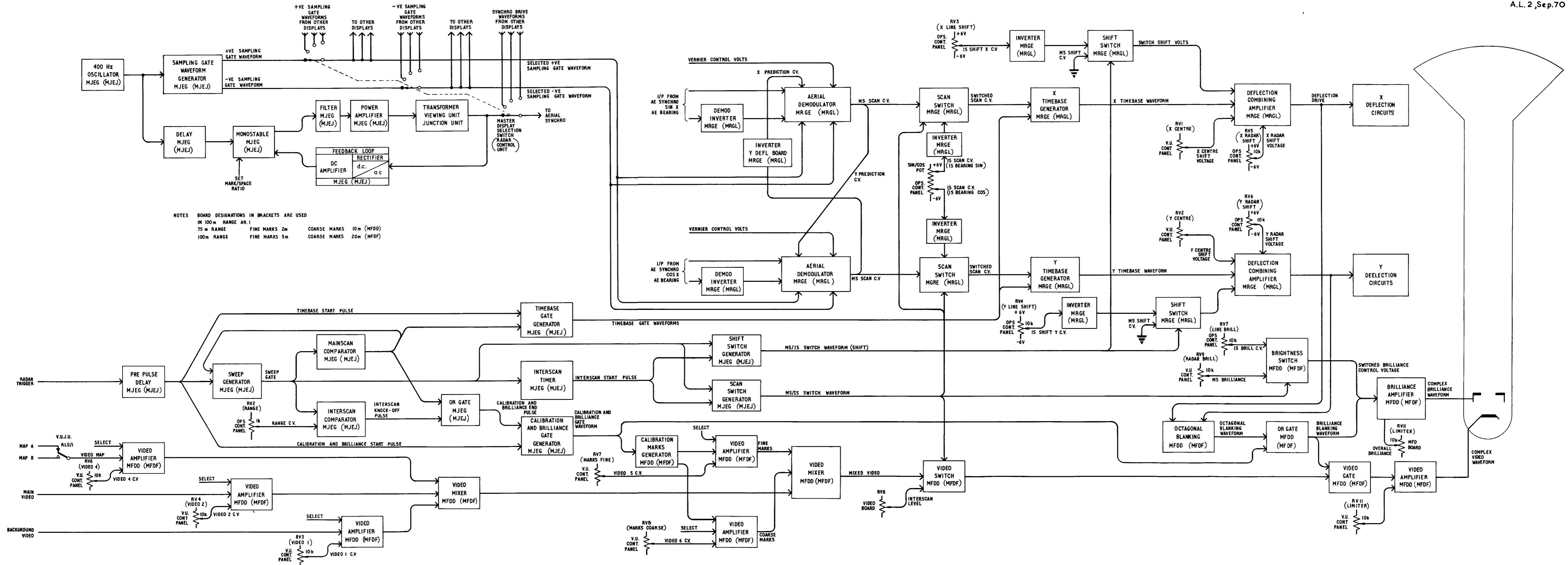
38. The circuit for the junction unit 12790/J/A used in the AR-1 application is given in A. P. 115K-1201-1, Part 2, Sect. 1, Chap. 5, App. 3.

39. Relays RLA, RLB and RLC are part of the bearing line/c. r. d. f. changeover circuits.

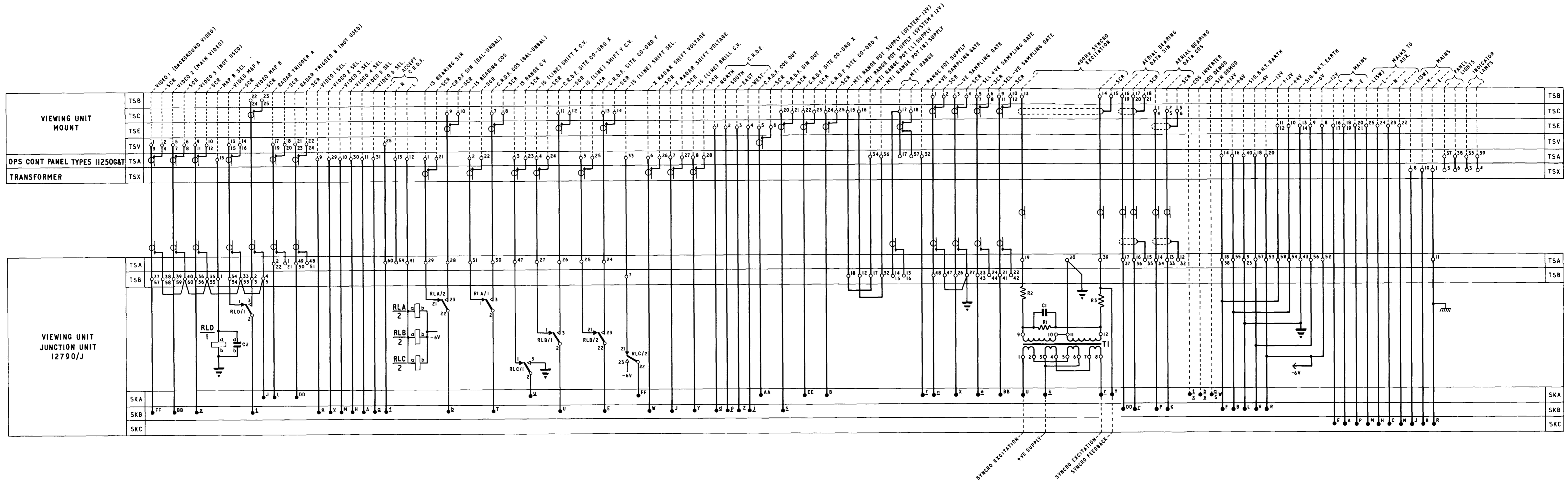
40. When c. r. d. f. is not selected (i. e. the C. R. D. F. push-button switch on the operator's control panel is in the 'off' position) relays RLA, RLB and RLC are de-energized. The outputs from the BEARING sine/cosine potentiometer on the operator's control panel are fed via relay RLA to the deflection boards (para. 21), the outputs from the X and Y LINE SHIFT potentiometers (on the operator's control panel) are fed via RLB to the deflection board (para. 23), and the range control voltage from the RANGE potentiometer is passed through RLC to the timing board (para. 12).

41. When c. r. d. f. is selected (providing, of course, that c. r. d. f. facilities are available) relays RLA, RLB and RLC are energized. The BEARING sine/cosine voltages and the X and Y LINE SHIFT voltages are replaced by control voltages obtained from outside the display, and the RANGE control voltage is replaced by 0V level.

42. Relay RLD is part of the video map selector circuit. When neither video map is selected RLD is energized since a potential of -12V is applied via the normally closed contacts of switch SL (MAP A) and diode MR1 on the operator's control panel; the video 4 channel (through which the video map signals are routed) is inhibited by a -12V level applied via normally closed contacts of switches SL and SH (MAP B). When a map A is selected RLD is de-energized, applying map A video signal to the video 4 channel, and the inhibiting level is removed. When map B is selected RLD is energized via the normally closed contact of switch SL (MAP A), applying map B video to the video channel, the channel inhibiting level being removed since switch SH (MAP B) normally closed contact is open.



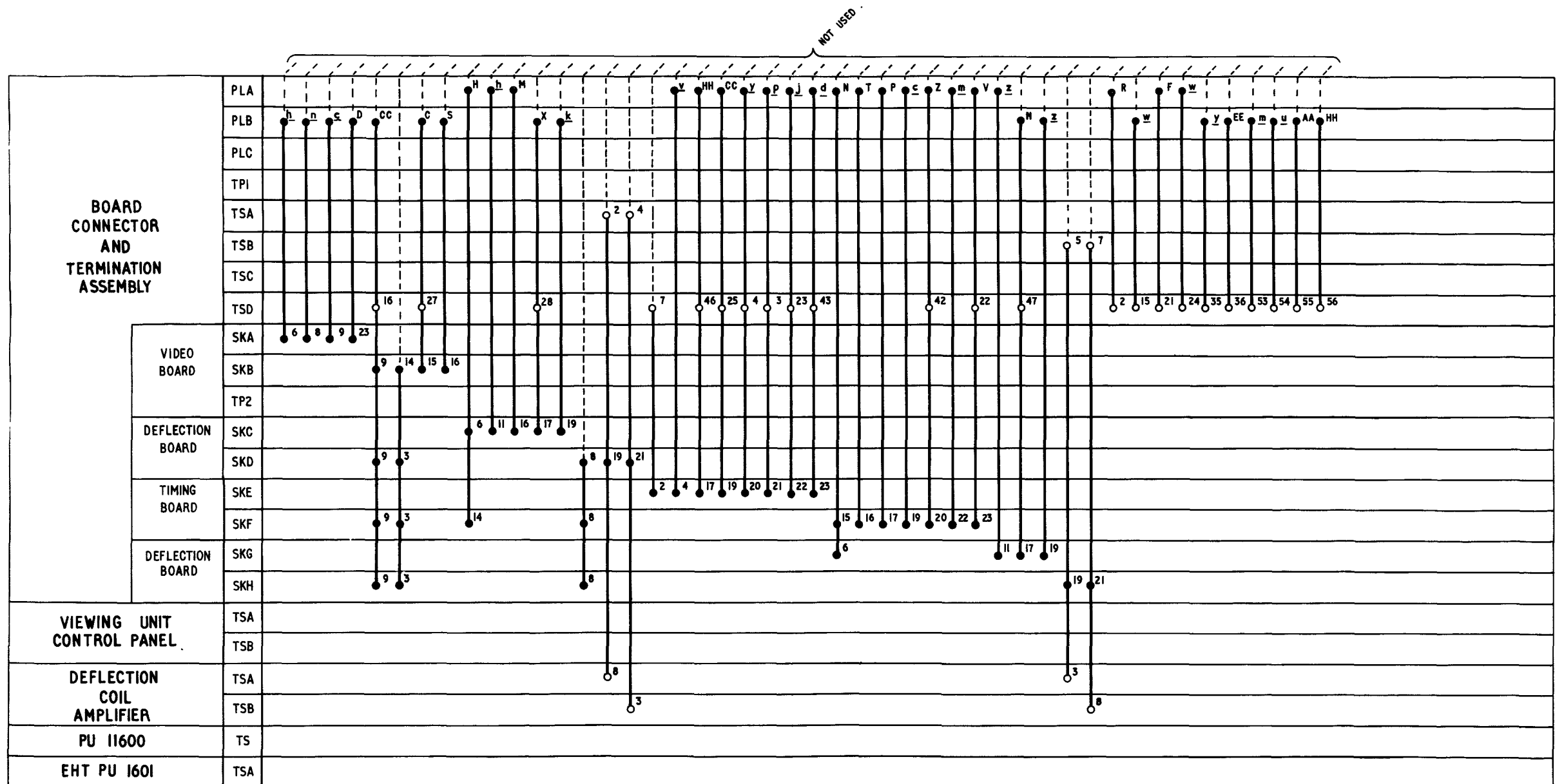
Radar type A.R.I. displays : block diagram



B/DDI/12852/A 155.2
B/DDI/12790/J 155.9
A.L.2, Aug.70

Radar type A.R.I. displays:interconnections (Part A)

Fig.2



Appendix 1

AR-1 75mi. DISPLAY: CONSOLE MAKE-UP

Item No.	Manufacturer's description	Part No.	NATO Designation	NATO Stock No.	Mod. Strike off	Publication References														
						Technical Information					In-situ servicing					Workshop servicing				
						A. P. 115K-	Pt.	S.	Ch.	P.	A. P.	Pt.	S.	Ch.	P.	A. P. 115K-	Pt.	S.	Ch.	P.
1	Console assy.	12852/A/A	Console, control indicator	5840-99-953-4116	NA	1205-1			1		(115K-1201-1 (4950 Int. Vol. (5, 2nd Edit- (ion Append- (ices A4, A5, (B3	3	1	3& 5)))))	1201-1	3	1	5	
2	Mk. 5 Autonomous Display	12600/N/A	NA	NA	1	1205-1			1											
3	Basic Viewing unit	12550/A	Cabinet, electrical equipment	948-8877	NA	1201-1	1		3											
4	Operator's control panel	11250T/A	Panel control	953-5059	0	1205-1			2											
5	Viewing unit mount	12800/A	NA	NA	0															
6	Viewing unit junction unit	12790/J/A	Interconnecting box	222-8099		1201-1	2	1	5											
7	Power unit	11600/A	Power supply 11600	948-9058	6	1201-1	2	1	1							1201-1	3	2	1	*
8	EHT power unit	11601/A	Power supply 11601	948-8878	4	1201-1	2	1	2							1201-1	3	2	2	*
9	Deflection coil drive amplifier	12502/A	Amplifier, direct current	948-8879	1	1201-1	2	1	3							1201-1	3	2	3	*
10	Deflection coil assembly	11702A	Coil assy., CRT deflection and focus	948-9055	2	1201-1	2	1	7											
11	Viewing unit control panel	11210/R/A	Panel control	955-3594	2	1201-1	2	1	4											
12	Cathode ray tube	CV 10949	Valve electronic CV 10949	037-5772																
		or CV 10948	Valve electronic CV 10948	037-5771																
13	Heat exchanger unit	11950/A	Cooler, liquid	948-9043	1	1201-1	2	1	6							1201-1	3	1	7	*
14	Pump assembly	12551/C	Pump, rotary, power driven	948-9059	0	1201-1	2	1	6											
15	Timing board MJEG	12137/A	Panel, electronic circuit	953-5056	4	1201-1	2	2	1							1201-1	3	2	1	*
16	Deflection board MRGE (2 off)	12012/A	Panel, electronic circuit	953-5055	3	1201-1	2	2	2							1201-1	3	2	2	*
17	Video board MFDD	12139/A	Panel, electronic circuit	953-5057	5	1201-1	2	2	4							1201-1	3	2	4	*

Appendix 2

AR-1 100mi. DISPLAY: CONSOLE MAKE-UP

Item No.	Manufacturer's description	Part No.	NATO Designation	NATO Stock No.	MOD Strike-off	Publication references														
						Technical Information					In-situ servicing					Workshop servicing				
						A. P. 115K-	Pt.	S.	Ch.	P.	A. P.	Pt.	S.	Ch.	P.	A. P. 115K-	Pt.	S.	Ch.	P.
1	Console assy.	12852/E/A	Console control indicator	5840-99-953-4115	NA	1205-1			1		(115K-1201-1 (4950, Int. (Vol. 5, 2nd edition (Appendices (A4, A5, B3	3	1	3&5		1201-1	3	1	5	
2	Mk. 5 Autonomous Display	12600/R/A	NA	NA	1	1205-1			1											
3	Basic Viewing unit	12550/A	Cabinet, electrical equipment	948-8877	NA	1201-1	1		3											
4	Operator's control panel	11250/G/A	Panel, control	955-3592	0	1205-1			2											
5	Viewing unit mount	12800/A	NA	NA	0															
6	Viewing unit junction unit	12790/J/A	Interconnecting box	222-8099		1201-1	2	1	5											
7	Power unit	11600/A	Power Supply 11600	948-9058	6	1201-1	2	1	1							1201-1	3	2	1	*
8	EHT power unit	11601/A	Power Supply 11601	948-8878	4	1201-1	2	1	2							1201-1	3	2	2	*
9	Deflection coil drive amp.	12502/A	Amplifier direct current	948-8879	1	1201-1	2	1	3							1201-1	3	2	3	*
10	Deflection coil assy.	11702/A	Coil assy. , CRT deflection and focus	948-9055	2	1201-1	2	1	7											
11	Viewing unit control panel	11210/T/A	Panel control	955-3596	1	1201-1	2	1	4											
12	Cathode ray tube	CV 10949	Valve electronic CV 10949	5960-99-037-5772	NA															
	or	CV 10948	Valve electronic CV 10948	5960-99-037-5771	NA															
13	Heat exchanger unit	11950/A	Cooler liquid	948-9043	1	1201-1	2	1	6							1201-1	3	1	7	*
14	Pump assembly	12551/C	Pump, rotary, power driven	948-9059	0	1201-1	2	1	6											
15	Timing board MJEJ	12198/A	Panel electronic circuit	955-3597	4	1201-1	2	2	1							1201-1	3	2	1	*
16	Deflection board MRGL (2 off)	12213/A	Panel electronic circuit	955-3595	3	1201-1	2	2	2							1201-1	3	2	2	*
17	Video board MFDF	12214/A	Panel electronic circuit	955-3593	5	1201-1	2	2	4							1201-1	3	2	4	*

*See also GRSC Master Work Sheets

Chapter 2

OPERATOR'S CONTROL PANELS (AR-1)

LIST OF CONTENTS

	Para.
GENERAL DESCRIPTION	1
CIRCUIT DESCRIPTION	
Bearing control	3
Range control	4
Line shift controls	5
Radar shift controls	7
Line brilliance controls	9
MTI range	11
Video selection	12
Video map selection	17
Range marker selection	20
CRDF	22
Panel lighting	23
Push-button illumination	24
Socket SKTA	25

LIST OF ILLUSTRATIONS

	Fig.
Operator's control panel Types 11250T and 11250G: component location	1
Operator's control panel Types 11250T and 11250G: circuit	2

GENERAL DESCRIPTION

1. The operator's control panel carries the majority of the controls required by the operator during normal operation. The panel is fitted to the viewing unit mount and is connected to the viewing unit through the viewing unit junction unit, and to external equipment through the mount terminal assembly. The controls on the

panel consist of internally illuminated push-button switches (bright when operative and dim when inoperative), and potentiometers.

2. Two types of panel are fitted in AR-1 installations; these differ only in the engraving on the 'fine' and 'coarse' range mark selectors. For convenience, the description that follows relates to a single panel type but will be found to relate to either. The panels fitted are:-

(1) 75n.m. display; Panel Type 11250/T, 5840-99-953-5059
2 and 10 mile marks.

(2) 100n.m. display; Panel Type 11250/G, 5840-99-955-3592
5 to 20 mile marks.

CIRCUIT DESCRIPTION

Bearing control

3. This control is a sine/cosine potentiometer (RV1) connected between the $\pm 6V$ supplies. Voltage outputs proportional to the sine and cosine of the BEARING control setting are passed to the X and Y deflection boards via TSA1 and TSA2 to control the angular position of the interscan marker line when it is used as a range and bearing line. Bearing settings can be read from an illuminated numerical display adjacent to the BEARING control.

Range control

4. This potentiometer (RV2) is connected between earth and the range potentiometer supply obtained from the timing board (MJE). The wiper potential is fed out of the panel via TSA3 to the interscan comparator circuit on the timing board. The RANGE control setting determines the length of the interscan marker line when it is used as a range and bearing line, and the range can be read from an illuminated numerical display adjacent to the control.

Line shift controls

5. The X LINE SHIFT potentiometer (RV3), Y LINE SHIFT potentiometer (RV4) and LINE SHIFT push-on/push-off switch (SB) are the line shift controls which move the interscan marker line with respect to the rest of the p.p.i. picture. In the 'off' position of the switch a potential of +6V is fed out of the panel via TSA33 to the shift inhibitor on the timing board (MJEC); this inhibitor is 'off' (i.e. not operative) and, under these conditions, the line shift control voltage outputs from the line shift potentiometers are inhibited by the shift switch circuits on the deflection boards so that the origin of the interscan marker line coincides with the origin of the mainscan.

In the 'on' position -6V is passed to the shift inhibitor and the X and Y LINE SHIFT potentiometers are operative. However, although c. r. d. f. facilities are not normally used in Radar Type AR-1 applications, operation of the CRDF push-button switch disconnects the outputs of the line shift potentiometers.

6. The X LINE SHIFT potentiometer slider potential is fed via TSA4 to the shift switch on the X deflection board (MRG). Similarly the output from the Y LINE SHIFT potentiometer is passed via TSA5 to the shift switch on the Y deflection board.

Radar shift controls

7. These are the RADAR SHIFT push-on/push-off switch (SC), and the two potentiometers X RADAR SHIFT (RV5) and Y RADAR SHIFT (RV6). The controls enable the complete picture to be off-centred in any direction by an amount equal to the maximum range of the system whilst maintaining accurate registration between the mainscan and the interscan marker line.

8. In the 'on' position of the RADAR SHIFT switch the relay RLA is energized. The X and Y radar shift voltages (derived from the X and Y RADAR SHIFT potentiometers) are fed to the deflection boards via contacts RLA1 and RLA2 of relay RLA and terminals TSA6 and TSA7. When the RADAR SHIFT switch is 'off' the radar shift voltages are replaced by earth level and the picture is centred (i. e. the centre of the c. r. t. coincides with the geographical location of the radar aerial).

Line brilliance controls

9. The push-on/push-off switch LINE ON/OFF (SA) and associated potentiometer LINE BRILLIANCE (RV7) enable the interscan marker line to be removed from the c. r. t. when not required, and its brilliance can be adjusted independently of the rest of the picture.

10. When the LINE ON/OFF switch is 'on' the IS line brilliance C. V. from the potentiometer slider is fed out of the panel via TSA8 to the brightness switch on the video board. When the switch is 'off' the slider potential is replaced by earth level which inhibits the interscan marker line.

MTI range

11. The MTI RANGE potentiometer (RV9) determines within limits the range over which the radar m. t. i. circuits operate. The potentiometer supply is fed into the display from m. t. i. circuits external to the display and the m. t. i. range voltage (from the potentiometer slider) is passed out of the display to the m. t. i. circuits.

Video selection

12. Push-on/push-off switches are provided to control the inhibitions on the video channels.

13. The Video 1 channel carries background video, and is controlled by the BACKGROUND switch (SE). When the switch is 'off' the channel is inhibited by a potential of -12V which leaves the panel via TSA9. In the 'on' position of the switch the -12V inhibiting voltage is removed.

14. The main radar video is carried on the Video 2 channel which is controlled by the MAIN VIDEO switch (SF); the operation of this switch is similar to that of switch SE (para. 13).

15. The Video 3 channel is controlled by the SSR push-button switch, the operation being similar to that of switch SE (para. 13). However, SSR is not used in the Radar Type AR-1 application.

16. The Video 4 channel is concerned with video map selection, and the operation of the associated controls is described in paras. 17 to 19.

Video map selection

17. The Video 4 channel is allocated to the video map presentation. Either Video Map A or B can be selected by the two push-on/push-off switches MAP A (SL) or MAP B (SH). When both switches are 'off' the video 4 channel is inhibited by a potential of -12V fed via both switches and TSA30 to the video amplifier.

18. When MAP A is selected the inhibiting voltage is removed from the Video 4 amplifier channel and the -12V level is removed from relay RLD in the viewing unit junction unit. Relay RLD is therefore de-energized, selecting video map A input to the video channel.

19. When MAP B is selected the inhibiting voltage is removed from the video amplifier and the -12V inhibiting level is used to energize relay RLD via the normally closed contacts of RLA and diode MR1. When RLD is energized then video map A is fed to the video amplifier.

Range marker selection

20. The fine and coarse range marks are selected by the push-on/push-off switches SJ and SK. These are engraved 2 N.M. MARKS and 10 N.M. MARKS on the 75-mile display and 5 N.M. MARKS and 20 N.M. MARKS on the 100-mile display.

21. When the fine marks are selected the -12V inhibiting level applied to the Video 5 amplifier channel via switch SJ and TSA11 terminals is disconnected. Similarly, selection of coarse marks removes the -12V level from the Video 6 channel.

CRDF

22. CRDF is not normally used in the Radar Type AR-1 application. However, a push-button switch CRDF (SD) is provided on the operator's control panel, together with associated relays RLA, RLB and RLC located in the viewing unit junction unit, but without external links in the relay solenoid circuits, so that the relays are permanently inhibited.

Panel lighting

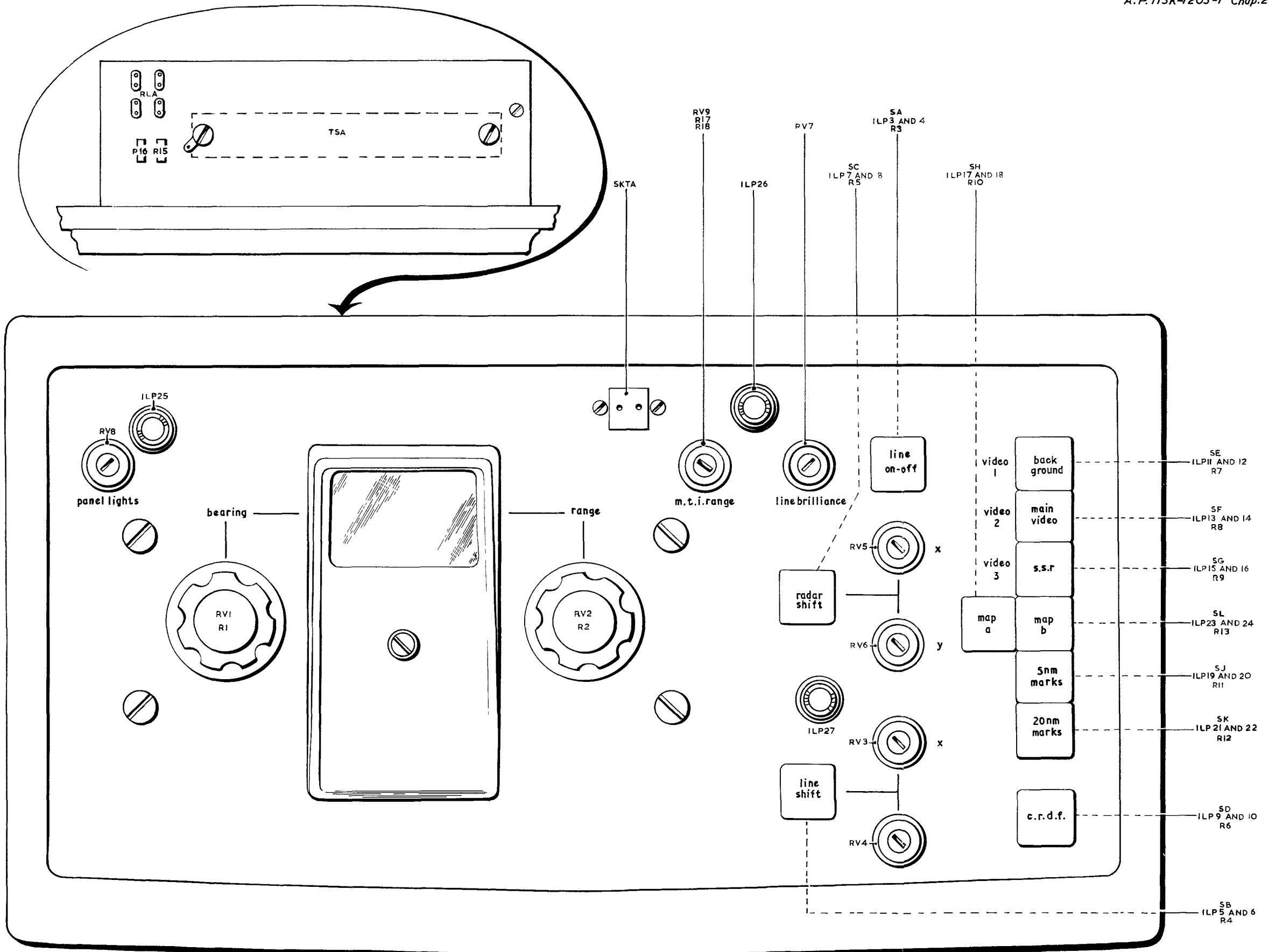
23. The three lamps ILP25, ILP26 and ILP27 are used for edge-lighting the panel. These lamps, together with the lamps used for illuminating the push-button switches, are fed from a 6.3V a.c. supply derived from one secondary of the mains transformer located in the viewing unit mount; the supply enters the control panel on terminals TSA37 and TSA38. The PANEL LIGHTS potentiometer control (RV8) provides control of illumination for the panel lights and the push-buttons.

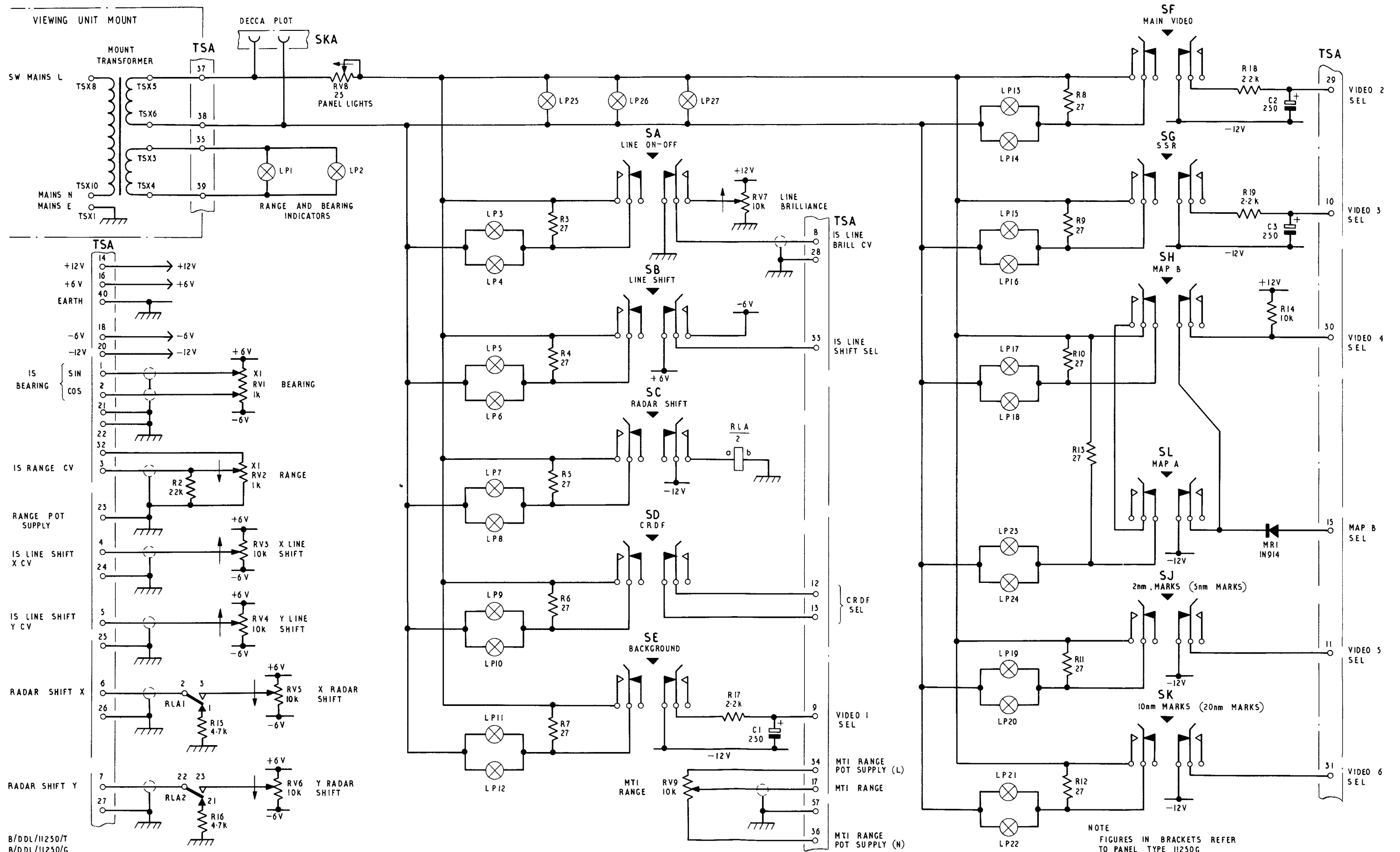
Push-button illumination

24. Two lamps integral with each push-button indicate the state of the associated switch. The lamp supply is derived from the 6.3V a.c. supply via the PANEL LIGHTS control as described in para. 23. The circuit of each lamp pair is identical, and the circuit of switch SA only is described. In the 'off' position of switch SA the lamps ILP3 and ILP4 are lit at reduced brilliance due to the series resistor R3. In the 'on' position the contacts of SA short out the resistor R3 and the lamps are illuminated at normal brilliance.

Socket SKTA

25. Socket SKTA on the front of the panel provides an a.c. outlet of 6.3V for a track plotter (not used in AR-1).





B/DD1/11250/T
B/DD1/11250/G

A.L.3 Jan.71

Operators control panel types 11250T and 11250G : circuit

NOTE
FIGURES IN BRACKETS REFER
TO PANEL TYPE 11250G

Fig. 2

Chapter 3

DISPLAY SERVICING (AR-1)

1. Servicing information specific to the AR-1 installation is not provided in this chapter; refer to A. P. 115K-1201-1, Part 3, Sect. 1, Chap. 3 and 5 for information relating to display accuracy tests and display setting-up. A list of test equipment necessary to undertake these tests and setting-up procedures is given in Table 1. Maintenance at first line should not entail more than is outlined in the chapters mentioned above.
2. Unit and P. W. board servicing procedures given in A. P. 115K-1201-1, Part 3, Sect. 2 and 3 are intended for use at third line.
3. Removal and replacement procedures for PU11600, EHT PU11601 and the deflection coil drive amplifiers are given in A. P. 115K-1201-1, Part 3, Sect. 2, Chap. 1, 2 and 3.

Table 1

LIST OF TEST EQUIPMENT

Description	Service/MNF Ref. No.
Multimeter CT498A	5QP/1057049
Voltmeter Electrostatic	5QP/16190
Oscilloscope CT536	10S/9522040
Digital Voltmeter	