HF RECEIVER UK/FRR 628
(RACAL Type RA.1772/DA76871B)

GENERAL AND TECHNICAL INFORMATION
AND
REPAIR AND RECONDITIONING INSTRUCTIONS

BY COMMAND OF THE DEFENCE COUNCIL

Ministry of Defence

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MODIFICATION RECORD

This publication is technically up-to-date in respect of the modifications listed below.

Mod. No.	Brief description
A7530	Replacement of resistors
A7454	Introduction of alternative 2nd-mixer board.
A8130	Introduction of alternative AFC board.
A8529	Introduction of alternative IF/AF boards.
A8778	Fitting additional resistors on PM370 board.
A8855	To prevent incorrect 'out of lock' indication.
A9006	Fitting a ferrite bead on PM336 board.
A9007	To change diodes D13, D14 on PM674 board.
A9597	Improved earthing.
A9662	To prevent amplifier oscillation on PM335 board.
A9722	To reduce spurious signals on PM336 board.
B0076	Change resistor value on PM364 board.
B0077	To reposition the mains fuse.
-	Introduction of alternative optical shaft encoder.
B0529	Addition of 1 kilohm resistors to transistors 1TR1, 1TR2 and 1TR3.
TC0024	Replacement of unobtainable capacitors.
►TC0015	Replacement of 0.4 to 1.6 kHz filter with a 1.1 to 2.9 kHz filter. ◄

LEADING PARTICULARS

RECEIVER HF RACAL TYPE RA.1772

FUNCTION	General purpose, ground station, fully synthesized h.f. communications receiver.
FREQUENCY RANGE	15 kHz to 30 MHz
MODES OF RECEPTION	A1, A2, A2H, A2J, A3, A3A, A3B, A3H, A3J.
TUNING	Switched selection of 1 MHz steps (0 to 29) and a continuously tuneable synthesizer in 10 Hz or 100 Hz steps over each 1 MHz band. Electronic digital frequency display to 10 Hz.
OVERSPILL	20 kHz at either end of each 1 MHz band. Overspill indication is provided.
TUNING ACCURACY	Plus or minus 5 Hz relative to the frequency of the wanted signal.
FREQUENCY STABILITY (Receiver 5820-99-635 -9352)	(1) Temperature: $\pm$ 6 parts in 10^{10} per ^{o}C. (2) Long term: $\pm$ 1.5 parts in 10^{8} over a 30 day period or $\pm$ 5 parts in 10^{10} per day.
ANTENNA INPUT	50 ohms to 75 ohms nominal. Coaxial BNC connector.
SENSITIVITY	(1) C.W. AND S.S.B. (A1,A2H,A3A,A3H,A3J) In a 3 kHz bandwidth the signal-to-noise ratio is better than: 500 kHz - 30 MHz, 15 dB with 1 µV e.m.f. input 50 kHz - 500 kHz, 15 dB with 3 µV e.m.f. input 15 kHz - 50 kHz, 15 dB with 10 µV e.m.f. input (2) D.S.B. (A2,A3). 8 kHz bandwidth In a 3 kHz bandwidth the signal-to-noise ratio is better than: 500 kHz - 30 MHz, 10 dB with 1.5 µV e.m.f. input, 70% modulated. 50 kHz - 500 kHz, 10 dB with 10 µV e.m.f. input, 30% modulated. 15 kHz - 50 kHz, 10 dB with 15 µV e.m.f. input, 70% modulated.
I.F. SELECTIVITY	(1) S.S.B. (A3A, A3J) Passband at -6 dB: 250 Hz to 3000 Hz Passband at -60 dB: -650 and +4100 Hz (2) I.S.B. (A3B) Passband at -6 dB: 250 Hz to 3000 Hz Passband at -60 dB: -400 and +4100 Hz

I.F. SELECTIVITY (cont.)

(3) C.W./M.C.W./A.M. (A1,A2,A3,A2H,A3H)

In addition to the S.S.B./I.S.B. filters, a symmetrical i.f. filter of 8 kHz bandwidth is fitted for a.m. reception. Also, 0.4 kHz and 1.2 kHz i.f. filters, offset by 1 kHz towards the upper sideband, are fitted for c.w. reception.

CROSS MODULATION

With a wanted signal greater than 300 µV e.m.f., in a 3 kHz bandwidth, an unwanted signal, 30% modulated, removed not less than 20 kHz, will be greater than 300 mV e.m.f., to produce an output 20 dB below the output produced by the wanted signal.

RECIPROCAL MIXING

With a wanted signal of less than 100 µV e.m.f., in a 3 kHz bandwidth, an unwanted signal more than 20 kHz removed will be greater than 70 dB above the wanted signal level to give a noise level 20 dB below the output produced by the wanted signal.

BLOCKING

With a wanted signal of 1 mV e.m.f. an unwanted signal more than 20 kHz removed must be greater than 500 mV to reduce the output by 3 dB.

INTERMODULATION PRODUCTS

(1) Out of band

With two 30 mV e.m.f. signals separated and removed from the wanted signal by not less than 20 kHz, the third-order intermodulation products are not less than -85 dB below either of the interfering signals and typically better than -90 dB.

(2) In band

Two in band signals of 30 mV e.m.f. will produce third-order intermodulation products of not greater than -40 dB.

SPURIOUS RESPONSES

(1) External

External signals, 20 kHz removed from the wanted signal, must be at least 80 dB above the level of the wanted signal to produce an equivalent output.

(2) Internal

Not greater than 3 dB above the noise level measured in a 3 kHz bandwidth.

A.G.C.

(1) Range

An increase in output of 100 dB above 2 µV e.m.f. will produce an output change of less than 6 dB.

(2) Switched selection of AGC OFF, SHORT and LONG time constants.

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A.F.C. (A3A, A3B, A3H)

(1) A front-panel switch selects pilot carrier, full carrier or a.f.c. off.

(2) Capture range : ± 50 Hz.

(3) Follow range: ± 500 Hz or beyond.

(4) Stability: Over a range of ± 10°C relative to 25°C, the incoming signal is held to within ± 2 Hz of its tuned frequency setting.

I.F. OUTPUT (A.G.C. ON)

100 uV e.m.f. (nominal) at 1.4 MHz into 50 ohms.

B.F.O.

+ 4 kHz to -2 kHz relative to 1.4 MHz.

AUDIO CHARACTERISTICS

(1) Output levels

(i) Line outputs, 1 mW nominal into 600 ohms, balanced, adjustable by preset level control on the front panel to +6 dBm.

(ii) Phone outputs, balanced, 10 mW nominal into 600 ohms.

(iii) 50 mW into an internal loudspeaker which is capable of being switched in or out of operation.

(iv) Connection for an external loudspeaker, 1W into 8 ohms.

(2) A.F. response

(i) Line outputs: within 1 dB from 100 Hz to 6000 Hz relative to the level of a standard 1000 Hz tone.

(ii) The overall a.f. response will be dependent upon the i.f. bandwidth selected.

(3) A.F. distortion

(i) Line outputs: not greater than 2% at the specified output of 1 mW nominal.

(ii) Loudspeaker outputs: not greater than 5% at 50 mW into the internal loudspeaker and 1W output into the external loudspeaker.

(iii) Phone outputs: not greater than 5% at the specified output of 10 mW nominal.

CROSSTALK (A3B)

With a wanted signal at a level of 1 mV and the a.f. output set to 1 mW, the crosstalk from an equal signal in the opposite sideband, at greater than

CROSSTALK (A3B) (cont)	400 Hz from the carrier, is not greater than -50 dB relative to 1 mW.
METERING	A meter is provided on the front panel to indicate r.f. level, a.f. level to line, and suitable performance or supply test levels.
POWER SUPPLY	100 - 125V or 200 - 250V, ± 10%, 45 - 65 Hz.
POWER CONSUMPTION	Approximately 60 VA (approx).
DIMENSIONS	For rack mounting: Height: 178 mm Width: 483 mm Depth: 410 mm
WEIGHT	Approximately 22 kg.

CONTENTS

Preliminaries

Title page
Amendment record sheet
Lethal warning
Modification record
Leading particulars
Contents (this list)

Chapters

1-1 General description
1-2 Functional description
1-3 Operating instructions
2-1 Detailed circuit description
2-2 Dismantling and re-assembly
2-3 List of test equipment
2-4 Receiver performance checks
2-5 Receiver alignment procedures
2-6 Fault diagnosis

Chapter 1-1

GENERAL DESCRIPTION

CONTENTS

	Para.
Introduction	1
Mechanical description	5
N.A.T.O. nomenclature	9

TABLES

No.		Page
1	Receiver sub-assemblies	3

ILLUSTRATIONS

Fig.		Page
1	Receiver : general view	2
2	Chassis layout : top view	5
3	Chassis layout : underside view	6

INTRODUCTION

1. The receiver radio 5820-99-635-9352 (Racal Type RA.1772) (fig. 1) is a fully synthesized, solid state, communications receiver providing reception facilities for l.s.b./u.s.b. (A3A,A3H,A3J), i.s.b. (A3B), a.m. (A3) and telegraphy (A1,A2H,A2J) with two i.f. filters offset by 1 kHz.

2. The frequency range of the receiver is 15 kHz to 30 MHz, and the built-in synthesizer is phase-locked to the output of a 5 MHz frequency standard. The MHz selection is in switched 1 MHz increments (MHz switch with associated dial); a single-knob tuning control tunes the synthesizer continuously over each 1 MHz band, with switched selection of FAST or SLOW tuning rates, or LOCK. In the LOCK position, the synthesizer does not respond to movement of the kHz tuning control. At the ends of each 1 MHz band, the tuning provides a 20 kHz overspill to eliminate the need for reverse tuning of the kHz control Overspill is indicated by an illuminated lamp behind the appropriate MHz dial setting, above or below the setting initially selected. An electronic digital display indicates the kHz setting to 10 Hz. Some receivers will be fitted with a battery module MS540 which ensures that the tuning state is maintained following a momentary mains failure or mains-born transient.

3. A built-in meter may be switched to indicate r.f. and a.f. signal levels as well as supply-voltage levels. A slow-motion BFO control is provided for c.w. operation.

4. A switched monitor loudspeaker is provided and two front panel mounted jack sockets permit headphone monitoring of the output selected by the MODE switch. When the right-hand phone jack is in use the internal loudspeaker is muted.

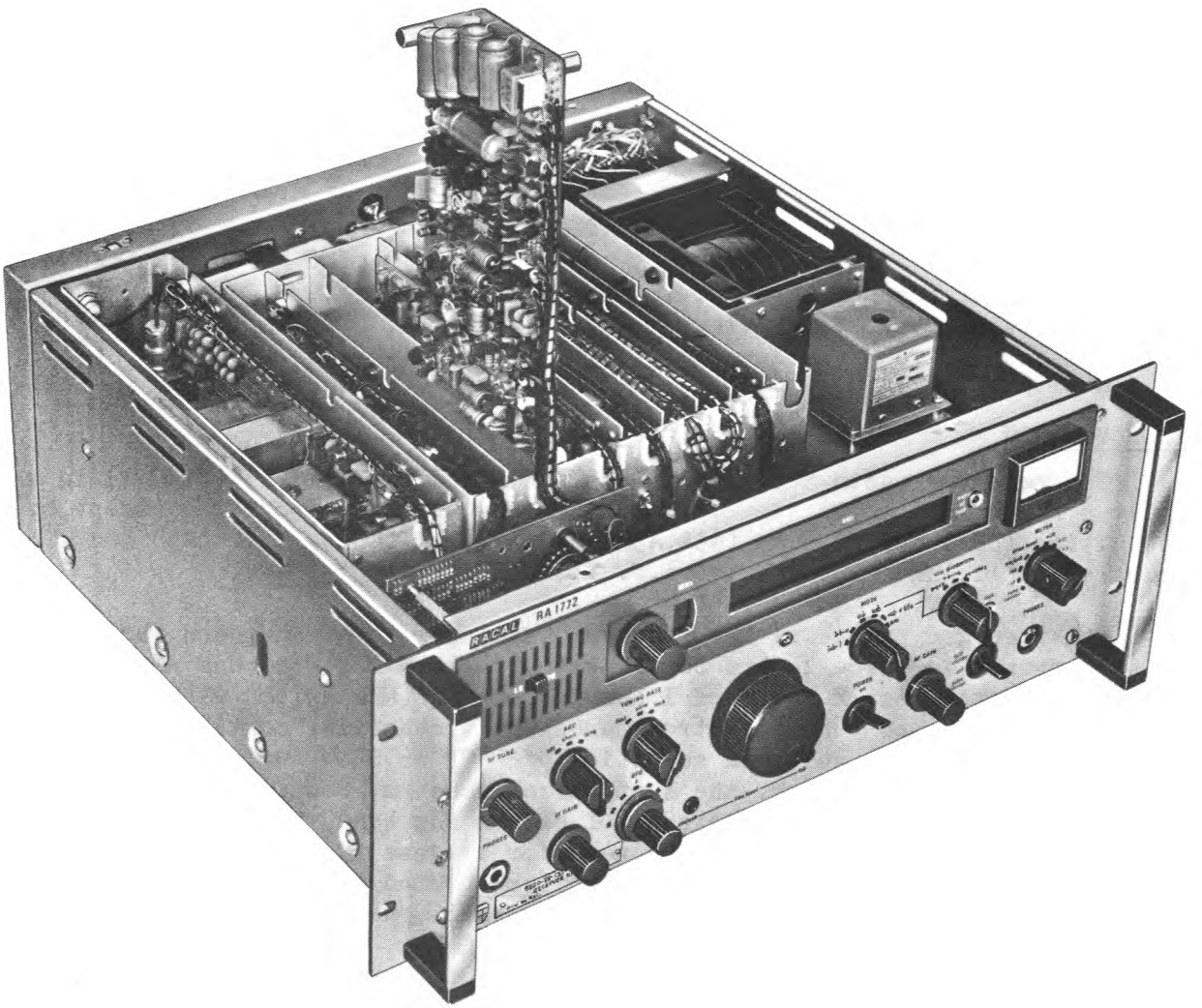


Fig.1 Receiver: general view

MECHANICAL DESCRIPTION

5 A rigid, die-cast, full-width chassis provides the basis for the main frame of the receiver. Mounted within compartments on the underside of this chassis are the first and second mixer boards together with three boards of the frequency generation system (hf loop board, transfer loop board and the 34 MHz generator board). The underside view of the receiver chassis is given in fig.3.

6 Mounted on the top of the cast chassis is an aluminium box structure which houses seven printed circuit boards, each individually screened (fig.2). These printed circuit boards may be hinged out and then fixed in position for servicing. Also mounted on the top of the chassis is the frequency standard module and the power supply transformer. The power supply regulator board is mounted on the inside of the rear panel and adjacent to this board are mounted the power supply smoothing capacitors. The power supply regulator output transistors are mounted on a heat-sink attached to the rear panel of the receiver. A further power supply board, the af and memory regulator board, is mounted adjacent to the power supply transformer. The display board (including the digital display) is mounted on the inside of the front panel, the logic board is attached to the front panel MHz switch, and the meter switching board is attached to the front panel METER switch.

7 A 12-volt battery module is mounted on the rear panel of the receiver. The purpose of this module is to preserve the frequency determining information applied to the synthesizer should a brief interruption of the main power supply occur.

8 The receiver may be safely operated (for servicing) with both the front and rear panel assemblies lowered in order to gain access to preset controls and other components. A general view of the receiver, with a printed circuit board in the raised position, is given in fig.1 whilst fig.2 shows the chassis layout as viewed from the top of the receiver.

NATO NOMENCLATURE

9 Table 1 gives the NATO title and number, and the makers title, which is employed throughout this publication, for the printed circuit boards and sub-assemblies of the receiver.

TABLE 1 RECEIVER SUB-ASSEMBLIES

NATO catalogue number	Maker's title
5820-99-638-5654	RF board PM582
5820-99-633-2065	First mixer board PM335
5820-99-633-2066	Second mixer board PM336
5820-99-638-5655	Filter board PS367
5820-99-643-0064	Power regulator board PM370
5820-99-633-2092	AF and memory regulator board PS427/1
5820-99-633-2068	Meter switching board PS419

TABLE 1 (cont.)

NATO catalogue number	Maker's title
5820-99-633-2063	Main if/af board PM364/1
5820-99-633-2062	ISB if/af board PM364/3
► 5820-99-638-2568	Low frequency (lf) loop board PM588
5820-99-638-2567	Upper loop board PM589 ◄
5820-99-633-8779	Transfer loop board PS338
5820-99-633-8780	High frequency (hf) loop board PS337
5820-99-638-0903	34 MHz generator board PM339
► 5820-99-638-5649	Logic board PS365 ◄
5820-99-633-2093	Display board PM371
5820-99-631-4080	Shaft encoder (optical) assembly
6625-99-634-4422	Frequency standard (oscillator) assembly
5820-99-631-8602	12 V battery module MS540
► 5820-99-638-5648	AFC board PM369
5820-99-649-2085	AFC board PM664 (provides improved performance) ◄

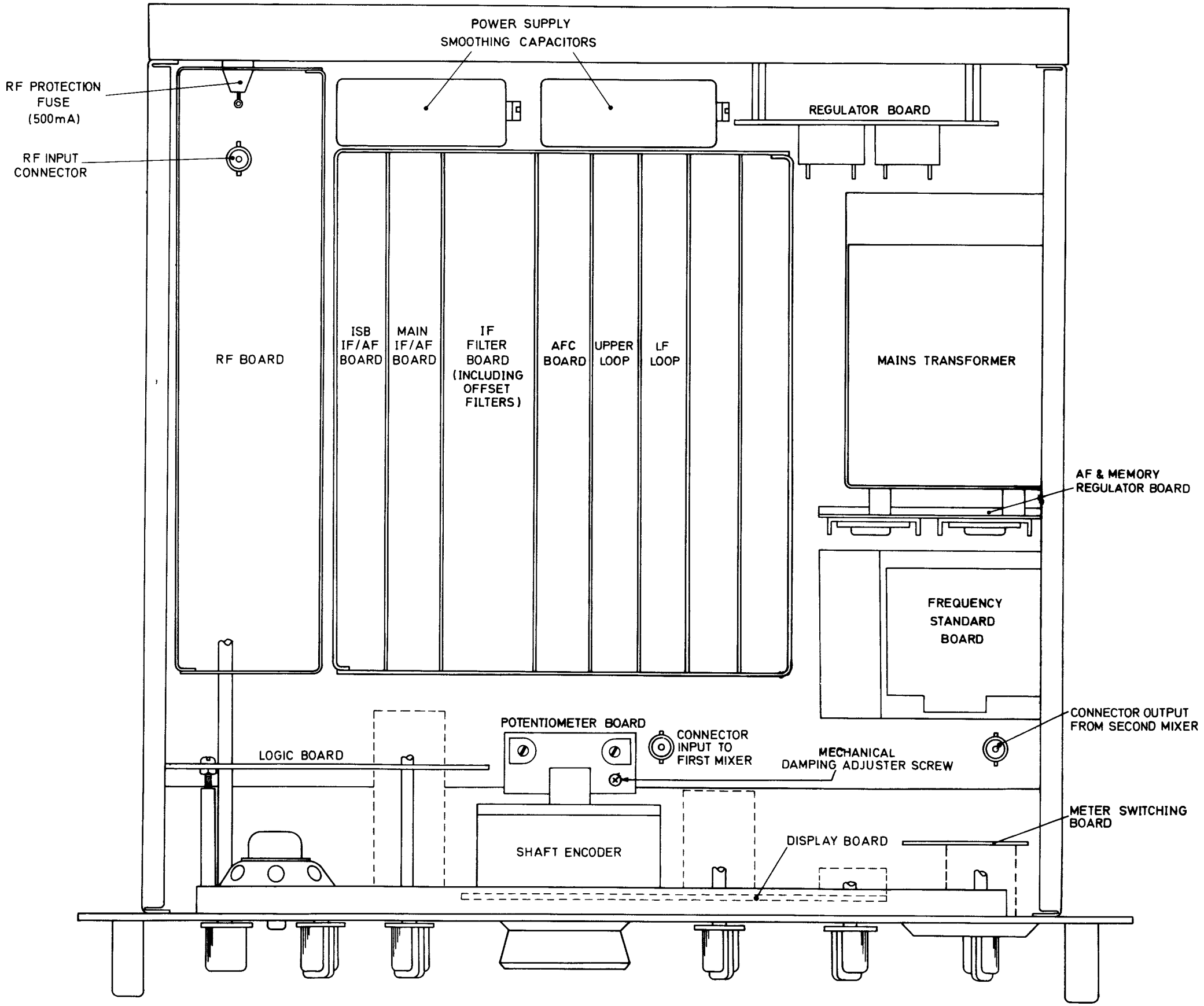


Fig. 2

Chassis layout : top view

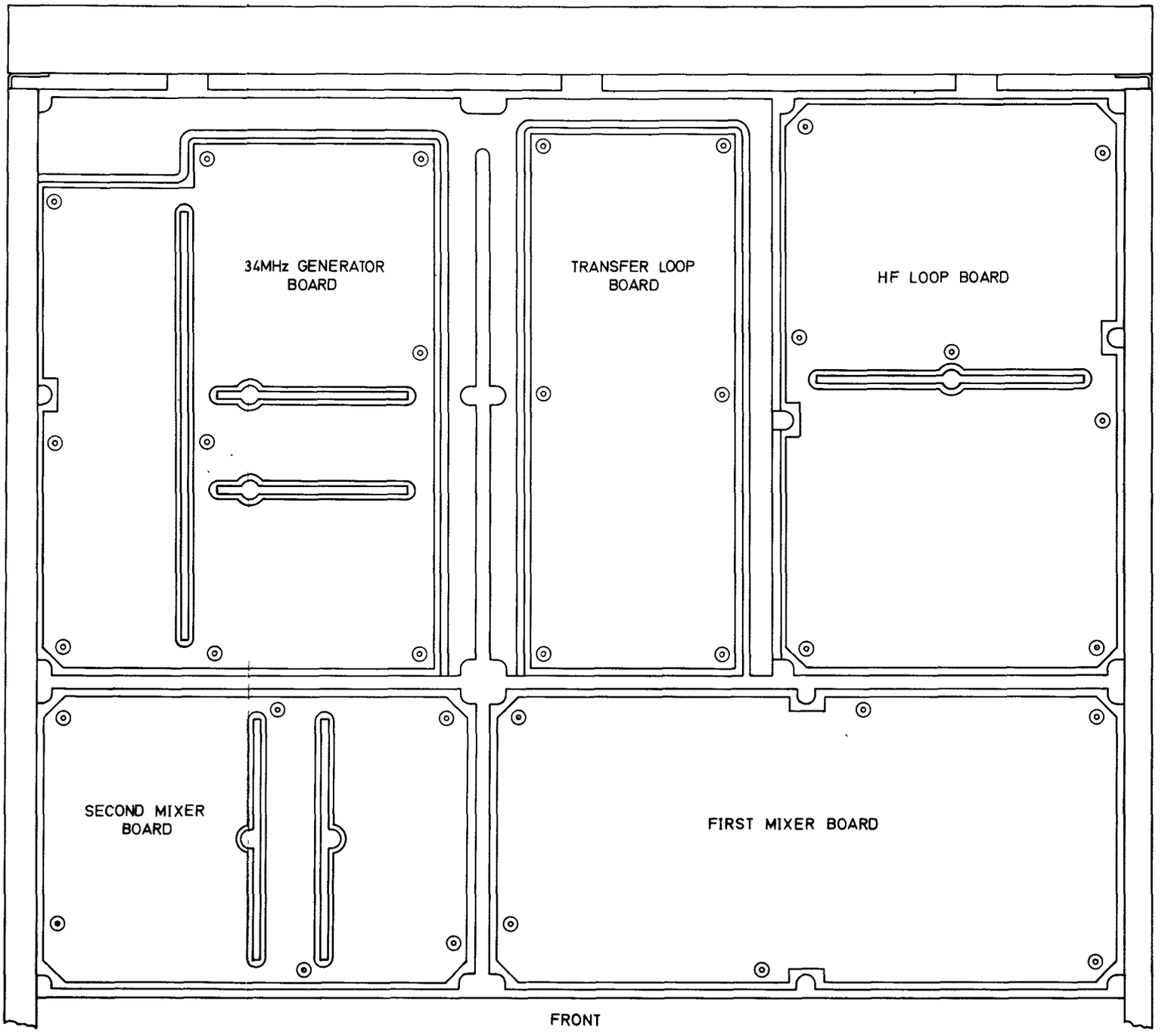


Fig.3 Chassis layout: underside view

Chapter 1-2

FUNCTIONAL DESCRIPTION

CONTENTS

Para.

1 Introduction
2 Frequency selection
3 MHz switch and logic board PS365
4 Optical shaft-encoder
5 Display board PM371
10 Up/down counter
12 Overspill
14 Lock indicator
15 Frequency synthesis
17 Frequency standard
19 1.4 MHz output; PM339
20 34 MHz output; PM339
21 35.4 MHz to 65.4 MHz output
22 Low frequency loop PM588
24 Tuning example
25 Lower transfer loop
28 Tuning example
29 Upper loop PM589
30 Tuning example
31 Upper transfer loop
34 Tuning example
35 HF loop PS337
36 Tuning example
37 Algebraic equation for frequency synthesis
48 RF/IF/AF section
49 RF unit; including rf board PM582
54 Protection stage
55 RF amplifier
56 First mixer PM335
60 Second mixer PM336
63 Main IF/AF board PM364/1
64 Product and af detectors
65 AGC detector
66 Audio pre-amplifier
67 Loudspeaker amplifier
68 ISB/IF/AF board PM364/3
69 Automatic frequency control PM369
► 77 Automatic frequency control PM664 ◄

Table — Page

1 Decimal to nines-complement conversion 9

Fig. — Page

1 Simplified block diagram: receiver 2
2 Block diagram: receiver tuning 5
3 Block diagram: frequency synthesizer 6
4 Block diagram: overall receiver 13

ILLUSTRATIONS (cont.)

Fig.		Page
5	Simplified block diagram : r.f. unit	14
6	Simplified block diagram : first mixer PM.335	15
7	Simplified block diagram : second mixer PM.336	16
8	Simplified block diagram : main i.f./a.f. board PM.364/1 ...	19
9	Simplified block diagram : a.f.c. board PM369	20
►10	Simplified block diagram : a.f.c. board PM664	23 ◄

INTRODUCTION

1. For explanation purposes, the receiver may be divided into three main sections, namely, the frequency selection process, the frequency synthesizer and the r.f./i.f./a.f. stages (fig. 1).

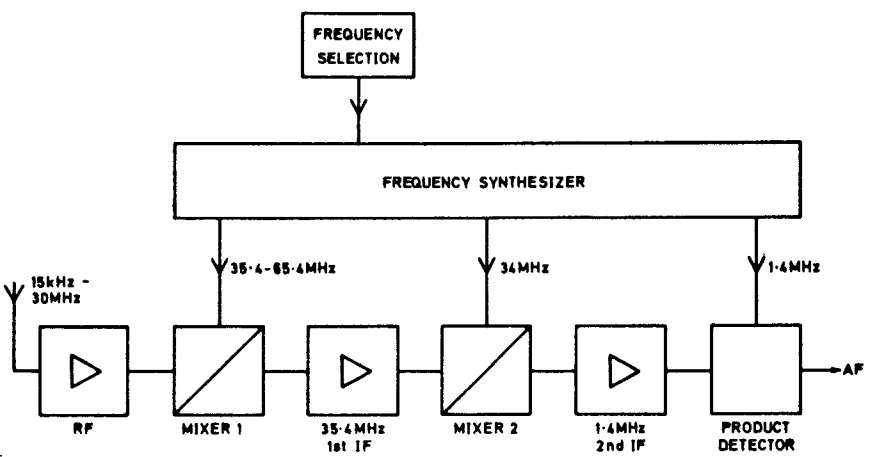


Fig.1 Simplified block diagram : receiver

FREQUENCY SELECTION

2. This section of the receiver embraces the MHz switch, the logic board PS.365, the optical shaft-encoder and the display board PM.371. A block diagram of the receiver tuning section is given in fig.2.

MHz switch and logic board PS.365

3. The MHz switch (mounted on the logic board) provides frequency range information (0 to 29 MHz), in decimal form, to the r.f. unit (seven lines), the first mixer board (two lines) of the r.f./i.f./a.f. section (fig. 4), and to the h.f. loop of the synthesizer (three lines) to select one of three oscillators. The 0 to 29 MHz decimal information is also converted into a nines-complement coded form (logic board) for the programmed dividers of the synthesizer transfer and h.f. loops (fig. 3).

Optical shaft-encoder

4. The KHz tuning control knob is coupled to the spindle of an optical shaft-encoder which is an optical displacement transducer of the incremental type.

A graticule, of a transparent material with opaque stripes, is made to rotate between a pair of lamps and a pair of photo-transistors. As a graticule rotates, the photo-transistors are alternately darkened and illuminated to produce two sinusoidal output waveforms. The two photo-transistors are physically displaced such that these two output waveforms are 90 degrees out of phase, with output A leading output B for one direction of rotation, and lagging output B for the reverse direction of rotation. The two output waveforms are applied to the display board.

Display board PM.371

5. The display board consists of a reversible (up/down) counter chain and associated digital display which provides 100 kHz, 10 kHz, 1 kHz, 100 Hz and 10 Hz frequency setting information, in binary-coded-decimal (BCD) form for the programmed dividers of the frequency synthesizer.

6. The sinusoidal A output signal from the shaft encoder (whilst the kHz control knob is rotated) is shaped and is then applied to three monostables, one of which is used to inhibit the out-of-lock indicator (para.14), whilst receiver tuning is in progress. The remaining two monostables are re-triggerable and are so arranged that one triggers on a positive-going input whilst the other triggers on a negative-going input. The monostable output signal, together with the shaped output derived from the shaft-encoder B signal, are applied to gating circuits which are controlled by the front panel TUNING RATE switch.

7. When the FAST tuning mode is selected, the output signals from both the positive-edge-triggered and the negative-edge-triggered monostables are utilised and at the same time the 10 Hz counter of the up/down counter chain is inhibited. In this mode, 500 pulses are applied to the up/down counter chain for one revolution of the shaft-encoder spindle, which produces a receiver tuning rate of 50 kHz per revolution in 100 Hz steps.

8. The positive-edge-triggered monostable is inhibited when the TUNING RATE switch is set to SLOW and, at the same time, the 10 Hz counter of the up/down counter chain is enabled. Thus, for one revolution of the shaft-encoder spindle, 250 pulses are applied to the counter which counts in 10 Hz steps at a rate of 2.5 kHz per revolution.

9. When the LOCK position of the TUNING RATE switch is selected, the gating circuits block the path of the output pulses and the setting of the up/down counter chain is locked.

Up/down counter

10. This consists of a chain of six cascaded up/down counter elements, five of which have an associated digital display to indicate the 100 kHz, 10 kHz, 1 kHz, 100 Hz and 10 Hz digits of the receiver frequency. The sixth counter element is used to provide the overspill facility (para. 12).

11. When the receiver POWER switch is first set to ON, an initial-zero circuit (not shown on fig.2) sets the counter chain to zero; it follows from this that should the main supply to the receiver be interrupted whilst the receiver is in use, the kHz portion of the receiver frequency would automatically be reset to zero. To prevent this from happening, a +12V battery module is fitted to the rear panel of the receiver. As the receiver kHz control is rotated, the resulting pulses from the gating circuits are counted and the BCD outputs are fed to the frequency display and also to the programmed dividers of the synthesizer.

Overspill

12. The overspill circuit allows the receiver to be tuned up to 20 kHz above or below the selected MHz switch setting. For example, with the MHz switch set to say, 3 MHz, the tuning range of the kHz control is from 2.97999 MHz to 4.02000 MHz. As the kHz display passes from 99999 to 00000, at the top end of the band, the lamp behind the 3 on the MHz dial extinguishes and the lamp behind the 4 illuminates. Similarly, when the kHz display passes from 00000 to 99999, at the bottom end of the band, the lamp behind the 3 on the MHz dial extinguishes and the lamp behind the 2 illuminates.

13. When the receiver is in the overspill condition, overspill data, in BCD form, is applied to the low and upper frequency loops of the synthesizer to modify the division ratios of the programmed dividers.

Lock indicator

14. The lock indicator circuit receives information from the phase-locked loops of the synthesizer and illuminates the OUT-OF-LOCK lamp on the front panel should any loop go out of phase-lock. The lock indicator circuit is inhibited when the receiver kHz control is rotated (para. 6).

FREQUENCY SYNTHESIS

15. The simplified block diagram of the receiver (fig. 1) shows the three mixer injection signals produced by the frequency synthesizer. The first i.f., at 35.4MHz,is high compared with the received signal frequency at the antenna, to provide good image rejection. To produce this first i.f., the frequency synthesizer must provide an output signal in the range 35.4 to 65.4 MHz. The second i.f., at 1.4 MHz, is low to provide good selectivity, and requires a fixed 34 MHz frequency output signal from the synthesizer. Finally, a frequency of 1.4 MHz is needed for the product detector for the reception of s.s.b. signals.

16. The indirect method of frequency synthesis is used where the required output frequencies (with the exception of the 1.4 MHz output) are derived from voltage-controlled oscillators which are phase-locked to a common frequency standard. A simplified block diagrm of the frequency synthesizer is given in fig.3.

Frequency standard

17. This is a 5 MHz fast-warm-up crystal oscillator of high accuracy and long-term stability. The crystal is mounted in a temperature controlled oven which, with the maintaining circuit and a buffer amplifier, is encapsulated in polyurethane foam to provide heat insulation.

18. The output signal from the frequency standard is applied to a divide-by-five stage (on the 34 MHz generator board) to produce a 1 MHz reference frequency for the synthesizer.

1.4 MHz output; 34 MHz board PM.339

19. The 1 MHz reference frequency is further divided by five to produce an output at 200 kHz. A 1.4 MHz crystal band-pass filter selects the seventh harmonic and this is amplified to produce a 1.4 MHz output at the required level.

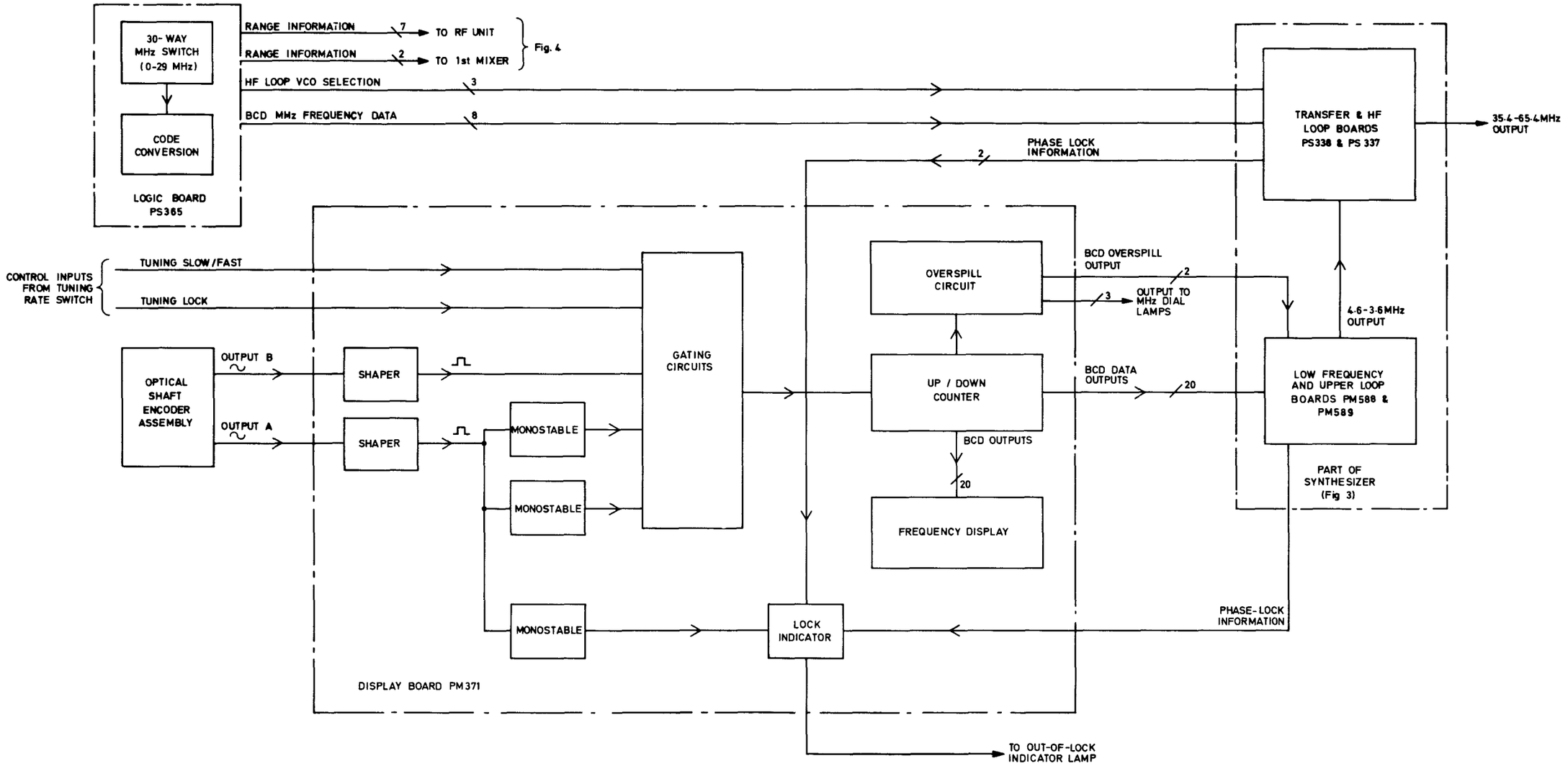


Fig. 2

Block diagram: receiver tuning

Issued Feb. 76

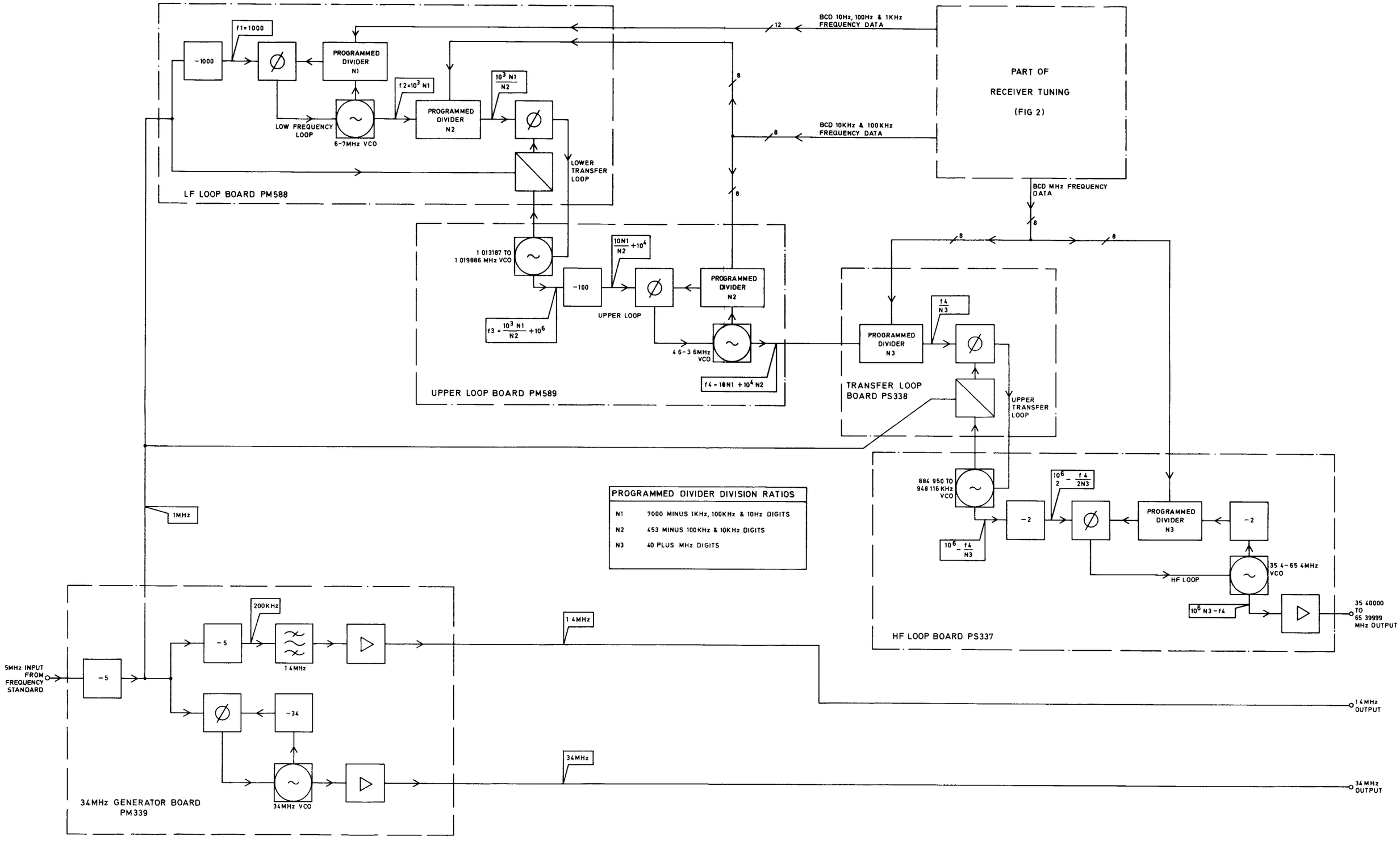


Fig.3

Block diagram : frequency synthesizer

Fig.3

34 MHz output; 34 MHz board PM.339

20. The 34 MHz second-mixer injection frequency is derived from a 34 MHz voltage-controlled oscillator (v.c.o.) which is phase-locked to the 1 MHz reference frequency. A sample of the v.c.o. output is first divided by 34 and is then phase-compared with the 1 MHz reference frequency; any difference in phase results in a correction voltage which is fed back to the v.c.o.

35.4 MHz to 65.4 MHz output

21. This is the main output signal from the frequency synthesizer; it covers the frequency range 35.40000 to 65.39999 MHz in 10 Hz increments and is controlled by the 30-way MHz switch and the shaft-encoder (kHz control). The output frequency is derived from five cascaded phase-locked loops where the divided output from one loop becomes the phase-detector input of the next loop; this process is described in para. 22 to 47.

Low frequency loop PM.588

22. The low frequency loop consists of a 6 to 7 MHz v.c.o., a programmed divider, N1, and a phase comparator. The phase comparator compares the phase of the output signal from the programmed divider with that of a 1 kHz reference frequency derived from the frequency standard. Should a phase difference exist, a correction voltage is derived which is fed back to the v.c.o. to eliminate the error.

23. The programmed divider, N1, has a division ratio of from 7000 to 6001 and is controlled by the 10 Hz, 100 Hz and 1 kHz digits of the selected receiver operating frequency; a receiver frequency setting of 000 sets the division ratio to 7000, a setting of 999 sets the division ratio to 6001, and the division ratio for intermediate frequency settings is given by the expression: N1 = 7000 minus selected 1 kHz, 100 Hz and 10 Hz digits. The divider consists of a number of cascaded decade counters where the start of a count sequence may be programmed by the output from the display board (controlled by the shaft-encoder) and where the counter is reset (strobed) when a count of 7000 is reached. When the v.c.o. has been driven to the correct frequency the reset (strobe) pulses will occur at a repetition rate of exactly 1k p.p.s., as will the output pulses applied to the phase comparator.

Tuning example

24. Consider a receiver operating frequency of 12.34567 MHz. The first mixer injection frequency required to produce the first intermediate frequency of 35.4 MHz is, therefore, 12.34567 MHz + 35.4 MHz which equals 47.74567 MHz. With reference to the operating frequency of 12.34567 MHz, only the last three digits, i.e. 567, need be considered for this part of the circuit. Thus the programmed divider, N1, is preset to start counting at 567 and counts up to 7000 viz a total of 6433 pulses (7000-567); this is equal to a v.c.o. frequency of 6.433 MHz.

Lower transfer loop

25. The lower transfer loop, so called because the low frequency increments at its input i.e. the 10 Hz, 100 Hz and 1 kHz digits, are transferred to its output, consists of a programmed divider, N2, a 1.013187 to 1.019886 MHz v.c.o a mixer and a phase comparator. It generates, together with the upper loop, the 100 kHz and 10 kHz digits of the variable output frequency.

26. The programmed divider, N2, has a division ratio of from 453 to 354 and is controlled by the 100 kHz and 10 kHz digits of the selected receiver operating frequency; this division ratio is modified to cover the range 455 to 352 when in the overspill condition i.e. 20 kHz beyond either end of the selected 1 MHz band. A receiver frequency setting of 00 for the 100 kHz and 10 kHz digits results in a division ratio of 453, a setting of 99 results in a division ratio of 354 and the division ratio for intermediate frequency settings is given by the expression: N2 = 453 minus the selected 100 kHz and 10 kHz digits.

27. The output signal from the low frequency loop is first divided by N2 and is then applied as one input to the phase comparator. The output from the v.c.o. is mixed with the 1 MHz reference frequency, derived from the frequency standard, and the difference frequency signal from the mixer is applied as the second input to the phase comparator. Thus the output voltage from the phase comparator drives the v.c.o. to a frequency which is exactly 1 MHz above the output signal frequency from the programmed divider, N2.

Tuning example

28. With reference to the receiver operating frequency of 12.34567 MHz (para. 24), the 100 kHz and 10 kHz digits required are 3 and 4 respectively. The division ratio of N2 is, therefore, 453-34 = 419. The 6.433 MHz output frequency from the low-frequency loop is divided by 419 and the result is added to 1 MHz.

$$\text{Lower-transfer-loop output} = \frac{6.433 \times 10^6}{419} + 10^6 \text{ Hz}$$

$$= 1.015353 \text{ MHz}$$

Upper loop PM.589

29. The output signal from the lower transfer loop is first divided by 100 and is then applied as one input to a phase comparator; the other phase comparator input is from a programmed divider, N2; a 3.6 to 4.6 MHz v.c.o. is driven to the required frequency by the phase comparator output. The programmed divider, N2, is set to the same division ratio as that of the lower transfer loop as described in para. 26.

Tuning example

30. The 1.015353 MHz output signal from the lower transfer loop (para.28) is first divided by 100 and is then multiplied by N2, i.e. 419.

$$\text{Upper loop output} = \frac{1.015353 \times 419}{100}$$

$$= 0.010154 \times 419$$

$$= 4.25433 \text{ MHz}$$

Upper transfer loop

31. This loop, in conjunction with the h.f. loop, generates the MHz portion of the variable output frequency, and is controlled by the 30-way MHz switch. It consists of a programmed divider, N3, a phase comparator, a mixer and a v.c.o. which covers the frequency range 884.950 to 948.116 kHz.

32. The programmed divider, N3, has a division ratio of from 40 to 69. In contrast to the previously described programmed dividers, N1 and N2, the division ratio of N3 is found by adding 40 to the setting of the receiver MHz switch. This is achieved by first converting the decimal 0 to 29 output from the MHz switch into a nines-complement code before application to the programmed divider which counts from the programmed starting point up to 99, and then to 39 when the reset occurs. Table 1 gives the conversion from decimal to nines-complement code.

TABLE 1

Decimal-to nines-complement conversion

Decimal	BCD				Nines complement				Decimal
	D	C	B	A	D9	C9	B9	A9	
0	0	0	0	0	1	0	0	1	9
1	0	0	0	1	1	0	0	0	8
2	0	0	1	0	0	1	1	1	7
3	0	0	1	1	0	1	1	0	6
4	0	1	0	0	0	1	0	1	5
5	0	1	0	1	0	1	0	0	4
6	0	1	1	0	0	0	1	1	3
7	0	1	1	1	0	0	1	0	2
8	1	0	0	0	0	0	0	1	1
9	1	0	0	1	0	0	0	0	0

33. The 4.6 to 3.6 MHz output from the upper loop is divided by N3 and is then applied as one input to a phase comparator. The output from the v.c.o. is mixed with the 1 MHz reference frequency, derived from the frequency standard, and the sum frequency output from the mixer is applied as the second input to the phase comparator. Thus the output voltage from the phase comparator drives the v.c.o. to a frequency which is equal to 1 MHz minus the output frequency from the programmed divider, N3.

Tuning example

34. The division ratio for the programmed divider, N3, is obtained by adding 40 to the MHz digits of the receiver operating frequency. Thus for the frequency of 12.34567 MHz (para. 24), N3 will be 40 plus 12 which equals 52. The 4.25433 MHz output from the upper loop (para. 30) is divided by 52 and the result is then subtracted from 1 MHz to give the upper loop output frequency

$$\text{Upper transfer loop output} = 1 - \frac{4.25433}{52} \text{ MHz}$$

$$= 1 - 0.081814$$

$$= 918.186 \text{ kHz}$$

35. The output signal from the upper transfer loop is first divided by two and is then applied as one input to a phase comparator. The output from a 35.4 to 65 MHz v.c.o. is also divided by two and is then applied to the programmed divider, N3, which in turn provides the second input to the phase comparator. Thus the v.c.o. is driven to the required frequency by the phase comparator output. The programmed divider, N3, is set to the same division ratio as that of the upper transfer loop.

Tuning example

36. The 918.186 kHz output from the upper transfer loop is first divided by two and is then multiplied by 2N3, i.e. 2 x 52, to give the final output frequency.

$$\text{First mixer frequency} = \frac{0.918186}{2} \times 2 \times 52 \text{ MHz}$$

$$= 0.918186 \times 52 \text{ MHz}$$

$$= 47.74567 \text{ MHz}$$

This figure is the receiver operating frequency plus the first intermediate frequency and agrees with the original frequency arrived at in para. 24.

ALGEBRAIC EQUATION FOR FREQUENCY SYNTHESIS

37. The variable output frequency of the synthesis section of the receiver may be worked out for any receiver-operating-frequency by using a simple algebraic equation. The following paragraphs show the derivation of this equation and should be read in conjunction with the simplified block diagram (fig.3).

38. The 1 kHz reference-frequency input to the phase comparator of the low-frequency loop, designated f1, is expressed as: $f1 = 10^3$ Hz. The output from the low-frequency loop (f2) is therefore:

$$f2 = 10^3.N1 \text{ Hz} \quad \ldots\ldots\ldots\ldots (1)$$

39. The lower-transfer-loop divides its input by N2 and then adds the result to 1 MHz. This is given by:

$$f3 = \frac{10^3.N1}{N2} + 10^6 \text{ Hz} \quad \ldots\ldots (2)$$

40. The output from the lower-transfer loop (f3) is first divided by 100 before being applied to the phase comparator of the upper loop. Dividing the equation (2) by 100 gives:

$$\frac{f3}{100} = \frac{10^3.N1}{100\ N2} + \frac{10^6}{10^2} \text{ Hz} \quad \ldots\ldots (3)$$

which resolves to:

$$\frac{10N1}{N2} + 10^4 \text{ Hz} \quad \ldots\ldots\ldots\ldots (4)$$

41. The output from the upper loop (f4) is now found by multiplying equation (4) by the division ratio N2:

$$f4 = 10N1 + 10^4.N2 \text{ Hz} \ldots\ldots\ldots(5)$$

42. The output from the upper loop (f4) is first divided by N3 before being applied to the phase comparator of the upper-transfer-loop. By dividing f4 by N3 gives:

$$\frac{f4}{N3} \text{ Hz} \ldots\ldots\ldots\ldots\ldots\ldots\ldots(6)$$

43. The output from the upper-transfer-loop (f5) is now found by subtracting the output frequency of N3 from 1 MHz.

$$f5 = 10 - \frac{f4}{N3} \text{ Hz} \ldots\ldots\ldots(7)$$

44. Frequency f5 is divided by 2 before being applied to the phase comparator of the h.f. loop.

$$\frac{f5}{2} = \frac{10^6}{2} - \frac{f4}{2N3} \text{ Hz} \ldots\ldots\ldots(8)$$

45. The final output frequency (f6) is now found by multiplying equation (8) by 2N3; therefore:

$$f6 = \frac{10^6\ 2N3}{2} - \frac{f4.2N3}{2N3} \text{ Hz} \ldots(9)$$

which resolves to:

$$f6 = 10^6\ N3 - f4 \text{ Hz} \ldots\ldots\ldots(10)$$

46. For the 12.4567 MHz receiver-operating-frequency (para.10), the division ratios of N1, N2 and N3 are established as below:

N1 = 6433 (para.24)

N2 = 419 (para.28)

N3 = 52 (para.34)

47. Substituting the values for N1 and N2 in equation (5):

$$f4 = (10 \times 6433) + (419 \times 10^4) \text{ Hz}$$

$$= 4\ 254\ 330 \text{ Hz}$$

Substituting the values of N3 and f4 in equation (10):

$$f6 = (52 \times 10^6) - 4\ 254\ 330 \text{ Hz}$$

$$= 47.74567 \text{ MHz.}$$

R.F./I.F./A.F. SECTION

48. The following paragraphs should be read in conjunction with the respective simplified block diagram (fig. 5 to 9) and the overall receiver block diagram (fig. 4).

R.F. unit; including r.f. board PM.582 (fig. 5)

49. The received signal at the antenna, in the frequency range 15 kHz to 30 MHz, is fed via a re-radiation filter and a 500 mA fuse to a wideband protection stage. This consists of a voltage-sensitive circuit and a relay (RLQ/1), which open-circuits the r.f. path for signals which exceed approximately 30V e.m.f. at the antenna socket. This relay is also used for receiver muting and operates when an earth is applied to the rear panel MUTE terminal.

50. From relay contact RLQ1, the received signal is applied to a 30 MHz low-pass filter and then takes one of a number of paths dependent on the RF TUNE control setting and also the selected position of the front panel MHz switch, as detailed below.

51. MHz switch set to 0 MHz position. An earth from the MHz switch is routed to relays RLA/1 and RLB/1 which become energized. The output signal from the 30 MHz low-pass filter is applied to a 1 MHz low-pass filter, via RLA1, and thence via RLB1 and contact RLR1 of the normally energized protection relay RLR/1, to the wideband r.f. amplifier.

52. MHz switch set to any position other than 0 MHz, and RF TUNE control set to WB (wideband). Operation of the microswitch (controlled by RF TUNE control) routes an earth from the MHz switch to relays RLN/1 and RLP/1. The relays energize and a path is provided from the low-pass filter to the wideband r.f. amplifier via RLN1, RLP1 and contact RLR1 of the normally-energized protection relay, RLR/1.

53. MHz switch set to any position other than 0 MHz, and RF TUNE control not in WB position. An earth from the MHz switch is applied to the appropriate pair of tuneable-circuit selection relays and a common +12V relay supply is provided by the normally-closed contacts of the microswitch. The contacts of the selected relays close and the received signal from the low-pass filter is applied to the appropriate tuned circuit, tuned by the RF TUNE control, and thence passed to the r.f. amplifier via RLR1.

Protection stage

54. A further protection stage is fitted which allows for 'working-through' off-tune signals of up to approximately 10V e.m.f. at the antenna socket. The circuit is similar to that of the wideband protection stage; relay RLR/1 becomes de-energized once the 10V e.m.f. threshold is exceeded and the signal path to the r.f. amplifier is broken.

R.F. amplifier

55. A conventional high-linearity circuit is used. After amplification, the received signal is passed via a 30 MHz low-pass filter to the first mixer.

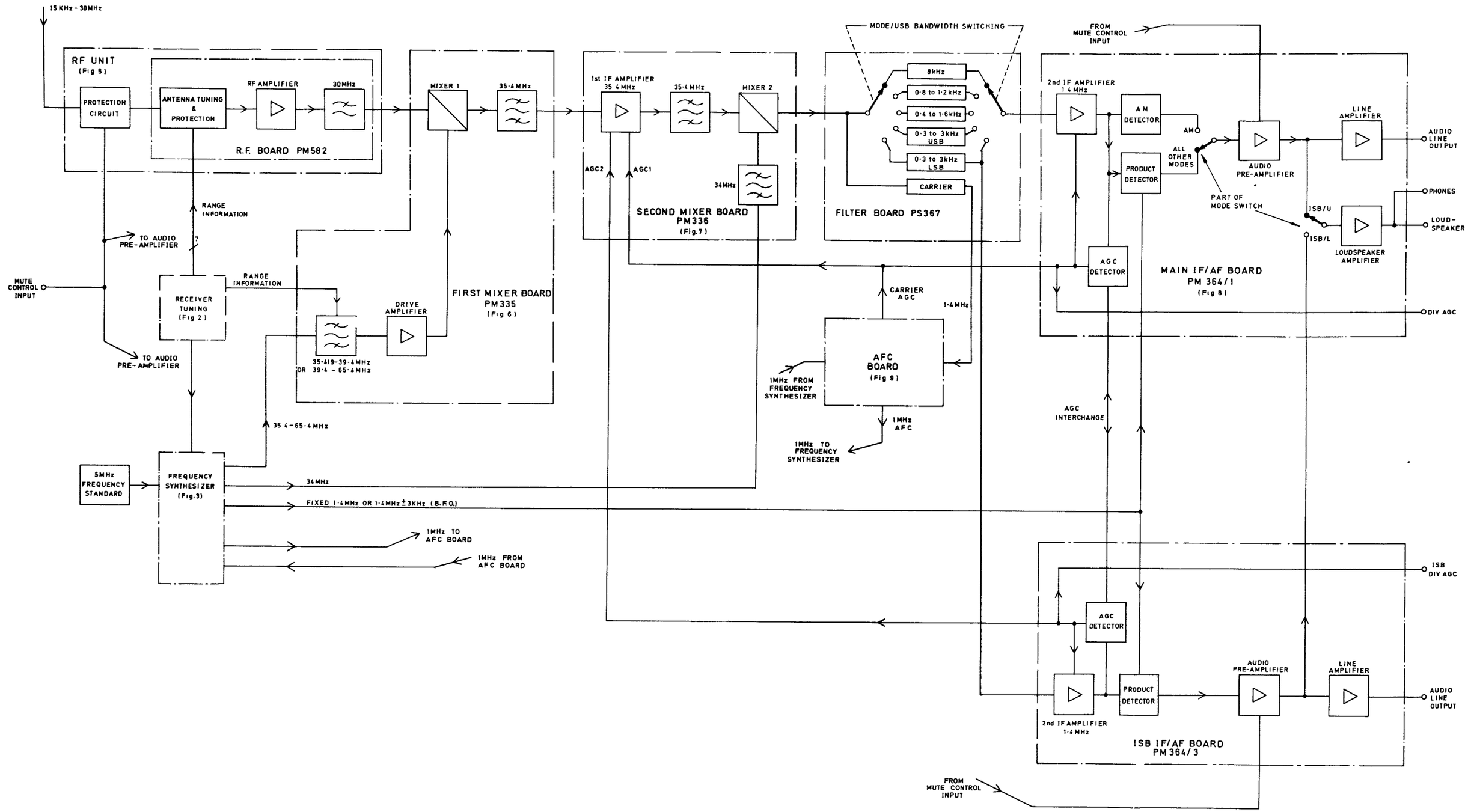
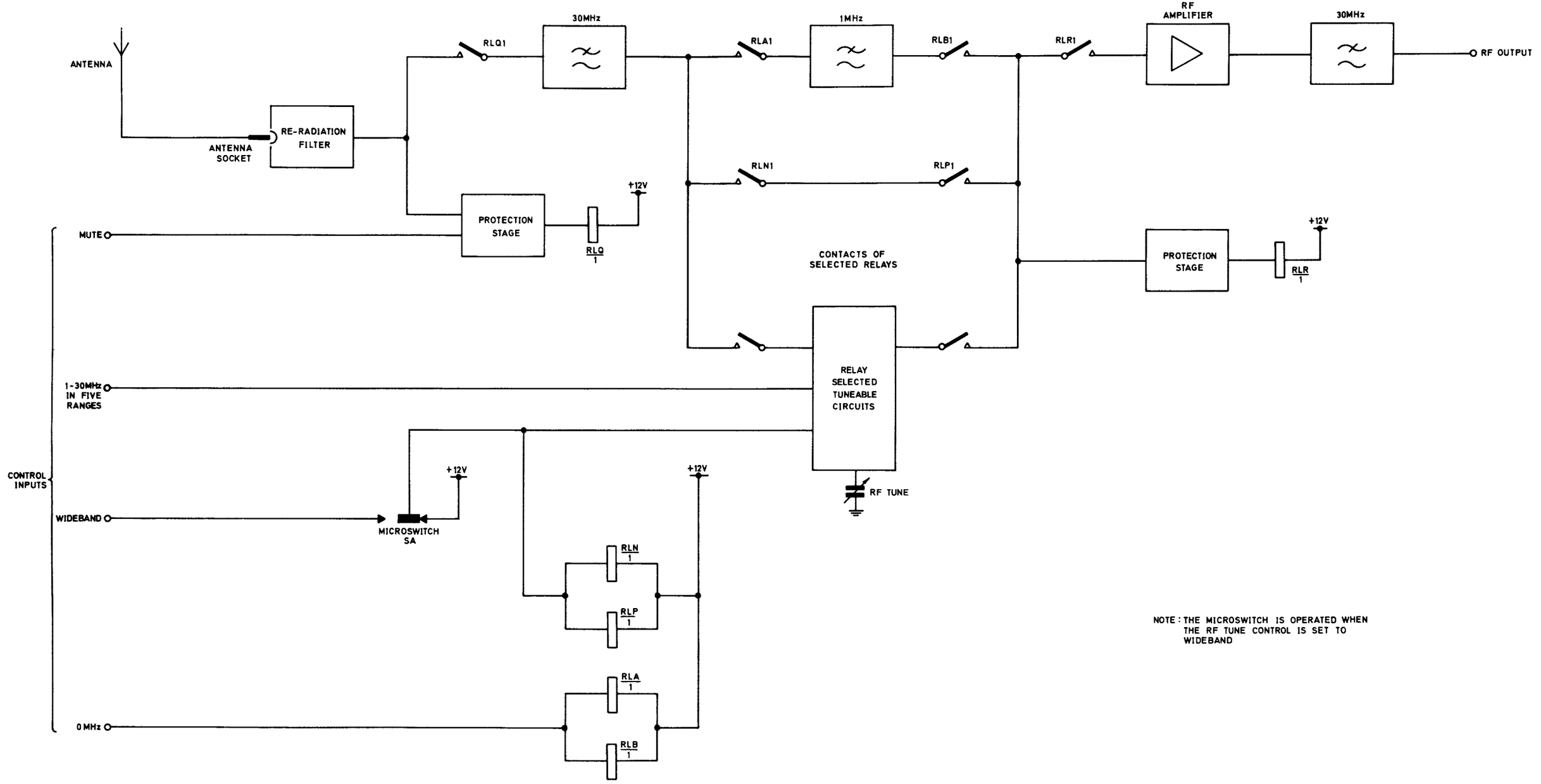


Fig.4

Block diagram: overall receiver

Issued Feb. 76



NOTE : THE MICROSWITCH IS OPERATED WHEN THE RF TUNE CONTROL IS SET TO WIDEBAND

Fig. 5

Simplified block diagram : RF unit

Fig. 5

First mixer PM.335 (fig. 6)

56. The output signal from the r.f. unit is mixed with the 35.4 to 65.4 MHz local-oscillator signal, from the frequency synthesizer, to produce the first i.f. at 35.4 MHz.

57. The local-oscillator signal is applied to one of two filters, dependent on the setting of the front panel MHz switch; for settings of 0, 1, 2 or 3 MHz, a filter with a passband of 35.415 to 39.4 MHz is selected whereas, for settings of 4 to 29 MHz, a filter with a passband of 39.4 to 65.4 MHz is selected.

58. The output signal from the selected filter is applied to a drive amplifier and then to a high performance mixer. A detector and amplifier circuit provides an indication of DRIVE LEVEL at the front-panel meter.

59. The output signal from the r.f. unit is mixed with the local-oscillator signal and the difference frequency output is fed via a 35.4 MHz band-pass filter to the second mixer.

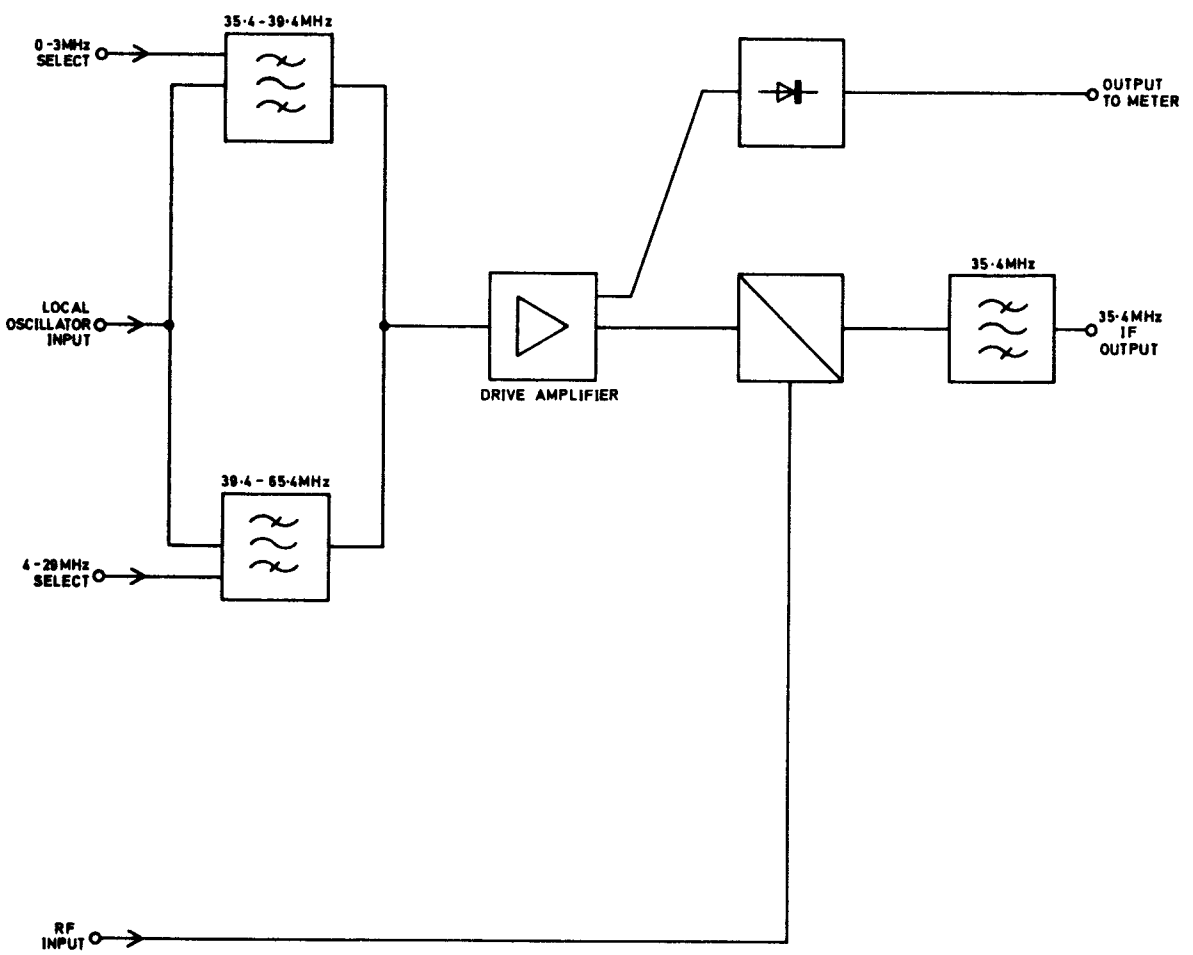


Fig.6 Simplified block diagram : first mixer PM.335

Second mixer PM.336 (fig. 7)

60. The 35.4 MHz first i.f. output from the first mixer is amplified and mixed with the 34 MHz output from the frequency synthesizer. This produces the second i.f., at 1.4 MHz, which is fed to the i.f. amplifier stages via the front-panel-selected s.s.b., i.s.b. or symmetrical filter (fig. 4).

61. The output signal level from the first stage of i.f. amplification is automatically controlled by the AGC1 and AGC2 inputs from the main i.f. board and i.s.b./i.f. board, respectively, via a voltage-controlled attenuator. The output from the second stage of i.f. amplification is applied to a balanced mixer via a 35.4 MHz band-pass filter.

62. The 34 MHz second-mixer injection frequency, from the frequency synthesizer section, is applied to the mixer via a 34 MHz band-pass filter. The difference-frequency output from the mixer, at 1.4 MHz, is amplified before being applied to the filter board.

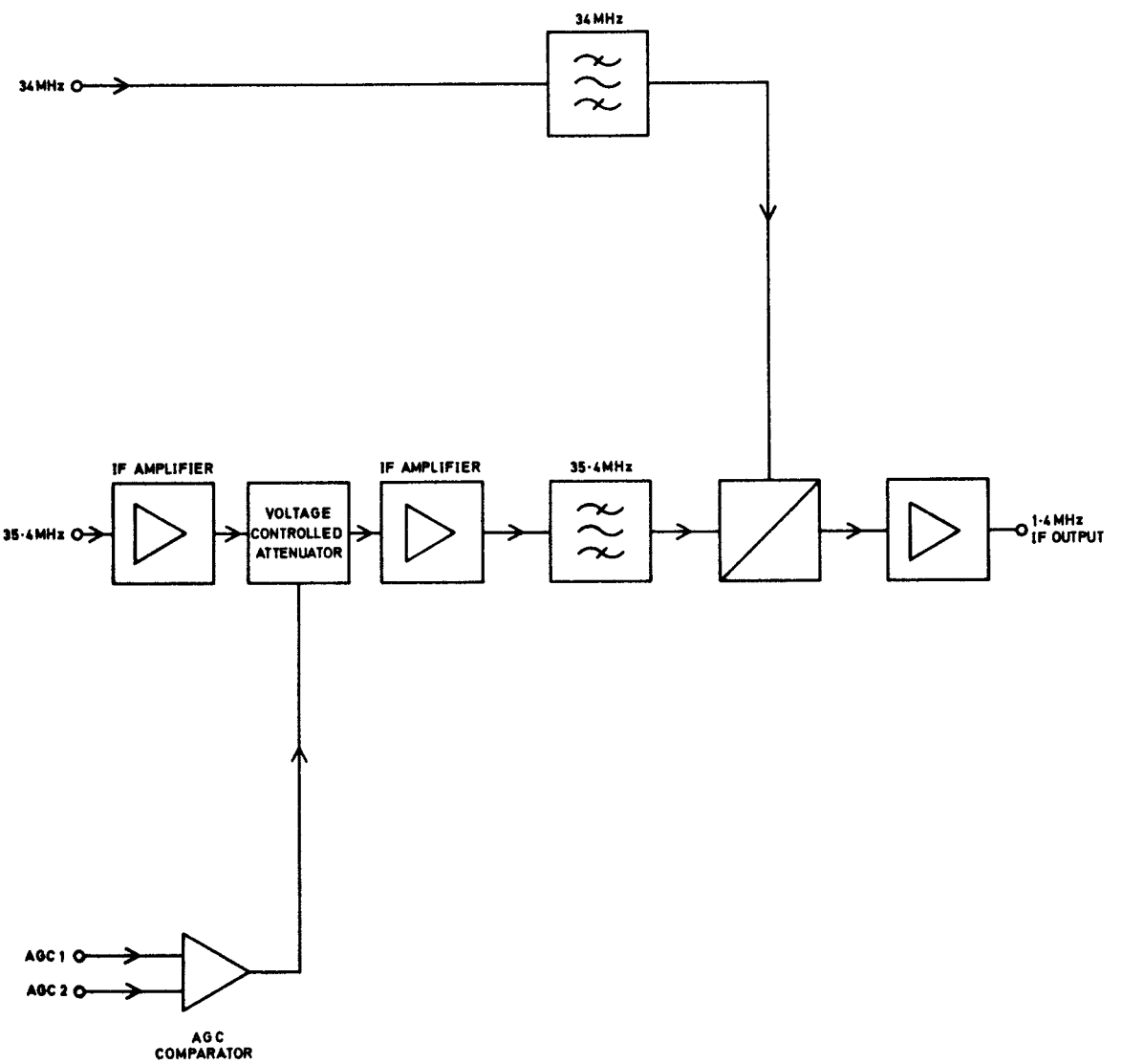


Fig.7 Simplified block diagram : second mixer PM.336

Main i.f./a.f. board PM.364/1 (fig. 8)

63. The 1.4 MHz second i.f. output signal from the second mixer is applied to the i.f./a.f. board via the selected 1.4 MHz filter (fig. 4). The i.f. amplifier stage consists of an automatic gain-controlled integrated-circuit amplifier which feeds two buffer amplifier stages; the output from one is applied to the product and a.m. detectors, whilst the output from the other is applied to the a.g.c. detector and the 1.4 MHz output amplifier.

Product and a.m. detectors

64. Detector selection is controlled by the front-panel MODE switch. The a.m. detector, which is of the envelope type, is selected in the AM position of the MODE switch, and a modified Foster-Seeley product-detector is selected for all other modes.

A.G.C. detector

65. The a.g.c. detector develops a direct voltage which is proportional to the amplitude of the 1.4 MHz i.f. signal. This gain-control voltage, after amplification, is applied to the 35.4 MHz first i.f. amplifier (on the second mixer board), a rear-panel terminal and also to the 1.4 MHz second i.f. amplifier via the front-panel a.g.c. switch. This switch provides for the selection of either a long or a short a.g.c. time-constant. In the OFF position, the a.g.c. voltage is removed from the 1.4 MHz second i.f. amplifier and the gain of this stage is then controlled by the front-panel IF GAIN control.

Audio pre-amplifier

66. The output signal from either the product-detector or the a.m. detector is applied to the audio pre-amplifier. This stage has a muting capability such that the output is inhibited when an earth is applied to the MUTE terminal on the rear panel. The amplified audio output is applied to the line amplifier via the AM/USB LINE LEVEL control and also to the loudspeaker amplifier via the MODE switch when set to any position other than ISB-L or LSB; in these two positions the audio pre-amplifier output from the i.s.b./i.f./a.f. board is applied to the loudspeaker amplifier.

Loudspeaker amplifier

67. The loudspeaker amplifier provides a 50 mW output for the internal loudspeaker, a 1 watt, 8-ohm output for an externally connected loudspeaker, and two 10 mW, 600-ohm headphone outputs.

I.S.B./I.F./A.F. board PM.364/3

68. This board is similar to the main I.F./A.F. board except that the AM detector is not utilised and a loudspeaker amplifier is not fitted.

Automatic frequency control PM.369 (fig. 9)

69. The a.f.c. facility is used to automatically lock the receiver frequency to that of the incoming carrier. This is achieved by transferring the frequency deviation of the received signal to a 1 MHz signal which is then applied to the synthesizer section of the receiver (34 MHz generator circuit) in place of the 1 MHz reference frequency derived from the frequency standard.

70. The 1.4 MHz second i.f. output from the carrier filter (on the filter board) is applied via an attenuator to an amplifier stage. The attenuator is controlled by the front panel AFC switch and is switched in for FULL CARRIER or out for PILOT CARRIER. The amplified 1.4 MHz carrier is fed to a crystal band-pass filter (passband 200 Hz) and is then mixed with a 1 MHz signal derived from the frequency standard. The resultant 400 kHz difference frequency output is amplified and buffered and is then applied as one input to a phase-comparator.

71. The output signal from a 1.6 MHz v.c.o. is divided by four and the resulting 400 kHz signal is applied as the second input to the phase-comparator.

72. The phase-comparator compares the frequency and phase of the 400 kHz input derived from the received signal with the 400 kHz input derived from the 1.6 MHz v.c.o. Any error between these two input signals is used to develop a direct control voltage which is applied, via the loop amplifier, to the 1.6 MHz v.c.o. to eliminate the error. Thus any frequency deviation in the received signal will cause a deviation in the frequency of the 1.6 MHz v.c.o.

73. A second output from the phase-comparator is used to develop an a.g.c. voltage which is proportional to the amplitude of the received carrier. This a.g.c. voltage, after amplification, is applied to the 1.4 MHz amplifier stage and also to a pair of output amplifiers. The AGC1 and AGC2 outputs are used to supplement the a.g.c. outputs from the main i.f./a.f. band and the i.s.b./i.f./a.f. board.

74. A second 400 kHz output from the divide-by-four stage is again divided, this time by 16, to provide a 25 kHz input to a digital phase-comparator. The second input signal to the digital phase-comparator, also at a frequency of 25 kHz, is derived from the reference 1 MHz input and a divide-by-40 stage. The digital output from the phase-comparator is applied to a voltage control circuit where it is converted to a direct voltage, the level of which is proportional to the difference in frequency and phase of the two input signals to the phase-comparator. This voltage is applied to a 7 MHz v.c.o. via a hold switch, a narrow band loop filter and a loop amplifier.

75. The hold switch is controlled by a signal-to-noise ratio detector. Should the signal-to-noise ration fall below a pre-determined threshold, or should the carrier input to the AFC board fail, the hold switch effectively open-circuits the output from the voltage control circuit, and holds the voltage level applied to the loop filter. This holds the frequency of the 7 MHz v.c.o. until an improvement in the signal-to-noise ratio occurs or until the carrier re-appears.

76. The 7 MHz output signal is applied to a divide-by-seven stage, and the final output signal, at 1 MHz plus or minus the frequency deviation, is applied to the 34 MHz generator board in place of the reference 1 MHz derived from the frequency standard. The purpose of this 1 MHz comparison is to pre-lock the 7 MHz v.c.o. to a nominal frequency before a.f.c. lock is attempted.

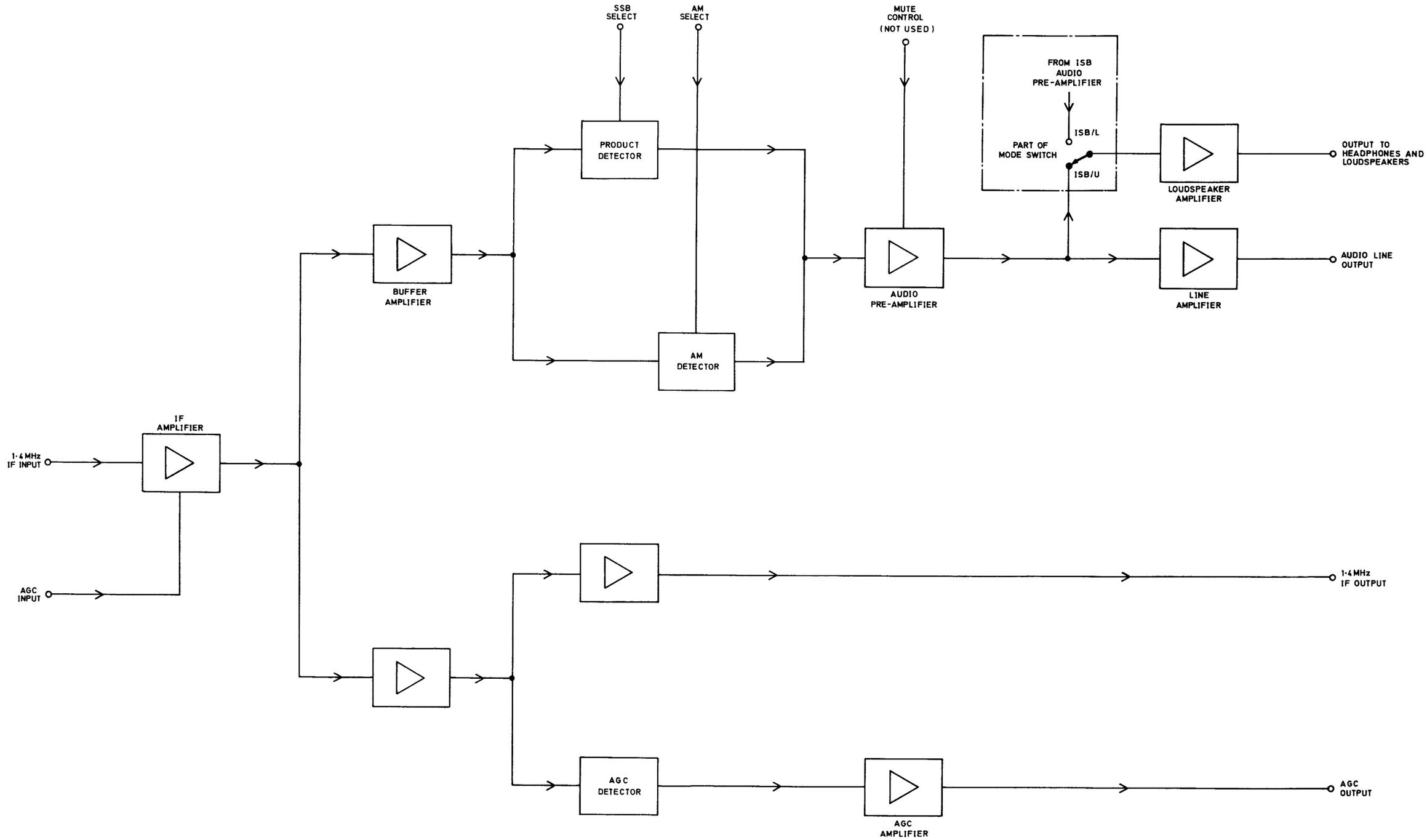


Fig. 8

Simplified block diagram : main IF/AF board PM364/1

Issued Feb. 76

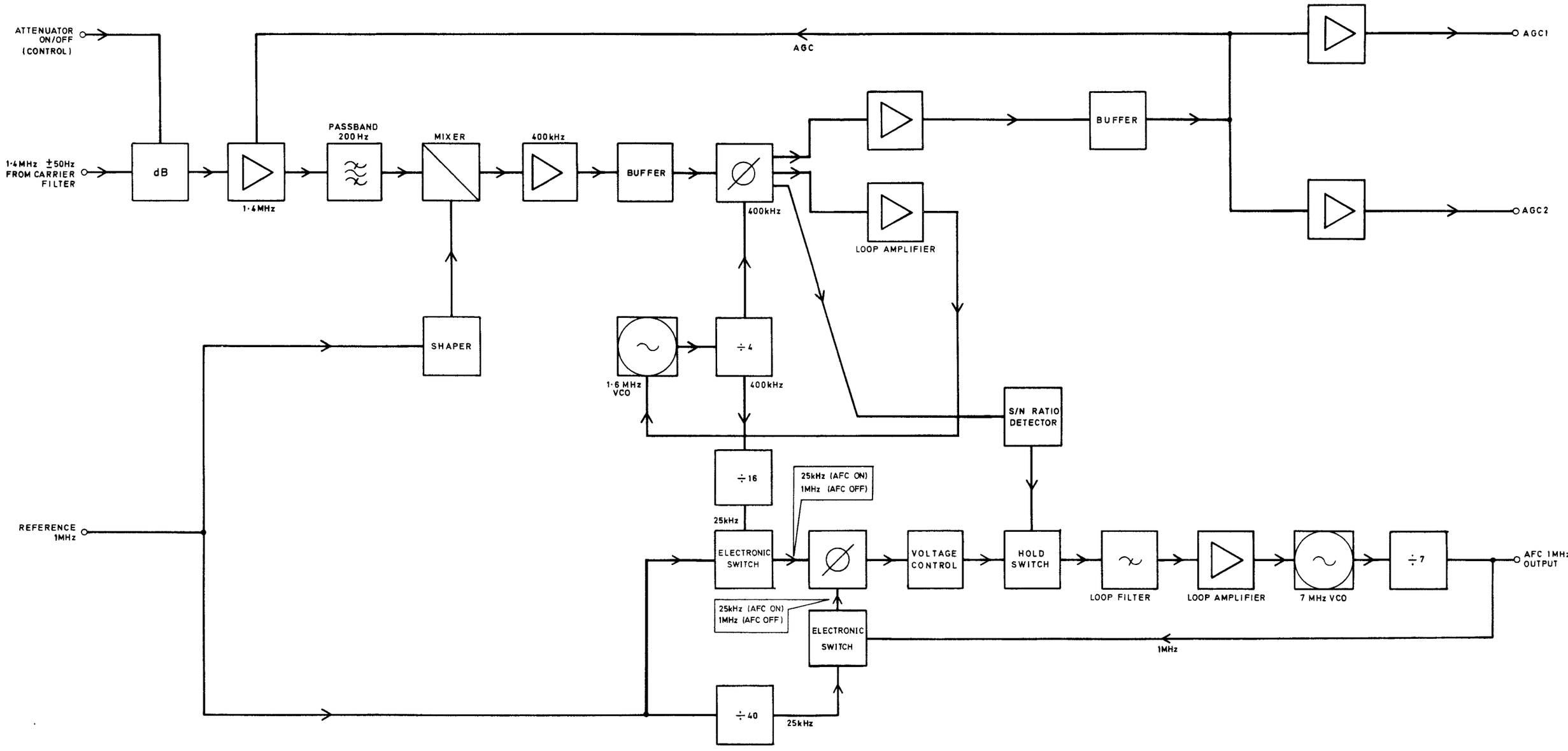


Fig. 9

Simplified block diagram: a.f.c. board

Fig. 9

Automatic frequency control PM664 (fig.10)

77 The afc board PM664 is a fully-interchangeable CMOS alternative to the PM369; it has an improved performance, and is fitted in receivers from serial number 1721 onwards.

78 The purpose of the afc system is to effectively stabilise the signal received from a drifting transmitter. This function is performed by slightly varying the frequency of the 34 MHz injection to the second mixer, maintaining a constant 1.4 MHz output signal. The 34 MHz injection is provided by an oscillator phase-locked to an applied 1 MHz input signal.

79 With AFC switched OFF, the 34 MHz generator uses the 1 MHz derived directly from the frequency standard. When the AFC is switched ON, the generator uses a 1 MHz signal derived from the afc board. The exact frequency of this signal is 1 MHz - $\Delta/34$ where Δ is the positive frequency error of the incoming carrier. The afc board accepts the 1.4 MHz carrier via the carrier filter, senses that an error is occurring, and adjusts the frequency of its 1 MHz output to correct this error.

80 The 1.4 MHz carrier appears at the input of the afc board after extraction from the main if signal via a 1.4 MHz carrier filter. The carrier is amplified, converted to 400 kHz by mixing with a 1 MHz signal and amplified again, resulting in a 400 kHz square wave suitable for driving CMOS stages.

81 The square wave is applied to the input of the digital mixer. The mixer is clocked by two 200 kHz signals spaced 72° in phase (1/5 of a clock period). The mixer provides two outputs, one a square wave at the error frequency, the other dc up/down information which is a logic '1' for negative error, and a '0' for positive error, for example:

81.1 If the transmitter drifts 100 Hz high, the error output will be 100 Hz, and the output a '0'.

81.2 If the transmitter drifts 50 Hz low, the error output will be 50 Hz, and the up/down output a '1'.

The two outputs are fed to a 12-bit binary counter, which increments up or down at the error rate.

82 The ten most significant outputs (Q2 to Q11) are connected to a 10-bit digital-to-analogue converter, and the analogue output is used, after buffering and level shifting, as the varactor control voltage of a 7 MHz oscillator. The 7 MHz oscillator signal is divided down to 1 MHz, and applied to the 34 MHz board. Since the correction rate is proportional to the error frequency, the lock-up time is a logarithmic function of the initial error.

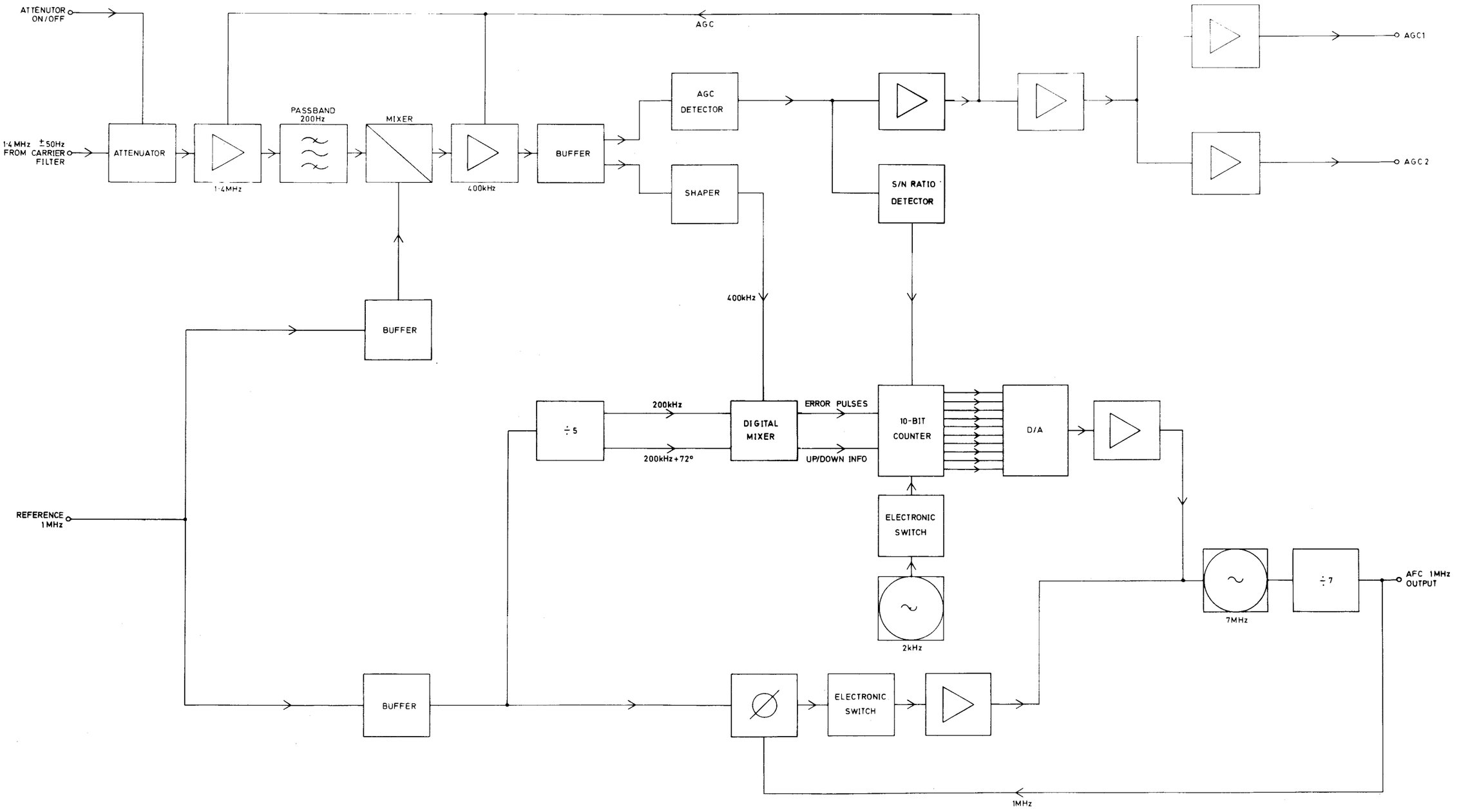


Fig.10

Simplified block diagram: afc board PM664

Chapter 1-3

SETTING-UP AND OPERATING PROCEDURES

CONTENTS

	Para.
Introduction	1
Preliminary setting up	2
Rear panel controls and connections	2
Initial switch-on	3
Tuning check	4
Functional check	5
Operating procedures	6
Function of controls	6
Receiver fitted with battery module MS.540	7
Receiver tuning	8
Setting-up procedure for LINE LEVEL controls	10

TABLES

No.		Page
1	Modes of reception	9

ILLUSTRATIONS

Fig.		Page
1	Location of controls and connectors	13

INTRODUCTION

1. This chapter contains the setting up and operating procedures for the RA.1772 receiver. It is assumed that the receiver has been correctly installed in its operating position.

PRELIMINARY SETTING-UP

Rear panel controls and connections

2. The connections to be made at the rear panel of the receiver, and the settings of the associated rear panel switches, are dependent upon the requirements of the particular installation. A brief description of each connection and switch is given below. A rear view of the receiver is given in fig. 1. Note that the receiver may have a battery module MS.540 fitted on the rear.

Identification	Function
POWER INPUT (receiver not fitted with battery module MS.540)	A three-pin socket (with associated 2 ampere fuse) for connection to the local source of power. DO NOT connect to this socket before ascertaining that the front-panel POWER switch is set to OFF and that the VOLTAGE SELECTOR has been correctly set.
POWER I/P (receiver fitted with battery module MS.540)	A three-pin socket (with associated 2 ampere fuse) on the side of the battery module (fig. 1) for connection to the local source of a.c. power. DO NOT connect to this socket before ascertaining that the front-panel POWER switch is set to OFF and that the VOLTAGE SELECTOR has been correctly set. CAUTION ... Initially, the BATTERY ON/OFF switch must be set to OFF (para. 7).
	Note ... Check that the POWER O/P lead from the 12V battery module is connected to the receiver POWER INPUT socket, and that the two flying leads are connected to the STD/+12V (red lead) and +12V (orange lead) terminals of TS2 on the rear panel of the receiver.
BATTERY ON/OFF (battery module MS.540)	This switch is set to ON when the standby 12V facility is required; refer to para. 7.
VOLTAGE SELECTOR	A selector plug which may be inserted in any one of twelve positions to cater for supply inputs in the range 100 to 125 volts or 200 to 250 volts. Note ... The supply voltage must remain within 10% of that selected since a low voltage will cause the internal regulation circuits to trip, and a high voltage will give rise to increased internal temperatures.
ANT 50 OHMS	A coaxial socket (with associated 500 mA fuse) for the connection of a 50 to 75-ohm unbalanced coaxial transmission line.
1 MHz IN/OUT socket and associated 1 MHz INT/EXT switch.	Accepts an external 1 MHz frequency standard when the associated 1 MHz switch is set to EXT, or provides a 1 MHz output when the switch is set to INT. A single receiver may be operated using an external frequency

Identification	Function
	standard or two receivers may be operated in the master/slave configuration, for diversity reception, using the frequency standard fitted to the master receiver.
LO IN/OUT socket and associated LO INT/EXT switch.	Accepts a local-oscillator signal (35.4 to 65.4MHz) when the associated switch is set to EXT (slave receiver), or provides a local oscillator output signal when the switch is set to INT (master receiver), where two receivers are interconnected for diversity reception.
34 MHz IN/OUT socket and associated 34 MHz INT/EXT switch.	Accepts a 34 MHz second mixer injection signal when the associated switch is set to EXT (slave receiver) or provides a 34 MHz output signal when the switch is set to INT (master receiver), where two receivers are interconnected for diversity reception.
MAIN IF OUTPUT	1.4 MHz i.f. output (u.s.b. or l.s.b., as selected at the MODE switch) for connection to external equipment. Nominal level 140 mV e.m.f. into 50 ohms. Note ... The sideband is inverted relative to the antenna input.
ISB IF OUT	1.4 MHz i.f. output (l.s.b. channel) for connection to external equipment. Nominal level 140 mV e.m.f. into 50 ohms. Note ... The sideband is inverted relative to the antenna input.
Terminal strip TS1:	
► 1) 2) LINE OUTPUT MAIN IF	Audio line output from main i.f. (u.s.b. or a.m., as selected at the MODE switch); 1 mW nominal into 600 ohms. Note that l.s.b. line output is obtained from TS1, pins 4 and 5. ◄
3 E	Earth.
4) 5) I.S.B. LINE OUTPUT	Audio line output from i.s.b./i.f. (l.s.b. channel; 1 mW nominal into 600 ohms.
6 LS	Audio output to external loudspeaker; u.s.b. or l.s.b., as selected at front panel MODE switch. 1 watt nominal into 8 ohms.
7 E	Earth.
8 NOT USED	
9 NOT USED	

	Identification	Function
Terminal strip TS2:		
1	DIV AGC	Diversity a.g.c. connection to second receiver for diversity reception.
2	E	Earth.
3	MUTE	An earth connection to this pin mutes the receiver at the r.f. stage; the a.f. stages are not muted.
4	NOT USED	
5	NOT USED	
6	+12V	+12V output (100 milliamps) for operation of the 12-volt battery module.
7	STD/+12V (and associated fuse)	+12V input from the battery module, for frequency retention purposes (para. 7).
8	DIV RL	Diversity relay. Not used but connected internally. (Not marked on fig. 1).
9	ISB DIV AGC	I.S.B. diversity a.g.c. connection to second receiver, for diversity reception.
Earth terminal:		For connection to the earthing system of the rack or cabinet.

INITIAL SWITCH-ON

3. (1) Set the rear panel 1 MHz, LO and 34 MHz INT/EXT switches to INT.

(2) Set the front-panel POWER switch to OFF.

(3) Ensure that the VOLTAGE SELECTOR (rear) is set to suit the local a.c. supply (para. 2).

(4) Connect the POWER I/P socket on the 12V battery module (rear) to the main source of a.c. supply.

(5) Set the BATTERY (rear) switch to ON.

(6) Set the POWER switch to ON.

CAUTION ...

It is essential that the receiver POWER switch is set to OFF before the receiver is disconnected from the main source of power. Refer to para.7.

(7) Check that the MHz dial glows and the kHz display reads 000.00. The OUT OF LOCK lamp may flash momentarily and should then remain extinguished.

(8) Set the METER switch, in turn, to +20, +15, +5 and -7; ensure that for each setting the meter indication is within the green sector of the meter scale.

TUNING CHECK

4. (1) Set the MHz switch to 3.

(2) Set the TUNING RATE switch to SLOW.

(3) Slowly spin the kHz control clockwise; the kHz display should increase in 10 Hz steps at a rate of 2.5 kHz per turn.

(4) Slowly spin the kHz control counter-clockwise; the kHz display should decrease in 10 Hz steps. As the display passes from 000.00 to 999.99, check that the lamp behind the 3 on the MHz dial extinguishes, and that the lamp behind the 2 illuminates.

(5) Continue to decrease the kHz display indication until it stops at 979.99.

(6) Turn the MHz control one position counter-clockwise; the illuminated 2 should move to the centre of the MHz scale.

(7) Spin the kHz control counter-clockwise; the kHz display should decrease from 979.99.

(8) Spin the kHz control clockwise; the kHz display should increase to 999.99, change to 000.00, and then stop at 020.00. As the display passes through 000.00, the lamp behind the 2 on the MHz dial should extinguish, and the lamp behind the 3 should illuminate.

(9) Turn the MHz control one position clockwise; the illuminated 3 should move to the centre of the MHz dial.

(10) Spin the kHz control clockwise; the kHz display should increase from 020.00.

(11) Set the TUNING RATE switch to FAST.

(12) Spin the kHz control in each direction in turn and check that the kHz display moves in 100 Hz steps at a rate of 50 kHz per turn. The '10 Hz' figure should remain stationary at 0.

(13) Set the TUNING RATE switch to LOCK.

(14) Spin the kHz control in each direction in turn and ensure that the kHz display indication does not vary.

Note ...

A mechanical damper is fitted to the tuning shaft and may be adjusted to the users preference (fig. 2 of Chap. 1-1).

OPERATIONAL CHECK

5. (1) Set the following controls as indicated:-

(a) AGC to SHORT

(b) AFC to OFF

(c) MODE to USB

(d) LOUDSPEAKER (LS) to ON

(e) IF GAIN fully clockwise

(f) AF GAIN fully counter-clockwise

(2) Turn the AF GAIN control progressively clockwise and check that the volume of white noise in the loudspeaker decreases.

(3) Set the AGC switch to OFF.

(4) Turn the IF GAIN control counter-clockwise and check that the noise in the loudspeaker decreases.

(5) Set the AGC switch to SHORT; the noise in the loudspeaker should be restored to the full level and the IF GAIN control should become inoperative.

(6) Set the AGC switch to LONG; the noise level in the loudspeaker should remain unchanged.

(7) Connect a suitable antenna to the receiver.

(8) Tune the receiver to a known signal and check for an acceptable audio output signal (refer to para. 6 for operating procedures).

OPERATING PROCEDURES

Function of controls

6. (1) RF TUNE: This is a 'front-end' tuning facility which is only used when the receiver is operated in close proximity to strong interfering signals. It is switched out of circuit when set to WB (wide-band).

(2) AGC: This is a three-position switch. In the OFF position the receiver gain is manually controlled (IF GAIN control); the selection of SHORT or LONG a.g.c. action is optional, dependent upon the operating mode and the propogation conditions. In either of these two positions, the IF GAIN control is inoperative.

(3) IF GAIN: See (2).

(4) TUNING RATE: A three-position switch. In the SLOW position, rotation of the kHz control alters the frequency in 10 Hz steps, whereas in the FAST position the frequency alters in 100 Hz steps. In the LOCK position, the receiver remains locked to the displayed frequency and the kHz control becomes inoperative.

(5) BFO: A slow-motion b.f.o. tuning control which provides a variable offset of up to approximately plus or minus 3 kHz relative to a signal offset by 1 kHz in the upper sideband. The b.f.o. is switched on by setting the MODE switch to USB + BFO.

(6) MHz control: The MHz control switch, with associated dial, for selecting the MHz portion of the required operating frequency (0 to 29 MHz).

(7) kHz control: A continuously tunable kHz control with associated electronic digital display.

(8) MODE: This switch selects the mode of operation and has six operational positions, as described below. There is an 8 kHz symmetrical i.f. filter for the AM position of this switch, and 3 kHz sideband filters for the USB and LSB positions.

ISB-L: I.S.B. (A3B) reception with the lower sideband audio output monitored at the two PHONES

sockets, the internal loudspeaker and the loudspeaker terminal on the rear panel.

ISB-U: I.S.B. (A3B) reception with the upper sideband audio output monitored at the two PHONES sockets, the internal loudspeaker and the loudspeaker terminal on the rear panel.

LSB: Single sideband (A2H, A2J, A3A, A3H, A3J) operation with the lower sideband selected. The l.s.b. audio output is available at the two PHONES sockets, the internal loudspeaker and the loudspeaker terminal on the rear panel.

USB: Single sideband (A2H, A2J, A3A, A3H, A3J) operation with the upper sideband selected, and a choice of bandwidths selected by the USB BANDWIDTH switch; two offset filters are provided for the A2 modes. A1 (c.w.) possible with the receiver tuning offset to provide suitable beat frequency. The u.s.b. audio output is available at the two PHONES sockets, the internal loudspeaker and the loudspeaker terminal on the rear panel.

USB + BFO: For A1, A2H and A2J modes, otherwise the facilities are as for USB.

AM: Double sideband a.m. (A2, A3) operation.

(9) USB BANDWIDTH: One of three i.f. filters may be selected; a 3 kHz filter for voice (or with b.f.o. telegraphy) reception; a 400 Hz or a 1.2 kHz filter, offset by 1 kHz, for telegraphy reception. The switch is only in circuit for the USB and USB + BFO positions of the MODE switch.

(10) POWER ON/OFF: See CAUTION (para. 3).

(11) AF GAIN: The a.f. gain control is used to adjust the audio level to the headphones, the internal loudspeaker and also the externally connected loudspeaker. Note that when the right-hand PHONES socket is used, the built-in loudspeaker is muted.

(12) AFC: For use with A3A, A3B and A3H operating modes, and is a three-position switch:

Up: FULL CARRIER (A3H)
Centre: OFF
Down: PILOT CARRIER (A3A or A3B)

An associated LOCK lamp glows when the a.f.c. is in operation and a carrier signal is present. The front panel meter includes an AFC scale. When the METER switch is set to TUNE CARRIER and the AFC switch is set to OFF, the meter provides an indication of receiver tuning. When the AFC switch is set to FULL or PILOT CARRIER (as appropriate) the meter provides an indication of available 'hold' range. It may, therefore, be used

		to determine whether a slight adjustment of the receiver tuning is required (due to a drift in the transmitted frequency) to maintain a.f.c lock.
(13)	METER:	This switch has nine positions, as described below.
	TUNE CARRIER:	For accurate tuning of full or pilot carrier signals, used in conjunction with the AFC switch.
	RF:	R.F. level indication, for general tuning purposes.
	LSB:	L.S.B. audio output level to the ISB LINE OUTPUT terminals.
	AM/USB:	A.M./U.S.B. audio output level to the MAIN IF LINE OUTPUT terminals.
	DRIVE LEVEL:	First mixer local-oscillator drive level.
	+20) +12) +5) -7)	Rail voltage monitoring.
(14)	LOUDSPEAKER ON/OFF	Internal loudspeaker switch
(15)	LINE LEVEL	Two preset controls are provided, one for the a.m./u.s.b. channel, and one for the l.s.b. channel (i.s.b. operation). The setting-up procedures for these controls are given in para. 10.

Receiver fitted with battery module MS.540

7. When the receiver POWER switch is set to ON, and the BATTERY ON/OFF switch on the battery module is at ON, a nickel-cadmium battery (within the battery module) is connected to a charging circuit. In the event of a momentary mains failure or a severe mains transient, the stored receiver tuning (kHz) information is retained and unaffected because the nickel-cadmium battery sustains the d.c. supply to the appropriate stages within the receiver.

CAUTION ...

If, while the receiver POWER switch is set to ON, the mains supply voltage is disconnected from the battery module (or the relevant mains supply socket), the nickel-cadmium battery will fully discharge in approximately 30 minutes; approximately 3 hours are required to fully recharge the battery. In this event, the tuning memory-retention facility will not be available for most of the recharging period.

WARNING ...

LETHAL VOLTAGES EXIST WITHIN THE BATTERY MODULE. DISCONNECT THE SUPPLY TO THE POWER I/P SOCKET AND SET THE BATTERY SWITCH TO OFF BEFORE REMOVING THE COVER.

Receiver tuning

8. The following procedure is given as a general guide to the correct use of the controls. Table 1 summarises the appropriate settings of the MODE and USB BANDWIDTH switches for the available modes of reception.

TABLE 1

Modes of reception

USB BANDWIDTH	MODE					
	ISB-L	ISB-U	LSB	USB	USB+BFO	AM
0.8 - 1.2.		A2H & J		A1* A2H & J	A1* A2H & J	
0.4 - 1.6		A2H & J		A1* A2H & J	A1* A2H & J	
0.3 - 3		A3B		A1** A2H & J A3A, H & J	A1** A2H & J	
Switch ineffective	A3B		A1** A2H & J A3A, H & J			A2 A3
Remarks	Built-in audio monitoring of lower sideband	Built-in audio monitoring of upper sideband	Pitch of A1 tone fixed	Pitch of A1 tone fixed	Pitch of A1 tone variable by b.f.o.	

* Receiver off-tuned by 1 kHz.

** Receiver off-tuned, in appropriate direction, by at least 300 Hz.

9. (1) Connect a pair of headphones to either of the two front-panel PHONES jacks. Alternatively, set the internal loudspeaker switch to ON.

Note ...

The internal loudspeaker is rendered inoperative when the right-hand PHONES jack is in use.

(2) Set the POWER switch to ON.

(3) Set the AGC switch as follows:-

(a) to OFF for hand-speed telegraphy reception; set the IF GAIN as appropriate.

Note ...

If preferred, the AGC switch may be set to LONG for telegraphy reception.

(b) to SHORT for a.m. reception (with carrier).

(4) Set the MODE switch as required (Table 1).

(5) For the USB + BFO position of the MODE switch (Table 1), set the USB BANDWIDTH switch to either 0.4 - 1.6 or 0.8 - 1.2.

Note ...

These positions of the USB BANDWIDTH switch enable reception of telegraphy transmissions which are offset by 1 kHz towards the upper sideband.

(6) For telegraphy reception (A2H, A2J), set the BFO control, initially, to about $1\frac{1}{2}$ divisions from '0'.

(7) Set the RF TUNE control to WIDEBAND.

(8) Set the AF GAIN control to an approximate mid-position.

(9) Set the MHz switch to indicate the required frequency on the MHz dial.

(10) Set the TUNING RATE switch to FAST and spin the kHz control until the desired frequency is approached, then set the TUNING RATE switch to SLOW.

(11) Adjust the kHz tuning to identify the required signal.

(12) If a.f.c. operation is desired, set the METER switch to TUNE CARRIER. Carefully tune the kHz control to the pilot carrier; the meter indication will decrease in level to '0' and then show a slow 'beat' as the receiver is brought into tune. Set the AFC switch to either FULL CARRIER(A3H) or PILOT CARRIER (A3J).

(13) When the AFC switch is operated, check that the AFC LOCK lamp is glowing when receiving A3A or A3H transmissions. If the signal fades, the AFC LOCK lamp may flash intermittently.

(14) When the AFC switch is in either the FULL or PILOT CARRIER position, check periodically that the AFC meter indication (METER switch at TUNE CARRIER) has not drifted to the extreme '+' or '-' end of the AFC scale. This would be caused by drift in the transmission frequency, and is corrected by adjusting the kHz tuning control (in 10 Hz steps) until the indication is nearer the '0' on the AFC scale; this adjustment must be carefully carried out so as to maintain illumination of the AFC LOCK lamp.

(15) Set the TUNING RATE switch to LOCK.

(16) For the USB + BFO mode, adjust the BFO control as required.

Note ...

The BFO control may also be used to read a weak c.w. signal in the presence of a strong signal by tuning the strong signal for zero beat on the meter.

(17) Adjust the AF GAIN control for optimum clarity and level of output.

(18) If interference of a certain type is experienced (e.g. cross-modulation), an improvement might be obtainable by adjusting the RF TUNE control to obtain maximum wanted signal level.

SETTING-UP PROCEDURE FOR LINE LEVEL CONTROLS

10. (1) Set the following controls as indicated:

(a) POWER switch to ON.

(b) AFC switch to OFF.

(c) MODE switch to USB.

(d) USB BANDWIDTH switch to 0.4 to 1.6.

(e) AGC switch to OFF.

(f) IF GAIN fully clockwise.

(g) METER switch to AM/USB.

(2) Connect a 600-ohm load across the MAIN IF LINE OUTPUT terminals (TS1, pins 1 and 2) on the rear panel.

(3) Connect the c.w. output from a signal generator, set to a frequency of 3.5 MHz and an output of 2 uV e.m.f., to the receiver antenna socket.

(4) Set the receiver tuning controls for a frequency of 3.5 MHz,. and search until the signal is heard in the loudspeaker or phones.

(5) Precisely adjust the receiver kHz tuning for a maximum indication on the front-panel meter.

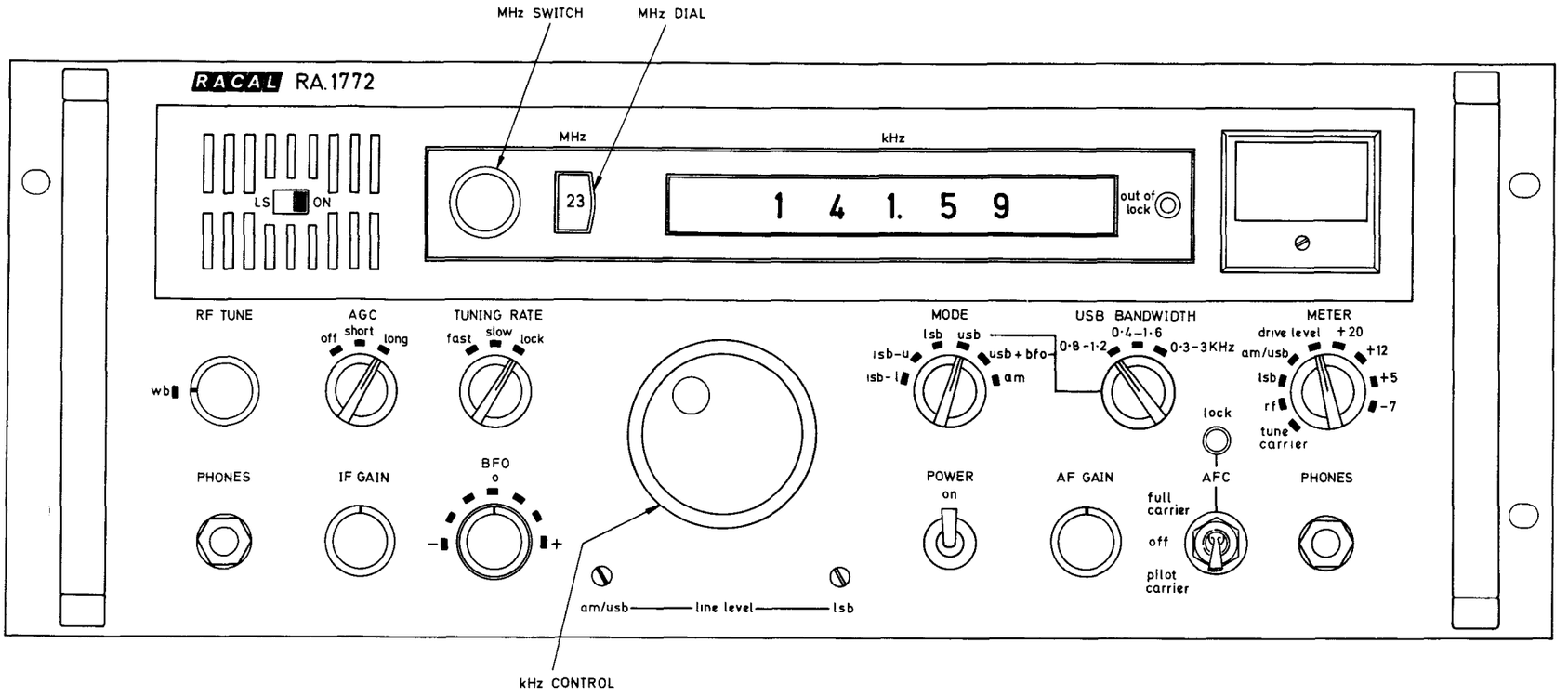
(6) If the level is being adjusted for connection to British G.P.O. lines, set the generator output to 200 mV e.m.f.

(7) Using a thin-bladed screwdriver, adjust the AM/USB LINE LEVEL control for a 1 mW audio output level, as indicated by the red line on the upper scale of the meter.

(8) Repeat the above procedure for the adjustment of the LSB LINE LEVEL control but set the MODE switch to LSB, the METER switch to LSB and transfer the 600-ohm load to the ISB LINE OUTPUT terminals (TS1, pins 4 and 5).

(9) Switch off and disconnect the signal generator.

(10) Remove the 600-ohm load.



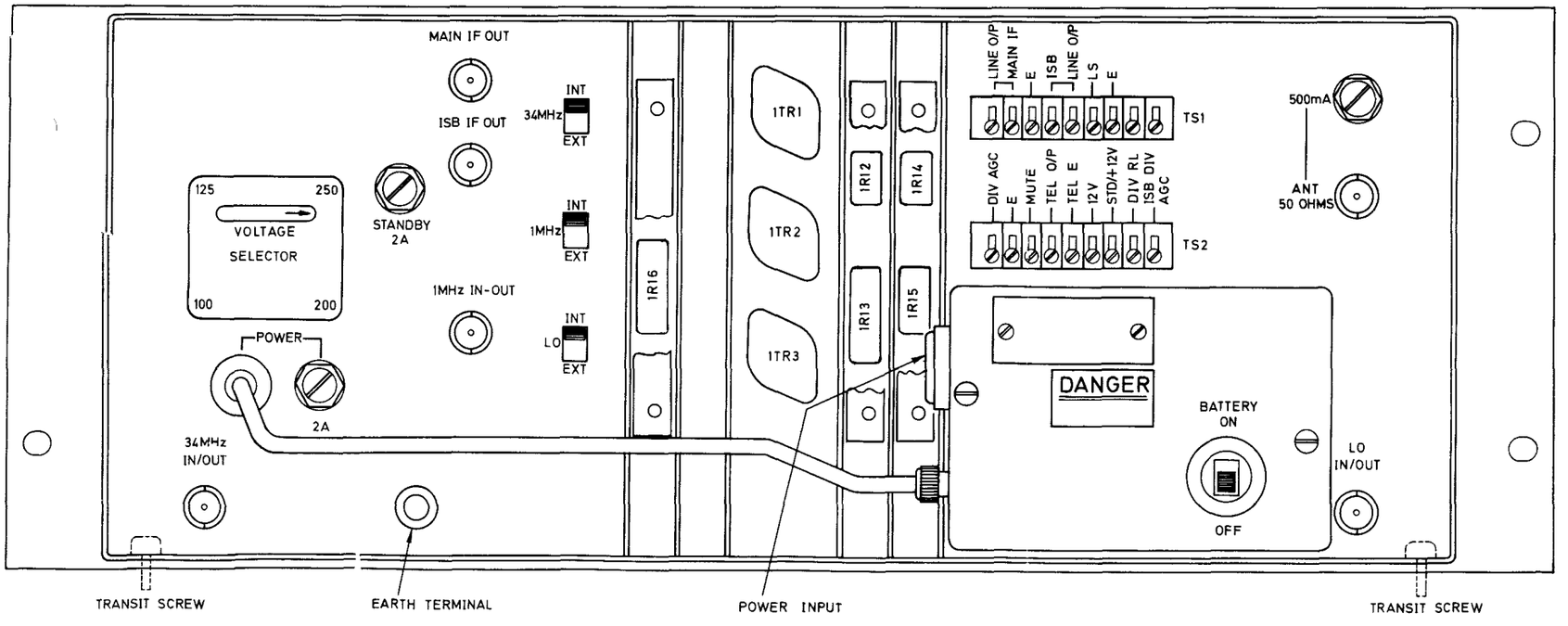


Fig 1

Location of controls & connectors

Issued Feb. 76

Chapter 2-1

DETAILED CIRCUIT DESCRIPTION

CONTENTS

	Para.
Logic board PS365	1
Optical shaft encoder	4
Display board PM371	5
Fast tuning mode	9
Slow tuning mode	10
Tuning lock	11
Up/down counters	12
Range blanking	16
Overspill	17
Out-of-lock detector	24
Frequency standard 9420	26
34MHz generator board PM339	28
34MHz oscillator	29
Divide-by-34 stage	31
1MHz divider	32
Phase comparator	35
1.4MHz generator	42
Low-frequency loop board PM588	46
6-7MHz voltage controlled oscillator	47
Programmed divider N1	48
Reference frequency divider	54
L.F. loop phase comparator	55
L.F. loop lock detector	60
Programmed divider N2	62
Mixer stage	67
Lower transfer loop phase comparator	68
Lower transfer loop lock detector	73
Upper loop board PM589	74
Lower transfer loop v.c.o.	75
Upper loop v.c.o./shaper	78
Programmed divider N2	79
Range blanking	84
Fixed divider	86
Phase comparator	87
Lock detector	92
Lock indicator	93
Transfer loop board PS338	94
Programmed divider N3	96
Mixer	102
Phase comparator	103
Lock indicator and fast lock circuit	108
High-frequency loop board PS337	113
Upper transfer loop oscillator	114
H.F. loop oscillators	117
Oscillator output buffer stages	120
Programmed divider N3	122
Phase comparator	129
Lock indicator and fast lock circuit	134
R.F. unit; including r.f. board PM582	139
Re-radiation filter	140
Wideband protection stage	141
Mute control	143
R.F. signal path	144

	Para
Protection stage	146
Wideband r.f. amplifier	148
First mixer board PM335	149
Drive amplifier	152
Mixer	154
Second mixer board PM336	155
PIN diode attenuator	157
Mixer	159
I.F. filter board PS367	160
Main i.f./a.f. board PM364/1	163
A.G.C. detector and amplifier stage	165
Hang detector	167
A.M. and s.s.b. detectors	172
Audio pre-amplifier	176
Audio line amplifier	177
Loudspeaker amplifier	178
I.S.B./i.f./a.f. board PM364/3	180
A.F.C. board PM369	181
Input attenuator and amplifier	181
Mixer	183
1.6MHz v.c.o.	184
Phase-comparator	185
A.G.C. stages	190
Signal-to-noise ratio-detector	193
Divide-by-16 stage	194
Divide-by-40 stage	195
Digital phase-comparator	196
Loop filter and amplifier	201
7 MHz v.c.o.	204
Divide-by-7 stage	205
Carrier tuning indicator	208
A.F.C. lock detector	210
A.F.C. on/off switching	216
Meter switching board PS419	226
Power supplies	228
Supply input filter	229
Regulator board PM370	230
-7V regulator	232
+5V regulator	233
+12V regulator	234
+20V regulator	235
A.F. and memory regulator board PS427/1	236
14.5V regulator	237
Memory supply	238
12V Battery module MS450	241
Oscillator	242
Supply detector	243
Electronic switch	244

TABLES

No.		Page
1	MHz switch-wafer SA1	4
2	MHz switch-wafer SA2	5
3	Code conversion	32
4	Programmed divider operation (PS338)	32
5	H.F. loop oscillator selection	36
6	H.F. loop oscillators	36
7	Programmed divider operation (PS337)	38

ILLUSTRATIONS

Fig.		Page
1	Timing diagram : fast tune mode	7
2	Timing diagram : up/down counter (display board)	9
3	Block diagram : 34MHz generator board PM339	13
4	Timing diagram : divide-by-34 stage	14
5	Timing diagram : phase-comparator	16
6	Timing diagram : strobe-pulse generation (l.f. loop PM588) ...	19
7	Timing diagram : lock detector	21
8	Timing diagram : strobe-pulse generation (lower transfer loop)	22
9	Block diagram : low frequency loop board PM588	25
10	Block diagram : upper loop board PM589	29
11	Timing diagram : fast-lock and indicator (upper transfer loop PS338)	34
12	Timing diagram : strobe-pulse generation (h.f. loop PS337) ...	38
13	Timing diagram : fast-lock and indicator (h.f. loop PS337) ...	41
14	Block diagram : upper transfer and h.f. loops PS338 and PS337	43
15	Waveform diagram (idealised) : a.g.c. hang detector	49
16	Timing diagram : sample-hold phase comparator (a.f.c. board PM369)	50
17	Timing diagram : digital phase-comparator (a.f.c. board PM369)	54
18	Timing diagram : lock-detector monostable (a.f.c. board PM369)	57
19	Timing diagram : 7MHz v.c.o. lock detector (a.f.c. board PM369)	58
20	Equivalent circuit : voltage regulator i.c.	62
21	Logic board PS365 : component layout	68
22	Logic board PS365 : circuit	69
23	Optical shaft encoder : component layout and circuit	70
24	Display board PM371 : component layout	71
25a	Display board PM371 : circuit (sht. 1)	72
25b	Display board PM371 : circuit (sht. 2)	73
26	Frequency standard assembly 9420	74
27	34MHz generator board PM339 : component layout	75
28a	34MHz generator board PM339 : circuit (sht.1)	76
28b	34MHz generator board PM339 : circuit (sht.2)	77
29	Low frequency loop board PM588 : component layout	78
30	Low frequency loop board PM588 : circuit	79
31	Upper loop board PM589 : component layout	80
32	Upper loop board PM589 : circuit	81
33	Transfer loop board PS338 : component layout	82
34	Transfer loop board PS338 : circuit	83
35	High frequency loop board PS337 : component layout	84
36	High frequency loop board PS337 : circuit	85
37	Re-radiation filter : component layout and circuit	87
38	R.F. board (tuned) PM582 : component layout	88
39	R.F. board (tuned) PM582 : circuit	89
40	First mixer board PM335 : component layout	90
41	First mixer board PM335 : circuit	91
42	Second mixer board PM336 : component layout	92
43	Second mixer board PM336 : circuit	93
44	I.F. filter board PS367 : component layout	94
45	I.F. filter board PS367 : circuit	95
46	Main i.f./a.f. board PM364/1 : component layout	96
47	I.S.B./I.F./A.F. board PM364/3 : component layout	97
48a	I.F./A.F. board PM364 : circuit (sht.1)	98
48b	I.F./A.F. board PM364 : circuit (sht.2)	99
49	A.F.C. board PM369 : component layout	101
50a	A.F.C. board PM369 : circuit (sht.1)	102
50b	A.F.C. board PM369 : circuit (sht.2)	103

Fig.		Page
51	Meter switching board PM419: component layout	104
52	Meter switching board PM419: circuit	105
53	Regulator board PM370: component layout	106
54	Power supply (including regulator board (PM370): circuit ...	107
55	AF and memory regulator board PS427/1: component layout ...	108
56	AF and memory regulator board PS427/1: circuit	109
57	Battery module MS450: component layout	110
58	Battery module MS450: circuit	111
59	Retention of frequency-setting information: supply flow diagram	113
60	Chassis front and rear: component layout	114
► 60a	Chassis rear: capacitor layout (Post Mod TC 0024)	114a ◄
61a	Receiver interconnection diagram (sht.1)	115
61b	Receiver interconnection diagram (sht.2)	116
61c	Receiver interconnection diagram (sht.3)	117

Annex

A	AFC board: PM664
B	2nd mixer board PM336: alternative version
C	IF/AF board PM674
D	Optical shaft encoder: alternative version

LOGIC BOARD PS365 (fig.22)

1 The logic board contains the front-panel-operated MHz switch, numerous steering diodes and eight buffer AND gates. It provides MHz frequency and range information for a number of circuits within the receiver.

2 The MHz switch has three wafers. wafer SA1 provides frequency range information for the rf unit (board pins 26 to 32) and the first mixer board (board pins 2 and 3); wafer SA2 provides MHz frequency setting information in nines-complement coded form for the programmed dividers of the upper transfer loop PS338 and the hf loop PS337 (board pins 7 to 14), whereas wafer SA3 provides oscillator selection information for the hf loop (pins 4,5 and 6).

3 The outputs controlled by wafers SA1 and SA2 are given in Tables 1 and 2 respectively. The wiper of wafer SA3 is connected to the LO INT/EXT switch. When this switch is set to INT, an earth (0V) is applied via SA3 to board pin 4 (01 output) for MHz switch settings from 0 to 7 inclusive, to board pin 6 (02 output) for settings from 8 to 17 inclusive or to board pin 5 (03 output) for settings from 18 to 28 inclusive, to select the appropriate oscillator. When the LO switch is set to EXT, the wiper of SA3 is open-circuited and all three oscillators on the hf loop board are switched off.

TABLE 1 MHz SWITCH-WAFER SA1

MHz switch setting	Board pin numbers								
	2	3	26	27	28	29	30	31	32
0		0						0	
1		0					0		0
2 - 3		0				0			0
4 - 7	0				0				0
8 - 14	0			0					0
16 - 29	0		0						0

TABLE 2

MHz switch-wafer SA2

MHz switch setting	Board pin numbers								Decimal
	10	9	8	7	14	13	12	11	
00	1	0	0	1	1	0	0	1	99
01	1	0	0	0	1	0	0	1	98
02	0	1	1	1	1	0	0	1	97
03	0	1	1	0	1	0	0	1	96
04	0	1	0	1	1	0	0	1	95
05	0	1	0	0	1	0	0	1	94
06	0	0	1	1	1	0	0	1	93
07	0	0	1	0	1	0	0	1	92
08	0	0	0	1	1	0	0	1	91
09	0	0	0	0	1	0	0	1	90
10	1	0	0	1	1	0	0	0	89
11	1	0	0	0	1	0	0	0	88
12	0	1	1	1	1	0	0	0	87
13	0	1	1	0	1	0	0	0	86
14	0	1	0	1	1	0	0	0	85
15	0	1	0	0	1	0	0	0	84
16	0	0	1	1	1	0	0	0	83
17	0	0	1	0	1	0	0	0	82
18	0	0	0	1	1	0	0	0	81
19	0	0	0	0	1	0	0	0	80
20	1	0	0	1	0	1	1	1	79
21	1	0	0	0	0	1	1	1	78
22	0	1	1	1	0	1	1	1	77
23	0	1	1	0	0	1	1	1	76
24	0	1	0	1	0	1	1	1	75
25	0	1	0	0	0	1	1	1	74
26	0	0	1	1	0	1	1	1	73
27	0	0	1	0	0	1	1	1	72
28	0	0	0	1	0	1	1	1	71
29	0	0	0	0	0	1	1	1	70

OPTICAL SHAFT ENCODER (fig. 23)

4. The shaft encoder is an optical displacement transducer of the incremental type. A graticule, of a transparent material with opaque stripes, is attached to the encoder spindle and is made to rotate between a pair of lamps and a pair of photo-transistors. As the graticule rotates, the photo-transistors are alternately darkened and illuminated, thereby producing two sinusoidal output waveforms at pins 3 and 1 of the sensor board. The two photo-transistors are physically displaced such that these two output waveforms are 90° out of phase, with output A leading output B for one direction of rotation and lagging output B for the reverse direction of rotation. The two outputs, preset by potentiometers R1, R2, are fed to the display board from pins 4 (output A) and 10 (output B) of the potentiometer board.

DISPLAY BOARD PM371 (fig. 25)

5. The display board consists of a reversible counter chain and associated digital display which provides 100kHz, 10kHz, 1kHz, 100Hz and 10Hz frequency setting information, in BCD form, for the programmed dividers of the l.f., lower transfer and upper phase-locked loops (PM588 and PM589).

6. The A output signal from the shaft encoder, at board pin 32, is applied to a shaper stage, TR2, and a Schmitt-triggered NAND gate, G1. The B output signal from the shaft encoder is applied to a similar circuit comprising TR3 and G2. The square-wave output from G1, at ML27 pin 8, is applied to three monostables, ML28a, ML28b, and ML33a; ML33a is used to inhibit the out-of-lock detector (para.25).

7. ML28a and ML28b are retriggerable monostables. With this type of device, a positive edge applied to the B input (pin 2) of ML28a will trigger the monostable since the A input (pin 1) is held at logic '0' (0V). When the monostable is triggered, the Q output (pin 13), which is normally at logic '0', will pulse to logic '1' for a period of time determined by the timing components (C7, R11) connected to C (pin 14) and R (pin 15); in this case, the period is approximately 7 microseconds. A logic '0' applied to the clear input CL (pin 3) overrides both the A and B inputs to ML28a and resets the Q output to logic '0'. ML28b functions in the reverse manner. A negative edge applied to the A input (pin 9) will trigger the monostable since the B input (pin 10) is held at logic '1' (approximately +5V); again, a 7 microsecond output pulse is produced.

8. The positive going output pulses from ML28b and ML28a (in the fast tune mode only, para.9) are applied to a series of pulse steering NAND gates, G4 to G11. Also applied to these gates is the square-wave output from G2 (ML27 pin 6) together with the inverted output, via G3 (ML17 pin 8).

Fast tuning mode

9. Figure 1 is a timing diagram for the fast-tune mode. When the fast tuning mode is selected (at the front panel), an earth (0V) is applied to board pin 29. This is routed to two OR gates, G13, G14, and also to an inverter, NAND gate G12. The resultant logic '1' output from G12, at ML8 pin 12, is applied to the clear inputs (CL) of monostable ML28a and the 10Hz up/down counter, ML6. As stated in para.7, a logic '0' is required to clear ML28a and the monostable is therefore enabled. ML6 however, is cleared and under this condition the + and - outputs, at pins 12 and 13, are forced to logic '1', thereby opening AND gates G16 and G17 for positive-going output pulses from either of the two OR gates, G13, G14. Thus in the fast tune mode, positive-going pulses are produced from both ML28a (positive edge triggered) and ML28b (negative edge triggered) by the square-wave output from G1, whilst ML6 is inhibited. In this mode, one revolution of the shaft encoder spindle produces 500 pulses, i.e. a tuning rate of 50kHz per turn.

Slow tuning mode

10. The earth is removed from board pin 29 when the slow tuning mode is selected; the +5V memory supply (A) is applied via R16 to the two OR gates, G13, G14, and to the inverter, NAND gate G12. The resultant logic '0' output from G12 (ML8 pin 12) is applied to the clear inputs (CL) of monostable ML28a and the 10Hz up/down counter, ML6. Thus ML28a is cleared, the Q output is forced to logic '0' and this is inverted by gates G4 and G6 to open gates G8 and G9 for the outputs from G5 and G7. ML6 is enabled and the output pulses from ML28b, at a rate of 250 per revolution of the shaft encoder spindle, are applied to either the up or the down input of ML6 via G10 or G11. The slow tuning rate is equal to 2.5kHz per turn.

Tuning lock

11. When the tuning rate switch is set to the LOCK position, an earth (0V) is applied to board pin 30. This inhibits gates G10 and G11 and stops the counting action of the up/down counter chain, ML1 to ML6.

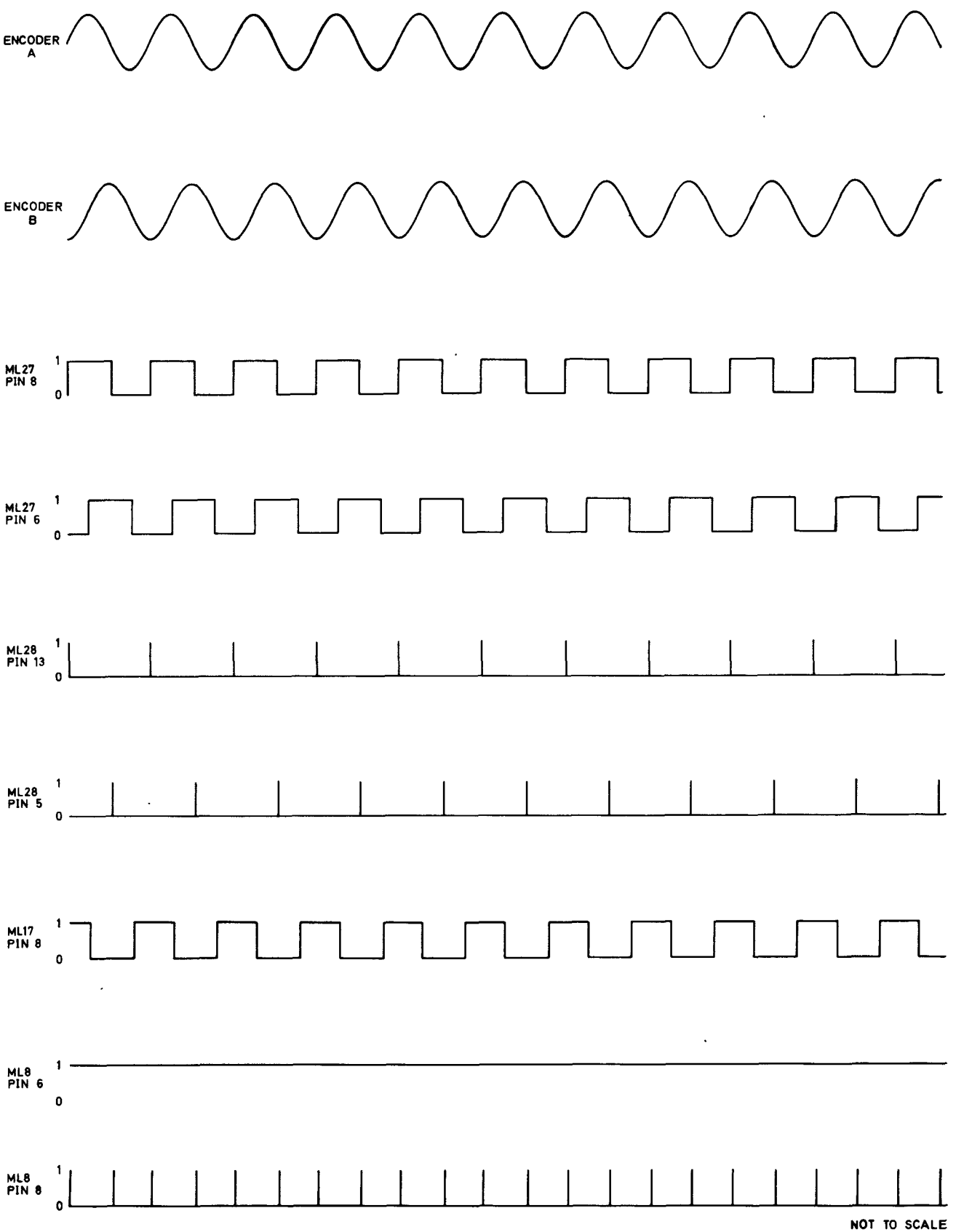


Fig.1 Timing diagram : fast-tune mode

Up/down counters

12. The output pulses from either G16 (up pulses) or G17 (down pulses) are applied to a chain of cascaded up/down BCD counters, ML1 to ML6. Each counter is triggered by a low-to-high level transition of either count input, and the direction of counting is determined by which count input is pulsed while the other count input is at logic '1'.

13. A logic '0' load-pulse is provided by TR4 when the receiver is first switched on. The memory +5V supply, at board pin 23, charges capacitor C27; TR4 conducts and effectively connects the load input of each counter to the 0V rail. Capacitor C27 discharges via R23 and TR4 is subsequently turned off.

14. The load pulse presets each counter to zero by transferring the 0V (logic '0') at the input pins (A, B, C, D) to the corresponding output pins (QA, QB, QC, QD). Thus the kHz portion of the receiver frequency is reset to zero each time the +5V memory supply is interrupted i.e. each time the receiver is switched on or following an interruption in the main source of a.c. power. To prevent this loss of frequency-setting information, the external +12V battery module is connected to the rear panel STD/+12V terminal (para.241).

15. A timing diagram depicting the operation of a single up/down counter is given in fig.2. This diagram shows the following sequence:

(1) Load (preset) to zero.

(2) Count up to nine, carry, zero, one and two.

(3) Count down to zero, borrow, nine, eight and down to two.

Range blanking

16. A negative-going range blanking pulse is applied to the upper loop board (PM454) via board pin 27, each time a 9 - to - 0 or a 0 - to - 9 transition of the 10kHz digit occurs. The borrow (-) and carry (+) lines between ML4 and ML3 are connected to a two - input AND gate, G23. When a logic '0' borrow or carry pulse occurs (fig.2) the resultant logic '0' output from G23 triggers a monostable, ML33b, which produces a negative - going output pulse (duration approximately 23mS) at ML33b pin 12.

Overspill

17. The overspill circuitry comprises ML1, gates G26 to G32 inclusive and lamp switching transistors TR5, TR6 and TR7. It extends the tuning range of the selected 1MHz band by 20kHz at each end of the band. For example, if the MHz switch is set to, say, 5MHz, the receiver frequency range covered by the kHz tuning control is from 4.97999 to 6.0200MHz. For frequencies below 5.00000MHz, lamp 'L' illuminates numeral 4 and for frequencies above 5.99999MHz, lamp 'H' illuminates numeral 6.

18. Using the example frequency of 5MHz, for any kHz control setting between 5.00000 and 5.99999MHz, the QA output from ML1 will be at logic '0'. This is inverted by NAND gate G27 and TR6 conducts to complete the circuit for lamp 'N' via board pin 25.

19. When the kHz control setting passes beyond 5.99999 into the overspill region, a carry pulse from ML2, at pin 12, is applied to the UP input of ML1. The QA output, at ML1 pin 3, changes to logic '1' and this is applied to AND gate G29. The logic '0' QD output at ML1 pin 7, inverted by G28, is also applied to G29 and the resulting logic '1' output causes TR7 to conduct and switch on lamp 'H' via board pin 26.

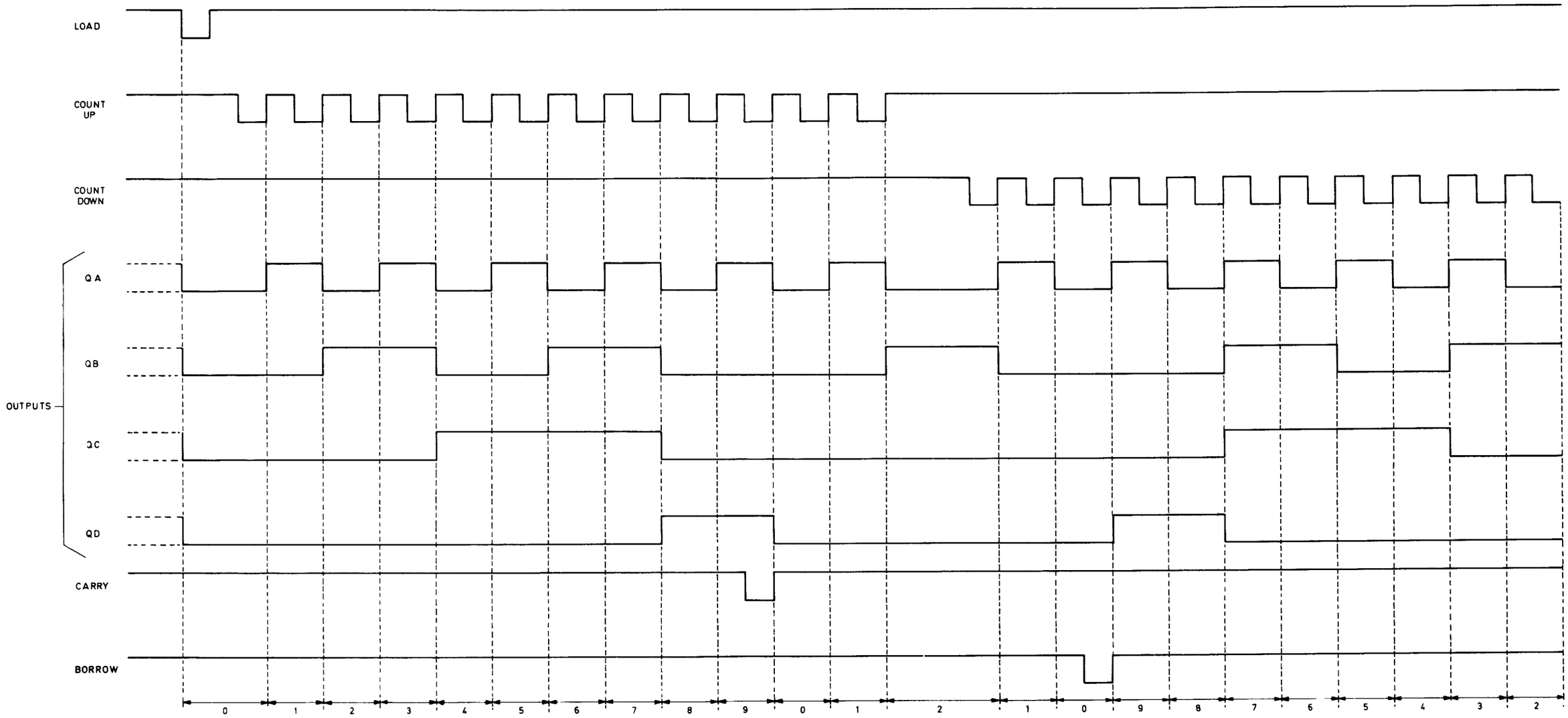


Fig.2

Timing diagram: up/down counter (display board)

20. The logic '1' output from G29 is also applied as one input to NAND gate G24. The second input to this gate is fed from the QB output from the 10kHz up/down counter, ML3. Thus when, in the overspill condition, ML3 reaches a count of binary 2, the QB output changes to logic '1', the output from G24 changes to '0' and the resultant '1' output from G10 stops the count-up sequence at 02000.

21. When the kHz control setting passes into the overspill region at the opposite end of the 1MHz band, i.e. settings below 5.00000MHz, a borrow pulse from ML2, at pin 13, is applied to the DN (down) input of ML1. This causes both the QA and the QD outputs, at ML1 pins 3 and 7, to change to logic '1' and lamp 'L' is illuminated via TR5 and board pin 24.

22. The logic '1' output at ML1 pin 7 is also applied as one input to NAND gate G25. The second input to this gate is fed from the QB output of the 10kHz up/down counter, ML3. Thus when, in the overspill condition, ML3 counts down to binary 7, the QB output changes to logic '1', the output from G25 changes to logic '0' and the resultant '1' output from G11 stops the count-down sequence at 97999.

23. Gates G26, G30, G31 and G32 are connected as a monostable to provide a positive going output pulse each time a '0' - to - '1' or a '1' - to - '0' transition occurs at its input. Pin 28 is fed from the A1 output at pin 7 of the logic board. With reference to Table 2, it can be seen that the logic level at pin 7 alternates as the switch is rotated. Thus each time the MHz switch is moved to an adjacent position, a logic level transition occurs at pin 28 of display board and a positive going pulse is applied to the clear (CL) input of ML1. When in the overspill condition therefore, the QA and/or the QD outputs are reset to logic '0' and lamp 'N' illuminates the numeral selected by the MHz switch.

Out-of-lock detector

24. The lock detector lines at board pins 33 (from PM589), 34 (from PS337) and 35 (from PS338) are applied to a diode OR gate, D1, D2, D3, and the out-of-lock lamp switching transistor, TR1. The collector of TR1 is taken to earth (0V) via D6 and board pin 40; pin 36 is connected to the out-of-lock lamp on the front panel.

25. ML33a is a re-triggerable monostable which inhibits the out-of-lock lamp switching transistor, TR1, whilst receiver tuning is in progress. The positive-going output pulse period is approximately 50mS.

FREQUENCY STANDARD 9420

26. The frequency standard assembly is mounted on a printed-circuit board (fig.26). No technical information is given in this publication because the assembly is a 4th-line repairable unit; in the event of failure, the unit is returned to the manufacturer. Chapter 2-5 contains a procedure for making an adjustment which corrects for the crystal ageing affect.

27. The supply for the unit is derived from the internally-generated +12V d.c.; refer to para.236 to 248 for further details.

34MHz GENERATOR BOARD PM339 (fig.28)

28. This board provides the 34MHz second mixer injection frequency; it also contains the 1.4MHz carrier re-insertion generator and the 1.4MHz BFO. A block diagram of the board is given in fig.3.

34MHz oscillator

29. The 34MHz oscillator stage, TR6, TR7, is controlled by the switching/voltage regulator transistor, TR1. With no earth applied to diode D1, TR1 conducts and provides a regulated +5V supply to the oscillator transistors. A sample of the oscillator output signal is fed to the buffer amplifier stage, TR3, TR5, and then, via the forward biassed switching diodes, D5 and D6, to a balanced output amplifier, TR11, TR12 and the rear panel 34MHz IN/OUT socket via board pin 22.

30. When the rear panel 34MHz INT/EXT switch is set to EXT (for slave operation), an earth is routed to D1, to switch off TR1 and thereby remove the +5V supply to the oscillator transistors, and also to the diode switch via L7. Diodes D5 and D6 are reverse biassed, diode D7 is forward biassed, and the 34MHz external input (from the master receiver) is routed via board pin 22, C34, D7 and C33 to the output amplifier, TR11, TR12.

Divide-by-34 stage (fig. 3)

31. A second output from the 34MHz oscillator is buffered by NAND gate G1 of ML2 before being applied to a divide-by-34 stage; this consists of a divide-by-two (ML4 CK1-A output) and a divide-by-17 stage (ML3, ML4 CK2-C output, G2 and G3). The 17MHz output from ML4 pin 5 is applied to the clock inputs of both halves of ML3 whilst the J1 input (ML3 pin 14) is held at logic '1' (+5V). The division factor of 17 is obtained by dividing the first 9 input clock pulses by three and the next 8 clock pulses by four. Thus for the first 9 clock pulses, 3 output pulses are produced (9 ÷ 3 = 3) and for the next 8 clock pulses, 2 output pulses are produced (8 ÷ 4 = 2), making a total of 5 output pulses for 17 input pulses. These 5 pulses are then divided by ML4 to produce a 3:2 mark-to-space ratio 1MHz squarewave output at ML4 pin 2. The operation of the divider is illustrated in fig. 4.

1MHz divider

32. The output from the 5MHz frequency standard, at board pin 27, is applied to a buffer amplifier, TR2, and then to a shaper stage, ML1, which is controlled by the rear panel 1MHz INT/EXT switch. When this switch is set to INT an earth is applied to board pin 16; this is routed to the reset (R9) inputs of ML1 (via L5) and enables the divider. The resultant 1MHz output from ML1 is amplified by TR9, and the filtered (C39, L9, C44) sinusoidal output is taken to the rear panel 1MHz IN/OUT socket, via board pin 4, and also to a shaper stage, TR13.

33. When the rear panel 1MHz INT/EXT switch is set to EXT, the earth is removed from the reset (R9) inputs of ML1 and the counter is inhibited. An external 1MHz signal (from a master receiver), applied to the rear panel 1MHz IN/OUT socket, is routed to the shaper stage, TR13, (via board pin 4) in place of the internally generated 1MHz signal.

34. The 1MHz squarewave output from TR13 is applied to ML7; this consists of four NAND gates which are used as buffers. The output from G8 at ML7 pin 6, is taken to the synthesizer, via board pin 6; the output from G9, at ML7 pin 11, is taken to the transfer loop, via board pin 8, and the output from G10, at ML7 pin 8, is taken to the phase comparator, via ML5. G11 of ML7, which has a controlling input from TR14, is used as part of the 1.4MHz carrier re-insertion generation circuit and is described in para. 43.

Phase comparator

35. The output signal from the 34MHz oscillator is divided to provide a

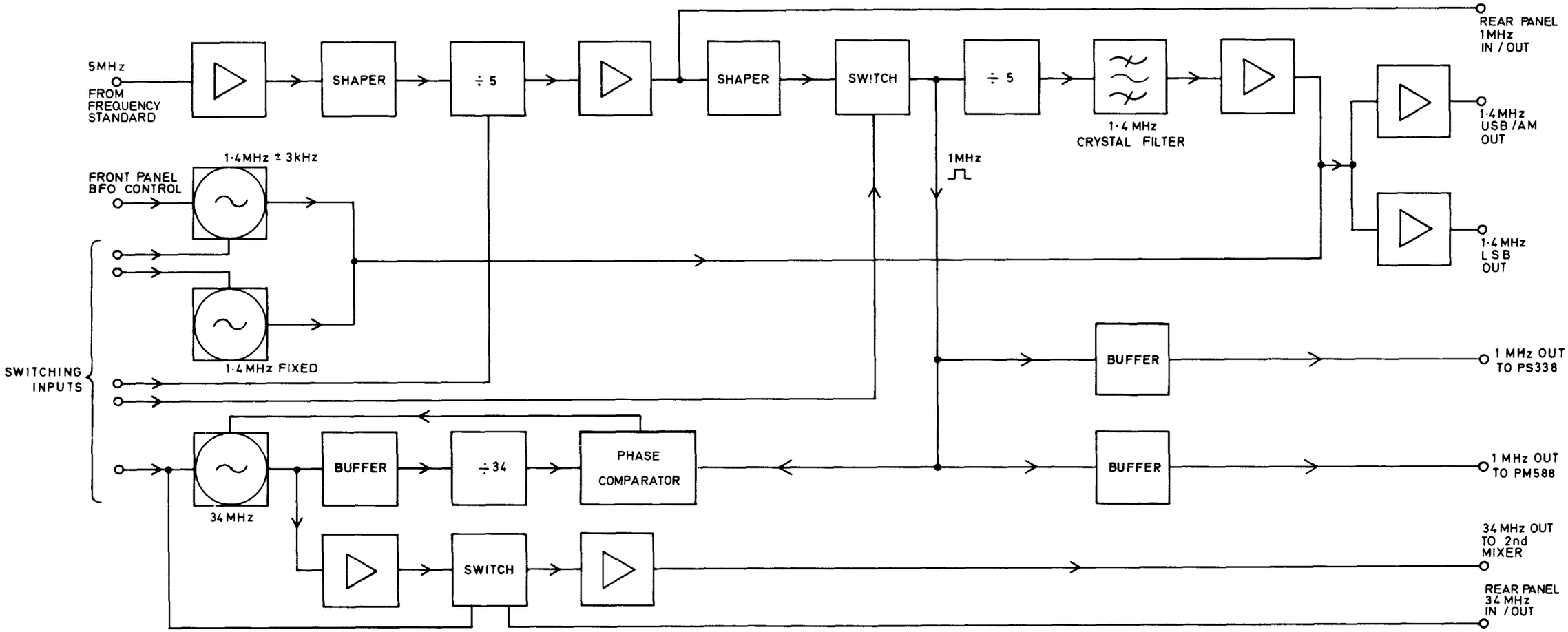
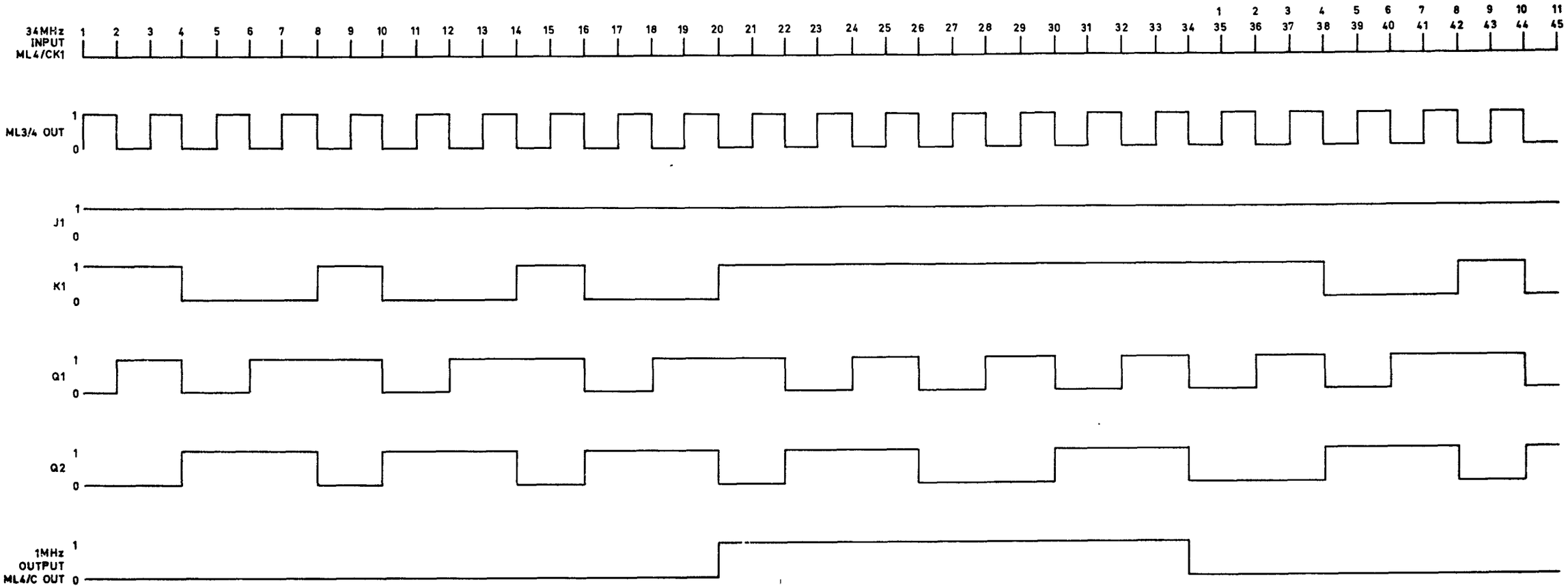
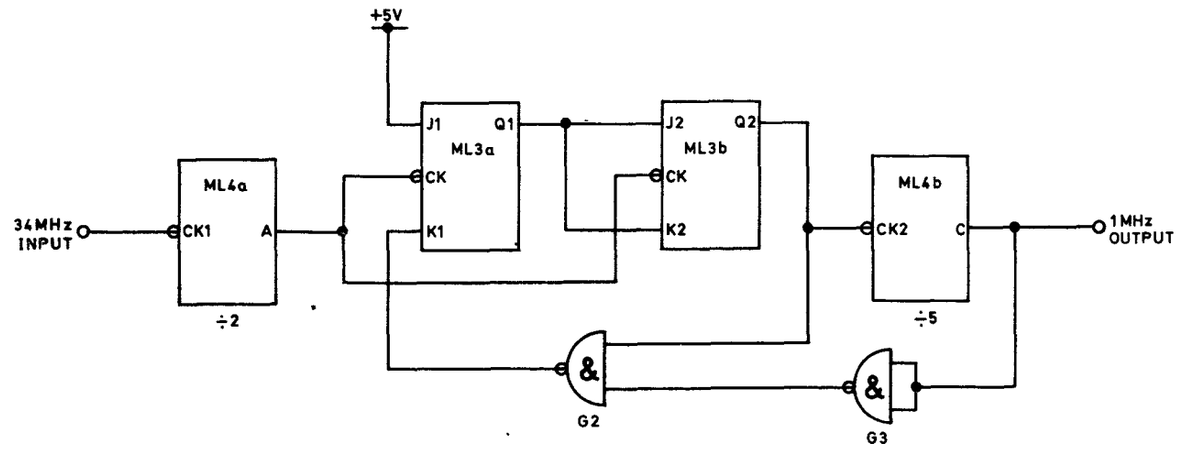


Fig. 3 Block diagram: 34 MHz generator board PM339





J-K Truth Table		
tn		tn + 1
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\bar{Q}n$

Fig. 4

Timing diagram: divide-by-34 stage

Fig. 4

frequency of 1MHz when the oscillator frequency is correct. This frequency is compared with a reference 1MHz frequency and any error between the two frequencies is used to develop a d.c. voltage which adjusts the oscillator frequency to eliminate the error. This voltage is generated in the phase comparator, and is applied to 34MHz oscillator varactor diode, D4, via L3.

36. The 1MHz reference frequency signal is derived either from the 5MHz frequency standard and 1MHz divider (ML7 pin 8) or within the a.f.c. board, connected to board pin 18. When a.f.c. is selected, an earth (logic '0') is applied to board pin 19. This is inverted by G6 of ML5 to open G7, and is also applied to G5 to open G4. The 1MHz signal at board pin 18 is now applied to the clock 1 input of ML6 (part of the phase comparator) via gates G7 and G4 of ML5. When a.f.c. is switched off, gates G5 and G4 are opened for the 1MHz reference frequency from ML7 pin 8.

37. The phase comparator consists of a dual D-type flip-flop, ML6, a two-input gate, G12 of ML2, and an output voltage control circuit, TR17, TR18, TR19. The action of the circuit is as follows.

38. The output from the divide-by-34 stage, at ML4 pin 12, is applied to the clock 1 input of ML6, whilst the reference frequency output, from ML5 pin 8, is applied to the clock 2 input of ML6. The D inputs to ML6 at pins 2 and 12, are both taken to the +5V rail (logic '1'). Thus when the positive edge from ML4 pin 2 clocks ML6, the Q1 output at pin 5 changes to '1' and the $\overline{Q1}$ output changes to '0'. Similarly, when the positive edge from ML5 pin 8 clocks ML6, the Q2 output changes to '1' and the $\overline{Q2}$ output changes to '0'. When both Q1 and Q2 are at '1', the output from the NAND gate, G12 of ML2, changes to '0', clearing both ML6 flip-flops via R74 and thus resetting the Q outputs to '0' and the $\overline{Q}$ outputs to '1'.

39. Consider the case where the 34MHz oscillator frequency is high. This will mean that the positive-going edge from the divide-by-34 stage will occur before the edge from the 1MHz reference frequency. The resultant setting and resetting of the flip-flops causes increased conduction of TR18, due to the $\overline{Q1}$ output waveform (fig.5) as compared with the conduction of TR19; this causes the voltage at the collector of TR18 to become less positive, thereby reducing the voltage applied to the varactor diode, D4, and reducing the oscillator frequency.

40. If the oscillator frequency is low, the divide-by-34 pulse will occur after the reference pulse, the $\overline{Q2}$ output waveform will cause increased conduction of TR19 and the voltage at the collector of TR18 will become more positive. The increased voltage applied to the varactor diode causes the oscillator frequency to increase, thus correcting the error.

41. When the two frequencies are in phase, the two flip-flops of ML6 are clocked at the same time; the $\overline{Q1}$ output waveform is equal to the $\overline{Q2}$ output waveform and the varactor line voltage remains constant.

1.4MHz generation

42. The 1.4MHz output signals at board pins 10 and 11 may be derived from the fixed-frequency carrier re-insertion generator, a beat frequency oscillator (b.f.o.) or a fixed offset 1.4MHz oscillator.

43. 1.4MHz carrier re-insertion generator. When a 1.4MHz carrier re-insertion output is required, an earth is connected to board pin 15; this is routed to the reset (Ro) inputs of a divide-by-five stage, ML8, via L11, and the divider is enabled. The earth is also routed to the base of TR14; the transisto:

switches off and a logic '1' is applied to the NAND gate, G11 of ML7, at pin 1 The gate opens and the 1MHz square-wave signal from TR13 is applied to the BD input of ML8. The resultant 200kHz output from ML8, at pin 8, is applied to a 1.4MHz crystal filter which selects the seventh harmonic of the input. The filter is followed by a two-stage amplifier, TR15, TR16, which feeds the two output amplifier stages, TR20, TR21.

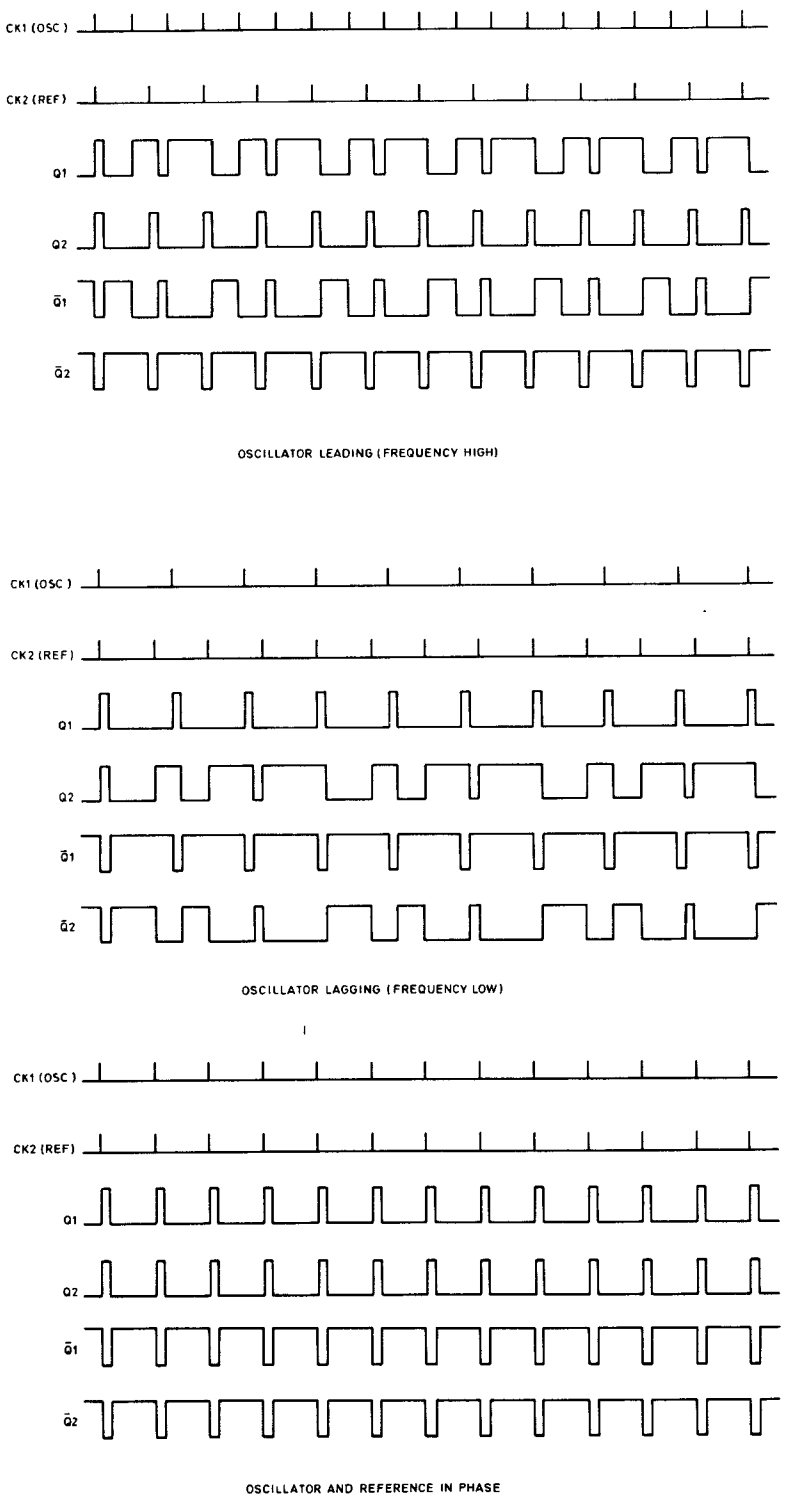


Fig.5 Timing diagram : phase comparator

44. B.F.O. The b.f.o. is selected by applying an earth to board pin 14; this completes the circuit for transistor TR8 which, with associated components, forms a 1.4MHz ± 3kHz oscillator. The front panel b.f.o. control (a potentiometer), which is connected to board pins 23, 24 and 25, controls the voltage applied to the varactor diode, D3, and hence the oscillator frequency. The b.f.o. output signal is coupled by C30 to the two output amplifier stages, TR20, TR21, and the amplified outputs appear at board pins 10 and 11.

45. Fixed offset 1.4MHz oscillator. This is an optional facility and consists of a crystal-controlled Colpitts oscillator, TR10. It is switched on by applying an earth to board pin 13 and the amount of frequency offset is determined by the frequency of the crystal, XL1, and the adjustment of C35. The oscillator output signal is coupled by C47 to the two output amplifier stages, TR20, TR21.

LOW-FREQUENCY LOOP BOARD PM588 (fig.30)

46. This board contains the low-frequency loop and also the programmed divider, mixer, phase comparator and lock detector circuits of the lower transfer loop; the lower transfer loop v.c.o. is contained on the upper loop board (PM589). A block diagram of the board is given in fig.9.

6 to 7 MHz voltage-controlled oscillator

47. The 6 to 7 MHz v.c.o. for the low-frequency loop consists of transistor TR1, a tuned circuit, L1, C1, C2, and a varactor diode D1; feedback is provided by the inverting gate, G1 (ML1). The square-wave output signal is applied to the programmed divider, N1, and also to the programmed divider of the lower transfer loop, N2, via G8 (ML1).

Programmed divider N1

48. The programmed divider consists of four presettable decade counters, ML3, ML5, ML6, ML10, NAND gates G2, G3, and a dual J-K flip-flop, ML11.

49. The decade counters have strobed parallel-entry capability such that the starting point of a count sequence may be preset. A '1' or a '0' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Ao, Bo, Co, Do) when the strobe (S) input is at '0'. The counting operation is performed on the negative-going edge of the input clock pulse.

50. The division ratio of the programmed divider, which is controlled by the 1kHz, 100Hz, 10Hz digits of the selected operating frequency, is given by the expression N1 = 7000 minus the selected digits, i.e. the division ratio is 7000 for a setting of 000 and is 6001 for a setting of 999. The operation of the divider is described below.

51. Binary coded decimal (BCD) frequency setting information is applied to the data inputs of ML3 (10Hz data), ML5 (100Hz data) and ML6 (1kHz data). The Da, Dc, and Dd data input of ML10 are connected to the 0V line whilst the Db data input is floating and is equivalent to logic '1'. ML10, therefore, is set to start counting at binary 2.

52. To start a counting sequence, assume that a logic '0' strobe pulse is applied to the strobe (S) input of each decade counter. As described in para.49, this causes the logic level applied to each input line (Da, Db, Dc, Dd) to be transferred to the corresponding output line (Ao, Bo, Co, Do). The negative-going edge of the clock pulse (from the v.c.o.) is applied to the

clock 1 input of ML3 and each pulse is now counted until an output from the counter of 8996 is reached, i.e. until the Do output from ML10 is at '1', the Ao and Do outputs from ML6 and ML5 are at '1', and the Bo and Co outputs from ML3 are at '1'. Since ML10 is set to start counting at 2, and since the remaining counters may be set to start counting at any number from 0 to 9, the maximum number of clock pulses that may be counted is equal to 8996 minus 2000 which equals 6996.

53. Once a count of 8996 is reached, the input lines to NAND gate G2 are all at logic '1' and the '0' output, inverted by G3, is applied to the K input of a dual negative-edge triggered J-K flip-flop, ML11. The operation of this flip-flop, which generates the strobe pulse for the decade counters, is given in the timing diagram, fig.6. From this diagram it can be seen that two clock pulses elapse to coincide with the end of the strobe pulse. Thus four clock pulses are counted by ML11, making a total count of 7000, i.e. 6996 + 4.

Reference frequency divider

54. The 1MHz input signal at board pins 45 and 46 is coupled by transformer T1 to a shaper stage, TR2; the square-wave output signal from the collector of TR2 is applied to a divider consisting of three decade dividers, ML2, ML4, ML7 and the output signal, at 1000p/s, is applied to one of the clock inputs of the l.f. loop phase comparator, ML8.

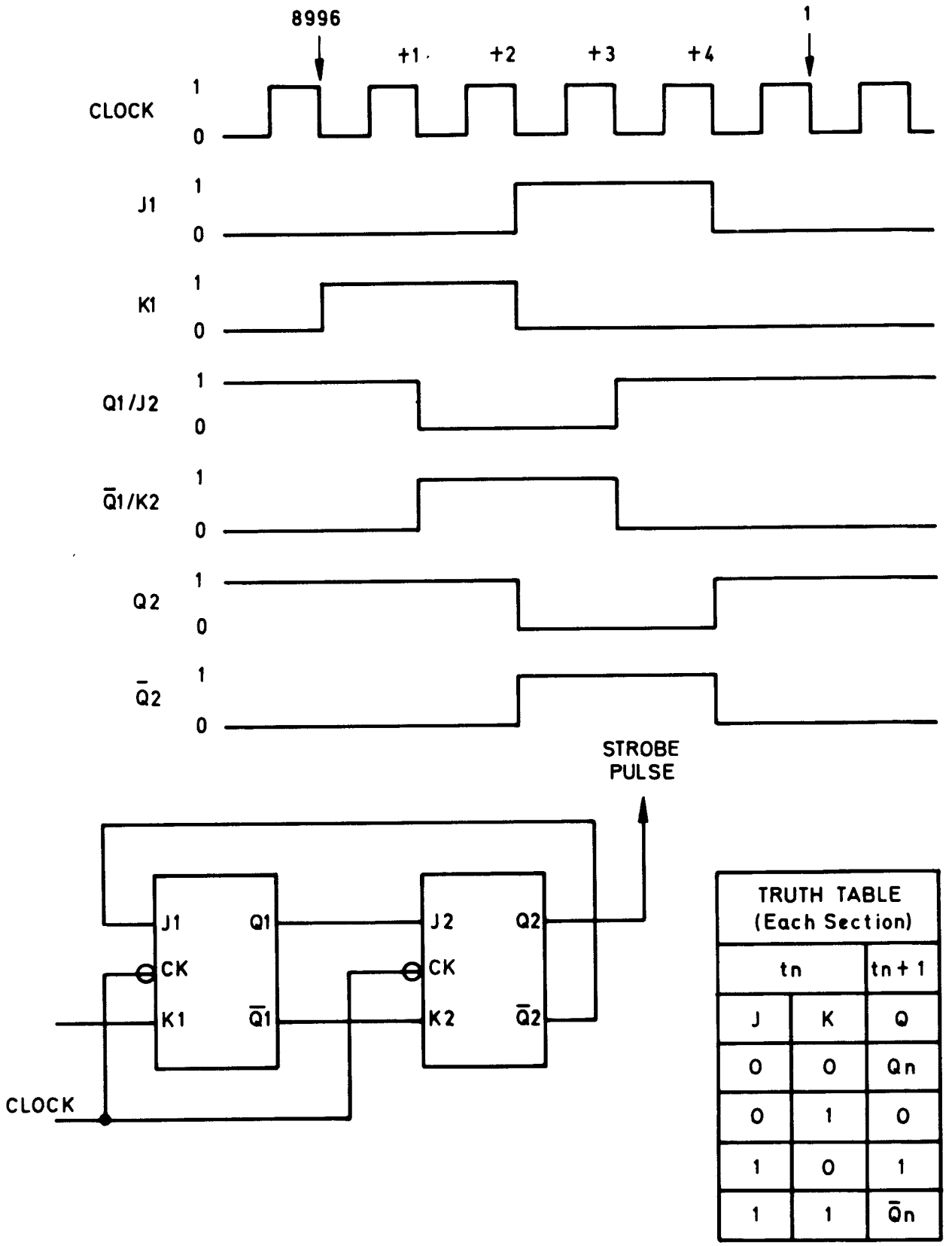
L.F. loop phase comparator

55. The phase comparator consists of a dual D-type flip-flop, ML8, a two-input NAND gate G4 and a voltage control circuit, TR3, TR4, TR5; TR24 is a high-impedance buffer stage. It compares the output frequency from the programmed divider, N1, with the output frequency from the reference divider; the error signal is used to develop a direct compensating voltage which is applied to the 6-7MHz v.c.o.

56. The output signal from the programmed divider, N1, from ML10 pin 12, consists of positive-going pulses which are applied to the clock input of ML8b (Pin 3). The output signal from the reference divider also consists of positive-going pulses, and these are applied to the clock input of ML8a (Pin 11). The D inputs of ML8, at pins 2 and 12, are both taken to the +5V rail (logic '1') via R50. Thus when the positive edge from ML10 pin 12 clocks ML8b, the Q output at pin 5 changes to '1' and the $\overline{Q}$ output changes to '0'. Similarly, when the positive edge from the reference divider clocks ML8a, the Q output at pin 9 changes to '1' and the $\overline{Q}$ output changes to '0'. When both Q outputs are at '1' the output from the NAND gate, G4 (ML1), changes to '0' clearing both flip-flops of ML8 via R53 and thus resets the Q outputs to '0' and the $\overline{Q}$ outputs to '1'.

57. Consider the case where the 6 to 7MHz v.c.o. frequency is high. This will mean that the positive edge from the programmed divider will occur before the positive edge from the reference divider. The resulting setting and re-setting of the flip-flops causes increased conduction of TR4, due to the Q output waveform from ML8b (fig.5) as compared with the conduction of TR5; this causes the voltage at the collector of TR4 to become less positive, thereby reducing the voltage applied to varactor diode, D1, and reducing the v.c.o. frequency.

58. If the v.c.o. frequency is low, the programmed divider output pulse will occur after the reference pulse, the Q output waveform from ML8a will cause increased conduction of TR5 and the voltage at the collector of TR4 will become more positive. The increased voltage applied to the varactor diode



TRUTH TABLE (Each Section)		
tn		tn + 1
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	Q̄n

Fig.6 Timing diagram : strobe pulse generation (l.f. loop PM588)

causes the v.c.o. frequency to increase, thus correcting the error.

59. When the two signals are equal in frequency and phase the two flip-flops of ML8 are clocked at the same time, the two Q output waveforms are equal and the varactor line voltage remains constant.

L.F. loop lock detector

60. The l.f. loop lock detector consists of a bistable latch, G5, G6 and an output buffer, G7. The $\overline{Q}$ outputs from the phase comparator, ML8, are connected directly to G5, and also to G6 via integrating components, R50, C19 and R51, C20. Under phase-locked conditions the in-phase negative-going $\overline{Q}$ output pulses from ML8, pins 6 and 8 ($\overline{Q}1$ and $\overline{Q}2$ of fig.5) are prevented from reaching G6 due to the time constants presented by the integrating components. Pins 1 and 2 of G6 therefore float up to logic '1' and the resulting logic '0' output, at G6 pin 12, forces the output of G5 to logic '1'. The inputs to the output buffer, G7, are connected in parallel with those of G6 and the logic '0' in-lock indication output is taken to board pin 1.

61. When an out-of-lock condition exists, the clock input waveforms applied to ML8 are no longer in phase and the resultant longer-duration negative-going output pulses from ML8 pin 6 or ML8 pin 8 (dependent on whether a phase lead or a phase lag exists) are sufficient in width to overcome the time constant presented by the respective integrating components. The effect of this is to produce an alternating '0' - '1' output signal from the buffer, G7, as shown in the timing diagram, fig.7.

Programmed divider N2

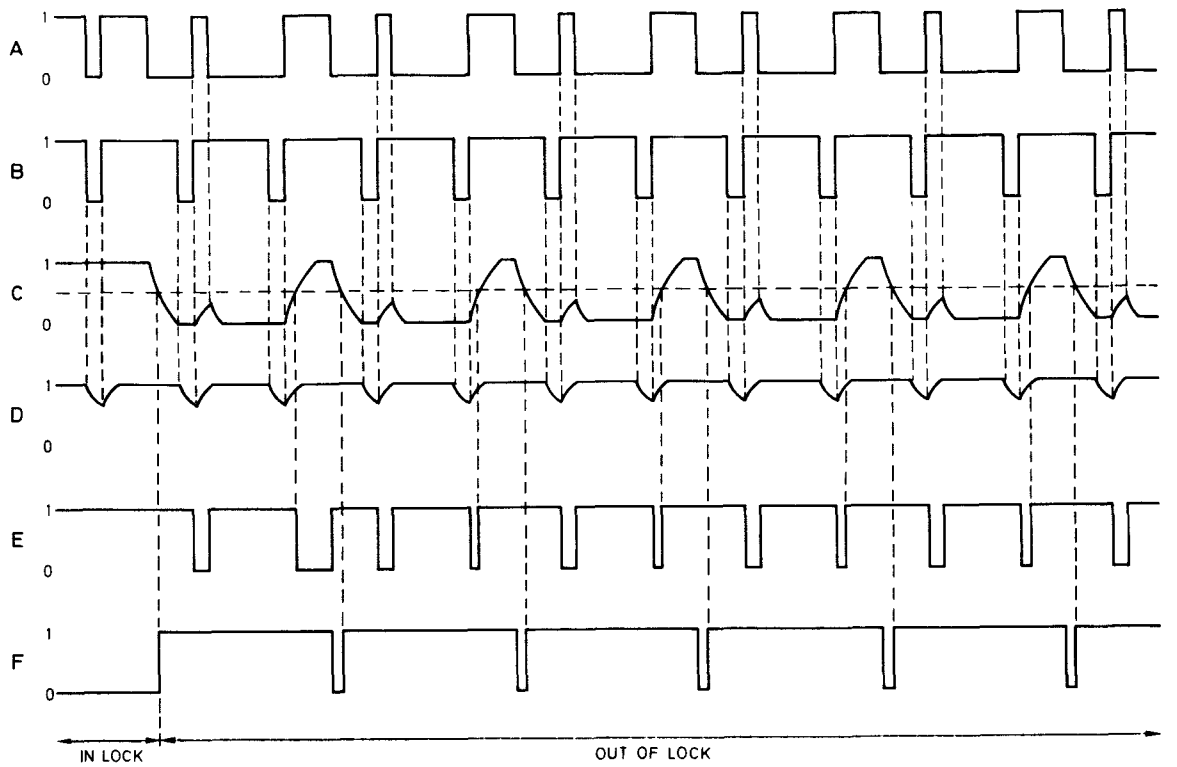
62. This programmed divider, which forms part of the lower transfer loop, consists of three presettable decade counters, ML14, ML15, ML19, NAND gates, G10, G11, and a dual J-K flip-flop, ML20.

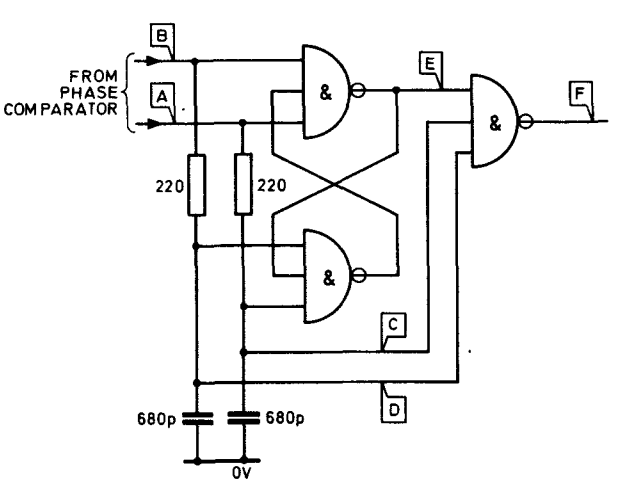
63. The decade counters have strobed parallel-entry capability such that the starting point of a count sequence may be preset. A '1' or a '0' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Ao, Bo, Co, Do) when the strobe (S) input is at '0'. The counting operation is performed on the negative-going edge of the input clock pulse.

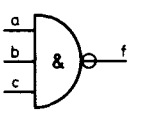
64. The division ratio of the divider is controlled by the 10kHz and 100kHz digits of the selected operating frequency and also by overspill data from the display board which is applied to ML19. The division ratio, without overspill, is given by the expression N2 = 453 minus selected digits; i.e. the division ratio is 453 for a setting of 00 and is 354 for a setting of 99. With overspill the division ratio is modified to cover the range 455 to 352. The operation of the divider is described below.

65. B.C.D. frequency setting information is applied to the data inputs of ML14 (10kHz data) and ML15 (100kHz data). When not in the overspill condition, the data inputs to ML19 are all at 0V (logic '0') and under this condition ML19 starts counting at zero.

66. To start a counting sequence, assume that a logic '0' strobe pulse is applied to the strobe (S) input of each decade counter. As described in paragraph 63, this causes the logic level applied to each data input line (Da, Db, Dc, Dd) to be transferred to the corresponding output line (Ao, Bo, Co, Do). The negative-going edge of the clock pulse (the output from the L.F. loop via G8) is applied to the clock 1 input of ML14 and each pulse is counted until a count of 449 is reached, i.e. until the Co output from ML19 is at '1',

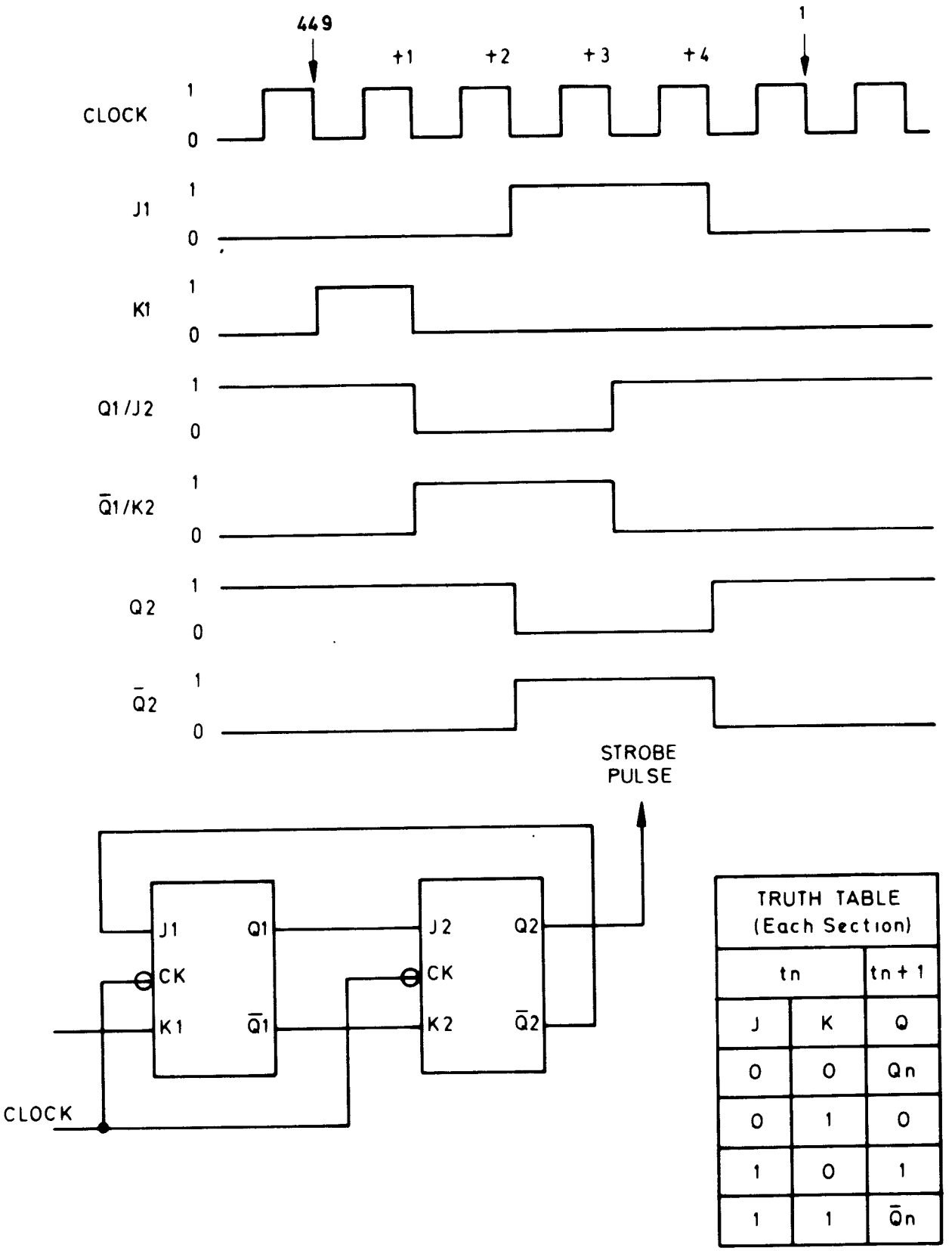






TRUTH TABLE 3-INPUT NAND GATE			
a	b	c	f
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Fig.7 Timing diagram : lock detector



TRUTH TABLE (Each Section)		
tn		tn + 1
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	Q̄n

Fig.8 Timing diagram : strobe pulse generation, lower transfer loop

the Co output from ML15 is at '1' and the Ao and Do outputs from ML14 are at '1'. Thus when a count of 449 is reached the four input lines to the NAND gate, G10, are at logic '1' and the resutling '0' output, inverted by G11, is applied to the K input of a dual, negative-edge triggered, J-K flip-flop, ML20. The operation of this flip-flop, which generates the strobe pulse for the decade counters, is given in the timing diagram, fig.8. From this diagram it can be seen that two clock pulses elapse before the start of the strobe pulse and a further two clock pulses elapse to coincide with the end of the strobe pulse. Thus four clock pulses are counted by ML20, making a total count of 453, i.e. 449 + 4, before the start of the next sequence.

Mixer stage

67. ML13 is an integrated circuit mixer where the 1MHz square wave from TR2 is applied to the carrier input, pin 8, and the 1.013 - 1.020MHz output from the lower transfer loop oscillator is applied to the signal input, pin 1. The output signal from the mixer, at pin 6, is applied to a low-pass filter, C27, C28 L3, which selects the difference frequency. The filter is followed by a buffer stage, TR19, and an output shaper, G9, which is fed from a voltage regulator consisting of TR20 and a 5.6V Zener diode, D3; the square-wave output from G9 is applied to the lower transfer loop phase comparator.

Lower transfer loop phase comparator

68. The phase comparator consists of a dual D-type flip-flop, ML16, NAND gate G15, and a voltage control circuit, TR21, TR22, TR23; TR25 is a high-impedance buffer stage. It compares the output signal frequency from the mixer with the output signal frequency from the programmed divider N2; any error between these two frequenciess is used to develop a control voltage which is applied to the lower transfer loop oscillator to eliminate the error. The action of the circuit is described below.

69. The output signal from the programmed divider, at ML20 pin 3, consists of negative-going pulses which are applied to the clock input of ML16b (pin 11). The output signal from the mixer via ML17 pin 6 is applied to the clock input of ML16a (pin 3). The D inputs of ML16, at pins 2 and 12, are both taken to the +5V (logic '1') via R66. Thus when the positive edge from ML20 pin 3 clocks ML16b, the Q output at pin 9 changes to '1' and the $\overline{Q}$ output at pin 8 changes to '0'. Similarly, when the positive edge from ML17 pin 6 clocks ML16a, the Q output at pin 5 changes to '1' and the $\overline{Q}$ output at pin 6 changes to '0'. When both Q outputs are at '1' the output from the NAND gate, G15, changes to '0' clearing both flip-flops of ML16 via R74 and thus resets the Q outputs to '0' and the $\overline{Q}$ outputs to '1'.

70. Consider the case where the output frequency from the mixer is high (due to an increase in the frequency of the lower transfer loop oscillator). This will mean that the positive edge from the programmed divider will occur after the positive edge from the mixer. The resulting setting and resetting of the flip-flops causes increased conduction of TR23, due to the Q output waveform from ML16a (fig.5), as compared with the conduction of TR21; this causes the voltage at the collector of TR23 to become less positive, thereby reducing the voltage applied to the varactor diode of the lower transfer loop oscillator. This causes a reduction in the oscillator frequency and a corresponding decrease in the output frequency from the mixer.

71. If the mixer output frequency is low (due to a decrease in the frequency of the lower transfer loop oscillator), the positive edge from the programmed divider will occur before the edge from the mixer, the Q output waveform from ML16b will cause increased conduction of TR21 and the voltage at the collector

of TR23 will become more positive. The increased voltage applied to the varactor diode of the lower transfer loop oscillator causes an increase in the oscillator frequency and a corresponding increase in the output frequency from the mixer.

72. When the two signals are equal in frequency and phase the two flip-flops of ML16 are clocked at the same time, the two Q output waveforms are equal and the varactor line voltage remains constant.

Lower transfer loop lock detector

73. This consists of a bistable latch, G12, G13, and an output buffer, G14. It is fed from the Q outputs of the phase comparator flip-flop, ML16, and produces a steady logic '0' in-lock signal or an alternating '0' - '1' out-of-lock signal at board pin 42. The action of the circuit, which is identical to that of the l.f. loop lock detector (para.60) is depicted in the timing diagram, fig.7.

UPPER LOOP BOARD PM589 (fig.32)

74. This board contains the upper loop, the lower transfer loop v.c.o. and also a lock indicator circuit; a block diagram of the board is given in fig.10.

Lower transfer loop v.c.o.

75. This voltage-controlled oscillator/shaper stage TR5, TR6, produces a square-wave output signal in the frequency range 1.013 to 1.020MHz. The tuned circuit comprises L4, capacitor C10, C11, C13, and a varactor diode, D4; positive feedback is applied to the tuned circuit via R14. TR4 and 5.6V Zener diode D3 provide supply voltage stabilization.

76. The oscillator output signal to the mixer stage of the lower transfer loop (PM588) is taken from the emitter of TR5 and is fed to board pin 8 via C12; the varactor line input, from PM588, is applied to D4 via board pin 7 and inductor L5.

77. The lower transfer loop v.c.o. output signal is taken from the collector of TR6 and may be monitored at TP1; it is applied to the lower loop phase comparator via a fixed divider stage ML4, ML6.

Upper loop v.c.o./shaper

78. The v.c.o./shaper stage comprises emitter-followers, TR19, TR2, inverting NAND gate, G1, and a tuned circuit, L1, C2, C3, and varactor diode, D2. Supply voltage stabilization is provided by TR1 and 5.6V Zener diode, D1. The oscillator output signal, in the frequency range 4.6 to 3.6MHz, is applied to the following:-

(1) The upper transfer loop board (PS338) via a NAND gate, G2, a filter R4, L2, C5, a tuned circuit, T1, C1, and board pins 1 and 2.

(2) The programmed divider, N2, of the upper loop via a NAND gate G3.

(3) ML8a (pin 11), which forms part of the strobe pulse generator for the programmed divider, N2.

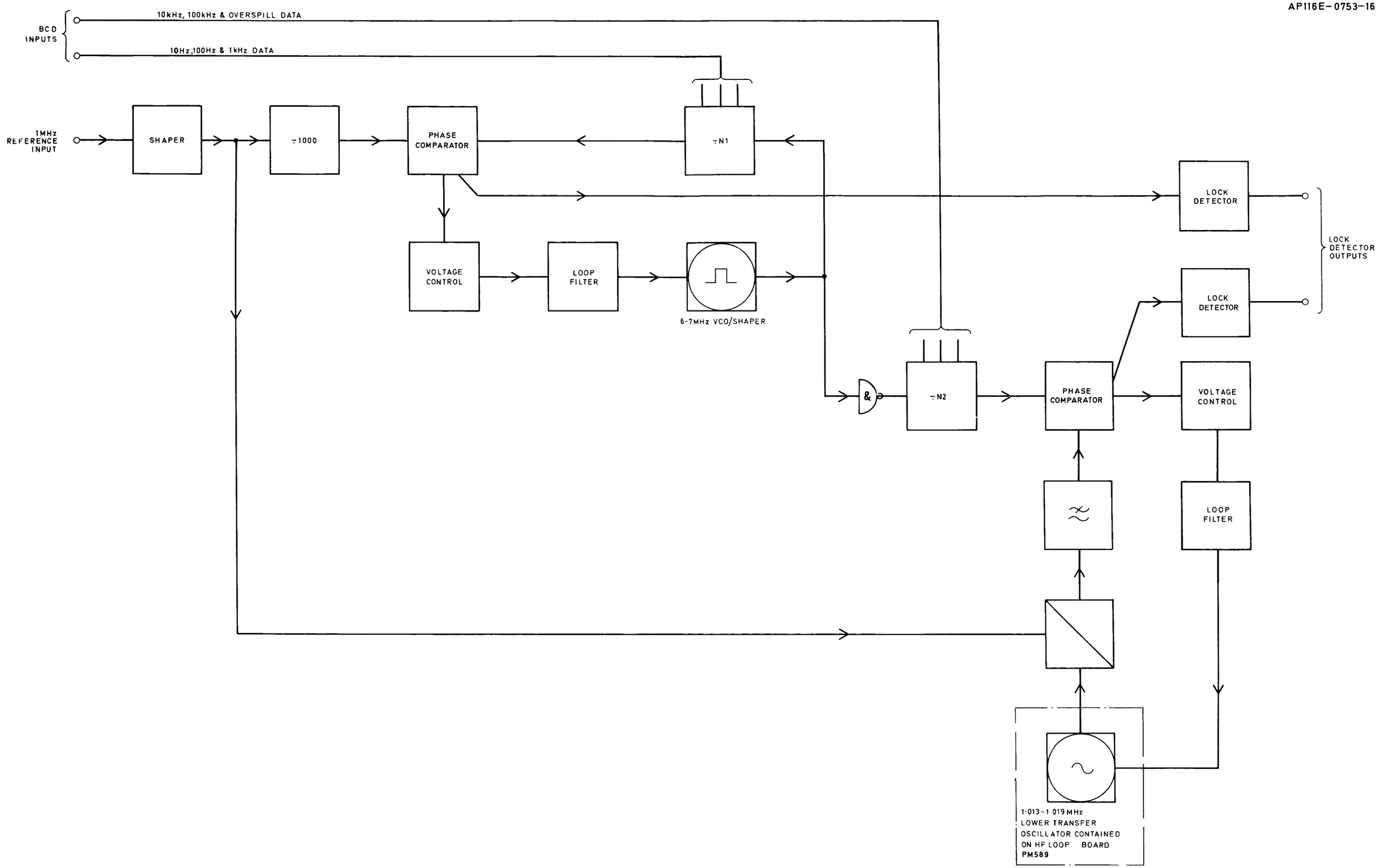


Fig.9

Block diagram : low frequency loop board PM588

Fig. 9

Chap.2-1

Programmed divider N2

79. The upper loop programmed divider, which has the same division ratio, N2, as that of the lower transfer loop, consists of three presettable decade counters, ML2, ML3, ML5, NAND gate G4, and a D-type flip-flop, ML8a.

80. The decade counters have strobed parallel-entry capability such that the starting point of a count sequence may be preset. A '1' or a '0' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Ao, Bo, Co, Do) when the strobe (S) input is at '0'. The counting operation is performed on the negative-going edge of the input clock pulse.

81. The division ratio of the divider is controlled by the 10kHz and 100kHz digits of the selected operating frequency and also by the overspill data from the display board which is applied to ML5. The division ratio, without overspill, is given by the expression N2 = 453 minus selected digits, i.e. the division ratio is 453 for a setting of 00 and is 354 from a setting of 99. With overspill the division ratio is modified to cover the range 455 to 352. The operation of the divider is described as follows.

82. B.C.D. frequency setting information is applied to the data inputs of ML2 (10kHz) and ML3 (100kHz). When not in the overspill condition, the data inputs to ML5 are all at 0V (logic '0') and under this condition ML5 starts counting at zero.

83. To start a counting sequence, assume that a logic '0' strobe pulse is applied to the strobe (S) input of each decade counter. As described in para.80, this causes the logic level applied to each data input line (Da, Db, Dc, Dd) to be transferred to the corresponding output line (Ao, Bo, Co, Do). The negative-going edge of the clock pulse (the 4.6 - 3.6MHz v.c.o, output via G3) is applied to the clock 1 input of ML2 and each clock pulse is counted until a count of 451 is reached, i.e. until the Co output from ML5 is at '1', the Ao and Co outputs from ML3 are at '1', and the Ao output from ML2 is at '1'. Thus when a count of 451 is reached, the four input lines to NAND gate G4 are at logic '1', and the output from G4, which is applied to the D input of flip-flop ML8a (pin 12), changes to '0'. The next clock pulse to arrive at ML8 pin 11 transfers the logic '0' at ML8 pin 12 to the Q output at pin 9, and this is applied as the strobe pulse to the three decade counters. The four input lines to the NAND gate, G4, are now no longer at logic '1' and the D input of ML8a changes to '1'. The next clock pulse to arrive at ML8 pin 11 transfers the logic '1' at ML8 pin 12 to the Q output at pin 9, the '0' strobe pulse is removed, and the counter is ready to start the next count sequence. Thus two clock pulses are used to generate the strobe pulse, making a total count of 453, i.e. 451 + 2.

Range blanking

84. The range blanking input, at board pin 11, is used to momentarily inhibit the two inputs to the upper loop phase comparator when, during receiver tuning, a 9-to-0 or a 0-to-9 transition of the 10kHz digit occurs. This allows the l.f. and lower transfer loop outputs to run up or down to the new frequency whilst the 3.6 to 4.6MHz v.c.o. is prevented from changing frequency.

85. The range blanking input line, which is normally at approximately +5V (logic '1'), is connected to the D (pin 12) and clear (pin 13) inputs of a D-type flip-flop, ML9a. This provides the required logic '1' to the D inputs of the phase comparator, ML8b, ML9b. The logic '0' 25 millisecond range blanking pulse, from the display board, clears ML9a and forces the Q output, at ML9 pin 9, to '0'. This is applied to the D inputs of the phase comparator

and also to the clear input of the strobe pulse generator flip-flop, ML8a. Thus a 25 millisecond strobe pulse, from ML8 pin 9, is applied to the programmed divider, N2, and the output is inhibited.

Fixed divider

86. The fixed divider consists of two decade counters, ML4, ML6, connected in cascade. The lower transfer v.c.o. output signal is applied to the A input of ML4 and the divide-by-100 output is taken from ML6 pin 11; this is applied as the clock input to the phase comparator (ML9b pin 3) and may be monitored at TP3.

Phase comparator

87. The phase comparator consists of two D-type flip-flops, ML8b, ML9b, NAND gate G5, and a voltage control circuit, TR16, TR17, TR18; TR20 is a high-impedance buffer stage. It compares the output frequency from the programmed divider with the output frequency from the fixed divider; the error is used to develop a direct compensating voltage which is applied to the 3.6 to 4.6MHz v.c.o.

88. The output from the programmed divider, at ML8 pin 8, consists of positive-going pulses which are applied to the clock input of ML8b (pin 3). The output from the fixed divider, at ML6 pin 11, also consists of positive-going pulses and these are applied to the clock input of ML9b (pin 3). The D inputs of both ML8b and ML9b are at logic '1' (para.85). Thus when the positive edge from ML8a pin 8 clocks ML8b, the Q output at pin 5 changes to '1' and the $\overline{Q}$ output at pin 6 changes to '0'. Similarly, when the positive edge from ML6 pin 11 clocks ML9b, the Q output at pin 5 changes to '1' and the $\overline{Q}$ output at pin 6 changes to '0'. When both Q outputs are at '1', the output from the NAND gate, G5, changes to '0', clearing both ML8b and ML9b; thus the Q outputs are reset to '0' and the $\overline{Q}$ outputs are reset to '1'.

89. Consider the case where the frequency from the programmed divider is high. This will mean that the positive edge from ML8a pin 8 will occur before the positive edge from ML6 pin 11. The resultant setting and resetting of the flip-flop causes increased conduction of TR18, due to the Q output waveform from ML8b (see Q1 on timing diagram fig.5), as compared with the conduction of TR16; this causes the voltage at the collector of TR18 to become less positive, thereby causing a reduction in the voltage applied to the varactor diode, D2, of the 3.6 to 4.6MHz v.c.o., and a corresponding reduction in the v.c.o. frequency.

90. If the output frequency from the programmed divider is low, the positive edge from ML8a pin 8 will occur after the positive edge from ML6 pin 11, the Q output waveform from ML9b pin 5 will cause increased conduction of TR16 and the voltage at the collector of TR18 will become more positive. The resultant increase in the voltage applied to the varactor diode, D2, causes a corresponding increase in the v.c.o. frequency, thus correcting the error.

91. When the two signals are equal in frequency and phase the two comparator flip-flops are clocked at the same time, the two Q output waveforms are equal and the varactor line voltage remains constant.

Lock detector

92. This consists of a bistable latch, G6, G7, and an output buffer, G8. It is fed from the $\overline{Q}$ outputs of the phase comparator flip-flops, ML8b, ML9b, and produces a steady '0' in-lock signal, or an alternating '0' - '1' out-of-lock

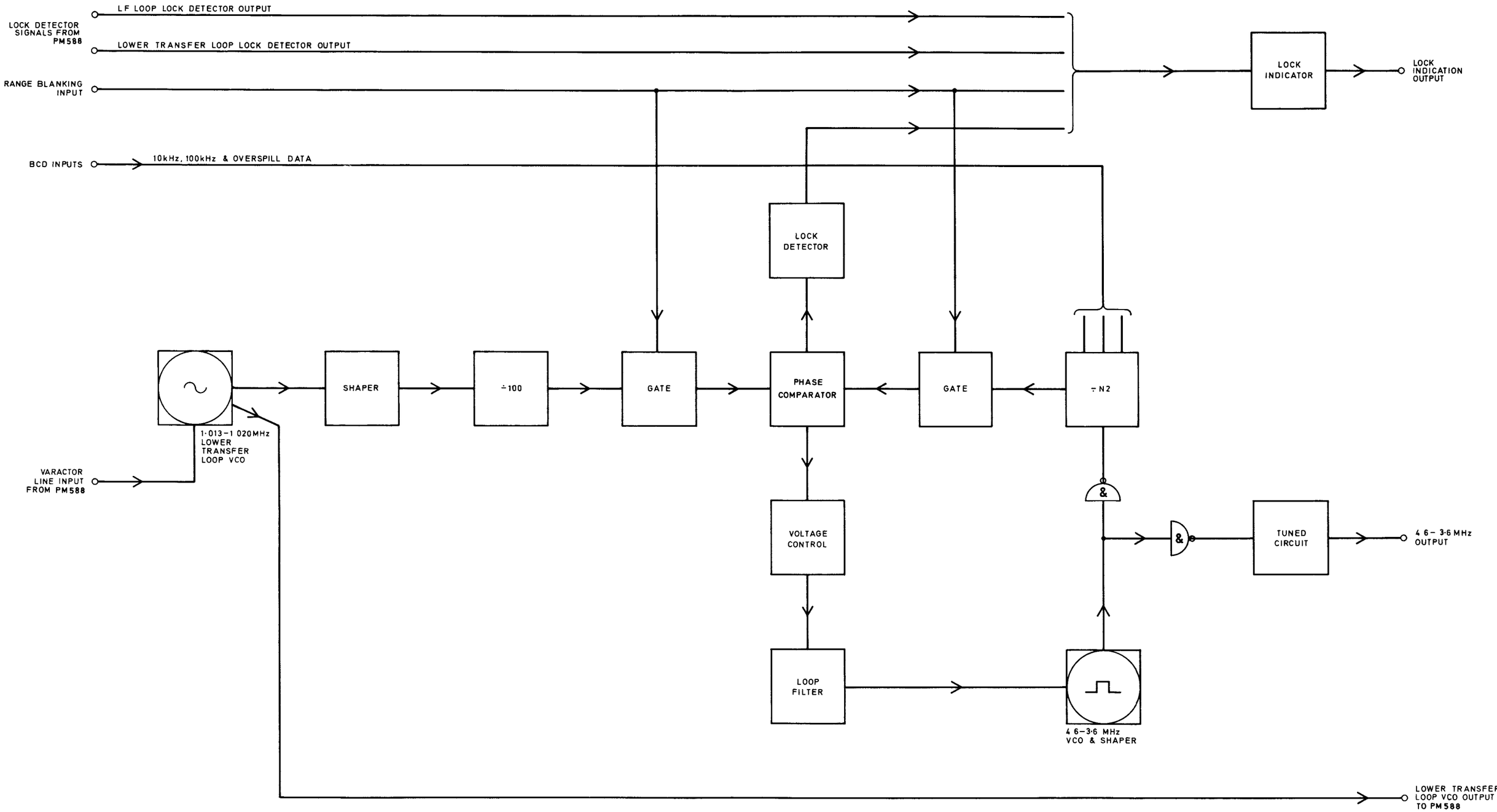


Fig.10

Block diagram : upper loop board : PM589

signal, at ML11 pin 8. The action of the circuit, which is identical to that of the l.f. loop lock detector (para.60) is depicted in the timing diagram, fig.8.

Lock indicator

93. The lock indicator consists of five NAND gates, G9 to G13 inclusive. The lock detector outputs from the l.f. and lower transfer loops (PM588) are applied to G10 and G9 via board pins 13 and 14 respectively, whilst the upper loop lock detector output, at ML11 pin 8, is applied to G11. The output from G13 ('1' for in-lock, '0' for out-of-lock) is applied to a diode OR gate and the out-of-lock indicator lamp driver on the display board.

TRANSFER LOOP BOARD PS338 (fig.34)

94. The transfer loop board contains the upper transfer loop (with the exception of the upper transfer loop oscillator which is located on the h.f. loop board PS337), programmed divider N3 and lock indicator circuits. This board, together with h.f. loop board, generates the 35.4 to 65.4MHz local oscillator injection frequency for the first mixer. A block diagram of the two boards is given in fig.14.

95. The 4.6 to 3.6MHz output signal from the upper loop, at board pin 17, is coupled by C3 to a shaper stage, TR4, TR5. The squarewave output is inverted by ML4a and is then applied to a programmed divider consisting of two pre-settable decade counters ML1, ML2, and inverter ML4b, a six-input NAND gate ML5 and a D-type flip-flop, ML6.

Programmed divider N3

96. The two decade counters ML1, ML2, have strobed parallel-entry capability so that the starting point of a count sequence may be preset. A '1' or a '0' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Ao, Bo, Co, Do) when the strobe (S) input is at '0'. The counting operation is performed on the negative-going edge of the input clock pulse.

97. The division ratio of the programmed divider, which is controlled by the front panel MHz switch, is given by the expression N3 = 40 plus selected MHz digits, i.e., when 00MHz is selected, the division ratio is 40, and when 29MHz is selected, the division ratio is 69. The operation of the divider is as follows.

98. Information from the front-panel 30-way MHz switch is applied to the logic board where it is converted into a BCD nines-complement code (Table 3). The nines-complement coded outputs from the logic board are applied to the data inputs of the two decade counters, 'units' to ML1 and 'tens' to ML2, and preset the starting point of a count sequence.

99. To start the counting sequence, assume that a logic '0' strobe pulse is applied to the strobe (S) inputs of both ML1 and ML2 (at pin 1). As described in paragraph 96, this causes the logic level applied to each input line (Da, Db, Dc, Dd) to be transferred to the corresponding output line (Ao, Bo, Co, Do) The negative going edge of the clock pulse (from the shaper stage, TR4, TR5 and the inverter ML4A) is now applied to the clock 1 input of ML1 at pin 8. Each clock pulse is now counted until a count of 37 is reached, i.e. until the Ao, Bo and Co outputs from ML1 and the Ao and Bo outputs from ML2 are all at logic '1'. (The C output from ML2 is applied to an inverter, ML4B, to inhibit binary 7).

TABLE 3

Code conversion

Decimal	BCD				Nines complement				Decimal
	D	C	B	A	D9	C9	B9	A9	
0	0	0	0	0	1	0	0	1	9
1	0	0	0	1	1	0	0	0	8
2	0	0	1	0	0	1	1	1	7
3	0	0	1	1	0	1	1	0	6
4	0	1	0	0	0	1	0	1	5
5	0	1	0	1	0	1	0	0	4
6	0	1	1	0	0	0	1	1	3
7	0	1	1	1	0	0	1	0	2
8	1	0	0	0	0	0	0	1	1
9	1	0	0	1	0	0	0	0	0

100. When a count of 37 is reached, the input lines to the NAND gate, ML5, are all at logic '1' and the '0' output, at ML5 pin 8, is applied to the D input of flip-flop ML6. The next clock pulse, which is applied to pin 3 of ML6, transfers the '0' at ML6 pin 2 to the Q output, at ML6 pin 5, and this is applied as the next strobe pulse to the two decade counters, ML1 and ML2, ready for the next count. The output from ML5 changes to logic '1' and the next clock pulse applied to ML6 causes the Q output to change to logic '1'; this output is applied to the phase comparator, ML8.

101. Table 4 shows the operation of the divider for various settings of the MHz switch.

TABLE 4

Programmed divider operation (PS338)

'MHz' setting	Nines Complement	Clock pulses				
		Count up to 100	Fixed count	Strobe-pulse Begin	Strobe-pulse End	Total division ratio
00	99	1	37	1	1	40
07	92	8	37	1	1	47
14	85	15	37	1	1	54
21	78	22	37	1	1	61
29	70	30	37	1	1	69

Mixer

102. ML3 is an integrated circuit mixer; the 1MHz reference frequency signal, shaped by TR1, TR2, is applied to pin 8 and the 885-948kHz transfer loop oscillator output signal, from the h.f. loop board, buffered by TR3, is applied to pin 4 via a low-pass filter, L9, L10, C29 to C32. The difference frequency output from the mixer, 115kHz to 52kHz, is coupled to a low-pass filter, L11, L12, C36, C38, C39, and is then applied to a shaper stage, TR6. The squarewave output from TR6 is applied to the phase comparator, ML8 via a buffer, ML7A.

Phase comparator

103. The phase comparator consists of a dual D-type flip-flop, ML8, a two-input NAND gate, ML7B and a voltage control circuit, TR7, TR8, TR9, TR10. It compares the output signal frequency from the programmed divider with the output signal frequency from the mixer; any error between these two frequencies is used to develop a d.c. voltage, which is applied to the transfer loop oscillator (on the h.f. loop board) to eliminate the error. The action of the circuit is as follows.

104. The output from the programmed divider, at ML6 pin 5, consists of negative going pulses; these are applied to the clock input of ML8b. The output from the mixer (via the low-pass filter, shaper and buffer), at ML7a pin 8, is applied to the clock input of ML8a. The D inputs to both ML8a and ML8a are taken to the +5V rail (logic '1'). Thus when the positive edge from ML6 pin 5 clocks ML8b, the Q2 output at pin 5 changes to '1' and the $\overline{Q}2$ output changes to '0'. Similarly, when the positive edge from ML7a pin 8 clocks ML8a, the Q1 output changes to '1' and the $\overline{Q}1$ output changes to '0'. When both Q outputs are at '1', the output from the NAND gate, ML7b, changes to '0', clearing both ML8 flip-flops via R38 and thus resetting the Q outputs to '0' and the $\overline{Q}$ outputs to '1'.

105. Consider the case where the frequency of the mixer output signal is high. This will mean that the positive edge from ML7a will occur before the edge from ML6. The resultant setting and resetting of the flip-flops causes increased conduction of TR7, due to the $\overline{Q}1$ output from ML8a (fig.5), as compared with the conduction of TR10; this causes the voltage of the collector of TR9 to become more positive, thereby increasing the varactor line voltage applied to the transfer loop oscillator on the h.f. loop board. This increases the oscillator frequency, but since this frequency is subtracted from the reference 1MHz in the mixer, ML3, the output frequency from the mixer is reduced.

106. If the mixer output signal frequency is low, the pulse from ML7a will occur after the pulse from ML6, the $\overline{Q}2$ output waveform from ML8b will cause increased conduction of TR10 and the voltage at the collector of TR9 will become less positive. Thus the reduced varactor line voltage applied to the transfer loop oscillator causes a reduction in oscillator frequency and a corresponding increase in the mixer output signal frequency.

107. When the two frequencies are in phase, the two flip-flops of ML8 are clocked at the same time, the $\overline{Q}1$ output waveform is equal to the $\overline{Q}2$ output waveform and the varactor line voltage remains constant.

Lock indicator and fast-lock circuit

108. This circuit comprises two monostables, ML9, ML10, a dual D-type flip-flop, ML11, and NAND gates ML4c, ML4d. Its purpose is to augment the

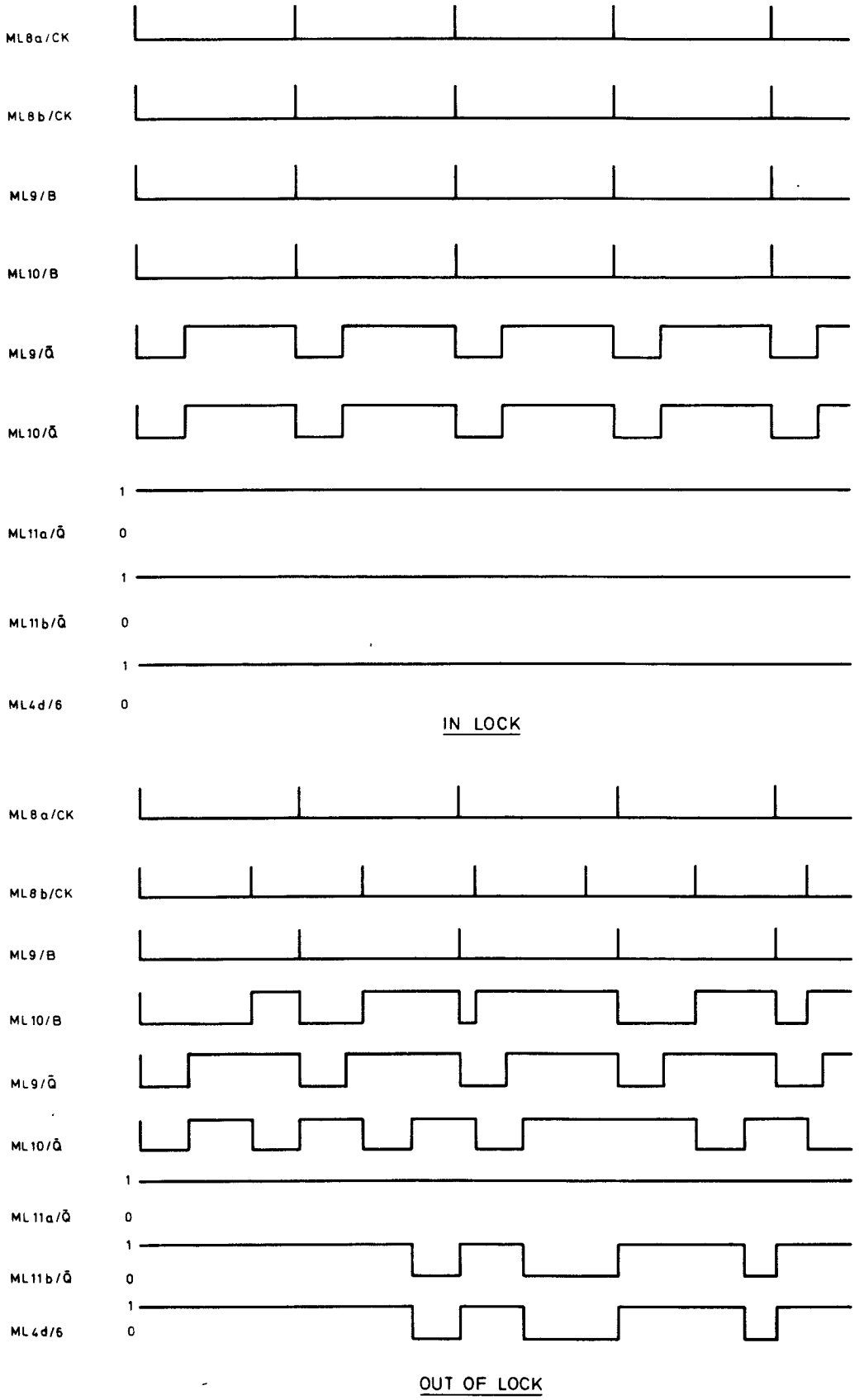


Fig.11 Timing diagram : fast lock and indicator (upper transfer loop PS338)

conduction of TR7 or TR10 in the out-of-lock condition and so obtain a faster return to the locked condition; it also provides a lock indication output signal. The action of the circuit is as follows.

109. The Q output from the phase comparator flip-flop, ML8a, is applied to the B input (Schmitt trigger) of the monostable, ML9, and also to the D and clear inputs of a D-type flip-flop, ML11a. Similarly, the Q output from ML8b is applied to the B input of the monostable, ML10, and also to the D and clear inputs of a second D-type flip-flop, ML11b. The two monostables, triggered when positive going signals are applied to the respective B inputs, each produce a negative going output pulse (Q), of approximately 1.5μs duration.

110. From the timing diagram, fig.11, it will be seen that for the in-lock condition, the $\overline{Q}$ outputs from the two flip-flops, ML11a, ML11b, are both at logic '1'; these two signals do not, however, affect the conduction of the voltage control transistors, TR7, TR10, due to the presence of the two diodes, D2, D3. The logic '0' output from ML4c is inverted by ML4d to produce a logic '1' in-lock signal at board pin 6.

111. If the output frequency from the mixer is low, as depicted by the out-of-lock waveform of fig.11; the negative excursion of the $\overline{Q}$ output from ML11b will be applied to TR10, via diode D3. The conduction of TR10 will, therefore, be rapidly increased to bring about a fast return to the in-lock condition. The $\overline{Q}$ output waveform from ML11b is also applied to ML4c to produce an alternating '0' - '1' out-of-lock signal at board pin 6.

112. Should the out-of-lock condition be due to a high mixer output frequency the $\overline{Q}$ output from ML11a will cause a rapid return to the in-lock condition by increasing the conduction of TR7; the $\overline{Q}$ output from ML11a is also applied to ML4c to produce an alternating '0' - '1' out-of-lock signal at board pin 6, as before.

HIGH-FREQUENCY LOOP BOARD PS337 (fig.36)

113. This board provides the 35.4 - 65.4MHz local-oscillator frequency for the first mixer; it also contains the 885-948kHz upper transfer loop oscillator. The block diagram of the h.f. loop board, together with the upper transfer loop board, is given in fig.14.

Upper transfer loop oscillator

114. Transistors TR17 and TR20, together with associated components, form a variable frequency LC oscillator, tunable by the voltage applied to the varactor diode D19. The varactor line voltage at pin 18, from the transfer loop board, is applied to D19 via a filter, C66, C67, R62, C69 and L19.

115. The oscillator output signal, at the collector of TR20, is applied to the clock input of a divide-by-two stage, ML12; the output from ML12, at pin 5, is applied as one signal input to the phase comparator, ML7.

116. A second output from the oscillator is coupled by C76 to a buffer amplifier TR21, the output from which is applied to the mixer on the transfer loop board, via C81 and pin 13.

H.F. loop oscillators

117. Three separate, switched oscillators are provided to cover the frequency range 35.400000 to 65.399999 MHz. Oscillator selection is controlled by the 30-way MHz switch on the front panel of the receiver; an earth (0V) is

connected to the appropriate switching transistor, TR1, TR2 or TR3 (via pins 28, 27 or 26 respectively) and the supply voltage to the selected oscillator is switched on. The oscillator selected is in accordance with Table 5.

TABLE 5

H.F. loop oscillator selection

Oscillator	Frequency range (MHz)	MHz switch setting
1	35.40000 to 43.9999	0 to 7
2	43.40000 to 53.9999	8 to 17
3	53.40000 to 65.39999	18 to 29

118. The three oscillators are similar in construction and operation. Frequency is controlled by the voltage applied to a pair of varactor diodes; this voltage, derived by the phase comparator, is applied via a common line and an inductor (L21, L22, L23) to each oscillator. The gain of the selected oscillator stage is automatically controlled by peak-detecting diodes D13, D14, and the current source transistor, TR13; the automatic gain control (a.g.c.) level is preset by R38.

119. The output from the selected oscillator transistor and associated buffer (Table 5) is amplified by TR10 and applied to:-

(1) The a.g.c. stage, TR13, via C26.

(2) A programmed divider, via C24.

(3) A pair of output buffer amplifier stages, TR14, TR15, via C36.

TABLE 6

H.F. loop oscillators

Oscillator number	Voltage switch	Oscillator circuit	Output buffer
1	TR3	TR6, D8, D9, L6	TR9
2	TR2	TR5, D6, D7, L5	TR8
3	TR1	TR4, D4, D5, L4	TR7

Oscillator output buffer stages

120. The output buffer amplifier stages, TR14, TR15, are conventional and are of similar design; stage gain is preset by potentiometers R44 (for TR14) and R50 (for TR15). The amplified outputs are fed to a diode switch, D16, D17, D18, which is controlled by the rear panel LO INT/EXT switch. When this switch is set to EXT, an earth (0V) is connected to board pin 25; this causes diodes D16 and D17 to become reversed biassed, and diode D18 to become forward

biassed. The outputs from the two buffer stages are inhibited and an external LO (local-oscillator) signal from a second receiver, connected to the rear panel LO IN/OUT socket, is routed to board pin 24 and thence via C57, D18, C58 and pin 22 to the first mixer board.

121. When the LO INT/EXT switch is set to INT, the earth is removed from board pin 25; diodes D16, D17 are now forward biassed and diode D18 is reverse biassed. The output signal from TR14 is routed to the first mixer board via C44, D16, C58 and board pin 22; the output signal from TR15 is routed to the rear panel LO IN/OUT socket via C54, D17, C57 and board pin 24.

Programmed divider N3

122. The programmed divider, which is set to the same division ratio, N3, as that of the upper transfer loop board programmed divider, consists of a shaper stage, TR11, TR12, a divide-by-two stage, ML2a, two presettable decade counters ML3, ML5, with associated gates, and three J-K flip-flops, ML2b, ML9a, ML9b.

123. The two decade counters, ML3, ML5, have strobed parallel-entry capability such that the starting point of a count sequence may be preset. A '1' or '0' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Ao, Bo, Co, Do) when the strobe (S) input is at '0'. The counting operation is performed on the negative-going edge of the input clock pulse.

125. Frequency setting information from the front panel 30-way MHz switch is applied to the logic board where it is converted into a nines-complement code (Table 2). The nines-complement coded outputs from the logic board are applied to the data inputs of the two decade counters, 'units' to ML3 and 'tens to ML5, and preset the starting point of a count sequence.

126. To start the counting sequence, assume that a logic '0' strobe pulse is applied to the strobe (S) inputs of both ML3 and ML5 (at pin 1). As described in para.123, this causes the logic level applied to each input line (Da, Db, Dc, Dd) to be transferred to the corresponding output line (Ao, Bo, Co, Do). The negative going edge of the clock pulse (from the shaper stage, TR11, TR12 and the divide-by-two ML2a) is now applied to the clock 1 input of ML3 at pin 8. Each clock pulse is now counted until a count of 35 is reached, i.e. until the Ao and Co outputs from ML3 and the Ao and Bo outputs from ML5 are all at logic '1'. The C output from ML5 is applied to an inverter ML6d, to inhibit binary 7.

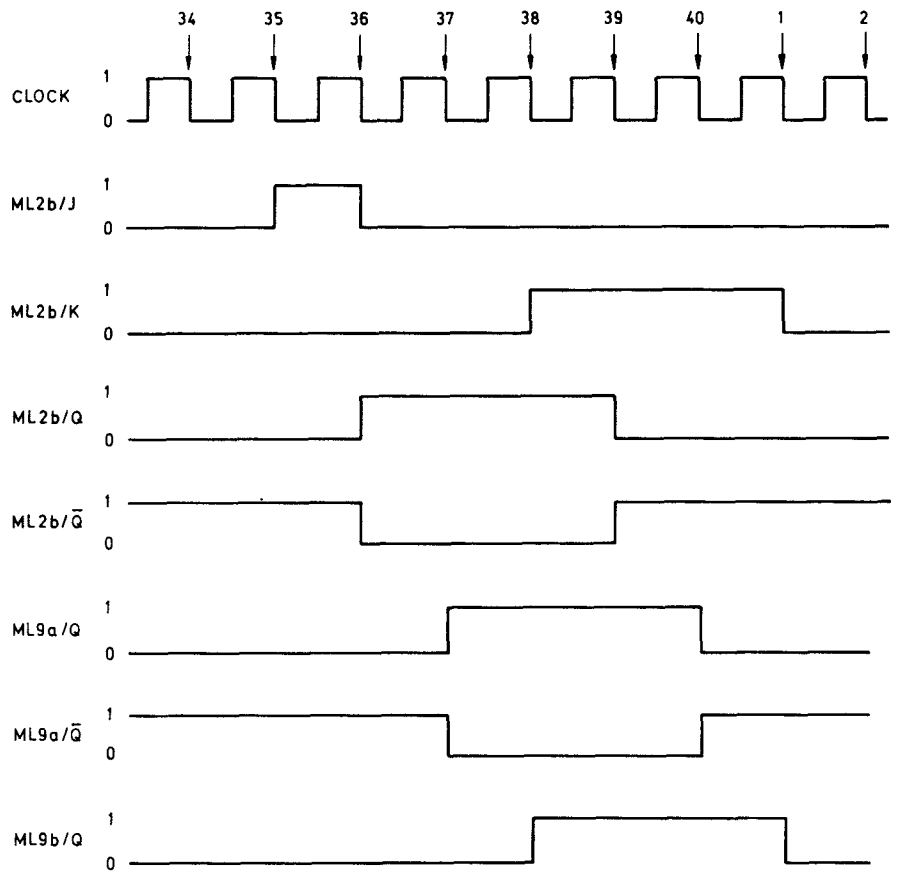
127. When a count of 35 is reached, the input lines to the AND gate, ML4b, are all at logic '1' and the '1' output, at ML4 pin 6, is applied to the J input of flip-flop ML2b. Both Q outputs from ML2b are fed to the dual J-K flip-flop, ML9 (Q to J, $\overline{Q}$ to K), and the Q output of ML9B is fed back to the K input of ML2b. The effect of this circuit is to produce a logic '0' strobe pulse (ML2b$\overline{Q}$) sufficient in width for the two decade counters, ML3 and ML5. As can be seen from the timing diagram, fig.12, the strobe pulse is extended to the negative-going edge of the 39th clock pulse, at which point the counting sequence is repeated.

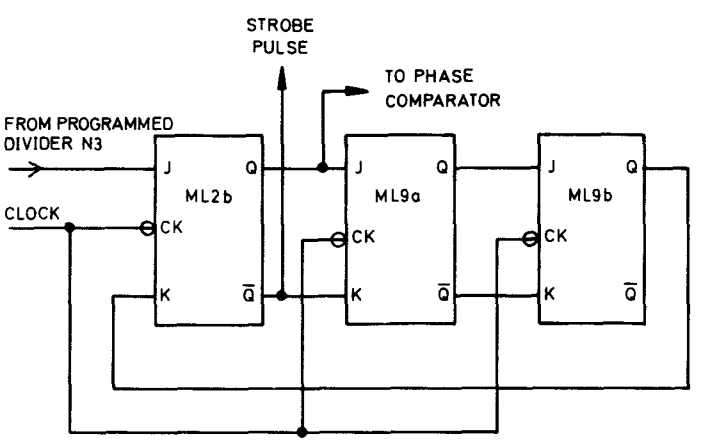
128. Table 7 shows the operation of the programmed divider for various settings of the MHz switch.

TABLE 7

Programmed divider operation (PS337)

'MHz' setting	Nines complement	Clock pulses			
		Count up to 100	Fixed count	Strobe pulse generation	Total division ratio
00	99	1	35	4	40
07	92	8	35	4	47
14	85	15	35	4	54
21	78	22	35	4	61
29	70	30	35	4	69





TRUTH TABLE (Each Section)		
tn		tn+1
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	Q̄n

Fig. 12 Timing diagram : strobe pulse generation(h.f. loop PS337)

Phase comparator

129. The phase comparator comprises a dual D-type flip-flop, ML7, a two-input NAND gate ML6 (pins 4, 5 and 6), and a voltage control circuit TR16, TR18, TR19. It compares the output frequency from the transfer loop oscillator (after division by two in ML12) with the output frequency from the programmed divider; the error is used to develop a compensating control voltage which is applied to the selected h.f. loop oscillator.

130. The programmed divider output, which is taken from ML2b pin 9, consists of positive-going pulses; these are applied to the clock input of ML7a. The output from the divide-by-two stage, ML12, at pin 5, is applied to the clock input of ML7b. The D inputs of both ML7a and ML7b are taken to the +5V rail (logic '1'). Thus when the positive edge from ML2b clocks ML7a, the Q output at pin 5 changes to '1' and the $\overline{Q}$ output changes to '0'. Similarly, when the positive edge from ML12 pin 5 clocks ML7b, the Q output changes to '1' and the $\overline{Q}$ output changes to '0'. When both Q outputs are at '1', the output from the NAND gate, ML6, changes to '0', clearing both ML7 flip-flops via R61 and thus resetting the Q outputs to '0' and the $\overline{Q}$ outputs to '1'.

131. Consider the case where the frequency of the selected h.f. loop oscillator output signal (which is applied to the programmed divider) is high. This will mean that the positive edge from ML2b will occur before the edge from ML12. The resultant setting and resetting of the flip-flops causes increased conduction of TR19, due to the $\overline{Q}$ output from ML7a (fig.5) as compared with the conduction of TR16; this causes a reduction in the varactor line voltage, taken from the collector of TR18, and thus a reduction in the frequency of the selected h.f. loop oscillator output signal.

132. If the frequency of the selected h.f. loop oscillator output signal is low, the edge from ML2b will occur after the edge from ML12; the $\overline{Q}$ output from ML7b will cause increased conduction of TR16, the voltage at the collector of TR18 will become more positive and this will cause an increase in the frequency of the selected h.f. loop oscillator output signal.

133. When the two frequencies are equal, the two flip-flops of ML7 are clocked at the same time, the $\overline{Q}$ waveform from ML7a is equal to that from ML7b and the varactor line voltage remains constant.

Lock indicator and fast lock circuit

134. The circuit comprises a monostable ML11, a D-type flip-flop ML12a, and two NAND gates ML6b, ML6c. Its purpose is to augment the conduction of TR16 or TR19 in the out-of-lock condition and so obtain a faster return to the locked condition; it also provides a lock indication output signal.

135. The Q output waveforms (fig.13) from the phase comparator, ML7a and b, are applied to NAND gates ML6b, ML6c, via integrating components R36, C92 and R60, C94 respectively, whilst the phase comparator $\overline{Q}$ output waveforms are applied to the A inputs of a monostable, ML11. Under phase-locked conditions, the in-phase positive-going Q output pulses from ML7a and ML7b are prevented from reaching ML6c, ML6b respectively due to the time constants presented by the integrating components; pins 9 and 12 of ML6, and also the D input of ML12a, are therefore at logic '0'. The resulting logic '1' outputs from ML6 pin 8 and 11 do not, however, affect the conduction of the voltage control transistors, TR16, TR18, TR19, due to D20 and D22.

136. ML11 is a negative edge-triggered monostable which produces a negative-going output pulse ($\overline{Q}$) of approximately 1.5 microsecond duration (timing

components R69, C75) when either or both of the A inputs are at logic '0' with the B input at logic '1'. (The B input is not connected externally and therefore floats up to logic '1'). Under phase-locked conditions, the in-phase negative-going phase comparator output pulses applied to ML11 produce a negative-going pulse train at ML11 pin 1 which clocks ML12a (positive-edge triggered) to produce a steady logic '1' in-lock signal at board pin 12 (fig. 13a)

137. If the output frequency from the programmed divider is low (fig.13b) the longer-duration positive-going output pulses at ML7b pin 9 are sufficient in width to overcome the time constant presented by integrating components R36 and C92. The effect of this, together with the $\overline{Q}$ output waveform from ML11, is to produce a negative-going output pulse from ML6b; this is applied to TR16, via D20, and rapidly increases the conduction of TR16 to bring about a fast return to the locked condition (in practice, a rapid succession of negative-going pulses appear at ML6b pin 11 as the programmed divider output frequency increases). At the same time, the combination of the D and CK waveforms applied to ML12a produce an alternating '0'-'1' out-of-lock signal at board pin 12.

138. Should the out-of-lock condition be due to a high programmed divider output frequency (fig.13c), the resulting longer-duration positive-going output pulses at ML7a pin 5 are sufficient in width to overcome the time constant presented by R60 and C94, and the negative-going output pulse at ML6c pin 8 will cause a rapid return to the locked condition by increasing the conduction of TR19; the output pulse from ML6c is also applied to the clear input of ML12a, and the combination of this and the $\overline{Q}$ output waveform from ML11 produces an alternating '0'-'1' out-of-lock signal at board pin 12, as before.

R.F. UNIT (fig. 37 and 39)

139. The r.f. unit consists of the re-radiation filter (fig.37) and the r.f. board PM582 (fig.39). Refer to fig.5 of Chap. 1-2 for the block diagram of the r.f. unit.

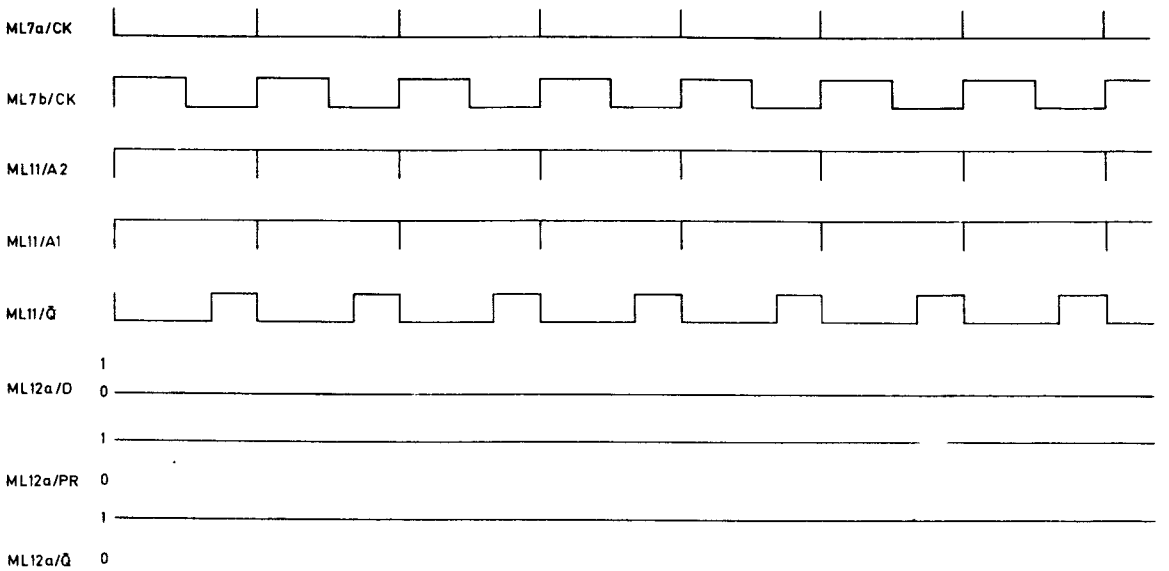
Re-radiation filter

140 The received signal at the antenna is applied to the r.f. board via a re-radiation filter and a 500 mA protection fuse. Capacitor C13 couples the received signal to the wideband protection stage.

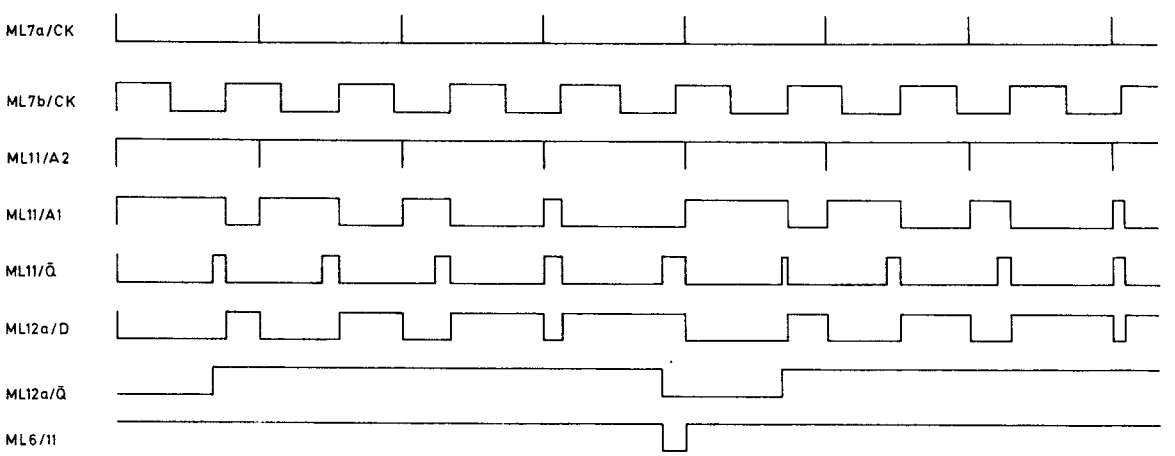
Wideband protection stage

141. This comprises transistors TR1, TR2, TR3, relay RIQ/1 and associated components. Under normal reception conditions, TR2 is turned off, TR3 is turned on and relay RIQ/1 is energized. Relay contact RIQ/1 is closed and the received signal is applied to a 30MHz low-pass filter, L7, L9, C14, C15, C16, C19 and C20.

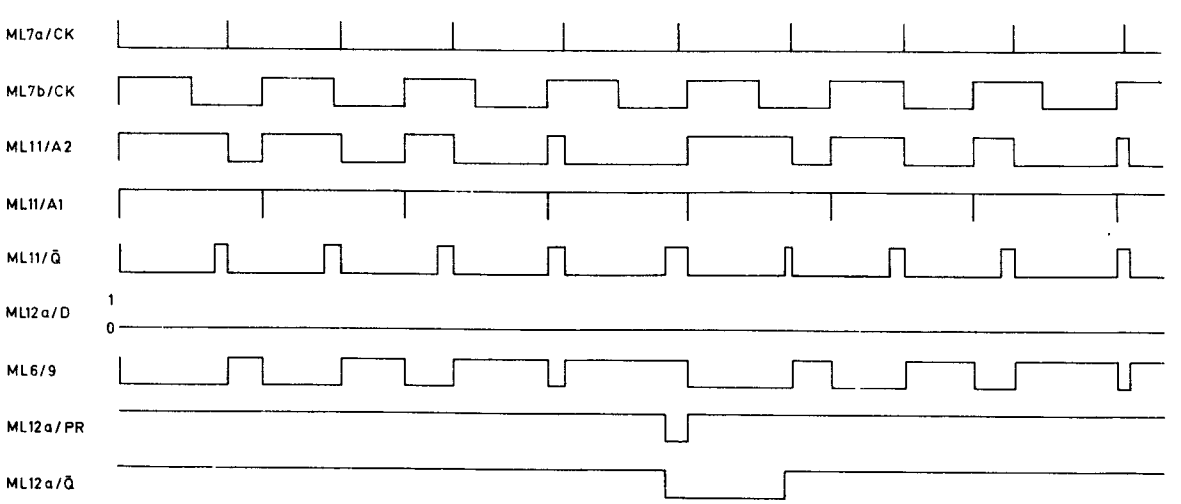
142. Should the amplitude of the received signal at the antenna socket exceed approximately 30V e.m.f. (threshold set by trimmer C31), the detected output from TR1, which is applied to the base of TR2, rises sufficiently positive to



(a) IN LOCK



(b) OUT OF LOCK (PROGRAMMED DIVIDER FREQUENCY LOW)



(c) OUT OF LOCK (PROGRAMMED DIVIDER FREQUENCY HIGH)

Fig. 13 Timing diagram : fast-lock and indicator (h.f. loop PS337)

cause TR2 to conduct. Conduction of TR2 causes TR3 to switch off, relay RLQ/1 is de-energised and contact RLQ/1 removes the received signal from the 30MHz low-pass filter.

Mute control

143. An earth, from the rear panel MUTE terminal, is routed to the base of TR3 via board pin 3 and diode D8. TR3 is turned off, relay RLQ/1 becomes de-energised, and the r.f. path to the 30MHz low-pass filter is broken.

R.F. signal path

144. The output signal from the 30MHz low-pass filter, which may be monitored at TP1, may take one of a number of paths dependent on the selected position of the front panel MHz switch, as follows:

(1) MHz switch set to 0MHz position: An earth from the MHz switch is routed to board pin 4. Relays RLA/1 and RLB/1 are energized, the received signal from the 30MHz low-pass filter is applied to the 1MHz low-pass filter via RLA1, and thence to the wideband r.f. amplifier via RLB1 and contact RLR1 of the normally energized protection relay,RLR/1

(2) MHz switch set to any position other than 0MHz and RF TUNE control set to WB (wideband): Microswitch SA, operated when the RF TUNE control is set to WB, routes an earth from the MHz switch at pin 13 to relays RLN/1 and RLP/1. The relays energized andthe received signal from the 30MHz low-pass filter is routed to the wideband r.f. amplifier via RLN1, RLP1 and contact RLR1 of the normally energized protection relay, RLR/1.

(3) MHz switch set to any position other than 0MHz, RF TUNE control not in WB position: An earth from the MHz switch is routed to the appropriate board pin (5 to 9) and the respective pair of relays are energised from a common +12V supply via the normally closed contacts of the microswitch, SA. The contacts of the selected relays close and the received signal from the 30MHz low-pass filter is applied to the appropriate tuned circuit, tuned by the RF TUNE control, and thence to the wideband r.f. amplifier via RLR1.

145. Contact 'wetting' for the reed-type control relays is provided from the +12V rail via resistors R9 and R11.

Protection stage

146. A further protection stage is fitted to allow 'working-through' off-tune signals of up to approximately 10V e.m.f. at the antenna socket. The circuit, which is similar to that of the wideband protection stage, comprises transistors TR4, TR7, TR8, relay RLR/1 and associated components. Under normal reception conditions TR7 is turned off, TR8 is turned on and relay RLR/1 is energized. Relay contact RLR1 is closed and the received signal is applied via C42 to the wideband r.f. amplifier.

147. Should the amplitude of the r.f. signal applied to the protection stage exceed approximately 10V e.m.f. (threshold set by C33) the detected output from TR4, which is applied to the base of TR7, rises sufficiently positive to cause TR7 to conduct. This causes TR8 to switch off, relay RLR/1 is de-energized and contact RLR/1 opens to remove the input to the wideband r.f. amplifier.

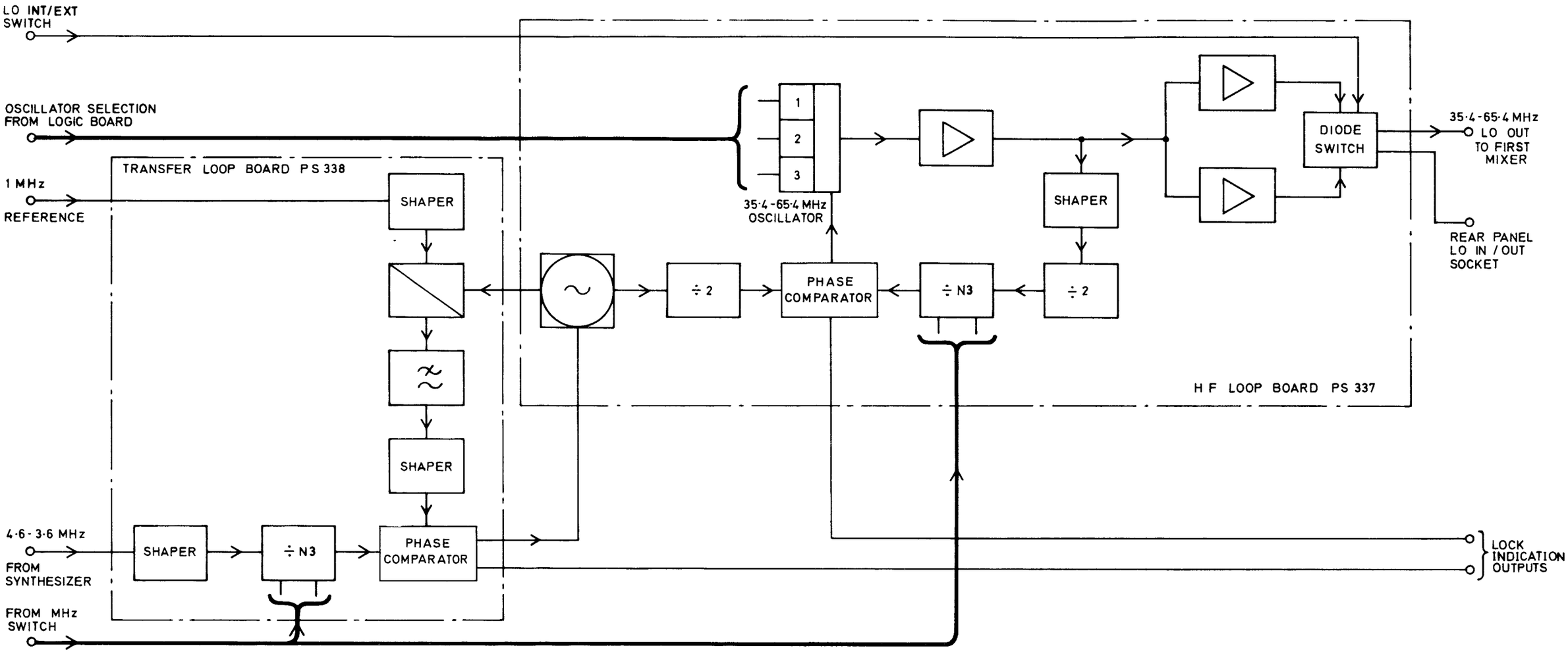


Fig. 14 Block diagram: upper transfer and h.f. loop board PS338 and PS337

Wideband r.f. amplifier

148. The wideband r.f. amplifier, TR5, TR6 is of conventional design. The amplified output is coupled by C51 to a five-section 30MHz low-pass filter and is then applied to the first mixer via board pin 12.

FIRST MIXER BOARD PM335 (fig.41)

149. Refer to fig.6 of Chap.1-2 for a block diagram of the first mixer board.

150. The 35.4 to 65.4 MHz local oscillator signal, from the frequency synthesizer, is applied to one of two band-pass filters, dependent on the setting of the front panel MHz switch. For settings of 0, 1, 2 or 3 MHz, an earth from the MHz switch is applied to board pin 11; this is routed to diode D1 via L2 and also to D3 via L11. Diode D1 becomes forward biassed and opens a path for the local oscillator signal at board pin 10 to a crystal notch filter (passband 35.415 to 39.4MHz with a notch frequency of 35.400MHz) via C2, D1 and C6. Diode D3 is also forward biassed and allows the output from the crystal filter to be applied to the drive amplifier via C20, D3 and C24. Diodes D2 and D4 are both reverse biassed, via the potential dividers R3, R4, R6 and R9, R11, R12 respectively, and thus isolate the LC band-pass filter.

151. For MHz switch settings between 4 and 29MHz inclusive, the earth is applied to board pin 8. This causes diodes D2 and D4 to become forward biassed and diodes D1 and D3 to become reverse biassed. Thus a path is opened for the local oscillator signal via the LC band-pass filter (pass-band 39.4 to 65.4MHz) whilst the crystal filter becomes isolated.

Drive amplifier

152. The mixer drive amplifier comprises transistors TR1, TR2 and TR5. The local-oscillator signal from the selected filter, which may be monitored at TP5, is coupled by C28 to a common-emitter amplifier TR1. This is followed by an emitter-coupled differential amplifier, TR2, TR5 and the balanced output is coupled by transformer T4 to the mixer circuit via transformer T6.

153. A second output from transformer T4 is rectified by diode D5 to provide a d.c. output via TR8 and board pin 5. This is fed to the meter switching board and provides a meter indication of the DRIVE LEVEL to the first mixer.

Mixer

154. The mixer is of the balanced bridge type and uses four n-channel insulated gate field effect transistors, TR3, TR4, TR6 and TR7. The local oscillator signal from T6 is capacity coupled to the gate of each transistor (via pin 30 to TR4 and TR6; via pin 26 to TR3 and TR7) whereas the r.f. input from the r.f. unit is coupled by transformer T7 to the source of each transistor (via pin 16 to TR3 and TR6; via pin 27 to TR4 and TR7). The mixer output is taken via transformer T5 from the drains of the four transistors and is applied to a 35.4MHz band-pass filter, FL1. Finally, the output from FL1, at the first intermediate frequency of 35.4MHz, is applied to the second mixer board via transformer T3 and board pin 3.

SECOND MIXER BOARD PM336 (fig.43)

155. Refer to fig.7 of Chap.1-2 for a block diagram of the second mixer board.

156. The 35.4MHz first i.f. output from the first mixer is applied to an amplifier stage, TR1, via board pin 13 and C1. The amplified output is applied

via C8 to a further amplifier stage, TR5, and is also applied via C7 to a voltage-controlled attenuator. This utilises two PIN diodes, D1, D2, and is controlled by the AGC1 and AGC2 input voltages at board pins 9 and 8, from the main and i.s.b. i.f./a.f. boards respectively.

PIN diode attenuator

157. The impedance presented to the 35.4MHz i.f. signal by the PIN diodes is a function of the forward direct current passing through the diodes. When no forward current is allowed to flow the impedance is extremely high and this impedance is progressively reduced as the forward current is allowed to rise.

158. The AGC voltage output from the emitter follower TR7 (or, in the ISB mode, the differential AGC output from TR7, TR8) is applied to the base of TR6. This stage controls the current flow through TR2 and TR3, and hence the current flow through the two PIN diodes, D1 and D2. Thus an increase in the AGC voltage causes an increased current to flow through the PIN diodes and the output from the tuned circuit of TR1 is reduced.

Mixer

159. A cross-coupled balanced mixer circuit, TR9, TR10, produces the 1.4MHz second intermediate frequency, this being the difference frequency between the 35.4MHz first i.f. and the second mixer injection signal from the 34MHz generator board. The 35.4MHz output signal from TR5 is applied via a band-pass filter to the base of TR9 and the 34MHz signal at board pin 7 is applied via a band-pass filter to the base of TR10. The output from the mixer is applied to a 1.4MHz i.f. amplifier stage, TR11, which has a stage gain of approximately 10dB, and the final output is applied to the i.f. filter board via pin 3.

I.F. FILTER BOARD PS367 (fig.45)

160. This board contains all the crystal filters which are used in the control of received signal selectivity. Filter selection is effected by applying an earth to the appropriate selection line and the filtered output is taken via diode switches to a common output line.

► Note...

Due to the inversion within the receiver, the filter selected for USB operation will have LSB characteristics, and that selected for LSB operation will have USB characteristics. ◄

161. Since the selection circuit for each filter is the same, only one example is given, that of filter FL1 , the carrier filter is permanently selected.

162. An earth from the MODE switch is applied to board pin 15. This is routed via L1 and L8 to diode D1, and also via L14 to diode D7. Diode D1 becomes forward biassed and opens a path for the i.f. signal at board pin 14 to FL1 via capacitor C2, D1, C3 and R8. Diode D7 is also forward biassed and the output from FL1 is routed to board pin 2 via C27, D7 and C35. The remaining diodes, D2 to D6 and D8 to D12, are all reverse biassed and isolate the i.f. signal from the remaining filters, FL2 to FL6.

MAIN I.F./A.F. BOARD PM364/1 (fig.48)

163. Refer to fig.8 of Chap.1-2 for a block diagram of the i.f./a.f. board.

164. The 1.4MHz i.f. signal from the filter board is applied to an integrated circuit gain-controlled amplifier, ML1. This device contains two amplifier sections which, in this application, are connected in cascade to provide high gain and a.g.c. range. The input signal is applied via C1 to pin 1 and the output from the first section, at pin 12, is applied via R3 and C7 to the input of the second section, at pin 10. The output, which is taken from pin 7, is applied via a band-pass filter and C12 to an i.f. output amplifier, TR2, TR4 and TR6. The output from TR6 is taken to the rear panel MAIN IF OUT socket via C23, R100 and board pin 2.

A.G.C. detector and amplifier stages

165. A second output from amplifier TR2 is coupled by C19 to the a.g.c. detector, TR7, TR9, and is also fed via C30 to the hang detector, TR11, switching amplifier stages ML3, ML4 and TR13 (para.168). The positive output voltage from the a.g.c. detector is taken from the emitter of TR7 and is applied to the switched time constant capacitors, C13, C14, C16 and C20, via R20. The front panel a.g.c. switch, when set to SHORT, routes an earth to board pin 25 and this connects R13 across the series/parallel connected time constant capacitors (effective total capacitance approximately 25μF). When the a.g.c. switch is set to LONG the earth is transferred to board pin 26; R13 is disconnected and capacitors C14 and C16 are short circuited to produce a time constant capacitance of 66μF (parallel combination of C13 and C20).

166. ML2 is connected as a linear amplifier. The output at pin 6 is applied via diode D2 and board pin 29 to various points within the receiver and also via the LONG and SHORT positions of the a.g.c. switch to board pin 30. Transistor TR1 and variable resistor R4 provide a means of shifting the d.c. level of the a.g.c. voltage before it is applied to the i.f. amplifier stage, ML1. When the a.g.c. switch is set to OFF a positive voltage is applied to board pin 30 via the manual IF GAIN control.

Hang detector

167. This circuit holds the level of the a.g.c. output voltage from ML2, following an interruption in the received transmission, for a period of approximately 2.5 seconds. The circuit is only operative when the a.g.c. switch is in the LONG position.

168. The i.f. output from TR2 is coupled to the base of detector TR11 via C19 and C30. The output from TR11 is applied to the inverting input of ML3 and the preset variable resistor R42 sets the voltage level applied to the non-inverting input such that the output at ML3 pin 6 is negative (clamped to approximately -0.7V by D7) when a received signal is present. This negative voltage is applied to the inverting input of ML4. The potential divider, R48, R49, sets the voltage applied to the non-inverting input of ML4 to approximately +7V and the resulting positive output, at ML4 pin 6, is applied to the base of TR13 via R53. Since this voltage is more positive than that applied to the emitter of TR13 (which is held at approximately +7V) the transistor is switched off and the resulting negative voltage at the collector of TR13 holds off TR3 via D9. Board pin 24 is taken to earth by the a.g.c. switch when set to LONG (as is pin 26).

169. When a break in the received transmission occurs the corresponding reduction in the emitter current of TR11 causes the voltage level applied to pin 2 of ML3 to fall below the preset voltage level applied to pin 3 (of ML3). The output from ML3 switches from negative to positive and capacitor C38 charges, via R45 and R46. Once the level of the exponentially rising voltage at ML4 pin 2 exceeds the level of the fixed potential applied to ML4 pin 3

(approximately +7V), the output of ML4, at pin 6, switches from positive to negative. TR13 conducts, the negative voltage applied to D9 is removed and TR3 conducts. The time constant capacitors C13 and C20 discharge via R17 and TR3 and the a.g.c. voltage output from ML2 falls exponentially to zero.

170. When the received transmission recommences, the emitter voltage of TR11 rises, the output of ML3 switches from positive to negative and C38 rapidly discharges via R46, D8 and the low impedance output circuit of ML3. The output of ML4 switches from negative to positive, both TR13 and TR3 are cut off and the a.g.c. voltage from TR7 charges the time constant capacitors, C13 and C20, via R20.

171. The operation of the hang detector circuit, as described above, and also where the duration of the break in the received signal is shorter than the hang time period, is shown in the waveform diagram, fig.15.

A.M. and s.s.b. detectors

172. The i.f. output from ML1 and the band-pass filter is coupled to a buffer stage TR8, via C12 and C15. The output from TR8, at TP4, is capacity coupled to both the a.m. detector, via C26, and the s.s.b. detector, via C29.

173. The low distortion a.m. detector, TR10, is followed by a low-pass filter, L5, R37, C31. A similar filter follows the s.s.b. detector which consists of a modified Foster-Seeley circuit, T1, D3 to D6, R43 and C33.

174. A diode switching arrangement, controlled by the MODE switch, is used to select the output from either the a.m. detector or the s.s.b. detector. In the AM position of the MODE switch, an earth is applied to board pin 7; this is routed to D11 via R52, the diode becomes forward biassed, and a path is opened for the output from the a.m. detector to the audio pre-amplifier via C37, D11 and C40. Diode D10 remains reverse-biassed and isolates the output from the s.s.b. detector.

175. For all remaining positions of the MODE switch, the earth is transferred to board pin 6. Diode D10 becomes forward-biassed and opens a path for the output from the s.s.b. detector whilst D11 becomes reverse-biassed and isolates the output from the a.m. detector.

Audio pre-amplifier

176. The output from the selected detector is applied to a high gain, impedance matching amplifier, TR14, TR15. The output, which is applied to the MODE switch and the preset u.s.b. line level control, via C41 and board pin 8, is muted by transistor TR16 when an earth is applied to board pin 10.

Audio line amplifier

177. The audio line amplifier consists of an integrated circuit linear amplifier, ML5, which drives the complementary output transistors, TR22 and TR23. The output signal, from the preset USB line level control, is applied to ML5 via board pin 11, C45 and a low-pass filter, R74 and C49. The audio line output is taken to the rear panel terminals via transformer T2 and board pins 15 and 16.

Loudspeaker amplifier

178. The input to the loudspeaker amplifier is switched (MODE switch) to receive either the pre-amplifier output from the main i.f./a.f. board (u.s.b.)

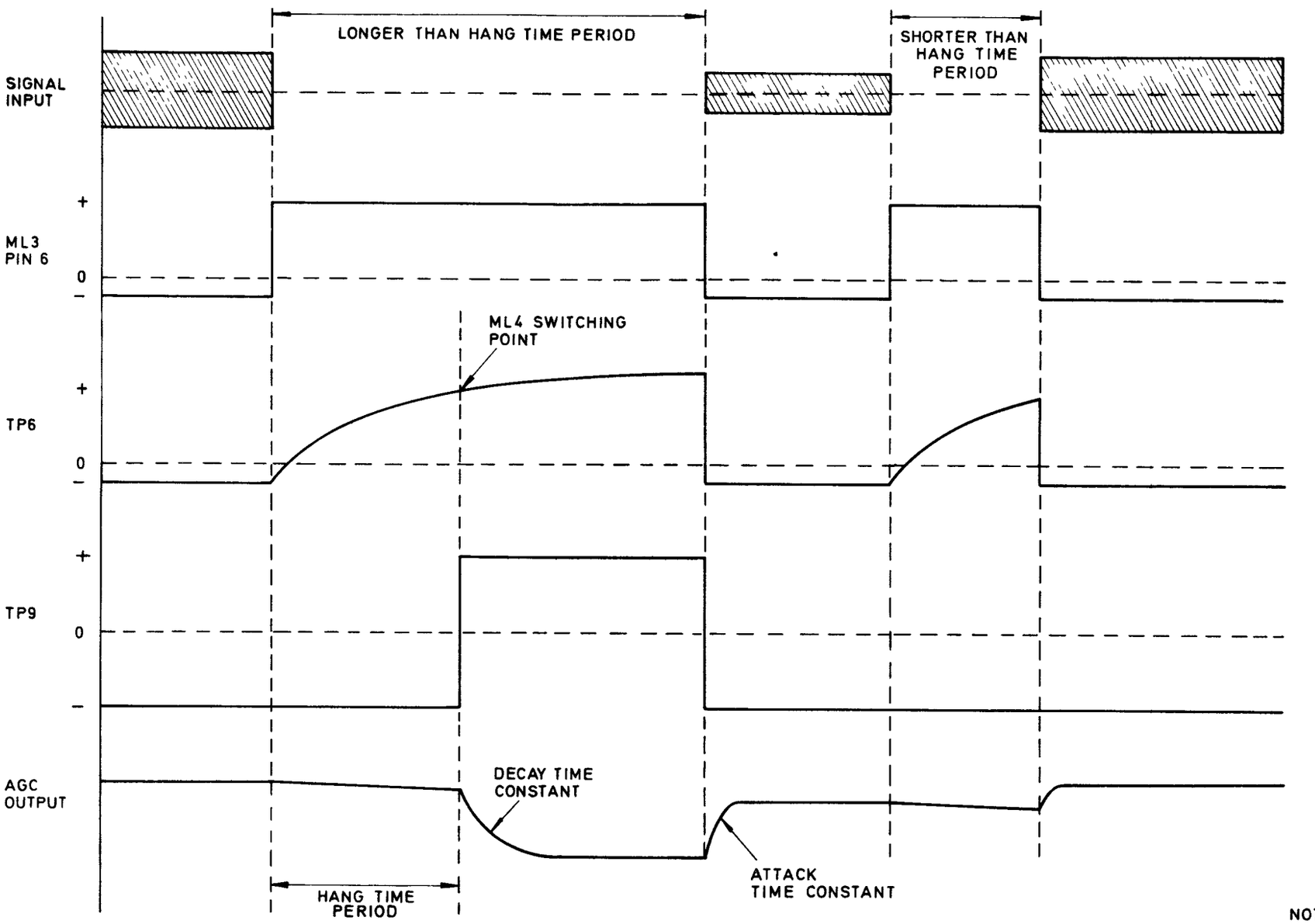


Fig.15

AL1, Mar. 76

Waveform diagram (idealised): a.g.c. hang detector

or that from the i.s.b./i.f./a.f. board (l.s.b.)

179. The direct-coupled amplifier comprises transistors TR17 to TR21, TR24 and TR25. The input from board pin 23 is applied to the input stage, TR17, via C42 and a low-pass filter, R69 and C47 with feedback components C46 and R72. This is followed by a further amplifier stage, TR18, with negative-feedback provided by C51. TR19 provides bias for the output transistors and R84 sets the quiescent current. Phase splitting is achieved by the use of complementary transistors, TR20, TR21, which drive the single-ended push-pull output stage, TR24, TR25. The amplifier output, at board pin 18, is taken direct to the rear panel loudspeaker terminal and via dropper resistors to the two headphone jacks and the internal loudspeaker.

I.S.B./I.F./A.F. BOARD PM364/3 (fig.48)

180. This board is similar to the main i.f./a.f. board except that it does not contain the loudspeaker amplifier components. The component layout for the board is given in fig.47.

A.F.C. BOARD PM369 (fig.50)

Input attenuator and amplifier

181. The 1.4MHz carrier signal is applied to an automatic gain-controlled i.f. amplifier stage, ML3, via an attenuator which is controlled by the front panel AFC switch. When this switch is set to FULL CARRIER, an earth is applied to board pin 14. Diode D3 becomes reverse-biassed, diodes D2 and D4 become forward-biassed and the carrier signal is routed to ML3 via C2, D2, attenuator resistors R4, R7, R8, R12, R14, D4 and C12. When the AFC switch is set to PILOT CARRIER, the earth is removed from board pin 14, diode D3 becomes forward-biassed, diodes D2 and D4 become reverse-biassed and the unattenuated carrier signal is applied to ML3 via C5, D3 and C11.

182. The i.f. amplifier ML3 contains two sections which, in this application, are connected in cascade. The input signal to the first section is applied to pin 14; the output at pin 12 is coupled by C27 to the input of the second section, at pin 10, and the final output, at pin 7, is applied to a balanced mixer via a 200Hz crystal band-pass filter.

Mixer

183. The mixer consists of transformer T1, diodes D5 to D8, C35, C36 and output transformer, T2. The 1.4MHz signal is applied to the primary winding of T1 and the 1MHz reference frequency, at board pin 11, is applied to the centre-tap of the secondary winding of T1 via R104, C18, shaper stage TR5, TR6, and C28. The resultant 400kHz output signal is applied to a cascaded two-stage amplifier, ML12, and is then buffered by emitter-follower, TR10, before being applied to a sample-hold phase comparator.

1.6MHz v.c.o.

184. The second input signal to the phase comparator is derived from a 1.6MHz v.c.o. This consists of transistors TR7 and TR8 with a varactor-diode-contt-rolled tuned circuit D9, C30, C31, L8 and C34. The square-wave output from TR8 is applied to a divide-by-two stage consisting of a D-type flip-flop, ML11a. The Q output from ML11a is applied to a further divide-by-two stage, ML11b, and the resulting 400kHz output at ML11b, pin 8 is applied as the sample pulse to the phase comparator via C58 and TR14.

Phase comparator

185. The sample-hold phase comparator compares the 400kHz output signal from the mixer (via ML12 and TR10) with the 400kHz reference frequency output signal from ML11b. Any frequency or phase error between these two signals is used to develop a direct voltage which is fed back to the 1.6MHz v.c.o. to eliminate the error. The action of the circuit is as follows.

186. The square-wave output from ML11b, pin 8 is applied to the differentiating components C58, R56, and the resulting sample pulse is applied to the base of TR14. When the base of this transistor is positive with respect to its emitter, it conducts and holds off TR13 by effectively connecting the gate of TR13 to 0V. Thus the negative-going edge of the sample pulse turns off TR14 and this allows TR13 to conduct for the duration of the sample pulse. The voltage level of the 400kHz signal, at the source of TR13, is transferred to the drain and this voltage, which is held by C61, is applied to the varactor diode, D9 of the 1.6MHz v.c.o., via the loop amplifier ML15, and the loop filter R73, C67. A potential divider R79, R80, and diode D13 prevent the level of the varactor line voltage falling below approximately +3V.

187. Incorrect phase-lock is prevented by the use of a quadri-correlator stage which comprises transistors TR15, TR16, TR24, TR25 and TR18. The 400kHz reference frequency square wave output from ML8a, which is 90° out of phase with that from ML11b, is applied to the differentiating components C56 and R55. The resulting negative-going sample pulse is applied to the base of TR16 to allow conduction of TR15 for the duration of the sample pulse. The voltage level of the 400kHz signal, at the source of TR15 (from TR10), is transferred to the drain and this voltage, which is held by C62, is applied to a differential amplifier TR24, TR25. Under phase-locked conditions, TR25 is on and both TR23 and TR24 are off. Thus TR18, which controls the phase comparator FET, is off, as is TR26 which feeds the out-of-lock stage (fig.50b).

188. The voltage across C62 varies according to the instantaneous voltage from the source of TR15, seen at the time of the sampling pulse. Should this voltage fall too far, when a phase error exists, TR24 and TR25 will switch on and TR13 will be inhibited via TR18 and TR23 to prevent further sampling. This ensures that sampling can only occur when C62 sees the peak of the 400kHz signal at the source of TR15, and further ensures that a voltage variation arising from a phase error is always of the correct sense to restore lock (fig.16).

189. Under phase-locked conditions the amplitude of the quadri-correlator output waveform, at TP12, is proportional to the amplitude of the received carrier. This output, therefore, is used to generate an a.g.c. voltage, and is also applied to the signal-to-noise ratio detector ML21.

A.G.C. stages

190. The quadri-correlator output voltage, held by C62, is applied via R71 to an operational amplifier ML16. This feeds a voltage follower stage ML24, which in turn feeds a buffer stage ML19, via the a.g.c. time constant components D12, R106, C81 and R109. C81 charges rapidly via D12 and R106 whilst a slow discharge path is provided by R109.

191. Transistor TR28 is controlled by the front panel AFC switch, via D1, G1 and G4 (fig. 50b) such that in the OFF position the transistor conducts and removes the input to ML24.

192. The output from ML19 is applied to output buffer stages ML22, ML23, and also to ML3 via R97, a d.c. level shift stage TR27, LK1 and L5.

Signal-to-noise ratio detector

193. The signal-to-noise ratio detector consists of an operational amplifier, ML21. The output from the quadri-correlator is applied to the non-inverting input,and the noise-threshold potentiometer, R87, sets the voltage level to the inverting input. The output from ML21 for an acceptable signal-to-noise ratio (normally 10dB) consists of a positive voltage (clamped to +4.7V by R100 and D17) and this changes to 0V onee the noise-threshold is exceeded.

Divide-by-16 stage

194. The 400kHz square-wave signal (plus or minus any frequency deviation D) from ML8a pin 5 (fig.50a) is applied to the divide-by-two section of ML5 at pin 8 (fig.50b). The resulting 200kHz ± D/2 output is taken from ML5 pin 5; it is then applied (when the a.f.c. is switched on) to the divide-by-8 section of ML6, at pin 6, to produce a 25kHz ± D/16 output at ML6 pin 12. This is applied via a NAND gate switch, G7, as one input to a digital phase comparator, ML9, at ML9a pin 3.

Divide-by-40 stage

195. The 1MHz reference frequency signal (from R104, fig.50a) is coupled by C9 to a shaper stage consisting of TR2 and NAND gate G2. The square-wave output from G2 is applied to the divide-by-five section of ML5, at pin 6; the resulting 200kHz output is then fed to the divide-by-eight section of ML7, at pin 6, and the 25kHz output at ML7 pin 12 (when the a.f.c. is switched on) is applied via a NAND gate switch, G9, as the second input to the digital phase comparator, ML9, at ML9b pin 11.

Digital phase comparator

196. The digital phase comparator consists of a dual D-type flip-flop, ML9a, ML9b, a two-input NAND gate, G10, and a voltage control circuit comprising transistors TR9,TR11 and TR12. It compares the 25 kHz ± D signal from ML6 with the 25kHz reference frequency signal from ML7 (which is derived from the 1MHz reference frequency). Any error existing between these two signals, due to a frequency deviation of the received signal, is used to develop a direct voltage which is applied via a hold switch, loop filter and loop amplifier (fig.9, Chap. 1-2) to a 7MHz v.c.o. The action of the circuit is described below, in conjunction with the timing diagram fig. 17.

197. The output from ML6, pin 12, is applied via a NAND gate switch G7, to the clock input of ML9a. The output signal from ML7, pin 12, is applied via a NAND gate switch, G9, to the clock input of ML9b. The D inputs of ML9 are not connected and float up to logic '1'. Thus when the positive edge from G7 clocks ML9a, the Q output at pin 5 changes to '1' and the $\overline{Q}$ output at pin 6 changes to '0'. Similarly, when the positive edge from G9 clocks ML9b, the Q output changes to '1' and the $\overline{Q}$ output changes to '0'. When both Q outputs are at '1' the output from the NAND gate, G10, changes to '0' clearing both flip-flops via R44 and thus resets the Q outputs to '0' and the $\overline{Q}$ outputs to '1'.

198. Consider the case where the output frequency from the ML6 is high, due to an increase in the frequency of the received signal. This will mean that the positive edge from ML6 will occur before the positive edge from ML7. The

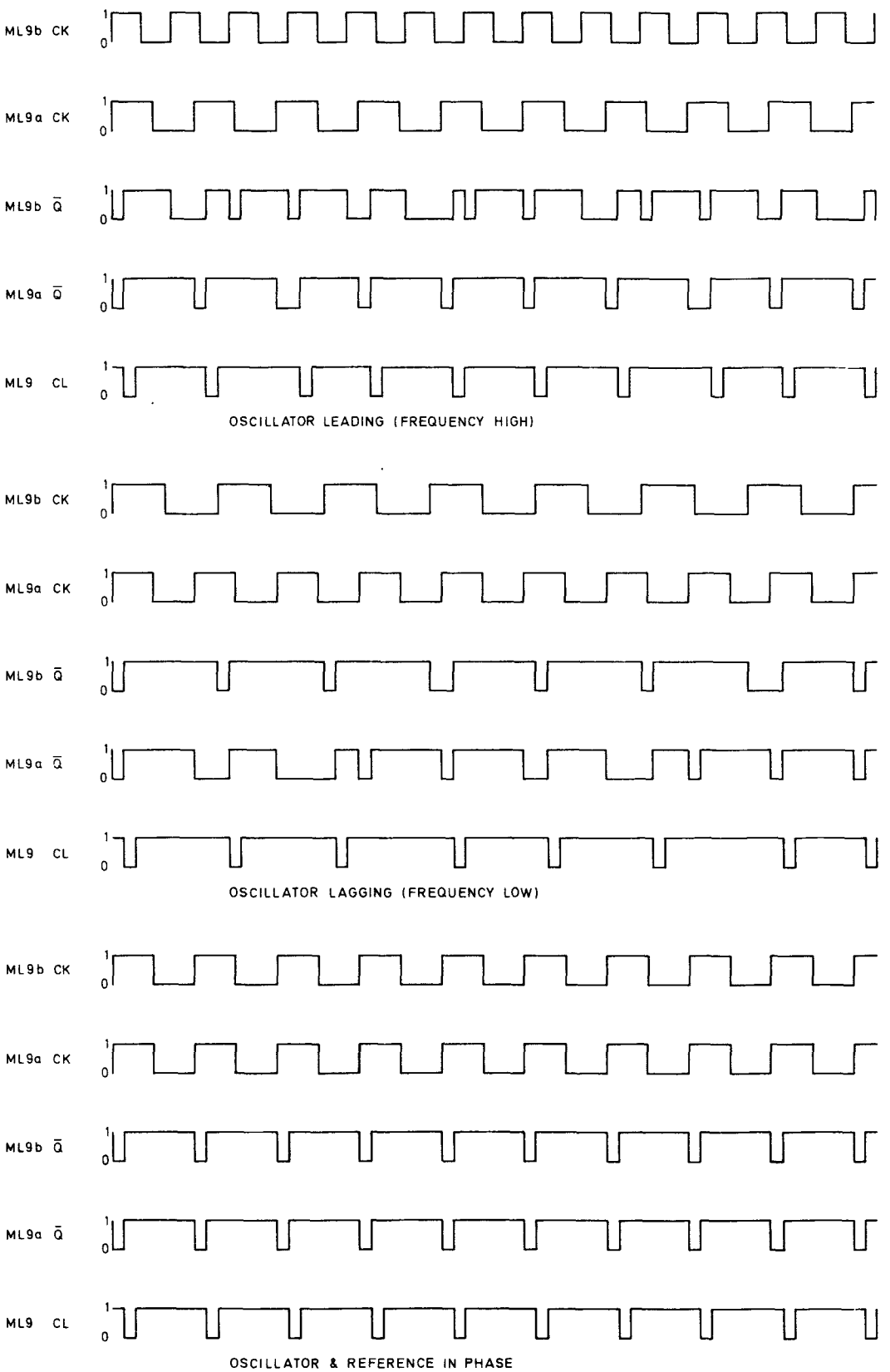


Fig.17 Timing diagram : a.f.c. digital phase comparator

resulting setting and resetting of the flip-flops causes increased conduction of TR9, due to the $\overline{Q}$ output waveform from ML9a (fig.17) as compared with the conduction of TR12; this causes the voltage at the collector of TR11 to become more positive, thereby increasing the voltage applied to the varactor diode of the 7MHz v.c.o. Thus the frequency of the 7MHz v.c.o. is increased in proportion to the increase in the frequency of the received signal.

199. If the output frequency from ML6 is low, due to a reduction in the frequency of the received signal, the positive edge from ML7 will occur before the edge from ML6. The Q output waveform from ML9b causes increased conduction of TR12, the voltage at the collector of TR11 becomes less positive, and the reduced voltage applied to the varactor diode of the 7MHz v.c.o. causes a corresponding reduction in the v.c.o. frequency.

200. When the two signals are equal in frequency and phase, the two flip-flops of ML9 are clocked at the same time, the two Q output waveforms are equal and the varactor line voltage remains constant.

Loop filter and amplifier

201. The output voltage from the collector of TR11 is applied to a loop filter, R72, C63, C64, via a hold switch, TR19. This transistor is switched off by the conduction of TR20 when either a loss of phase-lock of the 1.6MHz v.c.o. occurs (para.184) or a poor signal-to-noise ratio exists at the receiver input.

202. A guard ring, which is connected to the collector of TR22, is fitted around the loop filter components to prevent the inadvertant discharge of C63, as could otherwise occur, for example, due to moisture on the printed circuit board.

203. The loop filter is followed by a buffer amplifier, TR21, and a d.c. level shift stage consisting of variable resistor R74 and TR22. The varactor line voltage output, at TP4, is applied to the 7MHz v.c.o. and also to the meter switching board for carrier tuning purposes via R81, RIA/1 and board pin 7.

7MHz v.c.o.

204. This consists of transistor TR1 connected into a crystal-controlled Colpitts circuit with the parallel combination of preset trimmer C3 and varactor diode D11 in series with the crystal, XL1. The v.c.o. is driven to a frequency which is equal to 7MHz ± 7D*34, where D is the deviation of the received signal. The output signal is coupled by C10 to a shaper stage, TR3 and NAND gate G3, and the square-wave output signal is applied to a divide-by-seven stage, ML4.

Divide-by-7 stage

205. ML4 utilises a type of decade counter where the starting point of a count sequence may be preset. A '1' or a '0' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Ao, Bo, Co, Do) when the strobe (S) input is at '0'. The counting operation is performed on the negative-going edge of the clock pulse.

206. In this application, the Da data input is not connected and thus floats up to logic '1' (approximately +5V) whilst the remaining data inputs (Db, Dc, Dd) are all taken to logic '0' (0V). The counter therefore starts counting at binary 1 and resets at binary 8, i.e. at binary 8 the logic '1' Do output, inverted by G5, resets or strobes the counter, binary 1 is again loaded in and

the count sequence repeats.

207. The shaped output signal from the 7MHz v.c.o. is divided by seven and the resulting 1MHz ± D÷34 output is taken from ML4 pin 2. This is applied via board pin 10 to the 34MHz generator board where it is used in place of the 1MHz reference frequency derived from the frequency standard.

Carrier tuning indicator

208. The 200kHz ± D÷2 square wave output from ML5 pin 5 is applied to the D input of flip-flop ML8b, whilst the 200kHz reference frequency square wave from ML5 pin 12 is applied to the clock input of ML8b. The resultant square wave output from ML8b pin 9, the frequency of which is equal to D÷2, is applied to the negative edge-triggered inputs (A1 and A2) of a monostable, ML10. The B1 and B2 inputs of ML10 (not shown on the circuit diagram) are not connected and thus float up to logic '1'.

209. The negative-going edges of the output waveform from ML8b, therefore, trigger ML10 to produce a negative-going pulsed output signal of a fixed pulse width at a repetition rate equal to the difference frequency, D÷2. This signal is applied via G15, R94, RLA/1 and board pin 7 to the meter switching board where it is used for carrier tuning purposes.

A.F.C. lock detector

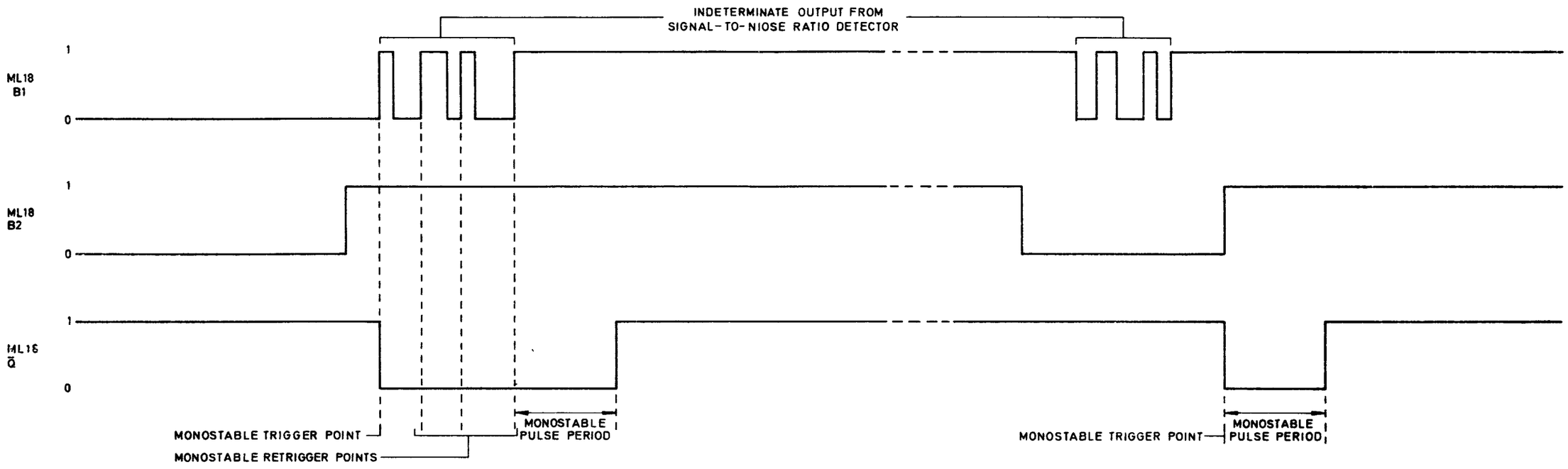
210. The output from the signal-to-noise ratio detector (ML21, fig.50a) is applied to the B1 input of ML18 and also to pin 11 of NAND gate G16 via R92, D15. The input to B2 of ML18 is from the 1.6MHz v.c.o. phase-locked loop lock detection circuit via TR26 (fig.50a) and this signal is also fed to pin 10 of NAND gate G16, via R95, D16.

211. ML18 is a retriggerable monostable. A positive-edge input, applied to one of the B inputs, will trigger the monostable provided the A1 and A2 inputs are at logic '0' (0V) and the remaining B input is at logic '1'. When the monostable is triggered, the Q output, which is normally at logic '1', will pulse to logic '0' for a period of time determined by the timing components R83, D14 and C69 (approximately 500 ms).

212. The purpose of the monostable is to allow time for all the stages (fig.50b) to stabilize following phase-lock of the 1.6MHz phase-locked loop; it also prevents the a.f.c. lock circuit from being driven rapidly between the locked and unlocked states due to an indeterminate output from the signal-to-noise ratio detector. The operation of the monostable is shown in the timing diagram fig. 18.

213. The output from G16 ('0' for in-lock, '1' for out-of-lock) is inverted by G13 and is then applied as one input to each of the four-input NAND gates, G14 and G15. G14 controls the a.f.c. lock lamp such that the lamp glows when all the inputs to G14 are at logic '1'. G15 applies the inverted form of the output signal from the tuning indicator (ML10 pin 6) to the meter switching board provided that the remaining inputs to G15 are at logic '1' and that the AFC switch is set to OFF (para.221).

214. The lock detector for the 7MHz v.c.o. phase-locked loop consists of buffer NAND gates, G11, G12, and a positive-edge-triggered dual D-type flip-flop, ML14a, ML14b. The Q outputs of the phase comparator flip-flops, ML9a and ML9b, are applied to the D inputs of ML14a and ML14b respectively; the clock input of ML14a is fed from NAND gate switch, G7, and inverter G11, whilst the clock input of ML14b is fed from NAND gate switch, ML2, and



NOT TO SCALE

Fig. 18

Timing diagram: lock detector monostable (a.f.c. board PM369)

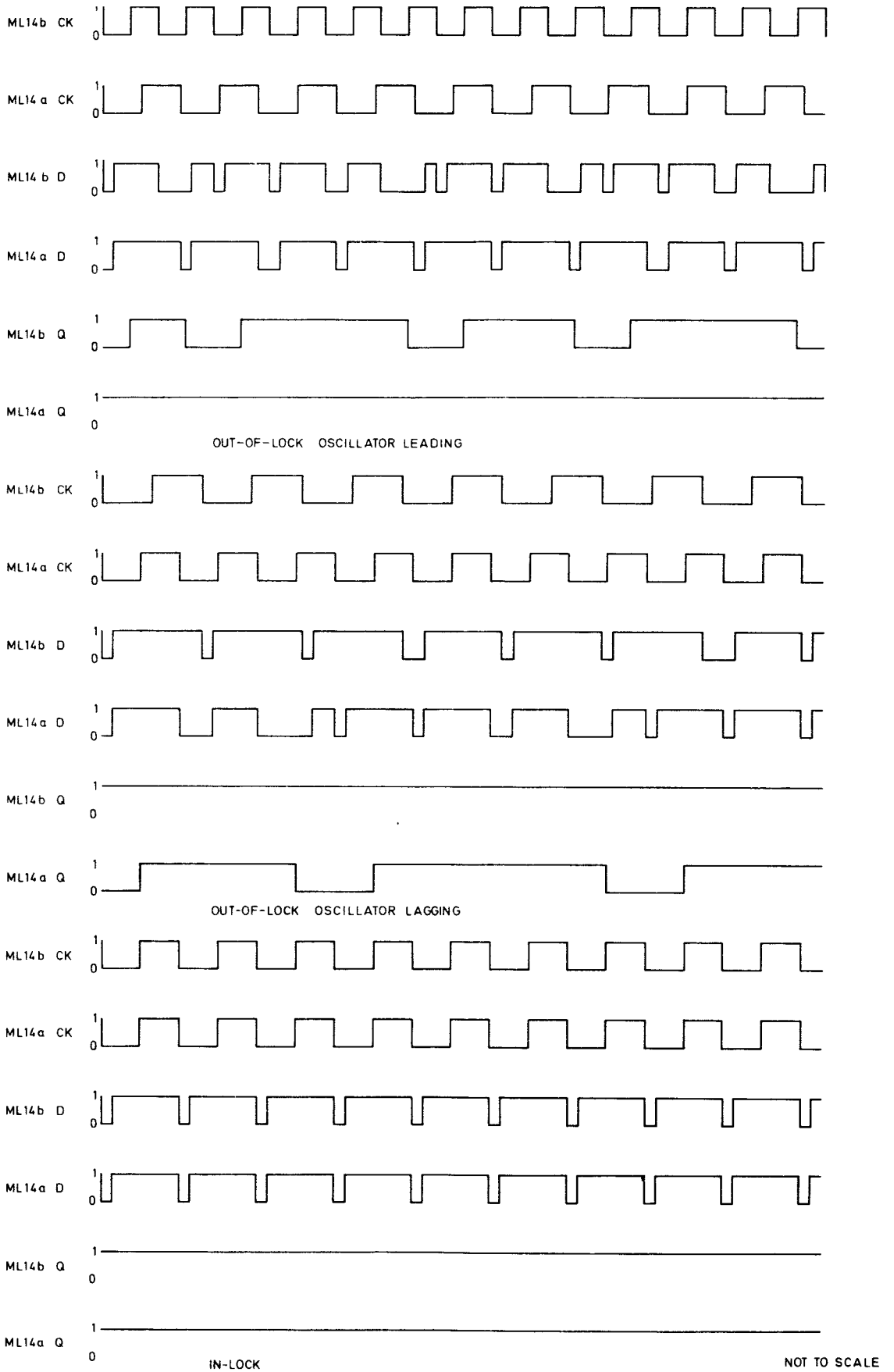


Fig.19 Timing diagram : a.f.c. 7MHz v.c.o. lock detector

inverter G12.

215. The operation of the lock detector is shown in the timing diagram, fig.19. From this diagram it can be seen that an alternating '0' - '1' output is produced for the out-of-lock condition and a steady logic '1' for the in-lock condition.

A.F.C. on/off switching

216. In either of the two a.f.c.-on positions of the AFC switch (FULL CARRIER and PILOT CARRIER), an earth (logic '0') is applied to board pin 13. This is routed to relay RLA/1 and also to a switch-contact bounce-eliminator G1, TR4.

217. Relay RLA/1 is energized and contact RLA1 connects the varactor line voltage for the 7MHz v.c.o. to the meter switching board via R81 and board pin 7.

218. The action of the AFC switch-contact bounce-eliminator is as follows. Prior to the operation of the AFC switch, the two inputs to G1 (ML1 pins 12 and 13) are both at logic '1'; pin 12 is connected to the +5V rail via R26, and the open-circuit at board pin 13 causes ML1 pin 13 to float up to approximately +5V. When the AFC switch is set to FULL CARRIER or PILOT CARRIER, the logic '0' applied to ML1 pin 13 causes the output, at ML1 pin 11, to change to logic '1'. The positive-going edge of this transition causes TR4 to conduct, and this connects ML1 pin 12 to the OV line (logic '0'). Thus the output from G1 is held at logic '1' regardless of a subsequent change in the state of the input applied to ML1 pin 13, until such time as C13 charges and TR4 turns off.

219. The logic '1' output from G1 is applied to an inverter, NAND gate G4, and the resulting logic '0' output is applied to G6 (ML1 pin 4), G8 (ML2 pin 1) and to the base of TR17. The logic '1' output from G6 opens gate G7 for the 25kHz square-wave output from ML6, and the logic '1' output from G8 opens gate G9 for the 25kHz square-wave output from ML7.

220. TR17 is held off unless either a loss of phase-lock of the 1.6MHz v.c.o. occurs (para.184) or a poor signal-to-noise ratio exists at the receiver input (para.193). Should either of these two conditions exist, a logic '1' output from G16 (para.210) causes TR17 to conduct. This in turn causes conduction of TR20 and the normally-on hold switch transistor, TR19, is turned off.

221. The logic '1' output from G1 (ML1 pin 11) is also applied to G17 (ML17 pins 1 and 2); should either a loss of phase-lock of the 1.6MHz v.c.o. occur or a poor signal-to-noise ratio exist at the receiver input, a logic '1' from G16 (ML17 pin 8) will be applied to G17 at M17 pin 13. The resulting logic '0' output, at ML17 pin 12, is applied as an inhibit signal to the reset (RD) inputs of dividers ML6 and ML7 and also the preset (PR) inputs of the digital phase comparator flip-flops, ML9a and ML9b.

222. When the AFC switch is set to the OFF position, the earth (logic '0') is removed from board pin 13. Relay RLA/1 is de-energized and contact RLA1 connects the outputfrom G15 to the meter switching board via R94 and board pin 7 (para.208 and 209).

223. Pin 13 of ML1 floats up to logic '1' (approximately +5V) and the resulting logic '0' output is applied to the following:-

(1) Inverting NAND gate, G4

(2) The strobe (S) input of ML6; this forces the Do output, at ML6 pin 12, to logic '1'.

(3) The strobe (S) input of ML7; this forces the Do output, at ML7 pin 12, to logic '1'.

(4) G14 (ML20 pin 2) to extinguish the AFC LOCK lamp.

(5) G17 (ML17 pins 1 and 2); this holds the output from G17 (ML17 pin 12) at logic '1' and prevents a logic '1' out-of-lock output from G16 (ML17 pin 8) from inhibiting dividers ML6 and ML7, and the digital phase comparator, ML9.

224. The logic '1' output from G4 opens gates G6 and G8; the logic '1' from ML6 pin 12 opens gate G7, and the logic '1' from ML7 pin 12 opens gate G9. The 1MHz square-wave reference output from G2 is now applied via G6 and G7 to the digital phase comparator flip-flop, ML9a, and also via G11 to the lock detector flip-flop, ML14a. The output signal from the divide-by-seven stage, ML4 at pin 2, is applied via G8 and G9 to ML9b of the digital phase comparator and also via G12 to ML14b of the lock detector. Thus when the AFC switch is in the OFF position, the 7MHz v.c.o. is phase locked to the reference 1MHz signal.

225. The logic '1' output from G4 is also used to switch off the a.g.c. via R101 (fig.50a) and it causes conduction of TR19, via TR20, TR17, to phase-lock the 7MHz v.c.o. to the 1MHz reference frequency.

METER SWITCHING BOARD PS419 (fig.52)

226. A double-pole nine-position switch (SA) connects the front panel meter (M1) to various metering points within the receiver, via the meter board stages, as follows:-

227. (1) Position 1: TUNE CARRIER. This position is used in conjunction with the AFC facility. When the AFC switch is set to OFF, the output signal from the carrier tuning indicator on the a.f.c. board (para.208) is applied to the meter via board pin 23, R12 and SA2. This is a positive going pulsed signal of a fixed pulse-width where the pulse repetition rate is equal to the difference in frequency between the received carrier frequency and an internally derived reference frequency; for precise carrier tuning, the receiver tuning control is adjusted for a minimum meter reading. When the AFC switch is set to either FULL CARRIER or PILOT CARRIER, the meter is connected to the varactor line of the 7MHz v.c.o. on the a.f.c. board and provides an indication of the available a.f.c. hold range (AFC + 0 - scale). It may be used to determine whether a slight adjustment of the receiver tuning is required (due to a drift in the transmission frequency) to maintain a.f.c. lock.

(2) Position 2: RF. This provides an indication of the strength of the received signal which is derived from the differential a.g.c. output from the main i.f./a.f. board and the i.s.b./i.f./a.f. board. In this switch position, the meter becomes part of a bridge network, the four arms being TR1/TR2, R1, R16/R17 and R18. TR1 and TR2 form a long-tailed pair, the input to each base being the differential a.g.c. voltage. With no aerial signal input to the receiver, R17 is adjusted

for meter zero; R14 alters the sensitivity of the meter circuit.

(3) Position 3: LSB. The audio line output signal from the i.s.b./i.f./a.f. board is applied to the meter via board pins 11 and 12, R3 and bridge rectifier D5 to D8.

(4) Position 4: AM/USB. The audio line output signal from the main i.f./a.f. board (which carries all modes except LSB) is applied to the meter via board pins 15 and 16, R2 and bridge rectifier D1 to D4.

(5) Position 5: DRIVE LEVEL. This provides an indication of the local-oscillator output drive level applied to the first mixer. A preset variable resistor on the first mixer board allows for adjustment to obtain a meter indication within the 'V' scale outer brackets.

(6) Positions 6, 7, 8 and 9: voltage rail monitoring. The regulated +20V, +12V, +5V and -7V outputs from the power supply regulator board are applied to the meter switch via suitable dropping resistors to provide, in each case, a meter indication within the green portion of the meter scale.

POWER SUPPLIES (fig.54)

228. The power supply section of the receiver comprises a supply input filter, voltage selector unit, mains transformer 1T1, regulator board PM370 and three series-pass power transistors mounted on a heatsink attached to the rear panel of the receiver; a number of resistors associated with the regulating stages are also mounted on the heatsink. Stabilised supplies of -7V, +5V, +12V and +20V are provided. Additional stages, mounted on the a.f. and memory board (para.236), are a +14.5V regulator for the audio amplifiers, and a +5V memory supply. The smoothing capacitors, 1C1a, 1C1b, 1C2a, 1C2b and 1C3 to 1C6, are mounted on the inside of the rear panel.

Supply input filter

229. The supply input, at 1PL1, is fed via a supply fuse, 1FS3, and a double-pole ON/OFF switch, to the supply input filter, 1L1, 1L2 and capacitors C18 to C21. The filtered output is connected to the mains transformer, 1T1, via the voltage selector unit 1VS1.

Regulator board PM370

230. This utilises four identical integrated-circuit regulators, ML1 to ML4; this device consists of a temperature compensated reference amplifier, error amplifier, series-pass transistor and a current limit stage; an equivalent circuit of the device is given in fig.20.

231. The error amplifier is used to compare the reference voltage (maximum approximately +7V) with a sample of the final stabilised output voltage (via a potential divider if greater than the reference voltage) and the output of the error amplifier is then used to control the series-pass transistor. This transistor is also controlled by a current limiting stage which itself is controlled by the current drawn from the supply by the external load.

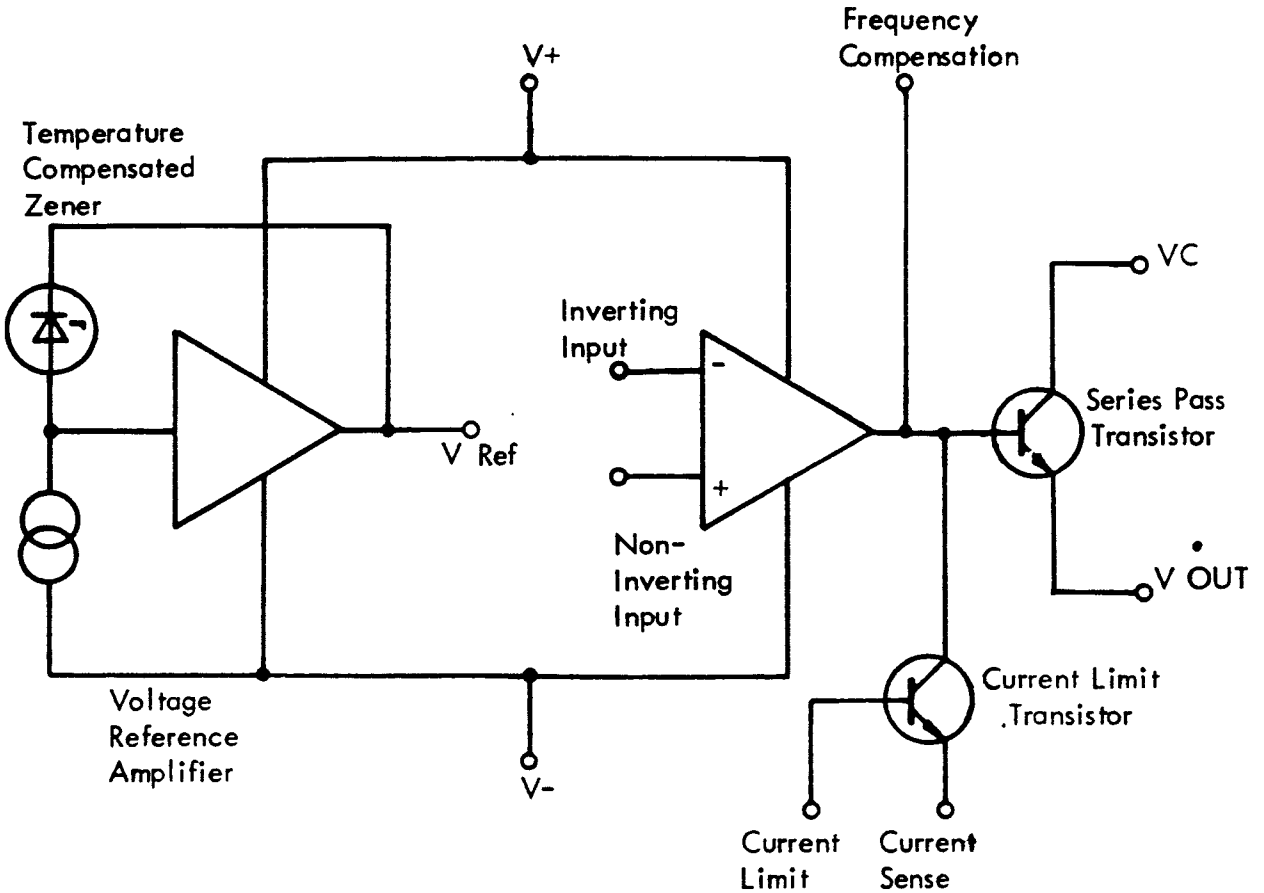


Fig. 20 Equivalent circuit : voltage regulator i.c.

-7V regulator

232. A 10V secondary winding of 1T1 is connected to a full-wave bridge rectifier, D1, via board pins 49 and 50 and link LK1. The positive output from D1 is applied to the collector of the external series pass transistor, 1TR1, via board pin 1, whereas the emitter of 1TR1 is returned to the negative output of D1 via pin 4, R21 and R14. The positive supply voltage for ML1 (V+), and also, the collector voltage (Vc) for the internal series pass transistor, is taken from the +12V regulated supply. The output from the reference amplifier (V REF) is applied via R1 to the non-inverting input of the error amplifier whilst the inverting input is connected to the -7V regulated output via a potential divider R13, R9, preset voltage-adjust potentiometer R8, and R7. Current 'foldback' is provided by R14, R21, 1R12 and 1R14.

+5V regulator

233. Bridge rectifier D2 is fed from a 10.5V secondary winding of transformer 1T1 via board pins 45 and 46 and link LK6. The positive output from D2 is applied to the collectors of the two series pass transistors, TR1 and 1TR2. The positive supply voltage for ML2 (V+) and also the collector voltage (Vc) of the internal series pass transistor are taken from the +20V regulated supply. The reference voltage level applied to the non-inverting input of the error amplifier is preset by the potentiometer, R3, and the inverting input is taken from the 5V output via R15. Current 'foldback' is provided by R16, R22, 1R13 and 1R15.

+12V regulator

234. This supply is derived from a 16.5V secondary winding of transformer 1T1. The positive output from the bridge rectifier, D3, is applied to the collectors of the two series pass transistors, TR2 and 1TR3, whereas the positive supply voltage for ML3 and the collector voltage for the internal series pass transistor are taken from the +20V regulated supply. The reference voltage is applied via R5 to the non-inverting input of the error amplifier whilst potentiometer R17 presets the voltage level applied to the inverting input. The regulated +12V output is taken to board pins 16, 17 and 18, and to the oven of the frequency standard via R32, D6 and pin 20. Current 'foldback' is provided by R18, R24 and 1R16.

+20V regulator

235. This stage, which is similar to the +12V regulator, is fed from a 23V secondary winding of 1T1 and bridge rectifier D4. The regulated output is preset by potentiometer R19. Current foldback is provided by R12, R20, R28 and R34.

A.F. AND MEMORY REGULATOR BOARD PS427/1 (fig.56)

236. Refer to fig.59 whilst reading the description of the PS427/1 board and the MS540 +12V battery module (para.241); this description assumes that the BATTERY switch (SA) on the MS540 is set to ON. This board contains two circuits. A regulator circuit provides a +14.5V supply for the main and i.s.b./i.f./a.f. boards; the 5V memory supply circuit relies for its operation on the output of the 12V battery module MS540. References to 'power failure' infer a momentary failure; in the event of a sustained power failure lasting for longer than 30 minutes - with the receiver still switched on - the battery (MS540) will discharge to approximately 10V (para.247).

14.5V regulator

237. This consists of a three-terminal positive-voltage regulator (ML2) together with a buffer amplifier (ML1) and a preset output-level-adjust potentiometer, R3. It is fed from an unregulated 23V supply from the power supply regulator board PM370 (fig.54).

Memory supply

238. An unregulated 14V supply from the regulator board PM370 (fig.54) is applied to board pin 9, whilst the 12V frequency standard supply is applied to board pin 8. The frequency supply (fig.56) is taken from the regulated +12V supply via a resistor and a diode (R32, D6) or, in the event of a power failure, from the 12V battery module (connected to the rear panel STD/ +12V terminal) via two series-connected diodes D7, D8 (fig.54).

239. The unregulated 14V supply at board pin 9 is routed by diode D2 to a three-terminal +5V regulator, ML3, and also to the base of TR1 via potential divider R5, R6. TR1 is turned on and thus holds off the regulator transistors TR2 and TR3 to isolate the +12V supply.

240. Should the main source of a.c. power subsequently fail, the 14V supply at board pin 9 is removed, TR1 is turned off and the +12V frequency standard supply is routed via TR2 and D1 to the +5V regulator, ML3.

12V BATTERY MODULE MS540 (fig.58)

241. When the POWER switch on the receiver is set from OFF to ON, the kHz portion of the digital frequency display is automatically set to 00.000. It follows from this that should a brief interruption of the power supply input occur, the kHz portion of the receiver frequency will again be set to zero. The output from the battery module is used to retain the frequency setting of the receiver during a brief interruption of the supply, and so avoid a possible loss of kHz tuning information.

Oscillator

242. The +12V supply from the receiver is used to power a 5kHz square-wave oscillator, ML1, and the current-pump stage TR1, TR2, C3, D2, R6, D4. The approximate square-wave output from ML1 (about 12V peak-to-peak) is applied to the current-pump stage to provide approximately +15V to charge the battery B1, via the battery ON/OFF switch SA. R6 sets the charging current which is, typically, 15 milliamps.

Supply detector

243. The main supply input at TS1 is full-wave rectified by D1 and is then applied via R5 to an optical coupler ML2. This consists of a light-emitting diode and a photo-transistor. When the supply is present, the photo-transistor conducts and ML2 pin 5 is effectively at OV.

Electronic switch

244. The requirements of the electronic switch are as follows:

(1) To allow the battery to charge when the receiver is working normally.

(2) To allow the battery to discharge to provide a +12V supply at board pin 4 should a main supply failure occur whilst the receiver is in use (i.e. receiver POWER switch set to ON).

(3) To prevent discharge of the battery when the receiver POWER switch is set to OFF.

(4) To prevent further battery discharge should the battery voltage fall to approximately 10V.

The action of the electronic switch for each of the above requirements is given below.

245. When the receiver is working normally, the presence of the +12V supply at board pin 3 causes TR6 to conduct (via R11) which in turn switches on TR3 and TR4. The +15V (approximately) output from the current-pump stage charges the battery via the battery ON/OFF switch and is also applied to the receiver +12V/STD terminal via TR4, D6 and board pin 4.

246. Should the main supply subsequently fail whist the receiver is in use, the photo-transistor (ML2) ceases to conduct and, provided the battery voltage is greater than 10V, the resultant current flow through R9 causes approximately 0.5V to be applied to the base of TR5. TR6 ceases to conduct (since the +12V supply from the receiver is no longer available) but the conduction of TR3 and TR4 is maintained via TR5, and the battery is allowed to discharge via TR4, D6 and board pin 4. If the on-load battery voltage falls below 10V, D5 ceases to conduct, TR5 switches off and this in turn switches off TR3 and TR4 to isolate

the battery. The electronic switch may be reset only by restoring the main supply with the POWER switch still set to ON.

247. When, whilst the main supply is available and connected, the receiver POWER switch is set to OFF, both TR5 and TR6 are held off to prevent conduction of TR3 and TR4, and so isolate the battery.

248. If, however, the main supply is disconnected whilst the receiver POWER switch is set to ON, then the battery will become fully discharged in approx. 30 minutes.

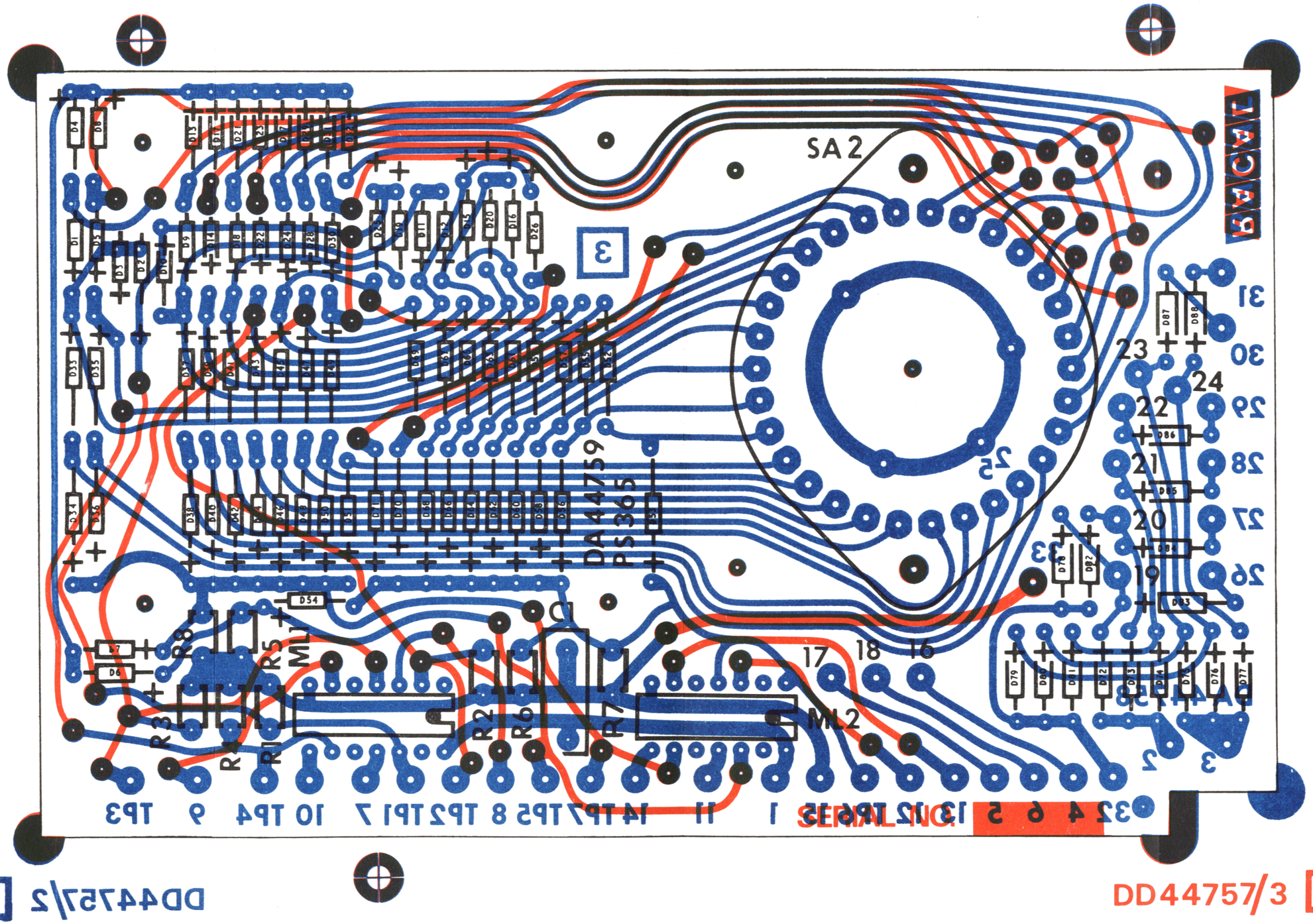


Fig. 21 Logic board PS365 : component layout

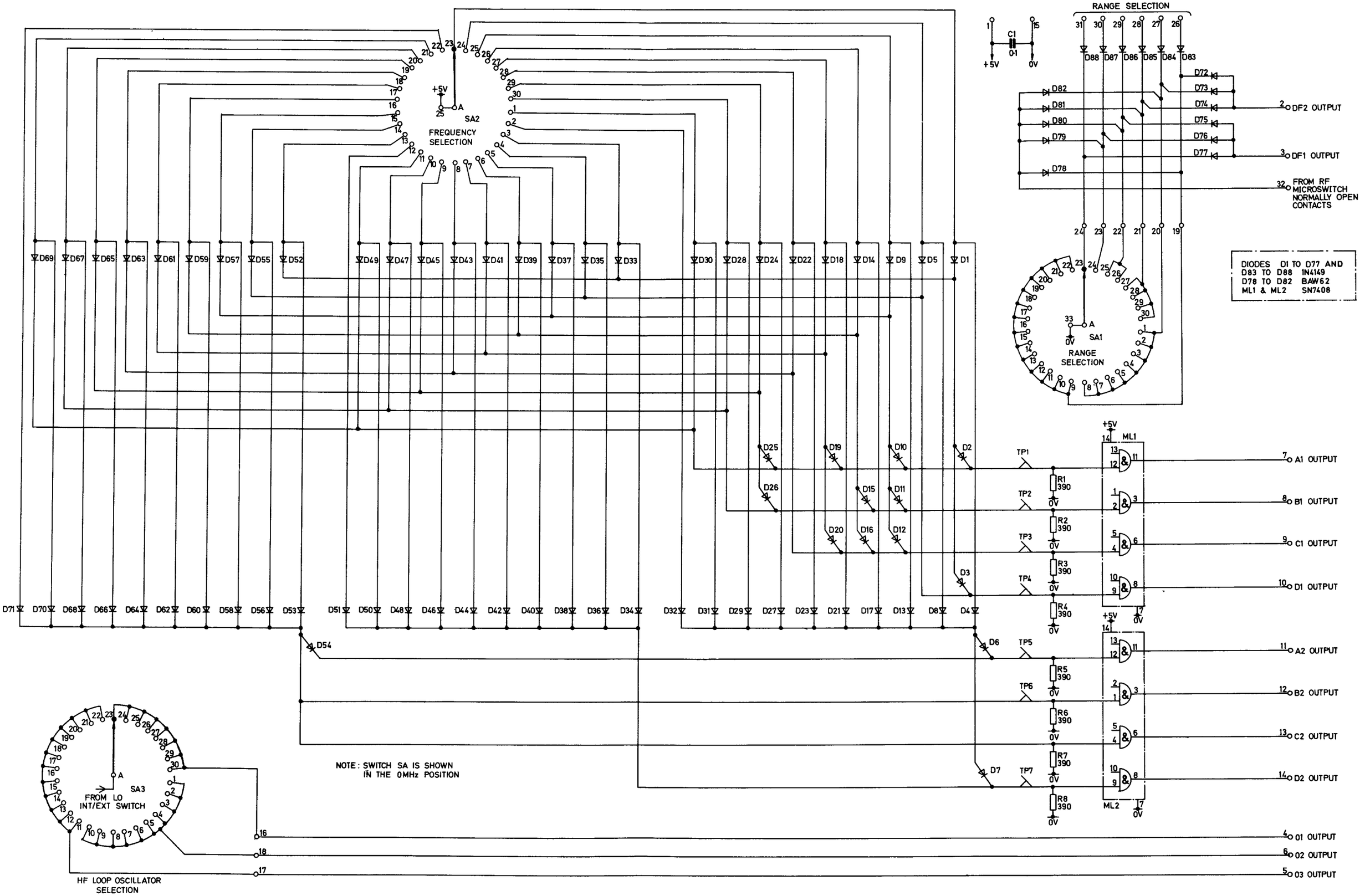


Fig. 22

Logic board PS365 : circuit

Fig. 22
Chap. 2-1
Page 69

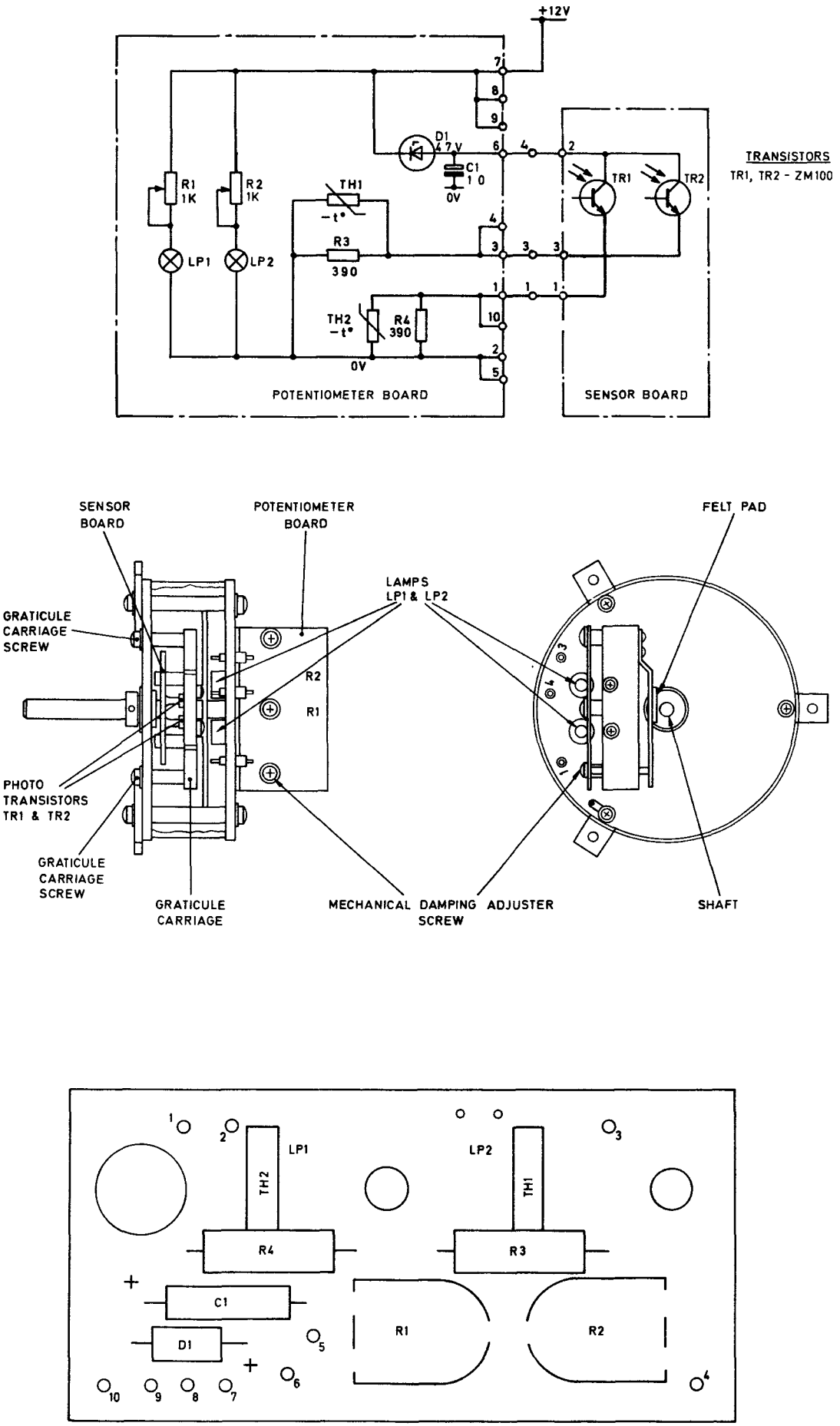


Fig.23 Optical shaft encoder: component layout and circuit

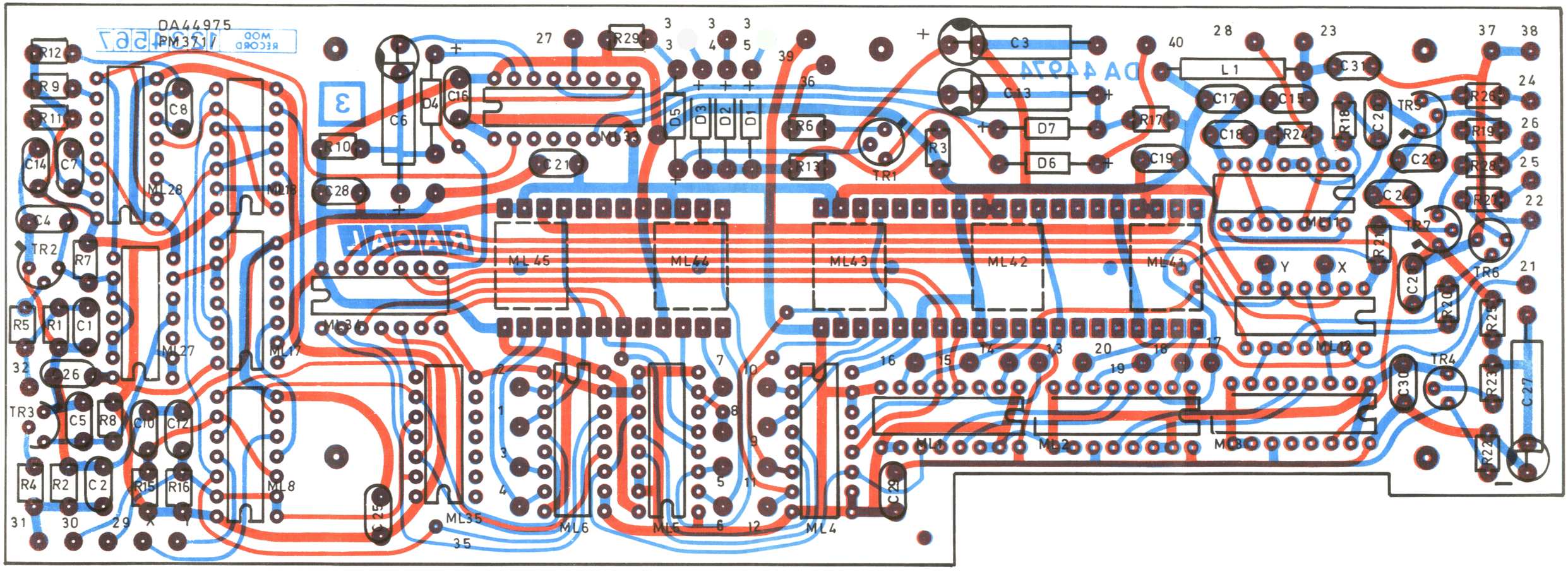


Fig 24 Display board PM371: component layout Fig 24

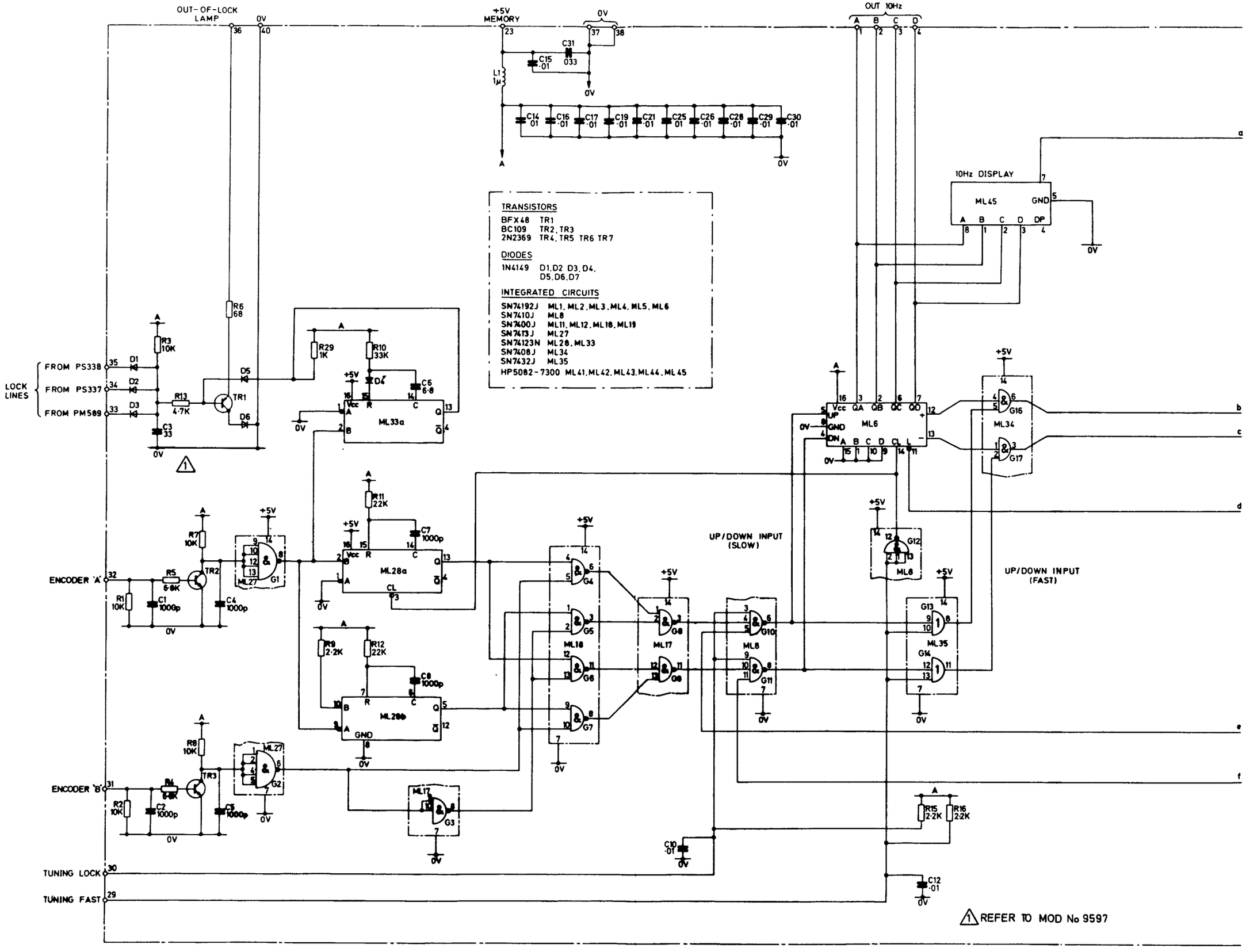


Fig. 25a

Display board PM371 : circuit (sheet 1)

Fig. 25a

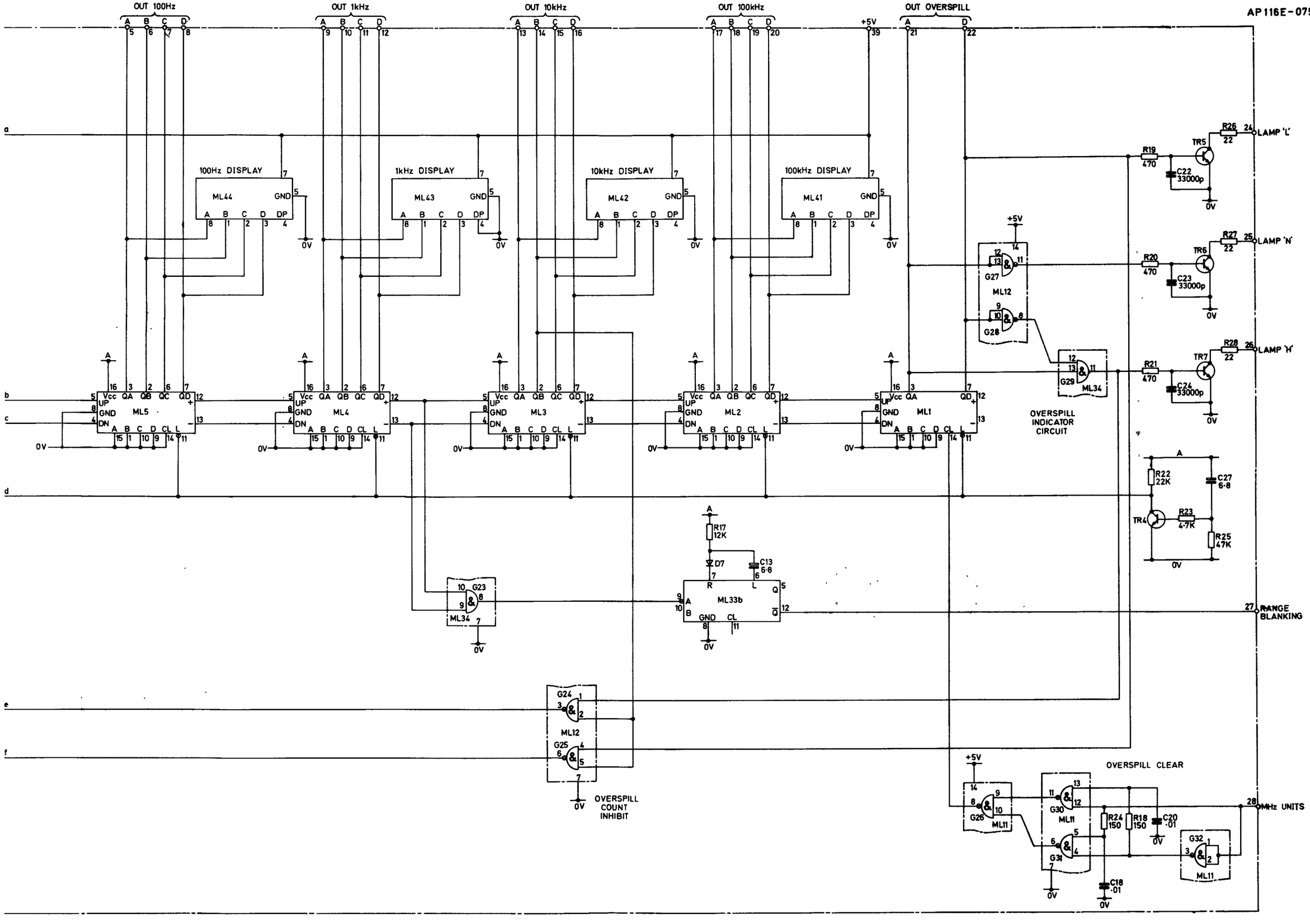
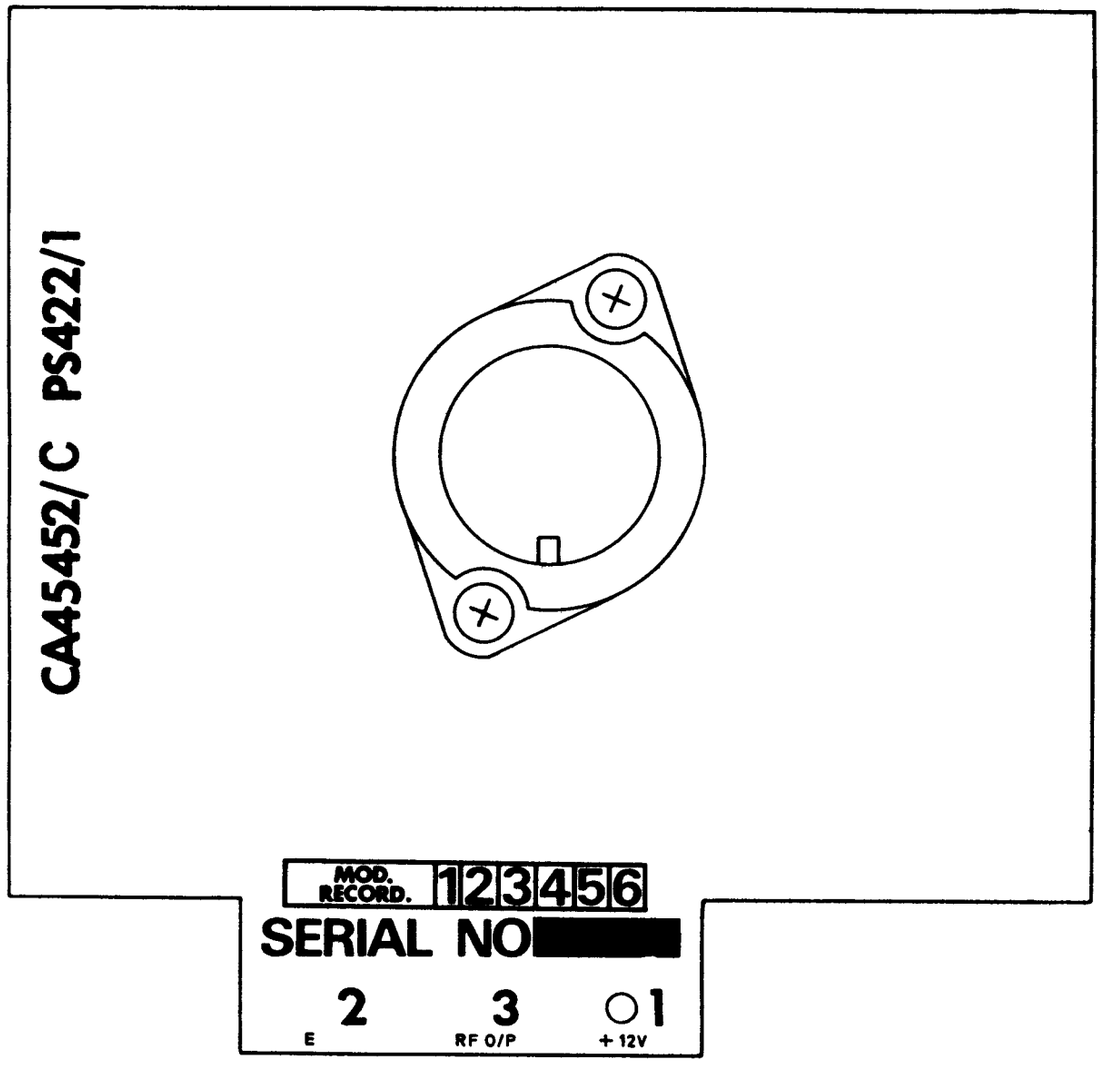
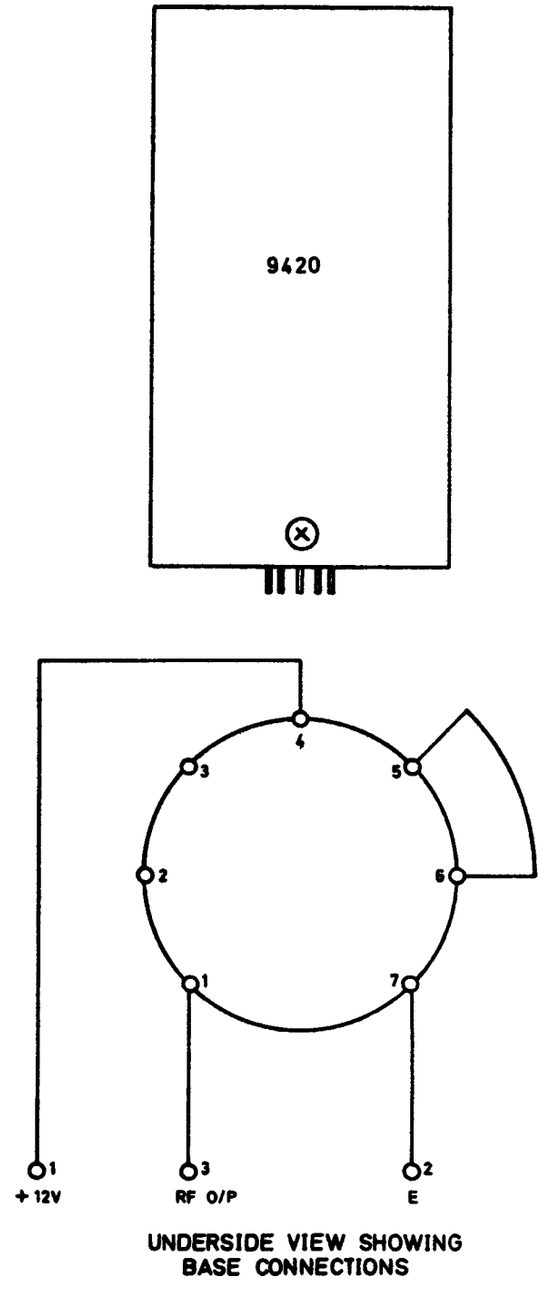


Fig. 25b

Display board PM371: circuit (sheet 2)





UNDERSIDE VIEW SHOWING BASE CONNECTIONS

Fig. 26

Frequency standard assembly 9420

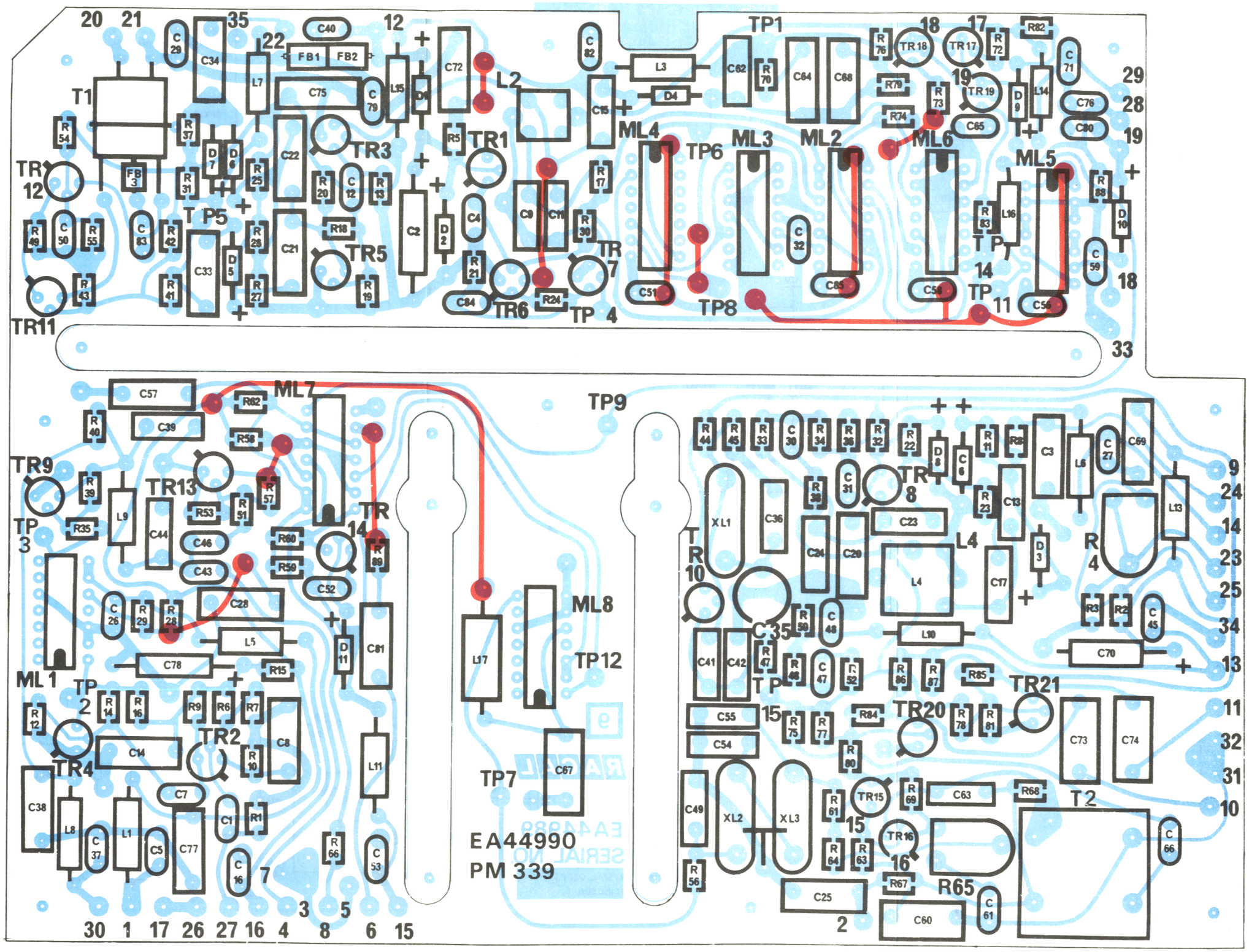


Fig. 27

34MHz generator board PM339: component layout

Fig. 27

Chap. 2-1

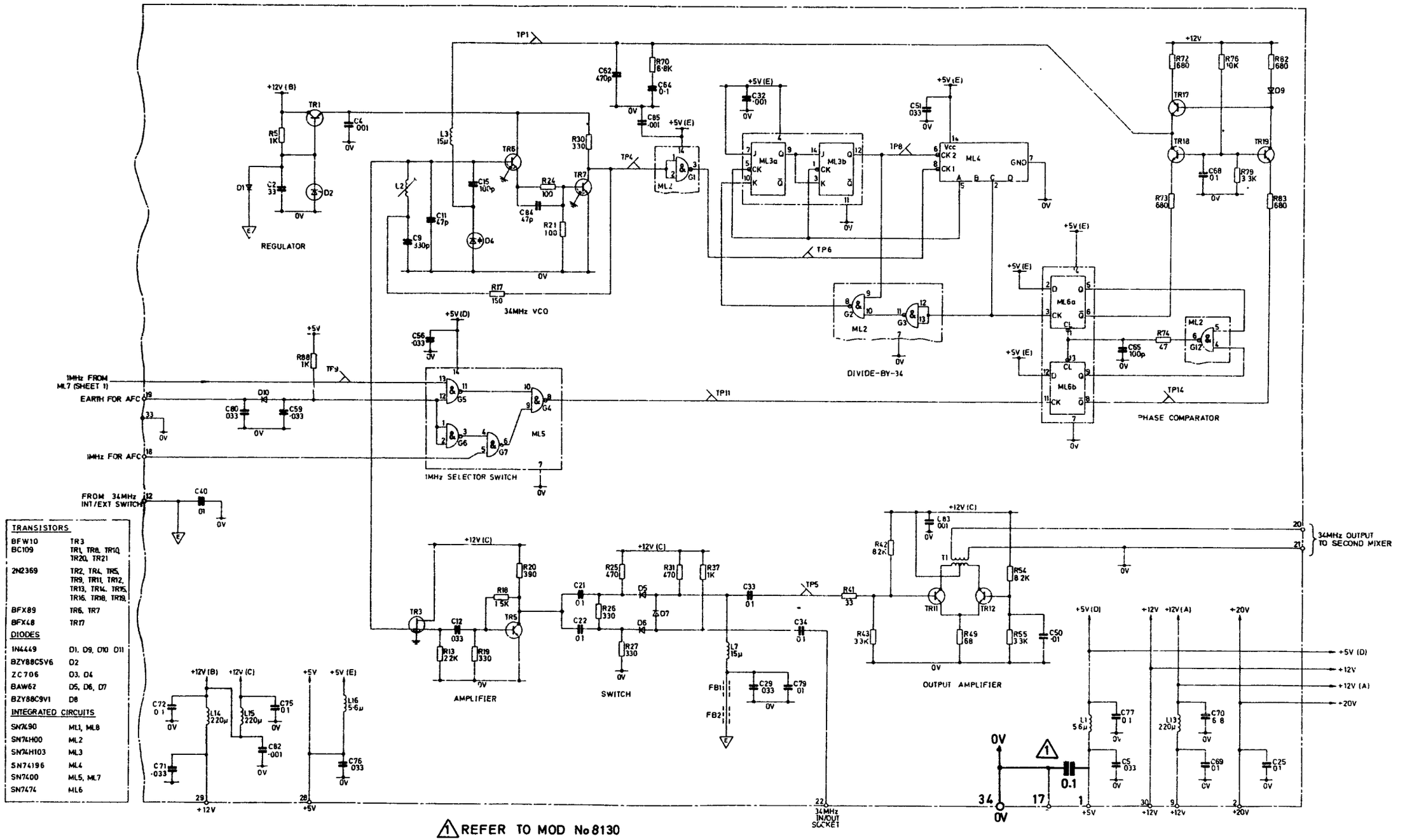
Page 75

AL1, Mar. 76

TRANSISTORS		DIODES		INTEGRATED CIRCUITS	
BC109	TR1, TR8, TR10, TR20, TR21	1N4149	D1, D9	SN7490	ML1, ML8
BFW10	TR3		D10, D11	SN74H00	ML2
2N2369	TR2, TR4, TR5	BZY88C5V6	D2	SN74H103	ML3
	TR9, TR11, TR12,	ZC706	D3, D4	SN74196	ML4
	TR13, TR14, TR15,	BAW62	D5, D6, D7	SN7400	ML5, ML7
	TR16, TR18, TR19	BZY88C9V1	D8	SN7474	ML6
BFX89	TR6, TR7				
BFX48	TR17				

1MHz IN/OUT SOCKET
5MHz INPUT FROM FREQUENCY STANDARD
AMPLIFIER & SHAPER
DIVIDE-BY-5
SHAPER
FROM SHEET 2
+20V
+12V (A)
+12V
+5V (D)
1MHz OUTPUT TO PM588
1MHz OUTPUT TO PS338
1MHz TO ML5 (SHEET 2)
FROM BFO TUNING POTENTIOMETER ON FRONT PANEL
1·4MHz VCO
1·4MHz CRYSTAL OSCILLATOR (OPTIONAL)
1·4MHz CRYSTAL FILTER
OUTPUT AMPLIFIERS
1·4MHz USB/AM OUTPUT
1·4MHz LSB OUTPUT
CONTROL BOARD
1MHz EARTH
1·4MHz EARTH
BFO EARTH
CRYSTAL EARTH

34MHz generator board PM339: circuit (sheet 1)



TRANSISTORS	
BFW10	TR3
BC109	TR1, TR8, TR10, TR20, TR21
2N2369	TR2, TR4, TR5, TR9, TR11, TR12, TR13, TR14, TR15, TR16, TR18, TR19
BFX89	TR6, TR7
BFX48	TR17
DIODES	
1N4449	D1, D9, D10 D11
BZY88C5V6	D2
ZC706	D3, D4
BAW62	D5, D6, D7
BZY88C9V1	D8
INTEGRATED CIRCUITS	
SN7490	ML1, ML8
SN74H00	ML2
SN74H103	ML3
SN74196	ML4
SN7400	ML5, ML7
SN7474	ML6

Fig. 28b

34 MHz generator board PM339: circuit (sheet 2)

Fig. 28b

May 85 (Amdt 10)

Chap 2-1

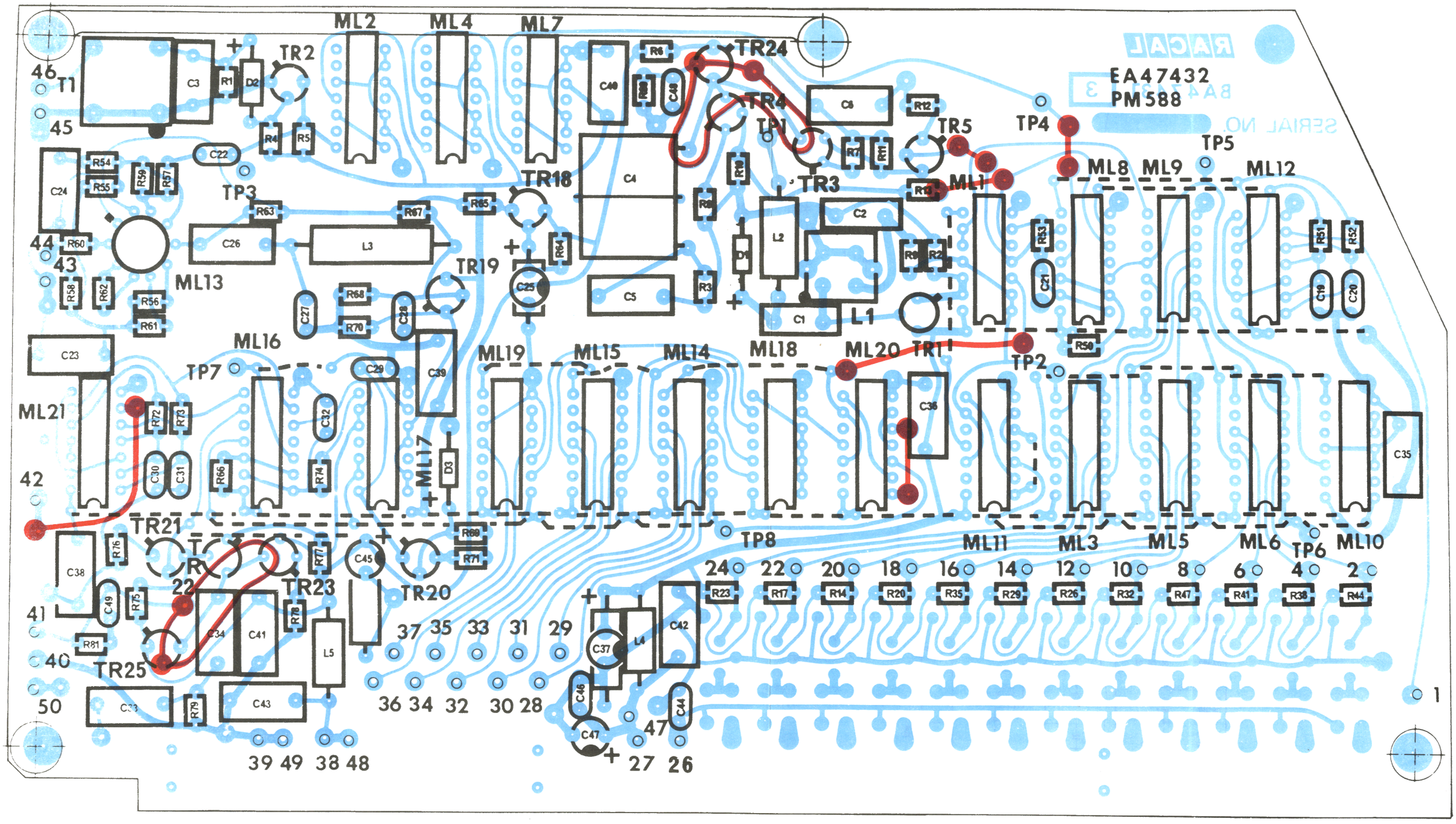


Fig. 29 Low frequency loop board PM588: component layout

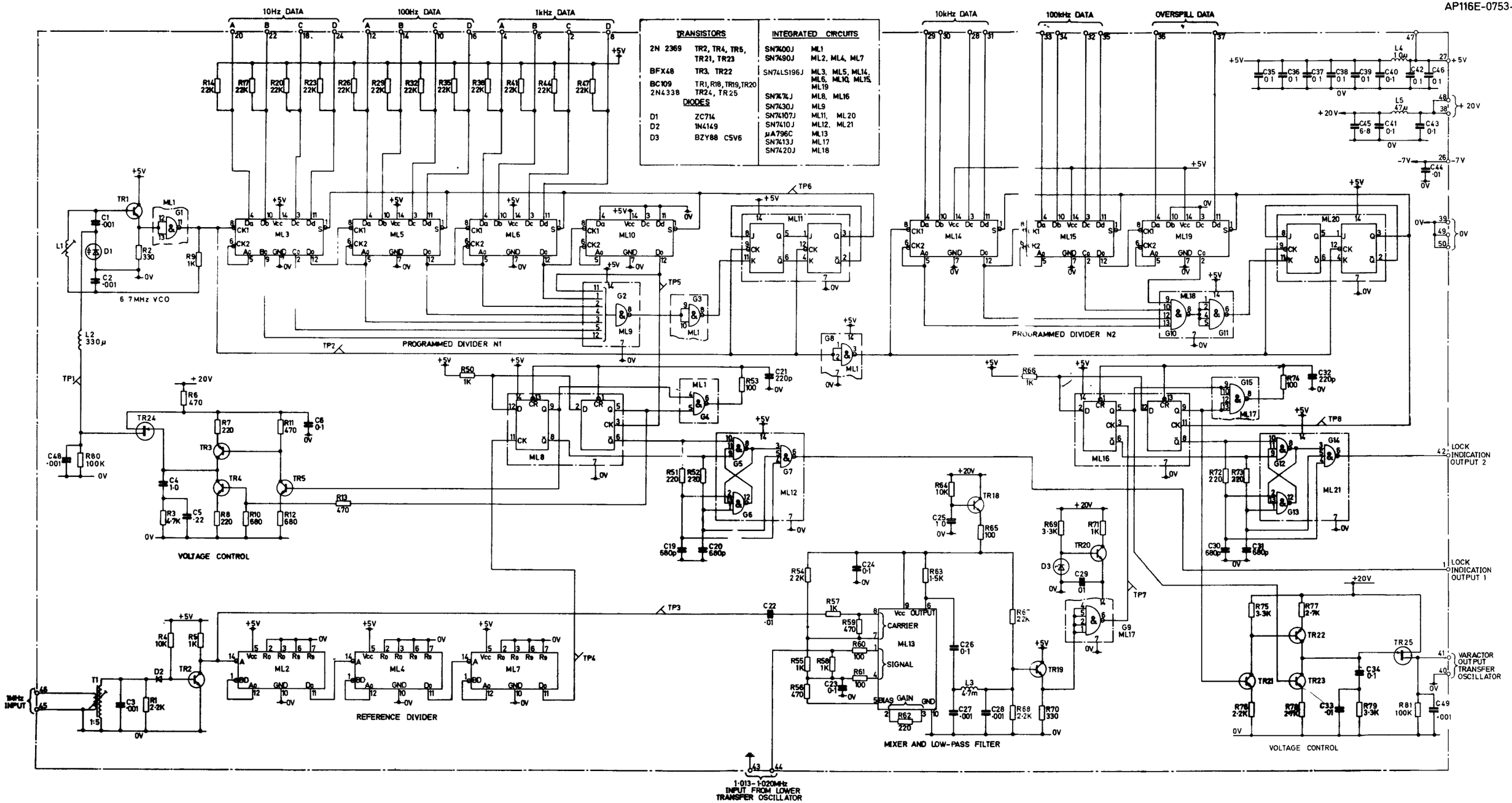


Fig. 30

Low frequency loop board PM588: circuit

Fig. 30

Chap. 2-1

Page 79

AL1, Mar. 76

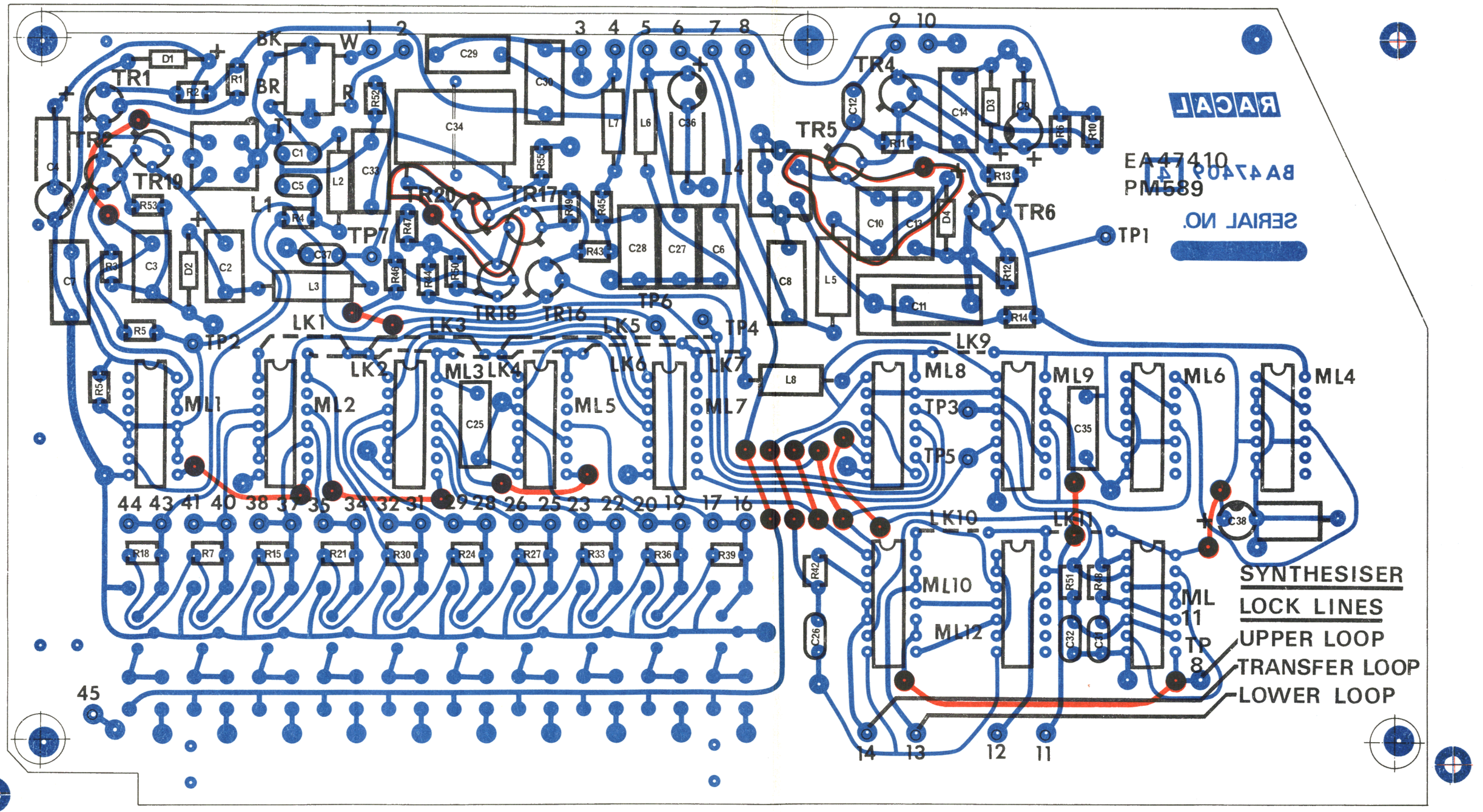
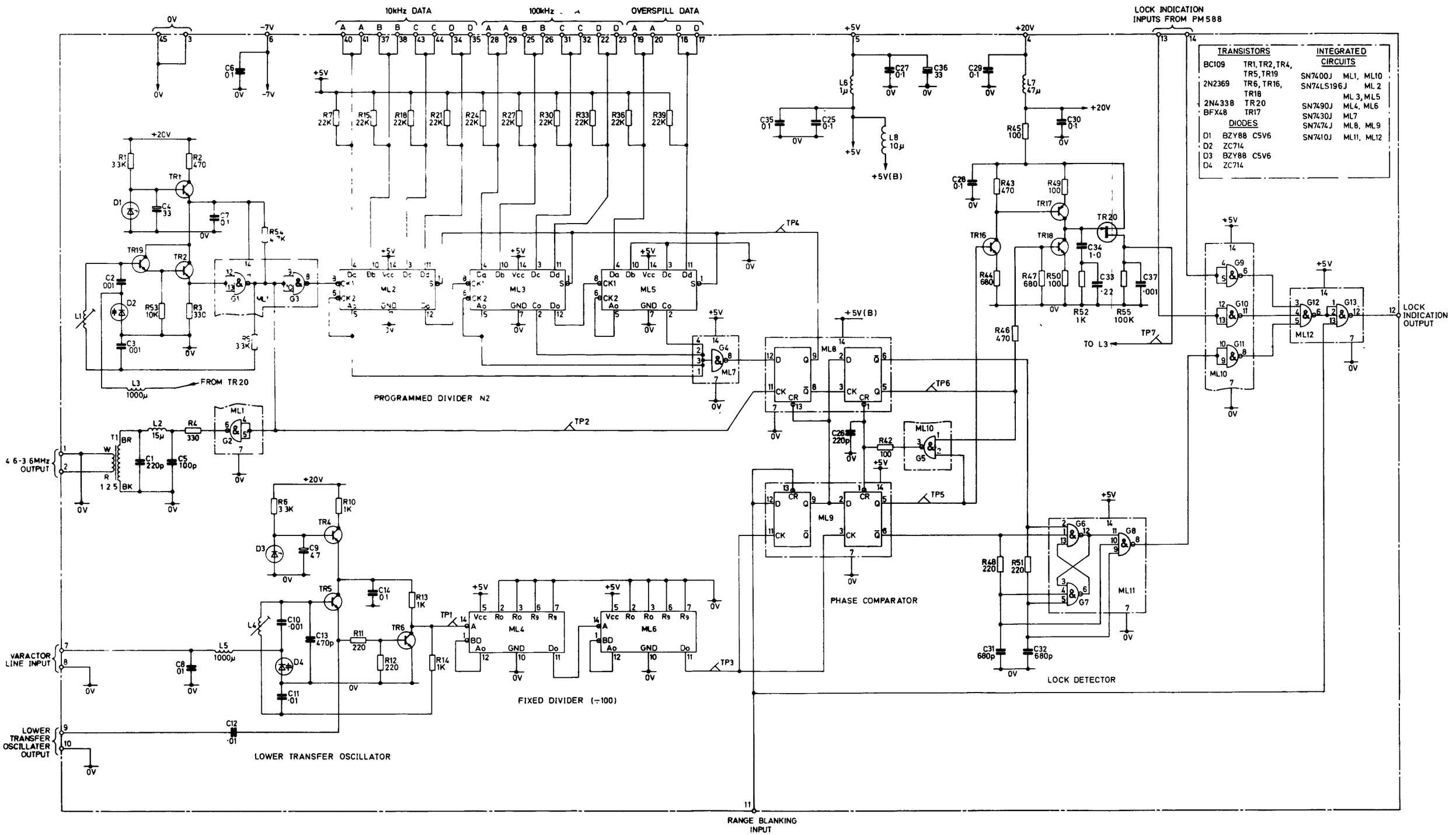


Fig. 31

Upper loop board PM589: component layout

Fig. 31



Upper loop board PM589 : circuit

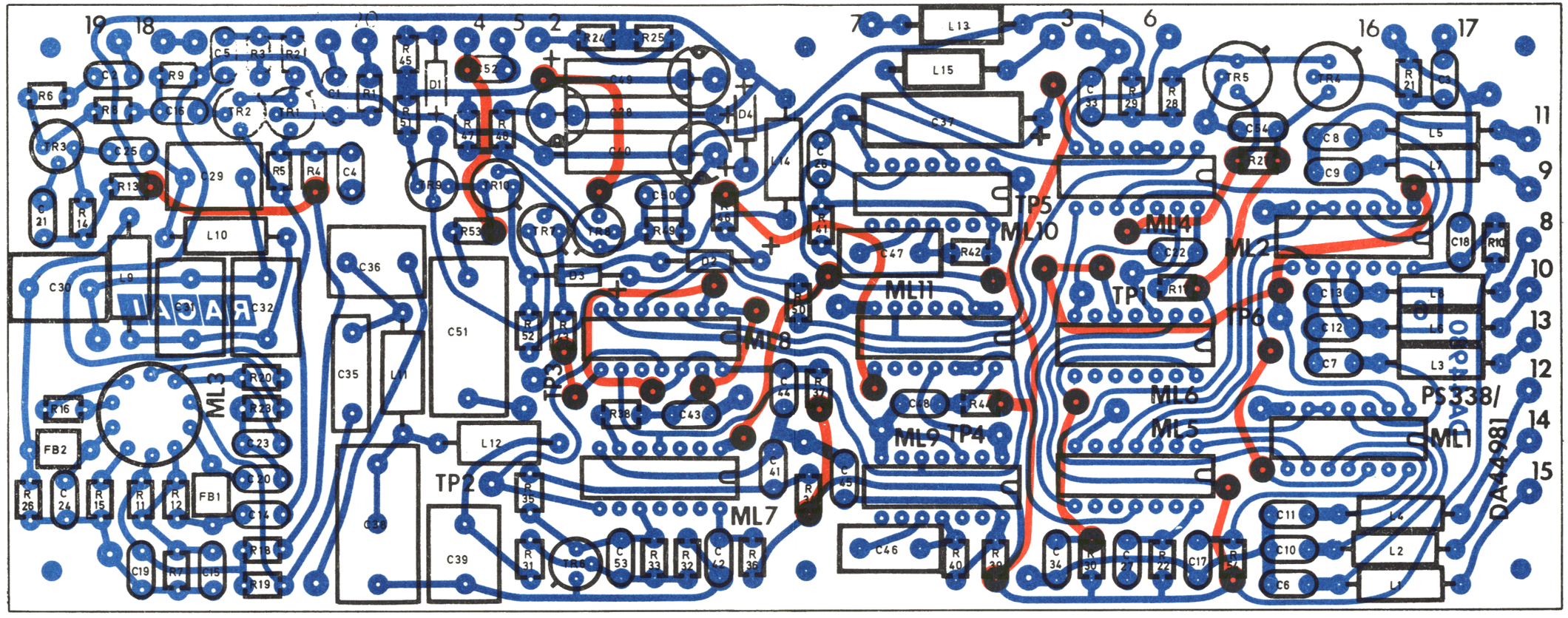


Fig. 33

Transfer loop board PS338: component layout

Fig. 33

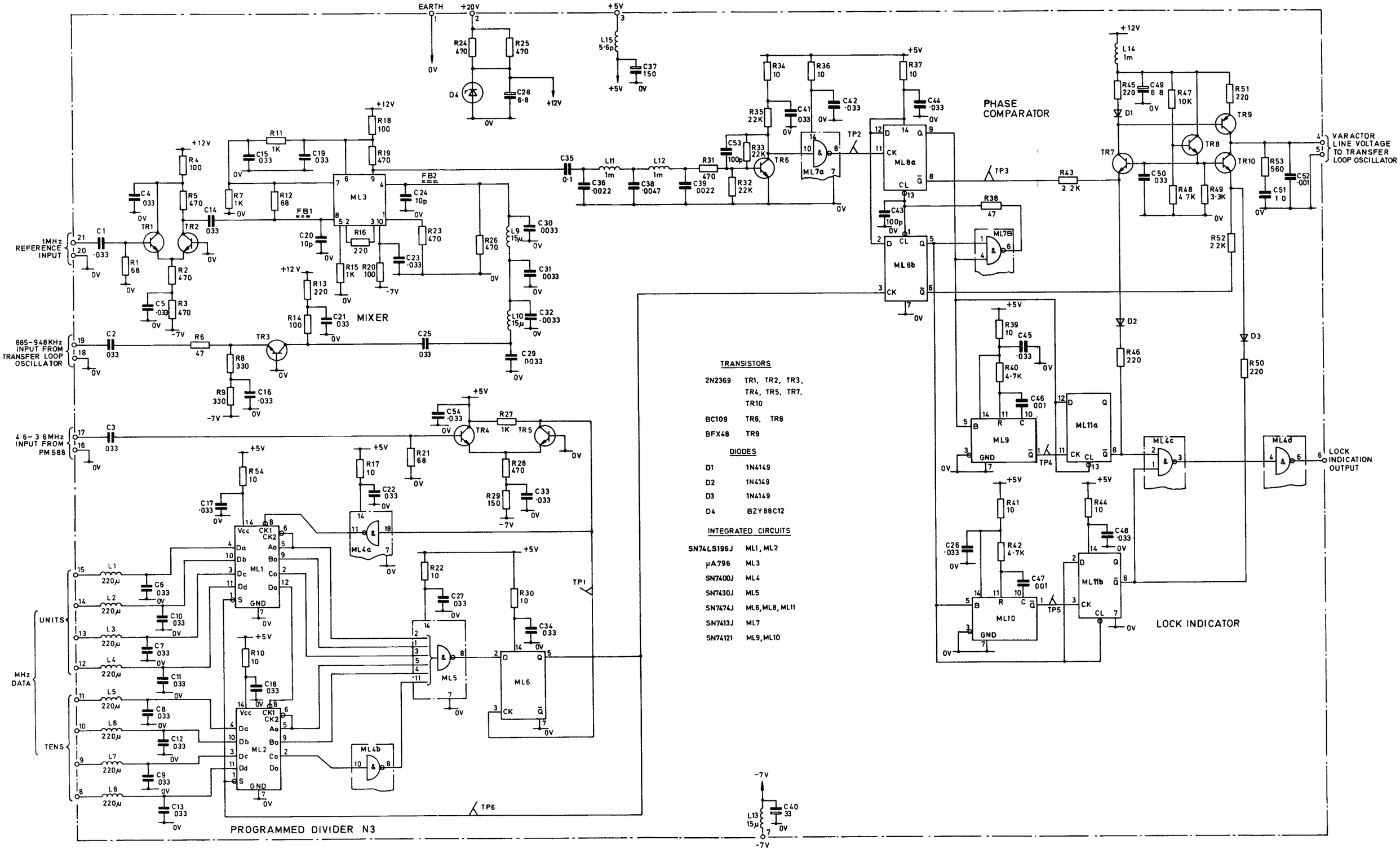


Fig. 34

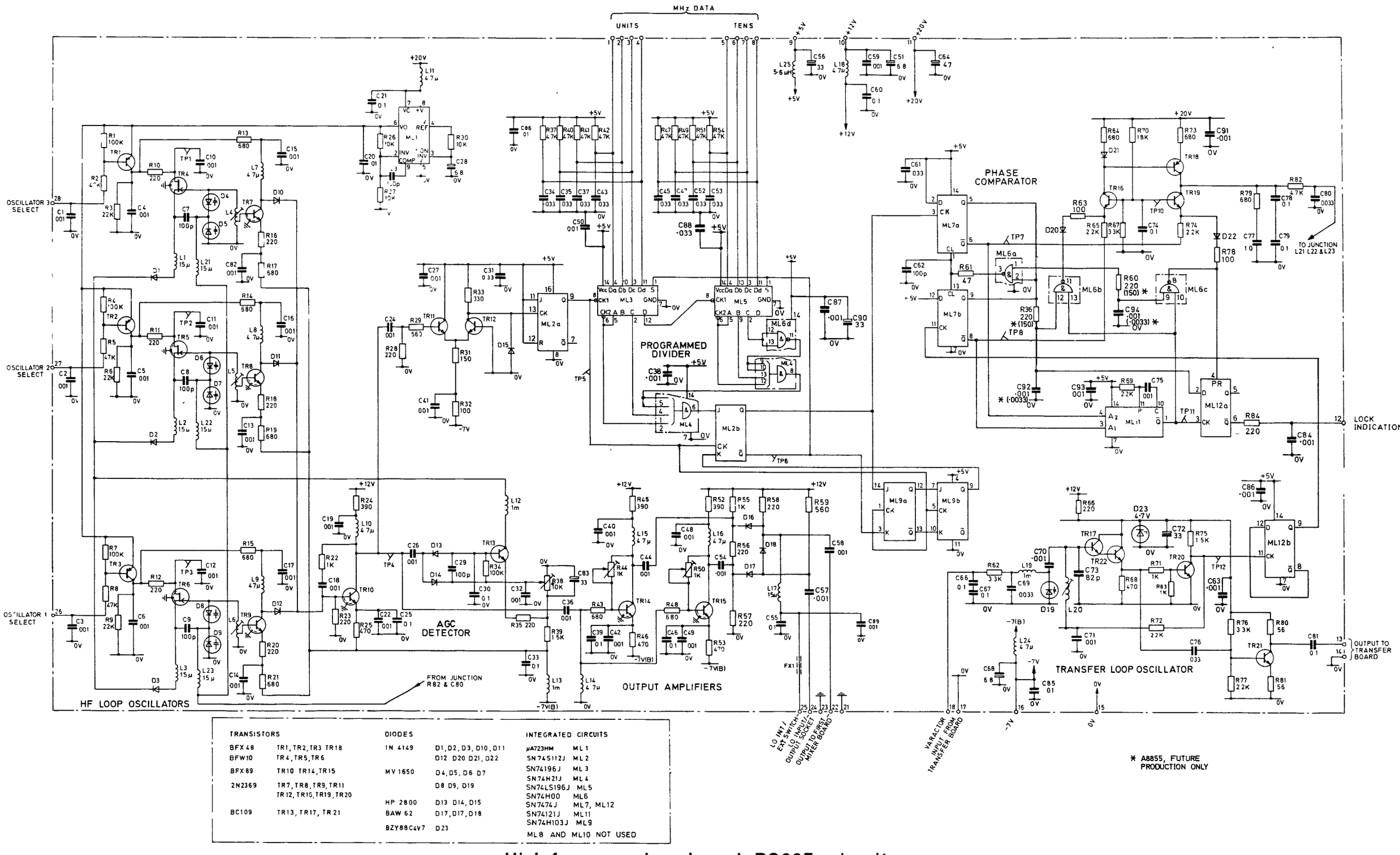
Transfer loop board PS338: circuit

Fig.34

Chap. 2-1

Page 83

AL 1, Mar. 76



TRANSISTORS		DIODES		INTEGRATED CIRCUITS	
BFX48	TR1, TR2, TR3 TR18	1N 4149	D1, D2, D3, D10, D11	μA723HM	ML1
BFW10	TR4, TR5, TR6		D12 D20 D21, D22	SN74S112J	ML2
BFX89	TR10 TR14, TR15	MV 1650	D4, D5, D6 D7	SN74196J	ML3
2N2369	TR7, TR8, TR9, TR11 TR12, TR16, TR19, TR20		D8 D9, D19	SN74H21J	ML4
		HP 2800	D13 D14, D15	SN74LS196J	ML5
BC109	TR13, TR17, TR21	BAW 62	D17, D17, D18	SN74H00	ML6
		BZY88C4V7	D23	SN7474J	ML7, ML12
				SN74121J	ML11
				SN74H103J	ML9
				ML8 AND ML10 NOT USED	

Fig.36

High frequency loop board PS337 : circuit

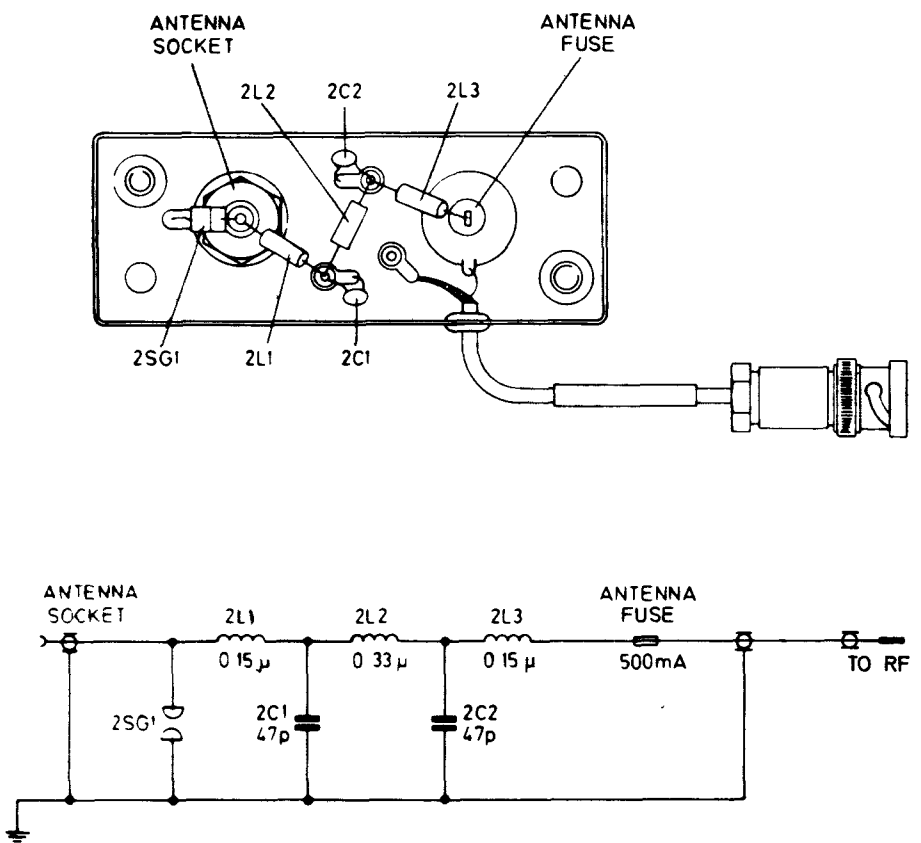
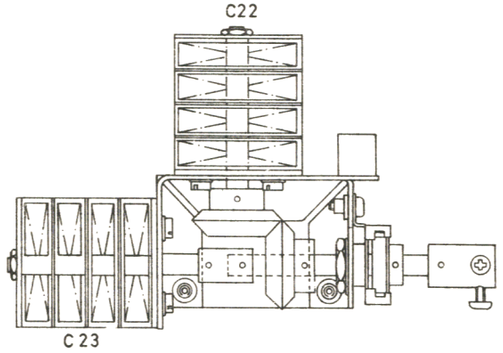
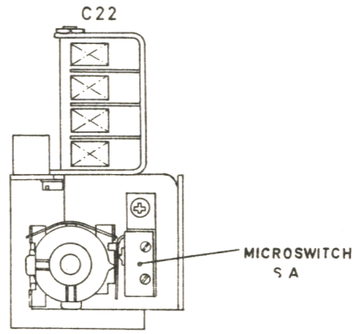


Fig.37 Re-radiation filter: component layout and circuit





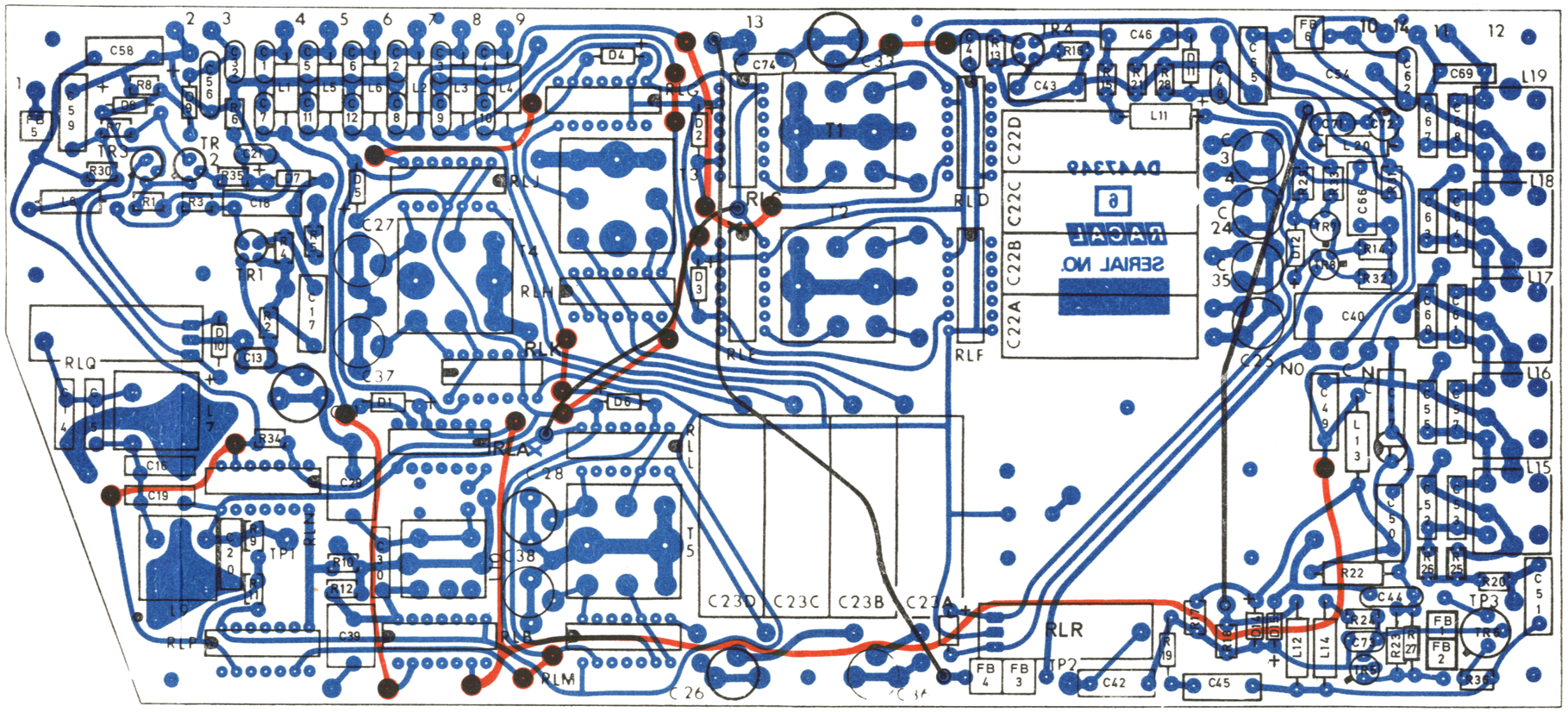


Fig. 38

R.F. board (tuned) PM582: component layout

Fig. 38

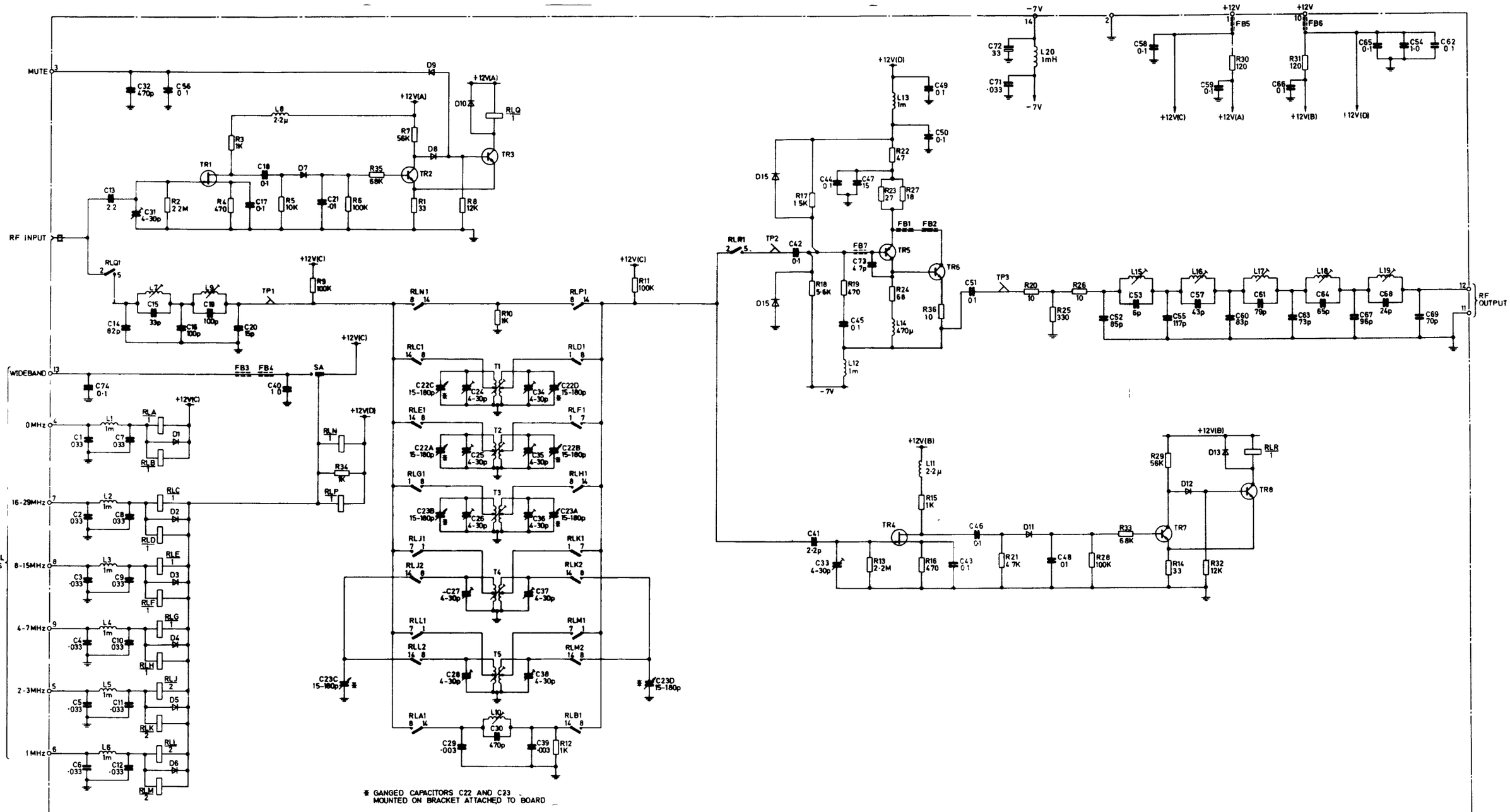


Fig. 39

R.F. board (tuned) PM582: circuit

Fig. 39
Chap. 2-1
Page 89

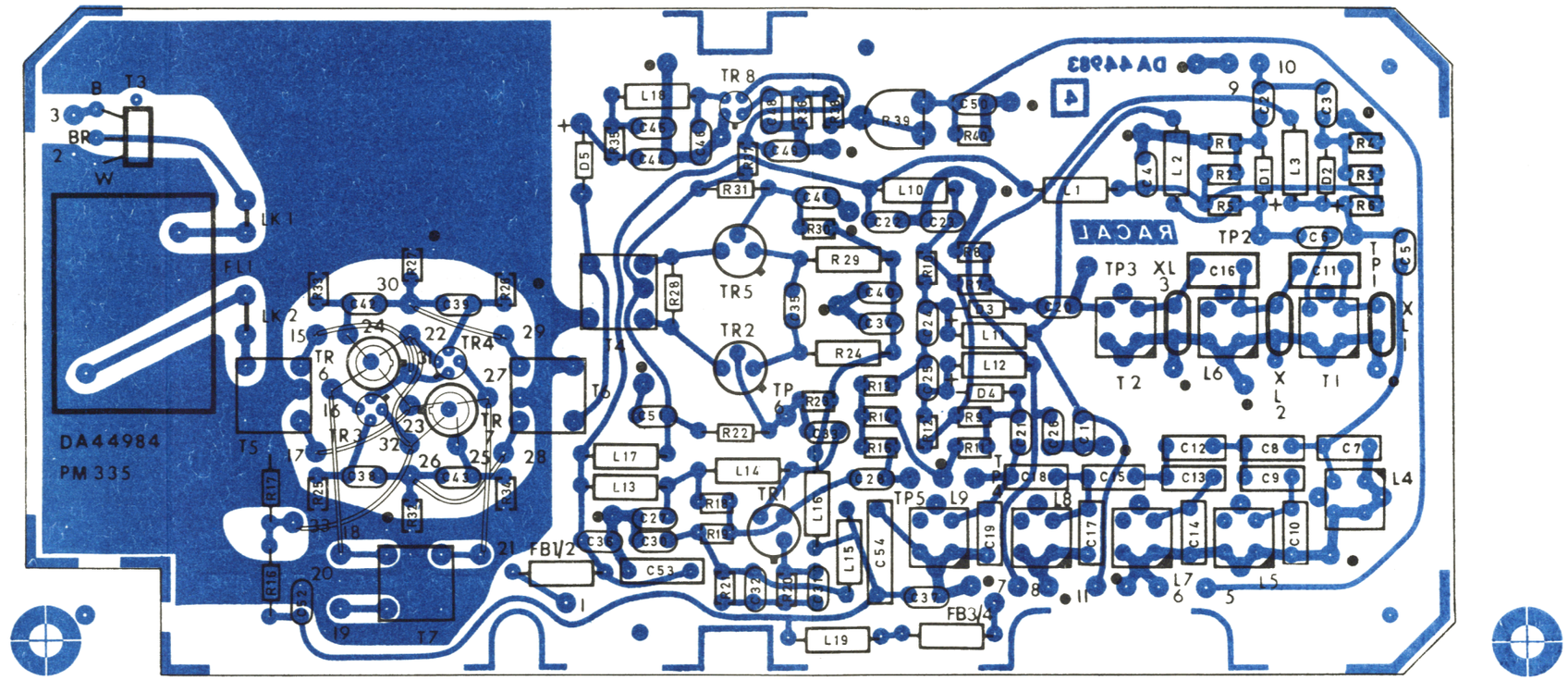


Fig. 40 First mixer board PM335 : component layout Fig. 40

TRANSISTORS

2N3866	TR1, TR2, TR5
BSV81	TR3, TR4, TR6, TR7
BFW10	TR8

DIODES

IN4149	D1, D2, D3, D4, D5

RF INPUT
0V
0-3 MHz SELECT
INPUT FROM LOCAL OSCILLATOR
4-30MHz SELECT
IF OUTPUT
OUTPUT TO METER
-7V
+12V

⚠ REFER TO MOD No A9662

First mixer board PM335 : circuit

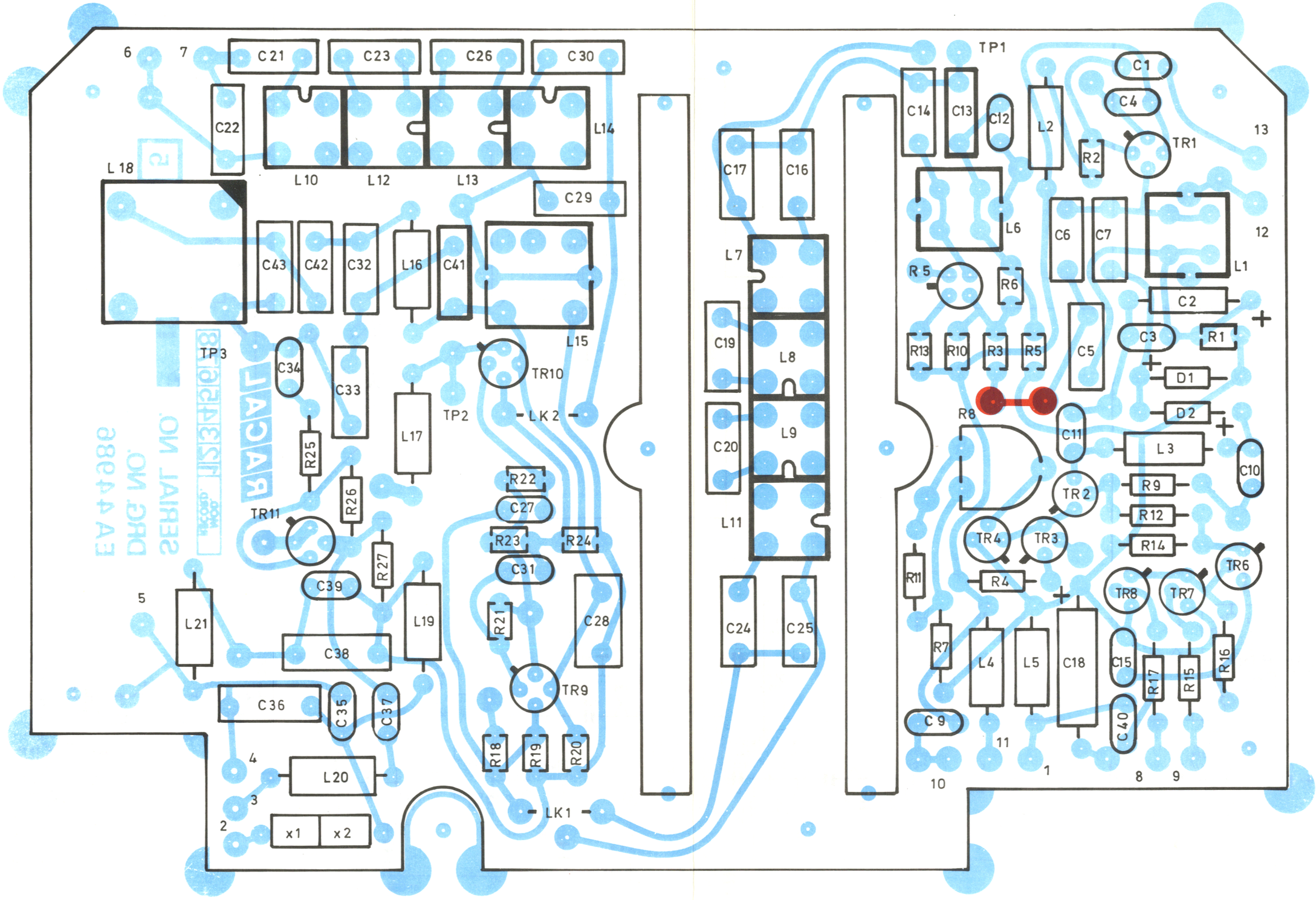


Fig 42

Second mixer board PM336: component layout

Fig 42

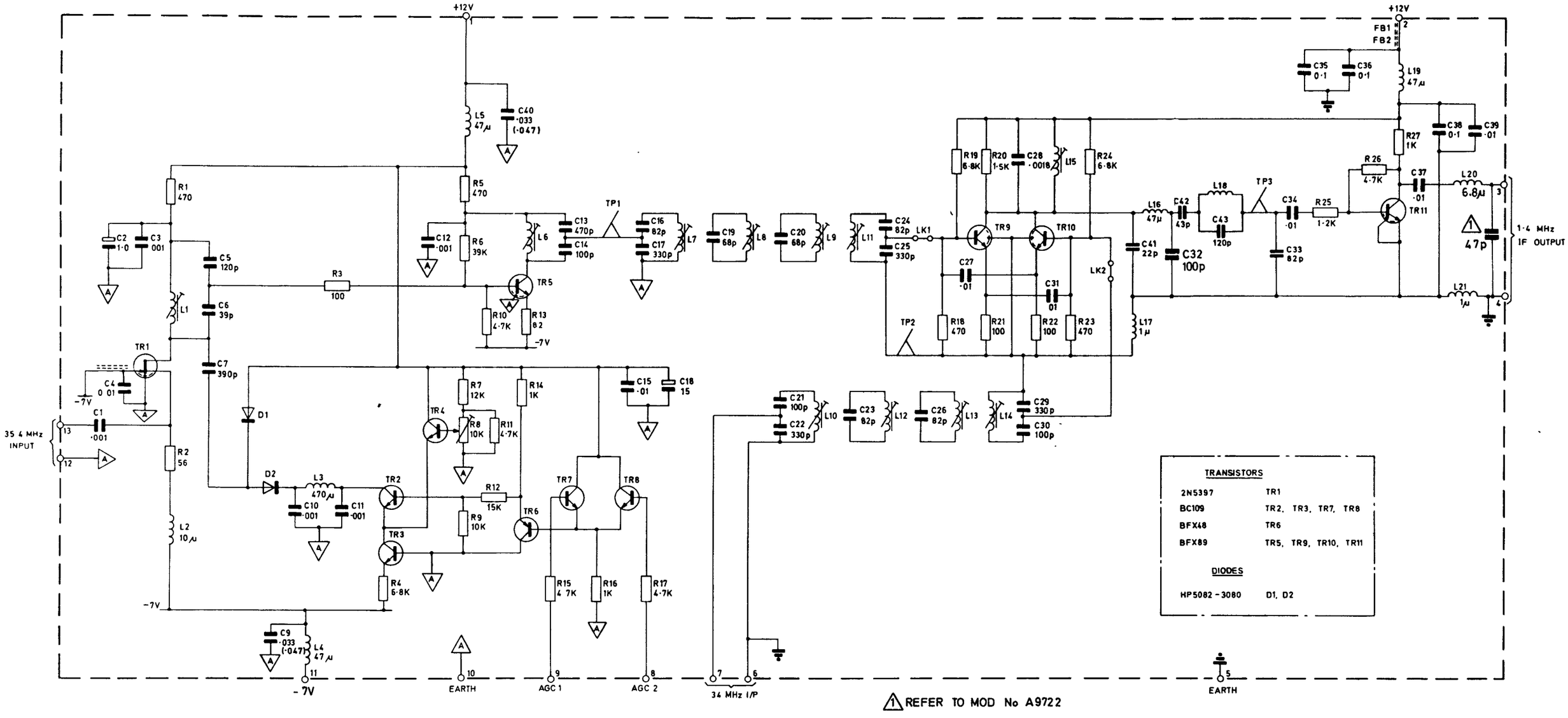


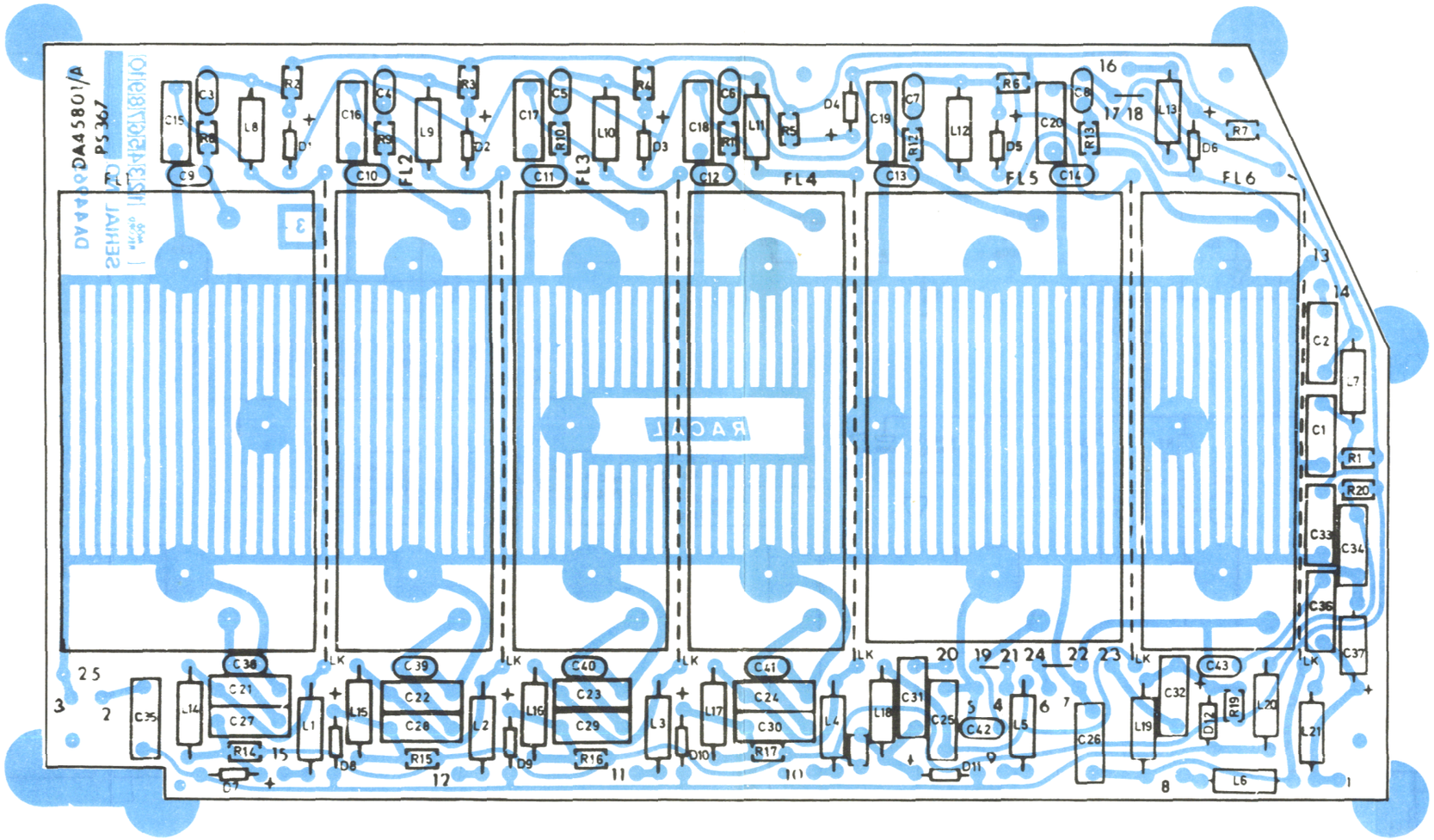
Fig. 43

Second mixer board PM336 : circuit

Fig. 43

Chap. 2-1

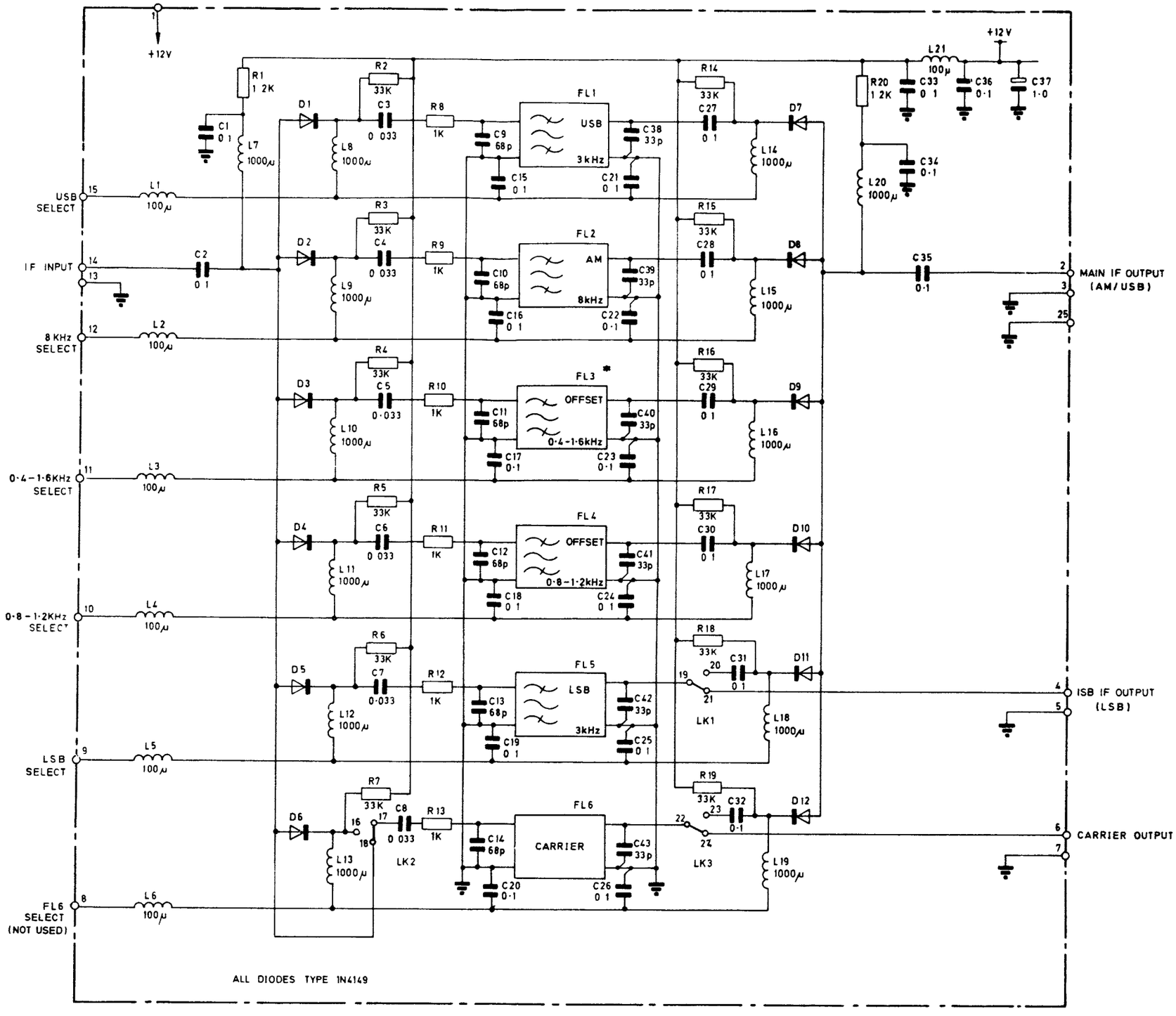
May 85 (Amdt 10)



I.F. filter board PS367 : component layout

Fig. 4 4
Chap 2-1

Fig. 4 4



NOTE Due to the inversion within the receiver, the filter selected for USB operation will have LSB characteristics, and that selected for LSB operation will have USB characteristics.

* Filter FL3, 1.1 to 2.9 kHz (Post Mod TC0015)

Fig. 45

I.F filter board PS367: circuit

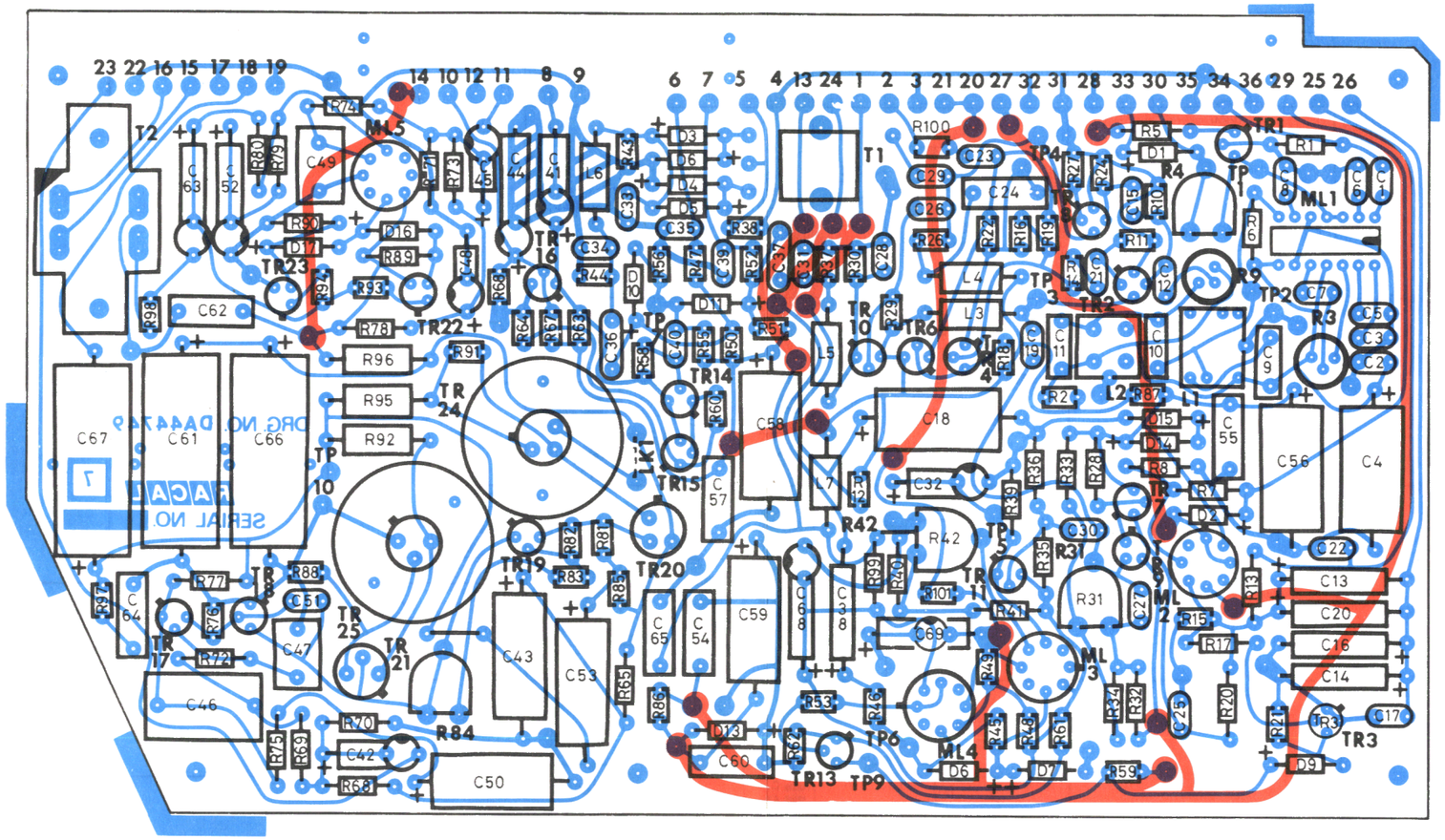
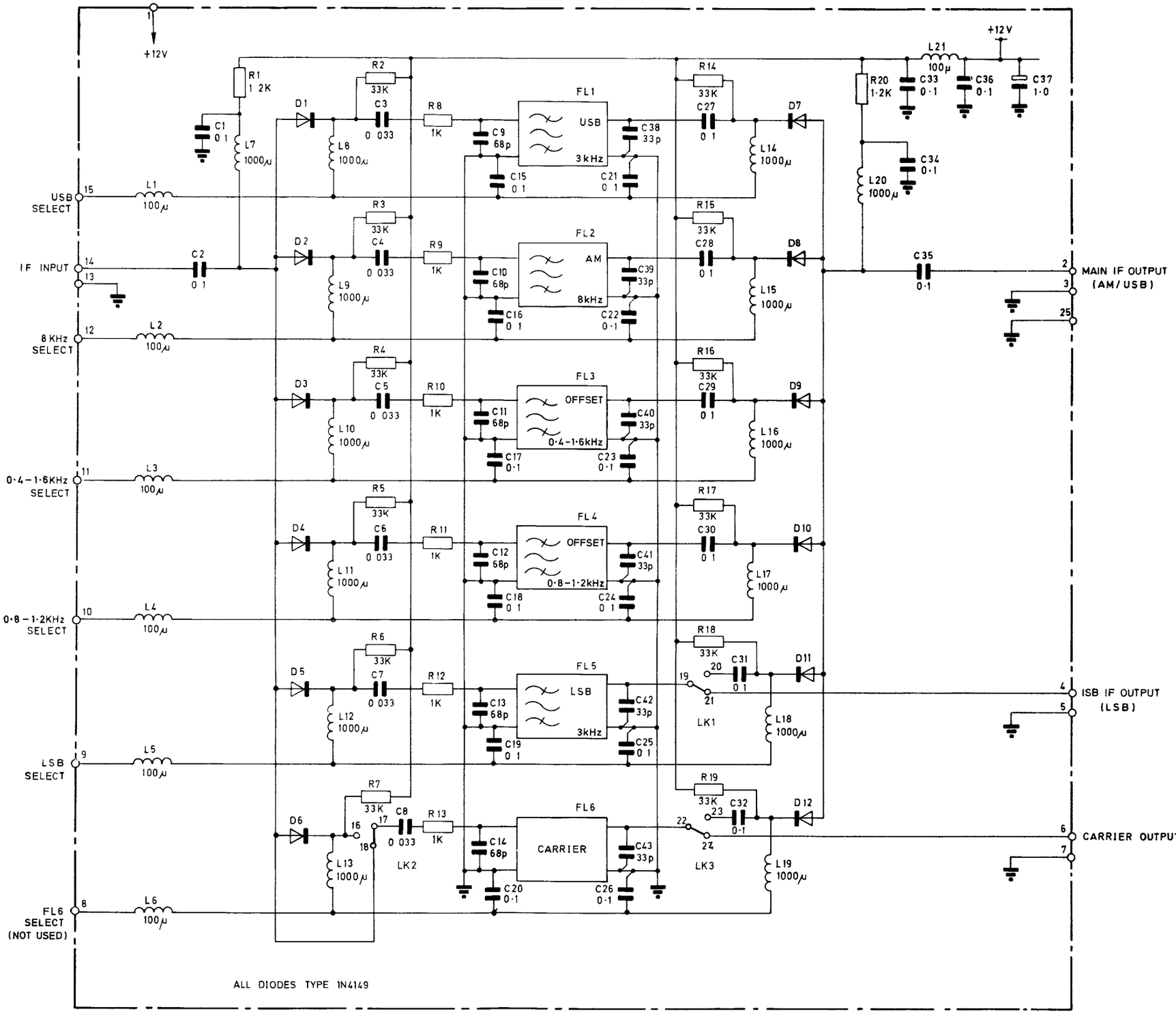


Fig. 46

Chap. 2-1
Page 96

Main I.F/A.F board PM364/1 : component layout

Fig. 46



NOTE DUE TO INVERSION IN RECEIVER USB FILTER FL1 HAS LSB CHARACTERISTICS AND LSB FILTER FL5 HAS USB CHARACTERISTICS.

I.F. filter board PS367: circuit

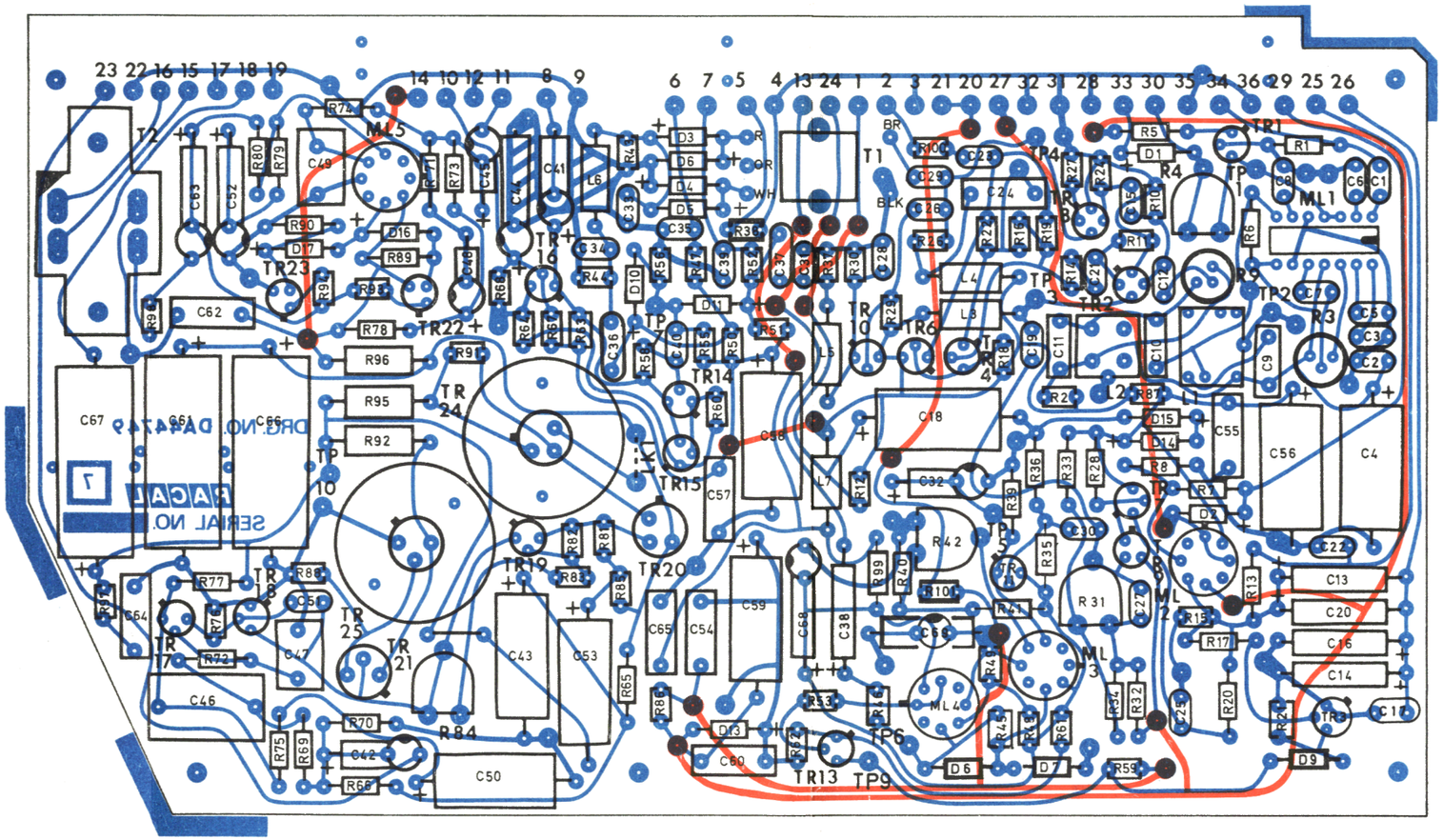


Fig. 46

Main I.F/A.F board PM364/1 : component layout

Fig. 46

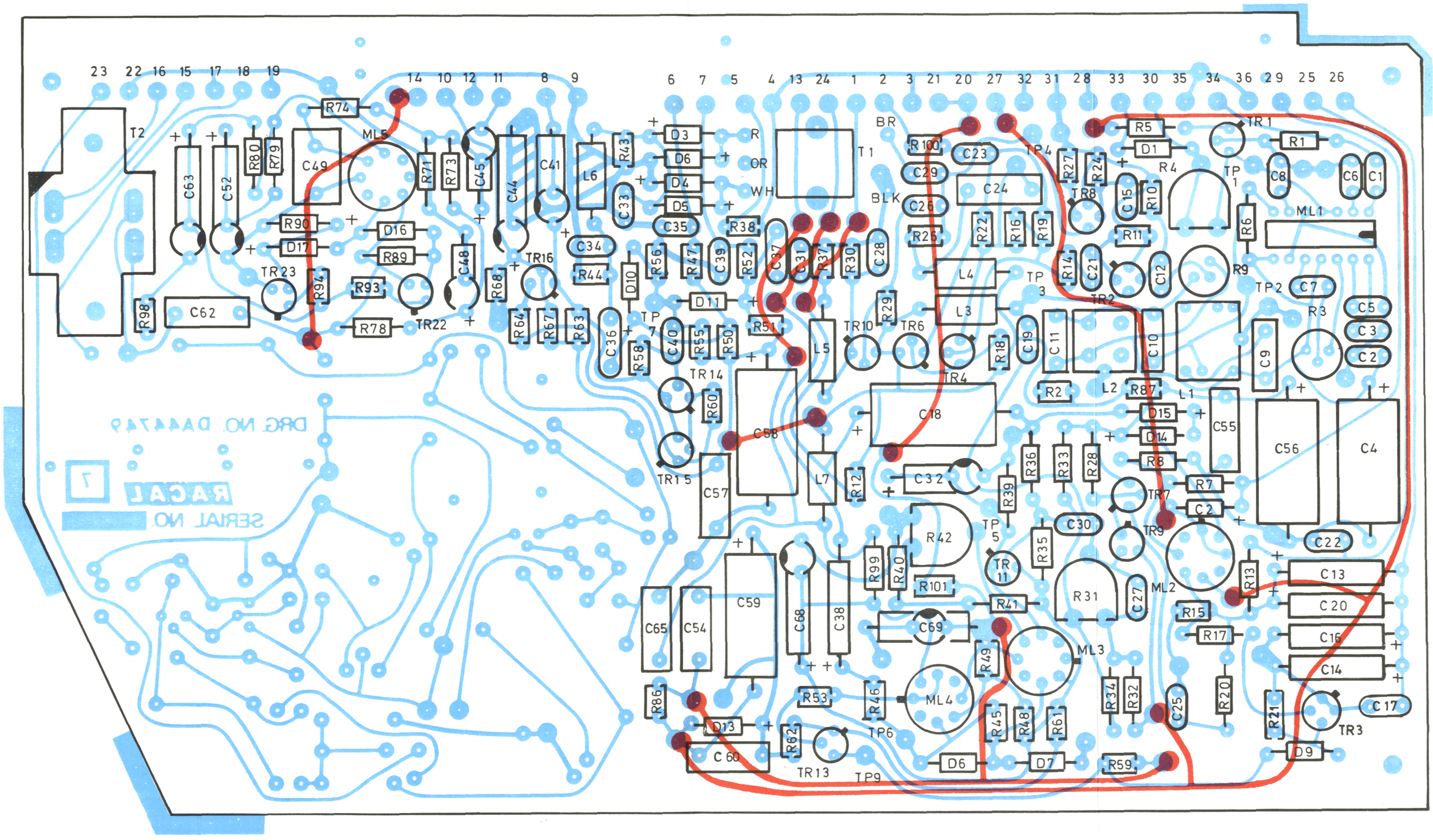
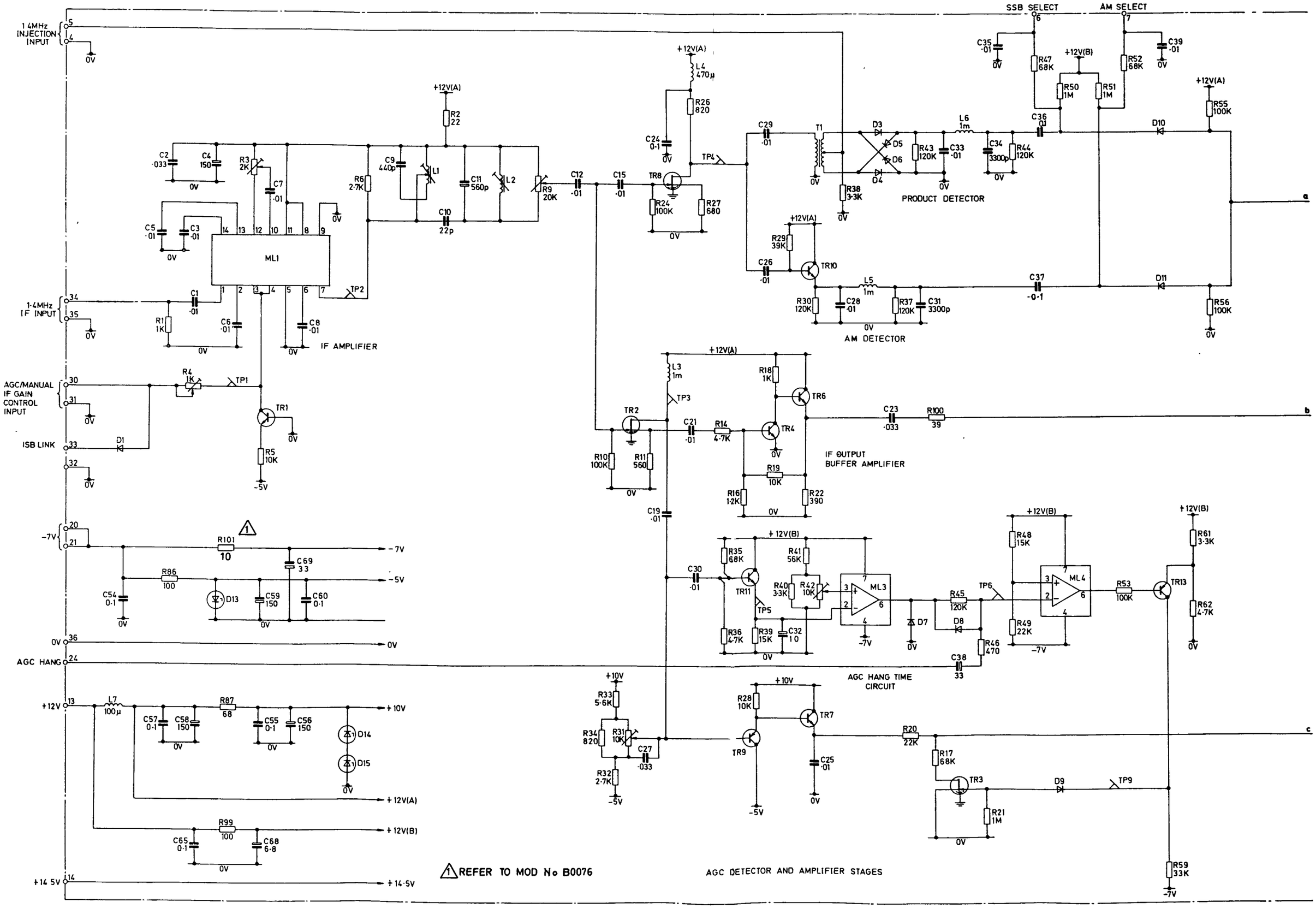


Fig 47

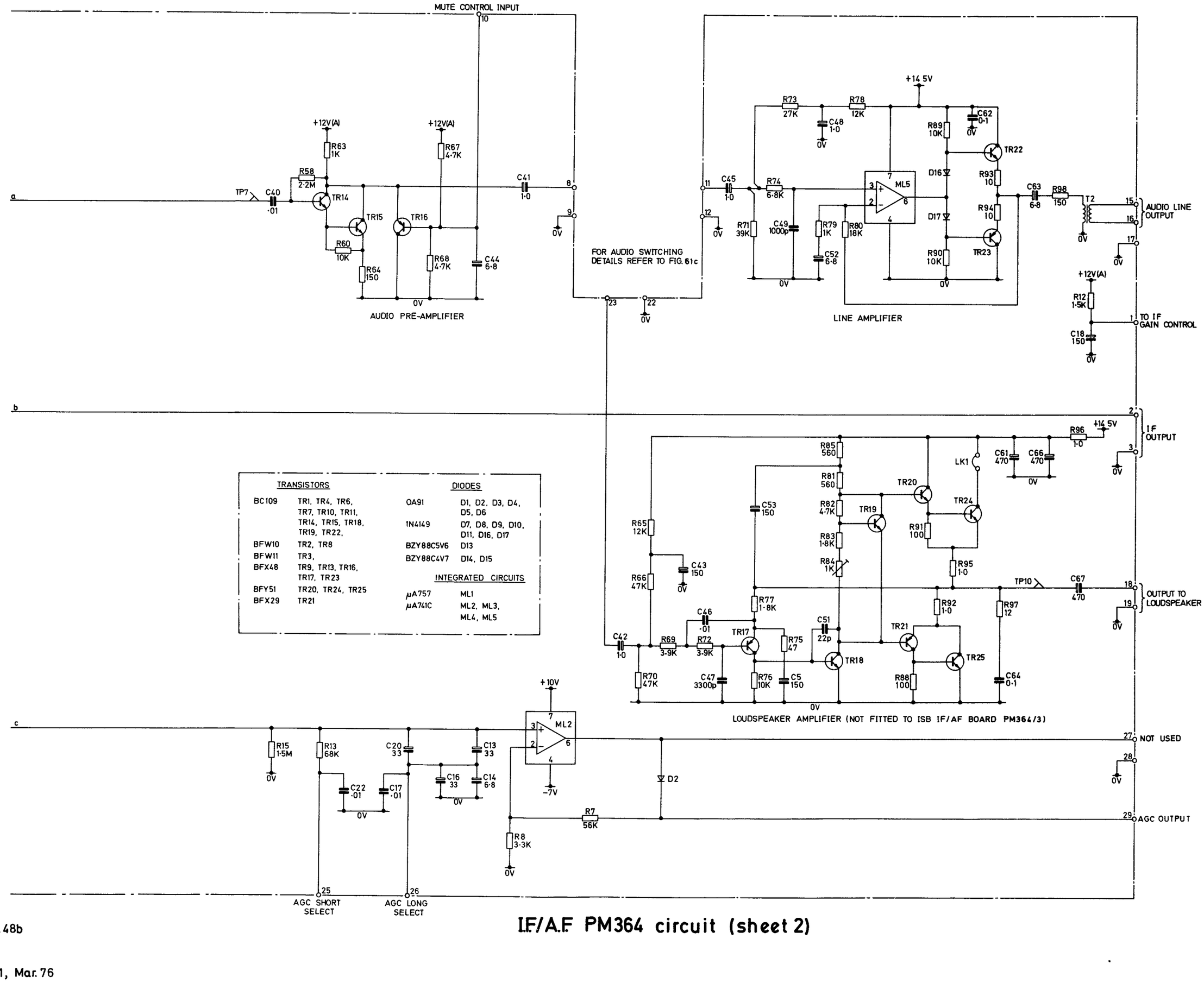
I.S.B./I.F./A.F. board PM364/3: component layout

Fig 47



I.F/A.F board PM364: circuit (sheet 1)

Fig. 48a



TRANSISTORS		DIODES	
BC109	TR1, TR4, TR6, TR7, TR10, TR11, TR14, TR15, TR18, TR19, TR22,	OA91	D1, D2, D3, D4, D5, D6
BFW10	TR2, TR8	1N4149	D7, D8, D9, D10, D11, D16, D17
BFW11	TR3,	BZY88C5V6	D13
BFX48	TR9, TR13, TR16, TR17, TR23	BZY88C4V7	D14, D15
BFY51	TR20, TR24, TR25	INTEGRATED CIRCUITS	
BFX29	TR21	µA757	ML1
		µA741C	ML2, ML3, ML4, ML5

Fig. 48b

I.F/A.F PM364 circuit (sheet 2)

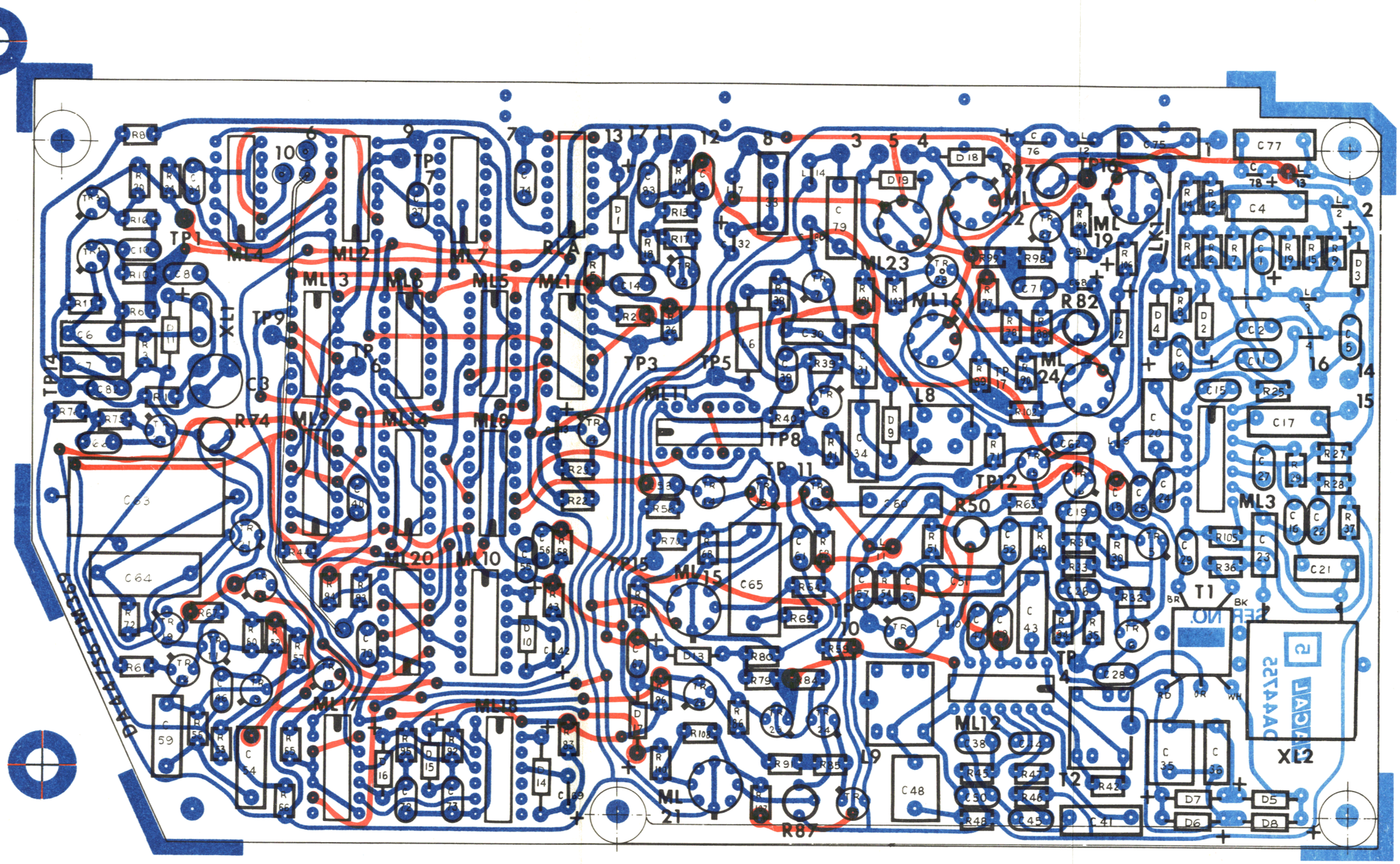


Fig. 49

A.F.C. board PM369: component layout

Fig. 49

Chap. 2-1

Page 101

AL1, Mar. 76

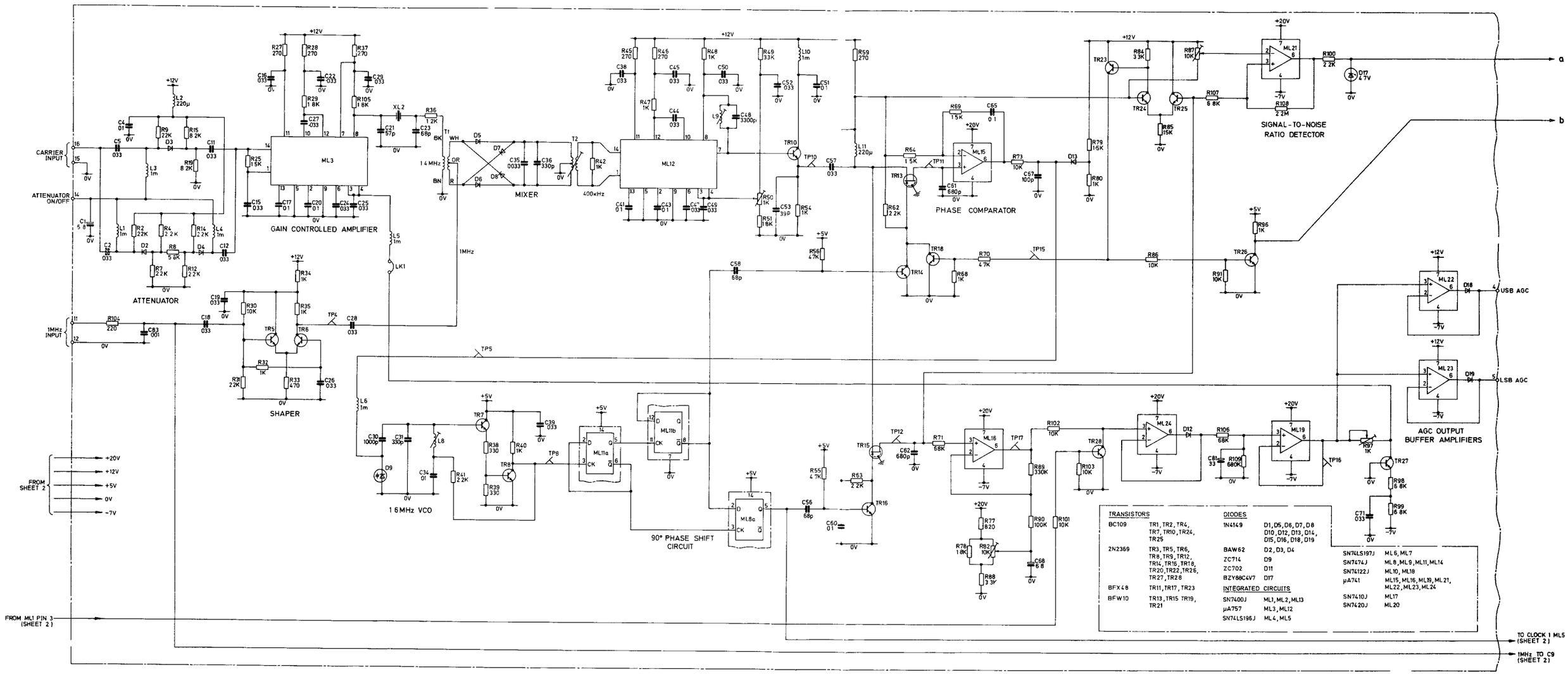


Fig. 50a

A.F.C. board PM369: circuit (sheet 1)

Fig. 50a

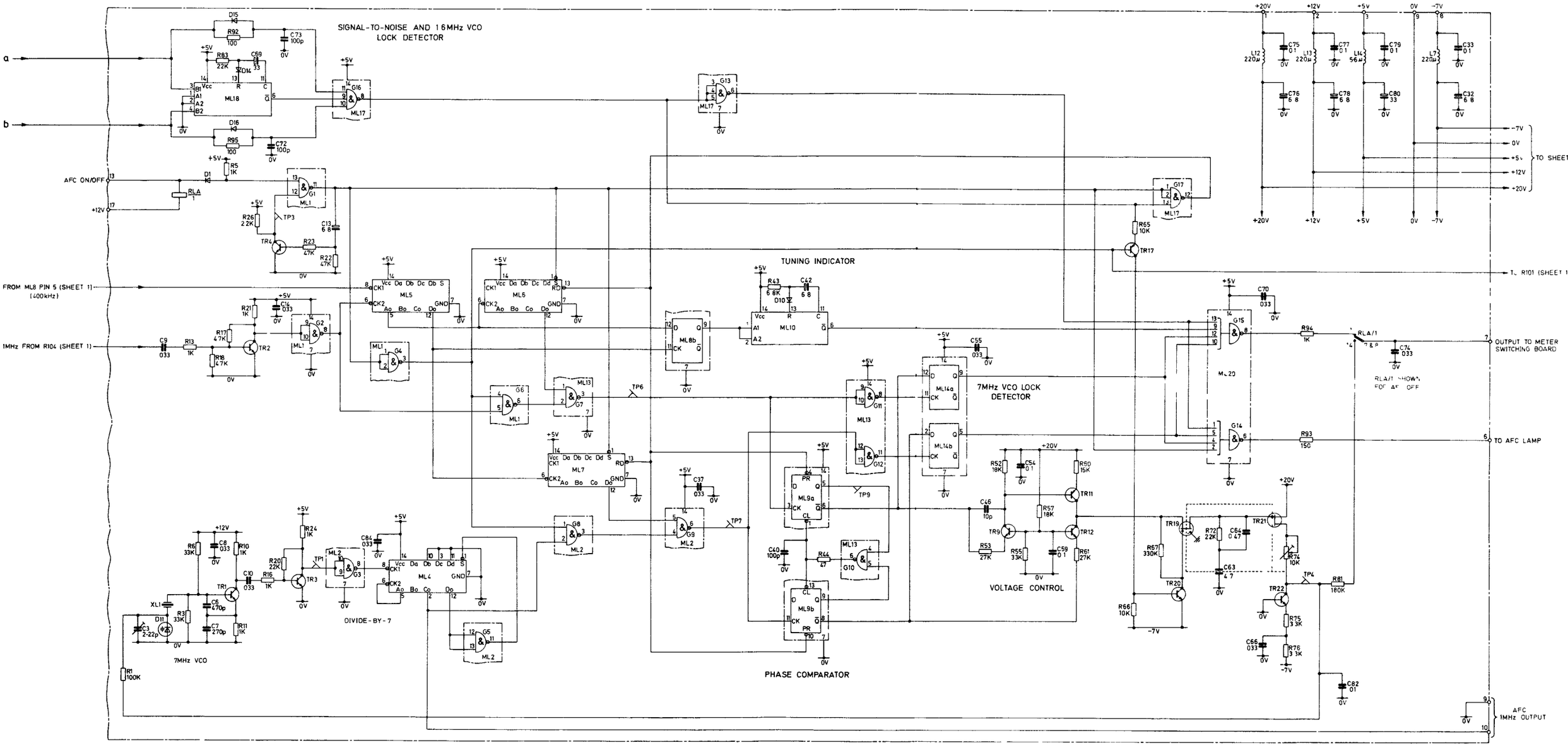


Fig. 50b

A.F.C. board PM369: circuit (sheet 2)

Fig. 50b

AL1, Mar. 76

Chap. 2-1

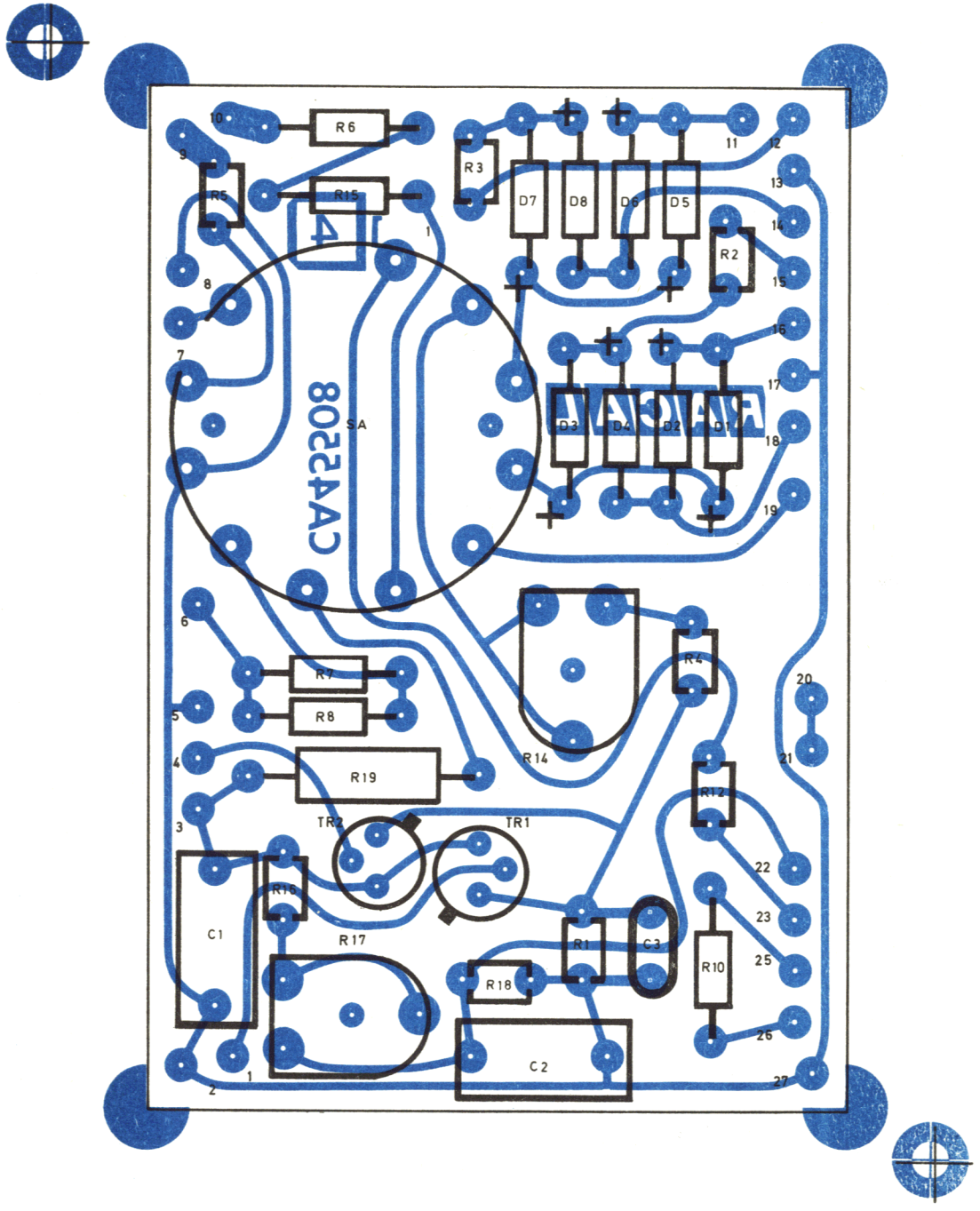


Fig. 51 Meter switching board PM419: component layout

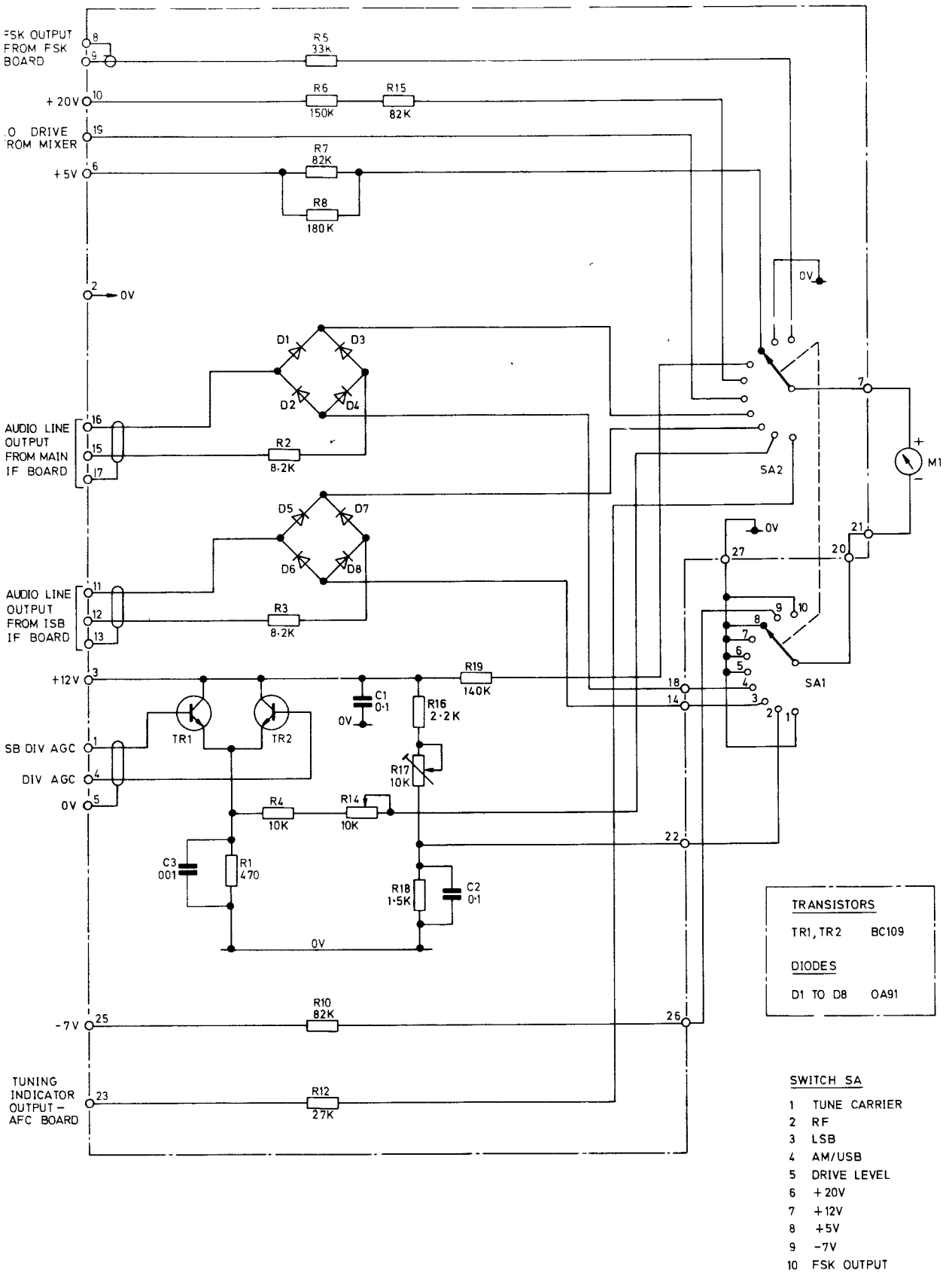


Fig.52 Meter switching board PM 419:circuit

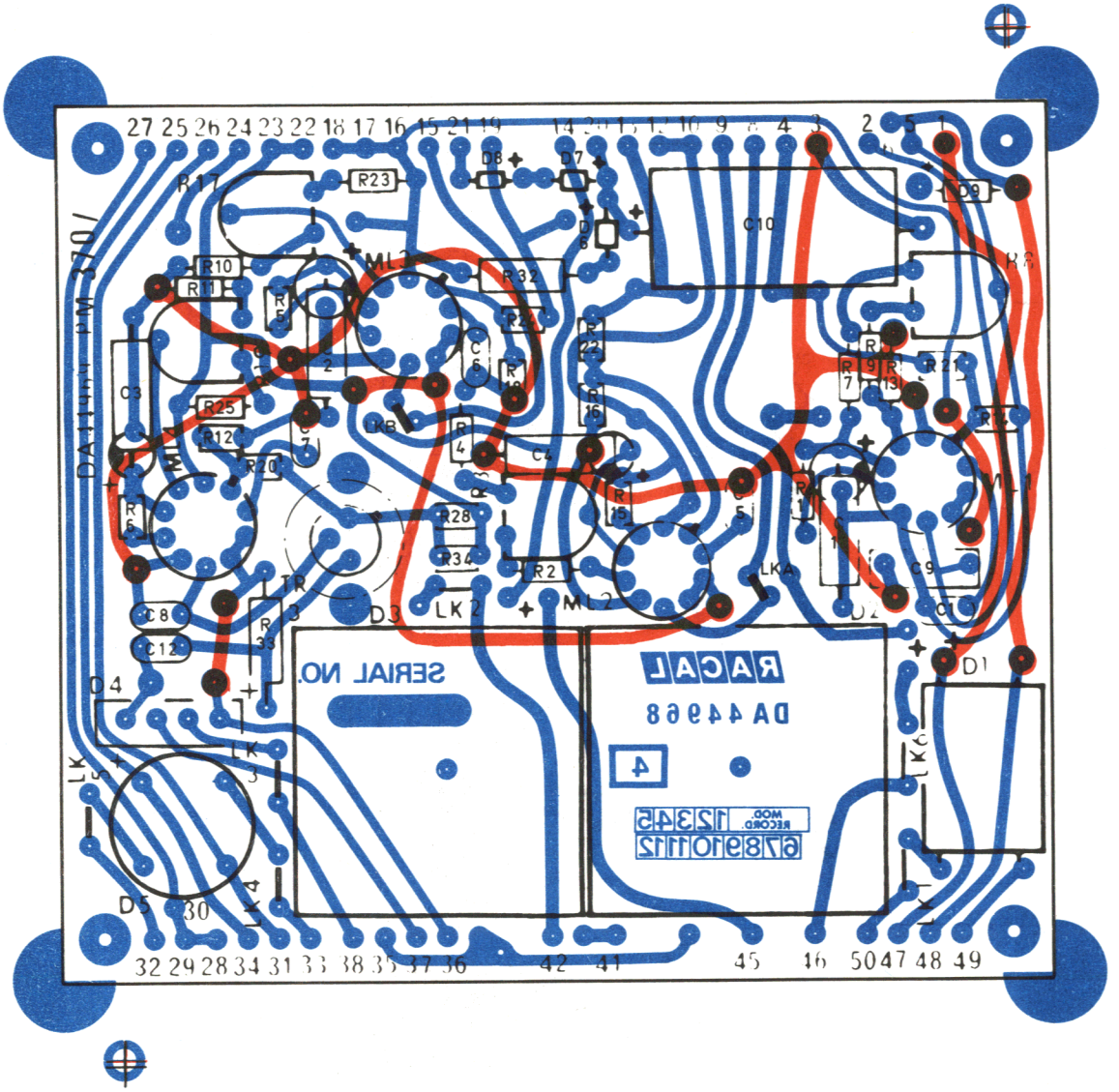


Fig.53 Regulator board PM370: component layout

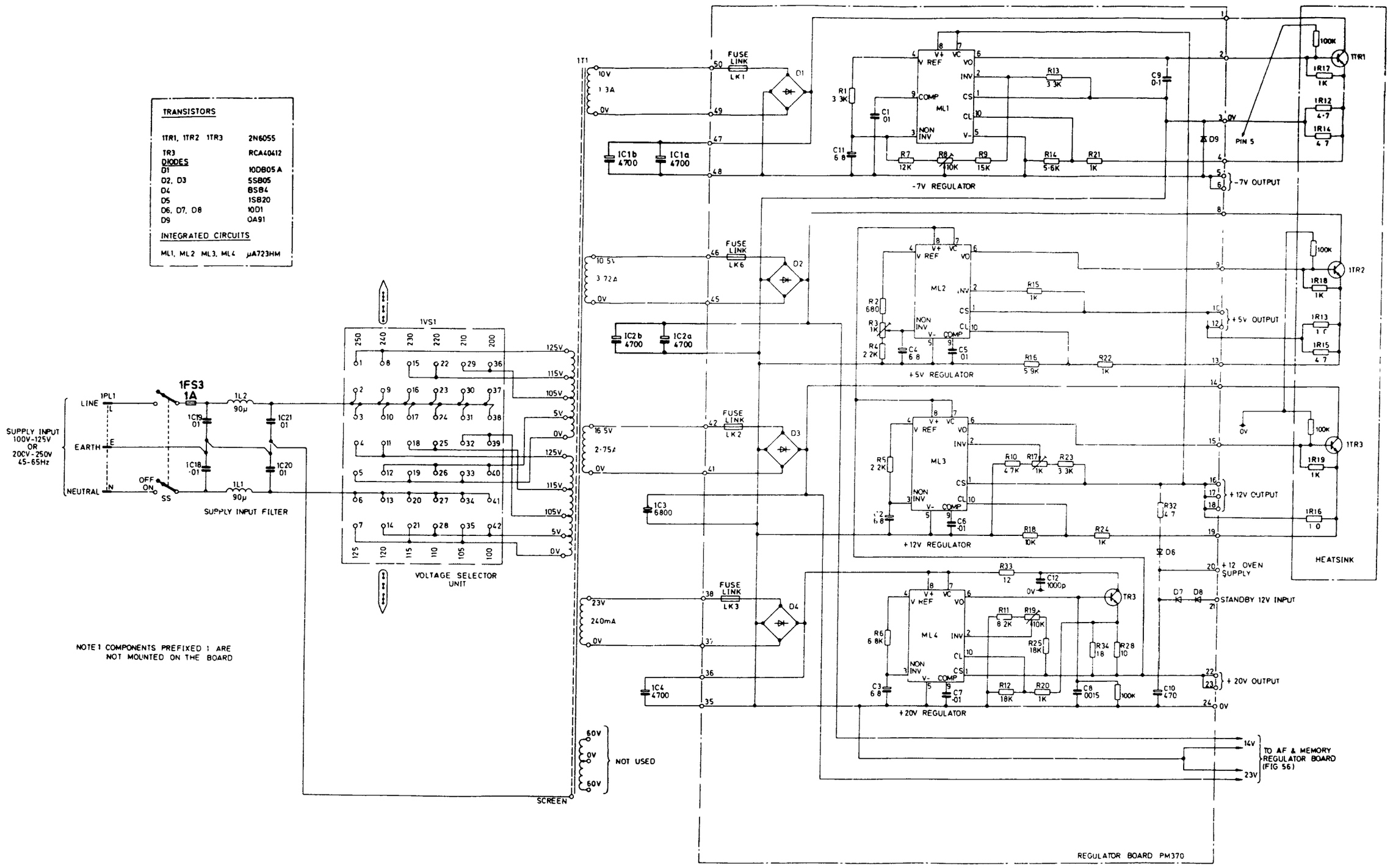


Fig. 54

Power supply: circuit

Fig.54

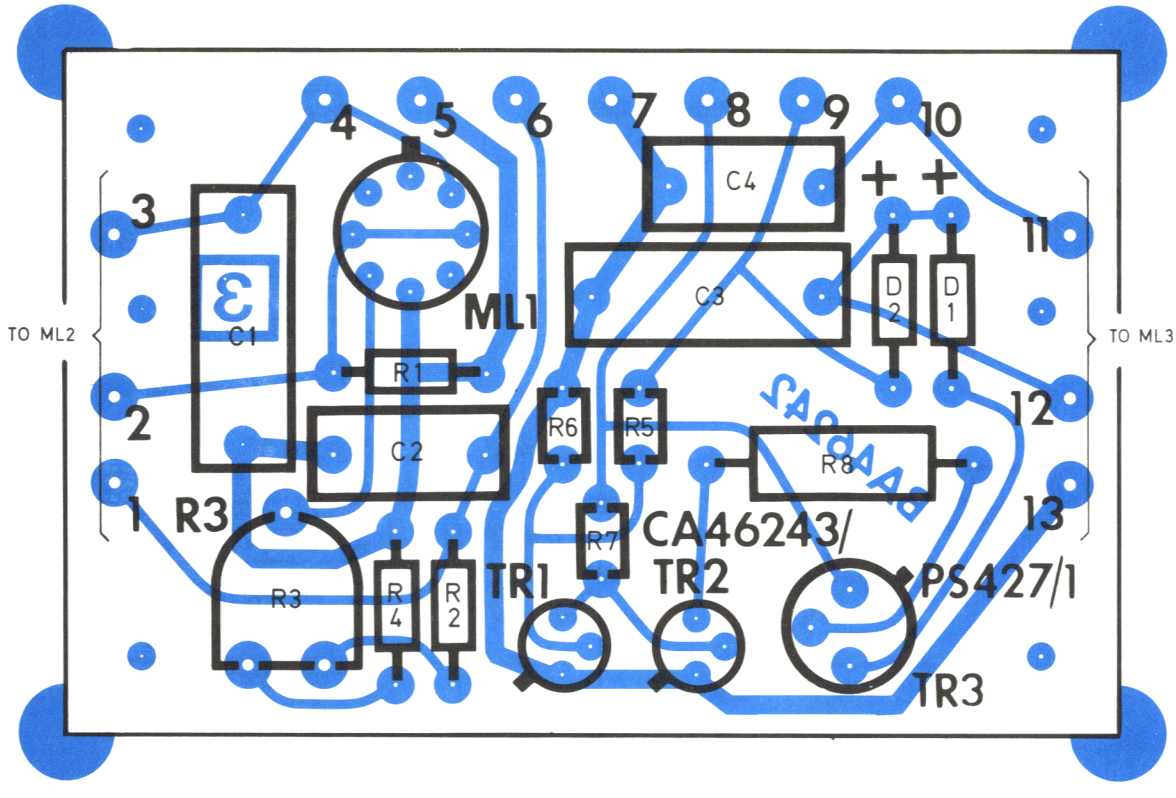


Fig. 55 A.F. and memory regulator board PS427/1 : component layout

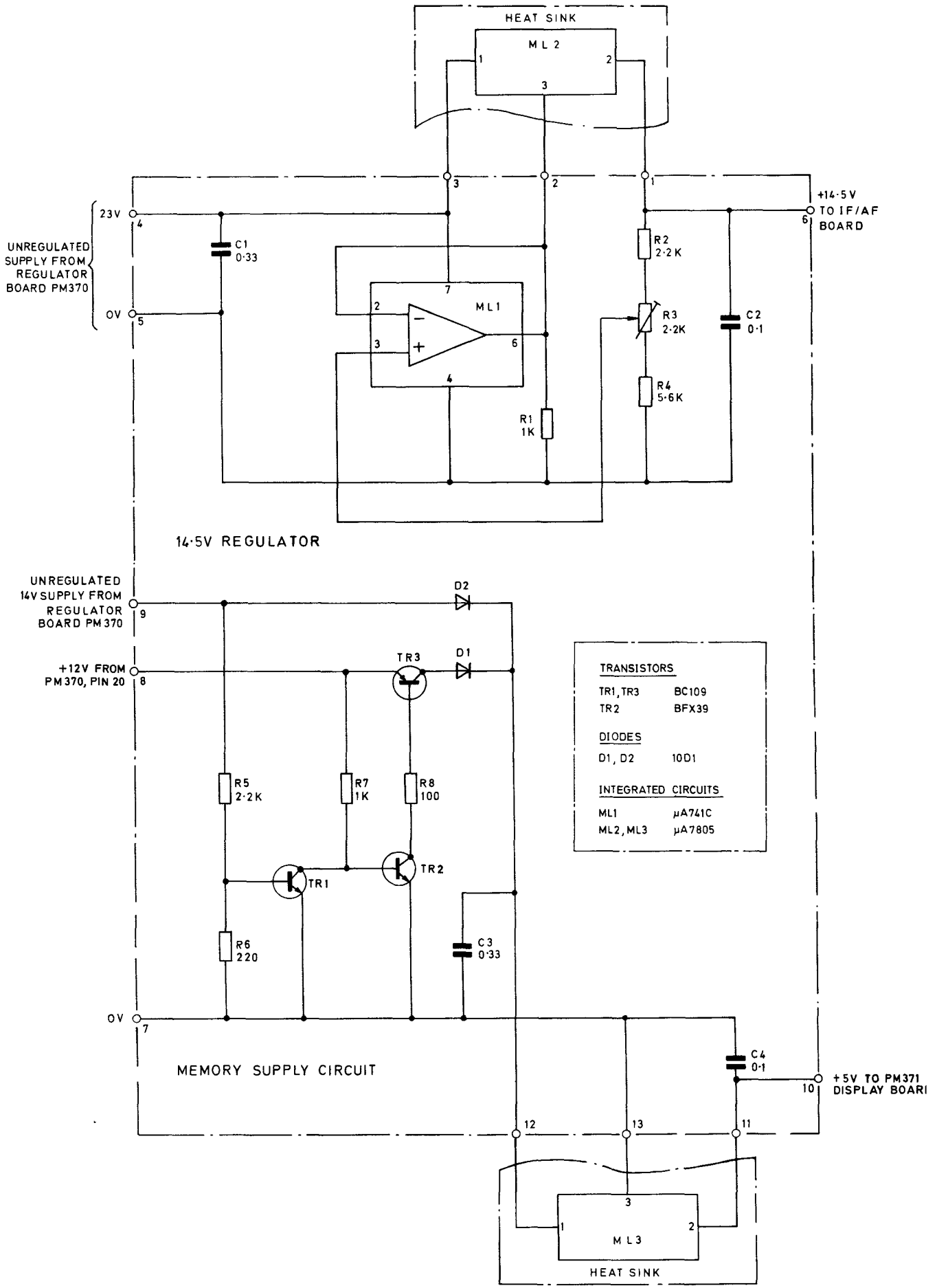
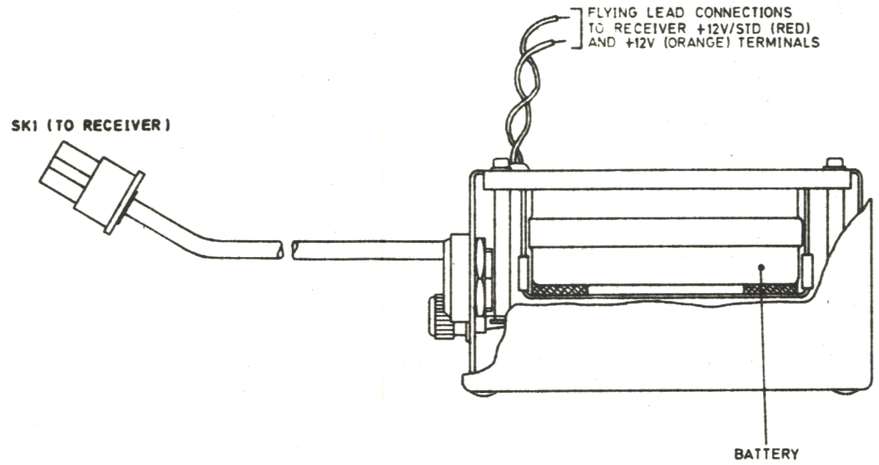
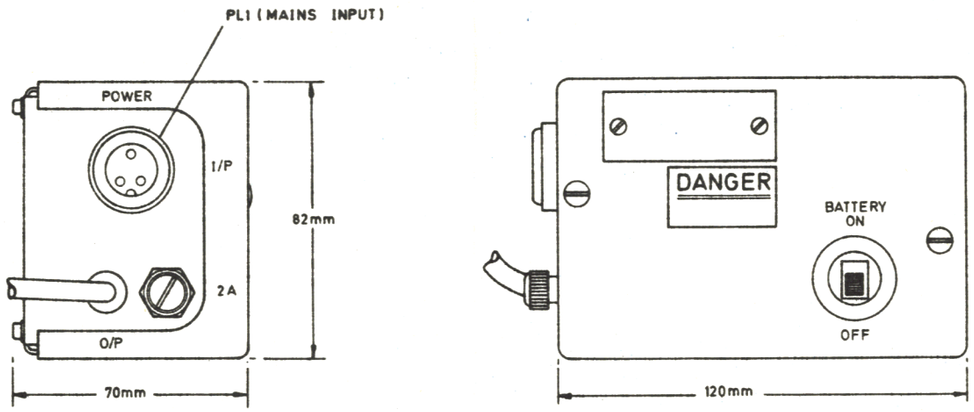
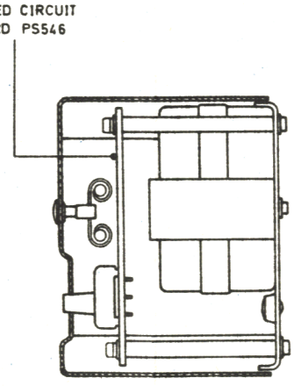


Fig. 56 A.F. and memory regulator board PS427/1: circuit







SECTIONAL VIEW

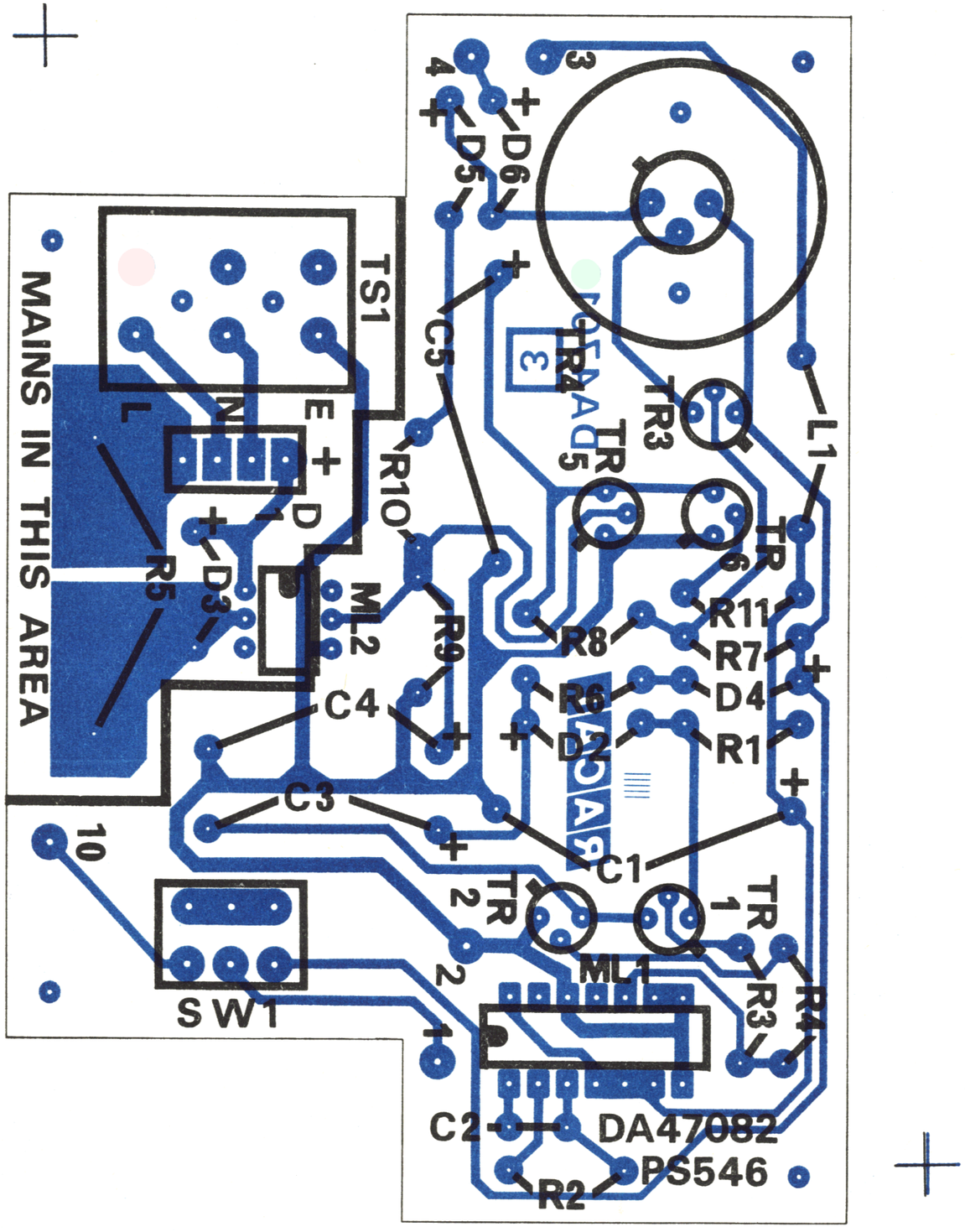
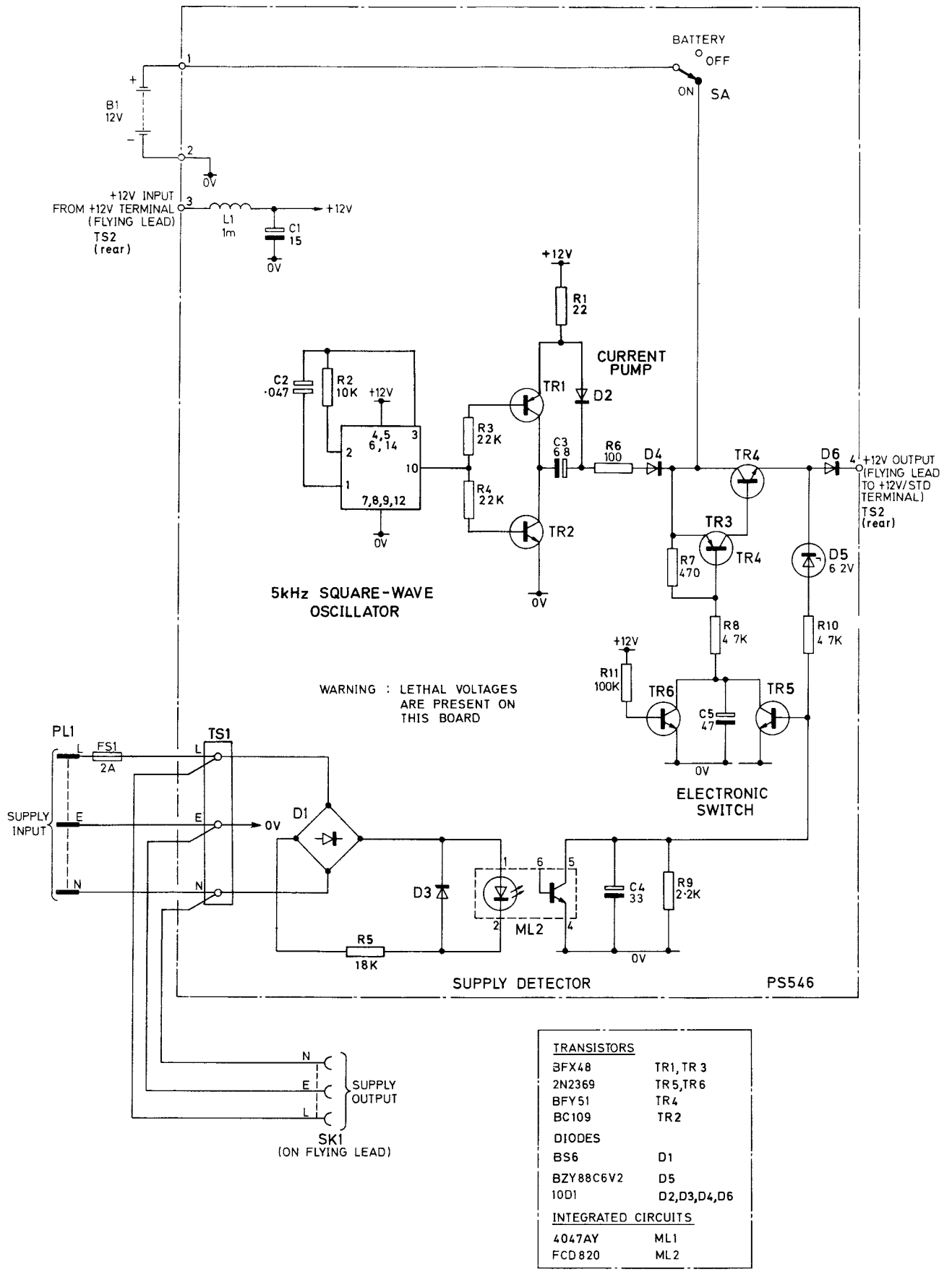


Fig. 57 **Battery module MS540: component layout** Fig. 57



TRANSISTORS	
BFX48	TR1, TR 3
2N2369	TR5, TR6
BFY51	TR4
BC109	TR2
DIODES	
BS6	D1
BZY88C6V2	D5
10D1	D2, D3, D4, D6
INTEGRATED CIRCUITS	
4047AY	ML1
FCD820	ML2

Fig. 58 Battery module MS540: circuit

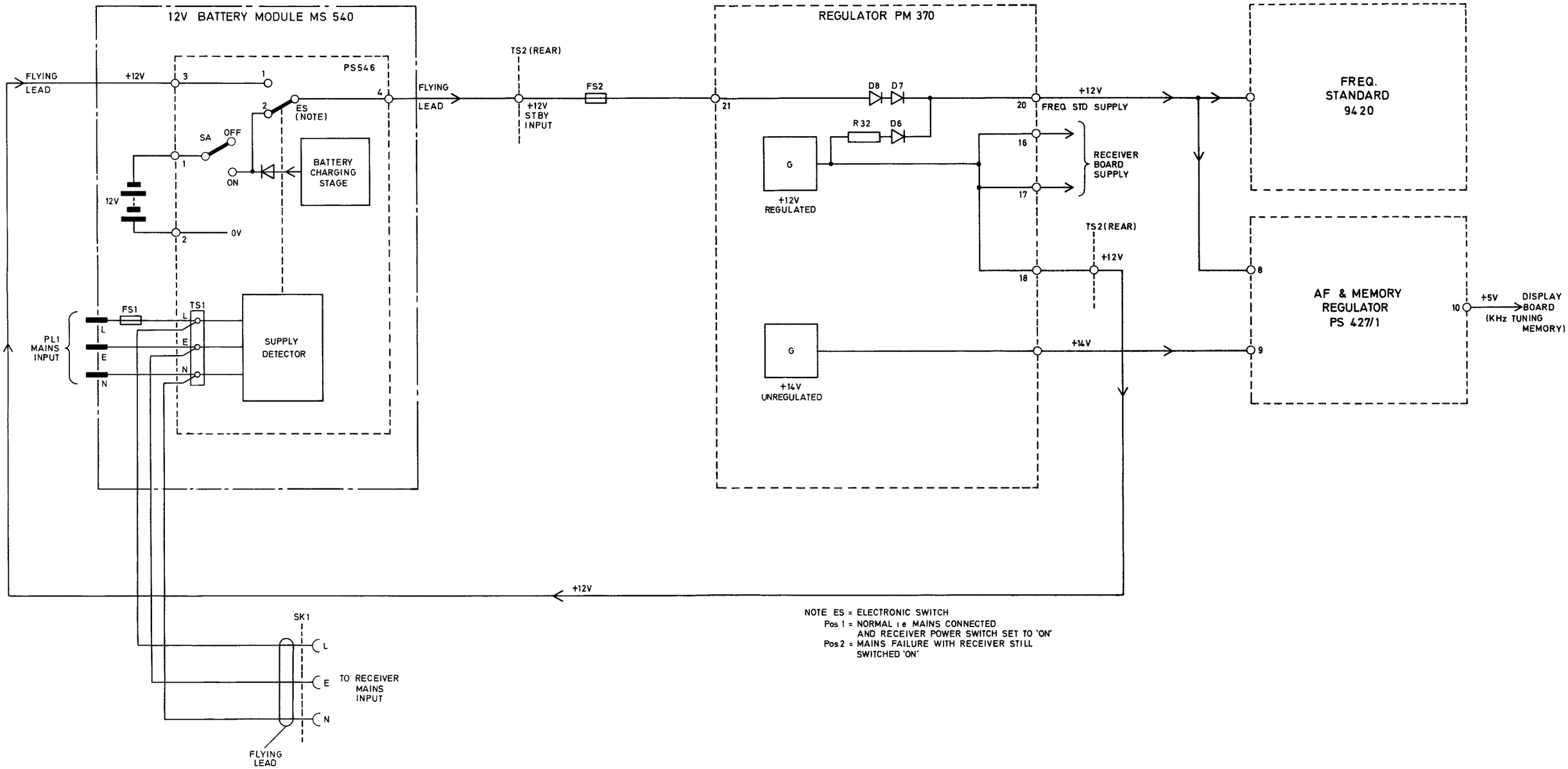
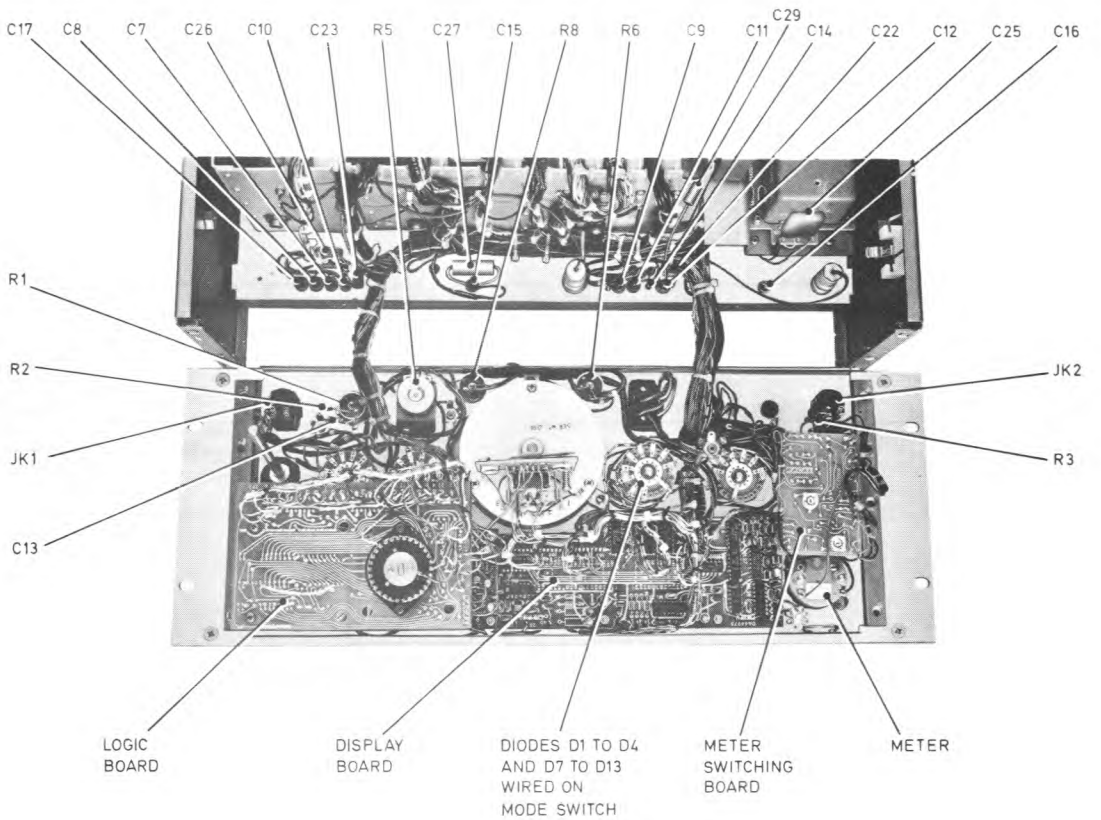
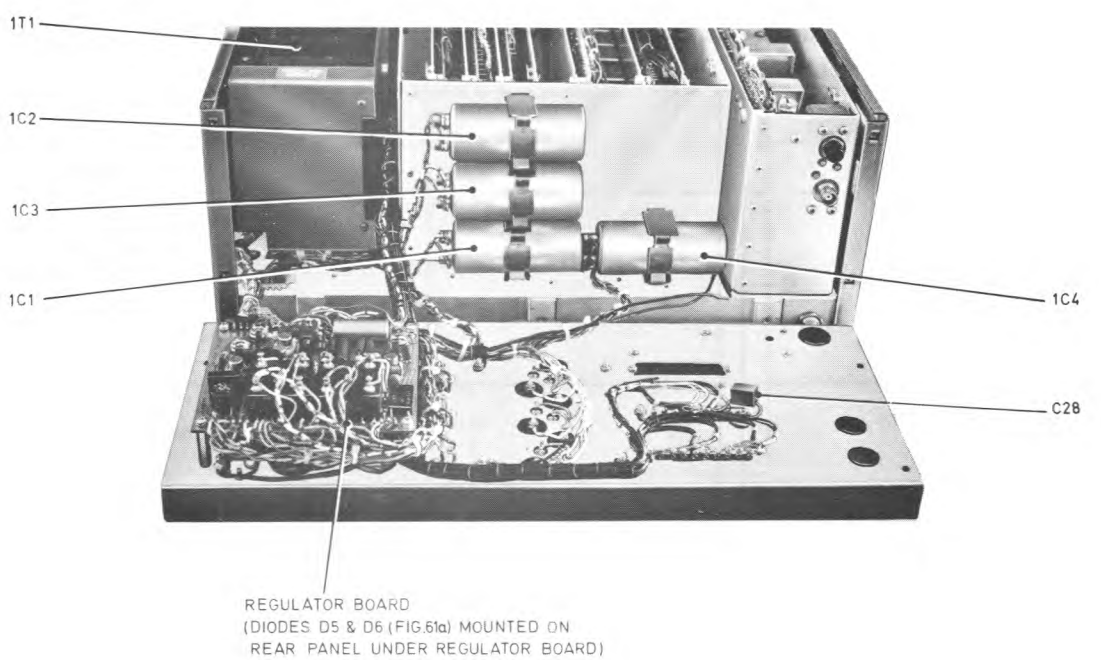


Fig 59

Retention of frequency-setting information: supply flow diagram

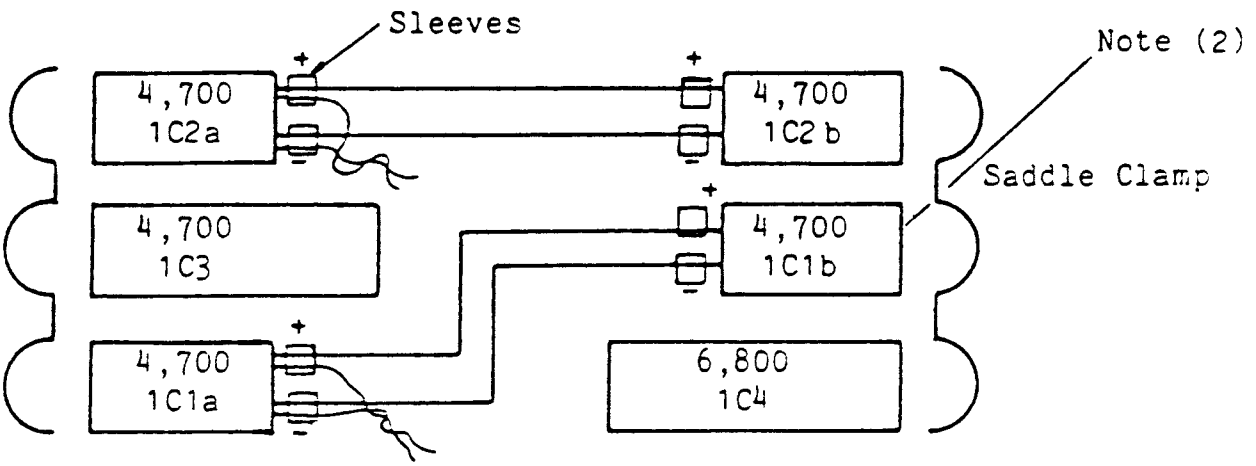


FRONT PANEL LOWERED



REAR PANEL LOWERED

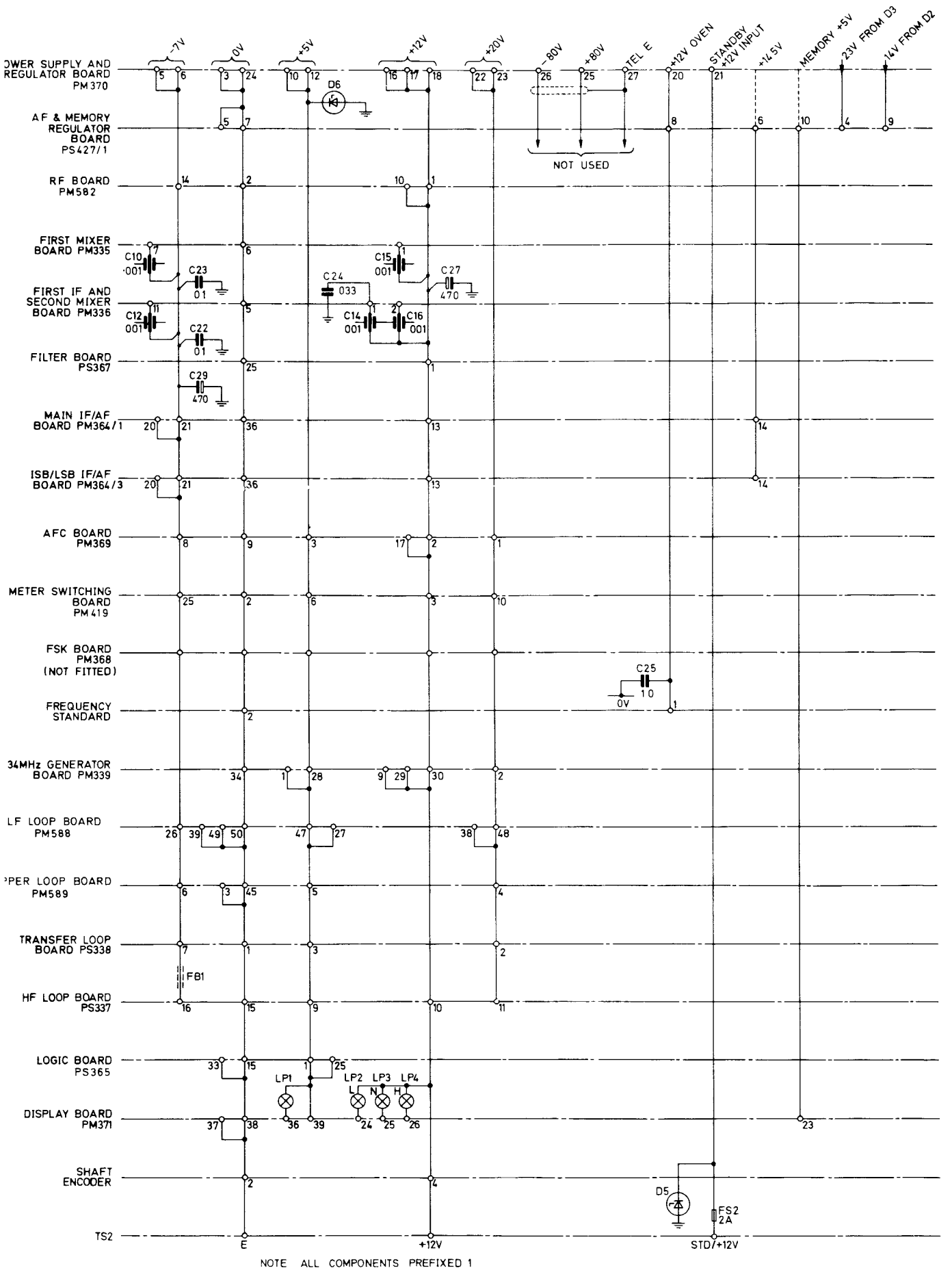
Fig. 60 Chassis front and rear: component layout



NOTE (1) 1C2a & 1C2b connected in parallel, twisted wire links.
1C1a & 1C1b connected in parallel, twisted wire links.

NOTE (2) When fitting Capacitor 1C1b ensure that capacitor contacts are offset by 90° to those of Capacitor 1C3.

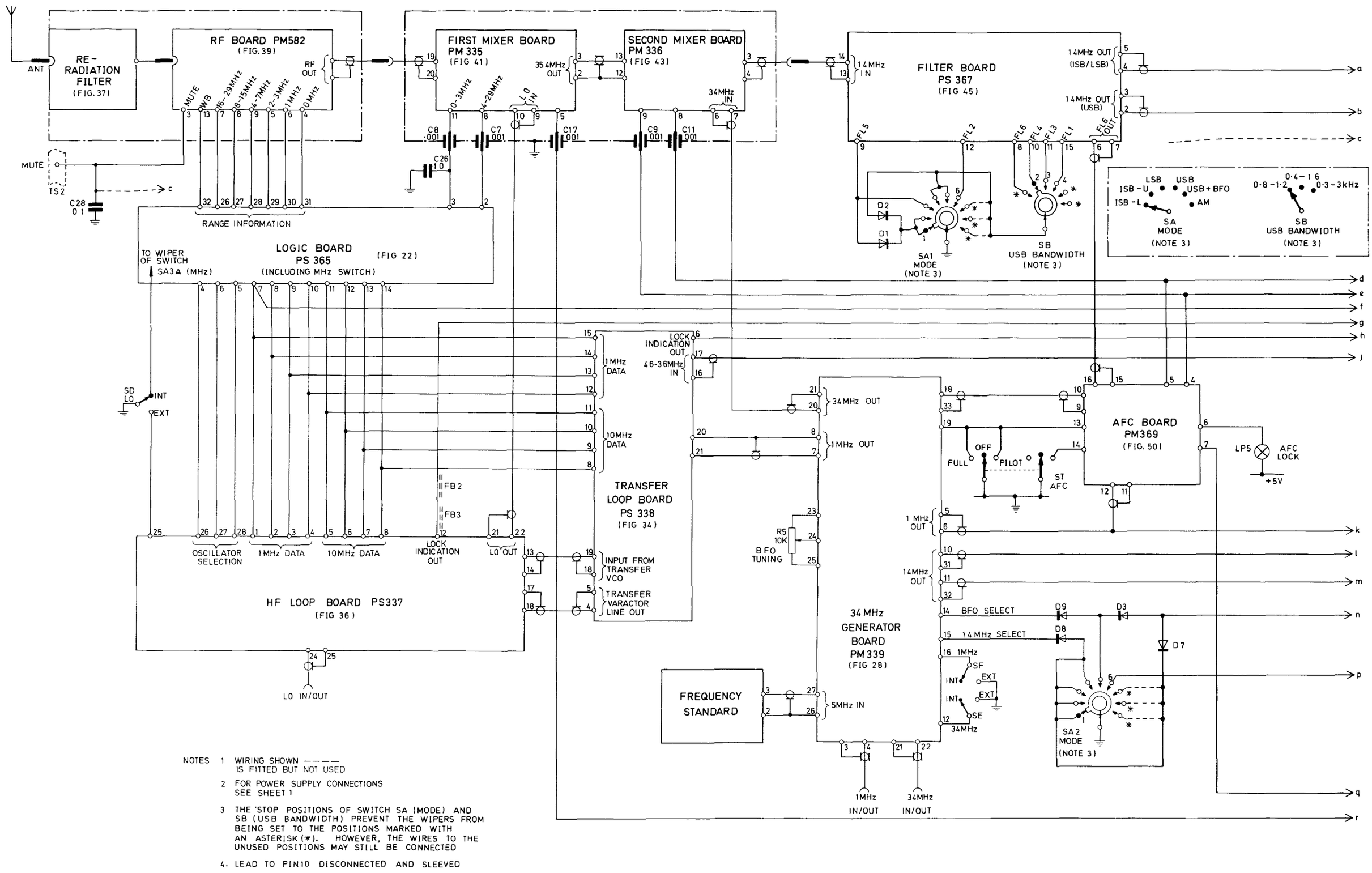
Fig.60a **Chassis rear: capacitor layout (Post Mod TC0024)** Fig.60a



g. 61a

Receiver interconnection diagram (sheet 1)

Fig 61a



NOTES 1 WIRING SHOWN – – – – IS FITTED BUT NOT USED

2 FOR POWER SUPPLY CONNECTIONS SEE SHEET 1

3 THE 'STOP POSITIONS OF SWITCH SA (MODE) AND SB (USB BANDWIDTH) PREVENT THE WIPERS FROM BEING SET TO THE POSITIONS MARKED WITH AN ASTERISK (*). HOWEVER, THE WIRES TO THE UNUSED POSITIONS MAY STILL BE CONNECTED

4. LEAD TO PIN10 DISCONNECTED AND SLEEVED

Receiver interconnection diagram (sheet 2)

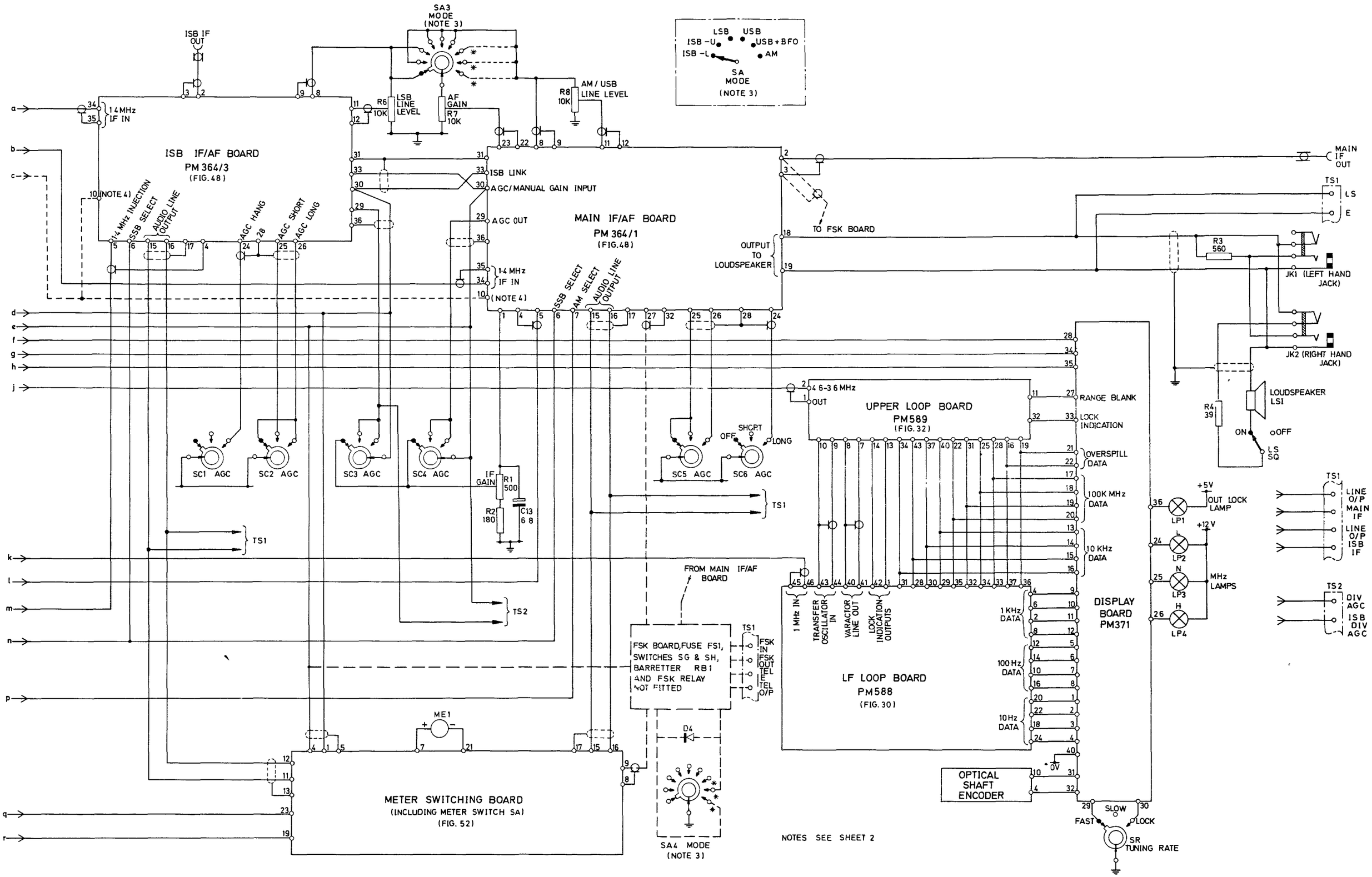


Fig. 61c

Receiver interconnection diagram (sheet 3)

Fig.61c
Chap 2-1
Page 117/118

Mar 83 (Amdt 9)

Chapter 2-1 Annex A

A.F.C. BOARD PM664

CONTENTS

Para.

1	Introduction
2	Input attenuator and amplifier
4	Mixer
5	400 kHz amplifier
6	AGC detector and amplifier
7	Signal-to-noise detector
8	1 MHz generator
9	Phase comparator
10	Divide-by-five stage
11	Digital mixer
15	2 kHz oscillator
16	Binary counter
18	Digital-to-analogue converter
19	Tuning indicator
20	Control monostable
21	A.F.C. lock lamp
22	ON-OFF switching
25	Adjustments

Fig.

		Page
1	Functional diagram: a.f.c. control system	7
2	A.F.C. board PM664: layout	9
3A	A.F.C. board PM664: circuit	10
3B	A.F.C. board PM664: circuit	11

Introduction

1 The a.f.c. board PM664 is a fully-interchangeable CMOS alternative to the PM369; it has an improved performance, and is fitted in receivers from serial number 1721 onwards.

Input attenuator and amplifier

2 The 1.4 MHz carrier signal is applied to an IF amplifier via an attenuator which is controlled by the front panel A.F.C. switch. When this switch is set to FULL CARRIER, an earth is applied to board pin 14; when the switch is set to PILOT CARRIER the earth is removed. The earth signal controls the transmission gate switch ML1 so that either an unattenuated signal (PILOT CARRIER) or 20 dB attenuated signal (FULL CARRIER) is applied to the 1.4 MHz IF amplifier. ML1 also performs the necessary logic inversion on the input from the A.F.C. switch.

3 The IF amplifier comprises ML2 and associated components and incorporates automatic gain control of approximately 38 dB. The output is passed through a crystal filter to remove out-of-band signal components.

Mixer

4 The mixer consists of ML3 and associated components. The 1.4 MHz signal is mixed with a 1 MHz reference to produce a 400 kHz output; the circuit is tuned to this frequency by L4 and C20. Bias is provided by R31, R33, R35 and R36 and the conversion gain is determined by R34. R29 is adjusted to balance the mixer so that the 1 MHz signal is suppressed.

400 kHz amplifier

5 The 400 kHz signal from the mixer is applied to the input of ML4, which provides 0 to 38 dB of automatically controlled gain. The amplified signal is buffered by TR3 and TR4 and applied to the waveform shaper comprising TR5 and TR6, connected as a long-tailed pair. The waveform shaper acts as a zero-crossing detector and provides an output suitable for driving CMOS logic.

AGC detector and amplifiers

6 A proportion of the 400 kHz signal is taken from the buffer output at TR4 emitter via C27 and fed to the AGC detector. The ac signal is rectified by diode D1, producing an AGC voltage at its cathode equal to the peak value of the ac signal plus 6 volts. The AGC voltage is filtered and amplified by ML5A; a dc offset is introduced, set by R5. The AGC time constants are set by R20, R22 and C16 to provide an attack time of approximately 150 mS and a decay time of approximately 1.55. The AGC voltage can be dumped by applying a logic '0' to board pin 17, which turns on TR2 and discharges C16; otherwise it is applied to the distribution amplifiers ML5B, ML5C and ML5D. R37 and R41 match the AGC voltage derived from the carrier with the main receiver AGC. R37 sets the slope of the carrier AGC characteristic and R41 offsets the output voltage so that it is about 80 mV below the main AGC voltage, corresponding to a 10 dB signal change. The carrier AGC is applied to the main AGC lines on the IF1 and IF2 boards and only takes control when the peak signal level falls by 10 dB.

Signal-to-noise detector

7 ML10a compares the peak signal voltage from the 400 kHz buffer stage with a level preset by the potential divider R113, R45 (which provides the adjustment) and R114. The output from ML10a is applied to the comparator ML10b via timing components to produce a fast-decay-slow-attach characteristic; the AFC is inhibited immediately if the carrier disappears and is not enabled until about 70 mS after the carrier returns. R45 is adjusted for AFC present on about 1.5 μV emf signal, at which level the LOCK lamp just flickers. The detector also inhibits AFC action if extraneous signals pass through the carrier filter.

1 MHz generator

8 TR8 and associated components form a voltage-controlled crystal oscillator which runs at 7 MHz. The output is converted to TTL level by TR9 and applied to the input of ML7 which is connected with ML6 to form a divide-by-seven circuit. The resultant 1 MHz output is applied to the 34 MHz board. A small proportion of the signal is amplified and converted to CMOS level by TR10.

Phase comparator

9 The output from TR10 is phase-compared with the 1 MHz signal from the 34 MHz board by a phase comparator comprising ML19 and ML20 (a and B). When the AFC is switched OFF a phase difference between the two signals produces a control signal; this is filtered by R94, C55 and C56, buffered by the voltage follower ML16a, then applied to the varactor diode D4 in the 1 MHz generator. In this way the 1 MHz generator is phase-locked to the 1 MHz standard so that when the AFC is first switched ON the 34 MHz generator is not so far off frequency that the carrier is shifted out of the passband of the carrier filter. Switching ON the AFC inhibits the generation of the varactor control signal by setting ML20b and resetting ML20a.

Divide-by-five stage

10 The 1 MHz frequency standard from the buffer TR7 is applied to the input of ML18 which is a divide-by-ten counter wired to divide by five. The resultant 200 kHz signal is produced at two outputs, Q1 and Q2. The phase difference between the Q1 and Q2 outputs is 1 μs which, at 200 kHz, is 72°.

Digital Mixer

11 The function of the mixer is to produce outputs according to the sign and modulus of the difference frequency between the 400 kHz carrier signal and an accurate 400 kHz. The mixer, ML17, is similar in operation to a quadrature mixer with the exception that the clock runs at 200 kHz and the phase difference is 72°. Both of these values are chosen because they are relatively simple to derive from 1 MHz using a divide-by-five counter and neither alter the output timing from that of a true quadrature mixer. The operation is best understood by reference to the timing diagrams.

12 R70, R71, R74 and R75 provide hysterisis around the mixer flip-flops to give increased immunity against noisy edges on the carrier signal, while any fast double edges are filtered out by R79, C45, R78 and C44. The edges are speeded up after filtering by ML12 pins 8, 9, 10 and 11, 12, 13.

13 Two outputs at the difference frequency are produced and fed to the clock and D inputs of ML13a, a D-type flip-flop. If the carrier frequency exceeds the reference ML13a is always clocked when the D input is high, so its Q output is constantly high. If the carrier frequency is lower than the reference ML13a is always clocked when the D input is low, so its Q output is constantly low. In this way the sign of the difference frequency is indicated by the Q output of ML13a.

14 One of the difference frequency outputs is applied to the tuning indicator and the other, together with the sign indication, is applied to the binary counter.

2 kHz oscillator

15 ML14 pins 8, 9, 10 and 11, 12, 13 are two CMOS inverting gates biased into the linear region and wired as an oscillator with C46 providing positive feedback. The oscillator is disabled when the AFC is switched ON.

Binary counter

16 When the AFC is ON a 12-bit synchronous up/down binary counter, consisting of ML22, ML23 and ML24, is incremented at the error frequency rate, up or down, according to the sign indication. The error frequency is applied to the monostable input ML15 pin 4 where pulses corresponding to an error frequency of less than 1.4 Hz are inhibited; if the error frequency exceeds 1.4 Hz the pulses are applied to the counter input. R88 and C53 delay the clock slightly so that the counter is not clocked at the same time as the up/down data changes. The ten most significant digits are applied to the D-A converter.

17 When the AFC is OFF the counter is clocked from the 2 kHz oscillator and the up/down information is taken from the comparator ML10d, which compares the voltage output from the D-A converter with the varactor voltage of the 7 MHz phase locked oscillator. This causes the counter to be held in such a state that when the AFC is switched ON and the D-A converter takes control of the varactor line, the initial frequency of the VCO is sufficiently close to 7 MHz that the signal is held within the passband of the carrier filter.

Digital-to-analogue converter

18 ML21 is a 10-bit multiplying digital-to-analogue converter. The output current is proportional to the multiplying factor, k, which is determined by the logic input from the binary counter, and to the voltage applied to pin 15, the V ref terminal. The converter includes an internal feedback resistor to which the output of ML16b is connected. A proportion of the output is fed back to the V ref terminal by ML16c. The combined effect of the feedback arrangements is to produce a non-linear relationship between K and the output voltage which compensates for the non-linear relationship between control voltage and frequency in the VCO and hence enhances the frequency accuracy of the AFC system.

Tuning indicator

19 Monostable ML15b produces 6 ms pulses at the error frequency rate and these are fed to the front panel meter. The meter performs a mechanical integration of the pulses and gives an apparently constant deflection proportional to the error frequency. When the AFC is switched ON, the meter is switched over to the varactor control line.

Control monostable

20 Monostable ML15a receives clock pulses from the digital mixer and produces 700 ms pulses at the error rate. The Q output of the monostable is connected to the Enable terminal of the counter chain, which is allowed to count only if the monostable remains set. Thus, if the pulses are greater than 700 ms apart, the counters will not be incremented; therefore no AFC signal is produced for an error frequency, of less than 1.4 Hz. This creates a 'dead-band' which prevents the AFC circuit from oscillating around the set frequency

AFC lock lamp

21 The AFC lock lamp is driven by TR11 from the transmission gate ML8 pin 9. The transmission gate is switched by the output of the NAND gate ML9 pin 9, which has three inputs connected so that the AFC lamp will light only if the following conditions apply:

(a) AFC is ON.

(b) The signal-to-noise ratio is acceptable.

(c) The error frequency is less than 1.4 Hz.

ON-OFF Switching

22 The AFC is switched ON or OFF by the presence or absence of an earth signal at pin 13 of the board. This is applied to the 'anti-bounce' circuit R63, C37 and ML10c, then routed to produce the required conditions when the AFC is switched OFF or ON.

23 When the AFC is switched OFF, carrier derived AGC to the main receiver is dumped. ML17b is reset, so that pin 6 of ML12 is low and clock pulses for the counter are taken from the 2 kHz oscillator, which is enabled by a '0' on ML14 pin 12. ML13a is reset, so that pin 2 of ML12 is low, and up/down information is taken from the output of comparator ML10d which is allowed to function by turning off TR13. TR12 is switched on, so that the VCO varactor line is supplied from the phase comparator and loop filter only. ML19 pin 13 is high, enabling reset pulses from the phase comparator, and a '0' on pin 13 of ML11 prevents ML15a from being cleared. Tuning indicator pulses are switched to the meter by the transmission gates of ML8.

24 When the AFC is switched ON, carrier derived AGC is allowed to pass to the main receiver. The '1' is removed from the reset pin of ML17b and is transferred to pin 12 of ML14, disabling the oscillator. Clock pulses for the counter are then taken via the control monostable, from the mixer. TR13 is switched on, holding pin 1 of ML10d low, and the '1' is removed from pin 10 of ML13a; this allows up/down information to be taken from the mixer. TR12 is switched off, ML20b is set and ML20a is reset, allowing the D/A converter only to supply the VCO varactor line. The transmission gates of ML8 switch the varactor voltage to the meter.

Adjustments

25 Refer to Chapter 2-5, para.41 for details of adjustments to the A.F.C. board PM664.

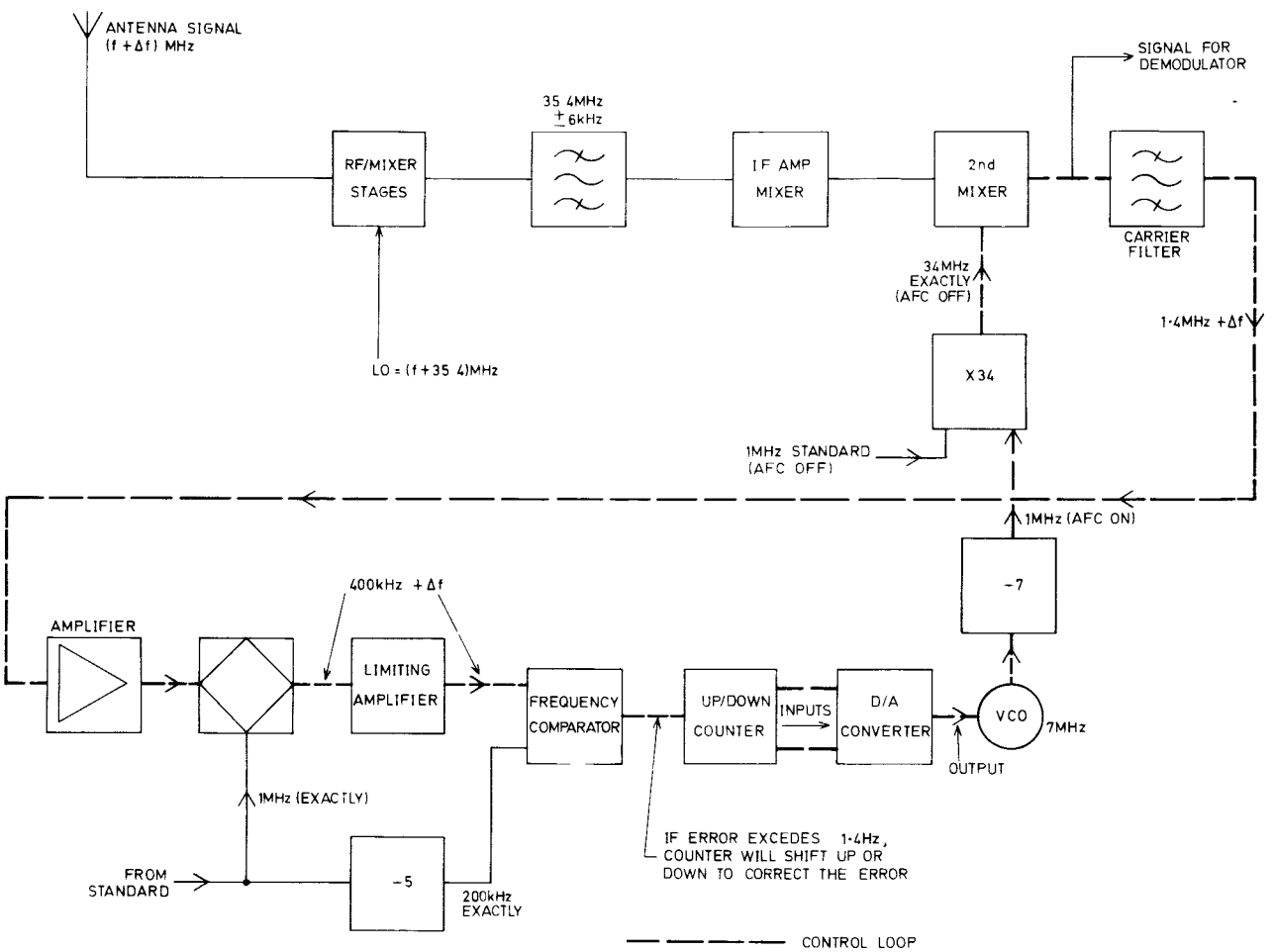


Fig.1 Functional diagram: a.f.c. control system

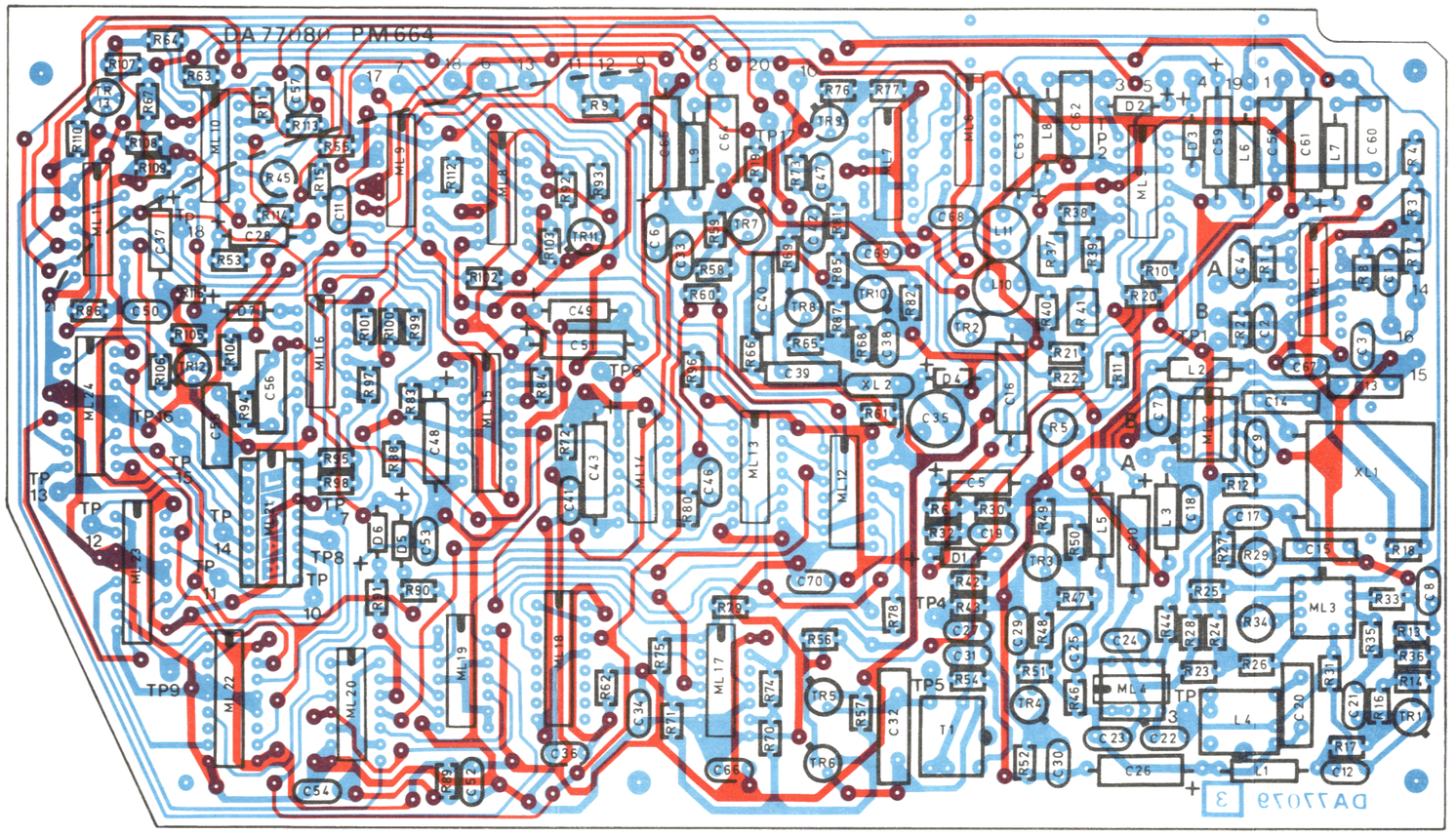
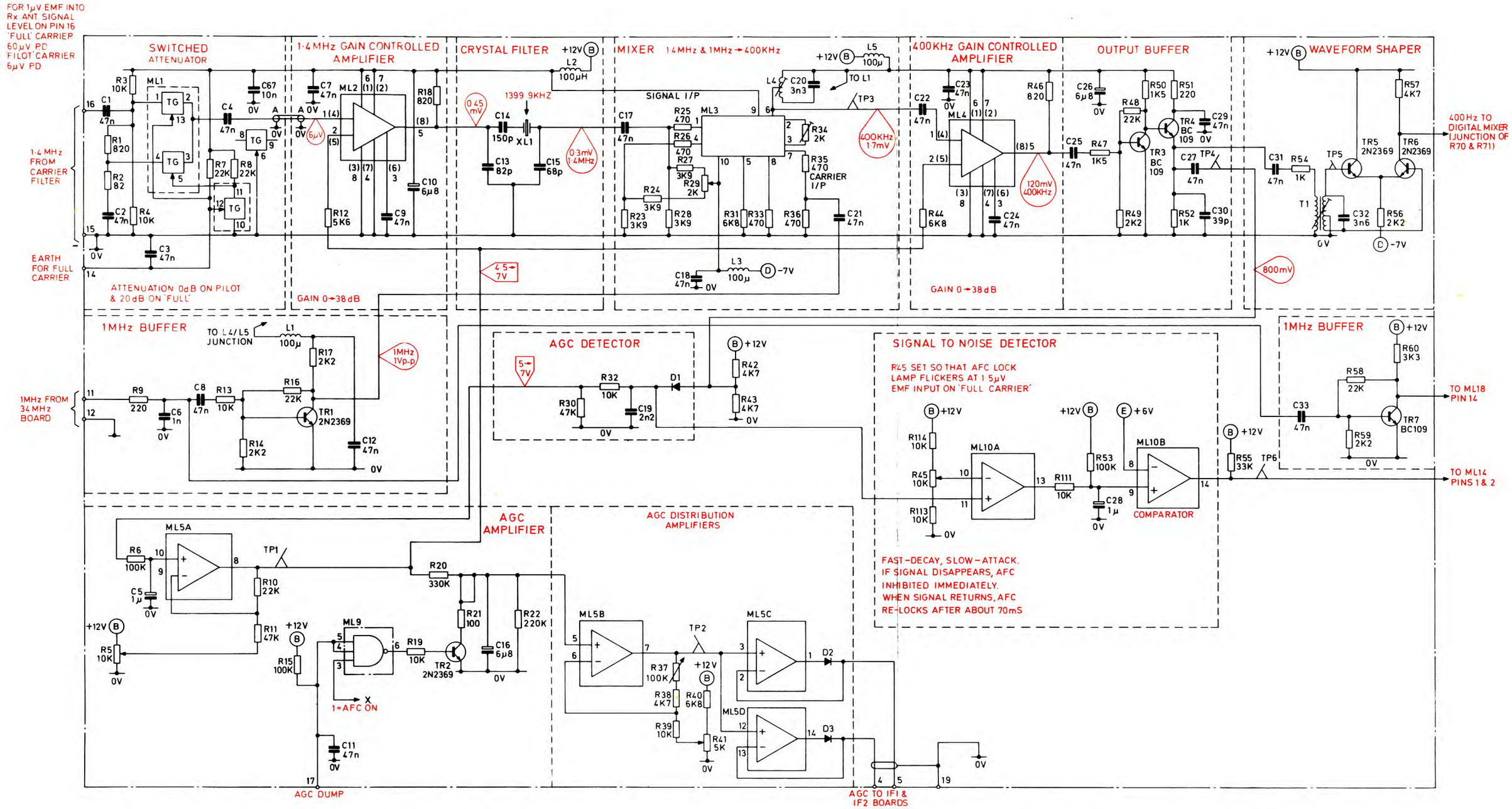


Fig. 2

A.F.C. board PM.664: layout

Fig. 2



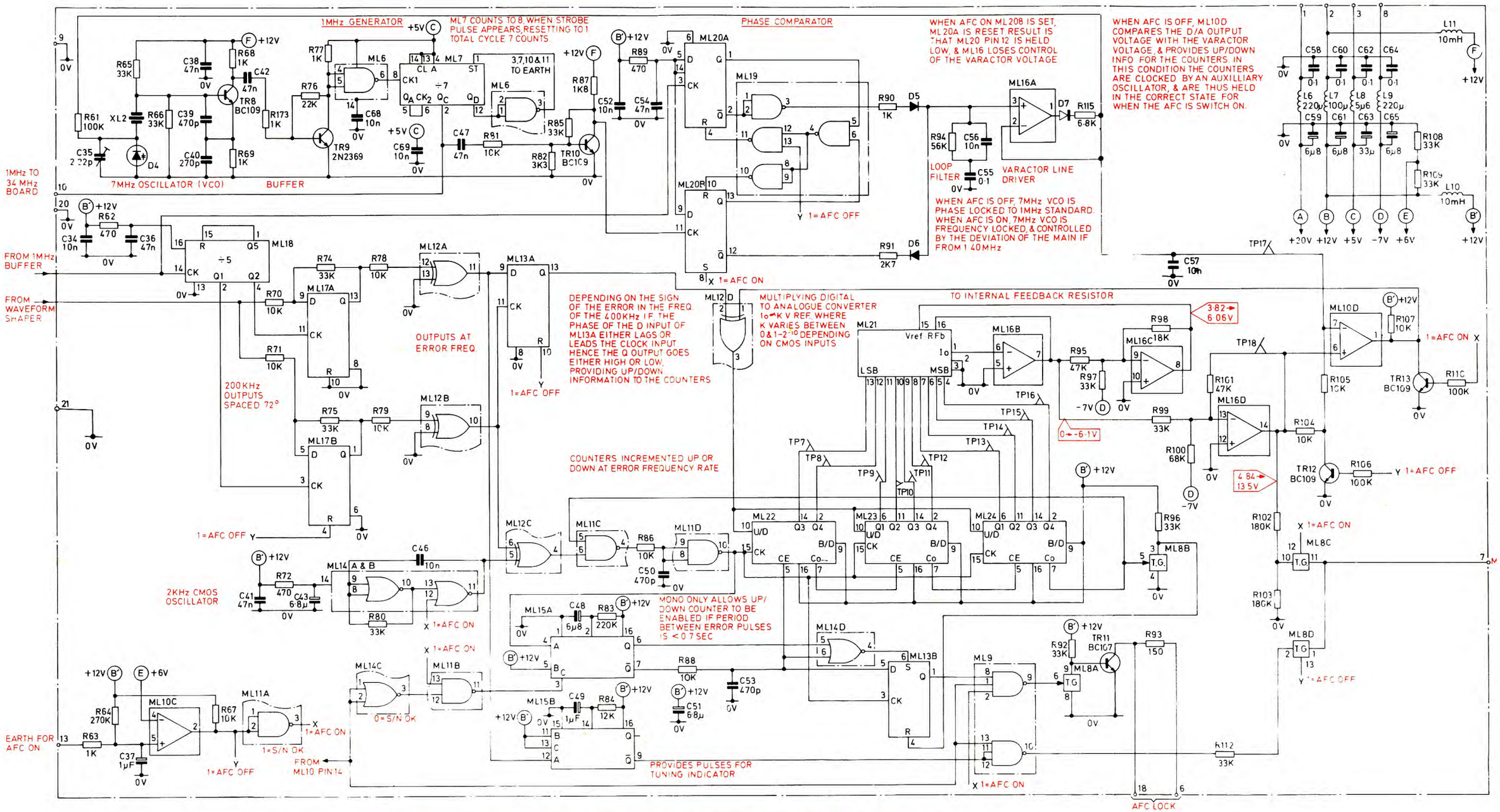
NOTE - ML2 & ML4

PIN NUMBERS IN BRACKETS APPLY WHEN D.I.L. ALTERNATIVES ARE USED (I.E. MC1350)

FIGURES SHOWN IN ◇ WERE MEASURED WITH AN AIRMEC 301A VALVE VOLTMETER (USING THE HIGH IMPEDANCE PROBE)

FIGURES SHOWN IN ◇ WERE MEASURED WITH AN AVO 8 (D.C. LEVEL)

Fig.3A A.F.C. board PM.664: circuit Fig.3A



PACKAGE	CD4066	MC1590G OR MC1350P	MC1596G	MC1590G OR MC1350P	LM324	7400J	74LS196J	CD4066	CD4023	LM239	CD4011	CD4070	CD4013	CD4001	MC14528	LM324	CD4013	CD4017	CD4011	CD4013	AD7520	CD4029	CD4029	CD4029
	ML1	ML2	ML3	ML4	ML5	ML6	ML7	ML8	ML9	ML10	ML11	ML12	ML13	ML14	ML15	ML16	ML17	ML18	ML19	ML20	ML21	ML22	ML23	ML24
+20V	–	–	–	–	–	–	–	–	–	3	–	–	–	–	–	4	–	–	–	–	–	–	–	–
+12V	14	6,7 (1,2)	6	6,7 (1,2)	4	–	–	14	14	–	14	14	14	14	5,11, 13,16	–	14	16	14	5, 9,14	14	9,16	9,16	9,16
+5V	–	–	–	–	–	14	4 13,14	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
0V	6,7 10	4,8 (3,7)	8	4,8 (3,7)	11	7	3,7 12,11	4,7 8	7	12	7	8,13 7	7,8	7	8,15 1	5,10 12	6,8, 10,7	8,13	7	7,6	2,3	3,4,8, 12,1,13	3,4,8 12,1,13	3,4,8 12,1,13
-7V	–	–	10	–	–	–	–	–	–	–	–	–	–	–	–	11	–	–	–	–	–	–	–	–
DE-COUPLED BY	C67	C7	–	C23	–	C68	C69	–	–	–	–	C70	–	R72, C41, C43	C51	–	C66	R62, C34, C36,	–	R89, C52, C54	–	–	–	–

NOTE – ML2 & ML4
PIN NUMBERS IN BRACKETS APPLY WHEN DIL ALTERNATIVES ARE USED (I E MC1350P)

A.F.C. board PM664: circuit

Fig.3B

Fig.3B

Chapter 2-1, Annex B

2nd MIXER BOARD PM336: ALTERNATIVE VERSION

CONTENTS

Para.
1 Introduction
2 Description

Fig. Page
1 2nd mixer board PM336 (alternative version): layout 3
2 2nd mixer board PM336 (alternative version): circuit ... 5

INTRODUCTION

1 This alternative board is introduced by modification number A7454.

DESCRIPTION

2 The modified board has a re-designed biassing arrangement for TR11, the affect of which is to reduce intermodulation products in the 1.4 MHz output. The modification details are as follows:

2.1 R27 changed from 1 kΩ to 560 Ω.

2.2 the addition of R28, R29, R30, CA4 and CA5.

3 When repairing this board, it should be noted that the physical location of the new components is critical.

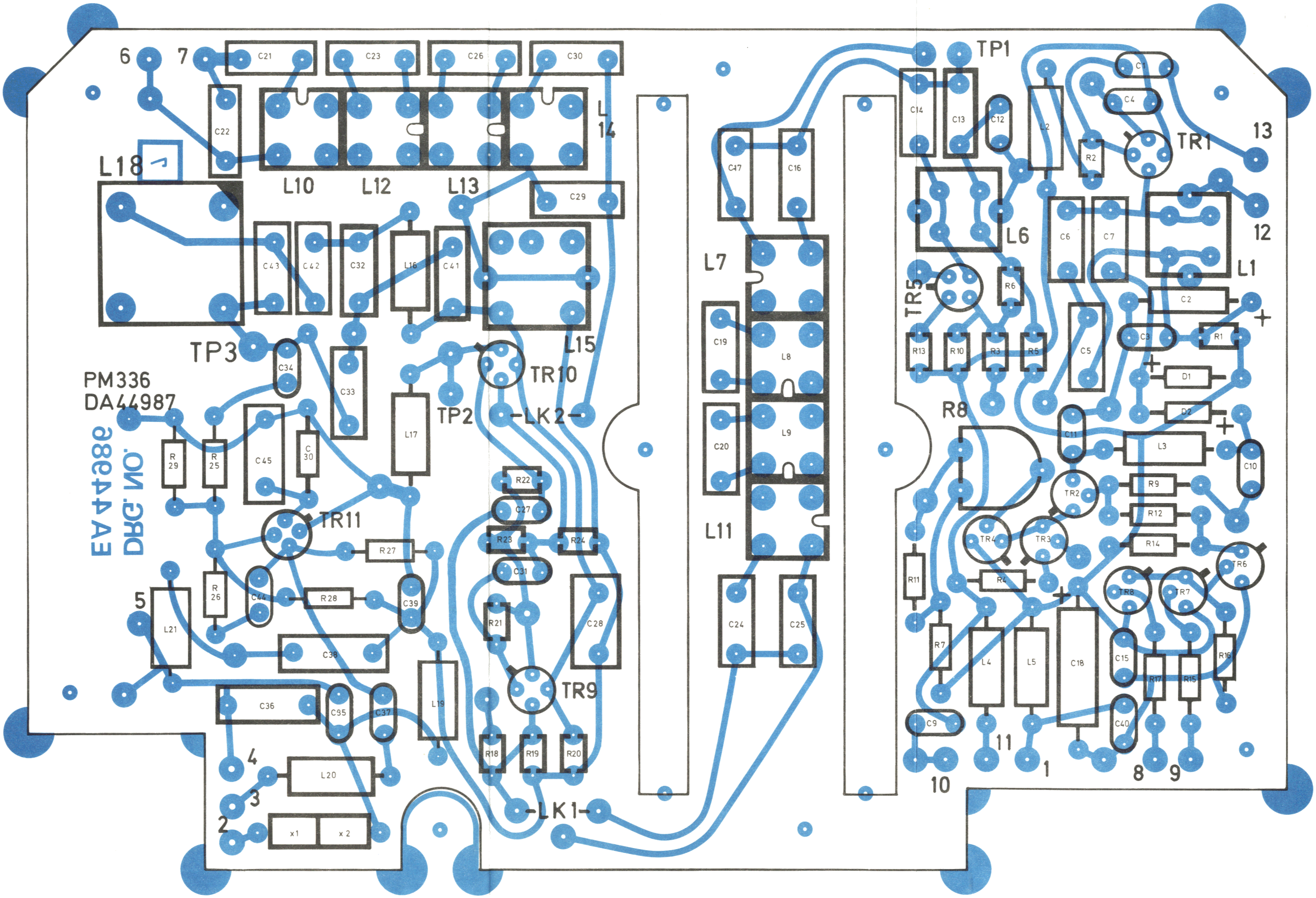
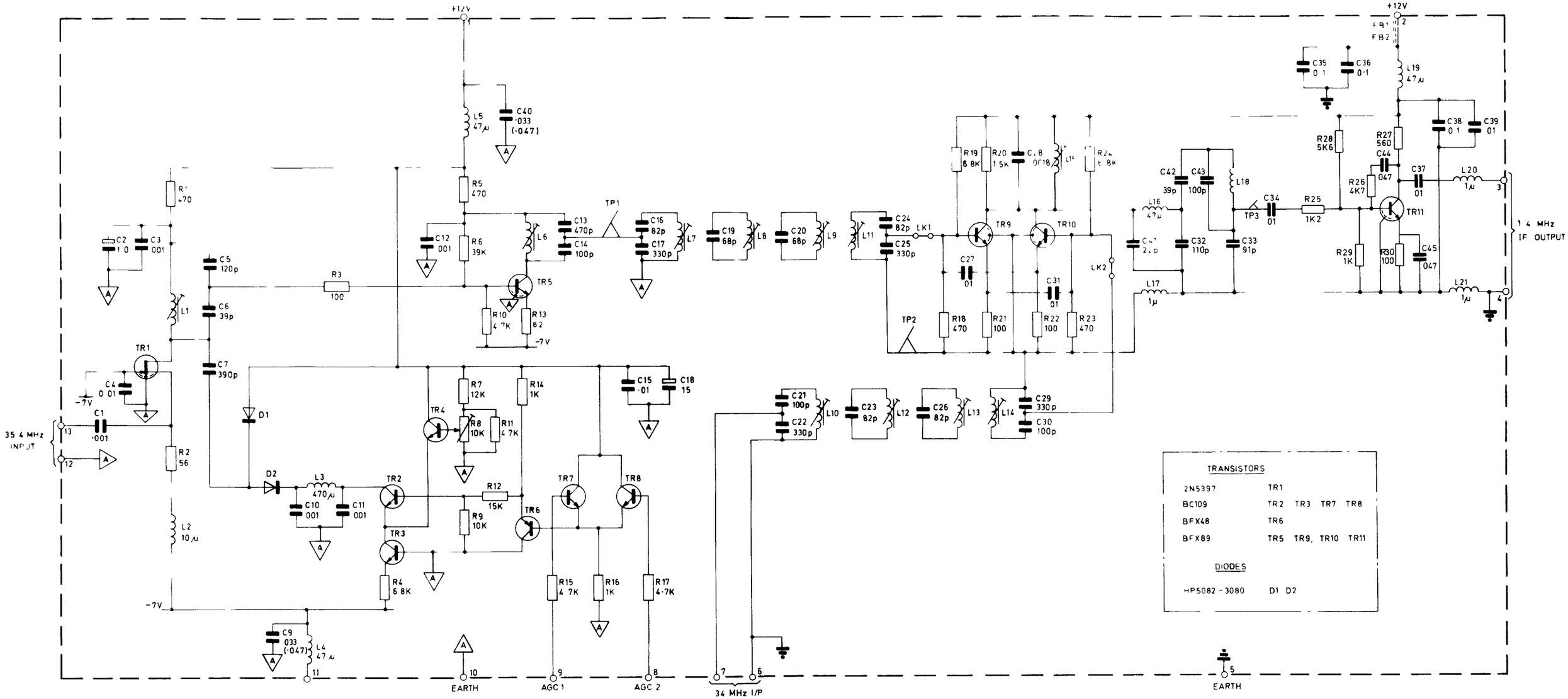


Fig.1

2nd mixer board PM336 (alternative version): layout

Fig. 1
Chap. 2-1, Annex. B
Page 3/4

Sept. 80 (Amdt. 6)



Second mixer board PM336 : circuit

Chapter 2-1 Annex D

OPTICAL SHAFT ENCODER: ALTERNATIVE VERSION

CONTENTS

Para

1 Introduction

2 Circuit description

7 Adjustments

10 Dismantling and reassembly

Fig. Page

1 Optical shaft encoder ST 77800 : board layout 3

2 Optical shaft encoder ST 77800 : circuit 5/6

INTRODUCTION

1 The optical shaft encoder referenced ST77800 is an alternative item to that described in Chap 2-1; it is fitted to selected receivers from serial number 1544 onwards.

CIRCUIT DESCRIPTION

2 The shaft encoder is an optical transducer of the incremental type. A graticule, of a transparent material with opaque strips, is attached to the encoder spindle and is made to rotate in the gaps between the LED light source and photo-transistors of a pair of optical switches (S1 and S2).

3 As the graticule rotates, the photo-transistors are alternately darkened and illuminated, thereby producing quasi-sinusoidal waveforms at pins 7 and 6 of the printed-circuit board.

4 The optical switches are physically displaced such that the two waveforms are 90 degrees out of phase, with output A leading output B for one direction of rotation and lagging output B for the reverse direction of rotation.

5 The sinewave outputs from S1 and S2 are converted into squarewave signals by the first two sections of ML1, and are then amplified to TTL levels by the other two sections of ML1. The voltage drop across the LED elements of S1 and S2 provides a fixed reference voltage for the amplifier stages. The unity mark/space ratios of the two squarewave outputs are set by means of R4 and R5.

6 The outputs from pins 2 and 1 of the printed-circuit board are applied to pins 31 and 32 respectively of the PM371 display board.

ADJUSTMENTS

7 The output waveforms are adjusted in the following manner:-

(1) Using a dual-trace oscilloscope, connect the Channel A probe to output pin 2 of the printed-circuit board.

(2) Connect the Channel B probe to output pin 1 of the board.

(3) Set the oscilloscope to display Channel A waveforms only.

(4) Check that the TUNING RATE switch is set to SLOW.

(5) Rotate the kHz tuning control in each direction in turn, and check that squarewave signals appear on the oscilloscope display. As necessary, adjust preset control R4 to obtain a unity mark/space ratio for the waveform.

(6) Set the oscilloscope to display Channel B waveforms only.

(7) Rotate the TUNE control, in each direction in turn, and check for squarewave signals on the display. As necessary, adjust preset control R5 to obtain a unity mark/space ratio for the waveform.

(8) Set the oscilloscope to display both channels, with the trigger signal provided by the Channel A waveform.

(9) Rotate the tune control in a counter-clockwise direction. Check that waveform A leads waveform B by 90 degrees.

(10) Rotate the tune control in a clockwise direction. Check that waveform A now lags waveform B by 90 degrees.

(11) Swtich OFF and disconnect the test equipment.

8 Further adjustment is not normally required. Should the phase displacement be other than 90 degrees, proceed as follows:-

(1) Obtain access to the shaft encoder and remove its cover.

(2) Slacken the screws securing the graticule carriage, and adjust the position of the carriage such that the 90 degree phase difference is obtained.

(3) Carefully re-tighten the screws whilst maintaining the desired phase difference.

(4) Refit the top cover and then refit the shaft encoder to the front panel assembly.

9 Mechanical damping is applied to the encoder shaft via a felt pad. The degree of damping is set by means of an adjuster screw.

DISMANTLING AND REASSEMBLY

10 To remove the shaft encoder proceed as follows:-

(1) Remove the kHz control knob.

(2) Lower the front panel and sub-panel together as one assembly.

(3) Remove the three screws securing the shaft encoder to the inside of the front sub-panel.

(4) Note the original positions and colour codes of any wires to be unsoldered.

11 The reassembly procedures are the reverse of those given for dismantling.

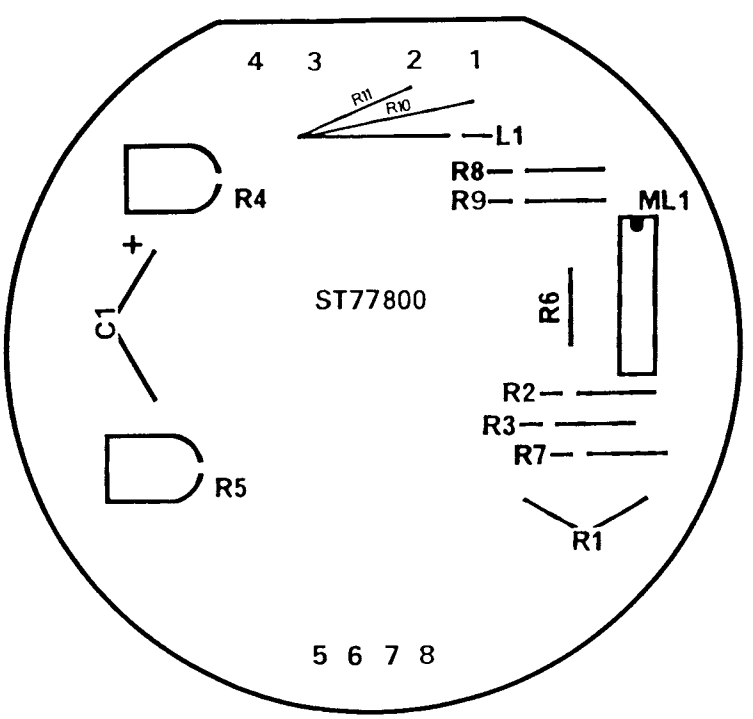


Fig 1 Optical shaft encoder ST77800: component layout

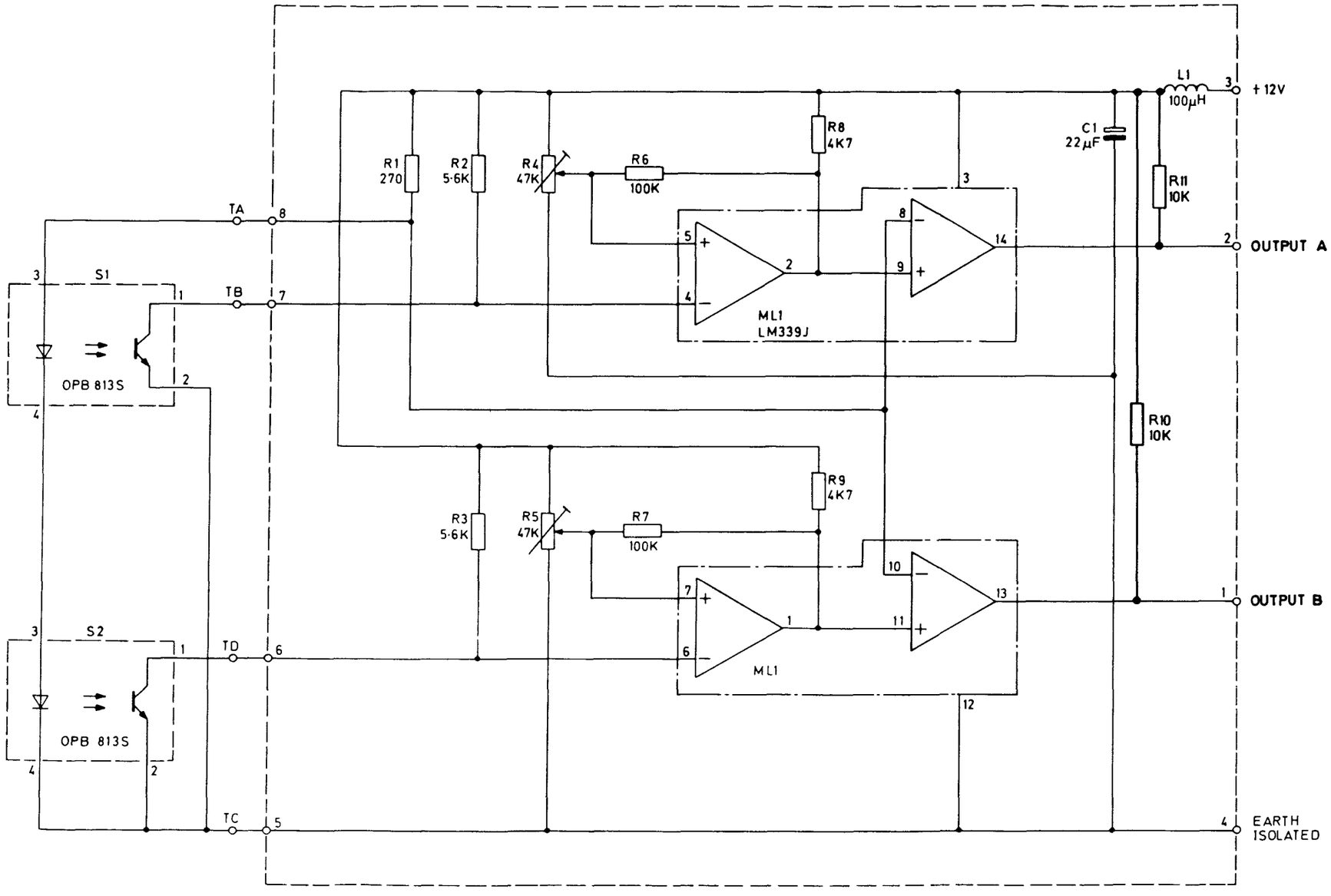


Fig 2

Optical shaft encoder ST77800 : circuit

Fig 2

Chapter 2-2

DISMANTLING AND RE-ASSEMBLY

CONTENTS

	Para.
Introduction	1
Initial procedure	2
R.F. board PM.582	3
Printed circuit boards - main compartment	5
Printed circuit boards - main chassis	6
Removal of front panel and front sub-panel	7
To lower front panel assembly	8
To remove front panel	9
Rear panel	11
Logic board PS.365	13
Alignment of MHz dial	15
Meter switching board PS.419	16
Display board PM.371	18
Power supply regulator board PM.370	20
A.F. and memory regulator board PS.427/1	22
Power transformer	24
Shaft-encoder	26
Cableform colour coding	28

TABLES

No.		Page
1	Cableform colour code : r.f. board PM.582	7
2	Cableform colour code : i.f. filter board PS.367	7
3	Cableform colour code : main i.f./a.f. board PM.364/1	9
4	Cableform colour code : i.s.b. i.f./a.f. board PM.364/3	12
5	Cableform colour code : l.f. loop board PM.588	14
6	Cableform colour code : upper loop board PM.589	15
7	Cableform colour code : 34 MHz generator board PM.339	17
8	Cableform colour code : transfer loop board PS.338	18
9	Cableform colour code : h.f. loop board PS337	19
10	Cableform colour code : first mixer board PM.335	20
11	Cableform colour code : second mixer board PM.336	20
12	Cableform colour code : logic board PS.365	21
13	Cableform colour code : meter switching board PS.419	22
14	Cableform colour code : display board PM.371	22
15	Cableform colour code : power supply regulator board PM.370	24
16	Cableform colour code : a.f. and memory regulator board PS427/1	26
17	Cableform colour code : power transformer	28
18	Cableform colour code : shaft encoder potentiometer board	28
19	Cableform colour code : a.f.c. board PM.369	29

ILLUSTRATIONS

Fig.		Page
1	Main transformer connections	27

INTRODUCTION

1. This chapter provides instructions for gaining access to the printed circuit boards, receiver sub-assemblies and chassis-mounted components. Should it be necessary to completely remove a printed circuit board, colour code tables for the cableform connections to each board are given. In general, the re-assembly is the reverse of the dismantling procedure.

INITIAL PROCEDURE

2. (1) Set the front panel POWER switch to OFF.

(2) Disconnect all the cable connectors at the rear of the receiver.

(3) Remove the two transit screws, if fitted, through the rear panel flange (fig.1 of Chap.1-3).

(4) Remove the four screws securing the receiver to the rack or table-top cabinet.

(5) Withdraw the receiver and place it on a flat clean working surface.

(6) Remove the receiver top cover plate, if fitted, which is held in place with Dzus fasteners.

R.F. BOARD PM.332

3. To gain access to the r.f. board, proceed as follows:

(1) Remove the top screening cover from the r.f. compartment.

(2) Locate the coupling on the RF TUNE control spindle and slacken the two screws. Withdraw the RF TUNE control spindle to disengage the coupling.

(3) Disconnect the coaxial r.f. input connector.

(4) Release the two bracket fixing screws within the r.f. compartment (left-hand side).

(5) The board may now be raised from the rear to hinge at the cableform (front) end. Once the board is vertical it may be held in position by sliding the nylon bush into the slot in the compartment side member.

4. To completely remove the r.f. board from the receiver, unsolder the cableform connections to the board pins. The cableform colour code for the board is given in Table 1.

PRINTED CIRCUIT BOARDS - MAIN COMPARTMENT

5. The compartment box structure mounted on the receiver chassis contains six printed circuit boards. After the top screening cover has been removed, each of these boards may be raised from the rear to hinge at the cableform (front) end. Once a board is vertical it may be held in position by sliding the nylon bush into the slot in the compartment side member. To completely remove any board unsolder the cableform connections to the board pins. The boards within this compartment are listed below, together with the Table number for the cableform colour-code and are identified on the top cover.

(1) I.F. filter board PS.367; Table 2

(2) Main i.f./a.f. board PM.364/1; Table 3

(3) I.S.B./I.F./A.F. board PM.364/3; Table 4

(4) L.F. loop board PM.588; Table 5

(5) Upper loop board PM.589; Table 6

(6) A.F.C. board PM.369; Table 19

PRINTED CIRCUIT BOARDS - MAIN CHASSIS

6. Five printed circuit boards are contained within compartments in the die-cast receiver chassis. To gain access to a board, remove the screening cover from the respective compartment. Each board may be lifted clear of the chassis by removing the securing screws and washers. To completely remove a board from the receiver, unsolder the cableform connections from the board pins. The boards contained within the chassis are listed below, together with the Table number for the cableform colour code.

(1) 34 MHz generator board PM.339; Table 7

(2) Transfer loop board PS.338; Table 8

(3) H.F. loop board PS.337; Table 9

(4) First mixer board PM.335; Table 10

(5) Second mixer board PM.336; Table 11

REMOVAL OF FRONT PANEL AND FRONT SUB-PANEL

7. The front panel together with the front sub-panel may be lowered as a complete assembly (para.8) to gain access to the front panel controls and associated compartments, the logic board, the meter switching board, the shaft-encoder and display board and the components mounted on the front top face of the die-cast chassis. Note that the receiver may be safely operated with the front panel assembly lowered.

To lower front panel assembly

8. (1) Remove the top screening cover from the r.f. compartment. Locate the coupling on the RF TUNE control spindle and slacken the two screws. Withdraw the RF TUNE control spindle to disengage the coupling.

(2) Slide the receiver forward such that the bottom edge of the front panel is clear of the working surface.

(3) Remove the six screws, each fitted with a nylon washer, securing the front panel to the receiver (three at each edge, adjacent to each handle).

(4) Support the front panel assembly and remove the two recessed screws, each with a spring washer, located one adjacent to each handle.

(5) The front panel assembly may now be lowered to 'hinge' on the connecting cableform.

To remove front panel

9. (1) Use the larger (1/16 in.) of the two socket wrenches provided (located in a clip attached to the right-hand side member) to remove all the front panel control knobs. Use the smaller socket wrench (1.5 mm) to remove the b.f.o. slow-motion dial.

(2) Disconnect the two wires to the front panel meter, using a 7 mm spanner. Replace the nuts and washers for safe keeping.

(3) Remove the eight screws, each fitted with a nylon washer, securing the front panel to the receiver (two in the centre of the front panel and three at each edge, adjacent to each handle).

(4) Lift off the front panel.

10. The front sub-panel may now be lowered by disconnecting the RF TUNE control spindle and removing the two screws, each with a spring washer, one at each edge of the sub-panel.

REAR PANEL

11. The rear panel may be lowered to 'hinge' on the connecting cableform. It is secured by seven screws, each with a spring washer, three at each side and one in the centre, below the transistors on the heat sink. Note that the receiver may be safely operated with the rear panel lowered.

12. It is necessary to lower the rear panel to gain access to the regulator board ► PM.370, the power supply smoothing capacitors 1C1a, 1C1b, 1C2a, 1C2b and 1C3 to 1C6 ◄ and resistors 1R9, 1R10. Two Zener diodes, D5 and D6, are mounted on the inside of the rear panel. To gain access to these diodes it is first necessary to remove the regulator board PM.370 (para.20).

LOGIC BOARD PS.365

13. To gain access to the logic board, it is necessary to lower the front panel and front sub-panel together as one assembly (para.8). Should it be necessary to completely remove the logic board from the receiver, proceed as follows:

14. (1) Remove the front panel (para.9).

(2) Remove the MHz dial.

(3) Lower the front sub-panel assembly (para.10).

(4) Unclip the three MHz lamp holders.

(5) Remove the four screws securing the MHz switch plate to the front sub-panel.

(6) Remove the two screws securing the logic board spacing pillars to the front sub-panel.

(7) The logic board, together with the MHz switch, may now be lifted clear. To completely remove the logic board from the receiver, unsolder the cableform connecting wires to the board pins and also the green/black wire connected to the wiper of switch wafer SA3. The cableform colour code for the logic board is given in Table 12.

Alignment of the MHz dial

15. When the MHz switch is set to 0 MHz, the switch wipers are almost in line with but slightly to the right of the top spacing pillars (viewed from the front of the receiver). With the switch in this position, the 0 MHz digit on the MHz dial should be in line with the centre of the three MHz lamps.

METER SWITCHING BOARD PS.419

16. To gain access to the meter switching board it is necessary to lower the front panel and front sub-panel together as one assembly (para.8). To completely remove the meter switching board and switch, proceed as follows.

17. (1) Remove the front panel (para. 9).

(2) Lower the front sub-panel (para. 10).

(3) Remove the nut and washer securing the meter switch to the front sub-panel.

(4) Withdraw the meter switching board and switch.

(5) Unsolder the cableform connections to the board pins. The cableform colour code for the meter switching board is given in Table 13.

DISPLAY BOARD PM.371

18. To gain access to the display board, lower the front panel and front sub-panel as one assembly (para. 8). To completely remove the display board from the receiver, proceed as follows.

19. (1) Unsolder the cableform connecting wires to the board pins. The cableform colour code for the display board is given in Table 14.

(2) Remove five nuts, each with a spring washer, securing the board to the inside of the front sub-panel.

(3) Lift out the board.

POWER SUPPLY REGULATOR BOARD PM.370

20. To gain access to the regulator board, lower the rear panel (para. 11). To completely remove the regulator board from the receiver proceed as follows.

21. (1) Unsolder the cableform connections to the board pins. The cableform colour code for the regulator board is given in Table 15.

(2) Remove the four screws, each with a flat and a spring washer, securing the board to the inside of the rear panel.

(3) Lift out the board.

A.F. and MEMORY REGULATOR BOARD PS.427/1

22. To gain access to the a.f. and memory regulator board, remove the sub-panel assembly containing the frequency module. This assembly is secured to the cast chassis with four screws, each with a spring washer. To completely remove the board, proceed as follows.

23. (1) Unsolder the cableform connections to the board pins. The cableform colour code for the AF and memory regulator board is given in Table 16.

(2) Remove the four securing screws, each with a spring washer.

(3) Lift out the board.

POWER TRANSFORMER

24. To gain access to the connections to the power transformer and the supply input filter components, proceed as follows:

(1) Lower the rear panel (para.11).

(2) Remove the four screws securing the transformer connection cover plate.

(3) Remove the cover plate.

25. To completely remove the power transformer from the receiver, proceed as follows:

(1) Unsolder the cableform connections to the transformer. The cableform colour code for the transformer is given in Table 17.

(2) Turn the receiver onto its side (left-hand as viewed from the rear panel).

(3) Remove the screening cover from the chassis compartment containing the 34 MHz board.

(4) Remove the nine screws, each with a spring washer, securing the 34 MHz board.

(5) Hinge out the 34 MHz board on its cableform to reveal the four transformer securing screws.

(6) Support the transformer and remove the four securing screws.

SHAFT-ENCODER

26. To remove the shaft-encoder proceed as follows:

(1) Remove the kHz control knob.

(2) Lower the front panel and front sub-panel together as one assembly (para. 8).

(3) Remove the three screws securing the shaft-encoder lugs to the inside of the front sub-panel.

(4) To remove the shaft-encoder completely, disconnect the wires from the potentiometer board at the rear of the shaft-encoder.

(5) The cableform colour code for the potentiometer board is given in Table 18.

27. To gain access to the sensor board and the graticule carriage, proceed as follows:

(1) Remove the black tape from the outer cover.

(2) Locate the opening in the outer cover. Spring out the cover and slide off.

(3) The graticule carriage is secured by two screws through the front flange plate. Do not release these screws unless it is absolutely necessary. To do so may upset the 90 degree phase relationship between the two output signals from the shaft-encoder.

CABLEFORM COLOUR CODING

28. Wire colours given in the following tables are intended as a guide only. Colours may occasionally differ from those given and in such cases it is recommended that the user amends the respective Tables accordingly.

TABLE 1

Cableform colour code : r.f. board PM.582

Board pin no.	Colour	Function
1	Orange	+12V
2	Black	0V (earth)
3	White/grey	Mute
4	White/red/blue	MHz select
5	Blue/grey	2-3 MHz select
6	Orange/black	1 MHz select
7	Orange/white	16-29 MHz select
8	Brown/red/violet	8-15 MHz select
9	White/red/grey	4-7 MHz select
10	Two orange	+12V
11	Black and screen for 12	0V (earth)
12	Coaxial	R.F. out
13	Blue/green	Wideband select
14	Violet	-7V

TABLE 2

Cableform colour code : i.f. filter board PS.367

Board pin no.	Colour		Function
1	Orange		+12V
2	Coaxial		U.S.B./A.M. output
3	Screen		
4	Coaxial		L.S.B.(I.S.B.) output
5	Screen		
6	Coaxial	yellow/black sleeves	Carrier output
7	Screen		
8	Red/blue/orange		Not used
9	Grey/orange		L.S.B. filter select
10	Red/green/white		0.8-1.2 kHz filter select
11	Red/green/grey		0.4-1.6 kHz filter select
12	Grey/blue/white		8 kHz filter select

TABLE 2 (cont.)

BOARD PIN NO.	COLOUR		FUNCTION
13	Screen	Red/blue sleeves	1.4 MHz i.f input
14	Coaxial		
15	White/black		U.S.B. filter select
16		BTC wire links	Carrier filter
17			
18			
19		BTC wire links	For i.s.b.(l.s.b.) output
20			
21			
22		BTC wire links	Carrier filter
23			
24			
25	Black		OV (earth)

TABLE 3

Cableform colour code : main i.f./a.f. board PM.364/1

Board pin no.	Colour		Function
1	Red/blue/orange		I.F. gain control
2	Two coaxial	Red/violet & brown/brown sleeves	I.F. output
3	Two coaxial screens		
4	Screen for pin 24		
5	Coaxial	Red/red sleeves	
6	Two red/black		S.S.B. select
7	Blue/green		A.M. select
8	Red	2-core screened	Audio pre-amplifier output
9	Two screens		Earth
10	Two grey/white		Not used
11	Blue		Line amplifier input
12	No connection		
13	Three orange		+12V
14	Red/blue		+14.5V
15	Blue	2-core screened violet sleeve	Audio line output
	Blue	2-core screened orange/violet sleeves	
16	Red		
	Red		
17	Two screens		Earth

TABLE 3 (cont.)

Board pin no.	Colour		Function
18	Red	2-core screened blue sleeve	Audio output to loudspeaker
	Red	2-core screened orange/red sleeves	
19	Blue		
	Blue		
	Two screens		
20	Violet		-7V
21	Violet with brown sleeve		-7V
22	Screen	Single core screened green/violet sleeves	Input to loudspeaker amplifier
23	Red		
24	Red	Single core screened green/orange sleeves, screen pin 4	A.G.C. hang
25	Red	2-core screened yellow/yellow sleeves	A.G.C. short select
26	Blue		A.G.C. long select
27	Red	Single core screened red/white sleeves	A.G.C. input (a.f.c. board)
28	Screen	2-core screened yellow sleeve	Earth
29	Red	Single core screened red/green sleeves	A.G.C. output
	Blue	2-core screened yellow/green sleeves	
30	Red		A.G.C. input
	Red		
31	Black		Earth
32	Screen		Earth
33	Blue		Special a.g.c. input

TABLE 3 (cont.)

Board pin no.	Colour	Function
34	Coaxial	1.4MHz i.f. input
35	Screen	Earth
	Screen	
36	Two screens	Earth

TABLE 4

Cableform colour code : i.s.b. i.f./a.f. board PM.364/3

Board pin no.	Colour		Function
1	No connection		
2	Coaxial	Brown/black sleeves	I.F. output
3	Screen		
4	Screen for pin 24		Earth
5	Coaxial	Red/red sleeves	1.4MHz injection input
6	Red/black		S.S.B. select
7	No connection		
8	Red	2-core screened	Audio pre-amplifier output
9	Two screens		Earth
10	Grey/white		Not used
11	Blue		Line amplifier input
12	No connection		
13	Orange		+12V
14	Red/blue		+14.5V
15	Blue	2-core screened grey sleeve	Audio line output
	Blue	2-core screened orange/grey sleeves	
16	Red		
	Red		
17	Two screens		Earth
18	No connection		
19	No connection		

TABLE 4 (cont.)

Board pin no.	Colour	Function
20	No connection	
21	Violet	-7V
22	No connection	
23	No connection	
24	Red single core screened green/yellow sleeves, screen pin 4	A.G.C. hang
25	Red ← 2-core screened yellow/violet sleeves	A.G.C. short select
26	Blue ←	A.G.C. long select
27	No connection	
28	Screen ← 2-core screened yellow sleeve	Earth
29	Blue ← 2-core screened yellow/grey sleeves	A.G.C. output
30	Blue ←	A.G.C. input
	Red ←	
31	Black	Earth
32	No connection	
33	Red ←	Special a.g.c. input
34	Coaxial ←	1.4MHz i.f. input
35	Two screens ←	Earth
36	Screen ←	Earth

TABLE 5

Cableform colour code : l.f. loop board PM.588

Board pin no.	Colour	Function
1	Green/black	Lock indication output 1
2	Orange/black	1 kHz data 'C' line
3	No connection	
4	Orange/red	1 kHz data 'A' line
5	No connection	
6	Grey/brown	1 kHz data 'B' line
7	No connection	
8	Grey/red	1 kHz data 'D' line
9	No connection	
10	Red/black	100 kHz data 'C' line
11	No connection	
12	Red/brown	100 kHz data 'A' line
13	No connection	
14	White/black	100 Hz data 'B' line
15	No connection	
16	White/green	100 Hz data 'D' line
17	No connection	
18	White/red	10 Hz data 'C' line
19	No connection	
20	White/green	10 Hz data 'A' line
21	No connection	
22	Green/brown	10 Hz data 'B' line
23	No connection	
24	Green/red	10 Hz data 'D' line
25	No connection	
26	Two violet	-7V
27	Two brown	+5V
28	Red/blue/orange	10 kHz data 'C' line
29	Red/blue/green	10 kHz data 'A' line
30	White/red/grey	10 kHz data 'B' line
31	White/blue/brown	10 kHz data 'D' line
32	White/blue /red	100 kHz data 'C' line
33	White/blue/grey	100 kHz data 'A' line
34	White/blue/green	100 kHz data 'B' line

TABLE 5 (cont.)

Board pin no.	Colour	Function
35	Red/brown orange	100 kHz data 'D' line
36	Blue	Overspill data lines
37	White	
38	Two red	+20V
39	Two black	0V (earth)
40	Screen for 41	0V (earth)
41	Coaxial green/black sleeves	Varactor line output
42	Orange/green	Lock indication output 2
43	Screen for 44	Earth
44	Coaxial green/red sleeves	Input from transfer oscillator
45	Two screens for 46	Earth
46	Two coaxials red/orange & orange/white sleeves	1 MHz input
47	No connection	
48	Two red	+20V
49	No connection	
50	Black	0V (earth)

TABLE 6

Cableform colour code : upper loop board PM. 589

Board pin no.	Colour		Function
1	Screen	Brown/blue sleeves	4.6 - 3.6 MHz output
2	Coaxial		
3	Black		0V (earth)
4	Two red		+20V
5	Two brown		+5V
6	Three violet		-7V
7	Coaxial	Green/black sleeves	Varactor line input
8	Screen		
9	Coaxial	Green/red sleeves	Transfer oscillator output
10	Screen		
11	Grey		Range blanking input
12	Red/orange/white		Lock indication output

TABLE 6 (cont.)

Board pin no.	Colour	Function
13	Green/black	Lock indication inputs from PM.588
14	Green/orange	
15	No connection	
16	Two white	Overspill data 'D' line
17	No connection	
18	No connection	
19	Two blue	Overspill data 'A' line
20	No connection	
21	No connection	
22	Two brown/red/orange	100 kHz data 'D' line
23	No connection	
24	No connection	
25	Two white/blue/green	100 kHz data 'B' line
26	No connection	
27	No connection	
28	Two white/blue/grey	100 kHz data 'A' line
29	No connection	
30	No connection	
31	Two white/blue/red	100 kHz data 'C' line
32	No connection	
33	No connection	
34	Two white/blue/brown	10 kHz data 'D' line
35	No connection	
36	No connection	
37	Two white/red/grey	10 kHz data 'B' line
38	No connection	
39	No connection	
40	Two red/blue/green	10 kHz data 'A' line
41	No connection	
42	No connection	
43	Two red/blue/orange	10 kHz data 'C' line
44	No connection	
45	Black	0V (earth)

TABLE 7

Cableform colour code : 34 MHz generator board PM.339

Board pin no.	Colour	Function
1	Brown	+5V
2	Red	+20V
3	Screen ← No sleeves	0V (earth)
4	Coaxial ← White sleeves	1 MHz input
5	Screen ← Red/orange sleeves	0V (earth)
6	Coaxial ←	1 MHz output
7	Screen ←	0V (earth)
8	Coaxial ←	1 MHz output
9	Two orange, one with green sleeve	+12V
10	Coaxial red/red sleeves, screen pin 31	1.4 MHz output (u.s.b./a.m.)
11	Coaxial red/brown sleeves, screen pin 32	1.4 MHz output (l.s.b.)
12	Blue/white	Slave earth
13	No connection	Crystal earth
14	Orange/green	B.F.O. earth
15	Brown/blue	1.4 MHz earth
16	Orange/brown	1 MHz earth
17	No connection	
18	Coaxial red/black sleeves, screen pin 33	A.F.C. 1 MHz
19	Brown/red/green	A.F.C. earth
20	Coaxial ← No sleeves	34 MHz output
21	Two screens ←	0V (earth)
22	Coaxial ← No sleeves	34 MHz output
23	White/brown/blue	B.F.O. control
24	Orange/black	
25	Green/brown	
26	Screen — Red/yellow sleeves	5 MHz input
27	Coaxial — Red/yellow sleeves	
28	Two brown, one with white sleeve	+5V
29	Two orange, one with green sleeve	+12V
30	Orange	+12V
31	Screen for pin 10	0V (earth)
32	Screen for pin 11	0V (earth)

TABLE 7 (cont.)

Board pin no.	Colour	Function
33	Screen for pin 18	OV (earth)
34	Black	OV (earth)

TABLE 8

Cableform colour code : transfer loop board PS.338

Board pin no.	Colour		Function
1	No connection		
2	Two red, one with white sleeve		+20V
3	Two brown, one with white sleeve		+5V
4	Coaxial	Brown/violet sleeves	Varactor
5	Screen		Line cutput
6	White/red/green		Lock indication output
7	Two violet		-7V
8	Two blue/red/green		MHz data 'D' line (tens)
9	Two blue/white/brown		MHz data 'C' line (tens)
10	Two blue/white/green		MHz data 'B' line (tens)
11	Two red/orange/grey		MHz data 'A' line (tens)
12	Two white/red/orange		MHz data 'D' line (units)
13	Two white/red/brown		MHz data 'C' line (units)
14	Two red/grey/blue		MHz data 'B' line (units)
15	Two red/grey/green		MHz data 'A' line (units)
16	Screen	Brown/blue sleeves	4.6 - 3.6 MHz input
17	Coaxial		
18	Screen	Brown/grey sleeves	Input from transfer loop oscillator
19	Coaxial		
20	Screen	No sleeves	1 MHz input
21	Coaxial		

TABLE 9

Cableform colour code : h.f. loop board PS.337

Board pin no.	Colour		Function
1	Grey/red/green		MHz data 'A' line (units)
2	Grey/red/blue		MHz data 'B' line (units)
3	Brown/red/white		MHz data 'C' line (units)
4	Orange/red/white		MHz data 'D' line (units)
5	Orange/red/grey		MHz data 'A' line (tens)
6	Blue/green/white		MHz data 'B' line (tens)
7	Blue/brown/white		MHz data 'C' line (tens)
8	Red/green/blue		MHz data 'D' line (tens)
9	Brown		+5V
10	Orange		+12V
11	Red		+20V
12	Brown/violet/red with two ferrite beads (FB2, FB3)		Lock indication output
13	Coaxial	Brown/grey sleeves	Transfer loop oscillator output
14	Screen		
15	No connection		
16	Violet with single ferrite bead (FB1)		-7V
17	Screen	Brown/violet sleeves	Varactor line input
18	Coaxial		
19,20	No connections		
21	Screen	No sleeves	Local oscillator output
22	Coaxial		
23	Screen	Brown/white sleeves	Local oscillator input/output socket
24	Coaxial		
25	Red/blue		L.O. int/ext switch
26	White		Oscillator 1 select
27	Grey		Oscillator 2 select
28	Blue		Oscillator 3 select

TABLE 10

Cableform colour code : first mixer board PM.335

Board pin no.	Colour		Function
1	Orange		+12V
2	Screen	No sleeves	35.4 MHz i.f. output
3	Coaxial		
4	No connection		
5	Red/orange/green		Output to meter
6	No connection		
7	Violet		-7V
8	White/blue		4 - 29 MHz select
9	Screen	No sleeves	Local oscillator input
10	Coaxial		
11	Orange/brown		C - 3 MHz select
12-18	No external connections		
19	Coaxial	No sleeves	R.F. input
20	Screen		

TABLE 11

Cableform colour code : second mixer board PM.336

Board pin no.	Colour		Function
1	Orange		+12V
2	Orange		+12V
3	Green		Output
4	Black		Earth
5	No connection		
6	Screen	No sleeves	34 MHz input
7	Coaxial		
8	White/blue		A.G.C.2
9	Orange/red		A.G.C.1
10	Black		Earth
11	Violet		-7V
12	Screen	No sleeves	35.4 MHz i.f. input
13	Coaxial		

TABLE 12

Cableform colour code : logic board PS.365

Board pin no.	Colour	Function
1	Brown	+5V
2	White/black	D.F.2 output
3	Orange/brown	D.F.1 output
4	Blue	01 output
5	White	03 output
6	Grey	02 output
7	Brown/white Grey/green/red	A1 output
8	Grey/blue/red	B1 output
9	White/brown/red	C1 output
10	White/orange/red	D1 output
11	Orange/violet/red	A2 output
12	White/green/blue	B2 output
13	White/brown/blue	C2 output
14	Green/blue/red	D2 output
15	Black	0V earth
16-25	No external connections	
26	White/orange	RANGE SELECTION OUTPUTS
27	Brown/red/blue	
28	Red/grey/white	
29	Grey/blue	
30	Orange/black	
31	White/red/blue	
32	Blue/green	R.F. microswitch
Wiper SA3	Green/black	L.O. int/ext switch

TABLE 13

Cableform colour code : meter switching board PS.419

Board pin no.	Colour	Function
1	Red ← 2-core screened orange/ blue sleeves	I.S.B. div a.g.c.
2	Two black, one with brown sleeve	0V (earth)
3	Orange	+12V
4	Blue ←	Div a.g.c.
5	Screen ←	0V (earth)
6	Brown	+5V
7	Red	Meter +
8	Screen ← single core screened	Not used
9	Red ← orange/black sleeves	
10	Red	+20V
11	Blue ← 2-core screened	Audio line output i.s.b. i.f.
12	Red ← orange/grey sleeves	
13	Screen ←	
14	No connection	
15	Red ← 2-core screened	Audio line output main i.f.
16	Blue ← orange/violet sleeves	
17	Screen ←	
18	No connection	
19	Orange/green	L.O. drive
20	No connection	
21	Black	Meter -
22	No connection	
23	Grey/red	Tuning indication
24	No connection	
25	Violet	-7V
26	No connection	
27	No connection	

TABLE 14

Cableform colour code : display board PM.371

Board pin no.	Colour	Function
1	White/green	10 Hz data 'A' line

TABLE 14 (cont.)

Board pin no.	Colour	Function
2	Brown/green	10 Hz data 'B' line
3	Brown/white	10 Hz data 'C' line
4	Green/red	10 Hz data 'D' line
5	Brown/red	100 Hz data 'A' line
6	Black/white	100 Hz data 'B' line
7	Black/red	100 Hz data 'C' line
8	White/grey	100 Hz data 'D' line
9	Orange/red	1 kHz data 'A' line
10	Grey/brown	1 kHz 'B' line
11	Orange/black	1 kHz data 'C' line
12	Grey/red	1 kHz data 'D' line
13	Red/blue/green	10 kHz data 'A' line
14	Red/grey/white	10 kHz data 'B' line
15	Red/blue/orange	10 kHz data 'C' line
16	White/blue/brown	10 kHz data 'D' line
17	White/blue/grey	100 kHz data 'A' line
18	White/blue/green	100 kHz data 'B' line
19	White/blue/red	100 kHz data 'C' line
20	Orange/brown/red	100 kHz data 'D' line
21	Blue	Overspill data 'A' line
22	White	Overspill data 'D' line
23	Orange/brown	Memory +5V supply
24	Grey/green	'L' MHz lamp
25	Orange/brown	'N' MHz lamp
26	Green/black	'H' MHz lamp
27	Grey	Range blanking
28	Brown/white	MHz units
29	Blue/green	Tuning fast
30	Green/orange	Tuning lock
31	Orange/blue	Encoder 'B'
32	Grey/orange	Encoder 'A'
33	Orange/red/white	Lock lines
34	Brown/red/violet	
35	White/red/green	
36	Green	Out-of-lock lamp

TABLE 14 (cont.)

Board pin no.	Colour	Function
37	Two black	0V (earth)
38	No connection	
39	Three brown	+5V
40	Black	L.O. switch

TABLE 15

Cableform colour code : regulator board PM.370

Board pin no.	Colour	Function
1	White/brown	1TR1 collector
2	Green/white	1TR1 base
3	Black	0V (earth)
4	Blue/white	1TR1 emitter
5	Violet with brown sleeve	-7V output
	Blue ← 2-core screened brown/green sleeves	
6	Two violet	
7	No connection	
8	White/grey	1TR2 collector
9	Green/brown	1TR2 base
10	Two brown one with white sleeve	+5V output
11	No connection	
12	Three brown	+5V output
13	Blue/green	1TR2 emitter
14	White/orange	1TR3 collector
15	Orange/green	1TR3 base
16	Red ← (Screen not connected)	+12V output
	Two orange, one with green sleeve	
17	Two orange	
18	Orange with brown sleeve	
19	Blue/orange	1TR3 emitter
20	Orange/red	+12V oven supply
21	Grey/orange	Standby +12V input
22	Two red	+20V output
23	Red with white sleeve	

TABLE 15 (cont.)

Board pin no.	Colour	Function
24	Black	0V (earth)
25	Red ← 2-core screened brown sleeve	Not used
26	Blue ←	
27	Screen ←	
28	Brown/blue	
29	Green	
30	Orange/brown	
31	Green/brown	
32	White/grey	
33	White/grey	
34	Grey/orange	
35	Blue/green	Connections to 1C4
36	Red/orange	
37	Grey/brown	23V a.c. winding 1T1
38	White/orange	
39	No connection	
40	No connection	
41	Orange/brown	16.5V a.c. winding 1T1
42	Grey/red	
43	No connection	
44	No connection	
45	Blue/grey	10V a.c. winding 1T1
46	Red/brown	
47	Blue/white	Connections to 1C1
48	Black/white	
49	Brown/blue	10.5V a.c. winding 1T1
50	Grey/orange	
D2-	Orange/blue	← Connections to 1C2
D2+	Grey/brown	Unregulated 14V supply
	Red/black	←
D3-	Two brown/white	Connections to 1C3 and
D3+	Two red/white	Unregulated 23V output

TABLE 16

Cableform colour code : a.f. and memory regulator board PS.427/1

Board pin no.	Colour	Function
1	Red/black	Connections to ML2
2	Red/orange	
3	Red/brown	
4	Red/white	Unregulated 23V supply
5	Brown/white	
6	Two red/blue	+14.5V output
7	Black	0V (earth)
8	Orange/red	+12V oven supply
9	Grey/brown	Unregulated 14V supply
10	Orange/brown	Memory +5V output
11	Orange/blue	Connections to ML3
12	Orange/brown	
13	Orange/green	

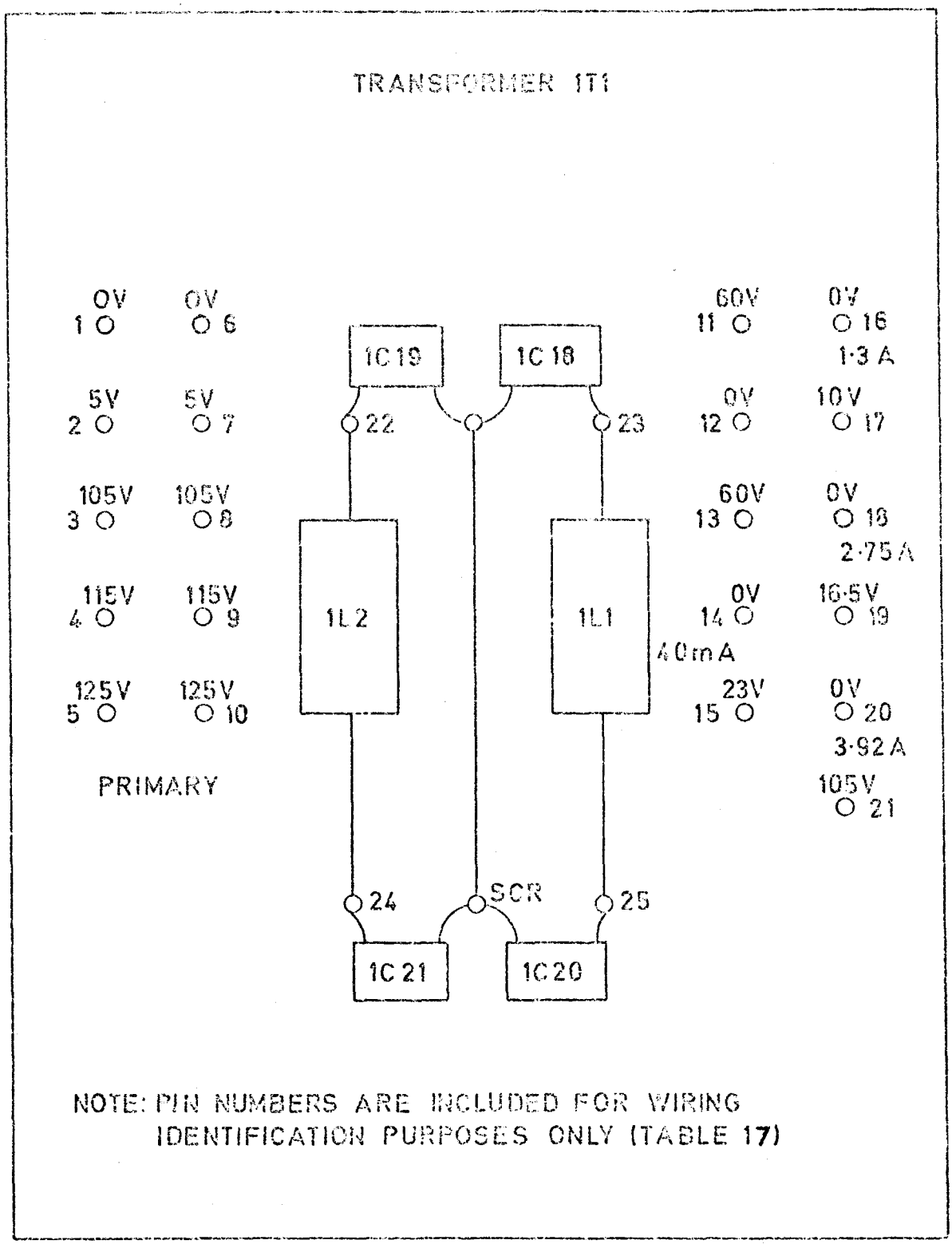


Fig.1 Main transformer connections

TABLE 17

Cableform colour code : power transformer (fig. 1)

Board pin no.	Colour		Function
1	White/blue		Primary connections
2	Orange/green		
3	Orange/blue		
4	Red/black		
5	Red/orange		
6	Creen/white		
7	White/brown		
8	Blue/green		
9	Black/white		
10	Red/white		
11	White/grey		Not used
12	Green		
13	White/grey		
14	Grey/brown		23V secondary
15	White/orange		
16	Brown/blue		10V secondary
17	Grey/orange		
18	Orange/brown		16.5V secondary
19	Grey/red		
20	Grey/blue		10.5V secondary
21	Red/brown		
22	Red	Twisted pair	A.C. supply in
23	Blue		
24	Red	Twisted pair	A.C. supply out
25	Blue		

TABLE 18

Cableform colour code : shaft encoder potentiometer board

Board pin no.	Colour	Function
1	B.T.C. - P.T.F.E. sleeve	Sensor output B
2		Earth
3	B.T.C. - P.T.F.E. sleeve	Sensor output A
4	Grey/orange	Output A

TABLE 18 (cont.)

Board pin no.	Colour	Function
5	Black	Earth
6	2 orange	+12V
7	Orange	
8	Orange	
9	Orange	
10	Orange/blue	Output B

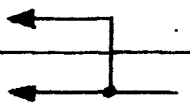
TABLE 19

Cableform colour code : a.f.c. board PM.369

Board pin no.	Colour	Function
1	Red	+20V
2	Two orange, one with green sleeve	+12V
3	Brown	+5V
4	Red ← green/green sleeve	U.S.B. a.g.c. output
5	Blue ←	L.S.B. a.g.c. output
6	Brown/red/white	To a.f.c. LOCK lamp
7	Red/blue/grey	Output to meter
8	Violet	-7V
9	Black	Earth (0V)
	Screen ←	Earth
10	Coaxial ←	A.F.C. 1 MHz output
11	Coaxial ← orange/white sleeves	1 MHz input
12	Two screens ←	Earth
13	Brown/red/green	A.F.C. on/off
14	Orange/red/blue	Attenuator on/off

TABLE 19 (cont.)

Board pin no.	Colour	Function
15	Screen	Earth
16	Coaxial	Carrier input
17	Orange	+12V



Chapter 2-3

LIST OF TEST EQUIPMENT

CONTENTS

Para.
Introduction 1

TABLES

No. Page
1 Test equipment and tools 1

INTRODUCTION

1. This chapter lists the common test equipment and tools necessary to carry out the performance checks, alignment procedures and fault diagnosis given in subsequent chapters. Authorised equivalent items of test equipment may be used instead of those listed in Table 1, provided that their parameters are at least as good as the equipment they replace.

TABLE 1

Test equipment and tools

Item No.	Reference No.	Nomenclature	Remarks
1	10S/6625-99-900-8337	Signal generator set CT452A	Quantity two required
2	10S/6257379	Signal generator (HP8640A)	
3		Signal generator (Rohde and Schwarz BN41001)	High output power.
4		Waveform analyser (Marconi TF2330A)	
5	10S/6625-99-951-5188	Waveform analyser (Racal 9058)	
6	10S/6625-99-628-5323	Digital frequency meter (Racal 9059)	
7	10S/6625-99-952-6577	Universal counter-timer (Racal 836)	Only required for Chap.2-6
8	10S/6625-99-199-2562	Oscilloscope set CT180A	

TABLE 1 (cont'd)

Item No.	Reference No.	Nomenclature	Remarks
9	110U/6625-00-464-7744	Dual channel vertical amplifier 1802A	For use with item 8
10	10S/9522195	Probe electronic test	For use with item 8
11	5QP/6625-99-105-7049	Multimeter set CT498A	
12	10S/1945895	Digital voltmeter	
13	10S/6625-99-955-6255	Electronic multi-meter CT471C	
14	10S/6625-99-193-4355	H.F. electronic voltmeter	
15	10S/6625-99-914-9811	Wattmeter absorption	
16		Combiner (Hatfield Instruments 3251/50/03)	
17			
18	10L/5905-99-222-0249	Attenuator, step 0-100dB in 1dB steps, 50 ohm	
19	10L/5826-99-115-7165	Attenuator fixed 10dB, 50 ohm	
20	6110-99-945-8802 or 6110-99-945-8801	Variable voltage stabilised power supply,	
21		Headphones 600 ohms	
22	10H/9437277	BNC "T" connector	
23		BNC termination 50 ohm	
24		Capacitor fixed 0.01µF, 50V	
25		Resistor fixed 1 kilohm 5% 0.25W	

TABLE 1 (cont'd)

Item No.	Reference No.	Nomenclature	Remarks
26		Trimming tool (Racal 908067)	Fitted within the r.f. compartment and to the inside of the right-hand side panel.
27		Trimming tool (Racal 909934)	

Chapter 2-4

RECEIVER PERFORMANCE CHECKS

CONTENTS

Para.
1 Introduction
2 Preliminary settings
3 Display
4 Frequency standard
5 Local oscillator output
6 34 MHz output
7 IF and af gain control check
8 LF signal-plus-noise/noise ratio
9 HF signal-plus-noise/noise ratio - ssb
10 HF signal-plus-noise/noise ratio - am
11 AGC and af gain control range checks
12 RF meter calibration
13 Ultimate signal-plus-noise/noise ratio - ssb
14 Single-signal selectivity
15 BFO range
16 Spurious response to external signals
17 Intermodulation (in band)
18 Cross modulation
► 19 A.F.C. tests (PM369)
20 A.F.C. tests (PM664) ◄

Table Page
1 KHz control-setting check 3
2 Audio output level check: USB mode 6
3 Audio output level check: ISB-L mode 7
4 Single-signal selectivity checks 10

INTRODUCTION

1 These tests may be carried out as part of routine servicing (Topic 4/5) or as an aid to the location of a fault. The checks should be carried out in the order given.

PRELIMINARY SETTINGS

2 Throughout the following tests, the switch on the 12 V battery module (when fitted) should be set to OFF; however, should it be necessary to switch off the receiver, upon switching on again the kHz part of the tuned frequency will have to be re-set.

(1) Check that the front-panel POWER switch is set to OFF.

(2) Set the 1 MHz, 34 MHz, and LO switches on the rear panel to INT.

(3) Check the setting of the VOLTAGE SELECTOR on the rear panel.

(4) Set the POWER switch to ON.

(5) Check that:-

(a) the MHz dial illuminates.

(b) the kHz display illuminates at 00000.

(c) the synthesizer OUT OF LOCK lamp illuminates and then extinguishes.

(6) Set the front panel METER switch, in turn, to +20, +12, +5 and -7. Check that for each position,the meter indication lies within the green portion of the meter scale.

DISPLAY

3. (1) Set the MHz control to 3.

(2) Set the TUNING RATE switch to SLOW.

(3) Slowly spin the kHz control clockwise; the kHz display should increase in 10Hz steps at a rate of 2.5kHz per turn.

(4) Slowly spin the kHz control counter-clockwise; the kHz display should decrease in 10Hz steps. As the display passes from 00000 to 99999, check that the lamp behind the 3 on the MHz dial extinguishes, and that the lamp behind the 2 illuminates.

(5) Continue to decrease the kHz display indication until it stops at 97999.

(6) Turn the MHz control one position counter-clockwise; the illuminated 2 should move to the centre of the MHz scale.

(7) Spin the kHz control counter-clockwise; the kHz display should decrease from 97999.

(8) Spin the kHz control clockwise; the kHz display should increase to 99999, change to 00000 and then stop at 02000. As the display passes through 00000, the lamp behind on the 2 on the MHz dial should extinguish, and the lamp behind the 3 should illuminate.

(9) Turn the MHz control one position clockwise; the illuminated 3 should move to the centre of the MHz scale.

(10) Spin the kHz control clockwise; the kHz display should increase from 02000.

(11) Set the TUNING RATE switch to FAST.

(12) Spin the kHz control in each direction in turn and check that the kHz display moves in 100Hz steps at a rate of 50kHz per turn. The '10Hz' figure should remain stationary at 0.

(13) Set the TUNING RATE switch to LOCK.

(14) Spin the kHz control in each direction in turn and ensure that the kHz display indication does not vary.

Note...

A mechanical damper is fitted to the tuning shaft and may be adjusted to suit the users preference (Chap.1-1, fig.2).

FREQUENCY STANDARD

4. (1) Ensure that the rear panel 1MHz and LO INT/EXT switches are set to INT.

(2) Connect the digital frequency meter to the 1MHz IN/OUT socket.

(3) Ensure that the digital frequency meter indicates 1000 000Hz plus or minus 1Hz.

(4) Disconnect the digital frequency meter from the 1MHz IN/OUT socket and connect in its place the h.f. electronic voltmeter (50Ω input impedance).

(5) Check that the h.f. electronic voltmeter indicates at least 180 millivolts.

(6) Set the 1MHz INT/EXT switch to EXT and ensure that the h.f. electronic voltmeter indication falls to zero.

(7) Set the 1MHz INT/EXT switch to INT.

LOCAL OSCILLATOR OUTPUT

5. (1) Set the MHz control to display 0.

(2) Set the kHz control for a display of 00000.

(3) Set the TUNING RATE switch to LOCK.

(4) Connect the 1MHz IN/OUT socket on the receiver to the External Standard socket on the digital frequency meter. Set the digital frequency meter to operate from an external 1MHz standard.

(5) Connect the digital frequency meter to the LO IN/OUT socket.

(6) Ensure that the digital frequency meter indicates 35 400 000Hz plus or minus 1Hz.

(7) Set the MHz switch to 1. Ensure that the digital frequency meter indicates 36 400 000Hz plus or minus 1Hz.

(8) Set the MHz switch to each position in turn and ensure that the digital frequency meter indicates 35.4MHz plus the MHz setting.

(9) Reset the MHz switch to 0.

(10) Set the kHz control to display the frequencies in Table 1, and ensure that the corresponding output frequencies are indicated on the digital frequency meter.

TABLE 1

kHz control-setting check

kHz display	Digital frequency meter reading (Hz)
000.00	35 400 000
111.11	35 511 110
222.22	35 622 220
333.33	35 733 330
444.44	35 844 440
555.55	35 955 550
666.66	36 066 660
777.77	36 177 770

TABLE 1 (cont'd)

kHz display	Digital frequency meter reading (Hz)
888.88	36 288 880
999.99	36 399 990
000 00 (MHz reads '1')	36 400 000

(11) Disconnect the digital frequency meter from the LO IN/OUT socket and connect in its place the h.f. electronic voltmeter (50Ω input impedance).

(12) Step the MHz switch through each position, i.e. 0 to 29, and check that the electronic voltmeter indication is not less than 180 millivolts for each position.

(13) Set the LO INT/EXT switch to EXT and ensure that the electronic voltmeter indication falls to zero.

(14) Set the LO INT/EXT switch to INT.

(15) Set the front panel METER switch to DRIVE LEVEL.

(16) Step the MHz switch through each position and check that the receiver meter indication falls within the 'V' portion of the meter scale for each position except 0 where the meter should indicate approximately half deflection.

(17) Set the MHz switch to 0 and the kHz to 015.00. Check that the meter indication lies within the 'V' portion of the meter scale.

34MHz OUTPUT

▶ 6. (1) Using the 'T'-connector, connect the h.f. electronic voltmeter (50Ω input impedance) and the digital frequency meter to the 34MHz IN/OUT socket. Set the AFC switch to OFF.

(2) Ensure that the frequency meter indicates 34 000 000Hz plus or minus 1Hz. Then disconnect the frequency meter. ◀

(3) Check that the h.f. electronic voltmeter indication is not less than 180 millivolts.

(4) Set the 34MHz INT/EXT switch to EXT and ensure that the h.f. electronic voltmeter indication falls to zero.

(5) Set the 34MHz INT/EXT switch to INT and disconnect the h.f. electronic voltmeter.

I.F. AND A.F. GAIN CONTROL CHECK

7. (1) Set the following controls as indicated:

(a) MHz to 3

(b) AGC to SHORT and AFC to OFF

(c) MODE to USB and USB BANDWIDTH to 3

(d) I.F. GAIN fully clockwise

(e) A.F. GAIN fully counter-clockwise and LS to ON.

(2) Turn the A.F. GAIN progressively clockwise and check that the noise in the loudspeaker increases.

(3) Set the AGC switch to OFF. Turn the I.F. GAIN counter-clockwise and check that the noise in the loudspeaker decreases.

(4) Set the AGC switch to SHORT. Check that the noise in the loudspeaker increases to full output and that the I.F. GAIN control is inoperative.

(5) Connect the headphones to the left-hand PHONES jack. Check that the noise in the loudspeaker remains and that the noise can also be heard in the headphones.

(6) Transfer the headphones to the right-hand PHONES jack. Check that there is no output from the loudspeaker and that noise can be heard in the headphones.

L.F. SIGNAL-PLUS-NOISE/NOISE RATIO

8. (1) Set the receiver controls as follows:

(a) TUNING RATE to FAST

(b) MHz to 0

(c) kHz to 015.00

(d) MODE to USB and USB BANDWIDTH to 3

(e) LS to OFF and AFC to OFF

(f) HEADPHONES plugged in

(2) Connect the wattmeter absorption to the LS and E terminals of TS1 on the rear panel. Set the wattmeter to 8 ohms.

(3) Connect the CW output from the signal generator (Chap.2-3, Table 1, item 1), set to a frequency of 15kHz and an output level of 10 microvolts. e.m.f., to the antenna socket.

(4) Tune the signal generator to the receiver.

(5) Set the AGC switch to SHORT.

(6) Adjust the A.F. GAIN for an indication of 100 milliwatts on the wattmeter.

(7) Set the AGC switch to OFF. Using the I.F. GAIN control, restore the AF output to 100 milliwatts on the wattmeter (0dB reference point).

(8) Off-tune the signal generator by at least 10kHz . Ensure that the AF output falls by not less than 15dB.

▶ (9) Tune the receiver to 50.00kHz.

(10) Set the signal generator to a frequency of 50kHz and an output level of 3 microvolts e.m.f.

(11) Repeat operations (4) to (8).

(12) Tune the receiver to 990.00kHz.

(13) Set the signal generator to a frequency of 990kHz and an output level of 1 microvolt e.m.f.

(14) Repeat operations (4) to (8). ◀

9. (1) Set the receiver controls as follows:

(a) TUNING RATE to FAST

(b) MHz to 28

(c) kHz to 020.00

(d) RF TUNE to WB

(e) AGC to SHORT

(f) MODE to USB and USB BANDWIDTH to 3

(g) LS to OFF and AFC to OFF

(h) HEADPHONES plugged in

(2) Connect the h.f. electronic voltmeter to the MAIN IF OUT socket on the rear panel (50Ω input impedance).

(3) Connect the CW output from the signal generator (Chap.2-3, Table 1 item 1), set to a frequency of 28.020MHz and an output level of 2 microvolts e.m.f., to the antenna socket.

(4) Tune the signal generator to the receiver for maximum response in the receiver passband.

(5) Note the level on the electronic voltmeter. This should not be less than 50 millivolts.

(6) Set the front panel AM/USB LINE LEVEL and A.F. GAIN controls fully clockwise.

(7) Use the wattmeter to measure the audio output levels at the following points. The levels should not be less than those shown in Table 2.

TABLE 2

Audio output level check: USB mode

Phones jack	600Ω	10mW
Loudspeaker terminals	8Ω	1w
Line O/P main I.F.	600Ω	4mw

(8) Set the MODE switch to ISB-L.

(9) Connect the h.f. electronic voltmeter to the ISB IF OUT socket.

(10) Tune the signal generator for maximum response within the receiver passband.

(11) Check that the electronic voltmeter indication is not less than 50 millivolts.

(12) Set the LSB LINE LEVEL and A.F. GAIN controls fully clockwise.

(13) Use the wattmeter to measure the audio output levels at the following points. The levels should not be less than those shown in Table 3.

TABLE 3

Audio output level check: ISB-L mode

Phones jack	600Ω	10mW
Loudspeaker terminals	8Ω	1W
Line O/P ISB	600Ω	4mW

(14) Set the MODE switch to USB.

(15) Reconnect the wattmeter, set to 8 ohms, to the loudspeaker terminals (TS1, LS and E).

(16) Set the signal generator output level to 1 microvolt e.m.f.

(17) Tune the signal generator to the receiver for maximum indication on the wattmeter.

(18) Adjust the A.F. GAIN control for an indication of 100mW on the wattmeter.

(19) Set the AGC switch to OFF. Adjust the IF GAIN control to restore the a.f. output to 100mW (0dB reference point).

Note...

DO NOT readjust the AF or IF GAIN controls for the remainder of this test.

(20) Off-tune the signal generator by at least 10kHz, and check that the a.f. output, as indicated on the wattmeter, falls by not less than 15dB.

(21) Retune the signal generator to the receiver. Adjust the RF TUNE control for a maximum indication on the meter. Off-tune the signal generator by at least 10kHz and check that the a.f. output falls by not less than 9dB. Set the RF TUNE switch to WB.

(22) Repeat operations (17) to (21) at each of the following frequencies. DO NOT adjust the AF GAIN or IF GAIN controls.

(a) 15.02MHz

(b) 8.02MHz

(c) 4.02MHz

(d) 3.02MHz

(e) 1.02MHz

H.F. SIGNAL-PLUS-NOISE/NOISE RATIO - A.M.

10. (1) Set the receiver controls as follows:

(a) MHz to 4

(b) kHz to 020.00

(c) TUNING RATE to LOCK

(d) RF TUNE to WB

(e) AGC to SHORT

(f) MODE to AM and USB BANDWIDTH to 3

(g) AFC to OFF

(h) LS to OFF

(j) HEADPHONES plugged in

(2) Connect the h.f. electronic voltmeter (50Ω impedance) to the MAIN IF OUT socket on the rear panel.

(3) Set the signal generator (Chap.2-3, Table 1, item 1) output level to 1.5 microvolts e.m.f. and c.w.

(4) Tune the signal generator to the receiver for maximum indication on the electronic voltmeter.

(5) Set the signal generator to give 70 per cent amplitude modulation at 400Hz.

(6) Adjust the A.F. GAIN control for an indication of 100mW on the wattmeter (connected between the LS and E terminals of TS1).

(7) Set the AGC switch to OFF.

(8) Adjust the IF GAIN control to restore the a.f. output to 100mW (0dB reference point).

(9) Switch off the modulation at the signal generator and check that the a.f. output level falls by not less than 10dB.

A.G.C. AND A.F. GAIN CONTROL RANGE CHECKS

11. (1) Set the receiver controls as follows:

(a) MHz to 3

(b) kHz to 500.00

(c) TUNING RATE to LOCK

(d) RF TUNE to WB

(e) AGC to SHORT

(f) MODE to USB and USB BANDWIDTH to 3

(g) LS to OFF and AFC to OFF

(h) HEADPHONES plugged in

(2) Set the output level from the signal generator (connected to the antenna socket) to 2 microvolts c.w.

(3) Tune the signal generator to the receiver for maximum response within the receiver passband.

(4) Adjust the AF GAIN control for an indication of 100 milliwatts on the wattmeter (connected between the LS and E terminals of TS1).

(5) Increase the output level from the signal generator to 200 millivolts e.m.f. (+100dB relative to 2 microvolts) and check that the a.f. output level does not increase by more than 6dB.

(6) Reset the signal generator output level to 2 microvolts.

(7) Set the AGC switch to LONG and repeat operations (4) and (5).

(8) Set the IF GAIN control fully counter-clockwise.

(9) Set the AGC switch to OFF.

(10) Check that the a.f. output level does not exceed 100 milliwatts.

(11) Set the AGC switch to SHORT.

R.F. METER CALIBRATION

12. (1) Set the METER switch to R.F.

(2) Increase the output level from the signal generator to 200 millivolts e.m.f. (+100dB relative to 2 microvolts).

► (3) Check that the dB reading on the meter is 100dB plus or minus 15dB. ◄

(4) Reduce the signal generator output level in 20dB steps down to 2 microvolts (0dB). Check that the dB reading on the meter is within plus or minus 15dB of the input level at each step.

ULTIMATE SIGNAL-PLUS-NOISE/NOISE RATIO - S.S.B.

13. (1) Set the receiver controls as follows:

(a) MHz to 3

(b) kHz to 500.00

(c) TUNING RATE to LOCK

(d) RF TUNE to WB

(e) AGC to SHORT

(f) MODE to USB and USB BANDWIDTH to 3

(g) LS to OFF and AFC to OFF

(h) HEADPHONES plugged in

(2) Increase the signal generator output level to 1 millivolt e.m.f. (+60dB relative to 1 microvolt).

► (3) Adjust the AF GAIN control for an indication of 1 watt on the wattmeter. ◄

(4) Connect the electronic multimeter (Chap.2-3, Table 1, item 13), set to measure a.c. voltage, across the wattmeter terminals, and note the level indicated.

(5) Set the AGC switch to OFF.

(6) Adjust the IF GAIN control for an indication of 1 watt on the wattmeter.

(7) Off-tune the signal generator by at least 10kHz.

(8) Check that the reading on the electronic multimeter falls by not less than 50dB. Disconnect the electronic multimeter.

SINGLE-SIGNAL SELECTIVITY

14. (1) Connect the h.f. electronic voltmeter (50Ω impedance) to the MAIN IF OUT socket.

(2) Connect the digital frequency meter, via the high impedance probe, across the electronic voltmeter.

(3) Set the AGC switch to OFF and the AFC switch to OFF.

(4) Set the USB BANDWIDTH switch to 3.

(5) Set the MODE switch to AM.

(6) Tune the signal generator to the receiver for maximum output as indicated on the electronic voltmeter.

(7) Adjust the IF GAIN control for an indication of 100 millivolts on the electronic voltmeter (0dB reference).

(8) Decrease the frequency of the signal generator until the electronic voltmeter indicates minus 5dB relative to the 0dB reference level established at operation (7).

(9) Note the frequency displayed on the frequency meter; it should not be greater than 1396.0kHz.

(10) Increase the frequency of the signal generator until the electronic voltmeter again indicates minus 5dB relative to the 0dB reference level.

(11) Note the frequency displayed on the frequency meter; it should not be less than 1404.0kHz.

(12) Repeat operations (4) to (11) for the s.s.b. and offset filters, setting the MODE/USB BANDWIDTH switches to the appropriate positions in accordance with Table 4; check that the 5dB limits are as specified.

TABLE 4

Single-signal selectivity checks

MODE/USB BANDWIDTH switch position	5dB bandwidths (kHz)	
	Not less than	Not greater than
AM, 8 kHz	1404.0	1396.0
USB, 0.4 - 1.6 kHz	1399.6	1398.4
USB, 1.1 - 2.9 kHz*	1398.900*	1397.100*
USB, 0.8 - 1.2 kHz	1399.2	1398.8
USB, 0.3 - 3 kHz	1399.7	1397.00
LSB, 0.3 - 3 kHz	1403.0	1400.30

* (Post Mod TC0015)

Note...

For the l.s.b. measurements, connect the electronic voltmeter to the ISB IF OUT socket.

B.F.O. RANGE

15. (1) Set the receiver controls as follows:

(a) MHz to 3

(b) kHz to 499.00

(c) TUNING RATE to LOCK

(d) RF TUNE to WB

(e) AGC to SHORT

(f) MODE to USB+BFO

(g) USB BANDWIDTH to 3

(h) LS to OFF and AFC to OFF

(j) HEADPHONES plugged in

(2) Connect the digital frequency meter and the signal generator (Chap.2-3, Table 1, item 1), to the receiver antenna socket using a "T" connector (Chap.2-3, Table 1, item 22).

(3) Set the signal generator frequency for a reading of 3 500.00kHz on the digital frequency meter.

(4) Disconnect the frequency meter and reconnect it across the wattmeter (connected between the LS and E terminals of TS1).

(5) Set the AF GAIN control for a reading of 100mW on the wattmeter.

(6) Set the BFO control to '+'.

(7) Check that the frequency indicated on the frequency meter is within the limits 3000Hz to 4000Hz.

(8) Vary the BFO control over the range and check that a tone can be heard in the headphones that decreases in frequency to zero beat and then increases in frequency.

(9) Set the BFO control to '-'.

(10) Check that the frequency indicated on the frequency meter is within the limits 3000Hz to 4000Hz.

Note...

If operations (7) and (10) do not yield the desired results, reset the range of the variable BFO by a slight adjustment of the 'BFO' inductor (access via hole in cover) on the 34MHz generator board, underside of receiver. Then repeat operations (6) to (10).

(11) Disconnect the frequency meter.

SPURIOUS RESPONSE TO EXTERNAL SIGNALS

16. (1) Set the receiver controls as follows:

(a) MHz to 3

(b) kHz to 500.00

(c) TUNING RATE to LOCK

(d) R.F. TUNE to WB

(e) AGC to OFF and AFC to OFF

(f) MODE to USB and USB BANDWIDTH to 3

(g) AF GAIN to mid-position

(h) IF GAIN fully clockwise

(j) LS to OFF

(k) HEADPHONES plugged in

(2) Set the signal generator (Chap.2-3, Table 1, item 1) to a frequency of 3.5MHz c.w. and the output level to 1 microvolt e.m.f.

(3) Tune the signal generator to the receiver for maximum indication on the wattmeter.

(4) Adjust the AF GAIN control for a reference level of 100 milliwatts on the wattmeter.

(5) Increase tne signal generator output level by 90dB.

(6) Tune the signal generator carefully from 50kHz to 3.48MHz and from 3.52MHz to 36MHz (ignore those frequencies which are direct sub-harmonics of 3.5MHz). Adjust the signal generator output level, as necessary, to restore the 100 milliwatt reference level for each spurious response encountered. Check that the signal generator output level required to restore the reference output exceeds plus 80dB relative to 1 microvolt.

INTERMODULATION (IN BAND)

17. (1) Set the receiver controls as follows:

(a) MHz to 3

(b) kHz to 500.00

(c) TUNING RATE to LOCK

(d) RF TUNE to WB

(e) AGC to LONG

(f) MODE to USB

(g) LS to OFF and AFC to OFF.

(h) HEADPHONES plugged in

(2) Connect the two signal generators (Chap.2-3, Table 1, item 1) designated A and B, to the combiner (Chap.2-3, Table 1, item 16). Connect the combiner output to the step attenuator and connect the output of the step attenuator to the h.f. electronic voltmeter (50 ohms input impedance).

(3) Set the step attenuator to 6dB.

(4) Set signal generator A to CARRIER OFF and adjust the output level of signal generator B, set to CW, for a reading of 15 millivolts on the electronic voltmeter.

(5) Set signal generator B to CARRIER OFF, signal generator A to CW, and adjust the output level of signal generator A for a reading of 15 millivolts on the electronic voltmeter.

(6) Disconnect the electronic voltmeter and connect the step attenuator output to the receiver antenna socket.

(7) Connect the wattmeter, set to 600 ohms, to the LINE OUTPUT MAIN IF terminals of TS1 on the rear panel of the receiver.

(8) Connect the waveform analyser (Chap.2-3, Table 1, item 4) across the wattmeter.

(9) Set the LOAD switch on the waveform analyser to OUT.

(10) Connect the digital frequency meter across the waveform analyser.

(11) Set the frequency of signal generator A for a reading of 1100Hz on the frequency meter.

(12) Set signal generator A to CARRIER OFF.

(13) Set signal generator B to CW and adjust its frequency for a reading of 1700Hz on the frequency meter.

(14) Disconnect the frequency meter.

(15) Adjust the AM/USB LINE LEVEL control for an output of 4mW on the wattmeter.

(16) Set signal generator A to CW.

(17) Tune the waveform analyser for maximum output at 1700Hz.

(18) Adjust the attenuator on the waveform analyser for an indication of 0dB on the waveform analyser meter.

(19) Tune the waveform analyser to the 1100Hz signal and check that the level indicated on the analyser meter is 0dB plus or minus 1dB.

(20) Tune the waveform analyser to each of the following frequencies, in turn, and check that any intermodulation product measured is not less negative than minus 40dB relative to the 0dB reference level of either tone.

(a) 500Hz

(b) 600Hz

(c) 2300Hz

(d) 2800Hz

(21) Set the MODE switch to ISB-L. Transfer the wattmeter to the ISB LINE OUTPUT terminals of TS1. Repeat operations (10) to (20). At operation (15), adjust the LSB LINE LEVEL control instead of the AM/USB LINE LEVEL control.

(22) Disconnect the waveform analyser and the wattmeter.

CROSS MODULATION

18. (1) Set the receiver controls as follows:

(a) TUNING RATE to FAST

(b) MHz to 5

(c) kHz to 000.00

(d) AGC to SHORT

(e) MODE to AM

(f) USB BANDWIDTH to 3

(g) AF GAIN to mid-position

(h) IF GAIN fully clockwise

(j) LS to OFF and AFC to OFF

(k) HEADPHONES plugged in

(2) Connect the two signal generators, designated A and B, to the combiner. Connect the combiner output to the step attenuator and connect the output of the step attenuator to the h.f. electronic voltmeter (50 ohms input impedance).

(3) Set the step attenuator to 6dB.

(4) Set signal generator A to CARRIER OFF and adjust the output level of signal generator B, set to CW, for a reading of 5 millivolts on the electronic voltmeter.

(5) Set signal generator B to CARRIER OFF, signal generator A to CW, and adjust the output level of signal generator A for a reading of 5 millivolts on the electronic voltmeter.

(6) Disconnect the electronic voltmeter and connect the step attenuator output to the receiver antenna socket.

(7) Set signal generator B to CW and reduce the output level of each signal generator by 30dB.

(8) Use the digital frequency meter to set up the signal generators as follows:

(a) Signal generator A (wanted signal) to 5000.000kHz, 30 per cent amplitude modulation at 400Hz.

(b) Signal generator B (unwanted signal) to 5020.000kHz, 30 per cent amplitude modulation at 400Hz.

(9) Connect the wattmeter, set to 8 ohms impedance, between the LS and E terminals of TS1.

(10) Tune the receiver to the wanted signal (A) for a maximum indication on the wattmeter.

(11) Adjust the AF GAIN control for an indication of 100 milliwatts on the wattmeter (0dB reference level).

(12) Switch off the modulation of the wanted signal (A) and check that the wattmeter indication falls by not less than 30dB.

(13) Increase the level of the unwanted signal (B) to obtain an indication on the wattmeter of 1 milliwatt.

(14) Check that the level of the unwanted signal (B) is not less than 60dB above signal (A) (the wanted signal) in order to produce a cross modulation figure of 3 per cent.

(15) Disconnect signal generators A and B.

► A.F.C. TESTS (PM369) ◄

19. (1) Set the receiver controls as follows:-

(a) MHz to 3

(b) KHz to 500.00

(c) TUNING RATE to LOCK

(d) RF TUNE to WB

(e) AGC to SHORT

(f) AFC to OFF

(g) MODE to AM

(h) IF GAIN fully clockwise

(j) METER to TUNE CARRIER

(2) Connect the signal generator (Chap.2-3, Table 1, item 1), set to a frequency of 3.5MHz and an output level of 1 millivolt e.m.f. (c.w.) to the receiver antenna socket.

(3) Tune the signal generator to the receiver frequency and, as the correct tuning position is approached, check that the meter reading decreases to the TUNE CARRIER mark.

(4) With the receiver correctly tuned to the input signal, set the AFC switch to FULL CARRIER.

(5) Check that the AFC LOCK lamp glows and that the meter indicates zero on the AFC scale.

(6) Set the AFC switch to OFF and then to PILOT CARRIER; check that the AFC LOCK lamp again glows.

(7) Slowly decrease the signal generator frequency until the meter indication coincides with the '-' mark on the AFC scale.

(8) Check that the AFC LOCK lamp is still glowing.

(9) Check that the signal generator frequency is not greater than 3 499.500kHz.

(10) Slowly increase the signal generator frequency until the meter indication coincides with the '+' mark on the AFC scale.

(11) Check that the AFC LOCK lamp is still glowing.

(12) Check that the signal generator frequency is not less than 3 500.500kHz.

(13) Retune the generator to 3 500.000kHz.

(14) Disconnect the signal generator at the receiver antenna socket.

(15) Increase the receiver tuned frequency by 50Hz.

(16) Set the AFC switch to OFF and then to FULL CARRIER.

19. (17) Reconnect the signal generator to the receiver antenna socket.

(18) Check that the AFC LOCK lamp is glowing.

(19) Retune the receiver to 3 500.000kHz.

(20) Disconnect the signal generator at the receiver antenna socket.

(21) Decrease the receiver tuned frequency by 50Hz.

(22) Set the AFC switch to OFF and then to FULL CARRIER.

(23) Reconnect the signal generator to the receiver antenna socket.

(24) Check that the AFC LOCK lamp is glowing.

(25) Set the AFC switch to OFF.

(26) Tune the signal generator to the receiver frequency and, as the correct tuning position is approached, check that the meter indication decreases to the TUNE CARRIER mark.

(27) With the receiver correctly tuned to the input signal, set the AFC switch to FULL CARRIER.

(28) Check that the AFC LOCK lamp glows and that the meter indicates zero on the AFC scale.

(29) Disconnect the signal generator at the receiver antenna socket.

(30) After a period of one minute, reconnect the signal generator to the receiver antenna socket.

(31) Check that the AFC LOCK lamp is glowing.

(32) Retune the signal generator to the receiver frequency.

(33) Reduce the signal generator output to 0.9 microvolts e.m.f.

(34) Check that the AFC LOCK lamp is extinguished.

(35) Increase the signal generator output to 3.0 microvolts e.m.f. Check that the AFC LOCK lamp is glowing and that the meter indicates zero on the AFC scale.

(36) Set the METER switch to RF.

(37) Increase the signal generator output to 10 microvolts e.m.f. Check that the front-panel meter indicates 20dB plus or minus 15dB.

(38) Increase the signal generator output in 20dB steps up to 100dB. Check that at each output setting the meter indicates the correct level within plus or minus 15dB and that the AFC LOCK lamp remains 'on'.

(39) Set the signal generator output to 20 microvolts e.m.f. Check that the AFC LOCK lamp extinguishes, that the meter indication decreases and that the AFC LOCK lamp again glows.

(40) Set the signal generator for 70 per cent amplitude-modulation at 1kHz.

(41) Set the MODE switch to USB + BFO and the USB BANDWIDTH to 0.8 - 1.2. Set the BFO control for a suitable audio tone output.

(42) Set the signal generator output to 64 microvolts e.m.f.

(43) Check that the AFC LOCK lamp is glowing.

(44) Adjust the AF GAIN control for an indication of 50 milliwatts on the wattmeter.

(45) Set the AFC switch to OFF. Check that any rise in the audio output level does not exceed +12dB.

(46) Set the AFC switch to PILOT CARRIER. Check that the AFC LOCK lamp glows and that the audio output level falls by not less than -15dB and not more than -25dB relative to the 50 milliwatt level.

(47) Disconnect all test equipment.

► A.F.C. TESTS (PM664)

20 Set the receiver controls as follows:-

20.1 MHz to 1

20.2 kHz to 020.00

20.3 RF TUNE to WB

20.4 AGC to OFF

20.5 MODE to AM

20.6 AFC to OFF

20.7 IF GAIN to fully clockwise

20.8 METER to TUNE CARRIER

20.9 LS to ON

21

21.1 Check that the front panel meter indicates full scale.

21.2 Connect the signal generator, set to a frequency of 3.5 MHz and a c.w. output level of 1 mV e.m.f., to the receiver antenna socket.

21.3 Tune the input signal to the receiver and, as the correct tuning position is approached, check that the meter reading decreases to the TUNE CARRIER mark, and beats at a low frequency as the audio tone decreases to zero beat.

21.4 With the receiver correctly tuned to the input signal, set the AFC switch to FULL CARRIER.

21.5 Check that the AFC LOCK lamp glows and the meter indicates zero on the AFC scale.

21.6 Set the AFC switch to OFF and then to PILOT CARRIER. Check that the AFC LOCK lamp again glows.

21.7 Connect the digital frequency meter to the MAIN IF OUT socket, and EXT STD to the 1 MHz IN/OUT socket on the receiver. Set the digital frequency meter for EXT STD operation and set the timebase to 10 s. Ensure that the frequency displayed is 1.4 MHz ± 2 Hz.

21.8 Set the TUNING RATE switch to SLOW.

21.9 Slowly increase the receiver frequency, allowing the a.f.c. to lock-up every 50 Hz, until the receiver frequency is 1.0205 MHz.

21.10 Ensure that the AFC LOCK lamp is still glowing.

21.11 Slowly re-tune the receiver to 1.020 MHz.

21.12 Slowly decrease the receiver frequency, allowing the a.f.c. to re-lock every 50 Hz, until the receiver frequency is 1.0195 MHz.

21.13 Ensure that the AFC LOCK lamp is still glowing. ◄

►21

21.14 Re-tune the receiver to 1.020 MHz.

21.15 Disconnect the signal generator at the receiver antenna socket.

21.16 Increase the receiver frequency by 50 Hz.

21.17 Set the A.F.C. switch to OFF and then to FULL CARRIER.

21.18 Reconnect the signal generator to the receiver antenna socket.

21.19 Ensure that the A.F.C. LOCK lamp glows within 13 s.

21.20 Re-tune the receiver to 1.020 MHz.

21.21 Disconnect the signal generator at the receiver antenna socket.

21.22 Decrease the receiver frequency by 50 Hz.

21.23 Set the A.F.C. switch to OFF and then to FULL CARRIER.

21.24 Reconnect the signal generator to the receiver antenna socket.

21.25 Ensure that the A.F.C. LOCK lamp glows within 13 s.

21.26 Set the A.F.C. switch to OFF.

21.27 Check that the meter indicates full scale.

21.28 Tune the receiver to the input signal and, as the correct tuning position is approached, check that the meter indication decreases to the TUNE CARRIER mark.

21.29 With the receiver correctly tuned to the input signal, set the A.F.C. switch to FULL CARRIER.

21.30 Check that the A.F.C. LOCK lamp glows and the meter indicates zero on the A.F.C. scale.

21.31 Set the TUNING RATE switch to LOCK.

21.32 Disconnect the signal generator at the receiver antenna socket.

21.33 After a period of one minute, reconnect the signal generator to the receiver antenna socket.

21.34 Check that the A.F.C. LOCK lamp is glowing.

21.35 Set the METER switch to RF.

21.36 Reduce the signal generator output to 1 μV e.m.f.

21.37 Check that the A.F.C. LOCK lamp is extinguished and that the front panel meter indicates 0 dB.

21.38 Increase the signal generator output to 3 μV e.m.f. and check that the A.F.C. LOCK lamp is glowing.

21.39 Set A.F.C. to OFF, and MODE to USB. Set the signal generator to 10 μV e.m.f. and tune it to the receiver passband. Measure and note the voltage at the DIV AGC terminal on the rear panel using the digital voltmeter. Set MODE to CW and BANDWIDTH to 3 kHz.

21.40 Tune the signal generator for zero beat on the tune-carrier meter. Switch the A.F.C. to FULL CARRIER and ensure that the LOCK lamp glows after a few seconds. Increase the signal generator output until the voltage at the DIV AGC terminal is the same as that noted in operation 21.39. Note the increase in signal generator output which should be 10 dB ± 5 dB. ◄

►21

21.41 Set MODE to USB and A.F.C. to OFF. Repeat operations 21.39 and 40 for a signal generator output of 300 μV e.m.f.

21.42 Ensure that the a.f.c. is locked. Set the signal generator output to 30 μV e.m.f. Set the AGC to MANUAL and decrease the IF GAIN until the LOCK lamp starts to flicker.

21.43 Switch to PILOT CARRIER and ensure that the LOCK lamp glows. Decrease the generator output until the A.F.C. LOCK lamp starts to flicker. Check that the decrease in level is 20 dB ± 5 dB.

21.44 Disconnect all test equipment. ◄

Chapter 2-5

RECEIVER ALIGNMENT PROCEDURES

CONTENTS

Para.

1 Introduction
6 Power supplies
8 Shaft-encoder and display board PM371
9 Low-frequency loop board PM588
10 Upper loop board PM589
11 Transfer loop board PS338
12 High-frequency loop board PS337
13 34 MHz generator board PM339
14 Main if/af board PM364/1
15 ISB if/af board PM364/3
16 Typical signal levels (if/af boards)
17 Filter board PS367
18 Preliminary
19 8 kHz symmetrical filter
20 3 kHz u.s.b. filter
21 0.4 - 1.6 kHz u.s.b. filter
22 0.8 - 1.2 kHz l.s.b. filter
23 3 kHz l.s.b. filter
24 Carrier filter
25 Second mixer board PM336
26 First mixer board PM335
28 R.F. board PM582
29 Protection stage
30 Mute circuit
31 A.F.C. board PM369
Final setting-up procedure i.f./a.f. boards
32 Main i.f./a.f. board
33 I.S.B. i.f./a.f. board
34 Mode and filter switches
35 Diversity a.g.c. adjustments
37 Main i.f./a.f. board
38 I.S.B. i.f./a.f. board
39 A.F.C. board
40 R.F. meter calibration
► 41 A.F.C. board PM664 ◄

Table Page

1 Power supply adjustments 2
2 R.F. board adjustments 25

Fig. Page

1 Tuning capacitor setting: 18-degree point 23

INTRODUCTION

1 This chapter contains alignment procedures for the receiver as a complete assembly. Instructions for checking the performance of the receiver are given in Chapter 2-4.

2. Under normal operating conditions the receiver will maintain the factory alignment over a long period of time. Re-alignment should, therefore, only be carried out following the replacement of a printed-circuit board or other components which affect the alignment, or where a known mis-alignment exists.

3. Should it be necessary to re-align the complete receiver, the following procedures should be carried out in the order given. Before attempting to re-align an individual sub-assembly it must be ascertained, where applicable, that the preceeding assemblies are functioning correctly. After re-alignment, ensure that screening covers are replaced using all screws provided.

4. If the specified performance cannot be attained by alignment, then a fault must be suspected and reference should be made to Chapter 2-6.

5. The required trimming tools are provided with each receiver; one is mounted in a clip attached to the inside of the right-hand side panel and a second is mounted within the r.f. compartment.

POWER SUPPLIES

6. Throughout the following tests, the switch on the 12V battery module (when fitted) should be set to OFF; however, should it be necessary to switch off the receiver, upon switching-on again the kHz part of the tuned frequency will have to be re-set.

7. (1) Lower the rear panel of the receiver (Chap.2-2, para.11).

(2) Connect the digital voltmeter between chassis (OV) and, in turn, the regulator board pins given in Table 1; if necessary, adjust the appropria control until the voltage is within the limits specified. Use the oscilloscope to measure the ripple voltage.

TABLE 1

Power supply adjustments

Regulator board pin	Nominal voltage	Voltage limits	Adjust	Ripple voltage
22	+20	± 100mV	R19	5mv p-p
16	+12	± 50mV	R17	5mV p-p
10	+ 5	± 50mV	R3	5mV p-p
5	- 7	± 50mV	R8	5mV p-p

(3) Connect the digital voltmeter between pin 14 on the main i.f./a.f. board and chassis. If necessary, adjust R3 on the a.f. and memory regulator board for a reading of +14.5V ± 50mV. Use the oscilloscope to measure the ripple voltage; this should not exceed 5 millivolts peak-to-peak.

(4) Connect the digital voltmeter between pin 23 on the display board (orange/brown wire) and chassis. Check that the digital voltmeter indicates +5V ± 50mV.

(5) Disconnect all test equipment and replace the rear panel.

Note ...

Throughout the receiver, the following cableform colours are used for d.c. power distribution:

+20V	Red	+14.5V	Red/blue
+12V	Orange	Memory +5V	Orange/brown
-7V	Violet	0V	Black
+5V	Brown		

SHAFT-ENCODER AND DISPLAY BOARD PM371

8. (1) Using a dual-trace oscilloscope (Chap.2-3, Table 1, items 8 and 9), connect the probe for channel A to ML27 pin 8 (encoder A output) and the channel B probe to ML17 pin 8 (encoder B output) on the display board.

(2) Set the oscilloscope to display channel A only.

(3) Ensure that the TUNING RATE switch is not in the LOCK position.

(4) Whilst rotating the kHz control, check that a square wave is displayed on the oscilloscope. If necessary, adjust R2 on the potentiometer board (attached to the shaft-encoder) for unity mark-to-space ratio.

(5) Set the oscilloscope to display channel B only.

(6) Whilst rotating the kHz control, check that a square wave is displayed on the oscilloscope. If necessary, adjust R1 on the potentiometer board for unity mark-to-space ratio.

(7) Set the oscilloscope to display both channels. Trigger the oscilloscope on the A channel waveform.

(8) Whilst rotating the kHz control, check that waveform A leads waveform B by 90 degrees. Adjustment should not normally be required but, should the displacement be other than 90 degrees, proceed as follows.

(9) Remove the shaft-encoder (Chap.2-2) and remove its cover. Slacken the graticule carriage screws and adjust the position of the carriage until a 90-degree phase difference is achieved. Tighten the carriage screws whilst maintaining the phase difference.

(10) Replace the cover and refit the shaft-encoder to the front panel assembly.

(11) Disconnect all test equipment.

LOW-FREQUENCY LOOP BOARD PM588

9. (1) Connect the h.f. electronic voltmeter (high-impedance probe) between the junction of R1 with D2, and chassis (0V). Adjust the core of transformer T1 (1MHz input) for a maximum indication on the h.f. electronic voltmeter. The level should be approximately 1V r.m.s.

(2) Set the kHz portion of the receiver frequency to 000.00.

(3) Connect the multimeter, set to the 25V d.c. range, between TP1 (positive) and chassis (negative).

(4) Adjust L1 (6-7MHz v.c.o.) for a reading of +14V on the multimeter.

(5) Measure the output signal level from the 6-7MHz v.c.o. at TP2 using the h.f. electronic voltmeter (high-impedance probe). The level should be approximately 1V r.m.s.

9. (6) Use the oscilloscope to monitor the test points listed below. Check that the signal levels displayed approximate to those indicated:-

TP3: 1MHz square wave, approximate 1:1 mark/space ratio, 3.5V p-p.
TP4: 1kpps, positive-going, 3.5V p-p.
TP5: 1kpps, positive-going, 3.5V p-p.
TP6: 1kpps, negative-going strobe pulse, 3.5V p-p.
TP7: 13 to 20kHz, square wave, 3.5V p-p.
TP8: 13 to 20kpps, negative-going strobe pulse, 3.5V p-p.

(7) Disconnect all test equipment.

UPPER LOOP BOARD PM589

10. (1) Set the kHz portion of the receiver frequency to 990.00.

(2) Connect the multimeter, set to the 25V d.c. range, between board pin 7 (positive) and chassis (negative).

(3) Adjust L4 for a reading of +14V on the multimeter.

(4) Set the kHz portion of the receiver frequency to 000.00.

(5) Connect the multimeter, set to the 25V d.c. range, between TP7 (positive) and chassis (negative).

(6) Adjust L1 for a reading of +16V on the multimeter.

(7) Connect the h.f. electronic voltmeter, 50-ohm input impedance, between board pin 2 and chassis (0V). Check that the level indicated is 225mV r.m.s. plus or minus 2dB, at kHz settings of 000.00, 500.00 and 990.00.

(8) Use the oscilloscope to monitor the test points listed below. Check that the signal levels displayed approximate to those indicated.

TP1: 1.013 to 1.020MHz square wave, 3.5V p-p.
TP2: 4.6 to 3.6MHz square wave, 3.5V p-p.
TP3: 10.13 to 10.20kpps, positive-going, 3.5V p-p.
TP4: 10.13 to 10.20kpps strobe pulse, negative-going, 3.5V p-p.
TP5 and
TP6: Phase-comparator output pulses, positive-going and in phase, 3.5V p-p.

(9) Disconnect all test equipment.

TRANSFER LOOP BOARD PS338

11. There are no adjustments for this board. Use the oscilloscope to monitor the test points listed below. Check that the signal levels displayed approximate to those indicated.

TP1: 4.6 to 3.6MHz square wave, 5V p-p.
TP2: 115 to 52kHz square wave, 3.5V p-p.
TP3: 115 to 52kpps, negative-going, 3.5V p-p.
TP4 and
TP5: 115 to 52kpps, 1.5 microsecond negative-going and in phase, 3.5V p-p
TP6: 115 to 52kpps strobe pulse, negative-going, 3.5V p-p.

HIGH-FREQUENCY LOOP BOARD PS337

12. (1) Set the receiver MHz switch to 29.

(2) Set the receiver kHz control to 999.99.

(3) Connect the multimeter, set to the 25V d.c. range, between board pin 18 (positive) and chassis (negative).

12. (4) Connect the digital frequency meter between board pins 13 and 14 (OV).

(5) Adjust L20 for a reading of 8V on the multimeter. Check that the digital frequency meter indicates 947.826kHz plus or minus 10Hz. Disconnect the digital frequency meter.

(6) Connect the multimeter, set to the 25V d.c. range, between TP3 (positive) and chassis (OV). Check that the multimeter indicates approximately 14V.

(7) Set the MHz switch to 17MHz. Transfer the positive lead of the multimeter to TP2. Check that the multimeter indicates approximately 14V.

(8) Set the MHz switch to 7MHz. Transfer the positive lead of the multimeter to TP1. Check that the multimeter indicates approximately 14V.

(9) Set the MHz switch to 29. Ensure that the kHz switch is set to display 999.99.

(10) Connect the h.f. electronic voltmeter, high-impedance input, between TP4 and chassis (OV).

(11) Adjust R38 for a reading of 1V r.m.s. on the h.f. electronic voltmeter

(12) Step the MHz switch through each position and check that the h.f. electronic voltmeter indication is 1V r.m.s. plus or minus 2.5dB at each switch position.

(13) Connect the h.f. electronic voltmeter, high-impedance input, between TP5 and chassis (OV). Check that the h.f. electronic voltmeter indicates approximately 1V r.m.s.

(14) Connect the h.f. electronic voltmeter, high-impedance input, between board pin 22 and chassis (OV).

(15) Adjust R44 for a reading of 320mV r.m.s. plus or minus 0.5dB on the h.f. electronic voltmeter.

(16) Connect the 50-ohm termination (Chap.2-3, Table 1, item 23) to the LO IN/OUT socket.

(17) Connect the h.f. electronic voltmeter, high-impedance input, between board pin 24 and chassis (OV).

(18) Adjust R50 for a reading of 320mV r.m.s. plus or minus 0.5dB on the electronic voltmeter.

(19) Connect the multimeter, set to the 25V d.c. range, between the junction of L22 with L23 and chassis (OV).

(20) Adjust L4 for a reading of 14V on the multimeter.

(21) Set the MHz switch to 17.

(22) Ensure that the kHz control is set to display 999.99.

(23) Adjust L5 for a reading of 14V on the multimeter.

(24) Set the MHz switch to 7.

(25) Ensure that the kHz control is set to display 999.99.

(26) Adjust L6 for a reading of 14V on the multimeter. Disconnect the multimeter.

(27) Connect the multimeter, set to the 10V d.c. range, between TP10 (positive) and chassis (OV). Check that the multimeter indicates approximately 3.5V. Disconnect the multimeter.

(28) Use the oscilloscope to monitor the test points listed below. Check that the signal levels displayed approximate to those indicated:-

12. TP6: 442 to 474kpps strobe pulses, negative-going, 3.5V p-p.
TP7 and
TP8: 442 to 474kpps phase-comparator output pulses, negative-going and in phase, 3.5V p-p.
TP12: 885 to 948kHz, approximate square wave, 2.8V p-p.

(29) Disconnect all test equipment.

34MHz GENERATOR BOARD PM339

13. (1) Ensure that the 34MHz INT/EXT switch is set to INT.

(2) Ensure that the 1MHz INT/EXT switch is set to INT.

(3) Connect the oscilloscope to TP3. Check that a 1MHz square wave is displayed, 2:3 mark-to-space ratio, at a level of not less than 2V p-p.

(4) Connect the h.f. electronic voltmeter, 50-ohm input impedance, to the 1MHz IN/OUT socket. Check that the level indicated on the h.f. electronic voltmeter is not less than 180 millivolts r.m.s.

(5) Connect the oscilloscope to board pins 6 and 5 (OV). Check that the amplitude of the 1MHz waveform displayed is approximately 0.5V p-p.

(6) Connect the oscilloscope to board pins 8 and 7 (OV). Check that the amplitude of the 1MHz waveform displayed is approximately 0.2V p-p.

(7) Connect the oscilloscope to TP9. Check that the amplitude of the 1MHz square wave displayed exceeds 2V p-p.

(8) Set the MODE switch to USB and the USB BANDWIDTH switch to 3.

(9) Connect the oscilloscope to TP7. Check that the frequency of the square wave displayed (3:2 mark-to-space ratio) is 200kHz and that the amplitude is approximately 3.5V p-p.

(10) Connect the oscilloscope to board pins 10 and 31 (OV).

(11) Tune T2 for maximum output on the oscilloscope.

(12) Adjust R65 to set the amplitude of the displayed 1.4MHz waveform to 0.8V p-p.

(13) Connect the digital frequency meter to board pins 10 and 31 (OV). Check that the digital frequency meter indicates 1 400 000Hz plus or minus 1Hz. Disconnect the digital frequency meter.

(14) Connect the oscilloscope to board pins 11 and 32 (OV). Check that the amplitude of the 1.4MHz waveform displayed is 0.8V p-p.

(15) Connect the digital frequency meter to board pins 11 and 32 (OV).

(16) Set potentiometer R4 fully clockwise.

(17) Set the MODE switch to USB+BFO.

(18) Set the front panel BFO control to '+'.

(19) Adjust inductor L4 for a digital frequency meter indication of 1 397 000Hz plus or minus 100Hz.

(20) Set the BFO control to '-'.

(21) Adjust R4 for a digital frequency meter indication of 1 403 000Hz plus or minus 100Hz.

(22) Repeat steps (18) to (21) until there is no further improvement. Disconnect the digital frequency meter.

(23) Connect the oscilloscope to TP15. Check that the amplitude of the waveform displayed is approximately 400mV p-p.

13. (24) Connect the oscilloscope to board pins 10 and 31 (OV). Check that the amplitude of the waveform displayed exceeds 0.5V p-p.

(25) Connect the oscilloscope to board pins 11 and 32 (OV). Check that the amplitude of the waveform displayed exceeds 0.5V p-p.

(26) Connect the digital frequency meter to board pins 20 and 21 (OV).

(27) Connect the 1MHz IN/OUT socket on the rear panel to the external-standard socket on the digital frequency meter. Set the digital frequency meter for external 1MHz standard operation.

(28) Connect the multimeter, set to the 10V d.c. range, to TP1 (positive) and chassis (OV).

(29) Adjust L2 for a multimeter indication of 7V. Check that the digital frequency meter indicates 34 000 000Hz. Disconnect the digital frequency meter.

(30) Disconnect the multimeter. Connect the h.f. electronic voltmeter, 50-ohm input impedance, to the 34MHz IN/OUT socket on the rear panel.

(31) Check that the h.f. electronic voltmeter indication is not less than 180 millivolts r.m.s.

(32) Connect the h.f. electronic voltmeter, high input impedance, to board pins 20 and 21 (OV).

(33) Check that the h.f. electronic voltmeter indication is within the limits 800 millivolts to 1.4 volts r.m.s.

(34) Disconnect all test equipment.

Note...

Typical signal levels at the test points not already covered are listed below.

TP2: 5Mpps, oscilloscope, 3V p-p.
TP4: 34MHz VCO output, h.f. electronic voltmeter, high-impedance input, 750mV r.m.s.
TP5: 34MHz, h.f. electronic voltmeter, high-impedance input, 400mV r.m.s.
TP6: 34MHz h.f. electronic voltmeter, high-impedance input, 1.4V r.m.s.
TP8: H.f. electronic voltmeter, high-impedance input, 1.4V r.m.s.
TP10: Not fitted.
TP11: 1MHz square wave, 3:2 mark-to-space ratio, oscilloscope, 3.5V p-p.
TP12: MODE switch to USB, 1MHz square wave, 3:2 mark-to-space ratio, oscilloscope, 3.5V p-p.
TP13: Not fitted.
TP14: 1Mpps, negative-going, oscilloscope, 3.5V p-p.

MAIN I.F./A.F. BOARD PM364/1

Note...

The following alignment procedures are carried out with the main i.f./a.f. board isolated from the remainder of the receiver. Further minor adjustments are therefore required following the alignment of the r.f., first mixer and second mixer boards. These adjustments are given in para.33 and 34

14. (1) Set the receiver front-panel controls as follows:-

14. (a) RF TUNE to WB.
(b) AGC to OFF and AFC to OFF.
(c) IF GAIN fully counter-clockwise.
(d) MODE to USB and USB **BANDWIDTH** to 3.
(e) AF GAIN fully counter-clockwise.

(2) Remove link 1 from the main i.f./a.f. board.

(3) Connect the multimeter, set to the 100 milliamp d.c. range, between the pins of link 1, with the negative lead of the multimeter connected to the pin nearest the edge of the board.

(4) Adjust potentiometer R84 for a reading of 15 milliamps on the multimeter.

(5) Disconnect the multimeter and replace link 1.

(6) Unsolder the coaxial lead connected to pin 2 on the filter board PS367 (the coaxial screen may be left connected to pin 3).

(7) Connect the 1 kilohm resistor in series with the coaxial lead connected to the 50-ohm output of the signal generator (Chap.2-3, Table 1, item 1) and connect the other end of this lead to the coaxial lead removed at operation (6). Connect the screen to pin 3 on the filter board.

(8) Connect the digital frequency meter to the UNCAL socket on the signal generator.

(9) Set the frequency of the signal generator to 1.400MHz, plus or minus 500Hz and the output level to 60 microvolts e.m.f.

(10) Set the IF GAIN control fully clockwise.

(11) Ensure that the MODE switch is set to USB.

(12) Ensure that the AF GAIN control is set fully counter-clockwise.

(13) Set potentiometers R3, R4 and R42 fully counter-clockwise.

(14) Set potentiometer R9 fully clockwise.

(15) Connect the h.f. electronic voltmeter, high-impedance input, to TP3.

(16) Adjust inductors L1 and L2 for a maximum indication on the h.f. electronic voltmeter.

(17) Adjust R9 for a level of 200 millivolts at TP3 and then repeat operation (16).

(18) Sweep the signal generator frequency from 1390kHz to 1410kHz. Note the frequency at which the peak output occurs. Also note the level of the peak output.

(19) Sweep the signal generator frequency again from 1390kHz to 1410kHz. Ensure that the output level remains within 1dB of the level noted at operation (18).

(20) Set the signal generator to the frequency noted at operation (18).

(21) Adjust R9 for an indication of 200 millivolts r.m.s. on the h.f. electronic voltmeter (connected to TP3).

(22) Adjust R3 to reduce the h.f. electronic voltmeter indication to 100 millivolts and then reset the level to 200 millivolts with R9.

(23) Repeat operations (18) and (19). If the 1dB tolerance of operation (19) cannot be met, repeat operations (16) to (23).

(24) Connect the digital voltmeter to board pins 29 (positive) and 28 (0V).

(25) Adjust R31 for an indication of 1.4 volts plus or minus 25 millivolts on the digital voltmeter.

14. (26) Transfer the digital voltmeter to board pins 30 (positive) and 28 (OV)

(27) Adjust the IF GAIN control for an indication of 1.4 volts plus or minus 10 millivolts on the digital voltmeter.

(28) Adjust R4 until the signal level at TP3, as indicated on the h.f. electronic voltmeter, decreases by 1dB. Disconnect the voltmeter.

(29) Reduce the signal generator output level by 4dB.

(30) Connect the multimeter, set to the 25V d.c. range, between TP6 (positive) and the -7 volt supply at board pin 20.

(31) Adjust R42 until the indication on the multimeter changes from positive 7 volts ± 1 volt to positive 14 volts ± 1 volt.

(32) Connect the h.f. electronic voltmeter, 50-ohm input impedance, to the MAIN IF OUT socket on the rear panel.

(33) Set the AGC switch to SHORT.

(34) Set the frequency of the signal generator to 1.400MHz plus or minus 500Hz and the output level to 60 microvolts e.m.f.

(35) Ensure that the i.f. output signal level, as indicated on the h.f. electronic voltmeter, is not less than 50 millivolts r.m.s.

(36) Increase the signal generator output level by 70dB. Ensure that the increase in the i.f. output signal level is not greater than 5dB.

(37) Reset the signal generator output level to 60 microvolts e.m.f. Set the AGC switch to LONG and repeat operations (35) and (36).

(38) Reset the signal generator output level to 60 microvolts e.m.f.

(39) Connect the electronic multimeter (Chap.2-3, Table 1, item 13) to board pins 8 and 9 (OV).

(40) Tune the signal generator for a maximum indication on the electronic multimeter. Ensure that the level indicated is not less than 150 millivolts r.m.s.

(41) Disconnect the electronic multimeter. Connect the wattmeter absorption, set to 8 ohms input impedance, between the LS and E terminals of TS1.

(42) Set the AF GAIN control fully clockwise and ensure that the wattmeter indication is not less than 1 satt.

(43) Set the AF GAIN control for an indication of 100 milliwatts on the wattmeter.

(44) Increase the signal generator output level by 70dB and ensure that the wattmeter indication is not greater than 100 milliwatts plus 5dB.

(45) Reduce the signal generator output level by 60dB.

(46) Set the MODE switch to AM.

(47) Set the signal generator for 30 per cent amplitude modulation at 1kHz.

(48) Set the AF GAIN control fully clockwise and ensure that the wattmeter indication is not less than 1 watt.

(49) Set the AF GAIN control for an indication of 1 watt on the wattmeter.

(50) Connect a wire link between the MUTE and E terminals of TS2. Ensure that the wattmeter indication decreases by not less than 40dB. Disconnect the wire link.

(51) Set the MODE switch to USB.

14. (52) Reset the signal generator output level to 60 microvolts e.m.f.

(53) Transfer the wattmeter absorption, set to 600 ohms input impedance, to the LINE OUTPUT MAIN IF terminals of TS1.

(54) Set the AM/USB LINE LEVEL control fully clockwise and ensure that the wattmeter indication is not less than 10 milliwatts.

(55) Set the MODE switch to AM.

(56) Set the signal generator for 30 per cent amplitude modulation at 1kHz.

(57) Increase the signal generator output level by 60dB. Ensure that the wattmeter indication is not less than 4 milliwatts.

(58) Switch off and disconnect all test equipment.

(59) Reconnect the coaxial lead, removed at operation (6), to pin 2 on the filter board.

Note...

See para.16 for typical signal levels.

I.S.B. I.F./A.F. BOARD PM364/3

Note...

The following alignment procedures are carried out with the i.s.b. i.f./a.f. board isolated from the remainder of the receiver. Further minor adjustments are therefore required following the alignment of the r.f., first mixer and second mixer boards. These adjustments are given in para.33.

15. (1) Set the receiver front-panel controls as follows:

(a) AGC to OFF and AFC to OFF
(b) MODE to LSB
(c) IF GAIN fully clockwise
(d) AF GAIN fully counter-clockwise

(2) Set potentiometers R3, R4 and R42 fully counter-clockwise.

(3) Set potentiometer R9 fully clockwise.

(4) Unsolder the coaxial lead connected to pin 4 on the filter board PS367 (the coaxial screen may be left connected to pin 5).

(5) Connect the 1 kilohm resistor in series with the coaxial lead connected to the 50 ohm output of the signal generator (Chap.2-3, Table 1, item 1). Connect the other end of this lead to the coaxial lead removed at operation (4). Connect the screen to pin 5 on the filter board.

(6) Connect the digital frequency meter to the UNCAL socket on the signal generator.

(7) Set the frequency of the signal generator to 1.400MHz, plus or minus 500Hz, and the output level to 60 microvolts e.m.f.

(8) Connect the h.f. electronic voltmeter, high input impedance, to TP3.

(9) Adjust inductors L1 and L2 for a maximum indication on the h.f. electronic voltmeter.

(10) Adjust R9 for a level of 200 millivolts r.m.s. at TP3 and then repeat operation (9).

(11) Sweep the signal generator frequency from 1390kHz to 1410kHz. Note the frequency at which the peak output occurs. Also note the level of the peak output.

15. (12) Sweep the signal generator frequency again from 1390kHz to 1410kHz. Ensure that the output level remains within 1dB of the level noted at operation (11).

(13) Set the signal generator to the frequency noted at operation (11).

(14) Adjust R9 for an indication of 200 millivolts r.m.s. on the h.f. electronic voltmeter (connected to TP3).

(15) Adjust R3 to reduce the h.f. electronic voltmeter indication to 100 millivolts and then reset the level to 200 millivolts with R9.

(16) Repeat operations (11) and (12). If the 1dB tolerance of operation (12) cannot be met, repeat operations (9) to (16).

(17) Connect the digital voltmeter to board pins 29 (positive) and 18 (OV).

(18) Adjust R31 for an indication of 1.4 volts plus or minus 10 millivolts on the digital voltmeter.

(19) Transfer the digital voltmeter to board pins 30 (positive) and 28 (OV).

(20) Adjust the IF GAIN control for an indication of 1.4 volts plus or minus 10 millivolts on the digital voltmeter.

(21) Adjust R4 until the signal level at TP3, as indicated on the h.f. electronic voltmeter, decreases by 1dB. Disconnect the h.f. electronic voltmeter.

(22) Reduce the signal generator output level by 4dB.

(23) Connect the multimeter, set to the 25V d.c. range, between TP6 (positive and the -7 volt supply at board pin 20.

(24) Adjust R42 until the indication on the multimeter changes from positive 7 volts $\pm$ 1 volt to positive 14 volts $\pm$ 1 volt.

(25) Connect the h.f. electronic voltmeter, 50-ohm input impedance, to the ISB IF OUT socket on the rear panel.

(26) Set the AGC switch to SHORT.

(27) Set the frequency of the signal generator to 1.400MHz plus or minus 500Hz and the output level to 60 microvolts e.m.f.

(28) Ensure that the i.f. output signal level, as indicated on the h.f. electronic voltmeter, is not less than 50 millivolts r.m.s.

(29) Increase the signal generator output level by 70dB. Ensure that the increase in the i.f. output signal level is not greater than 5dB.

(30) Reset the signal generator output level to 60 microvolts e.m.f. Set the AGC switch to LONG and repeat operations (28) and (29).

(31) Reset the signal generator output level to 60 microvolts e.m.f.

(32) Connect the electronic multimeter (Chap.2-3, Table 1, item 13) to board pins 8 and 9 (OV).

(33) Tune the signal generator for a maximum indication on the electronic multimeter. Ensure that the level indicated is not less than 150 millivolts r.m.s.

(34) Disconnect the electronic multimeter.

(35) Connect the wattmeter absorption, set to 600 ohms input impedance, to the ISB LINE OUTPUT terminals of TS1.

(36) Set the LSB LINE LEVEL control fully clockwise and ensure that the wattmeter indication is not less than 4 milliwatts.

15. (37) Set the LSB LINE LEVEL control for an indication of 1.0 milliwatt on the wattmeter.

(38) Increase the signal generator output level by 70dB and ensure that the wattmeter indication is not greater than 1.0 milliwatt plus 5dB.

(39) Connect the electronic multimeter across the wattmeter terminals.

(40) Adjust the LSB LINE LEVEL control for an output indication of 1.0 milliwatt.

(41) Connect a wire link between the MUTE and E terminals of TS2. Ensure that the output level is reduced by not less than 40dB. Remove the wire link.

(42) Switch off and disconnect all test equipment.

(43) Reconnect the coaxial lead, removed at operation (4), to pin 4 on the filter board.

Typical signal levels (i.f./a.f. boards)

16. The typical signal levels listed below are measured under the following test conditions, unless stated otherwise:

(1) Signal generator, output level set to 40 microvolts e.m.f., connected to the i.f. input pins 34 and 35 (filter board output open-circuit).

(2) Receiver front-panel controls set as follows (USB BANDWIDTH to 3):

MODE:	
Main i.f./a.f. board:	USB
I.S.B. i.f./a.f. board:	LSB
AGC	OFF
IF GAIN	Fully clockwise

(3) Measurements at TP2, TP3 and TP4 are made using the h.f. electronic voltmeter, high input impedance.

(4) Measurements at TP7, pins 8 and 9 and TP6 are made using the electronic multimeter.

TP2:	100 millivolts r.m.s.
TP3:	200 millivolts r.m.s. (set by R9)
TP4:	Between 90 and 130 millivolts r.m.s.
TP7:	Between 50 and 90 millivolts r.m.s.
Pins 8 & 9:	Not less than 150 millivolts, typically between 170 and 250 millivolts r.m.s.
TP6:	Signal generator output increased to 120 microvolts, amplitude-modulated 30 per cent at 1kHz: Between 50 and 90 millivolts r.m.s.

FILTER BOARD PS367

17. There are no adjustments to be made to the filter board. Since the filters are sealed units, any filter that fails to meet the performance figures given in the following paragraphs should be replaced.

Preliminary

18. (1) Remove the coaxial socket from the chassis-mounted second mixer output connector (fig.2, Chap.1-1).

(2) Connect the output of the signal generator (Chap.2-3, Table 1, item 1) to the filter board input via the coaxial socket disconnected at operation (

18. (3) Connect the digital frequency meter to the UNCAL output socket on the signal generator.

(4) Connect the h.f. electronic voltmeter, 50-ohm input impedance, to the MAIN IF OUT socket on the rear panel.

(5) Set the IF GAIN control fully clockwise.

(6) Set the AGC and AFC switches to OFF.

(7) Set the signal generator frequency to 1.4MHz and the output level to 150 microvolts e.m.f.

8kHz symmetrical filter

19. (1) Set the MODE switch to AM.

(2) Tune the signal generator for maximum output, as indicated on the h.f. electronic voltmeter. Ensure that the ouptut level is greater than 50 millivolts r.m.s. with the IF GAIN control fully clockwise.

(3) Set the IF GAIN control for an indication of 50 millivolts on the h.f. electronic voltmeter.

(4) Decrease the signal generator frequency until the output falls by 3dB relative to the 50-millivolt level. Ensure that the frequency indicated on the digital frequency meter is less than 1 396 000Hz.

(5) Increase the signal generator frequency until the output falls by 3dB relative to the 50-millivolt level. Ensure that the frequency indicated on the digital frequency meter is greater than 1 404 000Hz.

3kHz u.s.b. filter

Note ...

Due to the inversion within the receiver, the filter selected for u.s.b. operation will have l.s.b. characteristics and vice-versa.

20. (1) Set the MODE switch to USB.

(2) Connect the h.f. electronic voltmeter, 50-ohm input impedance, to the MAIN IF OUT socket on the rear panel.

(3) Tune the signal generator for maximum output, as indicated on the h.f. electronic voltmeter. Ensure that the output level is greater than 50 millivolts r.m.s. with the IF GAIN control fully clockwise.

(4) Set the IF GAIN control for an indication of 50 millivolts on the h.f. electronic voltmeter.

(5) Decrease the signal generator frequency until the output falls by 3dB relative to the 50-millivolt level. Ensure that the frequency indicated on the digital frequency meter is less than 1 397 000Hz.

(6) Increase the signal generator frequency until the output falls by 3dB relative to the 50-millivolt level. Ensure that the frequency indicated on the digital frequency meter is greater than 1 399 700Hz.

0.4-1.6kHz u.s.b. filter

21. (1) With the MODE switch at USB, set the USB BANDWIDTH switch to 0.4-1.6.

(2) Connect the h.f. electronic voltmeter, 50-ohm input impedance, to the MAIN IF OUT socket on the rear panel.

(3) Tune the signal generator for maximum output, as indicated on the h.f. electronic voltmeter. Ensure that the output level is greater than 50 millivolts r.m.s. with the IF GAIN control fully clockwise.

(4) Set the IF GAIN control for an indication of 50 millivolts on the h.f. electronic voltmeter.

(5) Decrease the signal generator frequency until the output falls by 3dB relative to the 50-millivolt level. Ensure that the frequency indicated on the digital frequency meter is less than 1 398 400Hz.

(6) Increase the signal generator frequency until the output falls by 3dB relative to the 50-millivolt level. Ensure that the frequency indicated on the digital frequency meter is greater than 1 399 600Hz.

0.8-1.2kHz u.s.b. filter

22. (1) With the MODE switch at USB, set the USB BANDWIDTH switch to 0.8-1.2.

(2) Connect the h.f. electronic voltmeter, 50-ohm input impedance, to the MAIN IF OUT socket on the rear panel.

(3) Tune the signal generator for maximum output, as indicated on the h.f electronic voltmeter. Ensure that the output level is greater than 50 millivolts r.m.s. with the IF GAIN control fully clockwise.

(4) Set the IF GAIN control for an indication of 50 millivolts on the h.f. electronic voltmeter.

(5) Decrease the signal generator frequency until the output falls by 3dB relative to the 50-millivolt level. Ensure that the frequency indicated on the digital frequency meter is less than 1 398 800Hz.

(6) Increase the signal generator frequency until the output falls by 3dB relative to the 50-millivolt level. Ensure that the frequency indicated on the digital frequency meter is greater than 1 399 200Hz.

3kHz l.s.b. filter

23. (1) Set the MODE switch to LSB.

(2) Transfer the h.f. electronic voltmeter, 50-ohm input impedance, to the ISB IF OUT socket on the rear panel.

(3) Tune the signal generator for a maximum output, as indicated on the electronic voltmeter. Ensure that the output level is greater than 50 millivolts r.m.s. with the IF GAIN control fully clockwise.

(4) Set the IF GAIN control for an indication of 50 millivolts on the electronic voltmeter.

(5) Decrease the signal generator frequency until the output falls by 3dB relative to the 50-millivolt level. Ensure that the frequency indicated on the digital frequency meter is less than 1 400 300Hz.

(6) Increase the signal generator frequency until the output falls by 3dB relative to the 50-millivolt level. Ensure that the frequency indicated on the digital frequency meter is greater than 1 403 000Hz.

Carrier filter

24. (1) On the filter board, remove the links between board pins 22 and 24 and pins 17 and 18; reconnect the links between board pins 22 and 23 and pins 16 and 17 respectively.

(2) Unsolder and remove the white/black wire from pin 15 on the filter board.

(3) Connect a temporary link between board pins 7 and 8.

(4) Set the MODE switch to USB.

(5) Ensure that the AFC and AGC switches are set to OFF.

(6) Connect the h.f. electronic voltmeter (50 ohms input impedance) to the MAIN IF OUT socket on the rear panel.

(7) Tune the signal generator for maximum output, as indicated on the h.f. electronic voltmeter.

(8) Set the IF GAIN control fully clockwise and check that the indication on the h.f. electronic voltmeter is greater than 50 millivolts r.m.s.

(9) Set the IF GAIN control for an indication of 50 millivolts on the electronic voltmeter.

(10) Decrease the signal generator frequency until the output falls by 3dB relative to the 50-millivolt output level. Check that the frequency indicated on the digital frequency meter is less than 1 399 950Hz.

(11) Increase the signal generator frequency until the output falls by 3dB relative to the 50-millivolt level. Check that the frequency indicated on the digital frequency meter is greater than 1 400 050Hz.

(12) Switch off and disconnect all test equipment.

(13) Remove the links between pins 22 and 23 and pins 16 and 17 on the filter board; reconnect the links between pins 22 and 24 and pins 17 and 18 respectively.

(14) Reconnect the white/black wire to board pin 15.

(15) Reconnect the coaxial socket to the chassis mounted second mixer output plug.

SECOND MIXER BOARD PM336

25. (1) Remove links 1 and 2 from the board.

(2) Set the front panel AGC switch to OFF.

(3) Set the IF GAIN control fully counter-clockwise.

(4) Ensure that the 34MHz INT/EXT switch is set to INT.

(5) Connect the h.f. electronic voltmeter, 50-ohm input impedance, between link 2 (pin adjacent to the screen) and TP2 (OV).

(6) Adjust inductors L10, L13 and L14 for a maximum indication on the h.f. electronic voltmeter.

25. (7) Repeat operation (6) until there is no increase in output.

(8) Check that the h.f. electronic voltmeter indication is not less than 600 millivolts r.m.s.

(9) Disconnect the h.f. electronic voltmeter and replace link 2.

(10) Set the MODE switch to USB and the USB BANDWIDTH switch to 3.

(11) Connect the h.f. electronic voltmeter, 50-ohm impedance, to the MAIN IF OUT socket on the rear panel.

(12) Connect the signal generator (Chap.2-3, Table 1, item 1) via the 0.01µF capacitor, between link 1 (pin farthest from the screen) and TP2 (OV) on the second mixer board.

(13) Set the signal generator to a frequency of 35.399MHz plus or minus 500Hz.

(14) Set the output level of the signal generator for an indication on the h.f. electronic voltmeter of 50 millivolts r.m.s.

(15) Tune L15 for a maximum indication on the h.f. electronic voltmeter, adjusting the output of the signal generator as necessary to maintain an indication of 50 millivolts r.m.s.

(16) Check that the signal generator output level does not exceed 8 microvolts e.m.f.

(17) Disconnect the signal generator and capacitor.

(18) Replace link 1 on the second mixer board PM336.

(19) Remove link 1 on the first mixer board PM335. Set R8 fully clockwise.

(20) Connect the output of the signal generator, set to a frequency of 35.399MHz, to the T3 end of link 1 on the first mixer board PM335.

(21) Set the signal generator output level for an indication on the h.f. electronic voltmeter of 50 millivolts r.m.s.

(22) Tune inductors L1, L6, L7, L8, L9 and L11 for maximum output as indicated on the h.f. electronic voltmeter. Repeat until there is no further improvement.

(23) Reset the signal generator output level for an indication of 50 millivolts on the h.f. electronic voltmeter.

(24) Check that the signal generator output level is less than 1.5 microvolts e.m.f.

(25) Set the receiver POWER switch to OFF and carefully unsolder the externally connected lead (orange/red) from pin 9 on the second mixer board.

(26) Connect the positive lead of the variable voltage-stabilized power supply to pin 9 on the second mixer board. Connect the negative lead to chassis (OV).

(27) Set the receiver POWER switch to ON and switch on the variable voltage power supply and set the output to 2.25 volts.

(28) Adjust potentiometer R8 for an output of 45 millivolts, as indicated on the h.f. electronic voltmeter.

(29) Set the output of the variable voltage power supply to 2.9 volts.

(30) Increase the signal generator output level by 38dB.

(31) Ensure that the output level, as indicated on the h.f. electronic voltmeter, is not greater than 50 millivolts r.m.s.

25 (32) Decrease the signal generator output level by 38dB.

(33) Disconnect the variable voltage power supply and reconnect the orange/red lead to pin 9 on the second mixer board.

(34) Unsolder the externally connected lead (white/blue) from pin 8 on the second mixer board.

(35) Connect the positive lead of the variable voltage power supply to pin 8 on the second mixer board. Connect the negative lead to chassis (0V).

(36) Switch on the variable voltage power supply and set the output to 2.25 volts.

(37) Ensure that the output level, as indicated on the h.f. electronic voltmeter, is between 40 and 50 millivolts r.m.s.

(38) Set the output of the variable voltage power supply to 2.9 volts.

(39) Increase the signal generator output level by 38dB.

(40) Ensure that the output level, as indicated on the h.f. electronic voltmeter, is not greater than 50 millivolts r.m.s.

(41) Disconnect the variable voltage power supply and reconnect the white/blue lead to pin 8 on the second mixer board.

(42) Replace link 1 on the first mixer board PM335.

(43) Disconnect all remaining test equipment.

FIRST MIXER BOARD PM335

26. (1) Set the receiver controls as follows:

(a) MHz to 1
(b) RF TUNE to WB
(c) LO INT/EXT to EXT
(d) MODE to USB
(e) USB BANDWIDTH to 3
(f) AGC to OFF and AFC to OFF
(g) IF GAIN fully clockwise

(2) Connect the signal generator (Chap.2-3, Table 1, item 1) to the LO INT/OUT socket on the rear panel. Set the frequency of the signal generator to 36MHz and the output level to 880 millivolts e.m.f. (+6dBm).

(3) Connect the h.f. electronic voltmeter, high-impedance input, to TP3.

(4) Sweep the frequency of the signal generator from 36 to 40MHz. Note the level of the peak response as indicated on the h.f. electronic voltmeter.

(5) Set the signal generator to a frequency of 35.415MHz.

(6) Tune T1, L6 and T2 to obtain an output on the h.f. electronic voltmeter of minus 5dB relative to the peak response noted at operation (4).

(7) Connect the h.f. electronic voltmeter to TP5.

(8) Sweep the frequency of the signal generator from 35.415 to 39.4MHz. Check that the level indicated on the h.f. electronic voltmeter remains within minus 6dB of the peak output level.

(9) Set the signal generator to a frequency of 35.400MHz. Check that the level indicated on the h.f. electronic voltmeter falls by not less than 25dB.

(10) Set the front panel MHz switch to 4.

26. (11) Connect the h.f. electronic voltmeter, high input impedance, to TP4.

(12) Set the signal generator to a frequency of 35.400MHz.

(13) Adjust L5 and L7 for a minimum indication on the h.f. electronic voltmeter.

(14) Set the signal generator to a frequency of 50.600MHz.

(15) Adjust L4, L8 and L9 for a maximum indication on the h.f. electronic voltmeter.

(16) Sweep the frequency of the signal generator from 39.400 to 65.400MHz. Check that the level indicated on the h.f. electronic voltmeter remains within minus 6dB of the peak output level.

(17) Disconnect the h.f. electronic voltmeter.

(18) Connect the electronic multimeter (Chap.2-3, Table 1, item 13) to board pin 30.

(19) Sweep the frequency of the signal generator from 39.4 to 65.4MHz. Check that the indication on the electronic multimeter remains within the limits 6 to 15 volts over the frequency range. If necessary re-adjust L4, L5, L7 and L8.

(20) Set the MHz switch on the front panel to 1.

(21) Sweep the frequency of the signal generator slowly from 35.415 to 39.400MHz. Check that the indication on the electronic multimeter remains within the limits 6 to 15 volts over the frequency range. Disconnect the electronic multimeter.

(22) Set the front-panel METER switch to DRIVE LEVEL.

(23) Set the LO INT/EXT switch on the rear panel to INT and disconnect the signal generator from the LO IN/OUT socket.

(24) Adjust potentiometer R39 to set the front-panel meter needle to the centre of the V portion of the scale.

(25) Set the receiver MHz switch to 1.

(26) Set the kHz control for a display of 000.00.

(27) Connect the output of the signal generator to the chassis-mounted first mixer input BNC connector (fig.2, Chap.1-1). Set the signal generator frequency to 1.000MHz and the output level to 5 microvolts e.m.f.

(28) Connect the h.f. electronic voltmeter, 50-ohm input impedance, to the MAIN IF OUT socket on the rear panel.

(29) Tune the signal generator for maximum output, as indicated on the h.f. electronic voltmeter. Check that the output level is not less than 50 millivolts r.m.s.

(30) Set the receiver frequency to 3.999MHz.

(31) Set the signal generator frequency to 4MHz.

(32) Tune the signal generator for maximum output, as indicated on the h.f. electronic voltmeter. Check that the output level is not less than 50 millivolts r.m.s.

(33) Set the receiver MHz switch to 4.

(34) Tune the signal generator for maximum output. Ensure that the output level is not less than 50 millivolts r.m.s.

(35) Set the receiver frequency to 29.999MHz.

26. (36) Set the signal generator frequency to 29.9MHz.

(37) Tune the signal generator for maximum output. Check that the output level is not less than 50 millivolts.

Note...

Typical signal levels at the remaining test points not already covered are listed below:

TP1: MHz switch settings 4 to 29, h.f. electronic voltmeter, high-impedance input, 1V r.m.s.

TP2: MHz switch settings 0 to 3, h.f. electronic voltmeter, high input impedance, 1.2V r.m.s.

TP6: H.F. electronic voltmeter, high input impedance, 900mV to 1.2V r.m.s. dependent on MHz switch setting.

27. If the output signal from the first mixer is very low, i.e. in the order of minus 10dB, a failure of one or more of the field-effect transistors, TR3, TR4, TR6, TR7, should be suspected. Use the following procedure to ascertain whether or not the mixer transistors are functioning correctly.

(1) Set the receiver POWER switch to OFF.

(2) Unsolder and remove the bare tinned copper (BTC) wire link from board pin 15.

(3) Connect the positive output from a 5-volt supply via a multimeter, set to the 100 milliamp d.c. range, to the BTC link wire removed at operation (2). Connect the negative lead from the 5-volt supply to chassis (0V).

(4) Set the receiver POWER switch to ON.

(5) Switch on the 5-volt supply. The current drawn from the 5-volt supply should be between 20 and 35 milliamps. If the current drawn is less than 15 milliamps or greater than 40 milliamps, TR3 and/or TR4 should be replaced.

(6) Switch off and disconnect the 5-volt supply.

(7) Set the receiver POWER switch to OFF.

(8) Replace the BTC wire link to board pin 15.

(9) To check transistors TR6 and TR7, proceed as follows:

(10) Disconnect the BTC wire link from board pin 17.

(11) Connect the positive output of the 5-volt supply via the multimeter, set to the 100-milliamp range, to the link wire removed from board pin 17. Connect the negative lead of the 5-volt supply to chassis (0V).

(12) Set the receiver POWER switch to ON.

(13) Switch on the 5-volt supply. The current drawn from the 5-volt supply should be between 20 and 35 milliamps. If the current drawn is less than 15 milliamps or greater than 40 milliamps, TR6 and/or TR7 should be replaced

Note ...

Before removing a (possibly serviceable) field-effect transistor from the board, wrap a piece of thin BTC wire round the transistor leads (between the base of the transistor and the board). A new field-effect transistor should be supplied with a shorting conductive-rubber ring over the transistor leads. The transistor leads should remain short-circuited until all the leads are soldered to the printed circuit board.

R.F. BOARD PM582

28. (1) Raise the r.f. board to the upright position.

(2) Set the RF TUNE control fully counter-clockwise (the WB position).

(3) Set the front-panel MHz switch to any position other than 0.

(4) Connect the output from signal generator A (Chap.2-3, Table 1, item 1) to the r.f. input socket on the board.

(5) Connect the digital frequency meter to monitor the output from signal generator A.

(6) Connect the h.f. electronic voltmeter, high-impedance input, between TP1 and chassis (OV).

(7) Set signal generator A to a frequency of 36.2MHz plus or minus 50kHz and set the output level to 1.0 volt e.m.f.

(8) Tune L9 for a minimum indicator on the h.f. electronic voltmeter.

(9) Set signal generator A to a frequency of 30.0MHz plus or minus 20kHz.

(10) Tune L7 for a maximum indication on the h.f. electronic voltmeter.

(11) Set signal generator A to a frequency of 20MHz plus or minus 1MHz. Note the level indicated on the h.f. electronic voltmeter.

(12) Sweep the frequency of signal generator A from 35.4 to 65MHz. Check that the h.f. electronic voltmeter indication is not less than 20dB below the level noted at operation (11).

(13) Disconnect the h.f. electronic voltmeter from TP1.

(14) Disconnect the r.f. output BNC plug from the chassis-mounted first mixer input connector (Chap.1-1, fig.2).

(15) Connect the waveform analyser (Chap.2-3, Table 1, item 5) to the r.f. output BNC plug.

(16) Set signal generator A to a frequency of 35.52MHz plus or minus 20kHz. Tune the waveform analyser to this signal, adjusting its attenuator as necessary, to obtain maximum sensitivity.

(17) Tune inductor L17 for a minimum indication on the waveform analyser.

(18) Set signal generator A to the following frequencies in turn. Repeat operations (16) and (17), in each case tuning the appropriate inductors for a minimum indication on the waveform analyser.

Frequency	Inductor
36.88MHz ± 50kHz	L18
40.74MHz ± 50kHz	L16

(19) Disconnect the waveform analyser and connect in its place the h.f. electronic voltmeter, 75-ohm input impedance.

(20) Set the frequency of signal generator A to 30MHz ± 20kHz and the output level to 10 millivolts e.m.f.

(21) Tune inductors L15 and L19 for a maximum indication on the h.f. electronic voltmeter.

(22) Repeat operations (15) to (21) inclusive.

(23) Set the frequency of signal generator A to 1MHz. Note the level indicated on the h.f. electronic voltmeter.

(24) Sweep the frequency of signal generator A from 1 to 30MHz. Ensure that the output level remains within 2.5dB of the level noted at operation (23).

28. (25) Disconnect signal generator A and substitute signal generator B (Chap.2-3, Table 1, item 2). Set signal generator B to a frequency of 30MHz and an output level of 1.0 millivolt e.m.f.

(26) Disconnect the h.f. electronic voltmeter from the r.f. output BNC plug and connect in its place the waveform analyser (Chap.2-3, Table 1, item 5).

(27) Set the waveform analyser for maximum sensitivity and tune it to the frequency of signal generator B. Adjust the waveform analyser attenuator to obtain a convenient reference level on the meter. Note the attenuator setting.

(28) Set signal generator B to a frequency of 35.4MHz and an output level of 1.0 volt e.m.f.

(29) Tune the waveform analyser to the frequency of signal generator B and set the waveform analyser attenuator to obtain the reference level set at (27). Note the new setting of the attenuator. Ensure that the difference in the attenuator settings is not less than 25dB.

(30) Set the frequency of signal generator B to 70 and 100MHz, in turn, and repeat operation (29). Ensure that in each case the difference in attenuator settings is not less than 25dB.

(31) Disconnect signal generator B and the waveform analyser.

(32) Connect the output of signal generator A, set to a level of 10 millivolts e.m.f., to the 75-ohm input of the h.f. electronic voltmeter. Note the level as indicated on the h.f. electronic voltmeter as a reference level.

(33) Disconnect signal generator A from the h.f. electronic voltmeter and re-connect it to the r.f. input socket on the r.f. board.

(34) Connect the h.f. electronic voltmeter to the r.f. output BNC plug.

(35) Set signal generator A to the following frequencies, in turn, and check that the output level, in each case, is as stated.

Frequency (MHz)	Output level relative to the reference level (dB)
0.015	Plus 9.0 ± 1.0
0.100	Plus 15.0 ± 1.0
1.000	Plus 15.0 ± 1.0
2.000	Plus 15.0 ± 1.0
4.000	Plus 15.0 ± 1.0
8.000	Plus 15.0 ± 1.0
16.000	Plus 15.0 ± 1.0
30.000	Plus 15.0 + 1-3.0

(36) Set the frequency of signal generator A to 2.2MHz and set the output level to 100 millivolts e.m.f.

(37) Set the receiver MHz switch to 0.

(38) Tune inductor L10 for a minimum indication on the h.f. electronic voltmeter.

(39) Set the frequency of signal generator A to 100kHz. Ensure that the output level, as indicated on the h.f. electronic voltmeter, is plus 15dB ± 1dB relative to the signal generator output level. Note the output level.

(40) Sweep the frequency of signal generator A from 50kHz to 1MHz. Check that the output level remains within 1dB over the frequency range.

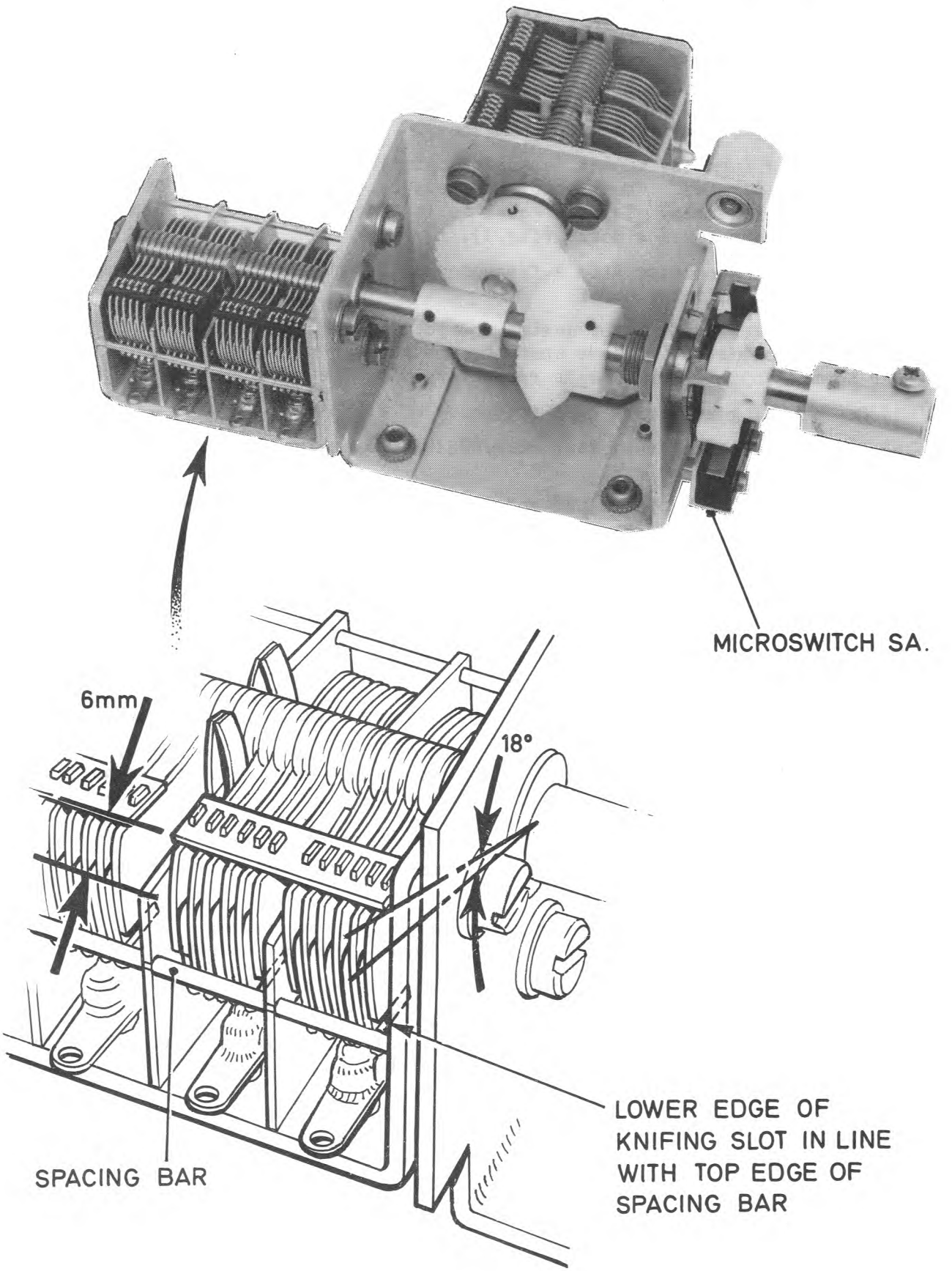


Fig.1 Tuning capacitor setting : 18-degree point

28. (41) Sweep the frequency of signal generator A from 2 to 6MHz. Check that the attenuation over the band, with respect to the output level noted at operation (39), is not less than 27dB.

(42) Set the MHz switch to 1.

(43) Set the tuning capacitor (C22/C23) control-spindle fully-counter-clockwise (capacitor vanes fully enmeshed).

(44) Carefully turn the tuning capacitor spindle clockwise until the micro-switch, SA, operates. Check that the variable capacitor is out of mesh by exactly 6 millimetres. This is equal to 18 degrees of rotation from the fully enmeshed reference point (fig.1).

(45) Set signal generator A to a frequency of 0.98MHz and set the output level to 100 millivolts e.m.f.

(46) Tune the cores of T5 for maximum output, as indicated on the h.f. electronic voltmeter. Ensure that the top and bottom cores of T5 are near to the top and bottom ends respectively of the windings.

(47) Set signal generator A to a frequency of 2.0MHz.

(48) Adjust the tuning capacitor (C22/C23) for a maximum indication on the h.f. electronic voltmeter.

(49) Tune trimmer capacitors C28 and C38 for a maximum output indication.

(50) Repeat operations (44) to (49) inclusive until no further increase in output can be obtained.

(51) Set the tuning capacitor fully counter-clockwise.

(52) Set signal generator A to a frequency of 1.0MHz. Note the output level indicated on the h.f. electronic voltmeter.

(53) Set the tuning capacitor for a maximum output indication. Check that the output level indicated is within 3dB of the level noted at operation (52)

(54) Set the frequency of signal generator A to 1MHz plus 125kHz and, in turn, to 1MHz minus 125kHz. Check that the attenuation, in each case, is not less than 16dB relative to the level at 1MHz.

(55) Set the frequency of signal generator A to 2MHz.

(56) Set the tuning capacitor fully counter-clockwise and note the output level indicated.

(57) Set the tuning capacitor for a maximum output indication. Check that the level indicated is within 3dB of the level noted at operation (56).

(58) Check that the attenuation 250kHz above and below 2MHz is not less than 16dB relative to the output level at 2MHz.

(59) Repeat operations (43) to (58) inclusive for the remaining transformers and trimmer capacitors in accordance with Table 2.

TABLE 2

R.F. board adjustments

MHz switch setting	Signal generator (MHz)	Trans-former	Capacitor	Output (dB) relative to operation (52)	Attenuation	
					At (MHz):	Not less than (dB):
2	2	T4	-	Within 3.0	±0.25	-16
	4	-	C27 + C37	Within 3.0	±0.5	-16
4	4	T3	-	Within 3.0	±0.5	-17
	8	-	C26 + C36	Within 3.0	±1	-17
8	8	T2	-	Within 3.0	±1	-17
	16	-	C25 + C35	Within 3.0	±2	-17
16	16	T1	-	Within 3.0	±2	-17
	30	-	C24 + C34	Within 3.0	±3.75	-17

Protections stage

29. (1) Disconnect signal generator A from the r.f. input connector and substitute signal generator C (Chap.2-3, Table 1, item 3).

(2) Connect the multimeter, set to the 25V d.c. range,between the collector of TR8 (positive) and chassis (OV).

(3) Connect the electronic multimeter (Chap.2-3, Table 1, item 13) to TP2.

(4) Set C31 to maximum capacitance.

(5) Set the frequency of signal generator C to 30MHz and set the output level to 3.8 volts e.m.f.

(6) Adjust C33 until the multimeter indication changes from +1 or +2 volts to +12 volts.

(7) Reduce the output level from signal generator C to 1 volt e.m.f. Check that the indication on the electronic multimeter is approximately 0.5 volt.

(8) Slowly increase the output level from signal generator C until the electronic multimeter indication falls to zero. Check that the signal generator output level is between 2.5 and 4.0 volts e.m.f.

(9) Connect the multimeter, set to the 25V d.c. range, between the collector of TR3 (positive) and chassis (OV).

(10) Connect the electronic multimeter to TP1.

(11) Set the output level of signal generator C to 10 volts e.m.f.

(12) Adjust C31 until the multimeter indication changes from +1 or +2 volts to +12 volts.

(13) Reduce the output level from signal generator C to 1 volt e.m.f. Check that the indication on the electronic multimeter is approximately 0.5 volt.

(14) Slowly increase the output level from signal generator C until the electronic multimeter indication falls to zero. Check that the signal generator output level is between 7 and 14 volts e.m.f.

(15) Disconnect the multimeter.

Mute circuit

30. (1) Set the output level of signal generator C to 1 volt e.m.f.

(2) Check that the indication on the electronic multimeter (connected to TP1) is approximately 0.5 volt.

(3) Connect a wire link between the MUTE and E terminals of TS2. Check that the electronic multimeter indication falls to zero.

(4) Remove the wire link from the MUTE terminal and check that the electronic multimeter again indicates approximately 0.5 volt.

(5) Switch off and disconnect all test equipment.

(6) Replace the coaxial r.f. output connection to the chassis-mounted first-mixer input connector.

AFC BOARD PM369

31. (1) Set the POWER switch to OFF and remove LK1 on the a.f.c. board.

(2) Set the POWER switch to ON.

(3) Set the receiver controls as follows:-

(a) MHz to 3

(b) kHz to 500.00

(c) TUNING RATE to LOCK

(d) RF TUNE to WB

(e) AGC to OFF

(f) IF GAIN fully clockwise

(g) MODE to AM

(h) USB BANDWIDTH to 3

(j) AFC to OFF

(k) METER to TUNE CARRIER

(4) Connect the signal generator (Chap. 2-3, Table 1, Item 2) via the step attenuator (Item 18) to the receiver antenna (ANT) socket.

(5) Set the step attenuator to 0dB.

(6) Set the signal generator to a frequency of 3.5MHz and a c.w. output of 10 millivolts e.m.f. at the ANT socket.

(7) Tune the receiver to the signal generator and for a minimum indication on the front panel meter (the meter needle may 'beat' slowly).

(8) Set R50 and R87 (a.f.c. board) fully counter-clockwise.

(9) Connect the negative lead of the variable-voltage power supply to chassis (0V) and the positive lead, via a 10k resistor, to the LK1-connection furthest from the edge of the a.f.c. board.

(10) Connect the h.f. electronic voltmeter (high-impedance input) to TP10.

(11) Switch on and adjust the output of the variable-voltage power supply for an indication of 750 millivolts plus or minus 0.5dB on the h.f. electronic voltmeter.

(12) Set the AFC switch to PILOT CARRIER. Check that the AFC LOCK lamp glows.

(13) Connect the digital voltmeter between TP17 (positive) and chassis.

(14) Adjust R82 for a digital voltmeter indication of 1.54 volts plus or minus 100 millivolts.

(15) Connect the digital voltmeter between TP16 (positive) and chassis and check that it indicates 1.4 volts plus or minus 100 millivolts.

(16) Set the AFC switch to OFF. Tune the signal generator for a minimum indication on the front panel meter (the meter needle may 'beat' slowly).

(17) Set the AFC switch to PILOT CARRIER and adjust C3 until the front-panel meter indicates zero on the AFC scale. Check that the AFC LOCK lamp is glowing; if the lamp extinguishes,set the AFC switch to OFF and then to PILOT CARRIER.

(18) Set the receiver POWER switch to OFF. Switch off and disconnect the variable-voltage power supply.

(19) Set the receiver POWER switch to ON. Re-tune the receiver (kHz) to the signal generator frequency.

(20) Set the step attenuator to 80dB (receiver input level 1 microvolt e.m.f.).

(21) Set the AFC switch to FULL CARRIER.

(22) Adjust R50 for an indication on the h.f. electronic voltmeter (connected to TP10) of 750 millivolts plus or minus 100 millivolts.

(23) Check that the AFC LOCK lamp is glowing.

(24) Set the receiver POWER switch to OFF and refit link LK1 to the a.f.c. board.

(25) Set the AFC switch to OFF and the receiver POWER switch to ON.

(26) Set R97 fully counter-clockwise.

(27) Re-tune the receiver (kHz) to the signal generator frequency.

(28) Set the AFC switch to PILOT CARRIER and check that the AFC LOCK lamp is glowing.

(29) Set the step attenuator to 0dB, and set the signal generator output level to 1 microvolt e.m.f. at the ANT socket.

(30) Connect the digital voltmeter between TP16 (positive) and chassis.

(31) Check that the digital voltmeter indicates 1.45 volts plus or minus 30 millivolts. If the voltmeter indication exceeds 1.48 volts, adjust R50 for an indication of 1.45 volts.

(32) Adjust R97 for a digital voltmeter indication of 1.4 volts.

(33) Set the step attenuator to 5dB. Check that the h.f. electronic voltmeter (connected to TP10) indication falls by not less than 3dB.

(34) Set the signal generator output level to 20 millivolts e.m.f. and set the step attenuator to 80dB (receiver input level of 2 microvolts e.m.f.).

(35) Set the AFC switch to FULL CARRIER and check that the AFC LOCK lamp glows.

(36) Set the AGC switch to SHORT and the MODE switch to USB.

31. (37) Connect the digital voltmeter between the DIV AGC terminal on the rear panel (positive) and chassis.

(38) Adjust R97 for a digital voltmeter indication of 1.50 volts plus zero or minus 30 millivolts.

(39) Set the AFC switch to OFF and tune the signal generator to the receiver (upper sideband) for a minimum indication on the front panel meter.

(40) Set the step attenuator to 50dB (receiver input level of 64 microvolts e.m.f.) and record the DIV AGC level as indicated on the digital voltmeter.

(41) Set the MODE switch to LSB and transfer the digital voltmeter to the ISB DIV AGC terminal on the rear panel. Tune the signal generator to the receiver (lower sideband) and record the ISB DIV AGC level as indicated on the digital voltmeter. Set the MODE switch to USB and reconnect the digital voltmeter to the DIV AGC terminal on the rear panel.

(42) Tune the signal generator to the receiver for a minimum indication on the front panel meter. Set the AFC switch to FULL CARRIER and check that the AFC LOCK lamp glows.

(43) Adjust R50 for a digital voltmeter indication which is within plus or minus 30 millivolts of the lower of the two voltage readings recorded in operations (40) and (41).

(44) Set the step attenuator to 80dB (receiver input level of 2 microvolts e.m.f.).

(45) Re-adjust R97 for a digital voltmeter indication of 1.50 volts plus or minus 30 millivolts.

(46) Set the signal generator output level to 10 millivolts e.m.f. and set the step attenuator to 80dB (receiver input level of 1 microvolt e.m.f.).

(47) Set the AGC switch to OFF and set the MODE switch to USB+BFO. Check that the AFC LOCK lamp is glowing. If the lamp is not glowing, repeat operations (34) to (45) inclusive.

(48) Set the step attenuator to 76dB (receiver input level to 1.5 microvolts e.m.f.).

(49) Adjust R87 until the AFC LOCK lamp just extinguishes.

(50) Set the step attenuator to 80dB and check that the AFC LOCK lamp is completely extinguished.

(51) Set the signal generator output level to 20 millivolts e.m.f. (receiver input level of 2 microvolts e.m.f.) and check that the AFC LOCK lamp is fully glowing.

(52) Disconnect the lead to the receiver antenna socket and check that the AFC LOCK lamp extinguishes.

(53) After a period of approximately one minute, re-connect the lead to the antenna socket. Check that the AFC LOCK lamp glows.

(54) Set the signal generator output level to 10 millivolts e.m.f. (receiver input level of 1 microvolt e.m.f.).

(55) Note the h.f. electronic voltmeter indication (connected to TP10).

31. (56) Set the step attenuator to 0dB and check that the h.f. electronic voltmeter indication does not increase by more than 4dB.

(57) Set the step attenuator to 80dB and check that the h.f. electronic voltmeter indication equals that noted at operation (55) after a period of not less than ten seconds.

(58) Set the step attenuator to 60dB.

(59) Set the AFC switch to OFF.

(60) Set the signal generator frequency to 10Hz above the receiver frequency and check that the front panel meter indication beats at 5Hz.

(61) Continue to increase the signal generator frequency and check that the front panel meter indicates full scale deflection at approximately 200Hz above the receiver frequency.

(62) Set the AFC switch to FULL CARRIER. Check that the front-panel meter indication decreases to the zero mark on the AFC scale and that the AFC LOCK lamp is extinguished.

(63) Decrease the signal generator frequency towards the receiver frequency and check that AFC lock is achieved when the signal generator frequency is not less than 50Hz above the receiver frequency.

(64) Repeat operations (59) to (63) inclusive but with the signal generator tuned to frequencies below the receiver frequency.

(65) With the AFC LOCK lamp glowing, slowly tune the signal generator until the front-panel meter indicates the '-' mark on the AFC scale.

(66) Check that the signal generator frequency is lower than 3499 500Hz.

(67) With the AFC LOCK lamp glowing, slowly tune the signal generator until the front-panel meter indicates the '+' mark on the AFC scale.

(68) Check that the signal generator frequency is higher than 3500 500Hz.

(69) Switch off and disconnect all test equipment.

FINAL SETTING-UP PROCEDURE: I.F./A.F. BOARDS

Main i.f./a.f. board

32. (1) Connect the output of the signal generator (Chap. 2-3, Table 1, item 1) to the receiver antenna socket.

(2) Connect the wattmeter absorption, set to the 8-ohm range, between the LS and E terminals of TS1.

(3) Set the frequency of the signal generator to 1.02MHz and set the output level to 1 microvolt e.m.f.

(4) Set the AGC switch to OFF, the MODE switch to USB, the USB BANDWIDTH switch to 3 and the IF GAIN control fully clockwise.

(5) Using the h.f. electronic voltmeter, high-impedance input, monitor TP3 and adjust R9 for an indication of 200 millivolts r.m.s.

(6) Connect the multimeter, set to the 5V d.c. range, between board pin 29 (positive) and chassis. Check that the multimeter indicates 1.4 volts plus or minus 150 millivolts.

(7) Disconnect the multimeter and the h.f. electronic voltmeter.

(8) Set the AGC switch to SHORT and set the AF GAIN control fully clockwise. Check that the wattmeter indication is greater than 1 watt.

(9) Set the AF GAIN control for an indication of 100 millwatts on the wattmeter.

(10) Set the AGC switch to OFF and set the IF GAIN control to restore the wattmeter indication to 100 milliwatts.

(11) Detune the signal generator by at least 10kHz and check that the signal-plus-noise-to-noise ratio exceeds 15dB.

(12) Retune the signal generator to the receiver.

(13) Transfer the wattmeter, set to the 600 ohms range, to the LINE OUTPUT MAIN IF terminals of TS1.

(14) Set the front-panel METER switch to AM/USB.

(15) Adjust the AM/USB LINE LEVEL control for an output of 1 milliwatt on the front-panel meter. Check that the wattmeter indication is 1 milliwatt plus or minus 1dB.

(16) Set the AGC switch to SHORT.

(17) Increase the output level of the signal generator, in 1dB steps, until the AGC knee is reached, i.e. where a further increase in the signal generator output level does not result in an increase in audio power output. Ensure that the signal generator output level is less than 1.7 microvolts e.m.f.

(18) Set the signal generator output level 2 microvolts e.m.f.

(19) Adjust the AM/USB LINE LEVEL control for a convenient reference level on the wattmeter.

(20) Increase the output level of the signal generator by 100dB above 2 microvolts.

(21) Ensure that the increase in the output power level is not greater than 5dB relative to the reference level established at operation (19).

(22) Set the AGC switch to LONG and repeat operations (18) to (21) inclusive.

(23) Set the AGC switch to SHORT and the METER switch to RF.

(24) Set the signal generator output level to 2 microvolts e.m.f.

(25) Tune the signal generator to the receiver.

(26) Adjust R17, on the meter switching board, for an indication of 0dB on the front-panel meter.

(27) Increase the output level of the signal generator by 100dB above 2 microvolts.

(28) Adjust R14 on the meter switching board for an indication of 100dB on the front-panel meter.

(29) Repeat operations (24) to (28) for optimum results.

I.S.B. i.f./a.f. board

33. (1) Connect the output of the signal generator (Chap. 2-3, Table 1, item 1) to the receiver antenna socket.

(2) Connect the wattmeter absorption, set to the 8 ohms range, between the LS and E terminals of TS1.

(3) Set the frequency of the signal generator to 1.02MHz and set the output level to 1 microvolt e.m.f.

33. (4) Set the AGC switch to OFF, the MODE switch to ISB-L and the IF GAIN control fully clockwise.

(5) Using the h.f. electronic voltmeter, high-impedance input, monitor TP3 and adjust R9 for an indication of 200 millivolts r.m.s.

(6) Connect the multimeter, set to the 5V d.c. range, between board pin 29 (positive) and chassis. Check that the multimeter indicates 1.4. volts plus or minus 150 millivolts.

(7) Disconnect the multimeter and the h.f. electronic voltmeter.

(8) Set the AGC switch to SHORT and set the AF GAIN control fully clockwise. Check that the wattmeter indication is greater than 1 watt.

(9) Set the AF GAIN control for an indication of 100 milliwatts on the wattmeter.

(10) Set the AGC switch to OFF and set the IF GAIN control to restore the wattmeter indication to 100 milliwatts.

(11) Detune the signal generator by at least 10kHz and ensure that the signal-plus-noise-to-noise ratio exceeds 15dB.

(12) Retune the signal generator to the receiver.

(13) Transfer the wattmeter, set to the 600-ohm range, to the ISB LINE OUTPUT terminals of TS1.

(14) Set the front-panel METER switch to LSB.

(15) Adjust the LSB LINE LEVEL control for an output of 1 milliwatt on the front-panel meter. Check that the wattmeter indication is 1 milliwatt plus or minus 1dB.

(16) Set the AGC switch to SHORT.

(17) Increase the output of the signal generator, in 1dB steps, until the AGC knee is reached, i.e. where a further increase in the signal generator output level does not result in an increase in audio power output. Ensure that the signal generator output level is less than 1.7 microvolts e.m.f.

(18) Set the signal generator output level to 2 microvolts e.m.f.

(19) Adjust the LSB LINE LEVEL control for a convenient reference level on the wattmeter.

(20) Increase the output level of the signal generator by 100dB above 2 microvolts.

(21) Check that the increase in the output level is not greater than 5dB relative to the reference level established at operation (19).

(22) Set the AGC switch to LONG and repeat operations (18) to (21) inclusive.

MODE AND FILTER SWITCHES

34. (1) Connect the wattmeter absorption, set to the 8-ohm range, between the LS and E terminals of TS1.

(2) Set the receiver controls as follows:

(a) MHz to 3
(b) kHz to 020.000
(c) TUNING RATE to LOCK
(d) RF TUNE to WB
(e) AGC to SHORT and AFC to OFF

(f) IF GAIN fully clockwise
(g) LS to ON
(h) USB BANDWIDTH to 3

(3) Connect the output of the signal generator (Chap. 2-3, Table 1, item 1) to the receiver antenna socket. Set the signal generator frequency to 3MHz and set the output level to 10 microvolts e.m.f.

(4) Set the MODE switch to LSB and, in turn, to ISB-L. Tune the signal generator from 3.00 to 3.05MHz on each mode. Check that, at 3.02MHz, a high note is heard in the loudspeaker which reduces in pitch to zero beat and then disappears.

(5) Set the MODE switch to USB and, in turn, to ISB-U. Tune the signal generator from 3.05 to 3.00MHz on each mode. Check that, at 3.02MHz, a high note is heard in the loudspeaker which reduces in pitch to zero beat and then disappears.

(6) Tune the signal generator to 3.021MHz; a 1kHz tone should be heard in the loudspeaker.

(7) Set the USB BANDWIDTH switch to 0.4-1.6; the 1kHz tone should remain at the same level, but the noise should decrease in level.

(8) Set the USB BANDWIDTH switch to 0.8-1.2; again the 1kHz tone should remain at the same level but a further decrease in noise level should occur.

(9) Set the LS switch to OFF.

(10) Set the MODE switch to USB+BFO.

(11) Turn the receiver onto its side and connect the digital frequency meter between pins 11 and 32 (OV) on the 34MHz generator board PM339.

(12) Set the front-panel BFO control to '-'.

(13) Adjust L4 on the 34MHz generator board until the frequency displayed on the digital frequency meter is 1 395 500Hz plus or minus 100Hz.

(14) Set the BFO control to '+'.

(15) Adjust R4 on the 34MHz generator board until the frequency displayed on the digital frequency meter is 1 402 500Hz plus or minus 100Hz.

(16) Repeat operations (12) to (15) inclusive until no further improvement can be obtained.

(17) Disconnect the digital frequency meter.

(18) Set the LS switch to ON; a tone should be heard.

(19) Set the USB BANDWIDTH switch to 3.

(20) Check that the audible tone changes pitch as the BFO control setting is altered; a zero beat note should occur at '0' approximately on the BFO control scale.

(21) Set the MODE switch to AM.

(22) Set the signal generator frequency to 3.020MHz.

(23) Set the signal generator for 70 per cent amplitude modulation at 400H:

(24) Tune the signal generator to the receiver and check that a 400Hz tone can be heard in the loudspeaker.

(25) Switch off and disconnect all test equipment.

DIVERSITY A.G.C. ADJUSTMENTS

35. Receivers leaving the factory are set up for optimum performance such that two receivers may be interconnected for diversity reception without the need of further adjustment. To ensure continued optimum performance, however, it may be necessary to periodically adjust the diversity a.g.c. output level (particularly after repair or re-alignment) in accordance with the following procedure.

36. (1) Set the receiver controls as follows:

(a) MHz to 5
(b) kHz to 200.00
(c) TUNING RATE to LOCK
(d) RF TUNE to WB
(e) AGC to SHORT
(f) MODE to USB
(g) USB BANDWIDTH to 3
(h) AFC to OFF

(2) Connect the output of the signal generator (Chap. 2-3, Table 1, Item 2), set to a frequency of 5.2MHz and output level of 20 millivolts e.m.f., via the step attenuator to the receiver antenna socket.

(3) Set the step attenuator to 80dB (receiver input level of 2 microvolts e.m.f.).

(4) Connect the digital voltmeter between the DIV AGC (positive) and E terminals of TS2 on the receiver rear panel.

Main i.f./a.f. board

37. (1) Raise the main i.f./a.f. board and secure in the vertical position.

(2) Tune the signal generator for a maximum indication on the digital voltmeter.

(3) Adjust R4 on the main i.f./a.f. board for an indication of 1.50 volts plus or minus 30 millivolts on the digital voltmeter.

(4) Set the step attenuator to 50dB (receiver input level of 64 microvolts e.m.f.) and record the level indicated on the digital voltmeter.

(5) Reset the step attenuator to 80dB.

(6) Replace the main i.f./a.f. board.

I.S.B. i.f./a.f. board

38. (1) Transfer the digital voltmeter to the ISB DIV AGC (positive) and E terminals of TS2 on the receiver rear panel.

(2) Set the MODE switch to LSB.

(3) Raise the i.s.b. i.f./a.f. board and secure in the vertical position.

(4) Tune the signal generator for a maximum indication on the digital voltmeter.

(5) Adjust R4 on the board for an indication of 1.50 volts plus or minus 30 millivolts on the digital voltmeter.

(6) Set the step attenuator to 50dB (receiver input level of 64 microvolts e.m.f.) and record the level indicated on the digital voltmeter.

(7) Reset the step attenuator to 80dB.

(8) Replace the board.

A.F.C. board

39. (1) Connect the digital voltmeter between the DIV AGC (positive) and E terminals of TS2 on the receiver rear panel.

(2) Set the MODE switch to USB and the METER switch to TUNE CARRIER.

(3) Raise the a.f.c. board and secure in the vertical position.

(4) Tune the signal generator for a maximum indication on the front panel meter.

(5) Set the AFC switch to FULL CARRIER and check that the AFC LOCK lamp glows.

(6) Adjust R97 on the a.f.c. board for an indication of 1.50 volts plus or minus 30 millivolts on the digital voltmeter.

(7) Set the step attenuator to 50dB (receiver input level of 64 microvolts e.m.f.) and check that the AFC LOCK lamp is glowing; slightly adjust the signal generator tuning, if required, to achieve a.f.c. lock.

(8) Adjust R50 on the board for a digital voltmeter indication which is within plus or minus 30 millivolts of the lower of the two voltage readings recorded at operations 37(4) and 38(6).

(9) Set the step attenuator to 80dB and check that the AFC LOCK lamp is glowing.

(10) Repeat operations (6) to (9) inclusive until no further improvement can be obtained.

(11) Replace the board.

R.F. meter calibration

40. (1) Set the AFC switch to OFF and the METER switch to RF.

(2) With the step attenuator set to 80dB (receiver input level of 2 microvolts e.m.f.), tune the signal generator for a maximum indication on the digital voltmeter (connected to the DIV AGC terminal).

(3) Ensure that the digital voltmeter indicates 1.50 volts plus or minus 30 millivolts.

(4) Adjust R17 on the meter switching board (nearest edge of board) for a reading of 0dB on the front panel meter.

(5) Set the step attenuator to 0dB and increase the signal generator output level to 200 millivolts e.m.f. (receiver input level of 2 microvolts plus 100dB).

(6) Adjust R14 on the meter switching board (near centre of board) for a reading of 100dB on the front panel meter.

(7) Switch off and disconnect all test equipment.

► A.F.C. BOARD PM664

41 Set the receiver controls as follows:

41.1 RF TUNE to WB.

41.2 AGC to SHORT.

41.3 MODE to CW.

41.4 MHz to 1.

41.5 KHz to 020.00

41.6 USB BANDWIDTH to 3.

41.7 AFC to OFF.

41.8 METER to TUNE CARRIER.

41.9 POWER to ON.

42

42.1 Remove the bookcase cover and stand the a.f.c. board vertically.

42.2 Unsolder the coaxial lead connected to pin 16, leaving the screen connected to pin 15.

42.3 Connect the digital voltmeter between TP17 and earth. Adjust C35 for a reading of 7.0 V ± 0.1 V. Ensure that the digital voltmeter reading changes as C35 is adjusted.

42.4 Measure the voltage between TP17 and TP18 with the digital voltmeter, and ensure that the reading is less than 50 mV.

42.5 Set the potentiometers as follows:-

(a) R5 - fully clockwise

(b) R34 - mid position

(c) R37 - fully clockwise

(d) R41 - fully counter-clockwise

(e) R45 - fully clockwise

42.6 Connect the electronic voltmeter to TP4; set to 3 V a.c. range. Adjust R29 for a minimum reading, increasing the sensitivity of the electronic voltmeter as necessary.

42.7 Set the electronic voltmeter, connected to TP4, to the 1 V range. Connect the signal generator to pin 16.

42.8 Set the frequency of the signal generator to 1.400 MHz ± 20 Hz and at an output level of 60 µV p.d.

42.9 Connect a temporary link between pin 14 and earth. Adjust L4 for a maximum indication on the electronic voltmeter and then set R34 for an indication of 800 mV ±100 mV. Remove the temporary link from pin 14.

42.10 Increase the signal generator output level to 90 µV p.d. Adjust R5 in a counter-clockwise direction until the signal level at TP4, as indicated on the electronic voltmeter, decreases by 1 dB. ◄

► 42

42.11 Increase the signal generator output level by 3 dB and note the electronic voltmeter indication.

42.12 Increase the signal generator output level by 60 dB. Ensure that the increase in the level at TP4 does not increase by more than 3.5 dB above the indication noted in operation 42.11.

42.13 Connect the electronic voltmeter to TP5 and adjust T1 for a maximum indication on the electronic voltmeter. Ignore any slow beat of the meter needle.

42.14 Observe the tuning meter and ensure that a beat is seen which is equal to the difference between the input signal and 1.400 MHz.

42.15 Reconnect the coaxial lead to pin 16. Connect the signal generator to the receiver antenna socket. Set the output level to 10 μV e.m.f. and tune it to the receiver passband.

42.16 Measure and note the a.g.c. voltage at pin 4 of the a.f.c. board using the digital voltmeter.

42.17 Increase the signal generator output by 30 dB (i.e. to 300 μV e.m.f.). Measure and note the a.g.c. voltage at pin 4 of the a.f.c. board.

42.18 Tune the signal generator for zero beat on the time carrier meter. Switch AFC to FULL CARRIER and ensure lock lamp glows after a few seconds. Set the signal generator output to 1 mV e.m.f.

42.19 Measure the voltage at TP2 on the a.f.c. board using the digital voltmeter. Adjust R41 until the voltage is within 10 mV of that noted in operation 42.16.

42.20 Reduce the signal generator output by 30 dB (i.e. to 30 μV e.m.f.). Adjust R37 until the voltage at TP2 is within 10 mV of that noted in operation 42.16.

42.21 Repeat operations 42.19 and 20 until no further improvement can be obtained.

42.22 Set AFC to OFF. Set the signal generator level to 10 μV e.m.f. Set MODE to USB and tune the signal generator to the receiver passband. Measure and note the voltage on the DIV AGC terminal on the rear panel with the digital voltmeter.

42.23 Set MODE to CW and BANDWIDTH to 3 kHz. Tune the signal generator for zero beat on the tune carrier meter. Switch the AFC to FULL CARRIER and ensure LOCK LAMP glows after a few seconds. Increase the signal generator output until the voltage on the DIV AGC terminal is the same as that noted in operation 42.22. Note the increase in signal generator output level which should be 10 dB ±5 dB. If this is incorrect, repeat operations 42.15 to 23.

42.24 Set AFC to OFF, MODE to USB. Repeat operations 42.22 and 23 for a signal generator output of 300 μV e.m.f.

42.25 Set AFC to OFF. Tune the signal generator for zero beat on the tune carrier meter. Set the output level to 2 μV e.m.f. Set AFC to FULL CARRIER and ensure that the LOCK LAMP glows after a few seconds. Adjust R45 until the LOCK LAMP starts to flicker.

42.26 Ensure LOCK lamp is definitely glowing at 3 μV e.m.f. input. ◄

Chapter 2-6

FAULT DIAGNOSIS

CONTENTS

Para.
1 Introduction
3 Fault-location tables
4 Use of tables
7 Typical voltage/signal levels
8 Low-frequency loop board PM588
9 Upper loop board PM589
10 Transfer loop board PS338
11 High-frequency loop board PS337
12 34 MHz generator board PM339
13 Main and i.s.b. i.f./a.f. boards PM364
14 Second mixer board PM336
15 First mixer board PM335
16 A.F.C. board PM369
17 Power supplies
► 18 Fault location: a.f.c. board PM664

Fig. Page
1 Waveforms: a.f.c. board PM664 77
2 Waveforms: a.f.c. board PM664 ... ... 78 ◄

Table Page
1 Fault-location : overall receiver (sub-assembly level) 11
2 Fault-location : synthesizer level (sub-assembly level) ... 24
3 Fault-location : l.f. loop PM588 and upper loop PM589 27
4 Fault-location : h.f. loop PS337 and transfer loop PS338 ... 32
5 Fault-location : 34 MHz generator PM339 37
6 Fault-location : main i.f./a.f. board PM364/1 43
7 Fault-location : i.s.b. i.f./a.f. board PM364/3 47
8 Fault-location : first mixer PM335 and second mixer PM336 ... 51
9 Fault-location : r.f. board PM582 55
10 Fault-location : display board PM371 58
11 Fault-location : a.f.c. board PM369 61
12 Fault-location : main power supply and regulator PM370 ... 68

INTRODUCTION

1 This chapter provides information to assist in the location of a fault to sub-assembly and component level. The information is presented in the form of Tables and these are supplemented with typical voltage and/or signal levels for the main printed-circuit boards. Following repair work, ensure that screening covers are replaced using all the screws provided (Chap.2-2).

2 Throughout the following procedures, the switch on the 12 V battery module (when fitted) should be set to OFF; however, should it be necessary to switch off the receiver, upon switching on again the kHz part of the tuned frequency will have to be reset.

FAULT-LOCATION TABLES

3 A Table consists of a number of logical steps, to check for the correct operation of a sub-assembly, where the route taken through the Table is

dependent upon the result of each step. Since this method of fault diagnosis, in general, will localise only one fault at a time, once a fault has been diagnosed and rectified, the Table in use should be recommenced at step 1 and followed through until no further fault is apparent.

Use of tables

4. Where the faulty area is completely unknown, reference should be made initially to Table 1 for the overall receiver. This Table isolates the fault either to a chassis-mounted component or to a printed-circuit board (or group of boards) in which case reference should be made to the Table for that board (or group of boards).

5. Where the likely area of a fault is known, direct reference may be made to the respective Table for that area. It must be noted, however, that certain Tables assume correct operation of associated boards. For example, Table 8 for the two mixer boards assumes that the main i.f./a.f. board is functioning correctly.

6. A list of the Tables is given on page 1.

TYPICAL VOLTAGE/SIGNAL LEVELS

7. Typical voltage and/or signal levels at test (and other) points on the main printed-circuit boards are given below. Frequency measurements are to an accuracy of plus or minus 10Hz (max.) unless otherwise stated.

Low-frequency loop board PM588

8. (1) The test-point signal levels listed below were measured with the kHz portion of the receiver frequency set to 000.00 and the TUNING RATE switch set to LOCK. Ensure that the 1MHz, 34MHz and LO INT/EXT switches on the rear panel are all set to INT. Set the MHz switch to 1.

TP1: +15V d.c. measured with multimeter (negative to 0V).

(2) The following test-point signals were measured using the oscilloscope:-

TP2: 7MHz square wave, 3.5V p-p.
TP3: 1MHz square wave, approximate 1:1 mark/space ratio, 3.5V p-p.
TP4: 1kpps, positive-going, 3.5V p-p.
TP5: 1kpps, positive-going, 3.5V p-p.
TP6: 1kpps, negative-going strobe pulse, 3.5V p-p.
TP7: 13 to 20kHz, square wave, 3.5V p-p.
TP8: 13 to 20kpps, negative-going strobe pulse, 3.5V p-p.

Board pin 46: 1MHz, 1.5V p-p.

Board pin 44: 1.01545MHz, 2.2V p-p.

Junction C26/L3: 15.45kHz, 5.2V p-p.

Emitter TR19: 15.45kHz, less than 0.8V to greater than 1.6V p-p, sine wave.

Board pin 1: logic '0' in-lock; logic '1' out-of-lock.

Board pin 42: logic '0' in-lock; logic '1' out-of-lock.

(3) The following d.c. voltages are measured using the multimeter (negative to 0V):-

Junction R55/R56: +4.7V

ML14 pin 5: +2V

Upper loop board PM589

9. (1) The following test-point signals are measured using the oscilloscope:-

TP1: 1.01545MHz square wave, 3.5V p-p.
TP2: 4.6MHz, square wave, 3.5V p-p.
TP3: 10.154kpps, positive-going, 3.5V p-p.
TP4: 10.154kpps, strobe pulse, negative-going, 3.5V p-p.
TP5 and TP6: phase-comparator output pulses, positive-going and in-phase, 3.5V p-p.

Board pin 9: 1.01545MHz, 2.2V p-p.

ML4 pin 11: 101.54kHz, 3.5V p-p.

Board pin 2: 4.6MHz, 800mV p-p.

ML7 pin 8: 10.154kpps, 3.5V p-p.

Board pin 12: logic '1' in-lock, logic '0' out-of-lock.

Board pin 11: normally logic '1'; pulses to logic '0', approximately 25mS, for range blanking when tuning past a 10kHz digit change.

(2) The following d.c. voltage measurements are made using the multimeter (negative to 0V):-

Board pin 7: +6.5V.

Emitter TR1: +5V ± 0.5V.

TP7: +15V.

Transfer loop board PS338

10. (1) The following signal levels were measured using the oscilloscope:-

TP1: 4.6MHz square wave, 5V p-p.
TP2: 112.195kHz square wave, 3.5V p-p.
TP3: 112.195kpps, negative-going, 3.5V p-p.
TP4 and TP5: 112.195kpps, 1.5 microsecond negative going, and in phase, 3.5V p-p.
TP6: 115 to 52kpps strobe pulse, negative going, 3.5V p-p.

Board pin 21: 1MHz, 750mV p-p.

Collector TR2: 1MHz, 500mV p-p.

Junction C2/R6: 887.805kHz, 1V p-p.

ML3 pin 4: 887.805kHz, 1V p-p.

Board pin 17: 4.6MHz, 800mV p-p.

Junction C35/L11: 400mV p-p.

Board pin 6: logic '1' in-lock; logic '0' out-of-lock.

(2) The following d.c. voltages were measured using the multimeter (negative to 0V):-

Junction D4/R24: +12V ± 1V.

High-frequency loop board PS337

11. (1) Use a multimeter, set to the 30V d.c. range, to monitor TP1, TP2 and TP3 (negative to 0V):-

TP1: MHz switch set to 7MHz, +14V ± 1V.
TP2: MHz switch set to 17MHz, +14V ± 1V.
TP3: MHz switch set to 27MHz, +14V ± 1V.

(2) Set the MHz switch to 27. Use the multimeter to measure the following voltages with respect to chassis (0V). Observe correct polarity. (Ensure LO, 34MHz and 1MHz switches are set to INT).

Emitter TR9: -0.7V d.c.

Base TR10: +2.4V d.c.

Emitter TR10: +2.0V d.c.

Junction D16/R55: +7.5V d.c.

Junction D17/R56: +3.3V d.c.

Junction D16/D18: +8.2V d.c.

Junction D17/D18: +4.0V d.c.

(3) Use the oscilloscope to monitor the collector of TR9:-

Collector TR9: 62.5MHz, 75mV p-p.

(4) Set the kHz control to display 999.99. Set the TUNING RATE switch to LOCK. Monitor TP4 using the h.f. electronic voltmeter, high-impedance input. Step the MHz switch through each position and check that the h.f. electronic voltmeter indication is as below:-

TP4: 1V r.m.s. $\pm$ 2.5dB.

(5) Use the oscilloscope to monitor the test-points listed below. Check that the signal levels displayed approximate to those indicated:-

TP5: 3.5V p-p.

TP6: 473kpps strobe pulses, negative-going, 3.5V p-p.

TP7 and TP8: 473kpps phase-comparator output pulses, negative-going and in-phase, 3.5V p-p.

(6) Connect the multimeter, set to the 10V d.c. range, between TP10 (positive) and chassis (0V):-

TP10: +3.5V d.c.

(7) Use the oscilloscope to monitor the following:-

TP12: 947kHz, approximate square wave, 2.8V p-p.

ML12, pin 5: half of transfer oscillator frequency, 3.5V p-p.

Board pin 13: 947kHz, 1V p-p.

Board pin 12: logic '1' in-lock; logic '0' out-of-lock.

34MHz generator board PM339

12. TP1: multimeter, +7V d.c.

TP2: 5Mpps, oscilloscope, 3V p-p.

TP3: 1MHz, square wave, 2:3 mark/space ratio, oscilloscope, 2V p-p.

TP4: 34MHz v.c.o. output, oscilloscope, approximately 3.5V p-p.

TP5: 34MHz, h.f. electronic voltmeter, high-impedance input, 400mV r.m.s.

TP6: 34MHz, h.f. electronic voltmeter, high-impedance input, 1.4V r.m.s.

TP7: 200kHz square wave, 3:2 mark/space ratio, oscilloscope, 3.5V p-p.

TP8: h.f. electronic voltmeter, high-impedance input, 1.4V r.m.s.

TP9: 1 MHz square wave, oscilloscope, 3.5V p-p.

TP10: not fitted.

TP11: AFC at OFF, 1MHz square wave, 3:2 mark/space ratio, oscilloscope, 3.5V p-p.

TP12: MODE switch to USB, 1MHz square wave, 3:2 mark/space ratio, oscilloscope, 3.5V p-p.

TP14: 1Mpps, negative-going, oscilloscope, 3.5V p-p.

TP15: oscilloscope, 400mV p-p.

Board pin 27: 5MHz, oscilloscope, 400mV p-p.

Base TR2: multimeter, +1.8V d.c.

Collector TR2: 5MHz, oscilloscope, 400mV p-p.

Collector TR9: 1MHz sine wave, oscilloscope, 1V p-p.

Board pin 4: 180mV p.d. loaded with 50-ohm load; 2V p-p not loaded.

Collector TR13: 1MHz, oscilloscope, 3.5V p-p.

Collector TR15: multimeter, +1.5V d.c.

Board pin 6: 1MHz, oscilloscope, 3.5V p-p.

Board pin 8: 1MHz, oscilloscope, 3.5V p-p.

Board pins 10 and 11: 1.4MHz, oscilloscope, 700mV p-p.

Note: Ensure 34MHz switch is set to INT.

Emitter TR1: multimeter, +5V d.c.

Junction D6/R27: multimeter, +5.1V d.c.

Junction D5/R25: multimeter, +8.5V d.c.

Junction D6/D7: multimeter, +5.8V d.c.

Junction D5/D7: multimeter, +9.2V d.c.

Base TR11: multimeter, 2.8V d.c.

Board pin 20: 34MHz, h.f. electronic voltmeter, high-impednance input 1V r.m.s.

Main and i.s.b. i.f./a.f. boards PM364

13. The typical signal levels listed below are measured under the following test conditions unless stated otherwise:-

(1) Signal generator (Chap.2-3, Table 1, item 1), frequency 1.4MHz, output level set for 200 millivolts e.m.f. at TP3 (signal generator output level should not exceed 100 microvolts e.m.f.), connected to the r.f. input, pins 34 and 35 (filter board output open-circuit).

(2) Receiver front-panel controls set as follows (USB BANDWIDTH at 3):-

(a) MODE: USB for main i.f./a.f. board.
LSB for i.s.b. i.f./a.f. board.

(b) AGC: OFF.

(c) IF GAIN: fully clockwise.

(3) Measurements at TP2, TP3 and TP4 are made using the h.f. electronic voltmeter, high input impedance:-

TP2: 100 millivolts r.m.s.

TP3: 200 millivolts r.m.s.

TP4: Between 90 and 130 millivolts r.m.s.

(4) Measurements at TP7, pins 8/9 and TP6 are made using the electronic multimeter (Chap.2-3, Table 1, item 13):-

TP7: Between 50 and 90 millivolts r.m.s.

Pins 8 and 9: Not less than 150 millivolts, typically between 170 and 250 millivolts r.m.s.

TP6: Signal generator output increased by 10dB, amplitude modulated 30 per cent at 1kHz: between 50 and 90 millivolts r.m.s.

(5) Disconnect the signal generator and use the multimeter to measure the following voltages (d.c.) with respect to chassis. Observe correct polarity:-

TP5: +0.25V

ML1 pin 1: +4.2V

ML1 pin 2: +4.2V

ML1 pin 6: +3.5V

ML1 pin 7: +11.5V

ML1 pin 8: +11.5V

ML1 pin 9: 0V

ML1 pin 10: +4.2V

ML1 pin 11: +11.5V

ML1 pin 12: +10V

ML1 pin 13: +6.5V

ML1 pin 14: +4.2V

Board pin 1: +5V

Base TR4: +0.6V

Base TR6: +6V

Emitter TR6: +5.4V

Junction C36/D10: AM; +4V
SSB; +3.3V

Junction C37/D11: AM; +3.5V
SSB; +4V

voltmeter sensitivity
20 000 ohms-per-volt

Emitter TR14: +2V

Emitter TR15: +1.4V

Collector TR15: +3V

Junction R33/R34: +0.5V ± 0.6V

Junction R32/R34: -0.5V ± 0.6V

Junction C45/R74: +7.25V

ML5 pin 3: +7.25V

ML5 pin 2: +7.25V

ML5 pin 6: +7.25V

Base TR22: +7.75V

Base TR23: +6.8V

Junction R93/R94: +7.25V

(6) The following d.c. measurements apply to the main i.f./a.f. board only (loudspeaker amplifier), with no signal present.

Junction C42/R69: +5.6V

Junction R65/R66: +12.5V

Junction R69/R72: +5.5V

Base TR17: +5.4V

Collector TR18: +6.4V

TP10: +7.1V

Second mixer board PM336

14. (1) The following measurements are made using the h.f. electronic voltmeter, high-impedance input. Connect the signal generator, set to a frequency of 35.400MHz and a c.w. output level of 20mV e.m.f., 50 ohms impedance, to the T3 side of link LK1 on the first mixer board PM335, with the link removed. Set the 34MHz INT/EXT switch to EXT, the MODE switch to USB and the AGC switch to OFF. Connect the multimeter, set to the 10V d.c. range, between board pin 9 and chassis (0V). Set the IF GAIN control for an indication on the multimeter of +2.25V.

Junction C1/R2: 35.4MHz input, 12mV r.m.s.

Junction C6/R3: 45mV r.m.s.

Junction D1/D2: 45mV r.m.s.

TP1: 100mV r.m.s.

LK1: 60mV r.m.s., using TP2 as earth connection.

(2) The following voltages (d.c.) are measured using the multimeter, with respect to chassis (0V). Observe correct polarity:-

Collector TR2: +11.5V

Junction R7/R8: +3V

Emitter TR6: +2.4V

Emitter TR7/TR8: +1.65V

Base TR5: -5.5V

Junction L6/R5: +8.5V

(3) The following measurements are made using the h.f. electronic voltmeter, high-impedance input, with the 34MHz INT/ENT switch set to INT:-

Board pin 7: 34MHz input, 1V r.m.s.

Between LK2 and TP2 (earth): 600mV r.m.s.

First mixer board PM335

15. (1) Set the MHz switch to 27MHz. The following measurements are made using a high input impedance, 65MHz oscilloscope:-

Board pin 10: 62.4MHz, 750mV p-p.

TP1: 750mV p-p.

TP4: 600mV p-p.

TP5: 400mV p-p.

TP6: 2V p-p.

Board pin 26: 20V p-p.

(2) The following voltages (d.c.) are measured using the multimeter, with respect to chassis (OV), with the MHz switch set to 27MHz.

Junction R3/R4:	+2V
Board pin 8:	+0.6V
Junction R1/R2:	+8.5V
TP2:	+11V
Base TR1:	-3.7V
Junction R20/R21:	-4.7V
Collector TR1:	+11.5V
TP6:	-2V
Junction R29/R30:	-7V
Base TR5:	-2V

A.F.C. board PM369

16. (1) Connect a signal generator (Chap. 2-3, Table 1, Item 1) set to a frequency of 3.5MHz and a c.w. output level of 10mV e.m.f., to the receiver antenna socket. Set the MODE switch to USB, AFC switch to OFF, IF GAIN fully clockwise, and the METER switch to TUNE CARRIER. Set the receiver frequency to 3.5MHz and tune the signal generator to the receiver for a minimum indication on the front-panel meter (the meter indication may beat slowly as the minimum is reached).

(2) The following measurements are made, using the oscilloscope, with the AFC switch set to FULL CARRIER and the AFC LOCK lamp glowing.

Board pin 16:	1.4MHz i.f. input, 40mV p-p.
ML3 pin 14:	40mV p-p.
ML3 pin 12:	40mV p-p.
Junction R36/T1:	40mV p-p.
Board pin 11:	1MHz input, 1.5V p-p.
TP4:	1V p-p.
TP8:	1.6MHz, 3.5V p-p.
ML8 pin 5:	400kHz, 3.5V p-p.
Base TR10:	400kHz, 2.6V p-p.
Collector TR14:) Collector TR16:)	400kHz, positive-going pulses, approximately 10V p-p.
ML1 pin 11:	Logic '1'.
ML1 pin 3:	Logic '0'.

ML5 pin 5:	200kHz)	
ML6 pin 12:	25kHz)	
ML5 pin 6:	1MHz)	3.5V p-p (approx.)
ML5 pin 12:	200kHz)	
ML7 pin 12:	25kHz)	

16. (2)
(Contd)

ML9 pin 5:)) ML9 pin 9:)	Very narrow, positive-going pulses, at 25kpps.
ML20 pins 1,2,5 & 4:	Logic '1'.
ML20 pin 6:	Logic '0'.
TP6 & TP7:	25kHz, approximately 3.5V p-p.

(3) The following voltages (d.c.) are measured using the multimeter, with respect to chassis, with the AFC switch set to FULL CARRIER and the AFC LOCK lamp glowing.

ML3 pin 7:	+10.5V
Base TR5:	+1.5V (oscilloscope, 1MHz, 1.5V p-p).
Base TR6:	+1.5V
TP4:	+8.5V (oscilloscope, 1MHz square wave, 1V p-p).
ML12 pin 13:	+5.8V
ML12 pin 6:	+2.4V
ML12 pin 8:	+7.6V
Junction R50/R51:	+0.5V
Junction R49/R50:	+3.0V
Junction R59/R64:	+9.5V
Junction R79/R80:	+4.5V
Junction R77/R82:	+16.5V
Junction R82/R88:	+11V
Base TR9:	+3.0V

(4) The following measurements are made using the oscilloscope with the AFC switch set to OFF.

ML6 pin 1:	logic '0'
ML6 pin 12:	logic '1'
ML1 pin 6:	1MHz, 3.5V p-p.
ML7 pin 12:	logic '1'
ML5 pin 12:	200kHz, approximately 3.5V p-p.
ML5 pin 5:	200kHz, approximately 3.5V p-p.
TP6:	1MHz, approximately 3.5V p-p.
TP7:	1MHz, approximately 3.5V p-p.

Power supplies

17. The following voltages (d.c.) are measured using the multimeter, with respect to chassis (OV), unless otherwise stated:-

ML4 pins 7 and 8:	+28V
ML4 pin 4:	+7.15V ± 0.5V
ML4 pin 3:	+7.15V ± 0.5V
ML4 pin 2:	+7.15V ± 0.5V
Board pins 22 and 23:	+20V output
Board pin 14:	+23V
ML3 pin 4:	+7.15V ± 0.5V
ML3 pin 3:	+7.15V ± 0.5V
ML3 pins 7 and 8:	+20V
ML3 pin 6:	+14.5V
ML3 pin 2:	+7.15V ± 0.5V
Board pins 16, 17 and 18:	+12V output
Board pin 8:	+14V
ML2 pin 4:	+7.15V ± 0.5V
ML2 pin 3:	+5V
ML2 pins 7 and 8:	+20V
ML2 pin 6:	+8V
Board pins 10 and 12:	+5V output
Board pins 1 and 47:	+10V
ML1 pin 4:	+7.15V ± 0.5V relative to board pin 5
ML1 pins 7 and 8:	+12V
Board pins 5 and 6:	-7V output
Between board pins 25 (positive) and 27:	+85V
Between board pins 26 (negative) and 27:	-85V

TABLE 1

Fault-location : overall receiver (sub-assembly level)

Note: This Table gives a fault-finding procedure with the receiver in the s.s.b mode; the relevant steps should be repeated for the l.s.b. channel (i.s.b mode).

STEP 1	Set the RF TUNE control to WB, AGC and AFC to OFF, the TUNING RATE switch to LOCK and the MODE switch to USB. Set the rear panel 1MHz, 34MHz and LO switches to INT. Ensure that no antenna is connected to the antenna socket, and that the voltage selector on the rear panel is correctly set. Connect the receiver to a suitable source of a.c. power and set the POWER switch to ON. Set the front-panel METER switch, in turn, to +20, +12, +5 and -7. Does the meter indicate within the green sector of the meter scale at each switch position?
Action	YES: Step 2. NO: Step 41.
STEP 2	Is the MHz display window illuminated?
Action	YES: Step 3. NO: Step 44.
STEP 3	Is the kHz display illuminated with each digit at zero?
Action	YES: Step 4. NO: Suspect a fault on the display board PM371 (Table 10).
STEP 4	Set the MHz switch to 3. Set the TUNING RATE switch to SLOW. Slowly rotate the kHz control clockwise. Does the kHz display increase in 10Hz steps at a rate of 2.5kHz per turn?
Action	YES: Step 5. NO: Step 48.
STEP 5	Slowly rotate the kHz control counter-clockwise. Does the display decrease in 10Hz steps at a rate of 2.5kHz per turn?
Action	YES: Step 6. NO: Suspect a fault on the display board PM371 (Table 10).
STEP 6	Set the TUNE RATE switch to FAST. Repeat steps 4 and 5. Does the display now increase and decrease in steps of 100Hz?
Action	YES: Step 7. NO: Suspect a fault on the display board (Table 10, begin at step 4).

TABLE 1 (Cont'd)

STEP 7	As the display passes from 00000 to 99990, does the lamp behind the 3 on the MHz dial extinguish and the lamp behind the 2 illuminate?
Action	YES: Step 8. NO: Suspect a fault on the display board PM371 (Table 10).
STEP 8	Continue to decrease the kHz display indication. Does it decrease to 97990 and then stop?
Action	YES: Step 9. NO: Suspect a fault on the display board PM371 (Table 10).
STEP 9	Set the MHz switch one position counter-clockwise. Has the illuminated 2 moved to the centre of the MHz dial?
Action	YES: Step 10. NO: Suspect a fault on the display board PM371 (Table 10).
STEP 10	Does the kHz display still indicate 97990?
Action	YES: Step 11. NO: Suspect a fault on the display board PM371 (Table 10).
STEP 11	Rotate the kHz control counter-clockwise. Does the kHz display decrease from 97990?
Action	YES: Step 12. NO: Suspect a fault on the display board PM371 (Table 10).
STEP 12	Rotate the kHz control clockwise. Does the display increase to 99990, change to 00000 and then stop at 02000?
Action	YES: Step 13. NO: Suspect a fault on the display board PM371 (Table 10).
STEP 13	As the kHz display passed through 00000, did the lamp behind the 2 extinguish and the lamp behind the 3 illuminate?
Action	YES: Step 14 NO: Suspect a fault on the display board PM371 (Table 10).
STEP 14	Set the MHz switch one position clockwise. Has the illuminated 3 moved to the centre of the MHz dial?
Action	YES: Step 15. NO: Suspect a fault on the display board PM371 (Table 10).
STEP 15	Does the kHz display still indicate 02000?
Action	YES: Step 16. NO: Suspect a fault on the display board PM371 (Table 10).

TABLE 1 (Contd)

STEP 16	Rotate the kHz control clockwise. Does the kHz display increase from 02000?
Action	YES: Step 17. NO: Suspect a fault on the display board PM371 (Table 10).
STEP 17	Rotate the kHz control in each direction one turn. Does the kHz display change at a rate of 50kHz per turn?
Action	YES: Step 18. NO: Suspect a fault on the display board PM371 (Table 10).
STEP 18	Does the 10Hz digit remain at zero?
Action	YES: Step 19. NO: Suspect a fault on the display board PM371 (Table 10).
STEP 19	Set the TUNING RATE switch to LOCK. Rotate the kHz control in each direction in turn. Does the kHz display remain static?
Action	YES: Step 20 NO: Suspect a fault in the wiring to the TUNING RATE switch.
STEP 20	Connect the receiver 1MHz IN/OUT socket to the external standard socket on the digital frequency meter. Set the digital frequency meter to operate from an external 1MHz standard. Connect the digital frequency meter to the LO IN/OUT socket on the rear panel. Set the kHz control to display 000.00. Set the MHz switch from 0 to 29MHz. Does the digital frequency meter display 35.400MHz plus the MHz switch setting?
Action	YES: Step 21. NO: Suspect a synthesizer fault (Table 3).
STEP 21	Does the OUT-OF-LOCK indicator lamp remain extinguished for each position of the MHz switch?
Action	YES: Step 22. NO: Step 51.
STEP 22	Set the METER SWITCH to DRIVE LEVEL. Set the kHz control to display 015.00. Step the MHz switch through each position. Does the meter indication lie within the V portion of the meter scale for each switch position?
Action	YES: Step 23. NO: Step 52.

TABLE 1 (Cont'd)

STEP 23	Set the MHz switch to 0 and set the kHz control to display 000.00. Does the front panel meter indicate half scale?
Action	YES: Step 24. NO: Suspect a fault on the first mixer board PM335, in the area of the notch filter.
STEP 24	Connect the digital frequency meter to the 34MHz IN/OUT socket on the rear panel. Does the frequency meter indicate 34 000 000Hz plus or minus 1Hz?
Action	YES: Step 25. NO: Suspect a fault on the 34MHz generator board PM339 (Table 5).
STEP 25	Set the receiver IF GAIN control fully clockwise, the MODE switch to USB, the METER switch to AM/USB, the USB BANDWIDTH switch to 3, the AF GAIN control fully counter-clockwise and the loudspeaker to ON. Set the RF TUNE control to WB and the AGC switch to OFF. Turn the AF GAIN control progressively clockwise. Can noise be heard in the loudspeaker?
Action	YES: Step 26. NO: Step 58.
STEP 26	Set the MODE switch to AM. Can noise be heard in the loudspeaker?
Action	YES: Step 27. NO: Suspect a faulty a.m. detector circuit on the main i.f./a.f. board, or a faulty a.m. selection circuit.
STEP 27	Set the MODE switch to USB+BFO. Does the level of noise in the loudspeaker increase?
Action	YES: Step 28. NO: Suspect a faulty 1.4MHz b.f.o. on the 34MHz generator board PM339 or a faulty c.w. selection circuit.
STEP 28	Set the USB BANDWIDTH to 0.4-1.6 and 0.8-1.2 in turn. Does the noise level in the loudspeaker decrease as the bandwidth is reduced?
Action	YES: Step 29. NO: Step 69.

TABLE 1 (Cont'd)

STEP 29	Connect a pair of headphones (600 ohms) to the left-hand PHONES jack. Reset the USB BANDWIDTH switch to 3. Can noise be heard in the headphones?
Action	YES: Step 30. NO: Suspect a fault in the area of the PHONES jacks, or faulty wiring.
STEP 30	Connect the headphones to the right hand PHONES jack. Can noise be heard in the headphones?
Action	YES: Step 31. NO: Suspect a fault in the area of the PHONES jacks, or faulty wiring.
STEP 31	Can noise still be heard in the loudspeaker?
Action	NO: Step 32. YES: Suspect a faulty right-hand PHONES jack or faulty wiring.
STEP 32	Connect the c.w. output of the signal generator, set to a frequency of 1.02MHz and an output level of 10 millivolts e.m.f., to the receiver antenna socket. Connect the wattmeter absorption, set to 8 ohms impedance, to the loudspeaker terminals (TS1, LS and E). Set the receiver frequency to 1.02MHz, set the MODE switch to USB, and set the AGC switch to SHORT. Tune the signal generator through 1.02MHz. Is a response heard in the loudspeaker?
Action	YES: Step 33. NO: Step 64.
STEP 33	Tune the signal generator for a steady tone in the loudspeaker. Reduce the signal generator output level to 1 microvolt e.m.f. Can the tone still be heard in the loudspeaker?
Action	YES: Step 34. NO: Step 64.
STEP 34	Using the AF GAIN control, can the wattmeter absorption indication be set to 1 watt?
Action	YES: Step 35. NO: Step 66.
STEP 35	Readjust the AF GAIN control for an indication of 100 milliwatts on the wattmeter absorption. Set the AGC switch to OFF and adjust the IF GAIN control to restore the wattmeter indication to 100 milliwatts. Off-tune the signal generator by at least 10kHz. Has the wattmeter indication fallen by not less than 15dB?
Action	YES: Step 36. NO: Step 38.

TABLE 1 (Cont'd)

STEP 36	Retune the signal generator to give a steady tone in the loudspeaker. Rotate the RF TUNE control away from the WB position and adjust for a maximum indication on the wattmeter absorption. Is the indication greater than 25 milliwatts?
Action	YES: Step 37. NO: Suspect faulty r.f. range switching at 1MHz.
STEP 37	Repeat steps 33 to 36 inclusive for receiver frequencies of 2.02MHz, 4.02MHz, 8.02MHz, 16.02MHz and 29.02MHz. Is the receiver response within the limits quoted for these steps?
Action	YES: Step 38. NO: Suspect faulty r.f. range switching at the appropriate MHz setting.
STEP 38	Set the receiver frequency to 3.5MHz, the TUNING RATE switch to LOCK, the RF TUNE control to WB, the AGC switch to SHORT and the MODE switch to USB. Set the output level from the signal generator (connected to the antenna socket) to 2 microvolts e.m.f. Tune the signal generator to the receiver for maximum response within the receiver passband. Adjust the AF GAIN control for an indication of 100 milliwatts on the wattmeter absorption (connected to the LS and E terminals of TS1). Increase the output level from the signal generator to 200 millivolts e.m.f. (+100dB relative to 2 microvolts). Is the increase in audio output level 5dB or less?
Action	YES: Step 39. NO: Step 68.
STEP 39	Set the AGC switch to OFF and set the IF GAIN control fully counter-clockwise. Is the audio output level 100 milliwatts or less?
Action	YES: Step 40. NO: Suspect a faulty IF GAIN control or associated components.
STEP 40	Connect the wattmeter absorption, 600 ohms impedance, to the LINE OUTPUT, MAIN IF terminals of TS1. Set the AM/USB LINE LEVEL control fully clockwise. Is the audio output level at least 4 milliwatts?
Action	YES: No fault apparent. To fully check the performance of the receiver, carry out the procedures given in Chap.2-4. NO: Suspect a fault on the main i.f./a.f. board, in the area of the line amplifier (Table 6).

TABLE 1 (Cont'd)

STEP 41	Does the front panel meter indicate within the green portion of the meter scale for any of the voltage positions of the meter switch?
Action	NO: Step 42. YES: Step 43.
STEP 42	Is the POWER fuse serviceable?
Action	YES: Step 43. NO: Replace POWER fuse.
STEP 43	Connect the digital voltmeter between chassis (0V) and each of the following pins in turn, on the meter switching board. Pin 10 (red) +20V Pin 3 (orange) +12V Pin 6 (brown) +5V Pin 25 (violet) -7V Are all the voltages correct?
Action	YES: Suspect a fault on the meter switching board, a faulty meter switch or meter, or a wiring fault. NO: Suspect a power supply fault or a wiring fault.
STEP 44	Connect the multimeter, set to the 25 volt d.c. range, between chassis (negative) and pin 6 on the potentiometer board (attached to the shaft encoder). Does the multimeter indicate +12V?
Action	YES: Step 45. NO: Suspect a wiring fault between the +12V supply and the MHz lamps.
STEP 45	Are the MHz lamps serviceable?
Action	YES: Step 46. NO: Replace unserviceable lamps.
STEP 46	Is there continuity between the MHz lamps and pins 24 (L), 25 (N) and 26(H) on the display board?
Action	YES: Suspect a fault on the display board PM371. NO: Trace and repair faulty wiring.
STEP 47	Are the shaft-encoder lamps illuminated? These lamps may be under-powered and thus may not glow brightly.
Action	YES: Step 48. NO: Step 50.

TABLE 1 (Cont'd)

STEP 48	Connect the oscilloscope, in turn, to pins 4 and 10 on the potentiometer board. Observe the oscilloscope whilst rotating the kHz control. Is a quasi-sinusoidal waveform displayed, approximate amplitude 1.8V peak-to-peak, in each case?
Action	YES: Step 49. NO: Suspect a faulty shaft encoder (sensor board).
STEP 49	Connect the oscilloscope, in turn, to pins 31 and 32 on the display board. Observe the oscilloscope whilst rotating the kHz control. Is the waveform displayed, in each case, the same as in the previous step?
Action	YES: Suspect a fault on the display board PM371 (Table 10). NO: Suspect a wiring fault between the shaft-encoder and the display board.
STEP 50	Connect the multimeter, set to the 25 volt d.c. range, between chassis (negative) and pin 4 on the shaft encoder. Does the multimeter indicate +12V?
Action	YES: Suspect unserviceable shaft encoder lamps or an open circuit 0V return wire from the shaft-encoder. NO: Suspect a wiring fault between the +12V supply and the shaft-encoder lamps.
STEP 51	Is the OUT-OF-LOCK indicator lamp extinguished for any of the following ranges of MHz switch settings? 0 to 7MHz inclusive 8 to 17MHz inclusive 18 to 29MHz inclusive
Action	YES: Suspect a malfunction of one or more of the h.f. loop oscillators. See Table 5. NO: Suspect a faulty synthesizer (Table 2).
STEP 52	Connect the h.f. electronic voltmeter, high input impedance, between pins 22 and 21 (0V) on the h.f. loop board PS337. Step the MHz switch through each position. Does the h.f. electronic voltmeter indicate 225 millivolts r.m.s. plus or minus 5dB at each switch position?
Action	YES: Step 53. NO: Suspect a faulty synthesizer (Table 2).

TABLE 1 (Cont'd)

STEP 53	Transfer the h.f. electronic voltmeter, high input impedance, to pins 10 and 9 (OV) on the first mixer board PM335. Does the voltmeter indicate 225 millivolts r.m.s. plus or minus 5dB?
Action	YES: Step 54. NO: Suspect a wiring fault between the h.f. loop board PS337 and the first mixer board PM335.
STEP 54	Connect the multimeter, set to the 5 volts d.c. range, between pin 11 on the first mixer board PM335 and chassis (OV). Does the multimeter indicate approximately +1.0V for the 0, 1, 2 and 3 settings of the MHz switch?
Action	YES: Step 55. NO: Suspect a faulty logic board or faulty wiring.
STEP 55	Transfer the positive lead of the multimeter to pin 8 on the first mixer board. Does the multimeter indicate approximately 1.0V for MHz switch settings 4 to 29 inclusive?
Action	YES: Step 56. NO: Suspect a faulty logic board or faulty wiring.
STEP 56	Connect the h.f. electronic voltmeter, high input impedance, to pin 30 on the first mixer board PM335. Does the voltmeter indicate between 6 and 15V r.m.s. for all settings of the MHz switch?
Action	YES: Step 57. NO: Suspect a faulty first mixer board PM335 (Table 8).
STEP 57	Connect the positive lead of the multimeter, set to the 250 microamp d.c. range, to pin 5 on the first mixer board. Connect the negative lead to chassis. Does the multimeter indicate approximately 80 microamps for all settings of the MHz switch?
Action	YES: Suspect a fault on the meter switching board or faulty wiring. NO: Suspect a fault on the first mixer board PM335, between D5 and pin 5.
STEP 58	Set the AGC switch to SHORT. Can noise be heard in the loudspeaker?
Action	NO: Step 59. YES: Suspect a faulty IF GAIN control or associated components.

TABLE 1 (Cont'd)

STEP 59	Connect the multimeter, set to the 25 volt d.c. range, between chassis (negative) and pin 14 on the main i.f./a.f. board. Does the multimeter indicate +14.5V?
Action	YES: Step 60. NO: Step 64.
STEP 60	Set the AGC switch to OFF. Set the MODE switch to AM. Can noise be heard in the loudspeaker?
Action	NO: Step 61. YES: Step 72.
STEP 61	Connect a pair of headphones (600 ohms) to the right-hand PHONES jack. Can noise be heard in the headphones?
Action	NO: Step 62. YES: Suspect a faulty loudspeaker, loudspeaker switch, R4 or associated wiring.
STEP 62	Connect the wattmeter absorption, 8 ohms impedance, between the LS and E terminals of TS1. Does the wattmeter indicate a noise level?
Action	NO: Step 63. YES: Suspect a fault in the area of the PHONES jacks, a faulty loudspeaker, or a wiring fault.
STEP 63	Connect the wattmeter absorption, 600 ohms impedance, to the LINE OUTPUT MAIN IF terminals of TS1. Set the AM/USB LINE LEVEL control fully clockwise. Does the wattmeter indicate a noise level?
Action	YES: Suspect a fault on the main i.f./a.f. board, in the area of the loudspeaker amplifier. NO: Suspect a fault on the main i.f./a.f. board, in the area of the audio pre-amplifier, or a faulty AM/USB LINE LEVEL control and associated wiring.
STEP 64	Transfer the positive lead of the multimeter to pin 6 on the a.f. and memory regulator board. Does the multimeter indicate +14.5V.
Action	NO: Step 65. YES: Suspect a wiring fault between the a.f. and memory regulator board and the main i.f./a.f. board.

TABLE 1 (Cont'd)

STEP 65	Transfer the positive lead of the multimeter to pin 4 on the a.f. and memory regulator board. Does the multimeter indicate approximately +23V?
Action	YES: Suspect a fault on the a.f. and memory regulator board, in the area of the 14.5V regulator circuit. NO: Suspect a wiring fault between diode D3 on the regulator board PM370 and the a.f. and memory regulator board, pin 4.
STEP 66	Set the AGC switch to OFF. Set the IF GAIN control fully clockwise. Set the c.w. output level of the signal generator (connected to the antenna socket) to 2 microvolts e.m.f. Tune the signal generator to the receiver for maximum indication on the wattmeter absorption. Adjust the AF GAIN control for an indication of 100 milliwatts on the wattmeter. Disconnect the signal generator from the antenna socket and connect it to the chassis mounted first mixer input socket (Chap.1-1, fig.2). Increase the signal generator output level to restore the wattmeter indication to 100 milliwatts. Is the increase in the signal generator output level 10dB or greater?
Action	YES: Step 67. NO: Suspect a fault on the r.f. amplifier board (Table 9).
STEP 67	Remove the cover from the first mixer board compartment in the base of the receiver (Chap.1-1, fig.3). Unsolder and disconnect link LK1 from the first mixer board. Connect the signal generator, set to a frequency of 35.400MHz and an output level of 1 microvolt e.m.f., to the T3 side of LK1. Set the AGC switch to SHORT. Adjust the AF GAIN control for a reference level of 100 milliwatts on the wattmeter absorption. Set the AGC switch to OFF. Adjust the IF GAIN control to restore the wattmeter indication to 100 milliwatts. Off-tune the signal generator frequency by at least 10kHz. Has the audio output level, as indicated on the wattmeter, fallen by not less than 17dB?
Action	YES: Suspect a fault on the first mixer board PM335 (Table 8). NO: Suspect a fault on the second mixer board (Table 8).

STEP 68	Unsolder and disconnect the a.g.c. input lead to the second mixer board, at pin 9. Connect the positive lead of the variable output power supply to pin 9 on the second mixer board, negative lead to chassis. Set the output of the variable voltage power supply to 1.4V d.c. Set the c.w. output level of the signal generator to 2 microvolts e.m.f. Set the AGC switch to OFF and set the IF GAIN control fully clockwise. Adjust the AF GAIN control for an indication of 100 milliwatts on the wattmeter absorption. Increase the output of the variable voltage power supply to 3.0V and increase c.w. output level of the signal generator to restore the wattmeter indication to 100 milliwatts. Is the increase in the signal generator output level at least 38dB?
Action	YES: Suspect a fault on the main i.f./a.f. board, in the area of the a.g.c. circuit. NO: Suspect a fault on the second mixer board, in the area of the gain control circuit.
STEP 69	Set the USB BANDWIDTH switch to 3. Set the 34MHz INT/EXT switch to EXT. Does the noise output level decrease?
Action	YES: Suspect a faulty filter selection circuit, wiring or switch. NO: Step 70.
STEP 70	Set the 34MHz INT/EXT switch to INT. Remove the cover from the first mixer board compartment in the base of the chassis. Connect the h.f. electronic voltmeter, high-impedance input, between LK2 and TP2 (earthy) on the second mixer board. Does the voltmeter indicate approximately 600 millivolts r.m.s.?
Action	YES: Step 71. NO: Suspect a faulty output amplifier on the 34MHz generator board PM339.
STEP 71	Disconnect the coaxial plug from the chassis-mounted second mixer output socket. Connect the signal generator, set to a frequency of 1.4MHz and an output level of 10 millivolts e.m.f., to the disconnected coaxial plug (via a back-to-back connector). Set the receiver MODE switch to USB, the USB BANDWIDTH switch to 3 and the AGC switch to SHORT. Carefully tune the signal generator until a steady tone is heard in the loudspeaker. Reduce the generator output level to 64 microvolts e.m.f. Can the AF GAIN be adjusted for an indication on the wattmeter absorption of 1 watt?
Action	YES: Suspect a fault on the second mixer board PM336 (Table 8). NO: Suspect a fault on the filter board PS367 or the main i.f./a.f. board PM364 (Table 6).

TABLE 1 (Cont'd)

STEP 72	Set the MODE switch to CW. Can noise be heard in the loudspeaker?
Action	YES: Suspect a fault on the 34MHz generator board in the area of the 1.4MHz generator. NO: Step 73.
STEP 73	Connect the h.f. electronic voltmeter, high-impedance input, between pins 5 and 4 (earthy) on the main i.f./a.f. board. Does the voltmeter indicate approximately 250 millivolts r.m.s. in all MODE switch positions except AM?
Action	YES: Suspect a fault on the main i.f./a.f. board in the area of the product detector or a faulty s.s.b. selector circuit. NO: Suspect a fault on the 34MHz generator board in the area of the 1.4MHz output buffer stages.

TABLE 2

Fault-location : synthesizer (sub-assembly level)

STEP 1	Set the POWER switch to ON. Set the rear panel 1MHz, 34MHz and LO switches to INT. Connect the h.f. electronic voltmenter 50-ohm input impedance, to the 1MHz IN/OUT socket. Does the voltmeter indicate at least 180 millivolts r.m.s.?
Action	YES: Step 2. NO: Step 9.
STEP 2	Disconnect the h.f. electronic voltmeter and connect in its place the digital frequency meter. Is the frequency displayed 1 000 000 Hz plus or minus 1Hz?
Action	YES: Step 3. NO: Step 13.
STEP 3	Disconnect the digital frequency meter. Connect the h.f. electronic voltmeter, 50-ohm input impedance, to the 34Hz IN/OUT socket. Does the voltmeter indicate at least 180 millivolts r.m.s.?
Action	YES: Step 4. NO: Step 14.
STEP 4	Disconnect the h.f. electronic voltmeter and connect in its place the digital frequency meter. Is the frequency displayed 34 000 000Hz plus or minus 10Hz?
Action	YES: Step 5. NO: Suspect a fault on the 34MHz generator board PM339.
STEP 5	Disconnect the digital frequency meter. Is the OUT-OF-LOCK indicator lamp extinguished?
Action	YES: Step 6. NO: Step 15.
STEP 6	Connect the digital frequency meter to the LO IN/OUT socket. Set the receiver MHz switch to 0. Set the kHz control to display 000.00. Is the frequency displayed 35 400 000Hz?
Action	YES: Step 7. NO: Step 19.

TABLE 2 (Cont'd)

STEP 7	Rotate the MHz switch through each position, i.e. 0 to 29. Is the frequency displayed on the digital frequency meter 35.4MHz plus the MHz switch setting?
Action	YES: Step 8. NO: Suspect a fault on the transfer loop board PS338, the h.f. loop board PS337, or the logic board PS365.
STEP 8	Rotate the kHz control. Does the digital frequency meter indication follow the receiver frequency?
Action	YES: No fault apparent. NO: Suspect a fault on the l.f. loop board PM588, upper loop board PM589 or display board PM371.
STEP 9	Connect the h.f. electronic voltmeter, 50-ohm input impedance, to pin 3 on the frequency standard board. Does the voltmeter indicate approximately 250 millivolts r.m.s.?
Action	YES: Step 10. NO: Step 12.
STEP 10	Connect the h.f. electronic voltmeter, 50-ohm input impedance to pin 27 on the 34MHz generator board PM339. Does the voltmeter indicate approximately 250 millivolts r.m.s.?
Action	YES: Step 11. NO: Suspect a faulty connection between the frequency standard board and the 34MHz generator board PM339.
STEP 11	Connect the h.f. electronic voltmeter, 50-ohm input impedance, to pin 4 on the 34MHz generator board PM339. Does the voltmeter indicate at least 180 millivolts r.m.s.?
Action	YES: Suspect a faulty connection between the 34MHz generator board PM339 and the 1MHz IN/OUT socket. NO: Suspect a fault on the 34MHz generator board PM339.
STEP 12	Connect a multimeter, set to the 25-volt d.c. range, between pins 1 (positive) and 2 on the frequency standard board. Does the multimeter indicate +12 volts?
Action	YES: Suspect a faulty frequency standard. NO: Suspect a wiring or a power supply fault.

TABLE 2 (Cont'd)

STEP 13	Connect the digital frequency meter to pin 3 on the frequency standard board. Is the frequency displayed 1 000 000Hz plus or minus 1Hz?
Action	YES: Suspect a fault on the 34MHz generator board PM339. NO: Suspect a faulty frequency standard.
STEP 14	Connect the h.f. electronic voltmeter, 50-ohm input impedance, to pin 22 on the 34MHz generator board PM339. Does the voltmeter indicate at least 180 millivolts r.m.s.?
Action	YES: Suspect a faulty connection between the 34MHz generator board PM339 and the 34MHz IN/OUT socket. NO: Suspect a fault on the 34MHz generator board PM339.
STEP 15	Use the oscilloscope to monitor, in turn, pins 33, 34 and 35 on the display board. Is approximately +3V present at each pin?
Action	YES: Suspect a fault on the display board in the area of TR1, ML33a. NO: Step 16.
STEP 16	Is approximately +3V present at pin 33 on the display board PM371?
Action	YES: Step 17. NO: Suspect a fault on the l.f. loop board PM588 or the upper loop board PM589.
STEP 17	Is approximately +3V present at pin 34 on the display board PM371?
Action	YES: Step 18. NO: Suspect a fault on the h.f. loop board PS337.
STEP 18	Is approximately +3V present at pin 35 on the display board PM371?
Action	NO: Suspect a fault on the transfer loop board PS338.
STEP 19	Connect the digital frequency meter to TP2 on the upper loop board PM454. Does the meter indicate 4.6MHz?
Action	YES: Suspect a fault on the transfer loop board PS338 or the h.f. loop board PS337. NO: Suspect a fault on the l.f. loop board PM588 or the upper loop board PM589.

TABLE 3

Fault-location : l.f. loop PM588 and upper loop PM589

STEP 1	Set the rear panel 1MHz, 34MHz and LO switches to INT. Connect a multimeter, set to the 25-volt d.c. range, between chassis (OV) and each of the following board pins in turn.

PM453	PM454	VOLTAGE
27	5	+5
38	4	+20
26	6	-7

	Are all the voltages correct?
Action	YES: Step 2. NO: Check the power supply and the connections to each board.
STEP 2	Connect the oscilloscope to ML10 pin 4 on PM589. Is OV indicated?
Action	YES: Step 3. NO: Step 8.
STEP 3	Connect the oscilloscope to ML10 pin 12 on PM589. Is OV indicated?
Action	YES: Step 4. NO: Step 5.
STEP 4	Connect the oscilloscope to ML10 pin 10 on PM589. Is OV indicated?
Action	YES: Step 5. NO: Step 15.
STEP 5	Connect the digital frequency meter to TP3 on PM588. Does the frequency meter indicate 1MHz?
Action	YES: Step 6. NO: Step 19.
STEP 6	Connect the digital frequency meter to TP4 on PM588. Does the frequency meter indicate 1kHz?
Action	YES: Step 7. NO: Suspect a fault on PM588 in the area of ML2, ML4, ML7.

TABLE 3 (Cont'd)

STEP 7	Connect the digital frequency meter to TP2 on PM588. Does the frequency meter indicate 7MHz minus the 1kHz, 100Hz and 10Hz digits of the receiver frequency multiplied by 100?
Action	YES: Step 8. NO: Step 20.
STEP 8	Connect the oscilloscope to pin 44 on PM588. Is the transfer loop oscillator output signal present?
Action	YES: Step 9. NO: Suspect a fault on PM589, in the area of the transfer loop oscillator (TR4, TR5, TR6) or faulty wiring to PM588.
STEP 9	Connect the oscilloscope to TP7 on PM588. Is the square wave signal displayed?
Action	YES: Step 10. NO: Suspect a fault on PM588, in the area of the mixer and low-pass filter (ML13, TR18, TR19, ML17, TR20, D3).
STEP 10	Connect the oscilloscope to TP8 on PM588. Is the negative-going strobe pulse-train signal displayed?
Action	YES: Step 11. NO: Suspect a fault on PM588, in the area of the programmed divider N2 (ML14, ML15, ML18, ML19).
STEP 11	Connect the universal counter-timer (Chap.2-3, Table 1, item 7), set to measure frequency ratio, between TP2 and TP8 on PM588. Is the ratio displayed equal to the division ratio of programmed divider N2? (N2 = 453 minus selected 100kHz and 10kHz digits of the receiver frequency).
Action	YES: Step 12. NO: Step 24.
STEP 12	Connect the oscilloscope to ML16 pin 5 on PM588. Is a narrow fixed-width pulse signal displayed?
Action	YES: Step 13. NO: Suspect a fault on PM588, in the area of the phase comparator (ML16, ML17), the voltage-control circuit (TR21, TR22, TR23) or an incorrect voltage/frequency characteristic of the transfer loop oscillator on PM589.

TABLE 3 (Cont'd)

STEP 13	Connect the oscilloscope to ML16 pin 9 on PM588. Is a narrow fixed-width pulse signal displayed?
Action	YES: Step 14. NO: Suspect a fault on PM588, in the area of the phase comparator (ML16, ML17), the voltage-control circuit (TR21, TR22, TR23) or an incorrect voltage/frequency characteristic of the transfer loop oscillator on PM589.
STEP 14	Connect the oscilloscope to ML10 pin 4 on PM589. Is 0V indicated?
Action	YES: Step 15. NO: Suspect a fault on PM588, in the area of the lock indication circuit (ML21, R72, R73, C30, C31).
STEP 15	Connect the digital frequency meter to TP1 on PM589. Note the frequency displayed. Transfer the frequency meter to TP3 on PM589. Is the frequency displayed equal to that noted above divided by 100?
Action	YES: Step 16. NO: Suspect a fault on PM589, in the area of the fixed divider (ML4, ML6).
STEP 16	Connect the digital frequency meter to TP2 on PM589. Is the frequency displayed equal to 4.6MHz minus the 100kHz and 10kHz digits of the receiver frequency?
Action	YES: Step 17. NO: Step 25.
STEP 17	Connect the oscilloscope to ML10, pin 10 on PM589. Is 0V indicated?
Action	YES: Step 18. NO: Suspect a fault on PM589, in the area of the lock detector circuit (ML11, R48, R51 ,C31, C32).
STEP 18	Connect the oscilloscope to board pin 12 on PM589. Is 0V indicated?
Action	YES: Suspect a fault on PM589, in the area of ML10, ML12. NO: No fault apparent.

TABLE 3 (Cont'd)

STEP 19	Connect the oscilloscope to pin 46 on PM588. Is a 1MHz signal displayed?
Action	YES: Suspect a fault on PM588, in the area of T1, TR2. NO: Suspect a fault on the 34MHz generator board PM339, or a wiring fault.
STEP 20	Connect the universal counter-timer, set to measure frequency ratio, between TP2 and TP6 on PM588. Is the ratio displayed equal to the division ratio of programmed divider N1? (N1 = 7000 minus the selected 1kHz, 100Hz and 10Hz digits of the receiver frequency).
Action	YES: Step 21. NO: Step 23.
STEP 21	Connect the oscilloscope to ML8 pin 5 on PM588. Is a narrow fixed-width pulse signal displayed?
Action	YES: Step 22. NO: Suspect a fault on PM588, in the area of the phase-comparator (ML1, ML8), the voltage-control circuit (TR4, TR5) or an incorrect voltage/frequency characteristic of the 7MHz v.c.o.
STEP 22	Connect the oscilloscope to ML8 pin 9 on PM588. Is a narrow fixed-width pulse signal displayed?
Action	YES: Suspect a fault on PM588, in the area of the lock-indication circuit (ML12, R51, R52, C19, C20). NO: Suspect a fault on PM588, in the area of the phase-comparator (ML1, ML8), the voltage-control circuit (TR4, TR5) or an incorrect voltage/frequency characteristic of the 7MHz v.c.o.
STEP 23	Are the coding inputs (1kHz, 100Hz, 10Hz data inputs) from the display board PM371 correct?
Action	YES: Suspect a fault on PM588, in the area of the programmed divider N1 (ML3, ML5, ML6, ML10). NO: Suspect a fault on the display board PM371 or a wiring fault.
STEP 24	Are the coding inputs (100kHz and 10kHz data inputs) to PM588 from the display board PM371 correct?
Action	YES: Suspect a fault on PM588, in the area of the programmed divider N2 (ML14, ML15, ML18, ML19). NO: Suspect a fault on the display board PM371 or a wiring fault.

TABLE 3 (Cont'd)

STEP 25	Connect the universal counter/timer, set to measure frequency ratio, between TP2 and TP4 on PM589. Is the ratio displayed equal to the division ratio of programmed divider N2? (N2 = 453 minus the selected 100kHz and 10kHz digits of the receiver frequency).
Action	YES: Step 26. NO: Step 28.
STEP 26	Connect the oscilloscope to TP6 on PM589. Is a narrow fixed-width pulse signal displayed?
Action	YES: Step 27. NO: Suspect a fault on PM589, in the area of the phase-comparator (ML9, G5), the voltage-control circuit (TR16, TR17, TR18) or an incorrect voltage/frequency characteristic of the 4.6 to 3.6MHz v.c.o.
STEP 27	Connect the oscilloscope to ML9 pin 5 on PM589. Is a narrow fixed-width pulse signal displayed?
Action	YES: Step 17. NO: Suspect a fault on PM589, in the area of the phase-comparator (ML9, G5), the voltage-control circuit (TR16, TR17, TR18) or an incorrect voltage/frequency characteristic of the 4.6 to 3.6MHz v.c.o.
STEP 28	Are the coding inputs (100kHz and 10kHz data inputs) to PM589 from the display board PM371 correct?
Action	YES: Suspect a fault on PM589, in the area of programmed divider N2 (ML2, ML3, ML5, ML7). NO: Suspect a fault on the display board PM371 or a wiring fault.

TABLE 4

Fault-location : h.f. loop PS337 and transfer loop PS338

STEP 1 — Set the rear panel 1MHz, 34MHz and LO switches to INT. Connect a multimeter, set to the 25-volt d.c. range, between chassis (0V) and the following board pins, in turn.

PS337	PS338	VOLTAGE
9	3	+5
10	-	+12
11	2	+20
16	7	-7

Are all the voltages correct?

Action — YES: Step 2.
NO: Check power supply and connections to each board.

STEP 2 — Connect the oscilloscope to pin 6 on PS338.

Is approximately +3V indicated?

Action — YES: Step 3.
NO: Step 4.

STEP 3 — Connect the oscilloscope to pin 12 on PM337.

Is approximately 3V indicated?

Action — YES: Step 4.
NO: Step 12.

STEP 4 — Connect the oscilloscope to pin 21 on PS338.

Is a 1MHz signal displayed?

Action — YES: Step 5.
NO: Suspect a fault on the 34MHz generator board PM339 or faulty wiring.

STEP 5 — Connect the oscilloscope to pin 19 on PS338.

Is the 885 to 948kHz transfer loop oscillator signal displayed?

Action — YES: Step 6.
NO: Suspect a fault on PS337, in the area of the transfer loop oscillator (TR17, TR20, TR21) or faulty wiring.

STEP 6 — Connect the oscilloscope to TP2 on PS338.

Is an approximate square wave signal displayed?*

Action — YES: Step 7.
NO: Suspect a fault on PS338, in the area of the mixer (TR1, TR2, TR3, ML3) or TR6, ML7a.

* The frequency of the signal at Step 5 must be correct for it to pass through filter L11, L12.

TABLE 4 (Cont'd)

STEP 7	Connect the oscilloscope to TP1 on PS338. Is a 4.6 to 3.6MHz signal displayed?
Action	YES: Step 8. NO: Suspect a fault on PS338, in the area of TR4, TR5, or faulty wiring.
STEP 8	Connect the universal counter-timer, set to measure frequency ratio, between TP1 and TP6 on PS338. Is the ratio displayed equal to the division ratio of programmed divider N3? (N3 = 40 plus the selected setting of the receiver MHz switch).
Action	YES: Step 9. NO: Step 27.
STEP 9	Connect the oscilloscope to TP3 on PS338. Is a narrow fixed-width pulse signal displayed?
Action	YES: Step 10. NO: Suspect a fault on PS338, in the area of the phase-comparator (ML8, ML7b), the voltage-control circuit (TR7, TR8, TR9, TR10), or an incorrect voltage/frequency characteristic of the transfer loop oscillator on PS337.
STEP 10	Connect the oscilloscope to ML8 pin 6. Is a narrow fixed-width pulse signal displayed?
Action	YES: Step 11. NO: Suspect a fault on PS338, in the area of the phase-comparator (ML8, ML7b), the voltage-control circuit (TR7, TR8, TR9, TR10) or an incorrect voltage/frequency characteristic of the transfer loop oscillator on PS337.
STEP 11	Is the OUT-OF-LOCK indicator lamp extinguished?
Action	YES: Step 12. NO: Suspect a fault on PS338, in the area of the lock-indicator circuit (ML9, ML10, ML11, ML4c, ML4d).
STEP 12	Connect the oscilloscope to ML7 pin 11 on PS337. Is a square wave signal displayed?
Action	YES: Step 13. NO: Suspect a fault on PS337 in the area of ML12 or ML7b.
STEP 13	Connect the oscilloscope to TP4 on PS337. Set the receiver MHz switch to 0MHz. Is the h.f. loop oscillator output signal displayed?
Action	YES: Step 14. NO: Step 28.

TABLE 4 (Cont'd)

STEP 14	Set the receiver MHz switch to 8MHz. Is the h.f. loop oscillator output signal displayed?
Action	YES: Step 15. NO: Step 30.
STEP 15	Set the receiver MHz switch to 18MHz. Is the h.f. loop oscillator output signal displayed?
Action	YES: Step 16. NO: Step 31.
STEP 16	Connect the oscillosccpe to pin 22 on PS337. Is the local oscillator (LO) output signal displayed?
Action	YES: Step 17. NO: Suspect a fault on PS337, in the area of the output amplifier (TR14) or the diode switch (D16, D17, D18).
STEP 17	Connect the oscilloscope to pin 24 on PS337. Is the LO output signal displayed?
Action	YES: Step 18. NO: Suspect a fault on PS338, in the area of the output amplifier (TR15) or the diode switch (D16, D17, D18).
STEP 18	Connect the oscilloscope to TP5 on PS337. Is an approximate square wave signal displayed?
Action	YES: Step 19. NO: Suspect a fault on PS337, in the area of TR11, TR12, ML2a.
STEP 19	Connect the oscilloscope to ML7 pin 3 on PS337. Is a positive-going pulse signal displayed?
Action	YES: Step 20. NO: Suspect a fault on PS337, in the area of the programmed divider N3 (ML3, ML5, ML4, ML2b, ML9, ML6).
STEP 20	Connect the oscilloscope to TP7 on PS337. Is a varying-width pulse signal displayed?
Action	NO: Step 21. YES: Step 32.
STEP 21	Connect the oscilloscope to TP8 on PS337. Is a varying-width pulse signal displayed?
Action	NO: Step 22. YES: Step 23.

TABLE 4 (Cont'd)

STEP 22	Connect the oscilloscope to TP7 on PS337. Is a narrow fixed-width pulse signal displayed?
Action	YES: Step 23. NO: Suspect a fault on PS337, in the area of the phase-comparator (ML6, ML7) or an incorrect voltage/frequency characteristic of the h.f. loop oscillator.
STEP 23	Connect the oscilloscope to TP8 on PS337. Is a narrow fixed-width pulse signal displayed?
Action	YES: Step 24. NO: Suspect a fault on PS337, in the area of the phase-comparator (ML6, ML7) or an incorrect voltage/frequency characteristic of the h.f. loop oscillator.
STEP 24	Is the OUT-OF-LOCK indicator lamp extinguished?
Action	YES: Step 25. NO: Suspect a fault on PS337, in the area of the lock-indicator circuit (ML8, ML10, ML11, ML6).
STEP 25	Are the coding inputs (MHz data inputs) from the logic board correct for the MHz switch position selected?
Action	YES: Step 26. NO: Suspect a fault on the logic board or a wiring fault.
STEP 26	Set the kHz portion of the receiver frequency to 000.00. Connect the digital frequency meter, in turn, to TP5 and TP6 on PS337 and record the frequencies displayed for each position of the receiver MHz switch. Compute the frequency ratio (N3) for each switch position, which should equal 40 plus the MHz switch setting. Is the frequency ratio correct?
Action	YES: No fault apparent. NO: Suspect a fault on PS337, in the area of the programmed divider N3 (ML3, ML5, ML9, ML2, ML6).
STEP 27	Are the coding inputs (MHz data inputs) from the logic board correct for the MHz switch position selected?
Action	YES: Suspect a fault on PS338, in the area of the programmed divider N3 (ML1, ML2, ML4, ML5, ML6). NO: Suspect a fault on the logic board or a wiring fault.
STEP 28	Connect the oscilloscope to the junction of diodes D10, D11 and D12 on PS337. Is the h.f. loop oscillator output signal displayed?
Action	YES: Suspect a fault on PS337, in the area of TR10. NO: Step 29.

TABLE 4 (Cont'd)

STEP 29	Set the front panel MHz switch to 18. Connect the multimeter, set to the 25-volt d.c. range, between chassis (negative) and TP3 on PS337. Does the multimeter indicate approximately +12V?
Action	YES: Suspect a fault on PS337, in the area of oscillator 1 (TR6, TR9). NO: Suspect a fault on PS337, in the area of ML1, or TR3, or faulty logic board, or faulty wiring.
STEP 30	Set the front panel MHz switch to 8. Connect the multimeter, set to the 25-volt d.c. range, between chassis (negative) and TP2 on PS337. Does the multimeter indicate approximately +12V?
Action	YES: Suspect a fault on PS337, in the area of oscillator 2 (TR5, TR8). NO: Suspect a fault on PS337, in the area of TR2, or faulty logic board, or faulty wiring.
STEP 31	Set the front panel MHz switch to 0. Connect the multimeter, set to the 25-volt d.c. range, between chassis (negative) and TP1 on PS337. Does the multimeter indicate approximately +12V?
Action	YES: Suspect a fault on PS337, in the area of oscillator 3 (TR4, TR7). NO: Suspect a fault on PS337, in the area of TR1, or faulty logic board, or faulty wiring.
STEP 32	Connect the multimeter, set to the 10-volt d.c. range, between chassis (negative) and the junction of L21, L22 and L23 on PS337. Does the multimeter indicate a static voltage level of approximately +3V?
Action	YES: Suspect a fault on PS337, in the area of the varactor diode of the selected h.f. loop oscillator, or incorrect coil adjustment. NO: Suspect a fault on PS337, in the area of TR19.
STEP 33	Connect the multimeter, set to the 25-volt d.c. range, between chassis (negative) and the junction of L21, L22 and L23 on PS337. Does the multimeter indicate a static voltage level of approximately +18V?
Action	YES: Suspect a fault on PS337, in the area of the varactor diode of the selected h.f. loop oscillator, or incorrect coil adjustment. NO: Suspect a fault on PS337, in the area of TR16, TR18.

TABLE 5

Fault-location : 34MHz generator PM339

STEP 1	Set the AFC switch to OFF. Set the rear panel 1MHz and 34MHz switches to INT. Connect the negative lead of the multimeter, set to the 25-volt d.c. range, to chassis and connect the positive lead, in turn, to the following board pins. PIN — VOLTAGE 1 — +5 2 — +20 9 — +12 Are all the voltages correct?
Action	YES: Step 2. NO: Suspect a power supply fault or faulty wiring.
STEP 2	Connect the oscilloscope to TP3. Is a 1MHz square wave, 3:2 mark/space ratio, approximate amplitude 2V peak-to-peak displayed?
Action	YES: Step 3. NO: Step 19.
STEP 3	Connect the h.f. electronic voltmeter, 50-ohm impedance, to the 1MHz IN/OUT socket. Does the voltmeter indicate at least 180 millivolts r.m.s.?
Action	YES: Step 4. NO: Suspect a fault in the area of amplifier stage TR9 or faulty wiring.
STEP 4	Connect the oscilloscope to the collector (can) or TR13. Is a 1MHz approximate square wave signal of 3V peak-to-peak amplitude displayed?
Action	YES: Step 5. NO: Suspect a faulty shaper stage, TR13, or a faulty gate, G8, G9, G10 or G11.
STEP 5	Connect the oscilloscope to board pin 6. Is a 1MHz approximate square wave signal of approximately 3V peak-to-peak amplitude displayed?
Action	YES: Step 6. NO: Suspect a fault in the area of G8.
STEP 6	Connect the oscilloscope to board pin 8. Is a 1MHz approximate square wave signal of approximately 0.2V peak-to-peak amplitude displayed?
Action	YES: Step 7. NO: Suspect a fault in the area of G9.

TABLE 5 (Cont'd)

STEP 7	Connect the oscilloscope to TP9. Is a 1MHz approximate square wave signal of at least 2V peak-to-peak in amplitude displayed?
Action	YES: Step 8. NO: Suspect a fault in the area of G10.
STEP 8	Set the MODE switch to USB. Connect the oscilloscope to TP7. Is a 200kHz 3:2 mark/space ratio square wave of approximately 3.5V peak-to-peak amplitude displayed?
Action	YES: Step 9. NO: Step 21.
STEP 9	Connect the oscilloscope to TP15. Is the amplitude of the 1.4MHz waveform displayed approximately 400 millivolts peak-to-peak?
Action	YES: Step 10. NO: Suspect a fault in the area of the crystal filter (XL2, XL3), TR15, TR16, or incorrect setting of T2 or R65.
STEP 10	Connect the oscilloscope to board pin 10. Is a 1.4MHz signal of approximately 0.8V peak-to-peak amplitude displayed?
Action	YES: Step 11. NO: Suspect a fault in the area of TR20.
STEP 11	Connect the oscilloscope to board pin 11. Is a 1.4MHz signal of approximately 0.8V peak-to-peak amplitude displayed?
Action	YES: Step 12. NO: Suspect a fault in the area of TR21.
STEP 12	Connect the digital frequency meter to board pin 10. Is a frequency of 1 400 000Hz plus or minus 1Hz displayed?
Action	YES: Step 13. NO: Suspect a fault in the area of ML8 or the 1.4MHz crystal filter (XL2, XL3).
STEP 13	Set the MODE switch to USB+BFO. Connect the oscilloscope to board pin 10. Is a 1.4MHz signal of approximately 0.5V peak-to-peak amplitude displayed?
Action	YES: Step 14. NO: Step 24.

TABLE 5 (Cont'd)

STEP 14	Connect the digital frequency meter to board pin 11. Set the BFO control to +. Is a frequency of 1 397 000Hz plus or minus 100Hz displayed?
Action	YES: Step 15. NO: Suspect an incorrect setting of R4 or L4, a faulty BFO control or associated components, or an incorrect voltage/ frequency characteristic of the 1.4MHz v.c.o. (TR8).
STEP 15	Set the BFO control to −. Is a frequency of 1 403 000Hz plus or minus 100Hz displayed?
Action	YES: Step 16. NO: Suspect an incorrect setting of R4 or L4, a faulty BFO control or associated components, or an incorrect voltage/ frequency characteristic of the 1.4MHz v.c.o. (TR8).
STEP 16	Connect the h.f. electronic voltmeter, high-impedance input, to board pin 20. Does the voltmeter indicate between 800 millivolts and 1.4 volts r.m.s.?
Action	YES: Step 17. NO: Step 25.
STEP 17	Connect the h.f. electronic voltmeter, 50-ohm impedance input, to the 34MHz IN/OUT socket. Does the voltmeter indicate at least 180 millivolts r.m.s.?
Action	YES: Step 18. NO: Suspect a fault in the area of the diode switch (D5, D6) or a wiring fault.
STEP 18	Connect the digital frequency meter to board pin 20. Connect the 1MHz IN/OUT socket on the rear panel to the external 1MHz input socket on the digital frequency meter and set the meter to operate from an external standard. Is a frequency of 34 000 000Hz displayed?
Action	YES: No fault apparent. NO: Step 30.
STEP 19	Connect the oscilloscope to TP2. Is an approximate 5MHz square wave signal, 3V peak-to-peak amplitude, displayed?
Action	NO: Step 20. YES: Suspect a fault in the area of the divide-by-five stage (ML1) or TR9.

TABLE 5 (Cont'd)

STEP 20	Connect the oscilloscope to board pin 27. Is a 5MHz signal of approximately 700 millivolts peak-to-peak amplitude displayed?
Action	YES: Suspect a fault in the area of the amplifier/shaper stage TR2, TR4. NO: Suspect a faulty 5MHz frequency standard or a wiring fault.
STEP 21	Connect the oscilloscope to TP12. Is a 1MHz 3:2 mark/space ratio square wave signal of approximately 3.5V peak-to-peak displayed?
Action	NO: Step 22. YES: Suspect a fault in the area of the divide-by-five stage ML8.
STEP 22	Connect the oscilloscope to the collector (can) of TR14. Does the oscilloscope indicate a voltage (d.c.) of approximately +5V?
Action	NO: Step 23. YES: Suspect a fault in the area of G11, or faulty wiring to board pin 15.
STEP 23	Connect the oscilloscope to board pin 15. Does the oscilloscope indicate OV?
Action	YES: Suspect a fault in the area of TR14. NO: Suspect a faulty MODE switch or a wiring fault.
STEP 24	Connect the oscilloscope to board pin 15. Does the oscilloscope indicate OV?
Action	YES: Suspect a fault in the area of the 1.4MHz v.c.o. (TR8). NO: Suspect a faulty MODE switch or a wiring fault.
STEP 25	Connect the h.f. electronic voltmeter, high impedance input, to TP5. Does the voltmeter indicate approximately 400 millivolts r.m.s.?
Action	NO: Step 26. YES: Suspect a fault in the area of the output amplifier stage TR11, TR12.
STEP 26	Connect the h.f. electronic voltmeter, high-impedance input, to the collector (can) of TR5. Does the voltmeter indicate approximately 400 millivolts r.m.s.?
Action	NO: Step 27. YES: Suspect a fault in the area of the diode switch (D5, D6).

TABLE 5 (Cont'd)

STEP 27	Connect the h.f. electronic voltmeter, high-impedance input, to TP4. Does the voltmeter indicate approximately 750 millivolts r.m.s.?
Action	NO: Step 28. YES: Suspect a fault in the area of the amplifier stage TR3, TR5.
STEP 28	Connect the multimeter, set to the 10-volt d.c. range, to the junction of C4 and the emitter of TR1. Does the multimeter indicate approximately +5V?
Action	NO: Step 29. YES: Suspect a fault in the area of the 34MHz v.c.o. (TR6/TR7).
STEP 29	Connect the oscilloscope to board pin 12. Does the oscilloscope indicate 0V?
Action	YES: Suspect the 34MHz switch is not set to INT, or suspect a faulty 34MHz switch or switch wiring. NO: Suspect a fault in the area of the voltage regulator transistor TR1.
STEP 30	Connect the oscilloscope to TP11. Is a 1MHz 3:2 mark/space ratio square wave signal of approximately 3.5V peak-to-peak displayed?
Action	YES: Step 31. NO: Suspect a faulty gate, G5, G6, G7 or G8.
STEP 31	Connect the oscilloscope to ML4 pin 2. Is a 1MHz 3:2 mark/space ratio square wave signal of approximately 3.5V peak-to-peak displayed?
Action	YES: Step 32. NO: Suspect a fault in the area of the divide-by-34 stage (ML3, ML4, G2, G3).
STEP 32	Connect the oscilloscope to TP14. Is a narrow fixed-width negative-going pulse signal of approximately 3.5V peak-to-peak displayed?
Action	YES: Step 33. NO: Suspect a fault in the area of the phase-comparator, ML6, G12, or incorrect voltage/frequency characteristic of the 34MHz v.c.o., a faulty varactor diode (D4) or incorrect adjustment of L2.

TABLE 5 (Cont'd)

STEP 33	Connect the oscilloscope to ML6 pin 6. Is a narrow fixed-width negative-going pulse signal of approximately 3.5V peak-to-peak displayed?
Action	YES: Step 34. NO: Suspect a fault in the area of the phase-comparator, ML6, G12, or incorrect voltage/frequency characteristic of the 34MHz v.c.o., a faulty varactor diode (D4) or incorrect adjustment of L2.
STEP 34	Connect the multimeter, set to the 10-volt d.c. range to TP1. Does the multimeter indicate approximately +7V?
Action	YES: No fault apparent. NO: Suspect fault in the area of the voltage-control circuit (TR17, TR18, TR19), D4 or the loop filter (C62, C64, R70).

TABLE 6

Fault-location : main i.f./a.f. board PM364/1

STEP 1	Connect the multimeter, set to the 25-volt d.c. range, between chassis (0V) and the following board pins, in turn (observe correct polarity). PIN NO. — VOLTAGE 13 — +12 14 — +14.5 20 — -7 Are all the voltages correct?
Action	YES: Step 2. NO: Check power supply and connections to the board.
STEP 2	Set the AGC and AFC switches to OFF, the RF TUNE control to WB, and the MODE switch to USB. Set the IF GAIN fully clockwise and the AF GAIN control fully counter-clockwise. Set the POWER switch to OFF. Unsolder and remove link LK1 from the board. Connect the multimeter, set to the 100-milliamp d.c. range, between the pins of LK1, with the negative lead of the multimeter connected to the pin nearest to the edge of the board. Set the POWER switch to ON. Does the multimeter indicate approximately 15 milliamps?
Action	YES: Replace LK1 and proceed to Step 3. NO: Suspect an incorrect setting of R84 or a faulty loudspeaker amplifier circuit.
STEP 3	Unsolder the coaxial lead connected to pin 2 on the filter board PS367 (the screen may be left connected to pin 3). Connect the 1 kilohm resistor in series with the coaxial lead connected to the 50-ohm output of the signal generator and connect the other end of this lead to the coaxial lead removed from pin 2 of the filter board. Set the signal generator frequency to 1.4MHz plus or minus 500Hz and set the output level to 64 microvolts e.m.f. Connect the h.f. electronic voltmeter, high-impedance input, to TP2 on the main i.f./a.f. board. Does the voltmeter indicate approximately 100 millivolts r.m.s.?
Action	YES: Step 4. NO: Step 18.
STEP 4	Connect the h.f. electronic voltmeter, high-impedance input, to TP3 on the main i.f./a.f. board. Does the voltmeter indicate approximately 200 millivolts r.m.s.?
Action	YES: Step 5. NO: Suspect a fault in the area of TR2, the 1.4MHz band-pass filter (L1, L2 etc.), or an incorrect setting of R9.

TABLE 6 (Cont'd)

STEP 5	Connect the h.f. electronic voltmeter, high-impedance input, to TP4 on the main i.f./a.f. board. Does the voltmeter indicate between 90 and 130 millivolts r.m.s.?
Action	YES: Step 6. NO: Suspect a fault in the area of TR8.
STEP 6	Connect the h.f. electronic voltmeter, 50-ohm input impedance, to the MAIN IF OUT socket on the rear panel. Ensure that the signal generator output level is set to 64 microvolts e.m.f. c.w. Does the voltmeter indicate approximately 50 millivolts r.m.s.?
Action	YES: Step 7. NO: Suspect a fault in the area of TR4, TR6.
STEP 7	Connect the electronic multimeter to TP7 on the i.f./a.f. board. Does it indicate between 50 and 90 millivolts r.m.s.?
Action	YES: Step 8. NO: Suspect a fault in the area of the product detector.
STEP 8	Set the MODE switch to AM. Set the signal generator for 30 per cent amplitude modulation at 1kHz and an output level of 180 microvolts e.m.f. Connect the electronic multimeter to TP7. Does it indicate between 50 and 90 millivolts r.m.s.?
Action	YES: Step 9. NO: Suspect a fault in the area of the a.m. detector.
STEP 9	Set the MODE switch to USB. Set the signal generator output level to 64 microvolts e.m.f. c.w. Connect the electronic multimeter to board pin 8. Does the electronic multimeter indicate at least 150 millivolts r.m.s.?
Action	YES: Step 10. NO: Suspect a fault in the area of the audio pre-amplifier.
STEP 10	Connect the wattmeter absorption, 600-ohm input impedance, to the LINE OUTPUT MAIN IF terminals of TS1. Set the AM/USB LINE LEVEL control fully clockwise. Does the wattmeter indicate at least 4 milliwatts?
Action	YES: Step 11. NO: Suspect a fault in the area of the line amplifier.

TABLE 6 (Cont'd)

STEP 11	Connect the wattmeter absorption, 8-ohm input impedance, to the LS and E terminals of TS1. Set the AF GAIN control fully clockwise. Does the wattmeter indicate at least 1 watt?
Action	YES: Step 12. NO: Suspect a fault in the area of the loudspeaker amplifier.
STEP 12	Connect the electronic multimeter to TP3 and adjust the signal generator output level for an indication of 200 milliwatts r.m.s. Connect the multimeter, set to the 10-volt d.c. range, between board pin 29 (positive) and chassis. Does the multimeter indicate +1.40 volts plus or minus 100 millivolts?
Action	YES: Step 13. NO: Step 19.
STEP 13	Increase the signal generator output level by 4dB. Does the multimeter (connected to board pin 29) indicate at least 3.0V d.c.?
Action	YES: Step 14. NO: Step 19.
STEP 14	Connect the multimeter to board pin 30 (positive). Connect the h.f. electronic voltmeter, high-impedance input, to TP3 and record the level indicated (IF GAIN control fully clockwise). Adjust the IF GAIN control for an indication of 1.4V plus or minus 30 millivolts on the multimeter. Has the signal level at TP3 fallen by not more than 1dB?
Action	YES: Step 15. NO: Suspect an incorrect setting of R4.
STEP 15	Connect the multimeter, set to the 25-volt d.c. range, between TP6 (positive) and the -7 volt rail at board pin 20. Does the multimeter indicate approximately +6V?
Action	YES: Step 16. NO: Suspect a fault in the area of ML3, TR11, or an incorrect setting of R42.
STEP 16	Reduce the signal generator output level until the multimeter indication changes to approximately +14 volts. Does the reduction in the signal generator output level approximate 4dB?
Action	YES: Step 17. NO: Suspect a fault in the area of ML3, TR11, or an incorrect setting of R42.

TABLE 6 (Cont'd)

STEP 17	Connect the multimeter, set to the 25-volt d.c. range, between TP9 (negative) and chassis. Does the multimeter indicate approximately -6V?
Action	YES: No fault apparent. NO: Suspect a fault in the area of TR3 or ML4.
STEP 18	Set the IF GAIN control fully clockwise. Connect the multimeter, set to the 2.5-volt d.c. range, between TP1 (positive) and chassis. Does the multimeter indication exceed 1.2 volts?
Action	YES: Suspect a fault in the area of the IF GAIN control, TR1, R4. NO: Suspect a fault in the area of ML1.
STEP 19	Connect the digital voltmeter between the positive lead of C20 and chassis. Does the voltmeter indicate approximately +80 millivolts d.c.?
Action	YES: Step 20. NO: Suspect a fault in the area of TR7/TR9 or an incorrect setting of R31.
STEP 20	Increase the signal generator output level by 4dB. Has the digital voltmeter indication increased to approximately +160 millivolts?
Action	YES: Suspect a fault in the area of ML2. NO: Suspect a fault in the area of TR7/TR9 or an incorrect setting of R31.

TABLE 7

Fault-location : i.s.b. i.f./a.f. board PM364/3

Note...

Before proceeding, check that the main i.f./a.f. board is functioning correctly.

STEP 1

Connect the multimeter, set to the 25-volt d.c. range, between chassis (0V) and the following board pins, in turn (observe correct polarity).

PIN NO.	VOLTAGE
13	+12
14	+14.5
20	-7

Are all the voltages correct?

Action

YES: Step 2.
NO: Check power supply and connections to the board.

STEP 2

Set the AGC and AFC switches to OFF, the RF TUNE control to WB, and the MODE switch to LSB. Set the IF GAIN fully clockwise and the AF GAIN control fully counter-clockwise. Unsolder the coaxial lead connected to pin 4 on the filter board PS367 (the screen may be left connected to pin 5). Connect the 1 kilohm resistor in series with the coaxial lead connected to the 50-ohm output of the signal generator and connect the other end of this lead to the coaxial lead removed from pin 4 of the filter board. Set the signal generator frequency to 1.4MHz plus or minus 500Hz and set the output level to 64 microvolts e.m.f. Connect the h.f. electronic voltmeter, high-impedance input, to TP2 on the i.f./a.f. board.

Does the voltmeter indicate approximately 100 millivolts r.m.s.?

Action

YES: Step 3.
NO: Step 16.

STEP 3

Connect the h.f. electronic voltmeter, high-impedance input, to TP3 on the i.f./a.f. board.

Does the voltmeter indicate approximately 200 millivolts r.m.s.?

Action

YES: Step 4.
NO: Suspect a fault in the area of TR2, the 1.4MHz bandpass filter (L1, L2 etc.), or an incorrect setting of R9.

STEP 4

Connect the h.f. electronic voltmeter, high-impedance input, to TP4 on the i.f./a.f. board.

Does the voltmeter indicate between 90 and 130 millivolts r.m.s.?

Action

YES: Step 5.
NO: Suspect a fault in the area of TR8.

TABLE 7 (Cont'd)

STEP 5	Connect the h.f. electronic voltmeter, 50-ohm input impedance, to the ISB IF OUT socket on the rear panel. Ensure that the signal generator output level is set to 64 microvolts e.m.f. c.w. Does the voltmeter indicate approximately 50 millivolts r.m.s.?
Action	YES: Step 6. NO: Suspect a fault in the area of TR4, TR6.
STEP 6	Connect the electronic multimeter to TP7 on the i.f./a.f. board. Does it indicate between 50 and 90 millivolts r.m.s.?
Action	YES: Step 7. NO: Suspect a fault in the area of the product detector.
STEP 7	Connect the electronic multimeter to board pin 8. Does the electronic multimeter indicate at least 150 millivolts r.m.s.?
Action	YES: Step 8. NO: Suspect a fault in the area of the audio pre-amplifier.
STEP 8	Connect the wattmeter absorption, 600 ohm input impedance, to the ISB LINE OUTPUT terminals of TS1. Set the LSB LINE LEVEL control fully clockwise. Does the wattmeter indicate at least 4 milliwatts?
Action	YES: Step 9. NO: Suspect a fault in the area of the line amplifier.
STEP 9	Connect the wattmeter absorption, 8-ohm input impedance, to the LS and E terminals of TS1. Set the AF GAIN control fully clockwise. Set the MODE switch, in turn, to ISB-L and ISB-U. Does the wattmeter indicate at least 1 watt for each position?
Action	YES: Step 10. NO: Suspect a fault in the area of the MODE switch or a wiring fault.
STEP 10	Set the MODE switch to LSB. Connect the electronic multimeter to TP3 and adjust the signal generator output level for an indication of 200 millivolts r.m.s. Connect the multimeter, set to the 10-volt d.c. range, between board pin 29 (positive) and chassis. Does the multimeter indicate +1.40 volts plus or minus 100 millivolts?
Action	YES: Step 11. NO: Step 17.

TABLE 7 (Cont'd)

STEP 11	Increase the signal generator output level by 4dB. Does the multimeter (connected to board pin 29) indicate at least 3.0V d.c.?
Action	YES: Step 12. NO: Step 17.
STEP 12	Connect the multimeter to board pin 30 (positive). Connect the h.f. electronic voltmeter, high-impedance input, to TP3 and record the level indicated (IF GAIN control fully clockwise). Adjust the IF GAIN control for an indication of 1.4V plus or minus 30 millivolts on the multimeter. Has the signal level at TP3 fallen by not more than 1dB?
Action	YES: Step 13. NO: Suspect an incorrect setting of R4.
STEP 13	Connect the multimeter, set to the 25-volt d.c. range, between TP6 (positive) and the -7 volt rail at board pin 20. Does the multimeter indicate approximately +6V?
Action	YES: Step 14. NO: Suspect a fault in the area of ML3, TR11, or an incorrect setting of R42.
STEP 14	Reduce the signal generator output level until the multimeter indication changes to approximately +14 volts. Does the reduction in the signal generator output level approximate 4dB?
Action	YES: Step 15. NO: Suspect a fault in the area of ML3, TR11, or an incorrect setting of R42.
STEP 15	Connect the multimeter, set to the 25-volt d.c. range between TP9 (negative) and chassis. Does the multimeter indicate approximately -6V?
Action	YES: No fault apparent. NO: Suspect a fault in the area of TR3 or ML4.
STEP 16	Set the IF GAIN control fully clockwise. Connect the multimeter, set to the 2.5-volt d.c. range, between TP1 (positive) and chassis. Does the multimeter indication exceed 1.2 volts?
Action	YES: Suspect a fault in the area of the IF GAIN control, TR1, R4. NO: Suspect a fault in the area of ML1.

TABLE 7 (Cont'd)

STEP 17	Connect the digital voltmeter between the positive lead of C20 and chassis. Does the voltmeter indicate approximately +80 millivolts d.c.?
Action	YES: Step 18. NO: Suspect a fault in the area of TR7/TR9 or an incorrect setting of R31.
STEP 18	Increase the signal generator output level by 4dB. Has the digital voltmeter indication increased to approximately +160 millivolts?
Action	YES: Suspect a fault in the area of ML2. NO: Suspect a fault in the area of TP7/TR9 or an incorrect setting of R31.

TABLE 8

Fault-location : first mixer PM335 and second mixer PM336

Note...

Before proceeding with this Table ensure that the main i.f./a.f. board is functioning correctly (Table 6).

STEP 1 Set the receiver controls as follows:-

MHz	15	AFC	OFF
kHz	020.00	MODE	USB
RF TUNE	WB	LS	OFF
AGC	SHORT	Headphones	Plugged in

Connect the wattmeter absorption, 8-ohm input impedance, between the LS and E terminals of TS1. Connect the signal generator, set to a frequency of 15.02MHz and a c.w. output level of 1 microvolt e.m.f., to the chassis-mounted first mixer input connector in place of the existing lead (Chap.1-1, fig.2). Tune the signal generator for a maximum indication on the wattmeter. Set the AF GAIN for a reading of 100mW on the wattmeter. Set the AGC switch to OFF and adjust the IF GAIN to restore the wattmeter indication to 100mW (0dB reference). Off-tune the signal generator by at least 10kHz.

Does the wattmeter indication fall by not less than 11dB?

Action YES: Step 2.
NO: Step 3.

STEP 2 Set the receiver MHz switch to 3 and the AGC switch to SHORT. Set the signal generator frequency to 3.02MHz and tune it for a maximum indication on the wattmeter absorption. Set the AF GAIN for a reading of 100mW on the wattmeter: set the AGC switch to OFF and set the IF GAIN to restore the wattmeter indication to 100mW. Off-tune the signal generator by at least 10kHz.

Does the wattmeter indication fall by not less than 11dB?

Action YES: No fault apparent.
NO: Suspect a high insertion loss in the 35.415 to 39.4MHz bandpass filter or faulty diode switching circuit on the first mixer board PM335.

TABLE 8 (Cont'd)

STEP 3	Set the receiver MHz switch to 8 and the AGC switch to SHORT. Set the signal generator frequency to 8.02MHz and tune it for a maximum indication on the wattmeter. Set the AF GAIN for a reading of 100mW on the wattmeter; set the AGC switch to OFF and set the IF GAIN to restore the wattmeter indication to 100mW. Off-tune the signal generator by at least 10kHz. Does the wattmeter indication fall by not less than 11dB?
Action	YES: Suspect a high insertion loss in the 39.4 to 69.4 band-pass filter or faulty diode switching circuit on the first mixer board PM335. NO: Step 4.
STEP 4	Set the front-panel METER switch to DRIVE LEVEL. Disconnect the signal generator from the first mixer input socket. Temporarily short-circuit pins 9 and 10 on the first mixer board PM335. Does the front-panel meter indication fall to approximately half-scale whilst the noise level in the headphones remains unchanged?
Action	YES: Step 5. NO: Suspect incorrect setting of R39 or faulty drive amplifier (TR2, TR5) on first mixer board.
STEP 5	Unsolder and remove link LK1 from the first mixer board PM335. Connect the signal generator, set to a frequency of 35.400MHz and an output level of 1 microvolt e.m.f., to the T3 side of LK1. Set the AGC switch to SHORT and set the AF GAIN for a reading of 100mW on the wattmeter. Set the AGC switch to OFF and set the IF GAIN to restore the wattmeter indication to 100mW. Off-tune the signal generator by at least 10kHz. Does the wattmeter indication fall by not less than 19dB?
Action	YES: Suspect faulty mixer (TR3, TR4, TR6, TR7), high insertion loss of FL1, or faulty transformer (T5, T7) on the first mixer board PM335. NO: Step 6.
STEP 6	Disconnect the signal generator and replace LK1 on the first mixer board. Unsolder and remove link LK2 from the first mixer board. Connect the signal generator, set to a frequency of 35.400MHz and an output level of 1 microvolt e.m.f., to the FL1 side of LK2. Set the AGC switch to SHORT and set the AF GAIN for a reading of 100mW on the wattmeter. Set the AGC switch to OFF and set the IF GAIN to restore the wattmeter indication to 100mW. Off-tune the signal generator by at least 10kHz. Does the wattmeter indication fall by not less than 15dB?
Action	YES: Suspect high insertion loss of filter FL1 on the first mixer board PM335. NO: Step 7.

TABLE 8 (Cont'd)

STEP 7	Replace link LK2 on the first mixer board PM335. Unsolder and remove LK1 from the second mixer board PM336. Connect the signal generator, set to a frequency of 35.400MHz and an output level of 10 microvolts e.m.f., via a 0.1 uF capacitor to the base of TR9. Set the AGC switch to SHORT and set the AF GAIN for a reading of 100mW on the wattmeter. Set the AGC switch to OFF and set the IF GAIN control to restore the wattmeter indication to 100mW. Off-tune the signal generator by at least 10kHz. Does the wattmeter indication fall by not less than 12dB?
Action	YES: Suspect a low gain first i.f. amplifier on the second mixer board PM336. Refer to step 8 to isolate faulty area. NO: Step 9.
STEP 8	Set the rear panel 34MHz INT/EXT switch to EXT. Unsolder and remove link LK2 from the first mixer board PM335. Replace link LK1 on the second mixer board PM336. Connect the output from the signal generator, set to a frequency of 35.400MHz and an output level of 20 millivolts e.m.f., to the FL1 side of LK2 on the first mixer board. Use the h.f. electronic voltmeter, high-impedance input, to monitor the following points on the second mixer board PM336. The signal levels quoted are typical. Board pin 13 — 10mV r.m.s. Junction D1, D2 — 40mV r.m.s. TR5 base — 40mV r.m.s. TP1 — 100mV r.m.s. LK1 (earth of meter to TP2) — 50mV r.m.s.
STEP 9	Ensure that the 34MHz INT/EXT switch is set to INT. Connect the h.f. electronic voltmeter, high-impedance input, between LK2 and TP2 (meter earth) on the second mixer board. Ensure that link LK1 on the second mixer board has been removed. Is the voltmeter indication greater than 600 millivolts?
Action	YES: Step 10. NO: Suspect faulty 34MHz generator board PM339, or faulty filter, L10 to L14, on the second mixer board PM336.
STEP 10	Connect the 1MHz IN/OUT socket on the rear panel of the receiver to the external standard socket on the digital frequency meter. Set the digital frequency meter to operate from an external 1MHz standard. Connect the digital frequency meter to the 34MHz IN/OUT socket on the rear panel. Does the digital frequency meter indicate 34 000 000Hz plus or minus 1Hz?
Action	YES: Step 11. NO: Suspect faulty 34MHz generator board PM339 (Table 5).

TABLE 8 (Cont'd)

STEP 11	Connect the multimeter, set to the 10-volt d.c. range, between TP1 (positive) and chassis on the 34MHz generator board PM339. Does the multimeter indicate between +6 and +8 volts?
Action	YES: Suspect faulty second mixer stage (TR9, TR10) or buffer stage (TR11) on the second mixer board. NO: Suspect faulty 34MHz generator board PM339 (Table 5).

TABLE 9

Fault-location : r.f. board PM582

Note...

Before proceeding with this Table, ensure that the first mixer board PM335, the second mixer board PM336 and the main i.f./a.f. board are all functioning correctly.

STEP 1 Set the receiver controls as follows:-

MHz	28	AFC	OFF
kHz	020.00	MODE	USB
RF TUNE	WB	LS	OFF
AGC	SHORT	Headphones	Plugged in
		USB BANDWIDTH	3

Connect the wattmeter absorption, 8-ohm input impedance, between the LS and E terminals of TS1. Connect the signal generator (50-ohm output impedance), set to a frequency of 28.02MHz and a c.w. output level of 1 microvolt e.m.f., to the receiver antenna socket. Tune the signal generator for a maximum indication on the wattmeter. Set the AF GAIN for a reading of 100mW on the wattmeter. Set the AGC switch to OFF and set the IF GAIN to restore the wattmeter indication to 100mW. Off-tune the signal generator by at least 10kHz.

Does the wattmeter indication fall by not less than 15dB?

Action YES: Step 2.
NO: Step 7.

STEP 2 Re-tune the signal generator to the receiver for a maximum indication on the wattmeter. Set the AGC switch to SHORT and set the RF TUNE control for a maximum indication on the wattmeter. Set the AF GAIN for a reading of 100mW on the wattmeter and set the AGC switch to OFF. Set the IF GAIN to restore the wattmeter indication to 100mW. Off-tune the signal generator by at least 10kHz.

Does the wattmeter indication fall by not less than 9dB?

Action YES: Step 3.
NO: Suspect incorrect coding input from logic board, faulty tuned circuit, micro-switch or relay.

STEP 3 Connect the 50-ohm impedance, high-output level signal generator (Chap.2-3, Table 1, item 3), set to a frequency of 30MHz and an output level of 1V e.m.f., to the input socket on the r.f. board. Connect electronic multimeter to TP1 on the r.f. board and check that it indicates approximately 0.5 volt p.d. Slowly increase the signal generator output level until the electronic multimeter indication falls to zero.

Is the signal generator output level between 7 and 14V e.m.f.?

Action YES: Step 4.
NO: Suspect faulty wideband protection stage or incorrect setting of C31 on the r.f. board.

TABLE 9 (Cont'd)

STEP 4	Set the RF TUNE control to WB. Connect the electronic multimeter to TP2 on the r.f. board. Set the signal generator output level to 1V e.m.f. and check that the electronic multimeter indicates approximately 0.5V p.d. Slowly increase the signal generator output level until the electronic multimeter indication falls to zero. Is the signal generator output level between 2.5 and 4.0V e.m.f?
Action	YES: Step 6. NO: Suspect faulty tuned protection stage or incorrect setting of C33 on the r.f. board.
STEP 5	Connect the 50-ohm impedance, high-output level signal generator, set to a frequency of 30MHz and an output level of 1V e.m.f., to the r.f. input socket on the r.f. board. Connect the electronic multimeter to TP1 on the r.f. board and check that it indicates approximately 0.5V p.d. Slowly increase the signal generator output level until the electronic multimeter indication falls to zero. Is the signal generator output level between 2.5 and 4.0 volts e.m.f.?
Action	YES: Step 6. NO: Suspect faulty wideband protection stage or incorrect setting of C31 on the r.f. board.
STEP 6	Set the output level of the signal generator to 1V e.m.f. and connect the electronic multimeter to TP1. Check that the electronic multimeter indicates approximately 0.5V p.d. Connect a wire link between the MUTE and E terminals of TS2. Does the electronic multimeter indication fall to zero?
Action	YES: No fault apparent. NO: Suspect faulty wideband protection stage, or faulty wiring between MUTE terminal and pin 3 on the r.f. board.
STEP 7	Connect the signal generator to the r.f. input socket on the r.f. board and repeat the signal-plus-noise/noise ratio check given in step 1. Does the wattmeter indication fall by not less than 15dB?
Action	YES: Suspect faulty re-radiation filter. NO: Step 8.
STEP 8	Set the signal generator frequency to 30MHz and set the output level to 1.0V e.m.f. Connect the electronic multimeter to TP1. Does the electronic multimeter indicate approximately 0.5V p.d.?
Action	YES: Step 9. NO: Suspect faulty wideband protection stage, relay RLQ or 30MHz low-pass filter (L7, L9).

TABLE 9 (Cont'd)

STEP 9	Connect the electronic multimeter to TP2. Check that the RF TUNE control is set to WB. Does the electronic multimeter indicate approximately 0.5V p.d.?
Action	YES: Step 10. NO: Suspect faulty relays RLN, RLP, or faulty tuned protection stage, relay RLR.
STEP 10	Connect the output of a signal generator, set to a frequency of 15MHz and an output level of 10 millivolts e.m.f., to the 50-ohm input of the h.f. electronic voltmeter. Note the level as indicated on the h.f. electronic voltmeter as a reference level. Disconnect the signal generator from the h.f. electronic voltmeter and re-connect it to the r.f. input socket on the r.f. board. Connect the h.f. electronic voltmeter to TP3 on the r.f. board. Is the output level, as indicated on the h.f. electronic voltmeter, within +13dB plus or minus 2.0dB of the previously established reference level?
Action	YES: Suspect a fault in 30MHz low-pass filter (L15 to L19). NO: Suspect a low gain r.f. amplifier stage TR5, TR6.

TABLE 10

Fault-location : display board PM371

STEP 1	Set the receiver POWER switch to OFF and then to ON. Connect a multimeter, set to the 10-volt d.c. range, between chassis (negative) and pins 23 and 39 , in turn, on the display board. Does the multimeter indicate +5V in each case?
Action	YES: Step 2. NO: Check power supplies and/or connections to board pins.
STEP 2	Are all the frequency display digits illuminated and at zero?
Action	YES: Step 3. NO: Step 11.
STEP 3	Set the TUNING RATE switch to SLOW. Rotate the kHz control clockwise. Does the display increase in 10Hz steps at a rate of 2.5kHz per turn?
Action	YES: Step 4. NO: Step 13.
STEP 4	Set the TUNING RATE switch to FAST. Rotate the kHz control clockwise. Does the display increase in 100Hz steps (10Hz digit at zero) at a rate of 50kHz per turn?
Action	YES: Step 5. NO: Suspect a faulty monostable, ML28a, or a faulty gate, G12, G13, G14, G16 or G17.
STEP 5	Rotate the kHz control clockwise until the display stops. Has it stopped at 02000?
Action	YES: Step 6. NO: Suspect a faulty overspill count-inhibit circuit, G24, G25.
STEP 6	Has the lamp in the centre of the MHz dial extinguished and the upper lamp of the MHz dial illuminated?
Action	YES: Step 7. NO: Suspect a faulty lamp, a faulty overspill indicator circuit (G27, G28, G29) or a faulty lampldriver transistor (TR5, TR6, TR7).
STEP 7	Rotate the kHz control counter-clockwise until the display stops. Has it stopped at 97999?
Action	YES: Step 8. NO: Suspect a faulty overspill count-inhibit circuit, G24, G25.

TABLE 10 (Cont'd)

STEP 8	Has the lamp in the centre of the MHz dial extinguished and the lower lamp of the MHz dial illuminated?
Action	YES: Step 9. NO: Suspect a faulty lamp, a faulty overspill indicator circuit (G27, G28, G29) or a faulty lamp-driver transistor (TR5, TR6, TR7).
STEP 9	Rotate the MHz switch one position counter-clockwise. Has the illuminated figure moved to the centre of the MHz dial?
Action	YES: Step 10. NO: Suspect a fault in the overspill-clear circuit, ML11 and associated components.
STEP 10	Connect the oscilloscope to board pin 27. Is a negative-going 25-millisecond pulse displayed when, whilst the kHz control is rotated, a 9-to-0 or a 0-to-9 transition of the 10kHz digit occurs?
Action	YES: No fault apparent. NO: Suspect a fault in the range blanking circuit, G23, ML33b.
STEP 11	Set the receiver kHz display to a figure other than 000.00. Set the POWER switch to OFF, wait ten seconds and then set the POWER switch to ON. Does the kHz display now read 000.00?
Action	YES: Step 12. NO: Suspect a fault in the initial zero circuit, TR4.
STEP 12	Check the data output codes for any digit not at zero, at the respective board pins. Are they all correct?
Action	YES: Any display not indicating zero is faulty and should be replaced (ML41 to ML45). NO: Suspect a faulty up/down counter (ML1 to ML6).
STEP 13	Connect the multimeter, set to the 10-volt d.c. range, to board pin 30. Does the voltmeter indicate approximately +5V?
Action	YES: Step 14. NO: Suspect a faulty TUNING RATE switch, faulty wiring or a faulty gate, G10, G11.

TABLE 10 (Cont'd)

STEP 14	Connect the oscilloscope to ML28 pin 5. Is a positive-going pulse signal displayed whilst the kHz control is rotated?
Action	YES: Step 15. NO: Step 16.
STEP 15	Connect the oscilloscope to ML6 pin 5. Rotate the kHz control clockwise. Is a positive-going pulse signal displayed?
Action	YES: Suspect a fault in the up/down counter chain, ML1 to ML6. NO: Suspect a faulty gate, G4 to G7.
STEP 16	Connect the oscilloscope to board pin 32. Is an approximately sinusoidal waveform displayed whilst the kHz control is rotated?
Action	YES: Step 17. NO: Step 19.
STEP 17	Connect the oscilloscope to board pin 31. Is an approximately sinusoidal waveform displayed whilst the kHz control is rotated?
Action	YES: Step 18. NO: Step 19.
STEP 18	Connect a dual-trace oscilloscope to ML27 pins 6 and 8. Are two waveforms displayed, 90 degrees out of phase with each other, whilst the kHz control is rotated?
Action	YES: Suspect a faulty monostable, ML28. NO: Suspect faulty TR2, TR3 or ML27, or incorrect setting of R1 and R2 on shaft-encoder.
STEP 19	Are the shaft-encoder lamps illuminated? These lamps may be under-run and hence may not glow brightly.
Action	NO: Step 20. YES: Suspect a faulty shaft-encoder.
STEP 20	Connect the multimeter, set to the 25-volt d.c. range, between chassis (negative) and pin 4 on the shaft-encoder. Does the multimeter indicate +12V?
Action	NO: Suspect a fault in the power supply or a wiring fault. YES: Suspect a faulty shaft-encoder.

TABLE 11

Fault-location : a.f.c. board PM369

STEP 1 — Set the receiver MODE switch to USB, the AGC switch to LONG, the AFC switch to OFF, the METER switch to TUNE CARRIER and the LOUDSPEAKER switch to ON. Set the rear panel 1MHz, 34MHz and LO switches to INT. Set the POWER switch to ON. Connect the multimeter, set to the 25 volt d.c. range, between the chassis and the following pins, in turn, on the a.f.c. board.

BOARD PIN	VOLTAGE
3	+5
2	+12
1	+20
8	-7

Are all the voltages correct?

Action — YES: Step 2.
NO: Suspect a power supply fault or faulty wiring.

STEP 2 — Connect the c.w. output of the signal generator, set to a frequency of 3MHz and an output level of 100 millivolts e.m.f., to the receiver antenna socket. Tune the receiver to the signal generator whilst observing the front-panel meter.

Does the meter indication decrease to zero coincident with a zero beat in the loudspeaker?

Action — YES: Step 3.
NO: Step 11.

STEP 3 — Set the AFC switch to PILOT CARRIER.

Does the AFC LOCK lamp glow?

Action — YES: Step 4.
NO: Step 39.

STEP 4 — Does the front-panel meter indicate zero on the AFC scale?

Action — YES: Step 5.
NO: Suspect a faulty relay RLA/1 or incorrect adjustment of C3 (Chap.2-5).

STEP 5 — Set the signal generator output level to 100 millivolts e.m.f. Set the AFC switch to OFF, then to FULL CARRIER.

Is the AFC LOCK lamp glowing?

Action — YES: Step 6.
NO: Suspect a fault in the input attenuator circuit (L1 to L4, D2 to D4, etc.).

TABLE 11 (Cont'd)

STEP 6	Decrease the signal generator output level to 1 microvolt e.m.f. Does the AFC LOCK lamp extinguish?
Action	YES: Step 7. NO: Suspect incorrect adjustment of R87 (Chap. 2-5) or a fault in the area of G14.
STEP 7	After a one minute time interval, increase the signal generator output level to 100 millivolts e.m.f. Does the AFC LOCK lamp glow?
Action	YES: Step 8. NO: Suspect a fault in the area of the 'hold' (TR17, TR19, TR21) or a drift in the signal generator frequency.
STEP 8	Slowly tune the signal generator 500Hz each side of 3MHz. Does the AFC LOCK lamp remain glowing?
Action	YES: Step 9. NO: Suspect that the frequency range of the 7MHz v.c.o. (TR1) is incorrect, or the signal generator tuning too rapid.
STEP 9	Slowly tune the signal generator 500Hz each side of 3MHz whilst observing the front-panel meter. Does the meter indication follow the tuning of the signal generator and remain within the AFC scale?
Action	YES: No fault apparent. NO: Suspect that the frequency range of the 7MHz v.c.o. (TR1) is incorrect.
STEP 10	Use the oscilloscope to monitor board pin 16. Is a 1.4MHz signal displayed?
Action	YES: Step 11. NO: Suspect a fault on the filter board PS367 or faulty wiring.
STEP 11	Use the oscilloscope to monitor board pin 11. Is a 1MHz signal displayed?
Action	YES: Step 12. NO: Suspect a fault on the 34MHz generator board PM339 or faulty wiring.
STEP 12	Connect the oscilloscope to TP10. Is a 400kHz sine wave signal displayed, approximately 2.5V p-p?
Action	YES: Step 13. NO: Suspect a fault between board pin 16 and TP10 (input attenuator ML3, mixer ML12, TR10).

TABLE 11 (Cont'd)

STEP 13	Disconnect the signal generator. Connect the 1MHz signal from the 1MHz IN/OUT socket to the antenna socket. Tune the receiver to 1MHz. Connect the oscilloscope to TP8. Is a 1.6MHz signal displayed?
Action	YES: Step 14. NO: Suspect a faulty 1.6MHz oscillator (TR7, TR8).
STEP 14	Connect the digital frequency meter to TP8. Is a frequency of 1 600 000Hz displayed?
Action	YES: Step 15. NO: Step 24.
STEP 15	Connect the oscilloscope to ML8 pin 12. Is a 200kHz approximate square wave displayed?
Action	YES: Step 16. NO: Suspect fault in area of ML5.
STEP 16	Connect the oscilloscope to ML8 pin 11. Is a 3:2 ratio square wave displayed?
Action	YES: Step 17. NO: Suspect fault in area of ML5, TR2 or G2.
STEP 17	Disconnect the 1MHz signal from the antenna socket, and reconnect the signal generator. Set the signal generator to a frequency of 3MHz and set the output level to 100 millivolts r.m.s. Set the receiver frequency to 3 000.00kHz. Connect the oscilloscope to ML8 pin 12 and adjust the signal generator frequency to display a 200kHz square wave. Connect the oscilloscope to ML8 pin 9. Is the difference frequency signal displayed?
Action	YES: Step 18. NO: Suspect faulty ML8.
STEP 18	Connect the oscilloscope to ML10 pin 6. Are fixed-width pulses at the difference frequency displayed?
Action	YES: Step 19. NO: Suspect faulty ML10.
STEP 19	Connect the oscilloscope to ML20 pin 8. Are fixed-width pulses at the difference frequency displayed?
Action	NO: Step 20. YES: Suspect faulty relay RLA/1, R94, or fault on meter switching board.

TABLE 11 (Cont'd)

STEP 20	Connect the oscilloscope to ML20 pin 13. Is a steady +3V (approximately) indicated?
Action	NO: Step 21. YES: Step 30.
STEP 21	Connect the oscilloscope to the anode of D17 (junction with R100). Is a steady +5V (approximately) indicated?
Action	NO: Step 22. YES: Suspect a fault in the area of ML18, G16, G13.
STEP 22	Connect the oscilloscope to the collector of TR16 (can). Are positive-going 400kHz pulses displayed?
Action	YES: Step 23. NO: Suspect faulty TR16.
STEP 23	Connect the oscilloscope to TP12. Is a steady +11V (approximately) indicated?
Action	YES: Suspect incorrect setting of R87 (Chap. 2-5) or faulty ML21. NO: Suspect a fault in the area of TR15.
STEP 24	Connect the oscilloscope to the collector (can) of TR16. Are positive-going pulses displayed, approximately 10V peak-to-peak?
Action	YES: Step 25. NO: Suspect a fault in the area of ML8/ML11.
STEP 25	Connect the oscilloscope to TP12. Is a low frequency a.c. signal displayed?
Action	YES: Step 26. NO: Suspect a fault in the area of TR15.
STEP 26	Connect the oscilloscope to TP15. Is a square wave signal displayed?
Action	YES: Step 27. NO: Suspect a fault in the area TR23, TR24, TR25.

TABLE 11 (Cont'd)

STEP 27	Connect the oscilloscope to the collector (can) of TR14. Are positive-going pulses, approximately 10V peak-to-peak, displayed?
Action	YES: Step 28. NO: Suspect a fault in the area of TR14.
STEP 28	Connect the oscilloscope to TP11. Is a low frequency a.c. signal displayed?
Action	YES: Step 29. NO: Suspect a fault in the area of TR13.
STEP 29	Connect the oscilloscope to TP5. Is a filtered version of the TP11 signal displayed?
Action	YES: Suspect a faulty 1.6MHz oscillator (TR7,TR8). NO: Suspect a fault in the area of ML15.
STEP 30	Connect the oscilloscope to ML20 pin 12. Is a steady +3V (approximately) level indicated?
Action	YES: Step 31. NO: Step 32.
STEP 31	Connect the oscilloscope to ML20 pin 10. Is a steady +3V (approximately) level indicated?
Action	NO: Step 32. YES: Suspect faulty G15.
STEP 32	Connect the oscilloscope to TP6. Is a 1MHz square wave signal displayed?
Action	YES: Step 33. NO: Suspect a fault in the area of G1, G4, G6, G7.
STEP 33	Connect the oscilloscope to TP7. Is a 1MHz square wave signal displayed?
Action	YES: Step 34. NO: Step 36.

TABLE 11 (Cont'd)

STEP 34	Connect the oscilloscope to TP9. Are narrow fixed-width pulses displayed?
Action	YES: Step 35. NO: Suspect a faulty phase-comparator (ML9, G10), voltage control circuit (TR9, TR11, TR12), or incorrect 7MHz v.c.o voltage/frequency characteristic.
STEP 35	Connect the oscilloscope to ML9 pin 9. Are narrow fixed-width pulses displayed?
Action	YES: Suspect a fault in the area of ML14, G11, G12. NO: Suspect a faulty phase-comparator (ML9, ML10), voltage control circuit (TR9, TR11, TR12), or incorrect 7MHz v.c.o voltage/frequency characteristic.
STEP 36	Connect the oscilloscope to board pin 10. Is a 1MHz signal displayed?
Action	NO: Step 37. YES: Suspect a fault in the area of G1, G4, G8, G9, etc.
STEP 37	Connect the oscilloscope to TP1. Is a 7MHz signal displayed?
Action	YES: Suspect a fault in the area of ML4, G3, G5. NO: Suspect a faulty 7MHz v.c.o. (TR1).
STEP 38	Connect the oscilloscope to ML20 pin 6. Is OV indicated?
Action	NO: Step 39. YES: Suspect faulty R93, a wiring fault, or faulty lamp.
STEP 39	Connect the oscilloscope to ML20 pin 2. Is approximately +3V indicated?
Action	YES: Step 40. NO: Suspect a fault in the area of the ON/OFF switch, ML1, TR4.
STEP 40	Connect the oscilloscope to board pin 18 on the 34MHz generator board PM339. Is a 4:3 ratio 1MHz square wave displayed?
Action	YES: Step 41. NO: Suspect a wiring fault from pin 10 on the a.f.c. board

TABLE 11 (Cont'd)

STEP 41	Set the 1MHz INT/EXT switch on the rear panel to EXT. Connect the oscilloscope to TP11 on the 34MHz generator board PM339. Is a 4:3 ratio 1MHz square wave displayed?
Action	YES: Step 42. NO: Suspect a fault on the 34MHz generator board PM339, in the area of ML5, or no earth applied to board pin 19.
STEP 42	Set the 1MHz INT/EXT switch to INT. Unsolder and remove the coaxial cable from board pin 16 on the a.f.c. board (the screen may be left connected to pin 15). Connect the output of the signal generator, set to a frequency of 1.400MHz and an output level of 100 millivolts e.m.f., to pin 16. Connect the oscilloscope to TP10. Is a 400kHz signal displayed?
Action	YES: Step 43. NO: Suspect a fault between board pin 16 and TP10 (input attenuator, ML3, mixer, ML12, TR10).
STEP 43	Connect the oscilloscope to ML17 pin 12. Is approximately +3V indicated?
Action	YES: Step 44. NO: Suspect a fault in the area of the ON/OFF switch (ML1, TR4), ML17, or lock indicator circuit.
STEP 44	Connect the oscilloscope to TP6. Is a 25kHz approximate square wave signal displayed?
Action	YES: Step 45. NO: Suspect a fault in the area of G7, ML6, G6, G4.
STEP 45	Connect the oscilloscope to TP7. Is a 25kHz approximate square wave signal displayed?
Action	YES: Suspect a faulty lock-indicator circuit (G11, G12, ML14), faulty G14, or phase-comparator (ML9 to TP4). NO: Suspect a fault in the area of G8, G9, ML7.

TABLE 12

Fault-location : main power supply and regulator PM370

Note...

(1) If the +20V supply fails, then the +12V, +5V and -7V supplies will also fail.

(2) If the +12V supply fails, then the -7V supply will also fail.

(3) Before proceeding with the following checks, ensure that the SUPPLY fuse is serviceable, the voltage selector VS1 is correctly set, and the POWER switch is set to ON.

STEP 1	Connect the multimeter, set to the 50-volt d.c. range, between board pin 22 (positive) and chassis (earth). Can R19 be set for an indication on the multimeter of +20V plus or minus 0.5V?
Action	YES: Step 14. NO: Step 2.
STEP 2	Connect the multimeter between ML4 pin 7 (positive) and chassis. Does the multimeter indicate approximately +30V d.c.?
Action	YES: Step 3. NO: Suspect a faulty rectifier diode D4, capacitor 1C4, faulty transformer 1T1, or a wiring fault between 1T1 and board pins 37 and 38.
STEP 3	Connect the multimeter between board pin 22 (positive) and chassis. Is the multimeter indication higher or lower than +20V?
Action	HIGHER: Step 10. LOWER: Step 4.
STEP 4	Set the receiver power switch to OFF. Unsolder and disconnect all the leads connected to board pins 22 and 23. Set the POWER switch to ON. Connect the multimeter between board pin 22 and chassis. Can R19 now be set for an indication on the multimeter of +20V plus or minus 0.5V?
Action	NO: Step 5. YES: Suspect that receiver is drawing excessive current from the +20V supply (typically 175mA) or faulty current-limit resistor, R28 or R34.

TABLE 12 (Cont'd)

STEP 5	Set the receiver POWER switch to OFF. Reconnect the leads removed from board pins 22 and 23. Set the POWER switch to ON. Connect the multimeter, set to the 10-volt d.c. range, between ML4 pin 4 (positive) and chassis. Does the multimeter indicate +7.15V?
Action	YES: Step 6. NO: Suspect faulty ML4.
STEP 6	Connect the multimeter between ML4 pin 3 (positive) and chassis. Does the multimeter indicate +7.15V plus or minus 0.5V?
Action	YES: Step 7. NO: Suspect faulty R6, C3 or ML4.
STEP 7	Connect the multimeter, set to the 50-volt d.c. range, between ML4 pin 6 (positive) and chassis. Is the multimeter indication greater than +20V?
Action	YES: Step 8. NO: Suspect fault in the area of TR3.
STEP 8	Connect the multimeter, set to the 25-volt d.c. range, to measure in turn the voltages at pins 2 and 3 of ML4 each with respect to chassis. Is the voltage at pin 2 lower than the voltage at pin 3?
Action	YES: Step 9. NO: Suspect faulty ML4.
STEP 9	Isolate ML4 pin 2 from the remaining circuity. Is the voltage at ML4, pin 2 still higher than than the voltage at ML4 pin 3?
Action	YES: Suspect faulty ML4. NO: Suspect that a component or a short-circuit is holding ML4 pin 2 at a high potential. Check for solder splashes, splayed wires, etc.
STEP 10	Connect the multimeter, set to the 10-volt d.c. range, between ML4 pin 4 (positive) and chassis. Does the multimeter indicate +7.15V?
Action	YES: Step 11. NO: Suspect faulty ML4.

TABLE 12 (Cont'd)

STEP 11	Connect the multimeter between ML4 pin 3 (positive) and chassis. Does the multimeter indicate +7.15V plus or minus 0.5V?
Action	YES: Step 12. NO: Suspect faulty R6, C4 or ML4.
STEP 12	Connect the multimeter, set to the 50-volt d.c. range, between ML4 pin 6 (positive) and chassis. Does the multimeter indicate between approximately +23 and +30V?
Action	YES: Step 13. NO: Suspect faulty TR3 or associated components.
STEP 13	Connect the multimeter, set to the 25-volt d.c. range, to measure the voltages at pins 2 and 3 of ML4, each with respect to chassis. Is the voltage at pin 2 higher than the voltage at pin 3?
Action	YES: Suspect faulty ML4. NO: Suspect a fault in the feedback path between the emitter of TR3 and ML4, pin 2.
STEP 14	Connect the multimeter between board pin 16 (positive) and chassis. Can R17 be set for an indication on the multimeter of +12V plus or minus 0.5V?
Action	YES: Step 27. NO: Step 15.
STEP 15	Connect the multimeter, set to the 50-volt d.c. range, between the collector of TR2 (board pin 14) and chassis. Does the multimeter indicate approximately +23V?
Action	YES: Step 16. NO: Suspect a faulty rectifier diode D3, capacitor 1C3, faulty winding on transformer 1T1 or a wiring fault between 1T1 and board pins 41 and 42.
STEP 16	Connect the multimeter, set to the 25-volt d.c. range, between board pin 16 (positive) and chassis. Is the multimeter indication higher or lower than +12V?
Action	HIGHER: Step 23. LOWER: Step 17.

TABLE 12 (Cont'd)

STEP 17	Set the receiver POWER switch to OFF. Unsolder and disconnect all the leads connected to board pins 16, 17, 18, 19, 20 and 21. Set the POWER switch to ON. Connect the multimeter between board pin 16 and chassis. Can R17 now be set for an indication on the multimeter of +12V plus or minus 0.5V?
Action	NO: Step 18. YES: Suspect that receiver is drawing excessive current from the +12V supply (typically 1.1A) or faulty current-limit resistor, R31.
STEP 18	Set the receiver POWER switch to OFF. Reconnect the leads removed from board pins 16, 17, 18, 19, 20 and 21. Set the POWER switch to ON. Connect the multimeter, set to the 10-volt d.c. range, between ML3 pin 4 (positive) and chassis. Does the multimeter indicate +7.15V?
Action	YES: Step 19. NO: Suspect faulty ML3.
STEP 19	Connect the multimeter between ML3, pin 3 (positive) and chassis. Does the multimeter indicate +7.15V plus or minus 0.5V?
Action	YES: Step 20. NO: Suspect faulty R5, C2 or ML3.
STEP 20	Connect the multimeter, set to the 25-volt d.c. range, between ML3 pin 6 (positive) and chassis. Does the multimeter indicate lower than +12V?
Action	YES: Step 21. NO: Suspect faulty TR2 or 1TR3.
STEP 21	Connect the multimeter to measure, in turn, the voltages at pins 2 and 3 of ML3, each with respect to chassis. Is the voltage at pin 2 lower than the voltage at pin 3?
Action	YES: Suspect faulty ML3. NO: Step 22.
STEP 22	Isolate ML3 pin 2 from the remaining circuitry. Is the voltage at ML3 pin 2 still higher than the voltage at ML3 pin 3?
Action	YES: Suspect faulty ML3. NO: Suspect that a component or a short-circuit is holding ML3 pin 2 at a high potential. Check for solder splashes, splayed wires etc.

TABLE 12 (Cont'd)

STEP 23	Connect the multimeter, set to the 10-volt d.c. range, between ML3 pin 4 (positive) and chassis. Does the multimeter indicate +7.15V?
Action	YES: Step 24. NO: Suspect faulty ML3.
STEP 24	Connect the multimeter between ML3 pin 3 (positive) and chassis. Does the multimeter indicate +7.15V plus or minus 0.5V?
Action	YES: Step 25. NO: Suspect faulty R5, C2 or ML3.
STEP 25	Connect the multimeter, set to the 25-volt d.c. range, between ML3 pin 6 (positive) and chassis. Does the multimeter indicate between +15V and +20V?
Action	YES: Step 26. NO: Suspect faulty TR2 or 1TR3.
STEP 26	Connect the multimeter to measure, in turn, the voltages at pins 2 and 3 of ML3, each with respect to chassis. Is the voltage at pin 2 higher than the voltage at pin 3?
Action	YES: Suspect faulty ML3. NO: Suspect a fault in the feedback path between the emitter of 1TR3 and ML3 pin 2.
STEP 27	Connect the multimeter, set to the 10-volt d.c. range, between board pin 10 (positive) and chassis. Can R3 be set for an indication on the multimeter of +5V plus or minus 0.5V?
Action	YES: Step 40. NO: Step 28.
STEP 28	Connect the multimeter, set to the 25-volt d.c. range, between the collector of TR1 (board pin 8) and chassis. Does the multimeter indicate approximately +14.5V?
Action	YES: Step 29. NO: Suspect faulty rectifier diode D2, capacitor 1C2, faulty transformer 1T1 or a wiring fault between 1T1 and board pins 45 and 46.
STEP 29	Connect the multimeter, set to the 10-volt d.c. range, between board pin 10 (positive) and chassis. Is the multimeter indication higher or lower than +5V?
Action	HIGHER: Step 36. LOWER: Step 30.

TABLE 12 (Cont'd)

STEP 30	Set the receiver POWER switch to OFF. Unsolder and disconnect all the leads from board pins 10 and 12. Set the POWER switch to ON. Connect the multimeter between board pin 10 (positive) and chassis. Can R3 now be set for an indication on the multimeter of +5V plus or minus 0.5V?
Action	NO: Step 31. YES: Suspect that receiver is drawing excessive current from the +5V supply (typically 2.2A) or faulty current limit resistors R27, R30.
STEP 31	Set the receiver POWER switch to OFF. Reconnect the leads removed from board pins 10 and 12. Set the POWER switch to ON. Connect the multimeter between ML2 pin 4 (positive) and chassis. Does the multimeter indicate +7.15V?
Action	YES: Step 32. NO: Suspect faulty ML2.
STEP 32	Connect the multimeter between ML2 pin 3 (positive) and chassis. Does the multimeter indicate +5V plus or minus 0.5V?
Action	YES: Step 33. NO: Suspect faulty R2, R3, R4 or C4.
STEP 33	Connect the multimeter between ML2 pin 6 (positive) and chassis. Does the multimeter indicate lower than +5V?
Action	YES: Step 34. NO: Suspect faulty TR1 or 1TR2.
STEP 34	Connect the multimeter to measure, in turn, the voltages at pins 2 and 3 of ML2, each with respect to chassis. Is the voltage at pin 2 lower than the voltage at pin 3?
Action	YES: Suspect faulty ML2. NO: Step 35.
STEP 35	Isolate ML2 pin 2 from the remaining circuitry. Is the voltage at ML2 pin 2 still higher than the voltage at ML2 pin 3?
Action	YES: Suspect faulty ML2. NO: Suspect that a component or a short-circuit is holding ML2 pin 2 at a high potential. Check for solder splashes, splayed wires, etc.

TABLE 12 (Cont'd)

STEP 36	Connect the multimeter between ML2 pin 4 (positive) and chassis. Does the multimeter indicate +7.15V?
Action	YES: Step 37. NO: Suspect faulty ML2.
STEP 37	Connect the multimeter between ML2 pin 3 (positive) and chassis. Does the multimeter indicate +5V plus or minus 0.5V?
Action	YES: Step 38. NO: Suspect faulty R2, R3, R4 or C4.
STEP 38	Connect the multimeter, set to the 25-volt d.c. range, between ML2 pin 6 (positive) and chassis. Does the multimeter indicate between approximately +8 and +20V?
Action	YES: Step 39. NO: Suspect faulty TR1 or 1TR2.
STEP 39	Connect the multimeter, set to the 10-volt d.c. range, to measure the voltages at pins 2 and 3 of ML2, each with respect to chassis. Is the voltage at pin 2 higher than the voltage at pin 3?
Action	YES: Suspect faulty ML2. NO: Suspect a fault in the feedback path from the emitter of 1TR2 and ML2 pin 2.
STEP 40	Connect the multimeter between board pin 5 (negative) and chassis. Can R8 be set for an indication on the multimeter of -7V plus or minus 0.5V?
Action	YES: No fault apparent. NO: Step 41.
STEP 41	Connect the multimeter, set to the 25-volt d.c. range, between board pin 1 (positive) and chassis. Does the multimeter indicate approximately +10V?
Action	YES: Step 42. NO: Suspect a faulty rectifier diode D1, capacitor 1C1, faulty transformer 1T1, or a wiring fault between 1T1 and board pins 49 and 50.
STEP 42	Connect the multimeter between board pin 5 (negative) and chassis. Is the multimeter indication higher or lower than -7V?
Action	HIGHER: Step 49. LOWER: Step 43.

TABLE 12 (Cont'd)

STEP 43	Set the receiver POWER switch to OFF. Unsolder and disconnect all the leads connected to board pins 5 and 6. Set the POWER switch to ON. Connect the multimeter, set to the 10-volt d.c. range, between board pin 5 (negative) and chassis. Can R8 now be set for an indication on the multimeter of -7V plus or minus 0.5V?
Action	NO: Step 44. YES: Suspect that receiver is drawing excessive current from the -7V supply (typically 500mA) or faulty current-limit resistor, R26, R29.
STEP 44	Set the receiver POWER switch to OFF. Reconnect the leads removed from board pins 5 and 6. Set the POWER switch to ON. Connect the multimeter between ML1 pin 4 (positive) and the case of ML1. Does the multimeter indicate +7.15V?
Action	YES: Step 45. NO: Suspect faulty ML1.
STEP 45	Connect the multimeter between ML1 pin 3 (positive) and the case of ML1. Does the multimeter indicate +7.15V plus of minus 0.5V?
Action	YES: Step 46. NO: Suspect faulty R1, C11 or ML1.
STEP 46	Connect the multimeter between ML1 pin 6 (positive) and the case of ML1. Does the multimeter indicate lower than +7V?
Action	YES: Step 47. NO: Suspect faulty 1TR1.
STEP 47	Connect the multimeter to measure, in turn, the voltages at pins 2 and 3 of ML1, each with respect to the case of ML1. Is the voltage at pin 2 lower than the voltage at pin 3?
Action	YES: Suspect faulty ML1. NO: Step 48.
STEP 48	Isolate ML1 pin 2 from the remaining circuitry. Is the voltage at ML1 pin 2 still higher than the voltage at ML1 pin 3?
Action	YES: Suspect faulty ML1. NO: Suspect that a component or a short-circuit is holding ML1 pin 2 at a high potential. Check for solder splashes, splayed wires, etc.

TABLE 12 (Cont'd)

STEP 49	Connect the multimeter between ML1 pin 4 (positive) and the case of ML1. Does the multimeter indicate +7.15V?
Action	YES: Step 50. NO: Suspect faulty ML1.
STEP 50	Connect the multimeter between ML1 pin 3 (positive) and the case of ML1. Does the multimeter indicate +7.15V plus or minus 0.5V?
Action	YES: Step 51. NO: Suspect faulty R1, C11 or ML1.
STEP 51	Connect the multimeter, set to the 25-volt d.c. range, between ML1 pin 6 (positive) and the case of ML1. Does the multimeter indicate between approximately +9 and +12V?
Action	YES: Step 52. NO: Suspect faulty 1TR1.
STEP 52	Connect the multimeter, set to the 10-volt d.c. range, to measure in turn the voltages at pins 2 and 3 of ML1, each with respect to the case of ML1. Is the voltage at pin 2 higher than the voltage at pin 3?
Action	YES: Suspect faulty ML1. NO: Suspect a fault in the feedback path from the emitter of 1TR1 and ML1 pin 2.

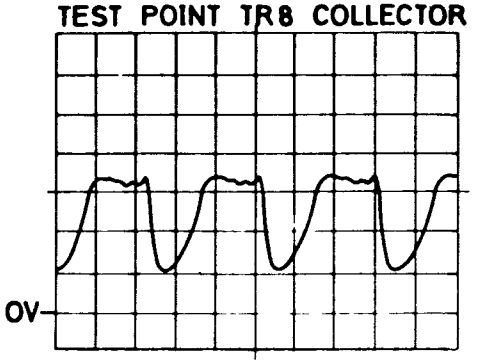
FAULT-LOCATION: A.F.C. BOARD PM664

18 The oscillograms in fig.1 and 2 are drawn from photographs of actual waveforms displayed on an oscilloscope. Because of component tolerances and differences in measuring equipment, observed waveforms may not appear identical to those shown. However, the shape of the waveform should be similar and the level within the limits stated.

19 The receiver and oscilloscope controls should be set in accordance with the information given in the diagram.

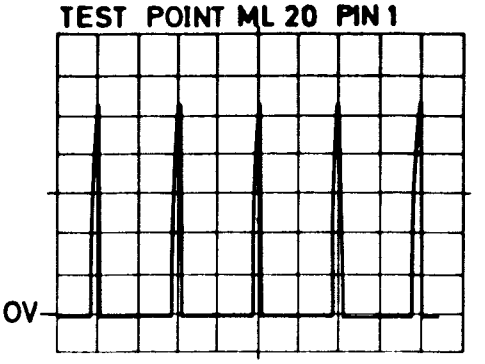
20 The waveform diagrams should be used in conjunction with the circuit diagram (Chap.2-1, Annex A) which indicates the circuit location of the waveforms and gives some typical DC voltage levels.

TEST POINT TR8 COLLECTOR



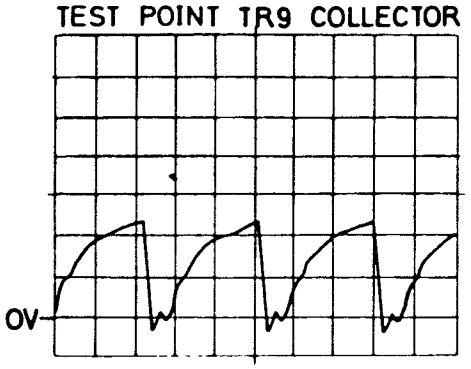
HORIZONTAL SCALE 50ns PER DIVISION
VERTICAL SCALE 2V PER DIVISION

TEST POINT ML 20 PIN 1



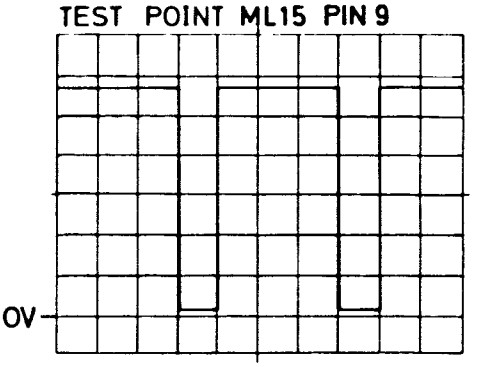
HORIZONTAL SCALE 2µs PER DIVISION
VERTICAL SCALE 2V PER DIVISION
LEVEL LIMITS TTL

TEST POINT TR9 COLLECTOR



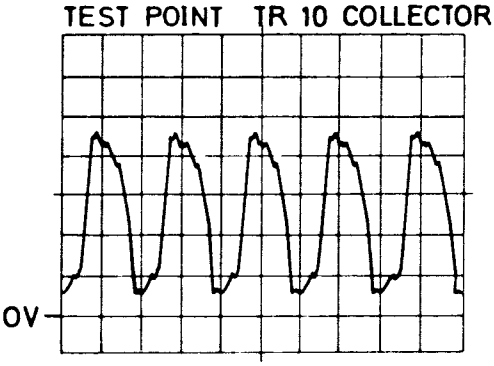
HORIZONTAL SCALE 50ns PER DIVISION
VERTICAL SCALE 2V PER DIVISION

TEST POINT ML15 PIN 9



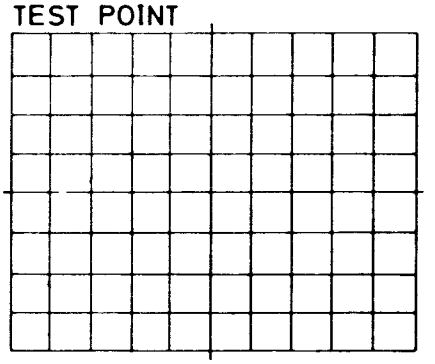
HORIZONTAL SCALE 2µs PER DIVISION
VERTICAL SCALE 2V PER DIVISION
LEVEL LIMITS TTL

TEST POINT TR 10 COLLECTOR



HORIZONTAL SCALE 0·5µs PER DIVISION
VERTICAL SCALE 2V PER DIVISION

TEST POINT

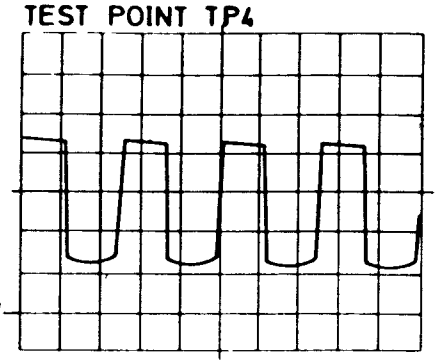


HORIZONTAL SCALE
VERTICAL SCALE
LEVEL LIMITS

NOTES 1 TTL LEVELS ARE ≤0·8V = '0' ≥2·4V = '1'
2 MEASUREMENTS MADE AT XX000·00kHz (DIGITS XX AS REQUIRED)
3. OSCILLOSCOPE INTENSITY MUST BE INCREASED TO DETECT NARROW PULSES.

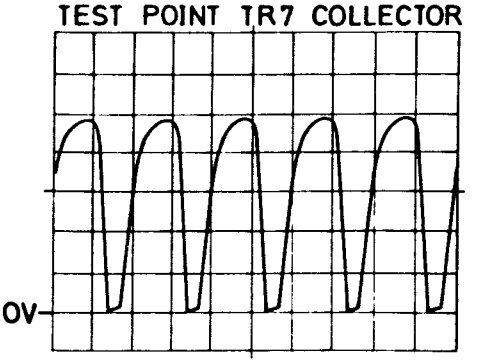
Fig.1 Waveforms: a.f.c. board PM664

TEST POINT TP4



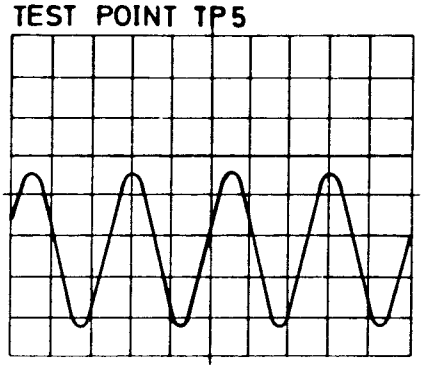
HORIZONTAL SCALE 1µs PER DIVISION
VERTICAL SCALE 2V PER DIVISION

TEST POINT TR7 COLLECTOR



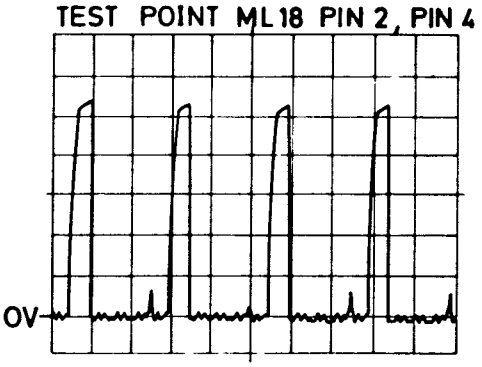
HORIZONTAL SCALE 0·5µs PER DIVISION
VERTICAL SCALE 2V PER DIVISION

TEST POINT TP5



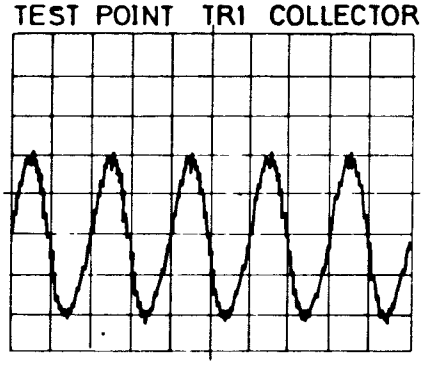
HORIZONTAL SCALE 1µs PER DIVISION
VERTICAL SCALE 1Va c PER DIVISION

TEST POINT ML18 PIN 2, PIN 4



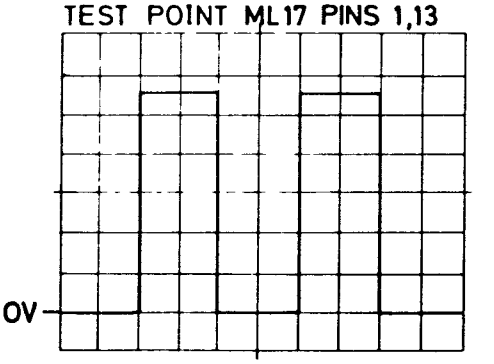
HORIZONTAL SCALE 2µs PER DIVISION
VERTICAL SCALE 2V PER DIVISION
LEVEL LIMITS TTL

TEST POINT TR1 COLLECTOR



HORIZONTAL SCALE 0·5µs PER DIVISION
VERTICAL SCALE 0·5Va.c. PER DIVISION

ML12 PINS 10,11
TEST POINT ML17 PINS 1,13



HORIZONTAL SCALE 2µs PER DIVISION
VERTICAL SCALE 2V PER DIVISION
LEVEL LIMITS TTL

NOTES : 1 TTL LEVELS ARE ≤0·8V = "0" ≥2·4V = "1"
2 MEASUREMENTS MADE AT XX000·00kHz (DIGITS XX AS REQUIRED)
3. OSCILLOSCOPE INTENSITY MUST BE INCREASED TO DETECT NARROW PULSES.

Fig.2 Waveforms: a.f.c. board PM664