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Colin Hinson

In the village of Blunham, Bedfordshire.



AP 116E-0755-6A2

July 1980

UK/FRR-627
REMOTELY-CONTROLLED HF RECEIVER
(Racal Type RA.1784)

BY COMMAND OF THE DEFENCE COUNCIL

Ministry of Defence

Sponsored for use in the

ROYAL AIR FORCE by D. Sigs (Air)

Prepared by Racal Communications Systems Ltd., Bracknell, Berks.

Publications authority : ATP/MOD (PE)

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the channel prescribed for the purpose in :

AP 100B-01 Order 0504

LETHAL WARNING

TAKE CARE!

VOLTAGES IN EXCESS OF 30 V (RMS) OR 50 V dc CAN BE LETHAL

MODIFICATION RECORD

A list of the modifications embodied in this publication is given in Topic-6A1, pages (vii) and (viii).

Maintenance manual (Parts 3 to 7)

RA. 1784 Serial Controlled HF Receiver



RACAL
The Electronics Group

Racal Communications Limited Western Road, Bracknell, RG12 1RG England
Tel: Bracknell (0344) 3244 Telex: 848166 Grams: Racal Bracknell.
Prepared by Central Handbooks Department, Racal Group Services Limited.
Printed in England

Ref. WOH 6247

Issue 3.4.79-200

LETHAL WARNING

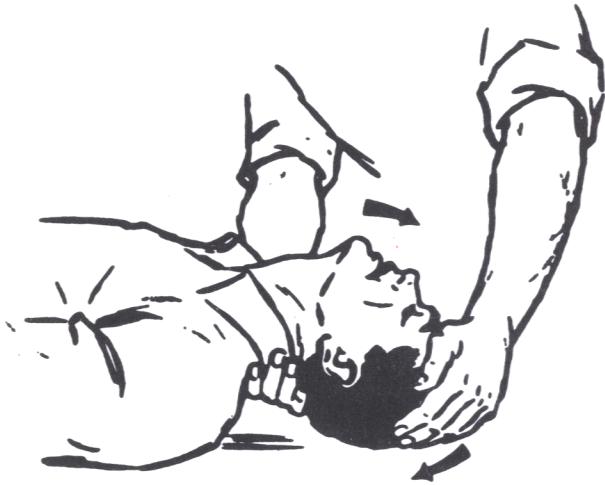
Voltages within this equipment are sufficiently high to endanger life.

Covers are NOT to be removed except by persons qualified and authorised to do so and these persons should always take extreme care once the covers have been removed.

Resuscitation instructions are given overleaf.

FIRST AID

in case of Electric Shock



1. Lay victim on his back.
2. Clear victim's mouth and throat.
3. Tilt victim's head back as far as possible and raise his head.
4. Pinch victim's nostrils.
5. Take a deep breath.
6. Cover the victim's mouth with your mouth and blow, watching his chest rise
Note: Blow forcefully into adults, but gently into children.
7. Move your face away to allow victim to breathe out, watching his chest fall.
8. Repeat first five to ten breaths at rapid rate; thereafter, take one breath every three to five seconds.
9. Keep victim's head back as far as possible all the time.

Have someone else send for a Doctor
Keep patient warm and loosen his clothing

**DO NOT Give liquids
until patient is conscious**

C H A P T E R 2
=====

R F U N I T
=====

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CHAPTER 1

FUNCTIONAL DESCRIPTION

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CHAPTER 1

FUNCTIONAL DESCRIPTION

INTRODUCTION

1. This chapter briefly describes the operation of the RF, IF and AF section of the receiver, and should be read in conjunction with the block diagram given in fig. 1.1. This diagram includes the optional half-octave filter board and the optional ISB IF board, which is the same as the main IF board.

RF BOARD

2. The received signal at the antenna, in the frequency range 15 kHz to 30 MHz, is applied to the RF board via the re-radiation filter. This unit also contains a 500 mA antenna surge protection fuse and a spark gap.
3. The output signal from the re-radiation filter is applied to a wideband protection stage which controls a normally-energized relay, RLA/1, such that when the r.m.s. level of the received signal at the antenna exceeds approximately 10V emf, the relay contact is opened and the RF path is broken.
4. From relay contact RLA1, the received signal is applied to a 0 to 30 MHz bandpass filter and thence via LK3, or the optional half-octave filter board and links LK1, LK2, to an in-band protection stage. The half-octave filter board contains eleven bandpass filters, one of which is automatically selected by the applied frequency setting data; each filter provides an additional 20 dB attenuation half an octave removed from the appropriate band edge.
5. The in-band protection stage opens relay contact RLC1 when signal levels in the passband of the selected half-octave filter exceed r.m.s. levels of 3V emf at the antenna socket. The relay contact is also opened when a 0V signal is applied to the MUTE terminal on the receiver rear panel (either directly or via the serial data and the interface unit).
6. The received signal at LK3 (or LK2) is also applied to an attenuator control circuit which controls relay RLB. When the r.m.s. level of the received signal at the antenna exceeds approximately 300 mV emf relay contact RLB1 opens and the received signal is applied via a 20 dB attenuator to the RF amplifier. The relay contact closes when the received signal level subsequently falls to approximately 100 mV emf. The attenuator control circuit may be inhibited if not required by the setting of a link on the RF board.
7. The RF amplifier has a wideband characteristic and provides a gain, from board input to board output, of approximately three times. The amplified output signal is applied via a 0 to 30 MHz low pass filter to the first mixer board.

FIRST MIXER BOARD

8. Mixer 1 combines the output signal from the RF board with the 35.415 to 65.4 MHz local oscillator signal from the synthesizer to produce the first intermediate frequency output at 35.4 MHz. The local oscillator signal is applied to the mixer stage via a drive amplifier and one of two bandpass filters; for receiver operating frequencies up to 3.99999 MHz the diode switching circuits route the signal via a 35.415 to 39.4 MHz bandpass filter, whilst for frequencies of 4 MHz and above the signal is routed via a 39.4 to 65.4 MHz bandpass filter. The output signal from the drive amplifier is also applied to a meter drive circuit, the output from which is applied to the receiver front panel meter via the interface unit (Part 4).
9. The output signal from the mixer is applied to a 35.4 MHz bandpass crystal filter and thence via a tuned 35.4 MHz buffer amplifier to the second mixer board.

SECOND MIXER BOARD

10. The 35.4 MHz first IF signal from the first mixer board is applied via a gain-controlled amplifier and bandpass filter to mixer 2 where it is mixed with the filtered and amplified 34 MHz signal from the synthesizer. The output signal from the mixer is applied via a 1.4 MHz low-pass filter to a variable attenuator (maximum attenuation approximately 20 dB). The gain of the buffer output amplifier is preset to obtain a voltage gain from board input to board output, of approximately 26 dB.
11. The stage gain of the input amplifier, and the attenuation level of the variable attenuator, are controlled by the d.c. output signal from the AGC combiner; this stage combines the AGC output signals from the main IF and (where fitted) the ISB IF boards, and produces a d.c. output voltage, the level of which is equal to the higher of the two input voltage levels.

IF FILTER BOARD

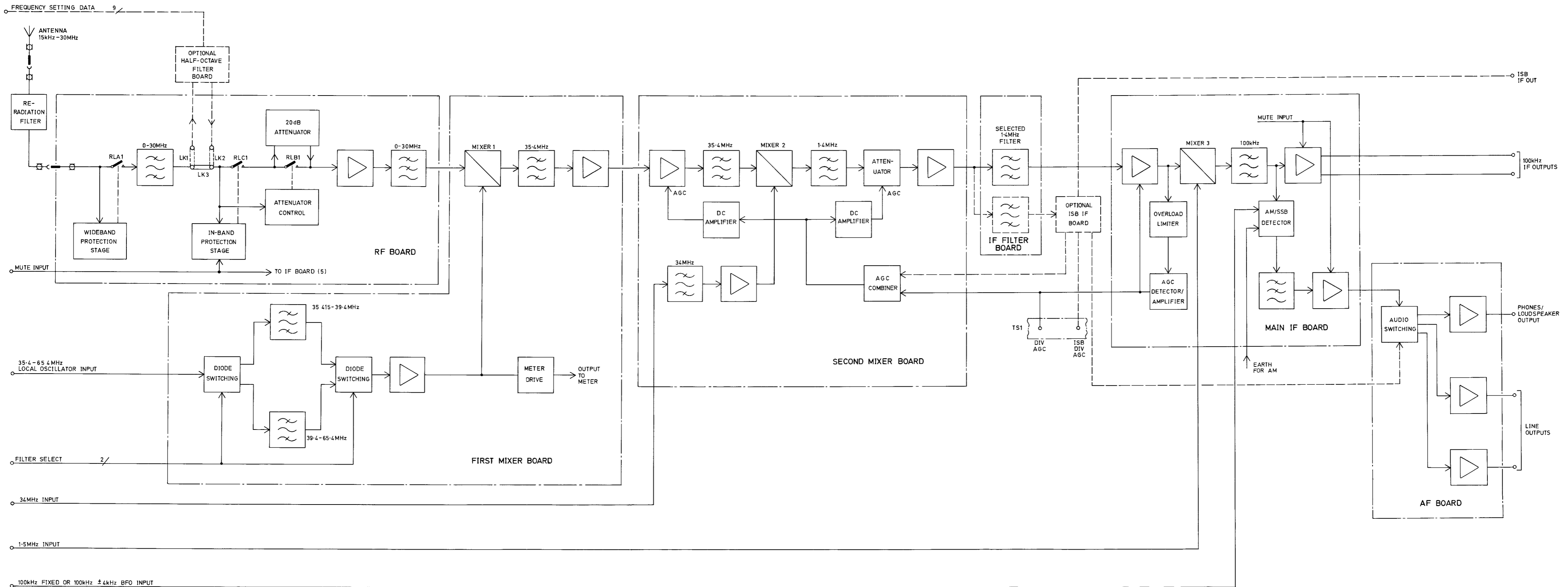
12. A total of six 1.4 MHz crystal filters may be fitted to the IF filter board. In standard production receivers two filter positions are occupied by the mode-selected SSB or ISB filters which allows up to four symmetrical filters to be fitted. If, however, a standard receiver is equipped with the AFC facility, a carrier filter is fitted which limits the number of symmetrical filters to three. If the receiver is equipped say, for USB only, then space is available for the fitting of five symmetrical filters.
13. Filter switching is accomplished using transmission gates which are controlled by logic '0' signals from the interface unit. Due to inversion within the receiver, the filter selected for USB operation has LSB characteristics and that selected for LSB operation has USB characteristics. In SSB receivers the 1.4 MHz output signal from the selected filter is applied to the main IF board; in ISB versions (when ISB is selected) a second output signal is applied to the ISB IF board.

IF BOARD

14. The optionally fitted ISB IF board is identical to the main IF board. The 1.4 MHz output signal from the IF filter board is applied to a gain controlled IF amplifier and then to mixer 3 where it is mixed with the 1.5 MHz signal from the synthesizer. The difference frequency output from the mixer is applied via a 100 kHz bandpass filter to the AM and SSB detectors, and also via a further amplifier to the 100 kHz output sockets on the receiver rear panel. For SSB/ISB modes a product detector is used which receives a fixed 100 kHz input signal from the synthesizer; for the CW mode, a variable 100 kHz signal (plus or minus up to 4 kHz in 10 Hz steps) is used. When the AM mode is selected, the 100 kHz output signal from the synthesizer is switched off, and an envelope detector is selected by the application of a 0V signal from the interface unit. The output signal from the detector is applied via a low-pass filter and an audio pre-amplifier stage to the AF board.
15. An output signal from the gain controlled input amplifier is applied via an overload limiter stage to the AGC detector and amplifier stages. These include the AGC time constant circuits, and the d.c. output voltage, the level of which is proportional to the level of the IF input signal, is applied to the input amplifier and also to the AGC combiner on the second mixer board.
16. The mute input signal to the 100 kHz output amplifier and the audio pre-amplifier is routed from the rear panel MUTE terminal. When an earth is applied to this terminal (either directly at the rear panel or via the serial data and the interface unit), the 100 kHz and audio output signals are switched off.

AF BOARD

17. The AF board contains three gain-controlled audio amplifiers; one provides the audio output to the phones and loudspeaker, whilst the remaining two provide audio line outputs. The audio input switching is controlled by the interface unit in accordance with the control settings at the control panel. Note that for SSB receivers, or ISB receivers set for SSB operation, the two audio line amplifiers are fed from a common input. The preset gain-adjustment potentiometers for the three amplifiers are mounted on the receiver front panel (which forms part of the interface unit - Part 4).



CHAPTER 2

RF UNIT

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CHAPTER 2

RF UNIT

INTRODUCTION

1. This chapter describes the re-radiation filter, RF board and the optional half-octave filter board, which are mounted in the RF unit. The circuit diagram of the re-radiation filter is given in fig. 2.1, the circuit of the RF board is given in fig. 2.2, and the circuit diagram of the half-octave filter board is given in fig. 2.4.

RE-RADIATION FILTER

2. The re-radiation filter is housed in a small metal box which is mounted on the rear face of the RF unit. It carries the antenna socket, together with a protection fuse and a spark gap. The RF connection to the RF board is made via a flying lead terminated in a BNC connector. Re-radiation with the antenna input terminated into 50 ohms is less than 10 microvolts.

RF BOARD PS514

Wideband Protection Stage

3. The received signal from the re-radiation filter is applied to the wideband protection stage via board pin 1 and C1. Under normal reception conditions, TR5 is cut off; this allow TR7 to conduct, RLA/1 is energised and contact RLA1 is closed.

4. Should the amplitude of the received signal at the antenna socket exceed a pre-determined threshold level (set by C4), the detected output from TR2 causes TR5 to conduct; TR7 is thus turned off, RLA/1 is de-energised, and contact RLA1 opens to break the path of the RF signal. The threshold is set by C4 such that RLA/1 becomes de-energised for signals which exceed approximately 10V r.m.s. emf at the antenna socket.

5. From relay contact RLA1, the received signal is applied to a 0 to 30 MHz low-pass filter; the stop-band characteristic of this filter is designed to introduce at least 20 dB attenuation between 35.415 and 65.4 MHz (the range of the local oscillator signal from the synthesizer). The filtered output is routed by LK3, or LK1, the half-octave filter board and LK2 (para. 14) to the in-band protection stage (para. 6) and the attenuator control circuit (para. 8).

In-band Protection Stage

6. The in-band protection stage, which is similar to the wideband protection stage, is only operational in receivers equipped with the optional half-octave filter board (para. 14). Under normal reception conditions TR15 is cut off, TR16 is turned on and relay RLC/1 is energised; contact RLC1 is closed and the path of the RF signal is completed.

Should the amplitude of the received signals at the antenna socket, which are within the passband of the selected half-octave filter, exceed a pre-determined threshold level (set by C30), the detected output from TR14 causes TR15 to conduct; TR16 is turned off, RLC/1 is de-energised, and contact RCL1 opens to break the path of the RF signal.

7. The threshold is set by C30 such that RLC/1 becomes de-energised for in-band signals which exceed approximately 3V r.m.s. emf at the antenna socket.

Attenuator Control Circuit

8. From relay contact RLC1, the received signal is applied to the diode protection circuit, either via relay contact RLB1 and C24 or via a 20 dB attenuator, R30, R32, R33, and C24. Relay RLB/2 is controlled by the attenuator control circuit such that when the signal level at the board input exceeds approximately 250 mV r.m.s. emf (within the passband of the half-octave filter, if fitted), the relay is de-energised; RLB1 is opened, RLB2 is closed, and the attenuator is brought into circuit. The 20 dB attenuator may be linked out if not required by the setting of link LK5.

9. The attenuator control circuit comprises a high impedance FET input amplifier TR1, TR3, a 0 to 30 MHz wideband amplifier TR4, TR6, detector diode D4, buffer stage TR8, a Schmitt trigger TR9, TR10, and the relay driver stage TR11. Under normal reception conditions, TR9 is cut off, TR10 is turned on, and thus the conduction of TR11 energises relay RLB/2. Should the level of the input signal at the antenna socket exceed a pre-determined threshold level (set by R9), the detected output levels from TR6 causes increased conduction of TR8 which turns on TR9; TR10 is turned off and this turns off TR11 to de-energise RLB/2.

10. The fast rise/slow decay time constant presented by C23 and R29 provides a delay of approximately five seconds; this stops the switching action of the Schmitt trigger for transients which exceed the threshold level.

11. When the 20 dB attenuator is in circuit, the voltage level at the collector of TR10 (approximately +12V) is applied to board pin 10; this is routed to the interface unit and a signal is sent to the control panel via the revertive data to indicate that 20 dB must be added to the signal strength meter reading.

Diode Protection Circuit

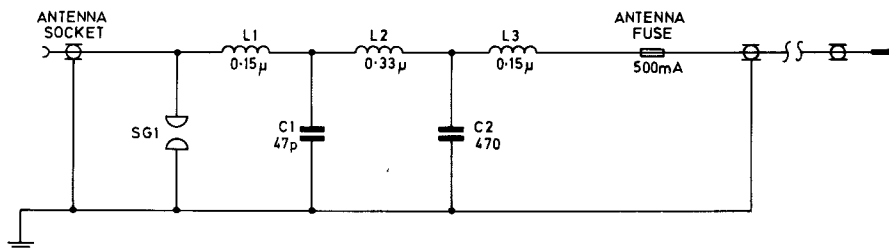
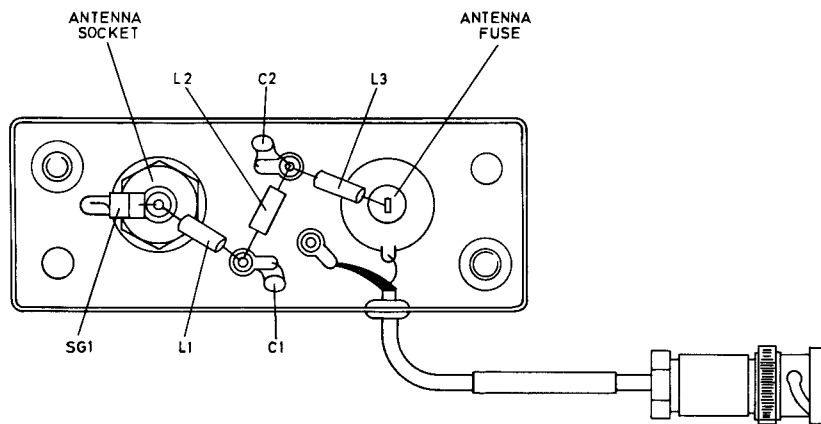
12. This circuit uses two fast-action switching diodes D7, D10, and a 6.2V zener diode D9. Under normal reception conditions the d.c. voltage at TP1 is approximately +16V, the voltage at the anode of D7 is approximately +12V and the voltage at the cathode of D10 is approximately +19V; thus both D7 and D10 are reverse biased. Should a high voltage transient signal be induced into the antenna (lightning, etc) which is too fast to operate the relay protection circuits, then the respective diode will conduct, i.e. D7 for negative and D10 for positive transients, to protect the RF amplifier stage.

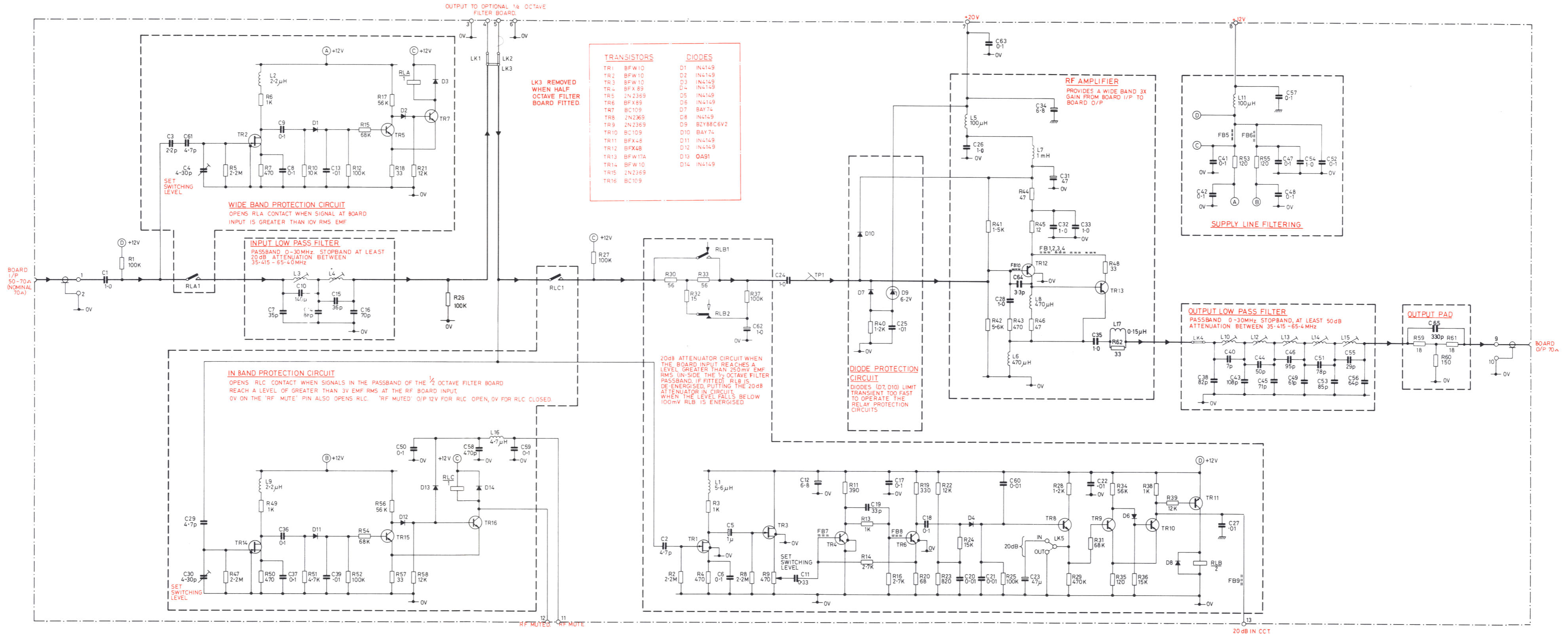
RF Amplifier

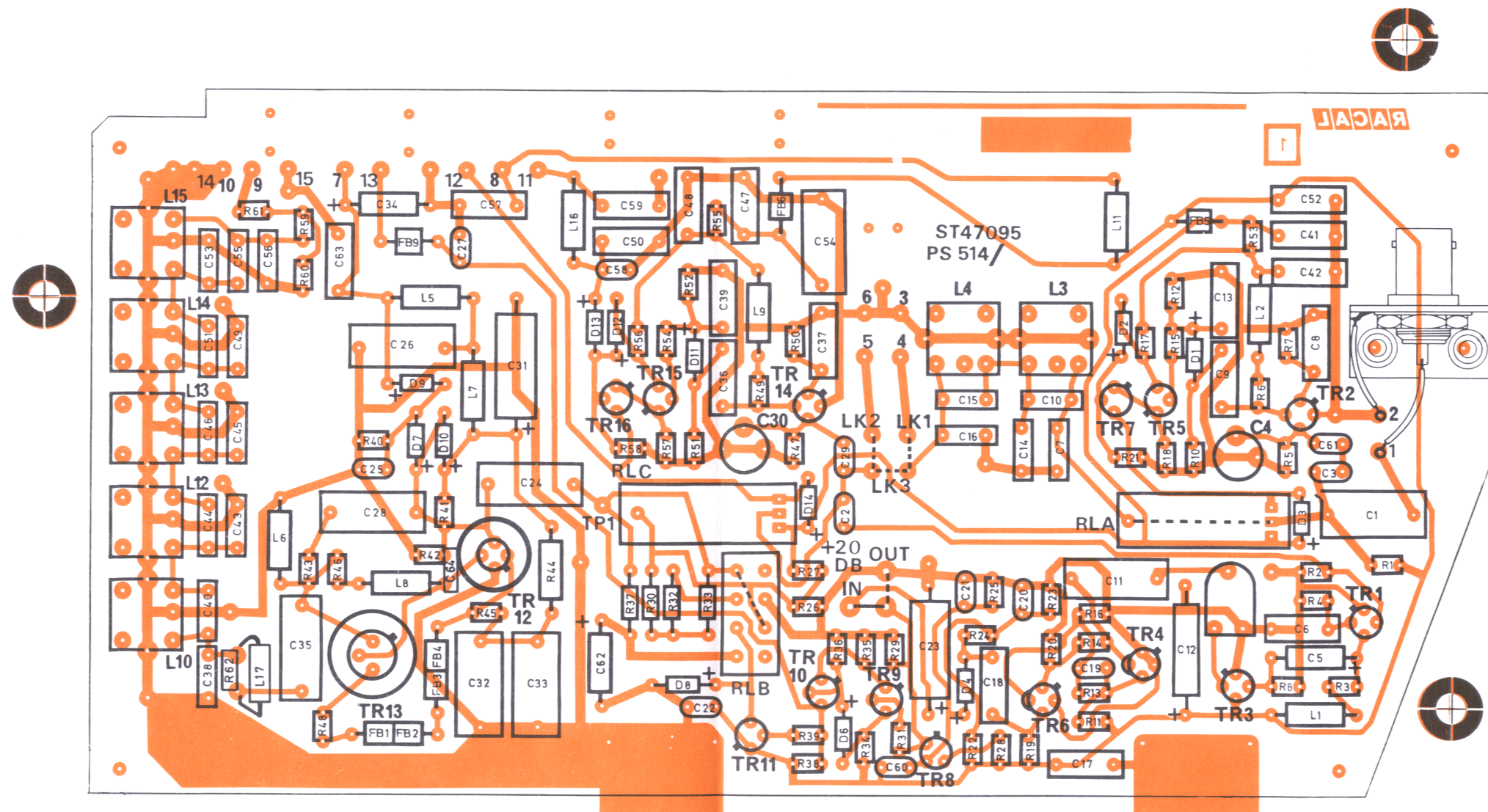
13. The RF amplifier stage TR12, TR13, has a wideband characteristic over the frequency range 15 kHz to 30 MHz, and provides a gain, from board input to board output, of approximately three times. The amplified output signal is coupled via C35, LK4, a 0 to 30 MHz low-pass filter, a 70 ohms impedance pad and board pin 7, to the first mixer board.

HALF-OCTAVE FILTER BOARD PS549

14. The optional half-octave filter board (fig. 2.4) contains ten bandpass filters, covering the frequency range 1 to 30 MHz, and a low-pass filter for frequencies below 1 MHz. Filter selection is achieved by the use of relays; the BCD frequency setting information from the decoder board, at board pins 5 to 13, is applied to a network of NOR gates, NAND gates and inverting buffers, and the appropriate relay is energised via an open-collector buffer/driver (ML4 or ML14).







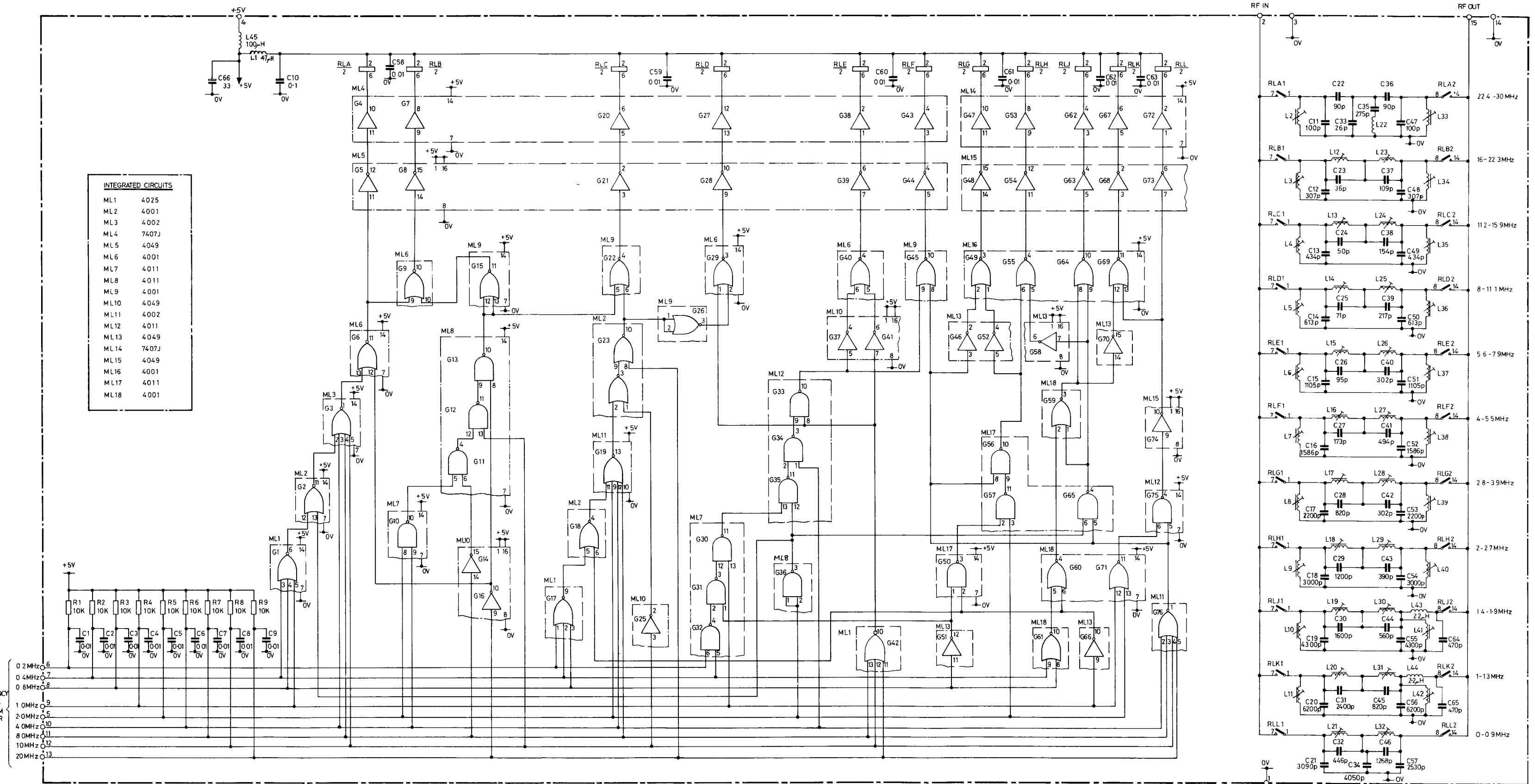
REFER TO MOD No A9599

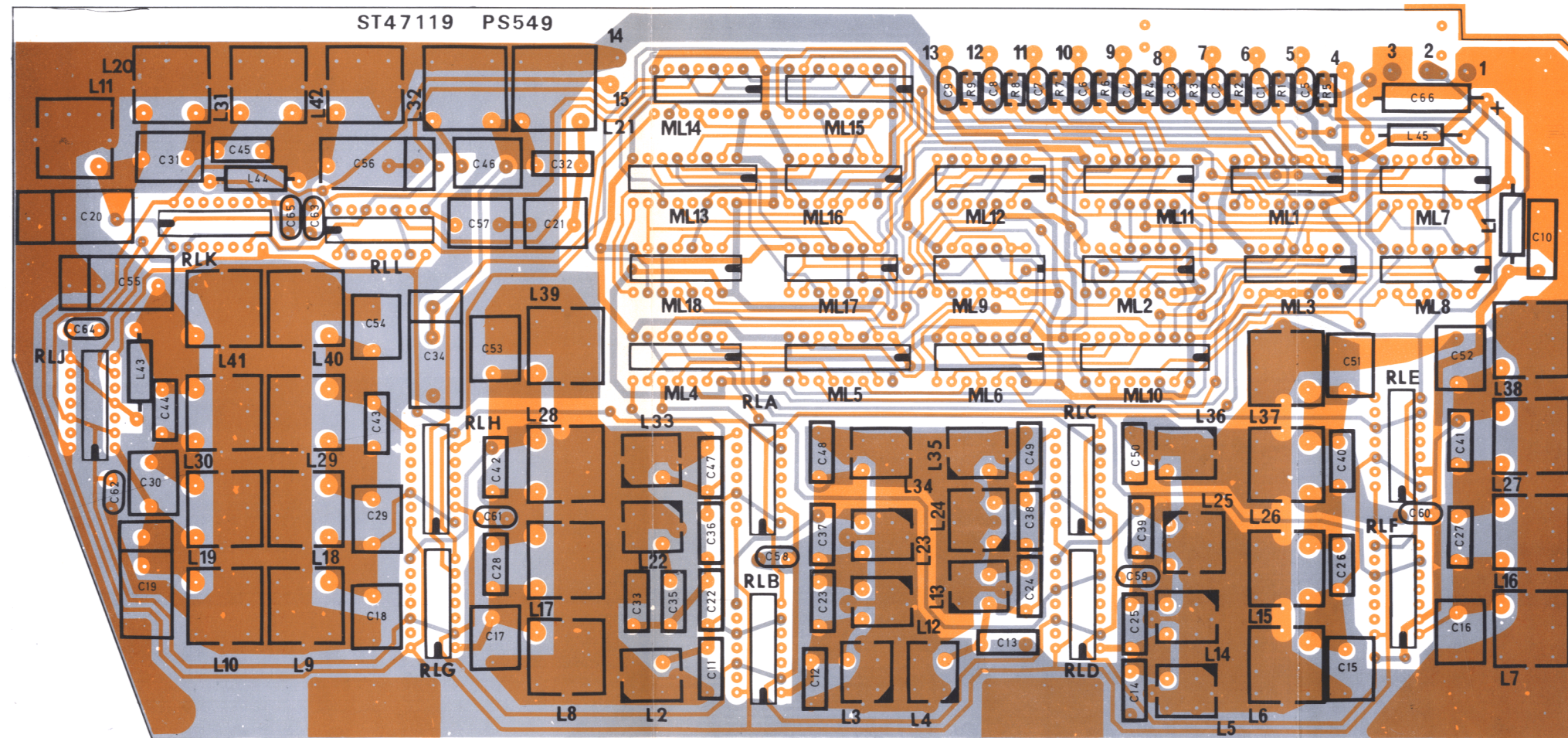
RACAL

WOH 6247	DA 47094/4	2-3
1		1/2
WOH 6247	DA 47054/4	2-3
1		2/2

Layout: R F Board

Part 3
Fig 2-3





RACAL			
WOH 6247	DA 47118 / 4	2-5	
1		1/3	
WOH 6247	DA 47118 / 4	2-5	
1		2/3	
WOH 6247	DA 47118 / 3	2-5	
1		3/3	

Layout: Half Octave Filter Board

CHAPTER 3

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FIRST MIXER BOARD PS512

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Layout: First Mixer Board PS512	3.2

CHAPTER 3

FIRST MIXER BOARD PS512

INTRODUCTION

1. The received RF signal from the RF board, in the frequency range 15 kHz to 30 MHz, is applied to the first mixer board where it is mixed with the filtered and amplified 35.415 to 65.4 MHz local oscillator signal from the synthesizer. The difference frequency output, at 35.4 MHz, is applied to a crystal bandpass filter and is then amplified before application to the second mixer board. A second output from the local oscillator drive amplifier is rectified to produce a d.c. output voltage which is proportional to the drive level; this voltage is applied to the front panel meter via the interface unit.
2. The circuit diagram of the first mixer board is given in fig. 3.1.

LOCAL OSCILLATOR FILTER SWITCHING

3. The local oscillator signal, at board pin 28, is applied to one of two bandpass filters, dependent on the receiver frequency range. For receiver frequencies in the range 15 kHz to 3.9 MHz, an earth is applied (via a diode) to board pin 29; this is routed to D2 via L3 and also to D4 via L15. Diode D2 is forward biased and opens a path for the local oscillator signal to a crystal notch filter (passband 35.415 to 39.4 MHz, with a notch frequency of 35.400 MHz) via C3, D2 and C9. Diode D4 is also forward biased and routes the output signal from the crystal filter to the drive amplifier via C34, D4, C41 and the impedance matching pad. Diodes D3 and D5 are reverse biased and thus isolate the LC bandpass filter.
4. For receiver frequencies in the range 4 to 30 MHz, an earth is applied (via a diode) to board pin 26; diodes D3 and D5 are forward biased, D2 and D4 are reverse biased, and the local oscillator signal is routed via C4, D3 and C7 to the LC bandpass filter. The output from this filter (passband 39.4 to 65.4 MHz) is then routed to the drive amplifier via C35, C42 and the impedance matching pad.

DRIVE AMPLIFIER

5. The mixer drive amplifier comprises a common-emitter pre-amplifier stage TR2, followed by an emitter-coupled differential power amplifier stage TR3, TR6. The balanced output signal is coupled by transformer T4 to the first mixer circuit (via T6) and also to the meter drive circuit (para. 6).

METER DRIVE CIRCUIT

6. The local oscillator drive signal output from transformer T4 is rectified by D6, smoothed, and then applied to a source follower TR9. R47 is adjusted for a front panel meter indication within the green band for a correct local oscillator drive level to the first mixer.

FIRST MIXER

7. The mixer is of the switching balanced-ring type and uses four N-channel insulated gate field effect transistors TR4, TR5, TR7 and TR8. The local oscillator signal is capacity coupled from T6 to the gate of each transistor whilst the RF input signal is coupled via T7 to the source of each transistor.
8. The transistors are switched in pairs, dependent on the direction of the applied local oscillator waveform (positive-going or negative-going); when the local oscillator signal at pin 5 is positive with respect to pin 7, transistors TR4 and TR8 are switched on whilst TR5 and TR7 are switched off. The RF input signal at T7 is then routed via TR4 and TR8 to the output transformer T5. Conversely, when pin 7 is positive with respect to pin 5, TR5 and TR7 are switched on, TR4 and TR8 are switched off, and the RF path is via TR5 and TR7.
9. The difference frequency output from the mixer, at 35.4 MHz, is coupled by T5 and LK2 to a 35.4 MHz crystal bandpass filter. In standard production receivers this filter (FL1) has a nominal bandwidth of ± 6 kHz. An optional narrow filter, nominal bandwidth ± 500 Hz (FL2), may also be fitted; this is selected on command from the interface unit which energises the relays.

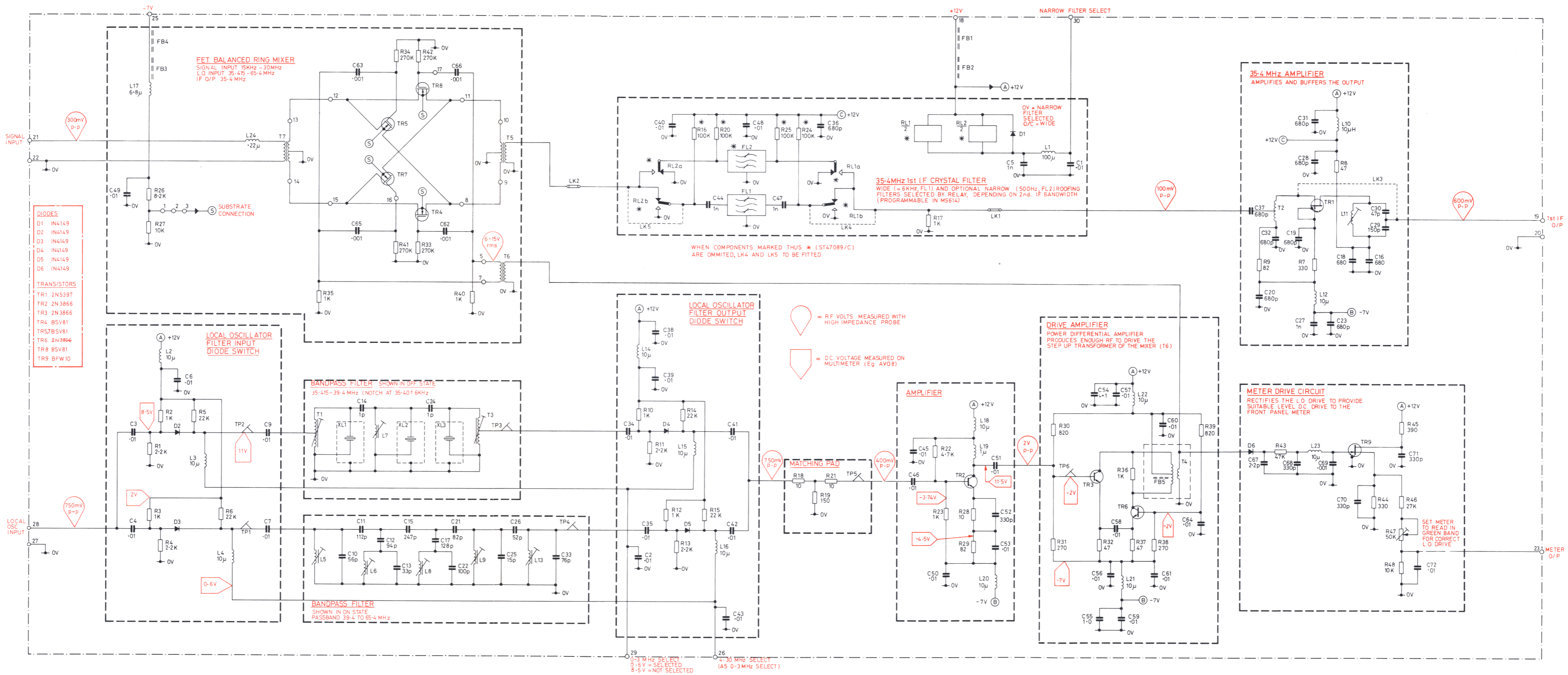
35.4 MHz BUFFER AMPLIFIER

10. The filtered 35.4 MHz output signal from the mixer is coupled by LK1 and C3 to the tuned buffer amplifier stage TR1 (LK3 is not fitted). Inductor L11 is tuned for a maximum output at 35.4 MHz which is applied to the second mixer board via board pin 19.

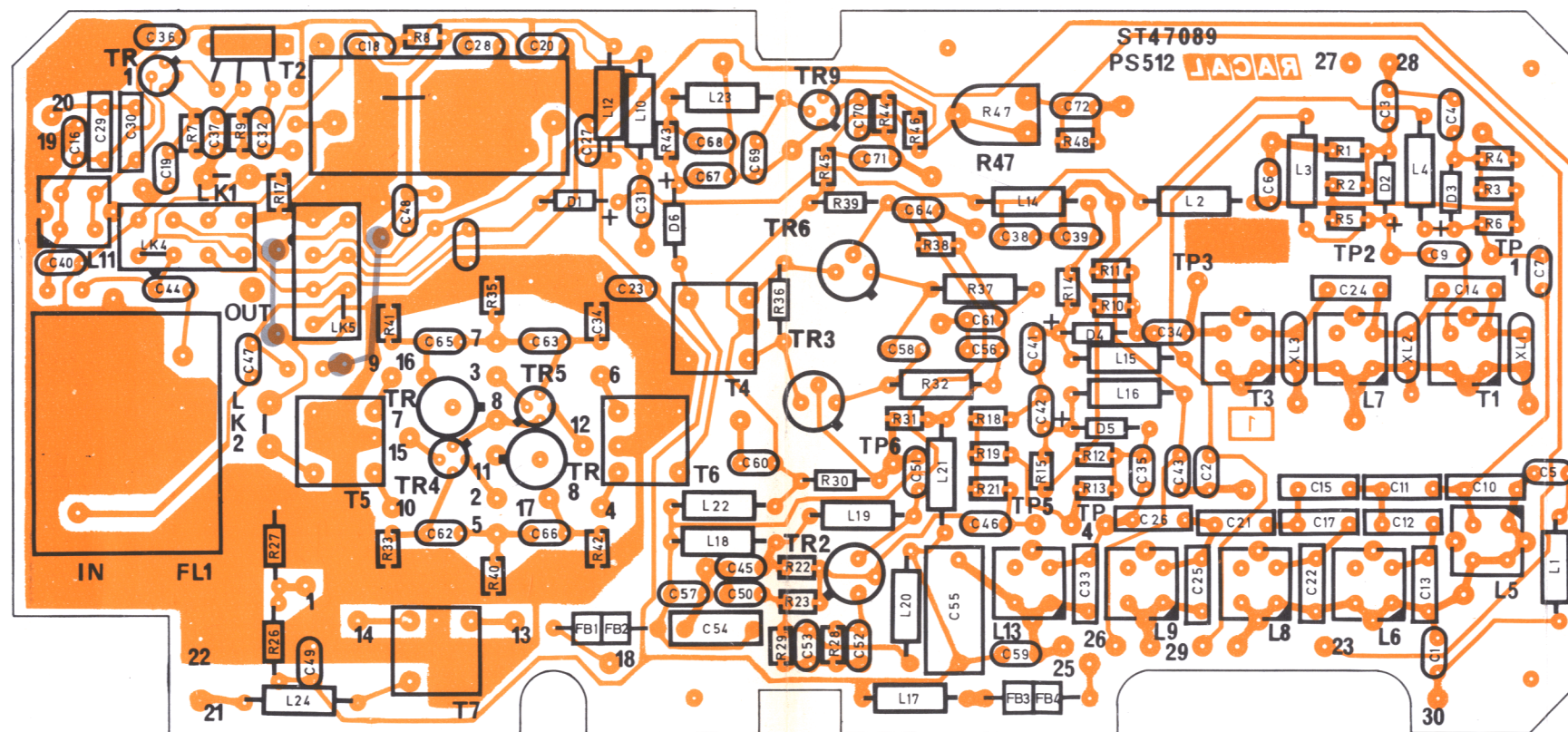
NOTE: BALANCED RING MIXER TRANSISTORS

The balanced ring mixer transistors TR4, TR5, TR7 and TR8 (type BSV81) are fitted as a matched quad, Racal part number 927897 (Manufacturer General Instruments). These transistors are colour coded (in accordance with the on-resistance with V_{gs} at 6V) and a failed transistor should be replaced with a similarly coded device. In an emergency situation, or where a degraded specification in respect of the response to external suprious signals is acceptable, then a mixture of devices with two only adjacent colours may be fitted.

<u>COLOUR</u>	<u>ON-RESISTANCE (ohms)</u>
BLACK	25 to 30
ORANGE	30 to 35
RED	35 to 40
GREY	40 to 45
YELLOW	45 to 50
GREEN	50 to 55
BLUE	55 to 60
VIOLET	60 to 65



RACAL		
WOH6247	DC47089	3/3-1
1		1/2
WOH6247	DC47089	3/3-1
2		2/2



WOH 6247	DA 47088/2	3-2
RACAL		2/3
WOH 6247	DA 47088/4	3-2
1		1/3
WOH 6247	DA 47088/3	3-2
1		3/3

Layout: First Mixer Board

Part 3
Fig. 3-2

CHAPTER 4
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SECOND MIXER BOARD PS513
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CHAPTER 4

SECOND MIXER BOARD PS513

INTRODUCTION

1. The 35.4 MHz IF output signal from the first mixer board is amplified and filtered before application to the second mixer; here it is mixed with the filtered and amplified 34 MHz signal from the synthesizer and the resultant 1.4 MHz output signal is applied via a voltage-controlled attenuator to a buffer amplifier stage. The board also contains an AGC voltage combiner; this stage combines the AGC voltages from the main IF and (where fitted) the ISB IF boards. The output is used to control the gain of the 35.4 MHz IF amplifier and the 1.4 MHz buffer amplifier. The circuit diagram of the board is given in fig. 4.1.

35.4 MHz IF AMPLIFIER

2. The 35.4 MHz IF input at board pin 14 is coupled by C2 to a gain-controlled amplifier stage TR1. The output signal from the tuned circuit L1, C6, C7 is coupled via C9 to a further amplifier stage TR5, and via C8 to a pair of PIN diodes D1, D2. The impedance of these diodes (which are parallel-connected for RF and appear across L1) is a function of the forward direct current flowing through the diodes; when no current is flowing the impedance is extremely high and this impedance is progressively reduced as the forward current rises. The current flowing through the diodes is set by the input attenuator controller, which in turn is controlled by the level of the AGC voltage from the AGC combiner. The amplified output signal is applied to the second mixer via LK1 and a 35.4 MHz bandpass filter.

INPUT ATTENUATOR CONTROLLER

3. The AGC voltage output from emitter follower TR6 (the level of which is the greater of the two inputs $V_{agc 1}$ and $V_{agc 2}$) is applied to a differential amplifier TR2, TR4. The threshold level at which TR2 begins to conduct is defined by R8 and TR4; R8 is adjusted so that when the signal level at the antenna socket reaches 0.75 mV emf, the level of the AGC voltage output from the emitter of TR6 is just sufficient to cause TR2 to conduct. TR3 is a current source for TR2 and TR4, and thus limits the maximum current flow through the PIN diodes.

4. Since the conduction of TR2 controls the current flow through the two PIN diodes, an increase in the applied AGC voltage increases the current flow through the diodes and the output level from TR1 is maintained.

SECOND MIXER DRIVE AMPLIFIER

5. The 34 MHz signal from the synthesizer, at board pin 8, is applied via a 34 MHz bandpass filter to a drive amplifier stage TR9. The amplified output, at approximately 8V peak-to-peak, is applied as the switching input to the second mixer.

SECOND MIXER

6. This is a balanced switching diode mixer comprising two transformers T1, T2, and four diodes D3 to D6. The 35.4 MHz signal is applied via LK2 to the primary winding of T1, and the 34 MHz switching input is applied to the centre-tapped secondary windings of T1 via R20 and R23. The output signal from T2 is applied via a 1.4 MHz low-pass filter and a voltage-controlled attenuator to the output buffer amplifier.

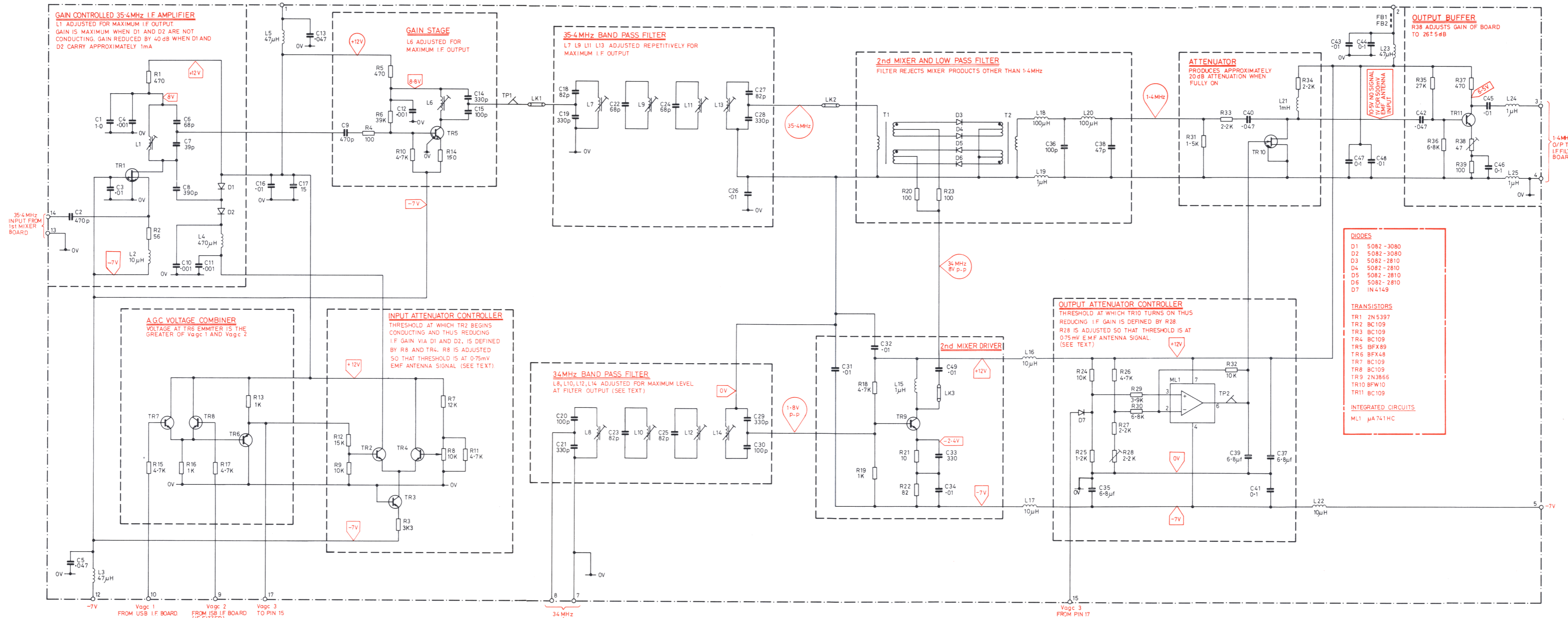
OUTPUT ATTENUATOR CONTROLLER

7. The voltage controlled attenuator comprises R31, R33, C40 and TR10. The source-to-drain impedance of TR10 is controlled by the level of the voltage applied to the gate; when fully on the attenuator produces approximately 20 dB attenuation.

8. The output from the AGC voltage combiner (V agc 3) is applied via board pin 15, D7 and R9 to the positive input terminal of an operational amplifier ML1. The voltage applied to the negative input terminal of ML1 is set by R28; this is adjusted so that when the signal level at the antenna socket reaches 0.75 mV emf, the level of the output voltage from ML1 is just sufficient to cause TR10 to conduct. An increase in the level of the applied AGC voltage increases the output voltage from ML1; this increases the conduction of TR10 and the level of the 1.4 MHz signal applied to the output buffer stage is reduced.

OUTPUT BUFFER AMPLIFIER

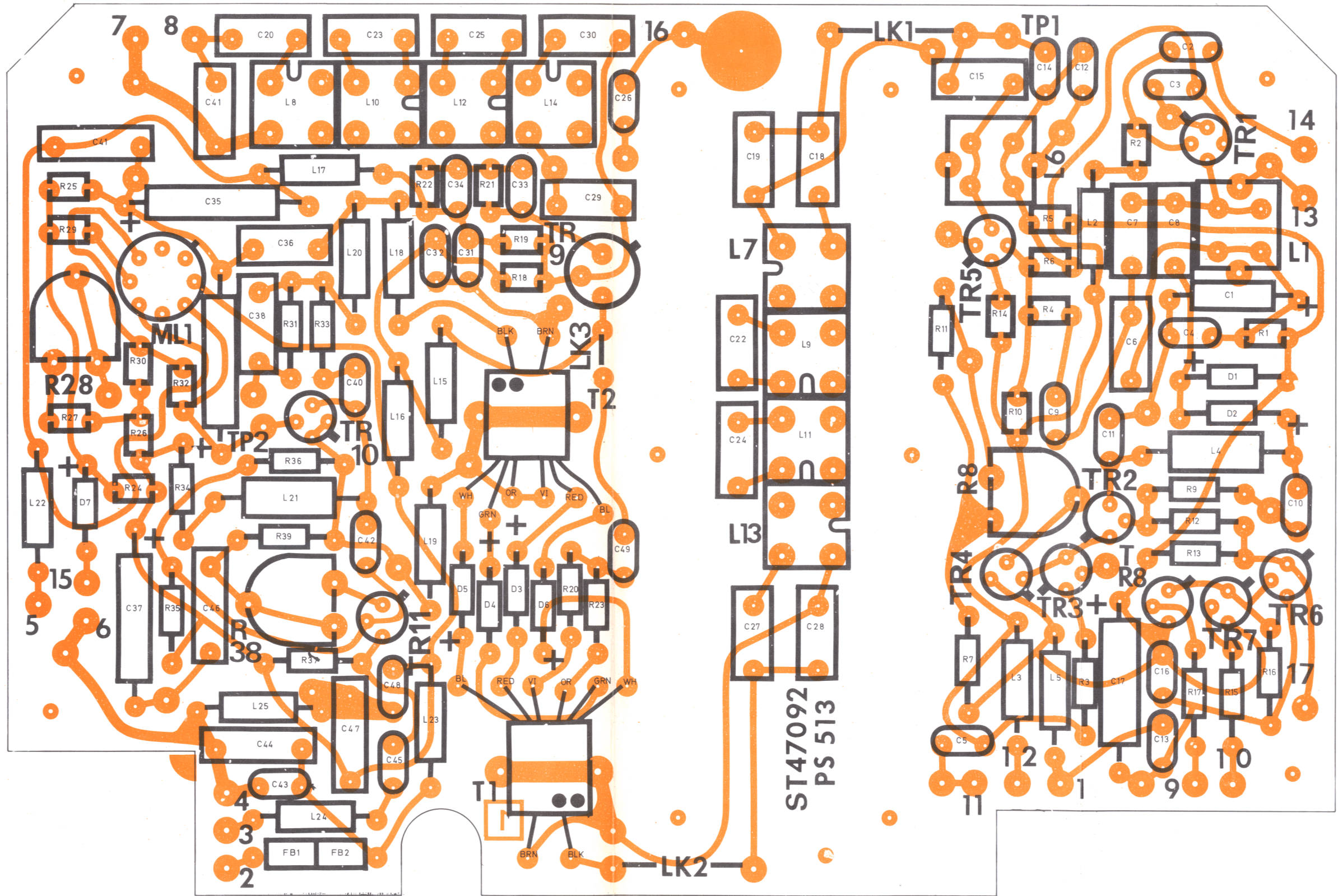
9. The 1.4 MHz output signal from the voltage controlled attenuator is coupled by C42 to the output buffer amplifier stage TR11. R38 is adjusted for a gain, from board input to board output, of 26 dB \pm 5 dB. The 1.4 MHz IF output is applied via board pin 3 to the IF filter board.



RACAL		
WOH 6247	DC 47092	3/4.1
1/2	1	2/2

Circuit: Second Mixer Board PS 513

Part 3 Fig 4.1



RACAL

WOH 6247	EA 47091/4	4-2
1		1/2
WOH 6247	EA 47091/4	4-2
1		2/2

CHAPTER 5

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IF FILTER BOARD PS663

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	<u>Fig.No.</u>
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CHAPTER 5

IF FILTER BOARD PS663

INTRODUCTION

1. The filter board contains the 1.4 MHz sideband and/or symmetrical crystal filters; up to six filters may be fitted and these are dependent on the various options available.
2. For SSB receivers (fitted for both upper and lower sideband operation) and ISB receivers, FL1 is the LSB channel filter whilst FL2 is the USB channel filter. If 6 kHz sideband filters are fitted at positions FL1 and FL2, the increased physical size of these filters precludes the fitting of a filter at position FL4.

NOTE: Due to the inversion within the receiver the USB channel filter has LSB characteristics and the LSB channel filter has USB characteristics.

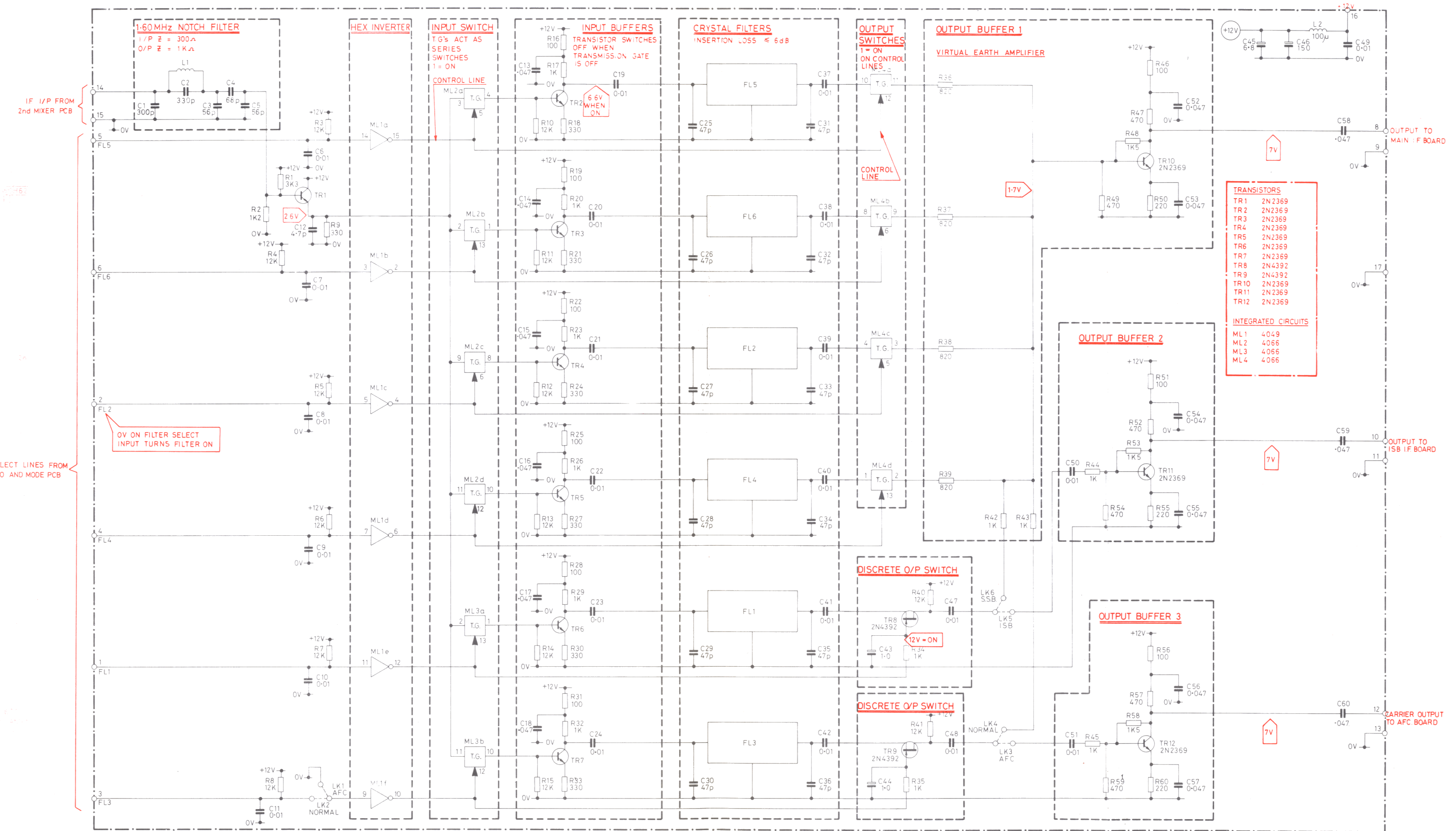
3. In receivers equipped with the optional AFC facility a narrow-band carrier filter is fitted at position FL3, links LK2 and LK4 are broken, and links LK1 and LK3 are made.
4. The remaining filter positions may be occupied by symmetrical filters, one of which may be selected for AM or CW modes. If the receiver is equipped for AM and CW only, then all six filter positions may be fitted with symmetrical filters; these may be selected from the following (the widest bandwidth filter is fitted at position FL6):

0.3 kHz, 1 kHz, 3 kHz, 6 kHz, 8 kHz, 13 kHz.

FILTER SELECTION (fig. 5.1)

5. The 1.4 MHz IF input signal from the second mixer board, at board pin 14, is applied to a 1.60 MHz notch filter (in earlier versions – serial numbers 120 to 264 – a 1.575 MHz notch filter was fitted. See components list for values of capacitors C1 to C5). From the notch filter the signal is applied to emitter follower stage TR1, and then in parallel to a bank of six transmission gates.
6. Since the selection circuitry is the same for each filter, only one example is given, that for filter FL5.
7. To select FL5 an earth is applied to board pin 5; this is inverted by ML1a and a logic '1' is applied to the control inputs of transmission gates ML2a and ML4a. The gates are opened and the 1.4 MHz signal from TR1 is applied via ML2a and the input buffer stage TR2 to filter FL5. The filtered output is routed via C37 and ML4a to a virtual-earth buffer-amplifier stage TR10; this stage has a gain of approximately two times (ratio of input resistor R36 to feedback resistor R48) and the output signal is routed to the main IF board via C58 and board pin 8.

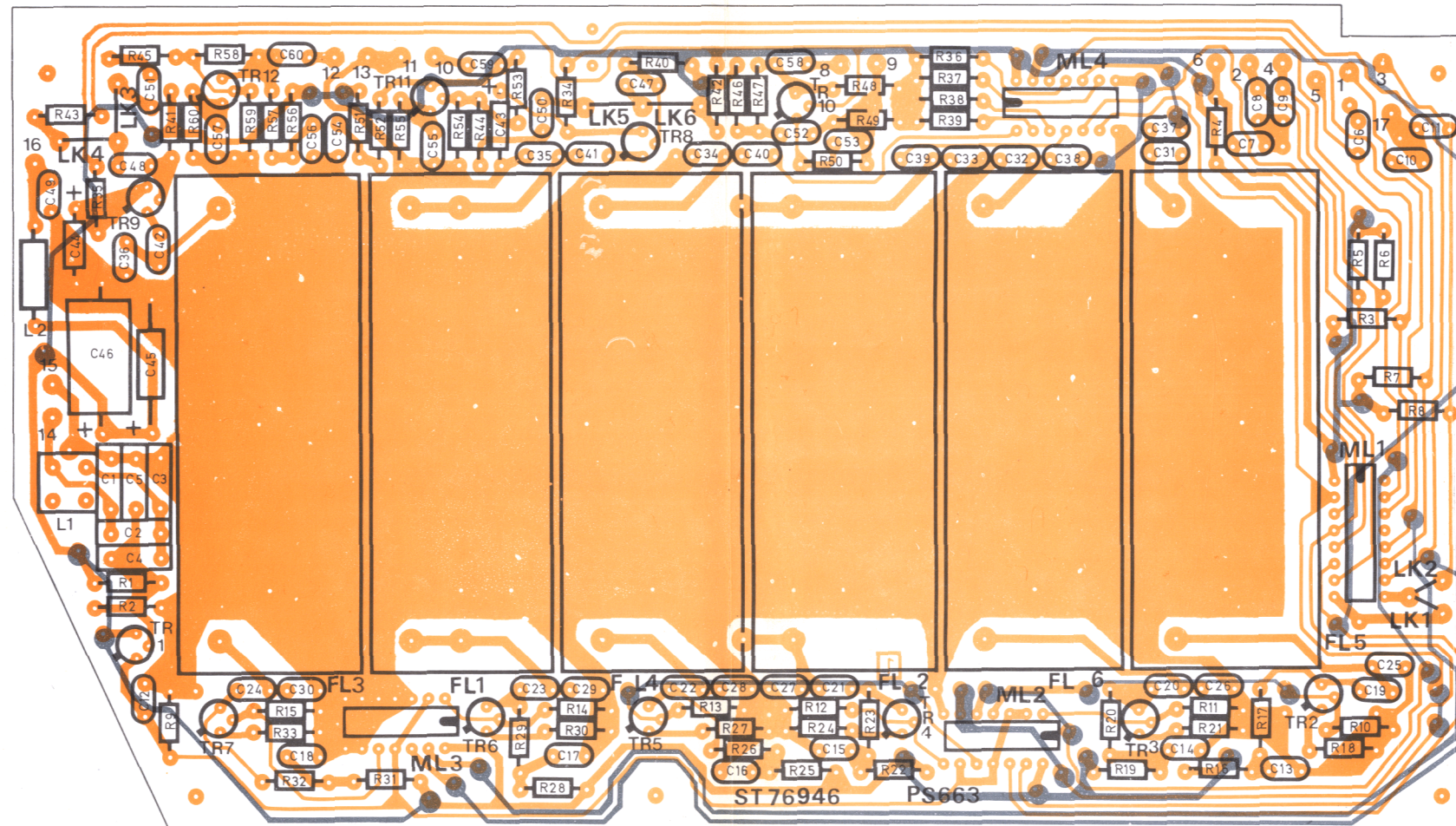
8. The output buffer stage TR11 is only used for ISB versions of the receiver (link LK6 broken, LK5 made); output buffer stage TR12 is only used for receivers equipped with the AFC facility (links LK2 and LK4 broken, LK1 and LK3 made).



- TRANSISTORS**
- TR1 2N2369
 - TR2 2N2369
 - TR3 2N2369
 - TR4 2N2369
 - TR5 2N2369
 - TR6 2N2369
 - TR7 2N2369
 - TR8 2N4392
 - TR9 2N4392
 - TR10 2N2369
 - TR11 2N2369
 - TR12 2N2369
- INTEGRATED CIRCUITS**
- ML1 4049
 - ML2 4066
 - ML3 4066
 - ML4 4066

RACAL		
WOH6247	DC76946	3/5-1
1		1/2
WOH6247	DC76946	3/5-1
1		2/2

Circuit : IF Filter Board PS663 Part 3
Fig. 5-1



WV	RACAL	DA 76945/2	5-2
WOH 6247		DA 76945/4	2/3
1			1/3
WOH 6247		DA 76945/3	5-2
1			3/3

CHAPTER 6

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IF BOARD PS661

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CHAPTER 6

IF BOARD PS661

INTRODUCTION

1. This board contains a high-gain 1.4 MHz IF amplifier, the AGC detector and amplifier stages, the third mixer, the 100 kHz IF amplifier, the AM/SSB detectors and an audio pre-amplifier stage.
2. Two identical IF boards are fitted in ISB versions of the receiver; when ISB is selected, the main IF board carries the USB channel and the ISB IF board carries the LSB channel. The circuit diagram of the board is given in fig. 6.2.

GAIN CONTROLLED IF AMPLIFIER

3. The 1.4 MHz IF output signal from the IF filter board, at board pin 2, is applied to a two-stage integrated circuit amplifier ML3, ML4. The AGC voltage is applied to both amplifiers, via R15 to ML3 and via R33 to ML4. The output signal from ML4 is matched into a 1.4 MHz bandpass filter via TR9 and is then fed to a buffer amplifier TR10, TR11; the output at TR9 is applied to the AGC detector via C34 and an overload limiter (para. 13), and to the third mixer via C42.

THIRD MIXER

4. This stage mixes the 1.4 MHz IF signal from TR11 with the 1.5 MHz signal from the synthesizer (at board pin 24) to produce the final IF output signal at 100 kHz. A switching type of integrated circuit mixer is used, ML8, where the 1.4 MHz signal is applied to the signal input (pins 1 and 4) and the 1.5 MHz signal is applied to the switching (carrier) input (pins 8 and 10) via a grounded base voltage amplifier/buffer stage TR14.
5. The output signal from ML8, at pins 6 and 12, is applied to a 100 kHz bandpass filter, R88, C46, T1 and the components bounded by the dashed line; link LK4 is normally connected from A to C and is temporarily moved to position A-B during re-alignment. The gain of the mixer stage is set by R87; this is adjusted for a level of 100 mV at the 100 kHz output socket on the rear panel (connected to board pins 27 and 28) terminated into 50 ohms, with an input level of 5 μ V at the antenna socket.

100 kHz IF AMPLIFIER

6. The output signal from the 100 kHz bandpass filter is applied to a buffer amplifier TR15, TR16 which feeds the AM and product detector (para. 8) and two 100 kHz IF amplifier stages, TR17, and TR21 (the links at TP14 are included for test purposes). From the main IF board, the two outputs at board pins 27, 28 and 29, 30 are taken to the two 100 kHz IF OUT sockets on the rear panel; for ISB versions, the output signal at pins 29 and 30 on the ISB IF board is taken to the ISB IF OUT socket on the rear panel, and the output at pins 27, 28 is not used.

IF MUTE

7. When an earth is applied to the rear panel MUTE terminal, either directly or via the serial data from the control panel, it is routed to board pin 26; this turns off TR20 and the +12V supply is removed from the buffer amplifier and the two 100 kHz IF amplifiers.

AM AND PRODUCT DETECTOR

8. This circuit uses a demodulator integrated circuit ML7. For SSB and CW reception, the 100 kHz IF signal is applied to the signal input (pins 1 and 4), and the 100 kHz signal from the synthesizer at board pin 32 (fixed frequency for SSB, variable by up to plus or minus 4 kHz for CW) is applied via NOR gate G4 to the carrier input (pins 8 and 10). The detected output signal, at pin 6, is coupled by C44 to an active low-pass filter TR18, and then to an audio pre-amplifier stage ML9B.
9. For AM reception, the 100 kHz signal is removed from board pin 32 and an earth is applied to board pin 17; this opens NOR gate G3 for the output signal from the AM detector amplifier, and the output NOR gate G4 is opened by the 0V input applied via R94.
10. The amplitude modulated 100 kHz IF signal is applied to the signal input of ML7 (as for SSB reception) and is also applied to the AM detector amplifier G1, G2; this effectively removes the amplitude modulation and produces a high-level squarewave output at the carrier frequency which is applied via G3 and G4 to the carrier input of ML7.

AUDIO PRE-AMPLIFIER

11. The audio pre-amplifier uses an operational amplifier ML9B. Negative feedback is applied via R131 and the gain figure of approximately eight times is set by the ratio of R131 plus R132 to R132. The audio output at board pin 15 is applied to the AF board.

AF MUTE

12. Board pin 19 is externally connected to board pin 26 (para. 7). When an earth is applied, TR19 is turned off and the +12V supply is removed from the low-pass filter and the audio pre-amplifier.

AGC DETECTOR

13. The 1.4 MHz IF signal output from TR10, at TR9, is applied to the temperature-compensated AGC detector stage TR5, TR6, via an overload-limited amplifier TR12, TR13; this stage has a linear gain characteristic up to the overload point when the output level remains constant for higher input signal levels. The positive output voltage from the detector is taken from the emitter of TR5 and is applied to the AGC amplifier.

AGC AMPLIFIER

14. The positive output voltage from the AGC detector is applied via switched time constant components to a linear d.c. amplifier stage ML1A. R14 and C11 are provided for spike reduction and may be brought into circuit by making link LK3 and breaking link LK2. When AGC SHORT is selected, a '1' is applied to board pin 9; this is applied to the control input of transmission gate G6, and R16 is connected across the time constant capacitor C8. When AGC LONG is selected, the '1' input is transferred from board pin 9 to board pin 8 and the additional parallel-connected time constant capacitors C9, C80 are brought into circuit via transmission gate G5. Transmission gate G7 forms part of the AGC hang circuit described in para. 18.

AGC Dump

15. The AGC dump circuit is activated each time AGC LONG is selected at the control panel. Its purpose is to discharge the time constant capacitors so that they may re-charge to the level of the signal being received. When an earth pulse is applied to board pin 7, TR1 conducts and turns on TR2, TR3 and TR4. TR2 and TR3, connected in parallel to produce a lower impedance, discharge time constant capacitors C8, C9 and C30, whilst TR4 discharges the spike reducer capacitor C11 when link LK2 is broken.

16. The AGC dump circuit is also used to effectively switch off the AGC when manual control of the IF gain is required; the earth is maintained at board pin 7, and the manual gain control voltage from the interface unit is applied to board pin 6 in place of the AGC output voltage from ML1A (diode D2 is thus reverse biased).

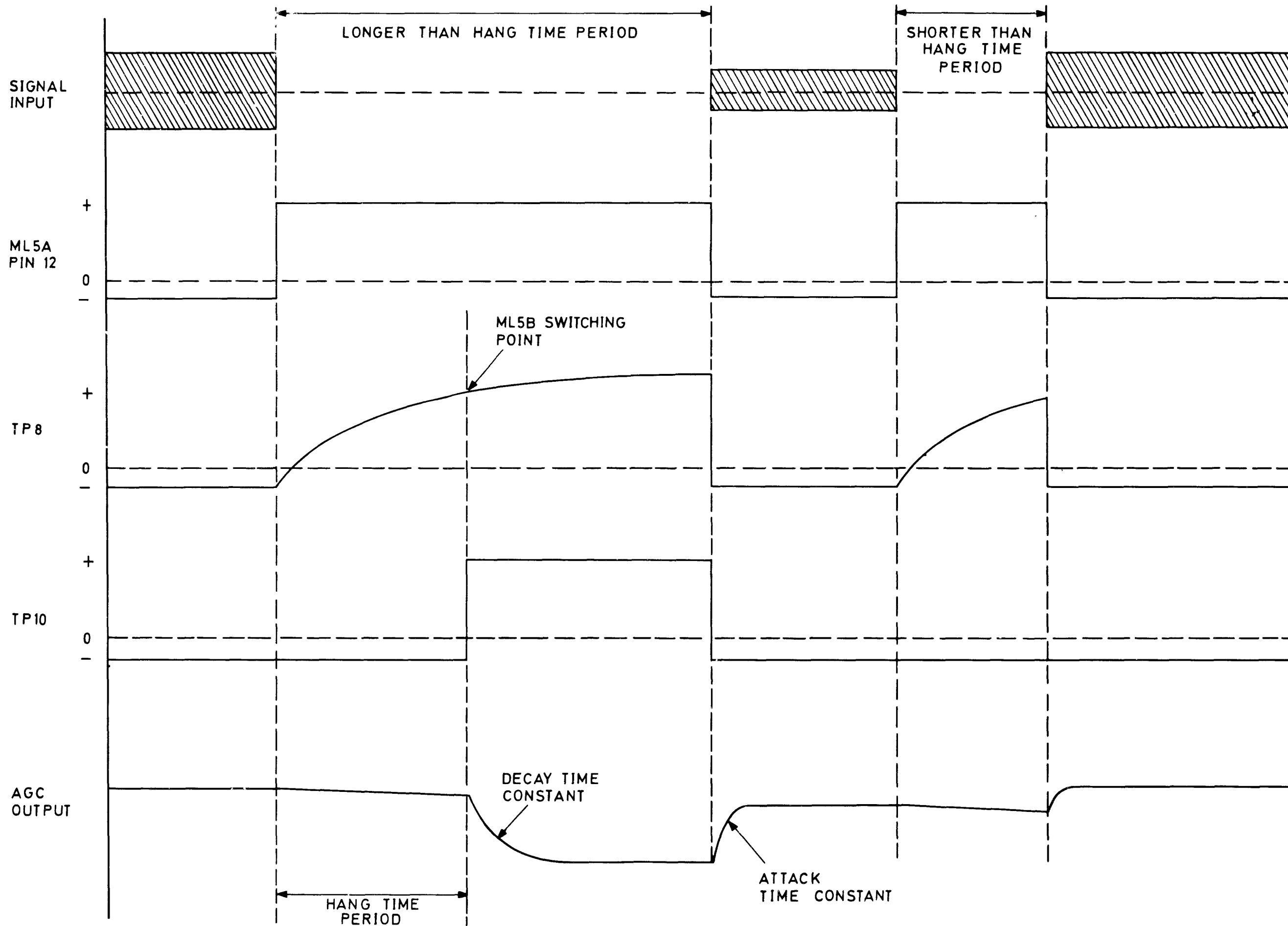
17. The gain control voltage at board pin 6 is applied to ML1B; this stage sets the AGC threshold and slope characteristics before application to the 1.4 MHz IF amplifier stages ML3, ML4.

AGC Hang

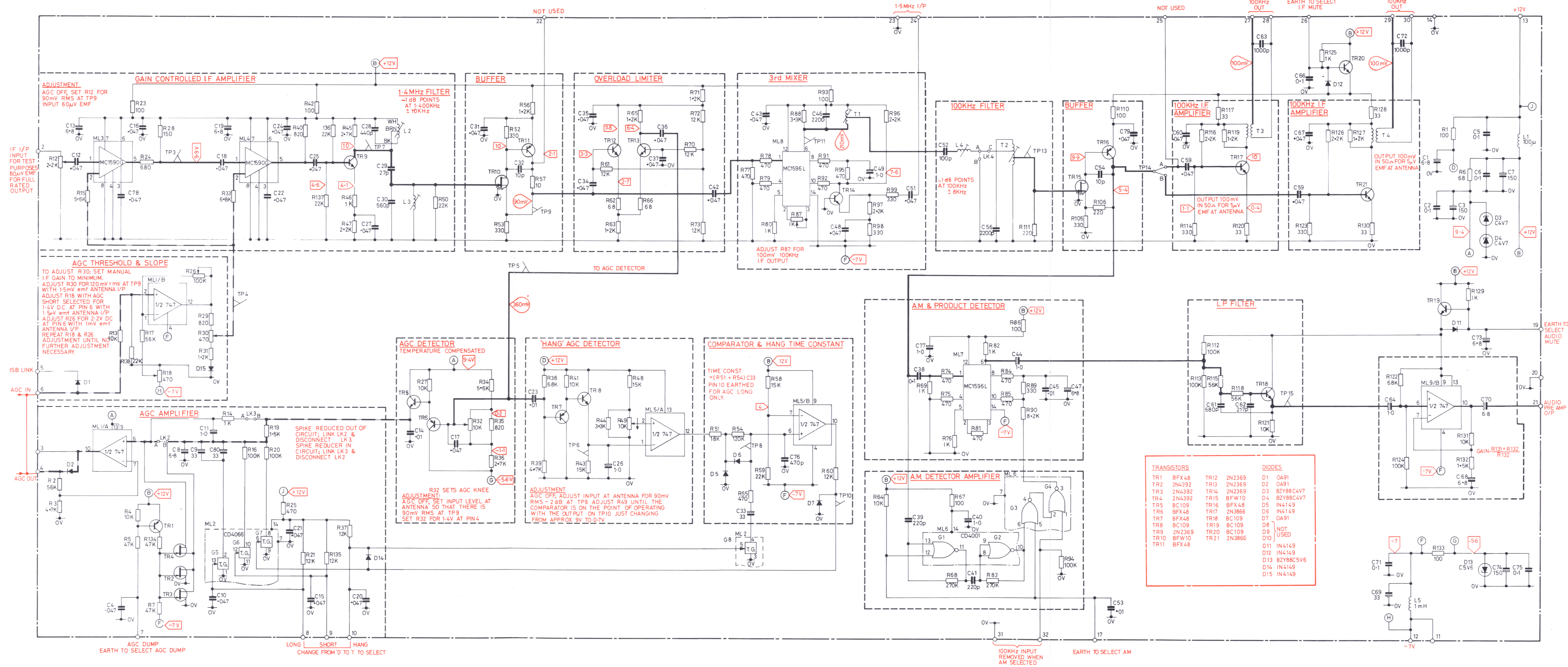
18. The AGC hang circuit maintains the level of the AGC output voltage from ML1A, following an interruption in the received transmission, for a period of approximately 2.5 seconds. The circuit is only operative when AGC LONG is selected.

19. The IF output signal from TR13 is coupled by C23 to a temperature-compensated detector stage TR7, TR8. The output from TR8 is applied to the inverting input of ML5A whilst R49 sets the voltage level applied to the non-inverting input such that the output at ML5A pin 12 is negative (clamped to approximately -0.7V by D5) when a received signal is present. This negative voltage is applied to the non-inverting input of comparator ML5B; the potential divider R58, R59 sets the voltage at the inverting input of ML5B to approximately +4V, and this results in a negative output at TP10, which is limited to approximately -0.7V by diode D7.

20. When a break in the received transmission occurs, the corresponding reduction in the emitter current of TR8 causes the voltage level at ML5A pin 1 to fall below the preset voltage level at ML5A pin 2; the output at ML5A pin 12 switches from negative to positive and capacitor C33 charges via R51, R54, R55 and transmission gate G8 (turned on by the '1' at board pin 10). Once the level of the exponentially rising voltage at ML5B pin 6 exceeds the level of the fixed potential applied to ML5B pin 7, the output at ML5B pin 10 switches from negative to positive; this is applied to the control input of transmission gate G7, the time constant capacitors discharge via R20 and G7, and the AGC voltage output from ML1A falls exponentially to zero.
21. When the received transmission recommences, the emitter current of TR8 rises, the output of ML5A switches from positive to negative and C33 rapidly discharges via R55, D6 and the low output impedance of ML5A. The output from ML5B switches from positive to negative, transmission gate G7 is turned off, and the AGC voltage from TR5 re-charges the time constant capacitors via R19.
22. The operation of the hang detector circuit, as described above, and also where the break in the received signal is shorter than the hang time period, is shown in the timing diagram fig. 6.1.



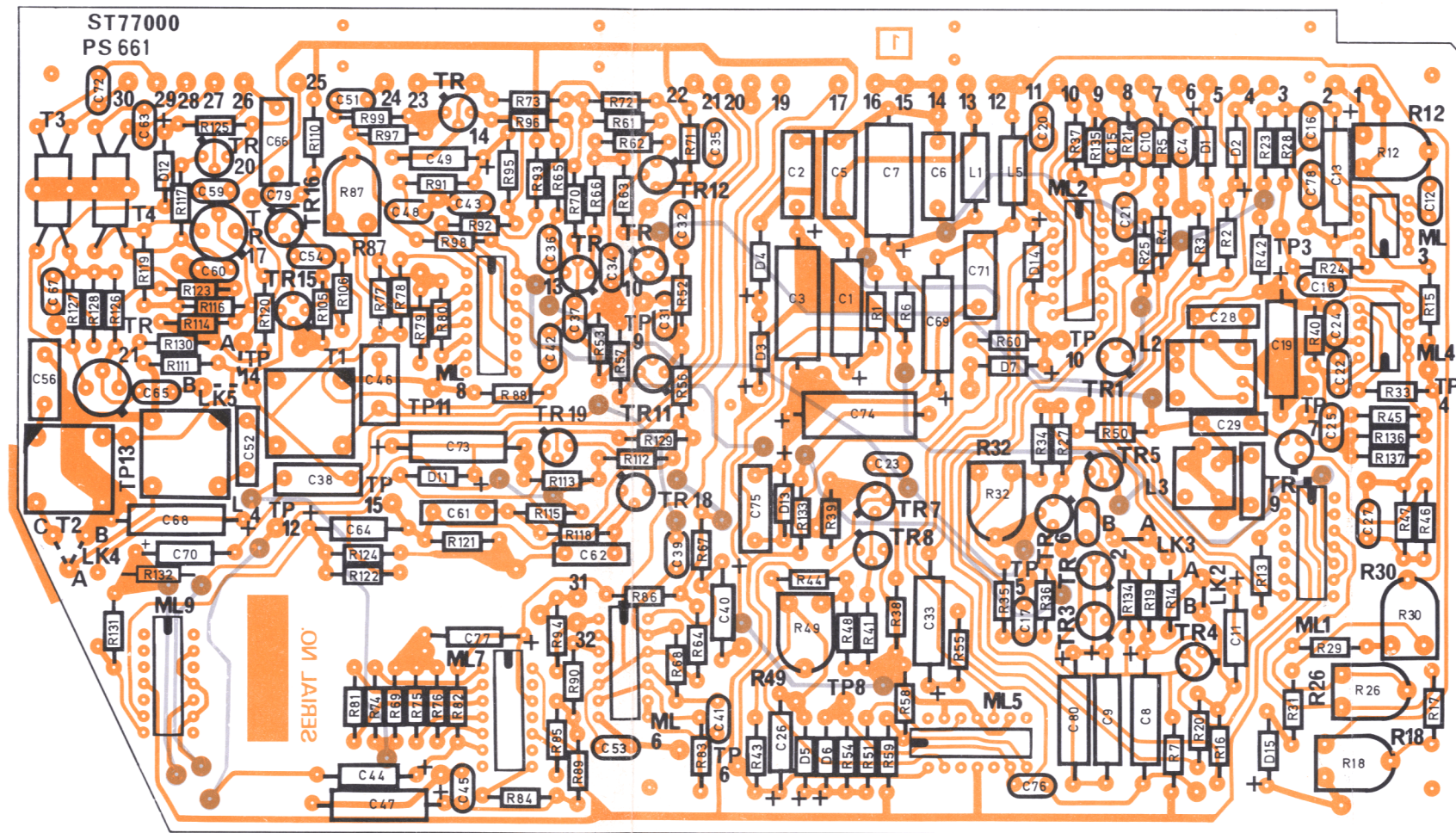
NOT TO SCALE



RACAL		
WOH6247	DC77000	3/6.2
1/2	1/2	2/2
WOH6247 DC77000 3/6.2		
1 1 2/2		

Circuit: I.F.
Board PS661

Part 3.
Fig.6.2



WOH 6247	DA 76999/2	6.3
RACAL		2/3
WOH 6247	DA 76999/4	6.3
1		1/3
WOH 6247	DA 75999/3	6.3
1		3/3

Layout: I F Board

C H A P T E R 7

=====

A F B O A R D P M 6 6 2

=====

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ILLUSTRATIONS

	<u>Fig.No.</u>
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Layout: AF Board PM662	7.2

CHAPTER 7

AF BOARD PM662

INTRODUCTION

1. This board contains three audio amplifiers; one supplies the audio monitor output to the phones socket, the rear panel loudspeaker terminals, the rear panel external control connector, and to the front panel meter via the interface unit, whilst the remaining two amplifiers provide the audio line output signals (line output and ISB line output terminals) together with rectified outputs for metering purposes.
2. The audio input switching, which is controlled by the serial data from the control panel via the interface unit, is arranged such that for SSB receivers (or ISB receivers switched to SSB) the audio output signal from the main IF board is applied to all three audio amplifiers, whilst for ISB receivers (set for ISB operation) one line amplifier is fed from the main IF board and the other line amplifier is fed from the ISB IF board. The input signal to the audio monitor amplifier is fed from the main IF board when ISB-U is selected, or from the ISB IF board when ISB-L is selected at the control panel.
3. The circuit diagram of the AF board is given in fig. 7.1.

AUDIO INPUT SWITCHING

4. The audio input switching is controlled by the MODE push-button switches on the control panel via the serial control data and the interface unit (BFO and mode board). Transmission gates (G7 to G12) are used as the switch elements and these are controlled by the logic levels on the three switching lines, at board pins 8, 7 and 6. For example, if a '0' is applied to board pin 8, the resulting '1' output from the inverting buffer G1 opens transmission gate G7 for the audio output signal from the ISB IF board, at board pin 9. When the '0' is removed from board pin 8, a '1' is applied to the input of G1 (from the +10V supply via R40) and the resulting '1' output from G2 opens transmission gate G8 for the audio output signal from the main IF board, at board pin 12.
5. Details of the audio switching arrangements for all modes for both SSB and ISB versions of the receiver are given in table 1.

GAIN-CONTROLLED AMPLIFIERS

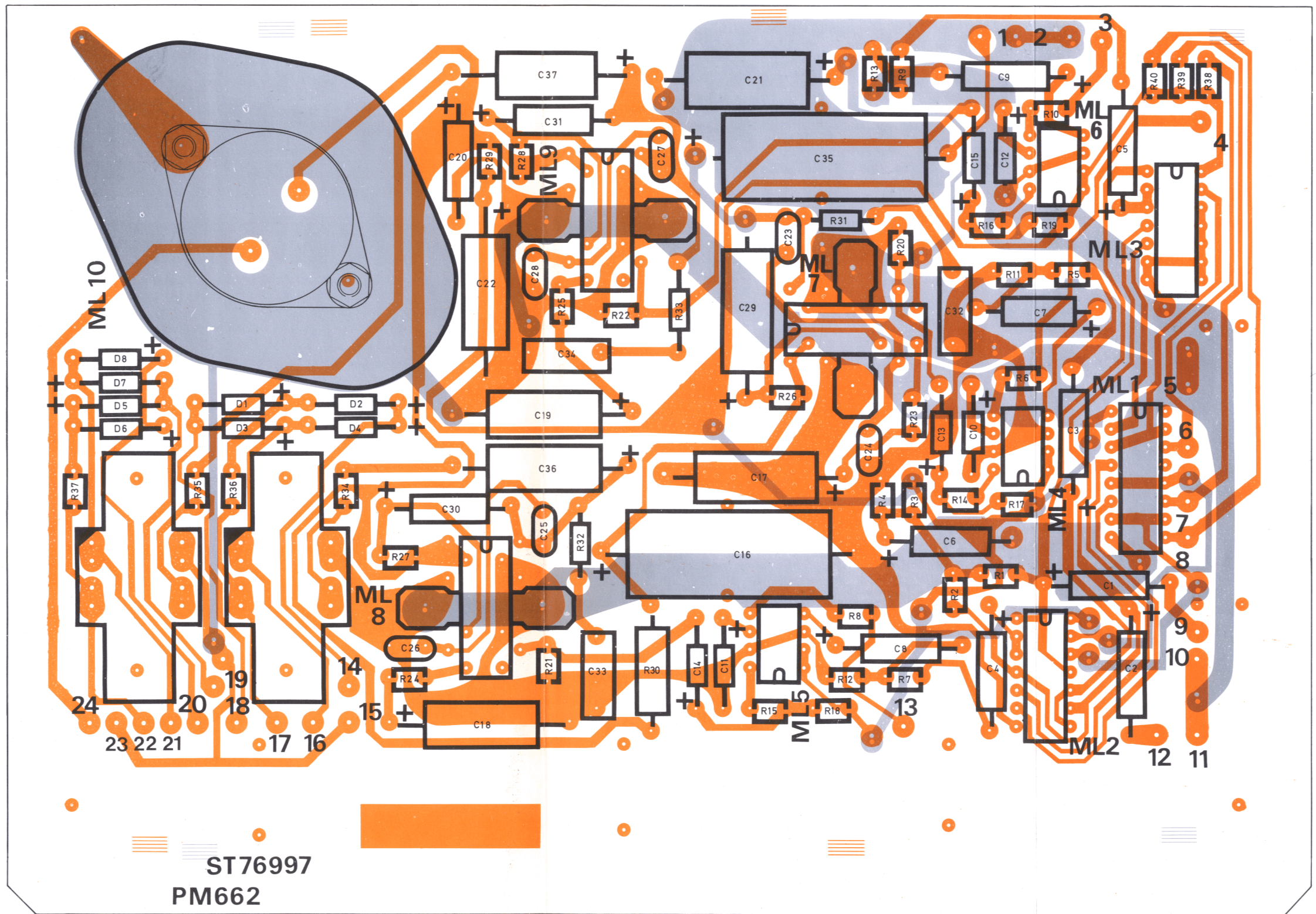
6. The three gain-controlled amplifiers are of similar construction and each use high-gain wideband amplifier integrated circuit ML4, ML5, ML6. The gain-control voltage applied to pin 2 is set by the respective level control on the receiver front panel (MONITOR LEVEL, USB LINE LEVEL and LSB LINE LEVEL controls).

Table 1: Audio Input Switching

MODE	AUDIO MONITOR AMPLIFIER		LINE 1 AMPLIFIER		LINE 2 AMPLIFIER	
	INPUT SOURCE	PIN 8 LEVEL	INPUT SOURCE	PIN 7 LEVEL	INPUT SOURCE	PIN 6 LEVEL
<u>SSB RECEIVERS</u>						
ALL MODES	MAIN IF	1	MAIN IF	1	MAIN IF	1
<u>ISB RECEIVERS</u>						
LSB	ISB IF	0	ISB IF	0	ISB IF	0
ISB-U	MAIN IF	1	MAIN IF	1	ISB IF	0
ISB-L	ISB IF	0	MAIN IF	1	ISB IF	0
OTHER MODES	MAIN IF	1	MAIN IF	1	MAIN IF	1

AF OUTPUT AMPLIFIERS

7. The audio monitor output amplifier, ML7, has a fixed gain of approximately 36 dB. The output from ML7, which is short-circuit protected, is coupled by C35 to the front panel PHONES socket, the loudspeaker terminals and the external control connector on the rear panel, and to the front panel meter via the meter board (part of the interface unit - Part 4).
8. The two line output amplifiers ML8, ML9 are similar and have a gain figure of approximately 29 dB. The output signals are transformer coupled to the rear panel LINE O/P and ISB LINE terminals, and are also applied via bridge rectifier circuits D1 to D4 and D5 to D8, to the front panel meter via the meter board (part of the interface unit).



RACAL	EA76996 / 3	7-2
		3/3
WOH 6247	EA76996 / 4	7-2
		1/3
WOH 6247	EA76996 / 2	7-2
		2/3

Layout: Audio Frequency Board

PART 4

P A R T 4
=====

I N T E R F A C E U N I T M S 6 1 4
=====

CONTENTS

CHAPTER 1	GENERAL DESCRIPTION
CHAPTER 2	DISMANTLING AND REASSEMBLY
CHAPTER 3	FUNCTIONAL DESCRIPTION
CHAPTER 4	SERIAL CONTROLLER BOARD PS667
CHAPTER 5	FREQUENCY AND MONITOR BOARD PS666
CHAPTER 6	BFO AND MODE BOARD PS668
CHAPTER 7	METER SWITCHING/STANDBY BATTERY BOARD PS669

CHAPTER 1

GENERAL DESCRIPTION

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Simplified Block Diagram: MS614 Interface Unit	1.1

CHAPTER 1

GENERAL DESCRIPTION

INTRODUCTION

1. The MS614 interface unit converts the serial control data from the MA.1072 into parallel form to control the various receiver functions, and also generates the serial revertive data which is sent back to the MA.1072 control panel. A simplified block diagram of the unit is given in fig. 1.1.

BRIEF TECHNICAL DESCRIPTION

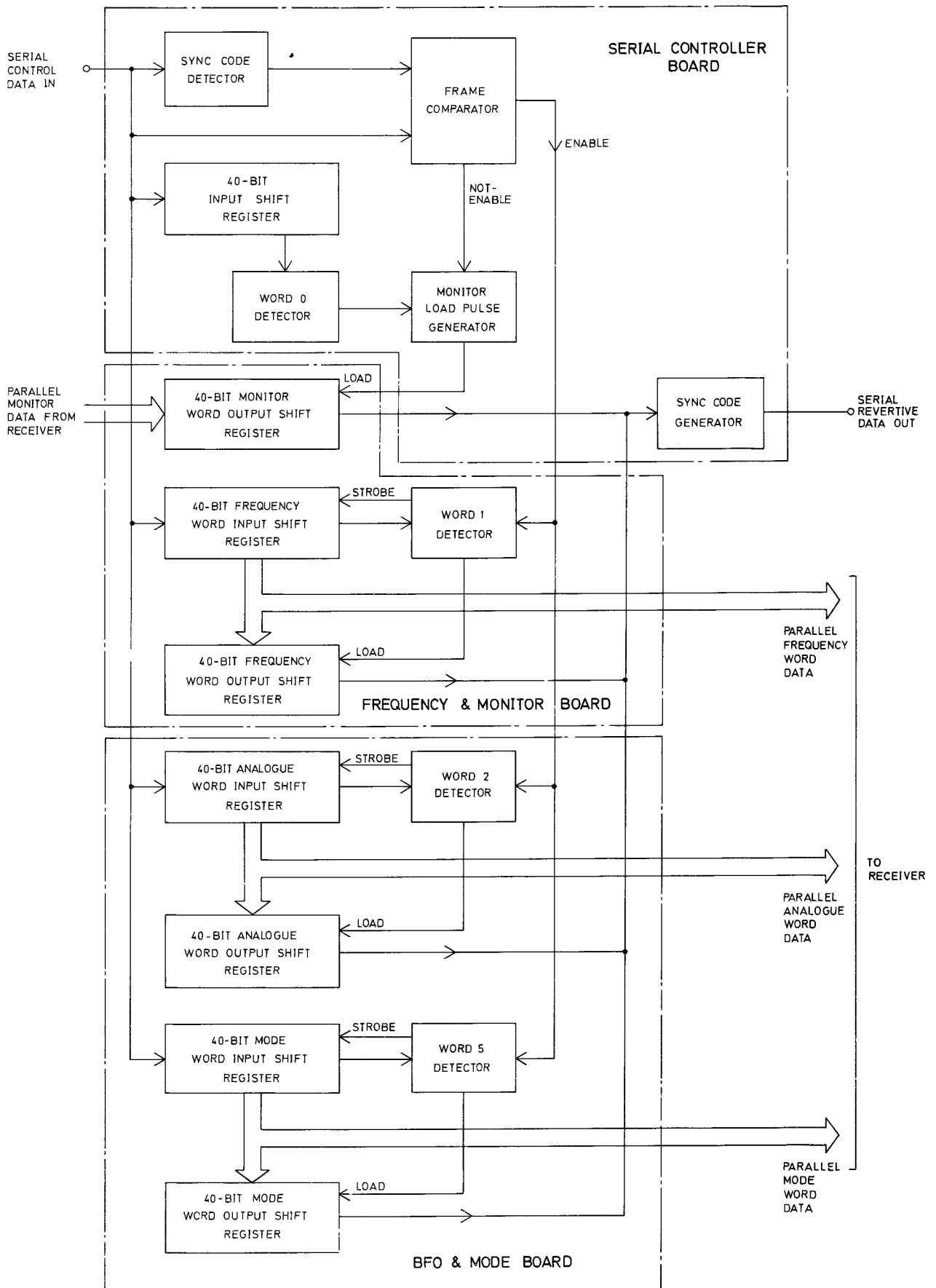
2. The serial control data from the MA.1072 is applied in parallel to the sync. code detector, frame comparator and 40-bit input shift register on the serial controller card, and to the 40-bit shift registers for the frequency word, the analogue word and the mode word. When a correct sync. code is recognised, the frame comparison takes place; if successful, an enable pulse is generated which is applied to the word ident. detectors for words 1 (frequency), 2 (analogue) and 5 (mode) via a common enable line.
3. For word 1, word 2 or word 5 data, the strobe output signal from the respective word detector enables the parallel output data from the associated 40-bit input shift register (which is applied to the receiver); a second output signal from the respective word detector loads the parallel data into the associated output shift register, and this is then serially clocked out as revertive data for application to the MA.1072 control panel via a sync. code generator.
4. For word 0 data, or should the frame comparison fail, a monitor load pulse is generated (either by the output from the word 0 detector or by the not-enable output from the frame comparator); the parallel monitor data from the receiver is loaded into the 40-bit monitor word output shift register and is then serially clocked out via the sync. code generator to the MA.1072.
5. A meter and associated switch on the front panel are provided for monitoring power supply and other signal levels from the receiver. These signals are applied to the meter switch via the meter switching/standby battery board. The standby battery is used to preserve the frequency setting and other data during a supply failure.

PHYSICAL DESCRIPTION

6. The interface unit comprises a metal box structure which is attached to the receiver front panel. The three main printed circuit boards (serial controller, frequency and monitor, and BFO and mode) are mounted one behind the other in spring-loaded slides. The meter switching/standby battery board is also mounted in spring-loaded slides and is positioned behind the front panel meter. The connections to the boards are made via flexible ribbon cable and connector assemblies from an interconnection board which is attached to the inner

rear face of the box structure. Four multi-way connectors are mounted on the interconnection board and these protrude through apertures in the rear member of the box structure for the mating connections from the receiver (one connector is wired to the external control connector on the receiver rear panel).

7. A cableform from the meter switching/standby battery board connects with the front panel meter switch, PHONES socket, the OUT OF LOCK lamp, and the three audio level adjustment potentiometers. A separate five-way connector on the rear member of the box structure is used for the supply connections to and from the front panel POWER switch and associated indicator lamp.



Simplified Block Diagram
MS614 Interface Unit

Part 4
Fig.1-1

CHAPTER 2

DISMANTLING AND REASSEMBLY

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BATTERY REMOVAL	10

ILLUSTRATIONS

	<u>Fig. No.</u>
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'POZIDRIV' SCREWDRIVERS

Metric thread cross-head screws fitted to Racal equipment are of the 'Pozidriv' type. Phillips type and 'Pozidriv' type screwdrivers are not interchangeable, and the use of the wrong screwdriver will cause damage. POZIDRIV is a registered trade mark of G.K.N. Screws and Fasteners Limited. The 'Pozidriv' screwdrivers are manufactured by Stanley Tools Limited.

CHAPTER 2

DISMANTLING AND REASSEMBLY

INTRODUCTION

1. This chapter provides instructions for gaining access to the printed circuit boards and chassis components of the MS614 interface unit. The dismantling and reassembly instructions for the remainder of the receiver are given in Part 1, Chap.2. In general, the reassembly is the reverse of the dismantling procedure.

REMOVAL OF INTERFACE UNIT

2. The interface unit, which includes the receiver front panel, is removed from the receiver as follows:
3.
 - (1) Slide the receiver forwards such that the bottom edge of the front panel is clear of the working surface.
 - (2) Remove the four chromed front panel screws adjacent to each handle, three fitted with a nylon washer and one recessed, fitted with a spring washer.
 - (3) Grip the two handles, slide the unit forwards sufficiently to allow the removal of the five connecting sockets, and then slide the unit forwards to clear the receiver side members.

NOTE: When reconnecting the interface unit to the receiver chassis ensure that the three right-hand multi-way connectors are correctly located by matching the coloured spots on the cable form connector shells with those adjacent to the interface unit plugs. These plugs are numbered, from the top, as PL7, PL8 and PL9; the five-way plug is PL11 and the left hand multi-way plug is PL10.

ACCESS TO METER SWITCHING BOARD

4.
 - (1) Remove the ribbon connector (brown spot) from the top edge of the meter switching board.
 - (2) Slide the board upwards to clear the guide slots. The board is connected via a cableform which has sufficient slack to allow the reconnection of the ribbon connector for maintenance purposes. Before applying power to the receiver insulate the underside of the board.

Battery Link

5. The two position link on the meter switching board may be set to the BATTERY OFF position to completely remove all power from the receiver.

MAIN COMPARTMENT BOARDS

6. The main compartment boards, namely, from front to rear, the serial controller board PS667, the BFO and mode board PS668, and the frequency and monitor board PS666, are held in slides in the main compartment. Electrical connections are made via ribbon cable and connector assemblies (from the interconnection board) which are colour coded for ease of identification. The coloured dots on the inside of the left-hand compartment side member match those of the left-hand connector on each board to indicate correct positioning.
7. To remove a board, disconnect the ribbon cable connectors from all of the boards and slide the board upwards.

FRONT PANEL REMOVAL

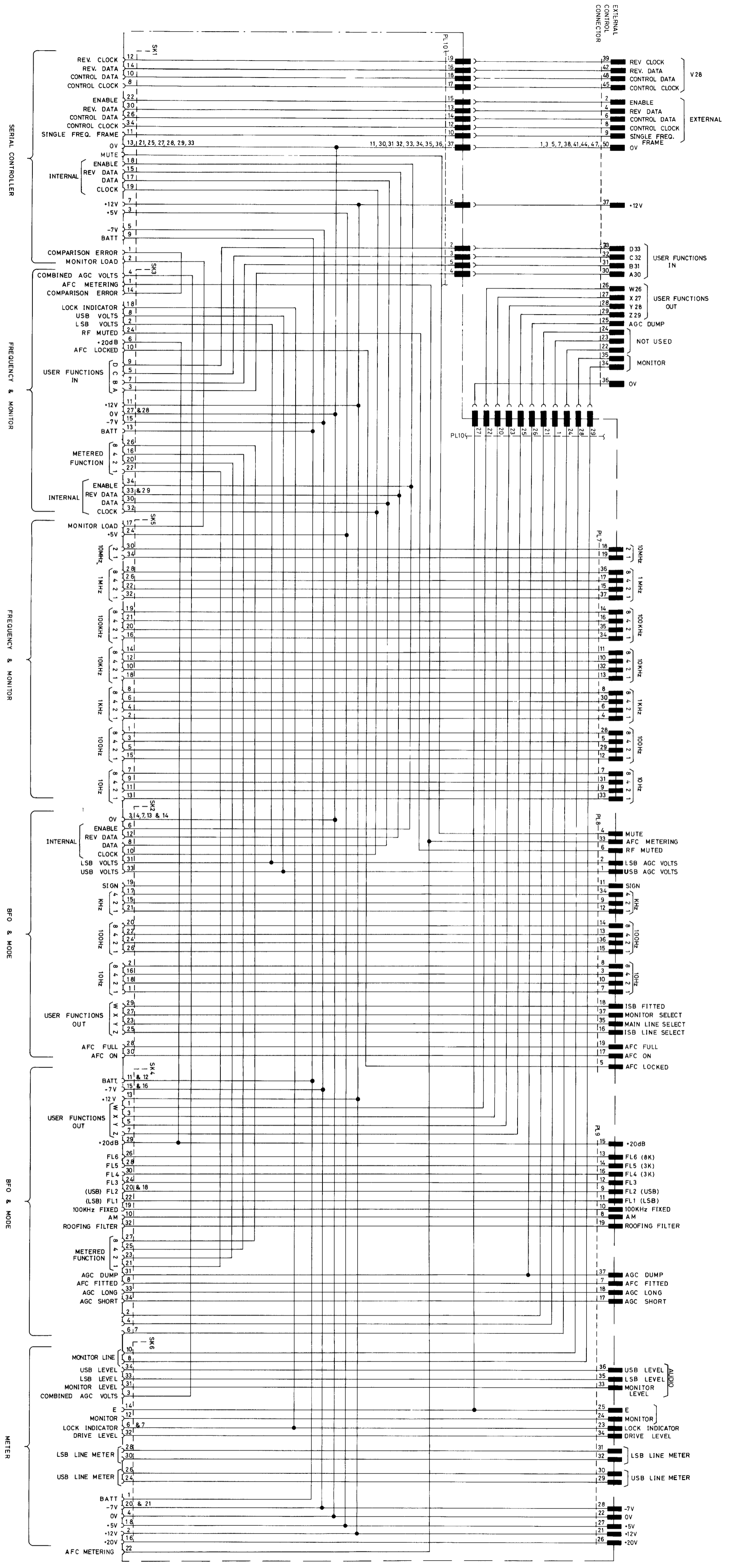
8. (1) Remove the end cap from the METER switch knob.
- (2) Using an 8 mm ring or socket spanner, release the knob collet nut and remove the knob.
- (3) Remove the three screws, each with a nylon washer, from the centre of the front panel.
- (4) The front panel is now attached only by the two leads to the front panel meter. To completely remove the front panel undo the nuts securing these leads to the meter. Replace the nuts for safe keeping.

INTERCONNECTION BOARD REMOVAL

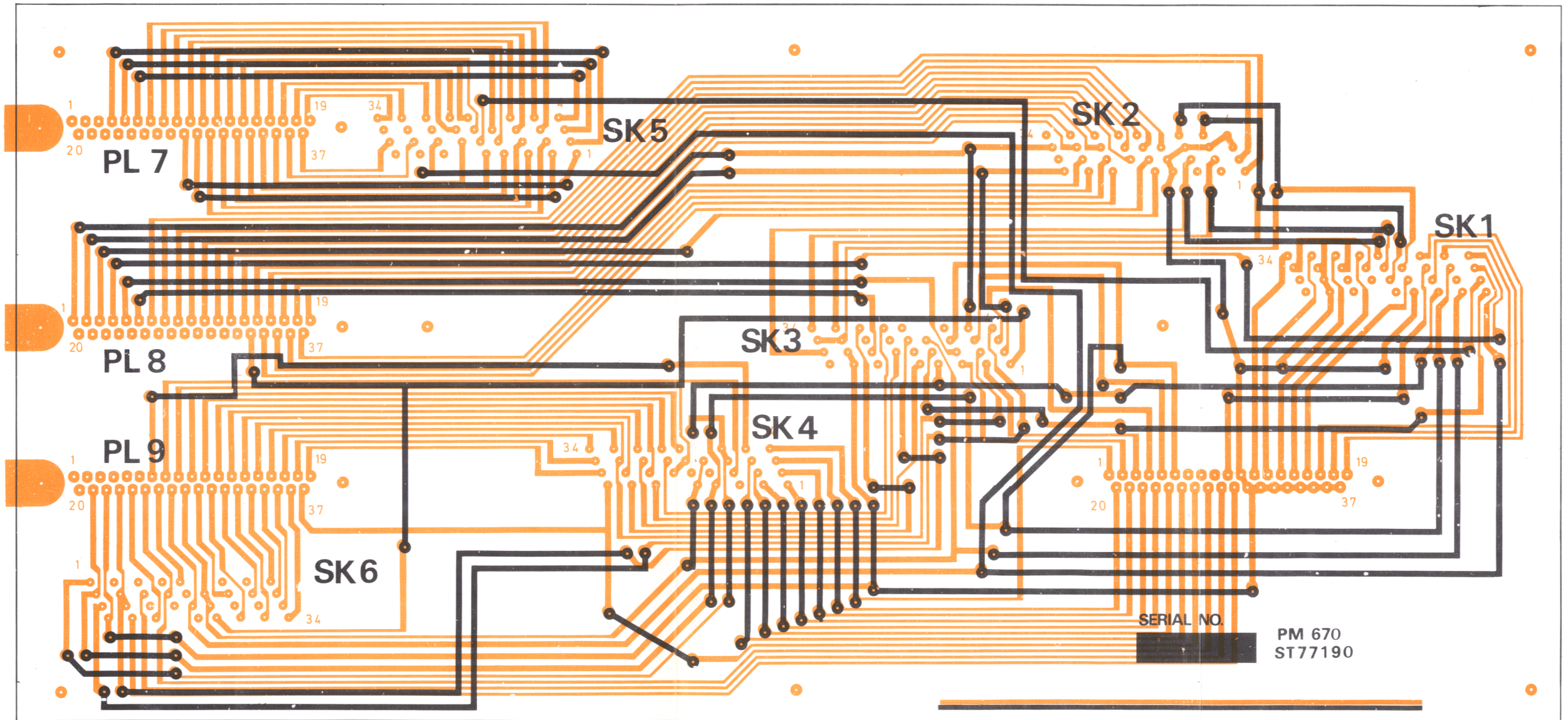
9. (1) Remove the three boards from the main compartment (para. 6).
- (2) Disconnect the ribbon cable connector from the meter switching board.
- (3) Remove the seven screws securing the rear plate, three at each side and one in the centre of the flange securing the rear plate to the base plate.
- (4) Remove the locking posts securing the four multi-way connectors to the rear plate.
- (5) Ease off the board from the push-fit nylon stand-off fasteners.

BATTERY REMOVAL

10. (1) Ensure that the battery link on the meter switching board is set to BATTERY OFF.
- (2) Remove the rear plate (steps (1), (2) and (3) of para. 9).
- (3) Unsolder the battery leads and remove the battery from the two spring clips.



Interconnection Diagram MS 614 Interface Unit



RACAL

WOH 7014	DA 77099 / 3	4/2-2
1		1/2
WOH 7014	DA 77099 / 2	4/2-2
1		2/2

CHAPTER 3

FUNCTIONAL DESCRIPTION

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CHAPTER 3

FUNCTIONAL DESCRIPTION

INTRODUCTION

1. This chapter briefly describes the operation of the interface unit, and should be read in conjunction with the functional diagram given in fig. 3.1. This diagram shows the basic blocks for the monitor word (word 0) and the frequency word (word 1) to illustrate the principles of operation; the same principles however, apply for the remaining words.

SYNCHRONISATION

2. The serial data and clock signals from the MA.1072 control panel are applied simultaneously to the frequency and monitor board, the BFO and mode board, and to the serial controller board. When a correct sync. code (a '0' followed by five '1s') is recognised by the sync. code detector on the serial controller board, a start signal is generated which is applied to:

- (1) A 40-bit counter which eventually generates an end-of-frame pulse.
- (2) A frame comparator which compares the next 40-bits of the incoming serial data with the contents of a 40-bit input shift register.
- (3) A clock control circuit which allows the application of 40 clock pulses to the frame comparator and to the 40-bit input shift register.

Thus when the end-of-frame pulse is generated, it signifies that a correct sync. code has been received and that the remaining 40-bits of the data word frame are correctly positioned in the input shift registers on the serial controller, frequency and monitor, and BFO and mode boards.

SERIAL DATA ROUTING

3. For the purposes of the following description, assume that the incoming serial data consists of two word 0 frames followed by two word 1 frames and then two word 5 frames. Assume also that the control inhibit bit (CHECK status) is not set (para. 12) and that the return monitor bit (single frequency frames) is not set (para. 13).

4. Word 0 is used for revertive monitor purposes only; it is sent by the MA.1072 as a routine data word to request the return of the monitor information. Since the monitor word frame is also returned following a frame comparison failure (see MA.1072 Maintenance Manual, Chap.2), it follows that every time a word 0 frame is received, a word 0 frame must be returned. Thus every time the word ident. detector detects the presence of word 0 in the 40-bit input shift register on the serial controller board, a monitor load pulse is generated by the combination of the word 0 detect output signal and the end-of-frame pulse.

The monitor load pulse is applied to the 40-bit monitor output shift register (frequency and monitor board), and the monitor data is loaded in.

5. The sync. code of the second word 0 frame is recognised by the 8-bit sync. code detector, the 40-bit counter is restarted, and the remaining 40 bits of the second word 0 frame are clocked into the 40-bit input shift register. At the same time, the monitor word is clocked out of the 40-bit output shift register, via a further shift register (serial controller board) which adds the 8-bit sync. code, and the complete word 0 frame is sent back to the MA.1072 control panel via the revertive data line.
6. The word ident. detector again detects the presence of word 0 in the 40-bit input shift register, a further monitor load pulse is generated as before, and the monitor data is loaded into the 40-bit output shift register.
7. The next frame received in this example contains word 1 which, following sync. code detection, is frame compared with word 0 (contained in the 40-bit input shift register). Since the two frames do not compare, a monitor load pulse is again generated, only this time by the combination of the frame comparator output, the resulting not-enable output, and the end-of-frame pulse. The second monitor word frame is clocked out to the MA.1072 and the monitor data is loaded into the 40-bit output shift register for the third successive time.
8. The next frame comparison (following sync. code detection) is between two word 1 frames; this time (assuming no bit errors are detected), the combination of the frame comparator output and the end-of-frame pulse results in the generation of an enable pulse which is applied via a common line to the word 1 ident. detector on the frequency and monitor board and the word 2 and word 5 ident. detectors on the BFO and mode board. The presence of word 1 in the frequency word input shift register (32-bit register followed by an 8-bit register) is detected, a strobe pulse is applied via NOR gate G1 (the control inhibit input is at '0') and the 32-bit frequency data word is applied in parallel form to both the 32-bit section of the frequency word output shift register and the synthesizer section of the receiver. The word 1 ident. detector also routes a parallel-entry pulse to the frequency word output shift register via NOR gate G2 (the return monitor bit is set to '0') and the 40 bits of the frequency word are loaded in. During this time, the third word 0 frame is clocked out as revertive data to the MA.1072 control panel.
9. The next data frame in the sequence contains word 5 (para. 3). Since this will not frame compare with word 1, a monitor load pulse is generated (frame comparator output and resultant not-enable pulse together with the end-of-frame pulse) and the monitor data is loaded into the monitor word 40-bit output shift register. At the same time, the frequency word is clocked out via the 8-bit sync. code generator to the MA.1072.
10. The last frame in this example sequence also contains word 5. This results in the generation of the enable pulse (assuming no bit errors are detected), the word 5 ident. detector on the BFO and mode board causes the mode word to be entered into the mode word output shift register, and this is clocked out via the 8-bit sync. code generator, following the transmission of the previously generated monitor word frame.

11. If the two word 5 frames do not compare, a monitor load pulse is generated (combination of the frame comparator output, the not-enable pulse and the end-of-frame pulse) and a monitor word frame is returned to the MA.1072.

CONTROL INHIBIT

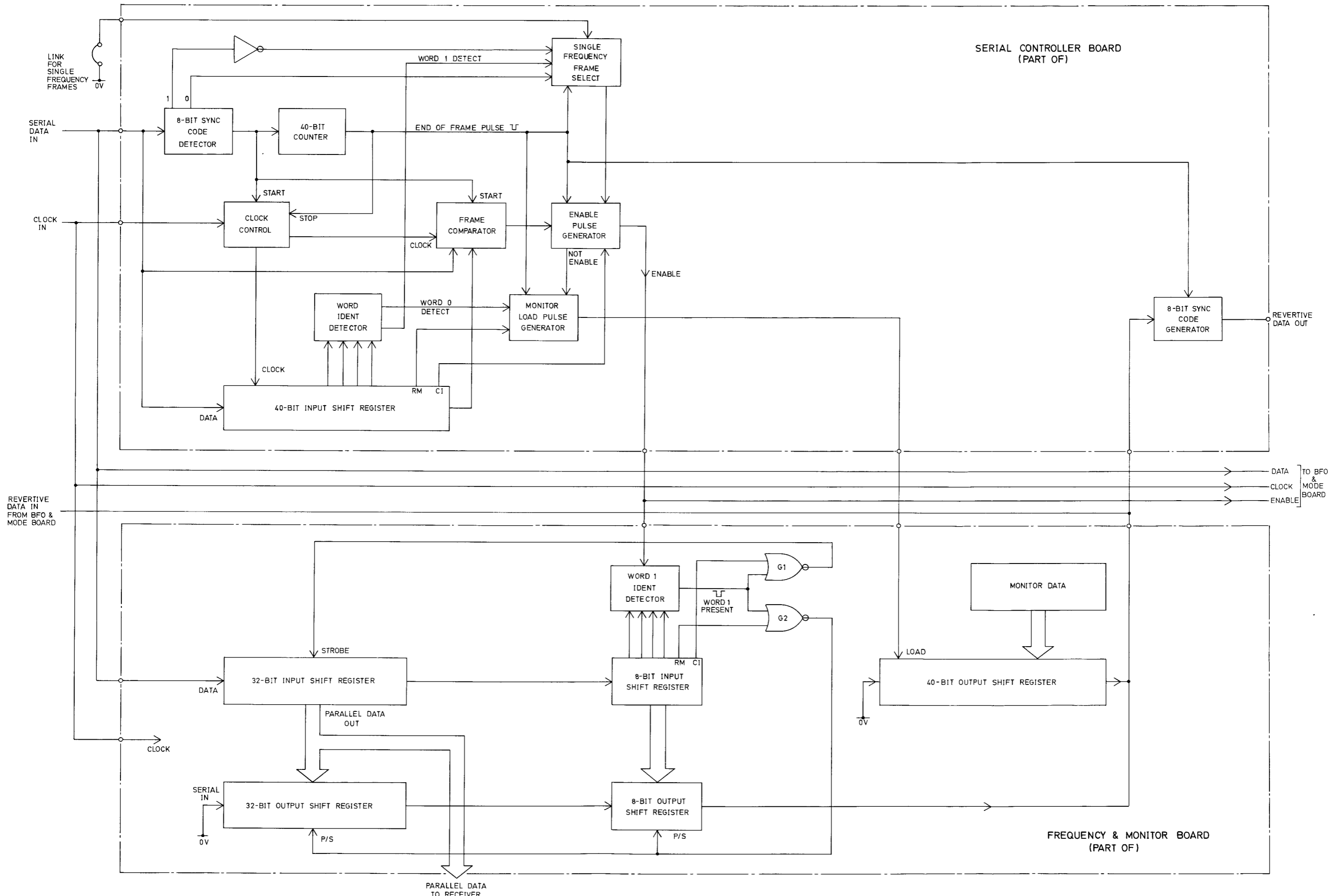
12. The control inhibit bit (bit 8 of the SCORE format) is set to a '1' at the MA.1072 when the CHECK status is selected. The control inhibit bit output from the 40-bit input shift register on the serial controller board causes the generation of the enable pulse (the frame comparator is by-passed), whilst the control inhibit bit outputs from the control word input shift registers prevent strobe pulse generation, i.e. the output from G1 is forced to a '0' and similarly for the remaining control words. The absence of the strobe pulse prevents the updating of the parallel output data (the parallel outputs of the data word input shift registers are latched) and thus further control of the receiver is inhibited. Since routine data only is received in the CHECK status, and since no frame comparison takes place, the control word ident. detectors cause the receiver setting information to be returned to the MA.1072 in sequential double frames which lag the forward data by one frame (48 bits).

RETURN MONITOR

13. The return monitor bit (bit 9 of the SCORE format) is set to a '1' at the MA.1072, together with a '0-1' code for the single-frame check bits (bits 46 and 47) of the frequency word, when single frequency word frames are required together with continuous revertive monitor. To allow the transfer of single frequency frames two connections are required, one at the MA.1072 and one at the RA.1784. A link is required between pins 17 and 11 (earth) at PL1 on the MA.1072 for the transmission of single frequency frames when free tuning, and a link is required between pins 9 and 7 (earth) at the external control connector on the RA.1784 rear panel to inhibit frame comparison on frequency frames. Note that the frequency frames are only sent singly whilst new frequency data is being generated; once the required frequency has been set, routine frequency frames are sent in pairs and frame comparison is restored at the RA.1784.
14. The link between pins 9 and 7 at the external control connector on the receiver rear panel routes a '0' to the single frequency frame select circuit on the serial controller board. To inhibit frame comparison on frequency frames, the remaining inputs to this circuit must all be at '0' when the end-of-frame pulse is generated; the output from the word ident. detector will pulse to '0' when the presence of word 1 in the 40-bit input shift register is detected, whilst the other two inputs are derived from the single frame check bits of the frequency word. When the last 40 bits of the frequency word are correctly positioned in the 40-bit input shift register, bits 40 to 47 will also be located in the 8-bit sync. code detector. The '0' code for bit 46 and the inverted '1' code for bit 47 are thus applied to the single frequency frame select circuit, the enable pulse is generated, and the frame comparator is effectively by-passed.
15. The return monitor bit output from the 40-bit input shift register on the serial controller board is applied to the monitor load pulse generator and the resulting load pulse enters the monitor data into the 40-bit monitor output shift register. The return

monitor bit output from the frequency word input shift register is applied via NOR gate G2 as a serial-entry signal to the frequency word output shift register to inhibit parallel data entry.

16. When tuning ceases at the MA.1072, routine data double frequency frames are transmitted, the single frame check bits of the frequency words are both set to '0', and thus frame comparison is restored.



C H A P T E R 4

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S E R I A L C O N T R O L L E R B O A R D P S 6 6 7

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C H A P T E R 4
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S E R I A L C O N T R O L L E R B O A R D P S 6 6 7
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INTRODUCTION

1. The serial controller board contains the synchronisation circuits, the frame comparator, the PTT/Mute control circuit and the sync. code generator for the revertive data.

1A. Two versions of the board are currently in Service use, the standard version and that incorporating Mod No. A 8882. A block diagram of the board is given in fig. 4.1 (modified version) and fig. 4.1A (standard version). The circuit diagrams for these versions are given in fig. 4.2 and fig. 4.2A respectively. The layout diagram (fig. 4.3) relates to the standard version only.

FUNCTIONAL DESCRIPTION

Control Data Input

2. The V28 inverted control data input from the MA.1072 (+12V for binary '0', -12V for binary '1'), at board pin 10 (fig.4.1), is converted to TTL levels (+5V for binary '1' and 0V for binary '0'); it is then applied via inverting buffer TR1 (at C-MOS levels) to the external control connector (on the receiver rear panel) via board pin 26, and via inverting buffer TR3 to the frequency and monitor board and to the BFO and mode board, via board pin 17. The inverted data output from TR3 is also applied via C-MOS inverter G1 to an 8-bit shift register ML15, a 40-bit shift register ML6, ML13, and to the frame comparator.

Control Clock Input

3. The V28 control clock signal from the MA.1072, at board pin 8, is converted to TTL levels and is then applied
- (1) To a TTL to V28 level conversion stage, which provides the revertive clock output signal (board pin 12).
 - (2) Via inverting buffer TR2 and board pin 34 to the external control connector (on the receiver rear panel).
 - (3) Via inverting buffer TR4 and board pin 19 to the frequency and monitor board, and the BFO and mode board.
 - (4) Via TR4 and G2 to the clock pulse generator.

Clock Pulse Generator

3A. The clock pulse generator produces a nominal 6µs negative-going pulse for each positive-going transition of the clock input signal, and a nominal 6µs positive-going pulse for each negative-going transition of the clock input signal.

3B. In the standard version, the pulse generator is formed by gates G8 to G10 and inverters G11 and G12. When Mod No. A8882 is incorporated, G8 to G12 are replaced by two D-type bistables ML19a, ML19b.

Sync. Code Detector

4. The serial control data output from G1 is clocked into an 8-bit shift register ML15; since the strobe and enable inputs are connected to the +12V rail, the parallel outputs are enabled and the contents of the register are applied in parallel form to the sync. code detector G14 to G17.

5. When a correct sync. code is detected i.e. a '0' followed by five '1's and then either a '0' - '1', a '1' - '0' or a '0' - '0' transmit/receive code, a '1' output signal is produced which is applied to the counter control stage (para.8), the PTT/Mute circuit via G7 (para.6) and the frame comparator (para.14).

PTT/Mute Circuit

6. Data bits 6 and 7 of the SCORE format are used for transmit/receive switching (PTT) where the transmit state may mute the receiver and set an associated transmitter to the transmit condition. For the transmit state bit 6 is set to a '1' and bit 7 is set to a '0', whilst for the receive state, bit 6 is set to a '0' and bit 7 is set to a '1'.

7. If data bits 6 and 7 are set for a '1' - '0' transmit mode in two successive sync. codes, the '0' output pulse from exclusive OR gate G7 enables the PTT/Mute circuit, and the '1' - '0' transmit code sets the output to a '0'. This is routed to the receiver to mute the RF and AF circuits and is also available at the rear panel MUTE terminal to set an associated transmitter to the transmit condition.

Counter and Control

8. The counter control stage consists of a bistable counter G18, G19; this circuit is set by the output signal from the sync. code detector, to produce a start signal for the 40-bit counter, and to enable the clock signal applied to the 40-bit input shift register via NOR gate G20, and is reset by:

- (1) the end-of-frame output pulse from the 40-bit counter (after 40 input clock pulses have been counted).
- (2) the output from the sync. code detector if five consecutive '1's are detected in the serial data.
- (3) the power fail detector in the event of a power failure.

9. The end-of-frame pulse output from the 40-bit counter is applied as a parallel entry enable pulse for the sync. code generator stage ML11 (para.18), and via inverting buffer G26 to:

- (1) the monitor load pulse generator.
- (2) the enable pulse generator.

- (3) the error counter ML10b (para. 16).

40-Bit Input Shift Register

10. Following the detection of a correct sync. code, the output signal from the counter control stage opens NOR gate G20 for the application of 40 clock pulses to the input shift register ML6, ML13. When the end-of-frame pulse occurs, the 40 bits of the data word are thus correctly positioned in the input shift register.
11. If the word detector ML5 detects the presence of word 0 in the input shift register, the word 0 detect output is applied, together with the end-of-frame pulse, to the monitor load pulse generator, a monitor load pulse is produced, and this is applied via board pin 2 to the frequency and monitor board (Chap.5).
12. The word 1 detect output signal from the word detector, together with the signal input at board pin 11 and return monitor (RM) bit output from the 40-bit input shift register, are concerned with single frequency frames; this is described in para. 20.
13. If the control inhibit (C1) bit of the serial control data is set a '1' (CHECK status selected at the MA.1072), an enable pulse is generated which is applied to the word boards via inverting buffer TR8 and board pin 18, and to the external control connector on the receiver rear panel via inverting buffer TR7 and board pin 22 (for use by external equipment utilising the extra word facility).

Frame Comparator

14. The frame comparator, which is reset each time a correct sync. code is detected, compares the 40 bits of data contained in the input shift register with the 40 data bits of the next word received from the MA.1072. The frame comparator output signal is applied to the enable pulse generator such that when the end-of-frame pulse is produced, a successful frame comparison generates the enable pulse, whilst a frame comparison failure generates the not-enable signal.
15. The enable pulse is applied via TR8 and board pin 18 to the word detectors for the frequency word (frequency and monitor board), the analogue word, and the mode word (BFO and mode board), whilst a not-enable signal causes the generation of the monitor load pulse which is applied to the monitor word output circuit (frequency and monitor board). Thus a frame comparison failure results in the generation of the monitor word which is returned to the MA.1072 via the revertive data highway.

Error Counter

16. The error counter consists of a two-stage shift register ML10b (which is reset by an output signal from the enable pulse generator each time a successful frame comparison occurs), and a three-diode AND gate D4, D5, D6. The error output signal at board pin 1 is applied to the frequency and monitor board where it is used to control the level of bit 34 of the monitor word. A '0' output at board pin 1, indicating no error, sets bit 34 to a '0', whilst when an error is detected, the '0' is removed and bit 34 is set to a '1' via a pull-up

resistor (on the frequency and monitor board) which is connected to the +12V rail.

17. The frame comparison technique employed produces the not-enable pulse, and hence a word 0 monitor frame, when two differently numbered data word frames are compared, and the enable pulse when two similarly numbered data word frames are compared which do not contain any bit errors. Since the not-enable pulse is also generated when two similarly numbered data word frames do not compare (due to bit errors), it follows that the not-enable signal is generated for three consecutive frames when a data error is detected. The logic '1' not-enable signal is applied to D4, and to D5 and D6 via the two-stage shift register ML10b such, that after three consecutive frame comparison failures, all three diodes are reverse biased, and bit 34 of the monitor word changes to a '1' to indicate a frame comparison error.

Sync. Code Generator

18. The sync. code generator consists of an 8-bit shift register ML11. The end-of-frame pulse is applied as a parallel entry enable, the sync. code (a '0', followed by five '1's, and then two '0's) at the parallel data input pins is loaded in, and is then serially clocked out to precede the word data at board pin 15 from the frequency and monitor board or the BFO and mode board. Board pin 30 is taken to the rear panel external control connector and is used by external equipment utilising the extra word facility (see Applications and Installation Manual, Chap. 12).

19. The serial output data from the sync. code generator is applied to a C-MOS to V28 conversion stage (ML17a) and is then applied as revertive data to the MA.1072 via board pin 14 and the revertive highway.

Return Monitor

20. The return monitor bit (bit 9 of the SCORE format) is set to a '1' at the MA.1072, together with a '0' - '1' code for the single frame check bits (bits 46 and 47) of word 1, when single frequency frames are required together with continuous revertive monitor data. When the last 40 bits of word 1 are correctly positioned in the 40-bit input shift register, bits 40 to 47 are also located in the sync. code detector. If a '0' - '1' code is present at data bits 46 and 47, and provided a '0' is applied to board pin 11 (from a link at the external control connector), then the enable pulse is generated coincident with the word 1 detect output from the word detector, and the end-of-frame pulse from the 40-bit counter.

21. The return monitor (RM) bit output from the 40-bit input shift register is applied to the monitor load pulse generator and the monitor load pulse is produced.

CIRCUIT DESCRIPTION (Fig. 4.2 and 4.2A)

Control Data Input

22. The inverted V28 control data input, at board pin 10, is applied to a line receiver ML9a; the inverted TTL output is applied via inverting buffer TR1 to the external control connector on the rear panel via board pin 26, and via

inverting buffer TR3 to the frequency and monitor and BFO and mode boards via board pin 17. The output from TR3 is also inverted by C-MOS NAND gate G1 before application to an eight-bit shift register ML15, the 40-bit input shift register stage ML6, and to the frame comparator G27.

Control Clock Input (Standard Version)

23. The V28 control clock input at board pin 8 is applied to a line receiver ML9b; the TTL output signal from ML9b is applied via inverter TR2 and board pin 34 to the external control connector, via inverter TR4 and board pin 19 to the frequency and monitor and BFO and mode boards, and via line driver ML17b and board pin 12 as the revertive clock signal to the MA.1072. The output from TR4 is also applied via C-MOS NAND gate G2 to the clock pulse generator.

Control Clock Input (Modified Version)

23A. The V28 control clock input at board pin 8 is applied to 'squarer' stages ML9d, ML9c and then level-converted by TR9, ML9b. The resultant TTL output signal from ML9b is applied via inverter TR2 and board pin 34 to the external control connector, via inverter TR4 and board pin 19 to the frequency and monitor and BFO and mode boards, and via line driver ML17b and board pin 12 as the revertive clock signal to the MA 1072. The output from TR4 also drives the clock pulse generator.

Clock Pulse Generator (Standard Version)

24. This comprises NOR gates G8, G9, NAND gate G10, and two output inverters G11, G12. The clock output signal from G2, which is the inverse of the input at board pin 8, is applied as one input to both G9 and G10 via inverter G8, and to the remaining input of both G9 and G10 via a 6 microsecond (approximately) delay circuit R7, C8. The effect of this is to produce positive-going 6 μ s pulses from G9 coincident with each negative-going transition of the clock signal at board pin 8, and negative-going 6 μ s pulses from G10 coincident with each positive-going transition of the clock signal at board pin 8. The output pulses from G9 are applied to the 8-bit shift register ML15, to the frame comparator ML22b, and via inverting NOR gate G11 to the 40-bit counter ML8, and the 40-bit input shift register stage ML6 via NOR gate G20. The output pulses from G10 are applied to the sync. code detector, and via inverting NOR gate G12 to the sync. code generator.

Clock Pulse Generator (Modified Version)

24A. The clock pulse generator is formed by the D-type bistables ML19a and ML19b and the associated delay networks R7, C8 and R21, C15. The clock signals via TR4 are applied to the clock input of ML19a, and inverted clock signals via NAND gate G2 are applied to the clock input of ML19b. The effect of these signals is to generate trains of 6 μ s pulses at the Q and \bar{Q} outputs of ML19a and at the Q and \bar{Q} outputs of ML19b. The positive-going output pulses at ML19 pin 1 are coincident with the negative-going transitions of the clock signal input at board pin 8, and the positive-going output pulses at ML19 pin 13 are coincident with the positive-going transitions of the clock signal input.

24B. The Q output from ML19a is applied to the sync. code generator (ML11 and ML10a), and the \bar{Q} output from ML19a is applied to the sync. code detector. The Q output from ML19b is applied to the 8-bit shift register ML15 and to the frame comparator ML22b. The \bar{Q} output from ML19b is applied to the 40-bit counter (ML8), and via NOR gate G20 to the 40-bit shift register ML6, ML13.

Sync. Code Detector

25. The serial control data from G1 is clocked into 8-bit shift register ML15. This device has a storage latch associated with each stage for strobing data from the serial input to the parallel outputs, Q0 to Q7. The data in each shift register stage is transferred to the storage latch when the strobe input is at logic '1', and the data in each storage latch appears at the respective parallel output pin when the enable input is at logic '1'. Since both the strobe and enable inputs are connected to the +12V rail, as the serial data is clocked in, it is also applied via the parallel outputs to the sync. code detector.

26. The sync. code detector comprises NAND gates G13, G14, G15 and two NOR gates G16, G17. When a correct sync. code (a '0' followed by five '1s' and then a '0' - '0' code, a '0' - '1' code or a '1' - '0' code) is present at the parallel output pins of ML15, the inputs applied to G16 are all at logic '0' and a positive-going output pulse appears at TP1. If five consecutive '1s' are subsequently detected in the data, the output from G17 changes to a '1'.

27. The output pulse at TP1 is applied to the muting circuit (para.32) via G7, and as a reset signal to the frame comparator (para.40); it is also applied together with the output from G17, to the counter controller (para.29).

Power Fail Detector

28. The power fail detector TR5 is powered from the internal battery supply (+12Vb) and monitors the +12Va output from the power supply section. If the +12Va supply falls to less than 10 volts, TR5 cuts off and 0V is applied to the counter controller to reset the counter.

40-Bit Counter and Control

29. The 40-bit counter uses two 4-stage divide-by-eight Johnson counters ML8, ML1. These devices are advanced on the positive-going transition of the clock input signal provided the reset and clock enable inputs are both at logic '0'. The counter is cleared to its zero count when the reset input is at logic '1'.

30. The counter controller consists of a bistable latch G18, G19. When a correct sync. code is detected, the '1' output pulse at TP1 sets the output of NOR gate G18 to a '0', and the reset is removed from the counter stages. ML8 produces one carry-out pulse for eight input clock pulses, and a positive-going pulse is produced at ML1 pin 4 for five input pulses at pin 14. Thus after a total count of 40 clock pulses, the counter is reset by the end-of-frame output pulse which is applied to the bistable latch via R18, C11. The counter is also reset to zero following a power failure ('0' output from the power fail detector) or if five consecutive '1s' are detected in the serial control data ('1' output from G17).

31. The end-of-frame pulse (at TP2) is applied as a parallel-entry enable pulse to the sync. code generator ML11 (para.50), and is also applied via inverting NOR gate G26 to the error counter ML10b (para.49), the enable pulse generator (G24) and the monitor load pulse generator (G31).

Muting

32. The muting circuit comprises three D-type flip-flops ML7a, ML7b, ML22a, three exclusive OR gates G4, G5, G7, two NOR gates G3, G6, non-inverting buffer ML2a, and an open-collector output inverter TR6.

33. When the transmit/receive bits of the sync. code (bits 6 and 7) are set to a '1' - '0' transmit code, and a correct sync. code is detected, the logic '1' Q1 output from ML15 is applied to the D input of ML7b and also to one input of G5. Similarly, the logic '0' Q0 output from ML15 is applied to the D input of ML7a and also to one input of G4. The sync. code detect output pulse at TP1 is applied to the clock inputs of ML7a and ML7b via G7, and the positive-going transition of this inverted pulse transfers the '1' at the D input of ML7a to the Q output. Provided the '1' - '0' transmit code is still present when the next correct sync. code is detected, the resulting '0' outputs from G3, G4 and G5, together with the second sync. code detect output pulse, produce a '1' output from G6; this clocks ML22a and the '0' at the D produces a '1' at the \bar{Q} output which is applied via buffer ML2a, inverter TR6 and board pin 4 as a 0V mute signal to the receiver. The RF and AF stages of the receiver are muted and an earth is available at the MUTE terminal on the receiver rear panel to key an associated transmitter.

34. The operation of the circuit for a '0' - '1' receive code is similar except that a '1' Q output from ML7a produces a '0' at the \overline{Q} output of ML22a, TR6 is switched off and the 0V mute output is not produced. If a '0' - '0' send/receive code is present, the resulting '1' output from G3 forces the output of G6 to a '0' and inhibits the clock input of ML22a.

40-Bit Input Shift Register

35. The 40-Bit input shift register consists of a 32-bit shift register ML6, followed by an 8-bit shift register ML13. ML6 is a variable length shift register where the number of bits is equal to the sum of the enabled length control inputs (in this case 1, 2, 4, 8 and 16) plus one. The data input is applied to the B terminal and is clocked into a device on the positive-going transition of the clock input signal. ML13 is an 8-stage shift and store register where each stage has an associated storage latch for strobing data from the serial input to the parallel outputs Q0 to Q7. The data in each shift register stage is transferred to the storage latch when the strobe input is at logic '1', and the data in each storage latch appears at the respective parallel output pin when the enable input is at logic '1'. Since both the strobe and enable inputs are connected to the +12V rail, as the serial data is clocked in, the Q0 to Q3 outputs are applied to the word detector ML5, the Q6 output is applied to the monitor load pulse generator, and the Q7 output is applied to the enable pulse generator.

36. Following the detection of a correct sync. code, the '1' output signal from the counter controller (G18) is applied to G20 to allow the application of 40 clock pulses to the input shift register. Thus when the end-of-frame pulse is generated, it signifies that the last 40 bits of a serial data word are positioned in the 40-bit input shift register.

Word Detector

37. The word detector utilises a dual binary to 1-of-4 decoder ML5. Each decoder has two select inputs (A and B), an enable input (\overline{E}), and four mutually exclusive outputs $\overline{Q0}$ to $\overline{Q3}$. When the enable input is at logic '1', the \overline{Q} outputs are held at logic '1' regardless of the state of the A and B select inputs.

38. If word 0 is present in the 40-bit input shift register, the A and B inputs to both decoders are at '0'; this results in a '0' at the $\overline{Q0}$ output of ML5a (table 1), ML5b is enabled, and a '0' is produced at the $\overline{Q0}$ output which is applied to the monitor load pulse generator.

39. If word 1 is present in the 40-bit input shift register, the A and B inputs of ML5a and the B input of ML5b are at logic '0' whilst the A input of ML5b is at logic '1'. This results in a '0' at the $\overline{Q1}$ output of ML5b and this is applied to the enable pulse generator.

Table 1: Binary to 1-of-4 Decoder Truth Table

INPUTS			OUTPUTS			
\bar{E}	B	A	\bar{Q}_3	\bar{Q}_2	\bar{Q}_1	\bar{Q}_0
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

X = don't care

Frame Comparator

40. This comprises an exclusive OR gate G27, D-type flip-flop ML22b and NOR gate G28. The sync. code detect output signal at TP1 is applied to the reset input of ML22b and the \bar{Q} output is reset to logic '1'. G27 now compares the 40 bits of data contained in the input shift register with the next 40 data bits from the MA.1072 (via G1); if the two sets of data compare, the output from G27 is maintained at a '0' and the '1' is thus maintained at the \bar{Q} output of ML22b. If a bit error is detected, the output from G27 changes to a '1', the \bar{Q} output of ML22b changes to a '0', and this is latched by the resulting '1' output from G28 which is applied to the set input of ML22b.

Monitor Load Pulse Generator

41. A monitor load pulse is generated each time the presence of word 0 in the input shift register is detected, following a frame comparison failure, and when the return monitor bit (bit 9 of the SCORE format) is set to a '1' in conjunction with the single frame check bits of word 1 (in computer-assisted installations it is possible for the return monitor bit to be set independently of the word 1 single frame check bits).

42. The generator comprises three NOR gates G29, G30 and G31; a '0' output from ML5b pin 12, signifying the presence of word 0 in the input shift register, is inverted by G29 and results in a '0' at the output of G30. This is applied to G31, together with the inverted end-of-frame pulse from G26, and a nominal 6 μ s monitor load pulse is generated.

43. The output signal from the frame comparator, at ML22b pin 12, is applied to G23 of the enable pulse generator. A logic '1' not-enable output from G23 (para. 44) signifying a frame comparison failure, is applied to G30, setting its output to '0' to produce the monitor load pulse as before. Similarly, a logic '1' return monitor bit output from the

input shift register (ML13 Q6) is applied to G30 with the same result. The not-enable output from G23 is also applied to D4 which forms part of the error counter (para. 49).

Enable Pulse Generator

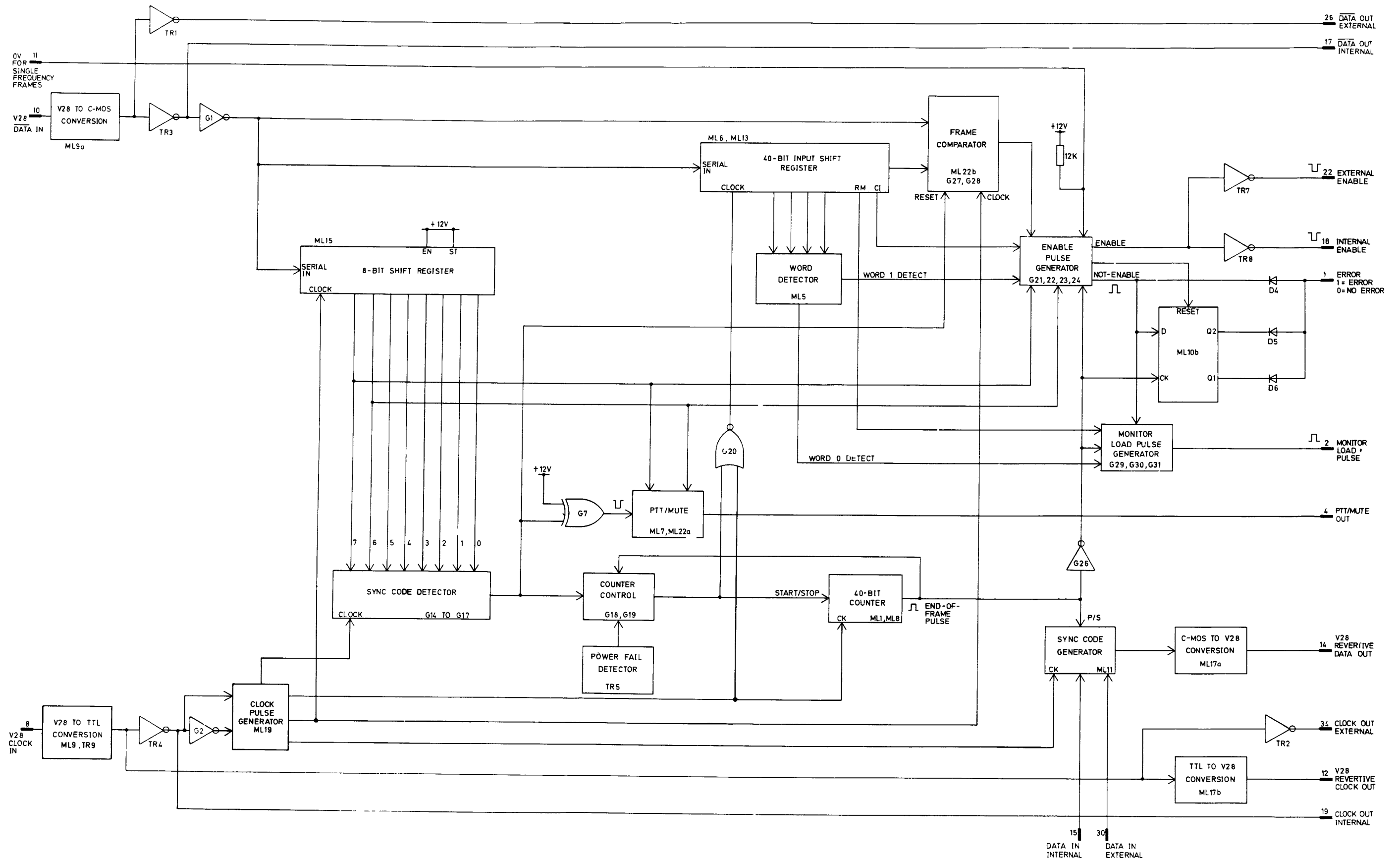
44. The enable pulse generator comprises four NOR gates G21 to G24, non-inverting buffer ML2b, and two open-collector output inverters TR7, TR8. It generates the enable pulse following a successful frame comparison, when the control inhibit bit is set to a '1' and also when the single frame check bits of the frequency word (bits 46 and 47) are set to a '0' - '1' code, coincident with a '0' output from ML5b pin 11 (signifying the presence of word 1 in the input shift register), and the presence of a '0' input at board pin 11.
45. The frame comparator output, at ML22b pin 12, is maintained at a '1' for a successful frame comparison; this is applied to G23, the resulting '0' output is applied to G24 together with the inverted end-of-frame pulse from G26, and the '1' output is applied to the inverting output stages TR7, TR8 via buffer ML2b. The negative-going 6 s (nominal) output pulse from TR7 is applied via board pin 22 to the external control connector on the receiver rear panel (for use by external equipment utilising the extra word facility), whilst the output from TR8 is applied via board pin 18 to the frequency and monitor and BFO and mode boards to enable the word detectors.
46. The control inhibit bit is set to a '1' at the MA.1072 when the CHECK status is selected. When the 40 bits of the control data word are correctly positioned in the input shift register, the control inhibit bit output, at ML13, Q7, is applied to G23, and the enable-pulse is produced.
47. Gates G21 and G22 are concerned with single frequency frames. When the 40 bits of the frequency word are correctly positioned in the 40-bit input shift register, data bits 40 to 47 are also located in the 8-bit shift register ML15. If the single frame check bits (bit 46 at ML15 Q1 and bit 47 at ML15 Q0) are set to a '0' - '1' code (signifying that new data frequency words are being generated at the MA.1072) and providing that a '0' is applied to board pin 11 (via a link at the external control connector), then all the inputs applied to G22 are at logic '0', and the '1' output produces the enable pulse, as before.
48. When routine control data is transferred from the MA.1072, the single frame check bits of word 1 revert to a '0' - '0' code, and the enable pulse is then generated via the frame comparator following a successful frame comparison.

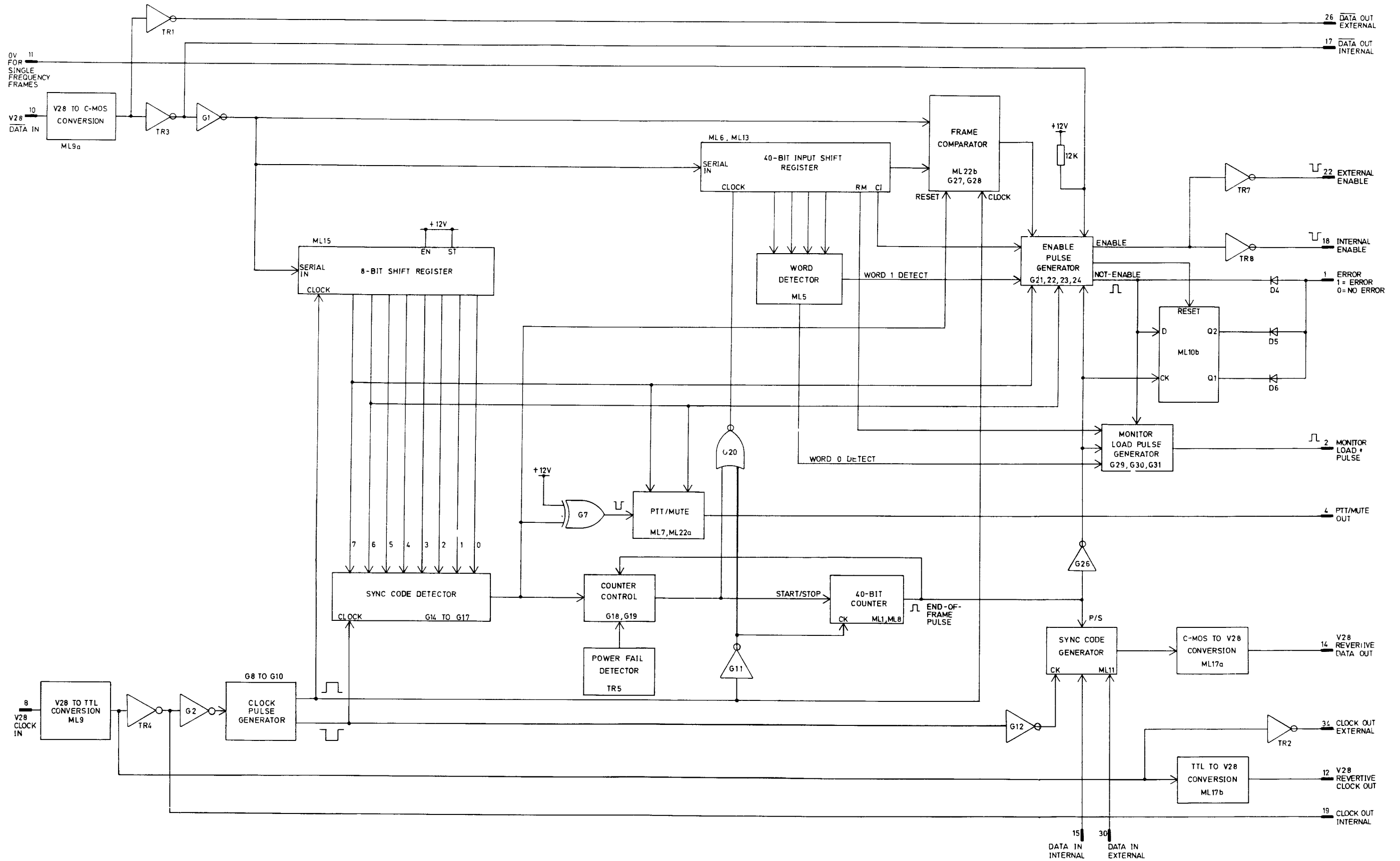
Error Counter

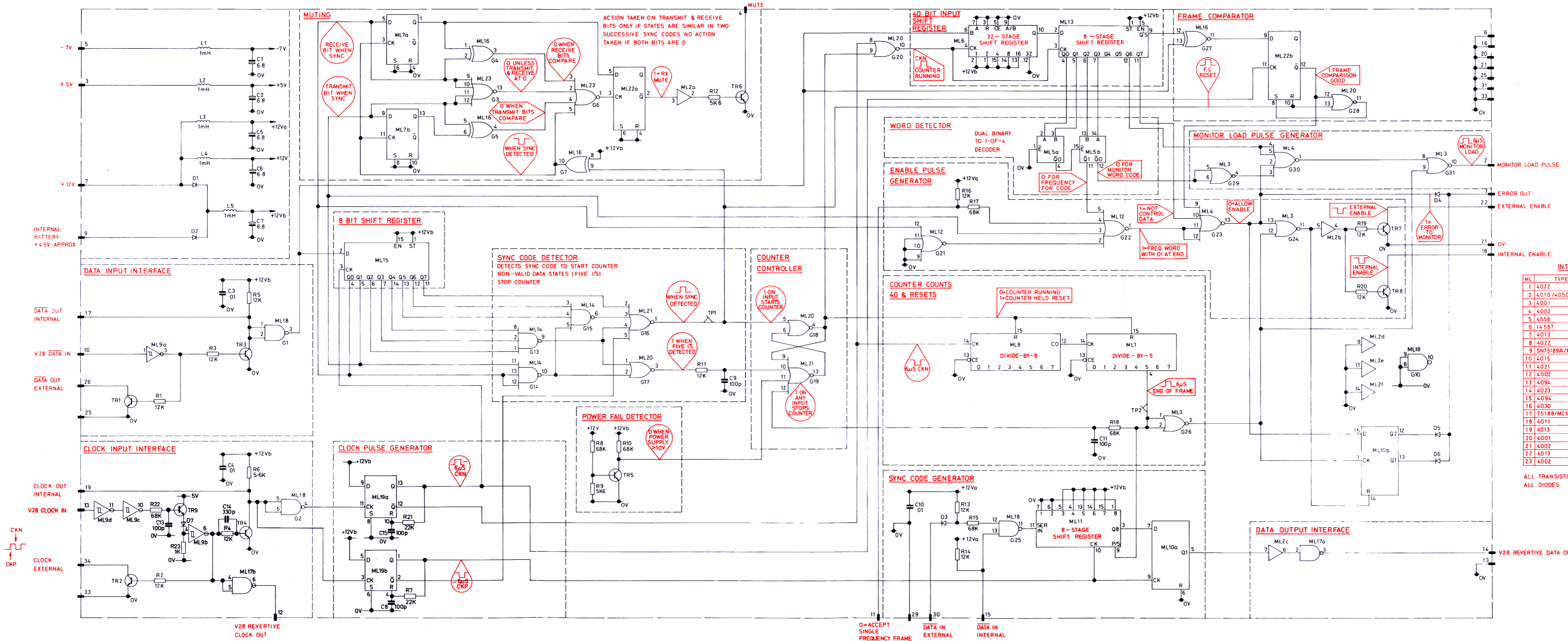
49. The error counter consists of a 2-bit shift register ML10b, and a three-diode AND gate D4, D5, D6. ML10b is reset (Q1 and Q2 outputs reset to '0') each time a successful frame comparison occurs, by the enable pulse output from G24. A frame comparison failure results in a logic '1' output from G23. This is applied to D4 and to the data input of ML10b. If three consecutive frame comparisons occur, then a '1' is applied to all three diodes, the '0' is removed from board pin 1, and the error line is pulled up to logic '1' via a resistor connected to the +12V rail (on the frequency and monitor board).

Sync. Code Generator

50. The inverted serial data for the enabled word, from the frequency and monitor board or the BFO and mode board, is applied to board pin 15, inverted by G25 and is then applied to the serial input of an 8-stage shift register ML11. The serial data from external equipment (utilising the extra word facility) is also applied to ML11, via the external control connector, board pin 30, D3 and G25.
51. The sync. code, i.e. a '0' followed by five '1's and then (in this case) two zeros, is set at the parallel input pins of ML11 and is jammed into the register by the end-of-frame pulse from ML1. The data is then serially clocked into ML11 to appear at the Q8 output in serial form preceded by the 8-bit sync. code. The D-type flip-flop ML10a introduces a one bit delay to achieve correct timing, and the serial data frames are then applied via buffer ML2c, a line driver stage ML17a, board pin 14 and the revertive data highway, to the MA.1072.







INTEGRATED CIRCUITS

ML	TYPE	+12Vg	+12Vb	OV	+5V	-7V
1	4022		16	8		
2	4010/4050		16	8	1	
3	4001		14	7		
4	4002		14	7		
5	4556		16	8		
6	14557		16	8		
7	4013		14	7		
8	4022		16	8		
9	SN75189A/MC1489A		7	14		
10	4015		16	8		
11	4021		16	8		
12	4002		14	7		
13	4094		16	8		
14	4023		14	7		
15	4094		16	8		
16	4030		14	7		
17	75188/MC1488L	14	7	7	1	
18	4011		14	7		
19	4013		14	7		
20	4001		14	7		
21	4002		14	7		
22	4013		14	7		
23	4002		14	7		

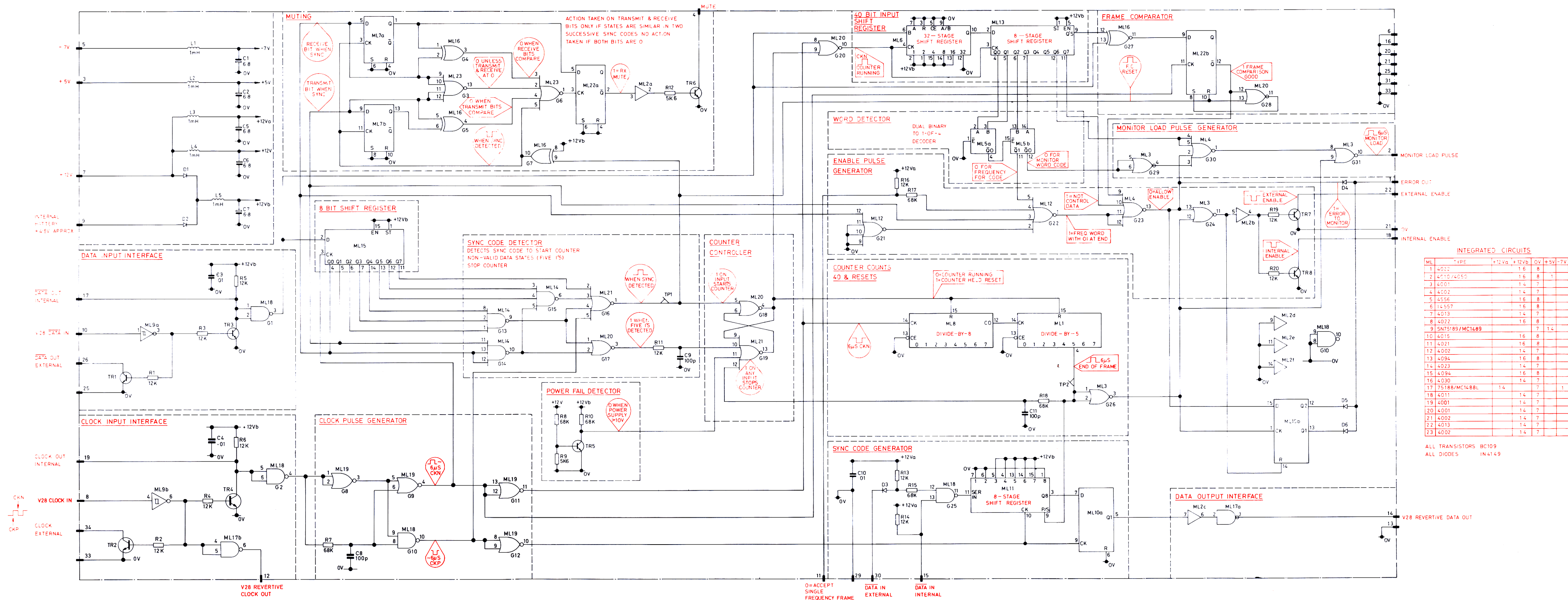
ALL TRANSISTORS BC109
ALL DIODES 1N4149

RACAL

WOH 6247	DC 76707	4/42	WOH 6247	DC 76707	4/42
1	1/2	1	1	1/2	2/2

Circuit: Serial Controller
Board PS667

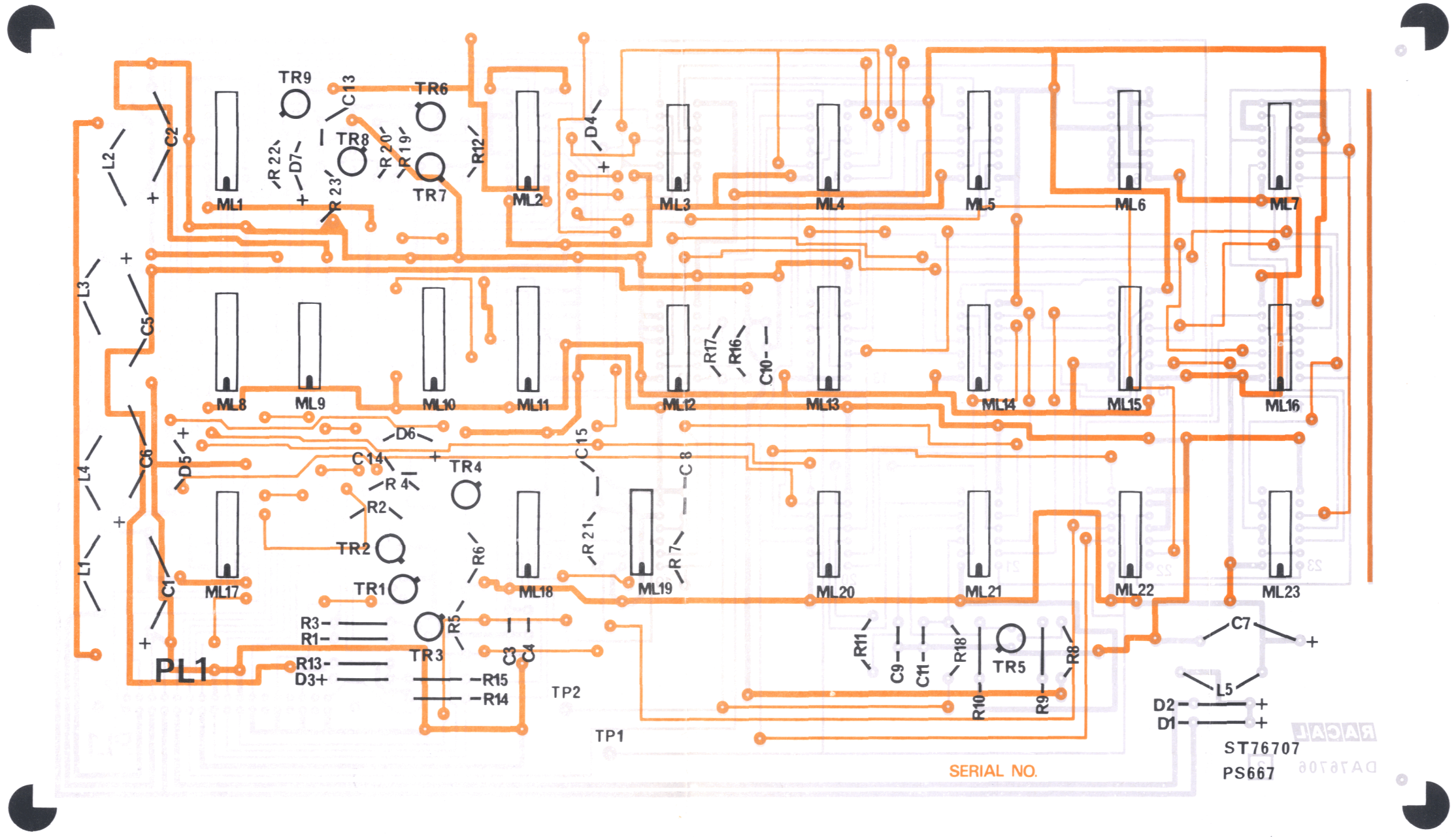
Part 4
Fig. 4-2



INTEGRATED CIRCUITS

ML	TYPE	+12V _a	+12V _b	OV	+5V -7V
1	4022	1.6	8		
2	4010/4050	1.6	8	1	
3	4001	1.4	7		
4	4002	1.4	7		
5	4556	1.6	8		
6	14557	1.6	8		
7	4013	1.4	7		
8	4022	1.6	8		
9	SN75189/MC1489	7	14		
10	4015	1.6	8		
11	4021	1.6	8		
12	4002	1.4	7		
13	4094	1.6	8		
14	4023	1.4	7		
15	4094	1.6	8		
16	4030	1.4	7		
17	75188/MC1488L	1.4	7		1
18	4011	1.4	7		
19	4001	1.4	7		
20	4001	1.4	7		
21	4002	1.4	7		
22	4013	1.4	7		
23	4002	1.4	7		

ALL TRANSISTORS BC109
ALL DIODES 1N4149



RACAL		
WOH7014	DA76706/4	4/4-3
		2/3

WOH7014	DA76706/4	4/4-3
1 2		3/3

CHAPTER 5

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FREQUENCY AND MONITOR BOARD PS666

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CHAPTER 5

FREQUENCY AND MONITOR BOARD PS666

INTRODUCTION

1. This board, as its name implies, contains the frequency word (word 1) and the monitor word (word 0) circuitry. A block diagram of the board is given in fig. 5.1; the circuit diagram is in two sheets, where sheet 1 contains the word 1 circuitry (fig. 5.2) and sheet two the word 0 circuitry (fig. 5.3).

FUNCTIONAL DESCRIPTION

FREQUENCY WORD

2. The inverted control data from the serial controller board, at PL3/30 (fig. 5.1), is applied via inverter G1 to a 40-bit input shift register ML6 to ML10. If word 1 is present in the register when the enable pulse occurs (at PL3/34), the word 1 detector ML5 is enabled and a correct word 1 identification code output from ML6 (data bits 12, 13, 14 and 15) results in a '0' output; provided that the control inhibit bit (bit 8) and the return monitor bit (bit 9) outputs from ML6 are not set to a '1', then a '1' is produced at the outputs of NOR gates G3 and G4.
3. The '1' output from G3 is applied to the strobe inputs of the input shift register stages ML7 to ML10, and the output from the power fail detector TR1 is applied to the enable inputs; this enables the parallel outputs, the BCD frequency setting data, at bits 20 to 45, is applied in paralleled form to the synthesizer section of the receiver, and is also applied, together with the remaining parallel output data, to the parallel inputs of a 40-bit output shift register ML16 to ML20.
4. The '1' output from G4 is applied as a parallel input enable signal to the output shift register stages, the parallel data is loaded in, and is subsequently clocked out in serial form via inverting buffer TR2 and PL3/33 to the serial controller board.
5. The control inhibit bit (bit 8) is set to a '1' when CHECK is selected at the MA.1072; the resulting absence of the strobe pulse output from G3 prevents the updating of the parallel output data (the parallel outputs of the input shift register are latched) and thus further control of the receiver frequency is inhibited. The '1' output from G4 is still produced however, and the latched parallel output data from the input shift register is loaded into the output shift register for subsequent return to the MA.1072.
6. The return monitor bit (bit 9) is set to a '1' at the MA.1072 when continuous revertive monitoring is required (normally used when single frequency frame transmission is required - see Chap.4). To prevent the return of the frequency word data to the MA.1072, the output from G4 is set to a logic '0' serial entry enable signal which is applied to the output shift register to inhibit parallel data entry.

MONITOR WORD

7. The monitor word (word 0) is used solely for revertive signalling and is returned to the MA.1072 each time the monitor load pulse is produced (on the serial controller board - Chap.4). This is applied as a parallel data entry pulse to a 40-bit shift register ML21 to ML25, the parallel monitor data is loaded in and is subsequently clocked out in serial form to the MA.1072 via TR5, PL3/33 and the sync. code generator on the serial controller board.

Revertive User Functions

8. Data bits 16 to 19 provide for the revertive user functions where up to four earth (0V) signals applied to the receiver (via the external control connector) are reproduced at rear panel connections at the MA.1072. A '0' at any (or all) of the user function input pins, PL3 pins 3, 7, 5 and 9, sets the corresponding data bit to a '1'.

Revertive Indicators

9. Data bits 29 and 31 to 34 are associated with the AFC LOCK, +20 dB, RF MUTE and FAULT indicators on the MA.1072 front panel. The AFC LOCK bit is set to a '1' when the receiver (equipped with the optional AFC board) has achieved AFC lock. Similarly, the transmitting (RF MUTE) bit is set to a '1' when the receiver is muted, and the reduced signal (+20 dB) bit is set to a '1' when the signal level at the receiver antenna socket is in excess of 300 mV (provided the facility has not been linked out on the RF board). The out-of-lock bit is set to a '1' following a fault condition in the synthesizer section of the receiver and the frame comparison error bit is set to a '1' when three consecutive frame comparison failures are detected (serial controller board); either of these conditions results in the illumination of the FAULT indicator at the MA.1072 (this indicator is also illuminated via circuitry within the MA.1072 following a break in the revertive data).

Metered Function

10. The metered function selection, i.e. RF level metering or AFC tuning, is initiated at the MA.1072 front panel by depressing either the RF LEVEL or the AFC TUNE push-button. A four-bit code is generated and is transferred to the receiver via the mode word data (word 5) as bits 20 to 23. The resulting four-bit coded output from the BFO and mode board (Chap.6) is routed to the frequency and monitor board, at PL3 pins 22, 20, 16 and 26, where BCD 1 selects RF level metering and BCD 2 selects AFC tune. The four-bit code is then returned to the MA.1072, via bits 36 to 39 of word '0' where it is used to illuminate either the RF LEVEL or the AFC TUNE push-button.

Meter Reading

11. The RF level or AFC tune meter reading is transferred to the MA.1072 in digital form via bits 40 to 42 and 44 to 47 of the word 0 data. Bit 43 is a forced zero to prevent the generation of a spurious sync. code.

12. The AFC metering voltage input at PL3/1 (from the AFC board) is applied via a buffer ML12a to a level shift and switching stage ML12d. The receiver IF gain control voltage from the main IF board at PL3/8, and that from the optional ISB IF board at PL3/2, is also applied to a level shift and switching stage ML1c, via an AGC voltage combiner ML12b, ML12c. The switching inputs are produced by the metering decode stage ML11, where BCD 1 at the four input lines enables ML1c (RF level metering) and BCD 2 enables ML12d (AFC tuning). The output voltage from either ML1c or ML12d, in the range 0V to -4.3V, is applied to an analogue-to-digital converter which comprises a 1 kHz oscillator G6, G7, a dual D-type flip-flop ML2, a binary up/down counter ML3, ML4, a digital-to-analogue converter ML1a, ML1b, ML13, and a switching voltage comparator ML1d, TR3.
13. The 1 kHz oscillator generates a clock waveform which is applied to ML2b, and to ML2a via inverter G8. ML2a generates $6\mu\text{s}$ (nominal) clock pulses for the up/down counter, whilst the output from ML2b controls the up/down count function.
14. The switching voltage comparator compares the analogue voltage level output from either ML1c or ML12d with that from the digital-to-analogue (D-to-A) converter; if a level difference exists, a '1' count-up or a '0' count-down output is produced, the inversion of which is applied to the binary counter via ML2b. The 7-bit binary output from the counter is thus increased or reduced until the output voltage level from the D-to-A converter is the same as the output voltage level from either ML1c or ML12d. When this happens, the up/down output from the switching voltage comparator alternates between '0' and '1' at the clock frequency, and thus the least significant bit output from the counter continually changes up and down by one count; this fluctuation is however, damped by the MA.1072 meter and a steady reading is produced.
15. The carry-out (CO) output from the binary counter is normally at logic '1' and changes to a '0' when the counter reaches its maximum count in the up mode or the minimum count in the down mode; when this occurs the D input of ML2a changes to a '0', the $6\mu\text{s}$ clock pulses are no longer produced, and the binary counter is stopped.
16. The monitor load pulse, which parallel-enables the shift register stages, is also used to inhibit the 1 kHz oscillator: This stops the action of the analogue-to-digital converter whilst the 7-bit binary coded meter reading data is parallel-loaded into ML23. The inverter G8 is included to delay the application of the binary counter clock signal until the count-up/count-down input has been determined.

CIRCUIT DESCRIPTION

FREQUENCY WORD (fig. 5.2)

40-Bit Input Shift Register

17. The inverted serial control data from the serial controller board, at PL3/30, is applied via inverting NOR gate G1 to the serial input of a 40-bit input shift register comprising five cascaded 8-stage shift registers ML6 to ML10. These devices have a

storage latch associated with each stage for strobing data from the serial input to parallel buffered outputs. The data in each shift register stage is transferred to the storage register when the strobe (ST) input is a logic '1', and the data in each storage register appears at the associated parallel output (Q0 to Q7) when the enable (EN) input is at logic '1'. Data is shifted on the positive-going transition of the clock input waveform.

Power Fail Detector

18. The power fail detector TR1 monitors the +12V output from the power supply section of the receiver, such that should this supply fall to less than 10V (approximately), conduction of TR1 ceases, the enable input is removed from the input shift register, and further up-dating of the receiver frequency setting data is inhibited.

Word 1 Detector

19. The word 1 detector comprises a dual binary to 1-of-4 decoder ML5. Each decoder has two select inputs (A and B), an enable input (\bar{E}), and four mutually exclusive outputs ($\bar{Q0}$ to $\bar{Q3}$). When the enable input is at logic '1', the outputs are maintained at a '1' regardless of the state of the A and B select inputs.

20. If word 1 data is present in the input shift register when the enable input (at PL3/34) occurs, ML5a is enabled and the four-bit binary 1 ident. output from ML6, at data bits 12 to 15, results in a '0' output from ML5a (table 1); provided that the control inhibit (CI) and return monitor (RM) bits are not set to a '1', then the '0' output from ML5a results in a '1' output from NOR gate G3, and a '1' output from NOR gate G4. The '1' output from G3 strobes the input shift register, whilst the '1' output from G4 is applied as a parallel input enable pulse to the 40-bit output shift register (para. 21).

40-Bit Output Shift Register

21. This comprises five cascaded 8-stage shift registers ML16 to ML20. These are static parallel or serial input/serial output shift registers. When the parallel/serial (P/S) input is at logic '0', data is serially shifted into (and out of) the register synchronously with the positive-going transition of the clock waveform; when the P/S input is at logic '1', the data at the parallel input pins is jammed into the register independently of the clock waveform.

22. When the word 1 detector detects the presence of word 1 in the input shift register, the resulting '1' output from G3 strobes the input shift register stages; the parallel frequency setting data output is applied to the parallel inputs of the output shift register, and to the synthesizer section of the receiver via buffers ML26 to ML30. The '1' output from G4 parallel enables the output shift registers, the parallel data is loaded in, and is subsequently clocked out in serial form to the MA.1072 via inverter TR2, PL3/33 and the sync. code generator on the serial controller board.

Control Inhibit

23. When the control inhibit bit, at ML6 Q7, is set to a '1', strobe pulse generation is inhibited via G3 and further up-dating of the frequency setting data is prevented.

Return Monitor

24. When the return monitor bit, at ML6 Q6, is set to a '1', the output of G4 is forced to a '0' to prevent parallel data entry of the 40-bit output shift register.

MONITOR WORD (fig. 5.3)

Output Shift Register

25. The 40-bit output shift register comprises five cascaded 8-bit shift registers ML21 to ML25. These are static 8-stage parallel or serial input/serial output shift registers. When the parallel/serial (P/S) input is at logic '0' data is serially shifted into the register synchronously with the positive-going transition of the clock waveform; when the P/S input is at logic '1', the data at the parallel inputs P1 to P8 is jammed into the register independently of the clock waveform. Since the monitor load pulse, at PL5/17, is routed to the P/S input of each stage, every time the monitor load pulse occurs, the data at the parallel input pins is jammed into the register and is subsequently clocked out in serial form to the MA.1072 via TR5, PL3/33 and the sync. code generator on the serial controller board.

User Functions

26. The revertive user function connections are made at the external control connector on the receiver rear panel, pins 30 to 33 for A to D respectively. When an earth is applied to any of these inputs, it is inverted by the respective NOR gate G9 to G12, and sets the respective bit of the word 0 data to a '1' (data bits 16 to 19).

Revertive Indicator Bits

27. Data bits 29 and 31 to 34 are associated with the AFC LOCK, +20 dB, RF MUTE and FAULT indicators on the MA.1072 front panel. A '0' AFC lock input at PL3/10 turns off TR4 and sets data bit 29 to a '1', whilst a '1' at any of the remaining inputs, at PL3 pins 6, 24, 18 and 14, directly sets the associated data bit to a '1'.

Metered Function

28. The BCD metered function input at PL3 pins 22, 20, 16 and 26, which comes from the BFO and mode board, is set to BCD 1 for RF level metering and to BCD 2 for AFC tuning. The 4-bit code is applied to ML21 as data bits 36 to 39, and is also applied to a decode circuit (para. 29).

Metering Decode

29. The 4-bit metered function code is applied to a decode circuit comprising a dual binary to 1-of-4 decoder ML11. Each decoder has two select inputs (A and B) an enable input (\overline{E}) and four mutually exclusive outputs ($\overline{Q0}$ to $\overline{Q3}$). When the enable input is a logic '1', the $\overline{Q0}$ to $\overline{Q3}$ outputs are maintained at logic '1' regardless of the state of the A and B select inputs.

30. The truth table for a single decoder is given in Table 1. From this table it can be seen that the $\overline{Q0}$ output from ML11a is only at logic '0' (to enable ML11b) when both the A and B inputs are at logic '0'; the $\overline{Q1}$ output from ML11b is at logic '0' for a '0' - '1' B-A input, and the $\overline{Q2}$ output is at logic '0' for a '1' - '0' B-A input. The '0' - '1' or '1' - '0' coded output signal from ML11b is used to select either the AFC tuning voltage or the IF gain voltage for application to the analogue-to-digital converter which generates the 7-bit meter reading data.

Table 1: 1-of-4 Decoder Truth Table

Inputs			Outputs			
Enable	Select		$\overline{Q3}$	$\overline{Q2}$	$\overline{Q1}$	$\overline{Q0}$
\overline{E}	B	A				
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

X = Don't care

AFC Tuning/RF Level Selection

31. The AFC tuning voltage input at PL3/1, from the optional AFC board, is applied to a buffer stage ML12a, and is then applied to a level shift and switching stage ML12d via R14 and R15. The main IF AGC voltage input at PL3/8, and that from the optional ISB IF board at PL3/2, are each applied to a buffer stage, ML12b and ML12c respectively; the output at TP1, which is equal to the higher of the two output voltages from ML12b and ML12c, is applied to a level shift and switching stage ML1c via a potential divider R16, R18 and R17.

32. The two level shift and switching stages are controlled by the outputs from the metering decode stage ML11b; a '0' $\overline{Q1}$ output effectively switches on ML12d (which becomes a virtual-earth amplifier) whilst the logic '1' $\overline{Q2}$ output switches off ML1c by applying reverse bias to D7. When RF level metering is selected the $\overline{Q1}$ output changes to a '1', and the $\overline{Q2}$ output changes to a '0'; ML12d is switched off and ML1c becomes a virtual-earth amplifier.
33. The output voltage from either ML12d or ML1c, in the range 0V to -4.3V (level shift preset by R15 or R18 respectively), is applied to a switching voltage comparator ML1d, TR3.

Analogue-to-Digital Converter

34. The RF level or AFC tuning meter reading is converted into a 7-bit digital signal for transfer to the MA.1072 via bits 40 to 42 and 44 to 47 of the word 0 data. The analogue-to-digital converter comprises a 1 kHz oscillator G6, G7, a counter control stage ML2, a binary up/down counter ML3, ML4, a digital-to-analogue (D-to-A) converter ML1a, ML1b, ML13, and a switching voltage comparator ML1d, TR3. These stages are described in the following paragraphs under the appropriate heading.

1 kHz Oscillator

35. This comprises NOR gates G6 and G7 with frequency determining components R13 and C20. The 1 kHz squarewave output from G7, together with the output from inverting NOR gate G8, is applied to the counter controller ML2.

Counter Controller

36. The counter controller consists of a dual D-type flip-flop ML2. ML2a generates the clock pulses for the binary up/down counter (providing the D input is at logic '1'), whilst ML2b controls the up/down input applied to the binary counter according to the output level from the switching voltage comparator. The squarewave output from the 1 kHz oscillator is applied to the clock input of ML2b in advance of the clock input applied to ML2a (via G8) so that the up/down function is properly determined before operation of the up/down counter.

Binary Up/Down Counter

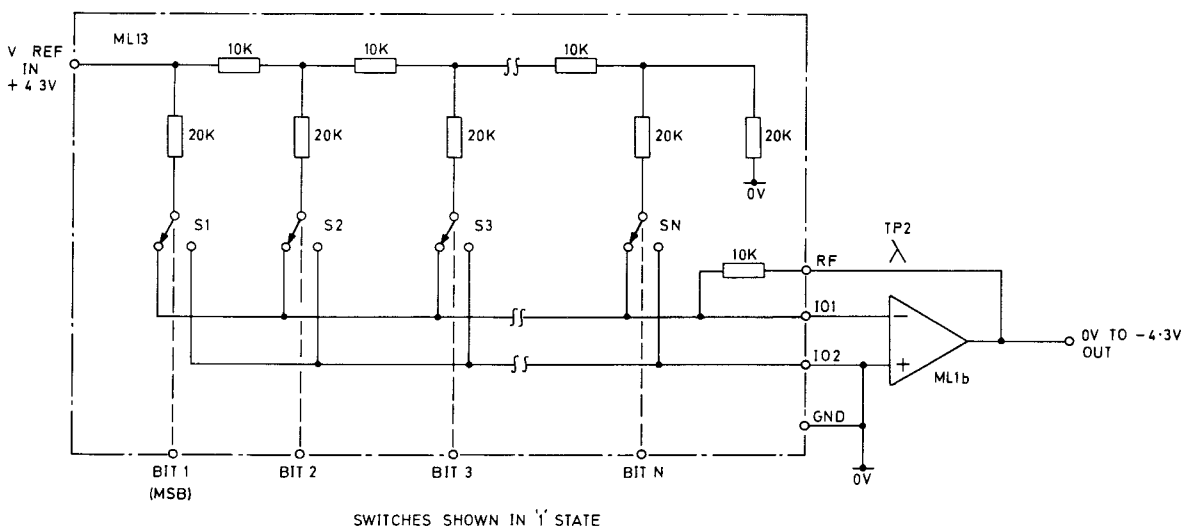
37. This uses two 4-stage counters, ML3, ML4, which are connected in the parallel-clock mode. The parallel inputs (for presetting the counter) are not used and are all connected to 0V, as are the preset enable inputs. The binary/decimal control inputs are connected to the +12V rail (for binary operation) whilst the clock inhibit input of ML4 is connected to 0V. The counter is advanced one count at the positive-going transition of the clock waveform when both the clock inhibit and preset enable inputs are at logic '0'. The advancement of ML3 is therefore inhibited until the CO output from ML4 changes from '1' to '0', and this only happens when ML4 reaches its maximum count in the up mode or its minimum count in the down mode. Similarly, the CO output from ML3 is normally at logic '1' and only changes to a '0' when the counter reaches its maximum count in the up mode

(binary 64 or 128 clock pulses) or the minimum count in the down mode (zero). The counter counts up when the up/down input is at logic '1', and down when the up/down input is at logic '0'.

38. The 7-bit binary coded output from the counter is applied to the output shift register (as data bits 40 to 42 and 44 to 47) and is also applied to a D-to-A converter ML13.

D-to-A Converter

39. ML13 is a 10-bit (bits 8, 9 and 10 are not used) multiplying D-to-A converter. From the functional diagram of this device given in fig. 5(i), it can be seen that the current at the I01 terminal, and hence the voltage developed across the feedback resistor, is dependent on the switch positions. With all the switches in the logic '0' state, the voltage at TP2 is zero; with all the switches in the '1' state, the voltage at TP2 is $-4.3V$, which, since the I01 terminal is connected to the inverting input of ML1b, is equal to the inverse of the reference voltage output from buffer ML1a. The output voltage from ML1b, in the range $0V$ to $-4.3V$, is applied to the switching voltage comparator (para. 40).



RACAL

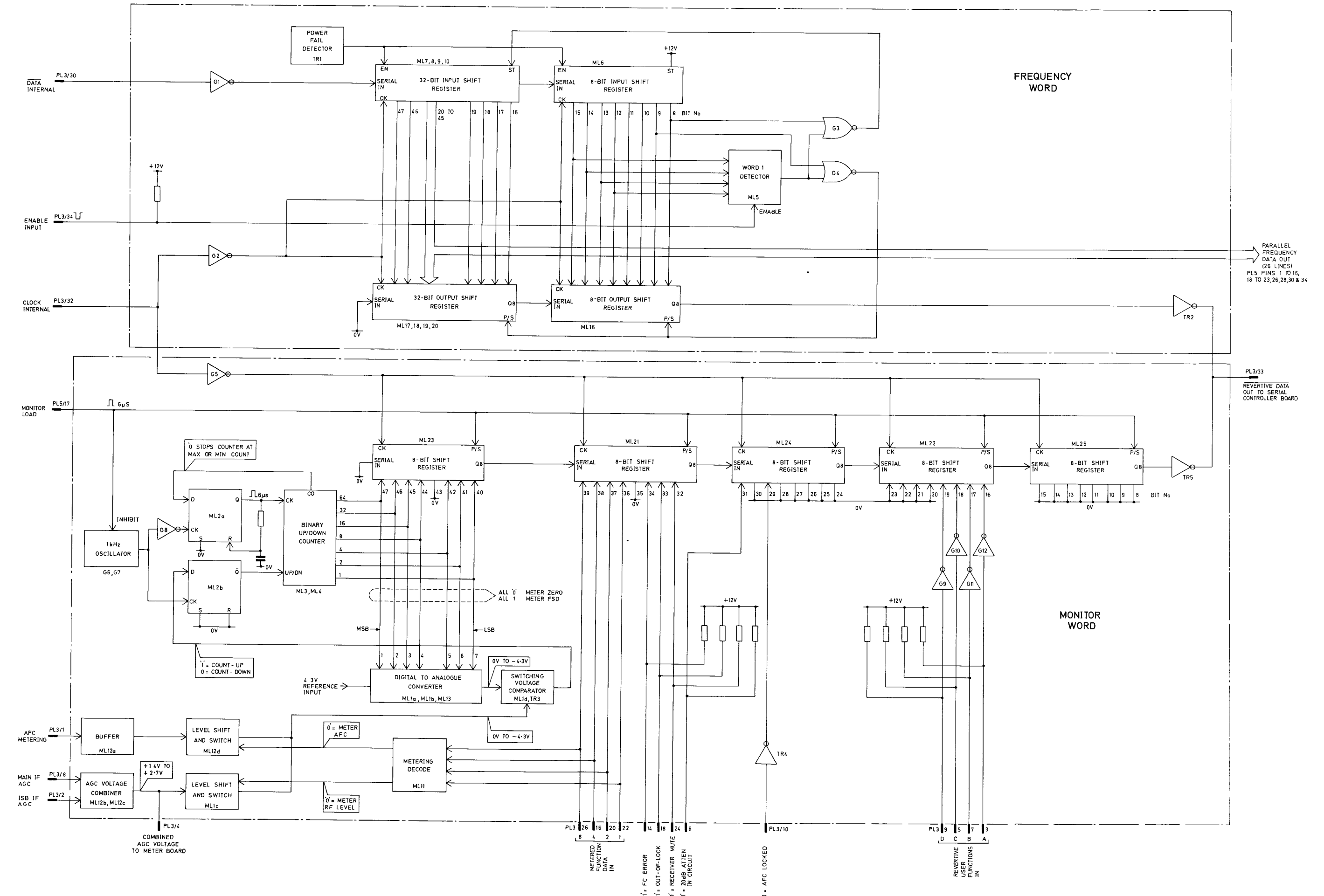
Functional Diagram : D to A Converter

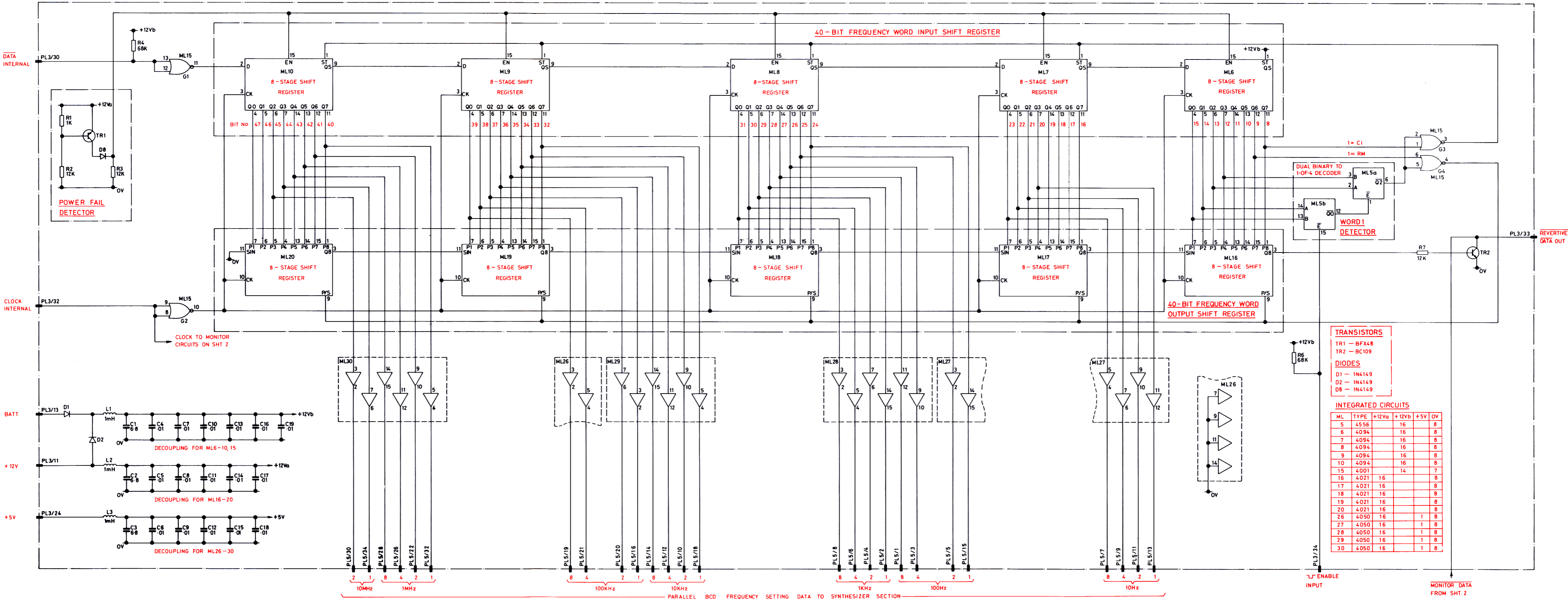
Fig.5(i)

Switching Voltage Comparator

40. This stage comprises a comparator ML1d and a switching transistor TR3. The output voltage from either the AFC tuning circuit or the RF level circuit, at TP5, is compared with the output voltage from ML1b, at TP2. If, for example, the voltage level at TP5 is less negative than the voltage level at TP2, the resulting positive output voltage from ML1d turns off TR3, a logic '1' is applied to the D input of ML2b, and this results in the application of a logic '0' count-down signal to the binary up/down counter; the counter then counts down until the voltage at TP2 is equal to the voltage at TP5. Conversely, if the voltage level at TP5 is more negative than the voltage at TP2, TR3 conducts, a logic '0' is

applied to the D input of ML2b, and the resulting logic '1' count-up signal causes the counter to count up until balance is again restored.

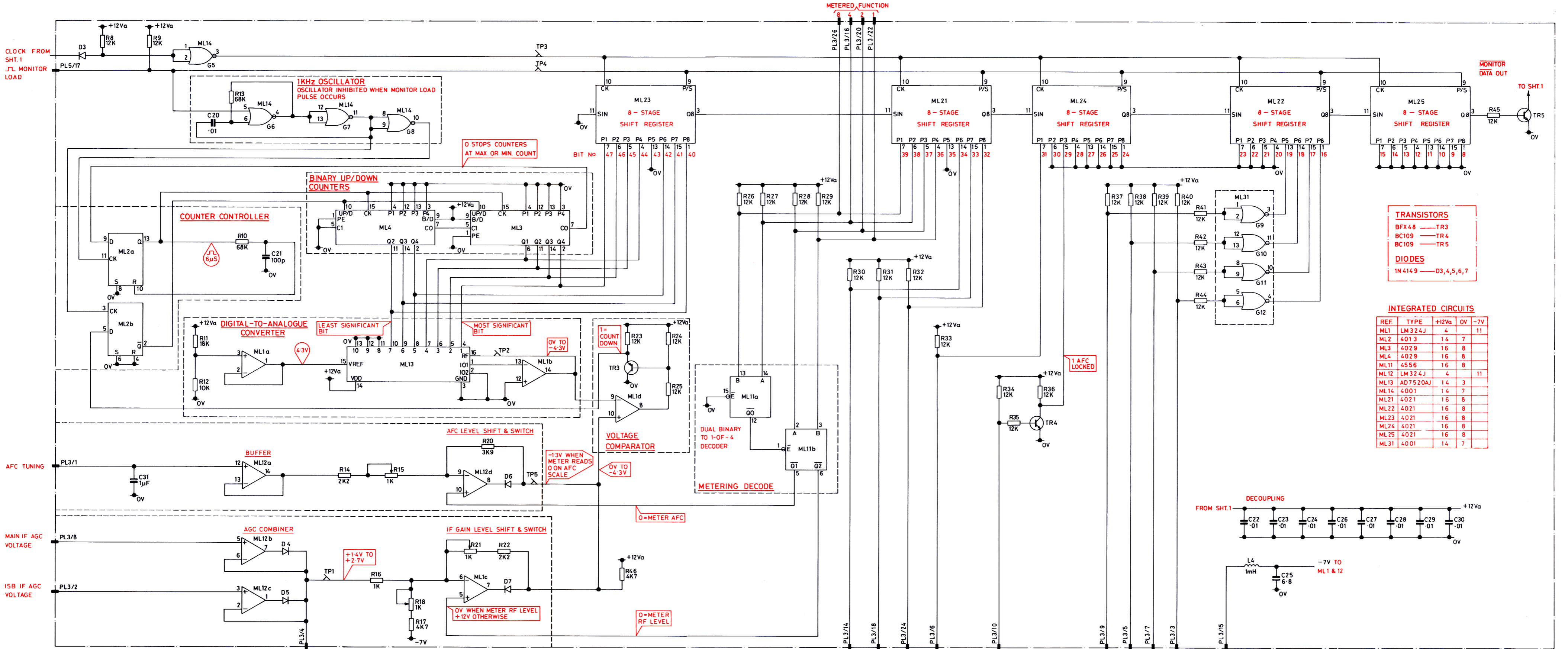




- TRANSISTORS**
- TR1 - BFX48
 - TR2 - BC109
- DIODES**
- D1 - 1N4149
 - D2 - 1N4149
 - D8 - 1N4149

INTEGRATED CIRCUITS

ML	TYPE	+12V _a	+12V _b	+5V	OV
5	4556		16		8
6	4094		16		8
7	4094		16		8
8	4094		16		8
9	4094		16		8
10	4094		16		8
15	4001		14		7
16	4021	16			8
17	4021	16			8
18	4021	16			8
19	4021	16			8
20	4021	16			8
26	4050	16		1	8
27	4050	16		1	8
28	4050	16		1	8
29	4050	16		1	8
30	4050	16		1	8



- TRANSISTORS**
 BFX 48 — TR3
 BC109 — TR4
 BC109 — TR5
- DIODES**
 1N 4149 — D3, 4, 5, 6, 7

INTEGRATED CIRCUITS

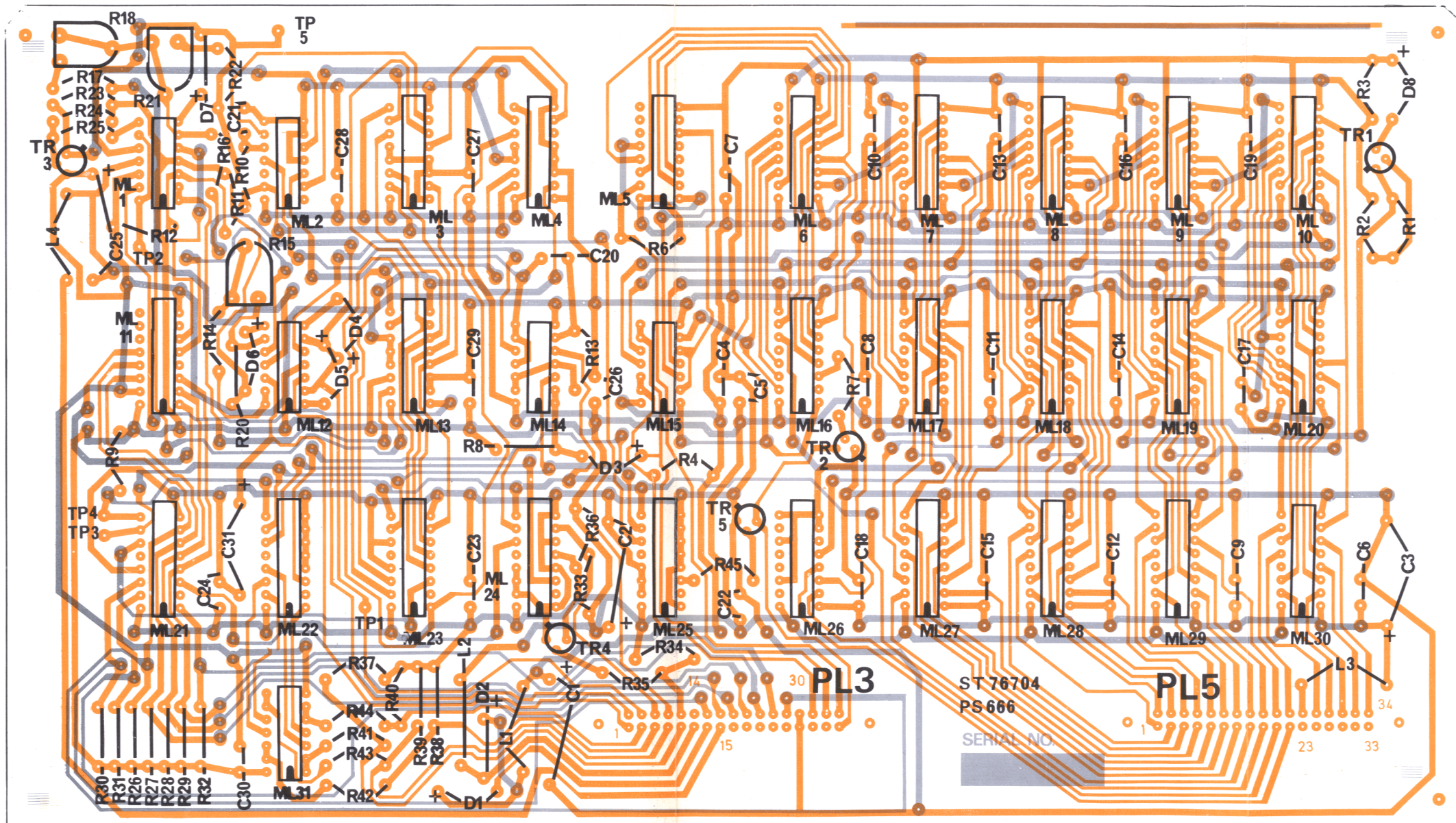
REF	TYPE	+12Va	OV	-7V
ML1	LM 324 J	4	11	
ML2	401 3	14	7	
ML3	402 9	16	8	
ML4	402 9	16	8	
ML11	455 6	16	8	
ML12	LM 324 J	4	11	
ML13	AD7520AJ	14	3	
ML14	4001	14	7	
ML21	4021	16	8	
ML22	4021	16	8	
ML23	4021	16	8	
ML24	4021	16	8	
ML25	4021	16	8	
ML31	4001	14	7	

RACAL

WOH 6247	DC 76704 SHT 2	4/5 3	WOH 6247	DC 76704 SHT 2	4/5 3
1	1/2	1	1	2/2	2/2

Circuit : Frequency &
 Monitor Board PS 666 (Sheet 2)

Part 4
 Fig 5.3



RACAL	DA 76703/4	4/5-4
		2/3
WOH 7014	DA 76703/4	4/5-4
1		1/3
WOH 7014	DA 76703/4	4/5-4
1		3/3

Layout: Frequency &
Monitor Board

CHAPTER 6

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BFO AND MODE BOARD PS 668

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CHAPTER 6

BFO AND MODE BOARD PS668

INTRODUCTION

1. This board, as its name implies, contains the BFO (analogue) word and the mode word circuits. A block diagram of the board is given in fig.6.1. The circuit diagram is produced on two sheets; sheet 1 (fig.6.2.) contains the BFO word (word 2) circuitry, whilst sheet 2 (fig.6.3.) contains the mode word (word 5) circuitry.

FUNCTIONAL DESCRIPTION

POWER FAIL DETECTOR

2. The power fail detector (fig.6.1.) provides the enable input for the 40-bit input shift registers for both the BFO word (para.3) and the mode word (para.8). If the +12V output from the power supply section of the receiver falls to less than approximately +10V, the enable input is removed and further updating of the parallel control data applied to the receiver is inhibited.

BFO WORD

40-Bit Input Shift Register

3. The inverted serial control data input from the serial controller board, at PL2/8, is applied via inverter G1 to a 40-bit input shift register ML11 to ML15. If word 2 is present in the register when the enable pulse occurs (at PL2/6), the word 2 detector ML23 is enabled and a correct word 2 identification code output from ML15 (data bits 12, 13, 14 and 15) results in a '0' output; provided that the control inhibit bit (bit 8) and the return monitor bit (bit 9) outputs from ML15 are not set to a '1', then a '1' is produced at the outputs of NOR gates G3 and G4.

4. The '1' output from G3 is applied to the strobe inputs of the input shift register stages ML11 to ML14. Provided that the enable inputs are also at logic '1' (para.2), the parallel outputs are enabled, and the word 2 data is applied to the parallel inputs of the 40-bit output shift register stages ML1 to ML4. The BFO frequency setting data, at bits 16 to 26, is also applied in parallel form to the receiver (decoder board) together with the BFO sign output at bit 27. Data bits 40 to 42 and 44 to 47 contain the manual IF gain control setting information; this is applied to a digital-to-analogue converter, and, provided the '0' enable input is present (para.12) the analogue gain control voltage outputs are applied to the main and ISB (where fitted) IF boards.

40-Bit Output Shift Register

5. This comprises five cascaded 8-stage shift registers ML1 to ML5. The data at the parallel input pins is jammed into the register by a '1' output pulse from G4, and the data is subsequently clocked out in serial form to the MA.1072 via TR2, PL2/12, the sync. code generator on the serial controller board and the revertive data highway.

Control Inhibit

6. The control inhibit bit (bit 8) is set to a '1' when CHECK is selected at the MA.1072; the resulting absence of the strobe pulse output from G3 prevents the updating of the parallel output data (the parallel outputs of the input shift register are latched) and thus further control of the receiver is inhibited. The '1' output from G4 is still produced however, and the latched parallel output data from the input shift register is loaded into the output shift register for subsequent return to the MA.1072.

Return Monitor

7. The return monitor bit (bit 9) is set to a '1' at the MA.1072 when continuous revertive monitoring is required (normally used when single frequency frame transmission is required - see chap.4). To prevent the return of the BFO word data to the MA.1072, the output from G4 is set to a logic '0' serial entry enable signal which is applied to the output shift register to inhibit parallel data entry.

MODE WORD

8. The operation of the mode word circuitry is similar to that of the BFO word described in the preceding paragraphs. It comprises a 40-bit input shift register ML16 to ML20 which is strobed by the output of the word 5 detector (via G26). The enabled parallel output data from the input shift register is applied to the parallel inputs of a 40-bit output shift register ML6 to ML10; this data is jammed into the register by the parallel-enable input pulse from the word 5 detector (via G17), and is subsequently clocked out in serial form to the MA.1072 via TR13, PL2/12, the sync. code generator on the serial controller board and the revertive data highway. The parallel output data from the input shift register is decoded (where necessary) and is then applied to the receiver. The functions of the various decode circuits are described in the following paragraphs.

Metered Function

9. Data bits 20 to 23 control the metered function and are set to BCD 1 for RF LEVEL or to BCD 2 for AFC TUNING. The 4-bit coded output, at PL4 pins 21, 23, 25 and 27, is routed to the frequency and monitor board where it is applied to the metering decode circuit and to the word 0 output shift register for return to the MA.1072.

AFC Decode

10. When the optional AFC board is fitted, a 0V connection from the AFC board is routed to the AFC decode circuit via PL4/8; the combination of this and a '1' at bit 24 results in a '0' AFC 'on' output at PL2/30, which is applied to the AFC board. Data bit 25 is set to a '1' for full carrier (-6dB), and results in a '0' at PL2/28, whilst data bit 27 is set to a '1' for pilot carrier (-20dB), and results in a '1' at PL2/28.

AM/CW Decode

11. The mode bits (bits 28 and 29), together with bit 32, are applied to the AM/CW decoder and also to the bandwidth and sideband decoder (para.15). For the AM mode, bit 32 must be at logic '1', bit 28 must also be at logic '1', and bit 29 must be at logic '0' (for a '0' output at PL4/10); for the CW mode, bit 32 must be at logic 1, bit 28 at logic '0' and bit 29 at logic '1', for a '1' output at PL4/10. The logic '1' bit 32 output is also applied via PL4/19 to the decoder board, where it strobes in the parallel BFO frequency setting data (from word 2) for the CW mode.

AGC Decode

12. Data bits 37, 38 and 39 convey the AGC information; bits 37 and 38 are applied to the AGC decoder where a '0'-'0' code selects AGC SHORT, and a '0'-'1' code selects AGC LONG. (a '1'-'1' code de-selects both short and long, and routes a '1' to the AGC dump decoder). Bit 39 is set to a '0' for MANUAL IF gain; this is applied to the digital-to-analogue converter for the manual IF gain control setting data (para.4) as an enable input.

AGC Dump Decode

13. Bit 36 is used for AGC dump and is set to a '1' in the first pair of mode word frames sent after AGC LONG is selected. Its purpose is to discharge the AGC long time constant capacitors, located on the IF board(s), so that they may re-charge to the level of the signal being received. The circuit generates a 3ms dump pulse (clocked for convenience by the input shift register strobe pulse) which is routed to the main and ISB (where fitted) IF boards via PL4/31.

14. When the AGC is switched off, a '1' output from the AGC decoder (para.12) causes a permanent dump to be applied to the receiver to keep the time constant capacitors discharged.

Bandwidth and Sideband Decode

15. This circuit controls the selection of the appropriate 1.4MHz crystal filter on the IF filter board. If data bit 32 is set to a '1', it signifies that the receiver is set to the AM or CW mode (para.11), and the coding of bits 40 to 42 is used to select one of the available symmetrical filters (see Part 3 Chap.5). If data bit 32 is set to a '0', the coding of bits 28 and 29 selects a sideband mode (table 1) and data bits 40 to 42 are not used.

Table 1: Sideband Selection

CODING			SIDEBAND
Bit 32	Bit 29	Bit 28	
0	0	0	USB
0	0	1	LSB
0	1	0	ISB-U
0	1	1	ISB-L

Roofing Filter Select

16. An optional narrow band ($\pm 500\text{Hz}$ nominal) 35.4MHz roofing filter may be fitted to the first mixer board; this filter may be switched into circuit (in place of the standard $\pm 6\text{kHz}$ bandwidth filter) in conjunction with any of the symmetrical 1.4MHz IF filters fitted to the IF filter board. A bank of six single-pole switches is fitted to the BFO and mode board, one for each filter; if for example, the switch associated with filter 4 is closed, when filter 4 is selected, a 0V signal at PL4/32 is routed to the first mixer board and the narrow-band roofing filter is selected.

Audio Switching Decode

17. The audio input signals applied to the amplifiers on the AF board (two line amplifiers and one monitor amplifier) are taken from the main IF board and/or the ISB IF board (ISB version only). For SSB receivers, or ISB receivers switched to SSB, the audio output signal from the main IF board is applied to all three audio amplifiers, whilst for ISB receivers set for ISB operation, one line amplifier is fed from the main IF board and the other line amplifier is fed from the ISB IF board. The input signal to the audio monitor amplifier is fed from the main IF board when ISB-U is selected, or from the ISB IF board when ISB-L is selected.

18. Three of the input signals applied to the audio switching decoder are taken from the bandwidth and sideband decoder, and a fourth input, at PL2/29, is connected to 0V when the ISB IF board is fitted.

User Functions

19. The four forward data user function outputs, at bits 47, 46, 45 and 44, are routed via inverters TR3 to TR6 and PL1 pins 7, 5, 3 and 1 respectively, to the external control connector on the receiver rear panel.

CIRCUIT DESCRIPTION

POWER FAIL DETECTOR

20. The power fail detector TR1 (fig.6.2) is powered by the +12V output from the power supply section of the receiver, and provides a '1' output signal which is applied to the enable inputs of the word 2 input shift register, and the word 5 input shift register (fig.6.3). If the level of the +12V supply falls to less than +10V (approximately), TR1 ceases to conduct, the enable signal is removed, and further up-dating of the word 2 and word 5 parallel data applied to the receiver is inhibited.

BFO WORD

40-Bit Input Shift Register

21. The inverted serial control data at PL2/8 is applied via inverting NOR gate G1 to a 40-bit input shift register comprising five cascaded 8-stage shift registers ML11 to ML15. These devices have a storage latch associated with each stage for strobing data from the serial input to the parallel outputs. The data in each shift register stage is transferred to the associated storage latch when the strobe input is at logic '1', and the data in each storage latch appears at the respective parallel output pin, Q0 to Q7, when the enable input is at logic '1'. Data is shifted on the positive-going transistion of the applied clock waveform.

Word 2 Detector

22. The word 2 detector uses a dual binary to 1-of-4 decoder ML23. A number of these devices are used on the BFO and mode board and consist of two types; type 4555 has '1' level outputs when selected, whilst type 4556 has '0' level outputs when selected. Each decoder has two select inputs (A and B), an enable input (E), and four mutually exclusive outputs. When the enable input is at logic '1' the outputs of the 4555 remain at '0' and the outputs of the 4556 remain at '1' regardless of the state of the select inputs A and B. A truth table for both types is given in Table 2.

Table 2: Binary to 1-of-4 Decoder Truth Table

INPUTS			OUTPUTS							
Enable		Select	4555				4556			
E	B	A	Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = don't care

23. If word 2 is present in the input shift register when the enable pulse occurs (at PL2/6), the A and B inputs of ML23a are both at '0' (data bits 15 and 14); the $\overline{Q0}$ output is thus also at '0' (table 2) and this enables ML23b. The '1' at data bit 13 is applied to the B input, and the '0' at data bit 12 is applied to the A input of ML29b, and the resulting '0' $\overline{Q2}$ output is applied to NOR gates G3 and G4; provided that the control inhibit bit output from ML15 is not set to a '1', then the '1' output from G3 is applied to the strobe inputs of ML11 to ML14 of the input shift register, and the parallel output data is applied to the output shift register (para.24).

40-Bit Output Shift Register

24. This comprises five cascaded 8-stage shift register stages ML1 to ML5. These are parallel or serial input/serial output registers. When the parallel/serial control input is at logic '0', data is serially shifted into the register synchronously with the positive-going transition of the clock waveform; when the parallel/serial control input is at logic '1', the data at the parallel input pins Q0 to Q7 is jammed into the register independently of the clock waveform.

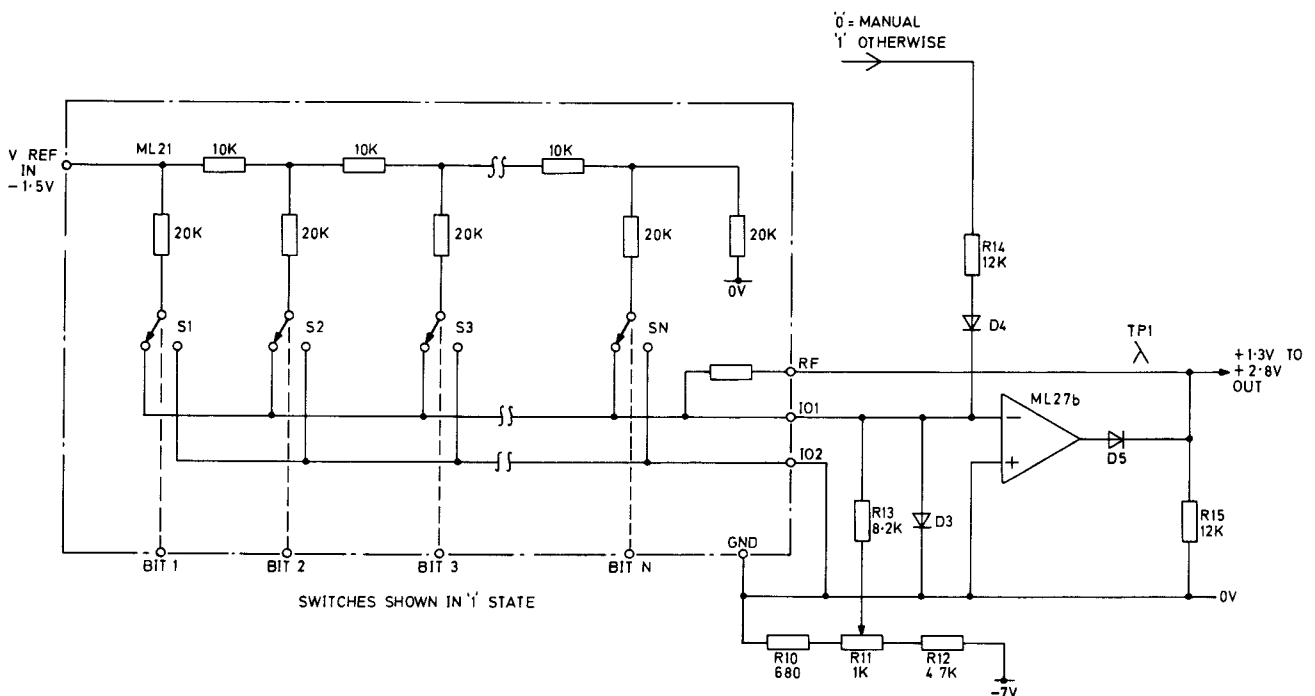
25. Provided that the return monitor bit output from ML15 (bit 9) is not set to a '1' when the presence of word 2 is detected, the '1' output from G4 is applied as a parallel entry pulse to the output shift register, the parallel data is loaded in, and is subsequently clocked out in serial form to the MA.1072 via inverter TR2, PL2/12, the sync. code generator on the serial controller board and the revertive data highway.

BFO Frequency Setting Data

26. The BFO frequency setting data is conveyed, in BCD form, via data bits 16 to 27; this is routed, together with the BFO sign bit (bit 28), to the decoder board (Part 2 Chap.8).

IF Gain Control Data

27. The digitised manual IF gain control setting information is conveyed via data bits 39 to 42 and 44 to 47 to a digital-to-analogue converter ML21, ML27. ML21 is a 10 bit (bits 9 and 10 are not used) multiplying D-to-A converter which is essentially a resistive ladder network and ten single-pole two-way switches controlled by the levels of the digital inputs. A functional diagram is given in fig.6(i). The current at the IO1 terminal, and hence the voltage developed across the feedback resistor, is dependent on the switch positions. With all the switches in the '0' state, the output voltage at TP1 is set by R11 to a level of +1.3V; with all the switches in the '1' state, the voltage at TP1 is equal to the inverse of the -1.5V reference voltage (applied to ML21 via buffer ML27a) plus the 1.3V offset voltage from R11, which equals +2.8V.



PART 4 Fig 6 (i) WOH70/L

RACAL

Functional Diagram : D to A Converter

Fig. 6(i)

28. When the manual gain is switched off, a '1' is applied to R14; this is limited to approximately +0.7V by D3 and reverse bias is applied to D4 via ML27b to inhibit any output at TP1.
29. The 1.3V to 2.8V output from ML27b is applied to a pair of buffer stages, ML27c, ML27d and thence via PL2/33 to the main IF board, and via PL2/31 to the ISB IF board (where fitted).

MODE WORD (fig.6.3)

30. The 40-bit input shift register ML16 to ML20, and the 40-bit output shift register ML6 to ML10, are similar to those of the BFO word (described in the preceding paragraphs). The input shift register stages are enabled by the output from the power fail detector (para.20), and are strobed by the output from NOR gate G16 when the presence of the word 5 data is detected (by ML26). The parallel output data is applied to the parallel input pins of the output shift register stages, and is jammed into these stages by the logic '1' output pulse from G17. The data is subsequently clocked out in serial form to the MA.1072 via inverter TR13, PL2/12 (fig.6.2), the sync. code generator on the serial controller card, and the revertive data highway.

Metered Function

31. The metered function data is transferred via bits 20 to 23 (BCD 1 for RF LEVEL, BCD 2 for AFC TUNE), and is routed to the frequency and monitor board via PL4 pins 21, 23, 25 and 27.

AFC Decode

32. Data bits 24 to 27 are applied to the AFC decoder which comprises a dual binary to 1-of-4 decoder ML24. Bit 24 is set to a '1' for the AFC-on condition; this is applied to ML24a together with a '0' AFC-fitted signal at PL4/8 (from the AFC board) and results in a '1' at the Q1 output (table 2). This is inverted by TR11 and is then routed to the AFC board via PL2/30.

33. The remaining three bits, 25, 26 and 27, are used for full or pilot carrier selection. Bit 25 is set to a '1' (with bits 26 and 27 at '0') for AFC FULL CARRIER (-6dB) and results in a '1' at the Q1 output of ML24b; this is inverted by TR12 and is then routed to the AFC board via PL2/28. For AFC PILOT CARRIER operation (-20dB), bit 27 is set to a '1', this is applied to the \bar{E} input of ML24b, the Q1 output is set to a '0' (table 2), and this results in a '1' at PL2/28.

AM/CW Decode

34. This uses a single binary to 1-of-4 decoder ML32b which is only enabled when bit 32 is set to a '1' (inverted by NAND gate G12). A '1'-'0' output from bits 28 and 29 sets the $\bar{Q1}$ output to a '0' (AM selected) whilst a '0'-'1' output sets the $\bar{Q1}$ output to a '1' (CW selected).

AGC Decode

35. The AGC information is conveyed via data bits 37, 38 and 39. Bits 37 and 38 are applied to a binary to 1-of-4 decoder ML34, where a '0'-'0' code selects AGC SHORT (via PL4/34) and a '0'-'1' code selects AGC LONG (via PL4/33). A '1'-'1' code denotes the AGC-off condition and results in a '1' at the Q3 output which is applied to the AGC dump decoder (para.38).

36. Bit 39 is set to a '0' for manual IF gain; this is routed to the D-to-A converter (fig.6.2) as an enable input.
37. The coding of bits 37, 38 and 39 is summarised in table 3.

Table 3: AGC Decode

CODING			FUNCTION
Bit 39	Bit 38	Bit 37	
0	0	0	MANUAL & SHORT
0	1	0	MANUAL & LONG
0	1	1	MANUAL ONLY
1	0	0	SHORT
1	1	0	LONG

AGC Dump Decode

38. The AGC dump decoder comprises a dual D-type flip-flop ML36, G7 and TR10. The dump bit (bit 36), which is set to a '1' in the first pair of mode word frames sent after AGC LONG is selected, is applied to the D input of ML36b; when this stage is clocked by the strobe pulse output from G16, the '1' is transferred to the Q output, and a 3ms pulse is generated (reset applied after time constant presented by R28 and C21). This pulse is inverted by TR10 and is then applied to the IF boards via PL4/31 where it is used to discharge the AGC LONG time constant capacitors.
39. The AGC dump pulse is also generated when the 20dB attenuator on the RF board is brought into circuit, a '1' is applied to the clock input of ML36a (via PL4/29), the '1' at the D input is transferred to the Q output, and a 1µs pulse is produced (reset applied after time constant of R27 and C20). This pulse is applied to the set input of ML36b, the Q output changes to a '1', and the 3ms dump pulse is produced.
40. When the AGC is switched off, a '1' is applied to the set input of ML36a (from the AGC decoder - para.35); the Q output is held at a '1' (the set input overrides the reset input), the Q output of ML36b is also held at a '1', and a permanent '0' dump output is produced to keep the AGC LONG time constant capacitors discharged.

Bandwidth and Sideband Decode

41. This circuit, which comprises three binary to 1-of-4 decoders ML30a, ML30b, ML32a, NAND gates G8 to G11 and NOR gates G14, G15, controls the selection of the appropriate 1.4MHz filter on the IF filter board (Part 3 Chap.5).

42. For the AM and CW modes, bit 32 is set to a '1'; this is inverted by either G9 or G10 to enable either ML30a or ML32a, in accordance with the coding of bits 40 to 42, for the selection of a symmetrical filter (table 4). The '1' at bit 32 is also applied to the \bar{E} input of ML30b to inhibit sideband selection.

Table 4: Symmetrical Filter Selection

CODING			FILTER SELECTED
Bit 42	Bit 41	Bit 40	
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6

43. When a sideband mode is selected, bit 32 is set to a '0'. This enables ML30b for the selection of a sideband mode in accordance with the coding of data bits 28 and 29 (table 1); it is also applied to G9 and to G10 to inhibit symmetrical filter selection by applying a '1' to the \bar{E} inputs of ML30a and ML32a (table 2).

Roofing Filter Select

44. This circuit consists of a miniature 6-pole 2-way switch SW1, NAND gate G22, and TR14. When a switch is closed and the associated filter is selected, a logic '0' is applied to G22, the '1' output is inverted by TR14, and is routed to the first mixer board to select the narrow-band roofing filter.

Audio Switching Decode

45. The audio switching decoder comprises NAND gates G13, G18, G19, and NOR gates G20, G21. Three of the applied input signals are taken from the sideband decoder, ML30b Q1, Q2 and Q3 outputs, and a fourth input is applied to inverter G13 ('0' for ISB, '1' otherwise).

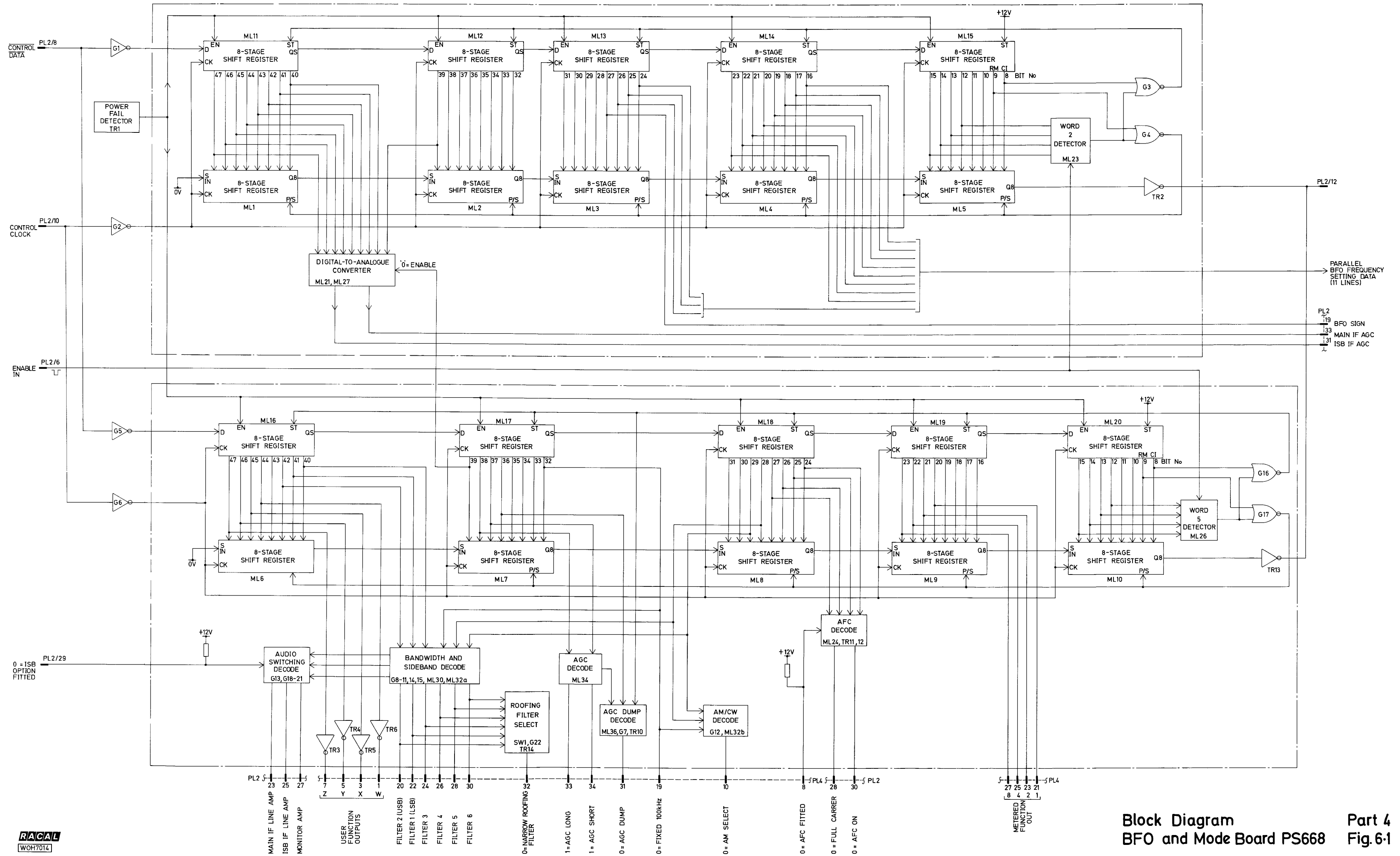
46. The output signals at PL2 pins 23, 25 and 27 are applied to a switching circuit on the AF board which routes the audio output signal from the main IF board, and that from the ISB IF board (where fitted) to the appropriate audio amplifier in accordance with table 5.

Table 5: Audio Switching Decode

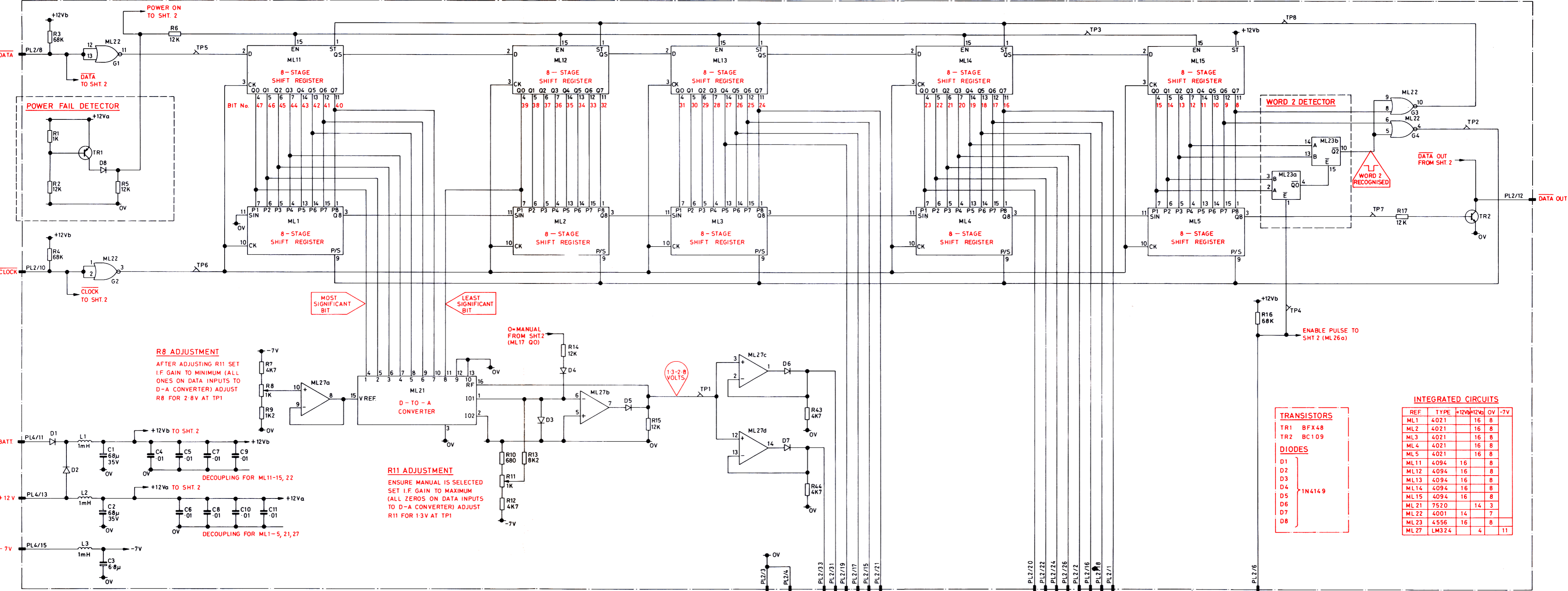
RECEIVER MODE	AUDIO AMPLIFIER		LINE 1 AMPLIFIER		LINE 2 AMPLIFIER	
	INPUT SOURCE	PL2/27 LEVEL	INPUT SOURCE	PL2/23 LEVEL	INPUT SOURCE	PL2/25 LEVEL
<u>SSB RECEIVERS</u>						
ALL MODES	MAIN IF	1	MAIN IF	1	MAIN IF	1
<u>ISB RECEIVERS</u>						
LSB	ISB IF	0	ISB IF	0	ISB IF	0
ISB-U	MAIN IF	1	MAIN IF	1	ISB IF	0
ISB-L	ISB IF	0	MAIN IF	1	ISB IF	0
OTHER MODES	MAIN IF	1	MAIN IF	1	MAIN IF	1

User Functions

47. The four forward data user function outputs, at bits 47, 46, 45 and 44, are routed via open collector inverter stages TR3 to TR6 and PL1 pins 7, 5, 3 and 1 respectively, to the external control connector on the receiver rear panel.



Block Diagram
BFO and Mode Board PS668
Part 4
Fig. 6-1



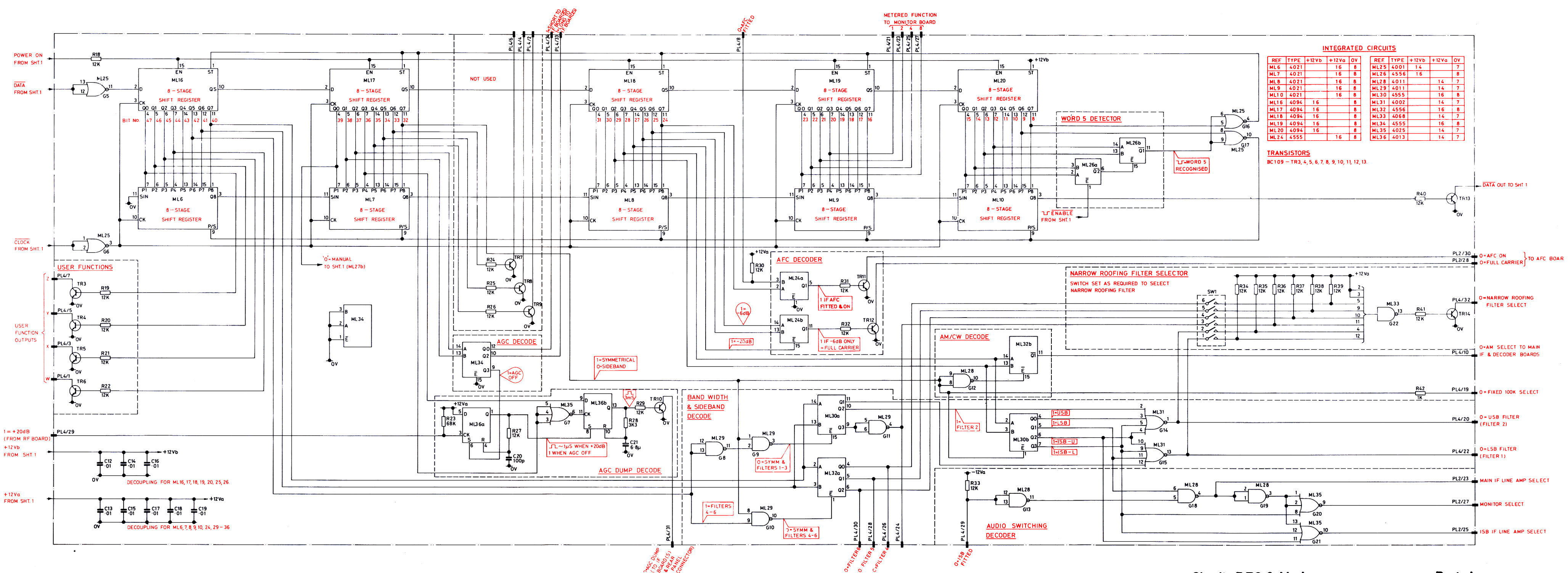
W0H6247	DC76710	SHT1	4/6.2	W0H6247	DC76710	SHT.1	4/6.2
1			2/2				2/2

TRANSISTORS	
TR1	BFX 48
TR2	BC109

DIODES	
D1	1N4149
D2	
D3	
D4	
D5	
D6	
D7	
D8	

INTEGRATED CIRCUITS				
REF	TYPE	+12Vb	+12Va	-7V
ML1	4021	16	8	
ML2	4021	16	8	
ML3	4021	16	8	
ML4	4021	16	8	
ML5	4021	16	8	
ML11	4094	16	8	
ML12	4094	16	8	
ML13	4094	16	8	
ML14	4094	16	8	
ML15	4094	16	8	
ML21	7520	14	3	
ML22	4001	14	7	
ML23	4556	16	8	
ML27	LM324	4	11	

Circuit: BFO & Mode Board (Sheet 1) Part 4 Fig 6.2



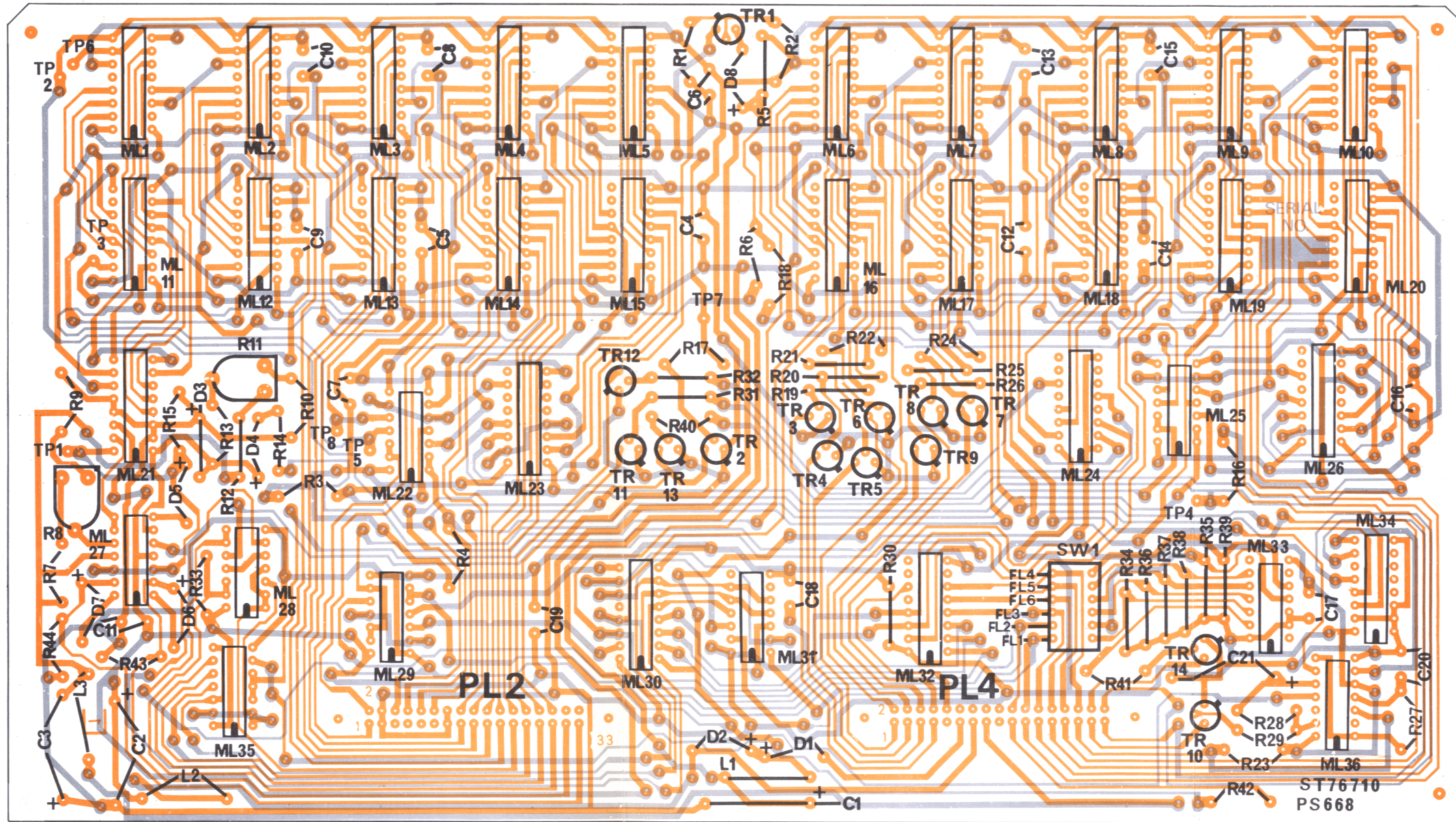
INTEGRATED CIRCUITS

REF	TYPE	+12Vb	+12Va	OV
ML6	4021	16	8	7
ML7	4021	16	8	8
ML8	4021	16	8	14
ML9	4021	16	8	14
ML10	4021	16	8	16
ML16	4094	16	8	14
ML17	4094	16	8	16
ML18	4094	16	8	14
ML19	4094	16	8	16
ML20	4094	16	8	14
ML24	4555	16	8	7
ML25	4001	14	8	7
ML26	4556	16	8	8
ML28	4011	14	7	7
ML29	4011	14	7	7
ML30	4555	16	8	8
ML31	4002	14	7	7
ML32	4556	16	8	8
ML33	4068	14	7	7
ML34	4555	16	8	8
ML35	4025	14	7	7
ML36	4013	14	7	7

TRANSISTORS
BC109 - TR3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13

WOH 6247	DC 76710 SHT.1	4/6.3	WOH 6247	DC 76710 SHT.1	4/6.3
1	1/2		1	1/2	2/2

Circuit: BFO & Mode Board PS668 (Sheet 2) Part 4 Fig6.3



RACAL	DA 76709/2	4/6-4
		2/3
WOH 7014	DA 76709/4	4/6-4
1		1/3
WOH 7014	DA 76709/3	4/6-4
1		3/3

Layout: BFO & Mode Board

CHAPTER 7
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METER SWITCHING / STANDBY BATTERY BOARD
=====

PS 669
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Layout: Meter Switching/Standby Battery Board	7.2

CHAPTER 7

METER SWITCHING/STANDBY BATTERY BOARD PS669

INTRODUCTION

1. This board contains the front panel meter drive circuitry, the standby battery, and the output transformer for the audio monitor line output. The circuit diagram of the board is given in fig. 7.1.

CIRCUIT DESCRIPTION

Power Supply Monitoring

2. The -7V, +5V, +12V and +20V outputs from the power supply section of the receiver, at PL6 pins 20, 18, 2 and 16 respectively, are applied to the meter switch 2S1 via suitable dropping resistors to produce a meter indication within the green portion of the meter scale for each supply.

Drive Level

3. The 35.4 to 65.4 MHz local oscillator drive signal (applied to the first mixer stage of the receiver) is also applied to a meter drive circuit on the first mixer board. A preset adjustable resistor is set to produce a meter indication (via PL6 pin 32) within the V scale brackets for a correct drive level.

Audio Monitor

4. The output signal from the audio monitor amplifier on the AF board is applied to the audio monitor line output transformer T1, and a full-wave bridge rectifier, D1 to D4, via PL6 pins 8 and 10. The output from T1 is applied via R18 to the front panel PHONES socket, 2JK1, and to the external control connector on the receiver rear panel via PL6 pins 12 and 14. The output voltage from the MONITOR LEVEL potentiometer 2R1, on the front panel, is applied to the AF board via PL6 pin 31.

5. The rectified audio monitor signal from D1 to D4 is applied to the meter switch via R8 and board pins 15 and 17.

AM/USB and LSB metering

6. The bridge rectifiers for the AM/USB and LSB audio signals are mounted on the AF board. The output voltages from the USB and LSB LINE LEVEL potentiometers, 2R2 and 2R3, are applied to the AF board via PL6 pins 34 and 33.

RF Level Metering

7. The AGC voltage input at PL6 pin 3 (combined AGC voltage for ISB versions) is used to provide an indication of received signal strength (dB scale on the front panel meter). The two preset potentiometers R14, R16 are adjusted to provide a 0 dB indication for a receiver input level of $2\ \mu\text{V}$, and an indication of 100 dB for a receiver input level of 200 mV, i.e. $2\ \mu\text{V}$ plus 100 dB). The setting-up procedures for these potentiometers are given in Part 1, Chap.4.

Carrier Tuning

8. The TUNE CARRIER position of the meter switching is only applicable to receivers equipped with the AFC facility. When AFC is switched off (at the MA.1072), the meter acts as a null indicator and should read approximately zero for an accurately tuned full or pilot carrier signal. When either AFC FULL or AFC PILOT is selected at the MA.1072, the meter provides an indication of available AFC hold range.

9. The output signal from the AFC board, at PL6 pin 22, is applied to the meter switch via a buffer stage ML1, and R19.

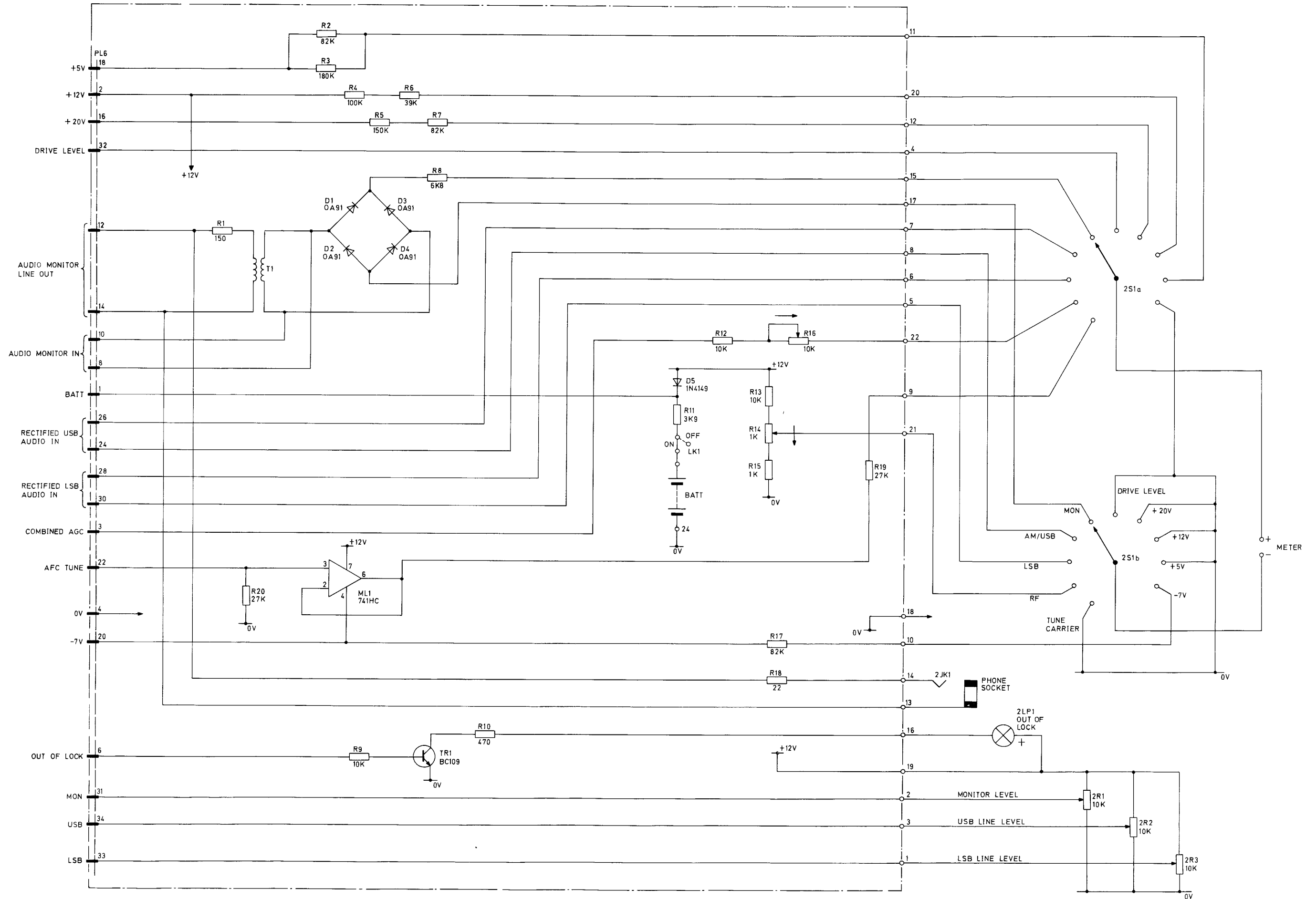
OUT-OF-LOCK Lamp

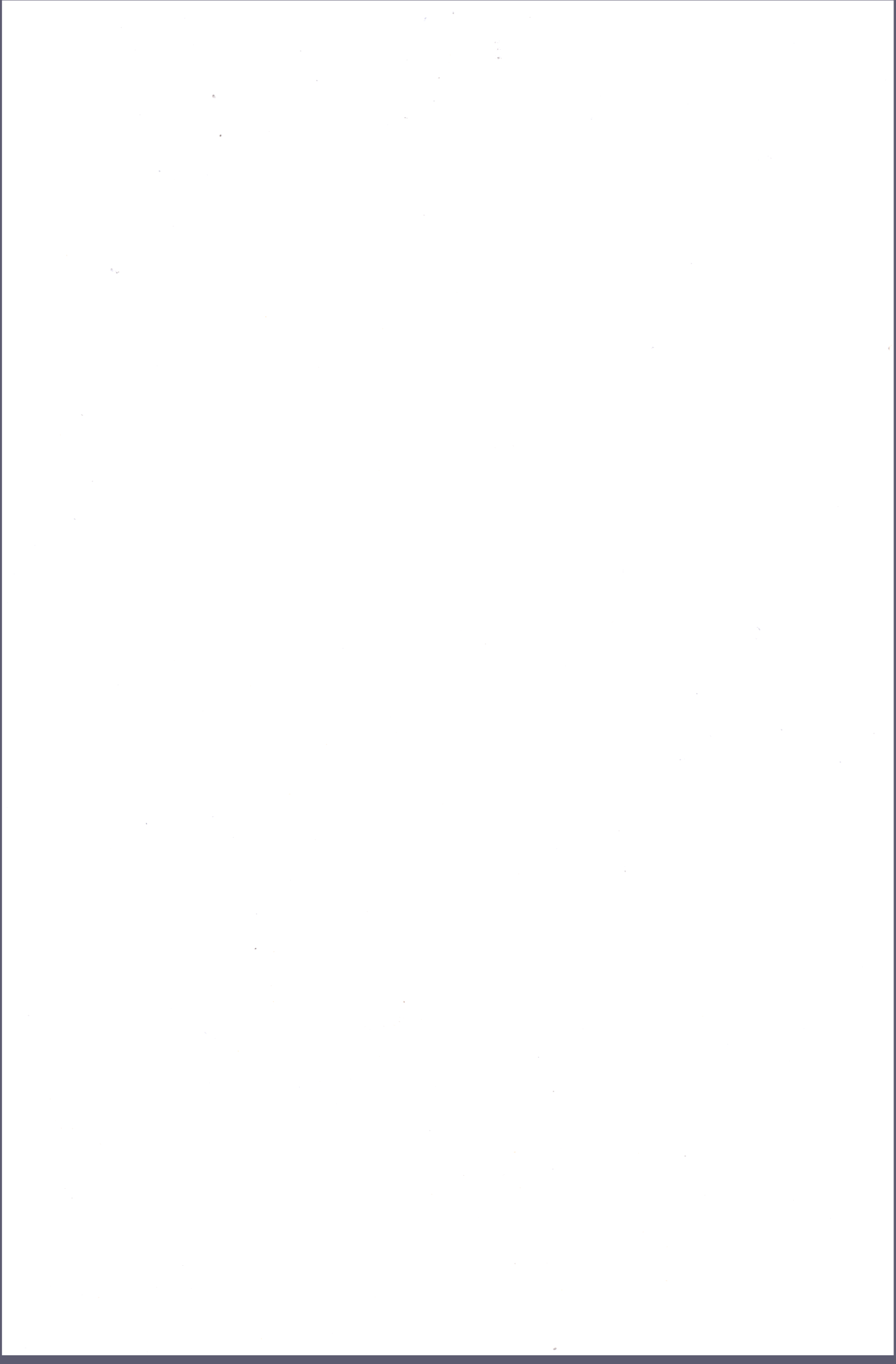
10. This lamp illuminates to indicate an out-of-lock condition at the synthesizer; a logic '1' out-of-lock input, at PL6 pin 6, is inverted by TR1 and 2LP1 is illuminated from the +12V supply.

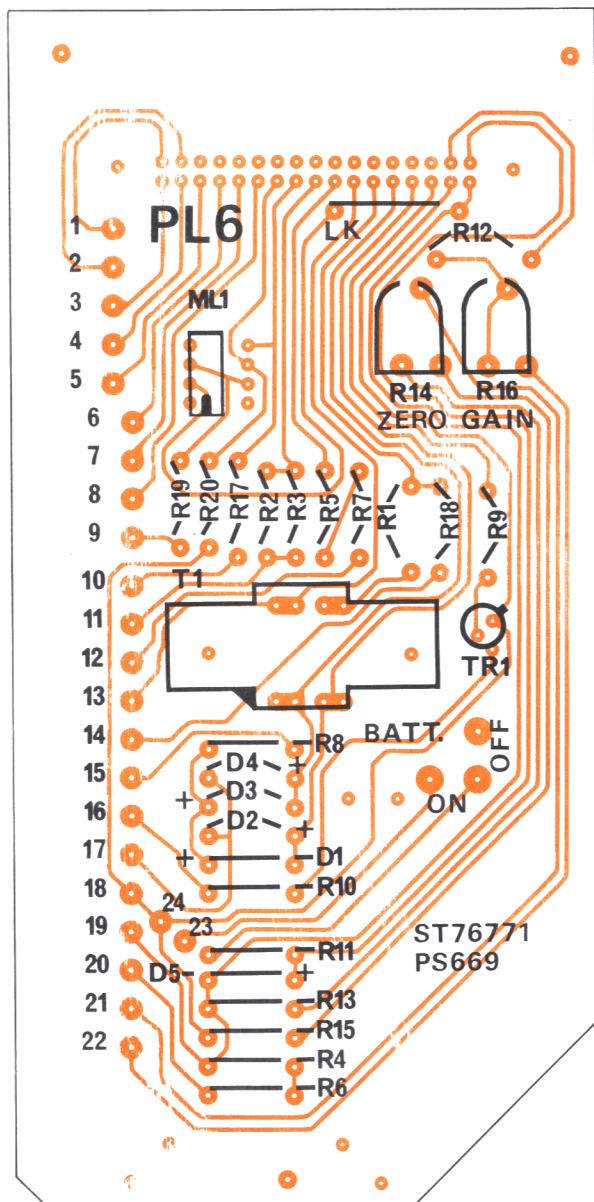
Standby Battery

11. This is a nickel cadmium re-chargeable battery, which supplies approximately +4.5V to various circuits of the interface unit to maintain frequency and other settings in the event of a supply failure. A two-position link LK1 is mounted on the meter board to allow the battery to be disconnected for receiver maintenance purposes.

12. The battery is charged, whilst the receiver is switched on, from the +12V supply via D5 and R11. Since the current drain from the battery during a supply failure is very low, the life of the battery is approximately the same as its shelf life, and it should be replaced at two-yearly intervals.







RACAL

WOH 7014	CA76770/3	4/7-2
1		1/2
WOH 7014	CA76770/3	4/7-2
1		2/2

Layout: Meter Switching/Standby
Battery Board

PART 5

P A R T 5
=====

A F C S Y S T E M
=====

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CHAPTER 1	FUNCTIONAL DESCRIPTION
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CHAPTER 1

FUNCTIONAL DESCRIPTION

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CHAPTER 1

FUNCTIONAL DESCRIPTION

INTRODUCTION

1. The optional AFC facility is used to automatically lock the receiver frequency to that of an incoming carrier. This is achieved by transferring the frequency deviation of the received signal to a 1 MHz signal which is then applied to the synthesizer section of the receiver (34 MHz board) in place of the 1 MHz reference frequency derived from the frequency standard. Since the 34 MHz second mixer injection signal is phase-locked to this 1 MHz signal, the receiver frequency is automatically adjusted by the correct amount.

AFC BOARD PM664

2. A simplified block diagram of the AFC board is given in fig. 1.1. The 1.4 MHz second IF output from the carrier filter (on the IF filter board) is applied direct to an amplifier stage when AFC PILOT is selected, or via an attenuator when AFC FULL is selected (at the MA.1072). The amplified 1.4 MHz carrier is fed via a crystal bandpass filter (passband 100 Hz) to a mixer stage where it is mixed with a 1 MHz signal derived from the frequency standard. The resultant 400 Hz difference frequency output is amplified and is then applied via a buffer stage to the AGC circuits, and to a digital mixer via a shaper stage.

Divide-by-five Stage

3. The 1 MHz reference frequency derived from the frequency standard is also applied to a divide-by-five stage which produces two 200 kHz outputs with a phase difference of 72° ; these outputs are applied to the digital mixer.

Digital Mixer

4. The digital mixer produces two outputs; one is a squarewave at the error frequency whilst the other provides up/down information. These outputs are applied to a 12-bit synchronous binary counter which increments the up/down data at the error rate. The ten most significant bit outputs from the counter are connected to a ten-bit digital-to-analogue converter, and the analogue output is applied via a buffer and a level-shifting stage to the varactor diode of a 7 MHz VCO.

AGC Detector

5. The AGC detector detects and amplifies the 400 kHz output from the buffer stage to produce the gain control voltage for the 1.4 MHz and 400 kHz amplifier stages. The AGC voltage is also applied to a pair of output amplifiers and the resulting AGC 1 and AGC 2 outputs are used to supplement the AGC outputs from the main and ISB (where fitted) IF boards.

Signal-to-Noise Ratio Detector

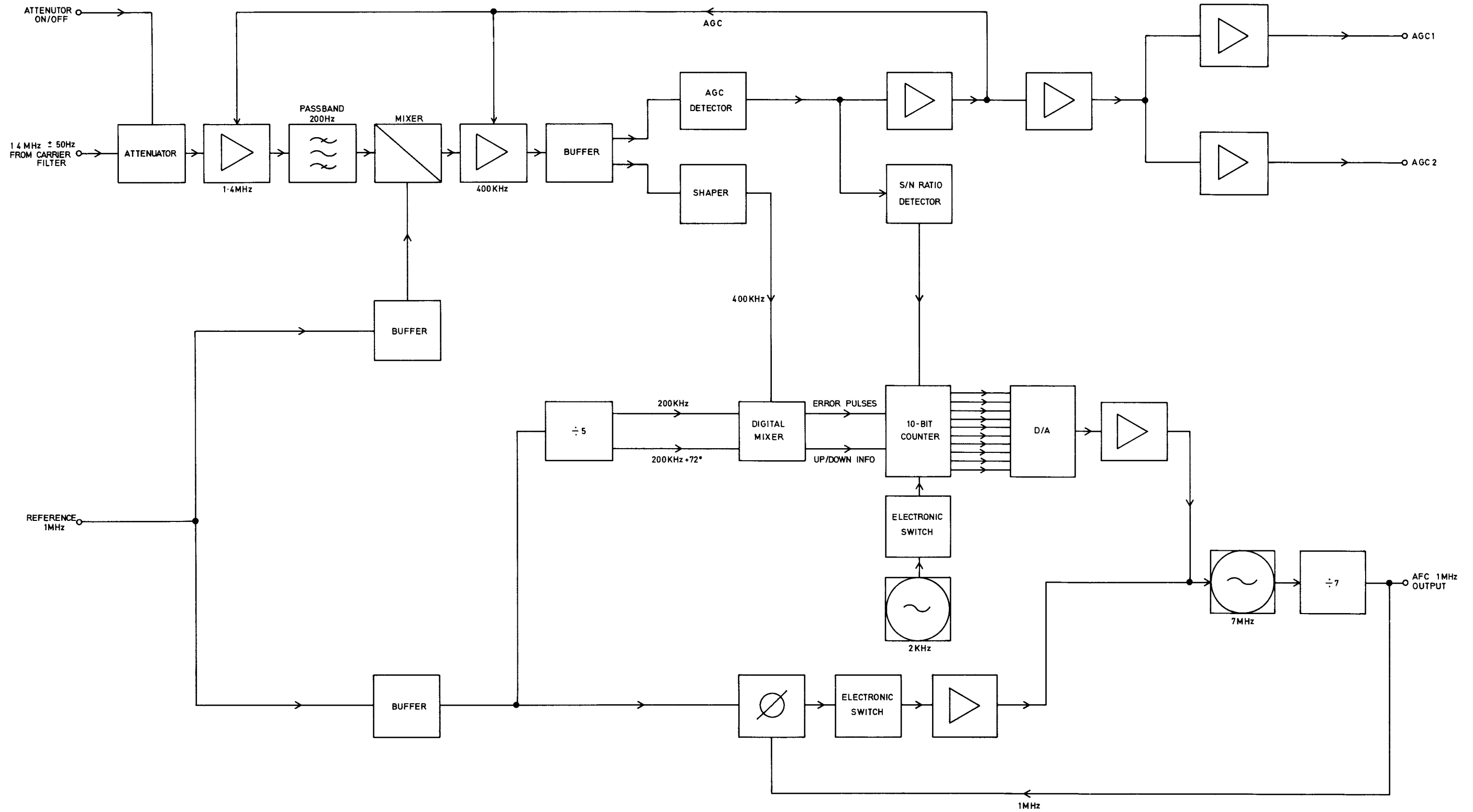
6. The signal-to-noise ratio detector is fed from the AGC detector such that should the carrier level fall below a pre-determined threshold, the counter and D/A converter are inhibited immediately. This holds the frequency of the 7 MHz VCO until the carrier is restored.

Divide-by-Seven Stage

7. The output signal from the 7 MHz VCO is applied to a divide-by-seven stage, and the final output signal, at a frequency of 1 MHz plus or minus the frequency deviation, is applied to the 34 MHz board in place of the reference 1 MHz frequency derived from the frequency standard.

Phase Comparator

8. When AFC is not selected at the MA.1072, the phase comparator compares the 1 MHz signal derived from the frequency standard with the 1 MHz signal derived from the 7 MHz VCO. This ensures that the 1 MHz output signal from the AFC board is in-phase with the 1 MHz output derived from the frequency standard when AFC is selected.



CHAPTER 2

CIRCUIT DESCRIPTION

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CHAPTER 2

CIRCUIT DESCRIPTION

INTRODUCTION

1. For convenience, the circuit diagram of the AFC board is covered by two sheets, fig. 2.3 on sheet 1 and fig. 2.4 on sheet 2. A simplified block diagram of the board is given in fig. 1.1 at the back of Chapter 1.

INPUT ATTENUATOR AND AMPLIFIER

2. The 1.4 MHz carrier signal is applied to an automatic gain controlled IF amplifier stage, ML2, via a switched attenuator which is controlled by the selection of either AFC FULL or AFC PILOT. Transmission gate switching is used in the attenuator. When AFC PILOT is selected at the MA.1072 the signal at C1 is fed via a transmission gate (ML1) to C4 unattenuated. When AFC FULL is selected at the MA.1072 an earth is applied to board pin 14 which changes the state of the transmission gates to route the signal from C2 via attenuator resistor R1 to C4 and IF amplifier ML2.
3. The gain controlled amplifier ML2 has a gain of up to 38 dB and has AGC applied to it via R12. The output at pin 5 of ML2 is fed via a 1.4 MHz crystal bandpass filter (insertion loss approximately 2 dB) to the mixer ML3.

MIXER

4. The 1.4 MHz signal is applied to pin 1 of ML3 via C17 and R25. The 1 MHz reference frequency, at board pin 11, is applied via R9, C8, R13, buffer stage TR1, C21 and R35 to pin 7 of ML3. The resultant 400 kHz output at pin 6 of ML3 is tuned by L4 and C20 to this frequency. Resistors R31, R33, R35 and R36 provide bias for ML3. The variable preset resistor R29 is adjusted to prevent the 1 MHz appearing at the output.

400 kHz GAIN CONTROLLED AMPLIFIER

5. The 400 kHz signal from the mixer ML3 is fed via C22 to ML4; this stage has a gain of up to 38 dB, and the AGC is applied via R44.

OUTPUT BUFFER

6. The output at pin 5 of ML4 is fed via C25 and R47 to a buffer stage TR3, TR4, which has a gain of approximately 23 dB. Two outputs are provided by TR4, the first to the waveform shaper and the second to the AGC detector.

WAVEFORM SHAPER

7. The waveform shaper comprises a long-tail pair TR5, TR6 and functions as a zero-crossing detector. The output from the collector of TR6 is connected to the junction of R70 and R71 of the digital mixer.

AGC DETECTOR

8. The diode detector D1 produces an output which is the sum of the peak voltage of the signal from the output buffer plus 6 volts derived from R42 and R43. The output from the D1 is fed to the AGC amplifier and the signal-to-noise detector.

AGC AMPLIFIER

9. The input to operational amplifier ML5A is filtered by R6 and C5 to produce an amplified AGC from the AGC detector output. The d.c. offset is set by the potentiometer R5. The output appearing at pin 8 of ML5A is applied to gain controlled amplifiers ML2, ML4 and via the time constant circuit to ML5B.

10. The time constant components are R6 and C5, C16 and R22. C5 charges rapidly via R6 to provide an attack time of about 150 milliseconds and R22 provides a slow discharge path for C16 with a decay time of about 1.5 seconds. Transistor TR2 is controlled by ML9A (via R63, RL10C and ML11) such that in the AFC OFF condition, the transistor conducts and discharges C16.

AGC DISTRIBUTION AMPLIFIERS

11. The d.c. level shift stage consists of ML5B, R37 and R41. The preset variable R37 determines the slope of the carrier AGC characteristic and preset potentiometer R41 offsets the output voltage so that it is about 80 mV below the main AGC voltage for the receiver. The carrier AGC is fed to the main AGC for the receiver via voltage follower distribution amplifiers ML5C and ML5D which only take control when the peak signal level falls by 10 dB.

SIGNAL-TO-NOISE RATIO DETECTOR

12. The detector ML10 compares the peak signal voltage from the AGC detector with the preset level set by R45 at the inverting input. The detector has a fast decay and slow attack characteristic, so that AFC is inhibited immediately if the carrier disappears or if extraneous signals pass through the carrier filter, and it is not enabled until about 70 milliseconds after the carrier is restored. R45 is adjusted for AFC present at approximately 2.0 μ V emf antenna signal. The AFC LOCK lamp should definitely be illuminated for a 3 μ V input and extinguished for 1 μ V input.

7 MHz VCO

13. The 7 MHz VCO consists of transistor TR8 connected into a crystal controlled Colpitts circuit with the parallel combination of preset trimmer C35 and varactor diode D4 in series with the crystal, XL2. The VCO is driven to a frequency which is equal to $7 \text{ MHz} \pm \frac{7D}{34}$ where D is the deviation of the received signal. The output signal is coupled by C42 to a shaper stage, TR9 and NAND gate ML6A, and the squarewave output signal is applied to a divide-by-seven stage, ML7.

DIVIDE-BY-7 STAGE

14. ML7 utilises a type of decade counter where the starting point of a count sequence may be preset. A '1' or a '0' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Qa, Qb, Qc, Qd) when the strobe (S) input is at '0'. The counting operation is performed on the negative-going edge of the clock pulse.

15. In this application, the Da data input is connected up to logic '1' (approximately +5V) whilst the remaining data inputs (Db, Dc, Dd) are all taken to logic '0' (0V). The counter therefore starts counting at binary 1 and resets at binary 8, i.e. at binary 8 the logic '1' Qd output, inverted by ML6, resets or strobes the counter, binary 1 is again loaded in and the count sequence repeats.

16. The shaped output signal from the 7 MHz VCO is divided by seven and the resulting $1 \text{ MHz} \pm \frac{D}{34}$ output is taken from ML7 pin 2. This output is applied via a shaper stage TR10 to the phase comparator and via board pin 10 to the 34 MHz board where it is used in place of the 1 MHz reference frequency, derived from the frequency standard.

PHASE COMPARATOR

17. The digital phase comparator consists of a dual D-type flip-flop ML20A and ML20B, four NAND gates ML19 and a varactor line driver ML16A. It compares the $1 \text{ MHz} \pm D/34$ from ML7 with the 1MHz reference frequency from TR7; any error between these two frequencies is used to change the level of a d.c. voltage which is applied to the 7 MHz VCO.

18. The output signal from ML7 is applied via TR10 to the clock input of ML20B, and the 1 MHz reference signal is applied to the clock input of ML20A. The D inputs of ML20 are held at logic '1'. The positive edge of the clock input to ML20B changes the \overline{Q} output at pin 13 to '1' and the \overline{Q} output changes to '0'. When both Q outputs are at '1' the outputs from the NAND gates (ML19) reset the Q outputs to '0' and the \overline{Q} outputs to '1'. The \overline{Q} output of ML20A is inverted by a NAND gate and applied via R90 and D5 to ML16A. The \overline{Q} output of ML20B is applied via R91 and D6 to ML16A.

19. Consider the case where the output frequency from ML7 is high, which means that this positive edge will occur first. The resulting setting and resetting of the flip-

flops causes the varactor line driver ML16A to decrease the voltage applied to the varactor diode of the 7MHz VCO thus reducing the frequency. Conversely if the output frequency from ML7 is low, the ML16A output will increase to increase the 7MHz VCO frequency.

20. When the two signals are equal in frequency and phase, the varactor line voltage remains constant.

DIVIDE-BY-5 STAGE

21. The 1MHz reference frequency signal (from the 1MHz buffer, sheet 1) is applied to ML18 which is a divide-by-10 ring counter with reset. A divide-by-5 ring counter is produced by connecting the Q5 output to the reset input. The 200kHz outputs at Q1 and Q2, which have a phase difference of 72° , are taken to the clock inputs of the digital mixer, ML17.

DIGITAL MIXER

22. The digital mixer consists of a dual D-type flip-flop ML17, EX OR gates ML12A, ML12B and a D-type flip-flop ML13A. ML17A and ML17B compare the 400kHz carrier signal (from the waveform shaper, sheet 1) with the 200kHz clock inputs from ML18, spaced at a constant phase difference of 72° . In timing diagrams fig. 2.1 and fig. 2.2 exaggerated examples are given where the input frequencies of 500kHz and 300kHz are shown respectively. The actual range is plus or minus 50Hz, but at this rate several hundred clock pulses would have to be given to show the generation of error pulses. In these timing diagrams, the Q outputs from ML17A and ML17B change state at the error frequency rate and are also 72° out of phase with each other. The Q outputs of ML17a and ML17b are filtered by R78, C44 and R79, C45 to remove spurious noise pulses. ML12A and ML12B ensure that square-edged pulses are applied to ML13A. Resistors R70, R71, R74 and R75 provide hysteresis around ML17A and ML17B. The Q output from ML13A is fed via EX OR gate ML12D to the binary counter as up/down information.

23. In timing diagram fig. 2.1, where the carrier frequency is higher than 400kHz, i.e. 500kHz, the D-input to ML13A is high when the clock input goes high, and the Q output from ML13A is high. In fig. 2.2, where the carrier frequency is lower than 400kHz, i.e. 300kHz the D input to ML13A is low when the clock input goes high, and the Q output from ML13A is low.

2kHz OSCILLATOR

24. The oscillator consists of two inverting NOR gates ML14 biased into the linear region with C46 providing positive feedback. The oscillator is disabled by a '1' at pin 12 of ML14, when AFC FULL or AFC PILOT is selected. When AFC is not selected the oscillator provides clock inputs to the binary counter.

BINARY COUNTER

25. The counter comprises ML22, ML23 and ML24 connected as a 12-bit synchronous up/down counter. The up/down information is derived via EX OR gate ML12D from ML13A when AFC FULL or AFC PILOT is selected and from ML10D when AFC is not selected.

26. The clock input is derived via EX OR gate ML12C, NAND gates ML11C and ML11D from ML12B when either AFC FULL or AFC PILOT is selected and from the 2 kHz oscillator when AFC is not selected.
27. The monostable ML15A produces 700 millisecond pulses at the error rate provided by the output from ML11D. The \overline{Q} output from ML15A is slightly delayed by R88 and C53 before it is applied to the clock enable input of ML22, so that the counter is not clocked at the same time as the data changes at the up/down inputs. The counter chain is only allowed to count if another error pulse arrives whilst the monostable is still triggered by the previous pulse. If the monostable has time to relax between error pulses, no count will take place. Thus, if the error pulses are greater than 700 milliseconds apart, i.e. the error frequency is less than 1.4 Hz, the counters are not incremented and this prevents hunting.
28. When the up/down input is at logic '1' the counter counts up and when the up/down input is at logic '0' the counter counts down. The ten most significant counter outputs are connected to the logic inputs of the digital to analogue converter.

DIGITAL-TO-ANALOGUE CONVERTER

29. The digital to analogue converter ML21 is provided with ten inputs from the up/down counter, a reference voltage input and a feedback input to produce an output current at pin 1. This output is applied to operational amplifier ML16B which provides the feedback to an internal feedback resistor in ML21 and also the input to operational amplifiers ML16C and ML16D. The output from ML16C is fed back to pin 15 of ML21 as the reference voltage and the output from ML16D is applied to ML10D.
30. The ML21 output current I_o is proportional to the following two quantities:
- (1) The multiplying fraction k which is dependent on the state of the inputs from the up/down counter.
 - (2) The reference voltage applied to pin 15 of ML21.
31. The result is that the I_o/k characteristic is made non-linear and the feedback proportion is used to compensate for the non-linear frequency/voltage curve of the 7 MHz VCO and achieve superior frequency accuracy.
32. When AFC is not selected, ML10D compares the output from ML16D with the varactor line voltage to provide up/down information for the binary counters.

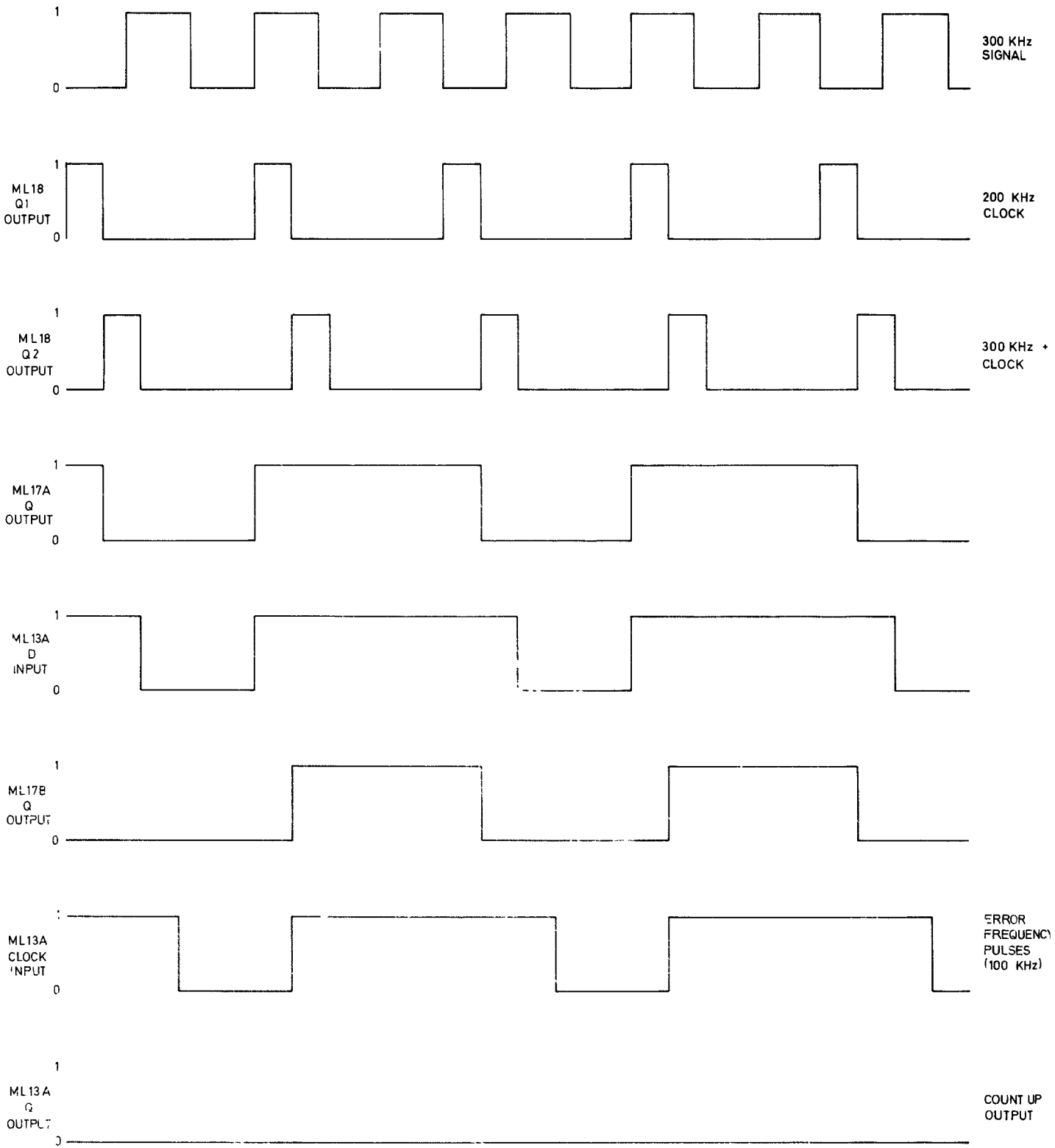
AFC LOCK INDICATOR

33. The lamp driver circuit consists of NOR gate ML14D, flip-flop ML13B, NAND gates ML9, transmission gate ML8A and transistor TR11. When either AFC FULL or AFC PILOT is selected, and provided that the error frequency is less than 1.4 Hz and the signal-

to-noise ratio is satisfactory, a '0' on pin 9 of ML9 is inverted by the transmission gate ML8A to permit transistor TR11 to conduct and illuminate the AFC LOCK indicator on the MA.1072 front panel (via the serial data).

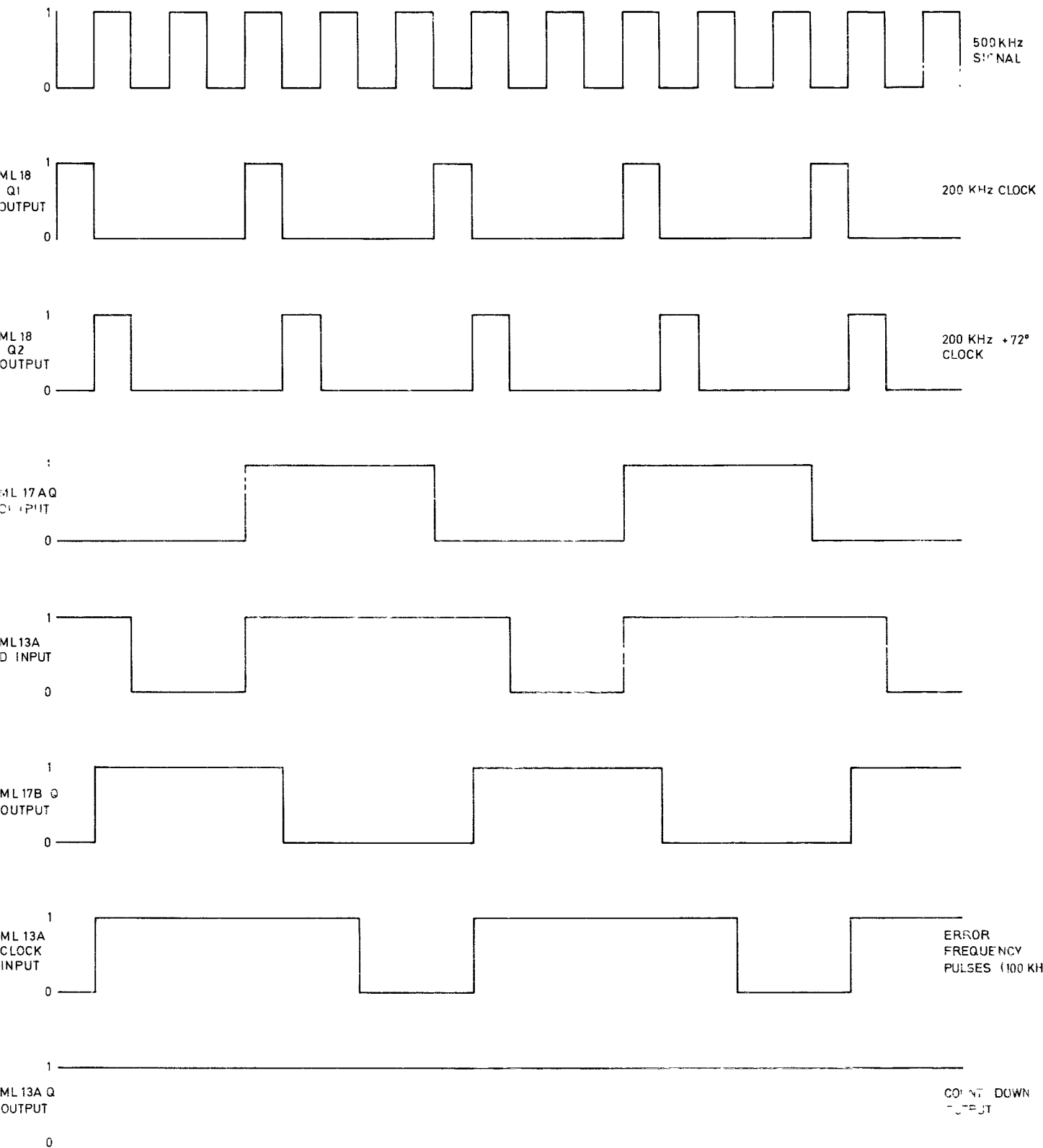
AFC ON/OFF SWITCHING

34. When either AFC FULL or AFC PILOT is selected, an earth (logic '0') is applied to board pin 13 and is routed to a switch anti-bounce circuit consisting of R63, C37 and ML10C.
35. The action of the anti-bounce circuit is as follows. Prior to the selection of AFC, the input at pin 5 of ML10C is at logic '1' (pin 5 is connected to the +12V rail via R64, and board pin 13 is open circuit) and the output at pin 2 is at logic '1'; this is applied to ML13A, ML17B, ML19, ML8D and TR12. When either AFC FULL or AFC PILOT is selected, the logic '0' applied to pin 5 of ML10C provides a logic '0' output. This is applied to NAND gate ML11A to produce a logic '1'. This latter output is applied to ML14B, ML11B, ML20B, ML9A, ML9B, ML8C and TR13.
36. When the AFC is switched off, the carrier derived AGC is removed from the IF board(s). ML17B is reset so that pin 6 of ML12C is at logic '0' and the clock pulses for the up/down counter are taken from the 2 kHz oscillator ML14A, ML14B and, with a logic '0' on pin 12, the oscillator will operate.
37. A logic '1' at pin 10 of ML13A resets ML13A so that pin 2 of ML12D is at logic '0'. Transistor TR13 is switched off to produce a logic '1' which allows the ML10D up/down information to be applied to pin 1 of ML12D. A logic '1' at pin 13 of ML19 allows reset pulses to arrive at ML20A whilst a logic '0' at ML20B pin 8 enables it, thus activating the phase comparator.
38. Transistor TR12 is switched on so that the varactor line is supplied only from the phase comparator and loop filter, whilst transmission gates ML8C and ML8D switch the tuning indicator pulses to the meter.
39. When either AFC FULL or AFC PILOT is selected the carrier derived AGC is allowed to pass to the IF board(s).
40. A logic '0' at pin 4 of ML17B enables it and allows the digital mixer to operate as described in paras. 22 and 23. The 2kHz oscillator ML14 is disabled by a logic '1' at pin 12.
41. Transistor TR12 is switched off by a logic '0', and a logic '1' on ML20B sets ML20B and resets ML20A to allow only the digital-to-analogue converter to supply the varactor line.
42. Transistor TR13 is switched on to apply a logic '0' to pin 1 of ML10D and to pin 1 of ML12D; this allows the up/down information to be taken from ML13A, whilst transmission gates ML8C and ML8D switch the varactor voltage to the meter.



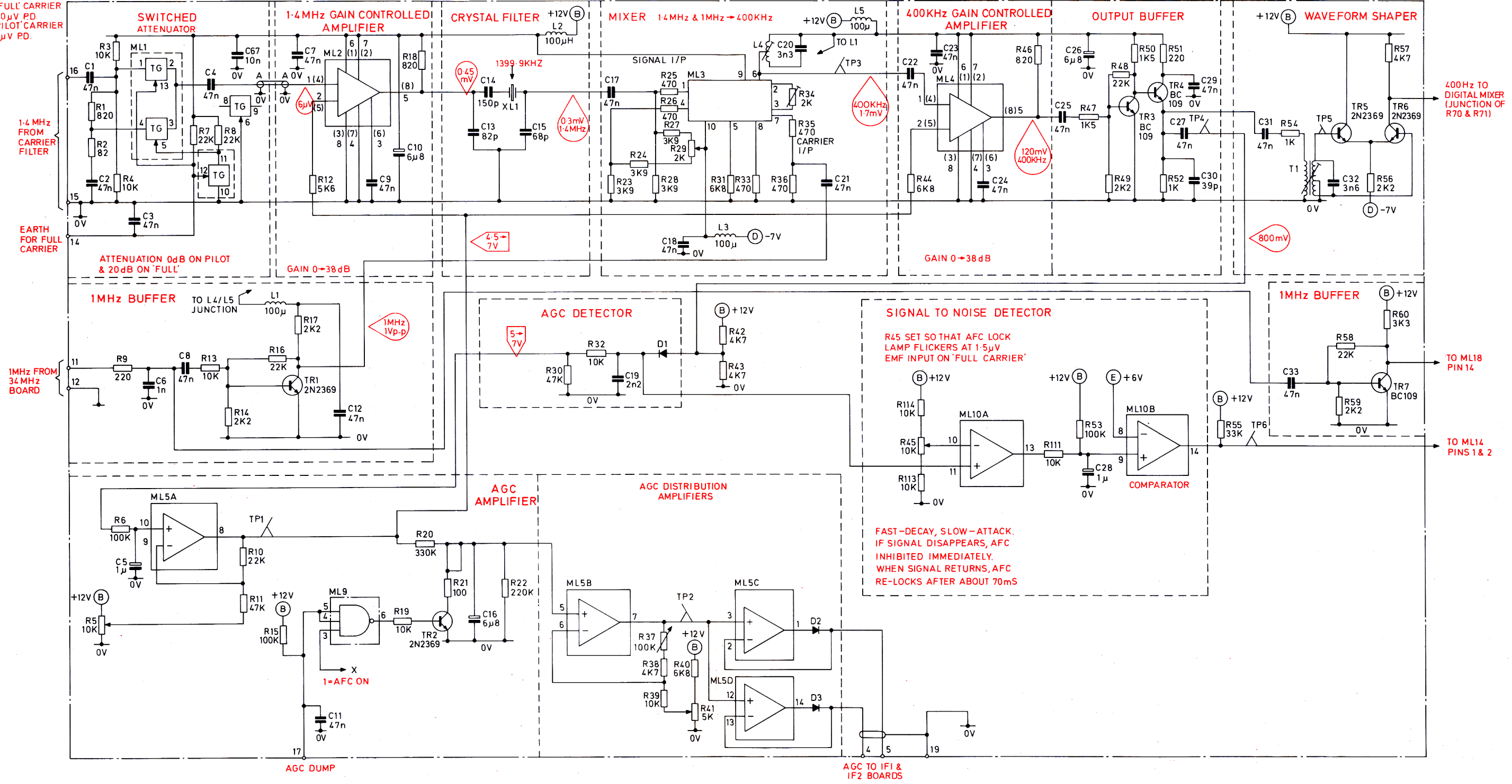
Timing Diagram:
Digital Mixer Frequency Low

Part 5
Fig. 2-1



Timing Diagram:
Digital Mixer Frequency High

FOR 1μV EMF INTO
Rx. ANT. SIGNAL
LEVEL ON PIN 16
'FULL' CARRIER
50μV PD.
'PILOT' CARRIER
6μV PD.



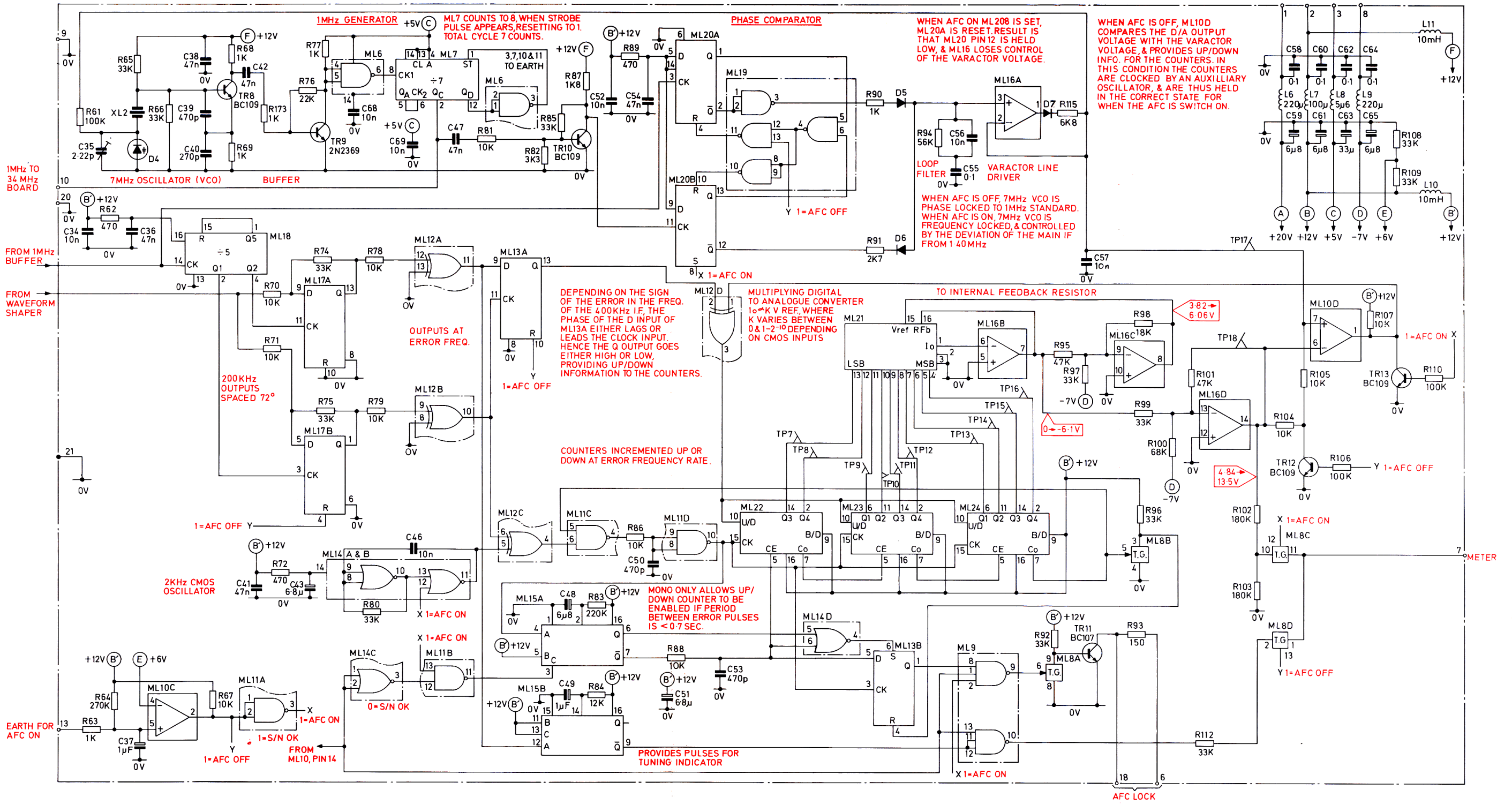
NOTE - ML2 & ML4

PIN NUMBERS IN BRACKETS APPLY WHEN D.I.L. ALTERNATIVES ARE USED (I.E. MC 1350)

FIGURES SHOWN IN WERE MEASURED WITH AN AIRMEC 301A VALVE VOLTMETER (USING THE HIGH IMPEDANCE PROBE)

FIGURES SHOWN IN WERE MEASURED WITH AN AVO 8 (D.C. LEVEL)

RACAL	WOH6247 DC77080 SHT.1	5/2-3
		1/2
	WOH6247 DC77080 SHT.1	5/2-3
		2/2



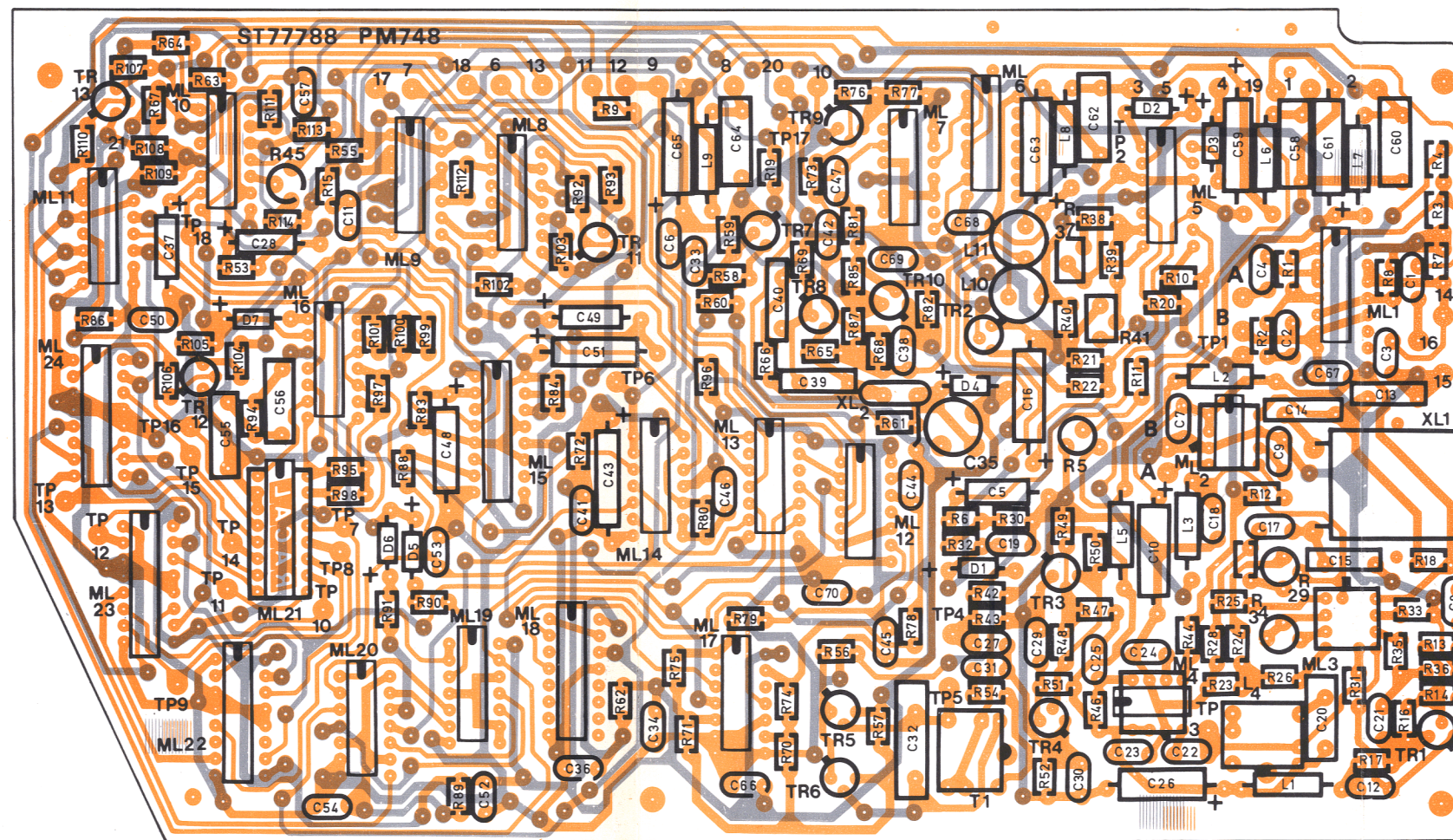
PACKAGE	CD4086	MC1596G OR MC1596P	MC1596G OR MC1596P	MC1596G OR MC1596P	LM332	7400J	74LS196J	CD4086	CD4023	LM239	CD4011	CD4070	CD4013	CD4001	MC1528	LM324	CD4013	CD4017	CD4011	CD4013	AD7520	CD4029	CD4029	CD4029
	ML1	ML2	ML3	ML4	ML5	ML6	ML7	ML8	ML9	ML10	ML11	ML12	ML13	ML14	ML15	ML16	ML17	ML18	ML19	ML20	ML21	ML22	ML23	ML24
+20V	-	-	-	-	-	-	-	-	-	3	-	-	-	-	4	-	-	-	-	-	-	-	-	-
+12V	14	6,7 (1,2)	6	6,7 (1,2)	4	-	-	14	14	-	14	14	14	14	5,11 (13,16)	-	14	16	14	5,9,14	14	9,16	9,16	9,16
+5V	-	-	-	-	-	14	4, 13,14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0V	6,7, 10	4,8 (3,7)	8	4,8 (3,7)	11	7	3,7, 10,11	4,7, 8	7	12	7	8,13, 7	7	7	8,15, 1	5,10, 12	6,8, 10,7	8,13	7	7,6	2,3	3,4,8, 12,1,13	3,4,8, 12,1,13	3,4,8, 12,1,13
-7V	-	-	10	-	-	-	-	-	-	-	-	-	-	-	11	-	-	-	-	-	-	-	-	-
DE- COUPLED BY	C67	C7	-	C23	-	C68	C69	-	-	-	-	C70	-	R72, C41, C43	C51	-	C66	R62, C34, C36	-	R89, C52, C54	-	-	-	-

NOTE :- ML2 & ML4
PIN NUMBERS IN BRACKETS APPLY WHEN D.I.L. ALTERNATIVES ARE USED (I.E. MC1550 P)

RACAL	WOH6247	DC77080	SHT 2	5/2-4
	2	5		1/2
	WOH6247	DC77080	SHT. 2	5/2-4
	2	5		2/2

Circuit: AFC Board PM664 (Sheet 2)

Part 5 Fig. 2-4



RACAL

WOH6247	DA77788	SHT. 4	5/2-5
11			1/3
WOH6247	DA77788	SHT. 2	5/2-5
11			2/3
WOH6247	DA77788	SHT. 3	5/2-5
11			3/3

PART 6

PART 6

POWER SUPPLIES

CONTENTS

CHAPTER 1	GENERAL DESCRIPTION
CHAPTER 2	POWER REGULATOR BOARD PS665

CHAPTER 1

GENERAL DESCRIPTION

CONTENTS

	<u>Para.</u>
INTRODUCTION	1
BRIEF DESCRIPTION	3

ILLUSTRATIONS

	<u>Fig. No.</u>
Distribution Board	1.1

CHAPTER 1

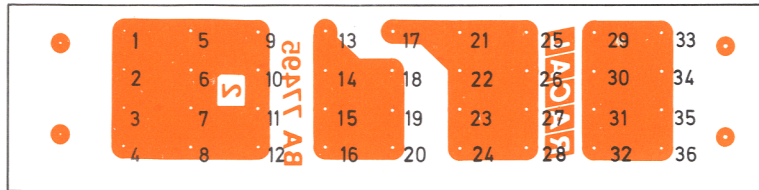
GENERAL DESCRIPTION

INTRODUCTION

1. The power supply section of the receiver provides regulated outputs at -7V, +5V, +12V and +20V. These supplies are distributed to the various circuits of the receiver via a distribution board which is mounted centrally at the front edge of the cast chassis (behind the interface unit). The connections to this board (fig. 1.1) are coloured violet for -7V, brown for +5V, orange for +12V and red for +20V; this colour coding is maintained throughout the receiver for the supply connections.
2. The regulated supply voltages are routed to the interface unit and may be monitored on the front panel meter. The MS614 interface unit contains a rechargeable battery (connected via a diode to the +12V supply rail) which maintains power to various interface unit circuits in the event of a supply failure. The standby battery circuit is fully described in Part 4 of this manual (RA. 1784 only).

BRIEF DESCRIPTION

3. The power supply section comprises the POWER input socket and associated fuse on the rear panel, a supply input filter which is mounted on the mains transformer, a voltage selector unit, the power regulator board, two bridge rectifiers, and three series-pass power transistors mounted on a heatsink attached to the rear panel. The main supply smoothing capacitors are mounted on the chassis between the mains transformer and the frequency standard board. Dismantling and re-assembly instructions for the power supply components are given in Part 1, Chap.2, whilst details of the chassis mounted components are given in Part 1, Chap.6.
4. The STD/+12V terminal and associated STANDBY fuse on the rear panel are provided for the connection of an externally generated +12V supply to maintain the operation of the 5 MHz frequency standard in the standby condition; i.e. when the receiver is switched off or during a supply failure.
5. The circuit description of the power supply section is given in Chap.2 in conjunction with the circuit diagram, fig. 2.2.



-7V SUPPLY (VIOLET)

PIN	TO/FROM
29	TO INTERFACE UNIT VIA PL9/29
30	TO UPPER & LOWER LOOP BOARDS
31	TO TRANSFER & HF LOOP BOARDS
32	TO MAIN IF BOARD
33	TO ISB IF BOARD
34	TO SECOND MIXER BOARD VIA 1C53 & 1C54
35	TO AFC BOARD
36	FROM REGULATOR BOARD PIN 10

+5V SUPPLY (BROWN)

PIN	TO/FROM
17	TO INTERFACE UNIT VIA PL9/27
21	TO DECODER BOARD
22	TO UPPER & LOWER LOOP BOARDS
23	TRANSFER & HF LOOP BOARDS
25	TO 34MHz BOARD
26	TO HALF-OCTAVE BOARD
27	TO AFC BOARD
28	FROM REGULATOR BOARD PIN 2

+12V SUPPLY (ORANGE)

PIN	TO/FROM
1	TO INTERFACE UNIT VIA PL9/21
2	TO DECODER BOARD
3	TO TRANSFER & HF LOOP BOARDS
4	TO MAIN IF BOARD
5	TO ISB IF BOARD
6	TO IF FILTER BOARD
7	TO 34MHz BOARD
8	TO RF BOARD VIA 1C49
9	TO AFC BOARD
10	TO SECOND MIXER BOARD VIA 1C44 & 1C45
11	FROM REGULATOR BOARD PIN 17

+20V SUPPLY (RED)

PIN	TO/FROM
13	TO INTERFACE UNIT VIA PL9/26
14	TO UPPER & LOWER LOOP BOARDS
15	TO TRANSFER & HF LOOP BOARDS
16	TO RF BOARD VIA 1C40
18	TO AFC BOARD
19	FROM REGULATOR BOARD PIN 22

NOTES : 1 -7V SUPPLY (VIA 1C55) AND +12V SUPPLY (VIA 1C48)
TO FIRST MIXER BOARD TAKEN DIRECT VIA SCREENED
WIRES FROM REGULATOR BOARD PINS 10 & 17
RESPECTIVELY.

2. THE AF BOARD CONTAINS A 3 TERMINAL VOLTAGE
REGULATOR CIRCUIT FED FROM 1D4

RACAL

WOH6247	BA77495/3	1:1
2		1/2

Layout : Distribution Board

Part 6
Fig.1.1

CHAPTER 2

=====

POWER REGULATOR BOARD PS665

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CONTENTS

	<u>Para.</u>
INTRODUCTION	1
-7V REGULATOR	3
+5V REGULATOR	4
+12V REGULATOR	5
+20V REGULATOR	7

ILLUSTRATIONS

	<u>Fig.No.</u>
Equivalent Circuit: Voltage Regulator IC	2.1
Circuit Diagram: Power Supplies	2.2
Layout: Power Regulator Board PS665	2.3

CHAPTER 2

POWER REGULATOR BOARD PS665

INTRODUCTION

1. The power regulator board (fig. 2.2) utilises four identical regulator integrated circuits, one for each supply. These devices consist of a temperature-compensated reference amplifier, an error amplifier, a series-pass transistor and a current limit stage. An equivalent circuit of the device is given in fig. 2.1.
2. The error amplifier is used to compare the reference voltage (maximum approximately +7V) with a sample of the final stabilized output voltage (via a potential divider if greater than the reference voltage); the output from the amplifier is then used to control the series-pass transistor. This transistor is also controlled by a current limiting stage which itself is controlled by the current drawn from the supply by the external circuitry.

-7V REGULATOR

3. A 10.5V secondary winding of 1T1 is connected to a full-wave bridge rectifier, D1, via board pins 11 and 15, and a 5A fusible link LK1. The positive output from D1 is applied to the collector of the external series-pass transistor 1TR1 via board pin 13, whereas the emitter of 1TR1 is returned to the negative output of D1 via board pin 6, R23 and R14. The positive supply voltage for ML1 (V+), and also the collector voltage (VC) for the internal series-pass transistor, is taken from the regulated +12V supply. The output from the reference amplifier (V REF) is applied via R1 to the non-inverting input of the error amplifier, whilst a sample of the -7V output is applied to the inverting input via a potential divider R13, R9 and preset voltage adjust potentiometer R8. Current foldback is provided by R14, R23, 1R1 and 1R2.

+5V REGULATOR

4. Bridge rectifier 1D3 is fed from a 10V secondary winding of transformer 1T1 via board pin 8, fusible 5A link LK2 and board pin 7. The positive output voltage from 1D3, smoothed by 1C23, is applied to the collector of the series-pass transistor 1TR2. The positive supply voltage for ML2 (V+), and also the collector voltage of the internal series-pass transistor, is taken from the regulated +20V supply. The reference voltage level applied to the non-inverting input of the error amplifier is preset by R3, and a sample of the +5V output is applied to the inverting input via R15. Current foldback is provided by R16, R24, 1R3 and 1R4.

+12V REGULATOR

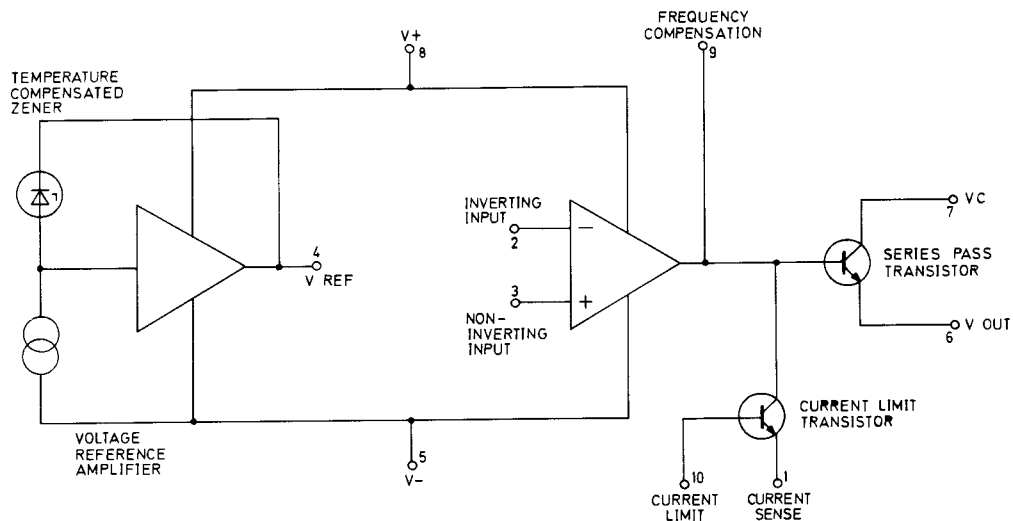
5. This supply is derived from a 16.5V output from 1T1 which is applied to bridge rectifier 1D4 and a 5A fusible link LK3. The positive output from 1D4 is applied to the collector of the series-pass transistor 1TR3 (and also to a three-terminal voltage regulator

on the AF board). The positive supply voltage ($V+$), and also the collector voltage for the internal series-pass transistor, is taken from the regulated +20V supply. The reference voltage is applied via R6 to the non-inverting input of the error amplifier whilst a sample of the +12V output is applied to the inverting input via a potential divider R25, preset voltage adjust potentiometer R17, and R10. The regulated +12V output is taken to board pin 17 (via 1R5) and is applied to the oven of the frequency standard via R29, D3 and board pin 5.

6. An externally applied +12V standby supply for the oven, protected by 1FS2 and zener diode 1D8, is taken to board pin 3. When the receiver is operational, diodes D4 and D6 are reverse biased by the regulated +12V supply and thus isolate the standby supply; when the receiver is switched off, or should a supply failure occur, the bias is removed and the +12V standby supply is routed to the oven via D6, D3 and board pin 5.

+20V REGULATOR

7. This stage, which is similar to the +12V regulator, is fed from a 23V secondary winding of 1T1 connected to bridge rectifier D2 via a 5A fusible link LK4. The regulated output is preset by R20; current foldback is provided by R27, R22 and R12.

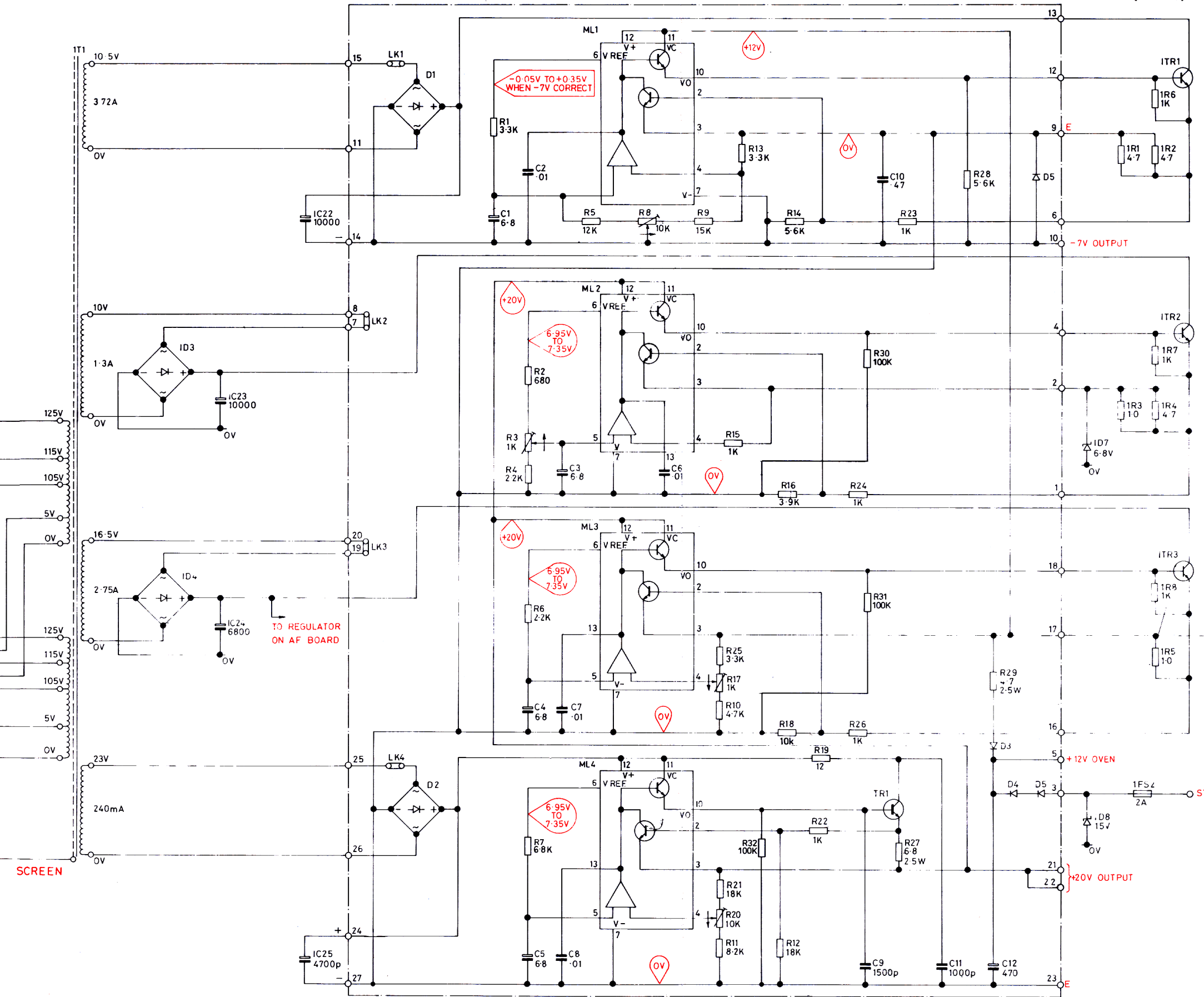
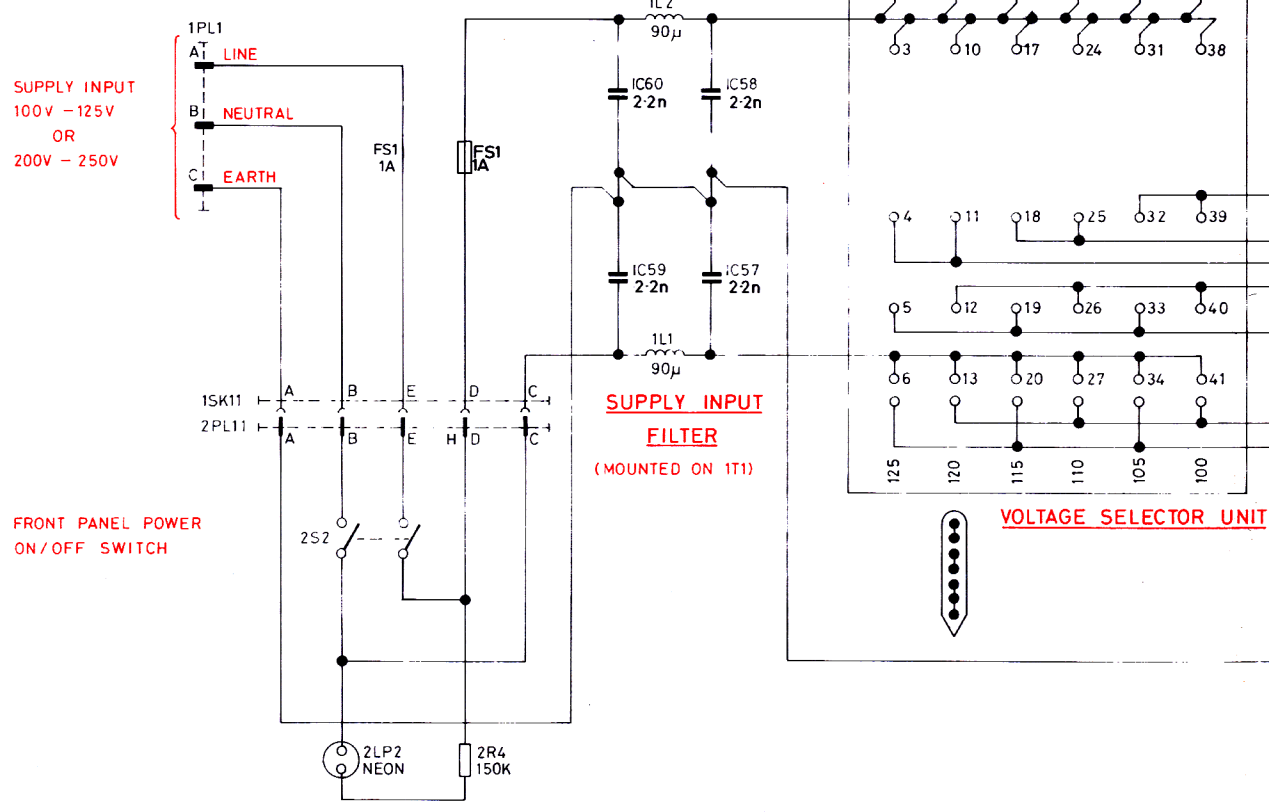


RACAL

Equivalent Circuit : Voltage Regulator IC

Part 6
Fig. 2.1

- TRANSISTORS**
RCA40412 — TR1
- DIODES**
10DB05A — D1
SBMB2 — D2
10D1 — D3, 4 & 6
- INTEGRATED CIRCUITS**
723DM — ML1, 2, 3 & 4
- LINKS**
40 SWG. BTC — LK1, 2, 3 & 4
SA FUSE
WIRE

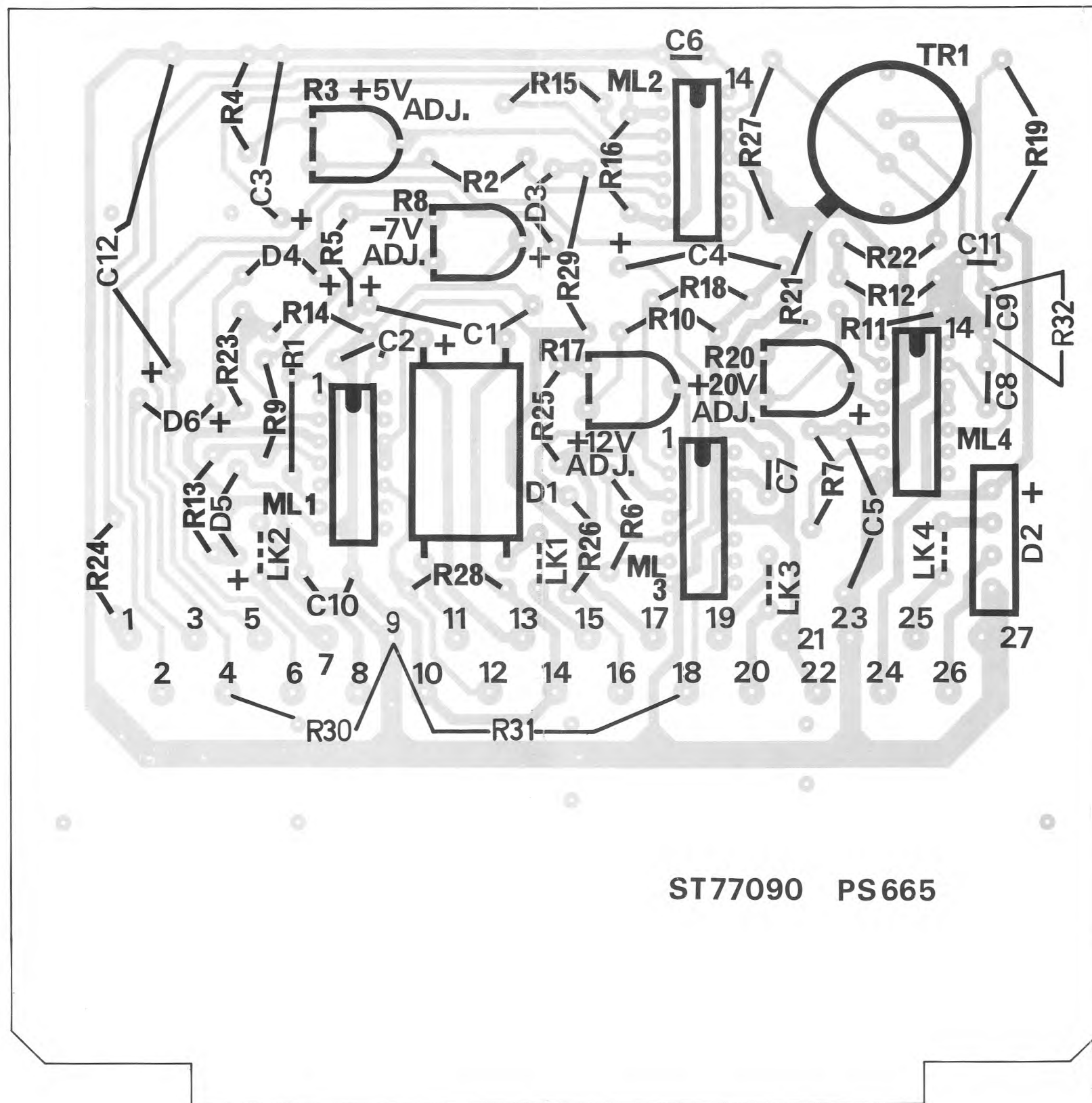


(COMPONENTS PREFIXED 1
CHASSIS MOUNTED REF ONLY
COMPONENTS PREFIXED 2
FORM PART OF INTERFACE
UNIT)

RACAL		
WOH 6247	DC 77090	6/2.2
1/2	1	2/2

Circuit: Power Supplies

Part 6
Fig.2.2



ST77090 PS665

RACAL		
WOH 6247	DA 77089/3	2-3
1		1/2
WOH 6247	DA 77089/3	2-3
1		1/2