TELEGRAPH AND DATA MESSAGE GENERATOR 5805-99-634-6057 (TREND COMMUNICATIONS TDMG 1B)

GENERAL AND TECHNICAL INFORMATION

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(TREND COMMUNICATIONS TDMG 1B)

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1. GENERAL DESCRIPTION

1.1 The Telegraph and Data Message Generator (T.D.M.G.) is a portable, mains operated equipment for testing telegraph and data transmission equipment and, when used in conjunction with the Telegraph and Data Signal Analyser (T.D.S.A.), for testing telegraph and data transmission links.

1.2 The equipment generates standard patterns and start stop messages over a wide bit speed (or baud) range and upon which can be imposed various types of telegraph distortion - refer to Fig. 1A. These patterns are available:-

i) Serially - at a nominal C.C.I.T.T. V24 level (± 6V).

ii) Fully isolated variable high level (10-110V single or double current).

iii) Electronic relay output (short circuit and open circuit with respect to Telegraph Earth).

1.3 The start stop patterns can also be obtained as a "parallel" output at logic level(0V and +5V) together with an associated "Character Present" pulse, via the 25-way socket at the rear of the equipment. The V24 output is also available at this socket together with other control signals.

OPERATOR'S INSTRUCTIONS

2. INSTALLATION

2.1. Ascertain the voltage level of the local mains supply.

2.2. Ensure that the mains voltage selector tap situated on the equipment rear panel is set to the appropriate position.

2.3. Connect the equipment to the mains supply - Switch 'ON'.

3. OPERATING INSTRUCTIONS

3.1. Test Messages

The required test message is selected by rotating the 12 position Test Message switch SW3.

3.1.1. Position 1 - Mark -

In this position the generated output is at a steady level which can be made to correspond to either Mark or Space dependant on the position of the 'Signal Polarity' switch.

3.1.2. Position 2 - (1:1-), 3, (2:2), 4, (1:6) and 7 (Q9S)

These sequences are defined by C.C.I.T.T. Recommendation R51 for telegraph communication circuit testing. The Q9S signal is an 8 character sequence and is made up as follows:-

LTRS, S, CR, LF, Q, FIGS, SPACE, 9, in International Telegraph Alphabet No. 2 Code (5 unit).

3.1.3. Position 5 - 511 PR -

In this position the 511-bit pseudo-random sequence recommended in C.C.I.T.T. V52 for isochronous distortion and error measurement.

3.1.4. Position 6 - RY -

With SW3 in this position a 54-character sequence of alternative 'R' and 'Y' characters conforming to International Telegraph Alphabet No. 2 Code.
'LF, CR, LF, CR' is automatically inserted before each sequence. When any distortion is imposed upon the generated signal the first 'LF, CR' remains undistorted to avoid overprinting if the output device fails to respond correctly to the degraded input signal.

3.1.5. Position 8 - REP CHAR -

SW3 in Position 8 enables a character, containing between 5 and 8 information elements to be set to any combination and generated repetitively.

3.1.5. (Contd/)

The number of information elements per character is selected by the 'Elements Per Character' switch and the appropriate number of element condition switches are set to give the required character code combination. This position also enables 1:3 and 1:7 continuous patterns to be generated, these being the other signals recommended in C.C.I.T.T. V52 for data transmission measurements.

3.1.6. Position 9 - PROG SEQUENCE -

Position 9 allows programming of up to 8 characters, of any combination and length between 5 and 8 information elements. Each character is represented by a column of holes, these being numbered 1 to 8 downwards. Pins inserted in these holes set the condition of the respective elements to Mark (or Binary 1). The number of information elements per character and length of sequence can be set by insertion of pins in the appropriate position in columns labelled CL and ML respectively. The bottom two rows of holes provide storage for 20 Programming pins. The use of the programme character facility can be extended, when, by arrangement of a control described later, the sequence can be set to precede either of the "Fox" test messages, whilst a further programmed sequence, as selected by another matrix mounted at the rear of the instrument, is used to follow the "Fox" message. This is particularly useful for preceding the message with an 'address' code and following it with an 'end of text' code. It can also be used for extending the number of characters printed in a line.

3.1.7. Position 10 produces the 'Fox' test messages in International Telegraph Alphabet No. 2 Code (5 unit) as recommended in C.C.I.T.T. R52 for the distortion margin measurement of start-stop apparatus. The complete sequence generated is as follows:

LF, CR, LF, CR, LTRS, THE SP QUICK SP BROWN SP FOX SP JUMPS SP OVER SP THE SP LAZY SP DOG SP FIGS 1 2 3 4 5 6 7 8 9 0

Of the 60 characters generated per complete test message, 54 including 'space' appear on a printed output. The first 'LF, CR,' is undistorted as described in 3.1.4.

3.1.8. Position 11 produces the 'Fox' test message in International Telegraph Alphabet No. 5 Code (7 unit plus 1 parity bit). The complete sequence includes both lower and upper case 'Fox' messages together with numerals and is as follows:

LF, CR, LF, CR, the SP quick SP brown SP fox SP jumps SP over SP the SP lazy SP dog SP 1 2 3 4 5 6 7 8 9 0 LF, CR, LF, CR,
THE SP QUICK SP BROWN SP FOX SP JUMPS SP OVER SP THE SP LAZY SP DOG SP 1 2 3 4 5 6 7 8 9 0

3.1.8. (Contd/)

Of the 116 characters generated per complete test message, 108 including 'space' appear on a printed output. The first 'LF CR' preceding upper and lower case lines is undistorted as described in 3.1.4.

By setting a control mounted on the rear of the equipment, to the appropriate position, characters of odd or even parity can be generated.

3.1.9. For the extreme clockwise position of the 'Test Message' switch a 54-character sequence of alternate 'U' and '*' characters to International Telegraph Alphabet No. 5 Code, is produced. This is the 7 unit code equivalent to the 5 unit code RY test. 'LF, CR, LF, CR,' is automatically inserted before each sequence with the first 'LF, CR,' undistorted as in 3.1.4.

4. START AND STOP PULSE

4.1. For test messages comprising a sequence of characters, as generated in positions 6 to 12 of the 'Test Message' switch a start pulse of one element is automatically inserted for each character. The start pulse can be omitted by the setting of a control on the rear of the instrument.

4.2. A stop pulse of 1, $1\frac{1}{2}$, or 2 elements in length can be selected by the 'Stop Pulse Length' switch for any of the character generating test messages. A position which completely eliminates the stop pulse is provided primarily to give greater flexibility in the pattern which can be selected using the element condition switches described in 3.1.5.

5. SIGNAL POLARITY

5.1. The output signal polarity can be inverted by setting the 'Signal Polarity' switch from either of its two left-hand positions to either of the two right-hand positions. In the character generating positions of the 'Test Message' switch, the start pulse polarity can be set by selecting the appropriate position on the left or right-hand of the 'Signal Polarity' switch.

6. OUTPUT MODE CONTROL

6.1. Serial outputs are provided on the front panel of the unit for normal use, and a parallel character output is available at the rear for special purpose use.

6.2. The test messages and patterns can be generated continuously with the control switch set to the 'Free Run' position.

6.3. With the switch set to 'Single Shot Char. or Message' the output can be generated character by character or sequence by sequence respectively under manual or electronic control. The pseudo-random test pattern is released 511-bit sequence by sequence in either 'Char' or 'Message' positions.

A message, sequence or character can be set to its beginning by depressing the 'Reset' push button, and in the 'Single Shot' positions, will remain static until the 'Start' button is depressed. The 'Ready' indicator shows that the ready-to-start condition has been reached either by operation of the 'Reset' button or on completion of a single shot test generation.

When using test patterns 1:1, 2:2, 6:1 or 1:6 in the 'Single Shot Message' setting, operation of the Reset button causes the output to stop. Subsequent operation of the Start button commences continuous generation of the pattern until the Reset button is again depressed.

6.4. The function of the Start button is electronically duplicated so that characters or messages can be released by external control via a connection on the rear of the instrument.

6.5. Action of either manual or electronic start control is delayed by between 20 and 200ms in order to simulate transmission delay in systems where characters are re-transmitted for errors checking purposes, or to simulate delay in output response of some electro-mechanical devices.

7. SPEED

7.1. With the 'cal/uncal' switch in the 'cal' position the following internally generated bit-rates are available. These are derived digitally from a crystal oscillator source with an accuracy and stability of better than 0.01% and 0.005% respectively.

Lower range:	(Bits/sec) 61.141, 45, 50, 75, 90, 100, 110, 150 200 and 220.
Upper range:	(Bits/sec) 300, 96, 600, 900, 1.2K, 1.8K, 2.4K, 3.6K, 4.8K, 7.2K and 9.6K.

7.2. With the cal/uncal switch in the 'uncal' position the same range of bit rates is available but derived from an oscillator which can be varied in frequency by $\pm$ 20%. Thus a continuous coverage from 30 bits/sec (37.5 - 20%) to 11.5K bits/sec (9.6K + 20%) is available with a long term stability of 1%. The 'uncal' indicator lights to show that the bit rate may be adjusted to a speed off nominal.

7.3. An external oscillator can be used with the bits/sec control switched to 'Ext I/P' and the external source connected to terminals at the rear of the instrument.

7.3. (Contd/)

A frequency at element-rate is required. This facility is intended for use with a synchronous modem which supplies its own timing signal. Frequencies from 30 bits/sec up to 10K bits/sec can be accommodated.

The input needs to be of rectangular waveform to C.C.I.T.T. V24, or logic level between 0v and 5v.

8. DISTORTION

8.1. The output signals can be subjected to either bias distortion or start element distortion. Bias distortion represents a shift in the average mark:space ratio and can be applied in either direction.

Start element distortion consists of shortening or lengthening the start element of a character, thus giving the remaining character elements a timing displacement relative to the leading edge of the start elements.

8.2. Distortion in 1% steps is digitally derived and can be imposed on any of the test waveforms by means of two control switches, 10's and units respectively.

8.3. The type of distortion applied can be selected by a control switch to be one of the following:

(a)	Mark Bias	(b)	Space Bias
(c)	Short Start	(d)	Long Start

or to provide 'worst case' conditions:

(d)	Mark and Space bias on alternate characters.
(e)	Short Start and Long Start on alternate characters.

N.B. When the bits/sec control is switched to 'Ext I/P', no distortion is imposed on the output, regardless of the distortion control setting.

9. OUTPUT SIGNALS

9.1. Outputs compatible with both high level telegraph equipment and C.C.I.T.T. V24 data communication equipment are provided. The inherent distortion present on the output signal is less than 0.1% for the V24 output at 9600 bits/sec. For the high-level output the distortion is less than 1% at 600 bits/sec, and less than 5% at 3600 bits/sec.

9.2. An output fully isolated from protective earth and internal signal ground is provided at two 4 m.m. sockets on the front of the instrument. (10-110v and Telegraph Earth). The level can be continually adjusted by means of multi-turn dial from 10-110v with an accuracy and stability of better than 2v. The output current is limited from 20mA to 100mA by a calibrated control on the front panel.
Single current negative or positive, or a double current output drive can be selected by adjustment of a pre-set selector switch on the rear of the unit. Matching of the positive and negative signalling levels is within 2v.

This output is capable of driving directly into telegraph equipment and physical lines at bit rates up to 3600 bits/sec.

9.3. An electronically simulated 'open/short circuit' contact is provided to drive equipment with internal signalling power supplies. Positive or negative supplies of up to 120v and current up to 100mA can be driven. This output is fully isolated and provided on a separate 4 m.m. socket on the front of the instrument and is referenced to Telegraph Earth. A series resistor of 1K is provided to protect the circuit from mis-use.

This output can be used at bit rates up to 3600 bits/sec.

9.4. An output compatible with C.C.I.T.T. V24 and E.I.A. RS-232 recommendations is provided on two 4 m.m. sockets on the front of the equipment (V24 and COMM.).

Provision is made for either Telegraph Earth or Signal Common to be connected to Protective Earth by linking between sockets on the front panel.

10. ANCILLARY CONTROLS

10.1. Certain facilities can be supplemented or modified by a control panel mounted at the rear of the instrument. Control is affected by insertion or omission of 'U' links between two columns of sockets on the panel.

10.2. PC + QBF (5): By insertion of a link, the 5-unit 'Fox' message can be preceded by the character sequence programmed on the front panel matrix and followed by the sequence programmed on the rear panel matrix. In this condition the programmed sequences are 'distortion free', regardless of the setting of the distortion controls, unless the internal DIST.FREE P. CHARS link on Logic Board 1 has been removed.

10.3. PC + QBF (8): By insertion of a link, the 8-unit 'Fox' message can be preceded by the character sequence programmed on the front panel matrix and followed by the sequence programmed on the rear panel matrix. As in 10.2. the programmed sequences are 'distortion free'.

10.4. MESS. BY MESS.: Insertion of a link enables generation of the 'front panel matrix programmed sequence' and the 'Fox message + rear panel programmed sequence' alternately for successive operations of the 'Start' button when in the 'Single-Shot Message' mode of working.

10.5. LC + UC: A link is normally inserted if the 8-unit 'Fox' message in lower case is to be preceded by the upper case message. With this link and the LC ONLY link extraced, only the upper case 'Fox' message is generated in the '8-unit' position of the 'Test Message' switch on the front panel.

10.6. LC ONLY: By insertion of a link, only the lower case 'Fox' message is generated in the '8-unit' position of the 'Test Message' switch.

10.7. ODD PARITY: A link must be inserted to change the normally even parity generated for 8-unit 'Fox' messages.

10.8. NO START: Insertion of a link deletes the start element normally present in each 'Start-Stop' character.

11. ANCILLARY INPUT/OUTPUT

11.1. Provision is made on the rear of the instrument for the input, output and monitoring of certain useful signals.

11.2. On the lower part of the control panel, sockets are provided for:

(a) Acceptance of an input timing source at element rate. This signal is required to be at logic (0 to +5v) or C.C.I.T.T. V24 level. (EL IN).

(b) Output of clock at 100 times element rate (100 x CLOCK OUT).

(c) Output of an element timing signal producing one cycle per element (EL TIMING OUT).

(d) Output of a character timing signal producing a pulse one element in width per character (CH TIMING OUT).

(e) Output of a message timing signal producing a pulse 1/100th of an element in width per message (MESS TIMING OUT).

(f) Output of a pseudo-random block timing signal producing a pulse one element in length per 511-bit sequence (BLOCK TIMING OUT).

(g) The two bottom sockets provide the 0v (Signal Common) connection to which all the signals on the panel are referred.

Signals (b) to (f) are all of logic level (0 to +5v).

11.3. A Cannon 25-way socket is provided to enable a parallel output or input to be used. (See table following).

11.3. Ancillary Input/Output (Contd/)

Skt. Pin No.	Signal	Function
1	CHAR. PRESENT PULSE	0v for first 4 information elements of character, otherwise +5v.
2	STOP PULSE	+5v for Stop element duration, otherwise 0v.
3	RUNNING	0v when instrument is running, +5v when instrument is reset.
4	EXT. R/S	Application of I/P greater than +3v duplicates action of 'Stop' button.
5	EXT. START	Application of I/P greater than +3v duplicates action of 'Start' button.
6	BIT 1 OUT	)
7	BIT 2 OUT	)
8	BIT 3 OUT	)
9	BIT 4 OUT	) Information elements of 'parallel output
10	BIT 5 OUT	) character'; 0v = 1, +5v = 0.
11	BIT 6 OUT	)
12	BIT 7 OUT	)
13	BIT 8 OUT	)
14	0v	Common Return.
15	V24 O/P	C.C.I.T.T. V24 output.
16	H.S. TIMING OUT	Timing Output 100 x element rate at 0v and +5v level.
17	EXT. TIMING I/P	Element Timing Input. Signal must go more +ve than +3v and more -ve than 0v for correct operation.
18	BIT 8 IN	)
19	BIT 7 IN	)
20	BIT 6 IN	)
21	BIT 5 IN	) "Parallel input" information elements;
22	BIT 4 IN	) 0v = 1, +5v or O/C = 0.
23	BIT 3 IN	)
24	BIT 2 IN	)
25	BIT 1 IN	)

12. CIRCUIT DESCRIPTION

12.1. General

Fig. 1 shows the Schematic Diagram for the T.D.M.G. The basic 100 x element-rate clock (HSS) is obtained by division as required from a 2.88 MHz oscillator. HSS is used to drive the 50-way Up/Down (reversible) counter which gives a total division of 100 to give the element-rate timing signal. Distortion is imposed by varying the division of this counter to give the required modification of element-length. Similarly, the stop element of a character can be increased to $1\frac{1}{2}$ or 2 elements by increasing the division to 150 or 200 respectively.

If the instrument speed control is set to 'Ext I/P', then the element timing signal is derived from the External Timing I/P instead of the Up/Down Control Logic. The element-rate signal is used to step the Character-Length counter, which can be made to count from 5 to 10, depending on the type and length of character required. This counter in turn steps the Message-Length counter which is used to address the Programmed Sequence logic and the Read-Only Memory (R.O.M.), the latter containing the Q9S and 5- and 8-unit Fox messages.

All the start stop message sources present their characters sequentially in parallel form to the Output Data Serialiser, where the individual elements are scanned and start and stop elements added if required by the Character-Length counter, afterwards being re-timed by a clocked bistable to give a clean output signal. This signal drives the various output circuits.

Transmission of 'Programmed Sequence + Fox Message' is done under the control of the Message Sequence Control counter which also controls the transmission of 'Lower Case + Upper Case 8-unit Fox message' when required.

The 511-bit Pseudo-Random Generator register is stepped by the same element-rate signal as that used to step the Character-Length counter.

13.0. LOGIC ELEMENTS

13.1. General

The digital integrated circuits used in the instrument consist of 3 types:

"930" series gates and bistables;
"9306" 10-way Up/down counters; and
National Semiconductors type "MM5220" M.O.S. Read only Memory (R.O.M.).

13.2. NAND Gates (936, 946, 962, 930, 932)

All gates perform the 'positive logic' NAND function, i.e. when all inputs to a gate are positive (logical '1' or MARK state) the output is at 0v (logical '0' or SPACE state); under all other input conditions the output is positive. With the 930 and 932 elements it is possible to expand the number of gate inputs by using the expander nodes available on pins 3 and 11.

A feature of all gates except the 932 is that several gate outputs can be joined together in the 'wire OR' configuration; with this arrangement any gate whose inputs are all high will hold the common output point low, i.e. all gates have to have at least one input low for the common output to go high.

13.3. Bistables (9093)

Apart from those contained in the 9306 up/down counters, all bistable circuits used are of the J-K, d.c. triggered, master/slave type (9093).

With this type of circuit, data is fed into the master (or input) bistable whilst the clock waveform is high. When the clock goes low, the slave (or output) bistable will take up the state of the master bistable. The Sd input can be used to switch the circuit asynchronously and overrides the clocked inputs.

The drawing conversion used in the circuit diagram is such that the bistable 'set' input and 'true' output is always considered to be the top pair of input/output connections on the symbol.

13.4. Up/Down Counters (9306)

The 9306 is a synchronously presettable, reversible, 10-way binary coded decimal (b.c.d.) counter made up from 4 bistables, the outputs of which represent each counter state in "weighted" code, i.e. Q0 = 1, Q1 = 2, Q2 = 4 and Q4 = 8 so that state 3 for example is represented by $Q0.Q1.\overline{Q2}.\overline{Q3}$.

If the 'counter enable' inputs CE are all high and the 'count direction' input CD is also high, then application of clock pulses to clock input CP will cause the counter to count "up", 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, etc. giving a "terminal count" output TC on each count of 9. If CD is low, then the counter will count "down", 9, 9, 7, 6, 5, 4, 3, 2, 1, 0, 9, 8, etc. giving output TC on each count of 0.

If "parallel enable" input PE is taken to 0v, CE will be over-ridden and the counter stages set to the states corresponding to the conditions imposed on inputs P0 - P3 under the control of clock input CP.

13.4. (Contd/)

The clock required to drive the counter is the inverse of that required to drive a "9093" type of bistable; data is fed into the counter whilst the clock is low and the counter stages change state immediately after the clock goes high.

13.5. Read-Only Memory and Drivers (MM5220 and DM8810)

The MM5220 is a 1024-bit static read-only memory (R.O.M.), the contents of which are customer-specified, being inserted during one stage of the device fabrication. The output can be obtained either in the form of 256 x 4 bit or 128 x 8 bit parallel words, under the control of the MODE CONTROL input; for the T.D.M.G., "128 x 8" operation is required and to obtain this the MODE CONTROL and A8 inputs are taken to a permanent 0v as shown in Fig. 3. VDD is also taken to 0v whilst VSS is taken to +12v and VGG to -12v. The R.O.M. is a "negative logic" device, i.e. a '1' is a more negative level than a '0' and with the aforementioned supply voltages a level on the A1 - A8 (binary address), MODE CONTROL or CHIP ENABLE inputs is considered to be a '1' between 0v and +4v and a '0' if between +10v and +12v. These high level signals are obtained by using DM8810 high level driver circuits, which are 2-input NAND gates with "free O/P collectors" capable of switching at +12v.

"CHIP ENABLE" is gated into the parallel outputs B1 - B8 and when at 0v will allow the outputs to take up the states of the 8-bit word selected by the binary address inputs A1 - A7. When CHIP ENABLE is high, B1 - B8 will remain low.

The truth table for the R.O.M. used in the instrument (MM5220 GJ) is given below. Address 0 is given by $\overline{A1}.\overline{A2}.\overline{A3}.\overline{A4}.\overline{A5}.\overline{A6}.\overline{A7}$, address 1 by $A1.\overline{A2}.\overline{A3}.\overline{A4}.\overline{A5}.\overline{A6}.\overline{A7}$. and so on. It must be remembered here that this is "negative logic", unlike the rest of the logic in the instrument, therefore a "0" output as given by the truth table is seen as a "1" by the "positive logic" circuits it drives and a "1" is seen as a "0".

13.6. MM5220 GJ R.O.M. TRUTH TABLE

Note: A "1" is a more negative output
A "0" is a more positive output

CH.	Address	B8	B7	B6	B5	B4	B3	B2	B1
9	0	1	1	1	0	0	1	1	1
SP	1	1	1	1	1	1	0	1	1
Figs.	2	1	1	1	0	0	1	0	0
Q	3	1	1	1	0	1	0	0	0
LF	4	1	1	1	1	1	1	0	1
CR	5	1	1	1	1	0	1	1	1
S	6	1	1	1	1	1	0	1	0
Ltrs.	7	1	1	1	0	0	0	0	0
O	8	1	1	0	0	1	1	1	1
9	9	1	1	0	0	0	1	1	0
8	10	0	1	0	0	0	1	1	1
7	11	0	1	0	0	1	0	0	0
6	12	1	1	0	0	1	0	0	1
5	13	1	1	0	0	1	0	1	0
4	14	0	1	0	0	1	0	1	1
3	15	1	1	0	0	1	1	0	0
2	16	0	1	0	0	1	1	0	1
1	17	0	1	0	0	1	1	1	0
SP	18	0	1	0	1	1	1	1	1
G	19	1	0	1	1	1	0	0	0
O	20	0	0	1	1	0	0	0	0
D	21	1	0	1	1	1	0	1	1
SP	22	0	1	0	1	1	1	1	1
Y	23	1	0	1	0	0	1	1	0
Z	24	1	0	1	0	0	1	0	1
A	25	1	0	1	1	1	1	1	0
L	26	0	0	1	1	0	0	1	1
SP	27	0	1	0	1	1	1	1	1
E	28	0	0	1	1	1	0	1	0
H	29	1	0	1	1	0	1	1	1
T	30	0	0	1	0	1	0	1	1
SP	31	0	1	0	1	1	1	1	1
R	32	0	0	1	0	1	1	0	1
E	33	0	0	1	1	1	0	1	0
V	34	1	0	1	0	1	0	0	1
O	35	0	0	1	1	0	0	0	0
SP	36	0	1	0	1	1	1	1	1
S	37	1	0	1	0	1	1	0	0
P	38	1	0	1	0	1	1	1	1
M	39	1	0	1	1	0	0	1	0
U	40	1	0	1	0	1	0	1	0
J	41	0	0	1	1	0	1	0	1
SP	42	0	1	0	1	1	1	1	1

13.6. Truth Table (Contd/)

CH.	Address	B8	B7	B6	B5	B4	B3	B2	B1
X	43	0	0	1	0	0	1	1	1
O	44	0	0	1	1	0	0	0	0
F	45	0	0	1	1	1	0	0	1
SP	46	0	1	0	1	1	1	1	1
N	47	1	0	1	1	0	0	0	1
W	48	0	0	1	0	1	0	0	0
O	49	0	0	1	1	0	0	0	0
R	50	0	0	1	0	1	1	0	1
B	51	1	0	1	1	1	1	0	1
SP	52	0	1	0	1	1	1	1	1
K	53	1	0	1	1	0	1	0	0
C	54	0	0	1	1	1	1	0	0
I	55	0	0	1	1	0	1	1	0
U	56	1	0	1	0	1	0	1	0
Q	57	0	0	1	0	1	1	1	0
SP	58	0	1	0	1	1	1	1	1
E	59	0	0	1	1	1	0	1	0
H	60	1	0	1	1	0	1	1	1
T	61	0	0	1	0	1	0	1	1
CR	62	0	1	1	1	0	0	1	0
LF	63	1	1	1	1	0	1	0	1
D	64	1	1	1	1	0	1	1	0
N	65	1	1	1	1	0	0	1	1
E	66	1	1	1	1	1	1	1	0
R	67	1	1	1	1	0	1	0	1
T	68	1	1	1	0	1	1	1	1
Ltrs.	69	1	1	1	0	0	0	0	0
O	70	1	1	1	0	1	0	0	1
9	71	1	1	1	0	0	1	1	1
8	72	1	1	1	1	1	0	0	1
7	73	1	1	1	1	1	0	0	0
6	74	1	1	1	0	1	0	1	0
5	75	1	1	1	0	1	1	1	1
4	76	1	1	1	1	0	1	0	1
3	77	1	1	1	1	1	1	1	0
2	78	1	1	1	0	1	1	0	0
1	79	1	1	1	0	1	0	0	0
Figs.	80	1	1	1	0	0	1	0	0
SP	81	1	1	1	1	1	0	1	1
G	82	1	1	1	0	0	1	0	1
O	83	1	1	1	0	0	1	1	1
D	84	1	1	1	1	0	1	1	0

13.6. Truth Table (Contd/)

CH.	Address	B8	B7	B6	B5	B4	B3	B2	B1
SP	85	1	1	1	1	1	0	1	1
Y	86	1	1	1	0	1	0	1	0
Z	87	1	1	1	0	1	1	1	0
A	88	1	1	1	1	1	1	0	0
L	89	1	1	1	0	1	1	0	1
SP	90	1	1	1	1	1	0	1	1
E	91	1	1	1	1	1	1	1	0
H	92	1	1	1	0	1	0	1	1
T	93	1	1	1	0	1	1	1	1
SP	94	1	1	1	1	1	0	1	1
R	95	1	1	1	1	0	1	0	1
E	96	1	1	1	1	1	1	1	0
V	97	1	1	1	0	0	0	0	1
O	98	1	1	1	0	0	1	1	1
SP	99	1	1	1	1	1	0	1	1
S	100	1	1	1	1	1	0	1	0
P	101	1	1	1	0	1	0	0	1
M	102	1	1	1	0	0	0	1	1
U	103	1	1	1	1	1	0	0	0
J	104	1	1	1	1	0	1	0	0
SP	105	1	1	1	1	1	0	1	1
X	106	1	1	1	0	0	0	1	0
O	107	1	1	1	0	0	1	1	1
F	108	1	1	1	1	0	0	1	0
SP	109	1	1	1	1	1	0	1	1
N	110	1	1	1	1	0	0	1	1
W	111	1	1	1	0	1	1	0	0
O	112	1	1	1	0	0	1	1	1
R	113	1	1	1	1	0	1	0	1
B	114	1	1	1	0	0	1	1	0
SP	115	1	1	1	1	1	0	1	1
K	116	1	1	1	1	0	0	0	0
C	117	1	1	1	1	0	0	0	1
I	118	1	1	1	1	1	0	0	1
U	119	1	1	1	1	1	0	0	0
Q	120	1	1	1	0	1	0	0	0
SP	121	1	1	1	1	1	0	1	1
E	122	1	1	1	1	1	1	1	0
H	123	1	1	1	0	1	0	1	1
T	124	1	1	1	0	1	1	1	1
Ltrs.	125	1	1	1	0	0	0	0	0
CR	126	1	1	1	1	0	1	1	1
LF	127	1	1	1	1	1	1	0	1

14. MAINTENANCE INSTRUCTIONS

14.1 ACCESS TO THE INSTRUMENT

WARNING : ISOLATE THE T.D.M.G. FROM THE MAINS SUPPLY BEFORE DISMANTLING

14.1.1 Access to the plug-in sub-boards may be gained by removing the top cover after unscrewing four 3mm Pozidrive screws located at each corner of the cover.

NOTE: To ensure that a stable environment exists when functionally testing and/or recalibrating the equipment, the top cover must be replaced and secured with the four 3mm Pozidrive screws.

Care should be taken when removing the following sub-boards:-

Logic Board 2 - Disconnect the co-axial connection from the front panel.

Programme Board - Disconnect four front and rear plug connections

After switching "ON" the mains supply, allow for a ten minute warm-up period.

14.1.2 To remove the front panel it is necessary to take off the top and bottom cover, the latter being held in place by four 3mm screws located at the feet centres. Place the carrying handle in its normal working position, i.e. supporting the unit, and unscrew the four 3mm screws.positioned, two in each side panel, just to the rear of the front panel. Disconnect the front panel wiring to the two sub-boards mentioned in paragraph 14.1.1., and the mains wiring plug mounted on the right hand side panel. The front panel may then be carefully removed from the Mother Board 100 way edge connector.

14.1.3 With the exception of the high level output voltage selector all knobs are removed from the front panel as follows:-

Pull out the plastic centre-piece which exposes either a hexagon headed or screwdriver-slotted collet nut. Lossening the nut by half to three-quarters of a turn will allow the knob to be withdrawn.

14.1.4 Replacement of faulty front panel components will in the case of the following controls require the removal of the decorative plate.

All lever switches
+ 20% Variable speed control
High level current limit and voltage selector
Single shot delay control
Programme character selector

The decorative plate is secured in place by all the components not listed above. The light emitting diodes are mounted in plastic clips and may be pressed out from the front of the panel.

14.1.5 Having removed the front panel it is then possible to withdraw the Mother Board after disconnecting plugs 2 and 3, and removing the rear support screw. The main function of the two plugs in question is as follows:-

PL2 - To route unstabilised d.c. supplies from the right hand side panel to the Mother Board.

PL3 - To connect rear panel components to the Mother Board.

Access to these plugs may be gained by removing all plug-in sub-boards.

The Mother Board rear support is a 3mm screw located on the underside, securing the board to the rear panel.

14.1.6 To remove either of the side panels it is first necessary to take off the carrying handle. This is done by unscrewing the large black chrome studs on the side panels using a 4mm hexagon slot wrench. The left hand side panel may then be removed completely by unscrewing the six 3mm countersunk screws, two at the front, four at the rear. The right hand side panel is connected to the rear panel by a cableform, and care must be taken not to damage the wiring when separating the two panels.

14.1.7 For the replacement of power transistors and other rear panel components it is possible by removing plugs 2 and 3, eight 3mm screws, four on each side, and the Mother Board rear support screw, to lay the rear panel flat in an accessible position.

14.2 REPLACEMENT OF COMPONENTS ON PRINTED CIRCUIT BOARDS

14.2.1 All printed circuit boards in this equipment, with track on both sides, have plated through holes. It is therefore only necessary to solder components on the underside of each board. When changing components on these boards the use of a hot soldering iron together with a solder sucking tool is recommended

14.3 ADJUSTMENT OF PRESET CONTROLS

14.3.1 Variable Oscillator (Logic Board 2)

After replacement of certain components in this circuit, re-adjustment of C7 may be required. Connect a frequency counter to the V24 terminals on the front panel, switch mains on, and set the controls for a free running 1:1 test message at a calibrated speed of 1200 bits/sec. Note the frequency counter reading. Switch CAL - UNCAL switch to the latter position and set the $\pm$ 20% control to NOM. Adjust C7 for the recorded frequency counter reading.

14.3.2 Stabilised Voltage Supplies (Power Supply Board)

After replacement of certain components on this board re-adjustment of RV's 1, 2 and 5 may be required. Set RV1 for a potential at power supply board edge connector pin 24 of + 5V ± 50 mV. Check edge connector pins R and 22 for voltages of + 12V ± 200 mV and - 12V ± 200 mV respectively.

Potentiometers RV2 and 5 are used to set the upper and lower ends of the high level output voltage control. Connect a voltmeter capable of reading between 10 and 110V across the high level output terminal. Switch mains on and set the control for a constant + ve MARK output with the speed control set to 50 Bits/sec. Set the high level output voltage control to 110V and adjust RV2 for the correct voltmeter reading. Reset the voltage control to 10V and adjust RV5 for the correct voltmeter reading. As these two preset controls interact, the procedure should be repeated until both upper and lower voltage limits are correct.

COMPONENT LISTS

15. COMPONENTS LIST

15.1. Board 1 Assembly - AKB 4388

15.1.1. Resistors:- Electrosil TR5 $\frac{1}{2}$W $\pm$ 5%

Cct. Ref.	Value	Cct. Ref.	Value	Cct. Ref.	Value
R1	1K	R11	1K	R21	2K7
R2	1K	R12	1K	R22	6K8
R3	1K	R13	1K	R23	6K8
R4	1K	R14	2K7	R24	6K8
R5	1K	R15	2K7	R25	6K8
R6	1K	R16	2K7	R26	6K8
R7	1K	R17	2K7	R27	6K8
R8	1K	R18	2K7	R28	6K8
R9	1K	R19	2K7	R29	3K9
R10	1K	R20	2K7	R30	1K

15.1.2. Integrated Circuits

Cct.Ref.	Type	Cct.Ref.	Type	Cct.Ref.	Type
IC1	9093	IC12	9093	IC23	DM 8810
IC2	9093	IC13	946	IC24	962
IC3	936	IC14	9093	IC25	936
IC4	9093	IC15	DM 8810	IC26	962
IC5	930	IC16	936	IC27	946
IC6	930	IC17	946	IC28	936
IC7	930	IC18	930	IC29	MM 5220GJ
IC8	962	IC19	930	IC30	946
IC9	946	IC20	946	IC31	930
IC10	946	IC21	930	IC32	936
IC11	9093	IC22	946	IC33	936

Board 1 Assembly - (Contd/)

15.1.3. Diodes

Cct. Ref.	Type
D2, D3, D7 D9 - 13.	IN 4148 alt. IS 44. IN 914, BAX 13.

15.2. Board 2 Assembly - AKB 8121

15.2.1. Resistors:- Electrosil TR5 $\frac{1}{2}$W $\pm$ 5%

Cct. Ref.	Value	Cct. Ref.	Value	Cct. Ref.	Value
R1	100K	R18	1K		
R2	5K6	R19	1K		
R3	10K	R20	1K		
R4	470K	R21	3K3		
R5	470	R22	18K		
R6	5K6	R23	1K		
R7	1K	R24	1K		
R8	1K	R25	1K		
R9	470				
R10	6K8			R44	2K7
R11	5K6			R45	1K
R12	1K			R46	1K
R13	180			R47	1K
R14	1K8			R48	1K
R15	2K2			R49	330
R16	3K3			R50	1K
R17	1K			R51	1K

15.2.2. Transistors

Cct. Ref.	Type	Cct. Ref.	Type	Cct.Ref.	Type
TR1	BFX 87	TR5	BFY 51	TR9	BSX 19
TR2	BSX 19	TR6	BC 107	TR10	BCY 70
TR3	BFY 51	TR7	2N 2906	TR11	BC 107
TR4	BC 107	TR8	BSX 19	TR12	BSX 19

Board 2 Assembly - (Contd/)

15.2.3. Capacitors

Cct. Ref.	Value	Wkg. Voltage	Type and Manufacturer
C1	0.22	160v	STC. CJA.
C2	100p	400v	TFF. Wima.
C3	1000p	400v	TFF. Wima.
C4	8-50p		557-000E. Trimmer Erie.
C5	0.01	100v	TFM. Wima.
C6	120p. 10%	30v	HS. Suflex.
C7	8-50p		557-000E. Trimmer Erie.
C8	0.01	100v	TFM. Wima.
C9	0.01	100v	TFM. Wima.

15.2.4. Integrated Circuits

Cct. Ref.	Type	Cct. Ref.	Type	Cct. Ref.	Type
IC1	9316	IC13	9093	IC25	962
IC2	9316	IC14	930	IC26	962
IC3	962	IC15	932	IC27	946
IC4	936	IC16	946	IC28	936
IC5	946	IC17	946	IC29	946
IC6	9093	IC18	930	IC30	9093
IC7	9093	IC19	936	IC31	946
IC8	9093	IC20	936	IC32	930
IC9	946	IC21	9093	IC33	9306
IC10	9316	IC22	936	IC34	946
IC11	930	IC23	936	IC35	9093
IC12	9093	IC24	936		

Board 2 Assembly - (Contd/)

15.2.5. Diodes

Cct. Ref.	Type
D1 - D12	IN 4148

15.2.6. Miscellaneous

Cct. Ref. if applicable	Item	Type/Part No./Manufacturer
X1	Crystal	2.88 MHz. A07973. BF.
X2	Crystal	2347.810 MHz.
RLY 1	Relay	121-C-1. Astralux.
	Socket (2)	450-3704-1-03. Cambion.

15.3. Board 3 Assembly

15.3.1. Resistors:- Electrosil TR5 $\frac{1}{2}$W $\pm$ 5%

Cct. Ref.	Value	Cct. Ref.	Value	Cct. Ref.	Value
R1	1K	R12	1K	R23	1K2
R2	1K	R13	1K	R24	1K5
R3	1K	R14	1K	R25	1K2
R4	1K	R15	1K	R26	1K
R5	1K	R16	1K	R27	1K
R6	1K	R17	1K	R28	1K
R7	1K	R18	3K3	R29	1K
R8	3K3	R19	1K	R30	1K
R9	18K	R20	18K	R31	1K
R10	1K	R21	5K6	R32	1K
R11	1K	R22	15K		

15.3.2. Transistors

Cct. Ref.	Type
TR1	BC 107 alternatives BC 207, 2N929.
TR2	BC 107 alternatives BC 207, 2N929.
TR3	BCY 70 alternatives BC 154, U19387.
TR4	2N 2906 alternatives BSX 29, 2N4916.
TR5	BSX 19 alternatives 2N706.
TR6	BSX 19 alternatives 2N706.

15.3.3. Diodes

Cct. Ref.	Type
D1 - D8	IN 914 alternatives 1344, IN4148, BAX 13.

Board 3 Assembly - (Contd/)

15.3.4. Capacitors

Cct. Ref.	Value	Wkg. Voltage	Type and Manufacturer
C1	0.1	250v	MPTL. I.T.T. alt. C281 VV Mullard.
C2	6.8 10%	6v	472. I.T.T.

15.3.5. Integrated Circuits

Cct. Ref.	Type	Cct. Ref.	Type	Cct. Ref.	Type
IC1	936	IC9	962	IC17	946
IC2	946	IC10	946	IC18	946
IC3	930	IC11	9093	IC19	9093
IC4	936	IC12	9093	IC20	962
IC5	936	IC13	936	IC21	930
IC6	962	IC14	946	IC22	930
IC7	962	IC15	930	IC23	962
IC8	962	IC16	930		

15.4. Power Supply Board - 202005

15.4.1. Resistors - Carbon Film $\frac{1}{2}$W $\pm$ 5% except where otherwise indicated

Cct.Ref.	Value	Cct.Ref.	Value	Cct.Ref.	Value
R1	1K5	R22	15K	R43	
R2	22K	R23	1K	R44	3K3 Met Flm $\pm$2%
R3	1K	R24		R45	4K7 Met Flm $\pm$2%
R4	56 - Elec TR.6	R25	56K	R46	470
R5	470	R26	470	R47	390
R6	220	R27	2K7	R48	82
R7	1K	R28	2K7	R49	82
R8	15K	R29	100	R50	A.O.T.
R9		R30	2K7	R51	5K6
R10	470	R31	100	R52	15K
R11	470	R32	5K6	R53	
R12	15K	R33	1K5	R54	33K
R13	56K	R34		R55	4K3
R14	220K	R35	8K2	R56	680
R15	10K	R36	2K7	R57	
R16	56 - Elect TR.6	R37	1K	R58	10K
R17	22K	R38	5K6	R59	10K
R18		R39	5K6	R60	2K2
R19	1K5	R40	1K2 Met Flm $\pm$2%	R61	
R20	1K	R41	1K2 Met Flm $\pm$2%	R62	
R21	220	R42	2K2	R63	

Power Supply Board - (Contd/)

15.4.1. Resistors (Contd/)

Cct.Ref.	Value	Cct.Ref.	Value	Cct.Ref.	Value
R64		R76	2K2	R87	220K Met Flm ±2%
R65		R77	3K9	R88	
R66		R78	330	R89	
R67		R79	1K	R90	10K
R68		R80	270	R91	6K3
R69	680	R81	1K5	R92	15K
R70		R82	3K9	R93	2K7
R71		R83	1K5	R94	2K7
R72		R84	470	R95	680
R73		R85	15K	R96	3K3
R74	1K	R86	220K Met Flm ±2%	R97	47K
R75	6K3				

15.4.2. Diodes

Cct. Ref.	Type	Cct.Ref.	Type
D1	BZY 88 C6V2 alt. IS 2062A		
D2	BZY 88 C5V6 alt. IS 2056A	D18	IN 4003
		D19	IN 4003
D5	BZY 88 C5V6 alt. IS 2056A		
D6	BYX 36/15 alt. IN 4001.	D25	IS 3200 alt. IN 5388A.
D7	BYX 36/15 alt. IN 4001.	D26	IS 3200 alt. IN 5388A.
D8	BYX 36/15 alt. IN 4001.	D27	IN 4148
D9	BYX 36/15 alt. IN 4001.		

Power Supply Board - (Contd/)

15.4.2. Diodes (Contd/)

Cct. Ref.	Type	Cct.Ref.	Type
D10	BZY 88 C5V6 alt. IS 2056A.	D43	IN 4003
D11	BZY 88 C5V6 alt. IS 2056A.	D44	BAX 17
D12	IN 4003	D45	IS 3200 alt. IN 5388A.
		D46	IS 3200 alt. IN 5388A.
		D47	BAX 17

15.4.3. Capacitors

Cct. Ref.	Value	Wkg. Voltage	Type and Manufacturer
C1	0.033	160v	TFM. Wima.
C2	0.033	160v	TFM. Wima.
C3	2.2	160v	EN 12.12. Erie.
C4	2.2	160v	EN 12.12. Erie.
C5 - C6	——	——	——
C7	0.1	250v	C281 VV. Mullard.
C8	0.1	250v	C281 VV. Mullard.
C9 - C10	——	——	——
C11	100	15v	Printylit. Wima.
C12	100	6v	Printylit. Wima.
C13	100	15v	Printylit. Wima.
C14	470	25v	Printylit. Wima.
C15	470	25v	Printylit. Wima.
C16	100	15v	Printylit. Wima.
C17 - C32	——	——	——
C33	1.0	160v	TFM. Wima.
C34	1.0	160v	TFM. Wima.

Power Supply Board - (Contd/)

15.4.4. Resistors Variable

Cct. Ref.	Value	Type and Manufacturer
RV1	500	Morganite 84. Cermet.
RV2	200	Morganite 84. Cermet.
RV5	50	Morganite 84. Cermet.

15.4.5. Integrated Circuits

Cct. Ref.	Type
IC1	962
IC2	MCT26/TIL 112
IC5	uA 741

15.4.6. Transistors

Cct.Ref.	Type	Cct.Ref.	Type	Cct.Ref.	Type
TR1	40327	TR15	BCY 70	TR33	2N2906
TR2	40327	TR16	BCY 70		
		TR17	BFY 51		
TR4	BCY 70	TR18	BF 258		
TR5	BC 107	TR19	BSX 19		
TR6	V 765	TR20	2N2906	TR39	BC 107
TR7	V 765	TR21	2N5416	TR40	BCY 70
		TR22	2N5416	TR41	BCY 70
*TR9	BFY 51	TR23	BC 107	TR42	2N2910
TR10	BC 107			TR43	2N2906
TR11	BCY 70	TR26	2N5416	TR44	BSX 19
*TR12	BFX 87			TR45	2N2906
TR13	BC 107	TR30	2N2906	TR46	40327
TR14	BC 107	TR31	BSX 19	TR47	2N5416

*Heatsink required for these items.

Power Supply Board - (Contd/)

15.4.7. Miscellaneous Items

Item	Part No. and Manufacturer
Heatsink (2)	5F-2. Redpoint (for use with TR9 and TR12).
Rear Matrix Board	AKB 4813, Trend.

15.5. Mother Board Assembly - AKB 7281

15.5.1. Resistors:- Carbon Film $\frac{1}{2}$W $\pm$ 5%

Cct. Ref.	Value
R1 - R16	1K
R17	390

15.5.2. Capacitor

Cct. Ref.	Value	Type and Manufacturer
C1	680p 10%	Style YD. Erie.

15.5.3. Transistor

Cct. Ref.	Type
TR1	BSY 19 alternative BSX 19, 2N 706.

15.5.4. Integrated Circuits

Cct. Ref.	Type	Cct. Ref.	Type
IC1	9306	IC9	946
IC2	9093	IC10	962
IC3	936	IC11	932
IC4	936	IC12	946
IC5	962	IC13	936
IC6	930	IC14	9093X
IC7	946	IC15	936
IC8	936	IC16	936

Mother Board Assembly - (Contd/)

15.5.5. Miscellaneous Items

Cct. Ref. if applicable	Item	Part No. and Manufacturer
SKT2	Connector	AKB 7950A. Trend.
SKT3	Connector	AKB 7949A. Trend.
SKT5	Edge Connector	EWD 40/40 FS. Ferranti.
SKT6	Edge Connector	EWD 32/32 FS Ferranti.
SKT7	Edge Connector	EWD 32/32 FS. Ferranti.
SKT8	Edge Connector	EWD 24/24 FS. Ferranti.
SKT9	Edge Connector	EWD 32/32 FS. Ferranti.
	Connector Guides (6)	P5000027. Cinch.
	Polarising Key (2)	

15.6. Front Panel Assembly - 202003

15.6.1. Resistor: Electrosil TR4

Cct. Ref.	Value
R1	150
R2	150

15.6.2. Potentiometers

Cct. Ref.	Value	Part No. and Manufacturer
RV1	250	Type MW. Reliance with $\frac{3}{4}$" mounting bush.
RV2	50K	Type MW. Reliance with $\frac{3}{4}$" mounting bush.
RV4	1K	Hel. 05.610. Reliance, alt. 173-489.

15.6.3. Switches

Cct. Ref.	Type	Part No. and Manufacturer
SW1	Wafer 2 pole 11 position	AKB 4405. Trend.
SW2	Toggle with Black Cap	MST.216 N. Waycom.
SW3	Wafer 4 pole 12 position	AKB 4404. Trend.
SW4	Lever 1 pole 4 position	AKB 4409. Trend.
SW5	Lever 1 pole 3 position	AKB 4408. Trend.
SW6	Toggle with Black Cap	MST.116 N. Waycom.
SW7	Wafer 3 pole 10 position	AKB 7438. Trend.
SW8	Wafer 60° Throw 2 pole 5 position	AKB 7439. Trend.
SW9	Wafer 36° Throw 2 pole 7 position	AKB 4407. Trend.

Front Panel Assembly - (Contd/)

15.6.3. Switches (Contd/)

Cct. Ref.	Type	Part No. and Manufacturer
SW10	Lever 1 pole 4 position	AKB 4409. Trend.
SW11	Toggle with Black Cap	MST.216 N. Waycom.
SW12	Lever 1 pole 4 position	AKB 4409. Trend.
SW14-SW21	Toggle with Black Cap	MST.116 D. Waycom.
PB1	Miniature 2 pole changeover.	Radio Spares.
PB2	Miniature with Black Cap.	T906. Arcolectric.

15.6.4. Indicators

Cct. Ref.	Item	Part No. and Manufacturer
LP1	Lamp - Solid State	5082-4850. Hewlett Packard.
LP2	Indicator - 240v Neon Red	L1902. Belling Lee.
LP3	Lamp - Solid State	5082-4850. Hewlett Packard.

15.6.5. Miscellaneous

Item	Qty.	Part No. and Manufacturer
Edge Connector(Modified)	1	AKB 4799-A. Trend.
Socket Black 4 m.m.	6	941-920. Radiall.
Plug.	2	460-3308-1-03. Cambion.
Counter Dial Multiturn.	1	Beckman Instruments.
Plugs for Matrix.	50	673-31-000-04. Ghielmetti Ltd.
Front Programme Matrix Board Assembly.	1	AKB 4803. Trend (see below).

15.6.6. Front Programme Matrix Board Assembly - AKB 4803

Item	Part No. and Manufacturer
Matrix Board.	AKB 4279-A. Trend.
Edge Connector 41 way (for chars. 1-4).	AKB 4839-A. Trend.
Edge Connector 38 way (for chars. 5-8).	AKB 4840-A. Trend.
Character 1 Cablestrip.	AKB 5349 alternative 7760.
Character 2 Cablestrip.	AKB 5350 alternative 7761.
Character 3 Cablestrip.	AKB 5351 alternative 7762.
Character 4 Cablestrip.	AKB 5352 alternative 7763.
Character 5 Cablestrip.	AKB 5353 alternative 7764.
Character 6 Cablestrip.	AKB 5354 alternative 7765.
Character 7 Cablestrip.	AKB 5355 alternative 7766.
Character 8 Cablestrip.	AKB 5356 alternative 7767.

15.7. Side Panel Assembly - 202010

15.7.1. Resistors:- Welwyn Type 21 10% 5W.

Cct. Ref.	Value
R91	10K
R92	10K

15.7.2. Capacitors

Cct. Ref.	Value	Wkg. Voltage	Type and Manufacturer
C24	10000	10v	KA 2027B. Erie.
C25	2000	16v	2000C 431 BR/E. Mullard.
C26	2000	16v	2000C 431 BR/E. Mullard.
C27	200	300v	CE 20L. T.C.C.
C28	200	300v	CE 20L. T.C.C.

Side Panel Assembly - (Contd/)

15.7.3. Miscellaneous

Cct. Ref.	Item	Part No. and Manufacturer
T1	Mains Transformer.	AKB 4440. Trend.
PL2	Connector Edge 26 way.	AKB 5397. Trend.

15.7.4. Switch Sub Assembly - AKB 7348

Cct. Ref.	Item	Part No. and Manufacturer
SW22	Switch Wafer Double pole 45° throw.	AKB 4438. Trend.
	Switch Bracket.	AKB 7349. Trend.

15.7.5. Filter Assembly - AKB 7643

Item	Part No. and Manufacturer
Filter.	P.O. Type 2A. GB Electrics (GB2277).
Filter Bracket.	AKB 7347. Trend.
Terminal Block. (½ block).	L 1350. Belling Lee.

15.8. Rear Panel Assembly - 202007

15.8.1. Transistors

Cct. Ref.	Type
TR34	2N 3055. R.C.A.
TR35-TR38	2N 3739. Motorola.

Rear Panel Assembly - (Contd/)

15.8.2. Miscellaneous

Item	Part No. and Manufacturer
Connector (6).	3771-1-0310. Cambion.
Connector Edge 37 way.	AKB 4840. Trend.
Socket 25 way.	43-81-048. Cinch.
Moulded Voltage Selector with Red Plug.	R80-8118-00-000. Cinch.
Base Assembly.	43/81/965. Cinch.
'O' Ring.	RT OS. 7. Trist Mouldings.
Fuse Holder.	L2006. Belling Lee.
Fuse Link Slow Blow. (1A for 240v). (2A for 110v).	20 x 5 m.m.
Plugs for Matrix (50).	673-31-000-04. Ghielmetti Ltd.
Rear Programme Matrix Board Assembly.	AKB 4813. Trend (see below).

15.8.3. Rear Programme Matrix Board Assembly - AKB 4813

Item	Part No. and Manufacturer
Matrix Board.	AKB 4279-A. Trend.
Edge Connector 37 way (for characters 9-12).	AKB 4841-A. Trend.
Edge Connector 38 way (for characters 13-16).	AKB 4840-A. Trend.
Character 9 Cablestrip.	AKB 5361-A. Trend. alternative AKB 7772.
Character 10 Cablestrip.	AKB 5362. Trend. alternative AKB 7773.
Character 11 Cablestrip.	AKB 5363. Trend. alternative AKB 7774.
Character 12 Cablestrip.	AKB 5364. Trend. alternative AKB 7775.
Character 13 Cablestrip.	AKB 5365. Trend. alternative AKB 7776.
Character 14 Cablestrip.	AKB 5366. Trend. alternative AKB 7777.
Character 15 Cablestrip.	AKB 5367. Trend. alternative AKB 7778.
Character 16 Cablestrip.	AKB 5368. Trend. alternative AKB 7779.

15.9. 16 Character Programme Board - AKB 4459

15.9.1. Integrated Circuits

Cct. Ref.	Type	Cct. Ref.	Type	Cct. Ref.	Type
IC1	930	IC10	930	IC19	930
IC2	930	IC11	930	IC20	933
IC3	936	IC12	930	IC21	933
IC4	930	IC13	930	IC22	933
IC5	930	IC14	930	IC23	933
IC6	933	IC15	930	IC24	933
IC7	933	IC16	936	IC25	933
IC8	933	IC17	946	IC26	933
IC9	933	IC18	930	IC27	933

15.9.2. Miscellaneous

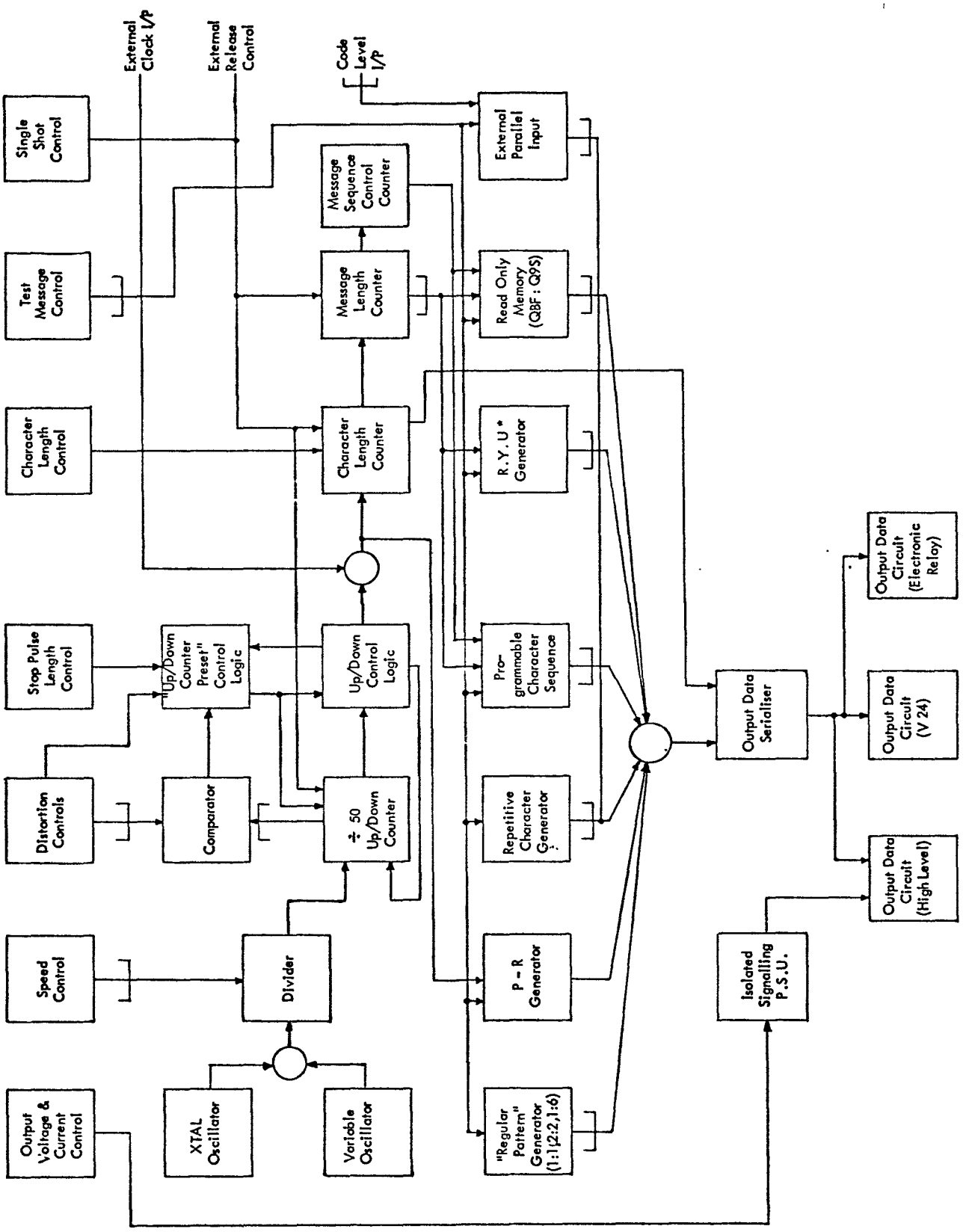
Item	Part No. and Manufacturer
Connectors	AKB 7952. Ferranti.
Connectors (2)	AKB 7949. Ferranti.
Connectors	AKB 7951. Ferranti.
Polarising Key (4)	K27. Ferranti.

15.10. Tagboard Assembly - AKB 4436

Item	Part No. and Manufacturer
Tagboard.	AKB 4439. Trend.
Barb Socket White (22)	S156. Oxley Developments.

15.11. Exterior Miscellaneous

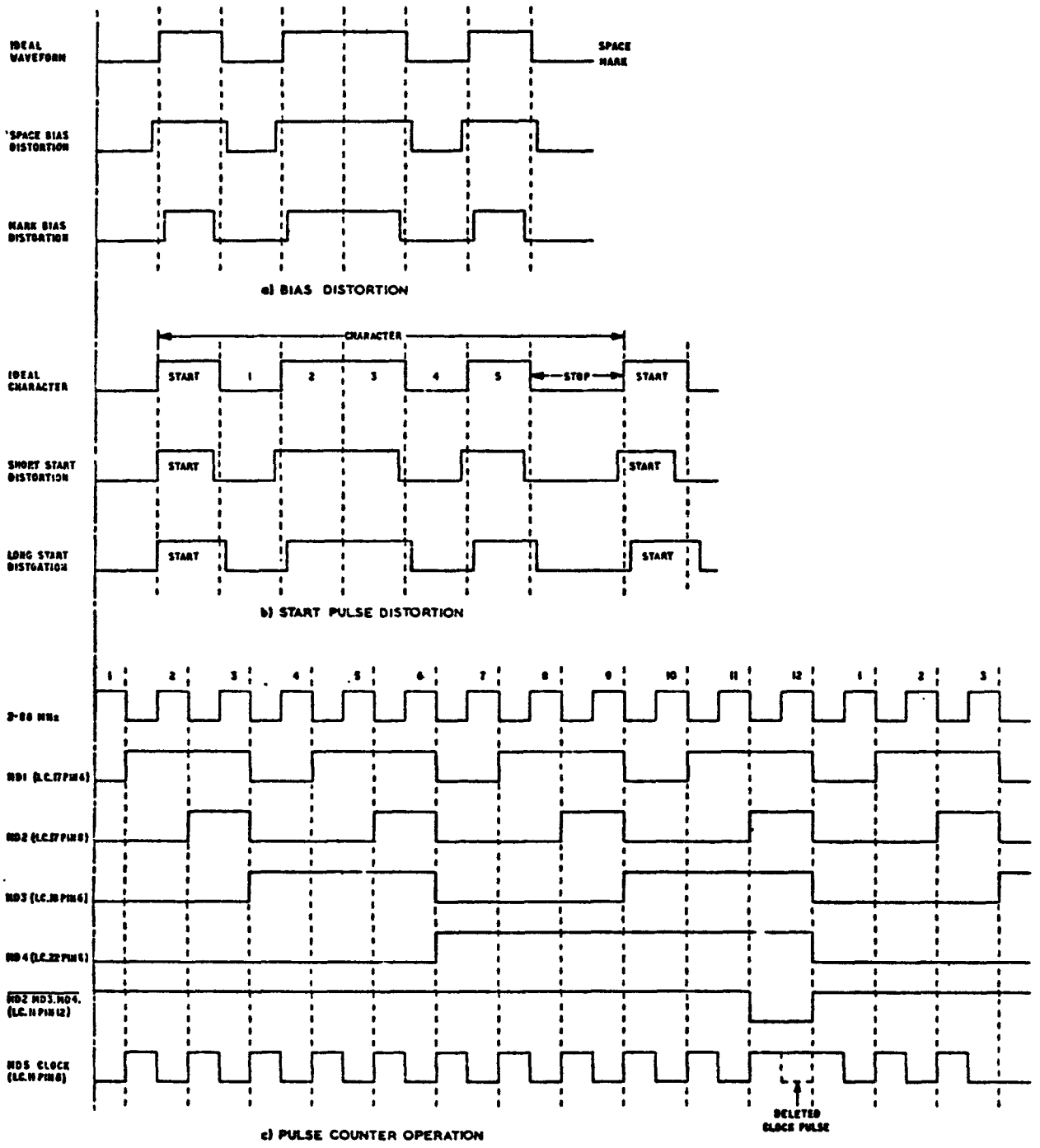
Item	Part No. and Manufacturer
Handle	AKB 7644. Trend.
Handle Mounting Block (LH)	AKB 7648. Trend.
Handle Mounting Block (RH)	AKB 7649. Trend.
Cover Handle Hinge (LH)	AKB 7661. Trend.
Cover Handle Hinge (RH)	AKB 7662. Trend.
Banana Plug Quick Release	941-460. Radiall.
Extractor Tool	673 H009. Gheilmetti.



BLOCK SCHEMATIC DIAGRAM

AHB-5378/2

FIG. 1



WAVEFORM ILLUSTRATION

Feb. 80 (Amdt. 1)

FIG. 1A.

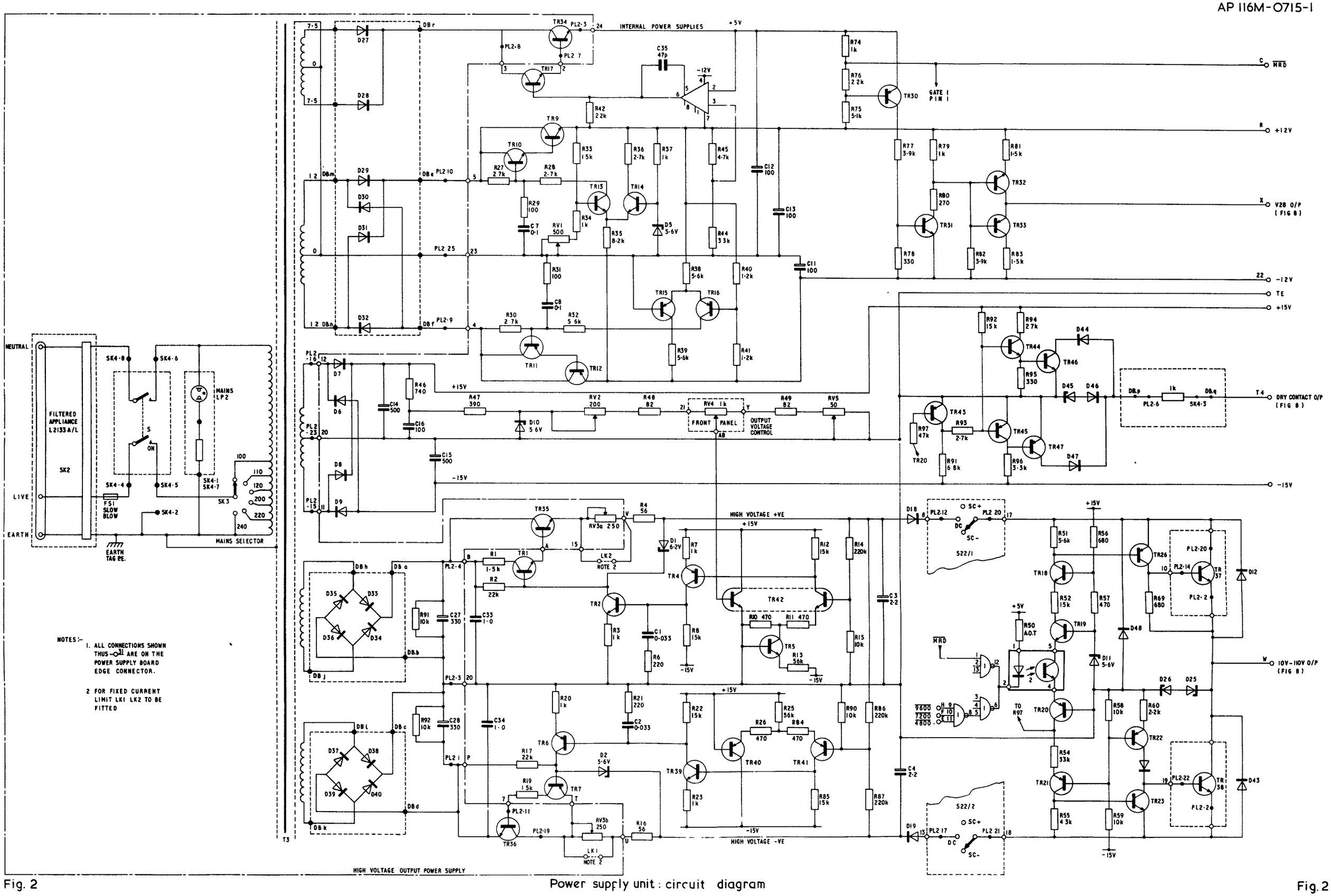


Fig. 2

Power supply unit : circuit diagram

Fig. 2

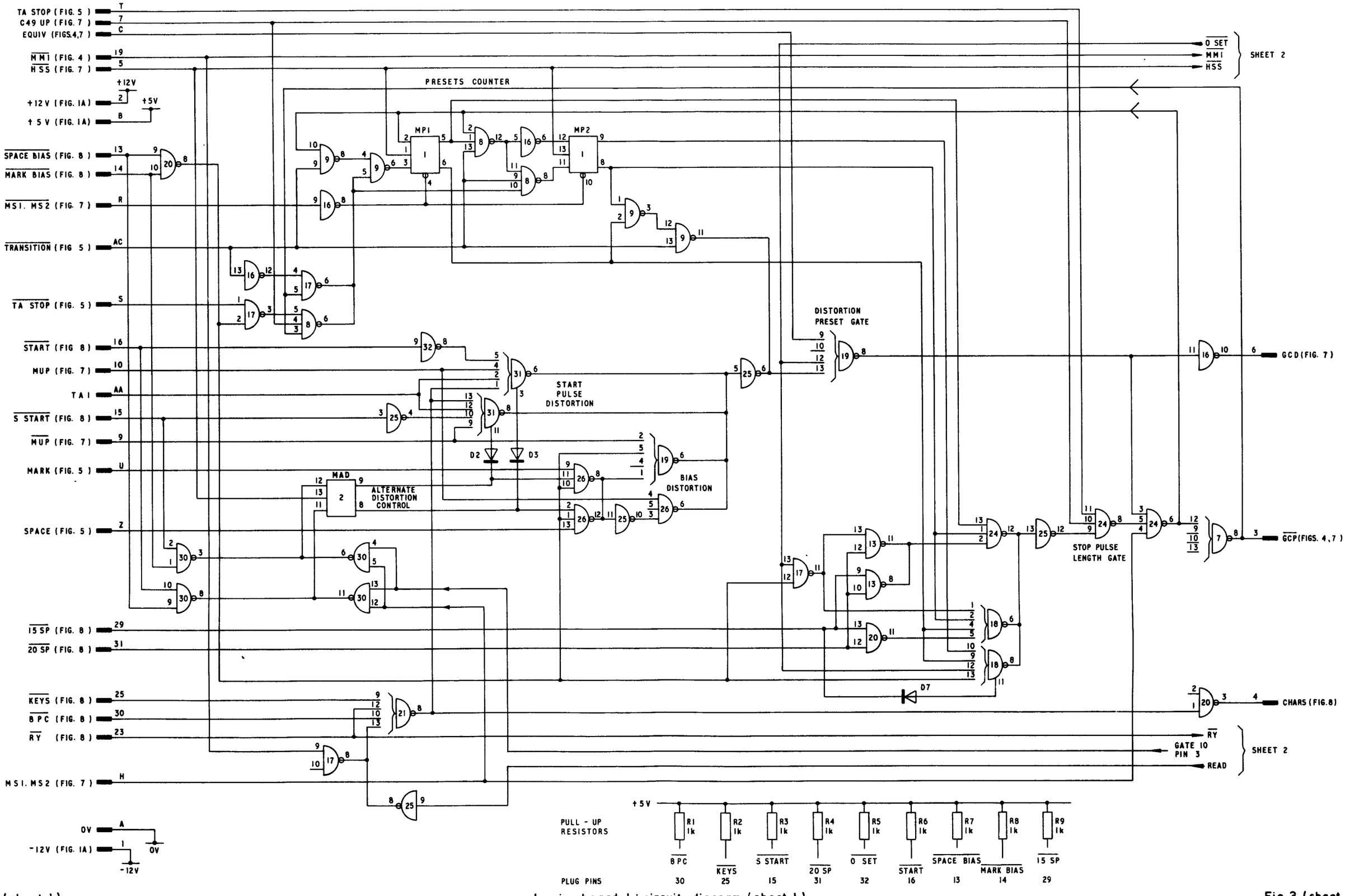


Fig. 3 (sheet 1)

Logic board 1 : circuit diagram (sheet 1)

Fig.3 (sheet 1)

Feb. 80 (Amdt.1)

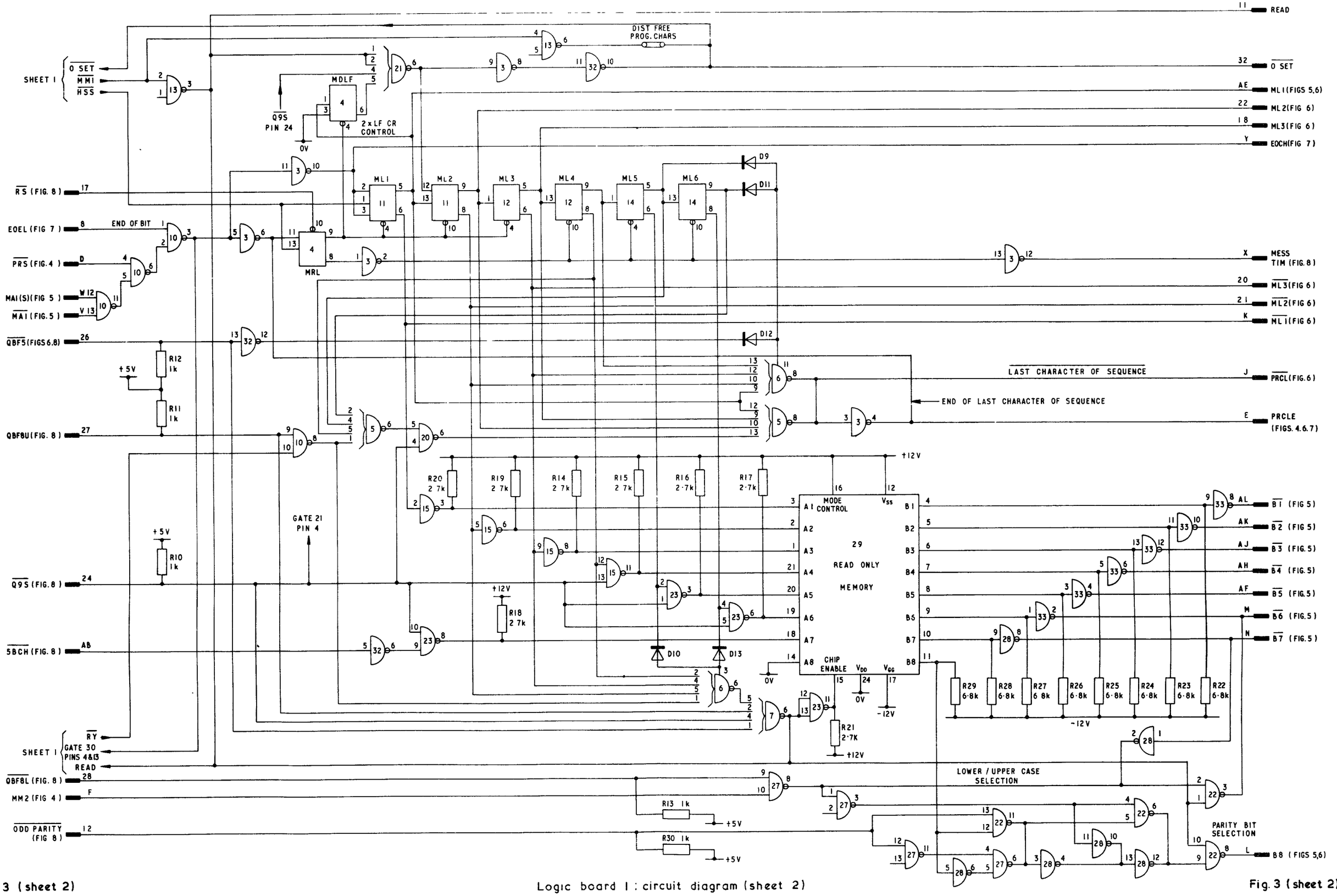


Fig. 3 (sheet 2)

Logic board 1 : circuit diagram (sheet 2)

Fig. 3 (sheet 2)

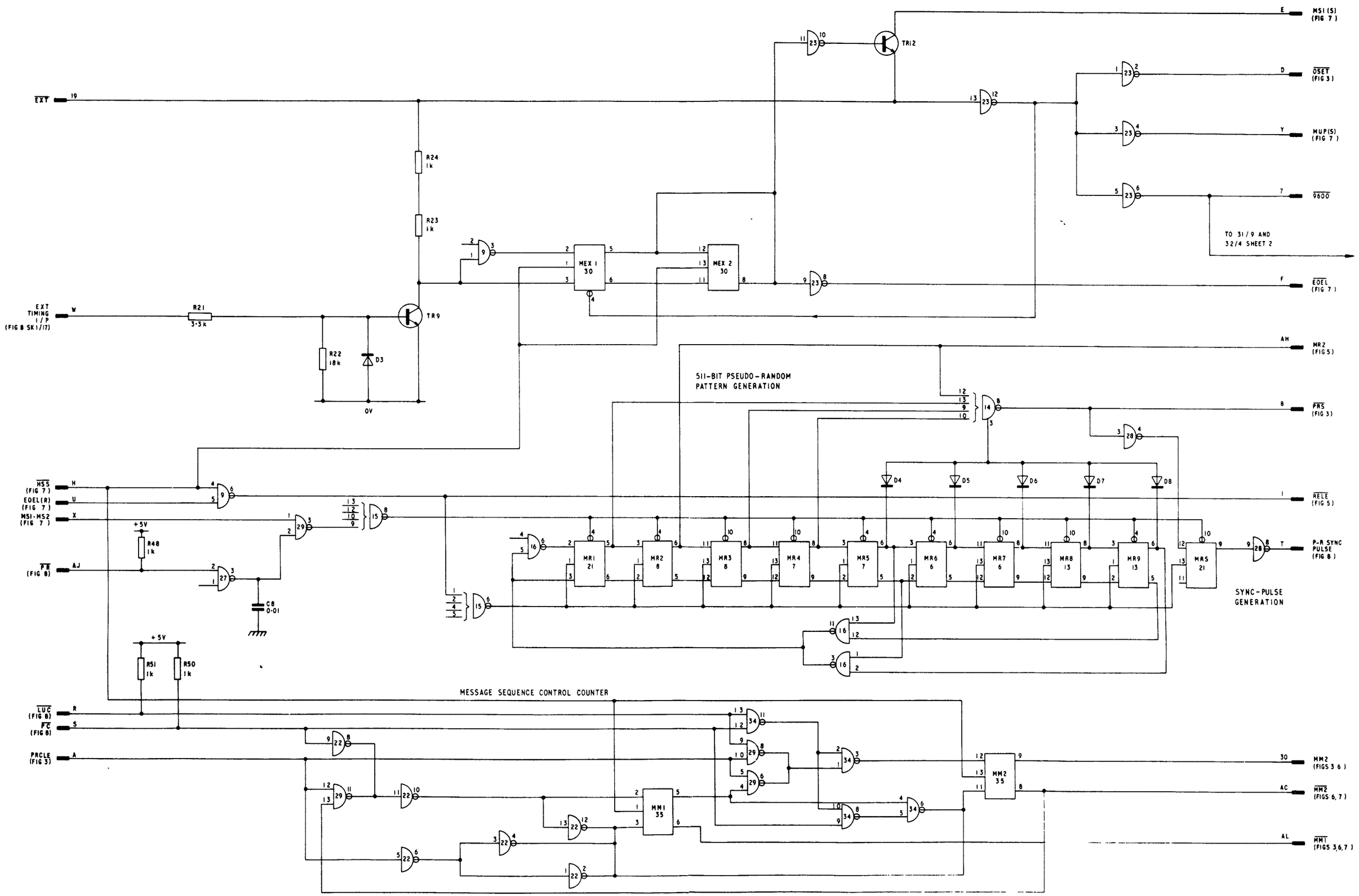


Fig. 4 (sheet 1)

Logic board 2 circuit diagram (sheet 1)

Fig. 4 (sheet 1)

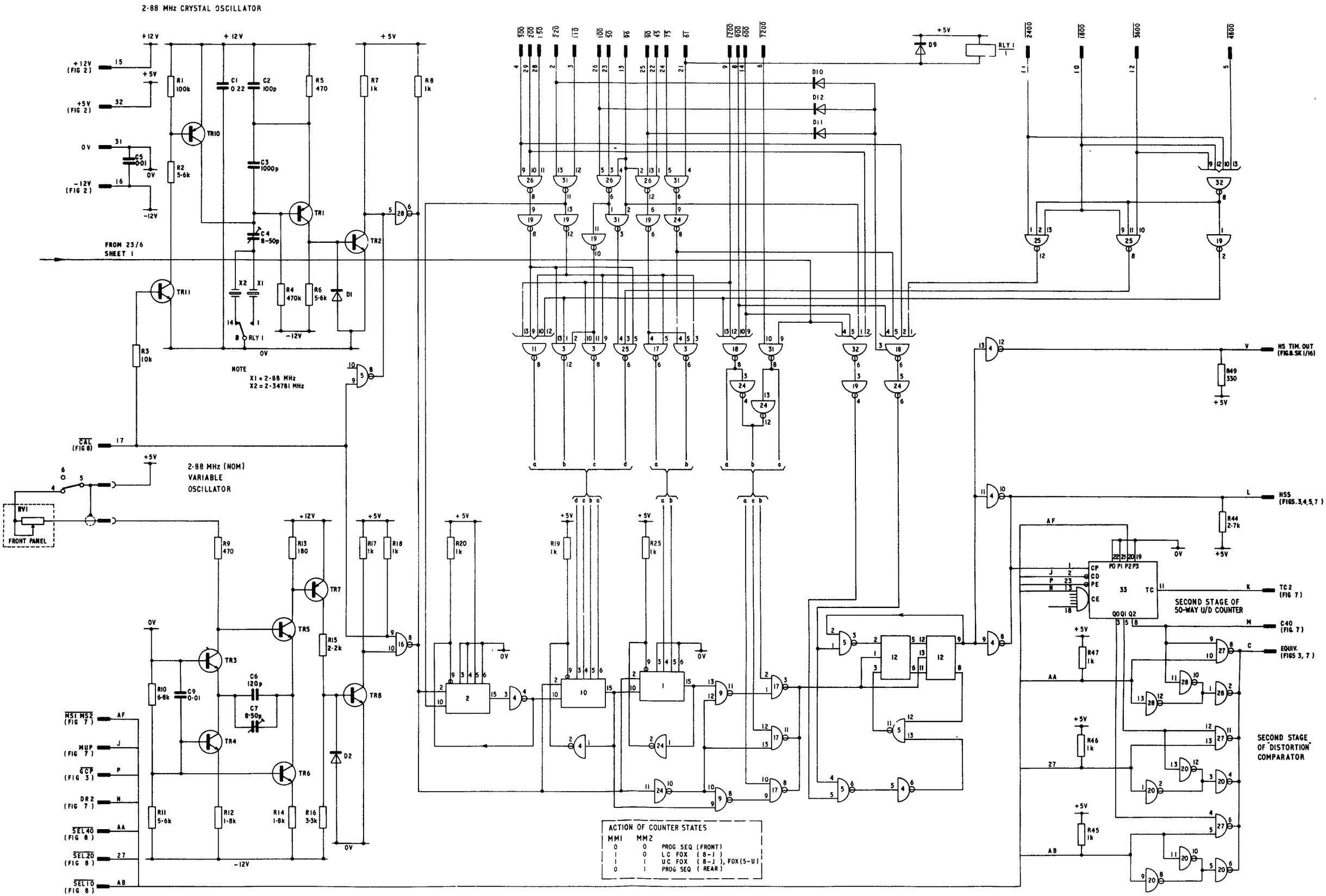


Fig. 4 (sheet 2)

Logic board 2 : circuit diagram (sheet 2)

Fig. 4 (sheet 2)

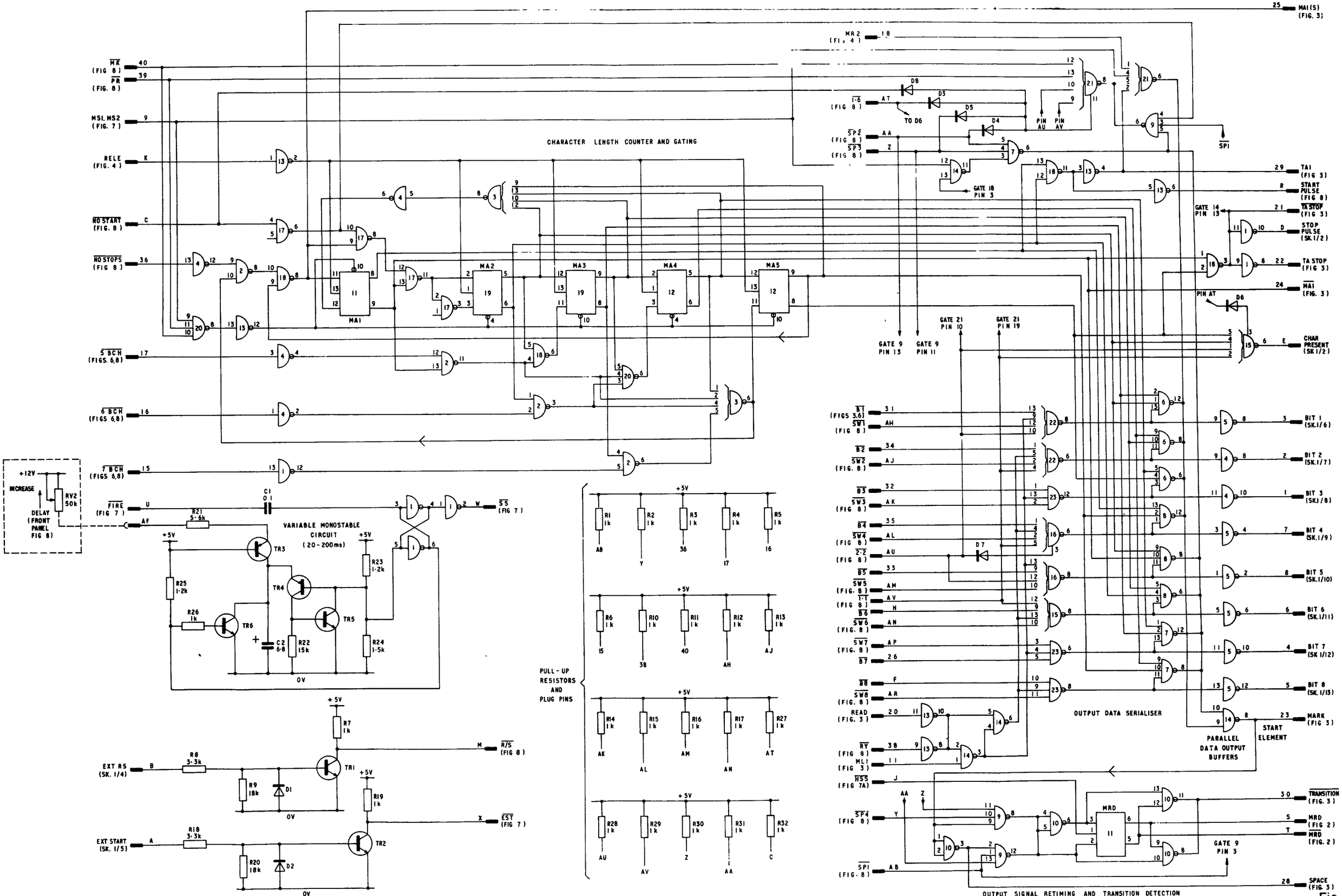


Fig. 5

Logic board 3 : circuit diagram

Fig. 5

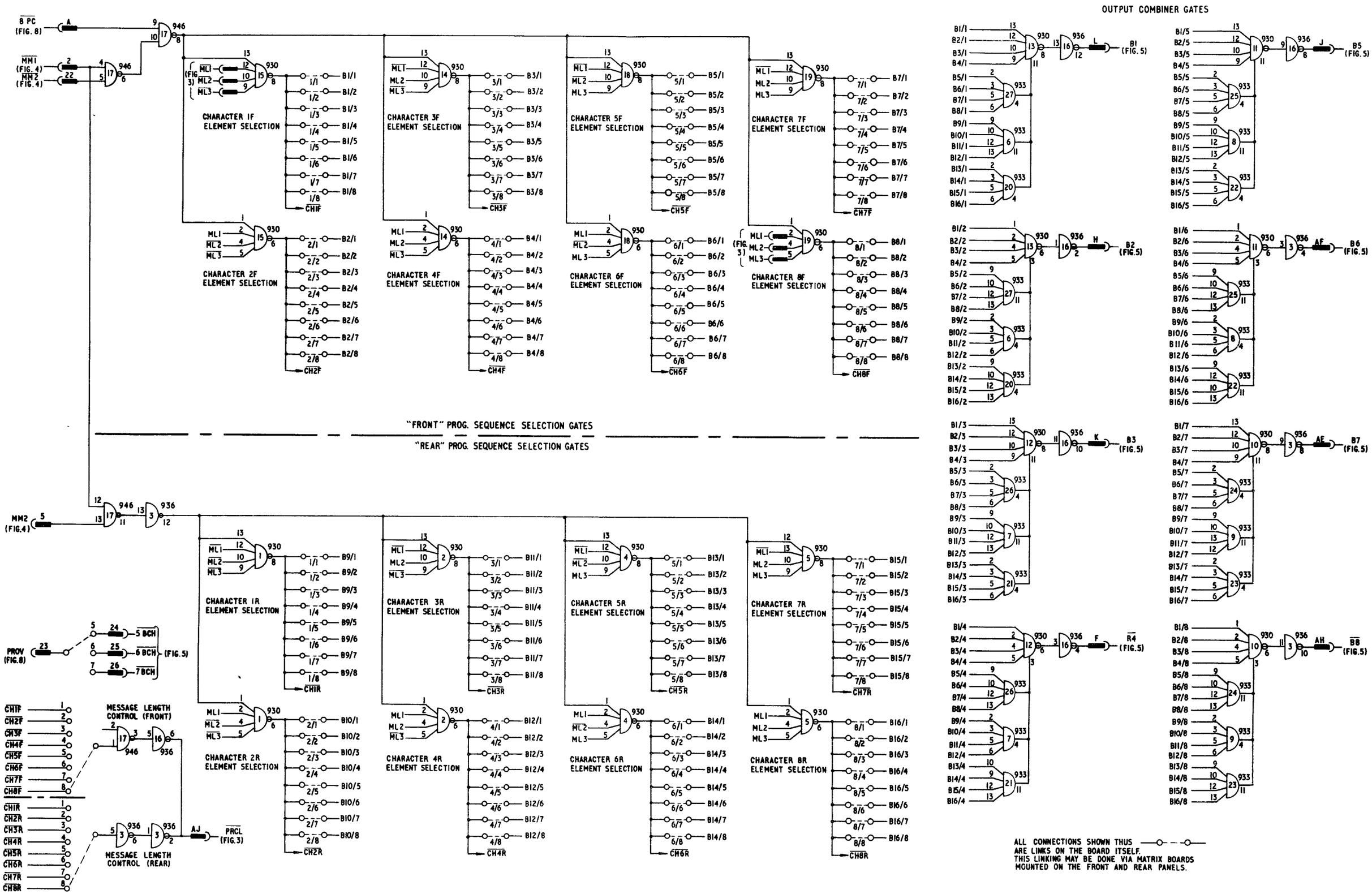


Fig. 6

Programme board : circuit diagram

Fig. 6

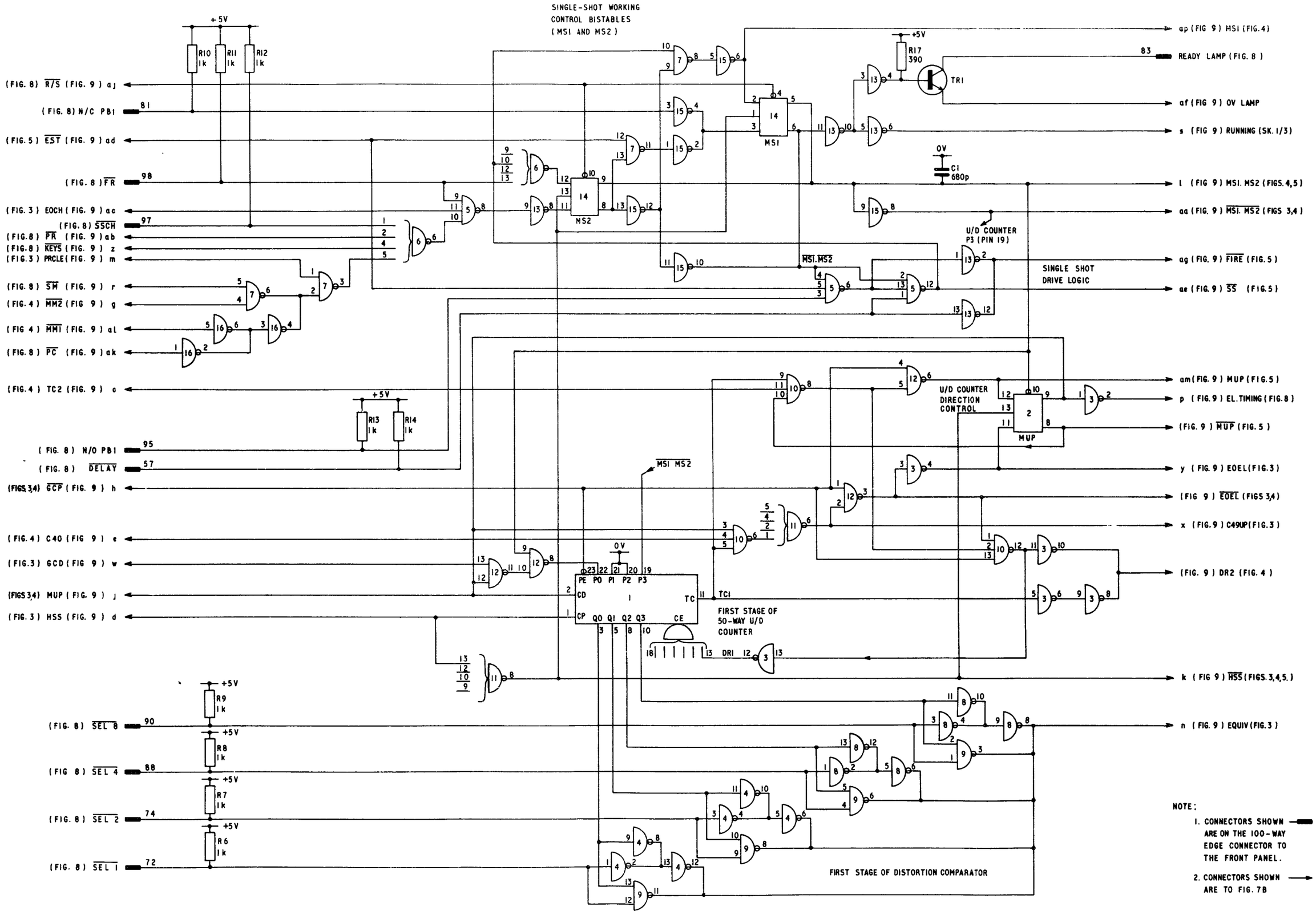


Fig. 7

Motherboard : circuit diagram

Fig. 7

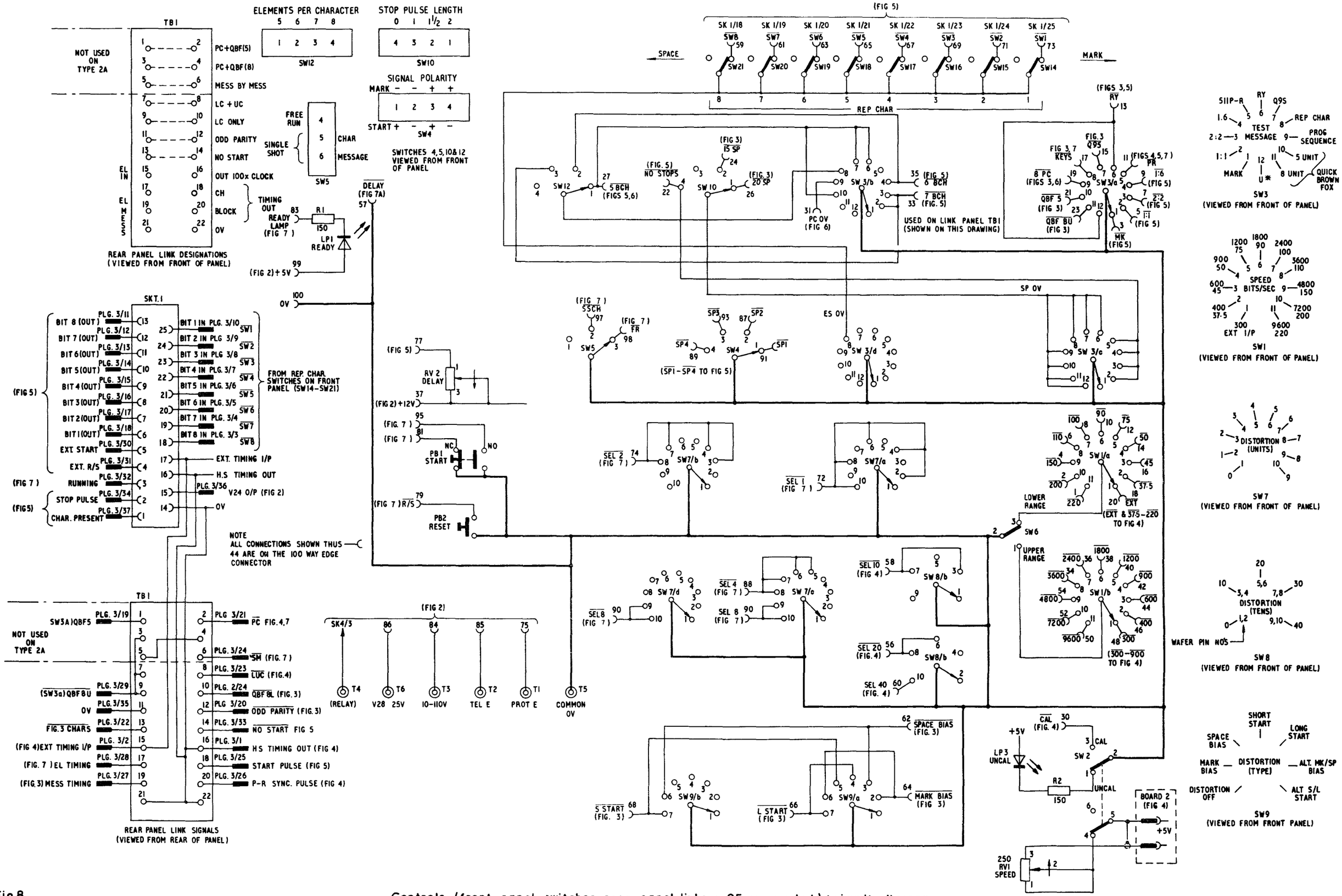
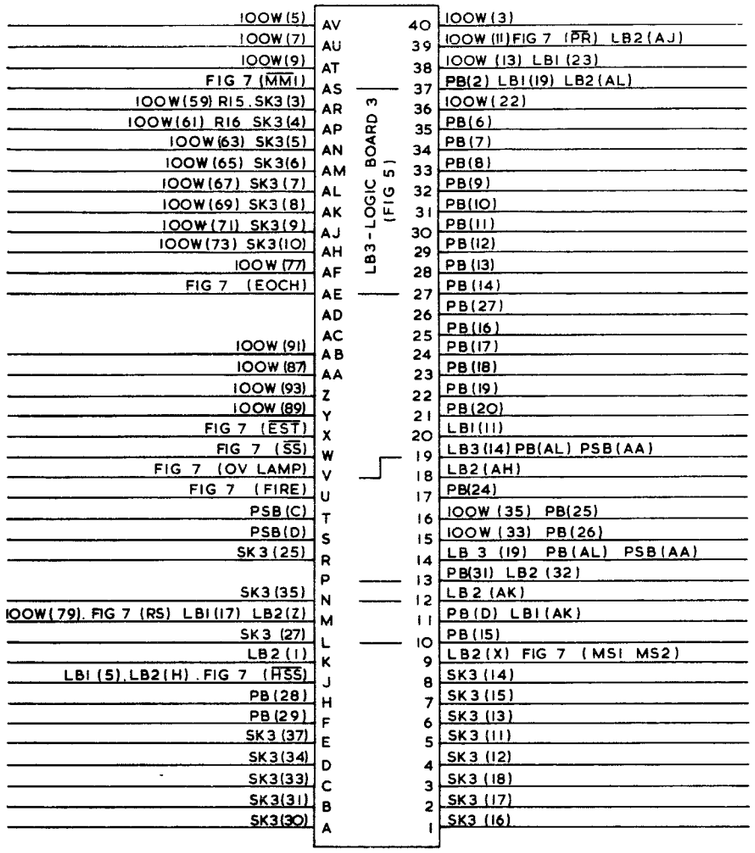
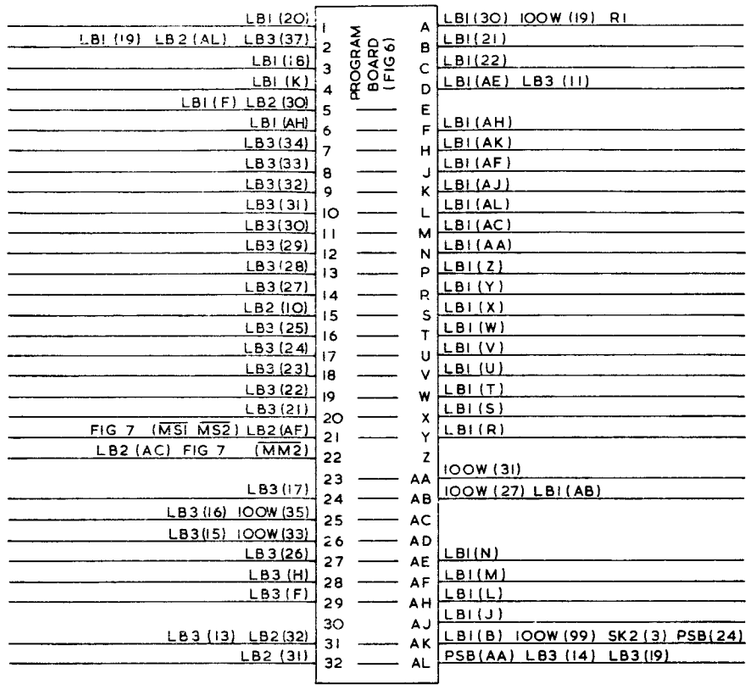
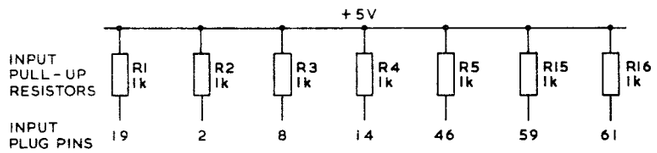
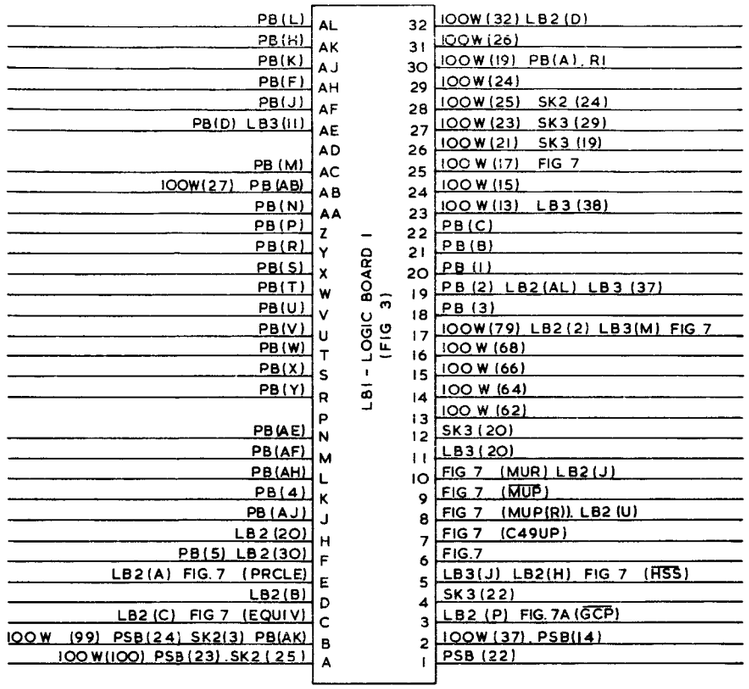


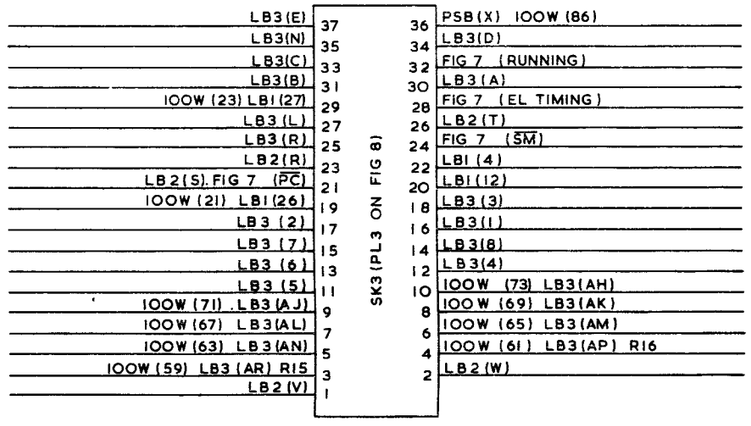
Fig.8 Controls (front panel switches, rear panel links & 25 way socket) : circuit diagram. Fig. 8

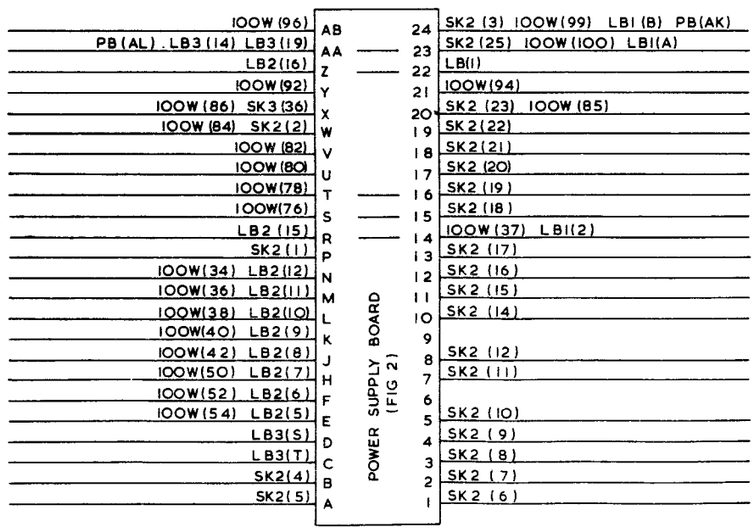


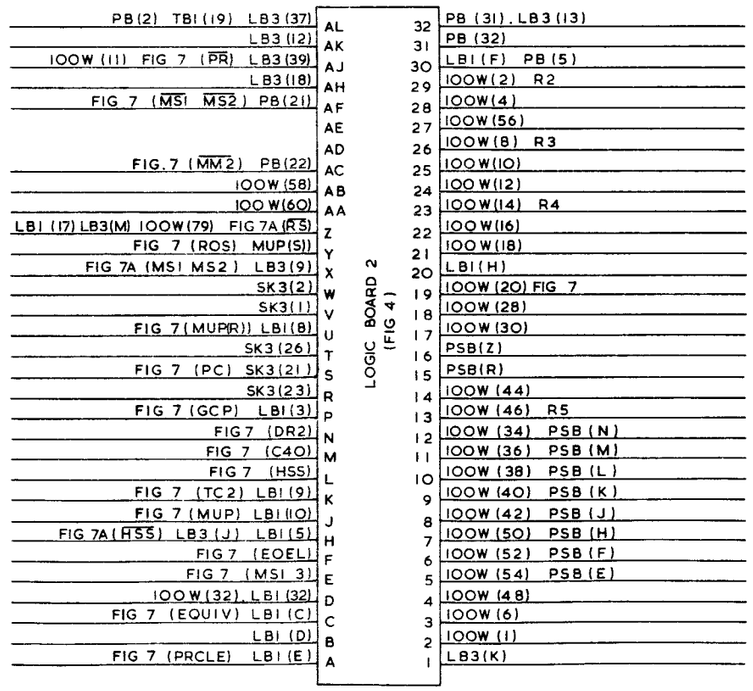












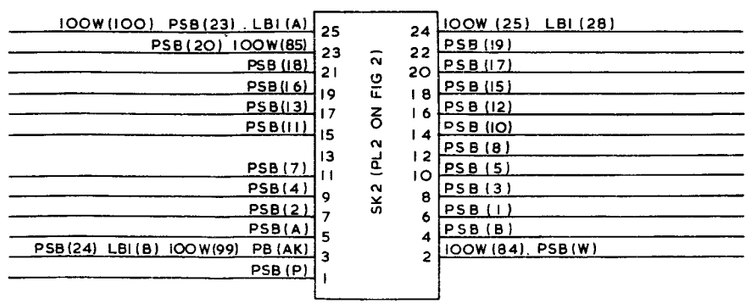


Fig. 9

Mother board : interconnection diagram

Fig. 9