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GENERATOR PULSE MODULAR CT578/3

(Gould-Advance PG52/B System)

GENERAL AND TECHNICAL INFORMATION

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Chapter 1

LEADING PARTICULARS

Title	Generator Pulse Modular CT578/3 (Gould Advance PG52B system)
Ref.no.	ZA/6625-99-620-4828
Purpose	To satisfy the requirements for a multi-purpose pulse generator with the inherent versatility offered by plug-in units.
Brief description	Generator Pulse Modular, CT578/3 basically consists of a main-frame and multiple plug-in modules constituting a system, affording repetition frequencies up to 30 MHz, with pulse widths down to 10ns and rise/fall times of 5ns. By choice of (output) modules, continuously variable outputs from 0V to 50V, positive and negative, into 50 ohms may be obtained, with full attenuation facility.

The PG52B system consists of the following modules:

	Plates Blanking	PG52P0
10S/1109171	Generator Pulse Sweep	PG52P1A
10S/1109172	Generator Pulse Width	PG52P2A
10S/1109173	Attenuator Variable	PG52P3A
10S/1109174	Variable Slope Output Unit	PG52P4A
10S/1109175	Summing Network	PG52P5
10K/1159270	Power Output Unit	PG52P6
10D/6222234	Fast Output Module	PG52P7
10D/6227363	Word Generator	PG52P8
10D/6283398	Gate Unit	PG52P9
10D/6222235	Trigger Unit	PG52P10

The main-frame contains all the necessary power supplies for the operation of a full complement of 8 modules. Each module is retained within the main-frame by two captive screws and derives power via edge-connector printed-circuit boards. Signal paths are external via BNC connectors and all inter-signals are at a common interface level. The majority of functions are by push-button selectors.

Note ...

Cooling is by forced air and blanking plates (supplied) must be fitted in all blank positions when the system is in use.

Power requirements

100V to 130V or 200V to 260V a.c. 45Hz to 60Hz at 120 Volt amperes (max).

MECHANICAL CHARACTERISTICS

Dimensions and weight	Width (mm)	Depth (mm)	Height (mm)	Weight (kg)
Main frame (without modules)	430	470	223	12.8
with 8 modules excluding P6	430	470	223	20.0
PG52P6	102	470	223	3.8
TP21 (used with P6)	14	19	9	0.7

ELECTRICAL CHARACTERISTICS

Generator pulse sweep PG52P1A	This module, termed the 'clock generator', provides the basic clock rates for the system and may be operated in either free-running, externally triggered or gated modes. The trigger mode may also be triggered manually for single shot applications or used as an aperodic divider (count-down). A sweep facility alternatively allows the internal frequency to be controlled over any selected 10:1 range by an external input.
Frequency range	0.1Hz to 30MHz in switched decade steps with uncalibrated fine control.
Accuracy	±5% at decade steps.
Sweep	Selected decade frequency range may be swept by an input voltage of +1.0V to +8V (approx) with an input resistance of greater than 1 k ohm.
Gating frequency	5MHz (max).
On	+5 volts.
Off	-0.1 volt.
Rise/fall time	1.0 µs (max).
Pulse width	0.5 µs (min) for off.
Trigger frequency	10MHz (max).
Source	External 6 volts or push-button.
÷ facility	Frequency: 2MHz (max). Ratio: ÷10 or ÷100
Clock	Synchronous with gate signal.
Output voltage	2 x 10 volts in parallel with separate test-point for c.r.o. Note ... Up to four P2A, P3A or P4 modules may be driven from parallel outputs.
Pulse-width generator PG52P2A	This Pulse Width or Delay Generator (PWD) may be used either as a variable pulse width generator or as a variable time delay generator, which can be interposed between the clock generator and another module to provide time

	delay between the clock or its trigger, and the output pulse.
Range	25ns to 1s in switched decade steps with uncalibrated fine control.
Calibration accuracy	±5% up to 5MHz
Duty-cycle	Below 10 MHz: 70% (max). Above 10 MHz: 50% (max).
Trigger level	Continuously variable between ±5 volts.
Sensitivity	2.5 volts (p-p) below 10 MHz. 5.0 volts (p-p) above 10 MHz.
Output	2 x 10 volts (positive) in parallel with separate test point for c.r.o
	Note...
	Up to four P2, P3 or P4 modules may be driven from parallel outputs. Two modules can be driven over full range of pulse widths or four modules with pulse widths greater than 50ns.

ATTENUATOR VARIABLE

PG52P3A	Standard 50 ohms output module with built-in attenuator and invert facility.
Input signal	Normally from clock generator P1A or the pulse width generator P2A but may be from any source with the necessary characteristics via either of two inputs.
Frequency	25MHz (max) - typically 30MHz.
Pulse width	20ns (min) - typically 16 ns.
Amplitude	+10 volts (max).
Rise time	5ns (typical)
Impedance	3 k ohm (min)
Output polarity	Plus and minus.
Amplitude	10 volts (max) continuously variable by independent control.
Rise time	7 ns (max). Typically 5 ns.
Impedance	50 ohms excepting on ±10 volt range. (Low impedance on ±10 volt range).

Attenuation	Push-button control on fixed ranges.
Ranges	10V, 5V, 2.5V, 1.0V, 0.5V, 0.25V and 0.1V with uncalibrated variable fine control.
Accuracy	±5% (fine control in calibrate position).
Distortion	Less than 5% of maximum pulse height on ±10V range. Typically less than 5% +20mV of max pulse height on all ranges.
Variable slope output module PG52P4A	Standard 50 ohms output module with variable rise/fall controls, dual input and invert facility.
Normal signal	Normally from clock or pulse width generator P1A or P2A but may be from any source with the necessary characteristics, via either of two inputs.
Frequency	8MHz (max).
Amplitude	0V to +10V (max).
Rise time	20ns (max).
Impedance	3 k ohms (min).
Output slope	Adjustable in decade steps with fine control over range 1 ns/volt to 100 ns/volt. Positive and negative slopes independently adjustable over 10:1 range by fine control.
Rise time	20 ns (min).
Linearity	Better than 5% full amplitude for slopes less than 10 ns/volt.
Level	10V, positive and negative, independently variable.
Impedance	50 ohms
Accuracy	±5% (at level control max).
Summing network PG52P5	
Function	This module is passive and may be used externally or as an integral part of the system. It consists of two independent resistive networks, one with two inputs and the other with three inputs, which permits the analogue summation of pulses

	(of different shape(s), amplitude or off-set) with tolerable attenuation. Inputs from PG52P3 or other signal sources may be used e.g. sine wave or d.c.
Two-input network	Delta circuit between two inputs and one output socket.
Impedance	50 ohms input/output (unterminated).
Output	Half sum of input voltages.
Three-input network	Similar to the two-input network but the output is one-third the sum of input voltage.
Input voltages	10V peak (max).
Power output module	
PG52P6	This module provides a positive or negative output of 50V (maximum) into 50 ohms with an unlimited duty-cycle. It has a dual input facility to permit the generation of output pulses from independent sources. It contains its own built-in power supply fed directly from the a.c. supply in the main-frame .
Input signal	Two inputs operating in an 'OR' function to +5V.
Frequency	3MHz (max).
Voltage	±20V peak (max).
Rise time	10 ns (max).
Impedance	Greater than 3 k ohms.
Pulse width	100 ns (min).
Output voltage	10V to 50V variable.
Polarity	+ve or -ve (with respect to earth).
Impedance	50 ohms (see note page 7)
Accuracy	±5% at 50V.
Duty-cycle	Unlimited (50W max).
Rise/fall time	Less than 15 ns (typically 10 ns).
Distortion	Less than ±8% of pulse height (typically 5% at 50V).

Power requirements	100V to 130V or 200V to 260V. 45Hz to 60Hz, 70W (max) or 20 volts batteries at 40 mA.
	Note... 50 ohms terminator, TP19 (supplied) enables high impedance loads to be driven.

Fast output module

PG52P7

This module provides simultaneous positive and negative pulses independently variable between 2.5V and 5V into 50 ohms. Variable delay (operating at leading edge of pulse) permits generation of output pulses 10 ns wide initiated by minimum width pulses of 25 ns from pulse width generator.

Input signal	Two sockets in 'OR' function (compatible with normal PG52 interface) to +6 volts.
Level	20 volts peak (max).
Frequency	30MHz (max).
Rise time	10 ns (max).
Impedance	1 k ohm.
Output polarity	Positive and negative.
Level	2.5V to 5V independently variable.
Rise time	Less than 1 ns
Fall time	Less than 2 ns
Impedance	50 ohms.
Distortion	8% (max) of pulse height.
Delay propagation	15 ns (approx).
Differential	Leading edge can be delayed by variable period up to 50 ns by front panel control (effectively reducing output pulse width).
Pulse width	10 ns (max).
Pulse coincidence	±2 ns (max).

Word generator

PG52P8

The word generator is essentially a waveform processing module for the PG52 system, enabling the generation of pulse patterns up to 16 bits in length and may be operated in a continuous or externally triggered cycle mode.

Word length	1 to 16 bits selected by rotary switch.
	Note...
	Synchronising output facility also enables modules to be encoded to extend the word length beyond 16 bits.
Pattern	Selected by 16 (toggle) switches.
Clock input	
PRF	10MHz (max).
Mark/space	50 ns.
Amplitude	+5 volts (min). ±20 volts (max).
Rise time	20 ns.
Impedance	Greater than 3 k ohms.
Start input	
Pulse width	20 ns
Amplitude	+5 volts (min). ±20 volts (max).
Rise time	20 ns (max).
Impedance	Greater than 3 k ohms.
Mode	
Repeat	Word patterns generated continuously, independent of start input signal.
External start	Word is initiated only when allowed by start input signal, viz: AC coupled: One word for each positive going edge of start signal. DC coupled: Word initiated only whilst start signal is positive (a gate function).

Word output	In non-return-to-zero (NRZ) mode word output consists of a positive signal for duration of each marked clock period (without return to zero between adjacent marked periods). In return-to-zero (RZ) mode, word output normally positive, giving negative pulse width of approx. 60 ns at beginning of each marked clock period.
Level	Standard +10V system interface.
Impedance	100 ohms (min),
Load	500 ohms (min) with short-circuit protection.
Propagation	80 ns (typical) delay from active (-ve going) clock edge.
Last pulse output	Positive signal for last period of each word generated.
Level	Standard +10V system interface.
Impedance	100 ohms.
Load	500 ohms (min) with short-circuit protection.
Propagation	60 ns (typical) delay from active (-ve going) clock edge.

Gate module

PG52P9

This module, basically a dual-input inverter, extends the versatility of the PG52 system in synthesis of complex waveforms. It consists of two independent active 4-input 'OR' gates operating at system interface level. Each input/output affords inversion facility.

Input voltage	
Normal	Mark: +5 volts Unmark: Less than +0.5 volt
Invert	Mark: Less than +0.5 volt Unmark: +5V (min)
Level	±20V peak (max)
Impedance	Greater than 5 k ohms
Pulse width	20 ns (min)

PRF	25MHz (max)
Output voltage	
Normal	+10V (approx) if any input is 'marked' 0V (approx) if no input is 'marked'
Invert	0V (approx) if any input is 'marked' +10V (approx) if no input is 'marked'
Impedance	Less than 100 ohms
Load	500 ohms (min) Short-circuit protection
Propagation	Less than 20 ns delay

Trigger module

PG52P10

This is a multi-purpose extension, affording trigger facilities from external signal or internal 50Hz line voltage. A periodic (switched) ÷2 stage provides 1:1 square-wave output at half input frequency. Addition output provides 1.0V pulse into 50 ohms for use as pre-pulse output of conventional pulse generator.

Trigger normal	
Input sensitivity	DC to 20 MHz: 0.5V (p-p) Up to 30 MHz: 1.0V (p-p)
Level range	+5V to -5V
Input voltage	+20V peak (max)
Bandwidth	DC to 30MHz
Impedance	Greater than 10 k ohms
Trigger attenuated (÷ button pressed)	
Input sensitivity	5V (p-p)
Level range	+50V to -50V
Voltage	± 200V peak (max) 100V r.m.s.
Bandwidth	DC to 10MHz
Impedance	Greater than 10 k ohms

Line

Trigger source	Push-button permits trigger from internal supply line in place of external signal via input socket.
Level	Control ranges from 10% to 90% of peak supply waveform (for mid-range sinusoidal supply)
Normal/Invert	Output phase inverted by this facility
Trigger output	2 parallel sockets affording up to 10 volts interface signal output.
Trigger pulse output	
Voltage	1.0V (min)
Impedance	50 ohms (approx)
Width	Variable from less than 25 ns to greater than 200 ns.
Duty-cycle	1:1 (max) not exceeding 20 MHz
Polarity	Positive or negative w.r.t. ground
Rise time	5 ns (approx) Protection against open/short circuit is provided.
Propagation delay	10 ns to 30 ns.

CLIMATIC CHARACTERISTICS

Temperature - operating	0^{o} to $40^{o}C$
- calibration	$20^{o}C$ (approx)
- de-rating	0.1% per ^{o}C

ACCESSORIES SUPPLIED

Terminators TP19	1 each per P3, P4 and P7 module
TP21	1 each per P6 module

Chapter 2

FUNCTIONAL DESCRIPTION

CONTENTS

ILLUSTRATIONS

INTRODUCTION

1. Generator pulse modular CT 578/3 comprises a main frame, PG52B, which provides power supplies and housing facilities for up to 8 plug-in modules. The main frame complement can be chosen from a range of waveform generating, processing and output modules to provide output pulses at repetition frequencies up to 30MHz, pulse widths down to 10ns and amplitudes between 5V and 50V. Signal paths between modules are completed externally via BNC/BNC connectors, all signals being at a common interface level. This method of interconnection also permits the system to be extended by interconnecting the modules housed in two or more main frames.

2. The modules available for installation in a main frame are as follows:

(1)	PG52P1A	Clock generator module
(2)	PG52P2A	Pulse width or delay module (PWD)
(3)	PG52P3A	Standard output module
(4)	PG52P4A	Variable slope module
(5)	PG52P5	Passive summing module
(6)	PG52P6	Power output module
(7)	PG52P7	Fast output module
(8)	PG52P8	Word generator module
(9)	PG52P9	Gate module
(10)	PG52P10	Trigger module

Brief description of modules

3. PG52P1A. The generator pulse swept (clock generator) provides the basic clock rates for the system and covers the frequency range 0.1Hz to 30MHz in free-running externally triggered or gated modes. In the trigger mode the generator may also be triggered manually for single shot applications, or used as an aperiodic ÷ 10 or ÷ 100 count-down. A sweep facility alternatively allows the internal frequency to be controlled over any selected 10:1 range by an external input.

4. PG52P2A (PWD). The variable pulse width generator is normally driven from a clock generator to determine the width of an output pulse, or interposed between the clock generator and another PWD generator to provide a delay between the clock and output pulses. It covers the range 25ns to 1.0s and while it may be driven from a clock or any other system interface signal, the input trigger level can be varied to suit direct operation from other signal sources.

5. PG52P3A. The standard output module provides positive and negative levels of output pulses into 50 ohms with rise and fall times of 5ns (typical). In addition these output pulses may be varied independently over their full range of 0V to 10V (20V p-p). Attenuated ranges allow these levels to be reduced successively from 10V to 100mV. A pulse invert

facility allows both the generation of negative pulses and output duty cycles approaching 100 per cent and the use of two input sockets allows the generation of output pulses from two independent sources.

6. PG52P4A. This is a variable slope output unit which, in addition to the independent 0 to +10V and 0 to -10V output level controls of the P3 module, has rise and fall rates adjustable from 1ns/V to 100ms/V with independent 10:1 controls for the positive and negative going edges. 20V signals can be generated into 50 ohms with any slope from a 2s ramp to a 20ns rise time. This module has dual input and invert facilities similar to the P3A.

7. PG52P5. The PG52P5 contains two independent resistive networks, one with two inputs and the other with three inputs which allow the analogue summation of pulses of different shape, amplitude or offset, but with some attenuation.

8. PG52P6. This module provides positive or negative voltage outputs of up to 50V into 50 ohms. It has an unlimited duty cycle and affords a maximum output power of 50W. This module has built-in power supplies, driven directly through the main frame from the incoming ac supply and offers dual input and invert facilities similar to the P3A module.

9. PG52P7. The PG52P7 provides simultaneous positive and negative output pulses of up to 5V into 50 ohms with rise times of 1ns. A variable delayed-start facility allows the generation of output pulse widths down to 10ns despite the minimum pulse width capability of 25ns of the P2 module. It also has a dual input facility.

10. PG52P8. This module generates pulse patterns of up to 16 bits in length and can operate in a continuous or externally triggered cycle mode. The output can be switched to be in a non-return-to-zero form or, via a P2A module, in a return-to-zero form. A synchronising output signal is provided at the end of the word to allow modules to be encoded to extend the word length beyond 16 bits.

11. PG52P9. This contains two independent four input"OR" gates with the facility to invert any input or output. This flexibility allows the simulation of pulse addition, pulse blanking, set/reset bistables etc. and may be used with advantage in the build-up of complex pulse waveforms.

12. PG52P10. The PG52P10 provides more flexible facilities for triggering the system from external signals or from the internal ac supply frequency. It has a slope and level selection control with a sensitivity of 500mV. In addition to the normal interface signal output this module provides an independent prepulse output of 1V into 50 ohms and enables variations in pulse width from 25ns to 200ns. A further ÷ 2 aperiodic count-down allows the generation of a 1:1 square wave at any frequency within the prescribed range.

Installation constraints

13. With the exception of PG52P6, power output module, each module may be fitted to any position in a main frame.

CAUTION ...

The PG52P6 should only be installed in the right-hand half of a frame due to ventilation problems.

MODULE CONFIGURATIONS (TYPICAL)

14. Provision of all modules as separate units allows them to be interconnected in a large number of configurations, each with a different pulse generating function. The following text describes some typical configurations.

Single pulse generator with delay (Fig. 1)

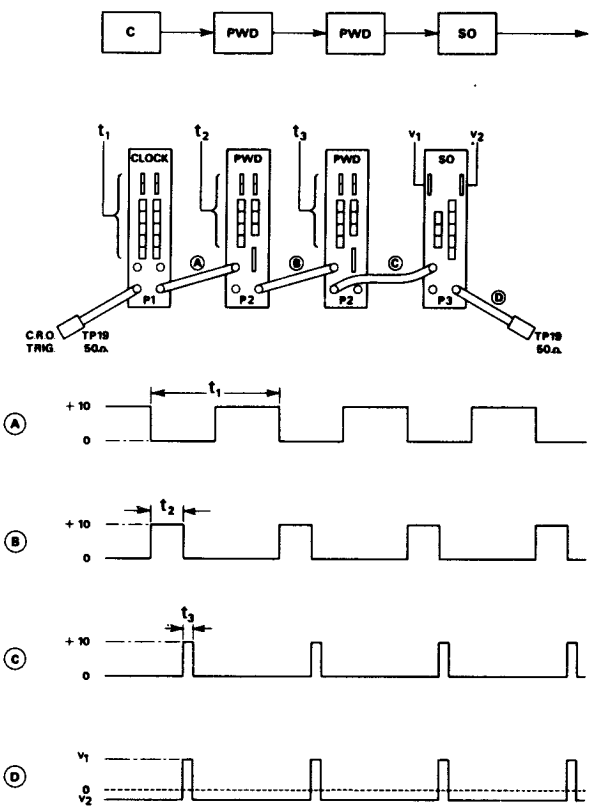

Fig. 1 Single pulse generator with delay

15. This straight forward arrangement is the equivalent of the conventional pulse generator. The generator pulse swept or clock generator, P1A drives through two pulse width generators, P2A modules in cascade into an output unit. These give the frequency, delay, width and amplitude controls respectively of conventional instruments. The standard output, P3A, and variable slope output, P4A, are shown to illustrate the multiple output capability of the system. The power output module, P6, or fast output module, P7, may each be used as output units to match any required application.

16. Waveforms are shown (fig. 1) for normal and inverted outputs, illustrating that positive or negative going pulses of any mark/space ratio can be obtained virtually from zero to infinity duty cycle.

Note ...

The 50 ohms termination, TP19, is shown on the output to emphasise the need for correct termination of the cable if the output waveforms are not to be distorted.

17. The unused output socket from the clock or first PWD module can be used as a prepulse to trigger an oscilloscope. Alternatively the trigger module, P10, may be interposed between the clock and first PWD and used to generate an independent conventional prepulse.

Simple double pulse generator (Fig. 2)

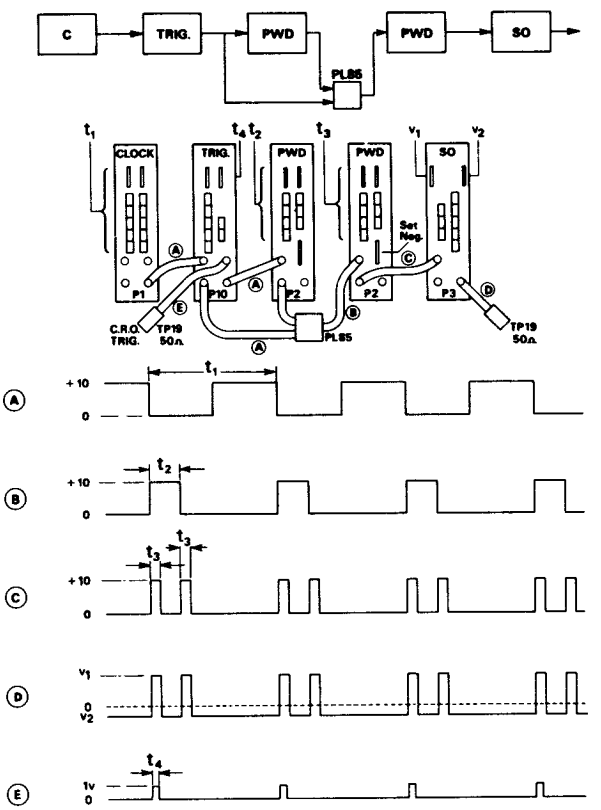

Fig. 2 Simple double pulse generator

18. Trigger module, P10, inserted between the clock and first PWD to provide a conventional pre-pulse or trigger pulse output is shown in Figure 2, (waveform E). This output may be used with any system. Alternatively if a system has to be externally triggered, such an external signal can be fed directly into a PWD module, P2A, with its variable trigger level facility, or, via a trigger module, P10, which affords a more sensitive input than the PWD as well as an inversion facility for selection of trigger from the positive or negative-going input slope.

19. Similarly, this example shows the use of a summing coupler, PL85, to trigger a PWD module, P2, on the negative going transitions of two independent inputs. As in the double pulse facility of most conventional pulse generators, the second PWD (width) is initiated both at the clock period which initiates the first PWD (delay) and at the end of the delay period. Waveform C shows the generation of periods (t3) at both the beginning and the end of the period (t2).

20. The spacing between the two periods (t3) is limited by the necessary recovery time of the generating PWD.

Note ...

> The PL85 is not suitable for use in this application with clock rates greater than 1MHz or with pulse separations less that 200ns.

Double pulse generator with independent width control

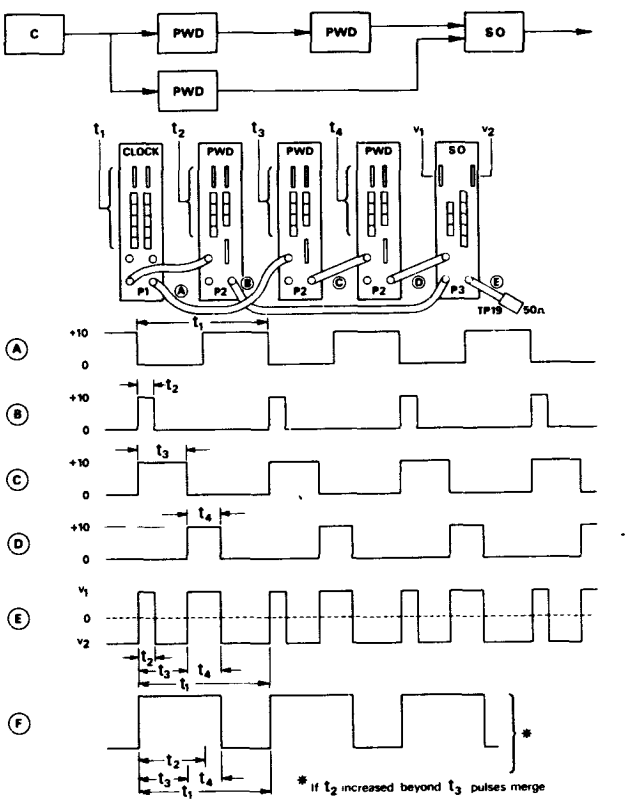

Fig. 3 Double pulse generator with independent width control

21. Figure 3 shows the addition of two output pulses in one standard output module, P3, to form a double pulse generator in which there is no limitation to the period between the two pulses. Note that as t3 is reduced or t2 increased, the pulses can be made to merge.

22. The SELECT INPUT A and B buttons on the output module may be used to remove each input pulse as required.

23. If the overlap capability of the pulses is not required it may be advantageous to drive the input of the second PWD module from the output of the first PWD, (rather than from the clock generator), thus effecting control of the waveform in terms of the first pulse width, the space and the second pulse width without interaction.

Double pulse generator with independent width and amplitude control

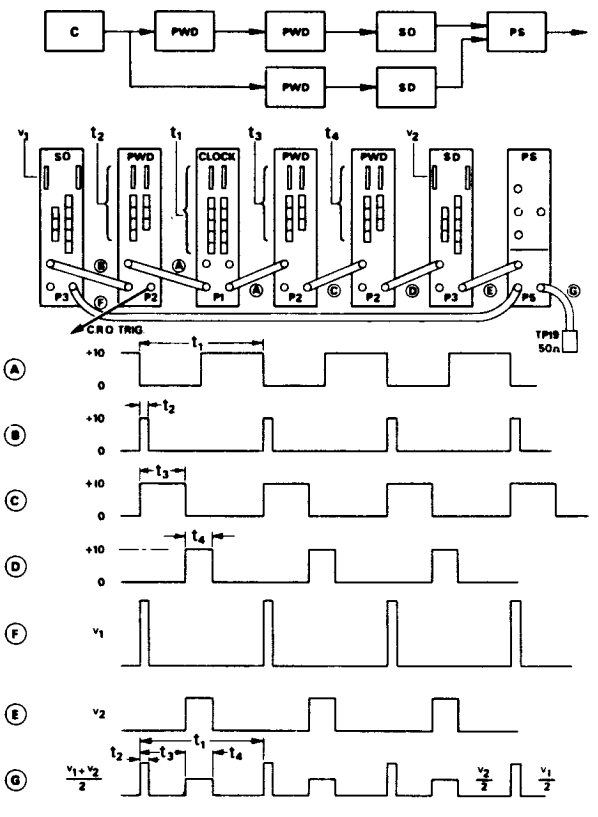

Fig. 4 Double pulse generator with independent width and amplitude control

24. In Figure 4 the use of the passive summing module, P5, to effect a double pulse generator with independent control of the polarity and amplitude of each pulse is illustrated. The clock drives two PWD chains as in Figure 3, but each chain is used independently to drive an output unit, the outputs of which are in turn added in a summing unit.

Note ...

The use of the summing unit limits the maximum output voltage of each pulse to 2.5V into 50 ohms, without affecting the 50 ohms back termination of the summing unit and its inherent 2:1 attenuation.

Note ...

Reducing t3 or increasing t2 will cause one pulse to 'climb' on top of the other as they overlap.

25. A variety of waveforms can be produced in this manner, particularly if P4A variable slope output modules are used. If P4 modules are used, however, they should be fed to the P5A module through a 50 ohm series resistor to maintain the back termination for the P5.

Triple pulse generator

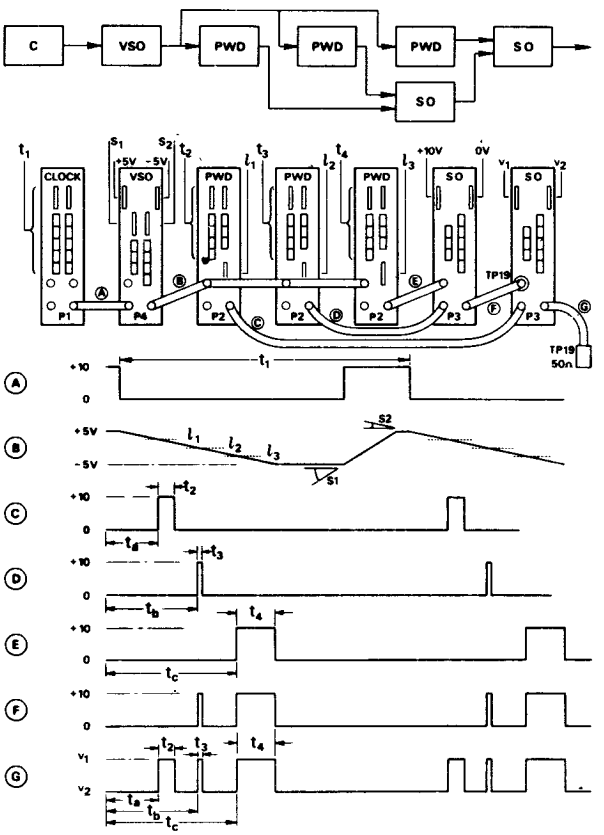

Fig. 5 Triple pulse generator

26. As illustrated in Figure 5, the trigger level controls on the PWD, P2A, determines the time at which the pulse is initiated. A clock drives a variable slope output module, P4A, set to give a negative going ramp from +5V to -5V, which is the trigger level range of the PWD. This ramp signal is fed as the input to 3 PWD units. The trigger level controls of each thus determines the point at which the pulse is initiated. Thus three pulses are generated with independent control of their width and relative position on the ramp. If the ramp slope is altered the relative positions of the three pulses change in proportion. To obtain the three pulses out on one line, one standard output module is used to combine two of them (D and E to F). This is combined with the third pulse C in the final output unit to give the required waveform. This form of combination is necessary because each output module is limited to two inputs.

27. Alternatively, similar triple pulse generation can be obtained using 5 or 6 PWD in the conventional way, extending the techniques given in para. 26.

28. The variable trigger level facility can also be used either to control the trigger point on any slowly varying waveform such as a sine wave, or to avoid spurious multiple pulsing where there is more than one transition through the normal trigger level, due to a ring or other unwanted distortion on a waveform.

Sweep frequency generator

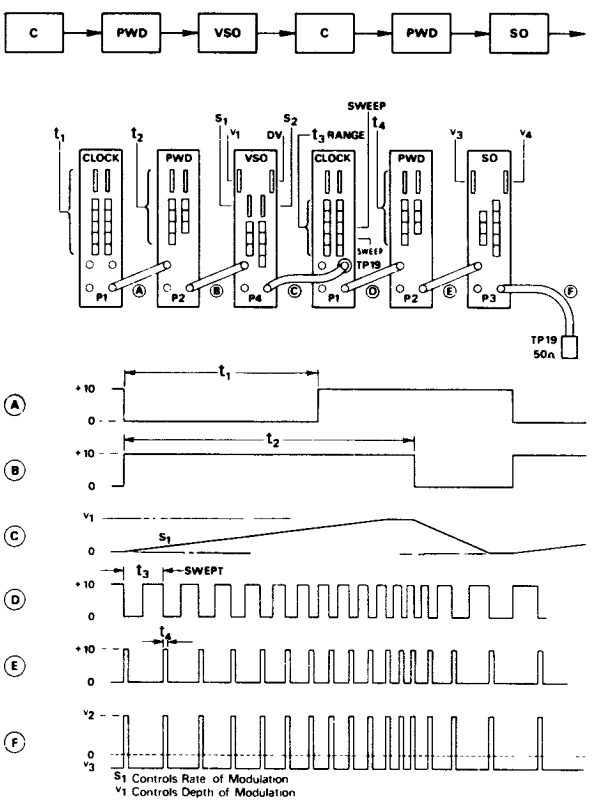

Fig. 6 Sweep frequency generator

29. Figure 6 shows the sweep facility of a clock generator, P1A module. A clock drives through a PWD, P2A into a variable slope output module P4A.

30. The output of this unit is set to be a slowly rising ramp voltage which feeds the sweep input of a second clock. Thus the output signal taken through a second PWD and a standard output module P3A is of pulses of fixed width whose frequency increases and decreases with the slow ramp voltage. The range of frequency modulation is determined by the amplitude of the sweep voltage.

Note ...

Any alternative signal can be used as the sweep input voltage (e.g. a dc line can be used for remote frequency control).

Pulse burst generator

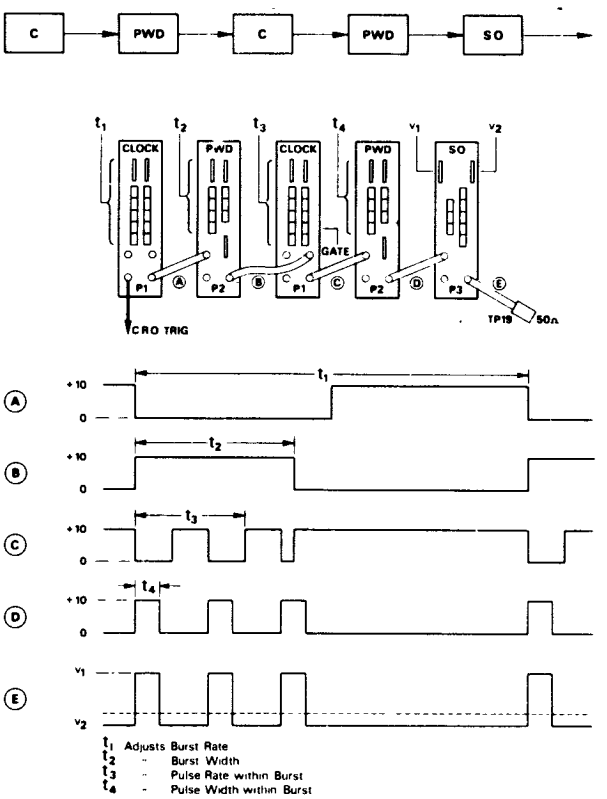

Fig. 7 Pulse burst generator

31. The example shown in Figure 7 uses two clock generator modules, P1A. The first determines the frequency at which bursts occur and drives a PWD, P2A, which in turn determines the duration of the burst by driving the gate input of the second clock, whilst the second clock determines the frequency of pulses within the burst and drives a second PWD, which determines the width of the pulses. The final output is taken from a standard output module, P3A.

32. The clock (and hence the first output pulse in a burst) always starts in synchronism with the application of a gate pulse. At the end of a gate pulse the clock output is clamped positive and cannot generate a spurious output pulse. The clock (not the PWD) is gated, hence output pulses initiated in the PWD are not foreshortened by the closing of the gate pulse. Thus, as the burst period, t2 (or the repetition period within the burst, t3,) is varied, an integral number of complete pulses will be generated, corresponding to the relationship between the two periods.

Note ...

Para. 37 and 38 give an alternative method of deriving the burst period using two PWD modules in place of a clock.

Serial word generator (Fig. 8)

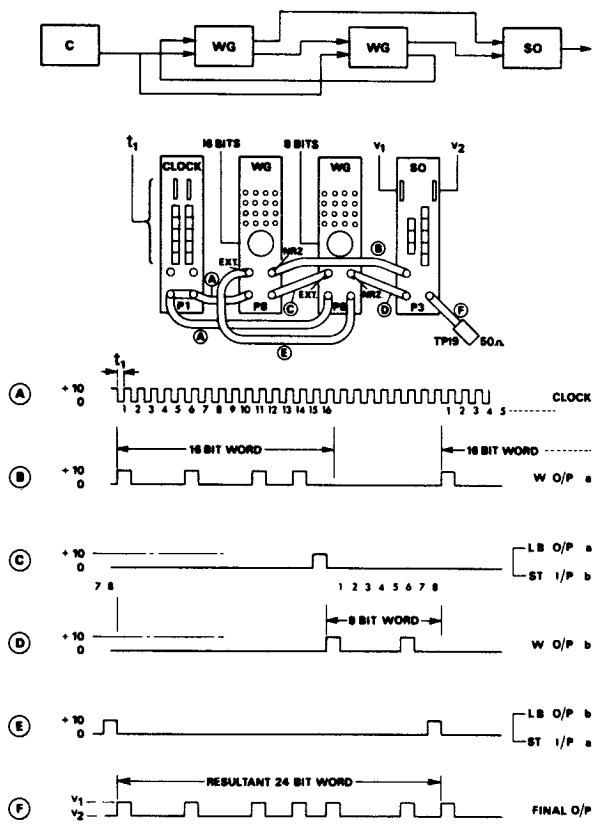

Fig. 8 Serial word generator

33. Word Generator P8, may be driven direct from a clock and fed into an output module to provide a non-return-to-zero waveform, cycling through any required pulse pattern up to 16 bits in length. Alternatively, a return-to-zero waveform may be obtained by inserting a PWD module between the word generator and output modules.

34. Figure 8 illustrates the extension of a non-return-to-zero waveform beyond 16 bits by cascading two word generators, the last bit output of each generator being used to start the other. It may be necessary however, to switch one generator momentarily from external start to initiate or repeat the cycle.

35. A 24 bit word is shown as the sum of 16 bits on one generator with 8 bits on the other but the total could be split in any convenient form (e.g. 12 + 12 bits).

36. The total word length could be extended beyond 32 bits, almost indefinitely by adding more word generators in the chain. Their outputs would then best be summed in a gate module, P9, before feeding an output module. A gate module should also be used (with all used inputs and the output set to invert) to sum R.Z. outputs from two or more word generators, followed by a gate module driving a PWD for the generation of return-to-zero waveforms beyond 16 bits in length.

Word burst generator (Fig. 9)

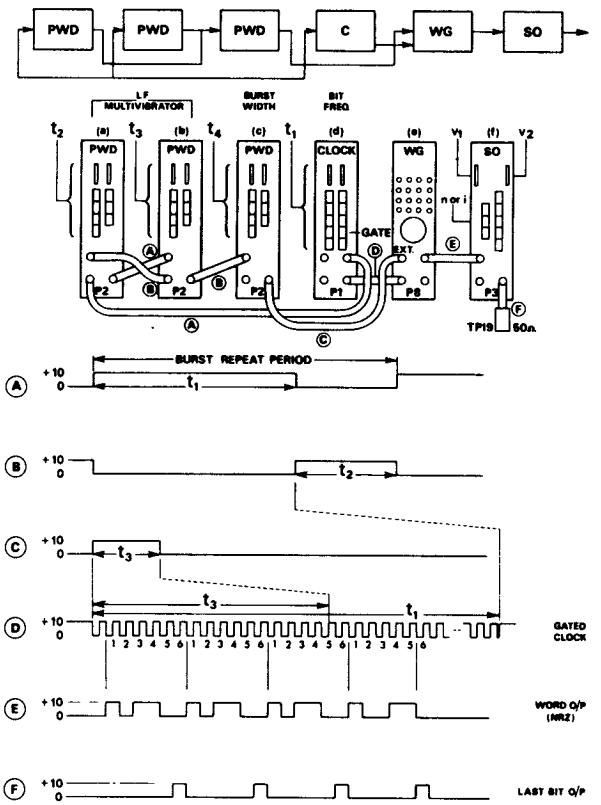

Fig. 9 Word burst generator

37. The use of a dc coupled external start for a word generator module is illustrated in Figure 9, with a clock generator providing a clock signal for the word generator and determining the bit rate.

38. With PWD modules cross-coupled to form a lower frequency multivibrator, thus determining the burst rate, the period between bursts is the sum of the two periods, t1 and t2. The two phases of this multivibrator output, A and B, are used to gate the clock (synchronising the clock pulses to the burst rate) and initiate a further PWD, which in turn determines the period of the word burst (the number of complete words in the burst). Hence the word generator will complete any words initiated during the period t3.

Note ...

If a single word is required at the slower rate, the period t3 may be reduced to less than 1 clock period, or, the external start input to the word generator may be ac coupled internally. In the latter case the third PWD need not be used and the external start taken from A.

Note ...

The technique of cross-coupling two PWD modules to form a multivibrator may be used for many other applications if a clock is not available.

Four-bit parallel word generator

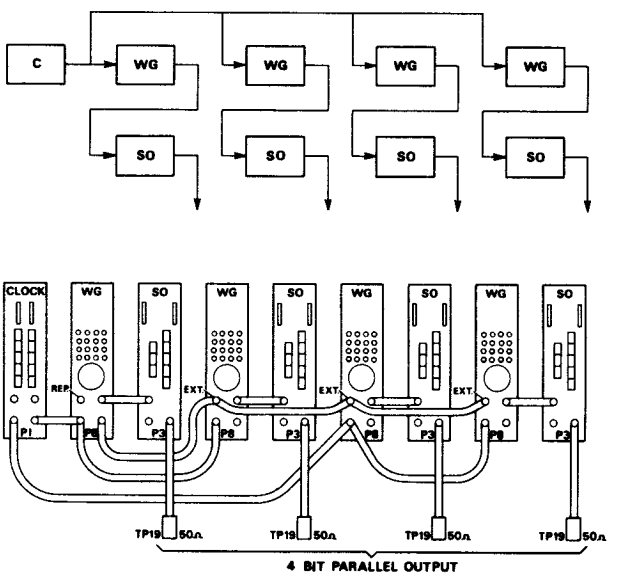

Fig. 10 4 bit parallel word generator

39. As shown in Figure 10, a number of word generators, PG52P8, may be used in parallel to produce a serial sequence of 4 bit parallel words. A common clock signal is fed to all word generators, P8, in parallel. The typical example shown produces a continuous pattern with one generator set to 'repeat' and the last output bit used as 'start' for the other three. All four generators should of course be set to the same word length.

40. Each of the four outputs (Fig. 10) is taken via an output module although this involves the use of more modules than can be accommodated in one main frame. Two frames may be used, with normal front panel interconnection, or another external clock source introduced, or, as another alternative, the word generator interface signals may be used directly if deemed suitable.

41. The illustration shows a system on 'repeat', but it is equally possible to operate all four generators from a common external start signal. Similarly, the RZ output may be used if each word output is fed via a PWD module to the output module. The width of each PWD should be set to the same value.

Trinary state word generator (Fig. 11)

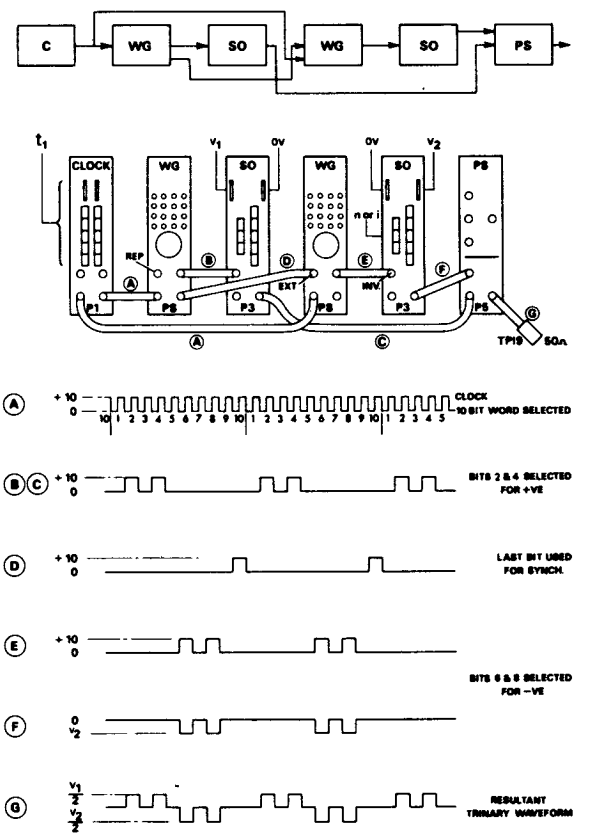

Fig. 11 Trinary state word generator

42. This shows a special application of the operation of two word generators, P8, in parallel to produce a 3-state output word (i.e. the level of each bit can be set as +ve, 0, or -ve). Both generators are set to the same word length and the last bit output of the one, operating in its repeat mode, is used as the 'start' of the other, so that the two operate in synchronism. For this purpose the word output of the one is taken directly through an output module with the output levels set to give a +ve pulse. The word output of the other is then taken via another output module, set to invert, with the output levels set for a negative pulse. By adding the two resultant output signals in a passive summing unit, P5, the state of each pulse position in the word can be set as follows:

(1) +ve - by setting the appropriate toggle switch on the first P8 module for a 'mark' (bits 2 and 4).

(2) OV - by setting neither toggle switch to 'mark' (or by setting both to mark).

(3) -ve - by setting the appropriate toggle switch on the second P8 module to 'mark' (bits 6 and 8).

Count down facilities

43. If very slow clock rates are required, it is possible to feed one clock into a second which is on its 'trigger divide' mode. This allows the 10 second repetition period of the first clock module to be extended to 100 or 1000 seconds, and further clock modules can be cascaded to extend the period further.

44. When required to synchronise a system to an external signal, it is often better to feed the signal directly into a PWD module rather than as trigger into a clock generator module in that the PWD has the variable trigger level facility and can also be set to a periodic count-down of any number up to 10. For further division (10 or 100) the output of the PWD can be fed to a clock module set to the 'trigger divide' function, thus enabling overall periodic division ratios of 20, 30, 40-90, 100, 200, 300-900 and 1000 to be obtained.

45. If the 50Hz supply (isolated and stepped down to a suitable voltage) is used as the trigger input, count down facilities may be used to derive slow clock rates with the accuracy of the supply frequency, e.g. a PWD set to 90ms approx. will count-down by 5 and, followed by a clock on ÷ 10, will give a reasonably accurate 1 second clock. Alternatively a second PWD, following the first but set to 550ms (approx), will divide by a further 6 and, if this is followed by a clock on ÷ 100, an overall ratio of 3,000 can be obtained, (i.e. one pulse per minute).

46. Similar techniques may be used at higher frequencies to derive periods based on an external crystal standard frequency.

Long delay periods (Fig. 12)

47. The maximum width or delay period which can be generated from a PWD module is 1 second, but this limit may be extended almost indefinitely with the arrangement shown in Figure 12.

48. The basic system which allows generated periods up to 8 seconds, requires a PL85 summing coupler, a P9 gate module and a P1A clock module. With the gate module cross-connected and switched as shown (fig. 12) to form a set/reset bistable, and a positive start signal applied directly at B or, (if necessary) generated from a negative going transition into a PWD module as shown, the bistable will be reversed, thus sending C high and gating the clock on. Output D of the clock, originally positive, will fall for a period corresponding with the clock rate setting (up to 8 seconds), i.e. the first part of the normal 4:1 mark-space output cycle on the low frequency ranges.

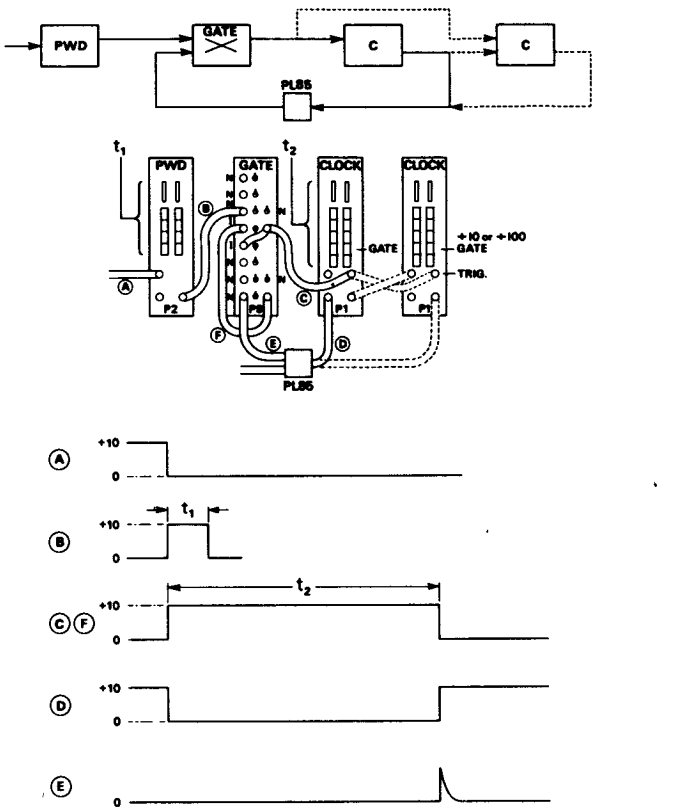

Fig. 12 Long delay periods

49. The positive transition at the end of the 8 second period will then be differentiated by the PL85 coupler to reset the bistable and hold the system locked off, until the next start signal is applied.

Note ...

PL85 is not used in the conventional mode. The signal from the clock is applied to the output lead while the gate is driven from the input lead, thus allowing a positive transition to be passed by the internal diode and capacitor coupling rather than the normal negative going transition which is used to trigger a PWD. The 8 second output can either be taken from the clock or from either side of the bistable, as required.

50. For periods longer than 8 seconds, the output of the first clock is used to drive a second clock which is set to external trigger and divide by 10 or 100. This is also gated by the bistable and the PL85 is driven from this second clock instead of the first. Thus the first clock is allowed to run for 8 or 80 cycles, each of which can be of 10 seconds duration, generating periods of 80 or 800 seconds.

Chapter 3

CIRCUIT DESCRIPTION

CONTENTS

ILLUSTRATIONS

MAIN FRAME PG52B (Fig. 3)

1. The PG52B main frame contains the power supply circuits and sockets which distribute the supplies to the 8 module positions.

2. The series/parallel primary windings of the supply transformer, T1, are fed from the incoming supply through the ON/OFF switch, S1, fuses FS1 and FS7, and the supply RANGE SWITCH, S2, which facilitates connection of the two windings in series for use on 200V/260V supplies or in parallel for 100V/130V supplies. The two 26V secondary windings drive similar rectifier and stabiliser circuits, the outputs of which are linked to give +20V and -20V lines. A 12V secondary winding similarly rectified and smoothed provides the +5V line, whilst a further 50V winding provides an ac supply to all 8 module positions.

DC power supply circuits

3. The +20V circuit is based on bridge rectifier D7 with its reservoir capacitor C1 and associated discharge resistor, R21. The unstabilised dc voltage across C1 is fed through fuse FS2 to the stabiliser circuit which is mounted on a printed circuit board. The voltage across zener diode D5 is compared at the base-emitter junction of TR5 with a proportion of the output voltage determined by R5, R28 and R19. Any inequality is amplified by TR5 and transferred through emitter follower TR3 to control the conduction level of the series regulator TR7, which is mounted on the rear panel for heat dissipation purposes. TR1, with D1 and R3, provides a high impedance current source to feed TR5 and D5 so giving TR5 a high voltage gain. R28 is used to set the output voltage to +20V and C3 provides a low output impedance to the rapid changes of load current imposed by the modules.

4. Overload protection is provided by TR1 and D3 which samples the voltage developed across R9 by the output current. If output current exceeds 2A, diode D3 conducts and cuts off TR1 so reducing the output voltage. This action protects TR7 against heavy peak overload currents of short duration which would not blow FS2.

5. The -20V and +5V stabiliser circuits are similar to the +20V circuit described in para. 3 and 4. The positive side of the -20V supply is linked to the negative side of the +20V supply as the common 0V point. The negative side of the +5V supply (0V, 5) is linked to this 0V point via R58. In order to reduce common earth return paths, the two 0V lines are only connected directly together within a module.

Supply distribution

6. Terminal board TB1, mounted behind the 8 sockets SKA to SKH acts as a star point from which the sockets are fed. C5, C6, C11 and C12 decouple the supplies at this point and prevent interaction between the individual modules.

7. The incoming ac supply is also distributed through separate fuses, FS4 and FS6, and the terminal block, TB2 to SKE, SKF, SKG and SKH. This is for use in the Power Module, P6, which has its own power supplies. It is linked from TB2 to SKH and fuse links are fitted in FS4 and FS6 only when required.

8. A fan with its dual windings connected across the primary windings of T1, is used to increase ventilation and prevent the instrument from overheating on full load.

CLOCK GENERATOR MODULE PG52P1A (Fig. 4)

9. This module provides the basic clock rates between 0.1Hz and 30MHz for the PG52 Modular Pulse Generator system. Free running, externally triggered or gated modes of operation are provided. The trigger mode can be used as an aperiodic ÷10 or ÷100 divider or initiated manually for single shot applications. A sweep facility alternatively allows the internal frequency to be controlled over any selected 10:1 range by an external input voltage.

Multivibrator and dividers

10. The basic clock generator consists of an emitter-coupled multivibrator, TR107 and TR108, whose frequency can be controlled over a 10:1 range by amplitude control of the emitter excursion and in decade steps by the value of capacitor switched into circuit. Fixed capacitor C110 and trimmer capacitor C131 are the timing components on the MHz x 10 range, all other capacitors being disconnected. The excursion of TR107 collector voltage is limited between +6.2V (defined by D118 through D114) and the output of the emitter follower TR106 applied via D112. As the wiper of the fine control potentiometer R160 is taken more positive, its potential is transferred through TR105 and TR106, so increasing the multivibrator frequency.

11. As the MHz x 1 and MHz x 0.1 and kHz x 10 ranges are selected, C116, C117 and C118 are added to the timing components so reducing the frequency accordingly. On the kHz x 10 and all faster ranges the multivibrator output from TR109 is fed directly via S104a and S108a to the output amplifier. However, on the kHz x 1 and kHz x 0.1 ranges, C118 remains in circuit holding the frequency of the multivibrator at 10kHz while S108a directs its output signal through one or both of the decade dividers, IC101 and IC102, giving the required frequency at the output. Each complete decade divider is an integrated circuit in one dual-in-line package and is followed by an output buffer emitter follower, TR110 or TR111.

12. Similarly on the Hz ranges, S106a switches C119 into circuit defining the frequency of the multivibrator in the 10Hz range while the decade dividers are switched into circuit to give outputs of 1Hz and 0.1Hz. Although the output of the multivibrator is an approximate square wave, the output of the decade dividers has a 1:4 mark/space ratio. Thus the output of the module is 1:1 on the MHz x 10, MHz x 1, MHz x 0.1, kHz x 10 and Hz x 10 ranges, and 1:4 on the other ranges.

13. R161, R162 and R163 are switched into circuit on the MHz, kHz and Hz ranges respectively to give fine control of the emitter current of TR107 and TR108, thus acting as calibration presets for those ranges.

Output stage

14. The signal from the multivibrator or the decade dividers is fed via S104b to the emitter-coupled pair, TR114 and TR115 and the output from the collector of TR115 is fed through the zener diode, D122, to operate TR117 as a saturated switch. The 0 to +10V collector voltage swing of this stage

is buffered by the emitter followers TR118 and TR119 which provide a low output impedance drive to the two output sockets, SKC and SKD. TR118 and TR119 are protected against accidental short circuit of the output by R153, R155, R156 and R157.

Sweep

15. When SWEEP is selected, S102 connects the gate/sweep input socket SKA in place of the fine control potentiometer, R160. This allows the sweep input signal to control the multivibrator frequency over the frequency range selected by the push buttons. D104, D105 and D106 with R103 protect the circuitry against excessive input signals.

Gate

16. When the gate function is selected, S101 operates and if the input signal on SKA is positive the transistor switch TR104 is turned on. D111 is therefore reverse biased and the circuit operates normally.

17. When the input signal drops to 0V, TR104 is turned off and its collector potential rises. D111 therefore conducts and reverse biases D110 so taking the multivibrator control voltage on the emitter of TR106 more positive than the potential of D118. Multivibrator TR107/TR108 is then inhibited.

18. The positive signal on the collector of TR104 is also transferred through the emitter of TR116 to the base of TR115. This action turns off TR115 irrespective of the base potential on TR114 and the output voltage is thus clamped at its positive level.

19. The final effect of turning off TR104 is to turn on TR112 momentarily through C112. The resulting negative-going pulse at TR112 collector is transferred through C123 to give a short positive pulse at the collector of TR113. This pulse resets both decade dividers to their '0' state.

20. When the gate is opened by returning the input signal positive, TR104 is turned on again. This removes the clamp from the multivibrator and from the output stage and allows normal operation to start in synchronism with the gate signal.

Trigger

21. When TRIGGER is selected, S104a disconnects the output of the multivibrator and connects in its place the output of a separate Schmitt trigger circuit formed by TR101 and TR102. This circuit can be driven either by an input signal on SKB or in a 'single shot' mode by the push button, S103.

PULSE WIDTH OR DELAY MODULE PG52P2A (Fig. 5)

22. The variable pulse width generator module is used within the PG52B system to determine the width of output pulses or the delay between one event and another. The module covers the range 25ns to 1 second and while it is mainly intended to be driven from other modules in the system, the input trigger level can be adjusted to allow the module to trigger as required from a variety of waveforms from other signal sources.

Variable level trigger circuit

23. This comprises the long-tailed pair, TR201 and TR202, driven from the current source, TR203. The input signal is applied directly to the base of TR201 while the base potential of TR202 is set by the trigger level control potentiometer, R246. TR202 is switched when the level of input signal applied from TR201 collector via R207 and C204 exceeds the potential established at TR202 base by R246. The output from TR202 collector drives TR204 which produces a 10 volt step. This step is differentiated by C208 to provide a trigger for the variable period monostable circuit TR205 and TR206.

Variable period monostable circuit

24. This circuit consists of a long-tailed pair, TR205 and TR206 with a capacitive feedback path from the collector of TR205 to the base of TR206. The appropriate timing capacitor (C212 to C221 inclusive) is connected via the double emitter follower, TR207 and TR208 and selected by S201 to S208. Charging current is fed to the capacitor from TR209 which is controlled by the variable period control, R245. The circuit is triggered from the positive spike produced by the variable trigger level circuit and applied to the base of TR205.

25. Normally conducting transistor TR205 is turned off when a positive going trigger edge from TR204 is applied via C208. The resultant negative step on the collector of TR205 is transferred through the selected timing capacitor to the base of TR206 which turns on and holds TR205 off. Diode D204 is reverse biased and the timing capacitor charges at a rate determined by the current source, TR209 whose base is connected via S201 to S208 to the preset calibration potentiometers R240 to R244. The current is variable over a ten to one range, the actual value being set by R245 (the fine period control).

26. As the selected timing capacitor charges, the base potential of TR206 rises until it reaches a point where TR206 is cut off. This turns on TR205 and the timing capacitor is rapidly discharged through D204 ready for the next trigger pulse.

27. The range of width is selected by S201 to S208. As the width is increased, larger values of capacitor are switched in cumulatively, i.e. in many cases the capacitor for one range is in parallel with those for smaller ranges. The capacitors switched in for any given range are as follows:

RANGE	SELECTED CAPACITORS
100ns	C212, C213 (AOT)
1µs	C212, C213, C214 and C215 (AOT)
10µs	C212 to C216
100µs	C212 to C217
1ms	C212 to C215 & C219
10ms	C212 to C216, C218 & C219
100ms	C212 to C220
1 s	C212 to C217 & C221

28. The preset control potentiometers, R240 to R244, set the maximum width on the 100µs to 1 second ranges respectively. Trimmer, C212, sets the maximum width on the 100ns range while the capacitors C214 with C215, C216 and C217 are matched to within ±2% so that adjustment of R240 on the 100µs range brings the 'µs' range within specifications.

Output stage

29. The output of the monostable is directly coupled through TR221 to the output emitter followers, TR212 and TR213. Transistor TR210 is ac coupled to the drive and turns on only for a short period to speed up the turn-off edge of TR211.

30. The output emitter followers provide a low output impedance and are protected by R234 to R237 against damage from accidental short circuiting of the output. Zener diode D209 and the emitter follower TR214 produce a +11 volt line to drive the input and output circuits and bias the monostable.

STANDARD OUTPUT MODULE PG52P3A (Fig. 6)

31. The P3A output module provides an output into 50 ohms with rise and fall times typically 5ns. The positive and negative levels of the output pulse may be varied independently over the range 0 to +10V and 0 to -10V respectively, i.e. 20V peak to peak but attenuated ranges allow these levels to be reduced successively from 10V to 100mV. A pulse invert facility allows both the generation of negative pulses and output duty cycles approaching 100%. The two input sockets allow the generation of output pulses from two independent sources.

Input switching

32. The A and B input signals drive saturated switches TR302 and TR303 such that a positive input to either will rapidly switch the common collector point from +20V to 0V. Input pulses are also coupled via C301 and C302 and the negative-going edges of these pulses turn on TR301 for a short period. This action ensures that the common collector point of TR302 and TR303 rapidly returns to +20V at the end of an input pulse.

33. The resultant signal from the common collector point is fed directly (in the normal mode) or via an inverting stage, TR304 and TR305, (in the INVERT mode) to a complementary emitter follower stage, TR306 and TR307. The output from TR306/TR307 is in turn level shifted by the zener diodes, D306 and D307 to drive the complementary saturated switch pair, TR308 and TR310. TR308 provides a constant current load for the level-shift network.

Level control and output

34. The emitter potential of TR309 can be controlled between approximate limits of 0V and +10V on the +V line by the positive level control. Similarly, the emitter potential of TR310 can be controlled between 0V and -10V on the -V line by the negative level control. Thus the common collector of TR309 and TR310 is rapidly driven between +V and -V when the transistors are switched. The base biasing is so arranged that always one but never both of the pair is on at any one time. D312 provides a small bias to the double emitter follower output pair, TR311 and TR312, with their common emitter junction being switched either directly or through the attenuator network, to the output socket.

Power supplies

35. The +V line is generated by the cascaded emitter followers, TR314 and TR313 from the wiper potential of the positive level control, R350. The -V line is similarly generated by TR315 and TR316 from the wiper potential of R352. Preset controls R349 and R351 set the maximum output voltages to +10V and -10V respectively.

VARIABLE SLOPE OUTPUT MODULE PG52P4A (Fig. 7)

36. The variable slope output module provides an output into 50 ohms with variable rise and fall times. The positive and negative levels of the output waveform may be varied independently over the range 0 to +10V and 0 to -10V respectively, i.e. 20V peak to peak while linear rise and fall slopes may be varied from 1ns/V to 100ms/V with independent 10:1 control on each slope. A 'pulse invert' facility allows both the generation of negative-going pulses and a duty cycle approaching 100%. Two input sockets allow the generation of output pulses from two independent sources.

37. The circuit functions as an 'OR' input gate and invert circuit controlling a complementary pair of current sources which either charge or discharge a timing capacitor at a controlled rate. The voltage swing on this capacitor is limited by catching diodes to variable positive and negative supply lines which control the amplitude of the pulse. An output stage acts as an impedance converter to transfer the voltage across the timing capacitor to the output socket at a low output impedance.

Input switching

38. The A and B input signals drive saturated switches TR402 and TR403 so that a positive input on either rapidly switches the common collector point from +20V to 0V. Input pulses are also coupled via C401 and C402 and the negative-going edges of these pulses turn on TR401 for a short period, giving rapid return of the common collector point to +20V at the end of an input edge.

39. The resultant signal from this common collector point is fed directly (in the normal mode) or via a similar inverting stage, TR404, TR406 and TR407. This output is in turn level shifted by the zener diode D406 to TR408 and TR409.

Waveform generation

40. TR410 and TR411 act as current sources taking positive and negative currents respectively from their common collector point. The current in each transistor is determined by the fine slope controls R452 and R453.

41. When TR408 is conducting R452 is switched into circuit to reverse bias TR401 so cutting it off as a positive current generator. TR409 is turned off at this time and TR411 conducts at a current level determined mainly by R453 and D412. D414 clamps the collector potential of TR411 (i.e. the voltage across the selected timing capacitor C413 to C412) at the -V line potential.

42. When the input signal is reversed, TR408 is turned off and TR409 turned on. TR411 is biased off by R430 and TR410 conducts at a positive current determined mainly by R452 and D409. The potential across the selected capacitor rises at a rate determined by the capacitor value and the defined positive current until it is clamped at the +V line by D413. When the input returns to its initial condition, TR410 is again turned off and TR411 turned on. The potential across the timing capacitor drops linearly under the control of the negative current in TR411 until it is again clamped by D414.

43. As the slope is changed on the selector switches, S401, S402, S404 and S407, the timing capacitors are switched in parallel as follows:

RANGE	SWITCH OPERATED	CAPACITORS
1-10ns/V	S401, S406	C413
10-100ns/V	S401, S405	C413, C414
0.001-1ms/V	S402, S407	C413, C415
1-10ms/V	S402, S406	C413, C416
10-100ms/V	S402, S405	C413, C417
0.1-1ms/V	S403, S407	C413, C418
1-10ms/V	S403, S406	C413, C419
10-100ms/V	S403, S405	C413, C420
		C421

Output stage

44. The voltage across the selected timing capacitor has the required slope and amplitude and is buffered by the output stage, TR412 and TR413. TR414 and TR415 form a complementary network of cascaded emitter followers driving the output socket, SK403.

Note ...

Provision is made in the unit to include a 50 ohm resistor in series with the output (R473 in parallel with R461) which can be by-passed by S408. However, these components are not normally fitted and the junction of R447 and R448 is connected directly to the output socket, SK403.

Power supplies

45. The +V and -V lines are controlled up to approximately +11V and -11V by the positive and negative level controls, R464 and R465. The potential on the wiper of R464 is coupled via the cascaded emitter followers, TR417 and TR416, to define the +V line with preset, R474, (set +10V) being used to set the maximum level and R450 (set +0V) the minimum level. If the output current exceeds 200mA the output protection circuit operates, the voltage across R454 then being sufficient to bring TR420 into conduction. This in turn brings TR421 into conduction so reducing the wiper potential of R464 and hence the output voltage. The output current is thus limited in the event of short circuits or low impedance loads. The -V line is controlled in a similar way from R465 through emitter followers, TR419 and TR418.

TR423 and TR422 form the current limiting circuit while presets, R466 (set -10V) and R449 (set -0V), set the control range.

PASSIVE SUMMING MODULE PG52P5 (Fig. 1)

46. The PG52P5 module contains two independent resistive networks which may be used singly or in combination to sum a number of inputs from 50 ohm sources onto a single 50 ohm output. By this means, complex waveshapes may be built up from separate pulses, sinewaves or other waveforms. Alternatively, the networks may be used as power dividers to split a single input from one 50 ohm source into a number of 50 ohm outputs. When used in this mode, the output signals are one half or one third of the applied input signal level depending on which network is being used.

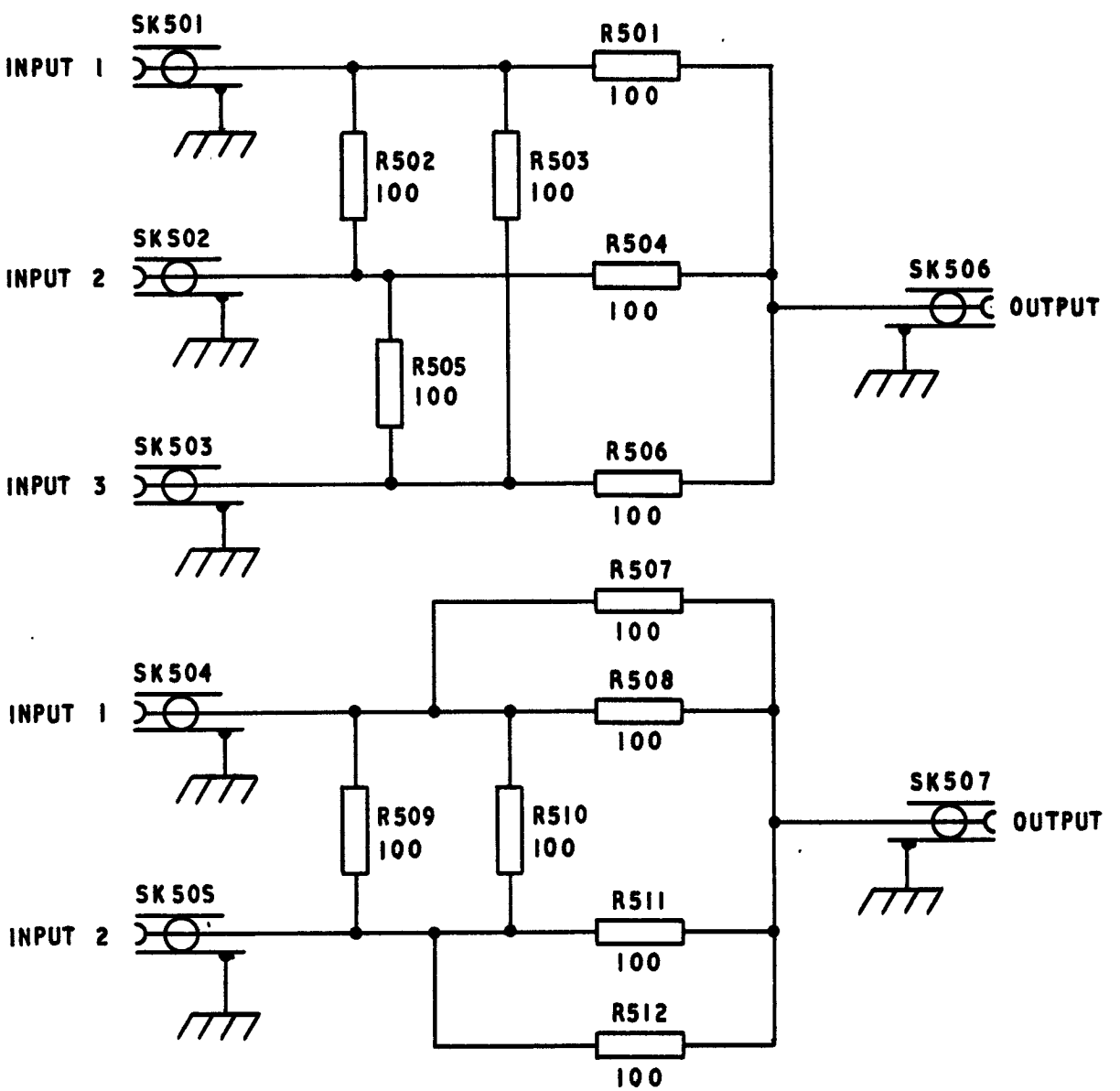

Fig. 1 PG52P5: circuit diagram

POWER OUTPUT MODULE PG52P6 (Fig. 8)

47. The PG52P6 module provides a positive or negative output of up to 50V into 50 ohms and has an unlimited duty cycle giving a maximum output power capability of 50W. A dual input facility allows the generation of output pulses from independent sources while an invert facility overcomes any duty cycle limitation of these inputs.

48. The module contains its own floating internal power supplies which can be connected to give either a positive or a negative output by grounding the appropriate output supply line. The level of output voltage can be varied between 10V and 50V by means of the SET OUTPUT LEVEL control.

49. The circuit is described in three sections, as follows:

(1) Input circuitry and slave bistable.

(2) Drive and output circuitry.

(3) Power supply and protection circuitry.

Input and slave bistable circuits

50. This part of the circuit is driven at the system interface level (+10V) which is referred to ground and to the +20 and -20 volt lines. The input sockets are connected to the bases of transistors TR601 and TR602, with diodes D601 and D604 providing protection against excessive input excursions. The input transistors are connected as a parallel gate and form one half of an emitter-coupled long-tailed network with transistor TR603.

51. The differential output from the circuit is coupled by C604 and C605 into the primary windings of transformers T602 and T603 and the resulting secondary voltages comprising sharp differentiated spikes (due to the time constant of the transformer and associated coupling capacitor) are fed via the polarity and inversion switches, S603 and S602, to the slave bistable TR610/TR614. The bistable is referred to 0V (the positive side of the 50V output supply) while the input signals are referenced to ground (the 0V and chassis of the system).

52. The bistable circuit is controlled by the pulses received through diodes D606 and D609 from the input stage, the set and reset state being determined by the polarity and inversion selection switches. TR612 and TR613 act as pull-up switches in the collectors of TR610 and TR614 respectively. The output from the bistable is coupled through R636 to the buffer and driver stages.

Buffer and driver circuits

53. The 0 to +12V pulse generated by the slave bistable passes through the complementary emitter follower pair, TR615 and TR616 to the complementary switches TR617 and TR618. Diodes D618, D619 and D623 bias the emitters of this pair so that only one of the pair is turned on at any time. The purpose of this circuit is to speed up the rise and fall times of the waveform applied to the second complementary emitter follower, TR619/TR620.

54. The low impedance pulse output from TR619/TR620 is level shifted by the zener diode D624 to give a signal switching between +5V and -5V approximately to drive the output switching transistor, TR621. TR623 supplies a constant current through D624, independent of changes in the 10V to 50V output supply due to variation of the SET LEVEL CONTROL.

55. The collector current of TR621 is supplied by a constant current source, TR624. TR621 collector voltage thus swings from 0V (in its 'on' state) towards -62V (in its 'off' state), until it is caught at -50V by diode D636. Transistor TR622 turns on only during positive-going transitions of the input pulse and is included to speed up the negative-going transition at TR621 collector as it turns off. The amplitude of the pulses at the collectors of transistors TR621 and TR622 is approximately five volts greater than the output level set by the SET LEVEL CONTROL, R612 i.e. a maximum level of some 62 volts, the range of control of the 50V output supply being from 12V to 61V.

56. The output circuit is formed by the complementary emitter follower, TR625/TR626 and six transistors, TR627 to TR632, connected as three parallel complementary emitter-follower pairs with current sharing resistors in each emitter. The resultant low impedance output which follows the waveform generated on the collector of TR627 is taken to the output socket, SKC. Diodes D643 and D644 clip transient reflections in mismatched output cables.

Output polarity and invert switching

57. The polarity of the output pulse is determined by S604 which grounds either the negative or positive side of the 50V output supply. This part of the polarity switch is mechanically linked to the front panel polarity switch S602 of which, sections S602a and S602b determine the phase of the output pulse in relation to the input pulse and provide the necessary inversion with polarity. The INVERT switch, S603, reverses the connection between the coupling transformers and slave bistable.

Power supply circuit

58. Apart from the input circuitry which operates from +20V and -20V supplies of the main frame, the module operates from a number of self generated, stabilised supply lines as follows:

(1) The output supply (variable between 10V and 50V), the positive side of which is referred to as the 0V line and the negative as the -50V line. There is also a -51V line, approximately 1V more negative than the -50V line.

(2) +12V and -5V lines with respect to 0V, i.e. the positive side of the variable output supply.

(3) -62V which is -12V with respect to -50V (the negative side of the variable output supply).

59. These supplies are derived from supply transformer, T601, fed from the input supply via the AUX. fuse in the mainframe and picked up on the rear connector, PLA. The line connection is fused by FS601 fitted before the input supply range selector switch, S601, in the transformer primary. The transformer has three independent secondaries which are rectified by full wave bridges, D601 to D603, and smoothed by capacitors, C644, C645 and C646, to give dc voltages of approximately 20 volts, 80 volts and 20 volts respectively. The output from bridge, D601 is connected via FS602 to a stabiliser circuit for the -12 volt and -5 volt lines.

60. The +12V line is obtained by driving zener diode, D629, from the current source transistor TR633 and using the 13V (approx.) zener-stabilised potential to provide the base voltage for the compound emitter follower arrangement TR635 and TR634. The output from the emitter of TR634 is then stabilised at approximately +12 volts above the 'OV' line. Most of the return current from this line and D629 flows through a second zener diode, D630, giving a further -5 volt line, with respect to OV. The +12V and -5V lines are used to feed both the slave bistable and associated buffer circuitry in the signal path and the stabiliser circuit for the 50V supply.

61. The 80V output from D602 is taken via FS603 to the stabiliser circuit of the 50 volt stabilised line referenced by zener diode D642. The resistor chain, R660, R619, R612, R633 and R622 acts as a potential divider between this reference and the -50V line. The potential at the junction of R619 and R612 is compared with OV by the long tailed pair, TR641 and TR642 and any difference is amplified by TR642 to provide a control voltage coupled via emitter follower TR606 to the series regulator, TR636.

62. If the -50V line is too negative, the base potential of TR641 is negative. Current is diverted from TR641 to TR642, the collector potential of TR642 goes further negative and this change is transferred through TR606 to reduce the conduction through TR636. The increase in collector-emitter voltage of TR636 shifts the whole of the unstabilised supply across C465 more positive with respect to OV hence sending the -50V line more positive and correcting the original error.

63. With the base of TR641 stabilised at OV, D642 drives a constant current of 10mA through R660, R619, R612, R663 and R662. R612 is the SET OUTPUT LEVEL control and is used to vary the output supply and hence the output pulse amplitude over the range 10 to 50V. R660 adjusts the current in the divider chain setting the pulse output to 50V at the calibrated point near the maximum end of R612 control range. The output voltage at the minimum end of the control range is set to 10V by adjustment of R662.

64. The total range of control of the 50V output supply is from approximately 12 volts to approximately 61V which, allowing for losses of voltage through the various components in the output stage, provides the over-range capability of 60V e.m.f. There is an approximate 1V difference in output stage loss between positive and negative outputs and this is overcome by the introduction of R620 and A.O.T. resistor R621 into the potential divider of the stabiliser circuit in the positive output mode only.

65. The control loop responds rapidly to increases of load current as TR636 turns on. The cascaded emitter follower pair, TR607 and TR637, complement TR606 and TR636 and conduct only to prevent any transient increase in output voltage when the load current is reduced.

66. The stabilised -50V line potential is used to define the voltage swing at the collector of TR612. The return current from this line is passed through D647 to generate a line approximately 1V more negative, -51V. The collectors of TR628, TR630 and TR632 output stage, are returned to this line and the additional negative bias avoids zero or forward bias of their collector base junctions.

Protection circuits

67. To prevent damage to the power supply or output transistors due to excessive input frequency or output loading, three forms of protection circuitry are included as follows:

(1) A mean current limit in the 50V stabiliser circuit.

(2) A peak current trip on the output line.

(3) An output frequency limiter.

68. The mean current limit is an integral part of the 50V stabiliser circuit. The emitter current of the series regulator transistor, TR636, flows through the current detector resistor, R652. As this current increases the potential at the junction of D632 and R650 rises and when this overcomes the negative bias introduced by R651 and R655, TR638 conducts. The collector potential of TR638 thus falls and the emitter follower TR639 transfers this change to over-ride the stabilising output of TR642 and reduce the stabilised supply voltage. R655 with preset R654 is returned to the stabilised voltage and the bias it introduces to the base of TR638 decreases as the line voltage decreases. Thus the current limit is reduced as the supply is reduced so giving a re-entrant characteristic to the stabiliser. The circuit will supply approximately 1A at 50V but only slightly more than 0.5A at 25V. The power supply output collapses if a load of less than 50 ohms is applied. Once an overload is removed the time constant of C648 with R656 and R657 limits the rate of recovery of the supply voltage.

69. The response times of the stabiliser as a whole and the current overload circuit in particular, are much slower than the switching time of the output stage. Decoupling capacitors C643, C653, C650 and C642 absorb the fast transients of rapid changes in load current.

70. Because of the relatively slow response of the mean current detection circuitry, further fast protection is necessary to prevent excessive current from damaging the output stage when the output is short circuited or driven into a low impedance load. A 1A trip circuit is therefore fitted and this must operate even when the output is being driven with narrow pulses at a low repetition rate and the average current is too low to operate the mean current protection circuit.

71. Peak current trip protection is provided by passing the output cable through a ferrite core on the output socket so forming a single turn primary winding of a current transformer, T604. A current transition in excess of 1A in the output induces an e.m.f. in the centre-tapped secondary winding sufficient to overcome the bias set by preset, R641. This causes D616 or D617 to conduct into the base of TR609 which, with TR608, forms a monostable with a period of approximately 2ms. Thus any excess output current is detected rapidly and drives the collector of TR608 positive for 2ms so turning on both TR611 and TR638 via R630 and R617 respectively. TR611 turning on locks the slave bistable and prevents the output stage from turning off while carrying a heavy current; turning on TR638 simultates a heavy overload current in the mean current detector and causes the stabilised output supply to collapse rapidly. After approximately 2ms, the clamp on the bistable is removed and after a further period of approximately 8ms, determined by C648, the power supply potential increases slowly. If the overload is still present on the output socket, the trip cycle will repeat.

72. The third protection circuit prevents damage to the output stage which would occur if it were driven faster than 3MHz. TR604 and TR605 form a monostable circuit with a period of approximately 330ns and a fast recovery. Each negative transition of the collector of TR610 in the slave bistable triggers the monostable via C608. The collector of TR604 therefore goes positive and turns on TR643 for 330ns so clamping the secondary drive to D606. Thus during this period, TR610 can be turned off but can not be turned on again. The slave bistable is then prohibited from responding to closely spaced pulse pairs or to input frequencies greater than 3MHz although it will follow such inputs in a count-down mode.

FAST OUTPUT MODULE PG52P7 (Fig. 9)

73. The fast output module operates from the +20V main frame supply and provides simultaneous positive and negative output pulses of up to 5V into 50 ohms with rise times of 1ns. A variable delayed start facility allows the generation of output pulse widths down to 10ns despite the minimum pulse width capability of 25ns of the P2 module. Two input sockets allow the generation of pulses from two independent sources.

Input delay

74. The positive-going input pulses at SKA and SKB are applied to the input gating circuit containing IC701 which is a standard TTL gate operated with resistor R710 connected from the common emitter (pin 4) to the -20V line. This arrangement converts the device into an emitter-coupled gate to increase the switching speed. The gate is protected against input signals of excessive amplitude by the network of diodes D701 to D705 inclusive.

75. Basically, the delay in the input circuit is effected by snap recovery diode D706 and a variable current source containing TR701. During intervals between input pulses, the current through D706 consists of the combined current from pin 6 of IC701 and TR701. The current from TR701 is always less than that from the IC and the difference current, determined by the setting of START DELAY control R706 through D706, controls the amount of charge stored in the diode. The forward voltage drop across D706 reverse biases the emitter base of TR702 and thus prevents the transistor from conducting.

76. When an input pulse turns the IC current off, the voltage across the diode remains constant and the only current which flows into D706 is the reverse current flow from TR701. Due to the characteristics of D706 this reverse current is accepted until the charge is exhausted, the period being determined by the current. The diode then becomes reverse biased and the current from TR701 flows into transistor TR702. When the input pulse ceases the gate current is turned on and immediately stops conduction of TR702.

Pulse amplification

77. The delayed output signal from TR702 is clamped by diodes D709 and D710 and then applied to two similar circuits, TR703/TR704 and TR705/TR706. One circuit produces the positive output pulse, the other produces the negative output pulse. Only the positive pulse circuit is described.

Note ...

The circuits differ in that an additional resistor, R764, is fitted in the tail of TR705 and TR706. This resistor is adjusted on test to minimise differential propagation delay between the two output circuits.

78. Transistors TR703/TR704, TR707/TR708 and TR712/TR713 are three buffer amplifier stages. Transistor TR711 is a constant current source in the tail of transistors TR712/TR713 and determines the level of the output pulse at TR713 collector.

Output level

79. POS OUTPUT LEVEL control potentiometer R756 determines the base potential of TR725 which in turn determines the base potential of TR721. Assuming the four switching diodes D726, D716, D717 and D718 are not conducting, the current through emitter resistor R750 is determined by the setting of R756 and zener diode D724 in the base of TR722. The emitter current of TR721 flows through TR723 and front-panel POS socket SKC to the load. Pulsing of the current through the load is controlled by the four switching diodes which in turn are controlled by the output pulses from TR713.

Pulse switching

80. The output from TR713 is applied to emitter follower TR719 whose bias is set by R741. This resistor is adjusted so that the emitter potential of TR719 allows diodes D726, D716, D717 and D718 to conduct during the interval between output pulses. Output current is therefore diverted to ground via TR719. When a pulse is present at the collector of TR713, the emitter of TR719 goes positive and hence the four diodes are switched off so that an output pulse is produced at SKC.

81. Transistor TR719 is biased by the preset resistor R741 to the threshold of conduction to minimise diode switching delay. Bias compensation for different settings of the POS OUTPUT LEVEL control is effected by TR717 whose base is fed via zener diode D722 from the emitter of TR721. Capacitor C710 effects high frequency compensation of the diode switching waveform.

WORD GENERATOR MODULE PG52P8 (Fig. 10)

82. The PG52P8 module is powered from the +20V, -20V and +5V main frame supplies. It allows the generation of pulse patterns up to 16 bits in length and can operate in a continuous or externally-triggered cycle mode. The output can be switched to be in a non-return-to-zero form or, via a pulse width delay module P2, in a return-to-zero form. A synchronising signal is provided at the end of the word to allow modules to be cascaded to extend the word length beyond 16 bits.

83. The operation of the unit is based on a 16 bit shift register with its associated control circuitry contained in 12 dual in-line packages of TTL integrated circuitry. Buffering between the 10V system interface input signals and the TTL circuitry and subsequent conversion back to a 10V level for the outputs is performed by discrete semiconductor amplifying and switching circuitry.

84. Integrated circuits 803, 804, 805 and 806, each contain a four bit shift register with the facility to enter information in parallel or serially. The ICs are connected in cascade to form a 16 bit shift register.

85. At the beginning of a word sequence a mark is introduced in the first stage (output P_1) and subsequent clock pulses shift this mark to P_2, P_3, P_4 etc., returning P_1, P_2, P_3 etc. to the unmarked state i.e. each P pin is marked for one period of the sequence. The pulse summing gates IC810 and IC811 are thus energised with the pulse pattern determined by the setting of the toggle switches, S801, S802 etc. IC812 further sums the output of IC810 and IC811 to form the word pattern required.

86. When the mark in the shift register reaches the position selected by the word length switch, S817, drive to the shift register is modified such that on the next clock signal all stages are cleared ready for the next cycle to commence.

Note ...

In the repeat mode the first stage is marked and the cycle is commenced immediately.

87. IC801 and IC802 control the shift register in this start stop sequence. IC's 807, 808 and 809 are used to prevent any lock up condition when the circuit is switched on or if a pulse is lost when the switches are operated during a word sequence.

Input circuits

88. The purpose of the circuitry associated with TR801 to TR807 inclusive, is to accept the 10V input start and clock signals and convert them to a 5V level, differentiated as necessary to drive the subsequent TTL circuits. TR807 is normally cut off via R819 but when the START INPUT, SKA, is driven positive, TR807 conducts and its collector voltage switches from +5V (limited by D810) to 0V. This transition is transferred by link ST to start a word sequence. If the AC/DC START switch, S820, is closed ST is held low for the period that the START INPUT is positive. If S820 is open, C809 differentiates the positive going input edge and ST is at 0V momentarily.

89. The clock input on SKB drives TR801 and its resulting collector potential switching between +5V and OV is buffered by the complementary emitter followers to provide a low impedance 5V drive which is the inverse of the clock input. Link C passes this signal to the TTL circuitry.

90. The negative going transitions of the clock input cause the pattern to shift while the corresponding positive transitions momentarily turn on TR804 so causing TR805 to turn off. The collector potential of TR805 is thus normally at OV and is driven to +5V for approximately 40ns at the leading edge of each clock pulse. This signal is passed via link C^1 to the TTL circuitry. C805 introduces a small delay in the generation of this pulse.

91. The positive going transitions of the clock input signals also cause the emitter of TR803 to drive negative and these negative-going transitions are coupled via C807 to turn on TR806. The resulting signal at TR806 collector which is normally held at OV and is driven to +5V for approximately 4ns on the return edge of each clock pulse, is coupled via $\overline{C^1}$ to the TTL circuitry.

Note ...

Each signal path from the input units to the TTL circuitry is taken via a link which can be broken to aid fault location.

Logic function

92. IC's 801, 802 and 812 contain TTL gates each performing a NAND function. All signal levels are normally +0.2V for the 'low' state and +3V for the 'high' state.

93. Each IC package, 803 to 806 is a four bit shift register which operates in the serial mode while the input to pin 9 is high. The serial input to the first bistable, applied to pins 2 and 3 linked, is shifted through the register on each 'low' to 'high' transition of the clock applied to pin 10.

94. The register operates in the parallel mode when the input to pin 9 is low. In this case, every 'low' to 'high' transition of the clock input shifts the data content one place and enters the input applied to pin 4, i.e. the logic at pin 4 appears at pin 15.

95. The state of the serial input, the parallel inputs and the serial/parallel control can be changed at any time without any change to the output. The outputs can only be changed when the clock goes 'high'.

96. In practice, all parallel entry pins are left unconnected, the equivalent of a high input, with the exception of the first stage input, pin 4, of IC803. The reset input, pin 1, and the inverse output from the last bit, pin 11, are unused. The final output, pin 11, of IC803 is connected to the shift input, pins 2 and 3, of IC804. Similarly, IC803 feeds IC805. The series/parallel control and clock inputs are connected to form a complete 16 bit register.

97. Fig. 1 shows the detailed pulse sequence in the different modes of operation. With the start switch, S818, set to EXT and the start coupling switch, S820, set to AC, the signal cycle function is as follows:

(1) The positive going start signal generates a short negative going ST pulse which sets the memory bistable, sending IC801/8 high.

(2) This removes the clamp applied to $\overline{C}^1$ pulses and the next pulse appears as a low on IC801/3. This sets the start bistable so sending E and hence P_o low.

(3) IC802/6, the series/parallel control, is initially low defining parallel entry to the register. With all parallel inputs high, all P points (P_1 to P_{16}) started high. P_o being low primes the parallel inputs to the first stage of the register and the next clock edge sends P_1 low.

(4) P_1 is fed directly to the series/parallel bistable at IC802/13 and sends IC802/6 high, switching the register to the parallel mode. P_1 also resets the memory and the start bistables.

(5) With the serial input to the register from IC809/11 high, the next clock pulse resets P_1 to the high state but sets P_2 low. Subsequent clock pulses transfer the low mark from P_2 to P_3, P_4, P_5 etc. towards P_{16}.

(6) Any of the pulse pattern switches, S801 to S816 inclusive, that are closed, allow their associated P pulses to pass to the corresponding point Q. The outputs of these gates are inverted and summed again in IC812.

(7) If the module is operating in the NRZ mode the summed waveform is in the form required and is passed directly to the output circuit via S819b. D811 with C803 and D812 with C806, prevent any gap appearing in the output between consecutive selected pulses at the instant when one Q pulse goes off and the next comes on.

(8) If the module is operating in the RZ mode the output waveform from IC810 and IC811 is strobed by the C^1 pulse train and the final inverting stage of IC812 is bypassed by S819b to generate the required output waveform. C805 provides a small delay in the generation of C^1 to prevent the leading edge of a Q pulse. This overlap could generate an unwanted output pulse at the end of an isolated marked output period.

(9) The generation of P pulses in sequence from the register continues until the pulse selected by the Word Length switch, S817, is reached. This pulse is taken as the last pulse, PL, and resets the series/parallel bistable sending IC802/6 low and converting the register for parallel entry.

(10) With P_o reset high at an earlier stage, the next clock pulse sets all P pulses high, effectively clearing the register and returning all stages to their initial condition, awaiting the next start signal

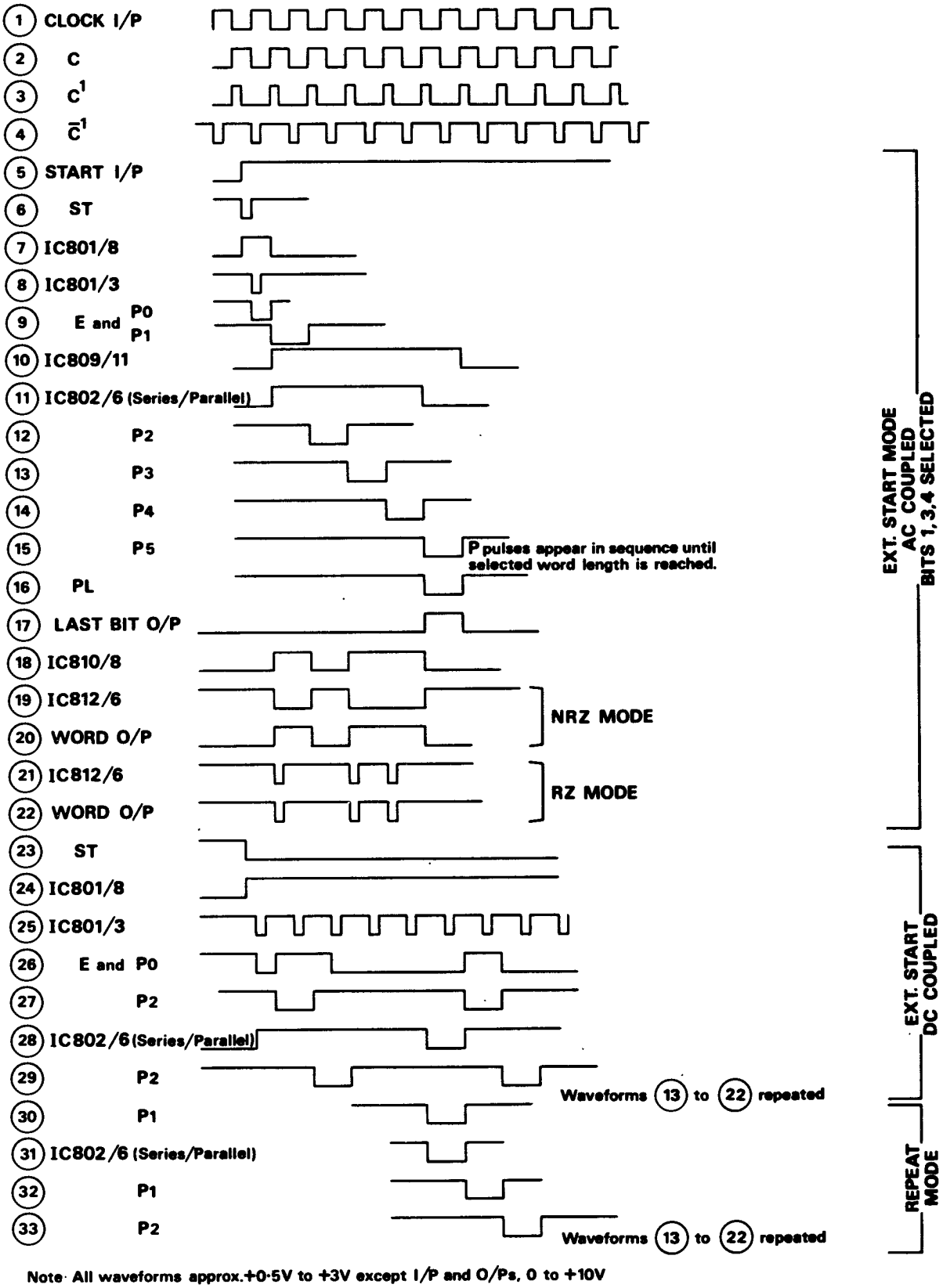

Fig. 2 PG52P8 detailed timing diagram

98. If the START is DC coupled, S820 closed, and the start input remains high beyond the P_1 period, the start memory bistable is not reset at P_1 and $\overline{C1}$ pulses continue to be generated at IC801/3. P_o goes high during the P_1 period but is set back low by the next $\overline{C1}$ pulse. At the end of the first word, P_L returns the register to the parallel mode but with P_o high, P_1 is generated at the next clock pulse and the sequence repeats. Re-cycling continues until the start signal is removed. The circuit then completes the word for which it has been primed before stopping. When the module is set to the REPEAT mode, S818 holds P_o permanently low. As described, P_L resets the bistable to operate the register in parallel entry but with P_o low, P_1 is again generated following PL and the sequence is continuous.

99. IC807, IC808 and IC809 combine as a pulse detector operating on the output of the register and feeding high signals into the register while there is a low on any output. If the word length switch S17 is turned during the generation of a word, PL may be lost. The register will stay in the serial mode and the mark will shift through the register until P_{16} is cleared. Without the pulse detector the system would then be locked against any further operation. However, the detector introduces a 'low' back into the first stage of the register and another cycle commences. The detector also prevents a similar locked condition when the unit is first switched on.

Output circuits

100. The low level outputs from the TTL circuitry for the word and last bit outputs, are amplified to the 10V system interface level by two identical circuits. Only the last bit circuit is described.

101. The +0.5V to +3V signal step at P_L is applied to the input of the current mode switch, TR808/TR809. The differential output from the collectors of these transistors is applied to the bases of TR810 and TR811. These form a further current mode switch and the current defined by R827 is switched via the collector of TR810 and R828. This generates a +10V pulse which is buffered by the complementary emitter followers, TR812 and TR813, to drive the output socket SKC through R833 and the test point through R864.

GATE UNIT MODULE PG52P9 (Fig. 11)

102. This module contains two independent four input gates which permit the synthesis of complex waveshapes. Each input and output has the facility of inversion and this flexibility allows it to be used in AND, NOR and NAND modes to achieve such functions as pulse addition, pulse blanking and the formation of a set/reset bistable.

103. The four input sockets SKA to SKD are directly coupled to the bases of transistors TR901, TR903, TR905 and TR910 respectively. Each of these transistors is connected as the input side of an emitter coupled current mode switching circuit, the other transistor having its base grounded. Resistors R902, R908, R913 and R923 ensure that the input transistor is normally turned off when the input is low or open circuit. Three diodes associated with each amplifier pair offer protection against excess input voltage by limiting the differential voltage developed between the two bases. The four input stages are identical, each consisting of an emitter coupled pair of transistors (similar to TR901 and TR902). The small

inductor in series with each collector load resistor speeds up signal transitions.

104. The output from each amplifier is taken via a switch (S901 to S904) so that the in-phase or inverted signal may be used to drive the subsequent gate circuit. The signal from each of these switches feeds into a diode gate, D907 to D910. With all the inputs high, the base emitter junction of TR906 is reverse biased due to R911.

105. Transistors TR906 and TR908 from an emitter coupled current mode switching pair with a constant emitter current from the current source transistor, TR907. When any of the collector voltages of transistors selected by S901 to S904 fall, the voltage drop causes the respective gate diode to conduct thus turning on TR906. The current determined by R916 then flows through the load resistor R914 and associated speed-up inductor L906 to give a +10V swing at the collector of TR906, whilst the collector potential of TR908 falls to 0V. The outputs from the collectors of TR906 and TR908 pass via a polarity selection switch, S905, into a complementary emitter follower stage TR911 and TR912 which provides a low impedance output to SKE and via R943 to a test point.

106. The output circuitry is protected against accidental short circuits by the series resistor R932 and the two collector current limiting resistors (R926 and R927) associated with the emitter follower stage.

107. The circuits containing transistors TR951 to TR963 operate in a similar manner to that described in para. 104 to 107.

108. With all inputs to the module low or open circuit and all switches set to N (normal) the output is at ground potential. An input pulse on SKA passes through the input amplifier and gate circuitry, and appears at the output socket in-phase with the input. By selecting the invert (I) position of S901 or S905, the output is inverted with respect to the input pulse. By suitable selection of switches S901 to S904 up to four inputs may be gated together to produce an output waveform on a single line.

TRIGGER MODULE PG52P10 (Fig. 12)

109. The PG52P10 trigger module provides facilities for triggering the system from external signals or from the internal 50Hz (60Hz) supply frequency. It has a slope and level selection control with a sensitivity of 500mV. In addition to the normal interface signal output it has an independent prepulse output of 1V into 50 ohms and of width variable from 25ns to 200ns. A further ÷2 aperiodic count down allows the generation of a 1:1 squarewave at any frequency. The module operates from the +12V supplies in the main frame.

Trigger source and amplification

110. The trigger input is applied either to SKA or is derived from the 50V ac line by S104, the front-panel INT LINE TRIG switch. The trigger signal is then applied to a 2:1 potential divider consisting of R106 and R107 and amplified by the long tail pair differential amplifier containing transistors TR101, TR102, TR103 and TR104. Diodes D101, D102, D103 and D104 in the base circuit of TR101 protect the amplifier against excessive input voltages.

Note ...

Additional 10:1 attenuation of the selected trigger may be introduced by means of the front-panel ATTEN 10:1 control.

111. The operating point of the amplifier, and hence the section of the input waveform selected for amplification, is determined by the setting of front-panel TRIG LEVEL control R117. This control has a range of -2.5V to +2.5V and the zero level is preset by R116.

Trigger generation

112. The output of the amplifier is fed from the collector of TR104 to the base of transistor TR105 which, with TR106, operates as a trigger circuit. Collector-to-base cross coupling provides back lash which prevents multiple triggering due to spurious signals on slow trigger pulses. Zener diode D108 stabilises the supply voltage to the input amplifier and trigger circuit.

113. The complementary trigger pulse outputs from the collectors of TR105 and TR106 are applied to the high speed integrated-circuit logic gate IC101a which functions as an invert select switch. The condition of the gate is dc controlled by front-panel NORM and INV switches S102a and S102b. When the INV button is actuated the trigger pulse polarity is opposite to that of the input signal.

Count down

114. The output from IC101a is applied to IC102 and IC101b. Integrated circuit IC102 introduces a ÷2 function and its output is also applied to IC101b. The logic condition of IC101b is dc controlled by S101, the front panel COUNT DOWN ÷2 switch, so that either ÷2 or direct output from the invert select switch is available. Zener diode D107 defines a -5V supply rail for both integrated circuit packages.

Trigger output signal

115. The selected output of IC101b is applied to:

(1) The trigger output circuit.

(2) The variable width trigger pulse circuit.

116. In the trigger output circuit, transistor TR114 operates in a long tail pair configuration with TR115 whose base is biased by the setting of R158. Current through TR115 is switched by the signal applied to TR114 and produces an output pulse of 0V to +10V in the collector of TR115. The output pulse is limited at +10V by catching diode D119 referenced to the 10V zener diode D120.

117. From the collector of TR115, the pulse is applied to a complementary emitter follower buffer stage containing transistors TR116 and TR117. The low impedance interface output pulse produced in the emitter circuit is routed through current limiting resistors to SKB, SKC and test point TP identified on the front panel as +10V TRIGGER OUTPUT.

Trigger pulse output

118. In the variable width trigger circuit, the output from IC101b is applied to the base of transistor TR107 which, with TR108, operates as a long tail pair amplifier with bias preset by R134. The output from the long tail pair switches transistor TR109 whose collector circuit contains inductor L102. A negative-going pulse applied to TR107 develops a fast positive-going pulse across L102 and this pulse, dc shifted by zener diode D112, triggers the emitter-coupled monostable circuit containing transistors TR110 and TR111. The recovery time of the monostable is determined basically by R137, R138 and R109 but can be varied by the front-panel TRIG PULSE WIDTH control to any period between 25ns and 200ns.

119. The monostable output is taken from the collector of TR111 and applied to the base circuit of TR113 which operates with TR112 as a long tail pair amplifier. The output pulses are developed across the collector load resistors, positive-going across R147 and negative-going across R149. The polarity of the output pulse is selected by S106a, the + and - POLARITY switch on the front panel.

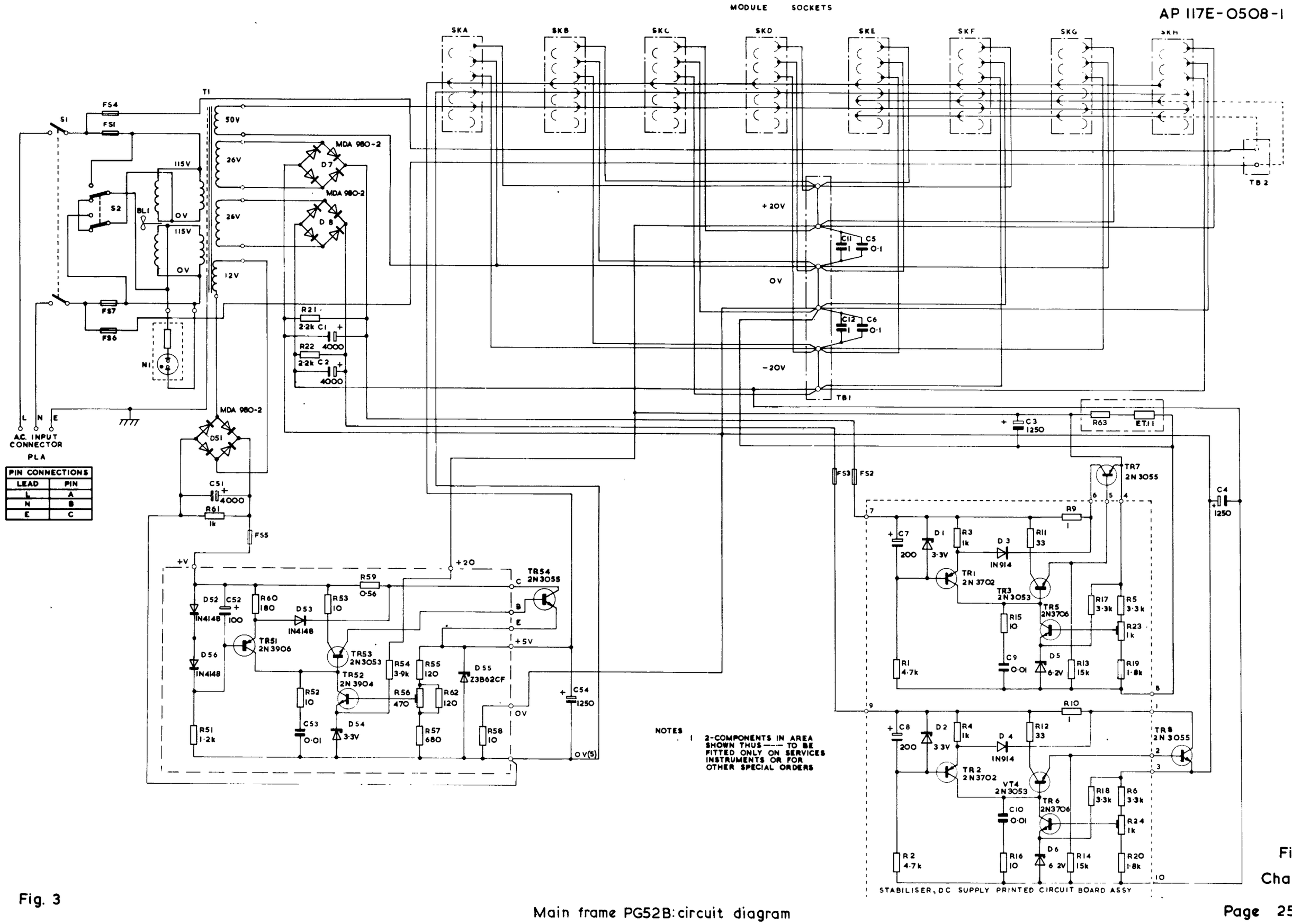

Fig. 3

Main frame PG52B: circuit diagram

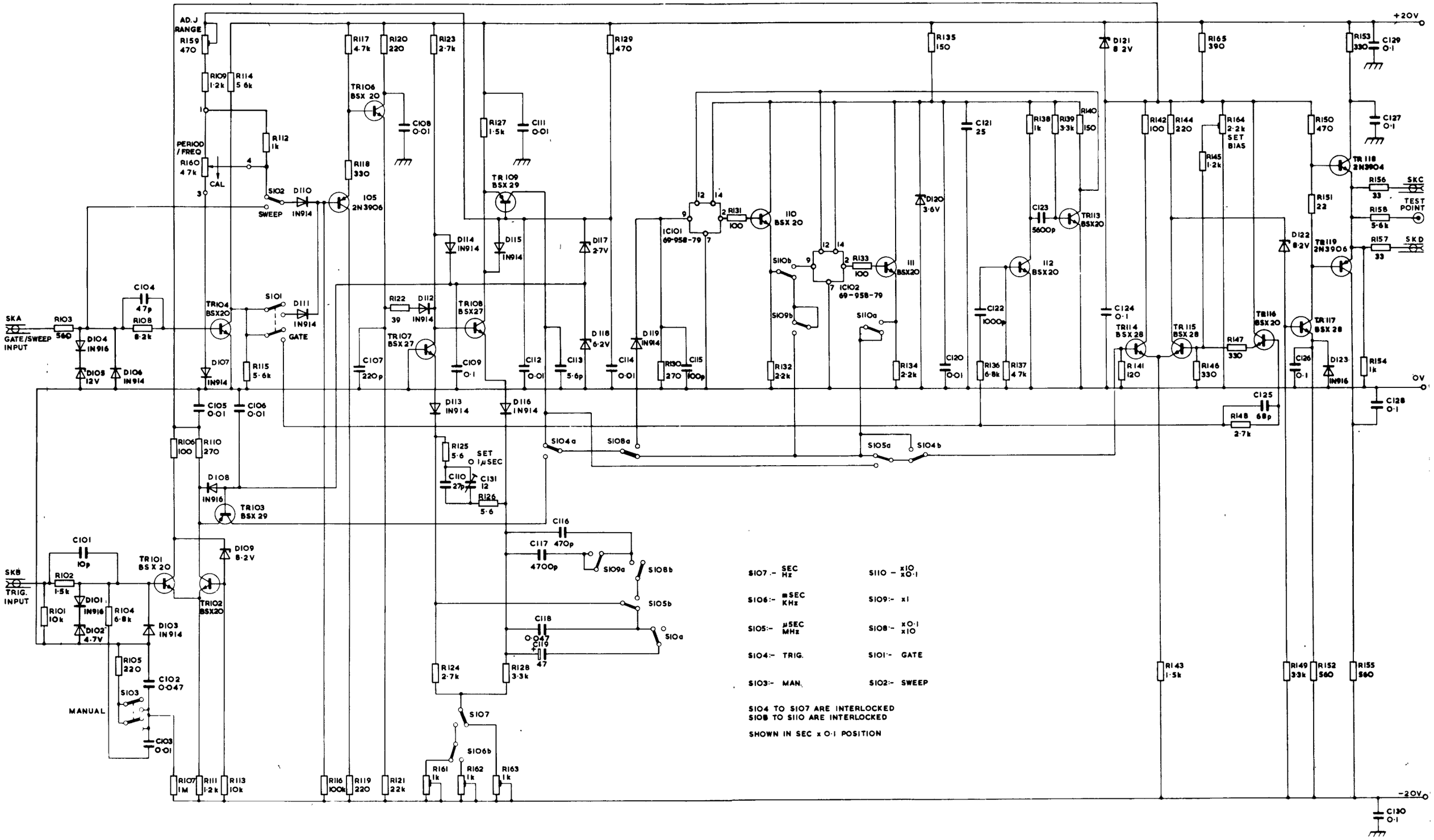

Fig. 4 Clock generator PG52 PIA : circuit diagram

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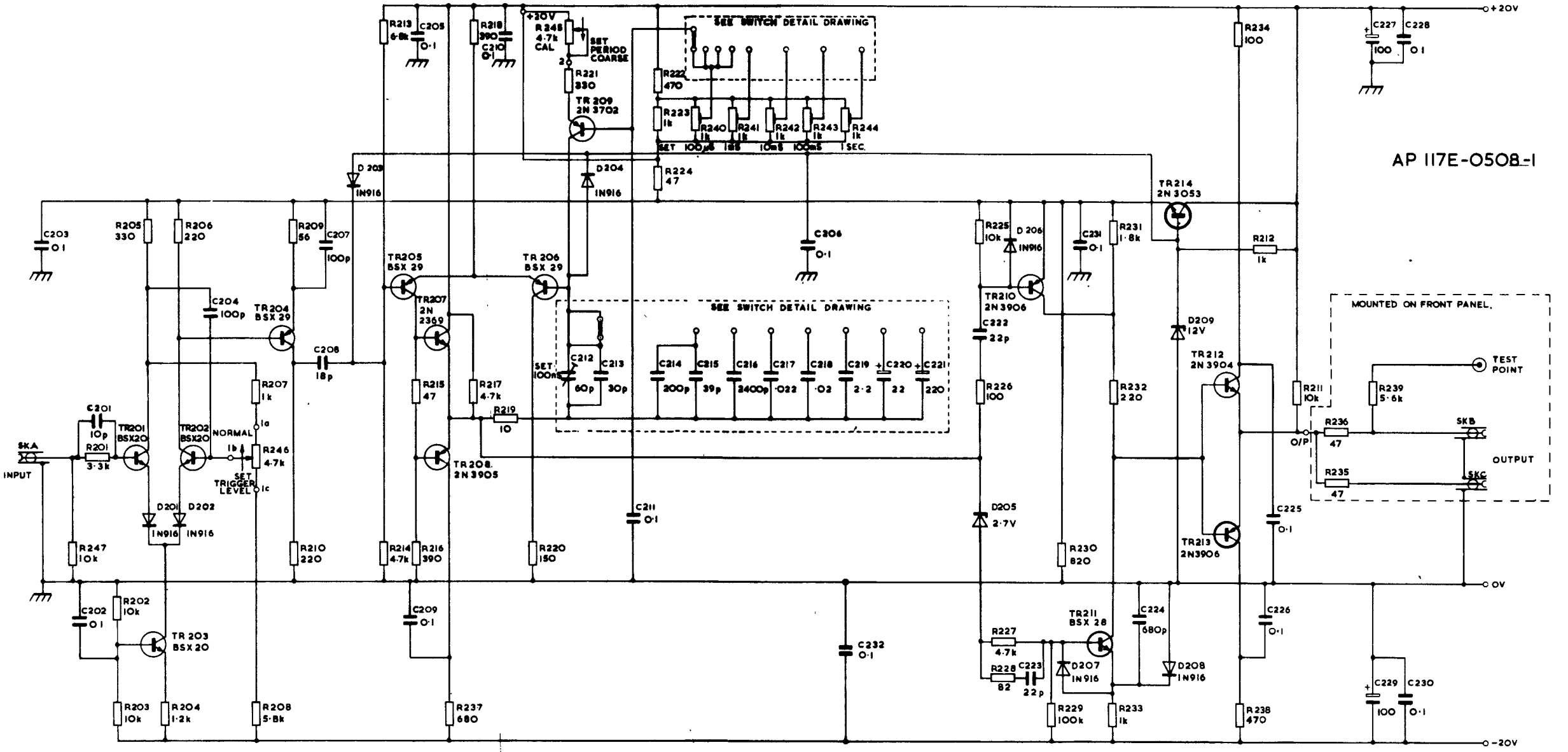
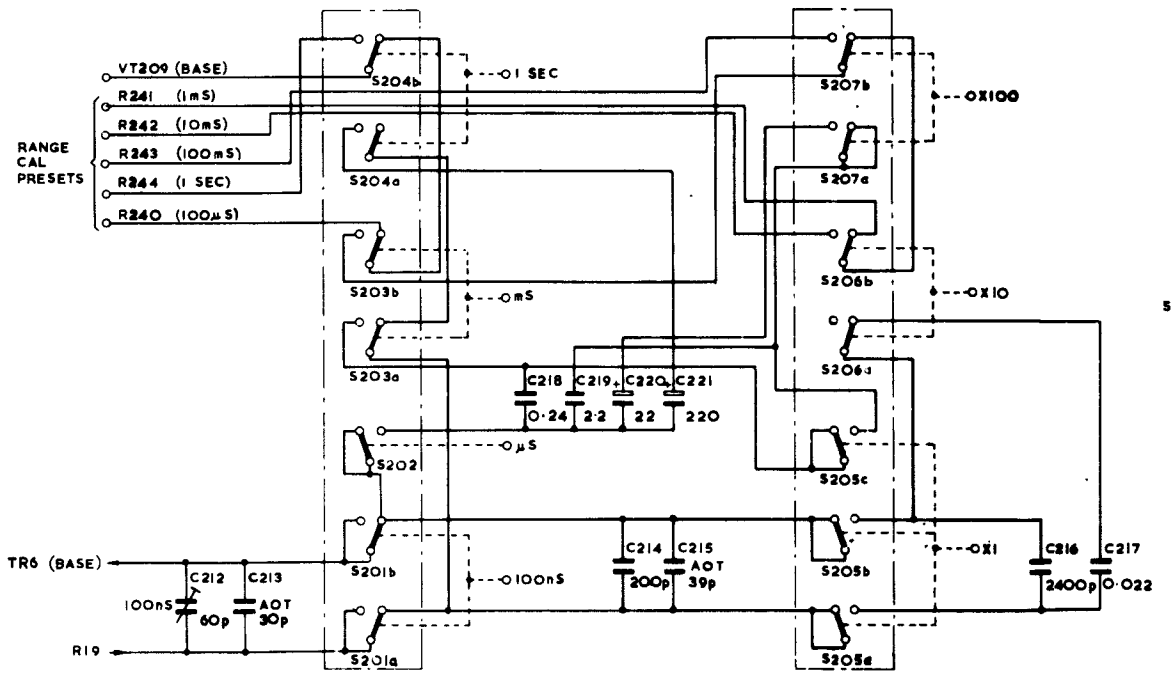




SWITCH DETAIL

S 201 TO S204 ARE INTERLOCKED AS UNITS BANK.
S 205 TO S207 ARE INTERLOCKED AS MULTIPLYING FACTOR BANK
SWITCHES DRAWN FOR µS x 1.

Fig. 5

Pulse width or delay module PG52 P2A: circuit diagram

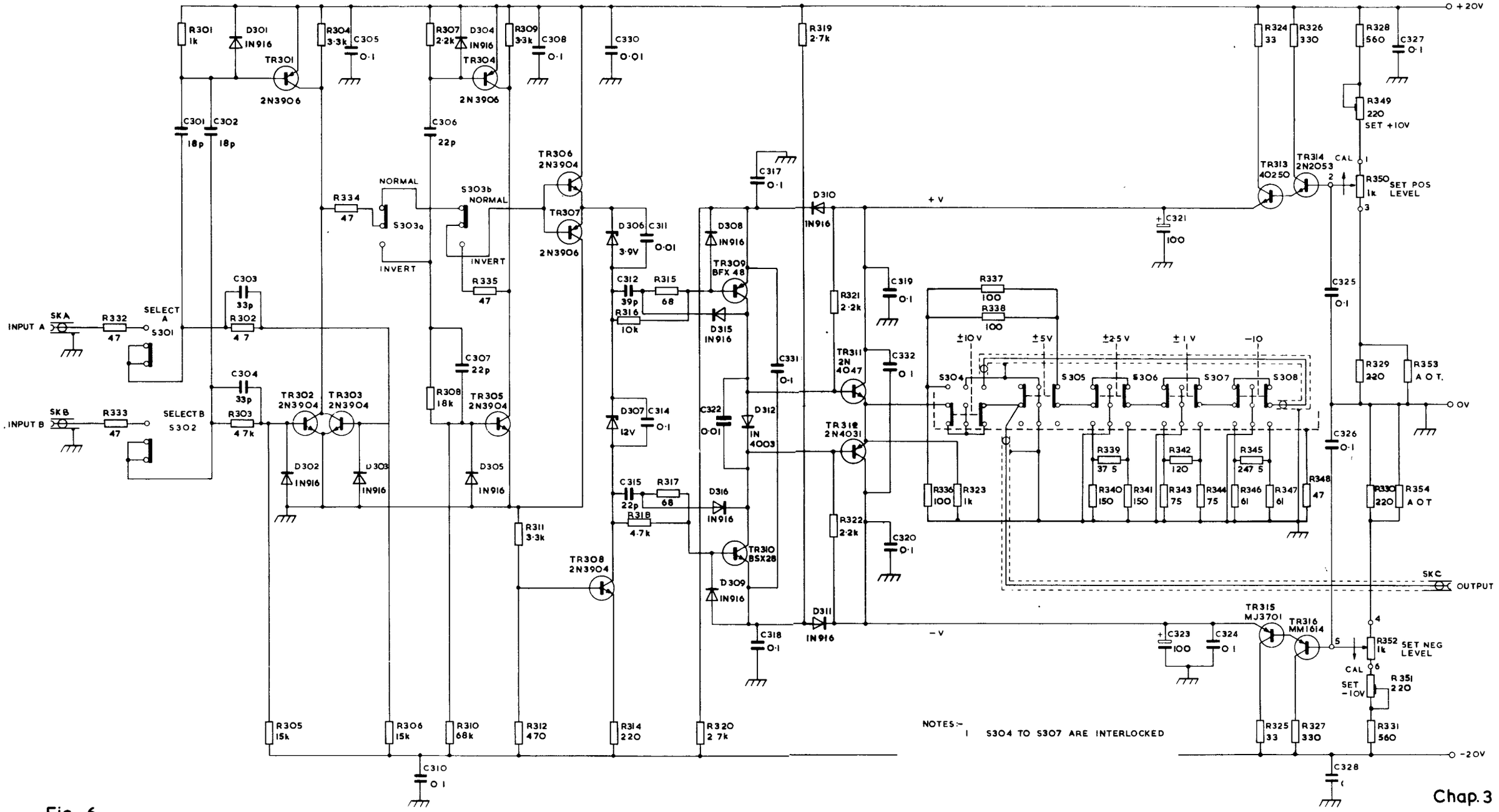
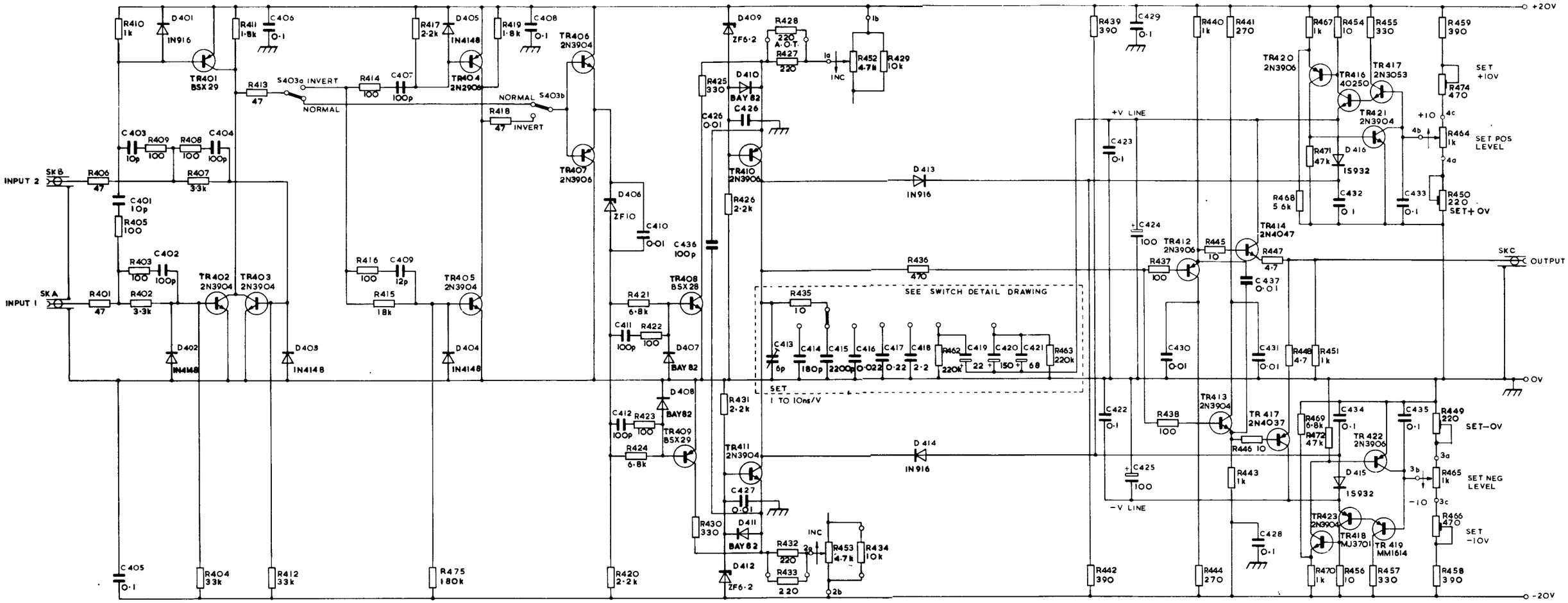
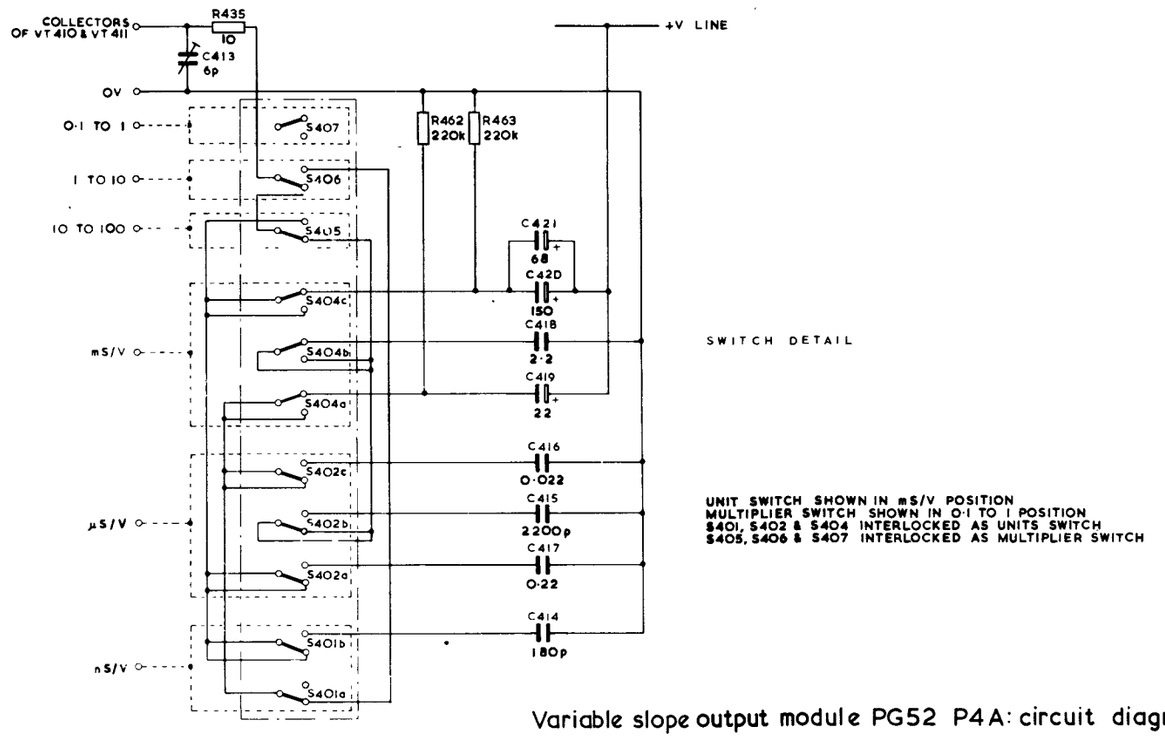


Fig. 6

Standard output module PG52 P3A: circuit diagram

Fig. 6





SWITCH DETAIL

UNIT SWITCH SHOWN IN mS/V POSITION
MULTIPLIER SWITCH SHOWN IN 0·1 TO 1 POSITION
S401, S402 & S404 INTERLOCKED AS UNITS SWITCH
S405, S406 & S407 INTERLOCKED AS MULTIPLIER SWITCH

Fig. 7

Variable slope output module PG52 P4A: circuit diagram

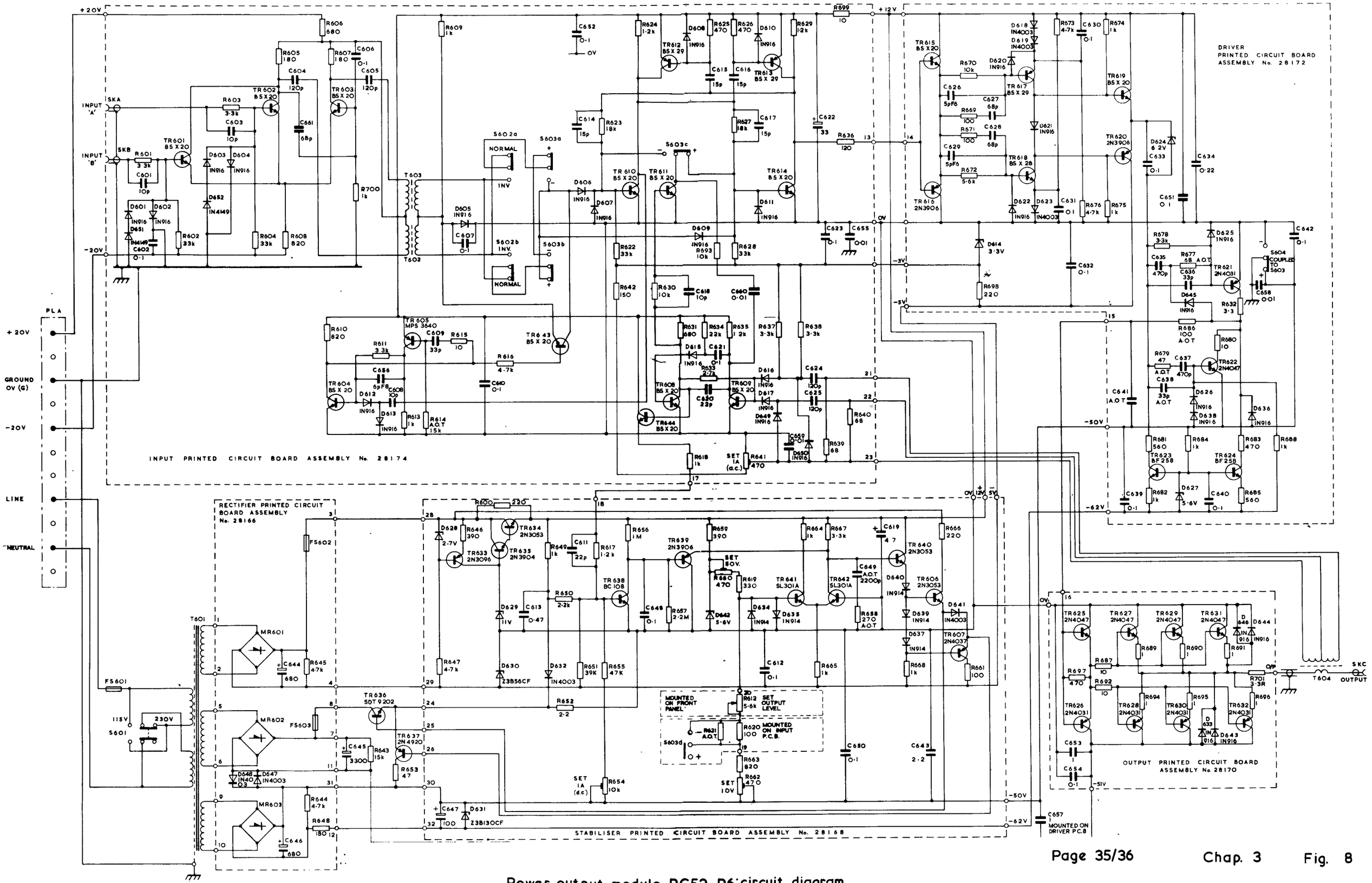


Fig. 8

Power output module PG52 P6: circuit diagram

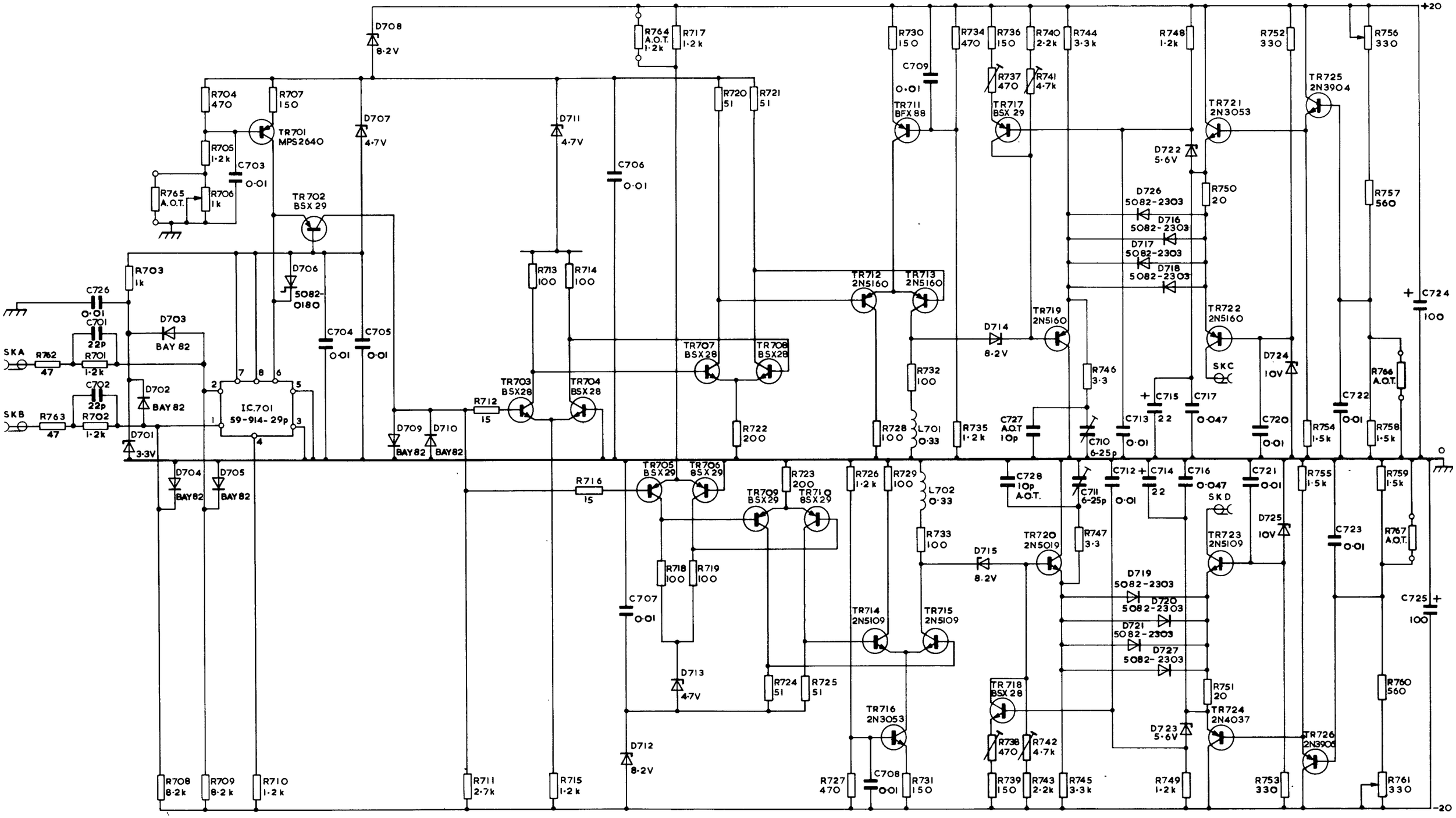


Fig. 9 Fast ouput module PG52 P7 : circuit diagram

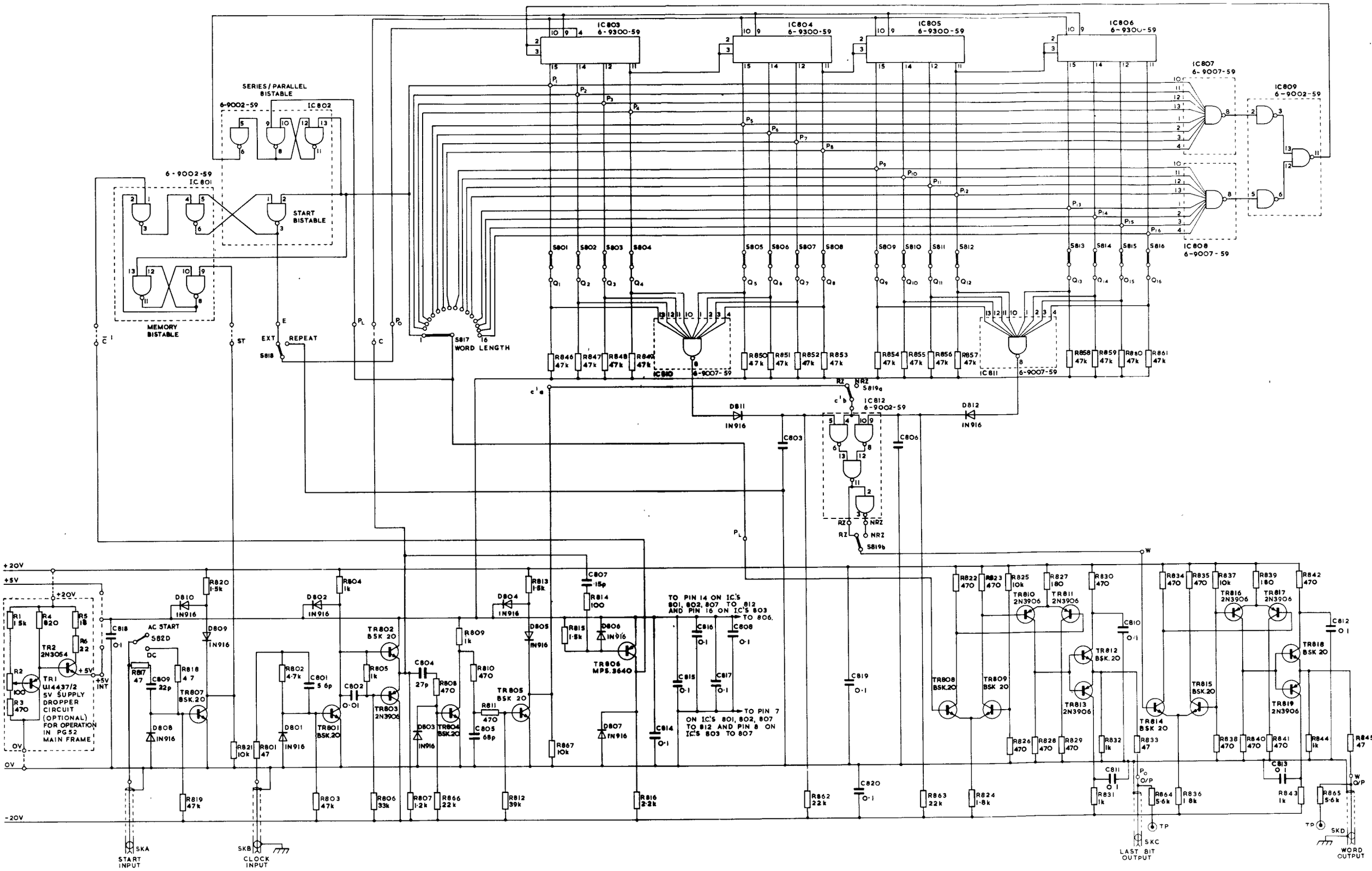


Fig. 10

Word generator module PG52 P8: circuit diagram

Fig. 10

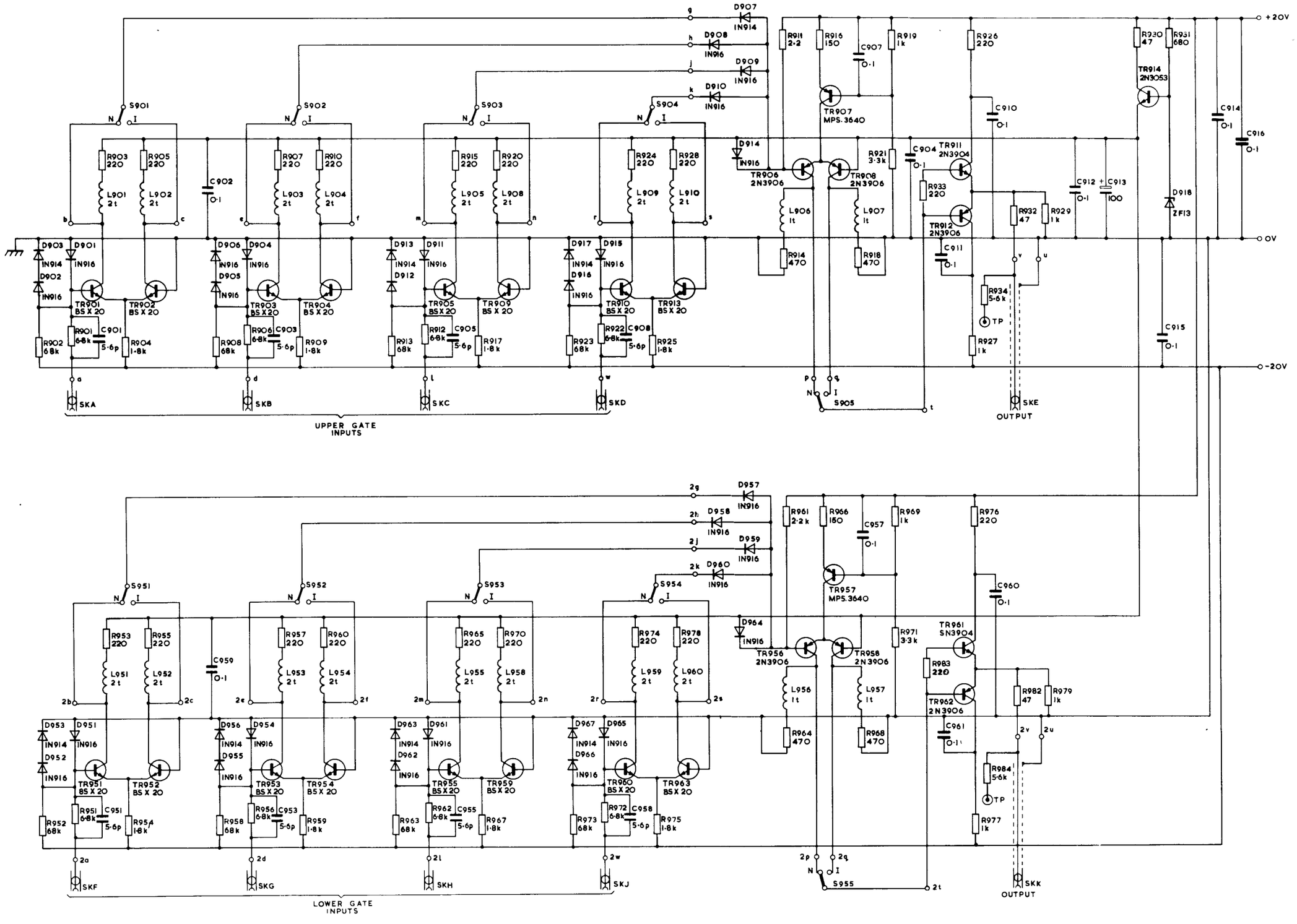


Fig. 11

Gate unit PG 52 P9 : circuit diagram

Fig. 11
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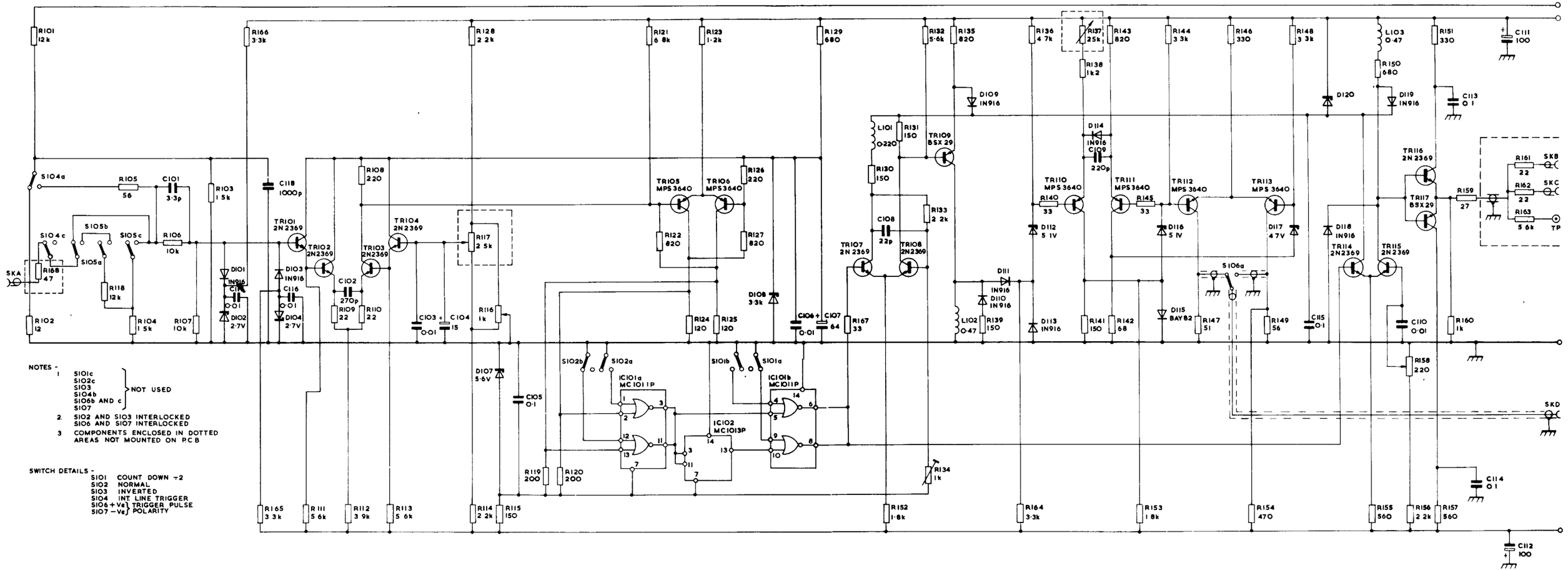

NOTES -

1. S101c, S102c, S103, S104b AND c, S106b AND c, S107 } NOT USED
2. S102 AND S103 INTERLOCKED
   S106 AND S107 INTERLOCKED
3. COMPONENTS ENCLOSED IN DOTTED AREAS NOT MOUNTED ON P.C.B

SWITCH DETAILS -

S101 COUNT DOWN ÷2
S102 NORMAL
S103 INVERTED
S104 INT. LINE TRIGGER
S106 +Ve } TRIGGER PULSE
S107 −Ve } POLARITY

Fig. 12 Nov.77 (Amdt 1) Trigger module PG52 P10: circuit diagram

Chapter 4

OPERATION

CONTENTS

CONTENTS (Cont.)

TABLES

ILLUSTRATIONS

POWER SUPPLIES

1. The CT578/3 modular pulse generator is designed to operate from 45Hz to 60Hz ac supplies in the range 100V to 130V or 200V to 260V. The equipment is normally supplied with the mains transformer taps set for 200V to 260V operation but this must be checked and, if necessary, changed before use by means of the recessed knob on the rear panel.

CAUTION ...

The mains input voltage determines the required current rating for slow-blow ac supply fuses. Correct ratings are

100V to 110V : 2A

200V to 260V : 1A

2. Fuse links are only fitted at FS4/FS6 when a power output module PG52P6 is installed in a main frame. The correct rating for these fuses is 4A.

VENTILATION

3. The equipment is ventilated by a fan mounted on the rear panel.

CAUTION ...

The air filter must be kept clean and the inlet and outlet areas at the rear of the equipment must never be obstructed.

4. To maintain the correct air circulation, a full complement of modules or blank panels (PG52P0) should be fitted when the equipment is operating. This is particularly important when a PG52P6 power output module is in use. If the permitted current loading (para. 5) is exceeded by plugging in an unwanted module to fill a gap, the module can be inserted upside down so that its plug does not engage with the socket on the main frame.

CURRENT LOADING

5. The internal +20V, -20V and +5V dc supplies are each limited to 2A. Any combination of plug-in modules may be used in one main frame providing that the total current drain for each dc supply does not exceed 2A. The maximum loads imposed by each module are given in Table 1.

TABLE 1

Modules maximum current loading

Module	+20V line	-20V line	+5V line
PG52P1A	0.25A	0.15A	NIL
PG52P2A	0.1A	0.05A	NIL
PG52P3A	0.3A	0.3A	NIL
PG52P4A	0.45A	0.45A	NIL
PG52P5	NIL	NIL	NIL

TABLE 1 (cont.)

Module	+20V line	-20V line	+5V line
PG52P6	0.05A	0.05A	NIL
PG52P7	0.35A	0.35A	NIL
PG52P8	0.15A	0.05	0.3
PG52P9	0.15A	0.1A	NIL
PG52P10	0.25A	0.25A	NIL

Note ...

The rating given for the PG52P3 and PG52P4 modules includes the 200mA drain from each supply when the full +10V to -10V output capability into a 50 ohm load is being used.

6. Table 1 shows that the most likely combinations of 8 modules do not exceed the 2A limitation. However, if a number of P3 or P4 modules is used at one time and the sum of the above loads does exceed 2A, a closer analysis may show that the supply is still not overloaded. For this purpose assume that each P3 module takes a quiescent current of 0.1A and each P4 module takes a quiescent current of 0.25A from each supply. The total quiescent current loading, plus the instantaneous peak output current, must not exceed 2A. The use of the attenuator of the P3 module does not relieve the load on the supply because the current is being delivered into the attenuator resistors if not into an external 50 ohm load. However, if either of the fine level controls on any output unit is not at maximum, the load is reduced accordingly. Also, if the output pulses from a number of units are separated in time, the instantaneous peak output current is not the sum of the peak output currents.

7. If however, the power supply is overloaded, the supply line voltage may drop and either the instrument may not perform to specification or the corresponding 2A fuse of the main frame may blow.

8. For less exacting applications where variable amplitude, specified rise time and overshoot etc., are not required, the 10V outputs from waveform generating or processing modules can be used directly into high impedance loads.

INTERCONNECTIONS

9. The provision of all modules as separate units allows a large number of configurations each with a different pulse generating function. Signal interconnection between modules is normally carried out by 7in. long BNC to BNC coaxial leads (PL81). Longer coaxial leads may be used if necessary but, where possible, this should be avoided by re-arranging the modules in the main frame. It is particularly important to keep interconnecting leads as short as possible if minimum repetition periods and pulse widths are required.

10. In setting up a complex function, each module should be set in turn along the signal path using the output test points to feed an oscilloscope for examination of the output waveform. The oscilloscope is best triggered externally from the clock generator module (PG52P1A) or from the first pulse width or delay module (PG52P2A). Alternatively, the trigger pulse output of a trigger module (PG52PLO) may be used.

11. The interface output modules P1, P2, P8 and P9 are each designed to drive up to four inputs. The outputs of the P1 and P2 modules are available on two BNC sockets in parallel. BNC "T" adaptors should be used to provide further fan-out up to the maximum of four. However the system cannot be used at its maximum frequency or minimum pulse widths with the full loading.

12. Typically each P1 or P9 module will drive:

(1) Any four modules up to 50MHz

(2) Any three modules up to 10MHz

(3) Any two P2, P3, P7 or P9 modules up to 20MHz

(4) One P3 or P7 module up to 30MHz.

13. Typically each P2 module will drive:

(1) Any four modules to widths greater than 40ns.

(2) Any two modules to the minimum width of 25ns.

Note ...

The passive summing unit (PG52P5) is a symmetrical delta network and while intended to sum the output pulses from different sources, it can also be used as a signal splitter. A pulse from one source can be split into two or three independent 50 ohm loads with an attendant loss of amplitude.

TERMINATION

14. Output modules P3, P4, P6 and P7 are designed to operate into a 50 ohm load. Distortion of the output pulse may occur if the units are not correctly terminated. It may also occur if the load is not connected through a 50 ohm cable such as the PL43. However, such distortion may be negligible from the PG52P4 variable slope output module if slow rise and fall rates are being used.

CLOCK GENERATOR MODULE PG52P1A

Normal internal operation

15. (1) Select the frequency/period units required, MHz/μs, kHz/ms, or Hz/s on the left hand bank of pushbuttons.

(2) Select the required multiplying factor x10, x1 or x0.1 on the right hand bank of pushbuttons.

Note ...

The three FREQUENCY/PERIOD unit buttons and the TRIG. button are interlocked and pressing any one will release the others. Similarly, the three multiplying factor buttons are interlocked. The GATE and SWEEP buttons should not be depressed.

(3) Set the fine control at the top of the panel in the CAL position. The output signal will be at the selected frequency/period within the calibration accuracy of ±5%.

16. Operation of the fine control away from the CAL position increases the frequency (decreases the period) at least over a deacde range (3:1 on 10MHz/0.1μs range). The intermediate scale marks of the fine control allow the control to be reset rather than provide calibration.

Sweep mode

17. When the SWEEP button is depressed, the fine FREQUENCY/PERIOD control becomes inoperative. The frequency/period can now be controlled over the appropriate decade range (3:1 on 10MHz/0.1μs range) by the application of a positive voltage on the GATE/SWEEP input socket. At approximately +1V the frequency/period will be the calibrated value and the decade sweep will be completed at approximately +8V. The frequency/period can be swept beyond the decade range but erratic operation may result before the output signal is finally blocked off by excessive signal.

Gate mode

18. When the GATE button is depressed, no output signal is present (output level stays at approximately +10V). The application of a positive signal to the GATE/SWEEP input socket will initiate the output signal. The first negative-going transition of the output signal occurs when the gate signal is applied and subsequent transitions at the set frequency. When the gate signal returns to 0V the output signal immediately returns to approximately +10V.

19. Any signal greater than +8V dc can be used as the gate signal although the output from a PG52P2A is normally used. The "off" level should not be more positive than +100mV and should have a minimum width of 0.5μs with rise and fall times less than 1μs. If a fast rise time is employed, the first output pulse occurs within 250ns of the application of the gate signal. Accurate gating of signals above 5MHz cannot be achieved. The input resistance is greater than 1k ohm and the input socket is protected against excessive input signals of up to ±20V peak.

External trigger mode

20. Operation of the trigger button disables the internal clock. With the multiplying factor selected to DIRECT, output transitions occur at the frequency of any signal applied to the trigger input socket, a positive-going input giving a negative-going output transition. With factors of ÷10 or ÷100 selected, the input frequency up to 2MHz is divided by the appropriate factor using the internal digital divider circuitry. The output mark/space ratio is then 1:4.

21. Directly coupled trigger inputs from dc to 10MHz can be accepted. The nominal input trigger point is +4V and it is recommended that the input signal drive is between 0V and +8V. Protection is provided against signals up to ±20V peak. The unit can be triggered from any low-frequency sinusoid or other waveforms which cross the trigger point only twice per cycle. The input resistance is greater than 1.5 k ohms.

22. It is possible to use the gate facility together with external trigger. On direct trigger, the output follows the trigger input when the gate signal is absent. On trigger ÷10 or ÷100, the dividers are reset to their zero state for approximately 5μs when the gate signal is removed and then continue to count. However, the output signal remains clamped at +10V until the gate signal is re-applied, when it follows the divider output.

Manual trigger, single cycle

23. With the TRIGGER and DIRECT buttons depressed, a single output pulse is generated each time the MAN. button is operated.

Output

24. The standard system interface output signal is provided through two parallel output sockets. These outputs are intended to drive the inputs of other modules but can alternatively feed any other load of impedance > 500 ohms. Loads < 500 ohms cause output current limiting and serious distortion of the waveform. Although the module is protected against short circuits it should not be run continuously in this condition.

25. The output is also fed through a 5.6k ohm resistor to a front panel test point. This facilitates connection of an oscilloscope for examination of the output waveform while the module is connected in a system. The duty cycle of the output waveform in the normal operating mode is either 1:1 or 1:4 depending on which frequency range is selected.

PULSE WIDTH OR DELAY MODULE PG52P2A

Trigger input

26. The module is triggered by a negative-going transition of the input through the trigger level which should be set at +5V (NORMAL) by the TRIGGER LEVEL control when the module is driven by a system interface output signal. For optimum operation above 10MHz it may be necessary to reduce the trigger level setting while at frequencies above 25MHz, triggering is unreliable.

27. The input can be driven by a wide range of waveforms e.g. low-frequency sine waves, ramp voltages etc. from any other source, the TRIGGER LEVEL control being set to select the point at which the period is initiated. Alternatively, the TRIGGER LEVEL control can be adjusted to avoid spurious triggering with noisy input waveforms.

28. The sensitivity of the trigger circuit about the trigger level is approximately 2.5V p-p for input frequencies below 10MHz, rising to approximately 5V p-p above 10MHz. The input resistance is greater than 3k ohms and the input circuitry is protected against voltages up to ±20V peak.

Period setting

29. Select the period units required (1s, ms, μs or 100ns on the left-hand bank of pushbutton switches). When using the ms and μs ranges, select the required multiplying factors (x1, x10 or x100) on the right-hand bank of pushbuttons. With the fine control in the CAL position, the period is that selected by the pushbuttons. Operation of the fine control away from the CAL position reduces the period over at least a decade range, e.g. to 25ns on the 100ns range.

Duty cycle limitations

30. The pulse width should not exceed 70% of the repetition period for outputs below 10MHz and should not exceed 50% of the repetition period for outputs above 10MHz. However, such limitations can be overcome by the use of the INVERT function on the output modules.

31. The unit can also be used to count-down the input frequency by up to a factor of 10 if the pulse width is set to an approximate multiple of the repetition period. In this case the fine period control should be adjusted to obtain a stable count-down.

Output

32. The standard system interface output signal is provided through two parallel output sockets, i.e. an approximate 0 to +10V waveform from a low source impedance (less than 100 ohms). It is intended to drive the inputs of other modules but it can alternatively feed any other load of impedance > 500 ohms; loads < 500 ohms cause output current limiting and the waveform may be seriously distorted. The module is protected against short circuits but should not be run continuously in this condition.

33. The output is also fed through a 5.6k ohm resistor to a front panel test point to facilitate connection of an oscilloscope while the module is connected in a system.

Propagation delay

34. When driven by a fast input signal, the leading edge of the output pulse occurs after a delay of typically 20ns.

STANDARD OUTPUT MODULE PG52P3A

Input

35. The P3A module is designed to accept switching inputs at standard interface signal levels. A positive signal on the selected input socket gives rise to a negative-to-positive output transition. The output returns to the negative level only when both inputs are at 0V. The output levels are reversed when the INVERT button is pressed, the output being negative while either input is positive and being positive while both inputs are at 0V. Inputs from other sources can be accepted providing they are less than ±20V peak and have rise times less than 20ns.

36. The module input resistance is greater than 3k ohms and the minimum specified input pulse width is 25ns. However, the module can operate with input pulse widths down to 16ns and at p.r.f.s. up to 30MHz.

Note ...

The p.r.f. limitation is a function of selected output level.

Amplitude control

37. Independent control of the positive and negative levels of the output pulse between 0V and +10V and 0V and -10V is provided by two fine controls

at the top of the panel. Each level is defined within 5% of 10V at the maximum end when the output is loaded by 50 ohms.

CAUTION ...

The module should not be operated with the level controls less than the equivalent of 1V apart.

Attenuator

38. The full +10V to -10V output into 50 ohms is provided at the output socket when the DIRECT ± 10V pushbutton is depressed. The level can be attenuated to ± 5V, ± 2V or ± 1V by operation of the appropriate pushbutton. Further attenuation to ± 0.5V, ± 0.2V and ± 0.1V can be obtained by depressing the ÷10 pushbutton.

Note ...

The ÷10 facility is not available with DIRECT ± 10V selected.

Waveshape

39. When terminated by 50 ohms the output rise and fall times for any large step on the ± 10V range is typically 5ns and perturbations or preshoot, overshoot, etc., are less than 5% of the maximum amplitude. The unit is dc coupled and droop is negligible. Use of the attenuator may introduce a further 1ns to the rise time together with extra perturbations of 20mV (50mV above 10MHz) noticeable only on the lowest ranges.

Note ...

Low level pulse waveforms without added perturbations can be obtained if external 50 ohm coaxial attenuators are used in the output lead.

Output impedance and termination

40. The unit provides a low output impedance on the DIRECT ± 10V range and a 50 ohm output impedance on the attenuated ranges. It is designed to work into a 50 ohm coaxial system and only under these conditions are the full output rise time and perturbation specification met.

Note ...

Excessive overshoot will occur if the output is not connected to the load via a 50 ohm coaxial cable such as the PL43.

41. If a high impedance load is to be driven, the 50 ohm termination TP19 should be used at the load end of the cable. With the limitation of excessive over-shoot, the unit can be used into high impedance loads when approximately twice the stated output voltage will appear on the attenuated ranges; not more than ± 11V will appear on the DIRECT ± 10V range.

Note ...

On attenuated ranges only, the unit can drive into low impedance or short circuit loads.

Propagation delay

42. The propagation delay between the application of an input pulse and the subsequent output transitions is approximately 20ns for normal outputs and 25ns for inverted outputs. There may also be a differential delay of 3ns between positive and negative-going edges.

VARIABLE SLOPE OUTPUT MODULE PG52P4A

Input

43. The PG52P4A module is designed to be driven from the standard +10V PG52 system interface signals from one of the range of waveform generating or processing modules. A positive input signal on either of the input sockets normally gives an output rising from negative to positive at the selected slope. The output returns to the negative level when both inputs are at 0V. This action is reversed when the INVERT button is operated, the output falling to the selected negative level while either input is positive and returning to the positive level when both inputs are at 0V.

44. Other pulse sources of > 10V but not greater than ± 20V peak can be used if the rise and fall times are less than 20ns. The input resistance is greater than 3k ohms, minimum input pulse width is 25ns and maximum pulse rate is 8MHz.

Amplitude control

45. Independent control of the positive and negative levels of the output pulse between 0V and +10V and 0V and -10V is provided by two controls at the top of the panel. Each level is defined within ± 5% of 10V at the maximum end when the output is loaded with 50 ohms. At the minimum end of each control (0V), the output level is within 200mV of 0V if the pulse amplitude is greater than 1V.

Note ...

The slope must be consistent with the pulse width if the selected levels are to be realised.

Slope control

46. The left-hand bank of pushbuttons selects the range of ns/V, µs/V or ms/V while the right-hand bank selects the multiplying factors, 0.1 to 1, 1 to 10 or 10 to 100. The 0.1 to 1 range is not available for ns units. Linearity on all but the fastest ranges is typically 1% after an initial 500mV step. On the fastest range (1ns/V to 10ns/V), the minimum rise time for the full 20V pulse is less than 20ns, but if the amplitude is reduced, the rise time may not drop below 10ns. On the 1ns/V to 10ns/V range there is also some rounding and the selected slope is maintained only between 20% and 80% of amplitude. If the slope control is set to prevent the output level from reaching its final value within the pulse width a triangular waveform is produced and this may introduce some distortion at the

change-over point at some settings of amplitude and slope.

Output impedance and termination

47. The circuit has an output impedance in the order of 5 ohms and is designed to work into a 50 ohm load. When operating into a high-impedance load the 50 ohm termination (TP19) should be used at the load end of the output cable to minimise distortion and ringing although such phenomena may be negligible at slower rise and fall rates. The output circuit is protected against short circuit but pulse distortion may occur if load resistance is less than 50 ohms.

CAUTION ...

The unit should not be run continuously into loads of less than 50 ohms impedance.

Propagation delay

48. The propagation delay between the application of an input edge and the subsequent change of output voltage is in the order of 35ns for the leading edge and 75ns for the trailing edge of a pulse. Thus with an input pulse of 25ns, output pulse widths at the fastest slope may not be less than 75ns. For this reason the maximum frequency of this unit is limited to 8MHz.

PASSIVE SUMMING MODULE PG52P5

49. The PG52P5 module contains two independent resistive networks as follows:

(1) A two-input network which is a symmetrical delta circuit between the two input sockets and the output socket.

(2) A three-input network which is a symmetrical 4-part network allowing the summation of three input signals on one output.

50. The resistive networks may be used singly or in combination to sum a number of inputs from 50 ohm sources onto a single 50 ohm output. By this means, complex waveshapes may be built up from separate pulses, sinewaves or other waveforms. Alternatively, the networks may be used as power dividers to split a single input from one 50 ohm source into a number of 50 ohm outputs. When used in this mode, the output signals are one half or one third of the applied input signal level depending on which network is being used.

Operating constraints

51. The peak signal voltage applied to any input should not exceed 10V. When driven by an output module PG52P3A, only the 5V or lower ranges should be used (50 ohms output impedance) since the 10V range has a low output impedance. If the PG52P4A or any other low-impedance source is used a 50 ohm termination such as TP19 should be connected to unused inputs.

POWER OUTPUT MODULE PG52P6

Preparation for use

CAUTION ...

Before inserting the PG52P6 module into the main frame ensure that the mains supply input selector is set correctly.

52. To change the input supply selector, remove the module top cover and remove the switch locking plate by unscrewing the two fixing screws. Slide the selector switch over and then turn the plate through 180°. Secure the two fixing screws and replace the top cover. Ensure that fuses FS4 and FS6 (main frame) and FS601 (PG52P6) are rated as follows:

Mains Supply	FS4 and FS6	FS601
100V to 130V	2A slow blow	4A
200V to 260V	1A slow blow	4A

53. The module will only operate in the right-hand half of the main frame where the internal cooling is adequate. Preferably it should be inserted in the extreme right-hand position but it may be used with one or two single-width modules to its right.

Ventilation

54. The module requires effective forced-air cooling within the main frame. It is important that the input and output areas on the rear and right side of the frame are not restricted. The frame must be operated with a full complement of modules or blank panels to ensure correct air circulation. To minimise power dissipation, installed modules not being used can be inserted upside down in the frame when they will not be connected to the internal supplies.

CAUTION ...

When using the module under full power into the TP21, ensure that ventilation of the TP21 is not restricted.

Input

55. The module is designed to be driven at the system interface levels (+10V) but other input voltages greater than +5V with rise and fall times less than 10ns can be used, maximum input voltage is ± 20V peak. Input resistance is approximately 3k ohms.

Note ...

The output level is determined by transitions of the input signals rather than the dc level and, after switch on, the state of the output is not determined until the first input transition is received.

Output

CAUTION ...

The unit is capable of delivering an output power of 50W. If used into a load with power dissipation of less than 50W the mean output power must be limited by restricting the input duty cycle.

56. With the positive (+) button only pressed, a positive input signal will drive the output from ground to a positive level between 10 and 50 volts, as determined by the OUTPUT LEVEL control on the front panel. With the negative (-) button only pressed, the output will swing from ground to the same negative level.

57. There is sufficient range on the level control to give an e.m.f. of 60V, but if 50V is exceeded when driving into a 50 ohm load the current overload circuit will operate. However the over-range facility can be used into a high impedance as described in paras. 63 and 64.

58. Operation of the INV button will cause the output to switch from the selected +ve level to ground for the duration of a positive input pulse. This facility overcomes any maximum mark/space ratio limitation of the input signal and allows the output duty cycle to approach 100%.

CAUTION ...

The PG52P6 module must not be operated into inductive loads.

59. The specified output will only be achieved when a non-reactive 50 ohm load and coaxial connector such as the PL43 is used. The output is protected against operation into short circuits, capacitive loads or any loads less than 50 ohms.

Protection

60. The internal power supply has a current-limiting characteristic such that it will supply a mean current of 1A at 50V output, 0.5A at 25V output etc. Thus, if any load less than 50 ohms is connected, the power supply voltage will shut down until such a load is removed.

61. Further protection is provided to detect any transient change of output current greater than 1A. In this condition the drive signals are inhibited and the 50V power supply shuts down for approximately 2ms. After this period the supply recovers and if the overload has been removed the unit will function normally. However, if the overload is still present the trip cycle will be repeated.

62. In order to avoid exceeding the maximum output-stage switching speed of 3MHz, an automatic protection circuit causes a count-down of input frequencies above 3MHz and inhibits the generation of consecutive pulses with leading or trailing edges separated by less than 330ns. As this can give a change of output duty cycle, particular care should be taken when operating with closely spaced pulses into loads less than 50W rating even though the input duty cycle is low.

Termination

63. If 100% duty cycle is required the output load must be capable of dissipating 50W. TP21 is provided for use as a 50 ohm 50W load having a through resistance of 50 ohms and when used with the shorting cap, provides correct termination of the cable PL43. An output can then be taken via a "T" adaptor from the input of the load to drive into a high impedance. Alternatively without the shorting cap fitted, 1 amp pulses can be taken from the output of the load into low impedance loads (>>50 ohms).

64. If some overshoot and ringing can be tolerated when driving a high impedance load, the TP21 can be connected directly to the output of the module as a 50 ohms through load (series resistor) to provide back termination of the cable used. In this way it is possible to use the over-range capability of the level control and achieve a 60V pulse into a high impedance.

Note ...

The use of a low-capacitance probe such as the Tektronix P6035 is recommended when monitoring the waveform across the input of the load.

FAST OUTPUT MODULE PG52P7

Inputs

65. The front-panel INPUT sockets A and B are connected to function as an OR gate and are normally driven from 0 to +10V system interface levels. The module can also be operated from an external pulse or sinewave source with a minimum input signal swing of 0 to +6V with a rise time of less than 10ns and maximum input levels of ±20V peak.

66. The input circuits are directly coupled and operate within the following frequency ranges:

(1) DC to 50MHz from a pulse source

(2) 10MHz to 50MHz from a sinusoidal source.

Outputs

67. For the duration of a positive input signal, the two OUTPUT sockets provide simultaneous positive and negative-going signals with respect to ground. The POS OUTPUT LEVEL and NEG OUTPUT LEVEL controls allow independent variation of the output voltages from less than 2.5V to greater than 5V. Typical rise time is less than 1ns and the fall time is less than 2ns. The pulse top abberation is less than 8% of maximum pulse height and the output must be connected to the load through a good quality 50 ohm cable and connector such as the PL43 or PL81.

68. Each output is essentially a variable current source in the range 50mA to 100mA and is intented to drive a 50 ohm load. Operation into short or open-circuit conditions or capacitive loads will not damage the current sources but they must not be driven into inductive or active loads.

69. The maximum output voltage is limited to approximately 10V for loads greater than 100 ohms. In this condition the output will be considerably distorted but if the load is not excessively capacitive, the leading edge transition time can still approach 1ns. The fall time depends upon the load and is likely to be of a long duration.

Delay

70. In addition to the propagation delay of approximately 25ns introduced by the module, a further delay can be introduced on the leading edge by means of the START DELAY control. This control can be used to reduce the output pulse period by up to 50ns. However, the full range of the control is available only if the recovery time between the end of one input pulse to the beginning of another is greater than 500ns. Reduction of the recovery time reduces the range of delay and conversely, smaller delay times require smaller recovery times, 20ns recovery being necessary for a 15ns delay.

71. If the start delay is greater than 30ns, the output rise time is likely to increase beyond 1ns. To produce the specified minimum output pulse width of 10ns the module should be driven from the 25ns minimum output of a pulse width delay module and a start delay of 15ns applied. As this implies a 20ns recovery time, the overall repetition period of 45ns is approximately equivalent to a frequency of 22MHz.

72. Above 22MHz, the START DELAY control offers some control of output mark/space ratio with square-wave or sinusoidal inputs. An output can be obtained up to approximately 50MHz when externally driven if the START DELAY is set to its optimum setting.

WORD GENERATOR MODULE PG52P8

Inputs

73. The inputs are normally intended to be driven from a clock generator P1A, a pulse width or delay unit P2A, a gate unit P9 or another word generator P8. Alternatively, the unit will operate from another pulse source within the specified limits. A minimum excursion of 0 to +5V is required, having a rise time of <20ns. The maximum permitted excursion is ±20V peak. Slower rise time pulses can be used on the clock or start inputs if the NRZ output mode or dc coupled start are used.

74. The clock input operates on the negative-going edge of the input waveform. The maximum specified clock frequency is 10MHz but the module will operate up to 13MHz. The minimum positive or negative duration of the clock period is 50ns, thus at 10MHz and above, an approximate square wave is required for the clock input. The start circuit is initiated by a positive-going input pulse, the duration of which should not be less than 20ns.

75. The outputs are at system interface level and have an output impedance of less than 100 ohms. The module can drive up to four other modules in the system or alternatively, any load of greater than 500 ohms. Loads less than 500 ohms will cause current limiting of the output stage and distortion will result. Short circuit protection is provided but the unit should not operate in this condition continuously.

76. Each output is also available via a 5.6k ohm resistor on a test point which is intended for oscilloscope monitoring whilst setting up.

Function

77. The word length is selected by the rotary switch and can be any number of bits between 1 and 16. The word pattern within the selected word length is set by the appropriate toggle switches, 1 to 16, which should be down for a "mark". Switches outside the selected word length have no significance.

Word outputs

78. The word output waveform can be selected to either of two modes by the NRZ-RZ switch. Waveform B of fig. 1 shows the "non-return-to-zero" mode (NRZ) of a 10 bit word. Each negative-going transition of the clock input signal shifts the output waveform through the selected pattern. The output goes positive for the full clock period of each selected bit and remains positive if two adjacent bits are selected (as bits 7 and 8 of waveform B).

79. In the "return-to-zero" mode (RZ) the word output (waveform C) is normally positive and gives an approximate 60ns negative-going pulse at the beginning of each selected bit. This can then be used to trigger a PWD module P2 to provide the conventional RZ waveform shown in trace D. The width of the positive-going mark pulses is determined by the PWD setting.

Last bit output

80. In addition to the word output, the duration of the last bit of any selected word length is marked by a positive-going pulse as shown in waveform E. This output is present whether or not the last bit of the word is selected as a mark on the word output.

Repeat mode

81. With the start switch set to REPEAT the selected word pattern is continuously cycled under control of the clock signal, independent of the start input, as shown in waveform A to E.

External start

82. With the start switch set to EXT, a word pattern will not start while the input is low. An internal switch, with access through one of the ventilation holes in the lower edge of the left-hand cover, determines whether a single word is initiated at each positive-going edge of the start input or, words continue to be initiated while the start signal is high. In early models this function is determined by link "aa" (open for ac or linked for dc).

83. AC coupled mode waveforms F to J (fig. 1) show the sequence following a positive-going transition of the start input when a single word is generated independent of the start pulse width. The word output is in synchronism with the clock. The presence of the start signal is recognised at the positive-going transition or "back edge" of the clock signal and the first output pulse period begins at the following negative-going clock transition.

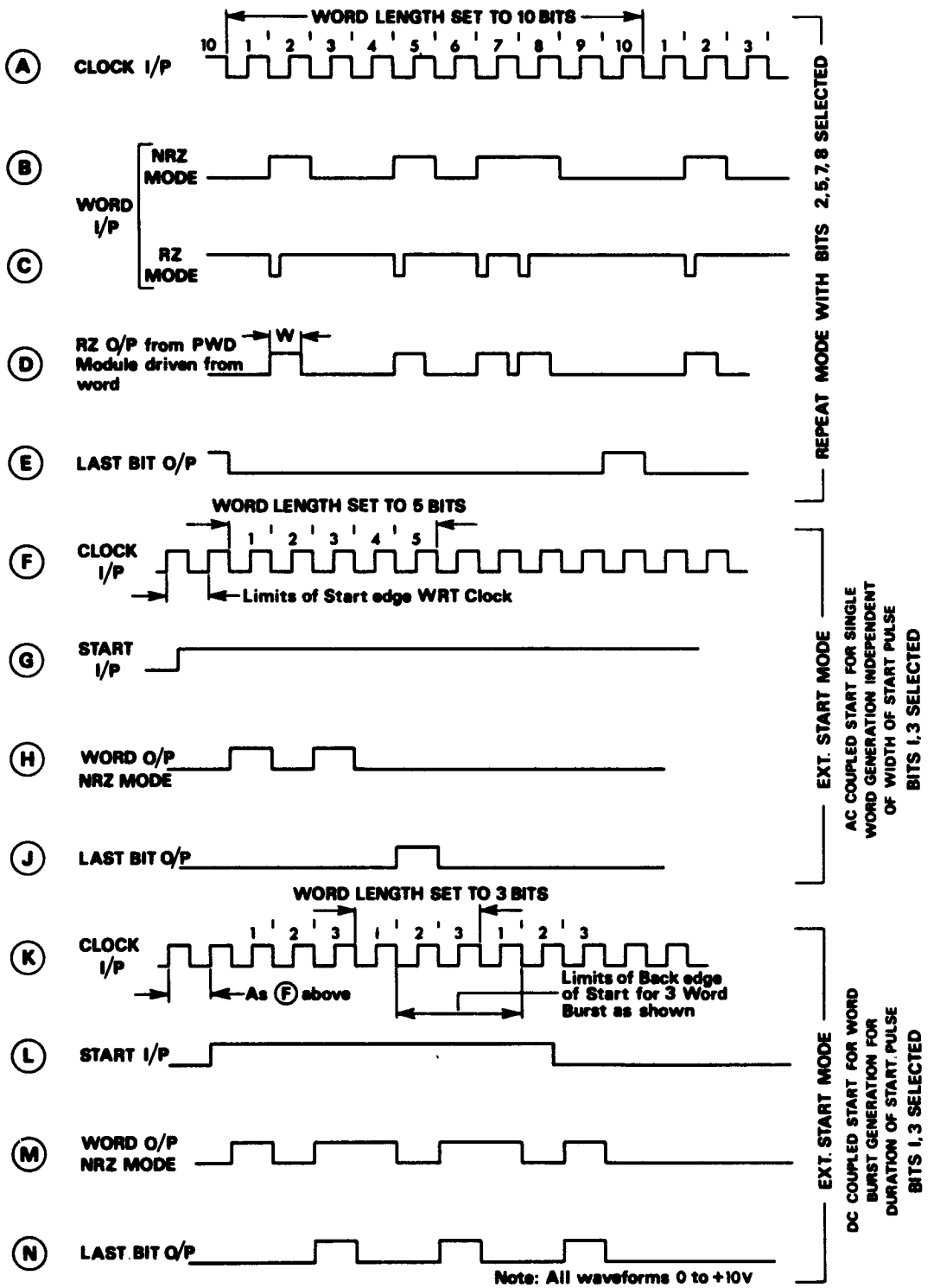

Fig. 1 PG52P8 function timing diagram

This sequence avoids the ambiguity which would occur when a start signal is applied coincident with a negative-going clock edge. As fig. 1 shows, the start signal can occur at any time between two positive-going transitions of the clock signal for the word to start at the following negative-going clock edge.

84. DC coupled mode waveforms K to N (fig. 1) show the sequence where words are initiated for the period that the start signal is high. A similar acceptence sequence occurs at the start of the word burst and if the positive start signal is removed before the end of the first pulse period of the first word, a single word only will be generated. However, if the start signal is prolonged beyond the first pulse period of the first or any subsequent word, it is accepted as a start for a further word sequence. The removal of the start signal does not shorten any word sequence for which a start signal has been accepted.

Applications

85. The module will extend the application of the PG52 system to assist in design and test of digital computer, data handling, PCM and similar systems. However, it can also be used as an aperiodic frequency divider which can be set to divide by any ratio up to 16. Two modules can further be connected to divide by any number which is the sum or the product of any two numbers between 1 and 16. A further application of the module is to produce a 1:1 square wave from a double-frequency signal by setting to a 2 bit word with one bit marked.

GATE UNIT MODULE PG52P9

Inputs

86. The inputs are intended to be driven by the system interface signals. However, the unit will operate from any other signal source which provides an input voltage swing of +0.5V to +5V; the maximum input voltage should not exceed ±20V peak. The unit will not always respond to input pulses less than 20ns in width of mark or space, giving a maximum operating frequency for square wave inputs of 25MHz.

Outputs

87. Each output has an impedance of less than 100 ohms and provides standard system interface signal levels. The outputs can drive any other modules in the system or, alternatively, any other load with an impedance of >500 ohms. Loads below 500 ohms will cause current limiting of the output stage and hence distortion will result. Protection against short circuit is provided but continuous operation in this condition should be avoided. Each output is also fed through a 5.6k ohm resistor to a front panel test point for monitoring with an oscilloscope.

Function

88. With the four toggle switches of any one gate in the NORMAL position, a high signal applied to any one input will drive the output high. When all four inputs are low, the output will be low. Operation of the output INVERT switch will invert the output level so that the output will be low if any one or more inputs are high, or high if all inputs are low.

89. Operation of any input INVERT switch will invert the function of that input, i.e. the normal output will be high if that input is low. Since an open circuit input is the equivalent of a low, unused inputs should be switched to NORMAL.

Propagation delay

90. When initiated with a fast input transition (10ns), the propagation delay before the output transition occurs will be less than 20ns.

Applications

91. The module is intended to increase the versatility of the PG52 system in the generation of complex pulse waveforms. Its most common applications are:

(1) To extend the two-input capability of all output modules when it is required to drive them from three or more sources. Eight inputs can be accommodated in all, when each output of the P9 is connected to an input of the power output module.

(2) To detect coincidence of two or more input pulses. If each input used is switched to INVERT, output will normally be positive and return low only when all inputs are high.

(3) To inhibit or blank one or more pulses from a pulse sequence. In this case the pulse sequence is applied to one input and that input and the output are set to invert. The blanking input is normally applied to another input. The output is then held low while the blanking input is high but follows the pulse sequence while the blanking input is low.

(4) To form a set/reset bistable. The two gates of the module can be cross-coupled by connecting the inverted output of each gate to the input of the other. A high signal to any unused input of one gate will then drive the bistable to lock in one direction and to the other gate to lock in the other direction. A more unusual application is to connect the normal output of either gate directly back to one of its own inputs. This forms a bistable which can be set by a 'high' applied to any other input of that gate but can only be reset by breaking the feedback path; hence a pulse detector with manual reset.

TRIGGER MODULE PG52P10

Inputs

92. (1) If the module is to be driven by normal system interface signals, set the TRIG LEVEL control fully clockwise to +5V and do not actuate the ATTEN 10:1 button.

(2) The module can be driven from any external source at a frequency from dc up to 30MHz. In normal operation, the TRIG LEVEL control can be set to any potential between +5V and -5V. The sensitivity about 0V is better than 500mV

peak-to-peak with input resistnace greater than 10k ohms, but the input signal should not exceed ±20V peak. If it is required to trigger from higher amplitude input signals (up to ±200V peak or 100V r.m.s.) the ATTEN +10 button should be actuated.

Line trigger

93. When the INT LINE TRIG button is actuated, the external signal input is disconnected and replaced by a signal derived from the incoming supply. Assuming the incoming supply is sinusoidal and of 230V (or 115V) amplitude the range of the TRIG LEVEL control is approximately 10% to 90% of the peak-to-peak amplitude.

Normal/invert

94. In the normal condition, the trigger output is positive while the input signal is above the trigger level and is at 0V when the input signal is below the trigger level. In the invert condition, the trigger output is positive when the input is below the trigger level and is at 0V when the input signal is above the trigger level. Thus if the trigger output is used to trigger a PWD P2 module which is initiated by the negative-going transition, the NORM and INV switches can be used for slope selection on external trigger inputs.

Count down ÷2

95. When the COUNT DOWN ÷2 button is actuated, an aperiodic binary divider stage is introduced between the trigger circuit and the trigger output. In the normal input mode it is stepped by the negative-going transition of the input signals. In the invert mode, it is stepped by the positive going transition.

96. The ÷2 facility is normally used when the generation of an accurate 1:1 square-wave is required. An input signal of twice the required output frequency is then used. Maximum input frequency is 30MHz.

Trigger output

97. The +10V TRIGGER OUTPUT provides a system interface level output with an impedance of less than 100 ohms. At test point is also provided for monitoring purposes.

Trigger pulse output

98. The TRIG PULSE OUTPUT is independent of the trigger output and provides a 1V pulse into 50 ohms at every negative-going transition of the trigger output. The pulse can be +ve or -ve with respect to ground by selecting the appropriate push buttons. Pulse width can be set to any width between 25ns and 200ns by the TRIG PULSE WIDTH control.

99. This output is intended to be used as the prepulse output of a conventional pulse generator to provide a pulse at the beginning of a delay period. For this application, the P10 trigger module should be inserted in the signal path of a system between clock and delay generating modules.

100. The output impedance is approximately 50 ohms and the rise time is approximately 5ns. The output waveform cannot be relied upon if the duty cycle is set to be greater than 50%, i.e., if the p.r.f. is set to exceed 2.5MHz at 200ns width and 20MHz at 25ns width. The output voltage is approximately 2V on open circuit and the output is fully protected against short circuit.

Propagation delay

101. The propagation delay from trigger input to trigger output is approximately 30ns. The delay between the leading edge of the trigger pulse and negative transition of the trigger output is approximately 10ns.

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