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Colin Hinson
In the village of Blunham, Bedfordshire.

TELEGRAPH & DATA SIGNAL ANALYSER

TREND®

maintenance manual

TELEGRAPH & DATA SIGNAL ANALYSER

HANDBOOK

TYPES 1A AND 2A

Applicable to Equipments with Serial Nos. from 22201.

TREND COMMUNICATIONS LIMITED
St. John's Estate
Tylers Green
High Wycombe
Bucks HP10 8HW
England.

Phone: Penn (049 481) 3721
Telex: 83625

Issue 4 April, 1976.

AMENDMENTS TO T.D.S.A. DATA

Parts List 8052

1) Item 45 — Add Alternative:
TRA 000670 Alt. Transistor 2N 3440 - Motorola.
TRA 000672 Alt. Transistor 2N 3440 - R.C.A.

2) Item 52 — Insert DIO 002067 Diode BAX 16 - Mullard - Qty.1. D2.

Parts List 4639

3) Item 29 — Insert DIO 002032 Diode BZY 88 C3V3 - Qty.1. D1.

Parts List 7425

4) Item 56 — Delete 2355.
Insert 2356.

Parts List 7271

5) Item 26 — Add N.B. Fit 17 and 24 after testing.

6) Item 30 — Insert CON 000154 I.C. Socket 14 way Cambion. Qty. 1.

Parts List 7930

7) Item 12 — Delete RES 000355 Res. 12K.
Insert RES 000351 Res. 8K2.

Parts List 7278

8) Item 19 — Delete CAP 000858 Cap. 470pF.
Insert CAP 000856 Cap. 100pF.

Circuit Changes

Fig. 5 — Capacitor C1 delete 470pF.
insert 100pF.

Fig. 6 — Diode D1 insert in +15v line as illustrated below.

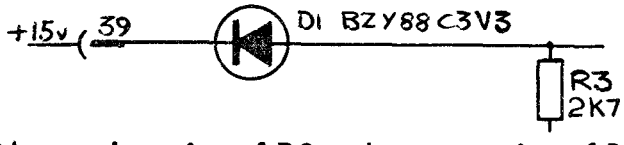


Fig. 8A — Insertion of D2 and reconnection of R10 as illustrated below.

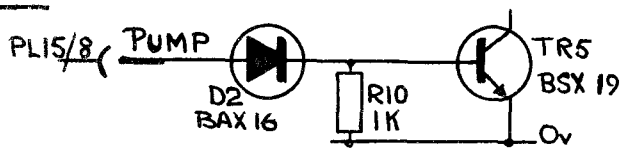


Fig. 9 — Resistor R2 delete 12K.
insert 8K2.

EQUIPMENT TDSA

HANDBOOK AMENDMENTS

PUB. No. 222.252

No.	Date	Authority	DETAILS	C/O
1	8.3.76	2781 2598 2544	COMPONENT LIST CHANGES MOTHER BD. R17 to be 1K8. R30 to be 8K2. R67 to be 180K C20 to be 0·01 ERIE HI-K/BIN/10222	ISS 4. April 76
2	"	2598 2544	RV2 to be 1K. RV3 is to be 500K.	"
3	"	2649	X AMP BOARD Add C16-100p C1 to be 0·1. C17 - 0·1uf TR4 to be 2N2905A D2:- delete.	"
4	"	2619	Y AMP BOARD C8 to be 0·01uf. 25v E no Disc Ceramic.	"
5	"	2746. 2592 2724 2573	LOGIC BOARD 1 C7 to be 5-50p ERIE Trimmer 557-0006. TR1 to be BFX87 C6 to be 120p 30v + SUFFIX 11S X1 to be Cathodeon A-C1973BF TR3 " " BFY51 TR5 " " "	"
6	"	2598	EHT. BOX R4 to be 1M R5 to be 330K.	"
7	"	2840 2718	FRONT PANEL LP1 to be PLASTRONICS 3SR-1-F4-AC-R-2 N-6. RV4 AND RV5 to be BOURNS CM1ZN-10K. DELETE R1.	"
8	"	2796 2759. 2573	FIGURE CHANGES FIG 2B R30-8K2 RV3 - 500K. R67-180K D2-BAX16 (EHT. TUBE BASE) FIG 3 TR1 - BFX87. C6 - 120p TR3, TR5 - BFY51. C7 - 5-25p	"
9	"	2981 2649. 2637	FIG 3A TR4 - 2N2905A. R8 - 1K2. R9 - 18C FIG 7 Delete IC 2C-11.10 CONNECT TR1 collector to IC 21-2.	"
10	"	2598 2619	FIG 9 R4 - 1M R5 - 330K FIG 8C C8 - 0·01uf Delete C15.	"
11	"	2565	FIG 10A+B RV2 - 1M Delete resistor above LP1. CHANGE Ref V24 to V28.	"
12	"	2674	FIG 11A. SK8 pin 24 add 'SS' to FIG 2A'.	"
13	"	2686	FIG 21. C10. Delete.	"
14	9.3.77	3202	PL 8050 } Item 36 Add R30. QTY Now 9 Add Item 75 Part 00/491 for 10K Daystrom 537-CO4S. RV4 8056 } Item 40 Delete R30 QTY Now 1 ON FIG 2G (8070) Insert RV4 (10K) between R30 & R29. R30 Now 4K7	
15	7.12.76	3157	PL 8043. Delete Item 11. 50 to 50 uf CAP Insert CAP00137I 47uf 250v. C1a Insert Item 12 CAP00137I CAP 47uf 500v C16 ON FIGS 11A & 11B Delete 50 to 50 Renumber as PLs	
16	21-11-77	3547	FIG 9 DELETE + 5250 V INSERT 5500V. DELETE FIG 2(B) FLYING HEAD TO FLHT. INSERT FIG 2A. FIG 2 DELETE 5250 V (TUBE CONNECTION) INSERT 5300 V.	

CONTENTS

INDEX TO FIGURES

CHAPTER 1

GENERAL DESCRIPTION

The Trend Telegraph and Data Signal Analyser (T.D.S.A.) is a portable, mains-operated instrument for testing tele graph and data transmission equipment. In conjunction with the Trend Telegraph and Data Message Generator (T.D.M.G.) it can be used for assessing the quality of telegraph and data transmission links.

The basic instrument (T.D.S.A. type 2A) provides for measurements of distortion on both start/stop and continuous (synchronous or "isochronous") data streams, which can be received over a wide bit-speed (or baud) range. These measurements can be made in series or shunt with the line being considered, accommodating the wide range of signal levels encountered on telegraph and data transmission equipment. The measurements are represented in the form of self-calibrating lines of dots on a cathode ray tube (C.R.T.). The C.R.T. can also be used to display the actual waveform of the data being measured.

The T.D.S.A. type 1A has all the facilities of the type 2A with the addition that it can be used to make error measurements on the start/stop messages and Pseudo-Random pattern generated by the T.D.M.G. It can also be used for parity checks on any start/stop characters which have "parity bits".

Mechanically, the unit is of robust and rigid construction. The two side panels are aluminium extrusions, as also is the rear panel. The front panel is a plastic injection moulding whilst the top and bottom covers are of black vinyl-covered sheet steel. The carrying handle is attached to the side panels and can be set under the unit to act as a stand. The mains lead is stored in the lid and when in use plugs into the rear panel.

Units from Serial No. 22201 differ from equipments with Serial Nos. up to B/N 22006 in that the Mother P.C.B. has a cut away to facilitate the flow of air over the E.H.T. and transformer unit and the X and Y deflector circuits to the C.R.T. are arranged on separate P.C.B's. mounted transversely behind the equipment front panel.

GLOSSARY OF TERMS

Term	Description
AKJ	Manufacturer's reference to drawings and/or assemblies.
A.O.T.	ADJUST ON TEST - Normally refers to Resistors or Capacitors, the value of which is not determined until the equipment is in the FINAL TEST STAGE.
5 BCH	5 Bit Character.
BCD	Binary Coded Decimal.
BYX	Manufacturer's Prefix Code - Diodes.
CAL	CALIBRATED - Switched to FIXED SPEEDS.
CE	Count Enable - Signal allowing Count to Start.
CEP	Count Enable - Parallel inputs to the BCD Decode Counter.
CET	Count Enable - Trickle inputs to the BCD Decode Counter.
CHIP ENABLE	Signal gated to the eight parallel outputs B1 - B8. When at 0v allows the outputs to take up the state of the 8 Bit word selected.
C-L Counter	Character Length Counter.
CO DOWN	Count '0' down signal/period of the main 50-way UP/DOWN counter.
COT	COUNT 0 Tens) UP/DOWN Counter count decode signals.
COU	COUNT 0 Units)
C.R.T.	Cathode Ray Tube.
DA	Digital to Analogue - Binary Weighted outputs.

Glossary of Terms (Contd/)

Term	Description
DATAN	'Normalized Input Data' signal.
D.D.	Display Distortion.
DIC	Display Input Character.
DM	Manufacturer's Prefix (National Semi Conductors Ltd.)
DRS	Distortion Reset.
EE	Expand Early - Logic signal.
EHT	Extra High Tension - refers to voltages.
EL	Expand Late - Logic signal.
ETC	Terminal Count.
HSS	High Spped Stroke - Signal '100 x Element Rate Clock' selected by speed BITS/SEC switches.
IC	Integrated Circuit.
I/P DATA	DATA received into the equipment. (The opposite of DATA being transmitted from the equipment as in the TDMG - O/P DATA).
JK J-K	) These are input terminals/connections to Bistables.
LAB.DIC	Combined Signal - Last Bit and Display Input Character.
LK1	Link 1 - Straps placed on Printed Circuit Boards. These may be broken or linked independant on facilities required.
LOST	'Look at Stop' signal.
M	Prefix M relates to a MEMORY DEVICE.
MD	Divider Bistable.

Glossary of Terms (Contd/)

Term	Description
MFB	Set by 'COUNT 49 UP' signal from UP/DOWN Counter to produce the final H.S.S.
MHS	Bistable which functions as ÷ 2 to produce the final HSS.
ML	Message Length Bistable.
MPL	Phase Lock Bistable.
MRD	Retimed Data Bistable.
M.R.E.	Psuedo Random Errors Bistable.
MST	Character Length Counter (Select Trace) Bistable.
MS1	START/STOP control Bistable.
MST1	MST1 - MST4 - four stage BINARY COUNTER.
MUP	The UP/DOWN Counter control of the main 50 way UP/DOWN counter. It is 'set' (MUP high) during the 'late' half cycle and 'reset' (MUP low) during the 'early' half cycle.
** N	Signifies NO to the questions posed in Flow Diagram(6)
NTD	Negative Transition Detected Signal.
PB1	Push Button Switch number 1, PB2 etc.
PEV	Parity Even.
POD	Parity Odd.
P-R	Pseudo Random.
PTD	Positive Transition Detected Signal.
PUMP	Signal to the X Amplifier. Square wave containing as many positive edges as there are dots required across the Cathode Ray Tube (C.R.T.) screen.

Glossary of Terms (Contd/)

Term	Description
R.O.M.	Read Only Memory.
SKT 1.	Socket 1.
Shroud	The cover protecting the connections on a plug.
Strobe	Strobe pulse - pulse much shorter than a repeated waveform, for examination of a display. Strobe - general term for detailed examination of a designated phase or epoch of a recurring waveform or phenomenon. Enlargement or intensification of a part of a waveform exhibited on a Cathode Ray Tube (C.R.T.)
tag	type of connection.
TC	Terminal (Final) Count.
TCA	Terminal Count output of the first (1st) stage of Counter 2, the subsidiary 50 way UP/DOWN Counter.
TCB	Terminal Count output of the second (2nd) stage of Counter 2.
TDD	Negative going Transition marker pulse.
TDN	Negative Transition Display Drive signal to 'y' Summing Amplifier.
TDP	Positive Transition Display Drive signal to 'y' Summing Amplifier.
TDS	Transition Detected Signal from Input Data Returning and Transition Detection circuit.
** 'y'	Signifies Yes to the question posed when using the Flow Diagram (6).
$\frac{Z}{\overline{Z}}$	) The complimentary outputs of the Eight Input) Multiplexes 9312 (Fig. 13B).

** The flow diagram (Dgm. 6) is used to pose questions to which there is a Yes (y) or No (N) answer. To follow the flow diagram, ask the question posed in the diamond ◇ . Follow the route indicated by the answer y or N.

CHAPTER 2

SPECIFICATION AND CONTROLS

2.1 Input Signals

The T.D.S.A. can accept both high level telegraph signals and low level data signals, and measurements can be made in either a shunt mode presenting a high impedance greater than 100K ohms or in a series loop mode, with a series impedance of 18 ohms. The shunt impedance may be switched to 1K ohm if desired.

2.1.1 The high level signals are connected to the upper input socket and referenced to the Telegraph Earth socket. Double current or Single current either polarity can be accepted as determined by the input mode switch.

2.1.2 The low level signal input is connected to the lower input socket and is referencedto the Common socket. This input is a C.C.I.T.T. V28 termination and accepts bi-polar signals in the range 3-25 volts.

2.1.3 The Series/Shunt mode switch is mounted on the rear of the instrument and the type of operation should be selected before any signal is connected to the instrument.

The high level input signals can be up to ±150 volts for shunt measurements or up to ±150mA for series measurements. When operating in a series mode the input is accepted on the high level socket and returned through the Telegraph Earth socket, in this mode the Telegraph Earth socket must not be connected to Protective Earth.

2.1.4 Start Pulse polarity can be selected by the 'Start' toggle switch to accept signals with negative or positive 'Start' polarity.

2.1.5 Amplitude Threshold Control: A calibrated potentiometer control mounted on the rear panel allows transition threshold to be adjusted. The threshold is defined as the point at which a change of state from Mark to Space or Space to Mark is recognised.

The calibration from 5 to 100 indicates volts for shunt measurement and mA for series measurements.

2.2 Speed

Two separate oscillators are provided, the first being a crystal controlled oscillator from which 21 fixed speeds are derived, the second a variable oscillator which allows any speed over the full range to be selected. Selection is by the Cal/Uncal switch.

2.2.1 Crystal oscillator speeds in bits/second.

37.5, 45, 50, 75, 90, 100, 110, 150, 200, 220, 300, 400, 600, 900, 1200, 1800, 2400, 3600, 4800, 7200, 9600.

Accuracy and stability are better than 0.01% and 0.005% respectively.

2.2.2 The variable oscillator is used in conjunction with the range selector switch and allows ±20% variation on any selected switched speed. Thus continuous coverage is provided over the range 30-11, 500 bits/second.

This oscillator has an accuracy of 2% and a long term stability of 1%.

2.2.3 An external timing source can be used to drive the T.D.S.A. This can be at bit rate or 100 times the bit rate required, and is accepted via a socket at the rear of the instrument as described in para.2.7.1.

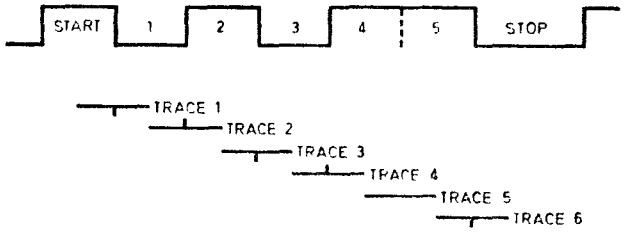
The type of signal required is:-

a) a rectangular waveform to V24 specification.

b) a rectangular waveform 0 to +5V.

2.3 Start/Stop Distortion Measurement

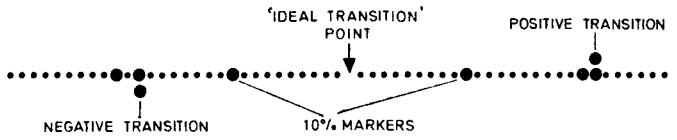
2.3.1 Start/Stop information is generated on a character by character basis, and the receiving equipment is prepared to receive each character by the recognition of a start element. Measurement must therefore be referenced to the leading edge of each start element. Distortion is defined as the displacement of a transition from the ideal instant expressed as a percentage of the information element. The T.D.S.A. inspects each transition over a range covering 49% early to 49% late, about the ideal transition point and these transitions are displayed on self calibrated horizontal trace displays.



Diag. 1

Diag.1 shows a typical 5 unit coded character with single bit start element and a $1\frac{1}{2}$ bit stop element. The diagram also shows the time relationship of the 6 "distortion display" traces, relevant to the 6 possible "transition positions", which are brought up on the C.R.T.; a 6 unit character would have 7 traces and so on, as selected by the Elements Per Character switch.

Each trace is made up of a horizontal line of marker dots representing the 98 one-percent divisions between 49% early and 49% late. The ideal or zero distortion point is identified by the absence of a dot in the trace centre, whilst, starting from the centre each tenth dot is brightened to denote the 10% points. Transitions are displayed by the presence of a dot above or below a marker dot, representing positive or negative transitions respectively. (See Diag.2).



Diag. 2

2.3.2 The Display Control switch selects the type of display as detailed below:

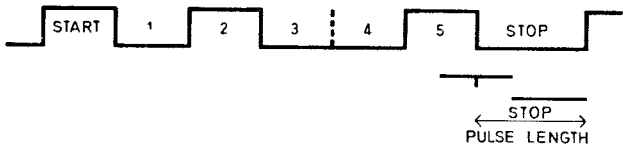
2.3.2.1 Hold Peak Distortion: With this display all of the traces are superimposed on each other and a collective distortion display is provided. The main facility in this position is the ability to store, update and display continuously the peak values of distortion measured for both Early and Late readings. The stores will hold the highest value of distortion received until manually reset by operation of the push button switch below the display control switch.

2.3.2.2 Separate Element Distortion: This display provides a vertical separation of the traces described above thus allowing inspection of each individual element distortion.

It is also possible to observe and measure speed error by utilising this method of display.

2.3.2.3 Input Waveform: The actual input signal waveform is displayed thus allowing observations to be made of rise and fall times and possibly contact bounce where relays are employed. To facilitate the latter, when the display is expanded as described in para.2.4, bright "dots" are superimposed on the waveform at intervals of 10% of a signal element.

2.3.2.4 Stop Pulse: To measure this period, the distortion display is started in the centre of the last information element and continued until the next start element is detected, thus the length of the display from the last information transition time to the end of the total display is a direct measurement of stop pulse length. Diag. 3 gives an example of a 5 unit code character with a $1\frac{1}{2}$ bit stop period.



Diag. 3

2.4 Synchronous Distortion Measurement

The synchronous measurement facility is used to measure distortion in continuous data streams, e.g. any of the standard line test patterns 1:1, 2:2, 511 bit pseudo-random patterns etc. The display is similar to that for Start/Stop Distortion Measurement (para. 2.3), with the exception that there is only one distortion trace even though the display control be set to Separate Element Distortion.

A synchroniser in the T.D.S.A. establishes a timing reference against which measurements are made. Synchronisation to any of the 'Cal' (fixed) speeds available on the T.D.S.A. is automatic when the Start/Stop-Free Run-Sync switch is set to 'Sync', but operation to a speed which is only obtainable by the Variable Oscillator is as follows:-

With the 'ST/ST-Free Run-Sync' switch set to Free Run the receiver speed is set to the nominal bit rate and the Display Control to Hold Peak Distortion. The transitions will then drift across the display and the Variable Oscillator control can then be adjusted to give a very slow rate ot transition drift.

Once this condition is achieved switch to Synchronous and the transition display will be locked about the ideal transition time on the display. A lamp indication on the front panel shows when the synchronised condition is achieved. The values of Peak Early and Late distortion will give a true value isochronous distortion.

When operating in a synchronous mode the Stop Pulse 'Display Control' position is not applicable, also the 'Separate Element Distortion' position gives a single horizontal trace without 'hold peak' transitions.

If a loop check is to be made on a system e.g. 'back-to-back' Modem then by employing a T.D.M.G. and a T.D.S.A. a common timing source can be used for both. This means that an absolute measurement distortion can be obtained when compensation for the delay between transmitter and receiver has been made. To do this the T.D.S.A. Speed Control is set to 'Ext' and the 100 times bit rate output signal from the T.D.M.G. used to drive the 100 times bit rate input on the T.D.S.A. back panel (see 8.1 - Ancillary Input/Output). The T.D.S.A. Start/Stop-Free Run-Sync switch is now set to 'Sync' to align the T.D.S.A. with the incoming data. When this is achieved (i.e. transitions are occurring equally spaced around the ideal transition point) the T.D.S.A. is set to 'Free Run'. This will disable the synchroniser, so that the T.D.S.A. retains a fixed reference for incoming data transitions.

2.5 Tube Controls

The standard C.R.T. display controls are provided on the front panel for Focus, Brilliance and Astigmatism. A Horizontal Magnifier switched control is also included to expand the display. This 4 position switch gives the following expansions:

a) 0% X 3. The distortion display in this position gives a coverage from 49% Early to 49% Late, with the trace centre at the zero distortion point. On Input Waveform, the whole character will be displayed.

b) 0% X 3. The distortion gives a coverage from 19% Early to 19% Late centred on the zero distortion point. On Input Waveform, the middle period only of the character will be displayed, magnified by 3.

c) 30% X 3. The distortion display gives coverage from 49%Early to 10% Early centred on the 30% Early point. On Input Waveform, the first part of the character will be displayed, magnified by 3.

d) 30% X 3. The distortion display gives coverage from 10% Late to 49% Late centred on the 30% Late point. On Input Waveform, the last part of the character will be displayed, magnified by 3.

2.6 Error Count

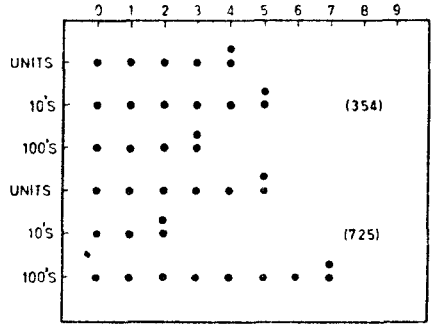
The error count system operates comparing the incoming data stream with an internally generated message or pattern and any discrepancies are defined as errors. The incoming patterns and messages must be the same as those generated within the T.D.S.A., as provided by the Trend T.D.M.G.

A pattern phase relationship must be correctly established to enable error detection, the phasing cycle within the T.D.S.A. being initiated by the 'Phase' push button. A lamp indication shows when the correct pattern phase is achieved. An automatic phasing action is initiated for the Start/Stop messages if nine consecutive characters are in error.

Element errors are defined as an incorrect comparison at a predetermined sampling time during the element period. The sampling points are selected by a switch mounted on the rear panel and can be switched in 5% steps from 5% to 45% through the element period for all patterns. For the 511 bit P-R pattern, it is also possible to sample at the 50% point.

A display of the error counters results by setting the Display Control to Error Store.

The display is shown on the C.R.T. as 6 rows of dots with each row containing up to 10 dots and thus representing a decade (see diagram). The most significant dot in each row is emphasised by a dual dot display. The count capacity is up to 10^6. This can be split to give two separate counters of up to 10^3 capacity each. By this means error rates can be established by counting errors in the first store and total information received into the second store.



Diag. 4

The Error Count Control switch allows the following types of error to be detected and displayed.

a) 5 unit Fox Character Error: In this position the error store counts every character which is in error during the 5 unit code (I.T.A. No.2) 'Quick Brown Fox' message as generated by the T.D.M.G.

b) 8 unit Fox Character Error: Character errors are detected in the 8 unit code (I.T.A. No.5) 'Quick Brown Fox' uppercase, even parity as generated by the T.D.M.G.
For both (a) and (b) a character is defined as being in error if one or more elements in the character are incorrect at the sampling time.

c) Parity Errors: For parity coded start/stop characters, errors can be counted for either Odd or Even parity.

d) 511 bit Pseudo-Random Pattern Errors: The error store can be set to count either element errors in the pseudo-random sequence, or block errors, which are full pseudo-random patterns of 511 bits which have one or more elements incorrect.

e) 'Q9S' Character Errors: Character errors can be counted in the Q9S message to C.C.I.T.T. recommendation R51.

The second error store control switch is mounted on the rear panel and controls the following store functions:

f) Overflow: This position places the second store in series with the first error store to provide 10^6 count capacity.

g) Block/Auto rephase: When using the first store as described in (d), then the second store counts pseudo-random block errors. When using the first store as described in (a), (b) and (e) then the second store counts the number of automatic rephasing actions.

h) Block/Messages Received: In this position the second store counts the total number of pseudo-random blocks or Fox messages or Q9S messages received.

i) Both error stores are under the control of the three position Count-Stop-Reset switch on the front of the unit.

2.7 Ancillary Controls

Certain facilities can be supplemented or modified by a control panel mounted at the rear of the instrument.

Control is affected by insertion or omission of 'U' links between two columns of sockets on the panel.

a) External Element Timing: By insertion of a link the T.D.S.A. can count errors in the 511 bit Pseudo-Random Pattern when using an external element rate timing source. (e.g. synchronous modem clock). For this mode of working the 'Speed Bits/Sec' switch should be set to any position other than 'Ext".

b) Hold Max. Pos. & Neg. only: By insertion of a link positive or negative transitions respectively are held in the peak distortion stores.

A potentiometer mounted on the rear of the instrument enables the amplitude of the 'Input Waveform' display to be varied.

2.8 Ancillary Input/Output

Provision is made on the rear of the instrument for the input and output and monitoring of certain useful signals.

2.8.1 Sockets are provided on the panel for:

a) Input timing source at 100 times bit rate. This signal is required to be at logic (0 to +5V) or CCITT V28 level (In 100x Clock).

b) Output timing at 100 times bit rate at logic level (Out 100x Clock).

c) Input of Element Timing Signal with level as on (a) (Timing Element In).

d) Output of an element timing signal producing one cycle per element at logic level. (Timing Element Out).

e) Output of a Character Timing signal producing a pulse which is low from the mid-point of the start element until the middle of the stop elements (5, 6, 7 unit characters) or the middle of the 8th information element (8 unit characters) at logic level (Timing CH).

f) Output of Message timing signal producing a pulse of 1/100 of an element in width per message at logic level (Timing Mess).

g) Output of Pseudo-Random block signal producing a positive pulse one element in length per 511 bit sequence at logic level (Timing Block).

h) The two bottom sockets on the panel provide the 0V (Signal Common) connection to which all the signals on the panel are referred.

2.8.2 A 25-way socket is provided to give access to the following:

Pin No.	Signal	Function
1	0V	Common Return
2	Received Data (Out)	Data normalised to logic level 0V=1, +5V=0.
3	Sig.El.Timing (Out) -% Dist.Counter Early/Late	1:1, positive transitions coincident with ideal data transitions. 0V during 'Early' +5V during 'Late'.
4	% Dist.Counter,BCD 1 +5V=1, 0V=0	
5	% Dist.Counter,BCD 2 +5V=2, 0V=0	
6	% Dist.Counter,BCD 4 +5V=4, 0V=0	Used in conjunction with Dist'n. Read-out Timing (pin 11) gives % distortion of transitions.
7	% Dist.Counter,BCD 8 +5V=8, 0V=0	
8	% Dist.Counter,BCD 10 +5V=10, 0V=0	
9	% Dist.Counter,BCD 20 +5V=20, 0V=0	
10	% Dist.Counter,BCD 40 +5V=40, 0V=0	
11	Distortion Read-out Timing	Negative going pulse, 0V and +5V, 1% of element per transition.
12	Element Error Pulse	Positive pulse, 0V and +5V per element in error in the Pseudo-Random sequence.
13	Block Error Pulse	Positive pulse, 0V and +5V per 511 bit block in error in the Pseudo-Random sequence.
14	Parity Error Pulse	Positive pulse, 0V and +5V per parity error in start/stop characters.
15	Character Error Pulse	Positive pulse, 0V and +5V per character error in Fox and Q9S messages.
16	Block Timing	Positive pulse, 0V and +5V see 2.8.1.(g)
17	Character Timing	Positive pulse, 0V and +5V see 2.8.1.(e)
18	Message Timing	Positive pulse, 0V and +5V see 2.8.1.(f)
19	100 x Clock Out	0V and +5V. see 2.8.1.(b)
20	Rephase Control (In)	0V to rephase, O/C or +5V normal.
21	100 x Clock In	See 2.8.1.(a)
22	Element Timing I/P	See 2.8.1.(b)
23	V28 Data (In)	Data Input
24-25	Not Used	

2.9 Operational Conditions

The instrument is designed to operate over a temperature range of 2°C to 40°C ambient and in a relative humidity between 40 and 90% ambient. All preset adjustments are made during manufacture and consequently no field calibration is necessary other than the C.R.T. display controls provided.

2.10 Mechanical

The unit is fully self contained and of rugged construction suitable for field use. The T.D.S.A. can be mounted together with a Trend Telegraph and Data Message Generator (T.D.M.G.) in a 19 inch rack. The rack mounting adaptor is available as an optional extra.

2.10.1 The T.D.S.A. dimensions are as follows:

Height	6 inches	15cms
Width	9 inches	23cms
Depth	18 inches	46cms
Weight	25 lbs	11.4kgs

2.10.2 The unit has an attractive two tone finish in black and silver grey.

2.11 Power Connections

The mains is connected by a 3 pin socket mounted on the rear panel. Each unit is provided with an 8ft mains cable with colour code conforming to the European standard.

The unit can operate with mains input 50 to 60Hz and with voltages in the ranges 190 to 250V or 95 to 125V. The appropriate tap setting is achieved by means of a voltage selector mounted on the rear panel. A 1A delay type fuse link is required for 240v, or a 2A link for 115v.

2.12 Model Variants

Two models of the unit are available:

T.D.S.A. No.1A: This model has all the facilities described.

T.D.S.A. No.2A: This model has none of the error count facilities. The 25 way socket described in 2.8.2 is also omitted.

CHAPTER 3

CIRCUIT DESCRIPTION

3.1 General

3.1.1 Start/Stop Distortion Measurements

In order to make measurements to an accuracy of 1% it is necessary first to provide a system clock at 100 x the element rate of the data stream to be measured. This clock is normally derived internally from one of the two 2.88MHz oscillators via the Speed Divider which is switched by the SPEED BITS/SEC switches to give the required frequency, although an external 100 x element rate signal can be used if required.

The selected 100 x element rate clock, HSS, drives a binary-coded decimal (b.c.d.) 50-way Up/Down (or Reversible) Counter. When the counter is allowed to run, the Up/Down Control causes the counter to count from 0 to 49 in the Up mode followed by 49 to 0 in the Down mode and so on, the result being a total count of 100 with the Up/Down Control (a bistable) switching at element rate. The element rate signal thus obtained is used to drive the 6-9-way binary Character Length Counter.

The purpose of the Up/Down Counter is to divide the elements of the incoming characters into one-percent divisions. The Character Length Counter is used to define the element transitions of the character, i.e. Start Elements - 1st Info. Element transition, 1st Info. Element - 2nd Info Element, etc., up to Last Info. Element - Stop Element transition. The count length of the Character Length Counter thus depends on the number of elements per start/stop character as selected by the ELEMENTS PER CHARACTER switch.

Control is exercised over the Up/Down and Character Length counters by the Start/Stop Control, such that when start polarity is detected at the Received Data Input Circuit, the counters are allowed to run for the duration of one character. The Short Start Reject Circuit ensures that if a supposed start signal turns out to be only a noise spike, then the counters will be reset and remain so until the next start polarity is detected.

The binary Character Length Counter stages are fed to a Digital-to-Analogue converter circuit, the output of which controls the Y deflection circuit of the C.R.T. to give the vertical positions of the 6-9 calibrated horizontal traces relevant to start/stop distortion measurements. The X deflection of each trace is obtained using a "Pump" circuit, which is driven by the 100 x element rate clock; this moves the trace horizontally across the tube face in "one-percent" increments giving a display of one-percent "dots". The middle dot is "blanked out" to indicate the centre or "0%" part of the trace whilst every tenth dot (counted from the "0%" point outwards in both directions) is "brightened up" to accentuate the "10%" markers.

3.1.1 continued

The detection of transitions on input data, accomplished in the Input Data Retiming circuit, is used to modify the Y deflection and at the same time increase the trace brightness to give the required indication on the display. The effect of this is to provide a small positive deflection of one of the trace's one-percent dots when a positive transition is detected and a negative deflection for a negative transition, the position of this deflection relative to the "0%" or "ideal transition" point giving the distortion present on that transition, e.g. a deflection 11 dots to the left of 0% on a trace indicates a transition distorted "11% Early".

The "Hold Peak Distortion" Store is used to hold those states of the Up/Down Counter which correspond to the early and late transitions of input data that occur farthest away from the "ideal transition" point. The output from this store is used to feed in "hold peak transitions" to the tube display Y Scan and Brightness circuits, alongside the actual transitions detected in the Input Retiming Circuit.

3.1.2 Isochronous Distortion Measurements

Isochronous measurements will normally be made with the START/STOP-FREE RUN-SYNC switch in the SYNC position. In this situation, unlike the START/STOP setting, the Up/Down Counter will run continuously after detecting the first start polarity signal. The Phase-Locking Circuit will "advance" or "retard" the counter as appropriate (by making the count 101 or 99 respectively), in an attempt to line up the counter's zero point with the incoming data transitions. In practice when phase-locking to distorted transitions, the counter's zero point will be lined up with the "average" transition position.

The display of actual and "held peak" transitions is performed in a similar manner to that for Start/Stop working, but only one trace of "marker dots" is produced even in the SEP ELEM DIST'N position of the DISPLAY CONTROL switch as more would be irrelevant.

Operation when switched to FREE RUN is the same as for SYNC, except that the Phase-Locking Circuit is disabled. This can be used for measuring the distortion present on Start/Stop "Blocks" of data.

3.1.3 Error Measurement (T.D.S.A. 1A only)

Character errors will be dealt with first. The Character Length Counter drives the Message Length Counter which has a length of count determined by the message selected on the ERROR COUNT CONTROL switch. The M.L. Counter is used to address the Read-Only Memory, which contains the Q9S and two Fox messages. When a phasing sequence is initiated, the M.L. Counter is held in its zero state by the Start/Stop Message Phasing Control until an incoming character agrees with that held in the R.O.M. When this has happened the M.L. Counter is allowed to step, but if 9 consecutive character errors are detected sometime later, an "out-of-phase" condition will be considered to exist and a new phasing sequence initiated.

3.1.3 continued

Parity errors are detected in the Parity Error Detection circuit by generating a "local" parity bit and comparing it with the actual parity bit received.

Errors can also be detected in the standard 511-bit Pseudo-Random sequence. This is done by first aligning the local Pseudo-Random Generator by means of the P-R Phasing Control and thereafter comparing the locally generated pattern with that being received. For such a measurement the instrument is normally run in the SYNC mode. Also available is the facility to use an EXTERNAL ELEMENT TIMING signal, e.g. for use with a Synchronous Modem which supplies its own timing.

There are two 3-decade Error Counters which can be used for the purpose of recording errors detected, number of start/stop messages received, number of automatic rephasing operations, etc. The display on the tube consists of 6 horizontal lines of up to 10 dots, where each line represents one of the counter decodes and the number of dots in the line represents the count (from 0-9) in that decode. These lines of dots are basically the distortion display traces where all but the "5%" dots have been "blanked out". For each line the Error Display Control causes the dot representing the "significant digit" of the associated counter to be given a deflection similar to that for a positive transition in the distortion display, whilst the rest of the line is held blanked out.

3.2 Logic Elements

3.2.1 General

The digital integrated circuits used in the instrument consist of 3 types:

Fairchild "930" series gates and bistables;
Fairchild "9300" type M.S.1. circuits;
National Semiconductors type "MM5220" M.O.S. Read only Memory (R.O.M.)

They are represented in the circuit diagrams by B.S. symbols or in the case of the more complex functions by a rectangle.

Circuits are numbered as follows:

Gates have the circuit reference number written in the middle of the symbol and the relevant pin numbers by their inputs and outputs. The circuit type number (e.g. "962" for a 3 input gate) is written by the symbol.

Bistables are treated in a similar manner to gates, but as the symbol is larger the circuit type number is written inside with the circuit reference number. Also written inside is the name of the bistable, e.g. "MUP" in bistable IC.13(1-6) on Fig.3.

The "9300" elements and R.O.M. are treated similarly with the addition of abbreviated titles for the pin functions.

3.2.2 NAND Gates (936, 946, 962, 930, 932 on Fig. 13A)

All gates perform the 'positive logic' NAND function, i.e. when all inputs to a gate are positive (logical '1' or MARK state) the output is at 0v (logical '0' or SPACE state); under all other input conditions the gate is positive. With the 930 and 932 elements it is possible to expand the number of gate inputs by using the nodes available on pins 3 and 11. The 932 element is used where a large "fan out" is required.

A feature of all gates except the 932 is that several gate outputs can be joined together in the 'wire OR' configuration; with this arrangement any gate whose inputs are all high will hold the common output point low, i.e. all gates have to have at least one input low for the common output to go high.

3.2.3 Bistables (9093 on Fig. 13A)

The bistables are of the d.c. triggered, J-K master/slave type. With this type of circuit, data is fed into the master (or input) bistable whilst the clock waveform is high. When the clock goes low, the slave (or output) bistable will take up the state of the master bistable. The Sd input can be used to switch the circuit asynchronously and over-rides the clocked inputs.

The drawing convention used in the circuit diagrams is such that the bistable 'set' input and 'true' output are always considered to be the top pair of input/output connections on the symbol, e.g. in Fig. 3 and for bistable MUP (IC. 13(1-6) the set input is pin 3 and true output ("MUP") is pin 6 whilst the reset input is pin 2 and the inverse output ("$\overline{\text{MUP}}$") pin 5. Also, in this case, the asynchronous input on pin 4 is used to set the bistable, as taking pin 4 low will force pin 6 high.

3.2.4 Up/Down Counters (9306 on Fig. 13A)

The 9306 is a synchronously presettable, reversible, 10-way binary coded decimal (b.c.d.) counter made up from 4 bistables, the outputs of which represent each counter state in "weighted" code, i.e. Q0 = 1, Q1 = 2, Q2 = 4 and Q3 = 8 so that state 3, for example is represented by $Q0.Q1.\overline{Q2}.\overline{Q3}$.

If the 'counter enable' inputs CE are all high and the 'count direction' input CD is also high, then application of clock pulses to clock input CP will cause the counter to count "up", 0, 1, 2, 3, 4, 5, 6, 7, 8, 9,0, 1, 2, etc. giving a "terminal count" output TC on each count of 9. If CD is low, then the counter will count "down" 9, 8, 7, 6, 5, 4, 3, 2, 1, 0, 9, 8, etc. giving output TC on each count of 0.

3.2.4 continued

If "parallel enable" input PE is taken to 0v, CE will be over-ridden and the counter stages set to the states corresponding to the conditions imposed on inputs P0 - P3 under the control of clock input CP.

The clock required to drive the counter is the inverse of that required to drive a "9093" type of bistable; data is fed into the counter whilst the clock is low and the counter stages change state immediately after the clock goes high.

3.2.5 B.C.D. Decade Counter (9310 on Fig. 13B)

The 9310 is a synchronously presettable, 10-way binary coded decimal (b.c.d.) counter made up from four bistables, the outputs of which represent each counter state in "weighted" code, i.e. Q0 = 1, Q1 = 2, Q2 = and Q3 = 8. State 3, for example, is represented by $Q0.Q1.\overline{Q2}.\overline{Q3}$.

If the count enable inputs CEP and CET are both high, and if the parallel enable input PE is also high, application of clock pulses to clock input CP will cause the counter to count 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, etc., giving a terminal count output TC on each count of 9. If CEP is low, counting is inhibited. If CET is low, counting is inhibited and TC held low regardless of the count.

If the parallel enable input PE is taken low, the counter stages will be set to the states corresponding to the condition imposed on inputs P0 - P3 under the control of clock input CP.

When the asynchronous master reset input MR is taken low, the counter will be reset to the "count 0" state, regardless of the other input conditions.

The clock required to drive the counter is the inverse of that required to drive a "9093" type of bistable; data is fed into the counter whilst the clock is low and the counter stages change state immediately after the clock goes high.

3.2.6 Dual 4-Bit Latch (9308 on Fig. 13B)

The 9308 consists of two separate 4-bit latch sections which provide parallel gated data storage. Each section has four outputs Q0, Q1, Q2, Q3, an over-riding master reset MR and a two-input active low AND enable.

Data enters a latch when both enable inputs are low. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs go high, the data present in the latch at that time is held in the latch and is no longer affected by the data input. The active low master reset over-rides all other input conditions and when activated forces the outputs of all the latches low.

3.2.7 5-Bit Comparator (9324 on Fig. 13B)

The 9324 is an expandable comparator which provides comparison between two 5-bit words A0 - A4 and B0 - B4, and can give one of three outputs, "less than" A< B, "greater than" A> B and "equal to" A=B. A high level on the active low enable inputs E forces all three outputs low.

Words of more than 5 bits are compared by connecting 9324 comparators in series; this is done by connecting the A>B and A<B outputs of the first 9324 to the A0 and B0 inputs respectively of the next stage.

3.2.8 Eight-Input Multiplexer (9312 on Fig. 13B)

The 9312 is an 8-input multiplexer which can select one bit of data from up to eight sources I0-I7. It has complementary outputs Z and $\overline{Z}$, active low enable E and internal select decoding. When E is high, output Z is low and $\overline{Z}$ high regardless of the other input conditions. Data is routed from one of the inputs I0-I7 to the outputs according to the three-input binary code applied to the select inputs S0 - S2.

3.2.9 Read-Only Memory and Drivers (MM5220 and DM8810 on Fig. 13A)

The MM5220 is a 1024-bit static read-only memory (R.O.M.), the contents of which are customer-specified, being inserted during one stage of the device fabrication. The output can be obtained either in the form of 256 x 4 bit or 128 x 8 bit parallel words, under the control of the MODE CONTROL input; for the T.D.S.A., "128 x 8" operation is required and to obtain this the MODE CONTROL and A8 inputs are taken to a permanent 0v as shown in Fig.3. VDD is also taken to 0v whilst VSS is taken to +15v and VGG to -15v. The R.O.M. is a "negative logic" device, i.e. a '1' is a more negative level than 1 '0' and with the aforementioned supply voltages a level on the A1 - A8 (binary address), MODE CONTROL or CHIP ENABLE inputs is considered to be a '1' between 0v and +4v and a '0' if between +10v and +15v. These high level signals are obtained by using DM8810 high level driver circuits, which are 2-input NAND gates with "free O/P collectors" capable of switching at +15v.

"CHIP ENABLE" is gated into the parallel outputs B1 - B8 and when at 0v will allow the outputs to take up the states of the 8-bit word selected by the binary address inputs A1 - A7. When CHIP ENABLE is high, B1 - B8 will remain low.

The truth table for the R.O.M. used in the instrument (MM5220 GJ) is given below. Address 0 is given by $\overline{A1}.\overline{A2}.\overline{A3}.\overline{A4}.\overline{A5}.\overline{A6}.\overline{A7}$, address 1 by $A1.\overline{A2}.\overline{A3}.\overline{A4}.\overline{A5}.\overline{A6}.\overline{A7}$. and so on. It must be rembered here that this is "negative logic", unlike the rest of the logic in the instrument, therefore a '0' output as given by the truth table is seen as a '1' by the "positive logic" circuits it drives and a '1' is seen as a '0'.

3.3 Detailed Description

3.3.1 Oscillators and Dividers (Fig.3)

The 100 x bit rate clock (HSS) required for operation of the T.D.S.A. is obtained from one of two 2.88MHz oscillators, followed by a divider chain which is conditioned by signals from the SPEED BITS/SEC switch SW9 to give the required division for the speed selected.

The 100 x bit rate clock obtained at the output of the Dividers is "frequency doubled" and the result "divided-by-two", thus giving the final 100 x bit rate clock HSS; this "divide-by-two" action is modified under the control of the Start/Stop Control to improve measurement accuracy.

The oscillators used are a fixed (crystal controlled) oscillator for use when precise setting of speed is required and a variable oscillator for use when checking start/stop synchronous distortion (speed error removed) or setting a speed not given directly by SW9.

3.3.1.1 Crystal Oscillator (Fig.3)

This is a straightforward Colpitts oscillator, transistor TR1 being the oscillating transistor. The collector of TR1, which takes no part in the oscillator action itself, is taken to the base of the buffer transistor TR2 from the collector of which the output is taken. Transistors TR10 and TR11 are used to inhibit oscillation when the Variable Oscillator is being used.

3.3.1.2 Variable Oscillator (Fig.3)

This is an emitter-coupled, emitter-timed oscillator. TR5 collector, which has no part in the action of the oscillator, provides a signal to drive transistor TR7 which in turn drives the output transistor TR8. Transistors TR4 and TR6 provide constant currents for the oscillator transistors TR3 and TR5, to give linear ramps on the emitters of TR4 and TR5 and thus make the switching points well defined. The amplitude of these ramps is controlled by the resistor RV6 in the collector of TR3, which is variable by ±20% at the front panel.

3.3.1.3 Oscillator Selection (Fig.3)

IC's.20(1,2;9,8) and 12(1,2,3) are used under the control of the CAL/UNCAL switch SW10 (Fig.10) to decide which of the two oscillators is to be employed. If SW10 is in the CAL position, signal $\overline{\text{CAL}}$ is low and the output of the crystal oscillator (TR2 collector) is allowed to switch IC.20(1,2) and hence drive the dividers as IC.20 pin 9 is low; in this situation IC.12 pin 2 is also low and thus inhibits the effect of the variable oscillator (TR8 collector). With SW10 in the UNCAL position, $\overline{\text{CAL}}$ and hence IC.20 pin 9 is high and pin 8 will hold the crystal oscillator output low; IC.12 pin 2 will now be high and therefore allow the variable oscillator to switch IC.12(1,2,3) and hence the divider. A further effect in this switch position is that the crystal oscillator is prevented from oscillating via transistors TR11 and TR10.

3.3.1.4 Speed Divider (Fig. 3)

The SPEED BITS/SEC switch SW9 (Fig. 10) applies signals ($\overline{9600}$, $\overline{7200}$, $\overline{4800}$ etc.) to condition the divider chain to give the output frequency required. $\overline{9600}$ will only be low when SW9 is set to 9600 bits/sec, $\overline{7200}$ low for 7200 bits/sec and so on down the range. $\overline{EXT}$ is low when SW9 is switched to EXT, when an external timing signal of 100 x the required bit rate (EXT TIM I/P) can be injected via transistor TR9.

Bistables MD1 and MD2 (IC's. 11(1-6) and 10(1-6) respectively form a divider which can divide by either 3 or 4, depending on the state of the signal on IC. 19 pin 4. If this signal is low (obtained with speeds of 7200, 3600, 1800, 900, 90 and 45 bits/sec), IC. 19 pin 6 and therefore MD1 input IC. 11 pin 2 will always be high and the divider will divide by 4. If the signal on IC. 19 pin 4 is high, however (i.e. all speeds other than those just listed), the signal appearing on IC. 11 pin 2 will be identical to that on IC. 10 pin 6 and the divider will divide by 3. The output of this stage (IC. 10 pin 8) drives a binary divided by 4 stage, MD3 and MD4 (IC's. 10(8-13) and 9(1-6)).

On all speeds other than 110 and 220 bits/sec, IC. 19 pin 10 is high and therefore allows MD4 (IC. 9 pin 6) to switch IC. 19(10, 9, 8) and hence the clock input (IC. 9 pin 13) to the divide by 2 stage, MD5. If either of these two speeds is selected, however, IC. 19 pin 10 goes low and IC. 25 pin 5 goes high; the signal which is now fed through to the clock input of MD5 is effectively the 2.88MHz oscillator square wave minus every twelfth positive excursion. This is obtained by decoding one of the states of the first two dividers, which are arranged to divide by a total of 12. This decode, obtained on IC. 24(3-6), is applied to IC. 25 pin 1 to inhibit every twelfth pulse of the 2.88MHz oscillator present on IC. 25 pin 4. This action reduces the effective frequency of the signal presented to the clock input of MD5 by a twelfth to 2.64MHz, thus enabling the 100 x bit-rate clock for 110 and 220 bits/sec working (i.e. 11 and 22KHz respectively) to be obtained by subsequent normal division, which would not have been possible with the original frequency of 2.88MHz.

Bistables MD6, MD7 and MD8 (IC's. 8 and 1(1-6)) may be arranged to divide by 5, 6 or 8. If IC. 12 pin 13 is high and IC. 19 pin 12 low (speeds 400, 220, 100 or 50 bits/sec) then the signal on MD5 input IC. 8 pin 2 will be the inverse of that on IC. 8 pin 9 and MD6 and MD7 will act as a divide by 3. The "ANDed" combination of MD6 and MD7, obtained via IC. 17(9, 8), is used to drive MD8, which gives a further division by 2 and thus a total division for the stage of 6. If IC. 19 pin 12 is high and IC. 12 pin 13 low (speeds 7200, 3600, 1800, 900, 220, 110, 90 or 45 bits/sec) the signal on MD6 input IC. 8 pin 3 will be the "ORed" combination of MD7 and MD8, thus making the whole stage divide by 5. If the signals on IC. 19 pin 12 and IC. 12 pin 13 are both low (all other speeds than those just mentioned) then the bistables will divide by 8.

3.3.1.4 continued

Bistables MD9 and MD10 (IC's.1(9-13) and 2(1-6)) may be arranged to divide by 3 or 4. If IC.16 pin 3 is high (speeds 110 or 220 bits/sec) then the signal on MD9 input IC.1 pin 12 will be identical to that on IC.2 pin 6 (MD10) and the divider will divide by 3. If IC.16 pin 3 is low, however (all speeds other than 110 or 220 bits/sec) then MD9 input IC.1 pin 12 will be permanently high and the divider will divide by 4.

Bistables MD11 - MD13 (IC's.2(8-13) and 3) will always act as a divide by 8.

Selection of the appropriate divider output for each speed is accomplished in the "Divider Output Selection" gates.

3.3.1.5 Final High Speed Clock Phase Adjustment (Fig.3)

To improve the measurement accuracy of the instrument, HSS (the 100 x bit rate clock) is arranged to go to its low level state immediately each new start element has been detected. This is accomplished by taking the initial 100 x bit rate signal on IC.26 pin 11, forming narrow negative pulses coincident with each transition on that signal and applying the resultant 200 x bit rate signal to the bistable MHS. The latter divides by two to produce the final version of HSS. MHS is reset via its asynchronous input every time a new start element is detected, i.e. every time MS1, the Start/Stop Control bistable (section 3.3.5) becomes set.

IC's.25(8-11;1,2,13,12), 26(1,2,13,12), 27(1,2;5,6) and 14(1,2) comprise the "narrow pulse forming" circuit, together with C9 and C10, which derives the clock input to MHS. IC.30(1,2;3,4;11,10;13,12) and C11 are used to form a narrow negative pulse to reset MHS via the asynchronous input on IC.11 pin 10, whenever MS1 becomes set, as detected by $\overline{MS1}$ on IC.30 pins 11 and 13 going low. $\overline{MHS}$ drives IC.29(8-13) to provide HSS and $\overline{HSS}$ is formed on IC.29(1-6).

3.3.2 50-Way Up/Down Counter and Up/Down Control (Fig.3)

The b.c.d. 50-Way Up/Down Counter is driven by the 100 x element-rate clock HSS. Its purpose is to define the 1% divisions of each incoming data element from 49% "Early" to 49% "Late" relative to the "ideal transition" point, the Up/Down Control giving the Early/Late indication. When allowed to run, the counter counts 0-49 "up" from the "ideal transition" time to the "ideal" mid-point of a data-element period and 49-0 "down" from the ideal mid-point to the ideal transition time. Any data transition detected during the "down" half-cycle is considered to be "Early" and one detected during the "up" half-cycle is considered to be "Late", the b.c.d. state of the counter at the instant of transition detection giving the magnitude of the displacement from the ideal, defined as a percentage of the element-period i.e. the "percentage distortion" of that transition. Fig.12C gives examples of "ideal", "early" and "late" transitions detected and also shows the action of the counter relative to the Up/Down Control, whilst Fig.12D gives examples in greater detail, showing the relationship of the counter outputs for transitions distorted by specified amounts.

3.3.2 continued

IC's.4 and 6 are each 10-way b.c.d. up/down counters and form the "units" and "tens" stages respectively. IC13(1-6) is MUP, the Up/Down Control which permits the counter to count up when pin 6 is high and down when pin 6 is low. MUP is set by the detection of "count 0-down" (CODOWN) at IC.21(4-6) causing pin 3 of IC.13 to go high, via IC.14 pin 3. It is reset by the detection of "count 49-up" (C49UP) at IC.21(1,2,13,12) causing pin 2 of IC.13 to go high via IC.21 pin 11. At these changeover points, the Up/Down Counter itself is prevented from stepping by a signal applied to the "count enable" input pin 13 of both IC.4-6, derived via IC.14(5,6;9,8 and 11,10), which is at 0v both at "count 0-down" and "count 49-up". This gives a "count 0" position either side of the "down-to-up" changeover point and a "count 49" position either side of the "up-to-down" changeover point as shown in Fig.12D. Gate IC's.28(8-11) and 12(4,5,6) are used to hold the counter in the "count 1-down" state when the Start/Stop Control is in its reset state (section 3.3.5) as shown in Fig.12D, whilst 27(11,10) and 14(13,12) are used to reset the counter to "count 0-up" for STOP PULSE measurement (see sections 3.3.5 and 3.3.8). IC.27(9,8) is used for "Phase-Locking" purposes (section 3.3.7).

3.3.3 Received Data Input Circuits (Fig.2A)

3.3.3.1 The signal input circuitry of the equipment consists of two amplifiers mounted on the mother board. The Waveorm Display Amplifier converts the wide range of input levels to a signal capable of driving the Y scan circuit, whilst the Input Data Amplifier produces the 0v and +5v signal $\overline{\text{I/P DATA}}$ to drive the logic circuits. In order to produce a faithful representation of the input on the C.R.T., the former amplifier, comprising TR's.17 and 42, does not saturate and has a variable feedback as gain control called Waveform Amplitude, mounted on the rear panel.

An attenuation circuit precedes both amplifiers to reduce the high voltage input signals to a more manageable level. Signals from the front panel V24 terminal are attenuated by R's 22 and 23 in order that TR14 is working within its design limits over the full range of V24 specified levels. The attenuation network for the high level input is dependent on the mode of T.D.S.A. working, i.e. series or shunt working as selected by the rear panel switch. For shunt working the input impedance is obviously required to be high, so the input from the front panel is attenuated by R24 and R22 before being converted to logic levels by the amplifier consisting of TR's 14 to 9. In the series working mode the equipment is required to present a very small impedance to the line, so with switch 16 in the closed position, the line signals are detected across an 18 ohm resistor R21. Zener Diodes D and D on the rear panel protect the input transistors against excessive voltage. TR13 is included in the emitter chain of TR14 to ensure a constant potential at the emitters.

3.3.3.2 Threshold Detection

A further function performed at the input to the Input Data Amplifier is selection of the threshold voltage at which transitions are detected on a high level input signal. Provision is made for threshold detection on three types of high level input by selecting the required position on the front panel switch SW2.

(a) Single Current +ve (SW2 position 3)

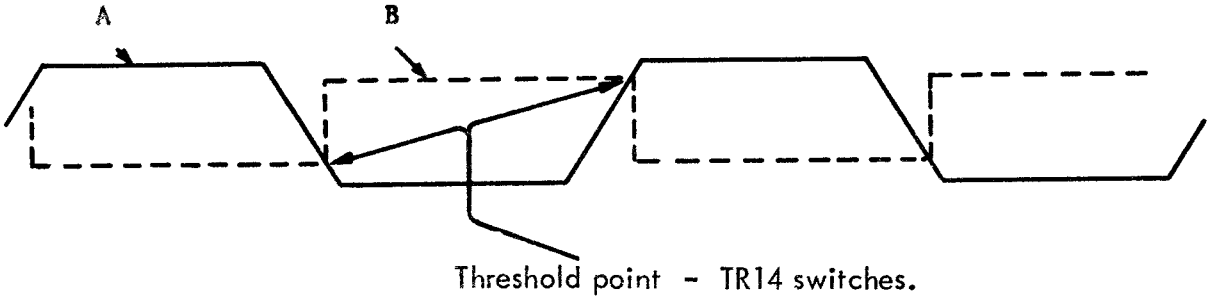
With the front panel input selector switch in this position, the threshold potentiometer, RV7, mounted on the rear panel, becomes part of a potential divider chain across the +15v rail through resistor R6 to R10. Threshold detection is made by comparing the potential on the wiper of RV7 with the input waveform at the common emitter pair TR14. When the voltage of a positive going transition on the R22 base of TR14 exceeds the threshold voltage on the other base, the potential at the junction of R20 and TR14 collector will fall to a level determined by the amount of constant current preset, by RV2. Negative going input transitions will cause TR14 to reset at the same threshold potential. TR14 collector waveform appears at the common emitter point of TR's 9 and 10, at the mean d.c. level of 0v, after a level change through zener diode D2. TR11 will reverse bias protection D1, is switched by this waveform to produce the logic level input to the digital circuitry $\overline{\text{DATA}}$.

(b) Single Current -ve (SW2 position 2)

For this type of input the threshold potentiometer RV4 is referenced to the -15v rail through R1.

(c) Double Current (SW2 position 1)

For this condition the output from the common emitters of TR's 9 and 10 is attenuated and fed back from RV4 wiper to TR14. The following waveform comparison is made by TR14.



Waveform A - Attenuated input waveform on TR14 base (R22).
Waveform B - TR14 base (Threshold potentiometer).

Diag.5.

As Waveform B is variable in amplitude, the point on the transition that TR14 changes state may be selected by the rear panel control. For correct threshold detection on double current the waveform at TR10 emitter must consist of equal voltage excursions about 0v. To obtain this condition the constant current through TR14 must be set by adjustment of RV2.

3.3.4 Input Data Retiming and Transition Detection (Fig. 4)

The logic level input data signal $\overline{\text{I/P DATA}}$ (see section 3.3.3) is fed to a 3-stage shift register MT1, MTE and MT2. Here it is retimed to the 100 x element rate clock $\overline{\text{HSS}}$ and transition of input data detected by comparing the shift register stages with each other. During the "Down" or "Early" half-cycle of the Up/Down Counter this comparison is between the first two stages, $\overline{\text{MT1}}$ and MTE, a positive transition being detected if MT1 and $\overline{\text{MTE}}$ are both high and a negative transition of MT1 and MTE are both high. For the "Up" or "Late" half-cycle the comparison is between the second and third stages, MTE and MT2, where a positive transition is detected if $\overline{\text{MTE}}$ and MT2 are both high and a negative transition if MTE and $\overline{\text{MT2}}$ are both high. The "transition - detected" pulses so obtained are equal in width to one period of $\overline{\text{HSS}}$. The distortion display requires that the deflections produced for all distortion values other than 0% are only present for the first (or negative) part of $\overline{\text{HSS}}$, so that nominally the deflection is only for half the transition - detected pulse period. This is achieved by gating the transition - detected signals with a signal HSS', equivalent to HSS at all but the 0% time as decoded from the Up/Down Counter. HSS' is also gated with the "transition" signals from the "Hold Peak" Stores - see section 3.3.9.

$\overline{\text{I/P DATA}}$ is fed to MT1 set input on IC.27 pin 2 and the inverse to the reset input on IC.27 pin 3 via IC.26(13,12). Negative transitions are detected using IC.31(1,2,13,12; 11,10,9,8). During the "Early" half-cycle 31(11,10,9,8) is used, as pin 11 ($\overline{\text{MUP}}$) is high, whilst during the "Late" half-cycle 31(1,2,13,12) is used, as pin 1 (MUP) is high. The "wire OR'ed"combination of these two gates is fed to IC.14(9,8) to produce the "negative transition detected" signal NTD, a positive pulse, on pin 8. Similarly, positive transitions are detected using IC's.30(8-13) and 31(3-6). During the "Early" half-cycle (30(8-13)) is used as pin 9 ($\overline{\text{MUP}}$) is high, whilst during the "Late" half-cycle 31(3-6) is used as pin 3 (MUP) is high. The "wire OR'ed" combination of the two gates is fed to IC.29(1,2) to produce the "positive transition detected" pulse PTD on pin 2.

NTD and PTD gated with HSS' at IC's.21(4,5,6) and 21(1,2,3) respectively to produce $\overline{\text{TDN}}$ and $\overline{\text{TDP}}$. These latter signals are also controlled by the "Hold Peak" Distortion Stores "Transition Display" Modification Logic - see section 3.3.9. $\overline{\text{TDN}}$ is further taken through IC.7(13,12) to produce TDN which drives the appropriate input to the Y Summing Amplifier (section 3.3.11.4) to produce the Y deflections relevant to negative transition markers. $\overline{\text{TDP}}$ is taken through IC's.15(13,12,11) and 26(8,9) to produce $\overline{\text{TDP}}'$, which drives the Y Summary Amplifier input relevant to positive transition markers. The latter two gates are necessary to enable the insertion of the positive "blip" to mark the significant digits to the Error Counters (section); if the DISPLAY CONTROL switch SW6 is not set to ERROR STORE, $\overline{\text{DE}}$ on pin 15 of IC.15 is high, thus enabling $\overline{\text{TDP}}$ to switch $\overline{\text{TDP}}'$.

3.3.4 continued

HSS' is formed using IC.8(13,12,11;10,9,8). Pin 9 is controlled by HSS, whilst pins 13 and 12 are controlled by the Up/Down Counter count decode signals COT and COU, which go high during the "count 0-tens" and "count 0-units" periods respectively of the Up/Down Counter. IC's.13(10,9,8) and 7(10,11) are used to clamp HSS' to 0v when ERROR STORE is selected by the DISPLAY CONTROL switch SW6, when $\overline{DE}$ on pin 11 of IC.7 is taken to 0v. This is to prevent "distortion" transition markers being superimposed on the Error Count display.

IC.14(3,4;5,6) is used to produce $\overline{TDD}$, which is a negative-going pulse for each distortion marker to be displayed, used in the Blanking and "Bright-Up" Waveform Generation circuits (sections 3.3.14 and 15). $\overline{TDD}$ is also controlled from the "Hold Peak" Distortion Stores circuit and the Error Counters (to produce the positive "blip" previously mentioned). IC.14(11,10;13 is used to produce a similar signal to TDD, but which is not controlled by the "transition" signals from the "Hold Peak" Distortion Stores, for use in the Phase-Locking Circuit (section 3.3.7).

3.3.5 Start/Stop Control (Fig.5)

For START/STOP working as selected by SW7, Start/Stop Control consists essentially of a bistable, MS1, which is set when start polarity is detected on the data input and reset when the centre of the stop element of the incoming character is reached, or if a "short start" condition is detected in the Short Start Reject Circuit (section 3.3.6). If SW7 is set to FREE RUN or SYNC, however, another bistable, MS2 (Fig.3), will be set half an element period after MS1 which will inhibit any further reset to MS1.

MS1 (IC.18(1-6)) is set via its asynchronous input on pin 4, using IC. 19(1,2,13,12). The inputs on this gate are $\overline{MS1}$ on pin 1 and STPOL on pin 2, which goes high when start polarity is detected on the data input. STPOL is derived using IC's.19(3-6), 20(10,9,8) and 6(8-13), controlled by the START polarity switch SW3; $\overline{I/P\ DATA}$ on IC.20 pin 10 goes high when the actual data input to the instrument goes positive, whilst $\overline{PST}$ on pin 9 is taken to 0v when switch SW3 is set to "+". IC.19(1,2,13,12) is also used to set MGR - see section 3.3.8.

For START/STOP working, MS1 is reset when the middle of the stop element is reached. The stop element time is obtained by decoding the appropriate state of the Character-Length Counter in the "Character-Length Selection" gates and switching the result through IC.20(1,2,3) via pin 2, whilst the element centre time "count 49-up" is ANDed to the result by feeding $\overline{C49UP}$ through IC.20(4,5,6) via pin 5. The result is applied to the reset input of MS1, pin 2 of IC.18.

The signal $\overline{SHORT\ START\ REJECT}$ on pins 1 and 4 of IC.20 will go low if a "short start" is detected during the first 40% of the start element period (section 3.3.6), thus resetting MS1.

For FREE RUN and SYNC settings of SW7, bistable MS2 (IC.13(8-13) on Fig.3) will be set when the centre-point of the start element period has been

3.3.5 continued

reached, via IC.20(3,4;5,6). The inverse output of MS2 (IC.13 pin 8) is then used to clamp the reset input to MS1 (IC.18 pin 2 of Fig.5), so that MS1 remains set. To get out of this condition, switch SW7 would have to be returned to START/STOP; this will take $\overline{SS}$ on MS2 asynchronous reset input (IC.13 pin 10) to 0v, holding MS2 reset and therefore allowing MS1 to be reset.

3.3.6 Short Start Reject Circuit (Fig.3)

The Short Start Reject Circuit action can be selected by wire links on Board 1, such that the main Start Stop Control bistable MS1 will be reset if more than a preset amount of continuous stop polarity is detected during the first 40% of a supposed start element. A decade counter clocked by HSS, the 100 x element rate clock, is allowed to run if stop polarity is detected during this 40%, but is held reset when start polarity is present on the input data line. If the 10% S.S. REJ link is present, a reset will be applied to MS1 if the decade counter reaches its terminal count, thus indicating that a 10% period of continuous stop polarity has taken place. If the 5% S.S.REJ link is present, MS1 will be reset if the decade counter reaches a count of 5.

The decade counter is formed by the "9310" IC.5. The CEP (enable) and PE(preset) inputs are controlled by IC.7(5,6), which holds these points low when the Up/Down Counter count exceeds 40, and IC.28(1,2,13,12) via IC.7(11,10). Pin 13 of IC.28, controlled by IC.27(13,12), goes high when stop polarity is present on the input data line and the other two inputs on pins 1 and 2 of IC.28, MST4 and MST1 respectively (from the Character-Length Counter, section 3.3.8), define the first half of the start element. IC.28(4-6) is used to provide the reset to MS1 ($\overline{\text{SHORT START REJ}}$) for the 10% S.S.REJECT setting whilst IC.26(1-6) provides the reset for 5% S.S. REJECT.

3.3.7 Phase-Locking Circuit (Fig.4)

The purpose of the Phase-Locking Logic is to line up the zero point of the 50-way Up/Down Counter with the time when an "average" incoming data transition might be expected, i.e. to line up the "count 0" position with the "ideal transition" time. This is done by examing the relationship of these transitions to the Up/Down Counter count. If the transitions tend to occur more in the "early" or "down" half-cycle of count, then the length of count is reduced to 99 until the relationship is correct. On the other hand, if the transitions tend to occur more in the "late" or "up" half-cycle, then the length of count is increased to 101 until the correct relationship is achieved. The corrections are applied at the "count 0-down" time of the Up/Down Counter. When shortening the count, the Counter goes straight from the "count 0-down" to the "count 1-up" state, whilst when lengthening the count, it stays on the "count 0-down" position for two periods of HSS, the 100 x element-rate clock.

3.3.7 continued

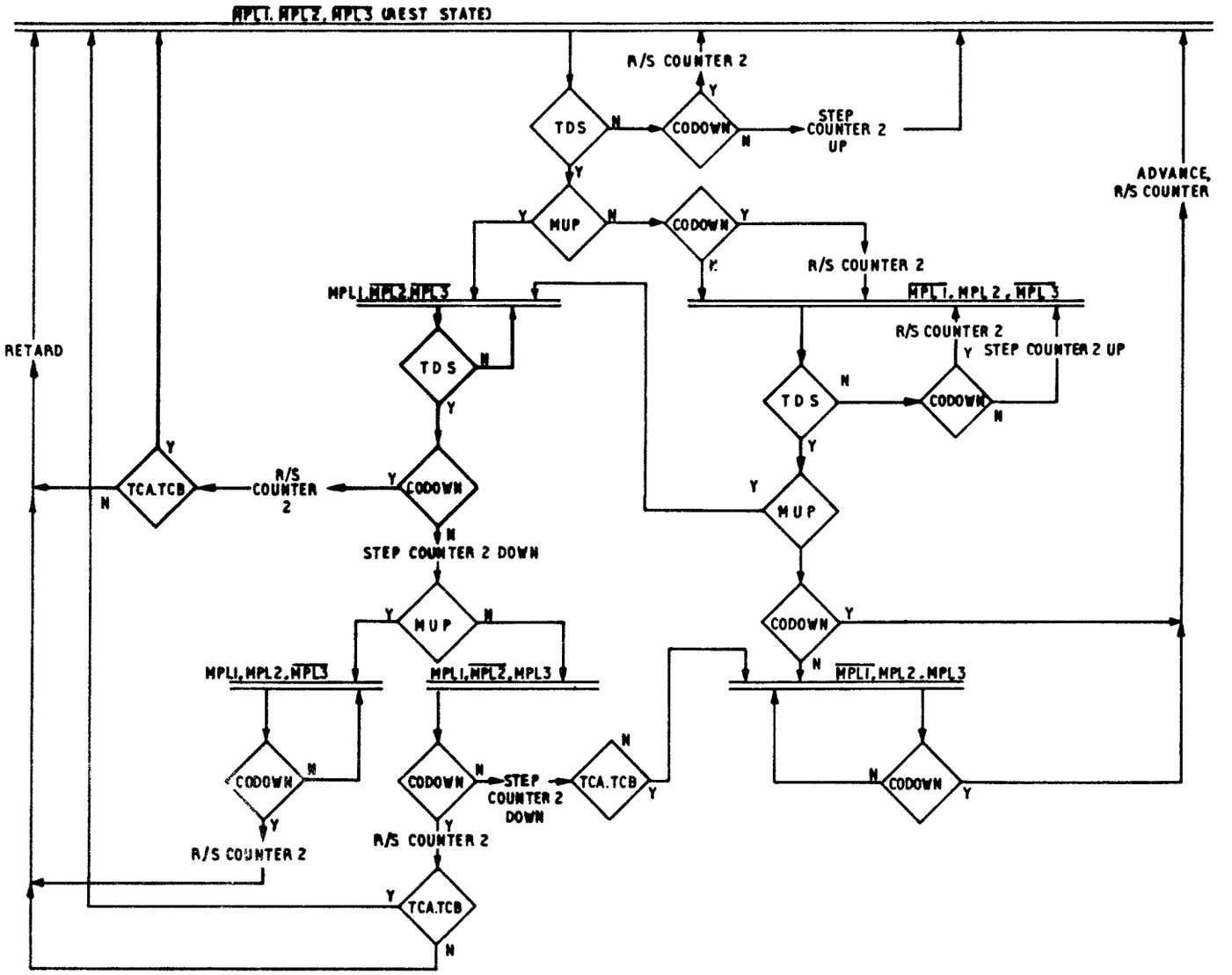
The type of correction to be applied is determined by comparing successive pairs of input data transitions as follows:

(a) If both transitions in a pair occur during the "early" or "up" half-cycle, then correction is applied to shorten (or "advance") the count;

(b) If both occur during the "late" half-cycle, then correction is applied to lengthen (or "retard") the count;

(c) If the two transitions occur during opposite half-cycles, then if the "early" transition occurs at a larger displacement from the counter zero point than does the "late" transition, "advance" correction is applied. Similarly, if the "late" transition is farther from the counter zero point than is the "early" transition, then "retard" correction is applied.

The phase-locking operation is controlled by a 3-stage counter, MPL 1-3, which is used to determine the sequence of actions. A subsidiary 50-way up/down counter is used for determining the relative displacement of successive "early" and "late" transitions. The action is best depicted using the following flow diagram, where the subsidiary up/down counter is referred to as "Counter 2":



FLOW DIAGRAM FOR PHASE-LOCKING ACTION
(SEE TEXT FOR TERMS USED)

AHB7697

DIAG. 6

3.3.7 continued

Note: (i) TDS is the "transition detected" signal from the Input Data Retiming and Transition Detection Circuit (section 3.3.4).

(ii) CODOWN defines the "count 0-down" period of the main 50-way Up/Down Counter.

(iii) TCA and TCB are the terminal count outputs of the first and second stages respectively of Counter 2, the subsidiary 50-way up/down counter.

(iv) MUP is the Up/Down Control bistable of the main 50-way Up/Down Counter. It is set (MUP high) during the "late" half-cycle and reset (MUP low) during the "early" half-cycle.

The 6 sets of double horizontal lines in the diagram represent the 6 combinations or "states" of MPL1-MPL3 which are used in the phase-locking sequence. The "diamond" symbols represent questions with "Yes" (Y) and "No" (N) answers. For example, starting from the "rest" state of $\overline{MPL1}.\overline{MPL2}.\overline{MPL3}$, if a transition is not present (TDS "N"), Counter 2 will be stepped in the up direction, except that if the main 50-way Up/Down Counter is on its "count 0-down" position (CODOWN "Y"), Counter 2 will be reset. If a transition is present (TDS "Y"), however, and the main Up/Down Counter is in its "up" half-cycle (MUP "Y"), then MPL1 will be set and the state of the Phase-Locking Circuit will now be $MPL1.\overline{MPL2}.\overline{MPL3}$. If the transition had occurred during the main Up/Down Counter's "down" half-cycle (MUP "N"), then MPL2 would be set instead and the state would become $\overline{MPL1}.MPL2.\overline{MPL3}$.

3.3.8 Character Length Counter (Fig.5)

This is a 4-stage binary counter, MST1-MST4, which for all positions of the DISPLAY CONTROL switch SW6 other than STOP PULSE is initially held in its "maximum count" position. When detection of start polarity on the data input causes the Start/Stop Control, MS1, to set (section 3.3.5) the counter is allowed to run, being stepped at the centre of each incoming data element period until the centre of the stop element period has been reached. At this point, and if the START STOP - FREE RUN - SYNC switch SW7 is set to START/STOP, MS1 will be reset and the C-L Counter Reset Control, MGR, set, which will reset the counter back to its "maximum count" position. This reset stays on until MGR itself is reset by MS1 being set again and the whole process repeated for the next character.

If the DISPLAY CONTROL switch is set to STOP PULSE the counter is still stepped at the centre of each element period, and when the centre of the step element period is reached and if SW7 is still set to START/STOP, MS1 will be reset, but the Character-Length Counter and Up/Down Counter (section 3.3.2) will be allowed to keep running until the next start polarity is detected on the data input. This sets MGR, which resets the Character-Length Counter to its "maximum count" position and the Up/Down Counter to "count 0-up" and sets MS1 (section 3.3.5). The process is then repeated for this next character.

3.3.8 continued

If SW7 is set to FREE RUN or SYNC, MS1 will not be reset again, thus allowing the counter to run continuously.

MST1-MST4 are formed by IC's.12 and 13. The input clock to MST1 is MUP, the Up/Down Control on IC.12 pin 1. MGR is IC.18(8-13), pin 9 of which is the reset signal to the counter. The clocked set input to MGR for all but STOP PULSE measurement is derived via IC.22(1,2;11,10;13,12); pin 11 is low as $\overline{\text{LOST}}$ on IC.1 pin 11 is high (see Fig.7A), $\overline{\text{C49UP}}$ on pin 1 is a signal from the Up/Down Counter which goes low at "count 49-up" and $\overline{\text{LAB}}$ on pin 13 is a signal which is low during the last state of the Character-Length Counter as selected by the ELEMENTS PER CHARACTER switch SW8 in the Start/Stop Control circuit. IC.19(1,2,13,12) applies control via MGR's asynchronous input pin 10 on IC.18; pin 1 is MS1's reset output and pin 2 is STPOL, a signal which goes high when start polarity as selected in the Start/Stop Control is present on the data input. The set output of MGR on pin 8 of IC.18 is controlled by IC.2(9,8); for other than STOP PULSE measurement, this output is clamped low by $\overline{\text{LOST}}$ on IC.1 pin 9 being high, but for STOP PULSE measurement the signal LOST.MGR is used to set MS1 in the Start/Stop Control circuit (section 3.3.5) after start polarity has been detected.

3.3.9 "Hold Peak" Distortion Stores (Fig.5)

These two stores are used to hold the maximum values of distortion for both "Early" and "Late" transitions of input data. When a transition is detected, the count of the 50-way Up/Down Counter at that instant is compared with the count held in one of the stores (the "Early" or "Late" store as appropriate). If the Up/Down Counter's count exceeds that held in the store, then the counter's count is fed into the store, together with the transition's polarity, to become the new "Hold Peak" value. The "Hold Peak" value of distortion is displayed by detecting when the Up/Down Counter and store counts agree and using this to insert a positive or negative "transition" marked as appropriate at that point. There is only one trace when the DISPLAY CONTROL switch SW6 is set to HOLD PEAK, even when SW7 is set to START/STOP; in this latter condition the 6-9 traces relevant to the SEP.ELEM DIST'N setting are combined into one (section 3.3.11) as the "Hold Peak" value of distortion is for all transitions.

The store for "Early" transitions consists of two 4-bit latches IC's.3(1-11) and 4(13-23). IC.4(10,11) is used to store the polarity of the transition, whilst the remaining 7 latches contain the BCD state of the Up/Down Counter which corresponds to the distortion of that transition. Similarly the "Late" Store consists of the two 4-bit latches IC's.3(13,23) and 4(1-11), where IC.4(10,11) stores the transition - polarity and the remaining latches store the BCD distortion of that transition.

The comparison of the Up/Down Counter and "Hold Peak" stores is done using the two "9324" comparator circuits, IC's.16 and 17. The "A" set of inputs to the comparators is controlled by the "Early" Store outputs during the "Early" or "down" half-cycles of the Up/Down Counter and by the "Late" Store during the "Late" or "up" half-cycle. This is accomplished using IC's.8,9,10(1,2,3;4,5,6;13,12,11) and 11(4,5,6;10,9,8;13,12,11) and signals MUP and $\overline{\text{MUP}}$ from the Up/Down Control bistable via IC.2(11,10;9,8). The "B" set of inputs is controlled by the inverse outputs of the Up/Down

3.3.9 continued

Counter ($\overline{C1}$, $\overline{C2}$ etc.).

The Transition Polarity Selection gates are used to control whether the Store up-dates on positive only, negative only or all transitions. The signal NEG ONLY on IC.7 pin 9 can be taken to 0v by a back-panel link (Fig. 11) if storage of negative transitions only is required. Similarly, $\overline{\text{POS ONLY}}$ on IC.7 pin 12 can be linked to 0v if storage of positive transitions only is required. Signals NTD and PTD on IC.7 pins 10 and 13 are respectively the "negative transition detected" and "positive transition detected" pulses - see section 3.3.4. When a transition is detected and according to the POS ONLY/NEG ONLY linking, IC.7 pins 8 and 11 will go low, taking one "active low" Enable input of each 4-bit latch circuit low.

Up-dating of the "Early" store is controlled by IC.14(1,2,13,12). Pin 1 has a signal from the comparison circuit which is high when the Up/Down Counter's count is greater than the count in the store. Pin 2 is fed by a 100 x element rate signal which is formed by inverting $\overline{\text{HSS}}$ and applying a delay circuit so that the signal goes high approximately 300 nanoseconds after $\overline{\text{HSS}}$ has gone low; this is necessary to prevent the store being up-dated incorrectly at the Up/Down Counter switching times. Pin 13 has the "count down" signal $\overline{\text{MUP}}$ from the Up/Down Control bistable, which goes high for the "Early" half-cycle of the Up/Down Counter. Coincidence of all 3 signals plus a "transition detected" condition as determined by the Transition Polarity Selection gates will generate a "transfer" condition at the "Early" Store by taking both the "active low" Enable inputs of the 4-bit latches low, thus enabling the latches to take up the states of the Up/Down Counter outputs present on 7 of their "D" inputs. The remaining "D" input, IC.4 pin 22 is controlled by MT1 from the Input Data Retiming and Transition Detection circuit (section 3.3.4), so that the corresponding "Q" output on IC.4 pin 23 will go high if the transition which initiated the transfer action is positive.

Up-dating of the "Late" Store is controlled by IC.14(8-11). The signals on the inputs are the same as for the "Early" gate desdribed above, excepting that pin 9 has the "count up" signal MUP, which goes high for the "Late" half-cycle of the Up/Down Counter. In a similar manner to the "Early" Store up-dating, coincidence of all 3 signals plus a "transition - detected" condition causes the state of the Up/Down Counter to be staticised in the latch circuits, together with the transition polarity.

The stores are reset manually by operating the HOLD PEAK RESET push-button PB1, which takes signal $\overline{\text{DRS}}$ on the reset (MR) inputs of the latches to 0v.

The "Hold Peak" transition markers are inserted using IC's.7(1,2,3) and 15. IC.15(1-6) is used to modify the signal TDP, which provides the positive transition marker as described in section 3.3.4. Pin 1 is controlled by the "Early" Store "transition polarity" output (IC.4 pin 23) during the "Early" half-cycle; this is accomplished via IC's.10(10,9,8), 11(1,2,3) and 7(4,5,6). Pin 14 is controlled by the comparator circuit and goes high when the Up/Down Counter and Store counts agree. Pin 2 has the same "deflection modification" signal HSS' as is used for insertion of "actual transition" markers, described in

3.3.9 continued

section 3.3.4. Pin 5 is low unless HOLD PEAK is selected by SW6, when the signal $\overline{\text{HOLPK}}$ on IC.14 pin 5 will be at 0v.

IC.15(8-13) is used to modify the signal $\overline{\text{TDN}}$, which provides the negative transition marker as described in section 3.3.4. The inputs on IC.15 pins 13,10 and 12 are the same as those on pins 2,5 and 4 respectively (on the "$\overline{\text{TDP}}$" gate), whereas that on pin 9 is the inverse of that on pin 1 to insert markers of the opposite polarity.

IC.7(1,2,3) is used to modify $\overline{\text{TDD}}$ which gives the relevant control in the "Bright-Up" Waveform Generation circuit for insertion of transition markers (sections 3.3.13.1 and 3.3.15). Pin 2 is fed by the comparator signal which goes high when the Up/Down Counter and Store counts agree, whilst pin 1 is only high if $\overline{\text{HOLPK}}$ is at 0v on IC.14 pin 5.

3.3.10 C.R.T. X Deflection Circuit (Figs. 2A, 4 and 8A)

The C.R.T. display in the X direction is made up of a series of dots corresponding to logic level information from the digital circuitry. This type of read-out has the advantage of being accurate without the need for complicated alignment against cursor lines.

3.3.10.1 Pump Circuit (Fig.8A)

Conversion from digital to analogue signals for the timebase is made using the Pump Circuit. The signal input to the X Amplifier P.C.B. from the logic is called PUMP, and takes the form of a square wave containing as many positive edges as there are dots required across the C.R.T. screen. This waveform is amplified by TR5 to present a 30v square wave to the pump input capacitor, C13. TR8, the pump transistor, is a common base amplifier with a predominantly capacitive load, C4. The negative edges of the waveform on C13 cause TR8 to conduct and so increase the negative charge across C4. As the collector of TR8 is a very high impedance point, C4 retains its charge until the next negative edge on C13 thereby producing a negative going staircase waveform. For normal start stop working the staircase consists of 99 steps, which is reset at a command from the logic by discharging C4 with TR9. The pump is reset by a positive pulse on the pump reset input REPUMP which turns off TR10, allowing TR9 to conduct due to the base current through R19. An impedance buffer, formed by emitter follower TR11 and 12, is used to couple the timebase waveform from TR8 collector to the input of the X Scan Amplifier. As the X sensitivity of the C.R.T. varies from tube to tube the timebase waveform amplitude is preset by adjusting the A.O.T. capacitor C3.

When using the instrument as an input waveform monitor, the display requirement changes from one element per scan to one character per scan. As the number of dots required for one element is 100, the timebase waveform when displaying a character contains the following number of steps:-

$$100 \times (\text{No. of Elements/Character} + 1.5)$$

3.3.10.1 continued

The reason for the additional 1.5 is that the whole of the start pulse and half a bit of stop pulse are included in the character display. To maintain the timebase waveform amplitude for correct scan length, with a greater number of steps, the pump input waveform on C13 is reduced in amplitude. This reduction is made by switching on TR6 for 5 bit input characters, and TR7 for 6,7 and 8 bit input characters.

3.3.10.2 Pump Input Waveform Generation (Fig.4)

The Pump Circuit input signal PUMP is for the most part equivalent to HSS, the 100 x element-rate clock. When displaying distortion, the effect of the cycle of HSS that occurs during the "count 0-up" period of the Up/Down Counter is gated out, so that the calibration dot positions on the C.R.T. screen for "count 0-down" and "count 0-up" are superimposed; put another way, this is so that the 0% Early and 0% Late marker positions are the same on the screen. When displaying start/stop distortion or the state of the Error Counters, the pump signal is also inhibited during the "all 1's" state of the Character-Length Counter.

PUMP is formed at IC.19(8-11). Pin 9 contains the 100 x element-rate signal $\overline{\text{HSS}}$. Pin 10 has the signal which inhibits PUMP at the "count 0-up" position whilst pin 11 has the signal which inhibits PUMP during the "all 1's" state of the C-L Counter.

3.3.10.3 Pump Reset Generation

The Pump Circuit is reset by the signal REPUMP formed on bistable MFB IC.28(1-6). For the distortion and Error Count display, this bistable is set by the "count 49-up" signal from the Up/Down Counter, i.e. at the end of each scan of marker dots, for all scans, except the last one, when displaying start/stop distortion or the state of the Error Counters. For the latter two conditions, MFB is set just before the beginning of the first trace. Once set, MFB is always reset half a period of HSS later via its asynchronous input. For the INPUT WAVEFORM position of SW6, MFB is set half an element-period after the beginning of the stop pulse, i.e. at the end of the last state of the Character-Length Counter.

The "end of trace" signal $\overline{\text{C49UP}}$ is applied to MFB's set input via IC.26(11,10). The remaining control to this point is applied via IC.26(5,6), and is as follows:

> IC.21(13,12,11) is used to enable the input for all scans except the last. LAB on pin 12 goes low during the last scan, i.e. the last state of the Character-Length Counter, whilst $\overline{\text{DIC}}$ on pin 13 is high for all positions of SW6 other than INPUT WAVEFORM. IC.26(3,4), on the other hand, is used to enable the input during the last state of the C-L Counter (LAB) for the INPUT WAVEFORM, STOP PULSE and non start/stop DISTORTION settings of SW6, as detected by IC.6(1,2,13,12).

MFB is reset using IC.21(10,9,8), which has $\overline{\text{HSS}}$ on pin 9 and $\overline{\text{MUP}}$ (from the Up/Down Control) on pin 10; the effect of this is to apply a negative pulse on IC.28 pin 4 half a period of HSS after the beginning of each trace.

3.3.10.4 X Scan Amplifier (Fig.8A)

The X Scan Amplifier, comprising TR's.13 to 17 mounted on the X Amplifier P.C.B. is a differential type using the input on TR13 base for the scan waveform, and the TR16 base input for X shift. Both input transistors are high frequency amplifiers driving the high voltage common base transistors, TR14 and 15 Quiescent current in both legs of the amplifier is set to approximately 5mA by the constant current transistor TR17. Resistors R25 and 35 are included to prevent either input transistor being switched off, which would limit the speed of operation.

Front panel controls include a horizontal magnifier which increases the gain of the amplifier by connecting the 330 ohm resistor R28 across R29 and R30. This gives an increase in gain of approximately 2.5 times on all switch positions except X1. High frequency gain compensation is provided in the form of C7 and C9 to speed up flyback on the magnified and X1 gain positions respectively. Adjustment of these A.O.T. capacitors is made by connecting a high impedance, low capacity oscilloscope probe to each X output point (TR's.14 and 15 collector). With the probes feeding into a dual trace oscilloscope, the latter being set to add algebraically one normal and one inverted trace, the capacitors are adjusted on their respective gain ranges for optimum flyback conditions at 9.6 Kbits/sec, i.e. not slow and rounded caused by too little capacity and no overshoot caused by too much capacity. Fig.12A gives typical examples of waveforms. The final A.O.T. capacitor, C6 compensates for the removal of the oscilloscope probes and is adjusted for overall picture improvement at 9.6 Kbits/sec by observing the C.R.T. display.

3.3.10.5 Switched X Shift Adjustment (Fig.8A)

On position 3 and 4 of the Horizontal Magnifier switch (50%E to 10%E and 10%L to 50%L), the required X shift is internally generated by the circuitry comprising TR's 18 to 22. Position 3 of the switch connects the logic signal EE (Expand Early) to 0v. This signal is routed via R92 on the motherboard to the emitter of TR19 on the X Amplifier P.C.B. and causes the latter transistor to conduct. A collector current of 1mA, set by R92 4.7K, pulls down the base, and hence emitter of TR18 to a voltage determined by R39 and R40 in parallel. TR18 then increases the current through the lower leg of the X shift potentiometer chains, taking the base of TR16 positive, which centres the early part of the X scan on the C.R.T. Because of a tolerance on the C.R.T. X sensitivity, the amount of X shift requires is preset for a given tube by the A.O.T. resistor R39. To generate the required X shift on switch position 4, the logic signal EL (Expand Late) is routed through R93 on the motherboard to TR20 on the X Amplifier P.C.B. The circuit action is similar to that previously described, but with one more inversion, such that TR22 increases the current through the upper leg of the X shift potentiometer chain, pulling TR10 base more negative. The amount of X shift is preset by the A.O.T. resistor R44.

C12 (47p) is connected between TR16 base and 0v to eliminate the effect of high frequency oscillations.

3.3.11 C.R.T. Y Deflection Circuit (Figs. 2A, 4 and 8B)

Four types of waveform are required for Y deflection:-

3.3.11 continued

(i) A step waveform for the SEP. ELEM DISTN (START/STOP only) STOP PULSE and ERRORS STORE (type 1A only) positions of the DISPLAY CONTROL SWITCH, to give the appropriate number of "element transition" scans.

(ii) A steady "mid-screen" condition for the HOLD PEAK DISTN and SEP. ELEM DISTN (FREE RUN and SYNC modes), where a single scan of marker dots is required.

(iii) Positive and negative transition markers for all but the INPUT WAVEFORM display.

(iv) The input data waveform when set to INPUT WAVEFORM.

For the step waveform of (i), a 4 input binary number DA1-DA4 is applied to R33, R35, R37 and R39. These resistors control the input to the Summing Amplifier (IC.2) and are of such values that a unit level change of DA2 produces twice the voltage excursion on IC.2 pin 6 as that produced by a unit level change of DA1. Similarly a change of unit level at DA3 has four times the effect as that of DA1 and a unit change at DA4 eight times the effect.

The mid screen position (ii) is obtained by holding the DA converter inputs to a fixed position.

The Transition Markers $\overline{TDP}$ (positive transitions) and TDN (negative transitions) (iii) are applied to pin 6 of IC.2 via resistors R26 and R27 respectively and provide the basic 'Y' deflection. The inputs are of opposite polarity and cause the 'blip' to move upwards in the case of a $\overline{TDP}$ pulse and downwards in the case of a TDN pulse.

For the Input Waveform display (iv) the output of the Waveform Display Amplifier (Fig.2A - motherboard) is applied via SW6 (Fig.10) to the 'Y' Scan Amplifier.

3.3.11.1 Digital to Analogue Converter (Fig.8B)

The four element (DA1-DA4) logic inputs to the DA converter are buffered by IC.1-3, 4-5, 6-8, 9-12,13.

The logic state at the input pins of the IC's. determine the voltage level across the associated resistors and hence the level of voltage output from the DA converter to the Summing Amplifier IC.2.

'Pull up' and A.O.T. resistors are included to compensate for variations in the output characteristics of the logic "IC's" buffering the DA converter.

'SUM OUT' output is the result of the total level of inputs to the summing amplifier IC.2 and the amount of amplifier set in by RV4.

3.3.11.2 Digital to Analogue Converter Input Generation (Fig.4)

To give the step waveform described in section (i), the logic controlling the D to A Converter inputs arranges that for the STOP PULSE position of SW6, DA1 is equivalent to the output $\overline{MST1}$ of the 1st bistable stage of the Character-Length Counter, DA2 equivalent to $\overline{MST2}$ from the 2nd bistable, DA3 to $\overline{MST3}$ from the 3rd bistable and DA4 to $\overline{MST4}$ from the 4th bitstable. The same is true for the SEP.ELEM DIST (START/STOP only) and ERROR STORE positions of SW6, except that the "DA" signals are switched to give the "middle scan" position when the Character-Length Counter is in the "all 1's" condition, i.e. for the period starting one-half of a unit element after the beginning of the stop element and ending at the mid-point of the next start element; stated alternatively, this is the period between the end of the last scan for one character and the beginning of the first scan for the following character.

For the condition described in section (ii), the logic arranges the "DA" inputs to give the "middle scan" position continuously. When the ELEMENTS PER CHARACTER switch SW8 is set for 5-unit characters, the middle scan is considered to be the 4th one, i.e. the scan for displaying the transition time between the 3rd and 4th information elements. For 6-8 unit characters the 6th scan position is selected.

The "DA" inputs are formed using IC's.12,20(1,2;3,4;5,6;11,10;13,12) and 13(1,2,3). Selection of the middle scan is done using IC's.6(3-6) and 7(1,2). IC.6 pin 5 is taken low when HOLD PEAK is selected by SW6. Pin 4 always remains high. Pin 3 is controlled by IC.13(4,5,6;13,12,11); it will be held low.

(a) if SYNC or FREE RUN is selected by SW7 and SW6 is not set to ERROR STORE, in which case the signals $\overline{DE}$ and $\overline{SS}$ on IC.13 pins 5 and 4 respectively will be high.

or (b) if the Character-Length Counter is in its "all 1's" state, as detected by signals MST3 and MST4 on IC.13 pins 12 and 13 respectively being high.

When the middle scan is selected, IC.6 pin 6 goes high, and IC.7 pin 2 low, thus preventing the Character-Length Counter outputs ($\overline{MST1}$, $\overline{MST2}$, etc.) from switching the "DA" signals.

3.3.11.3 Y Summing Amplifier (Fig.8B)

IC.2, a linear integrated circuit type ML301AS, is used to add positive and negative transition markers to the D to A waveform. It is operated as an inverting amplifier, the two functions being fed in via input resistors R26 and R27 to pin 2. Transition markers are derived in the logic as $\overline{TDP}$'(negative pulses coinciding with position transitions) and TDN (Positive pulses coinciding with negative transitions). Variable gain, controlled by RV4 in the feedback loop, is used to compensate for the C.R.T. Y sensitivity tolerance, and covers a range of about 0.1:1 to 1.2:1. The 150pF capacitor C8 connected between pins 1 and 2 of IC.5, acts as a speed-up capacitor, by-passing the p.n.p. stage within the IC. and thus improving the device slew rate. Frequency compensation in the form of C10 and supply de-coupling capacitors C9 and 11 are the remaining discrete components required to operate the amplifier.

3.3.11.4 Y Scan Amplifier (Fig.8B)

This amplifier, mounted on the 'Y' Amp Board is similar to the X scan amplifier (section 3.3.10.4) but has no facility for changing the gain. Internally generated Y shift is applied in one direction by the circuitry comprising TR's.6,7 and 8, which is operated when measuring stop pulse length by the front panel logic signal $\overline{\text{LOST}}$.

3.3.12 E.H.T. Box (Fig.9)

This unit consists of two circuit boards and a transformer mounted in a copper plated plastic box, the whole being secured to the rear panel by four nylon screws. TR1, the oscillator transistor, is also mounted on the rear panel for heat dissipation purposes. A simple feedback oscillator is used to convert a 30v stabilised input to the required C.R.T. supplies. The transformer, wound on two Mullard ferrite E cores type FX 1106, has a 12 turn primary winding and a 2 turn feedback winding, C2 being selected for an operating frequency of approximately 25 KHz. Oscillation amplitude is adjusted by means of R1, the A.O.T. resistor, and is initially set to give a potential of -490v at pin 6. Four transformer secondary windings provide the C.R.T. supplies as follows:-

Sec 1 - Output 1375 peak into voltage quadrupler D's 3,4, 5 and 6 for a C.R.T. final anode supply of +5500v.

Sec 2 - Output 490v peak half wave rectified by D1 for -490v C.R.T. cathode supply.

Sec 3 - Output 550v peak half wave rectified by D2 for -550v brightness control potentiometer.

Sec 4 - Output 11v r.m.s. for C.R.T. heaters.

C.R.T. Brightness is controlled by varying the potential on grid 1 from the brightness pot connected between -490v (cathode) and -550v, this allowing -60v for cut-off. The front panel focus control completes a potential divider chain with R's 4 and 5 to supply a focus electrode voltage range of 100v to 220v with respect to the cathode. All supplies to and from the E.H.T. box are connected to the rest of the unit by plug 12 which mates with a socket mounted on the motherboard.

3.3.13 C.R.T. Control Circuits

D.C. conditions for the C.R.T. are arranged such that the majority of the electrodes with signals on are referenced to mean potentials of approximately 100v, therefore capable of being directly driven by transistor circuitry. For this reason the cathode is operated at -500v and the final anode at +5500v, giving a p.d.a. potential of 6KV.

3.3.13.1 "Bright-up" and Blanking Circuits (Figs.2A, 8A and 8B)

Brightness modulation is used to produce C.R.T. trace markers in the form of bright-up for 10% and blank for 0% indication. Bright-up pulses are formed in the logic and routed to the motherboard (Fig.2A) as BRIGHT, these are amplified and inverted by TR26 and a.c. coupled to grid 1 of the C.R.T. As there is a tolerance on the grid cathode potential for a given display brightness, the amplitude of the bright-up pulses is set for a particular tube by adjustment of the A.O.T. resistor R74. The signal BRIGHT is also generated when a transition is detected, being used to bright-up the transition markers when the display is set to Distortion Display. In addition to this, the logic signal TDD is used by TR2 on the X Amp Board (Fig.8A) to increase the size of the bright-up pulse applied to grid 1 of the C.R.T.

Grid 2 is a separate electrode provided in the C.R.T. for blanking, and is driven by the Y Amp Board circuit (Fig.8B) comprising TR's 9 and 10 which converts the logic input BLANK to large amplitude negative pulses referenced to a potential of approximately +110v. Because the circuit is required to blank 1% marker dots at high bit rates, a high speed switching transistor TR10 is used to control a high voltage transistor TR9 with a relatively low low output impedance.

3.3.13.2 Astigmatism (Fig.2A)

This control, RV2, mounted on the front panel, forms part of a potential divider chain with R66 on the motherboard, to supply a voltage range of 125v to the C.R.T. electrode a 3.

3.3.13.3 Trace Curvature (Fig.2A)

This effect is reduced to a minimum by adjustment of the screen control preset potentiometer, RV3, mounted on the underside of the motherboard.

3.3.13.4 Twist Control (Fig.2A)

Twist compensation for the square faced tube is made by adjustment of RV6 mounted on the motherboard. This preset control is used to vary in both directions the current through a twist coil, which is positioned around the neck of the C.R.T.

3.3.13.5 Focus (Fig.2A)

This control, RV3, is mounted on the front panel and provides a variable focussing voltage to anode a 2 of the C.R.T.

3.3.14 Blanking Waveform Generation (Logic, Fig.4)

The signal BLANK on IC.15 pin 8 goes high whenever "blanking" of the C.R.T. trace is required.

This occurs on:

(i) the 0% marker position for the HOLD PEAK DISTN, SEP.ELEM DISTN and STOP PULSE positions of SW6, unless a transition marker is being displayed;

(ii) the period starting one-half of a unit element after the beginning of the stop element and ending one-half of a unit element after the beginning of the next start element, when SW6 is set to HOLD PEAK DISTN or SEP.ELEM DISTN and SW7 to START/STOP;

(iii) the period starting after the start element transition has been detected and ending at the centre of the last information element, when SW6 is set to STOP PULSE;

(iv) the period starting one-half of a unit element after the beginning of the stop element and ending at the beginning of the next start element when SW6 is set to INPUT WAVEFORM and SW7 to START/STOP;

(v) the periods outside the displayed trace(s) for the X3 positions of the HORIZONTAL MAGNIFIER when SW6 is set to HOLD PEAK DISTN or SEP.ELEM DISTN;

(vi) the periods between the marker dots for the ERROR STORE position of SW6.

BLANK is formed on IC.15(10,9,8). To meet the requirements of (ii) and (iv), pin 10 has a signal common to the Pump Input Waveform Generation circuit (section 3.3.10.2), which goes low during the "all 1's" state of the Character-Length Counter when SW7 is set to START/STOP and SW6 to any position other than INPUT WAVEFORM; it will also go low during this period if SW6 is set to ERROR STORE, regardless of the setting of SW7. If SW6 is set to INPUT WAVEFORM, then the signal will also go low if MS1, the Start/Stop Control bistable, is reset.

IC.15(4,5,6) is used to insert the blanking signals of (i), (iii) and (v), by controlling IC.15 pin 9. Pin 4 contains the signal DD, high for all but the INPUT WAVEFORM and ERROR STORE positions of SW6. IC.6(8-11) is used to insert the 0% blanking of (i) via IC.8 pin 4, whilst IC.8 pin 5 is controlled by IC.25 (to insert the blanking described in (iii)) and IC's. 29(3,4;5,6) and 22(1,2,3;4,5,6) (to insert the blanking described in (v)).

The blanking described in (vi) is effected by controlling the signal $\overline{\text{BLANKE}}$ on IC.15 pin 10 from Logic Board 5 (Fig.7); this is described in section 3.3.2

3.3.15 "Bright-Up" Waveform Generation (Logic, Fig.4)

The signal $\overline{\text{BRIGHT}}$ is used to "bright-up" the 10% and transition markers for the distortion displays. The logic to accomplish this is on Logic Board 2 (Fig.4). "Bright-up" markers are also produced at intervals of 10% of a signal element when INPUT WAVEFORM is selected and the HORIZONTAL MAGNIFIER switch SW5 is set to one of the "X3" positions; the logic to accomplish this is on the Mother Board (Fig.2B). The signal $\overline{\text{BRIGHT}}$ is "active low", hence its "NOT" designation.

On Fig.4, IC.18(8-13) is used to insert the distortion display 10% and transition markers. Pin 9 has a signal common to the Pump Input Waveform Generation circuit (section 3.3.10.2), which goes low during the "all 1's" state of the Character-Length Counter when SW7 is set to START/STOP and the DISPLAY CONTROL switch SW6 to any position other than INPUT WAVEFORM; it will also go low during this period if SW6 is set to ERROR STORE, regardless of the setting of SW7. Pin 12 contains the signal DD ("Distortion Display"), formed on Logic Board 3 (IC.21(1-6) on Fig.5), which goes high if SW6 is set to HOLD PEAK DISTN, SEP.ELEM DISTN or STOP PULSE. Pin 13 contains a signal which goes low when blanking is required for the "X3" positions of the HORIZONTAL MAGNIFIER, or for the start and information element period when set to STOP PULSE - see section 3.3.14. Pin 10 has a signal which goes high when a 10% marker dot or a transition marker is to be displayed; TDD on IC.15 pin 1 is the negative going transition marker pulse described in section 3.3.4, whilst the 10% marker control is exercised using IC.8(1,2,3).

The INPUT WAVEFORM 10% "bright-ups" are accomplished using IC.1 on the Mother Board (Fig.2B). If any of the "X3" positions are selected by the HORIZONTAL MAGNIFIER switch SW5, then one of signals $\overline{\text{EM}}$, $\overline{\text{EL}}$ or $\overline{\text{EE}}$ on pins 4, 3 or 5 respectively will be taken to 0v. If SW6 is set to INPUT WAVEFORM then $\overline{\text{DIC}}$ on pin 1 will also be at 0v, thus raising pin 11. The remaining signal on pin 9 is COU, formed on Logic Board 2 (Fig.4), which goes high when the "units" stage of the Up/Down Counter is on count 0, thus the signal BRIGHT on IC.1 pin 1 will be taken low at 10% intervals.

3.3.16 Fox and Q9S Message Error Detection (Fig.6)

Errors in an incoming FOX or Q9S message are detected by comparing it with a locally derived message. The latter message is obtained by addressing the Read-Only Memory (ROM) with the Message-Length Counter. The ROM presents the characters of the message in parallel form to the Local Start/Stop Character Generation circuit, where they are serialised and retimed on bistable MRD. The output of MRD is compared with the incoming message in the Start/Stop Character Error Detection Circuit, where bistable MCE becomes set for each character in error, being reset at the end of each character. The incoming message has to be delayed for two periods of $\overline{\text{HSS}}$ through the Input Data Delay Register, MDD1 and MDD2, to compensate for timing differences between the incoming and locally generated data.

3.3.16 continued

The Element Sampling Point Generation circuit (section 3.3.19) is used to generate the strobe used for sampling the comparison between the two data streams; this strobe can be switched in 5% steps from the 5% Early and Late points of the element to the 45% Early and Late points, using the ERROR THRESHOLD switch SW14 on the rear panel of the unit.

The Start/Stop Message Phasing Control circuit (described below) holds the Message Length Counter initially in the reset state, corresponding to the first character position of the message being received, e.g. "Line Feed" in the case of either FOX message. When the incoming character agrees with this locally-generated character, the reset to the M.-L. Counter is removed and the counter is allowed to step at the end of each character, thus keeping the locally-generated message in phase with the incoming message.

The Start/Stop Message Phasing Control consists of a decade counter which is reset at the end of each error-free character, but which is incremented each time a character-error is detected. If 9 consecutive characters are found to be in error, an "out-of-phase" condition is considered to exist, denoted by the "terminal count" (ETC) on IC.25 pin 15 of the decade counter being present. It is this latter condition which isused to hold the M.-L. Counter in its reset state.

3.3.16.1 Message-Length Counter (Fig.6)

This is a six-stage binary counter, the purpose of which is to define the character positions in the FOX or Q9S messages. The M.-L. Counter Reset Control bistable MRL is used to reset the counter to zero when the end of the message is reached. For the two FOXmessages, the 2 x LF, CR Control bistable MDLF is used to make the counter cycle through its first two states twice because of the double line feed, carriage return sequence at the beginning of each message. Additional resets are applied to the counter when phasing.

The counter itself is formed by bistables ML1-ML6. ML1 changes state with each "end-of-character" signal present on pins 2 and 3 of IC.5, whilst the rest of the counter is "ripple-through". The "end-of-character" signal is formed using IC's.11(4,5,6) and 9(1,2). For the FOX messages, the 2 x LF, CR control MDLF controls the input to ML2 via IC.11(13,12,11), so that ML2 will set until ML1, which clocks MDLF on IC.4 pin 13, has set and reset once.

For the Q9S message, however, Q9S on IC.11 pin 13 will be low, thus holding pin 11 high and allowing the counter to count without interruption. When running normally, the M.L. Counter Reset Control bistable MRL is set when the end of the sequence is detected, using IC's. 19(3,4;5,6), 11(1,2,3;10,9,8) and 16(1,2,13,12), thus resetting the counter by taking the asynchronous inputs of ML2-ML6 and MDLF low, it is unnecessary to reset ML1 at this point as the bistable resets itself.

When the Start/Stop Phasing Control is in its "out-of-phase" condition, signal $\overline{\text{ETC}}$ on the asynchronous inputs of MRL and ML1 will be low, thus holding the M.-L. Counter reset. $\overline{\text{ETC}}$ is also taken low via IC.22(3,4)

3.3.16.1 continued

and TR2 when the PHASE push-button PB2 is pressed, when PHASE on IC.22 pin 3 will go low.

3.3.16.2 Read-Only Memory and Local Start/Stop Character Generation (Fig.6)

The information elements of the FOX and Q9S message characters are stored in the ROM which is addressed by the M.-L. Counter (previous section). Each character is produced at the ROM output in the form of 5-8 parallel bits of information. These are serialised in the local Start/Stop Character Generation circuit, where "start" and "stop" elements are also added, before being fed to the Start/Stop Chara cter Error Detection circuit (next section).

IC's.6 and 7 are DM8810's, the high-level drivers required to drive the ROM address inputs A1-A6. The ROM outputs B1-B8 are fed to IC.20, a "9312" eight-input multiplexer circuit, which is used to serialise the data under the control of the Character-Length Counter outputs MST1', MST2' and MST3'. IC's.3 and 2 (13,12;1,2;5,6) are used to determine the required polarity of start and information elements for the local data, as selected by the START and INFO.EL switches SW3 and SW4 on the front panel. The resultant serial signal is sampled at the '0%' point of the Up/Down Counter, the '0%' signal being formed at IC.18(8-13) and applied via IC.2(9,8;11,10). It is then retimed at bistable MRD.

3.3.16.3 Start/Stop Character Error Detection and Start/Stop Message Phasing Control (Fig.6)

IC.1(4,5,6;10,9,8) is used to compare the incoming message with the locally-generated message. The result is strobed by a signal from the Element Sampling Point Generation circuit (section 3.3.19) via IC.22(1,2;13,12) and the result used to set bistable MCE when an error is detected. MCE is reset at the end of each character by the same signal that is used to step the M.-L. Counter.

The reset output of MCE is fed to the clock input IC.25 pin 2 of the "9310" decade counter of the Start/Stop Message Phasing Control, so that the counter will be stepped at the end of each character in error. At the end of each error-free character, however, a reset will be applied to the counter via IC.26(3-6). When 9 consecutive characters are in error, the counter will reach "count 9" and the terminal count output ETC on IC.25 pin 15 will go high, forcing pin 7 low via IC.19(1,2) and thus maintaining the counter in this position until an error-free character is detected again. Whilst signal ETC is present, the M.-L. Counter is held reset. This condition is also used to control the IN PHASE lamp via IC.23(10,9,8) on Board 5 (Fig.7), which drives IC.9(3,4) and TR1 on Board 4 (Fig.6) which in turn drive the lamp.

3.3.17 Parity Error Detection (Fig.6)

This circuit consists of a bistable MPAR which is reset at the beginning of each character and then allowed to switch every time an information element that is a "1" is detected on the retimed incoming data (bistable MR1 on Fig.7). For the E PARITY position of ERROR COUNT CONTROL switch SW12, an error will be recorded if MPAR and MR1 disagree at the end of a character, whilst in the 0 PARITY position an error will be recorded if MPAR and MR1 agree at this time. MR1 is the first stage of the register used in the Pseudo-Random Generation.

IC.23(1-6) is used to reset MPAR at the beginning of each character; MST1, MST2 etc. are outputs from the Character-Length Counter. IC.16(8-11) is used to sample MR1 (Pin 10) at the element centre C49UP(M) (Pin 11) and set and reset MPAR via IC's. 9(9,8) and 15(10,9,8). Odd or Even parity error detection is determined using IC.15(1,2,3;13,12,11); $\overline{POD}$ on pin 1 goes low when SW12 is set for Odd parity whilst $\overline{PEV}$ on pin 13 goes low for Even parity. IC's.1(13,12,11), 11(9,10) and 15(4,5,6) are used to compare MPAR and MR1. The result is sampled by the same "end-of-character" signal that drives the Message-Length Counter at IC.26(1,2,13,12); pin 2 contains the "end-of-character" signal, pin 13 the result of MPAR and MR1's comparison and pin 1 $\overline{HSS}$, the 100 x element-rate clock. The latter condition is included to gate our transition spikes.

3.3.18 Pseudo-Random Sequence Error Detection (Figs. 6 & 7)

Errors in an incoming 511-bit pseudo-random data stream are detected by comparing it with a locally-generated data stream. The latter sequence is derived using the Pseudo-Random Generator (Fig.6) which is aligned with the incoming data by means of the P-R Phasing Control. Errors are detected by comparing the first stage of the register in the P-R Generator with the output of the Input Data Delay Register (Fig.6) and strobing this either with the output of the Element Sampling Point Generation circuit (Fig.6, section 3.3.19), or CENTRE, the "P-R Centre-Sampling Strobe for Error Check" formed on Board 5 (Fig.7). The Input Data Delay Register is used to delay the incoming data by two periods of $\overline{HSS}$, to compensate for timing differences between the incoming and locally-generated data.

3.3.18.1 Pseudo-Random Generator and Phasing Control (Fig.7)

The P-R Generator is a 9-stage shift register, where the outputs of the fifth and ninth stages are combined in an "Exclusive OR" gate and the result fed back to the first stage. The "all 1's" state of the register is used to set bistable MPRS to derive the P-R Block Timing pulse. The register is clocked by an element-rate signal derived under the control of the P.-R. Phasing Control circuit, as described later. For phasing, this clock consists of a narrow pulse occurring at the element mid-point, so that the received data signal which is being clocked into the register is sampled at the optimum point. When phasing is complete, the clock reverts to being a square wave, the positive edge occurring at the same time position as the narrow pulse would have done but the negative edge now occurring 50% of an element later; as the register switches on negative clock-edges, this means that data derived from the register will have the same nominal bit-phase as the incoming data.

The P-R Phasing Control also controls the input to the 2nd stage MR2 of the register. When phasing, this input consists of the "normalised input data" signal DATAN, whilst when phasing is complete the input is taken from the first stage MR1, so that the 511-bit pattern is circulated. DATAN is formed under the control of the INFO.EL polarity switch SW4, such that a Mark on the INPUT terminal will result in DATAN going positive, regardless of the actual polarity at the terminal.

The P-R Phasing Control circuit consists of two bistables, MPR1 and MPR2, which control the inputs, reset and clock line to the P.-R. Generator. When both bistables are reset, the register-clock consists of a square wave, the negative edges of which coincide with the nominal transition-times of the incoming data . Depressing the PHASE button will take the signal $\overline{\text{PHASE}}$ on MPR1's asynchronous input low and thus set the bistable. This in turn will cause MPR2 to be set on the next clock pulse, but before this happens the condition MPR1.$\overline{\text{MPR2}}$ is used to clear the register. When MPR2 has set, the clock to the register becomes the element mid-point narrow pulse described earlier, in order to clock data into the register via MR2's inputs. When data has been clocked right the way through the register, detected by MR9 becoming set, MPR1 is reset and in turn this resets MPR2, thus reverting the register clock back to the square wave and MR2's inputs to being supplied by MR1.

DATAN and $\overline{\text{DATAN}}$ are derived using IC's.27(10,9,8;13,12,11) and 29(1,2). The input to MR2 is switched using IC.35(10,9,8;13,12,11;1,2,3). The "Exclusive OR" gate on MR1's input is formed by IC.19(1,2,3;4,5,6) and the result applied via IC.27(1,2,3). For P-R working, pin 2 of IC.27 is high but for all other settings of the ERROR COUNT CONTROL SW12 this signal is low and MR1 is fed by DATAN (via IC.27(4,5,6), principally so that in either of the PARITY positions of SW12, MR1 can supply a retimed incoming data signal for parity error detection (see section 3.3.17). The "all 1's" signal is detected on IC.3(8-13).

For the P-R Phasing Control, the register-reset signal is applied using IC. 19(13,12,11). The mid-point sampling pulse is made up using IC.12(8-13), R19, C1 and IC.11(10,9,8) in a straightforward pulse-shortening circuit. The input to this circuit is derived from either the Up/Down Control bistable MUP or the external element-rate ELEMENT TIM. I/P. The latter signal is selected by the USE EXT.EL.TIMING link being present in the Tag Board on the Rear Panel (Fig.11A), when signal $\overline{\text{EXEL}}$ on IC.20 pin 9 is taken to 0v. The selection between the narrow and square wave clock signal for the register is done using IC's.11(4,5,6) and 12(1-6), the latter also providing the drive requirement. IC.29(3,4;5,6;9,8) is used to provide the centre-sampling strobe required for error checks (next section).

If the P-R AUTO REPHASE link is present, phasing will be initiated at the end of every block which contains one or more errors, using IC.28(1,2,13,12) to control the signal $\overline{\text{PHASE}}$. Pin 1 is controlled by MPRS, the P-R Block Timing bistable, pin 2 by the Block Error signal obtained from IC.21 pin 8 (see next section), whilst pin 13 will only be high if the ERROR COUNT CONTROL SW12 is set to either of the 511 P-R positions.

3.3.18.2 Element and Block Error Detection (Fig.6)

Elements in error in the P-R sequence are detected by comparing MR1, the first stage of the P-R Generator register, with MDD2, the output of the Input Data Delay Register. This comparison is strobed either with the output of the Element Sampling Point Generation circuit (section 3.3.19) or by the mid-point strobe signal CENTRE if either the USE EXT.EL.TIMING link is present on the rear panel tag board or the ERROR THRESHOLD % switch SW14 is set to 50. This comparison is used to set bistable MRE, which will reset itself one period of $\overline{\text{HSS}}$ later. The Block Error Detection circuit consists of a pair of "gate" IC's cross-coupled to form a bistable. This bistable is switched one way whenever the "element-error" bistable MRE is set and is switched back the other way at the end of the 511-bit block as detected by MPRS, the P-R Block Timing bistable.

MR1 and MDD11 are compared using IC.21(4,5,6;10,9,8). IC.18(1-6) is used to strobe this comparison with the output of the Element Sampling Point generation; pin 1 contains HSS to prevent unwanted switching spikes whilst pin 5 is low when centre-sampling is required, as described in the previous paragraph. The "50%" setting of SW14 is detected using IC.22(5,6;9,8;11,10). Centre-sampling of the data-comparison is done using IC.16(3-6).

The Block Error Detection "cross-coupled" bistable is formed by IC.17(3,4) and, on Board 5 (Fig.7), IC.21(10,9,8). IC.23(8-11), R29, C1 and IC.1(1,2,3) (all on Fig.6) are used to shorten the signal $\overline{\text{MPRS}}$ from the P-R Block Timing bistable, to give a narrow reset pulse to the Block Error bistable.

3.3.19 Element Sampling Point Generation (Fig.6)

The function of this circuit is to generate a strobe one period of HSS wide to sample the comparison of incoming data with locally-generated data for the purpose of error detection. This strobe is used in both Pseudo-Random Sequence Error Detection (section 3.3.18.2) and Fox and Q9S Message Error Detection (section 3.3.16.3).

The circuit consists of a "9324" comparator circuit whose A=B output goes high when the Up/Down Counter is on the clock times selected by the ERROR THRESHOLD % switch SW14 on the back panel (Fig.11A). The inverse ouputs of the 10's stage of the Up/Down Counter are fed to the first 3 "B" inputs of the comparator whilst the switch outputs, which are "inverse BCD" except for $\overline{\text{SEL5}}$ are fed to the "A" inputs. $\overline{\text{COUNT 5}}$ is applied to the "B3" input to give the intermediate "5%" strobe points whilst COU is applied to the "B4" input to give the "10%" strobe points.

3.3.20 Error Counters (Fig.7)

There are two 3-decade counters, which can be used either to count different functions in parallel or to count the same function in series where Error Counter No.2 acts as an extension to Error Counter No.1; this action is controlled by the COUNTER 2 function switch SW15 on the rear panel.

3.3.20 continued

The functions to be counted are selected via the Error Counter Input Gating. When the counters have reached a count of 999 or a total series count of 999,999 (depending on whether the OVERFLOW function has been selected or not), an inhibit is applied to prevent further counting. Inhibits are also applied when phasing to any of the standard Start/Stop messages on the 511-bit P-R sequence.

For Error Counter No.1, IC.21(13,12,11) is used to enable character errors to be counted for the 5U FOX CHAR, 8U FOX CHAR and Q9S CHAR positions of the ERROR COUNT CONTROL switch SW12. IC.30(1,2,13,12) enables element errors to be counted for the 511-P-R ELEM position of SW12 whilst IC.28(3-6) enables block errors to be counted in the 511 P-R BLOCK position. IC.11(13,12,11) is used to apply an inhibit to the first counter decade when the counter is full. IC36(5,6) applies an inhibit during phasing to Start/Stop messages and IC's.35(4,5,6) and 11(1,2,3) applies an inhibit during phasing to P-R sequences.

For Error Counter No.2, IC.30(3-6) enables the counter to act as an overflow to Error Counter No.1 in the OVERFLOW position of SW15 on the rear panel. The number of P-R Blocks or Start/Stop Messages received is counted using IC.31(9,8) in conjunction with IC's.31(11,10) and 13(13,12,11;10,9,8). The number of Automatic Rephasing actions when receiving start/stop messages is counted using IC.14(1,2,13,12) and Block Errors are counted using IC.14(3-6). IC.31(5,6) applies an inhibit to the first counter decade when the counter is full. IC.36(1,2;3,4) applies an inhibit during phasing to P-R sequences.

3.3.21 Error Display Control (Fig.7)

The error count display is a modified form of the normal "Element Separated" distortion display for a 5-unit character. The tube display consists of 6 horizontal lines of up to 10 dots, where each line represents the decode of a particular counter decade and the number of dots in the line represents the count (0-9) in that decade. These lines of dots are basically the distortion display traces where all but the "5%" marker dots have been blanked out. For each line, the dot representing the "significant digit" of the associated counter decade is given a deflection similar to that for a positive transition in the distortion display, whilst the rest of the line is held blanked out.

The "significant digit" dot is detected by comparing the state of the error counter decade with the state of the "Marker" Counter. This latter counter is also a decade counter, which is reset at the end of each trace scan and stepped for each possible digit position, i.e. at the points corresponding to the 5% markers of the distortion display.

To compare this counter with each of the Error Counters in turn, the "Marker" Counter outputs are fed to the Equivalence Detection circuit "B" inputs, whilst Multiplexer circuits are used under the control of the Character-Length Counter to select the four "A" inputs to the Equivalence Detection circuit; each Multiplexer is fed by the same stage of each decade, so that one Multiplexer selects the "1's" input to the comparator, the next the "2's", the

3.3.21 continued

next the "4's" and the last the "8's". The A=B output from the Equivalence Detection circuit is used to give the "positive transition" marker and also to set bistable MBL. This bistable remains set until the end of the trace scan and whilst set causes the display to be blanked. The Blanking Control also arranges that the intervals between the error display markers are blanked.

IC's. 17, 18, 25 and 26 are the "9312" Multiplexer circuits used to select respectively the "1's", "2's", "4's" and "8's" inputs to the "9324" comparator IC. 16, the Equivalence Detection circuit, which compares these inputs with those obtained from the "Marker" Counter IC. 24. Signal $\overline{\text{COUNT 5}}$ on the ENABLE input on IC. 16 pin 1 goes low at the "5%" points referred to earlier, so that the Equivalence Detection circuit can only give an output at these times. The same signal is used to step the "Marker" Counter. This counter is reset at the end of each scan by the signal C49UP(M), applied via IC. 22(9,8) to its present input on IC. 24 pin 9.

3.3.22 Power Supplies (Figs. 2A and 11)

Mains input to the unit is routed through a 1 amp anti-surge fuse and switch to a mains voltage selector mounted on the rear panel. The front panel mains indicator is connected across the 240v transformer primary to make it independant of input voltage.

3.3.22.1 D.C. Supplies (Fig. 11)

The following d.c. supplies are derived from four transformer secondaries, rectified by diodes mounted on the transformer tag panel, and stabilised, with the exception of the +250v, on the mother board.

(a) +250v. Bridge rectified by diode D1 to D4 and smoothed by C1 and R1. This rail is not stabilised and is used for tube controls and scan amplifiers.

(b) +30v. Bridge rectified by diodes D5 to D8 and smoothed by C2. This rail when stabilised on the mother board is used for E.H.T. and X timebase generation.

(c) +15v and -15v. Half-wave rectified from a common transformer winding by diodes D9 and D10 and smoothed by C's 3 and 4. These supplies, after stabilisation, are used widely for the conversion from digital to analogue signals.

(d) +5v. Full-wave rectified by diodes D11 and D12 mounted on the rear panel for heat sink purposes and smoothed by C's 5 and 6. This supply is stabilised and used mainly for driving the digital integrated circuits.

3.3.22.2 Supply Stabilisers (Fig. 2A)

All four stabilisers, mounted on the mother board, are of a conventional design using a differential amplifier, the output of which drives the final series transistor via an emitter follower. Therefore the following description of the

+15v stabiliser applies in principle to the remaining three. The non-inverting input of the differential amplifier, TR1 base, is held at a constant voltage by the 5.6 zener diode D9, while the inverting input, TR2 base, is used to sense variations on the stabiliser output. A positive variation on the +15v line will cause a corresponding negative variation at TR2 colle ctor, and as there is no inversion through TR3 and TR4 the output will return to its set level. RV1 is a preset voltage control primarily to set the +15v output, but as all stabilisers use the +15v line for a reference, this control affects all stabilised outputs. Adjusting RV1 to set the +5v ensures that all stabilised supplies are within the design limits. The differential amplifier in the +5v stabiliser is an integrated circuit type 741, which gives the advantage of high gain with low offset voltage.

CHAPTER 4

MAINTENANCE INSTRUCTIONS

4.1 Access to the Instrument

WARNING: Isolate the T.D.S.A. from the mains supply before dismantling.

4.1.1 Access to the plug-in sub-boards may be gained by removing the top cover after unscrewing four 3mm Pozidrive screws located at each corner of the cover.

N.B. Care should be taken when removing the following sub-board. (See General Assembly.)

Board 1 - Disconnect the coaxial connection from the front panel.

4.1.2 For removal of the front panel it is necessary to take off the carrying handle, top cover and bottom cover, the latter being held in place by four 3mm screws located at the feet centres. The carrying handle may be disconnected by unscrewing the studs on the side panels using a 4mm hexagon socket wrench. Four 3mm countersunk screws securing the front panel are then accessible, located two each side of the unit. Before complete removal of the front panel the following connections should be removed:

a) PL 11 - Mounted on the left hand side panel and used to connect the mains input to the front panel ON/OFF switch.

b) PL 10 - Mounted on the left hand side panel and used to connect d.c. supplies to the mother board stabilisers.

c) Coaxial connection to board 1 used for variable oscillator frequency control.

The front panel may then be carefully removed from the mother board 100-way edge connector.

4.1.3 Front panel knobs may be removed by pulling out the plastic centre piece which exposes either a hexagon headed or screwdriver slotted collet nut. Loosening the nut by half to three-quarters of a turn will allow the knob to be withdrawn.

4.1.4 Replacement of faulty front panel components will in the case of the following controls require removal of the decorative plate:

All lever switches
Brilliance Control
Focus Control
Astigmatism Control
±20% Variable Speed Control
x and y Shift Control

4.1.4 continued

The decorative plate is secured in place by all the components not listed above. The light emitting diodes are mounted in plastic clips and may be pressed out from the front of the panel. The mains ON indicator is a neon, held in position by a nut at the rear of the panel.

4.1.5 For access to the C.R.T. the front panel must first be removed as described in 4.1.2. Slacken the two screws on the C.R.T. front support bracket, which clamp the mu-metal screen, partly remove the tube and remove the base connection, E.H.T. connection, and twist coil flying leads at the mother board. The C.R.T. complete with its mu-metal screen may then be withdrawn from the equipment.

4.1.6 In order to adjust certain C.R.T. display parameters it is necessary to operate the equipment with the mother board mechanically remote from the left hand side extrusions. To separate these sub-units, the front panel and right hand side panel must first be removed. The latter has no wiring or components attached to it so may be disconnected from the rear panel after removing four 3mm countersunk screws. After removing the mother board rear support, a 3mm screw located on its underside, and the two printed circuit board plugs PL's 6 and 7 the board may be moved clear of the left hand side panel components. To restore the equipment to an electrically operational condition, the front panel must be connected to the mother board 100-way edge connector with PL 10 and PL11 re-connected.

4.1.7 Rear panel components include power transistors, 5v rectifying diodes and E.H.T. box. Access to these components may be gained by removing top and bottom covers, all plug-in boards, plugs PL 6, PL 7 and PL 12, eight 3mm screws, four on each side, and the mother board rear support screw. The rear panel may then be laid flat in an accessible position. If the E.H.T. box is removed from the rear panel it must be replaced using nylon screws.

4.2 Replacement of Components on Printed Circuit Boards

4.2.1 All printed circuit boards in this equipment, with track on both sides, have plated through holes. It is, therefore, only necessary to solder components on the underside of each board. When changing components on these boards the use of a hot soldering iron together with a solder sucking tool is recommended.

4.3 Adjustment of Preset Controls

4.3.1 Stabilised Supplies

All stabilised supplies are referenced to the +15v rail, and may be set up by adjusting RV1, on the underside of the mother board, for the correct potential on the +5v line to be 5.1v $\pm$200mV.

4.3.2 ±20% Variable Oscillator

This oscillator should be adjusted such that its frequency when set to NOM is equal to that of the fixed oscillator. To achieve this connect an input to the unit that produces a 0% transition marker on the bottom trace of an element separated display when switched to a fixed speed. Set the variable speed control to NOM and switch to the UNCAL position. Adjust C7 on board 1 for a display corresponding to that on the fixed oscillator, i.e. a 0% transition marker on the final trace.

4.3.3 x Scan Amplitude

To allow for the C.R.T. manufacturer's tolerance on x plate sensitivity, C7 is adjusted for the correct trace length on each particular tube. An increase in the value of C7 reduces the trace length.

4.3.4 x Amplifier High Frequency Compensation

High frequency compensation for this amplifier is provided by A.O.T. capacitors C6 and C7, the values of which may be selected in the following way:

a) Set up two 10:1 probes using the square wave output from an oscilloscope with a dual trace facility.

b) Connect these probes, one to each of the two x plate outputs on the sub-board, and earth both locally to 0v.

c) Set the oscilloscope to add one normal and one inverted channel of the same gain.

d) Set the T.D.S.A. for a X1 elements separated display on FREE RUN at 9600 BITS/SEC.

e) Adjust C7 on the sub-board for an oscilloscope waveform as close as possible to the ideal waveform shown in Fig. 12A.

f) Switch EXPANDED TRACE to X3 30%E and adjust C6 for the condition given in (e).

g) Remove both oscilloscope probes and set EXPANDED TRACE to X1.

h) Adjust C3 for the optimum spacing of displayed dots in the x direction between 40% and 49% early.

4.3.5 x Shift Preset

Adjustment for the amount of preset x shift required, when increasing the gain of the x amplifier by the EXPANDED TRACE switch, is made by A.O.T. resistors R32 and R39 in the sub-board. The former resistor should be adjusted to centralise the trace on X3 30%E and the latter on X3 30%L.

4.3.6 y Gain Preset

A small amount of adjustment on the display y amplitude is provided by RV4 on the underside of the mother board.

4.3.7 y Amplifier High Frequency Compensation

High frequency compensation for this amplifier is provided by the A.O.T. capacitors C3 and C12, the values for which may be selected in the following way:

a) Set up two 10:1 oscilloscope probes as in 4.3.4(a) and connect them to the y plate outputs on the sub-board.

b) Connect to the input of the T.D.S.A. a 5 unit continuous signal with all 5 elements in a negative condition, and set the controls to view this on an elements separated display at 9600 bits/sec.

c) Using the oscilloscope delayed trace facility, expand the transition marker on the first flat portion of the staircase waveform.

d) Adjust C3 on the sub-board for an oscilloscope display as close as possible to the ideal waveform shown in Fig. 12B.

e) Remove both oscilloscope probes and adjust C12 to compensate for any overshoot, on the transition or flyback points, due to the probe removal.

4.3.8 Twist Correction

Compensation for any display twist on the square faced C.R.T. is provided by RV6, on the underside of the mother board.

4.3.9 Trace Curvature Correction

Adjustment of RV3 on the underside of the mother board will provide trace curvature correction, and should be set in conjunction with the front panel ASTIG control.

4.3.10 10% Markers

A.O.T. resistor R74 provides adjustment for the amplitude of brightness modulation on the 10% markers.

4.3.11 Threshold Detection Preset

After replacement of certain input amplifier components, RV2 on the underside of the mother board may need resetting in the following way:

a) Connect to 1:1 V24 waveform to the input of the T.D.S.A.

b) Set the instrument for shunt working and monitor the junction of TR9 and TR10 emitters with an oscilloscope.

c) Adjust RV2 until the oscilloscope waveform has equal amplitude positive and negative transitions.

CHAPTER 5 - COMPONENTS LIST

INDEX

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 4639-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	4646MD-7	Circuit Diagram.	Ref.	
2	4647MD-8	Drilling Details.	1	
3				
4	ICE000274 ICE001747 ICE001748	I.C. 936 DC - Fairchild. Alt. I.C. U6A 9936 59X- S.G.S. Alt. I.C. MIC 936 5D - I.T.T.	5	IC2,9,17,19,22.
5	ICE000272 ICE001743 ICE001744	I.C. 962 DC - Fairchild. Alt. I.C. U6A9962 59X- S.G.S. Alt. I.C. MIC 962 5D - I.T.T.	2	IC16,26.
6	ICE000273 ICE001745 ICE001746	I.C. 946 DC - Fairchild. Alt. I.C. U6A9946 59X- S.G.S. Alt. I.C. MIC 946 5D - I.T.T.	5	IC1,3,11,15,21.
7	ICE000277 ICE001755 ICE001756	I.C. 930 DC - Fairchild. Alt. I.C. U6A9930 59X- S.G.S. Alt. I.C. MIC 930 5D - I.T.T.	1	IC18.
8	ICE000276 ICE001749 ICE001750	I.C. 932 DC - Fairchild. Alt. I.C. U6A 9932 - S.G.S. Alt. I.C. MIC 932 5D - I.T.T.	1	IC23.
9	ICE000043 ICE001737 ICE001738	I.C. 9093X DC - Fairchild. Alt. I.C. U6A9093 59X- S.G.S. Alt. I.C. MIC 9093X 5D - I.T.T.	7	IC4,5,8,10,12,13,27.
10	ICE000258 ICE001778 ICE001779 ICE001780 ICE001781	I.C. 9310 PC - Fairchild. Alt. I.C. 9310 DC - Fairchild. Alt. I.C. MC 8310P - Motorola. Alt. I.C. U6M9310 59X - Adv.u. Dev. Alt. I.C. U7B 9310 59X - Adv.u. Dev.	1	IC25.
11	ICE000256 ICE001766 ICE001767 ICE001768 ICE001769	I.C. 9324 PC - Fairchild. Alt. I.C. 9324 DC - Fairchild. Alt. I.C. MC 8324P - Motorola. Alt. I.C. U6M 9324 59X - Adv.u. Dev. Alt. I.C. U7B 9324 59X - Adv.u. Dev.	1	IC24.
12	ICE000257 ICE001770 ICE001771 ICE001772 ICE001773	I.C. 9312 PC - Fairchild. Alt. I.C. 9312 DC - Fairchild. Alt. I.C. MC 8312P - Motorola. Alt. I.C. U6M 9312 59X - Adv.u. Dev. Alt. I.C. U7B 9312 59X - Adv.u. Dev.	1	IC20.
13		I.C. M.M.5220 G.J. - National.	1	IC14

ISSUE	6	7	8
DATE	21.5.76. 8.2.78	20.3.78	1.6.78
E.N. Nº	3569	3615	3702

CHECKED	TITLE	SHEET 1 OF SHEETS 2	PRINT ISSUED DATE
DATE	BOARD 4 ASSY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 4639-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
14	ICE001958	I.C. DS 8810 - National.	2	IC6,7.
15				
16	RES000383	Res. 2K7 5% ½w Erie 122.	7	R1,2,3,4,5,6,7.
17	RES000352	Res. 6K8 5% ½w Erie 122.	8	R10,11,12,13,14,15,16,17.
18	RES000339	Res. 1K 5% ½w Erie 122.	7	R8,20,21,22,23,30,31.
19	RES000353	Res. 5K6 5% ½w Erie 122.	7	R18,19,24,25,26,27,28.
20	RES000319	Res. 100 ohms 5% ½w Erie 122.	1	R29.
21	RES000346	Res. 390 ohms 5% ½w Erie 122.	1	R9.
22				
23	CAP 002356	Cap. 1,500pF 500v. 10%. Erie 61013.	1	C1.
24				
25	TRA000229	Transistor BC 107 - Mullard.)	2	TR1,2.
	TRA001551	Alt. Transistor BC 107 - Texas.)		
	TRA001552	Alt. Transistor BC 107 - S.G.S.)		
	TRA001553	Alt. Transistor BC 107 - Motorola.)		
	TRA001554	Alt. Transistor BC 107 - National.)		
26				
27	ACC002609	Transistor Pad TO518-002-Jermyn	2	For TR1,2.
28				
29	DIO 002032	Zener Diode BZY88 C3V3 - Mullard.	1	D1.

ISSUE	1.	2.	3.	4.	5.	6.	7	8
DATE	21.5.76	29.3.77.	31.3.77.	13.6.77.	30.11.77.	8.2.78	20.3.78	1.6.78
C.N. Nº		3198	3221.	3310.	3498.	3569	3615	3702

CHECKED		TITLE	SHEET 2 OF SHEETS 2	PRINT ISSUED DATE
DATE		BOARD 4 ASSY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ-5216-A-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	5399MD-9	Tagboard	1	
2				
3				
4	CON000290	Socket 40S/156 White - Oxley	15	

ISSUE	1.m			
DATE	18.5.79.			
C.N. Nº				
CHECKED		TITLE TAGBOARD ASSEMBLY	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ-5422-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	5417MD-7	Rear View of Front Panel.	Ref.	
2	5189MD-6	Circuit Diagram of Components on Front Panel.	Ref.	
3				
4				
5	4642MD-9	Front Panel	1	
6	5230MD-,	Lever Switch 1 Pole 3 Pos. bias	1	SW B
7	5233MD-7	Lever Switch 2 Pole 4 Pos.	3	SW2, 5 and 8.
8	4408MD-7	Lever Switch 1 Pole 3 Pos.	1	SW7
9				
10	IND000021	Solid State Lamp 5082-4850 - H-Packard.	3	LP2,3 & 4.
11	ACC000010	Plastic Clips 5082-4707 - H-Packard.	3	
12	POT001925 POT002064	Pot. 250 ohms Spectrol Reliance MW.) Alt. Pot. 250 ohms Colvern CLR 1106)	1	RV6
13				
14	POT 002385	Pot. 10K Type L - Plessey.	2	R4, 5.
15				
16	POT000558	Pot. TM Boums 3852C-161-105A.	3	RV1, 2, 3.
17				
18				
19				
20	FIX001140	Screw M2.5 x 6 Ch.Hd.Sl.Cd.Pl.	10	
21	FIX001207	Washer M2.5 Shakeproof Blk.Steel.	10	
22	FIX001303	Nut M2.5 Cd. Pl.	10	
23				
24				
25	FIX001173	M3 Banc-Loc Insert MV3B-M3-PSM.	4	

ISSUE	1.m 2.			
DATE	12.5.76 12.7.77.			
C.N. Nº	3349.			
CHECKED		TITLE FRONT PANEL ASSY. STAGE 1.	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG NO AKJ 3645-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	CON000138	Plug 460-3308-1-03 - Cambion.	2	
2	CON001466	Sleeve 508-1974-06-0010 - Cambion.	2	
3				
4	WIR001458	Sleeve H12 x 20 - Hellermann.	6	
5				
6	WIR 000692	22 swg. Copper Wire.	½m.	
7				
8	WIR 002142	Single Screened Lead 7/0048 - Permanoid.	1m.	
9				
10	WIR 002161	PTFE Sleeving, Red.	¼m.	

ISSUE	[illegible]			
DATE	21.5.76.			
C.N. Nº				
CHECKED		TITLE FRONT PANEL LINKS ASSY.	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AK 1-5994-P1

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	Not Numbered	Green/Yellow	½m	7/0076
2	Not Numbered	Blue	½m	7/0076
3	Not Numbered	White	½m	7/0076
4	Not Numbered	Violet/Brown	½m	7/0076
5	Not Numbered	Violet/Orange	½m	7/0076
6	Not Numbered	White/Brown	½m	7/0076
7	Not Numbered	Red/Green	½m	7/0076
8	Not Numbered	Green	½m	7/0076
9	Not Numbered	White/Green	½m	7/0076
10	Not Numbered	White/Red	½m	7/0076
11	Not Numbered	Green/Black	½m	7/0076
12	Not Numbered	Pink	½m	7/0076
13	Not Numbered	Brown	½m	7/0076
14	Not Numbered	Red/Blue	½m	7/0076
15	Not Numbered	Violet	½m	7/0076
16	Not Numbered	Yellow	½m	7/0076
17	Not Numbered	White/Black	½m	7/0076
18	Not Numbered	White/Orange	½m	7/0076
19	Not Numbered	Blue/Grey	½m	7/0076
20	Not Numbered	Blue/White	½m	7/0076
21	Not Numbered	Red	½m	7/0076
22	Not Numbered	Orange	½m	7/0076
23	Not Numbered	Red/black	½m	7/0076
24	Not Numbered	Grey	½m	7/0076
25	Not Numbered	Blue/Orange	½m	7/0076
26	Not Numbered	Black/White	½m	7/0076
27	Not Numbered	Green/White	½m	7/0076
28	Not Numbered	Red/Orange	½m	7/0076
29	Not Numbered	Orange/Brown	½m	7/0076
30	Not Numbered	White/Grey	½m	7/0076
31	Not Numbered	Orange/Blue	½m	7/0076
32	Not Numbered	Black	1m	14/0076

ISSUE	~			
DATE	18.5.76.			
C.N. Nº				
CHECKED		TITLE T.D.S.A. TYPE 1 C/F 10 PARTS LIST	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ-/142-A-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	5232MD-8	Tube Support (Rear)	1	
2				
3	WIR001342	Ins. Stand Off Terminal W6005 - Harwin	3	
4				
5				
6	CON001494	Plug 40P/156 - Oxley.	1	
7	CON000290	Socket 40S/156 White - Oxley	1	
8				
9	RES000489	Res. 6K8 6w 10% Welwyn W22.	1	R51
10	RES000490	Res. 5K6 6w 10% Welwyn W22.	1	R52
11				
13	FIX002050	Screw 6BA x 3/16" Ch.Hd.Sl.Cd.Pl.	3	
14				
15	FIX001973	Washer 6BA Shakeproof Blk.	3	
16				
17	MOU001228	'U' Section BRS 1A - Kapak Walker.	½m	
18				

ISSUE	1			
DATE	18.5.76.			
C.N. Nº				
CHECKED		TITLE TUBE SUPPORT (REAR) ASSY.	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG NO AKL-7271-P-P1

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	7270MD-6	Circuit Diagram.	Ref.	
2	7269MD-8	Drilling Details.	1	
3				
4	RES000347	Res. 330 ohms 5% ½w Erie 122.	1	R22
5	RES000351	Res. 8K2 5% ½w Erie 122.	1	R21
6	RES000346	Res. 390 ohms 5% ½w Erie 122.	1	R9
7	RES000342	Res. 680 ohms 5% ½w Erie 122.	1	R16
8	RES000339	Res. 1K 5% ½w Erie 122.	11	R1-8, R17,R20,R23.
9	RES000352	Res. 6K8 5% ½w Erie 122.	1	R15
10	RES000355	Res. 12K 5% ½w Erie 122.	1	R12
11	RES000375	Res. 22K 5% ½w Erie 122.	1	R10
12	RES000374	Res. 27K 5% ½w Erie 122.	1	R13
13	RES000368	Res. 82K 5% ½w Erie 122.	1	R11
14	RES000335	Res. 1M5 5% ½w Erie 122.	1	R14
15	RES000343	Res. 560 ohms 5% ½w Erie 122.	2	R18 & R19.
16	CAP000895	Cap. 0.47 uF 250v Mullard C281 VV.	1	C1
17	DIO000235 DIO001810 DIO001811	Diode IN 4148 - Mullard. Alt. Diode IN 4148 - Fairchild. Alt. Diode IN 4148 - I.T.T.	2	D1, D2.
18	TRA000229 TRA001551 TRA001552 TRA001553 TRA001554	Transistor BC 107 - Mullard. Alt. Transistor BC 107 - Texas. Alt. Transistor BC 107 - S.G.S. Alt. Transistor BC 107 - Motorola. Alt. Transistor BC 107 - National.	4	TR2,3,5,6.
19	TRA000227	Transistor BSX 19 - Mullard.	1	TR1.
20	TRA000225 TRA 001562	Transistor 2N 2906 - Mullard. Alt. Transistor 2N 2906 - Motorola.	1	TR4.
21	ACC 002609	Transistor Pad TO518-002-Jermyn	6	For TR1 - 6.
22	ICE000274 ICE001747 ICE001748	I.C. 936 DC - Fairchild. Alt. I.C. U6A 9936 51S - S.G.S. Alt. I.C. MIC 936 5D - I.T.T.	7	IC7,14,16,20,26,29,32.
23	ICE000273 ICE001745 ICE001746	I.C. 946 DC - Fairchild. Alt. I.C. U6A 9946 51S - S.G.S. Alt. I.C. MIC 946 D - I.T.T.	9	IC3,8,11,12,13,15,21, 22,23.

ISSUE	1.	2.	4
DATE	18.5.76.	30.11.77.	8.2.78
C.N. Nº		3498.	3569

CHECKED		TITLE	SHEET 1 OF SHEETS 2	PRINT ISSUED DATE
DATE		BOARD 2 ASSY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ-7271-B-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
24	ICE000272 ICE001743 ICE001744	I.C. 962 DC - Fairchild. Alt. I.C. U6A 9962 51S - S.G.S. Alt. I.C. MIC 962 5D - I.T.T.	6	IC2,6,9,19,25,31.
25	ICE000277 ICE001755 ICE001756	I.C. 930 DC - Fairchild. Alt. I.C. U6A 9930 51S - S.G.S. Alt. I.C. MIC 930 5D - I.T.T.	4	IC1,10,18,30.
26	ICE000043 ICE001737 ICE001738	I.C. 9093X DC - Fairchild. Alt. I.C. U6A 9093 51S - S.G.S. Alt. I.C. MIC 9093X 5D - I.T.T.	4	IC24,28,17,27. N.B. Fit 17 and 24 after test.
27	ICE001783	I.C. U6N 9306 59X Adv.u . Dev.	2	IC4, 5.
28	CAP 002359	Cap. 150 PF 750v. 20%. Erie 61013.	1	C3
29	CAP 002362	Cap. 1,000 PF 750v. 20%. Erie 61013.	1	C2
30	CON 000154	I.C. Socket 14 way 703-4014-01-04-12 - Cambion.	1	For I.C. 17 & 24 Test.

ISSUE	1.	2.	3.	4
DATE	18.5.76.	4.4.77.	13.6.77.	8.2.78
..N. Nº		3158.	3310.	3569

CHECKED		TITLE	SHEET 2 OF SHEETS 2	PRINT ISSUED DATE
DATE		BOARD 2 ASSY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7278B-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	7277MD-6	Circuit Diagram.	Ref.	
2	7276MD-8	Drilling Details.	1	
3				
4				
5	ICE000274	I.C. 936 DC - Fairchild.)		
	ICE001747	Alt. I.C. U6A 9936 5IS - S.G.S.)	4	IC1,2,5,22.
	ICE001748	Alt. I.C. MIC 936 5D - I.T.T.)		
6	ICE000259	I.C. 9308 PC - Fairchild.)		
	ICE001774	Alt. I.C. 9308 DC - Fairchild.)		
	ICE001775	Alt. I.C. MC 8308P - Motorola.)	2	IC3,4.
	ICE001776	Alt. I.C. AM 9308 59C Adv.u Dev.)		
	ICE001777	Alt. I.C. U6N 9308 59X Adv.u Dev)		
7	ICE000277	I.C. 930 DC - Fairchild.)		
	ICE001755	Alt. I.C. U6A 9930 5IS - S.G.S.)	4	IC6,15,23,21.
	ICE001756	Alt. I.C. MIC 930 5D - I.T.T.)		
8	ICE000273	I.C. 946 DC - Fairchild.)		
	ICE001745	Alt. I.C. U6A 9946 5IS - S.G.S.)	7	IC7-11,19,20.
	ICE001746	Alt. I.C. MIC 946 5D - I.T.T.)		
9	ICE000043	I.C. 9093 X DC - Fairchild.)		
	ICE001737	Alt. I.C. U6A 9093 5IS - S.G.S.)	3	IC12,13,18.
	ICE001738	Alt. I.C. MIC 9093 X 5D - I.T.T.)		
10	ICE000272	I.C. 962 DC - Fairchild.)		
	ICE001743	Alt. I.C. U6A 9962 5IS - S.G.S.)	1	IC14.
	ICE001744	Alt. I.C. MIC 962 5D - I.T.T.)		
11	ICE000256	I.C. 9324 PC - Fairchild.)		
	ICE001766	Alt. I.C. 9324 DC - Fairchild.)		
	ICE001767	Alt. I.C. MC 8324 P - Motorola.)	2	IC16,17.
	ICE001768	Alt. I.C. U6M 9324 59X - Adv.u Dev.)		
	ICE001769	Alt. I.C. U7B 9324 59X - Adv.u Dev.)		
12				
13				
14				
15				
16	RES000339	Res. 1K 5% ½w Erie 122.	11	R1-4,R6-8,R10-13.
17				
18				
19	CAP 002353	Cap. 100 PF 750v. 10%. Erie 61013.	1	C1.
20	CAP 002355	Cap. 680 PF 750v. 10%. Erie 61013.	1	C2.

ISSUE	1.	2.	3.
DATE	19.5.76.	31.3.77.	13.6.77.
C.N. Nº		3213	3310.

CHECKED		TITLE	SHEET 1 OF SHEETS 2	PRINT ISSUED DATE
DATE		BOARD 3 ASSY.		

WELD COMMUNICATIONS LTD.	PARTS LIST	DRG No AKJ 7278B-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	DIO000235 DIO001810 DIO001811	Diode IN 4148 - Mullard.) Alt. Diode IN 4148 - Fairchild.) Alt. Diode IN 4148 - I.T.T.)	1	D1

ISSUE	1.A			
DATE	19.5.76.			
E.N. No				
CHECKED		TITLE BOARD 3 ASSY.	SHEET 2 OF SHEETS 2	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7291-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	7290MD-6	Circuit Diagram.	Ref.	
2	7289MD-7	Drilling Details.	1	
3				
4	ICE000274 ICE001747 ICE001748	I.C. 936 DC - Fairchild. Alt. I.C. U6A 9936 5IS - S.G.S. Alt. I.C. MIC 936 5D - I.T.T.	7	IC7,14,15,17,20,27,30.
5	ICE000273 ICE001745 ICE001746	I.C. 946 DC - Fairchild. Alt. I.C. U6A 9946 5IS - S.G.S. Alt. I.C. MIC 946 5D - I.T.T.	5	IC12,16,19,22,23.
6	ICE000272 ICE001743 ICE001744	I.C. 962 DC - Fairchild. Alt. I.C. U6A 9962 5IS - S.G.S. Alt. MIC 962 5D - I.T.T.	5	IC21,24,28,25,26.
7	ICE000277 ICE001755 ICE001756	I.C. 930 DC - Fairchild. Alt. I.C. U6A 9930 5IS - S.G.S. Alt. I.C. MIC 930 5D - I.T.T.	1	IC18.
8	ICE000276 ICE001749 ICE001750	I.C. 932 DC - Fairchild. Alt. I.C. U6A 9932 - S.G.S. Alt. I.C. MIC 932 5D - I.T.T.	1	IC29.
9	ICE001783	I.C. U6N 9306 59X Adv. u. Dev.	2	IC4, 6.
10	ICE000258 ICE001778 ICE001779 ICE001780 ICE001781	I.C. 9310 PC - Fairchild. Alt. I.C. 9310 DC - Fairchild. Alt. I.C. MC 8310P - Motorola. Alt. I.C. U6M 9310 59X Adv. u. Dev Alt. I.C. U7B 9310 59X Adv. u. Dev	1	IC5.
11	ICE000043 ICE001737 ICE001738	I.C. 9093X DC - Fairchild. Alt. I.C. U6A 9093 5IS - S.G.S. Alt. I.C. MIC 9093X 5D - I.T.T.	8	IC1,3,8,9,10,13,2,11.
12	RES000442	Res. 470 ohms 2% ½w Electrosil TR5.	1	R7.
13	RES000319	Res. 100 ohms 5% ½w Erie 122.	3	R46,47,48.
14	RES000345	Res. 470 ohms 5% ½w Erie 122.	1	R2.
15				
16	RES000366	Res. 100K 5% ½w Erie 122.	1	R44.
17	RES000339	Res. 1K 5% ½w Erie 122.	28	R4, 13-16, 18-29, 32-42.
18	RES000385	Res. 2K2 5% ½w Erie 122.	3	R11,10,8.
19	RES000314	Res. 220 ohms 5% ½w Erie 122.	1	R9.
20	RES000382	Res. 3K3 5% ½w Erie 122.	2	R12,31.
21	RES000353	Res. 5K6 5% ½w Erie 122.	3	R3,6,45.

ISSUE	1 ~	4.	5	6 ~.
DATE	18.5.76.	12-1-78.	8.2.78	10.4.78
C.N. Nº		3524	3569	3643

CHECKED		TITLE	SHEET 1 OF SHEETS 3	PRINT ISSUED DATE
DATE		BOARD 1 ASSY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG. No. AKJ 7291-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY.	CIRCUIT LOCATION
22	RES 000352	Res. 6K8 5% ½w Erie 122.	1	R5.
23	RES 000349	Res. 10K 5% ½w Erie 122.	1	R43.
24	RES 000376	Res. 18K 5% ½w Erie 122.	1	R30.
25	RES 000358	Res. 470K 5% ½w Erie 122.	1	R1.
26	RES 000347	Res. 330 ohms 5% ½w Erie 122.	1	R49.
27	DIO 000235 DIO 001810 DIO 001811	Diode IN 4148 - Mullard. Alt. Diode IN 4148 - Fairchild. Alt. Diode IN 4148 - I.T.T.	6	D1 - 6.
28	MIS 002158	Insulating Tape P.V.C. Black.	A/R	To insulate crystal.
29				
30	CAP 000956 CAP 002377	Cap. 47pF Tubular Erie YD. Alt. Cap. 47pF 500v. 20% Erie Ceramic 'K'.	1	C4.
31	CAP 002362	Cap. 1,000pF 750v. 20%. Erie 61013.	1	C3.
32	CAP 002373	Cap. 0.01uF 250v. 10%. Erie 61013.	3	C1,5,8.
33	CAP 001928	Trimmer Cap. 8pF - 50pF Erie 557000E.	1	C7.
34	CAP 001035	Cap. 120pF 30v. 10%. Suflex HS.	1	C6.
35	TRA 000654 TRA 001573 TRA 001574 TRA 001575	Transistor BFY 51 - Mullard. Alt. Transistor BFY 51 - National. Alt. Transistor BFY 51 - S.G.S. Alt. Transistor BFY 51 - Motorola.	2	TR3,5.
36	TRA 000228 TRA 001564 TRA 001565	Transistor BCY 70 - Mullard. Alt. Transistor BCY 70 - Texas. Alt. Transistor BCY 70 - National.	2	TR1,TR10. * See AKJ 7291-PL Sheet 3 for TDSA 1B.
37	TRA 000227	Transistor BSX 19 - Mullard.	3	TR2,8,9.
38	TRA 000229 TRA 001551 TRA 001552 TRA 001553 TRA 001554	Transistor BC 107 - Mullard. Alt. Transistor BC 107 - Texas. Alt. Transistor BC 107 - S.G.S. Alt. Transistor BC 107 - Motorola. Alt. Transistor BC 107 - National.	3	TR4,6,11.
39	TRA 000225 TRA 001562	Transistor 2N 2906 - Mullard. Alt. Transistor 2N 2906 - Motorola.	1	TR7.
40	ACC 002609	Transistor Pad TO518-002-Jermyn	8	

ISSUE	2.	3.	4.	5.	6.
DATE	18.5.76.	13.6.77.	30.11.77.	12-1-78.	8.2.78	10.4.78
C.N. No.		3310.	3498.	3524	3569	3643

CHECKED		TITLE BOARD 1 ASSY.	SHEET 2 OF SHEETS 3	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG. No. AKJ 7291-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY.	CIRCUIT LOCATION
41	MIS 000209	Crystal 2.88 MHz - Crystal Elect.	1	Xtal 1.
42	CON 000294	Socket 450-3704-1-03 - Cambion.	2	Fit to track side on board.
43	CAP 000855	Cap. Disc 0.1uF 30v. Erie Transcap 811T.	2	C12,13.
44	CAP 002359	Cap. 150pF 750v. 20%. Erie 61013.	1	C9.
45	CAP 002353	Cap. 100pF 750v. 10%. Erie 61013.	2	C2,10.
46	CAP 002361	Cap. 330pF 750v. 20%. Erie 61013.	1	C11.
47	WIR 000692	22 s.w.g. BTC Wire.	.1m	
48	WIR 002159	.5 m.m. Bore Black PVC Sleeving.	.1m	
49	ACC 002608	Transistor Pad TO5-001-Jermyn	2	
		On TDSA 1B only fit as follows:-		
50	TRA 000228	Transistor BCY 70 - Mullard.)		
	TRA 001564	Alt. Transistor BCY 70 - Texas.)	1	TR10.
	TRA 001565	Alt. Transistor BCY 70 - National.)		
51	TRA 001932	Transistor BFX 87 - Mullard.)	1	TR1

ISSUE	1.	2. ~	4.	5.	6 ~
DATE	18.5.76.	13.6.77.	12-1-78.	8.2.78	10.4.78
C.N. No.		3310.	3524.	3569	3643

CHECKED		TITLE BOARD 1 ASSY. T.D.S.A. 1B.	SHEET 3 OF SHEETS 3	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ /324B-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	7323MD-6	Circuit Diagram.	Ref.	
2	7322MD-8	Drilling Details. PCB. ISS. 6	1	
3				
4				
5				
6	ICE000274 ICE001747 ICE001748	I.C. 936 DC - Fairchild.) Alt. I.C. U6A 9936 5IS - S.G.S.) Alt. I.C. MIC 936 5D - I.T.T.)	4	IC20,22,29,31.
7	ICE000273 ICE001745 ICE001746	I.C. 946 DC - Fairchild.) Alt. I.C. U6A 9946 5IS - S.G.S.) Alt. I.C. MIC 946 5D - I.T.T.)	8	IC11,13,19,21,23,27, 35,36.
8	ICE000272 ICE001743 ICE001744	I.C. 962 DC - Fairchild.) Alt. I.C. U6A 9962 5IS - S.G.S.) Alt. I.C. MIC 962 5D - I.T.T.)	3	IC14,28,30.
9	ICE000276 ICE001749 ICE001750	I.C. 932 DC - Fairchild.) Alt. I.C. U6A 9932 - S.G.S.) Alt. I.C. MIC 932 5D - I.T.T.)	2	IC3,12.
10	ICE000043 ICE001737 ICE001738	I.C. 9093X DC - Fairchild.) Alt. I.C. U6A 9093 5IS - S.G.S.) Alt. I.C. MIC 9093X 5D - I.T.T.)	7	IC1,2,4,5,6,10,15.
11	ICE000258 ICE001778 ICE001779 ICE001780 ICE001781	I.C. 9310 PC - Fairchild.) Alt. I.C. 9310 DC - Fairchild.) Alt. I.C. MC 8310P - Motorola.) Alt. I.C. U6M 9310 59X Adv. u.Dev) Alt. I.C. U7B 9310 59X Adv. u.Dev)	7	IC7,8,9,24,32,33,34.
12	ICE000257 ICE001770 ICE001771 ICE001772 ICE001773	I.C. 9312 PC - Fairchild.) Alt. I.C. 9312 DC - Fairchild.) Alt. I.C. MC 8312 P - Motorola.) Alt. I.C. U6M 9312 59X Adv. u. Dev.) Alt. I.C. U7B 9312 59X Adv. u. Dev.)	4	IC17,18,25,26.
13	ICE000256 ICE001766 ICE001767 ICE001768 ICE001769	I.C. 9324 PC - Fairchild.) Alt. I.C. 9324 DC - Fairchild.) Alt. I.C. MC 8324P - Motorola.) Alt. I.C. U6M 9324 59X - Adv. u.Dev.) Alt. I.C. U7B 9324 59X - Adv. u.Dev.)	1	IC16.
14				
15				
16	RES000339	Res. 1K 5% ½w Erie 122.	14	R1-7,11,12,15-18,20.
17	RES000353	Res. 5K6 5% ½w Erie 122.	4	R8,9,10,21.

ISSUE	2 ... 3 ...
DATE	19.5.76. 8.2.78
C.N. Nº	3569

CHECKED		TITLE	SHEET 1 OF SHEETS 2	PRINT ISSUED DATE
DATE		BOARD 5 ASSY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ.7324B-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
18	RES000382	Res. 3K3 5% ½w Erie 122.	1	R13.
19	RES000376	Res. 18K 5% ½w Erie 122.	1	R14.
20	RES000319	Res. 100 ohms 5% ½w Erie 122.	1	R19.
21				
22	ACC 002609	Transistor Pad TO518-002-Jermyn	2	For TR 1 & 2.
23	CAP 002373	Cap. 0.01 uF 250v. 10%. Erie 61013.	1	C1.
24				
25	DIO000235 DIO001810 DIO001811	Diode IN 4148 - Mullard.) Alt. Diode IN 4148 - Fairchild.) Alt. Diode IN 4148 - I.T.T.)	6	D1-6.
26	TRA000227	Transistor BSX 19 - Mullard.	2	TR1 & 2.

ISSUE	1 ~ 2. ^ 3 ~			
DATE	18.5.76. 13.6.77. 8.2.78			
C.N. Nº	3310. 3569			
CHECKED		TITLE BOARD 5 ASSY.	SHEET 2 OF SHEETS 2	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ-7350-A-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	7349MD-9	Switch Bracket.	1	
2	5219MD-7	Rotary Switch 2 Pole, 2 Position.	1	

ISSUE	1.m			
DATE	9.5.76.			
E.N. Nº				
CHECKED		TITLE SWITCH SUB-ASSY.	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7425-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	5216PL-9	Tagboard Assy.	1	
2	7350PL-9	Switch Sub-Assy.	1	
3	7445PL-8	Pot. Bracket Sub-Assy.	1	
4	7937PL	E.H.T. Box Assy.	1	
5	7374MD-1	Rear Panel.	1	
6	7302MD-9	Power Input Decorative.	1	
7	7427MD-8	Rear Panel Decorative.	1	
8	7608PL-8	Cableform 10.	1	
9	7936MD-8	E.H.T. Cover Mtg. Tray.	1	
10	7294MD-9	Foot.	4	
11				
12				
13	8110MD-9	Pillar.	1	
14	HOL001241	Fuse Holder L2006-Belling Lee.	1	
15	FUS 002413	Fuse 315 mA S 502 - Beswick.	1	
16	CON001619	Filtered Appliance Inlet L2133A/1 - Belling Lee.	1	SKT9.
17	CON 002778	Voltage Selector MP44-McMurdo	1	
18				
19	8111MD-9	Locking Plate.	1	
20				
21	CON001920	Socket R43-81-048 - Cinch.	1	SKT8.
22	CON001913	Base Assembly R43/81/965 - Cinch.	1	
23	TRA001557	Transistor 2N 3055 - Mullard.	1	
	TRA001556	Alt. Transistor 2N 3055 - Silicon.		
	TRA001558	Alt. Transistor 2N 3055 - Motorola.		
	TRA001559	Alt. Transistor 2N 3055 - Ferranti.		
	TRA001560	Alt. Transistor 2N 3055 - S.G.S.		
	TRA001561	Alt. Transistor 2N 3055 - Fairchild.		
	TRA000223	Alt. Transistor 2N 3055 - R.C.A.		
24	DIO002065	Diode BYX 42-300 - Mullard.	2	
	DIO002066	Alt. Diode 6F10 - Int. Rectifier.		
25	ACC001388	Insulating Kit 56295 - Mullard.	1	
26	ACC000255	Insulating Bush A1230 - Jermyn..	2	
27	[illegible]405	Heat Transfer Washer A26-3024 - Jermyn.	2	

ISSUE	1	3	6
DATE	[illegible]3.76	1.9.77. 23.3.78	17.4.78
C.N. Nº	3398.	3607	3579

CHECKED	TITLE	SHEET 1 OF SHEETS 2	PRINT ISSUED DATE
DATE	TYPE 1A REAR PANEL ASSEMBLY		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7425-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
28	MOU001914	'O' Ring RTOS 7 - Trist.	4	
29	FIX 001853	Solder Tag M5 RC238 - Ross Courtney.	2	
30	MOU 001422	Boot 2-180930-0 - AMP.	3	
31	FIX001058	Screw M2.5 x 10 C'Sk.Hd.Sl.Cd.Pl.	4	
32	FIX001059	Screw M2.5 x 12 C'Sk.Hd.Sl.Cd.Pl.	6	
33	FIX001234	Screw M2.5 x 10 Pan.Hd.Pozi.Chrome	1	
34	FIX001092	Screw M2.5 x 12 Pan.Hd.Sl. Chrome.	2	
35	FIX001145	Screw M3 x 6 Ch.Hd.Sl.Cd.Pl.	2	
36	FIX001153	Screw M4 x 20 Ch.Hd.Sl.Cd.Pl.	4	
37	FIX001209	Washer M2.5 Crinkle - Berym.Cu.	4	
38	FIX001207	Washer M2.5 Shakeproof Blk.Steel.	7	
39	FIX001210	Washer M3 Crinkle Berym. Cu.	4	
40				
41	FIX001303	Nut M2.5 Cd.Pl.	10	
42	FIX001307	Washer M4 Shakeproof Steel Blk.	4	
43	FIX001305	Nut M4 Cd. Pl.	4	
44	FIX001126	Screw M3 x 8 Nylon Ch.Hd. Sl.	4	
45	FIX001184	Screw M3 x 12 Ch.Hd.Sl.Cd.Pl.	2	
46	FIX001838 FIX001431	Solder Tag M3.) Alt. Solder Tag 6BA.)	2	
47	FIX001304	Nut M3 Cd.Pl.	2	
48	FIX001170	M3 Pre.Hard.Insert - P.S.M.	12	
49	FIX001088	Screw M2.5 x 5 Pan.Hd.Sl.Chrome.	1	
50				
51	WIR001458	Sleeve H12 x 20 - Hellermann.	2	
52	WIR001459	Sleeve H15 x 20 - Hellermann.	26	
53	WIR001460	Sleeve H20 x 20 - Hellermann.	13	
54	WIR001464	Sleeve H100 x 25 - Hellermann.	1	
55	7602PL-7	Cableform 2 Assy.	1	
56	CON 000111	Socket 74/10/2356/10 - Painton.	1	SKT.10.
57	CON 001247	Socket 9 way R43-81044-00-000 - Cinch.	1	SKT.11.
58	[illegible]	Faston Receptacle 42599-2 AMP	3	

ISSUE	1.	2.	3.	4.	5	6
DATE	[illegible]	31.3.77.	15.6.77.	23.8.77.	23.3.78	17.4.78
C.N. Nº		3228.	3329.	3388.	3607	3579

CHECKED		TITLE	TYPE 1A REAR PANEL ASSEMBLY	SHEET 2 OF SHEETS 2	PRINT ISSUED DATE

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7426-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	5417MD-7	Rear View of Front Panel.	Ref.	
2	7550MD-6	Switch Circuit Diagram.	Ref.	
3				
4	7607PL-9	Cableform 9 Assy.	1	
5	7603PL-8	Cableform 3 Assy.	1	
6				
7				
8	5645PL	Front Panel Links Assy.	1	
9	6007MD-9	Front Panel Links Wiring/Insp.Schedule	Ref.	
10				
11	5422PL	Front Panel Assy. Stage. 1.	1	
12	7601PL-8	Cableform 1 Assy.	1	
13				
14				
15				
16				
17				
18				
19	5259MD-7	Wafer Switch 2 Pole 11 Pos,	1	SW9.
20	5187MD-7	Wafer Switch 3 Pole 5 Pos.	1	SW6.
21	5188MD-7	Wafer Switch 1 Pole 7 Pos.	1	SW12.
22	4799MD-9	Modified Edge Connector.	1	SKT14.
23				
24	WIR000253	Sleeve 10 m.m. x 10 m.m. Clear Plastic.	1	Fitted over terminal T4.
25				
26	CON000114	Socket 4 m.m. 941-920 - Radiall.	4	T1,2,3,4.
27	SWI 002799	Switch KTA 106D- Waycom.	3	SW3,4,11.
28	SWI 002800	Switch KTA 206N- Waycom.	2	SW1,10.
29	ACC 002801	Lever Cap . Black CP01 - Waycom	5	(For Items 27 & 28).
30	SWI 000489	Switch-Push Button R521QJJBlack, Rendar	2	PB1,2.
31	SWI 001540	Alt. T906 - Arcolectric		
32	[illegible]	Neon 35R-1-F4-AC-R-2-N-6 Plastronics.	1	With Spire Nut. LP1.

ISSUE	1. 2. 3. 4. 5 6
DATE	19.5.76. 17.6.77. 12-7-77. 12-1-78.
C.N. Nº	3299 3353. 3174. 3690 3716

CHECKED		TITLE	SHEET 1 OF SHEETS 2	PRINT ISSUED DATE
DATE		TYPE 1A FRONT PANEL ASSEMBLY. STAGE 2.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7426-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
33				
34				
35				
36				
37				
38				
39		Wire 7/02 White Dye Yellow/Green.	.08m	Used for earthing SW.1.
40	WIR001434	Ins. Stand Off Terminal W8005 - Harwin.	3	
41	FIX001183	Screw M3 x 10 Ch.Hd.Sl.Cd.Pl.	2	
42	FIX001210	Washer M3 Crinkle - Berym.Cu.	2	
43	FIX001910	Screw 8BA x 3/16 Csk.Hd.Sl.Cd.Pl.	4	
44	FIX 001853	Solder Tag M5 RC238 - Ross Courtney.	1	Fit under body of SW1.
45				
46	RES000467	Res. 150 ohms 2% ¼w Electrosil TR4.	3	R2,3 & 4.
47	WIR001459	Sleeve H15 x 20 - Hellermann.	46	
48	WIR001460	Sleeve H20 x 20 - Hellermann.	3	

ISSUE	1	4.	5	6
DATE	19.5.76.	12-1-78.		
C.N. Nº	3174.	3690.	3716	
CHECKED		TITLE TYPE 1A FRONT PANEL ASSEMBLY. STAGE 2.	SHEET 2 OF SHEETS 2	PRINT ISSUED DATE

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ-7445-B-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	5223MD-8	Potentiometer Bracket.	1	
2	7438MD-7	Rotary Switch 3 Pole 10 Pos.	1	SW14.
3	5434MD-7	Rotary Switch 1 Pole 3 Pos.	1	SW15.
4				
5				
6	POT000567	Pot. 1K Bourns 3852A-202-102A.	1	RV7.
7	POT000557	Pot. 25K Bourns 3852A-202-253A.	1	RV8.

ISSUE	1.			
DATE	19.5.76.			
C.N. Nº				
CHECKED		TITLE TYPE 1 POT BRACKET SUB-ASSY	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG. No. AKJ-7452-B-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY.	CIRCUIT LOCATION
1	222406-2	Screen Fixing Brkt.	1	
2	222407-3	Screen.	1	
3				
4	DIO 002032	Zener Diode BZY88C3V3 - Mullard.	2	D1 & D2.
5				
6				
7				
8				
9				
10				
11	RES 000487	Res. 1K 10 w 5% Welwyn W23.	1	
12	WIR 001342	Ins. Stand Off Terminal W6005 - Harwin.	2	
13				
14				
15	FIX 002050	Screw 6BA x 3/16" Ch.Hd.Sl.Cd.Pl.	2	
16				
17	FIX 001306	Washer M3 Shakeproof Blk.Stl.	2	
18	FIX 001973	Washer 6BA Shakeproof Blk.	2	
19	FIX 001307	Washer M4 Shakeproof Blk.Stl.	2	
20	FIX 001145	Screw M3 x 6 Ch.Hd.Stl.Cad.Pl.	2	
21	FIX 001151	Screw M4 x 8 Ch.Hd.Stl.Cad.Pl.	2	
22				
23				
24	5637MD-9	Wiring Schedule.	Ref.	
25	5643MD-9	Inspection Schedule.	Ref.	

ISSUE	2.			
DATE	19.5.76. 15.6.77.			
C.N. No.	3329.			
CHECKED		TITLE SCREEN ASSY.	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7601-B-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	WIR001510	Lacing Cord 1.0 m.m.	A/R	
2	WIR001503	Ident Sleeve 2 m.m. Red - HelvinP20	2	
3	WIR001504	Ident Sleeve 2 m.m. Orange - Helvin P20.	2	
4	WIR001505	Ident Sleeve 2 m.m. Yellow - Helvin P20.	2	
5	WIR001506	Ident Sleeve 2 m.m. Green - Helvin P20.	2	
6	WIR001507	Ident Sleeve 2 m.m. Blue - Helvin P20	2	
7	Not Numbered	Black.	2.7m	14/.0076 PVC Cov. Wire
8	" "	Green/Yellow.	0.4m	" " " "
9				
10	Not Numbered	Brown.	1.4m	7/.0076 PVC Cov. Wire.
11	" "	Red.	1.7m	" " " "
12	" "	Orange.	1.2m	" " " "
13	" "	Yellow.	1.3m	" " " "
14	" "	Green.	1.1m	" " " "
15	" "	Blue.	1.3m	" " " "
16	" "	Violet.	1.7m	" " " "
17	" "	Grey.	1.4m	" " " "
18	" "	White.	1.1m	" " " "
19	" "	Pink.	1.4m	" " " "
20	" "	Red/Black.	0.2m	" " " "
21	" "	Violet/Brown.	0.3m	" " " "
22	" "	White/Red.	0.2m	" " " "
23	" "	White/Orange.	0.3m	" " " "
24	" "	White/Yellow.	0.2m	" " " "
25	" "	White/Green.	0.2m	" " " "
26	WIR 002142	Single Screened Lead 7/0048 - Permanoid.	1.4m	

ISSUE	1			
DATE	17.3			
C.N. Nº				
CHECKED		TITLE T.D.S.A. 1A & 2A. CABLEFORM 1	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7602-C-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	Not Numbered	Orange.	1.3m	7/.0076 PVC Cov. Wire.
2	" "	Yellow.	0.4m	" " " "
3	" "	Green.	0.5m	" " " "
4	" "	Violet.	1.0m	" " " "
5	" "	Grey.	0.5m	" " " "
6	" "	White.	0.9m	" " " "
7	" "	Black.	0.6m	" " " "
8	" "	Pink.	0.6m	" " " "
9	" "	Red/Brown.	0.7m	" " " "
10	" "	Red/Orange.	0.7m	" " " "
11	" "	Red/Green.	1.0m	" " " "
12	" "	Red/Blue.	0.7m	" " " "
13	" "	Red/White.	0.6m	" " " "
14	" "	Red/Black.	0.5m	" " " "
15	" "	Violet/Brown.	0.7m	" " " "
16	" "	Violet/Orange.	0.6m	" " " "
17				
18	" "	White/Red.	1.0m	" " " "
19	" "	White/Green.	0.7m	" " " "
20				
21				
22				
23	Not Numbered	Brown.	0.8m	14/.0076 PVC Cov. Wire.
24	" "	Red.	0.6m	" " " "
25	" "	Orange.	0.4m	" " " "
26	" "	Yellow.	0.4m	" " " "
27	" "	Green.	1.1m	" " " " 0.4m. 2A only. 0.7m. 1A/1B only.
28	" "	Blue.	1.2m	14/.0076 PVC Cov. Wire.
29	" "	Violet.	0.4m	" " " "
30	" "	Grey.	0.4m	" " " "
31	" "	Black.	1.8m	" " " "

ISSUE	1 M			
DATE	19.5.76.			
C.N. Nº				
CHECKED		TITLE T.D.S.A. 1A & 2A. CABLEFORM 2.	SHEET 1 OF SHEETS 2	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7602-C-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
32	Not Numbered	Red/Black.	0.4m	14/.0076 PVC Cov. Wire.
33	" "	Green/Yellow.	0.6m	" " " "
34				
35				
36				
37	WIR001326	'Insulok' Cable Tie T18R.	48m.	
38				
39				
40	WIR 002142	Single Screened Lead 7/0048 - Permanoid.	0.7m	

ISSUE	1.				
DATE	19.5.76.				
C.N. Nº					
CHECKED		TITLE	T.D.S.A. 1A & 2A. CABLEFORM 2.	SHEET 2 OF SHEETS 2	PRINT ISSUED DATE
DATE					

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7603-B-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	WIR001510	Lacing Cord 1.0 m.m.	A/R	
2	CON 002056	Shell 9 way R43-81960-00-000 Cinch	1	
3	CON002060	Plug 74/10/2301/10 - Painton.	1	PL10.
4	CON 002055	Plug 9 way R43-81043-00-000 Cinch.	1	PL11.
5				
6	WIR001459	Sleeve H15 x 20 - Hellermann.	6	
7	WIR001460	Sleeve H20 x 20 - Hellermann.	17	
8	WIR001461	Sleeve H30 x 25 - Hellermann.	1	
9				
10	WIR 002142	Single Screened Lead 7/0048 - Permanoid.	0.7m	
11				
12	Not Numbered	Brown.	0.5m	14/.0076 PVC. Cov. Wire
13	" "	Red.	1.1m	" " " " 0.5m 2A only. 0.6m 1A/1B only.
14	" "	Blue.	0.5m	14/.0076 PVC Cov. Wire
15	" "	Black.	0.5m	" " " "
16	" "	Red/Black.	0.5m	" " " "
17	" "	Green/Yellow.	0.5m	" " " "
18				
19	Not Numbered	Orange.	0.6m	7/.0076 PVC Cov. Wire.
20	" "	Yellow.	0.6m	" " " "
21	" "	Violet.	0.6m	" " " "
22	" "	Grey.	0.6m	" " " "
23	" "	White.	0.6m	" " " "
24	" "	Pink.	0.6m	" " " "
25	" "	Red/Brown.	0.6m	" " " "
26	" "	Red/Orange.	0.6m	" " " "
27	" "	Red/Green.	0.6m	" " " "
28	" "	Red/Blue.	0.6m	" " " "
29	" "	Red/White.	0.6m	" " " "
30	" "	Violet/Brown.	0.6m	" " " "
31	" "	Violet/Orange.	0.6m	" " " "

ISSUE	1.	2.		
DATE	19.5.77.	15.6.77.		
.N. Nº	3329.			
CHECKED		TITLE T.D.S.A. 1A & 2A. CABLEFORM 3.	SHEET 1. OF SHEETS 2	PRINT ISSUED DATE
ATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7603-B-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
32	Not Numbered	White/Red.	0.6m	7/.0076 PVC Cov. Wire
33	" "	White/Green.	0.6m	" " " "

ISSUE	1
DATE	19.5.76.
C.N. Nº	

CHECKED		TITLE	SHEET 2 OF SHEETS 2	PRINT ISSUED DATE
DATE		T.D.S.A. 1A & 2A. CABLEFORM 3.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7607-A-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	Not Numbered	Brown.	0.4m	7/.0076 PVC Cov. Wire.
2	" "	Red.	0.6m	" " " "
3	" "	Orange.	0.7m	" " " "
4	" "	Yellow.	0.6m	" " " "
5	" "	Green.	0.9m	" " " "
6	" "	Blue.	0.4m	" " " "
7	" "	Violet.	0.3m	" " " "
8	" "	Grey.	0.4m	" " " "
9	" "	Black.	0.7m	" " " "
10	" "	Pink.	0.4m	" " " "
11	" "	White/Orange.	0.3m	" " " "
12				
13	WIR001510	Lacing Cord 1.0 m.m.	A/R	

ISSUE	1.			
DATE	19.5.76.			
E.N. Nº				
CHECKED		TITLE T.D.S.A. 1A. CABLEFORM 9.	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ-7608-B-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1				
2	5598MD-9	Edge Connector.	2	PL6 & PL7.
3				
4				
5	WIR001510	Lacing Cord 1.0 m.m.	A/R	
6				
7	WIR001458	Sleeve H12 x 20 - Hellermann.	23	
8	Not Numbered	Violet/Brown.	0.2m	7/.0076 PVC Cov. Wire.
9	" "	Violet/Orange.	0.2m	" " " "
10	" "	Brown.	0.3m	" " " "
11	" "	Red.	0.5m	" " " "
12	" "	Orange.	0.6m	" " " "
13	" "	Yellow.	0.3m	" " " "
14	" "	Green.	0.3m	" " " "
15	" "	Blue.	0.8m	" " " "
16	" "	Violet.	0.8m	" " " "
17	" "	Grey.	0.3m	" " " "
18	" "	White.	0.2m	" " " "
19	" "	Black.	0.8m	" " " "
20	" "	Pink.	0.5m	" " " "
21	" "	Red/Brown.	0.3m	" " " "
22	" "	Red/Orange.	0.2m	" " " "
23	" "	Red/Green.	0.2m	" " " "
24	" "	Red/White.	0.2m	" " " "
25	" "	Red/Black.	0.3m	" " " "
26	" "	Green/White.	0.3m	" " " "
27	" "	White/Brown.	0.4m	" " " "
28	" "	White/Red.	0.4m	" " " "
29	" "	White/Orange.	0.5m	" " " "
30	" "	White/Green.	0.3m	" " " "
31	" "	White/Blue.	0.4m	" " " "
32	" "	White/Grey.	0.3m	" " " "

ISSUE	1.M			
DATE	19.5.76.			
C.N. Nº				
CHECKED		TITLE T.D.S.A. 1A. CABLEFORM 10.	SHEET 1 OF SHEETS 2	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7608-B-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
33	Not Numbered	White/Black.	0.3m	7/.0076 PVC Cov. Wire.

ISSUE	1.m			
DATE	19.5.76.			
C.N. Nº				
CHECKED		TITLE T.D.S.A. 1A. CABLEFORM 10	SHEET 2 OF SHEETS 2	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7930-B-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	7164MD-7	Circuit Diagram.	Ref.	
2	7929MD-9	Drilling Details.	1	
3				
4				
5	WIR001368	Terminal Pin H2105A - Harwin.	2	'C' & '0v' holes only.
6				
7				
8				
9	RES000331	Res. 4.7 ohms 5% ½w Erie 122.	1	R3.
10	RES000325	Res. 33 ohms 5% ½w Erie 122.	1	R1.
11	RES000324	Res. 47 ohms 5% ½w Erie 122.	1	R6.
12	RES000351	Res. 8K2 5% ½w Erie 122.	1	R2.
13	RES000360	Res. 330K 5% ½w Erie 122.	1	R5.
14	RES000338	Res. 1M 5% ½w Erie 122.	1	R4.
15				
16				
17	CAP000852	Cap. 0.01 uF 630v. Radio Spares 113-673.	2	C4,C5.
18	CAP000871	Cap. 0.1uF 160v 10% Wima T.F.M.	1	C2.
19	CAP000985	Cap. 1.0uF 35v. I.T.T.	1	C3.
20	CAP001498	Cap. 10uF 35v. Wima Printilyt.	1	C1.
21				
22				
23	DIO000231 DIO001814	Diode SCM40 - Semtech.) Alt. Diode 1AV 65 - Int. Rectifier.)	2	D1, D2.
24				
25				
26				
27				
28				
29				

ISSUE	1	2.		
DATE	20.5.76.	31.3.77.		
C.N. Nº	3189			
CHECKED		TITLE E.H.T. BOARD ASSY.	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7932-A-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	7931MD-9	Tagboard.	1	
2	7164MD-7	Circuit Diagram.	Ref.	
3				
4				
5	CAP000845	Cap.220pF 8KV.Style A. Erie CD13.	4	C6 - C9.
6				
7	DIO000231 DIO001814	Diode SCM40 - Semtech.) Alt. Diode 1AV 65 - Int.Rectifier)	4	D3-D6.
8				
9	WIR000312	Avlug 1/16" 1107-0208.	6	

ISSUE	1.m			
DATE	19.5.76.			
C.N. Nº				
CHECKED		TITLE TAGBOARD ASSY. (E.H.T. BOX).	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

PARTS LIST | DRG Nº AKJ 7937-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	7930PL-8	E.H.T. Board Assy.	1	
2	7932PL-9	Tagboard Assy.	1	
3	7935MD-8	E.H.T. Cover.	1	
4				
5	7934MD-9	Termination & Clamp Board.	1	
6	7933MD-9	Insulator.	1	
7	7938PL-8	Cableform Assy.	1	
8	222404-4	Insulator.	1	
9	8038PL-8	Transformer Assy.	1	
10				
11	CON002055	Plug R43/B1/043 - Cinch.	1	PL12.
12	CON002056	Shell 9 way R43/B1/960 - Cinch.	1	
13	FIX002052	Screw 6BA x 3/16" C'Sk.Hd.Sl.Cd.Pl.	2	
14	FIX001838	Solder Tag M3.	1	
15	Not Numbered	Wiring Schedule.	Ref.	
16	Not Numbered	Inspection Schedule.	Ref.	
17	WIR 002160	E.H.T. Cable 13/0.2. 357-441 R.S. Comp	55cm	
18	MOU001479	Grommet H.V. 2156 - Hellermann.	2	
19	FIX001418	Drive Fastener 239-ED111-01 - Fastex.	2	
20	FIX000847	Nylon Spacer 44.5 m.m. lg. SK.569. Fitted with M3 Inserts - G & B Proj.	4	
21	TRA000659	Transistor MJE 3055 - Motorola.	1	
22	ACC002057	Heat Transfer Washer A26-3025.Jermyn	1	
23	FIX001126	Screw M3 x 8 Nylon Ch.Hd.Sl.	1	
24	FIX001210	Washer M3 Crinkle - Berym. Cu.	12	
25	FIX001304	Nut M3 Cd.Pl.	2	
26	FIX001145	Screw M3 x 6 Ch.Hd.Sl.Cd.Pl.	10	
27	WIR000312	Avlug 1/16" 1107-0208.	10	Used on Item 5.
28	CON002058	Shroud R71-12426 - United Carr.	1	
29	CON001495	Conn. R71-10425 - Cinch.	1	
30	FIX000641	Nylon Spacer 13 m.m. SK.570. - Fitted with M3 inserts. - G & B Proj.	2	
31				

ISSUE	1.	2.		
DATE	19.5.77.	12-7-77.		
C.N. Nº	3353.			
CHECKED		TITLE E.H.T. BOX ASSY.	SHEET 1 OF SHEETS 2	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7937-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
32	FIX001066	Screw M3 x 12 C'Sk.Hd.Sl.Cd.Pl.	1	
33	FIX001146	Screw M3 x 8 Ch.Hd.Sl.Cd.Pl.	2	
34				
35	WIR001316	'P' Clip NX1 - Insuloid.	1	
36				
37	WIR001460	Sleeve H20 x 20 - Hellermann.	1	
38	WIR001458	Sleeve H12 x 20 - Hellermann.	7	

ISSUE	1.m			
DATE	19.5.76.			
C.N. Nº				
CHECKED		TITLE E.H.T. BOX ASSY.	SHEET 2 OF SHEETS 2	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7938-B-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	Not Numbered	Brown.	0.6m	7/0.2 PVC Cov. Wire
2	" "	Red.	0.4m	" " " "
3	" "	Orange.	0.6m	" " " "
4	" "	Yellow.	0.6m	" " " "
5	" "	Green.	0.8m	" " " "
6	" "	Blue.	0.2m	" " " "
7	" "	Violet.	0.6m	" " " "
8	" "	Grey.	0.2m	" " " "
9	" "	White.	0.2m	" " " "
10	" "	Pink.	0.8m	" " " "
11				
12				
13	WIR001510	Lacing Cord 1.0 m.m.	A/R	

ISSUE	1.m			
DATE	20.5.76.			
C.N. Nº				
CHECKED		TITLE	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE		E.H.T. CABLEFORM.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ.8038B-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	MAG000168	Bobbins Neosid 3004	2	
2	MAG000171	'E' Core Fx 1007 - Mullard	2	
3	MIS 000590	Yellow Polyester Adh. Tape 9 m.m.wide x .001" thk. - Goldcrest.	20cm	
4				
5				
6	Not Numbered	35 s.w.g. En.Cu.Wire S/F.	A/R	Supplied by Manufacturer.
7	Not Numbered	30 s.w.g. En.Cu.Wire S/F.	A/R	Supplied by Manufacturer.
8				
9	Not Numbered	Tape - Insulating.	A/R	Supplied by Manufacturer.
0				
11	Not Numbered	Sleeving. Black.	A/R	Supplied by Manufacturer.
2	Not Numbered	Sleeving. Brown.	A/R	Supplied by Manufacturer.
13	Not Numbered	Sleeving. Red.	A/R	Supplied by Manufacturer.
4	Not Numbered	Sleeving. Orange.	A/R	Supplied by Manufacturer.
15	Not Numbered	Sleeving. Yellow.	A/R	Supplied by Manufacturer.
6	Not Numbered	Sleeving. Green.	A/R	Supplied by Manufacturer.
17	Not Numbered	Sleeving. Blue.	A/R	Supplied by Manufacturer.
8	Not Numbered	Sleeving. Violet.	A/R	Supplied by Manufacturer.
19	Not Numbered	Sleeving. Grey.	A/R	Supplied by Manufacturer.
0	Not Numbered	Sleeving. White.	A/R	Supplied by Manufacturer.

ISSUE	1.m			
DATE	18.5.76.			
E.N. Nº				
CHECKED		TITLE TRANSFORMER ASSY. (EHT BOX)	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8043-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	8042MD-7	Tube Front & CapSupport.	1	
2				
3				
4	WIR001322	'P' Clip NX11 - Insuloid.	4	
5	WIR001324	'P' Clip NX14 - Insuloid.	2	
6	CON001494	Plug 40P/156 - Oxley.	2	
7	CON000290	Socket 40S/156 White - Oxley.	2	
8	CAP000927	Cap. 4,700uF 10v Mullard 07114472.	2	C5,C6.
9	CAP000926	Cap. 2,200uF 25v Mullard 07116222.	2	C3,C4.
10	CAP000925	Cap. 2,200uF 40v Mullard 07117222.	1	C2.
11	CAP 001370	Cap. 47uF 250v. EN R.R. - I.T.T..	1	C1A.
12	CAP 001371	Cap. 47uF 500v. EN R.R. - I.T.T.	1	C1B.
13	FIX001187	Screw M4 x 10 Ch.Hd.Sl.Cd.Pl.	6	
14	FIX001211	Washer M4 Crinkle - Berym.Cu.	6	
15	FIX001134	Washer M4 Plain Cd.Pl.	6	
16	FIX001305	Nut M4 Cd.Pl.	6	
17	FIX 002050	Screw 6BA x 3/16 Ch.Hd.	4	
18	MIS001428	Tesamoll 761 1/8" x 1".	14"	
19	FIX 001973	Washer 6BA S.P.	4	
20	RES000798	Res. 820 ohms 1% 2w Electrosil TR8.	2	R1,R2.
21				
22	5637MD-9	Wiring Schedule.	Ref.	Sht. 5 of 6.
23	5643MD-9	Inspection Schedule.	Ref.	Sht. 4 of 4.
24	MIS001542	Board Guide MCG/7140 - Imhofs.	2	
25				
26	WIR 001342	Insulator H.6005 - Harwin.	4	

ISSUE	1.	2.	3.
DATE	21.5.76.	3.5.77.	27-9-77.
C.N. Nº		3157.	3291.

CHECKED		TITLE	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE		TUBE FRONT AND CAPACITOR SUPPORT SUB-ASSY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8044-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	8043PL	Tube Front and Capacitor Support Sub-Assy.	1	
2	222100-2	Mains Transformer Brkt. Assy.	1	
3	7452PL-8	Screen Assy.	1	
4	7196MD-7	Side Panel.	1	
5				
6	7619MD-9	Insulating Strip.	1	Use Adhesive Thixofix.
7	7142PL-9	Tube Support (Rear) assy.	1	
8				
9				
10	5521MD-9	Special Nut.	2	
11				
12				
13	FIX001414	M4 Solder Tag.	1	
14				
15	MOU001228	'U' Section Brs 1A - Kapak Walker	½m approx	
16				
17				
18				
19	FIX001170	M3 Pre. Hard. Insert - P.S.M.	2	
20	FIX001166	Press Screw M3 x 16 - Rosan.	2	
21	FIX001044	Screw M4 x 12 Hex.Hd. Cd.Pl.	10	
22	FIX001307	Washer M4 Shakeproof Steel Blk.	12	
23	FIX001305	Nut M4 Cd. Pl.	14	
24				
25	WIR001459	Sleeve H15 x 20 - Hellermann.	29	
26	FIX 001134	Washer M4 Plain Cd.Pl.	4	

ISSUE	1			
DATE	18.5.76.			
C.N. Nº				
CHECKED		TITLE	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE		SIDE PANEL ASSY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8045-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	8044PL	Side Panel Assy.	1	
2	7425PL	Rear Panel Assy.	1	
3				
4				
5				
6				
7				
8	7547MD-6	Cir. Dia. Rear & Side Comps.	Ref.	
9	5995MD-9	Cableform 10 Wiring Schedule.	Ref.	
10	5996MD-9	Cableform 10 Inspection Schedule.	Ref.	
11	6005MD-9	Rear Panel Links Wiring Schedule.	Ref.	
12	6006MD-9	Rear Panel Links Inspection Schedule.	Ref.	
13				
14				
15	CON 001246	Base 9 way R43-81961-00-000 - Cinch.	1	
16				
17				
18	FIX 001141	Screw M2.5 x 8 Ch.Hd.Stl.Cad.Pl.	2	
19	FIX 001303	Nut M2.5 Cad.Pl.	2	
20	FIX 001207	Washer M2.5 Shakeproof Blk.Steel.	2	

ISSUE	1.	2.		
DATE	21.5.76.	15.6.77.		
C.N. Nº	3329.			
CHECKED		TITLE	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE		TYPE 1A POWER SUPPLY ASSEMBLY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG. No. AKJ 8047-A3-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY.	CIRCUIT LOCATION
1	7609MD-9	Wiring Schedule.	Ref.	
2	7610MD-9	Inspection Schedule.	Ref.	
3	8051PL	Y. Amp. Board Assy.	1	
4	8052PL	X. Amp. Board Assy.	1	
5	7426PL	Front Panel Assy. Stage 2.	1	
6	8045-PL	Power Supply Assy.	1	
7	8063PL	Mother Board & Cableform Assy.	1	
8	7291PL	Board 1 Assy.	1	
9	7271PL-8	Board 2 Assy.	1	
10	7278PL-8	Board 3 Assy.	1	
11	4639PL-8	Board 4 Assy.	1	
12	7324PL-8	Board 5 Assy.	1	
13	8141MD-4	Insulating Strip.	3	See Assy. Drg.
14	MIS 000599	Double Sided Adhesive Acrylic Polyester Based.	A/R	Use with Item 13.
15	5627MD-9	Spacer.	4	Use Adhesive Thixofix.
16	7619MD-9	Insulating Strip.	1	Use Thixofix Adhesive for Item 14.
17	8040MD-7	Side Panel.	1	
18	5521MD-9	Special Nut.	2	
19	5468MD-9	Screen.	1	
20				
21	NOB 001531	Knob Assy. for 184 Lever Switch - D.H.Cont.	5	
22				
23	NOB 002257	Knob S210-250 Black - Sifam.	3	
24	NOB 002258	Cap C210 Grey - Sifam.	3	
25	NOB 002259	Pointer P210 Grey - Sifam.	3	
26	NOB 002260	Knob S150-250 Black - Sifam.	1	
27	NOB 001861	Cap C150 Grey - Sifam.	1	
28	NOB 002261	Pointer P150 Grey - Sifam.	1	
29	NOB 002262	Knob S100-125 Black - Sifam.	5	
30	NOB 002263	Cap C100 Grey - Sifam.	5	

ISSUE	1.	2.	3.
DATE	21.5.76.	29.3.77.	12-7-77.
C.N. No.		3212.	3353.

CHECKED		TITLE	TDSA TYPE 1A GENERAL ASSY.	SHEET 1 OF SHEETS 2	PRINT ISSUED DATE
DATE					

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8047-A3-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
31	NOB 002264	Pointer P100 Grey - Sifam.	5	
32				
33	IND000022	Oscilloscope Tube D10-210 x 15 - Thorn.	1	
34	MAG000308	Mu-Metal Shield - Magnetic Shields.	1	
35	MAG000178	Twist Coil T24 - Vere.	1	
36				
37	FIX001083	Screw M3 x 8 C'Sk.Hd.Pozidriv.Cd.Pl	12	
38	FIX001146	Screw M3 x 8 Ch.Hd.Sl.Cd.Pl.	1	
39	FIX001210	Washer M3 Crinkle - Berym.Cu.	1	
40				
41	FIX001166	Press Screw M3 x 16 - Rosan.	2	
42	FIX001170	M3 Pre.Hard. Insert - P.S.M.	2	
43				
44	FIX001216	Washer M3 Fibre.	1	
45	FIX001183	Screw M3 x 10 Ch.Hd.Sl.Cd.Pl.	2	
46	FIX001306	Washer M3 Shakeproof Steel Blk.	2	
47	FIX001304	Nut M3 Cd.Pl.	2	
48				
49				
50	7428MD-6	Front Panel Decorative.	1	
51	7429MD-8	Identification Decorative.	1	
52				
53	FIX 001339	Self Tap. Screw No. 2B x 3/16" Pan.Hd.Stl.Cad.Pl.	3	

ISSUE	1.	2.	3.
DATE	21.5.76	29.3.77.	13.6.77.
C.N. Nº		3212.	3299

CHECKED		TITLE	SHEET 2 OF SHEETS 2	PRINT ISSUED DATE
DATE		TDSA TYPE 1A GENERAL ASSY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8050-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	8070MD-6	Circuit Diagram.	Ref.	(2 Sheets).
2	8057MD-7	Drilling Details. P.C.B. Issue 12	1	
3				
4				
5	CON 000298 CON 002788	Edge ConnEWD32/32/FS - Ferranti) Alt. T6P55600/AA/32/32-Ultra)	2	Skt.1,2.
6	CON 000300 CON 002790	Edge Conn EWD40/40/AA/FS -Ferranti Alt. T6P55600/40/40-Ultra	3	Skt.3,4,5.
7	7953MD-9	Edge Connector	2	Skt.6,7.
8				
9				
10				
11	MIS 000533	Vinyl Toluenated Alkyd V991 - Stirling Varnish.	A/R	
12				
13				
14	WIR000312	Avlug 1/16" 1107-0208.	28	
15	ICE000274 ICE001747 ICE001748	I.C. 936 DC - Fairchild.) Alt. I.C. U6A 9936 59X- S.G.S.) Alt. I.C. MIC 936 5D - I.T.T.)	2	IC2,3.
16	ICE000272 ICE001743 ICE001744	I.C. 962 DC - Fairchild.) Alt. I.C. U6A 9962 59X- S.G.S.) Alt. I.C. MIC 962 5D - I.T.T.)	1	IC1.
17	ICE001941 ICE001942 ICE001943 ICE001944	I.C. uA 741 HC - Fairchild.) Alt. I.C. LM 741 CH - National.) Alt. I.C. MC 1741 CG - Motorola.) Alt. I.C. U5B 7741 39X - S.G.S.)	1	IC4.
18				
19				
20	RES000375	Res. 22K 5% ½w Erie 122.	1	R114.
21	RES000328	Res. 18 ohms 5% ½w Erie 122.	1	R21.
22				
23	RES000319	Res. 100 ohms 5% ½w Erie 122.	2	R7, R8.
24	RES000372	Res. 39K 5% ½w Erie 122.	1	R66.
25				
26	CAP 002370	Cap. .022uF 250v.20%. Erie 61013.	1	C21
27	RES000369	Res. 68K 5% ½w Erie 122.	1	R70.

ISSUE	Previous C/Notes	11	12	13
DATE	3202 3436 3538 3615 3692	9.8.78.	29 8 78	30.8.78
C.N. Nº	3353 3454 3569 3673 3738 3775	3771	3752	

CHECKED		TITLE	SHEET 1 OF SHEETS 4	PRINT ISSUED DATE
DATE		TYPE 1A MOTHER BOARD ASSY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8050-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
28	RES000342	Res. 680 ohms 5% ½w Erie 122.	1	R12.
29	RES000339	Res. 1K 5% ½w Erie 122.	3	R13,14,29.
30	RES000388	Res. 1K5 5% ½w Erie 122.	1	R94.
31	RES000387	Res. 1K8 5% ½w Erie 122.	1	R17.
32	RES000385	Res. 2K2 5% ½w Erie 122.	3	R16,22,74.
33				
34				
35	RES000381	Res. 3K9 5% ½w Erie 122.	1	R11.
36	RES000380	Res. 4K7 5% ½w Erie 122.	9	R26,2,3,15,18,20,92,9 R30.
37	DIO002032	Zener Diode BZY88C3V3 - Mullard.	1	D14.
38	RES000363	Res. 180K 5% ½w Erie 122.	1	R67.
39	RES000352	Res. 6K8 5% ½w Erie 122.	3	R23,1,6.
40	RES000351	Res. 8K2 5% ½w Erie 122.	1	R27.
41	RES000349	Res. 10K 5% ½w Erie 122.	2	R19,25.
42	RES000332	Res. 2M2 5% ½w Erie 122.	1	R113.
43	RES000377	Res. 15K 5% ½w Erie 122.	3	R4,5,28.
44				
45				
46	RES000371	Res. 47K 5% ½w Erie 122.	3	R68,69,115.
47				
48	RES000366	Res. 100K 5% ½w Erie 122.	1	R24.
49				
50				
51				
52	CAP 002512	Cap. 47uF 40v. 01617479-Mullard	3	C2,3,4.
53				
54	CAP000879	Cap. 100uF 16v Wima Printilyt.	1	C8.
55	CAP000959 CAP000960	Cap. 220pF Tubular Erie ZD.) Alt. Cap. 220pF Tubular Erie AD.)	1	C9.
56				
57				
58				

ISSUE	Previous C/Notes	11	12	13
DATE	3252 3436 3538 3615 3692 9.8.78.	29 8 78	30.8.78	
C.N. Nº	3353 3494 3569 3673 3738 3775	3771	3752	

CHECKED		TITLE	SHEET 2 OF SHEETS 4	PRINT ISSUED DATE
DATE		TYPE 1A. MOTHER BOARD ASSY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8050-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
59	CAP 000852	Cap. 0.01uF 630v. 113-673 R.S.	1	C13.
60	Not Numbered	A.O.T.	2	C1.
61	CAP001009	Cap. 0.22uF 250v Mullard C281 V.V.	1	C17.
62	DIO000235 DIO001810 DIO001811	Diode IN 4148 - Mullard.) Alt. Diode IN 4148 - Fairchild.) Alt. Diode IN 4148 - I.T.T.)	1	D1.
63	ACC002019	Transistor Pad H181 - Permark.	15	Do not fit to TR26.
64	DIO001899	Zener Diode BZY88-C10-Mullard.	1	D2.
65				
66	TRA000229 TRA001551 TRA001552 TRA001553 TRA001554	Transistor BC 107 - Mullard.) Alt. Transistor BC 107 - Texas.) Alt. Transistor BC 107 - S.G.S.) Alt. Transistor BC 107 - Motorola.) Alt. Transistor BC 107 - National.)	4	TR10,12,13,42.
67	ACC001375	Transistor Pad 10277 - Milton Ross.	4	For IC4 & IC5 and TR14 & TR17.
68	ACC002608	Transistor Pad .TO5-001-Jermyn	4	For TR4,5,16,22.
69	TRA000227	Transistor BSX 19 - Mullard.	2	TR11,26.
70	TRA000654 TRA001573 TRA001574 TRA001575	Transistor BFY 51 - Mullard.) Alt. Transistor BFY 51 - National.) Alt. Transistor BFY 51 - S.G.S.) Alt. Transistor BFY 51 - Motorola.)	1	TR16.
71				
72	TRA000224 TRA000655	Transistor 2N 2910 - Gen.Electric.) Alt. Transistor BFY 82 - S.G.S.)	2	TR14,17.
73				
74	TRA000228 TRA001564 TRA001565	Transistor BCY 70 - Mullard.) Alt. Transistor BCY 70 - Texas.) Alt. Transistor BCY 70 - National.)	1	TR9.
75	POT 001491	Pot. 10K - Daystrom 567-00HS.	1	RV4.)
76	POT000571 POT000560	Pot. 1K. Bourns 3305P-1-102.) Alt. Pot. 1K Daystrom 567-00HS.)	2	RV1) RV2.)) To be mounted on rear of board.
77	POT000556	Pot. 500K. Daystrom 567-00HS.	1	RV3.)
78				

ISSUE	Previous C/Notes	11	12	13
DATE	3202 3436 3538 3615 3692	9.8.78.	29 8 78	30.8.78.
C.N. Nº	3353 3494 3569 3673 3738 3775		3771	3752

CHECKED		TITLE	TYPE 1A. MOTHER BOARD ASSY.	SHEET 3 OF SHEETS 4	PRINT ISSUED DATE
DATE					

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8050-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
79	POT000550	Pot. 5K. Daystrom 567-00HS.	1	RV9. To be mounted at rear of board.
80				
81				
82				
83				
84	ACC001907	Heatsink 5F-2-Redpoint.	3	For TR4,5,22.
85	WIR 002157	Clear PVC Sleeving M60 x 0.5.	17mm	Use with C2.
86				
87	POT000559	Pot. 2K. Daystrom 567-00HS.	1	RV6. Mounted on rear of board.
88				
89	RES000423	Res. 4K7 2% ½w Electrosil TR5.	1	R96.
90	RES000417	Res. 10K 2% ½w Electrosil TR5.	1	R95.
91				
92				
93	RES000382	Res. 3K3 5% ½w Erie 122.	1	R75.
94				
95	WIR 000692	22 swg B.T.C. Wire.	A/R	LK1,2,3.

ISSUE	Previous C/Notes				11	12	13
DATE	[illegible]	[illegible]	3538	3615	3692	9.8.78.	29 8 78	30.8.78.
C.N. Nº	3353	[illegible]	3539	3673	3738	3775	3771	3752

CHECKED		TITLE	TYPE 1A. MOTHER BOARD ASSY.	SHEET 4 OF SHEETS 4	PRINT ISSUED DATE
DATE					

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8051-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	3016MD-9	Drilling Drawing.	1	
2	8060MD-7	Circuit Diagram.	A/R	
3				
4				
5	RES000324	Res. 47 ohms 5% ½w Erie 122.	2	R1,10.
6	RES000319	Res. 100 ohms 5% ½w Erie 122.	3	R48,49,53.
7	RES000316	Res. 150 ohms 5% ½w Erie 122.	1	R7.
8	RES000347	Res. 330 ohms 5% ½w Erie 122.	1	R12.
9	RES000340	Res. 820 ohms 5% ½w Erie 122.	1	R15.
10	RES000339	Res. 1K 5% ½w Erie 122.	6	R6,8,22,23,24,25.
11	RES000389	Res. 1K2 5% ½w Erie 122.	1	R45.
12	RES000388	Res. 1K5 5% ½w Erie 122.	1	R30.
13	RES000387	Res. 1K8 5% ½w Erie 122.	1	R21.
14	RES000385	Res. 2K2 5% ½w Erie 122.	1	R39.
15	RES000383	Res. 2K7 5% ½w Erie 122.	1	R31.
16	RES000382	Res. 3K3 5% ½w Erie 122.	2	R18,41.
17	RES000381	Res. 3K9 5% ½w Erie 122.	1	R13.
18	RES000380	Res. 4K7 5% ½w Erie 122.	5	R16,37,28,46,47.
19	RES000353	Res. 5K6 5% ½w Erie 122.	2	R42,43.
20	RES000352	Res. 6K8 5% ½w Erie 122.	1	R20.
21	RES000349	Res. 10K 5% ½w Erie 122.	2	R35,11.
22				
23	RES000375	Res. 22K 5% ½w Erie 122.	5	R3,14,33,26,27.
24	RES000374	Res. 27K 5% ½w Erie 122.	1	R17.
25	RES000373	Res. 33K 5% ½w Erie 122.	1	R44.
26	Not Numbered	A.O.T.	5	R19,38,36,34,32.
27	RES000384	Res. 2K4 5% ½w Erie 122	1	R40.
28	RES000471	Res. 8K2 2% 1w Electrosil TR6.	1	R4.
29	RES000470	Res. 10K 2% 1w Electrosil TR6.	2	R2,9.
30	POT000864	Pot. 1K Bourns VA-05-H.	1	RV1.
31				
32				

ISSUE	1.m 4.w			
DATE	20.5.76. 8.2.78			
E.N. Nº	3569			
CHECKED		TITLE Y.AMP. BOARD ASSY.	SHEET 1 OF SHEETS 3	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG. No. AKJ 8051-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY.	CIRCUIT LOCATION
33	CON 000140	Mini.Conn. 8129-06-603-003 - Varelco.	1	SKT13.
34	CON 000139	Mini.Conn. 8129-015-603-003 - Varelco.	1	SKT14.
35	CAP 000898	Cap. 0.1uF 250v. Mullard C281 V.V.	3	C1,4,5.
36	CAP 000956	Cap. 47pF Tubular. Erie YD.	3	C10,12,13.
37	CAP 000962	Cap. 22pF Tubular. Erie YD.	1	C7.
38	CAP 001498	Cap. 10uF 35v.Wima Printilyt.	1	C6.
39	CAP 000202	Cap. 0.01uF 25v. Erie Transcap 831T.	1	C8.
40	CAP 000948	Cap. 100uF 10v. Mullard 01614101.	1	C16.
41	CAP 000980	Cap. 1.5uF 35v. I.T.T.	1	C9.
42	Not Numbered	Capacitor A.O.T.	2	C2,3.
43	ICE 000274 ICE 001747 ICE 001748	I.C. 936 DC - Fairchild.) Alt. I.C. U6A 9936 5IS - S.G.S.) Alt. I.C. MIC 936 5D - I.T.T.)	1	IC1.
44	ICE 002086 ICE 002087	I.C. LM 301 AN - Fairchild.) Alt. I.C. LM 301 AN - National.)	1	IC2.
45	CAP 000957	Cap. 100pF Tubular. Erie YD.	1	C14.
46	TRA 000648 TRA 000670 TRA 000672	Transistor 40327 - R.C.A.) Alt. Transistor 2N 3440 - Motorola.) Alt. Transistor 2N 3440 - R.C.A.)	2	TR1,4.
47	TRA 000229 TRA 001551 TRA 001552 TRA 001553 TRA 001554	Transistor BC 107 - Mullard.) Alt. Transistor BC 107 - Texas.) Alt. Transistor BC 107 - S.G.S.) Alt. Transistor BC 107 - Motorola.) Alt. Transistor BC 107 - National.)	5	TR2,3,5,6,8.
48	TRA 000228 TRA 001564 TRA 001565	Transistor BCY 70 - Mullard.) Alt. Transistor BCY 70 - Texas.) Alt. Transistor BCY 70 - National.)	3	TR7,12,13.
49	TRA 000227	Transistor BSX 19 - Mullard.	1	TR10.
50	TRA 001933 TRA 001934	Transistor BF 258 - Texas.) Alt. Transistor BF 258 - Fairchild.)	1	TR9.
51	CAP 000982	Cap. 22uF 25v. I.T.T.	1	C11.
52	ACC 001907	Heatsink 5F-2 - Redpoint.	3	For TR1,4,9.
53				
54	ACC 002608	Transistor Pad 'TO5-001-Jermyn	3	For TR1,4,9.

ISSUE	1.	2. ~	3.	4. ~
DATE	21.5.76.	29.3.77.	30.11.77.	8.2.78
C.N. No.		3172.	3498.	3569

CHECKED		TITLE	Y.AMP. BOARD ASSY.	SHEET 2 OF SHEETS 3	PRINT ISSUED DATE
DATE					

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG. No. AKJ 8051-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY.	CIRCUIT LOCATION
55	ACC 002609	Transistor Pad 'TO518-002-Jermyn	9	For TR2,3,5,6,7,8,10, 12,13.
56	WIR 000692	22 swg. Tinned Cu. Wire.	A/R	Links.
57	CON 000157	Conn. Snaplox 050/LT/B2 - Oxley.	2	Y1, Y2.
58	WIR 000312	Avlug 1/16" 1107-0208.	16	R4,19,32,34,36,38. C2,C3.

ISSUE	1. ~ 4. ~			
DATE	21 5.76. 8.2.78			
C.N. No.	3569			
CHECKED		TITLE Y.AMP. BOARD ASSY.	SHEET 3 OF SHEETS 3	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8052-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	8017MD-9	Drilling Drawing.	1	
2	8059MD-7	Circuit Diagram.	A/R	
3				
4				
5	RES000324	Res. 47 ohms 5% ½w Erie 122.	3	R47,25,37.
6	RES000319	Res. 100 ohms 5% ½w Erie 122.	2	R27,32.
7	RES000316	Res. 150 ohms 5% ½w Erie 122.	1	R46.
8	RES000315	Res. 180 ohms 5% ½w Erie 122.	2	R12,9.
9	RES000347	Res. 330 ohms 5% ½w Erie 122.	1	R31.
10	RES000345	Res. 470 ohms 5% ½w Erie 122.	2	R29,30.
11	RES000342	Res. 680 ohms 5% ½w Erie 122.	2	R20,28.
12	RES000340	Res. 820 ohms 5% ½w Erie 122.	1	R41.
13	RES000339	Res. 1K 5% ½w Erie 122.	5	R1,4,10,14,17.
14	RES000389	Res. 1K2 5% ½w Erie 122.	2	R7,8.
15	RES000388	Res. 1K5 5% ½w Erie 122.	1	R19.
16	RES000387	Res. 1K8 5% ½w Erie 122.	1	R18.
17	RES000385	Res. 2K2 5% ½w Erie 122.	5	R13,16,21,40,43.
18	RES000382	Res. 3K3 5% ½w Erie 122.	2	R2,5.
19	RES000381	Res. 3K9 5% ½w Erie 122.	1	R34.
20	RES000352	Res. 6K8 5% ½w Erie 122.	2	R38,45.
21	RES000471	Res. 8K2 2% 1w Electrosil TR6.	1	R23.
22	RES000349	Res. 10K 5% ½w Erie 122.	2	R6,33.
23	RES000355	Res. 12K 5% ½w Erie 122.	1	R3.
24	RES000375	Res. 22K 5% ½w Erie 122.	2	R26,35.
25	RES000374	Res. 27K 5% ½w Erie 122.	1	R42.
26	RES000370	Res. 56K 5% ½w Erie 122.	1	R22.
27	Not Numbered	A.O.T.	3	R39,44,11.
28	RES000317	Res. 130 ohms 5% ½w Erie 122.	1	R15.
29	RES000470	Res. 10K 2% 1w Electrosil TR6.	2	R24,36.
30	CAP000898	Cap. 0.1uF 250v Mullard C281 V.V.	2	C2,5.
31	CAP000956	Cap. 47pF Tubular Erie YD.	3	C13,14,12.
32	CAP000951	Cap. 0.033uF 160v 10% Wima T.F.M	1	C4.

ISSUE	1.	2.	5.
DATE	21.5.76.	4.11.77.	8.2.78
C.N. Nº	3469.		3569

CHECKED		TITLE X.AMP. BOARD ASSY.	SHEET 1 OF SHEETS 3	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG. No. AKJ 8052-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY.	CIRCUIT LOCATION
33	CAP 002375 CAP 002120	Cap. 0.022uF 250v. 10%. Erie 61013. Alt. Cap. .022pF Tubular. Erie AD.	2	C11*, C15.
34	CAP 000983	Cap. 47uF 16v. I.T.T.	1	C10.
35	CAP 000871	Cap. 0.1uF 160v. 10%. Wima TFM.	1	C8.
36	Not Numbered	Cap. Erie H1-K Type AD. A.O.T.	4	C6,7,9,3.
37	CAP 000855	Cap. Disc 0.1uF 30v. Erie Trans.811T.	1	C17.
38	DIO 000235 DIO 001810 DIO 001811	Diode IN 4148 - Mullard. Alt. Diode IN 4148 - Fairchild. Alt. Diode IN 4148 - I.T.T.	1	D1.
39	CAP 000957	Cap. 100pF Tubular Erie YD.	1	C16.
40	TRA 000227	Transistor BSX 19 - Mullard.	6	TR1,2,3,4,5,8.
41	TRA 000229 TRA 001551 TRA 001552 TRA 001553 TRA 001554	Transistor BC 107 - Mullard. Alt. Transistor BC 107 - Texas. Alt. Transistor BC 107 - S.G.S. Alt. Transistor BC 107 - Motorola. Alt. Transistor BC 107 - National.	8	TR6,7,12,13,17,19, 20,22.
42	TRA 002068 TRA 002069 TRA 002070 TRA 002071 TRA 002072	Transistor BC 109 - Mullard. Alt. Transistor BC 109 - Texas. Alt. Transistor BC 109 - S.G.S. Alt. Transistor BC 109 - Motorola. Alt. Transistor BC 109 - National.	1	TR11.
43	TRA 002074	Transistor BSX 29 - S.G.S.	1	TR10.
44	TRA 002075 TRA 002076	Transistor 2N 2905A - Mullard. Alt. Transistor 2N 2905A - Motorola.	1	TR9.
45	TRA 000648 TRA 000670 TRA 000672	Transistor 40327 - R.C.A. Alt. Transistor 2N 3440 - Motorola. Alt. Transistor 2N 3440 - R.C.A.	2	TR14,15.
46	TRA 000228 TRA 001564 TRA 001565	Transistor BCY 70 - Mullard. Alt. Transistor BCY 70 - Texas. Alt. Transistor BCY 70 - National.	2	TR18,21.
47	TRA 000654 TRA 001573 TRA 001574 TRA 001575 TRA 001576	Transistor BFY 51 - Mullard. Alt. Transistor BFY 51 - National. Alt. Transistor BFY 51 - S.G.S. Alt. Transistor BFY 51 - Motorola. Alt. Transistor BFY 51 - I.T.T.	1	TR16.
48	ACC 001907	Heatsink 5F-2 - Redpoint.	2	For TR14,15.
49	C [illegible]96	Cap. 0.01uF 500v. Erie 811.	1	C1.

ISSUE	1.	2.	3.	4.	5.
DATE	31.5.76.	29.3.77.	13.6.77.	30.11.77.	8.2.78
C.N. No.		3172.	3310.	3498.	3569

CHECKED		TITLE	SHEET 2 OF SHEETS 3	PRINT ISSUED DATE
DATE		X.AMP. BOARD ASSY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG. No. AKJ 8052-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY.	CIRCUIT LOCATION
50	ACC 002608	Transistor Pad TO5-001-Jermyn	3	For TR14,15,9.
51	ACC 002609	Transistor Pad TO518-002-Jermyn	19	For Remaining TR's.
52	CAP 000854	* Alternative: Cap. 0.022uF 25v. Erie Transcap 831T.	1	C11 * only.
53	DIO 002067	Diode BAX 16 - Mullard.	1	D2.
54	CON 000139	Mini-Conn. 8129-015-603-003 - Varelco.	1	SKT15.
55	CON 000140	Mini-Conn. 8129-06-603-003 - Varelco.	1	SKT16.
56	WIR 000692	22 swg. Tinned Cu. Wire.	A/R	Links.
57	CON 000157	Conn. Snaplox 050/LT/B2 - Oxley.	2	X1,X2.
58	WIR 000312	Avlug 1/16" 1107-0208.	12	R39,R44. C3,6,7,9.

ISSUE	2. ~ 5.			
DATE	21.5.76. 31.3.77. 8.2.78			
C.N. No.	3220. 3569			
CHECKED DATE		TITLE X.AMP. BOARD ASSY.	SHEET 3 OF SHEETS 3	PRINT ISSUED DATE

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8061-C-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	Not Numbered	Black.	0.5m	PVC Cov. Wire 7/0.2mm.
2	" "	Brown.	1m	" " " "
3	" "	Red.	1m	" " " "
4	" "	Orange.	1m	" " " "
5	" "	Yellow.	0.5m	" " " "
6	" "	Green.	1m	" " " "
7	" "	Blue.	1m	" " " "
8	" "	Violet.	1m	" " " "
9	" "	Grey.	1m	" " " "
10	" "	White.	1m	" " " "
11	" "	Pink.	0.5m	" " " "

ISSUE	1.m			
DATE	21 5.7[illegible]			
C.N. Nº				
CHECKED		TITLE TDSA 1A & 2A. CABLEFORM 11.	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8062-C-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	Not Numbered	Black.	1m	PVC Cov. Wire 7/0.2mm
2	" "	Brown.	1m	" " " "
3	" "	Red.	0.5m	" " " "
4	" "	Orange.	1m	" " " "
5	" "	Yellow.	1m	" " " "
6	" "	Green.	1m	" " " "
7	" "	Blue.	1m	" " " "
8	" "	Violet.	1m	" " " "
9	" "	Grey.	0.75m	" " " "
10	" "	White.	1m	" " " "
11	" "	Pink.	1m	" " " "
12	WIR 002142	Single Screened Lead 7/0048 - Permanoid	1m	
13	WIR002051	Ident Sleeve 1 m.m. Red - Helvin P10	2	

ISSUE	1.M			
DATE	21.5.76.			
C.N. Nº				
CHECKED		TITLE TDSA 1A & 2A. CABLEFORM 12.	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8063-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	8050PL	Mother Board Assy.	1	
2	8061PL	Cableform - X. Amp.	1	
3	8062PL	Cableform - Y. Amp.	1	
4	8065PL	Cableform - Tube Base.	1	
5	5627MD-9	Spacer.	2	
6	CON001247	Socket R43/81/044 - Cinch.	1	SKT12.
7	CON001246	Base Assembly R43/81/961 - Cinch.	1	Use with Item 6.
8	CON001927	Conn. Guides P5000027 - Cinch.	7	
9				
10	FIX001182	Screw M2.5 x 20 Ch.Hd.Sl.Cd.Pl.	9	
11	FIX001132	Washer M2.5 Plain Cd.Pl.	9	
12				
13	FIX001303	Nut M2.5 Cd.Pl.	9	
14	FIX001215	Washer M2.5 Fibre.	9	
15				
16	Not Numbered	Wire 7/.0076 PTFE Cov'd. Red.	.5m	
17	ACC001543	Tube Base B12F - Mullard.	1	
18	DIO001955 DIO001956	Diode IN 914 - Mullard.) Alt. Diode IN 914 - Motorola.)	1	D1.
19	DIO002067	Diode BAX16 - Mullard.	1	D2.
20	CON001493	Conn. Snaplox LSB2/156 - Oxley.	4	
21				
22				
23	CON000121	Mini.Conn. 8129-015-605-003 - Varelco.	2	
24	CON000156	Mini.Conn. 8129-06-605-003 - Varelco.	2	
25	WIR001458	Sleeve H12 x 20 - Hellermann.	45	
26	WIR001459	Sleeve H15 x 20 - Hellermann.	14	
27	WIR001460	Sleeve H20 x 20 - Hellermann.	1	

ISSUE	1.M			
DATE	21.5.2.			
C.N. Nº				
CHECKED		TITLE TYPE 1A MOTHER BOARD & CABLEFORM ASSYs.	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8065-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	Not Numbered	White.	8.5m	7/0.2 Wire.
2	" "	Coloured Dye (Colour Research).	A/R	
3	WIR001510	Lacing Cord 1.0 m.m.	A/R	

ISSUE	1.m			
DATE	21.5.76.			
C.N. Nº				
CHECKED		TITLE TDSA 1A & 2A CABLEFORM - TUBE BASE	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº 222000-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	7292MD-5	Case	1	
2	8047PL	General Assy.	1	
3	CON0019 8	3 Pole Socket L1949 - Belling Lee.	1	
4	FIX001067	Screw M4 x 8 C'Sk.Hd.Sl.Cd.Pl.	2	
5	8068MD-	Cover - Top	1	
6	8069MD-7	Cover - Bottom	1	
7	7649PL-8	Handle Mounting Block Assy. (RH).	1	
8	7648PL-8	Handle Mounting Block Assy. (LH).	1	
9	7644MD-	Handle	1	
10	7661MD-	Cover Handle Hinge (LH)	1	
11	7662MD-	Cover Handle Hinge (RH)	1	
12	222101	Accessories Kit	1	
13	MIS 002705	Mains Lead Coding Label	A/R	
14	MOU002060	Grille Plastic No.300- Eng. Ent.	4	
15	FIX001133	Washer M3 Plain Cd. Pl.	4	
16				
17	MIS00142	Tesamoll 720 5/32" x 3/4"	4	Use Thixofix and use with Item 5 & 6.
18	MOU0014	Foot Plastic 438 - Eng. Ent.	4	
19	FIX0011	Screw M4 x 20 Ch.Hd.Sl.Cd.Pl.	4	
20	FIX0011	Screw M3 x 6 Pan Hd.Pozidriv. Blk. Chrome.	4	
21				
22	FIX00108	Screw M2.5 x 6 Pan.Hd.Sl. Chrome.	16	
23	MIS001908	Polythene Bag 24" x 48" with B.O.T. label.	1	
24	FIX001207	Washer M2.5 Shakeproof Blk. Steel.	16	
25				
26	FIX001213	Washer M4 Single Coil Spr.Blk.	4	
27	FIX001303	Nut M2.5 Cd.Pl.	16	
28	Not Num. d	Handbook	1	Included in Item 29.
29	222405-4	Packing Container 13¼" x 11¼" x 24¼"	1	
30	4029MD-9	Manufacturing Label	1	Fitted to underside of bottom cover.
31	FIX 1 35	Rokut Rivet 201-080551-00 - I.T.W.	4	Use with Item 30.

ISSUE	1.	2.	3
DATE	18.5.76.	1.2.77.	8.3.78
T.N. Nº	3169	3594	

CHECKED		TITLE	SHEET 1 OF SHEETS1	PRINT ISSUED / DATE
DATE		T.D.S.A. TYPE 1A FINAL ASSY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº 222100-A2-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	222400-1	Mains Transformer.	1	
2	222401-4	Brkt. Transformer Mtg.	1	
3	222102-4	Plate & Spacer Assy.	1	
4	ICE002080 ICE002081 ICE002082	Volt. Regulator uA 7815 KC Fairchild) Alt. Volt. Regulator LM 7815 KC - National.) Alt. Volt. Regulator MC 7815 CK - Motorola.)	2	IC. 1 & 3.
5	ICE002083 ICE002084 ICE002085	Volt. Regulator uA 7915 KC Fairchild) Alt. Volt. Regulator LM 7915 KC - National.) Alt. Volt. Regulator MC 7915 CK - Motorola.)	1	IC.2.
6	ACC 00[illegible]	Insulating Bush A22-2001 - Jermyn.	6	
7	ACC001440	Trans. Insul. A26-3023/005 TO3 - Jermyn.	3	
8	FIX001183	Screw M3 x 10 Ch. Hd. Sl. Cd. Pl.	6	
9	FIX001304	Nut M3 Cd. Pl.	6	
10	FIX001306	Washer M3 Shakeproof Stl. Blk.	6	
11	FIX001838	Solder Tag M3.	6	
12	WIR001458	Sleeve H12 x 20 Hellermann.	6	3 lengths cut in half.
13	CAP000863	Cap. 0.33uF 160v 20% Wima T.F.M.	6	
14	DIO001850	Diode BYX 36-150 - Mullard.	3	
15	DIO000621	Diode BYX 36-600 - Mullard.	10	
16	WIR 000692	Links 22 swg. BTC Wire.	A/R	
17	FIX001151	Screw M4 x 8 Ch. Hd. Sl. Cd. Pl.	4	
18	FIX001305	Nut M4 Cd. Pl.	4	
19	FIX001307	Washer M4 Shakeproof Steel Blk.	4	
20	FIX001380	'Spire' Captive Nut No. 6 SNU 2811-17-00.	4	
21	FIX002099	'Spire' Screw No. 6 x 5/8".	4	
22	FIX001136	Washer M4 Lg. Dia. Plain Cd. Pl.	4	
23	WIR 002144	Sleeving 1 m.m. P.T.F.E. Blk.	A/R	Use with Item 16.
24	CAP 000996	Cap. 2.2uF 63v. Wima Printilyt.	3	C13,14,15.
25	CAP 000819	Cap. 100uF 25v. Erie 20101.	1	C16.
26	RES 000319	Res. 100 ohms 5% ½w - Erie 122.	1	R6.
27	RES 000342	Res. 680 ohms 5% ½w - Erie 122.	1	R5.

ISSUE	1.	3.
DATE	18.5.76.	7.3.77. 4.4.77.
C.N. Nº		3192. 3230.

CHECKED		TITLE	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE		TRANSFORMER BRKT. ASSY.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº 222102 A4 PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	222402-4	Spacer	4	
2	222403-4	Plate-Compt. Mtg.		

ISSUE	1			
DATE	27.5.76			
C.N. Nº				
CHECKED		TITLE PLATE & SPACER ASSY.	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 5493-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	5417MD-7	Rear View of Front Panel.	Ref.	
2	5713MD-6	Circuit Diag. of F. Panel Comps.	Ref.	
3				
4				
5	4642MD-0	Front Panel.	1	
6	5233MD-7	Lever Switch 2 Pole 4 Pos.	3	SW2,5,8.
7	4408MD-7	Lever Switch 1 Pole 3 Pos.	1	SW7.
8	IND000021	Solid State Lamp 5082-4850 - H. Packard.	2	LP2,3.
9	ACC000010	Plastic Clip 5082-4707 - H.Packard.	2	
10				
11	POT001925 POT002064	Pot. 250 ohms - Spectrol Reliance MW) Alt. Pot. 250 ohms - Colvern CLR1106)	1	RV6.
12				
13				
14	POT 002385	Pot. 10K. Plessey Type L. .	2	RV4,5.
15				
16	POT000558	Pot. 1M - Bourns 3852C-161-105A.	3	RV1,2,3.
17				
18	FIX001140	Screw M2.5 x 6 Ch.Hd.Sl.Cd.Pl.	8	
19	FIX001207	Washer M2.5 Shakeproof Blk. Steel.	8	
20	FIX001303	Nut M2.5 Cd.Pl.	8	
21				
22				
23				
24				
25	FIX001173	M3 Banc-Loc.Insert MV3B-M3 - P.S.M.	4	

ISSUE	1	2.
DATE	27.5.76.	12.7.77.
C.N. Nº	3349.	

CHECKED		TITLE	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE		TYPE II FRONT PANEL ASSY. STAGE I.		

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 5496-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	5223MD-8	Potentiometer Bracket.	1	
2				
3				
4	POT000567	Pot. 1K - Bourns 3852A-202-102A.	1	
5	POT000557	Pot. 25K - Bourns 3852A-202-253A.	1	

ISSUE	1.w.			
DATE	27.5.76.			
C.N. Nº				
CHECKED		TITLE TYPE II POT. BRACKET SUB-ASSY.	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7418-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1				
2	7350PL	Switch Sub-Assy.	1	
3	5496PL	Pot. Bracket Sub-Assy.	1	
4	7937PL	E.H.T. Box Assy.	1	
5	7606PL	Cableform 8 Assy.	1	
6	7936MD-8	E.H.T. Cover Mtg. Tray.	1	
7	7374MD-1	Rear Panel.	1	
8	7302MD-9	Power Input Decorative.	1	
9	7420MD-8	Rear Panel Decorative.	1	
10	5216PL	Tagboard Assy.	1	
11				
12	7294MD-9	Foot.	4	
13	8110MD-9	Pillar.	1	
14	HOL001241	Fuseholder L2006 - Belling Lee.	1	
15	FUS 002413	Fuse 315mA S 502 - Beswick.	1	
16	CON001619	Filtered Appliance Inlet L2133A/L Belling Lee.	1	SKT9.
17	CON 002778	Voltage Selector MP44 - McMurdo	1	
18	CON 000920	Faston Receptacle 42599-2 AMP	3	
19	8111MD-9	Locking Plate.	1	
20	MOU 001422	Insulating Boot for Conn.41729AMP	3	
21				
22				
23	TRA001557 TRA001556 TRA001558 TRA001559 TRA001560 TRA001561 TRA000223	Transistor 2N 3055 - Mullard.) Alt. Transistor 2N 3055 - Silicon.) Alt. Transistor 2N 3055 - Motorola.) Alt. Transistor 2N 3055 - Ferranti.) Alt. Transistor 2N 3055 - S.G.S.) Alt. Transistor 2N 3055 - Fairchild.) Alt. Transistor 2N 3055 - R.C.A.)	1	TR1,
24	DIO002065	Diode BYX42-300 - Mullard.	2	
25	ACC001388	Insulating Kit 56295 - Mullard.	1	
26	ACC000255	Insulating Bush A1230 - Jermyn.	2	
27	ACC 001405	Heat Transfer Washer A26-3024 - Jermyn.	2	
28	[illegible]001914	'O' Ring RTOS 7 - Trist.	4	

ISSUE	1.	2.	3	4	5
DATE	27.5.76.	1.9.77.	23.3.78	17.4.78	8 8.78.
C.N. Nº		3398.	3610	3579	3773

CHECKED		TITLE	TYPE 2A. REAR PANEL ASSEMBLY.	SHEET 1 OF SHEETS 2	PRINT ISSUED DATE
DATE					

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7418-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
29	FIX 001853	Solder Tag M5 RC238 - Ross Courtney.	2	
30	FIX001153	Screw M4 x 20 Ch.Hd.Sl.Cd.Pl.	4	
31	FIX001058	Screw M2.5 x 10 C'Sk.Hd.Sl.Cd.Pl.	4	
32	FIX001059	Screw M2.5 x 12 C'Sk.Hd.Sl.Cd.Pl.	6	
33	FIX001090	Screw M2.5 x 10 Pan.Hd.Sl. Chrome.	1	
34	FIX001092	Screw M2.5 x 12 Pan.Hd.Sl. Chrome.	2	
35	FIX001145	Screw M3 x 6 Ch.Hd.Sl.Cd.Pl.	2	
36				
37	FIX001209	Washer M2.5 Crinkle - Berym.Cu.	4	
38	FIX001207	Washer M2.5 Shakeproof Blk. Steel.	7	
39	FIX001210	Washer M3 Crinkle - Berym.Cu.	2	
40	FIX001307	Washer M4 Shakeproof Steel Blk.	4	
41	FIX001303	Nut M2.5 Cd.Pl.	10	
42	FIX001305	Nut M4 Cd.Pl.	4	
43	FIX001125	Screw M3 x 6 Nylon Ch.Hd.Sl.	4	
44	FIX001042	Screw M3 x 10 Pan.Hd.Cd.Pl.	2	
45	FIX001838	Solder Tag M3.	2	
46	FIX001304	Nut M3 Cd.Pl.	2	
47	FIX001170	M3 Pre.Hard.Insert - P.S.M.	12	
48				
49	FIX001088	Screw M2.5 x 5 Pan.Hd.Sl.Chrome.	1	
50				
51	WIR001458	Sleeve H12 x 20 - Hellermann.	2	
52	WIR001459	Sleeve H15 x 20 - Hellermann.	26	
53	WIR001460	Sleeve H20 x 20 - Hellermann.	13	
54	WIR001464	Sleeve H100 x 25 - Hellermann.	100	
55	7602PL-7	Cableform 2 Assy.	1	
56	CON 000111	Socket 74/10/2355/10 - Painton.	1	SKT.10.
57	CON 001247	Socket 9 way R43-81044-00-000 - Cinch.	1	SKT.11.

ISSUE	1.	2.	3	4	5
DATE	27.5.76.	15.6.77.	23.3.78	17.4.78.	8.8.78.
.N. Nº		3329.	3610	3579	3773

CHECKED		TITLE	SHEET 2 OF SHEETS 2	PRINT ISSUED DATE
ATE		TYPE 2A. REAR PANEL ASSEMBLY.		

REND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7421-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	7551MD-7	Rear View of Front Panel.	Ref.	
2	7549MD-6	Switch Circuit Diagram.	Ref.	
3				
4				
5				
6				
7	5646MD-9	Front Panel Links Wiring Schedule.	Ref.	
8				
9				
10				
11	5493PL	Front Panel Assy. Stage 1.	1	
12	7601PL	Cableform 1 Assy.	1	
13	7603PL	Cableform 3 Assy.	1	
14	5645PL	Front Panel Links.	1	
15				
16				
17				
18	5259MD-7	Wafer Switch 2 Pole 11 Pos.	1	SW9.
19	5528MD-7	Wafer Switch 3 Pole 4 Pos.	1	SW6.
20	4799MD-9	Modified Edge Connector.	1	SKT14.
21				
22	WIR000253	Sleeve 10 m.m. x 10 m.m. Clear Plastic.	1	Fitted over Terminal T4.
23	CON000114	Socket 4 m.m. 941-920 - Radiall.	4	T1-T4.
24	SWI 002799	Switch KTA 106D - Waycom.	3	SW3,4, & 11.
25	SWI 002800	Switch KTA 206N - Waycom.	2	SW1,10.
26	SWI 000689 SWI 001540	Switch Push Button R52101-Rendar Alt. T906 - Arcolectric	1	PB1.
27	ACC 002801	Lever Cap Black CP01 -Waycom	5	(For items 24 and 25)
28				
29				
30	IND001879	Neon 35R-1-F4-AC-R-2-N-6 - Plastronics.	1	With Spire Nut.
31				
32				

ISSUE	1.	2.	3.	4.	5	6
DATE	27.5.76	13.6.77.	12-7-77.	12-1-78.		
C.N. Nº		3299.	3353.	3174.	3690	3716

CHECKED		TITLE TYPE 2A. FRONT PANEL ASSY. STAGE 2.	SHEET 1 OF SHEETS 2	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7421-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
33				
34				
35				
36	WIR001434	Ins. Stand Off Terminal W8005 - Harwin.	4	
37	FIX001183	Screw M3 x 10 Ch.Hd.Sl.Cd.Pl.	2	
38	FIX001210	Washer M3 Crinkle - Berym.Cu.	2	
39	FIX001910	Screw 8BA x 3/16 C'Sk.Hd.Sl.Cd.Pl.	3	
40.	FIX 001853	Solder Tag M5 RC 238 - Ross Courtney.	1	Fit under body of SW1.
41				
42	RES000467	Res. 150 ohms 2% ¼w - Electrosil TR4.	2	R2 & R3.
43				
44				
45				
46		Wire 7/02 White Dye Yellow/Green.	.08m.	Used for earthing SW1.
47	WIR001459	Sleeve H15 x 20 - Hellermann.	46	
48	WIR001460	Sleeve H20 x 20 - Hellermann.	3	

ISSUE	1. 4. 5 6			
DATE	27.5.78. 12-1-78.			
C.N. Nº	3174. 3690 3716			
CHECKED		TITLE TYPE 2A. FRONT PANEL ASSY. STAGE 2.	SHEET 2 OF SHEETS 2	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 7606-PL.

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION.
1	Not Numbered	Brown.	0.2m	7/.0076 PVC Cov. Wire
2	" "	Red.	0.2m	" " " "
3	" "	Orange.	0.2m	" " " "
4	" "	Yellow.	0.2m	" " " "
5	" "	Green.	0.2m	" " " "
6	" "	Blue.	0.2m	" " " "
7	" "	Black.	0.2m	" " " "
8				
9	5598MD-9	Edge Connector.	2	PL6 & PL7.
10				
11	WIR001326	'Insulok' Cable Tie T18R.	2	

ISSUE	1.v			
DATE	27.5.76.			
C.N. Nº				
CHECKED		TITLE T.D.S.A. 2A. CABLEFORM 8.	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG. No. AKJ-8056-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY.	CIRCUIT LOCATION
1	8070MD-6	Circuit Diagram	Ref	(2Sheets)
2	8057MD-7	Drilling Details P.C.B. Iss12	1	
3				
4				
5	CON 000298	Edge Conn. EWD32/32/FS-Ferranti)	2	Skt1,2
	CON 002788	Alt T6P55600/AA/32/32-Ultra)		
6	CON 000300	Edge Conn. EWD/40/40/FS-Ferranti)	1	Skt3.
	CON 002790	Alt. T6P55600/40/40- Ultra)		
7	AKB 7953-9	Edge Connector	2	Skt6,7.
8				
9				
10				
11	MIS 000533	Vinyl Toluenated Alkyd V991- Stirling Varnish	A/R	
12				
13				
14	WIR 000312	Avlug 1/16" 1107-0208	28	
15	ICE 000274	I.C. 936DC - Fairchild)	2	IC2,3.
	ICE 001747	Alt. U6A 9936 51S - S.G.S.)		
	ICE 001748	Alt. MIC 936 5D - I.T.T.)		
16	ICE 000272	I.C. 962DC - Fairchild)	1	IC1.
	ICE 001743	Alt. U6A 9962 51S - S.G.S.)		
	ICE 001744	Alt. MIC 962 5D - I.T.T.)		
17	ICE 001941	I.C. uA 741 HC - Fairchild)	1	IC4
	ICE 001942	Alt. LM 741 CH - National)		
	ICE 001943	Alt. MC 1741 CG - Motorola)		
	ICE 001944	Alt. U5B 7741 39X - S.G.S.)		
18				
19				
20	RES 000375	Res. 22K 5% ½w Erie 122	1	R114
21	RES 000328	Res. 18ohms 5% ½w Erie 122	1	R21
22				
23	RES 000319	Res. 100ohms 5% ½w Erie 122	2	R7,8.
24				
25				
26	CAP 002870	Cap. .022uF 630v Erie M312	1	C21
27	RES 000369	Res 68K 5% ½w Erie 122	1	R70

ISSUE	Previous 12			
DATE	C/Notes 3569 3692 3756 30.8.78.			
C.N. No.	C202 3436 3673 3738 3771 3754			
CHECKED		TITLE	SHEET 1 OF SHEETS 4	PRINT ISSUED
DATE		TYPE 2A MOTHER BOARD ASSY		DATE

MY 99725 R

...E COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ-8056-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
28	RES000342	Res. 680 ohms 5% ½w - Erie 122.	1	R12.
29	RES000339	Res. 1K 5% ½w - Erie 122.	3	R13,14,29.
30	RES000388	Res. 1K5 5% ½w - Erie 122.	1	R94.
31	RES000387	Res. 1K8 5% ½w - Erie 122.	1	R17.
32	RES000385	Res. 2K2 5% ½w - Erie 122.	3	R16,22,74..
33				
34				
35	RES000381	Res 3K9 5% ½w - Erie 122.	1	R11.
36	RES000380	Res. 4K7 5% ½w - Erie 122.	9	R26,2,3,15,18,20,92,93 R30.
37	DIO002032	Zener Diode BZY88C3V3 - Mullard.	1	D14.
38	RES000363	Res. 180K 5% ½w - Erie 122.	1	R67
39	RES000352	Res. 6K8 5% ½w - Erie 122.	3	R23,1,6.
40	RES000351	Res. 8K2 5% ½w - Erie 122.	1	R27.
41	RES000349	Res. 10K 5% ½w - Erie 122.	2	R19,25.
42	RES000332	Res. 2M2 5% ½w - Erie 122.	1	R113.
43	RES000377	Res. 15K 5% ½w - Erie 122.	3	R4,5,28.
44				
45				
46	RES000371	Res. 47K 5% ½w - Erie 122.	3	R68,69,115.
47				
48	RES000366	Res. 100K 5% ½w - Erie 122.	1	R24.
49				
50				
51				
52	CAP 002512	Cap, 47uF 40v. 01617479-Mullard	3	C2,3,4.
53				
54	CAP000879	Cap. 100uF 16v. - Wima Printilyt.	1	C8.
55	CAP000960	Cap. 220pF Tubular - Erie AD.	1	C9.
56				
57				
58				
59	CAP 000852	Cap. 0.01uF 630v. - 113-673 R.S.	1	C13.

ISSUE	Previous C/Notes 11 12			
DATE	3692 3771 29.8.78. 30.8.78.			
C.R. Nº	3436 3738 3756 3754			
CHECKED	TITLE TYPE 2A. MOTHER BOARD ASSY.		SHEET 2 OF SHEETS 4	PRINT ISSUED DATE
DATE				

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ-8056-PL.	

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
60	Not Numbered	A.O.T.	2	C1.
61	CAP001009	Cap. 0.22uF 250v. - Mullard C281v.v	1	C17.
62	DIO000235 DIO001810 DIO001811	Diode IN 4148 - Mullard.) Alt. Diode IN 4148 - Fairchild.) Alt. Diode IN 4148 - I.T.T.)	1	D1.
63	ACC002609	Transistor Pad TO518-002 - Jermyn	15	Do not fit to TR26.
64	DIO001899	Zener Diode BZY88-C10 - Mullard.	1	D2.
65				
66	TRA000229 TRA001551 TRA001552 TRA001553 TRA001554 TRA001555	Transistor BC 107 - Mullard.) Alt. Transistor BC 107 - Texas.) Alt. Transistor BC 107 - S.G.S.) Alt. Transistor BC 107 - Motorola.) Alt. Transistor BC 107 - National.) Alt. Transistor BC 107 - I.T.T.)	4	TR10,12,13,42.
67	ACC001375	Transistor Pad 10277 - Milton Ross.	4	For IC4,IC5, TR14 & 17.
68	ACC 002608	Transistor Pad TO5-001-Jermyn	4	For TR4,5,16,22.
69	TRA000227	Transistor BSX 19 - Mullard.	2	TR11,26.
70	TRA000654 TRA001573 TRA001574 TRA001575 TRA001576	Transistor BFY 51 - Mullard.) Alt. Transistor BFY 51 - National.) Alt. Transistor BFY 51 - S.G.S.) Alt. Transistor BFY 51 - Motorola.) Alt. Transistor BFY 51 - I.T.T.)	1	TR16.
71				
72	TRA000224 TRA000655	Transistor 2N 2910 - Gen.Electric.) Alt. Transistor BFY 82 - S.G.S.)	2	TR14,17.
73				
74	TRA000228 TRA001564 TRA001565	Transistor BCY 70 - Mullard.) Alt. Transistor BCY 70 - Texas.) Alt. Transistor BCY 70 - National.)	1	TR9.
75	POT 001491	Pot. 10K - Daystrom 567-00HS.	1	RV4))RV1)
76	POT000560	Pot. 1K - Daystrom 567-00HS.	2	)RV2))
77	POT000556	Pot. 500K - Daystrom 567-00HS.	1	RV3) To be mounted on) rear of board.
78				)
79	POT000550	Pot. 5K - Daystrom 567-00HS.	1	RV9)
80				

ISSUE	Previous C/Notes				12		
DATE	3202	3549	3692	3771	30.8.78.		
C.N. Nº	3436	3673	3738		3754		
CHECKED		TITLE	TYPE 2A. MOTHER BOARD ASSY.			SHEET 3 OF SHEETS 4	PRINT ISSUED DATE
DATE							

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG. No. AKJ-8056-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY.	CIRCUIT LOCATION
81				
82				
83				
84	ACC 001907	Heatsink 5F-2-Redpoint	3	For TR4,5,22.
85	WIR 002157	Clear PVC Sleeving M60 x 0.5	17mm	Use with C2.
86	RES 000372	Res. 39K 5% ½w Erie 122	1	R66
87	POT 000559	Pot. 2K-567-00HS. - Daystrom	1	RV6. Mounted on rear of board
88				
89	RES 000423	Res. 4K7 2% ½w - Electrosil TR5	1	R96
90	RES 000417	Res. 10K 2% ½w - Electrosil TR5	1	R95
91				
92				
93	RES 000382	Res. 3K3 5% ½w - Erie 122	1	R75.
94				
95	WIR 000692	22swg. BTC Wire	A/R	LK1,2,3.
96				
97				
98				
99				
100				

ISSUE	previous	12		
DATE	C/Notes	3569 3692 3756 30.8.78.		
C.N. No.	3202 3486	3673 3738 3771 3754		
CHECKED		TITLE	SHEET 4 OF SHEETS 4	PRINT ISSUED
DATE		TYPE 2A MOTHER BOARD ASSY		DATE

MY 99725 R

TREND COMMUNICATIONS LTD.	PARTS LIST	DRG Nº AKJ 8064-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	8056PL	Mother Board Assy.	1	
2	8061PL	Cableform - X. Amp.	1	
3	8062PL	Cableform - Y. Amp.	1	
4	8065PL	Cableform - Tube Base.	1	
5	5627MD-9	Spacer.	2	
6	CON001247	Socket R43/81/044 - Cinch.	1	SKT12.
7	CON001246	Base Assembly R43/81/961 - Cinch.	1	Used with Item 6.
8	CON001927	Conn. Guides P5000027 - Cinch.	4	
9				
10	FIX001182	Screw M2.5 x 20 Ch.Hd.Sl.Cd.Pl.	6	
11	FIX001132	Washer M2.5 Plain Cd.Pl.	6	
12				
13	FIX001303	Nut M2.5 Cd.Pl.	6	
14	FIX001215	Washer M2.5 Fibre.	6	
15				
16	ACC001543	Tube Base B12F - Mullard.	1	
17	DIO001955 DIO001956	Diode IN 914 - Mullard.) Alt. Diode IN 914 - Motorola.)	1	D1.
18	DIO002067	Diode BAX 16 - Mullard.	1	D2.
19	CON001493	Conn. Snaplox LSB2/156 - Oxley.	4	
20				
21				
22	CON000121	Mini. Conn 8129-015-605-003 - Varelco.	2	
23	CON000156	Mini. Conn. 8129-06-605-003 - Varelco.	2	
24				
25	WIR001458	Sleeve H12 x 20 - Hellermann.	45	
26	WIR001459	Sleeve H15 x 20 - Hellermann.	14	
27	WIR001460	Sleeve H20 x 20 - Hellermann.	1	

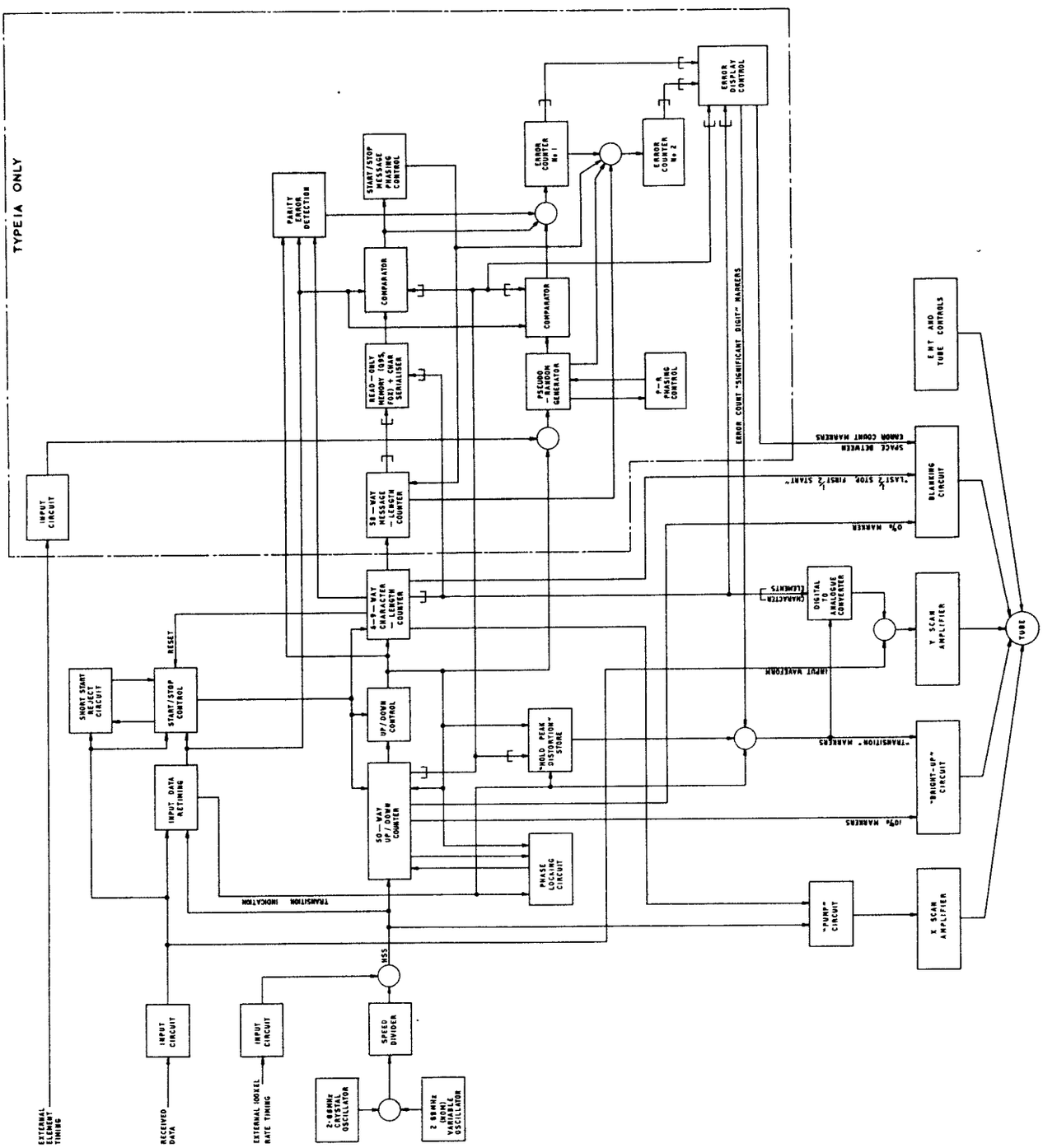
ISSUE	1.
DATE	27.5.75.
C.N. Nº	

CHECKED		TITLE	TYPE 2A. MOTHER BOARD AND CABLEFORM ASSYS	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE					

DRG Nº 232000-PL

ITEM	COMPUTER CODE	DESCRIPTION	QTY	CIRCUIT LOCATION
1	[illegible]MD-6	Case.	1	
2	[illegible]PL	General Assy.	1	
3	CON001968	3 Pole Socket L1949 - Belling Lee.	1	
4	FIX001067	Screw M4 x 8 C'Sk.Hd.Sl.Cd.Pl.	2	
5	8068MD-7	Cover - Top.	1	
6	8069MD-7	Cover - Bottom.	1	
7	7649PL-8	Handle Mounting Block Assy. (RH).	1	
8	7648PL-8	Handle Mounting Block Assy. (LH).	1	
9	7644MD-8	Handle.	1	
10	7661MD-8	Cover Handle Hinge (LH).	1	
11	7662MD-8	Cover Handle Hinge (RH).	1	
12	222101	Accessories Kit.	1	
13	MIS 002705	Mains Lead Coding Label	A/R	
14	MOU002063	Grille Plastic No. 300 - Eng. Ent.	4	
15	FIX001133	Washer M3 Plain Cd.Pl.	4	
16				
17	MIS001427	Tesamoll 720 5/32" x 3/4".	4 strips	Use Thixofix and use with Items 5 & 6.
18	MOU001489	Foot Plastic 438 - Eng. Ent.	4	
19	FIX001153	Screw M4 x 20 Ch.Hd.Sl.Cd.Pl.	4	
20	FIX001108	Screw M3 x 6 Pan.Hd.Pozidriv. Blk. Chrome.	4	
21	FIX001304	Nut M3 Cd. Pl.	4	
22	FIX001089	Screw M2.5 x 6 Pan.Hd.Sl.Chrome.	16	
23	MIS001908	Polythene Bag 24" x 48" with B.O.T. Label.	1	
24	FIX001207	Washer M2.5 Shakeproof Blk. Steel.	16	
25	222405-4	Packing Container 13¼" x 11¼" x 24¼".	1	
26	FIX001213	Washer M4 Single Coil Spr. Blk.	4	
27	FIX001303	Nut M2.5 Cd.Pl.	16	
28	Not Numbered	Handbook.	1	Included in Item 29.
29	0001MD-9	Packing Instruction.	1	
30	4029MD-9	Manufacturing Label.	1	Fitted to underside of bottom cover.
31	F[illegible]385	Rokut Rivet 201-080551-00 - I.T.W.	4	Use with Item 30.

ISSUE	1.	2.	3	
DATE	26.5.76.	1.2.77.	8.3.78	
C.N. Nº		3169	3594	
CHECKED		TITLE T.D.S.A. TYPE IIA. FINAL ASSY.	SHEET 1 OF SHEETS 1	PRINT ISSUED DATE
DATE				



AHB 5537/1

BLOCK SCHEMATIC DIAGRAM

FIG.1.

TERMINAL		INTERCONNECTIONS									
		LOGIC BOARD 1		LOGIC BOARD 2		LOGIC BOARD 3		X AMPLIFIER		Y AMPLIFIER	
1—40	A—AV	1—32	A—AL	1—32	A—AL	1—40	A—AV	15—(1-15)	15—(1-6)	13—(1-6)	14—(1-15)
1	A	W95	W(93)	+5v				FIG 7A	W43	2(T)	FIG 7A
2	B		W(26)	Ov				2(AB). 3(AK). FIG 7A	FIG 3B	2(N). 3(AF).	W(33). 1(19).
3	C		W(91)		+15v			Ov	W(44). Y14(10). FIG 7A	2(S)	W(66)
4	D		W(89)		-15v		6(4)	2(28). 3(T).	W(49). Y14(8). FIG 7A.	2(R)	2(W)
5	E		W(87)	1(27)	1(AA). 3(27).		6(5)	+5v	W(45)	+5v	-15v
6	F	W97	W(85)	1(26).	3(34)		W(76)	W(48). TB(4)	W(51)	Ov	+15v
7	H	W99	W(84)	1(25)	3(14). FIG 7A	2(25)		2(P)			TB(5). FIG 7A
8	J	3(AV)	W(83)	1(AJ). 3(11)	3(AN)	2(24)					X16(4). 12(2). FIG 7A
9	K	2(X). 3(17)	W(82)	1(AH)	W(75). 3(15)	2(23)		W(31)			W(25)
10	L	2(27). 3(AU)	W(81)	W(77). 1(N)	W(73). 3(31). Y14(14)	2(22)		W(29)			W(44). X15(3). FIG 7A
11	M	W(86)	W(79)	1(AC). 3(16). FIG 7A	W(52). Y14(13)	1(AJ). 2(8)		2(U)			W(12). 1(23). 2(16). 3(32)
12	N	W(88)	W(77). 2(10)	1(AE). 3(29).	3(AA). Y13(2)	W(78). 1(23). 2(16). Y14(6)					W(46)
13	P	W(90)		3(28)	X15(7)	1(R)		+15v			W(32). 2(M).
14	R	W(92)	3(13)	1(24)	Y13(4)	2(H). FIG 7A	W(67)	-15v			W(75). 2(*). 3(31)
15	S	W(94)	3(19)	1(AD). 3(30)	Y13(3)	W(75). 2(K).	W(65)	FIG 7A			W(42)
16	T	W(96)	3(20)	W(78). 1(25). 3(12). Y14(11)	Y13(1)	1(AE). 2(11). FIG 7A.	2(28). Y13(4).				
17	U	W(98)	3(21)	2(V). FIG 7A	X15(11)	1(9). 2(22).	2(30)				
18	V	W(100)	3(22)		2(17). FIG 7A	W(71). 2(Y).	2(31)				
19	W	W(33). Y15(2).	3(23)	Y14(1)	Y14(4)	1(S)	W(67)				
20	X	7(16)	3(24)	Ov	1(9). 3(17).	1(T)	FIG 7A				
21	Y	7(15)	3(25)	W(80)	W(71). 3(18).	1(U)	FIG 7A				
22	Z		3(26)	3(10)	3(AM)	1(V)	FIG 7A				
23	AA	W(78). 2(16). 3(12). Y14(11)	2(E). 3(27)	3(9)	3(AL)	1(W)	FIG 7A				
24	AB	2(14)		3(8)	3(AK). X15(2) FIG 7A	1(X)	FIG 7A				
25	AC	2(7)	2(21). 2(12)	3(7)	3(AJ)	1(Y)	FIG 7A				
26	AD	2(6)	2(15). 3(30)		3(AH) FIG 7A	1(Z)	FIG 7A				
27	AE	2(5)	2(11). 3(16). FIG 7A	1(10). 3(AU).	3(AF)	1(AA). 2(E)	2(AF)				
28	AF	-15v	3(32)	3(T). X15(4).	3(AE)	2(13)	2(AE)				
29	AH		2(9)	W(64)	W(72). FIG 7A	1(AC). 2(12)	2(AD)				
30	AJ	+15v	2(8). 3(11).	3(U)	W(68) FIG 7A	1(AD). 2(15)	2(AC)				
31	AK	+5v		3(V)	W(70). FIG 7A	W(73). 2(L). Y14(14).	2(AB). X15(2)				
32	AL		Ov	W(66). Y14(3) FIG 7A		1(AF)	2(AA)				
33	AM						2(Z)				
34	AN					2(F)	2(J)				
35	AP					+5v					
36	AR					Ov					
37	AS						3(B)				
38	AT						W(53)				
39	AU						1(10). 2(27).				
40	AV						1(8)				

TERM	SK6	SK7	SK12
1			Ov
2		W(23)	X16(4). Y14(8). FIG 7A
3		FIG 3B	
4	3(D)		
5	3(E)		W(56)
6	FIG 7A		TB(2). FIG 7A
7	FIG 7A		W(52)
8	FIG 7A		W(60)
9	FIG 7A		TB(3)
10	FIG 7A		
11	FIG 7A	Ov	
12	FIG 7A		
13	FIG 7A		
14	FIG 7A		
15	FIG 7A	1(21)	
16	FIG 7A	1(20)	

NOTE:-

PREFIX 'W' INDICATES 100-WAY EDGE CONNECTO
" TB - CONNECTIONS TO TUBE BA
" X OR Y - AMPLIFIER BOARD CONNECTIONS
" 1, 2 OR 3 " LOGIC BOARD CONNECTIONS
" 6, 7 OR 12 " CONNECTION TO SKTS 6, 7 OR 12
FIG 3B INDICATES CONNECTION BY FLYING LEAD TO MOTHER BOARD CIRCUITRY.

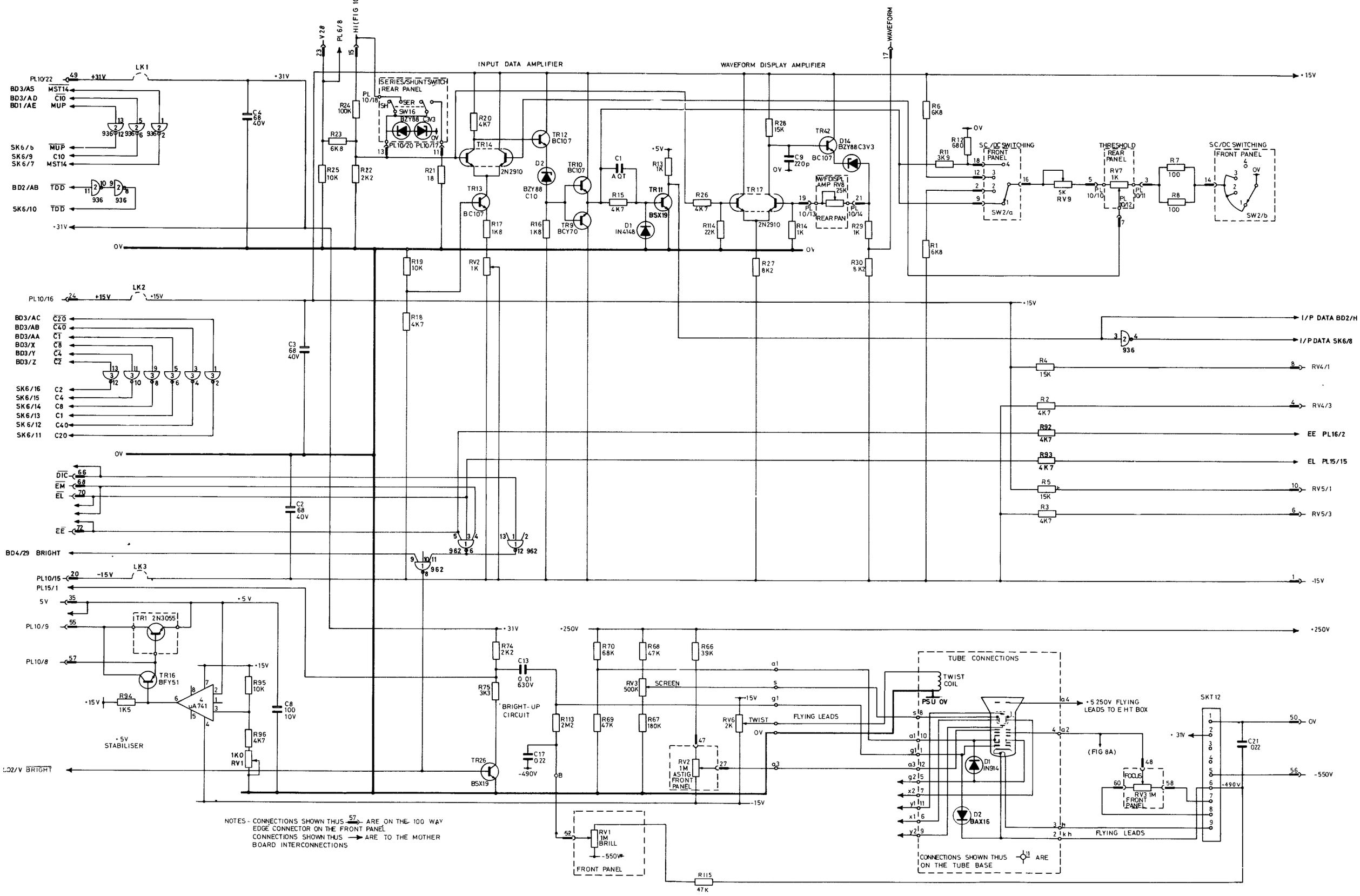
233901

MOTHERBOARD - INTERCONNECTIONS

FIG. 2A

PIN No.	FUNCTION	DISTRIBUTION
1	- 15V	LB1(28), LB2(D), LB4(40), Y.AMP 14(5), X.AMP 15(14), 100W(20), FIG.2B.
2		FIG.2B.
3		FIG.2B.
4		FIG.2B.
5		FIG.2B.
6		FIG.2B.
7		FIG.2B.
8		FIG.2B.
9		FIG.2B.
10		FIG.2B.
11		FIG.2B.
12		FIG.2B.
13		FIG.2B.
14		FIG.2B.
15		FIG.2B.
16		FIG.2B.
17		FIG.2B.
18		FIG.2B.
19		FIG.2B.
20	- 15V	100W(1), LB1(28), LB2(D), LB4(40), Y.AMP 14(5), X.AMP 15(14), FIG.2B.
21		FIG.2B.
22		
23	V28	FIG.2B, SKT7(2).
24	+ 15V	FIG.2B, LB1(30), LB2(C), LB4(39), Y.AMP 14(6), X.AMP 15(13).
25	RV 4/2	Y.AMP 14(9).
26	$\overline{2400}$	LB1(B), LB5(AD).
27	a3	PIN 12 TUBE BASE.
28	SPPS	LB4(19).
29		X.AMP 15(10).
30	$\overline{PHASE}$	LB4(15), LB4(S), LB5(15), LB5(S), LB5(L), SKT7(6).
31		X.AMP 15(9).
32	$\overline{DE}$	LB2(M), LB5(K), Y.AMP 14(13).
33	$\overline{EXT}$	LB1(19), LB5(AE), Y.AMP 14(2).
34	$\overline{EPS}$	LB4(J), LB5(8), LB5(J).
35	+ 5V	FIG.2B, LB1(31), LB2(1), LB3(35), LB4(35), LB5(AP), Y.AMP 13(5), X.AMP 15(5).
36	$\overline{PM}$	LB5(H).
37	$\overline{PRE}$	LB5(E).
38	$\overline{NM}$	LB5(F).
39	$\overline{PLB}$	LB5(D).
40	$\overline{QBF5}$	LB5(C).
41	$\overline{QBFS}$	LB4(S), LB5(2).
42		Y.AMP 14(15).
43	SW5/b/2-4	X.AMP 16(1).
44	+ 250V	FIG.2B, Y.AMP 14(10), X.AMP 16(3).
45	SW5/b/w	X.AMP 16(5).
46	Y-IN	Y.AMP 14(12).
47		FIG.2B.
48	a2	X.AMP 15(6), PIN 4 TUBE BASE.
49	+ 31V	FIG.2B, Y.AMP 14(8), X.AMP 16(4).
50	0V	LB1(AL), LB2(2), LB3(36), LB4(36), LB5(AR), Y.AMP 13(6), X.AMP 15(3), SKT7(11), LB4(AV), LB2(20), FIG.2B, SKT12(1).

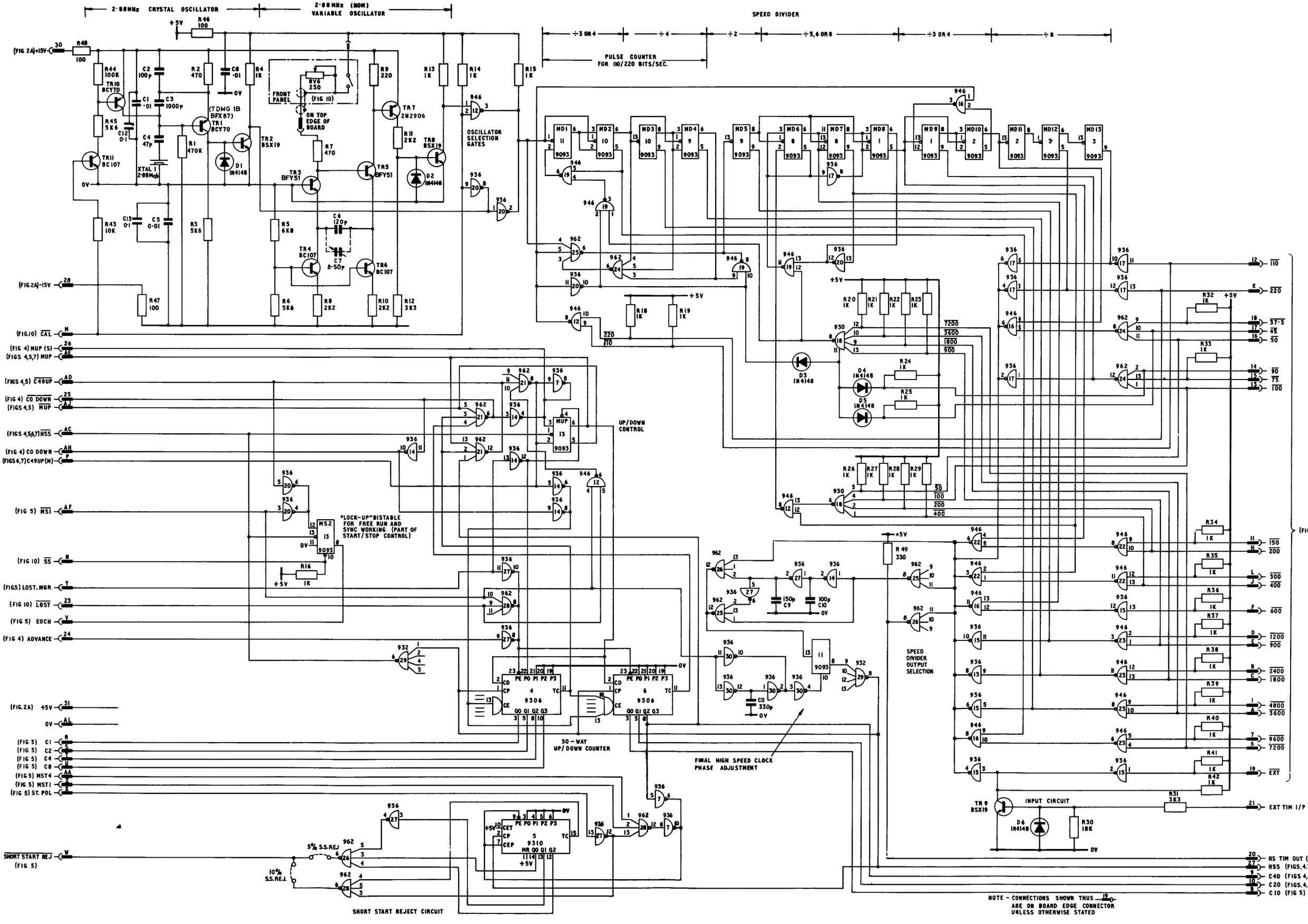
PIN No.	FUNCTION	DISTRIBUTION
51	RV5/2	X.AMP 16(6).
52	RV1/W	FIG.2B.
53	$\overline{DRS}$	LB3(AT).
54		
55		FIG.2B.
56	- 550V	SKT12(5).
57		FIG.2B.
58		SKT12(7).
59	$\overline{ECO}$	LB5(B).
60		SKT12(8).
61	$\overline{POD}$	LB4(4).
62		
63	IN PHASE	LB4(5).
64	$\overline{SYWK}$	LB2(29).
65	$\overline{7BCH}$	LB3(5).
66	$\overline{DIC}$	FIG.2B, LB2(32), Y.AMP 14(3).
67	$\overline{PST}$	LB3(W).
68	$\overline{EM}$	FIG.2B, LB2(AJ).
69	$\overline{6BCH}$	LB3(R).
70	$\overline{EL}$	FIG.2B, LB2(AK).
71	$\overline{HOLPK}$	LB3(18), LB2(Y).
72	$\overline{EE}$	FIG.2B, LB2(AH).
73	$\overline{5BCH}$	LB2(L), LB3(31), Y.AMP 14(14).
74	$\overline{PEV}$	LB4(3).
75	$\overline{ELCOMB}$	LB2(K), LB3(15).
76	$\overline{ELSEP}$	LB3(F).
77	$\overline{SS}$	LB1(N), LB2(10).
78	$\overline{LOST}$	LB1(23), LB2(16), LB3(12), Y.AMP 14(11).
79	$\overline{CAL}$	LB1(M).
80	IN SYNC LP	LB2(21).
81	$\overline{300}$	LB1(L).
82	$\overline{220}$	LB1(K).
83	$\overline{400}$	LB1(J).
84	$\overline{200}$	LB1(H).
85	$\overline{600}$	LB1(F).
86	$\overline{150}$	LB1(11).
87	$\overline{900}$	LB1(E).
88	$\overline{110}$	LB1(12).
89	$\overline{200}$	LB1(D).
90	$\overline{100}$	LB1(13).
91	$\overline{800}$	LB1(C).
92	$\overline{90}$	LB1(14).
93	$\overline{3600}$	LB1(A).
94	$\overline{75}$	LB1(15).
95	$\overline{4800}$	LB1(1).
96	$\overline{50}$	LB1(16).
97	$\overline{7200}$	LB1(6).
98	$\overline{45}$	LB1(17).
99	$\overline{9600}$	LB1(7).
100	$\overline{37.5}$	LB1(18).



AKJ 8070 - D.

MOTHER BOARD - POWER SUPPLY. - CIRCUIT DGM.

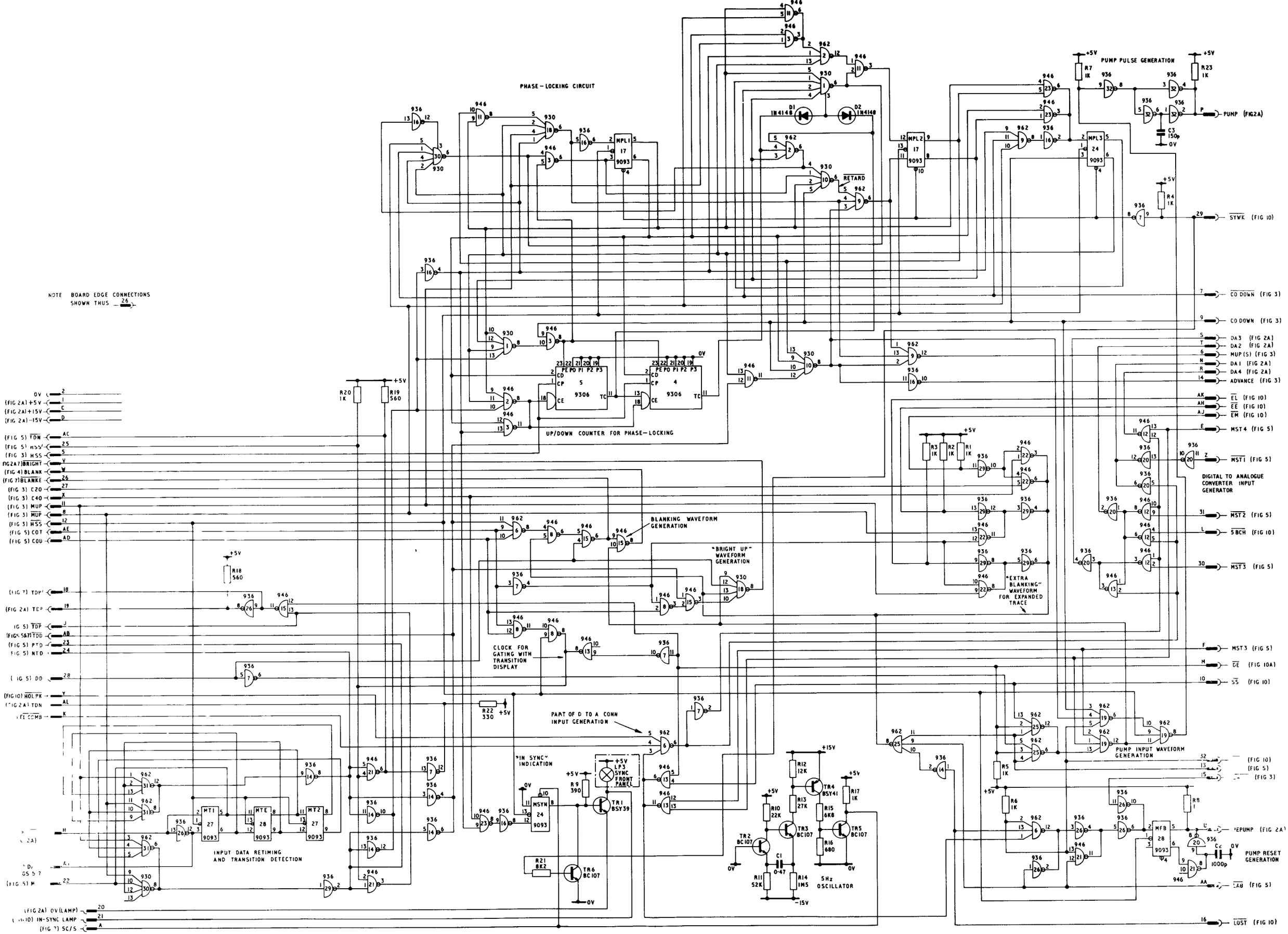
FIG. 2B.



AKJ 7290 - D

LOGIC BOARD 1 - CIRCUIT DIAGRAM.

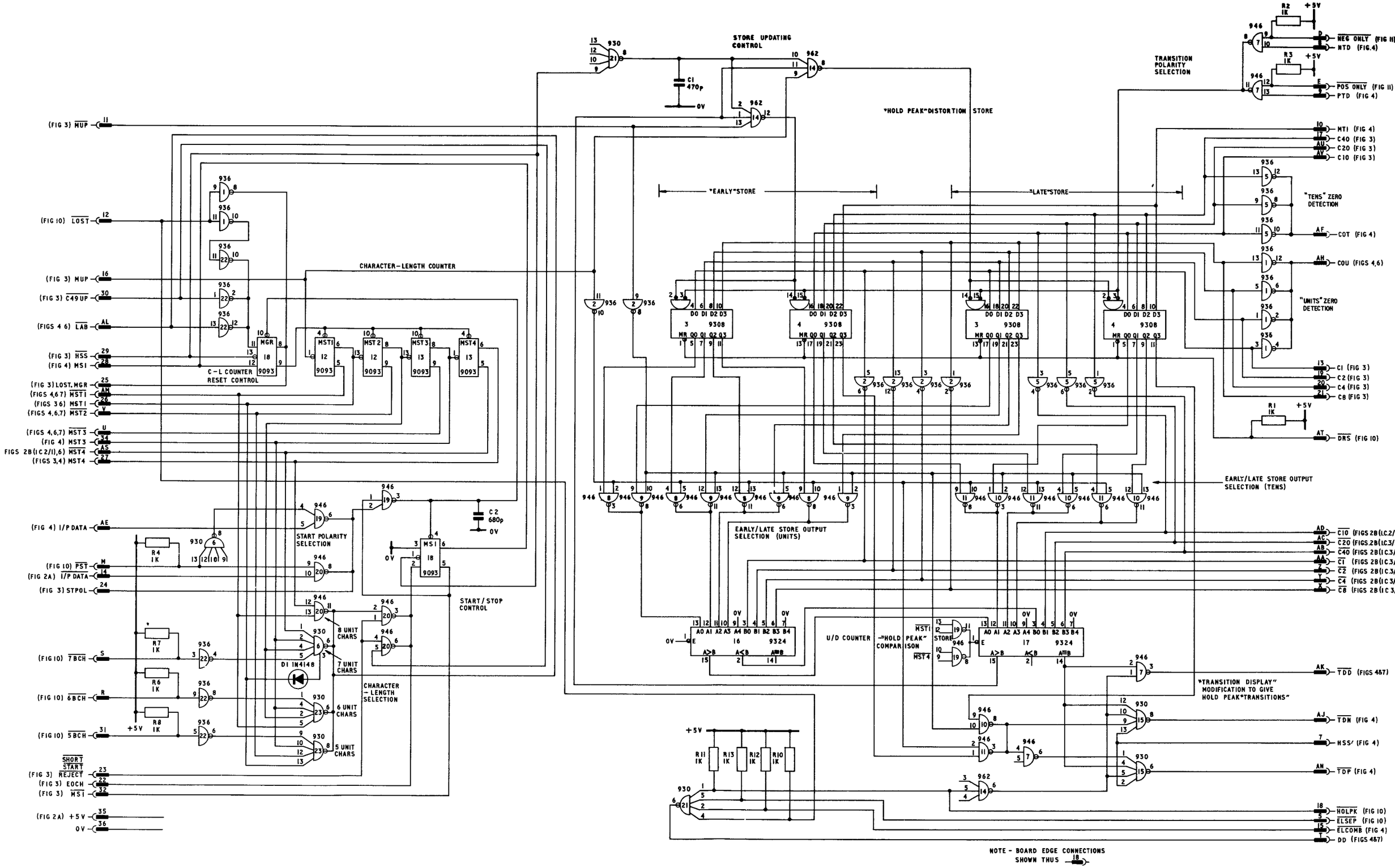
FIG. 3.



AKJ 7270 –

LOGIC BOARD 2 – CIRCUIT DIAGRAM.

FIG. 4 .



AKJ 7277 - D

LOGIC BOARD 3 - CIRCUIT DIAGRAM.

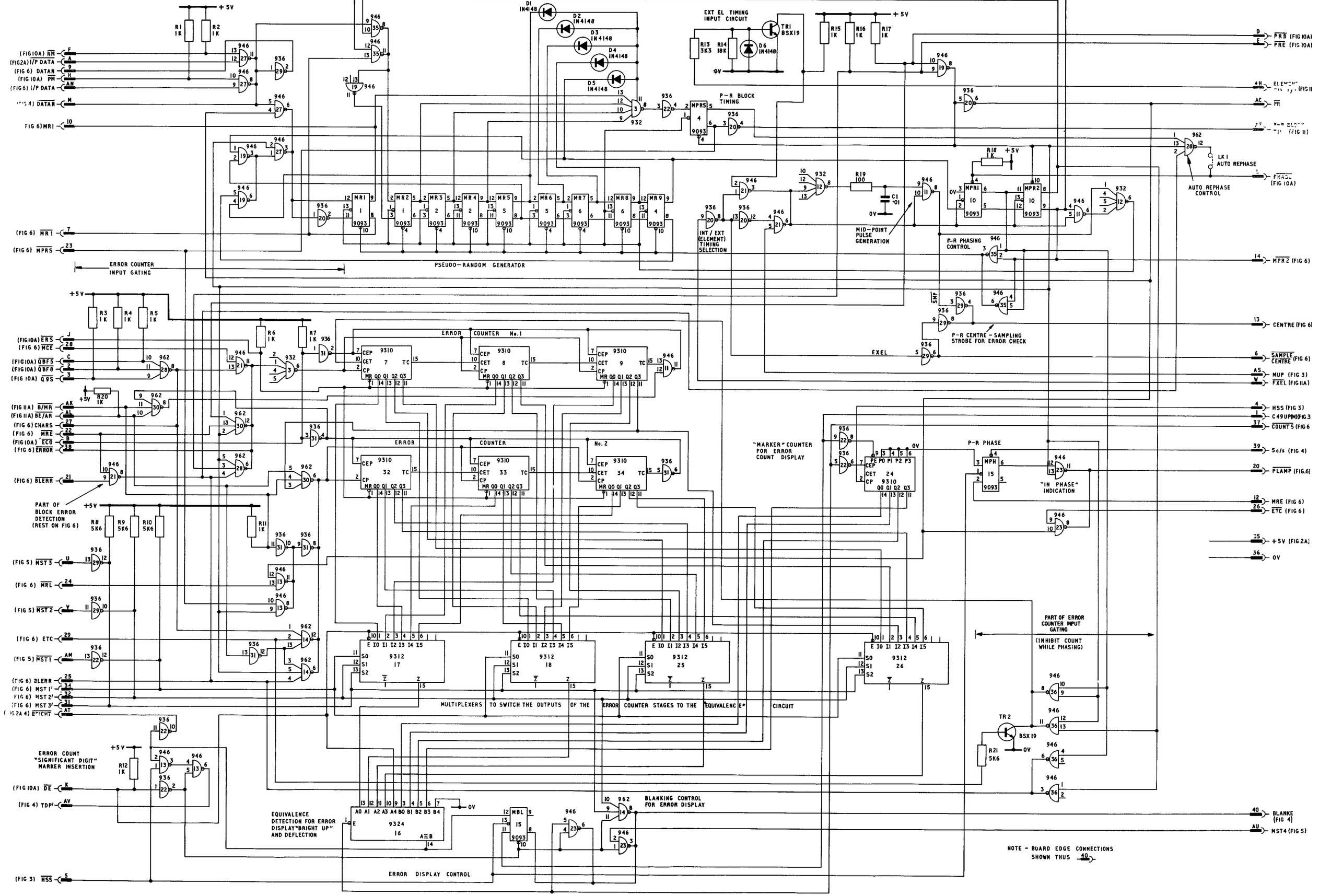
FIG. 5.

(FIG.2A) +15V
(FIG 2A) +5V
R8 1K
R3 2K7
R2 2K7
R1 2K7
R4 2K7
R5 2K7
R6 2K7
R7 2K7
MESSAGE-LENGTH COUNTER
READ-ONLY MEMORY
MMS2206J
R11 6K8
R12 6K8
R13 6K8
R14 6K8
R15 6K8
R16 6K8
R17 6K8
R10 6K8
9312
LOCAL START/STOP CHARACTER GENERATION
(FIG 7) ETC
(FIG 10A) TBF8
(FIG 5) EAB
(FIG 3) MSS
(FIG 7) ETC
(FIG 7) MRL
(FIG 5&11A) PHASE
0V
(FIG 10A) Q9S
(FIG 11A) MESSAGE TIMING
(FIG 10A) PEV
(FIG 7) CHARS
(FIG 7) MRI
(FIG 3) C49UP(M)
(FIG 5) MST1
(FIG 5) MST2
(FIG 5) MST3
(FIG. 5) MST4
(FIG 10A) POD
(FIG 7) ERROR
(FIG 11A) PARITY ERRORS
(FIG 7) MRI
(FIG 7) DATAN
(FIG 7) SAMPLE CENTRE
(FIG 7) MPR 2
(FIG. 7) DATAN
(FIG. 7) CENTRE
(FIG 7) FLAMP
(FIG 2A) 0V (LAMP)
(FIG 10A) TO IN PHASE LAMP
(FIG 11A) SEL 10
(FIG 11A) SEL 20
(FIG 11A) SEL 40
(FIG 11A) SEL 5
2XLF, CR CONTROL
M-L. COUNTER RESET CONTROL
PARITY ERROR DETECTION
START/STOP MESSAGE PHASING CONTROL
START/STOP CHARACTER ERROR DETECTION
ELEMENT SAMPLING POINT GENERATION
P-R ELEMENT ERROR DETECTION
"IN PHASE" LAMP DRIVE
TR2 BC107
TRI BC107
INPUT DATA DELAY REGISTER
PART OF BLOCK ERROR DETECTION (REST ON FIG 7)
NOTE - BOARD EDGE CONNECTIONS SHOWN THUS
AM MST 1' (FIG 7)
AL MST 2' (FIG 7)
40 -15V (FIG 2A)
AK MST 3' (FIG 7)
19 0V (FIG 10A)
AJ CHARACTER ERRORS (FIG 11A)
J ERS (FIG 10A)
AF MCE (FIG 7)
26 C10
25 C20
24 C40
29 COU
23 C1 (FIG 5)
21 C4
22 C2
20 C8
AS COUNT 5 (FIG 7)
H MRE (FIG 7)
7 MRE (FIG 7)
8 ELEMENT ERRORS (FIG 11A)
AA MPRS (FIG 7)
AC BLERR (FIG 7)
9 BLOCK ERRORS (FIG 11A)
Y BLERR (FIG 7)

AKJ 4646 - D

LOGIC BOARD 4 - CIRCUIT DIAGRAM.

FIG. 6.

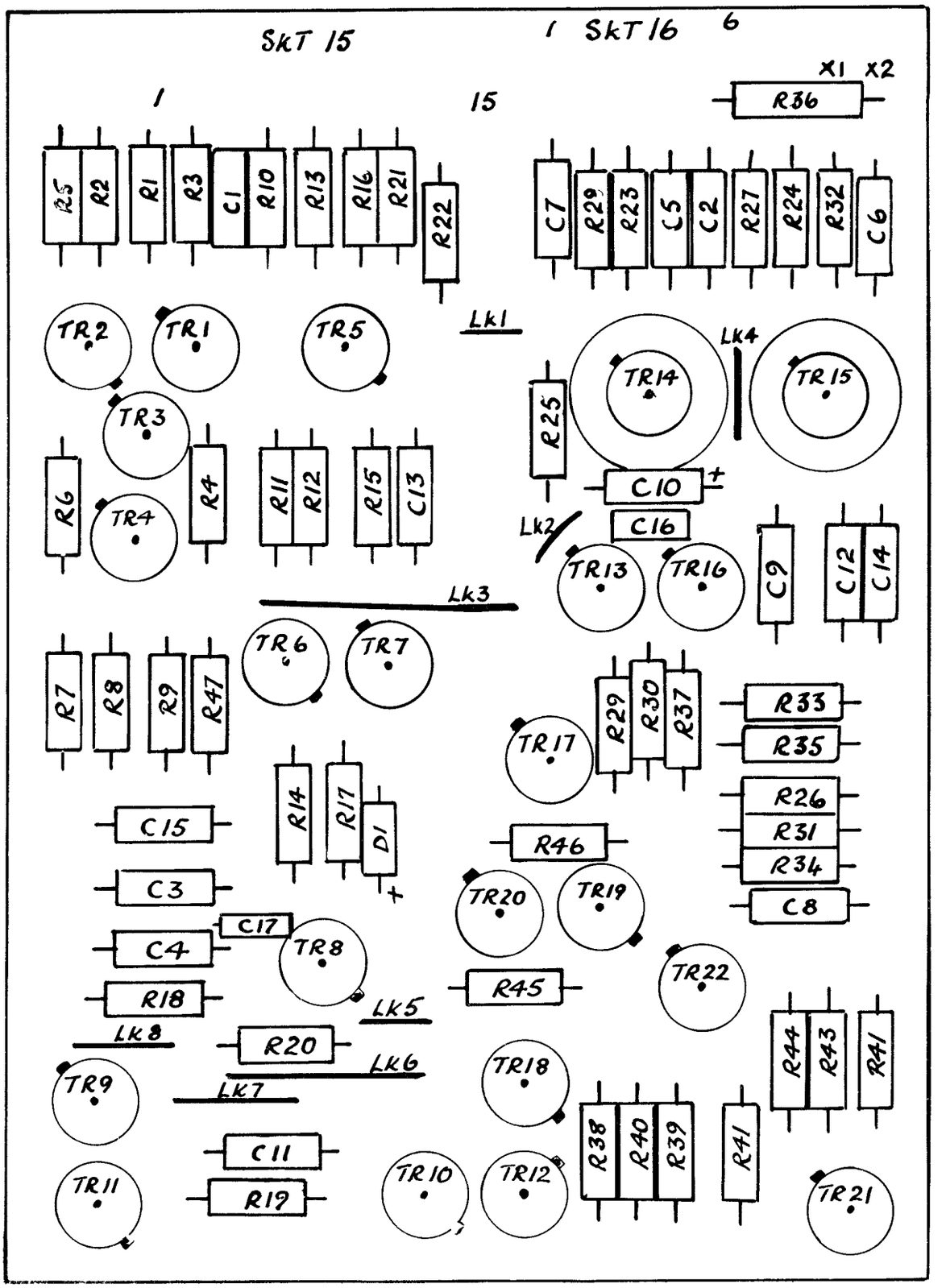


AKJ 7323 - D

LOGIC BOARD 5 - CIRCUIT DIAGRAM.

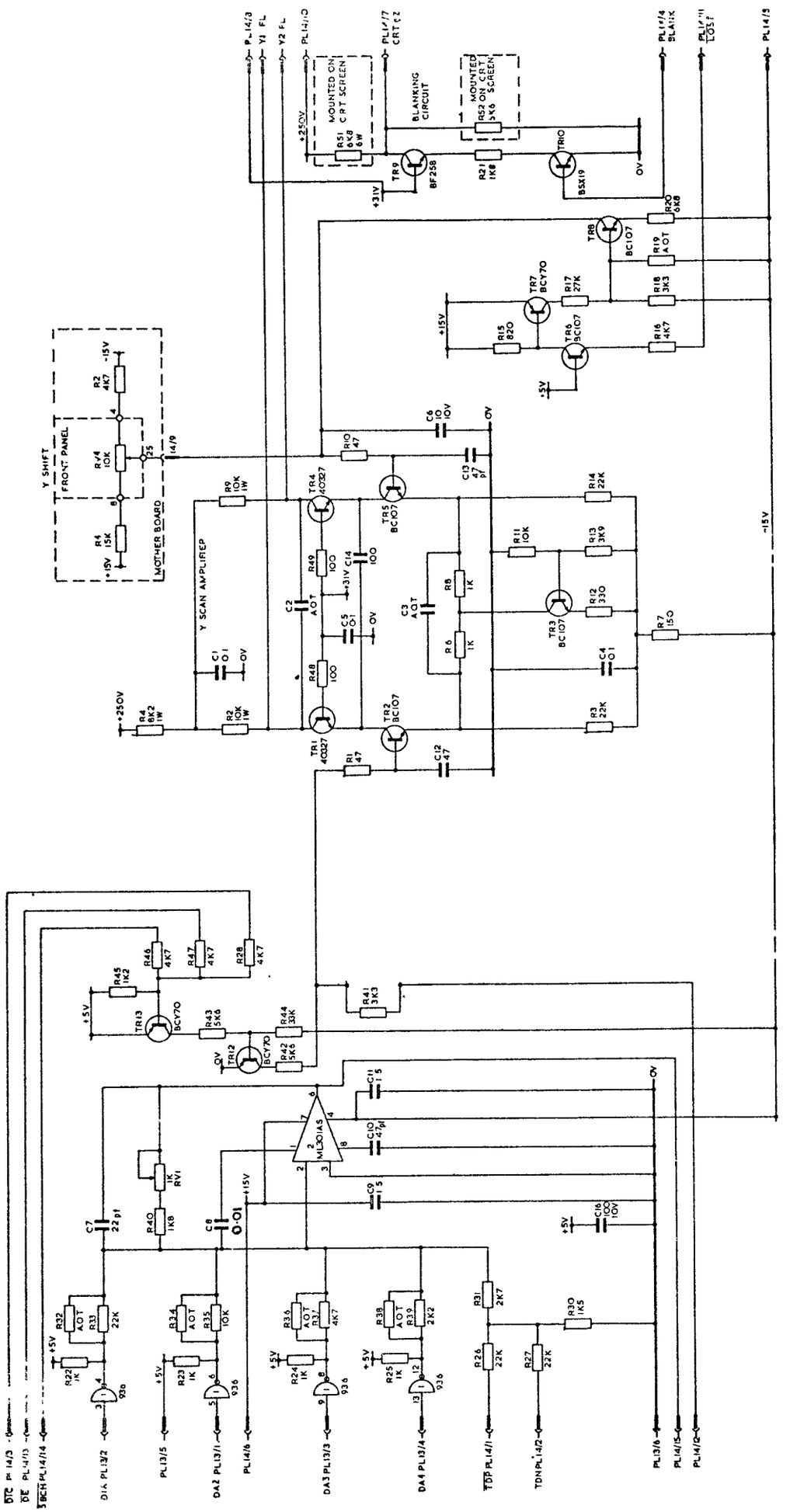
FIG. 7.

X AMPLIFIER BOARD – CIRCUIT DIAGRAM.



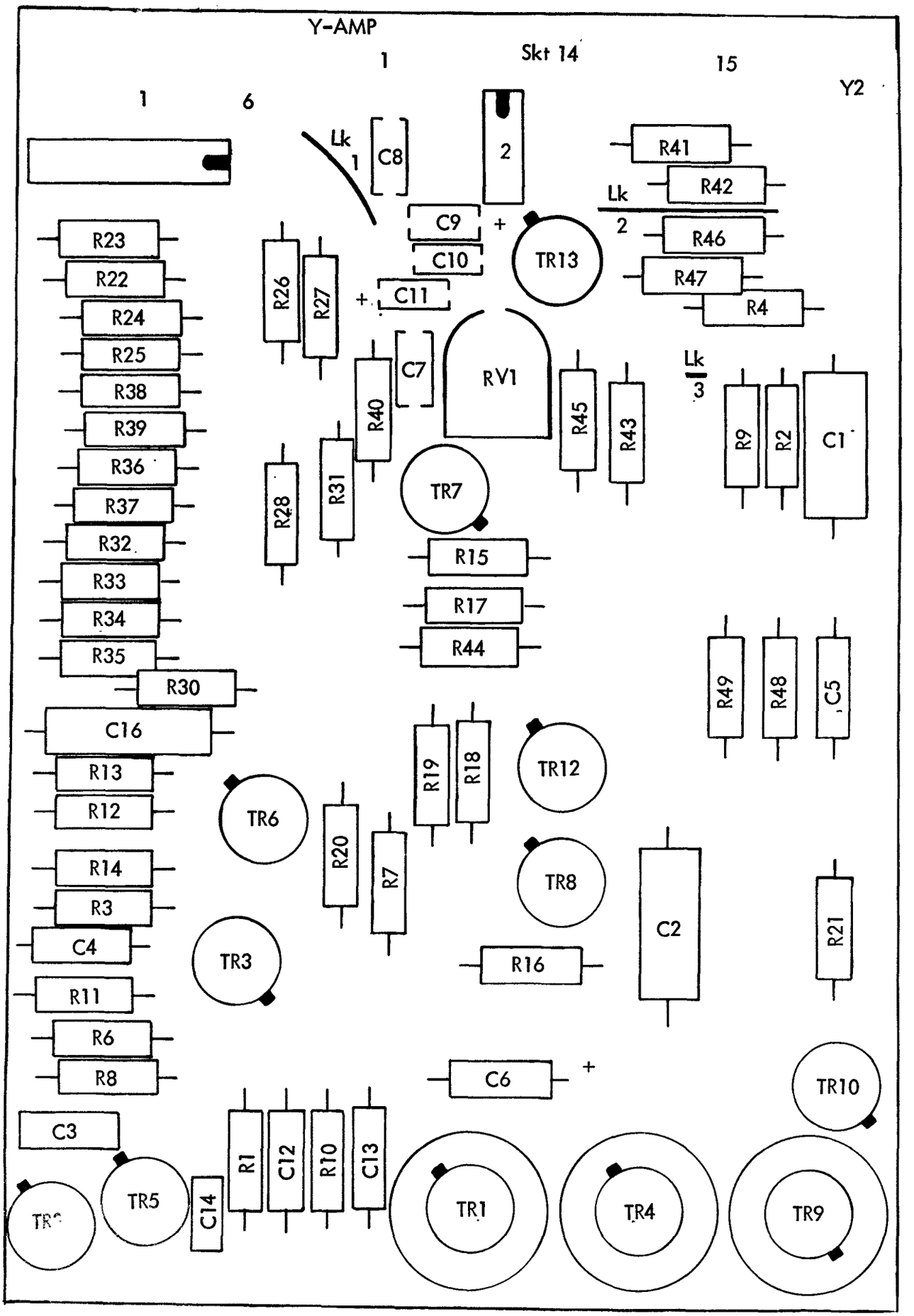
X AMPLIFIER - COMPONENT LOCATION

FIG.8B.



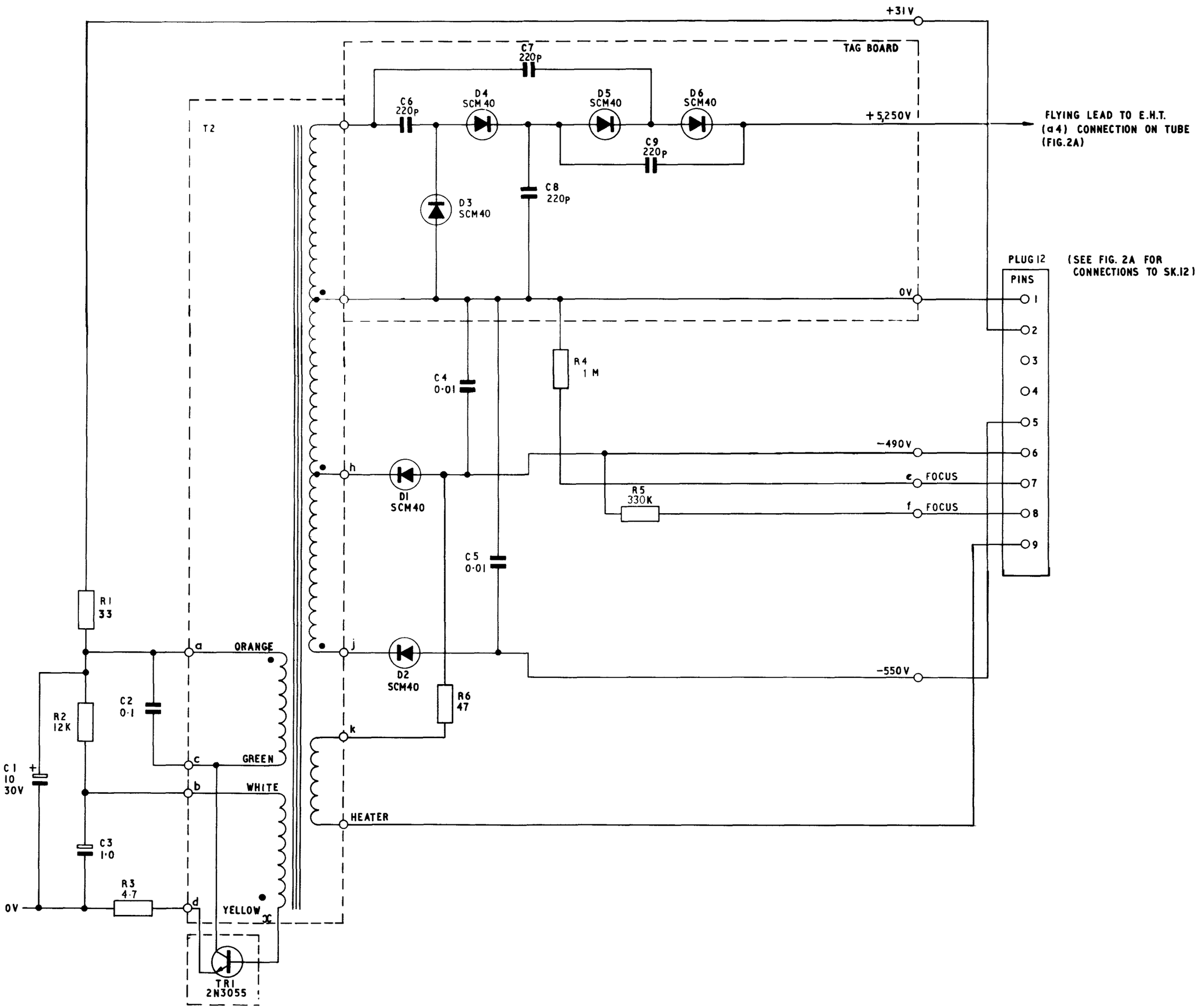
Y AMPLIFIER BOARD - CIRCUIT DIAGRAM.

FIG.8C.



Y AMPLIFIER - COMPONENT LOCATION

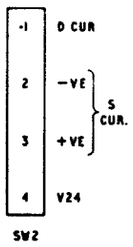
FIG.8D.

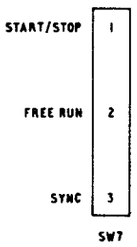


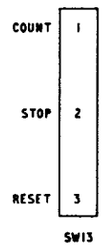
AKJ 7164

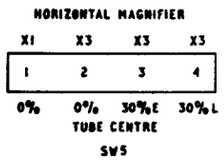
E.H.T. BOX - CIRCUIT DIAGRAM

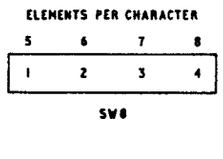
FIG. 9 .

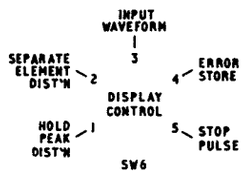


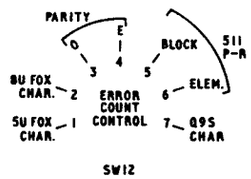


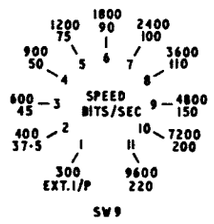




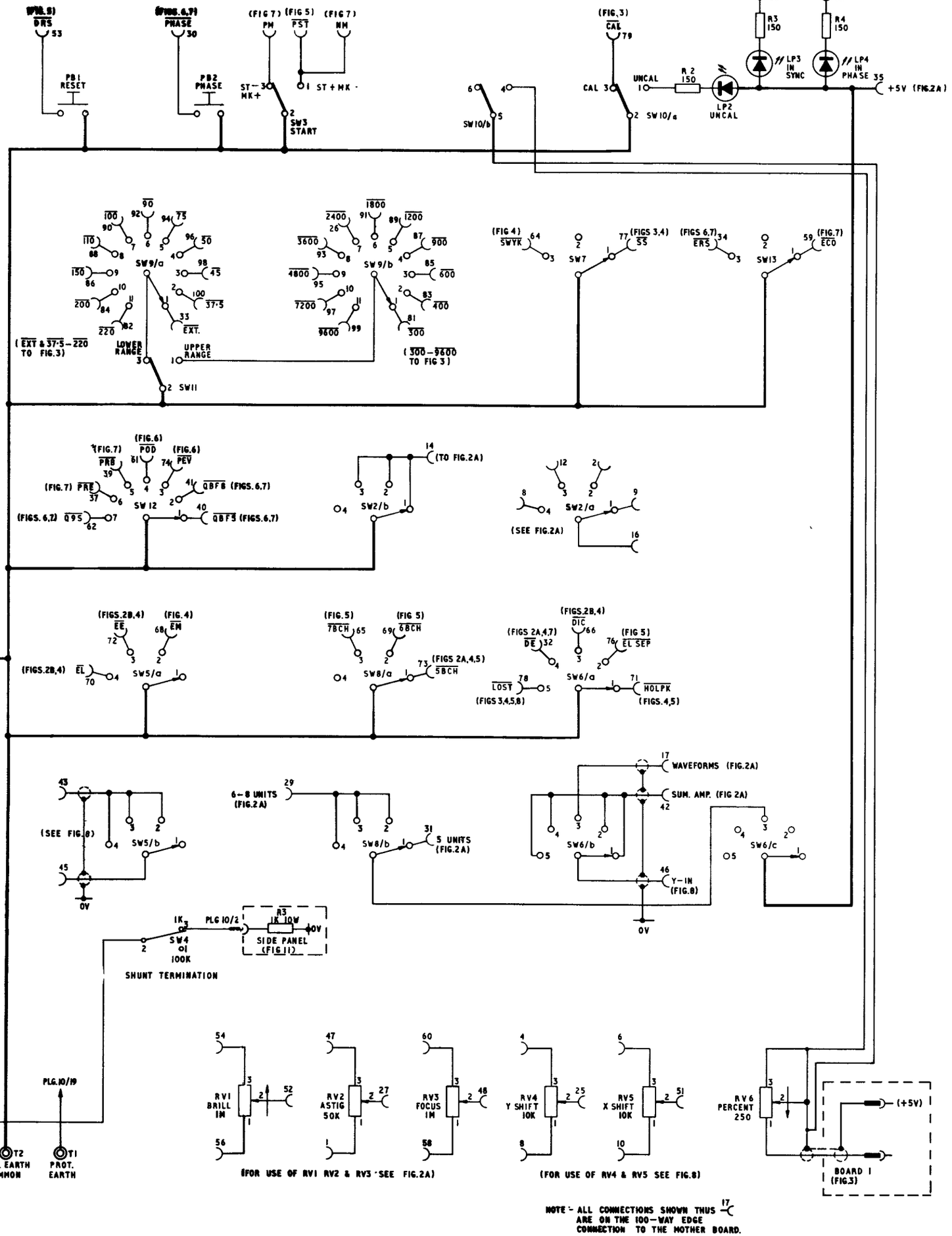


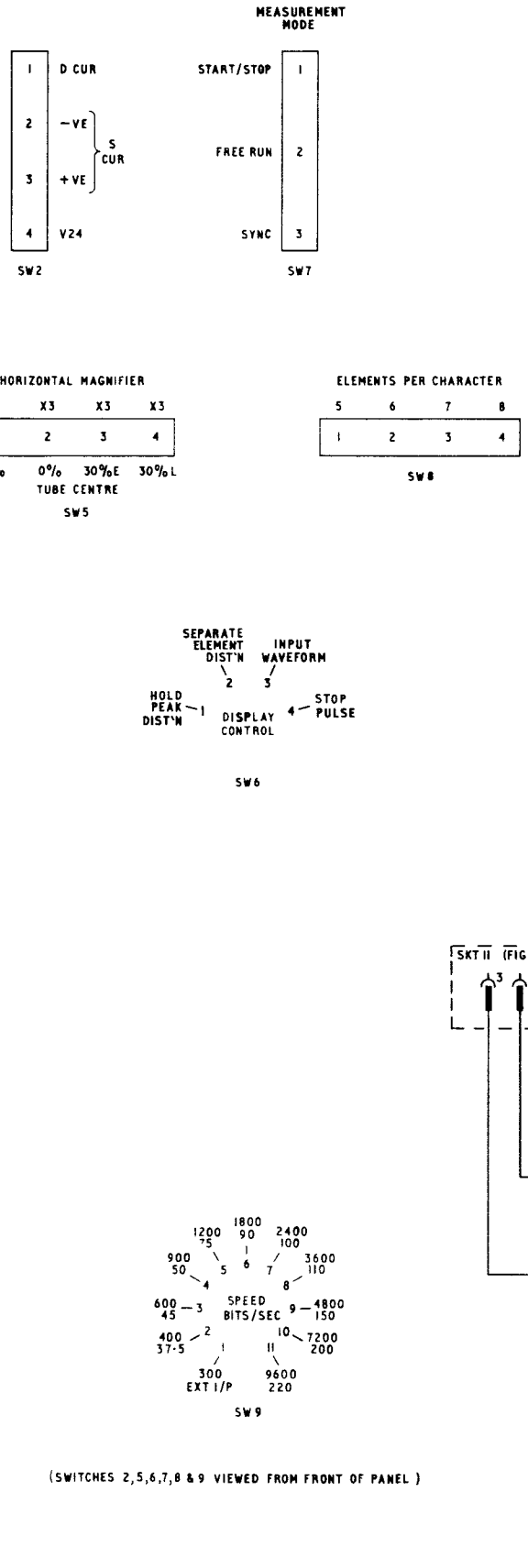






(SWITCHES 2,5,6,7,8,9,12&13 VIEWED FROM FRONT OF PANEL)

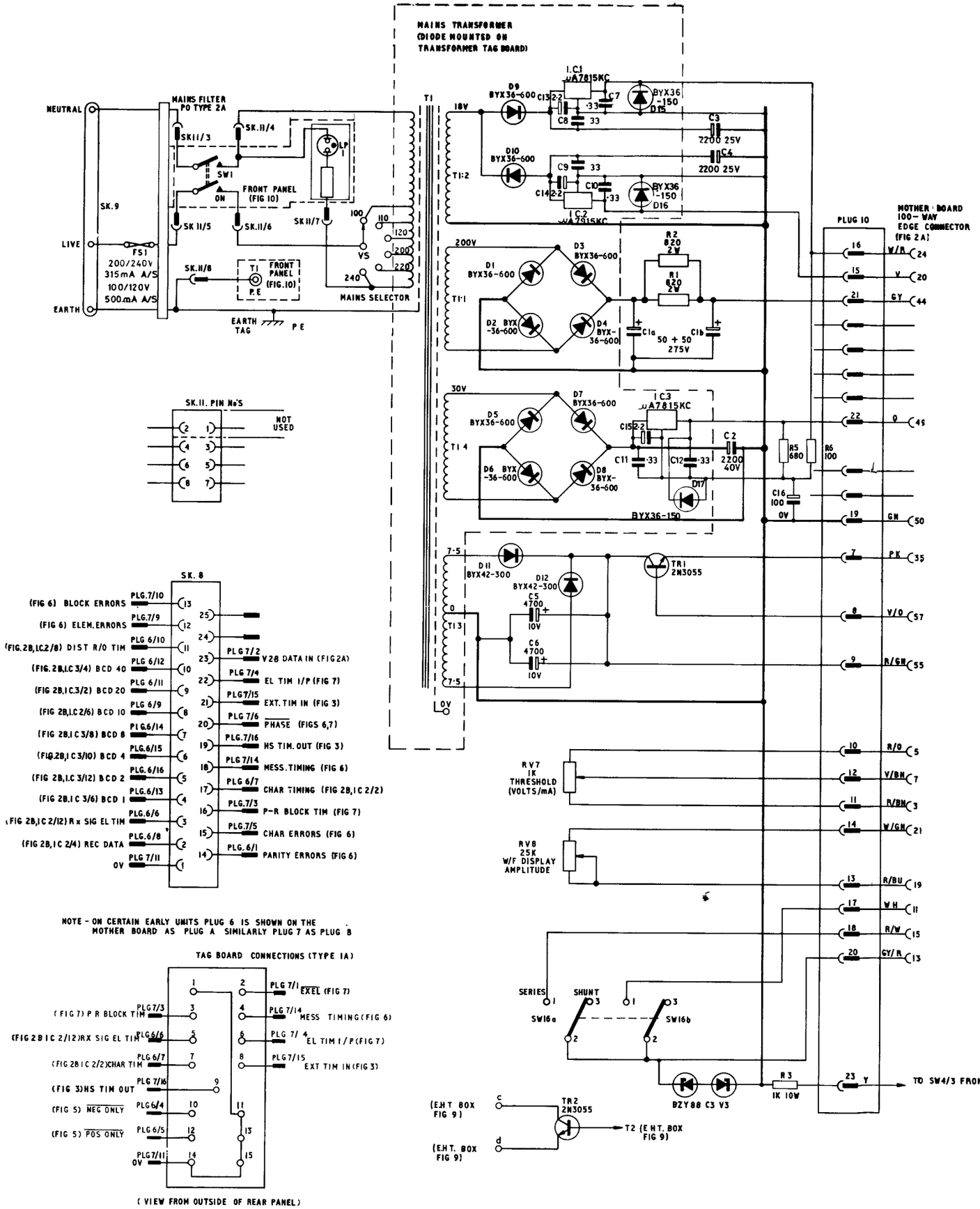




AKJ 7549 - D

FRONT PANEL COMPONENTS (TYPE 2A) - CIRCUIT DIAGRAM

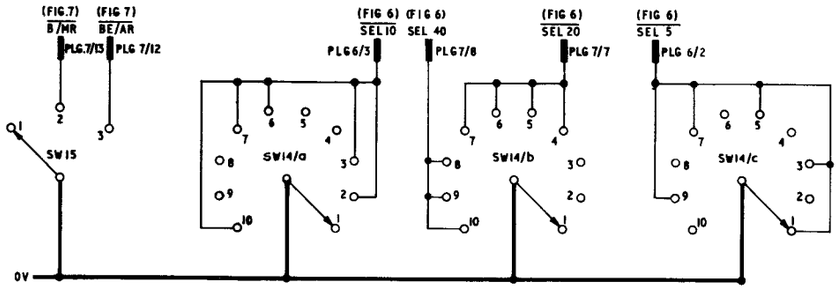
FIG. 10B .

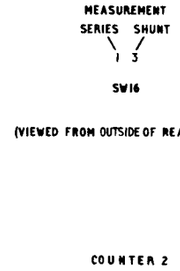


NOTE - ON CERTAIN EARLY UNITS PLUG 6 IS SHOWN ON THE MOTHER BOARD AS PLUG A SIMILARLY PLUG 7 AS PLUG B

TAG BOARD CONNECTIONS (TYPE 1A)

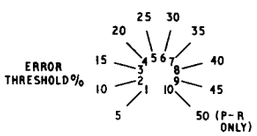
(VIEW FROM OUTSIDE OF REAR PANEL)





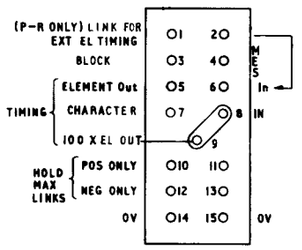
(VIEWED FROM OUTSIDE OF REAR PANEL)

(VIEWED FROM OUTSIDE OF REAR PANEL)



(VIEWED FROM OUTSIDE OF REAR PANEL)

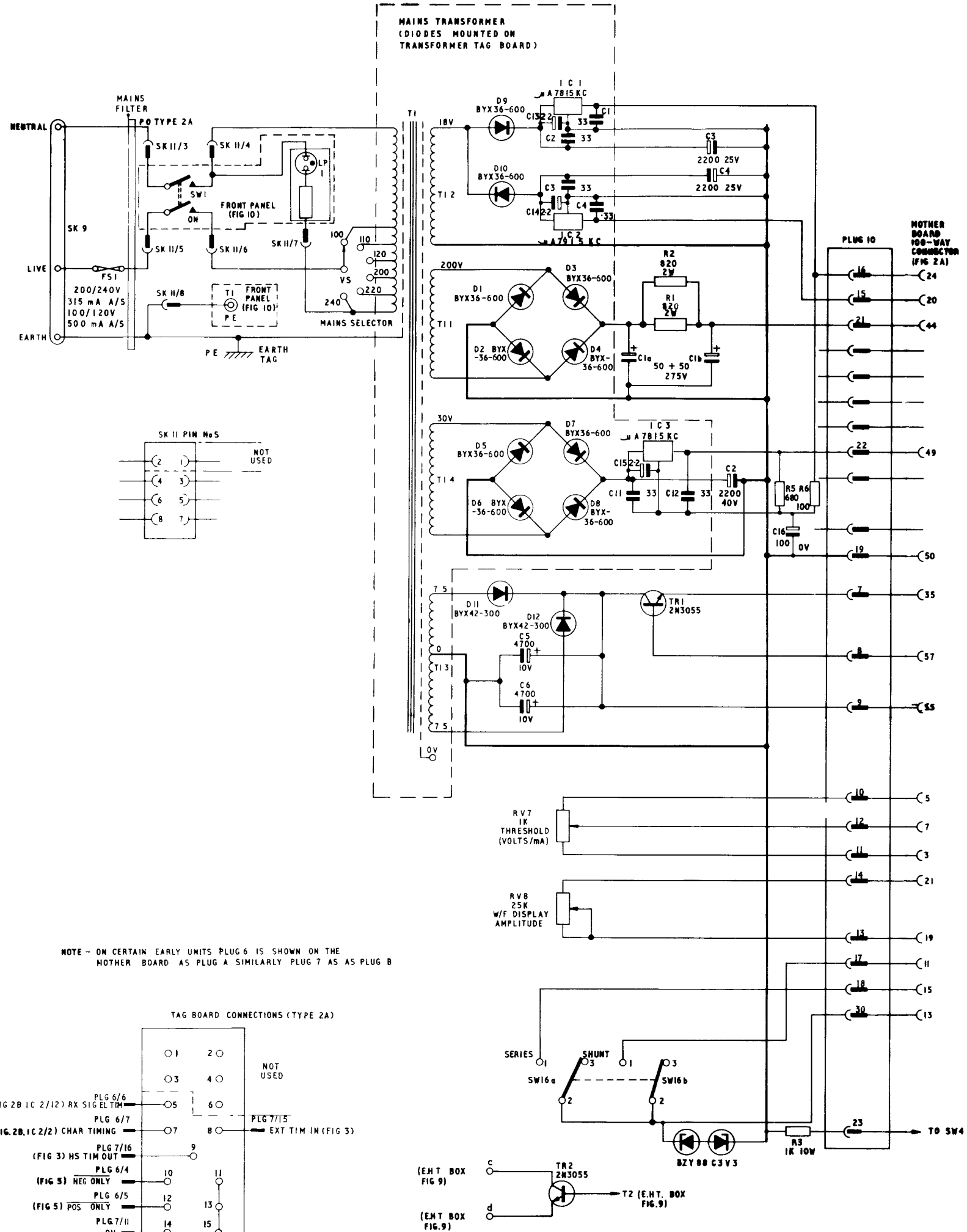
TAG BOARD ANNOTATION (TYPE 1A)



(VIEWED FROM OUTSIDE OF REAR PANEL)

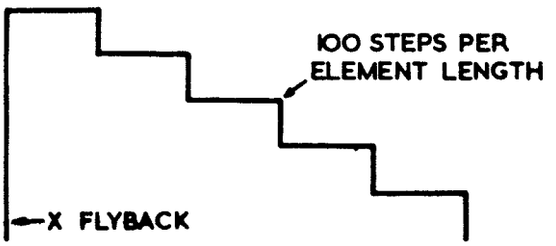
REAR & SIDE PANEL COMPONENTS (TYPE 1A) - CIRCUIT DIAGRAM

FIG. 11A .

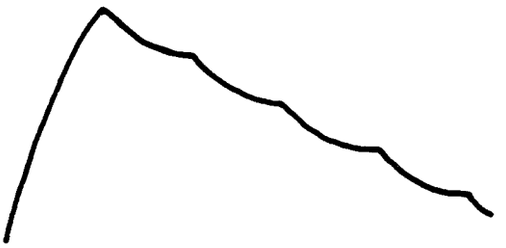


REAR & SIDE PANEL COMPONENTS (TYPE 2A) - CIRCUIT DIAGRAM

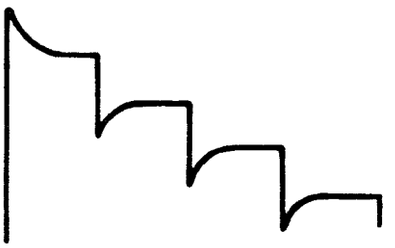
FIG. 11B .



IDEAL x SCAN WAVEFORM

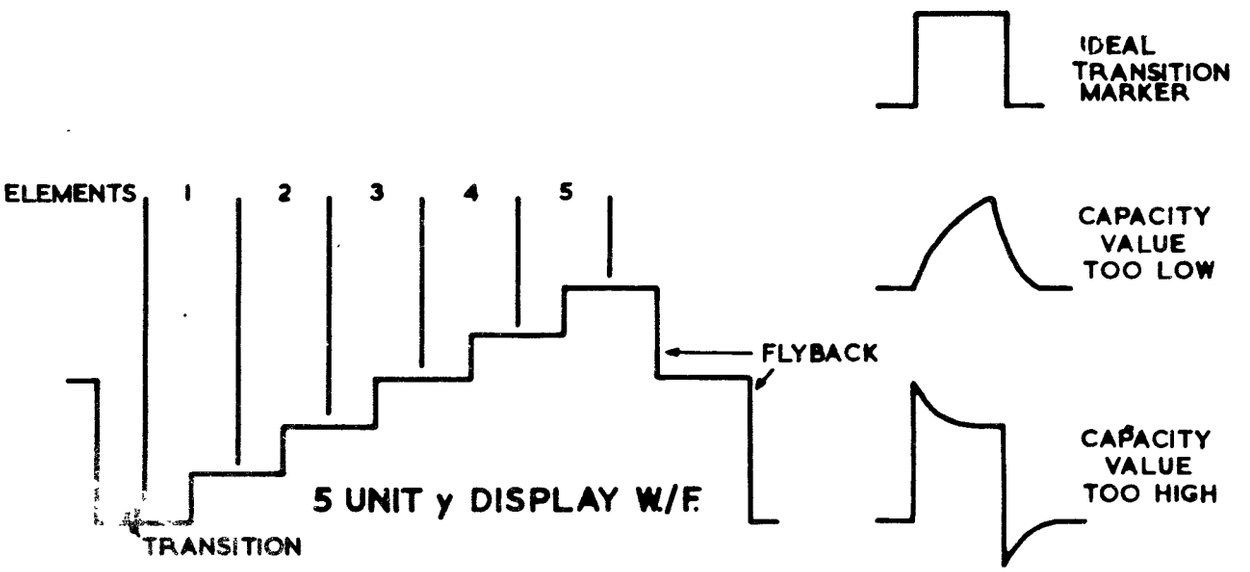


CAPACITY VALUE TOO LOW



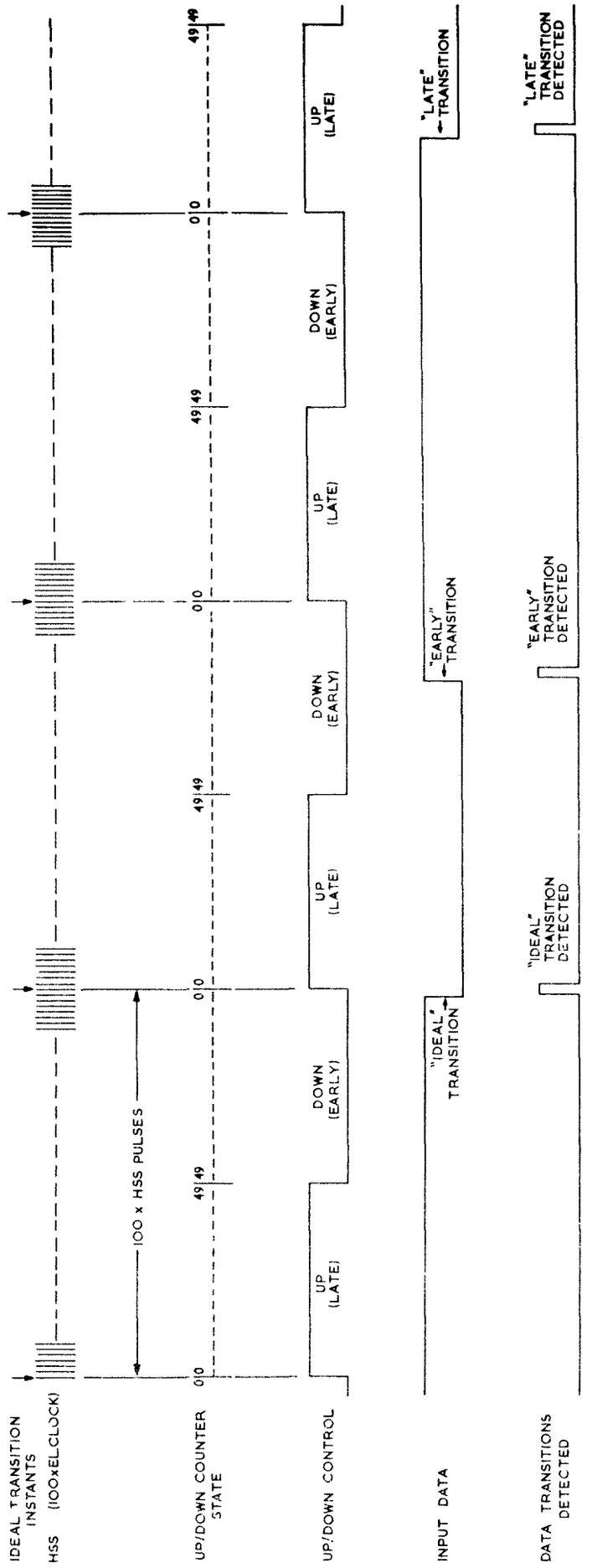
CAPACITY VALUE TOO HIGH

X SCAN AMPLIFIER H.F. COMPENSATION (4.3.4.) FIG. 12A.



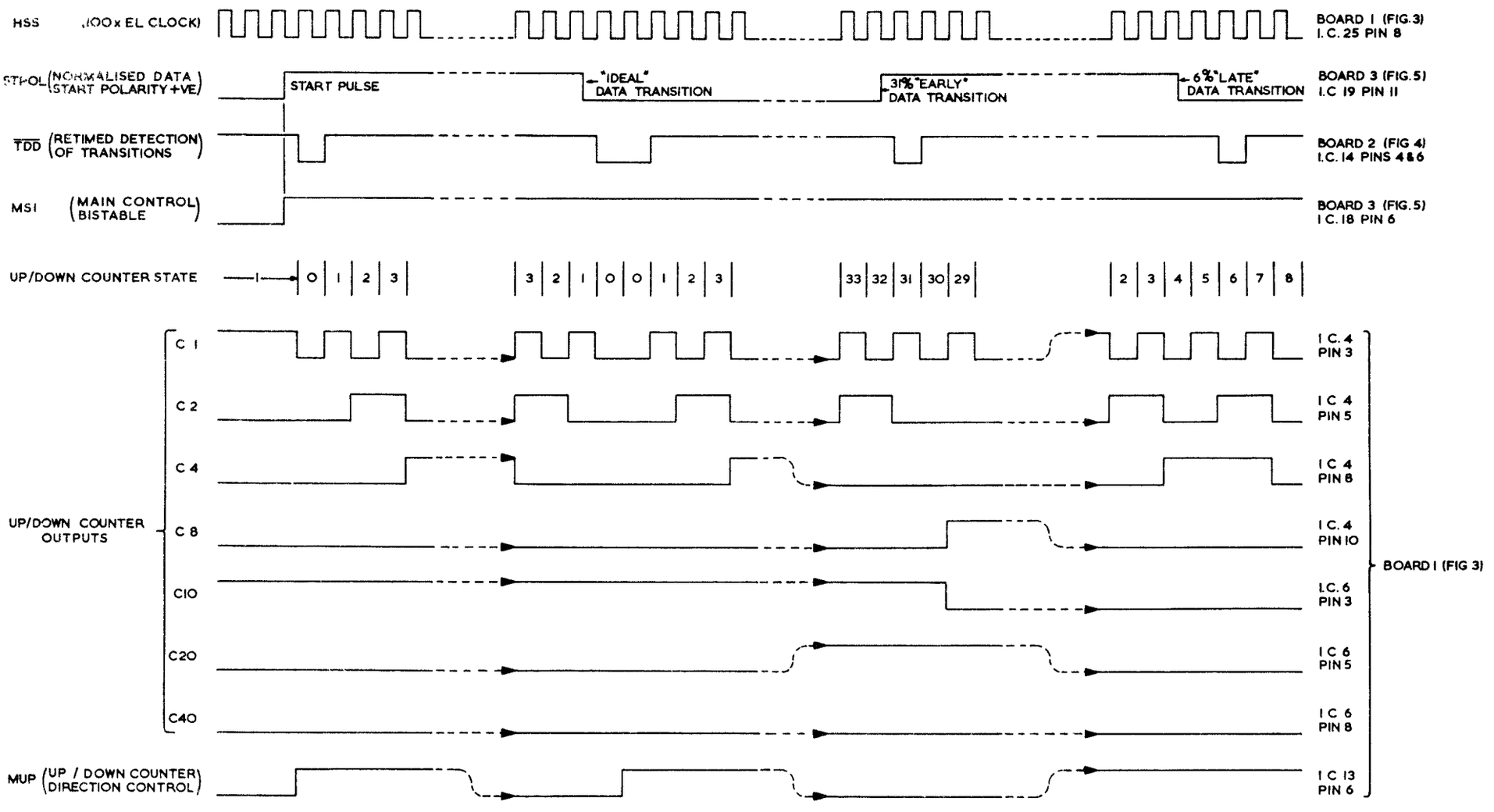
Y SCAN AMPLIFIER H.F. COMPENSATION (4.3.7.)

FIG. 12B.



RELATIONSHIP OF UP/DOWN COUNTER TO INCOMING DATA TRANSITIONS

FIG. 12C.

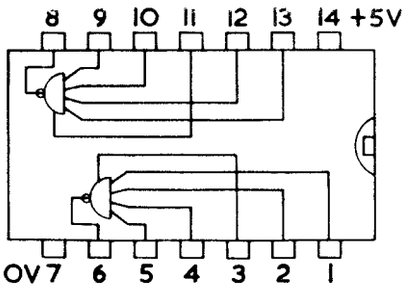


RELATIONSHIP OF UP/DOWN COUNTER TO START ELEMENT TRANSITION AND SUBSEQUENT TRANSITIONS DISTORTED BY VARIOUS AMOUNTS

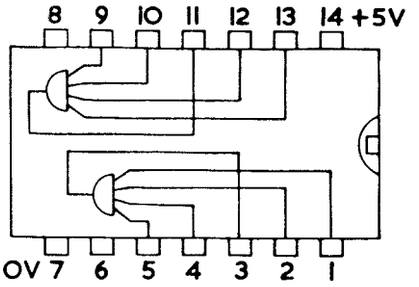
FIG. 12D.

930 DUAL 4 INPUT NAND GATE

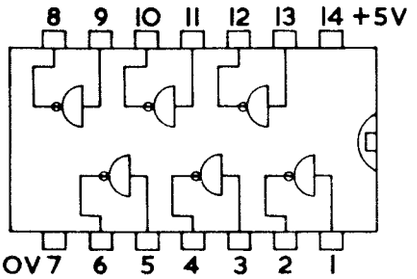
932 DUAL INPUT BUFFER



933 DUAL 4 INPUT EXPANDER

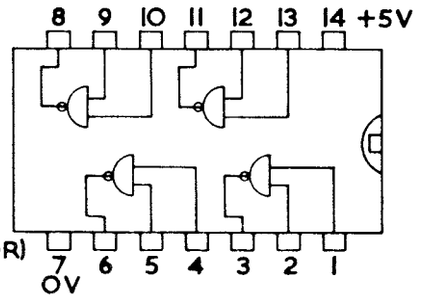


936 HEX INVERTER

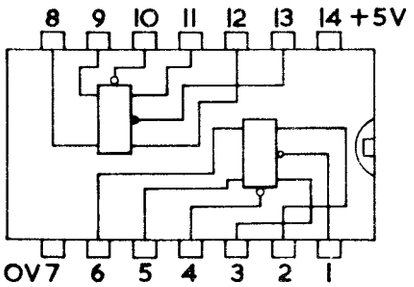


946 QUAD 2 INPUT NAND GATE

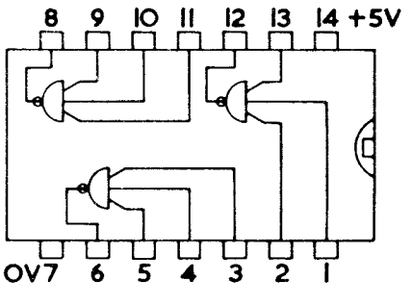
DM 8810 QUAD HIGH LEVEL DRIVER (OPEN COLLECTOR)



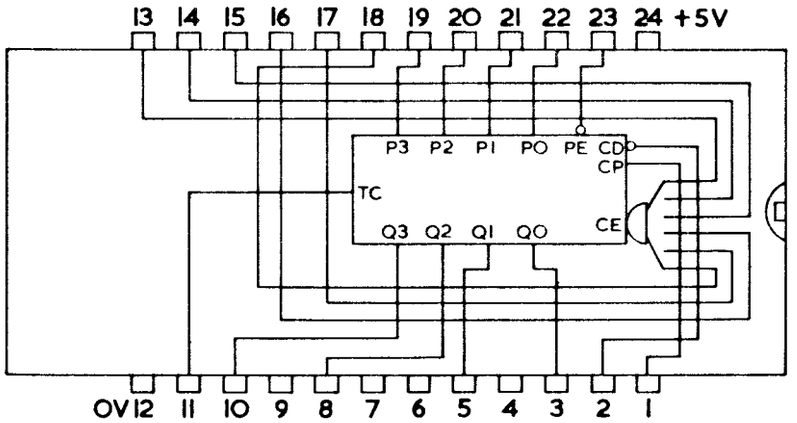
9093 DUAL CLOCKED JK FLIP-FLOPS



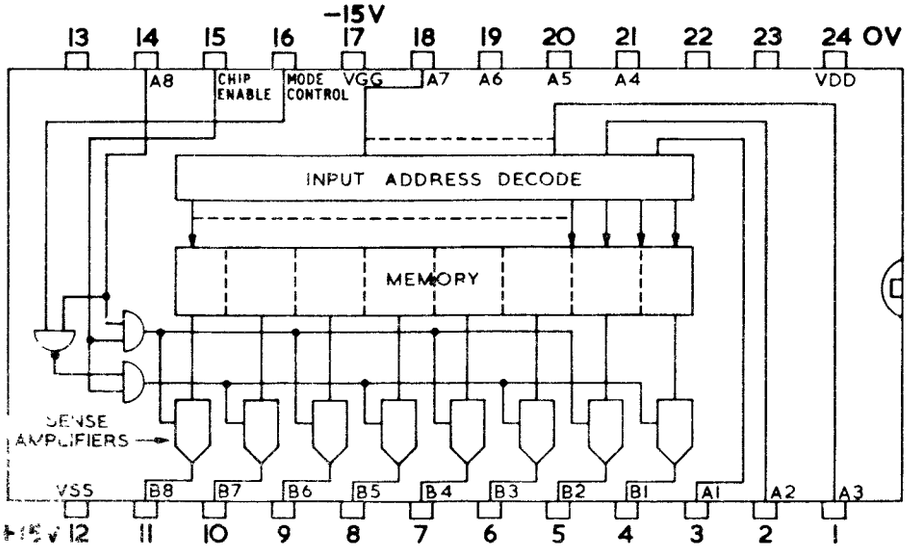
962 TRIPLE 3 INPUT NAND GATE



9306 10-WAY UP/DOWN BCD COUNTER



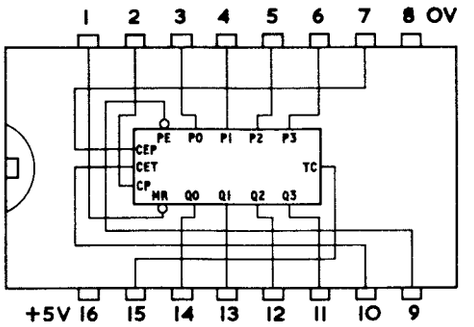
MM5220 1024-BIT READ ONLY MEMORY



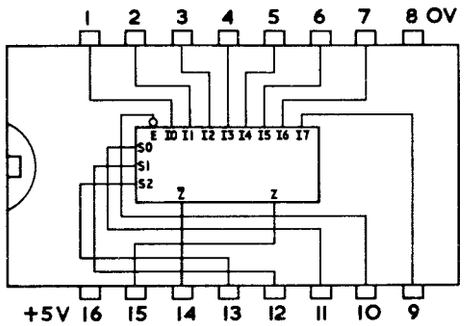
I.C. PIN CONNECTIONS

FIG. 13A.

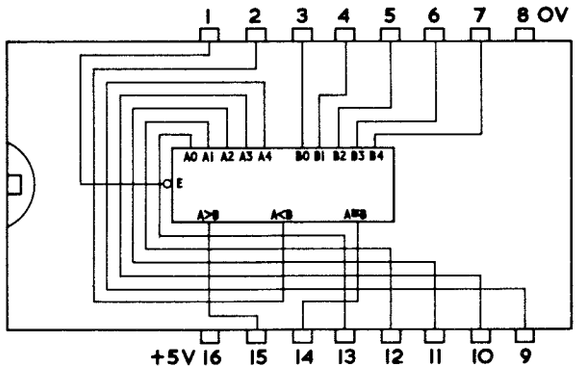
9310 BCD DECADE COUNTER.



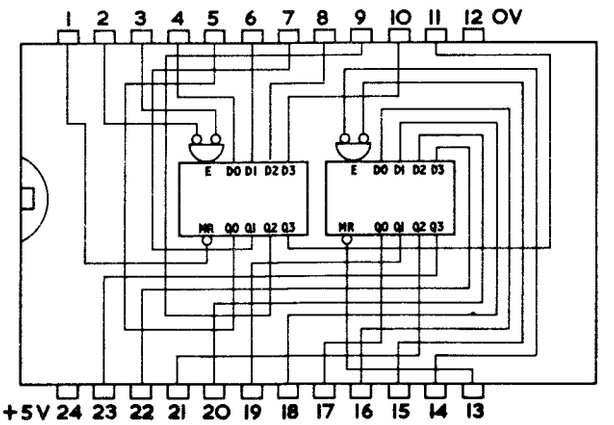
9312. 8 INPUT MULTIPLEXER.



9324. 5 BIT COMPARATOR.

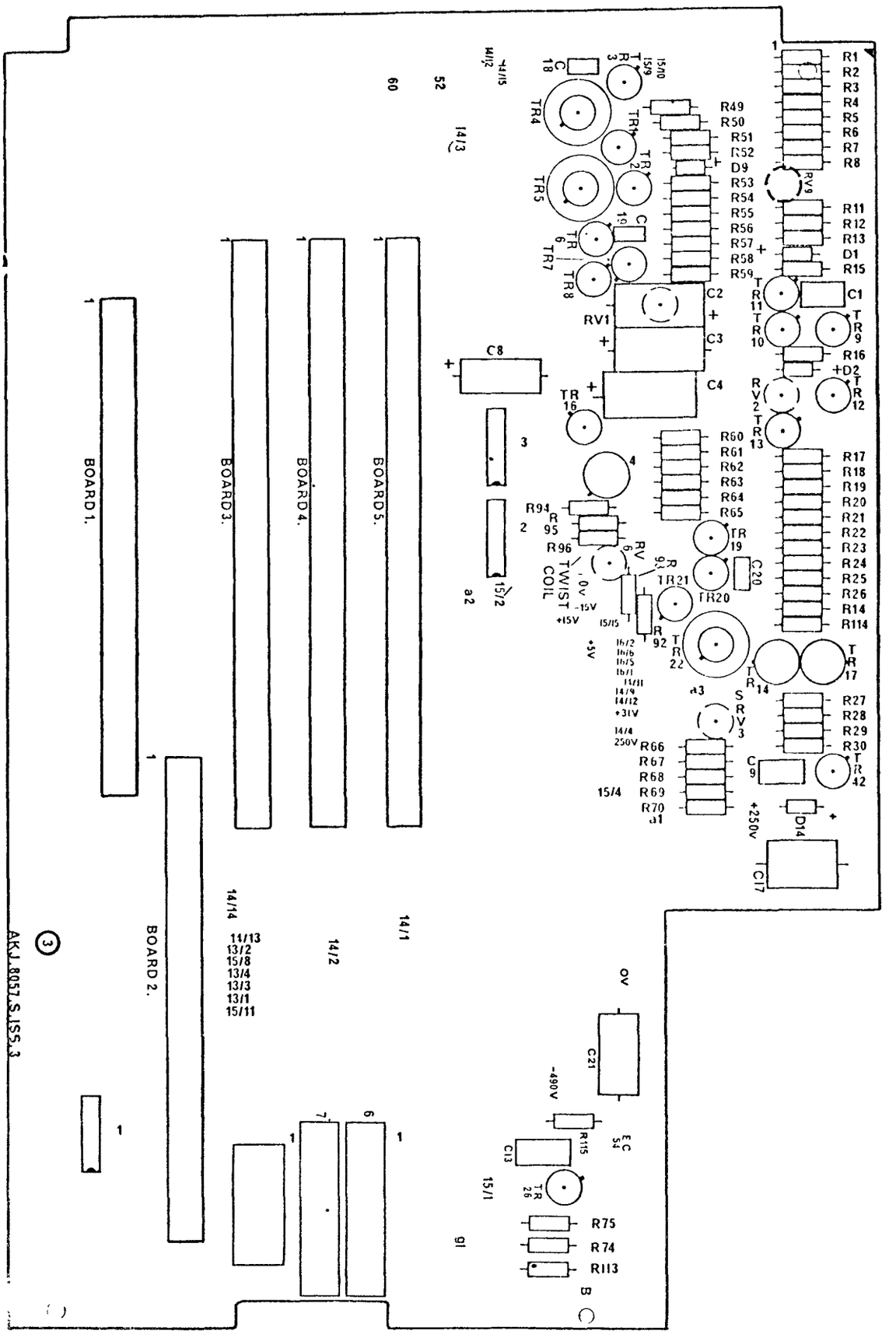


9308 DUAL 4 BIT LATCH.

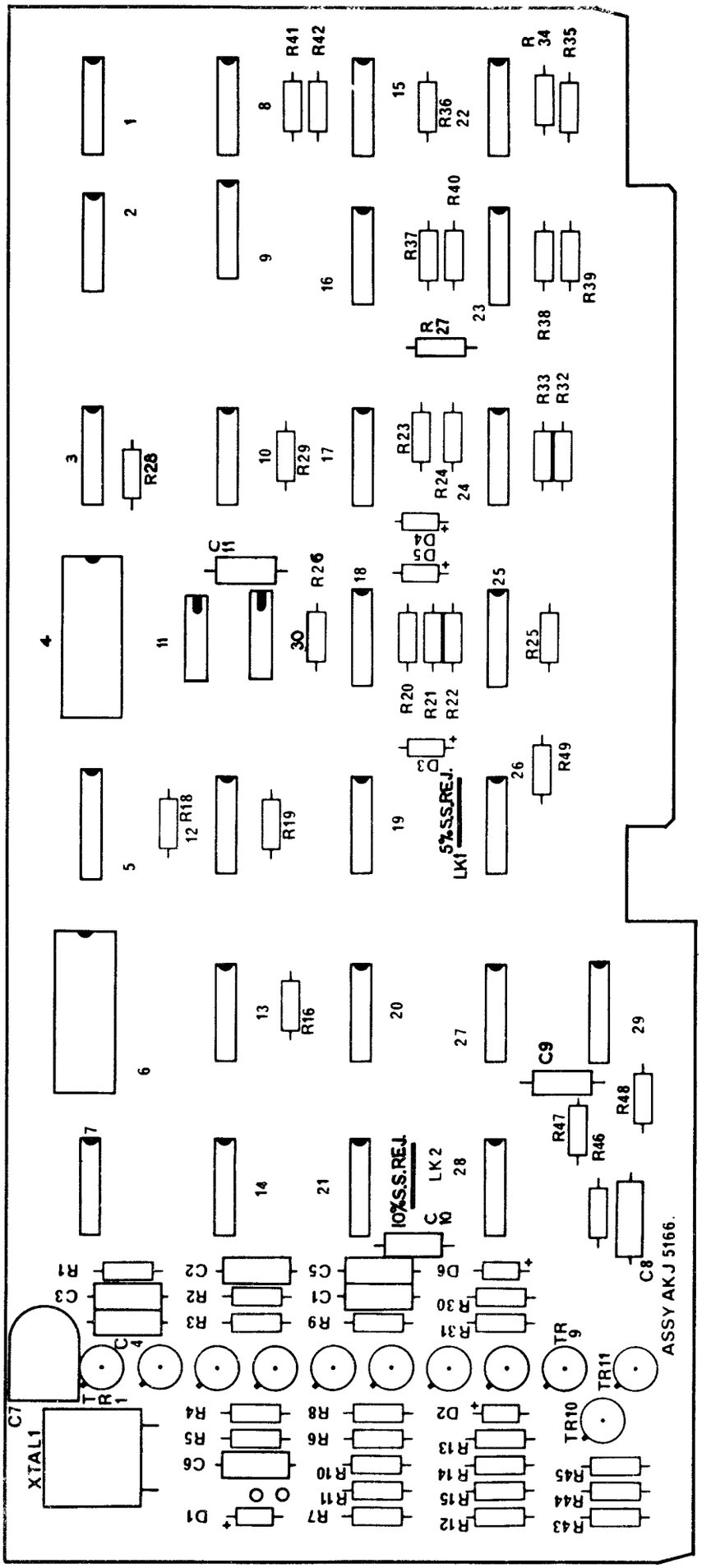


I.C.PIN CONNECTIONS

FIG.13B.

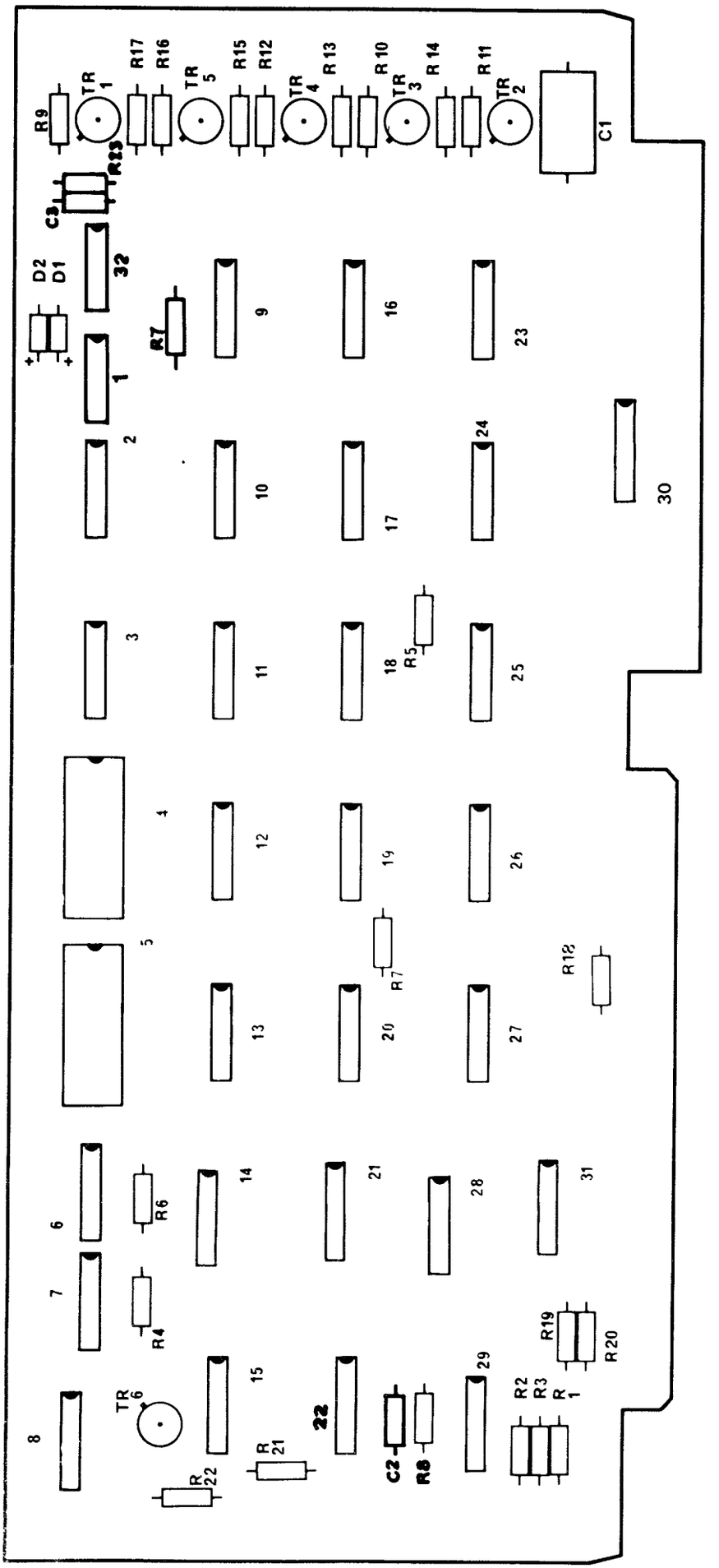


MOTHER BOARD - COMPONENT LOCATION FIG.14.

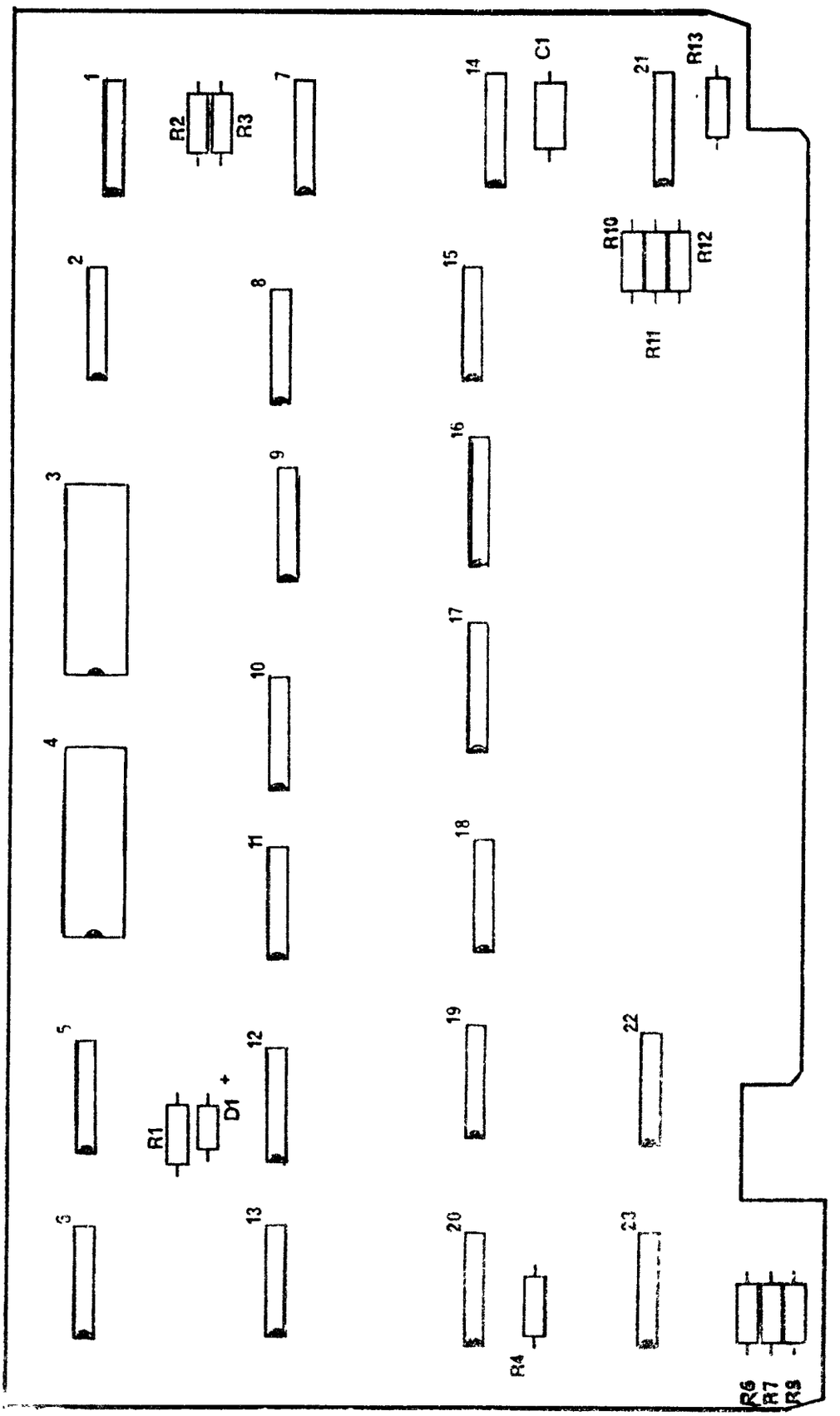


LOGIC BOARD 1 - COMPONENT LOCATION

FIG.15.

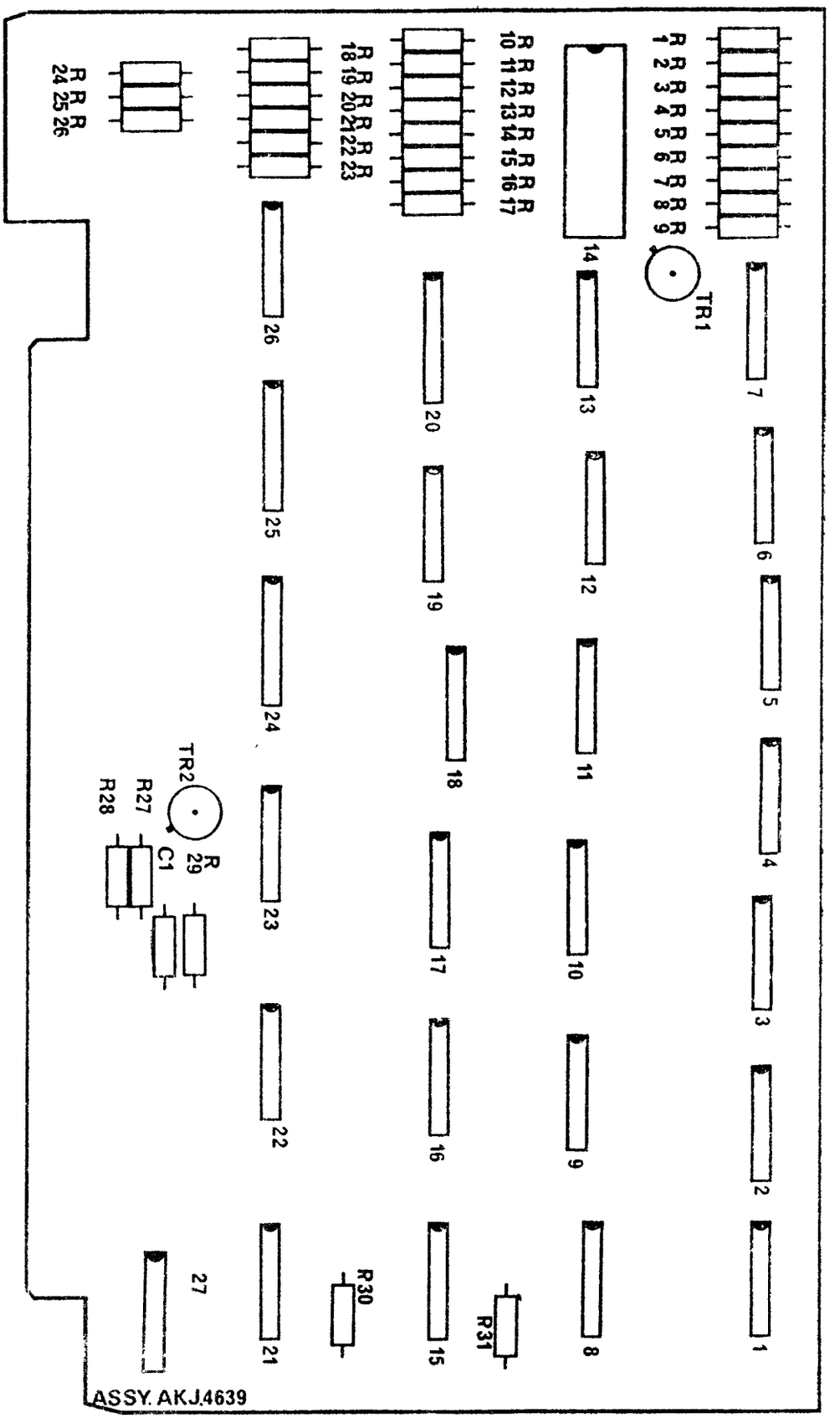


LOGIC BOARD 2 - COMPONENT LOCATION FIG.16



LOGIC BOARD 3 - COMPONENT LOCATION

FIG.17.



LOGIC BOARD 4 - COMPONENT LOCATION.

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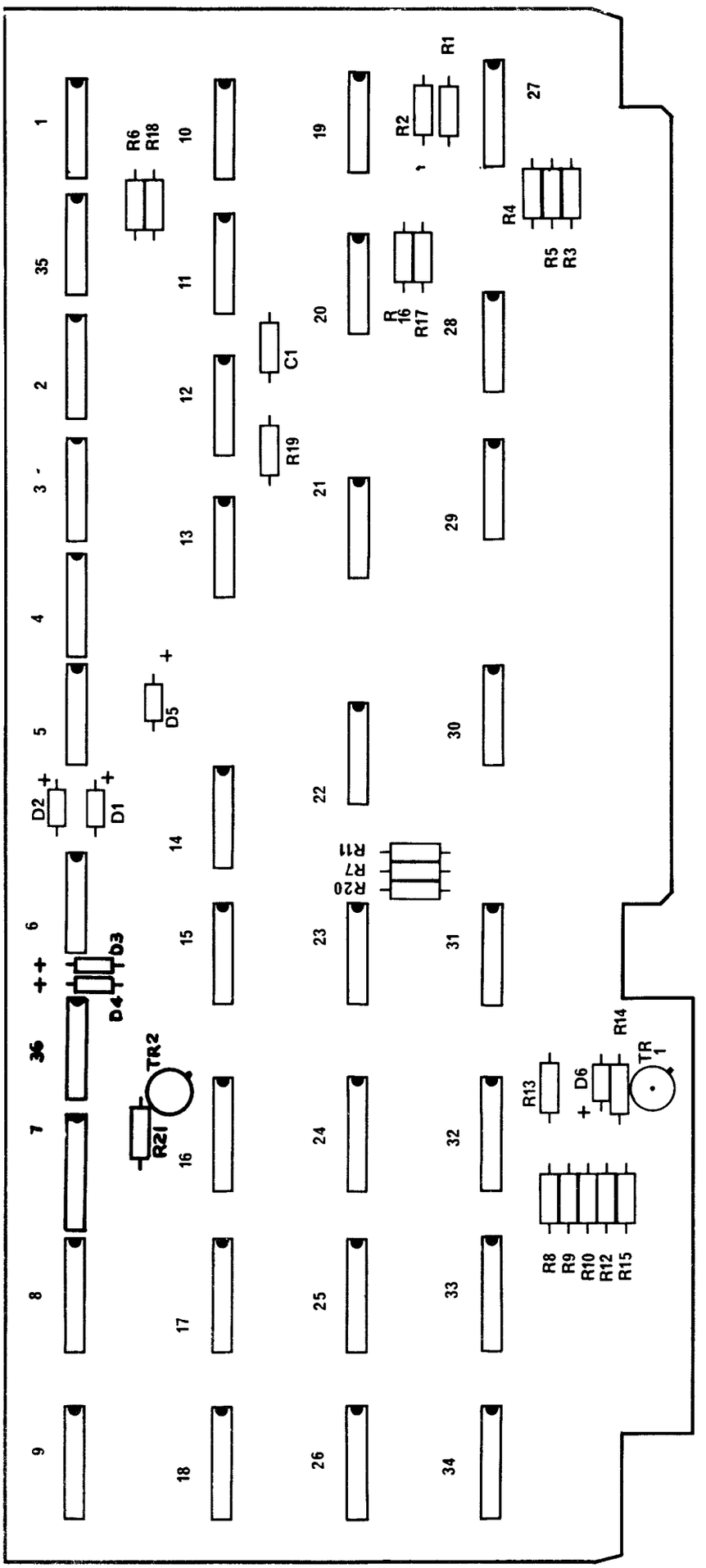
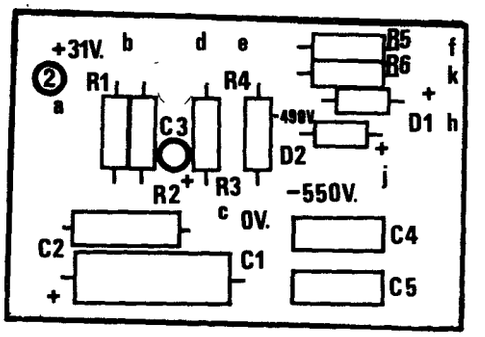
FIG. 18



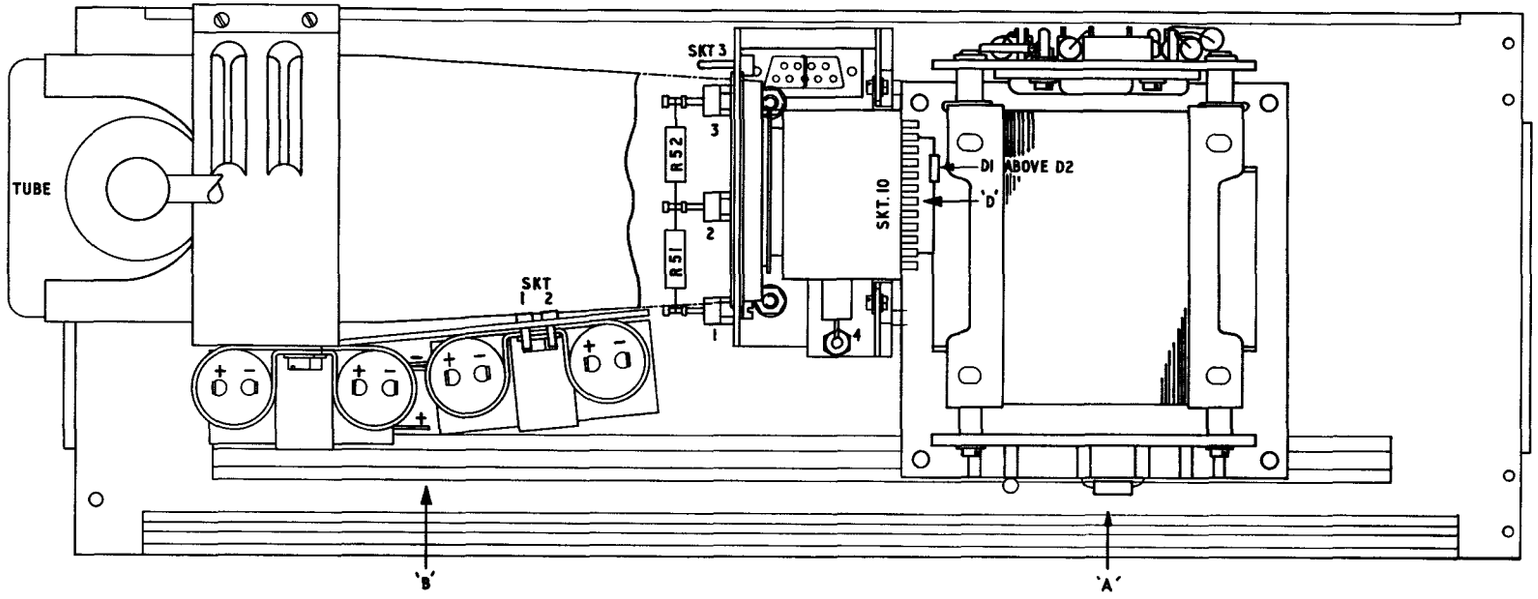
LOGIC BOARD 5 - COMPONENT LOCATION



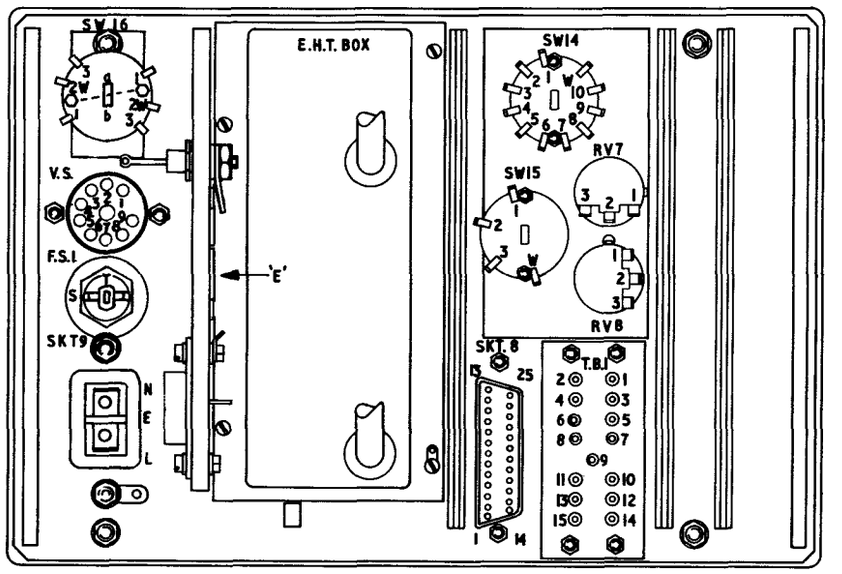
E.H.T. PCB - COMPONENT LAYOUT.

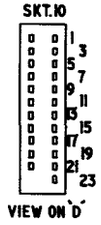
FIG.21.

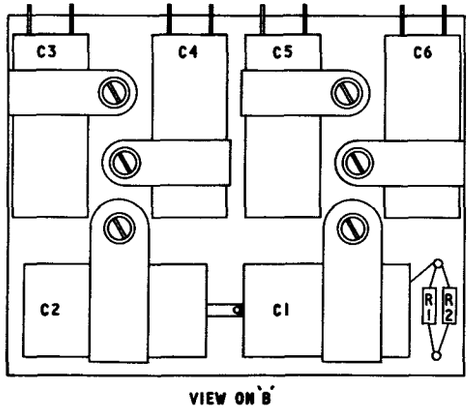
L.H. SIDE PANEL VIEWED FROM INSIDE UNIT. TYPES 1A & 2A & 2C

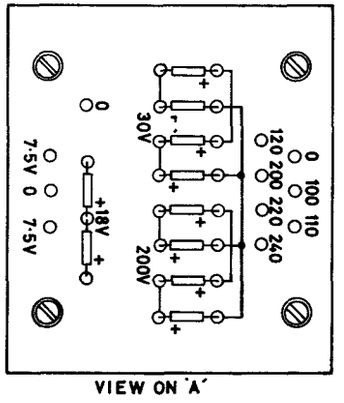


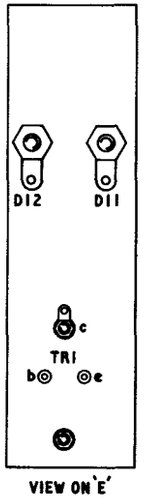
REAR PANEL VIEWED FROM INSIDE UNIT. TYPE 1A



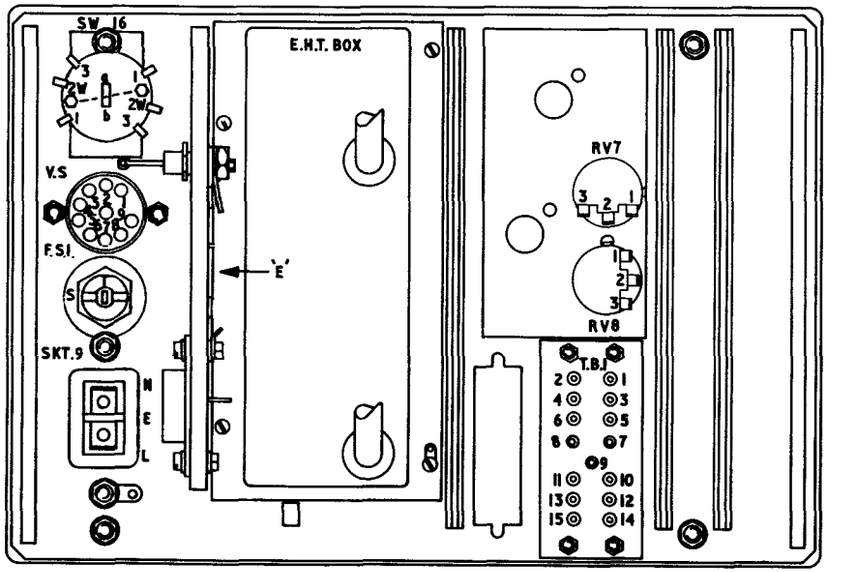








REAR PANEL VIEWED FROM INSIDE UNIT. TYPE 2A & 2C



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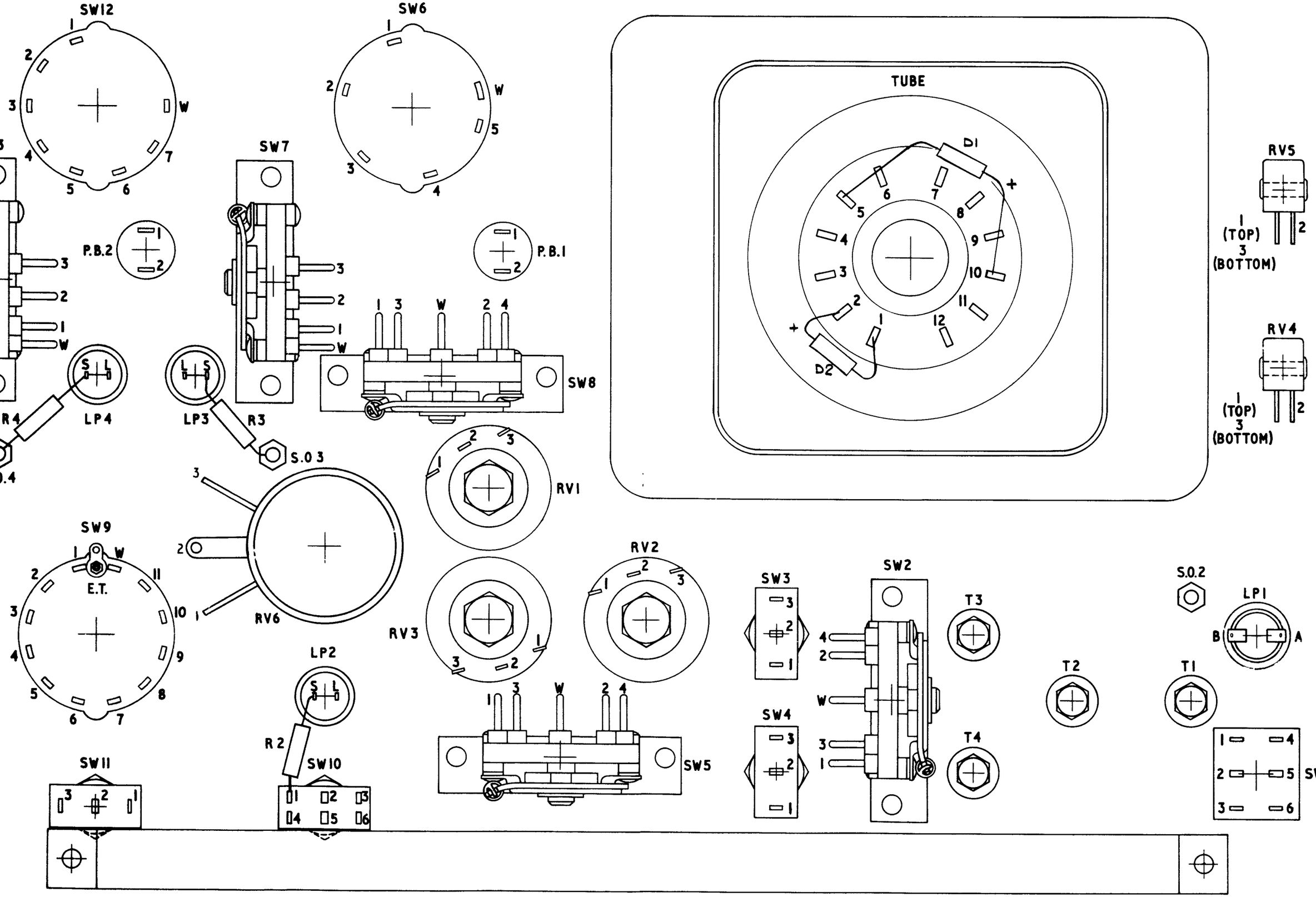
REAR & SIDE PANEL COMPONENT ASS'Y. TYPES 1A & 2A

FIG. 22



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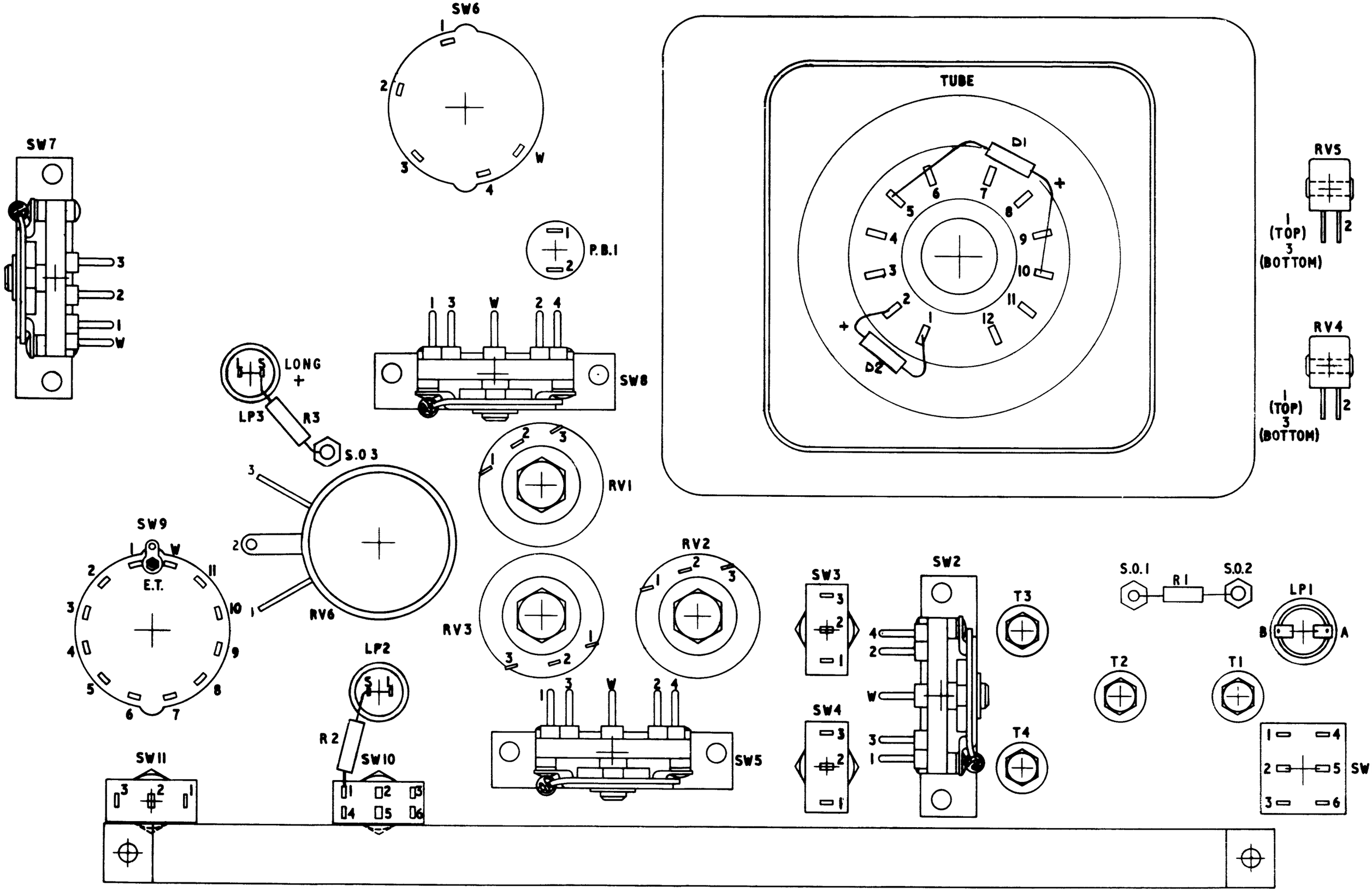
REAR VIEW - FRONT PANEL (TYPE 1A)

FIG. 23A .



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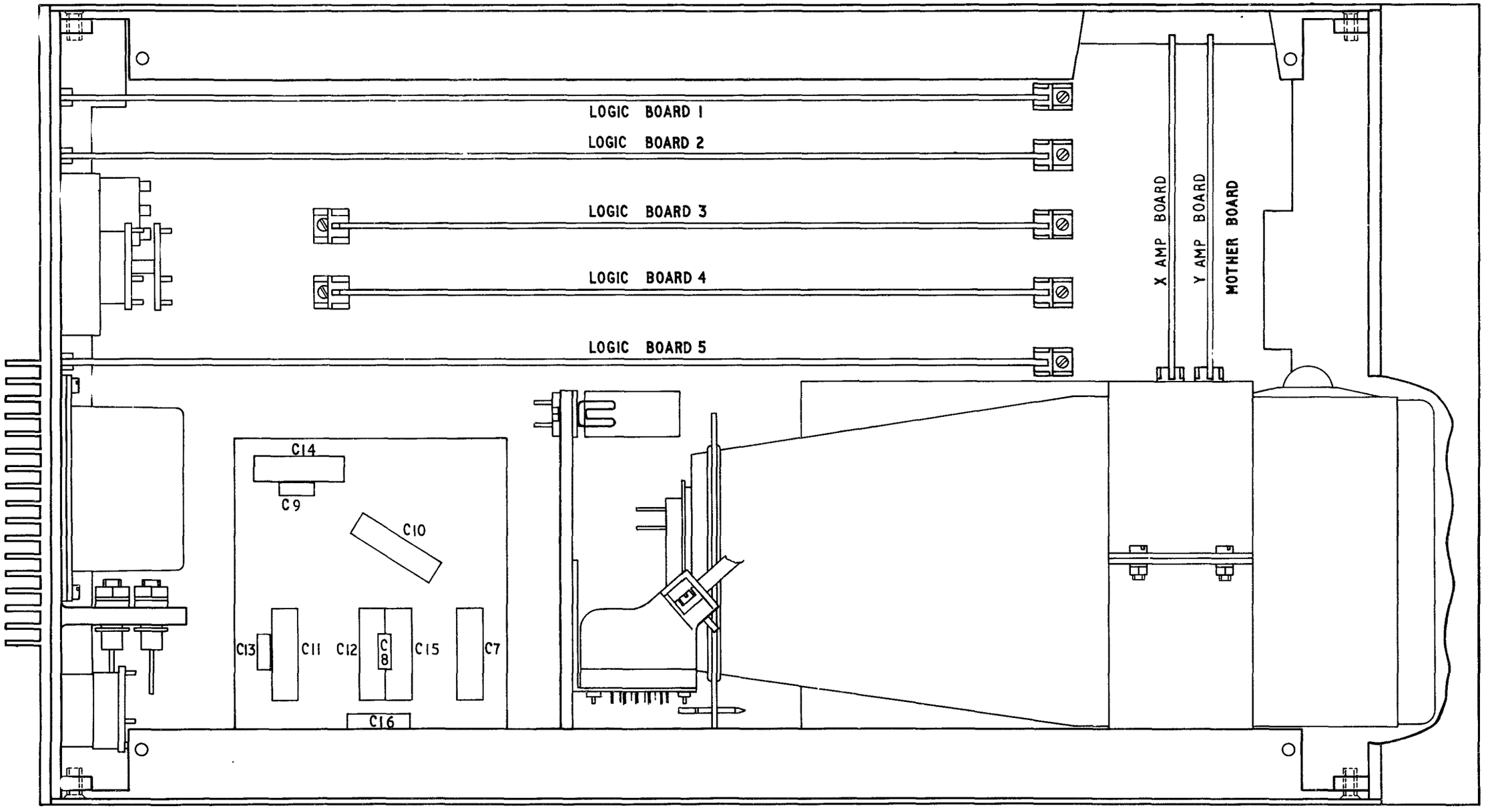
REAR VIEW - FRONT PANEL (TYPE 2A)

FIG. 23B .

VIEW FROM TOP WITH LID REMOVED.

NOTE:- LOGIC BOARDS 4 & 5 NOT FITTED ON TYPE II.



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GENERAL ASS'Y.

FIG.24