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Colin Hinson

In the village of Blunham, Bedfordshire.

**AP 116E-0277-16**

(December 76)



**DRIVE UNITS, RADIO  
(RACAL MA. 1720 SERIES)**

**TECHNICAL AND REPAIR INFORMATION**

**BY COMMAND OF THE DEFENCE COUNCIL**

**Ministry of Defence**

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## NOTE TO READERS

This Air Publication gives detailed information on the MA. 1720 series of transmitter drive units which are used in a variety of operational circumstances. All variants may be operated locally by means of the front panel controls. Provision is also made for remote-controlled operation from external equipment. For details of the external connections required for a particular configuration reference should be made to the relevant Associated Publications as listed below.

## LIST OF ASSOCIATED PUBLICATIONS

AP 116E-0276-16A and 16B UK/FRT 625 10 kW HF Linear Amplifier (Racal Type TA 1800A).



# WARNINGS

CONTROL OF SUBSTANCES HAZARDOUS TO HEALTH

MAKE SURE YOU KNOW THE SAFETY PRECAUTIONS AND FIRST AID  
INSTRUCTIONS BEFORE YOU USE A HAZARDOUS SUBSTANCE

READ THE LABEL ON THE CONTAINER IN WHICH THE SUBSTANCE IS SUPPLIED

READ THE DATA SHEET APPLICABLE TO THE SUBSTANCE

OBEY THE LOCAL ORDERS AND REGULATIONS

## WARNINGS

(1) LETHAL VOLTAGE. DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT.  
REFER TO JSP 375 VOL2 AND DEFSTAN 61-15 ISS 3.

## MODIFICATION RECORD

This publication is technically up-to-date in respect of the modifications listed below.

<u>Mod. No.</u>	<u>Strike No.</u>	<u>L.R.U.</u>	<u>Brief description</u>
A6641	3 (1720A)	-	Removal of resistors.
A7536	3 (1720S)	-	Change in capacitor value
A7621	4 (1720S)	-	Capacitor added
A7649	5 (1720S)	-	Change of resistor value
A7885	6 (1720S)	-	New front panel
A8932	16 (1720S)	-	Change out-of-lock stage
A9598	18 (1720S) 7 (1720A)	-	Change of resistor values
A9912	19 (1720S) 8 (1720A)	-	Addition of Diode 1N4002

## LEADING PARTICULARS

## DRIVE UNIT, TRANSMITTER 10D/5820-99-624-5395 (MA. 1720A).

Function ... ..	The drive unit is a solid-state equipment which provides a low-level modulated r.f. output to the linear amplifier stages of the h.f. communications transmitter. Carrier frequency generation is by means of an in-built synthesizer.
Frequency range ... ..	1.600 MHz to 29.999 MHz in 100Hz steps.
Frequency stability ... ..	With internal frequency standard (Racal type 9400).  (1) $\pm 1$ part in $10^8/^\circ\text{C}$ over temperature range $-10^\circ\text{C}$ to $+55^\circ\text{C}$ .  (2) Long term stability: $\pm 5$ parts in $10^9$ over any 24-hour period after 30 days.  Provision is also made for the use of an external frequency standard.
Modes of emission ... ..	U.S.B./L.S.B. (A3J, A3A), compatible A.M. (A3H), I.S.B. (A3B), C.W. (A1), M.C.W. (A2H, A2J).
Carrier suppression ... ..	Selection by front-panel control for -6 dB, -16 dB, -26 dB, -50 dB (suppressed).
R.F. power output ... ..	25mW to 200mW into 50 ohms, by pre-set adjustment.
Intermodulation products ... ..	Better than -50 dB relative to either one of two equal tones in a standard two-tone test.
C.W./M.C.W. Keying input ... ..	Operation by closed loop. A2J or A2H emission achieved by internally generated 1000 Hz tone in selected sideband.
Keying speed ... ..	200 bauds max.
Hum ... ..	-50 dB relative to p.e.p.
Spurious emissions (single frequency) ... ..	Better than -50 dB relative to p.e.p.
Harmonic radiation ... ..	Better than -30 dB relative to p.e.p.

Unwanted sideband suppression		Better than -50 dB relative to p.e.p.
In band noise	... ..	-50 dB relative to p.e.p. in a 3.0 kHz bandwidth.
Wideband noise	... ..	-100 dB relative to p.e.p. in a 3.0 kHz bandwidth.
Muting	... ..	Better than -70 dB relative to p.e.p. in a 3.0 kHz bandwidth.
Audio input level	... ..	-30 dBm to +10 dBm into 600 ohms by pre-set adjustment. Carbon or specified dynamic microphone.
A.F. response	... ..	Within 4 dB from 300 Hz to 3000 Hz relative to peak response.
Audio a.g.c.	... ..	An audio input variation of $\pm 10$ dB relative input signal between -20 dBm and 0 dBm, will produce a change in output level of less than 2 dB.
Power supply	... ..	100-125V or 200-250V, 45-65 Hz, single phase.
Power consumption	... ..	70 VA nominal.
Dimensions	... ..	Height                      Width                      Depth 178                              483                              508 mm
Weight	... ..	19.5 kg

## DRIVE UNIT, TRANSMITTER 10D/5820-99-631-8611 (MA. 1720S)

The leading particulars given on the previous prelim. pages apply to this variant except for the following:-

Frequency stability	... ..	With internal frequency standard (Racal type 9420).  (1) $\pm 6$ parts in $10^{10}/^{\circ}\text{C}$ over temperature range $-10^{\circ}\text{C}$ to $+55^{\circ}\text{C}$ .  (2) Long term stability: $\pm 5$ parts in $10^{10}$ over any 24-hour period after 30 days.  Provision is also made for the use of an external frequency standard.
A.F. response	... ..	Within 4 dB from 300 Hz to 3400 Hz relative to peak response.

## APPENDIX 1

## MA 1720B AND RTTY FACILITY

AP 116E-0277-16 was published for use with Transmitter Drive Units MA 1720A & S. These units were not fitted with the RTTY Generator Board PS 568. Since publication of the A.P. the Drive Unit MA 1720B has entered service and is fitted with the PS 568 and provides an RTTY facility. The MA 1720A's in service are now also being modified (Mod TC 0080) to provide an RTTY facility by addition of PS 568.

This Appendix provides details of the RTTY facility, it also reflects the current build state of in service MA 1720B's.

## TRANSMITTER DRIVE UNIT

MA1720 B

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TECHNICAL SPECIFICATION

## Parameters

Frequency:	1 to 29.9999MHz in 100Hz steps.
Frequency Stability and Accuracy:	Standard version (Racal Fast warm-up type 9400): (a) Frequency variation with temperature: $\pm 1 : 1:10^8/\text{°C}$ over temperature range $-10\text{°C}$ to $+60\text{°C}$ . (b) Ageing: $\pm 5 : 10^9$ over any 24 hour period, after 30 days. Optional version (Racal Type 9420): (a) Frequency variation with temperature: $\pm 6 : 10^{10}/\text{°C}$ over temperature range $-10\text{°C}$ to $+60\text{°C}$ . (b) Ageing: $\pm 5 : 10^{10}$ over any 24 hour period, after 30 days. Provision is made for the use of an external frequency standard.
Modes of Emission:	USB/LSB (A3A, A3J) Compatible AM (A3H) ISB (A3B) MCW (A2H, A2J in USB or LSB) CW (A2J in LSB) Optional: RTTY (F1) (tone shift keying in selected sideband).
Power Output:	200mW max. into 50 ohm load. Power variation not more than $\pm 1\text{dB}$ over the frequency range. Power output is adjustable between 25mW and 200mW.
Carrier Suppression:	The carrier levels related to modes (and relative to p.e.p.) are:- (a) $-6\text{dB} \pm 1\text{dB}$ (A3H) (b) $-16\text{dB} \pm 1\text{dB}$ (A3A) (c) $-26\text{dB} \pm 1\text{dB}$ (A3A) (d) Not less than $-40\text{dB}$ (A3J) (e) Tune $-6\text{dB} \pm 1 \text{dB}$ (preset)
Unwanted Sideband Suppression:	$-50\text{dB}$ relative to p.e.p.



Audio Input Level: -30dB to +10dBm into 600 ohm balanced, by preset adjustment.

Audio AGC: An audio input variation of  $\pm 10$ dB relative to an input signal between -20dBm and 0dBm produces a change in output level not greater than 2dB.

AF Response: Standard: Not greater than 4dB below peak response from 300Hz to 3000Hz.  
Optional: Not greater than 4dB below peak response from 300Hz to 6kHz.

Intermodulation Products: Better than -50dB relative to either one of two equal tones in a standard two-tone test.

Hum: Better than -50dB relative to p.e.p. in one sideband.

Single Frequency Spurious Emissions: Better than -53dB relative to p.e.p.

Harmonic Radiation: Better than -30dB relative to p.e.p.

Inband Noise: Better than -50dB relative to p.e.p. in a 3kHz bandwidth.

Wideband Noise: Better than -100dB relative to p.e.p. in a 3kHz bandwidth 500kHz off tune.

Mute: Better than -70dB below p.e.p. in a 3kHz bandwidth.

RTTY Keying Input: Single current (neutral/positive) or neutral/negative) or double current (polar), from external 5V supply. Input impedance approximately 500 ohms.

Frequency Shift: 85Hz to 850Hz by preset adjustment, centred on 2kHz offset from the nominal carrier frequency. Centre frequency stability is within 2% of total frequency deviation.

Telegraph Distortion: Not greater than 5%.

CW/MCW/Keying Input: Operation by contact closure.

CW/RTTY Keying Rate: 200 bauds maximum.

CW On/Off Ratio: Better than -55dB relative to p.e.p.

Extended Control: Maximum operating loop impedance 200 ohms.

Meters: A meter is provided on the front panel to indicate line inputs, input setting levels, RF output and internal supply voltages.

Terminations:	Front Panel:	<p>Two sockets for audio input, microphone inputs or monitoring.</p> <p>Connector for test equipment to monitor RF output.</p>
	Rear Panel:	<p>Supply input with voltage selector panel.</p> <p>Two audio inputs.</p> <p>Keying input. Loop keying connections.</p> <p>RTTY input.</p> <p>RF output.</p> <p>External frequency standard input.</p> <p>Extended and remote control connectors.</p> <p>Receiver muting and/or antenna switching from two sets of contacts on internal relay.</p> <p>Receiver input for monitoring purposes.</p> <p>Amplifier control (Supply On, Coarse Tune Initiate, Ready, Mute, Reduced Power, Reset/Fault).</p> <p>Earth Connection.</p>
Controls:	(1) Supply:	Push button, illuminated when power ON.
	(2) Standby:	Push button, illuminated when ON.
	(3) EHT/Ready:	Push button, illuminated when associated amplifier is READY.
	(4) Reset/Fault:	Push button, illuminated when drive unit is out of lock or amplifier fails.
Frequency Setting:		6 digit thumbwheel selector switch. (Local Control)

Tune/Mute/  
Operate Switch: Tune - Supplies a pre-set carrier level for tuning

Mute - Mutes drive unit and associated amplifier

Operate Low: Low Power, approx. 6dB below p.e.p. by adjustable internal preset control.

Operate High: Full Power.

Control Selector  
Switch: Selects: Local Synthesizer = (SYNTH)  
Local Programmer = (PROG)  
Extended = (EXT)  
Remote = (REMOTE)

Mode Selector Switch: Switch: SSB, -6dB, -16dB, -26dB, suppressed carrier.

ISB, -6dB or -26dB carrier.

Key, -6dB or suppressed carrier.

AM -6dB carrier.

RTTY Test - Selects 'Mark'

RTTY - Tone Shift Keying

CW - Selects LSB mode with 1kHz keyed tone. Operating frequency manually reset by adding 1kHz on the thumbwheel switch.

Sideband Selector Switch: Selects Upper or Lower Sideband.

VOX/PTT/Transmit Switch: VOX - Automatic Voice Switching.

PTT - Press to talk.

Transmit - Continuous transmission.

Meter Switch: Measure Line input levels, setting line amplifier levels, RF output and internal supply voltages.

Line Input Levels: Two front panel preset controls for setting audio input to the centre of the AGC control range.

Indicator Lamps:                   Supply ON     )  
   ) Drive Unit  
   In-Lock     )  
  
   Standby        )  
   )                )  
   Ready           ) From associated Amplifier  
   )                )  
   Reduced Power   )  
   )                )  
   Reset/Fault    )

Power Supplies:                   100 - 125V a.c.  
  
   or   200 - 250V a.c.  
  
   45 - 60 Hz

Consumption 70VA approximately.

Control Facilities:               Local  
   Extended via multicore cable and the MA1040  
   Remote Control Panel.  
   When used with the MA1038 Pre-programmed  
   Selector the MA1720 may be operated on any  
   one of six (MA1038A) or ten (MA1038B) pre-  
   selected channels.

Remote via suitable remote control system  
   e.g. Racal MA1722/MA.1085/MA1040 or  
   MA1722/MA1090. For remote control of the  
   MA1720/MA1038 the LA1517/LA.1518 10 channel  
   sequential tone system is used.

Dimensions:                       Height:               178mm (7in)  
   Width:               483mm (19in)  
   Depth:               508mm (20in)  
   Weight:               19.5kg (42.91b)

Environment:                       Temperature Operating - 10°C to +55°C  
   Temperature Storage - 40°C to +70°C  
   Relative Humidity 95% at +40°C

The equipment is suitable for air  
   transportation in unpressurised conditions  
   and for operation at altitudes of 3000  
   metres above sea level; it is also suitable  
   for transportable and maritime mobile  
   operation and meets certain clauses of  
   British Defence Specification DEF 133 Table  
   L2. In general the parameters in this  
   specification are measured in accordance  
   with CCIR and IEC recommendations.

VARIANTS OF TRANSMITTER DRIVE UNIT MA1720

The following details describe briefly the differences between the various types of MA1720.

- MA1720A: Standard version Transmitter Drive Unit. Synthesized 1MHz to 30MHz in 100Hz steps, USB/LSB (A3A, A3H, A3J), ISB (A3B), compatible AM (A3H), MCW (A2H, A2J), CW (A1). Capable of local (synthesized or pre-programmed), extended and remote control. Includes type 9400 Frequency Standard and 300Hz to 3000Hz filter.
- MA1720B: As MA1720A but with RTTY (F1) included.
- MA1720C: As MA1720A but with 300Hz to 6000Hz filter.
- MA1720D: As MA.1720B but with 300Hz to 6000Hz filter.
- MA1720E: As MA1720A but with Type 9420 Frequency Standard.
- MA1720F: As MA1720B but with Type 9420 Frequency Standard.
- MA1720G: As MA1720C but with Type 9420 Frequency Standard.
- MA1720H: As MA1720D but with Type 9420 Frequency Standard.
- MA1720L: As MA1720A but with 300 - 6000Hz filter and RTTY (F1), and less frequency standard.
- MA1720M: As MA1720A but with marine 2.7kHz USB filter, and less audio AGC.
- MA1720S: As MA1720A but with Type 9420 Frequency Standard and 300Hz to 3400Hz filter.

ACCESSORIES

AA650/B           Fist microphone, carbon insert, with pressel switch.  
Lead terminated with Rendar plug type R41101.

AA651/B           Handset, carbon microphone, EM receiver (300ohm), with  
pressel switch. Lead terminated with Rendar plug type  
R41101.

AA652/A           Stowage bracket for AA650B fist microphone.

AA652/B           Stowage bracket for AA651/B handset.

AA653/B           Desk microphone, carbon insert, with pressel switch.  
Lead terminated with Rendar plug type R41101.

AA655/A           Boom microphone and headset, EM inserts, with pressel  
switch and lapel clip. Lead terminated with Rendar plug  
type R41101.

AA660/C           Headset, 600 ohm, with lead terminated with Rendar plug  
type R41101.

AA670/D           GNT morse key. Lead terminated with Rendar plug type  
R41101.

AA671/C           Miniature morse key with knee strap. Lead terminated  
with Rendar plug type R41101.

## Chapter 1

## FUNCTIONAL DESCRIPTION

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## INTRODUCTION

1. The purpose of the drive unit MA.1720 (fig.1) is to provide a low-level (25mW to 200mW) modulated r.f. output in the frequency range 1.6 to 30MHz (nom.). The internally-generated carrier frequency is produced by a synthesizer which is locked to a high-stability 5MHz standard frequency source. The carrier frequency is selected by six thumbwheel switches (front-panel) which enable selection to be made in 100Hz steps over the frequency range 1.6000MHz to 29.9999MHz. Note that the switch selecting the most significant digit cannot be set to any digit above '2'.

## FACILITIES

2. Two variants of the drive unit are presently in Service use; the differences are detailed in para.71. The facilities provided by these variants are described below. Note that since the circuits for f.s.k. operation are not fitted, the RTTY and RTTY TEST positions of the front-panel mode switch are inoperative.

### Operational modes

3. (1) Single sideband (upper or lower) with either -16dB, -26dB or fully-suppressed carrier.
- (2) Independent sideband with either -16dB or -26dB carrier.
- (3) Keyed tone with either -6dB or fully suppressed carrier.
- (4) Compatible a.m. with -6dB carrier.
- (5) C.W. (lower sideband) with 1kHz keyed tone.
- (6) VOX
- (7) P.T.T. : press-to-talk.
- (8) Transmit : continuous transmission.

4. The VOX facility is available on the Line 1 audio input, and enables two-way conversation to be carried out without manual switching. Provision is also made for muting an associated receiver.



Monitoring

5. The front-panel jack sockets, LINE 1 (u.s.b.) and LINE 2 (l.s.b.), enable the audio line inputs to the drive unit to be monitored using high-impedance headphones. Contacts are also provided on LINE 1 jack for a press-to-talk, sidetone output, and connection of an output from an associated receiver.

Inputs

6. Rear panel connectors provide for connection of two 600-ohm balanced line inputs and telegraph keying inputs. The 600-ohm balanced audio inputs may vary between -30dBm and +10dBm (relative to 1mW); two front-panel preset controls enable the input level to be set to the centre of the a.g.c. range.

7. The signal input socket SK9, which is mounted on the rear panel, provides monitor facilities for audio 1 and audio 2 inputs and the audio output from an associated receiver. The associated receiver output may also be monitored at terminal strip TS1 at the rear of the unit.

8. An r.f. monitor socket mounted on the front panel permits connection of test equipment to monitor the r.f. output of the drive unit.

Metering

9. A front panel meter is used, in conjunction with a meter switch, to indicate the line input levels, line input setting levels, the internal supply voltages and the r.f. output level. A green band on the meter scale indicates the correct setting for audio levels and internal supply voltages.

Extended/remote control

10. Ancillary units are required to provide the facilities selected by the following three positions of the front-panel LOCAL/EXTENDED/REMOTE switch:-

- (1) LOCAL (PROG): pre-selection of channel operation frequency.
- (2) EXTENDED: local extended control of transmitter.
- (3) REMOTE: control of transmitter extended to a remote site via telephone cables or radio link.

Frequency standard

11. The internal 5MHz reference signal for the synthesizer is provided by a crystal-controlled oscillator which is housed in a fast warm-up oven.

12. A facility is also provided (on the rear of the unit) for connecting and switching to an external 5MHz standard frequency source.

## CONSTRUCTION

13. The unit is housed in a cast alloy chassis which is compartmented (fig.2 and 3) to provide screening between assemblies liable to mutual interference. Printed-circuit boards are mounted on either side of the chassis.

14. Access is gained to assemblies mounted on the top of the chassis by removing the top panel which is secured by screws to the side and rear panels. Assemblies mounted on the underside of the chassis are protected by individual lids which afford easy access to each assembly; all printed-circuit boards are wired-in and, with the exception of the mixer and output board, may be hinged outwards for servicing purposes.

15. The front, side and rear panels are all constructed of steel; the rear panel carries the heat sinks for the power transistors. The front panel is connected to the main cableform via two multi-pin connectors and may be completely detached from the chassis for test purposes.

16. To facilitate cooling, slots in the chassis, the top cover, and compartment lids allow air to flow freely throughout the unit.

## BRIEF FUNCTIONAL DESCRIPTION

17. Referring to the simplified block diagram (fig.4) of the drive unit, the main functions are each covered on a printed-circuit board, and are as follows:

(1) Low-level board: audio and keying inputs are set-up prior to being applied to balanced modulators; a 1.4 MHz sub-carrier is applied to the modulator and also used for carrier re-insertion purposes.

(2) Mixer and output board: the modulated 1.4 MHz output from the low-level board is passed through two stages of mixing and amplification to provide a 25mW to 200mW r.f. output.

(3) Three synthesizer boards and 34 MHz generator board: the 1.4 MHz sub-carrier and the local-oscillator voltages for the two mixers are produced by the synthesizer.

(4) Control board: contains solid-state switches, initiated by front-panel controls, which select operational modes.

(5) Power supply board: this board, in conjunction with the main chassis-mounted components e.g. mains transformer, produces four low-level, positive, d.c. supply voltages.

## A.F. and r.f. stages (fig.4)

18. The principle of operation of the drive unit is apparent from an examination of fig.4.

19. The modulating input signals are applied to the balanced modulator via the automatic gain control amplifiers. The outputs of the a.g.c. amplifiers are switched by reed relays which are controlled by the setting of the front panel mode selector switch in the s.s.b./i.s.b. modes; channel 1 input is used to generate the s.s.b. upper or lower sideband whilst channel 2 input is used to generate the lower sideband in the i.s.b. mode.

20. The audio outputs from the a.g.c. amplifiers are mixed, in the balanced modulators, with the 1.4 MHz output from the frequency synthesizer; the required sidebands are obtained by filtering. The suppressed carrier output from balanced modulator 1 is applied to the l.s.b. filter and the output from balanced modulator 2 is applied to the u.s.b. filter, to compensate for a sideband inversion (para.7) which occurs in the final mixer.

21. The 1.4 MHz signal from the synthesizer is also applied to a carrier re-insertion stage where it is attenuated by 6, 16 or 26dB (suppressed carrier greater than -40dB), dependent upon the mode of emission selected. A summing amplifier adds the s.s.b. or i.s.b. signals to the carrier and the resultant signal is mixed with the 34 MHz output from the synthesizer to produce an i.f. of 35.4 MHz. The 35.4 MHz i.f. signal is finally mixed with the 36.4 to 65.4 MHz output from the synthesizer to produce the 1 to 30 MHz r.f. output.

### Synthesizer

25. Figure 5 shows that the synthesizer produces the following three outputs:

- (1) 36.4 to 65.4 MHz as the final mixer injection frequency.
- (2) 34 MHz for injection into the first mixer.
- (3) 1.4 MHz for injection into the balanced modulators and the carrier re-insertion.

26. The indirect method of frequency synthesis is used where the required output frequencies (with the exception of the 1.4 MHz output) are derived from voltage-controlled oscillators which are phase-locked to an input frequency derived from the 5 MHz standard frequency source. Algebraic equations, for calculating each loop oscillator frequency, are given in para. 39 to 43.

27. 34 MHz generator. The 5 MHz signal is divided by five, on the 34 MHz generator board, and the 1 MHz output fed to the l.f. loop board. This 1 MHz signal is also applied to a phase-locked loop containing a 34 MHz v.c.o. the output from which is fed via a band-pass filter to the first mixer on the mixer and output board (fig.4).

28. L.F. loop. This generates the kHz part of the synthesizer output frequency. The low-frequency loop consists of an 18 to 23 MHz v.c.o., a programmed divider, N1, and a phase-comparator. The phase-comparator compares the phase of the output signal from the programmed divider with that of a 500 Hz reference frequency derived from the frequency standard. Should a phase difference exist, a correction voltage is derived which is fed back to the v.c.o. to eliminate the error.

29. The programmed divider, N1, has a variable division ratio in the range 36001 to 46000, and is controlled by the 100 Hz, 1 kHz, 10 kHz and 100 kHz frequency selector switches. A frequency setting of 9999 sets the division ratio to 36001; a setting of 0000 sets the division ratio to 46000; the division ratio for intermediate frequency settings is given by the expression  $N1 = 46000$  minus the setting of the above four frequency selector switches.

30. The programmed divider N1 is a reversible decade counter programmed to commence a counting sequence at a point dependent on the setting of the four selector switches; a reset operation takes place when the 'count' reaches 46000.

31. Consider a frequency setting of 12.3456 MHz; the required final mixer injection frequency is 12.3456 MHz plus 35.4 MHz i.e. 47.7456 MHz. Ignoring the MHz part of this frequency, the divider N1 is preset to start a counting sequence and count up to 46000; the v.c.o. output frequency for these switch settings is N1 times the input reference frequency to the phase-comparator i.e. 21.272 MHz.

32. The 21.272 MHz main output from the v.c.o. is fed via a divide-by-five stage to the transfer loop. Note that the output frequency from the l.f. loop is in the range 3.6 to 4.6 MHz hence, the actual output is 4.2544 MHz.

33. The 1 MHz input to the l.f. loop is divided by five to produce 200 kHz; a 1.4 MHz crystal filter selects the seventh harmonic and this is amplified to produce a 1.4 MHz injection signal for the balanced modulators.

34. Transfer loop. This loop, in conjunction with the h.f. loop, generates the MHz portion of the output frequency. It consists of a programmed divider, N2, a phase comparator, a mixer and a v.c.o. (h.f. loop board) which covers the frequency range 885 to 947.8 kHz.

35. The programmed divider, N2, has a division ratio from 40 to 69. In contrast to the previously described programmed divider N1, the division ratio of N2 is found by adding 40 to the setting of the MHz switch. This is achieved by first converting the decimal 0 to 29 into a 'nines complement' code before application to the programmed divider which counts from the programmed starting point up to 99, and then to 39 when the reset occurs. Table 1 gives the conversion from decimal to nines-complement code.

TABLE 1  
Decimal to nines-complement b.c.d. conversion

Decimal	BCD				Nines complement				Decimal
	D	C	B	A	D9	C9	B9	A9	
0	0	0	0	0	1	0	0	1	9
1	0	0	0	1	1	0	0	0	8
2	0	0	1	0	0	1	1	1	7
3	0	0	1	1	0	1	1	0	6
4	0	1	0	0	0	1	0	1	5
5	0	1	0	1	0	1	0	0	4
6	0	1	1	0	0	0	1	1	3
7	0	1	1	1	0	0	1	0	2
8	1	0	0	0	0	0	0	1	1
9	1	0	0	1	0	0	0	0	0

36. The output from the l.f. loop is divided by N2 and is then applied as one input of a phase-comparator. The output from the v.c.o. is mixed with the 1 MHz reference frequency, derived from the frequency standard, and the difference frequency output from the mixer is applied as the second input to the phase-comparator. Thus the output voltage from the phase-comparator drives the v.c.o. to a frequency which is equal to 1 MHz minus the output frequency from the programmed divider, N2.

37. The division ratio for the programmed divider, N2, is obtained by adding 40 to the MHz digits of the output frequency. Thus for a frequency of 12.3456 MHz, N2 will be 40 plus 12 which equals 52. The 4.2544 MHz output from the l.f. loop (para.31) is divided by 52 and the result is then subtracted from 1 MHz to give the transfer loop output frequency.

$$\begin{aligned} \text{Transfer loop output} &= 1 - \frac{4.2544}{52} \text{ MHz} \\ &= 1 - 0.081815 \text{ MHz} \\ &= 918.185 \text{ kHz} \end{aligned}$$

38. H.F. loop. As stated in para.10, the v.c.o. for the transfer loop is on the h.f. loop board. The output from this v.c.o. is fed via a divide-by-two stage to the h.f. loop containing a programmed divider N2 with the same range of division ratios as for the transfer loop. The output from this loop, which also contains a further divide-by-two stage, is 2N2 times the input frequency to the phase comparator. Hence, the output from the v.c.o. is:

$$\begin{aligned} &918.185/2 \times 2 \times N2 \\ &= 47.7456 \text{ MHz (para.31)} \end{aligned}$$

39. Loop equations. The variable output frequency from the synthesizer may be worked out for any frequency setting by using a simple algebraic equation. The following paragraphs show the derivation of this equation.

40. The 1 MHz reference frequency input to the low-frequency loop, designated f1, is expressed as:  $f1 = 10^6$  Hz. The output from the l.f. loop (f2) is therefore:

$$f2 = \frac{10^6}{5 \times 400} \times N1 \times \frac{1}{5} \text{ Hz} \dots\dots\dots (1)$$

41. The input to the transfer loop (equation (1)) is initially divided by N2 before being applied to the transfer loop; hence the input to the phase-comparator is:

$$\begin{aligned} f2 &= \frac{10^6}{5 \times 400} \times \frac{N1}{N2} \times \frac{1}{5} \text{ Hz} \\ &= \frac{10^6}{10^4} \times \frac{N1}{N2} \text{ Hz} \\ &= 100 \times \frac{N1}{N2} \text{ Hz} \dots\dots\dots (2) \end{aligned}$$

The transfer loop inverts the frequency range of equations (2) and subtracts it from 1 MHz; the output from the v.c.o. is:

$$f3 = 10^6 - 100 \times \frac{N1}{N2} \text{ Hz} \dots\dots\dots (3)$$

42. The input to the h.f. loop (equation (3)) is divided by a factor of two and applied to the phase-comparator as:

$$\frac{f_3}{2} = \frac{10^6}{2} - \frac{100}{2} \times \frac{N_1}{N_2} \text{ Hz} \dots\dots\dots (4)$$

The h.f. loop, which also contains a further divide-by-two stage, provides the following output frequency:

$$\begin{aligned} f_4 &= f_3 \times 2 \times N_2 \text{ Hz} \\ &= \frac{10^6 \times 2 \times N_2}{2} - \frac{100}{2} \times \frac{N_1}{N_2} \times 2 \times N_2 \text{ Hz} \\ &= 10^6 N_2 - 100 N_1 \text{ Hz} \dots\dots\dots (5) \end{aligned}$$

43. As shown in fig.5, the division ratios N1 and N2 are evolved as follows:

$$N_1 = 46000 \text{ minus kHz digits} \dots\dots\dots (6)$$

$$N_2 = 40 \text{ plus MHz digits} \dots\dots\dots (7)$$

44. It will be observed that the equation shown on fig.5 symbolizes the input reference frequency to the l.f. (1 MHz) as f1.

DETAILED FUNCTIONAL DESCRIPTION

45. The following description is primarily concerned with:

- (1) the a.f. and keying input paths (fig.6).
- (2) the front-panel and solid-state switching (fig.7).

The complete interconnections for the boards within the drive unit are given on sheets 1, 2 and 3 of fig.8.

A.F. input switching and monitoring (fig.6)

46. The flow-circuit in fig.6 is largely self-explanatory, and traces the path of the a.f. and keying inputs from either the rear connectors or front-panel jack sockets through to the low-level board PM341; the detailed description of the low-level modulation process is contained in Chap.8. Fig.6 also shows the meter monitor circuit and the jack socket monitoring circuits for each input channel; a detailed description of this facility is given in Chap.9.

47. With reference to the jack sockets JK1 and JK2, the following points should be noted:

- (1) the pick-off terminals for the jack plug are those lettered 'a' on the socket diagram.
- (2) when a plug is not inserted, there are no breaks in the audio and keying paths for each channel.
- (3) the keying input is to channel 1 only; however, this input can also be inserted on either JK1 or JK2 at pin 11.
- (4) when a plug is inserted and turned clockwise, the audio (contacts 12) and the keying (contacts 11) line input paths (from rear panel) are broken, and the audio/key input is then derived from the front-panel jack plug. To monitor line inputs without breaking the signal paths to the low-level board, either terminals 2 and 11 (keying input) or 3 and 12 (audio input) must be linked in the jack plug.

- (5) the a.f. output from an associated receiver can be monitored at contact 1a of JK1 only.
- (6) the output from a local microphone or key can be connected at terminal 12 of JK1 or JK2 (a.f.) or terminal 11 of JK1 (key).
- (7) a sidetone signal can be monitored at contact 5 of JK1 or JK2.
- (8) a d.c. supply for a carbon microphone is available at contact 4 of JK1 or JK2.

48. The meter monitoring and setting-up facility utilizes a meter amplifier on the low-level board for the audio lines, and a r.f. detector (not shown) on the mixer and output board for the 200mW r.f. output level measurement. The a.f. meter amplifier circuit is calibrated by R195 on the low-level board. The line input levels are measured in the LINE 1 and 2 positions of the meter switch; these levels are preset by R12 and R11 and measured in the SET 1 and 2 positions of the meter switch.

Front-panel and solid-state switching (fig.7a and 7b)

49. The flow circuit in fig.7 shows all control lines which carry 'command' voltages generated by switches on the front panel; it also shows how these 'command' levels are used, via solid-state switches, to select the mode of operation required from the drive unit.

50. The functions of all pins in the multi-pin connectors on the rear of the drive unit are given in Tables 2 to 5. The facilities used with a particular linear amplifier will be evident from the relevant interconnecting diagram.

TABLE 2

Extended frequency control lines : pin functions on PL3

Pin	Function	Remarks
9	1 )	x 100Hz )
10	2 )	
11	4 )	
12	8 )	
5	1 )	x 1kHz )
6	2 )	
7	4 )	
8	8 )	
1	1 )	x 10kHz )
2	2 )	
3	4 )	
4	8 )	

Inverted B.C.D.

TABLE 2 (cont.)

Pin	Function	Remarks
21	1 )	Inverted B.C.D.
22	2 )	
23	4 ) x 100kHz	
24	8 )	
17	1 )	Inverted Nines - complement B.C.D.
18	2 )	
19	4 ) x 1MHz	
20	8 )	
13	1 )	
16	) x 10MHz	
	8 )	

TABLE 3

Extended/remote control lines : pin functions on SK2

Pin	Function	Pin	Function
1	Not used	20	Not used
2	Not used	21	RTTY
3	I.S.B. control	22	L.S.B. control
4	Not used	23	Low power control
5	High power control	24	-26dB control
6	-16dB control	25	-6dB control
7	Key supp. control	26	Key -6dB control
8	Vox control	27	Not used
9	Extended 'tx' lamp	28	Extended 'e.h.t. on'
10	Extended 'reset'	29	Extended 'standby on'
11	Extended 'tune'	30	Extended 'reset' lamp
12	Extended 'reduced power' lamp	31	Extended 'ready' lamp
13	Extended 'in-lock'	32	Extended mute
14	Remote 'on'	33	Extended 'on'
15	Extended mode control	34	Extended p.t.t.
16	-7V	35	0V
17	+5V	36	+12V
18	+20V	37	Remote p.t.t.
19	Local p.t.t.		



TABLE 4

Status/control lines to linear amplifier : pin functions on SKT6

Pin	Function	Voltage	Action
1		+12V	
2	Fault	0V = fault +12V = normal	Lights the 'reset' lamp and mutes the MA.1720 under fault condition.
3	Ready	0V = ready +12V = not ready	Lights the 'ready' lamp; the absence of the 'ready' signal reverts the output of the MA.1720 to the 'tune' signal.
4	Reset (coarse-tune-initiate)	0V = normal +12V = reset	When the 'reset' button is depressed, the MA.1720 is de-muted and a coarse-tune-initiate signal is applied to the linear amplifier.
5	Reduced power	0V = lamp 'off' +12V = lamp 'on'	Lights 'reduced power' lamp when the linear amplifier is operating on reduced power.
6	E.H.T. 'on'	+12V = 'off' 0V = 'on'	Switches on linear amplifier e.h.t. supplies.
7	Standby	+12V = normal 0V = 'on'	Sets the linear amplifier to 'standby'.
8	Mute	+12V = normal 0V = mute	Mutes linear amplifier.
9	-	0V	Earth
10	Not used		
11	Coarse-tune-initiate (reset)	0V = normal +12V = reset	Sets linear amplifier to the coarse-tune-condition.

TABLE 5

Input signals : pin functions on SKT9 and TS1

Pin		Function	Pin		Function
SKT9	TS1		SKT9	TS1	
1 )	1	Audio 1 input	25	18	Screen for RTTY input
2 )	2		15		Not used
14	3	Screen for audio 1 input	19		Audio 1 monitor (sidetone)
3 )	4	Audio 2 input	20		Screen for audio 1 monitor
4 )	5		21		Audio 2 monitor (sidetone)
16	6	Screen for audio 2 input	22		Screen audio 2 monitor
5	13	KEY input	23	19	0V
17	14	Screen for key input	24	20	+12V
6	15	Audio from receiver			
18	16	Screen for audio from receiver			
7*	7	Normally closed			
8*	8	Relay contacts (change-over)			
9*	9	Normally-open			
10*	10	Normally-closed			
11*	11	Relay contacts (change-over)			
12*	12	Normally-open			
13	17	RTTY input			

\* Pins 7 to 12 are external connections to RLA which is operated when the MA.1720 is muted.

51. Initially, the following description of fig.7 presupposes certain conditions set up on the front panel switches; these conditions are as follows:

- (1) SUPPLY pushbutton released (out) hence lamp extinguished.
- (2) STANDBY pushbutton released (out) hence lamp extinguished.
- (3) EHT pushbutton released (out).
- (4) TUNE/MUTE/OPERATE switch to OPERATE HIGH.
- (5) LOCAL/EXTENDED/REMOTE switch to LOCAL SYNTH.
- (6) SIDEBAND switch to LOWER.
- (7) VOX/P.T.T./TX switch to TX.
- (8) MODE switch to SSB-16.

52. The effect of the remaining positions of the above switches is indicated where appropriate in the following paragraphs. A full description of the PM345 control board is given in Chap.9; fig.7 includes the complete circuit of the PM345.

#### Switching-on

53. When the SUPPLY pushbutton (fig.6) is depressed, the mains input voltage is connected via the voltage selector (rear) to the drive unit power supply (Chap.9) and the low-level d.c. voltages for all the boards in the drive unit are produced.

54. When the STANDBY pushbutton is depressed, a +12V 'command' voltage is applied via SA2F, D2 (front panel) and SF to pin 13 of the control board PM345; this results in a 0V level at pin 14 of the PM345. When the EHT pushbutton is depressed, a +12V 'command' voltage is applied via SA2F, D1 and SG to pin 15 of the PM345; this results in a 0V level at pin 16 of the PM345. These 0V 'commands' are applied via pins 1 and 6 of SKT6 (rear) to switch-on the linear amplifier.

#### Frequency selection

55. It is now assumed that the operating frequency has been selected on the six thumbwheel switches, hence the synthesizer will have gone out-of-lock and then re-locked (IN-LOCK lamp glowing). The effect of the synthesizer momentarily going out-of-lock is to produce a sharp-edged negative-going pulse (logic '0') at pin 9 of G4 (PM345); this causes the latch stage G3/G4 to trip and produce a logic '1' at pin 11 of ML2. This results in the following:

- (1) The output of G9 (ML1) changes from logic '0' to logic '1'.
- (2) The level at pin 5 (PM345) changes from +12V (nom.) to 0V (nom.).
- (3) The RESET lamp glows because TR6 conducts.
- (4) The IN-LOCK lamp is momentarily extinguished because TR4 momentarily conducts.

The 0V 'command' at pin 5 (PM345) is applied to pin 12 of the mixer and output board PM342 (Chap.8) to mute the r.f. output from the drive unit; this 0V 'command' is also applied via pin 8 of SKT6 to mute the linear amplifier and hence minimise the radiation of noise during a frequency changing action.

56. After the RESET button has been operated, the linear amplifier applies a 'not ready' command, via pin 3 of SKT6 (rear) to pin 8 (PM345). This +12V command, via TR13 and TR14 (PM345), produces a 'tune' voltage (+12V) at pin 11 (PM345) which is routed to pin 27 (PM341) and produces the following actions:

- (1) The channel 1 audio path (PM341) is muted, via D28, D12 and R21, by TR1.
- (2) The 1.4MHz carrier is re-inserted, via D29, D41 and R166, by TR49.
- (3) The 1.4MHz re-inserted carrier is attenuated to the 'tune' level, via D29 and R220, by TR61.
- (4) The full-power attenuator, for the 1.4MHz output, is switched in, via D29, D51 and R215, by TR58.
- (5) The low-power attenuator, for the 1.4MHz output, is inhibited, via D29 and R209, by TR59 and TR56.
- (6) The READY lamp is extinguished via pin 10 (PM345).

57. The presence of the 'not ready' +12V command at pin 3 of SKT6 also results in an open-circuit, via TR13, TR14, TR17 and TR16, at pin 12 (PM345); this open-circuit is applied via pin 8 of PL1 (front panel) and SA1B to the wipers of the MODE switch SB. Hence, the MODE switch has no 'command' voltage (+12V) at its wipers and, therefore, cannot institute mode changes.

#### Reset operation

58. Until the RESET pushbutton is depressed, the linear amplifier remains in the state described in para.55 to 57. When the RESET switch is depressed a -12V 'command' is applied, via SA2F, D3, switch SE (RESET) and pin 3 of PL1 on the front-panel, to pin 29 (PM345); this results in the following actions:

- (1) A +12V coarse-tune-initiate command is applied, via TR2, TR1 and pin 30 of the PM345, to the linear amplifier.
- (2) The monostable ML4 is triggered, via TR2 and G1 (ML2), for 2 seconds to produce a logic '0' output which resets the latch G2/G3 in ML2 (para.55). Hence, the level at pin 11 of G5 (ML2) reverts to logic '0' which, via G7, G9, TR9 and pin 5 results in a logic '1' being applied to pin 5 (PM342) and the muting 'command' being removed from the drive unit output stage. Hence, the linear amplifier is now fed with an attenuated 1.4MHz 'tune' signal, and commences the coarse-tune action.
- (3) The RESET lamp is extinguished by TR6.

59. When the linear amplifier has completed its tuning process, a 'ready' command (0V) is fed back to pin 3 of SKT6 (rear of drive unit). This is applied to pin 8 (PM345) and results in the following actions:

- (1) A 0V command, via TR13 and TR14, appears at pin 11 (PM345) which cancels the 'tune' condition; hence, the states described in (1) to (6) of para.56 are reversed.
- (2) A +12V level, via TR13, TR14, TR17, TR16 and pin 12 (PM345) is applied to pin 8 of PL1 (front panel); hence, the MODE switch now has the 'command' level necessary to institute mode changes (para.57) if required.

60. The READY lamp is now glowing and the transmitter is operational for the frequency and mode previously selected.

Mode selection

61. For the lower-sideband SSB-16 mode previously selected (para.51), the following occurs:

- (1) Switch wafer SB1F (front panel) applies a +12V command, via pin 17 (SKT1) and pin 23 (PM341), which results in the following:
  - (a) The 1.4 MHz carrier re-insertion amplifier TR51 being switched on by TR49/TR50/TR52 via D43, D37 and R166.
  - (b) The 1.4 MHz, -16dB attenuation stage TR60 being activated via D43 and R216.
  - (c) The channel 1 audio attenuator TR32 being activated via D43 and R116.
  - (d) The channel 2 audio attenuator TR30 being activated via D43 and R115; this channel is not used in s.s.b. mode.
- (2) Switch wafer SB2F open-circuits the +12V command, via pin 33 of PL1, which is reconnected by the SIDEBAND switch (SL) in the LSB position; hence the +12V command is routed via pin 33 of PL1 to pin 30 (PM345) to energize the relay RLA/1. Contact RLA1 changes over to route the channel 1 audio input into the u.s.b. modulator and filter path; a subsequent frequency inversion (PM342) inverts the signal into the l.s.b. path.

62. The effect of a mode change is as follows. Assume that ISB-26 is selected by the MODE switch SB; the operation of the SIDEBAND switch SL becomes ineffective. Switch wafer SB2F applies a +12V command, via pin 18 of SKT1 (front-panel) to pin 29 (PM341) which has the following affects:

- (1) The i.s.b. switching relay RLB/1 (PM341) is energized via D31, R92, TR31; hence the audio channels 1 and 2 are switched to the l.s.b. and u.s.b. modulators respectively.
- (2) The channel 1 audio attenuator TR28 is activated via D31, D26 and R91.

63. Switch wafer SB1F applies a +12V command, via pin 35 of SKT1 (front-panel), to pin 20 (PM341) which has the following affects:

- (1) The 1.4 MHz carrier re-insertion amplifier TR51 is switched on by TR49/TR50/TR52 via D44, D40 and R116.
- (2) The 1.4 MHz, -26dB attenuation stage TR53 is activated via D44 and R200.

64. If the MODE switch SB is set to CW, and LSB is still selected by the SIDEBAND switch, wafer SB2F applies a +12V command, via pin 33 of PL1 (front panel) to pin 30 (PM341); this energizes the l.s.b. switching relay RLA/1 (PM341). Contact RLA1 routes the channel 1 audio signal to the u.s.b. modulator. Switch wafer SB1F applies a +12V command, via pin 34 of SKT1 (front panel), to pin 46 (PM341) with the following affects:

- (1) The 1 kHz tone oscillator is switched on, via D3 and R24, by TR9 and TR14 (PM341).
- (2) The a.g.c. input amplifier of audio channel 1 is turned 'off', via D3, D18, D12 and R21 by TR1 (PM341).

65. The mute-delay stage on the PM341 board provides a 0V output, until a key is depressed, which is routed from pin 47 (PM341) to pin 21 (PM345); the key contacts are connected to pins 44 and 43 of the PM341 board. This 0V signal is applied to D9 (PM345) of the diode OR gate D14, D16, D9 and D11; this results in the NAND gate G9 (ML1) producing a logic '1' output which is inverted by TR9 to produce a logic '0' muting signal to the drive unit output stage on the PM342 board (pin 12). Hence, the drive unit output is muted until the key is depressed when the level at pin 21 (PM345) rises to +12V and the muting level is removed from pin 5 (PM345). The mute-delay stage introduces a 2 second delay, following the cessation of the keying action, before the drive unit is again muted.

66. The effect of selecting other modes of operation can be deduced from fig.7 in the same manner as previously described.

#### Fault condition

67. The fault input at pin 2 of SKT6 (Table 4) is normally at +12V but falls to 0V when a linear amplifier fault occurs. When a fault occurs, the output from the latch stage ML2 (PM345) rises to logic '1' causing the RESET lamp to glow and, via G7 (ML3), G9 (ML1) and TR9, the transmitter to become muted as described in para.55. When the linear amplifier fault has been cleared, the RESET switch is depressed in order to restore normal operating conditions.

#### Reduced power

68. The reduced-power input line (pin 5 of SKT6) is normally at 0V; when a reduced-power condition prevails, a +12V command is applied to TR10 (PM345) which causes the REDUCED POWER lamp to glow via pin 7 (PM345) and pin 5 of PL1 (front-panel).

#### P.T.T. input

69. The pressel contacts are connected to pins 19 and 36 (+12V) of SKT2 (rear of drive unit); hence, the p.t.t. input appears at pin 19 and is applied, via switch SH (P.T.T. position), switch SA2F, pin 27 of PL1 and pin 19 (PM345) to the diode OR gate referred to in para.65. The action of setting switch SH to P.T.T. is to mute the drive unit, i.e. when the pressel is in the 'normal' (released) position, a logic '1' occurs at the output of G9 (ML1). When it is depressed, the muting action is removed.

#### VOX input

70. When a 'voice' mode is selected and switch SH is set to VOX, the level at pin 12 (PM341) is 0V until a speech signal occurs in channel 1. This 0V level is applied, via pin 15 of PL1 (front-panel), switches SH and SA2F, pin 27 of PL1 (front-panel), pin 19 (PM345) and D11, to the diode OR gate (para.65); this results in a mute output (logic '1') from G9 (ML1) which mutes the drive unit output. When an audio signal appears in channel, pin 12 (PM341) rises to +12V and the muting effect is removed.

VARIANTS

71. The following paragraphs give the differences between variants of the MA.1720 series.

Drive unit MA.1720A

72. The MA.1720A is fitted with a frequency standard assembly Type 9400 having a nominal stability of 1 part in  $10^8$  over the temperature range of  $-10^{\circ}\text{C}$  to  $+60^{\circ}\text{C}$ .

73. The sideband filters fitted to this variant have a 3kHz bandwidth.

Drive unit MA.1720S

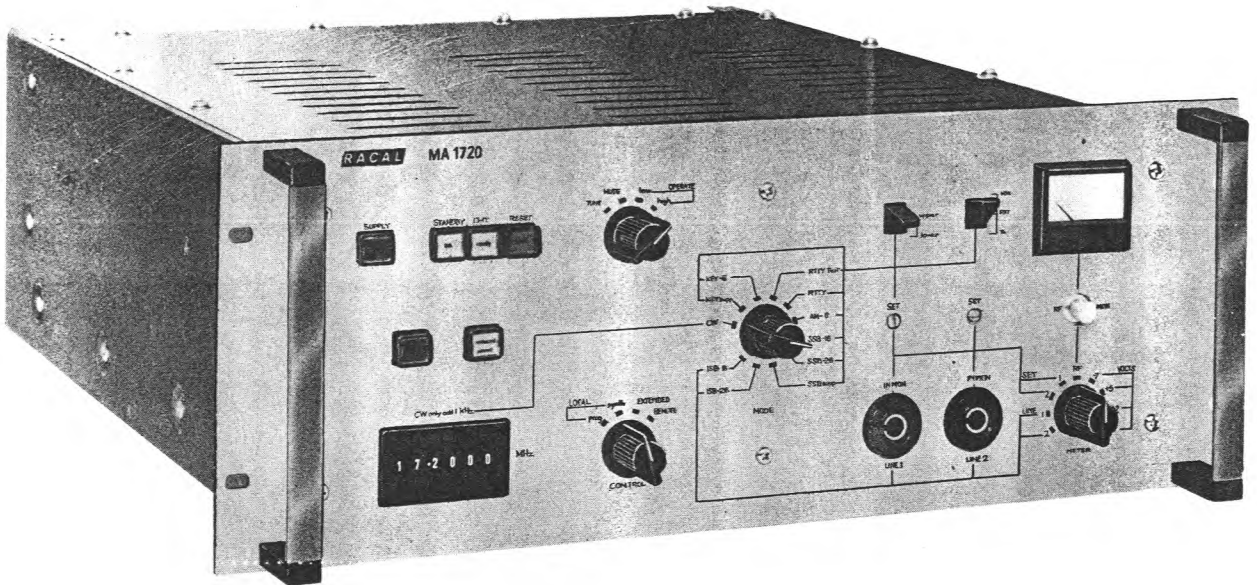
74. The MA.1720S is fitted with a frequency standard assembly Type 9420 having a nominal stability of 6 parts in  $10^{10}$  over the temperature range of  $-10^{\circ}\text{C}$  to  $+60^{\circ}\text{C}$ .

75. The sideband filters fitted to this variant have a 3.4kHz bandwidth.

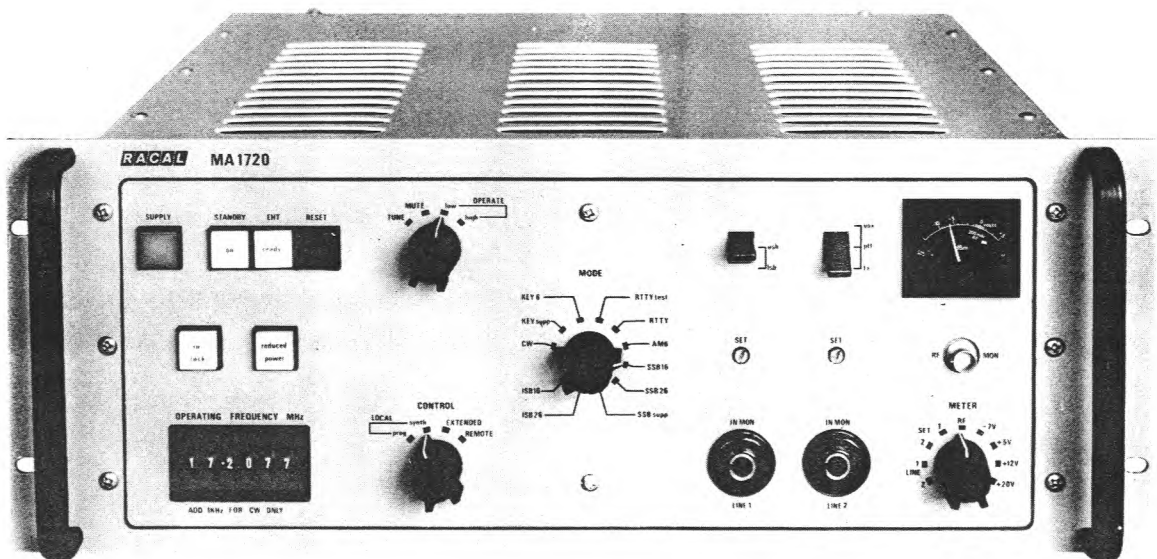
TABLE 4

## List of sub-assemblies

Sub-assembly	Nato No.	Manufacturer's ref.
Standard frequency source	5820-99-635-2527	9400
34MHz generator board	5820-99-631-6959	PM344
LF loop board	5820-99-633-8778	PM349
Transfer loop board	5820-99-633-8779	PS338
HF loop and oscillator board	5820-99-635-9488	PS337
Low level board	5820-99-631-9827	PM341
Mixer and output board	5820-99-631-4957	PM342
Noise immunity board	5820-99-631-6961	PM346
Control board	5820-99-631-6960	PM345
Power supply board	5820-99-631-6958	PM343



OLD VERSION



NEW VERSION

Fig.1 Drive unit : front view



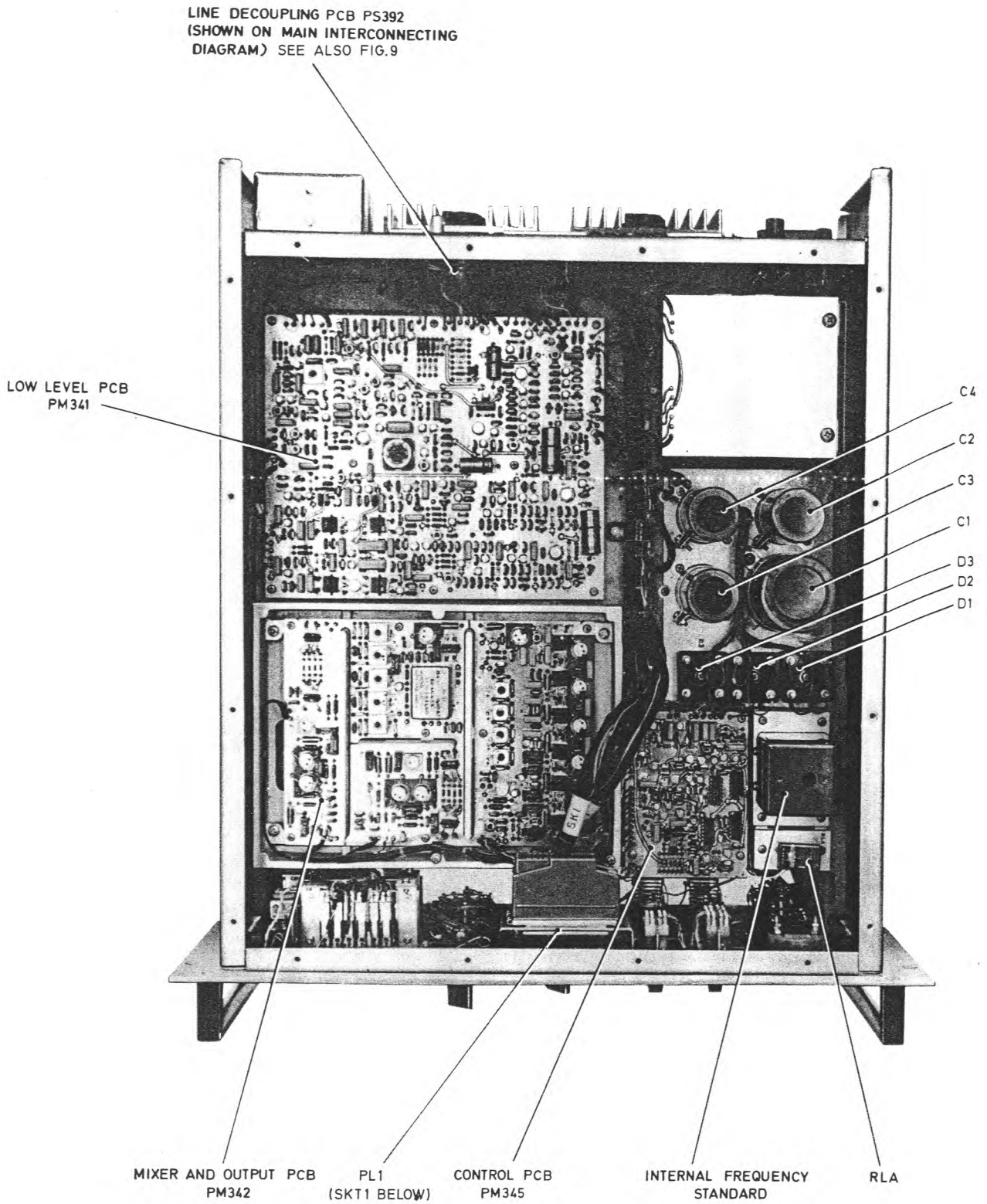


Fig.2 Drive unit : chassis top

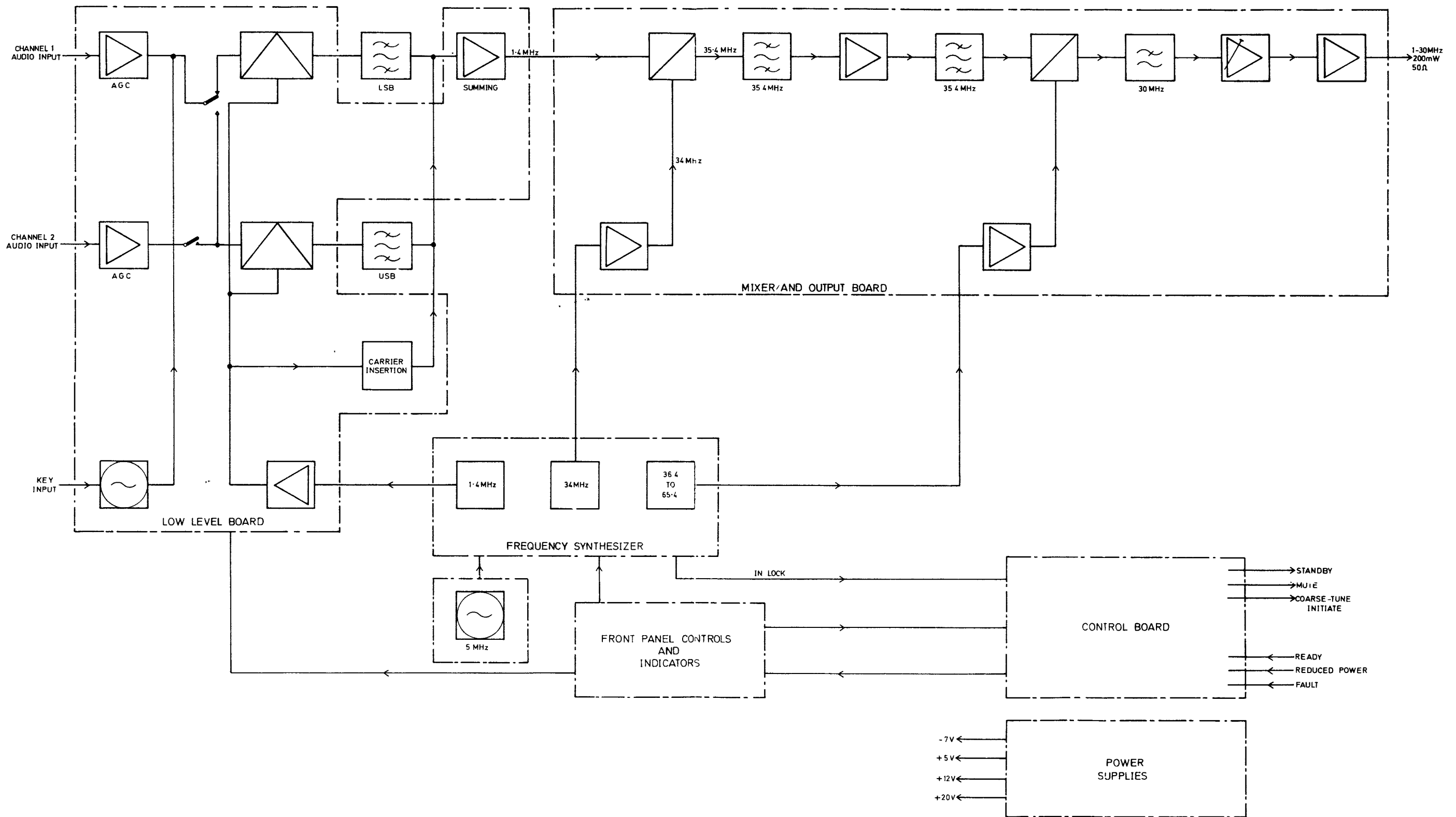


Fig.4

Drive unit : simplified block diagram

Fig.4

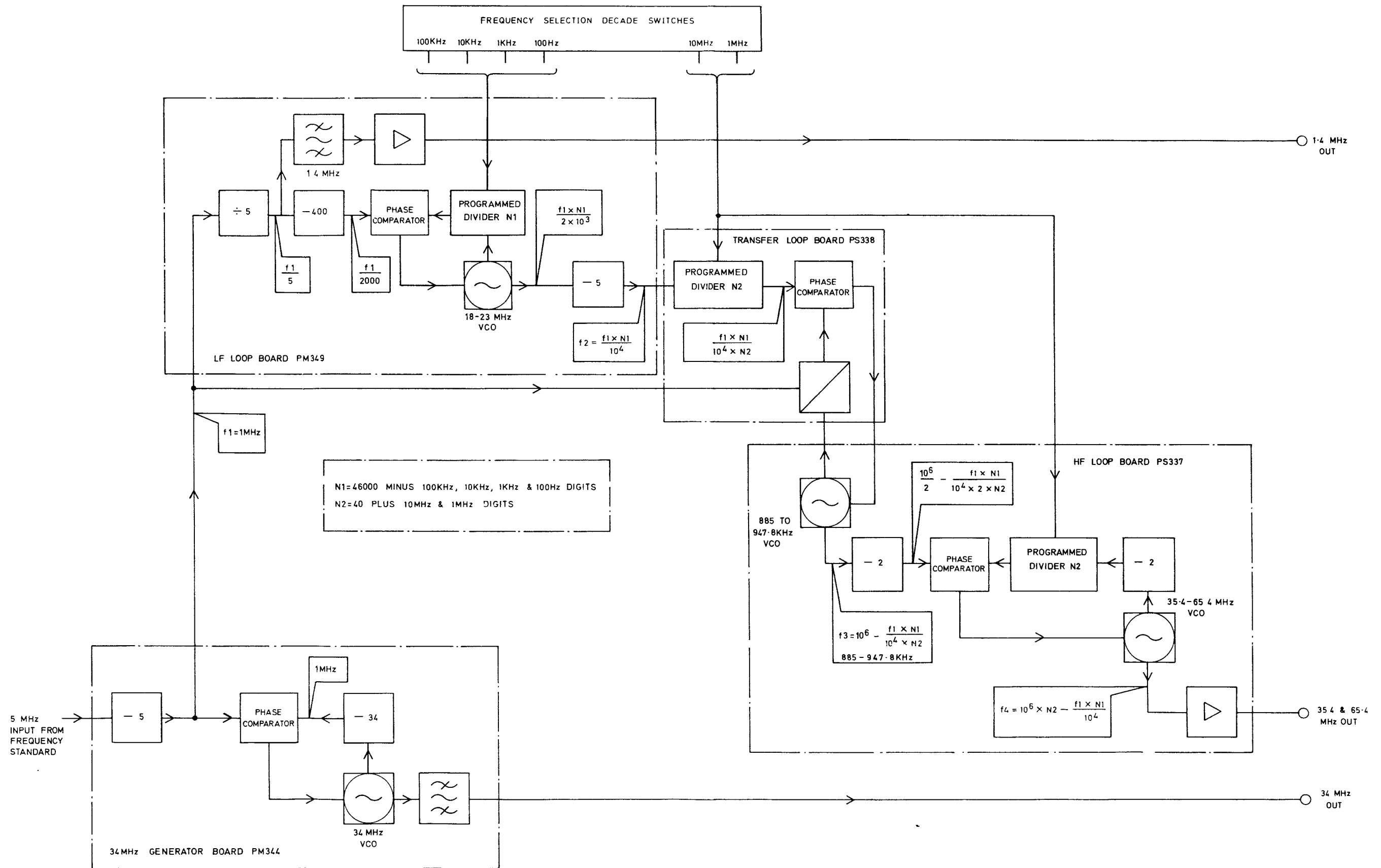


Fig.5

Synthesizer ::simplified block diagram

Fig.5

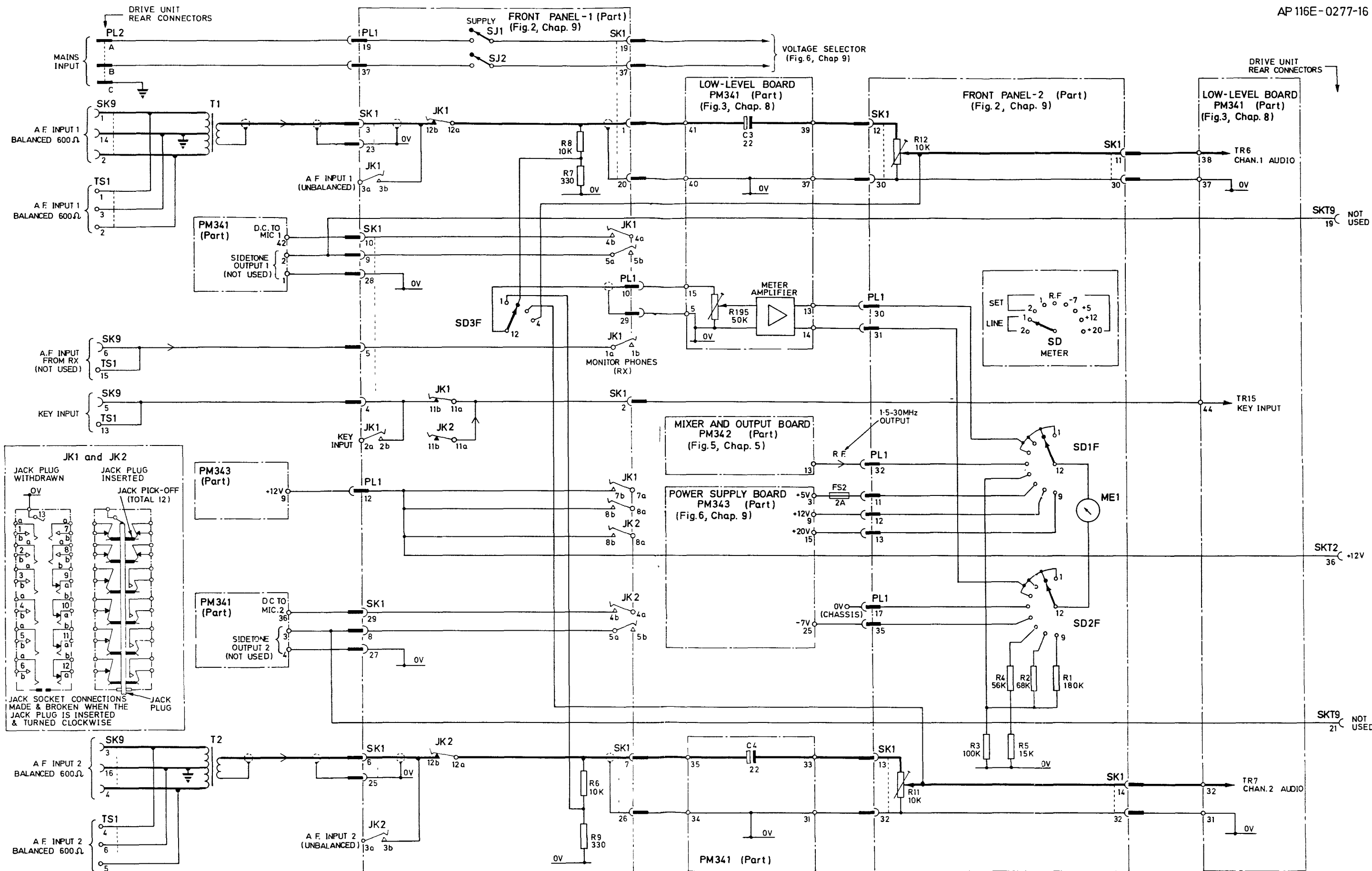


Fig. 6

A.F. and keying input paths: flow circuit

Fig. 6



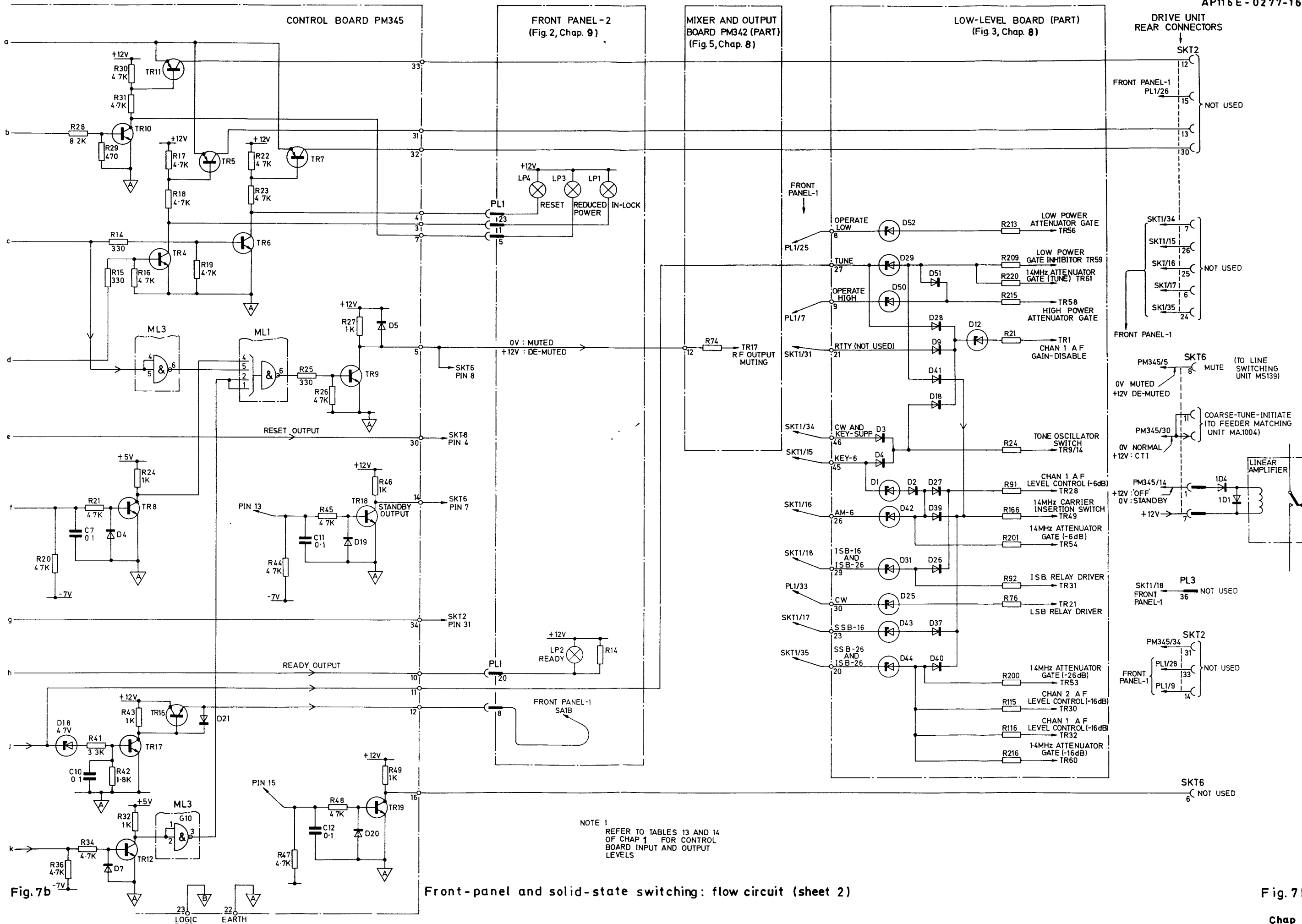


Fig. 7b

Front-panel and solid-state switching: flow circuit (sheet 2)

Fig. 7b

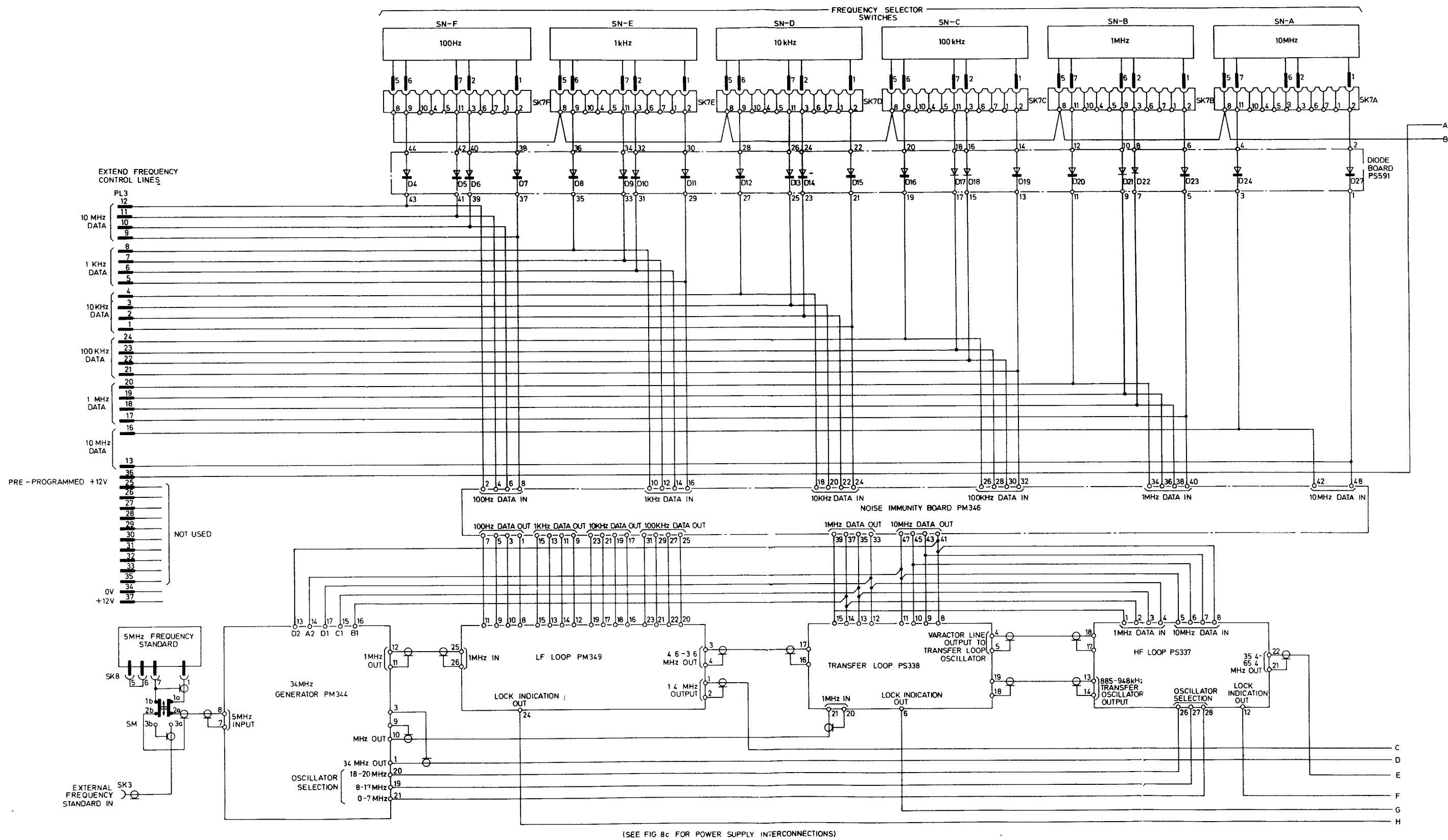


Fig. 8a

Drive unit: interconnection diagram (sheet 1)

Fig. 8a

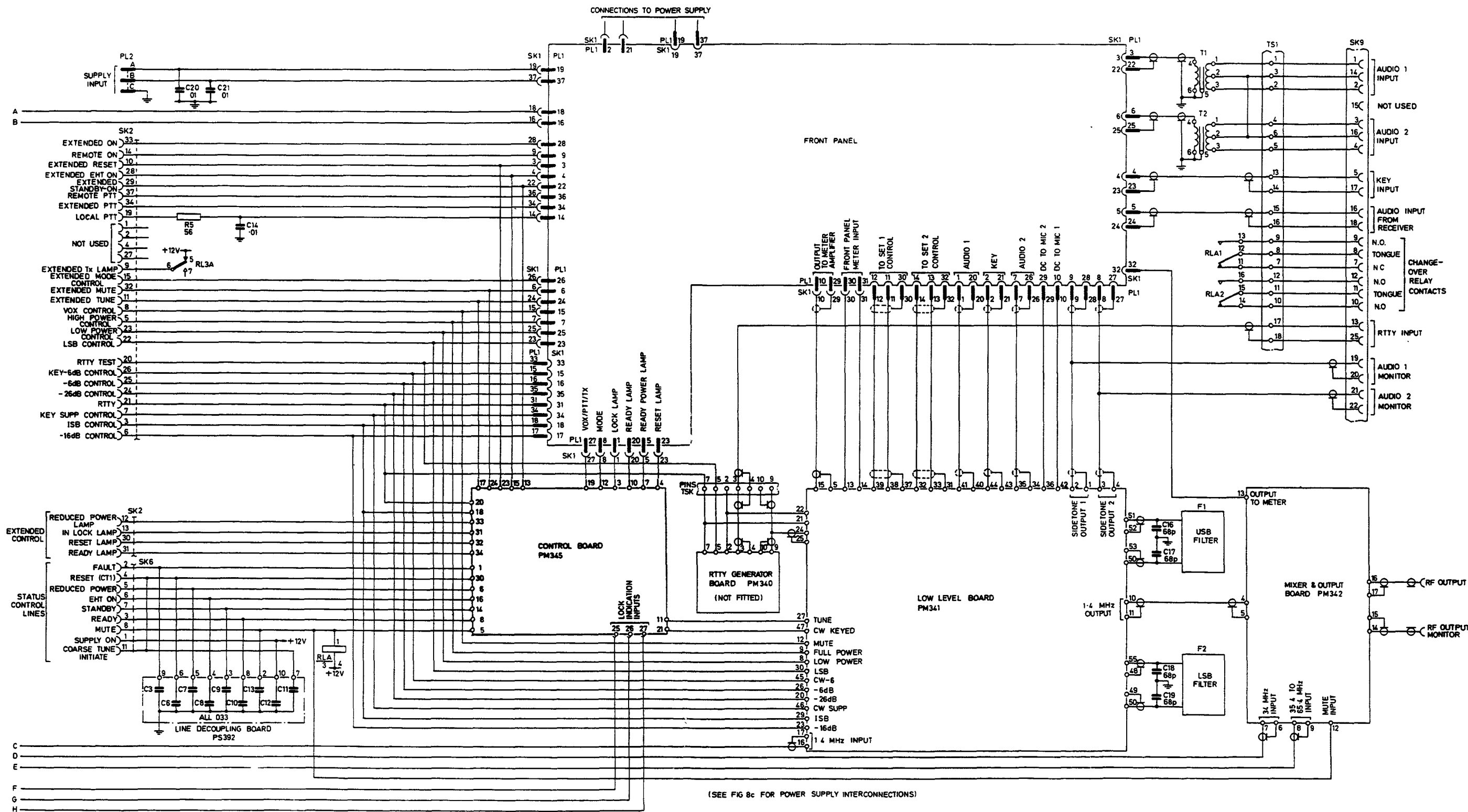


Fig.8b

Drive unit : interconnecting diagram (sheet 2)

Fig.8b



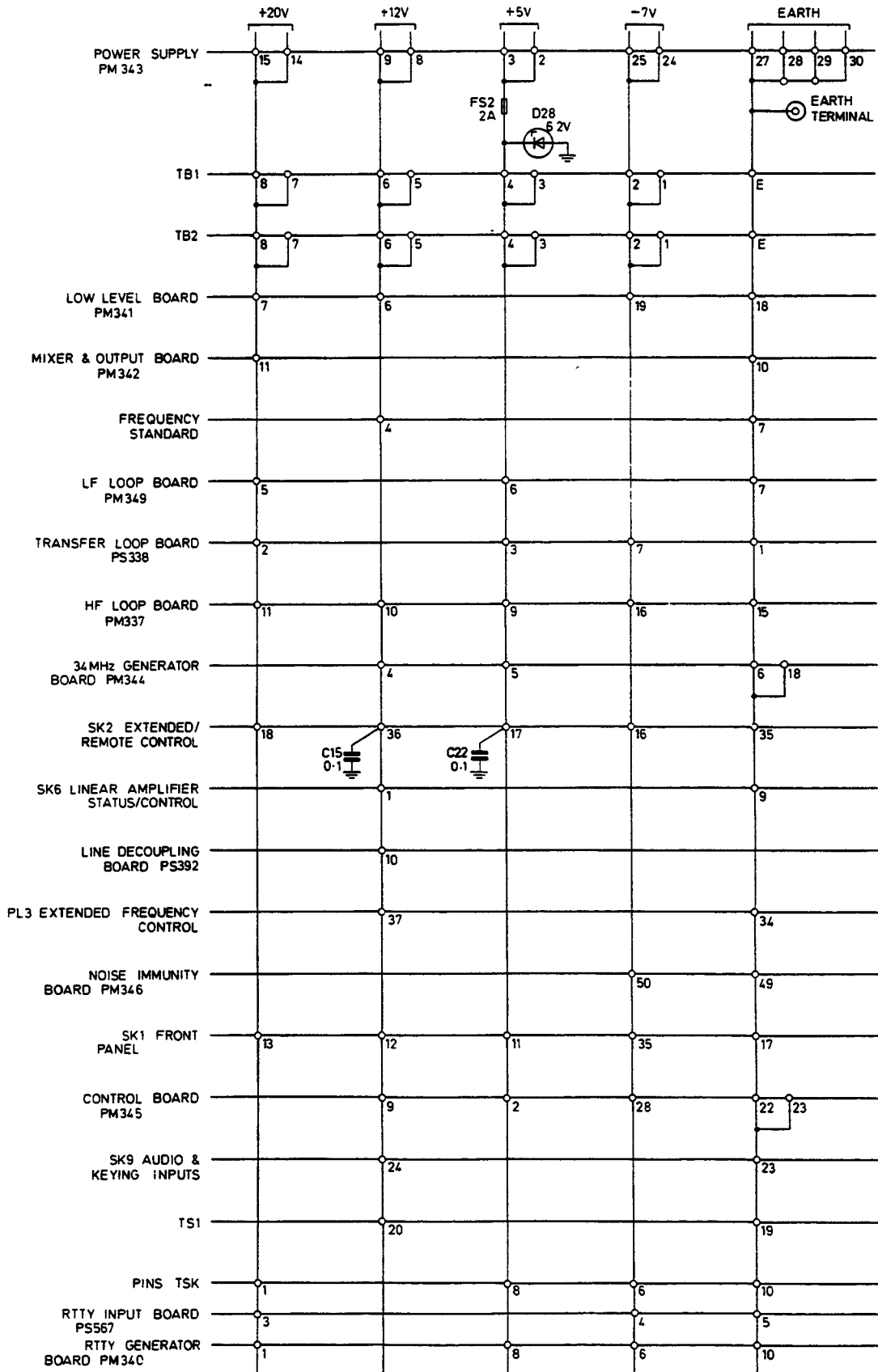
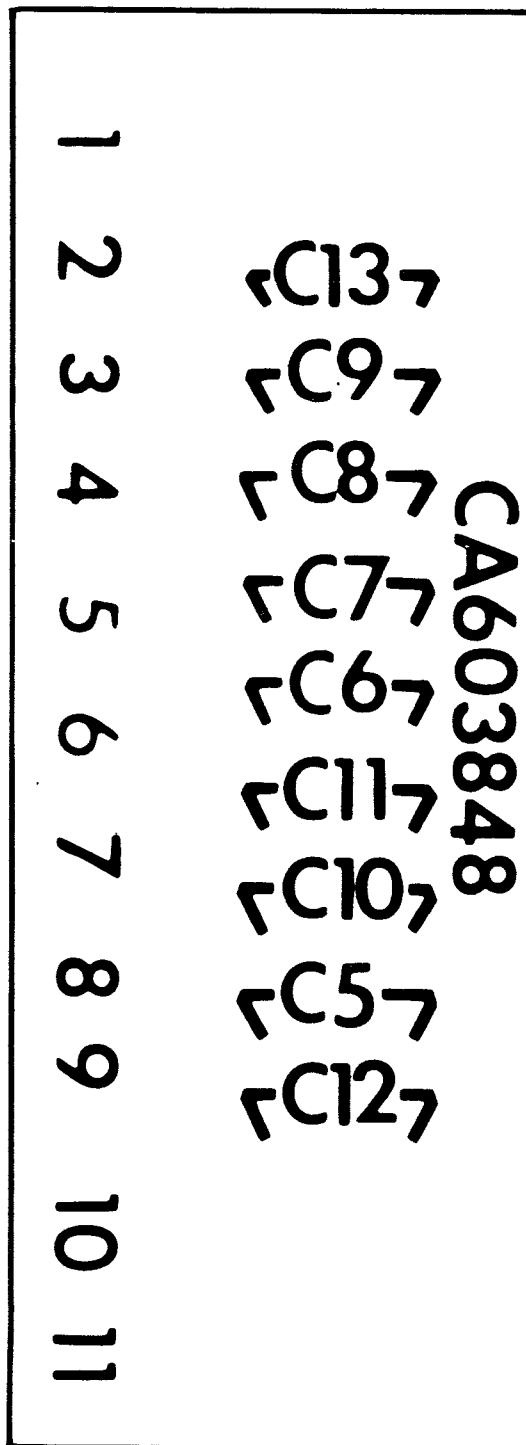
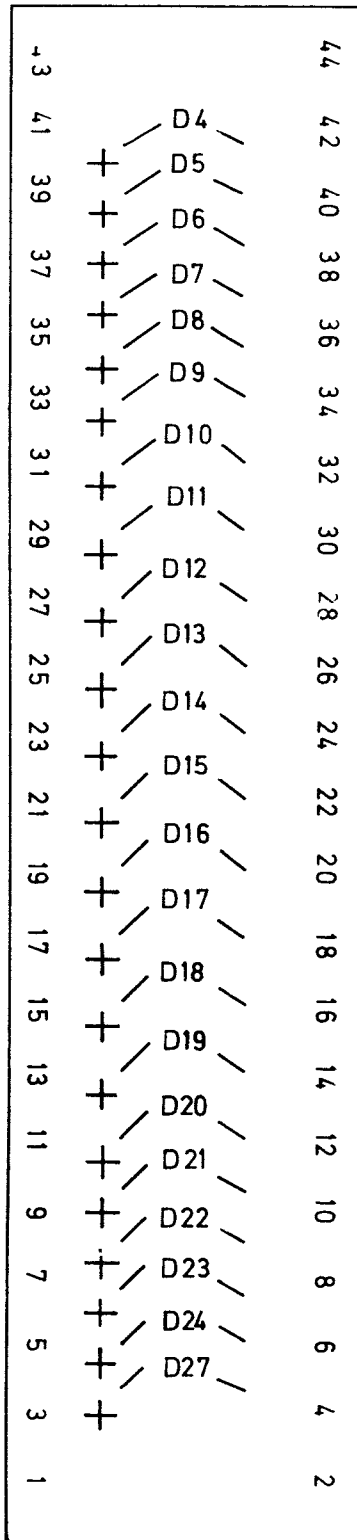


Fig.8c Drive unit : interconnection diagram (sheet 3)



NOTE: CIRCUIT IS SHOWN ON OVERALL INTERCONNECTING DIAGRAM FIG.8

Fig.9 Line decoupling board PS392 : component layout



NOTE: CIRCUIT IS SHOWN ON OVERALL  
INTERCONNECTING DIAGRAM FIG 8

Fig.10 Diode board PS591 : component layout

## Chapter 2

## SETTING-UP AND OPERATING

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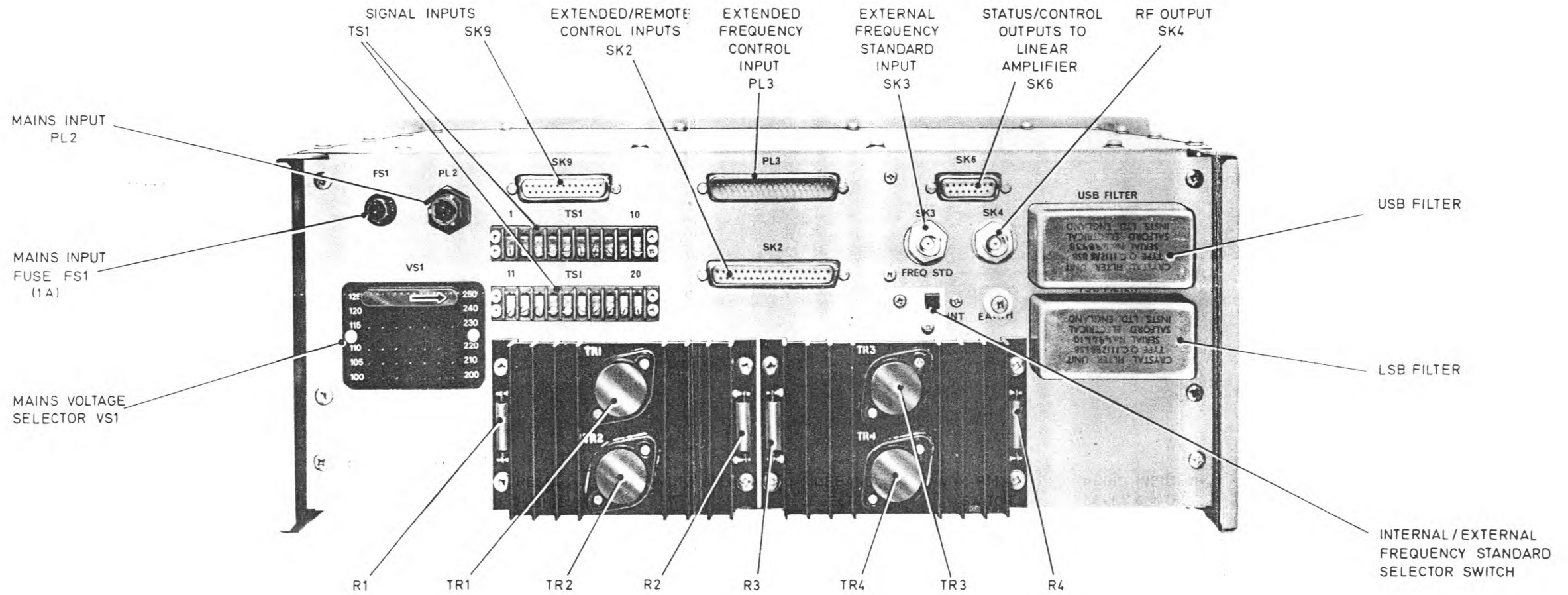
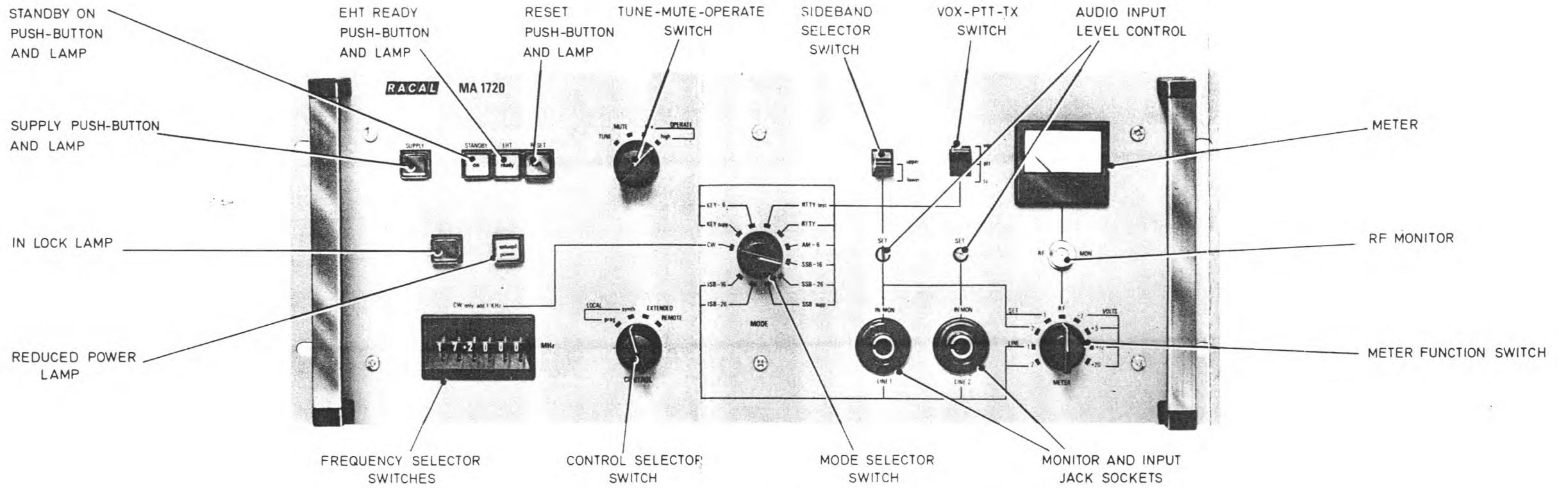
INTRODUCTION

1. This chapter describes the functions of the controls and indicators followed by the setting-up and operating procedures.

FUNCTIONS OF CONTROLS AND INDICATORS

2. The location of all operational controls is given in fig.1.
3. The functions of the front panel controls and indicators are as follows:-
  - (1) SUPPLY pushbutton (with locking action): controls the a.c. supply to the MA.1720. The a.c. supply is normally kept 'on' to maintain the best stability and ageing characteristics of the frequency standard.
  - (2) SUPPLY lamp: glows when power is switched on.
  - (3) STANDBY pushbutton (with locking action): provides a +12V 'command' signal to the associated linear amplifier.
  - (4) STANDBY lamp: glows when the STANDBY pushbutton is operated.
  - (5) EHT pushbutton (with locking action): provides a +12V 'command' signal to the linear amplifier.

- (6) READY lamp: indicates transmitter operational state.
- (7) RESET pushbutton (non-locking): provides a +12V 'command' signal to the linear amplifier. This pushbutton is depressed:-
- (a) Whenever the MA.1720 is set to a new operating frequency.
  - (b) When a re-tune action is required, irrespective of a frequency change.
  - (c) To restore the linear amplifier to normal operation after the clearance of a fault.
- (8) RESET lamp: glows when either:-
- (a) The MA.1720 is muted due to the re-setting of the frequency selector switches.
  - (b) A fault condition is signalled from the linear amplifier.
- (9) REDUCED POWER lamp: glows when the linear amplifier is operating on reduced power output.
- (10) IN LOCK lamp: glows when the synthesizer is locked to the selected frequency.
- (11) TUNE/MUTE/OPERATE switch (four position):-
- (a) TUNE: selects the low-level 'tune' signal.
  - (b) MUTE: mutes the drive to the linear amplifier.
  - (c) OPERATE LOW: selects reduced r.f. output levels (-6dB approx. from the MA.1720.
  - (d) OPERATE HIGH: selects normal r.f. output levels from the MA.1720. This switch position is the one normally used.
- (12) VOX/PTT/TX switch (three position):-
- (a) VOX: voice-operated transmit/receive switching.
  - (b) PTT: manual 'press-to-talk' transmit/receive switching.
  - (c) TX: continuous transmission.
- (13) Frequency selector switches (six thumbwheels): the function is self-evident. The operating frequency is displayed in decade form.
- (14) CONTROL selector switch (four position):-
- (a) LOCAL PROG: this position is selected if the operating frequency is set by means of an external pre-programmer unit.
  - (b) LOCAL SYNTH: the normal position of the switch, i.e. with the operating frequency set by the thumbwheel switches.
  - (c) EXTENDED: control effected via an external control panel.
  - (d) REMOTE: control effected via a remote control system.
- (15) MODE selector switch (eleven position) and sideband selector switch (two position): selection of the following operational modes:-
- (a) CW: continuous wave (keyed carrier) mode. Note that in this mode the frequency selector switches are set to 1kHz above the required operating frequency.



Drive unit : Location of controls

Fig.1

- (b) KEY SUPP: keyed tone in sideband, carrier suppressed.
- (c) KEY -6; keyed tone in sideband with -6dB carrier.
- (d) RTTY TEST: not used.
- (e) RTTY: not used.
- (f) AM-6: compatible a.m. with -6dB carrier.
- (g) SSB-16, UPPER: single sideband with -16dB carrier.
- (h) SSB-16, LOWER: single sideband with -16dB carrier.
- (j) SSB-26, UPPER: single sideband with -26dB carrier.
- (k) SSB-26, LOWER: single sideband with -26dB carrier.
- (l) SSB SUPP, UPPER: single sideband, carrier suppressed.
- (m) SSB SUPP, LOWER: single sideband, carrier suppressed.
- (n) ISB-26: independent sideband with -26dB carrier.
- (p) ISB-16: independent sideband with -16dB carrier.

(16) METER switch (nine position): for measuring the following parameters (operating conditions are given in Table 1):-

- (a) LINE 2: line 2 audio input level.
- (b) LINE 1: line 1 audio input level.
- (c) SET 2: audio input level to line 2 amplifier.
- (d) SET 1: audio input level to line 1 amplifier.
- (e) RF: r.f. output level to the linear amplifier.
- (f) -7 VOLTS     )
- (g) +5 VOLTS     ) supply rails.
- (h) +12 VOLTS    )
- (j) +20 VOLTS    )

- (17) SET LINE 1 (preset): adjusts audio level to line 1 amplifier.
- (18) SET LINE 2 (preset): adjusts audio level to line 2 amplifier.
- (19) METER: used in conjunction with METER switch.

4. The following front panel monitoring points are also provided:-

- (1) RF MON (coaxial connector): provides a sample of the r.f. output for use with external test equipment e.g. a frequency counter.
- (2) IN/MON LINE 1 jack (multiway connector): provides monitoring and signal access to this audio path.
- (3) IN/MON LINE 2 jack: as for item (2).

#### SETTING-UP INSTRUCTIONS

5. The setting-up procedures are carried out, in the order given, at initial switch-on or after a repair.

### Preliminary adjustments

6. (1) Ensure that the main a.c. supply to the transmitting set is switched OFF.
- (2) Set the SUPPLY pushbutton on the MA.1720 to OFF (released).
- (3) Remove the MA.1720 from the cabinet.
- (4) Check that the main voltage selector is set for the local supply voltage; re-set as necessary.
- (5) Set the FREQ. STD. switch to INT or EXT as required.
- (6) Check that fuse-link FS1 is serviceable and of correct rating (500mA).
- (7) Re-fit the MA.1720 to the cabinet and secure.

#### Note...

When re-fitting the unit to the cabinet, ensure that all cables are dressed to their correct positions. Where cable connections are disturbed, it is assumed that the connections are re-made correctly.

- (8) Set the front panel controls as follows:-
  - (a) SUPPLY pushbutton to OFF.
  - (b) STANDBY pushbutton to OFF.
  - (c) EHT pushbutton to OFF.
  - (d) CONTROL switch to LOCAL SYNTH.
  - (e) MODE switch to SSB SUPP.
  - (f) Sideband switch to UPPER.
  - (g) VOX/PTT/TX switch to TX.
  - (h) TUNE/MUTE/OPERATE switch to OPERATE HIGH.
  - (j) Frequency selection switches to 03.0000MHz or as required.

### Switch-on sequence

7. (1) Set the main a.c. supply switch to ON.
- (2) Depress the SUPPLY pushbutton and check that the SUPPLY and IN-LOCK lamps glow.
- (3) Depress the STANDBY pushbutton and check that the STANDBY lamp glows.
- (4) Check that the RESET lamp is extinguished; if not, depress the RESET pushbutton.

### Supply voltages

8. Set the METER switch to the -7, +5, +12 and +20 VOLTS positions in turn. A meter-reading within the green band should be obtained in each case.



LINE LEVELS

9. It is assumed for setting-up purposes that test tones of the required line input level, e.g. 0dBm, are being applied to the AUDIO 1 and AUDIO 2 inputs.
10. (1) Set the METER switch to LINE 1 and check that the meter indicates the AUDIO 1 input level e.g. 0dBm.  
 (2) Set the METER switch to SET 1.  
 (3) Adjust the SET LINE 1 preset control until a 0dBm level is obtained.  
 (4) Set the METER switch to LINE 2 and check the AUDIO 2 input level.  
 (5) Set the METER switch to SET 2.  
 (6) Adjust the SET LINE 2 control until a 0dBm level is obtained.
11. (1) Set the METER switch to RF.  
 (2) Check that the meter indicates -3dB:(100mW r.f. output) approximately  
 (3) Set the sideband selector switch to LOWER and repeat step (2).
12. (1) Re-set the sideband switch to UPPER.  
 (2) Disable the AUDIO 2 input.  
 (3) Set the MODE switch to ISB -26.  
 (4) Check that 25mW r.f. output (-9dB on the meter) is obtained.  
 (5) Disable the AUDIO 1 input.  
 (6) Re-connect the AUDIO 2 input.  
 (7) Check that 25mW output is again obtained.

## Note...

If the AUDIO 1 input is now re-connected, a 100mW p.e.p. output is developed from the dual-tone input. Under these conditions, the meter indicates -6dB approximately.

Switch-off sequence

13. (1) Set the STANDBY pushbutton to OFF (released).  
 (2) Set the TUNE/MUTE/OPERATE switch to MUTE.

## Note...

The SUPPLY pushbutton on the MA.1720 should be left ON.

OPERATING PROCEDURES

14. It is assumed that the setting-up procedures have been completed and that the required audio line inputs are present.
15. Set the front panel controls as follows:-
- (1) SUPPLY pushbutton to ON i.e. with lamp glowing.  
 (2) STANDBY pushbutton to OFF.  
 (3) TUNE/MUTE/OPERATE switch to OPERATE HIGH or as required.  
 (4) CONTROL switch to LOCAL SYNTH.

(5) Frequency selector switches (thumbwheels) to desired operating frequency.

(6) MODE and 'sideband' switches as required.

(7) VOX/PTT/TX switch as required.

16. Depress the STANDBY pushbutton and check that the STANDBY, RESET and IN LOCK lamps glow.

17. Depress the EHT pushbutton.

18. Depress the RESET pushbutton and check that the RESET lamp is extinguished. Allow time for the associated transmitter to carry out its tuning procedures. When the READY lamp glows, the transmitter is ready to accept traffic.

#### Change of operating mode or frequency

19. Changes to the operating mode or sideband may be made during normal transmission by re-setting the MODE and 'sideband' switches on the MA.1720 as required.

20. Changes to the operating frequency are made as follows:-

(1) Reset the thumbwheel switches on the MA.1720 to the new frequency.

(2) Depress the RESET pushbutton.

TABLE 1

Signal levels - front panel meter

Switch position	Normal indication
LINE 2	Dependent upon line input level
LINE 2	Dependent upon line input level
SET 2	0dBm (nominal): adjusted by the appropriate SET control.
SET 1	0dBm (nominal): adjusted by the appropriate SET control.
RF	As logged for each mode.
-7	Within green band.
+5	Within green band.
+12	Within green band.
+20	Within green band.

TABLE 2

## Signal levels - monitor sockets

Test-point	Instrument	Normal indication
R.F. MON socket	Oscilloscope	Up to 0.3Vp-p (as logged) when terminated in 50Ω.
	Electronic Voltmeter	Up to 0.1V r.m.s. (as logged) when terminated in 50Ω.
IN/MON LINE 1 jack )	A.F. signal	See Note
)	source or	
IN/MON LINE 2 jack )	headphones	

## Note...

The jacks provide for the injection of audio test signals to the drive unit or for headphone monitoring of the normal line inputs.

## Chapter 3

## SERVICING

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### INTRODUCTION

1. This chapter contains a list of the relevant test equipment required to carry out the fault-finding procedures which follow.
2. The fault-finding procedures are separated under the following headings:
  - (1) fault-finding to board or sub-assembly level.
  - (2) fault-finding to component level.
3. In addition to the procedures given in this chapter, the task of fault-finding to board level requires a reference to fig. 6, 7 and 8 and the detailed functional description in Chap.1. Fault-finding to component level requires an understanding of the descriptions given in Chap.7,8 and 9.

### TEST EQUIPMENT

4. The following items of test equipment are required:
  - (1) Multimeter CT498A.
  - (2) Oscilloscope CT588.
  - (3) Microphone with built-in pressel switch.
  - (4) Electronic voltmeter.
  - (5) Morse key.
  - (6) Frequency counter (Racal 9059).
  - (7) L.F. signal generator (Marconi TF2005R).

### FAULT LOCATION

5. As previously stated, the flow-circuits in fig. 6 and 7 of Chap.1 function as a useful aid to fault-finding to board level. Initially, a functional check is carried out from which deductions are made as to where the fault might exist. All checks are carried out, unless otherwise stated, with the drive unit on a bench and connected to a mains supply.

### FREQUENCY STANDARDS (9400 AND 9420)

6. The frequency standard is a replaceable sub-assembly which, if found to be faulty, is returned to the manufacturer. A performance check and adjustment procedure is given in Chap.6.
7. To check that the frequency standard is functioning, ensure that the drive unit has been switched on for at least 30 minutes and connect an

oscilloscope to pin 8 on the 34MHz generator board; the amplitude of the displayed waveform should be 800mV p-p. However, although the output level may be correct, a failure in the crystal oven control stages would result in the output frequency shifting up by 125Hz; this can be checked using the frequency counter. A further fault indication is obtained by measuring the current drawn from the +12V d.c. supply. Refer to Table 1 and use the multimeter to make the measurement; unsolder the lead to pin 4 of SKT8 (fig.8, Chap.1).

TABLE 1  
Frequency standard : supply current

	Supply current	
	Type 9400 (MA.1720A)	Type 9420 (MA.1720S)
Normal	60 to 70mA	120 to 125mA
Fault	25 to 30mA	25 to 30mA

#### BOARD-LEVEL FAULT-LOCATION

8. It is assumed that no fault exists in the inter-board wiring which can be checked using the interconnecting diagrams (fig. 8) in Chap.1. It is also assumed that all lamps and fuses are satisfactory. Before switching on the drive unit, set the front-panel controls as follows:

- (1) SUPPLY switch to 'off'.
- (2) STANDBY switch to 'off'.
- (3) TUNE/MUTE/OPERATE switch to OPERATE HIGH.
- (4) MODE switch to C.W.
- (5) VOX/PTT/TX switch to TX.
- (6) Link pins 13 and 14 of TS1 (rear).
- (7) LOCAL/EXTENDED/REMOTE switch to LOCAL SYNTH.
- (8) Depress the SUPPLY pushbutton.

Note...

It is not necessary to depress the STANDBY pushbutton.

- (9) Set the METER switch, in turn, to the -7V, +5V, +12V and +20V positions. Check that, for each position, the meter indication is within the green band; if not, refer to Chap.6 for the adjustment procedure. If one or the other of these supply voltages is not present, either a fault exists on the PM.343 board or a short-circuit exists in the wiring within the drive unit.
- (10) Observe that the following lamps are glowing:
  - (a) SUPPLY.
  - (b) RESET.
  - (c) IN LOCK.

9. Should the IN LOCK lamp fail to glow, a fault may exist on one or more of the three synthesizer boards PM.349, PS.338 and PS.337 (fig. 3, Chap.1). Using the multimeter, monitor in turn pins 12 (PS.337), 6 (PS.338) and 24 (PM.349). A normal reading is +5V (nom.); an abnormal (fault) reading of 0V

indicates the faulty board(s). However, a further out-of-lock condition can exist where the IN LOCK lamp continues to glow; in this case, the use of an oscilloscope will display short-duration negative-going pulses on the above affected in-lock line(s).

10. Carry out the following functional checks:

- (1) Connect a 50 $\Omega$  dummy load to the r.f. output socket (SKT4) on the rear of the unit.
- (2) Simulate a 'ready' input command from the linear amplifier by linking pin 3 to pin 9 (OV) of SKT6 (rear).
- (3) Set the six frequency selector switches to an arbitrary setting.
- (4) Depress the RESET pushbutton and observe the following:
  - (a) the RESET lamp extinguishes following a 2-sec delay.
  - (b) the IN LOCK lamp momentarily extinguishes; however, this is not discernible.
- (5) Set the METER switch to R.F. and check for a meter reading of 200mW approximately.

11. If the meter reading is zero and the lamps are indicating correctly, check that +12V (nom.) exists at pin 5 of the PM.345 board; if not, the PM.345 board may be at fault. Alternatively the muting stage on the PM.342 board may be at fault.

- (1) Connect the multimeter between pin 7 (+ve) and pin 9 (OV) of SKT6.
- (2) Depress the STANDBY switch and observe that the meter reading drops from +12V to OV. If not, a fault exists on the PM.345 board.
- (3) Link pin 2 (+12V) of SKT2 (rear) to pin 5 of SKT6 (rear) in order to simulate a 'reduced-power' input command from the linear amplifier.
- (4) Check that the REDUCED POWER lamp glows; if not, a fault exists on the PM.345 board.
- (5) Remove the link made in (3) above.
- (6) Using the multimeter, check that pin 8 (SKT6) is at +12V.
- (7) Set the TUNE/MUTE/OPERATE switch to MUTE and check that the multimeter now reads OV; if not, a fault exists on the PM.345 board.
- (8) Reset the TUNE/MUTE/OPERATE switch to OPERATE HIGH.
- (9) Connect the multimeter (+12V d.c.) between pin 4 (SKT6) and earth.
- (10) Depress and hold the RESET switch and check that the meter reading changes from OV to +12V, and that the RESET lamp glows; if not, a fault exists on the PM.345 board. Release the switch.
- (11) Simulate a linear amplifier fault by linking pin 2 to pin 9 (OV) of SKT6. Check that the RESET lamp is glowing and that the r.f. output meter indication has dropped to zero (muted condition).
- (12) Depress the RESET switch and observe that, for a period of two seconds, the RESET lamp extinguishes and the r.f. output indication is restored (not-muted condition). If the preceding results are not obtained, a fault may exist in either the PM.345 board or the muting stage of the PM.342 board; the fault is on the PM.342 board if the r.f. output meter indication does not drop to zero when the RESET switch is operated.
- (13) Remove the link between pins 2 and 9 of SKT6 and observe that the RESET lamp is extinguished and the r.f. output indication is restored.

(14) Remove the link between pins 13 and 14 of TS1 (rear).

13. The following tests check the operation of the MODE switch, the TUNE/MUTE/OPERATE switch and the VOX/PTT/TX switch; it is assumed that audio input-level-setting has been correctly carried out; refer to Chap. 2.

- (1) Set the MODE switch to AM-6.
- (2) Set the VOX/PTT/TX switch to TX.
- (3) Check that the TUNE/MUTE/OPERATE switch is set to OPERATE HIGH.
- (4) Check that the r.f. output meter indication is 100mW, approximately, with no audio input to the drive unit.
- (5) Set the TUNE/MUTE/OPERATE switch to OPERATE LOW and observe that the r.f. output indication reduces by a further 6dB approximately; if not, a fault exists on the PM.341 board.
- (6) Reset to OPERATE HIGH.
- (7) Set the MODE switch to SSB SUPP and observe that the r.f. output indication has dropped to zero.
- (8) Connect a microphone into the LINE 1 jack socket (JK1, pin 12a); speak into the microphone and observe that a speech-modulated r.f. output indication occurs on the meter. If not, a fault exists in the channel 1 audio stages of the PM.341 board.
- (9) Reset the MODE switch to AM-6.
- (10) Set the TUNE/MUTE/OPERATE switch to MUTE and check that the r.f. output meter indication is zero.
- (11) Speak into the microphone and observe that there is no speech modulated r.f. indication on the meter.
- (12) Reset to OPERATE HIGH.
- (13) Set the VOX/PTT/TX switch to VOX and check that the r.f. output indication is zero.
- (14) Check that an r.f. output indication occurs when speaking into the microphone, and that this indication is sustained for approximately two seconds following the cessation of speech. If not, a fault may exist in either the 'vox' control stages of the PM.341 board or on the PM.345 board. The 'vox' control stages are checked by monitoring pin 12 (PM.341) and observing that the level rises from 0V to +12V when speech occurs; this +12V indication should remain for two seconds following cessation of speech.
- (15) Set the VOX/PTT/TX switch to PTT.
- (16) If the microphone has a built-in pressel switch, the pressel contacts should be connected to pins 6b and 7b of the jack plug. Alternatively, a pressel action is obtained by temporarily joining pin 19 to pin 36 of SKT2 (rear).
- (17) Check that the r.f. output indication is zero.
- (18) Operate the microphone pressel and observe that an r.f. output indication occurs. If not, a fault exists on the PM.341 board.
- (19) Disconnect the microphone.
- (20) Connect an electronic voltmeter across the 50Ω dummy load at the r.f. output socket (SKT4).



- (21) With the MODE switch still in the AM-6 position, note the reading on the electronic voltmeter as a reference.
- (22) Set the mode switch, in turn, to each of the following positions and note that the voltmeter reading is either 10dB or 20dB, as appropriate, below the reading noted in (21) above: SSB-16, SSB-26, ISB-16 and ISB-26. If not, a fault exists on the PM.341 board.
- (23) Connect a morse key to pins 13 and 14 of TS1.
- (24) Set the MODE switch, in turn, to C.W., KEY SUPP and KEY-6 and refer to Table 2 for the appropriate r.f. output meter indications.

TABLE 2

C.W., key suppressed and key (-6dB) mode checks

Meter with key:	Mode switch setting		
	C.W.	KEY SUPP	KEY-6
up	0	0	50mW
down	200mW	200mW	100mW (approx.)

COMPONENT-LEVEL FAULT-LOCATION

14. The following information consists mainly of in-situ measurements of voltage levels at specified points on the boards. The location of monitoring points is shown on the component layout diagrams in Chap.7,8 and 9. With the exception of the mixer and output board, monitoring on the reverse side of all boards is made possible by removing the fixing screws and hinging the board up on the cable harness.

Power supply board PM.343

15. Check the four unregulated input voltages to the board as follows:

- (1) +30V d.c.  $\pm$  3V at pin 17.
- (2) +18V d.c.  $\pm$  3V at pin 12.
- (3) +10V d.c.  $\pm$  2V at pin 6.
- (4) +4.5V d.c.  $\pm$  1.5V at pin 22.

16. If any one of the above voltages is incorrect, check the associated rectifiers and secondary voltage on T3. If these voltages are correct, the board must be checked as follows.

17. Note that if the +20V supply fails, then the +12V and +5V supplies also fail. Check the board voltage levels, as given in Table 3, using a multimeter; the voltages are measured with respect to chassis (0V) unless otherwise stated.

TABLE 3

## Power supply board : voltage levels

Monitor at:	Measured voltage
ML2, pin 7 or 8	+30V
ML2, pin 4	+7.15V $\pm$ 0.5V
ML2, pin 3	+7.0V $\pm$ 0.5V
ML2, pin 2	+7.15V $\pm$ 0.5V
Board pin 14 or 15	+20V (output)
Board pin 10	+18V $\pm$ 3V
ML3, pin 4	+7.15V $\pm$ 0.5V
ML3, pin 3	+7.15V $\pm$ 0.5V
ML3, pin 7 or 8	+20V
ML3, Pin 6	+14.5V
ML3, pin 2	+7.15V $\pm$ 0.5V
Board pin 8 or 9	+12V (output)
Board pin 4	+10V $\pm$ 2V
ML4, pin 4	+7.15V $\pm$ 0.5V
ML4, pin 3	+5V
ML4, pin 7 or 8	+20V
ML4, pin 6	+8V
Board pin 2 or 3	+5V (output)
Board pin 22	+4.5V $\pm$ 1.5V
ML1, pin 4	+7.15V $\pm$ 0.5V relative to board pin 25 (approx. 0V with respect to earth)
ML1, pin 7 or 8	+4.5V with respect to earth
Board pin 25	-7V

18. Check that the four preset controls R12 (-7V), R22 (+20V), R23 (+12V) and R9 (+5V) effectively adjust the appropriate output voltage level. This latter check, in conjunction with the data in Table 3, should locate the component(s) which have failed.

#### Mixer and output board PM.342

19. Using a multimeter, refer to Table 4 and check the transistor emitter voltages listed; set the MODE switch to AM-6.

TABLE 4

Mixer and output board : emitter voltages (d.c.)

Transistor	Emitter voltage (d.c.)
TR13	5.8V
TR12	5.6V
TR11	2.8V
TR10	2.6V
TR9	2.6V
TR15	8.0V
TR6	3.2V
TR5	4.0V
TR8	6.0V
TR3	3.2V
TR2	4.0V

20. Using an oscilloscope, refer to Table 5 and check the r.f. voltages at the collectors of the transistors; set the MODE switch to C.W.

TABLE 5

Mixer and output board : collector r.f. voltages

Transistor	Collector voltage (p-p)
TR13	16.0V
TR12	7.5V
TR11	4.0V
TR10	1.6V
TR9	0.8V
TR15	0.3V
TR6	15 to 20V (35 to 60MHz)
TR5	15 to 20V (35 to 60MHz)
TR8	1.0V
TR3	15 to 20V (35.4MHz)
TR2	15 to 20V (35.4MHz)

21. If the board is functioning correctly, the nominal current drawn from the supply is 900mA (d.c.) when +12V d.c. is applied to pin 12 (de-muted condition and the MODE switch is set to AM-6.

22. If excessive break-through from the 2nd local oscillator is suspected, re-align the 30MHz low-pass filter in accordance with the instructions in Chap.5.

23. The levels of the three inputs to the board are as follows:

- (1) 1.4MHz (pin 4) at 600mV p-p from the PM.341 board.
- (2) 34MHz (pin 7) at 0dBm (225mV) from the PM.344 board.
- (3) 35.4 to 65.4MHz at 0dBm (225mV) from the PS.337/3 board.

Should any of these inputs be at an abnormal level, a fault exists on the board from which it is derived.

#### Low-level board PM.341

24. Proceed as follows:

- (1) Set the mode switch to KEY SUPP and the SIDEBAND switch to LSB.
- (2) Link pins 13 and 14 of TS1 (rear). Using an electronic voltmeter, check that the collector of TR14 is at +12V (nom.), and that the collector of TR1 is at -7V (nom). If not, check TR9, TR14 and TR1.
- (3) Set the TUNE/MUTE/OPERATE switch to OPERATE HIGH.
- (4) Connect an oscilloscope to pin 16 and check that the displayed waveform is approximately 600mV p-p at 1.4MHz. If not, check the 1.4MHz generator on the PM.349 board (para.39).
- (5) Using the oscilloscope, monitor at TP5 on the board for a level of 620mV p-p at 1.4MHz. If not, check the 1.4MHz gain-controlled amplifier TR40 and TR43 to TR46.
- (6) Using the oscilloscope, check for a squarewave of 4V p-p (nom.) at the collectors of TR41 and TR42.
- (7) Using the oscilloscope, check for a sinewave of 1V p-p at the collector of TR57. If not, check TR55 and TR57.
- (8) Set the SIDEBAND switch to USB and check (audibly) that relay RLA/1 de-energizes. If not, check TR21.
- (9) Set the MODE switch to ISB-16 and check (audibly) that relay RLB/1 energizes. If not, check TR31.
- (10) Set the MODE switch to KEY-6 and reset the SIDEBAND switch to LSB.
- (11) Using an electronic voltmeter (+12V d.c.), check the voltage levels shown in Table 6.

TABLE 6

Key-6 mode : voltage levels

Monitor at:	Measured voltage
pin 45 on board	+12V nom.
TR14 collector	+12V nom.
TR28 collector	0V nom.
TR50 collector	+5.5V nom.
TR54 collector	0V nom.
TR1 collector	-7V nom.

Check the appropriate transistors if any of the above results are not obtained.

(12) Set the MODE switch to SSB-16 and, using an electronic voltmeter, check the levels shown in Table 7.

TABLE 7  
SSB-16 mode : voltage levels

Monitor at:	Measured voltage
pin 23 of board	+12V nom.
TR50 collector	+5.5V nom.
TR30 collector	0V nom.
TR32 collector	0V nom.
TR60 collector	0V nom.
TR2 collector	+15V nom.
TR3 collector	-5.6V nom.

If any of the above results are not obtained, check the appropriate transistor(s).

(13) Connect an audio signal generator into the LINE 1 jack socket (JK1, pin 12a).

(14) Adjust the generator output level to 0dBm, using an oscilloscope, at pin 38 of the board. Set the generator frequency to 1kHz. Set the METER switch to SET 1 and adjust the SET LINE 1 control for an indication in the centre of the green band; check that the level on pin 38 is 75mV p-p approximately.

(15) Using an oscilloscope, check the levels shown in Table 8.

TABLE 8  
Channel 1 audio levels

Monitor at:	Measured voltage (approx.)
TR12 collector	20mV p-p
TP2 on board	4V p-p

(16) Set the MODE switch to ISB-26 and, using an electronic voltmeter, check the levels shown in Table 9.

TABLE 9  
ISB-26 mode : voltage levels

Monitor at:	Measured voltage
pin 20 on board	+12V nom.
pin 29 on board	+12V nom.
TR50 collector	+5.5V

TABLE 9 (contd.)

Monitor at:	Measured voltage
TR53 collector	0V nom.
TR28 collector	0V nom.

If any of the above results are not obtained, check the appropriate transistor

(17) Transfer the audio signal generator to the LINE 2 jack socket. Set the METER switch to SET 2 and adjust the SET LINE 2 control for an indication in the centre of the green band; check, using an oscilloscope, that the level at pin 32 of the board is still 75mV p-p approximately.

(18) Using an oscilloscope, check the levels shown in Table 10.

TABLE 10

## Channel 2 audio levels

Monitor at:	Measured voltage (approx.)
TR13 collector	20mV p-p
TP3 on board	4V p-p

(19) In order to check the meter amplifier, measure the voltages, shown in Table 11, using an oscilloscope.

TABLE 11

## Meter amplifier : voltage levels

Monitor at:	Measured voltage (approx.)
pin 15 on board	75mV p-p
TR64 collector	1.5V p-p squarewave

25. To check the 1kHz c.w. oscillator, proceed as follows:

(1) Set the MODE switch to C.W.

(2) Check that pins 13 and 14 of TS1 (rear) are still linked.

(3) Using an oscilloscope, monitor at TP1 on the board; the level of the displayed waveform should be within the limits of 3.0V to 5.0V p-p, limiting on one peak and folding back 1.0V (approx.).

26. Similar checks to the above, for the remaining positions of the MODE switch, can be evolved by a reference to fig. 7 of Chap.1. and fig. 3 of Chap.8.

Control board PM.345

27. The localisation of a fault on the PM.345 board is revealed, to a large extent, by the tests given in para.10 to 13 of this chapter. It is recommended that the board-level tests in these paragraphs be carried out again referring to Table 12 which gives the areas of possible failure on the board.

TABLE 12  
Control board : area of failure

Para. reference	Check the following:
11	TR9, ML1(G9), ML3(G7), ML2, ML4, ML3(G1), TR2
12(2)	TR18
12(4)	TR10
12(7)	TR9, ML1(G9), TR8
12(10)	TR1, TR2
12(12)	TR9, ML1(G9), ML3(G7), ML2, TR3
13(14)	TR9, ML1(G9), ML3(G7), ML3(G10), TR12

28. Further tests can be evolved by referring to the technical description (Chap.9) and fig.7 of Chap.1. Tables 13 and 14 give the input and output pin functions, respectively, together with appropriate voltage levels.

TABLE 13  
Control board : input pin functions

Pin	Function	Input levels
6	Reduced power	0V : normal +12V : reduced power
1	Fault	+12V : normal 0V : fault
25,26	As for pin 27	
29	RESET switch	-4V : released +12V : depressed
13	STANDBY switch	-4V : released +12V : depressed
27	In-lock	+5V : in-lock 0V : out-of-lock
15	EHP switch	-4V : released +12V : depressed
24	MUTE select	+12V : selected -4V : not selected

TABLE 13 (contd.)

Pin	Function	Input levels
8	Ready	0V : ready +12V : not ready
17	TUNE select	+12V : 'tune' selected 0V : 'tune' not selected
21	C.W. mode selected	+12V : key 'down' 0V : key 'up'
19	P.T.T. line (Set to P.T.T.)	+12V : pressel operated 0V : pressel not operated

TABLE 14

Control board : output pin functions

Pin	Function	Output levels
4	RESET lamp	0V : 'on' +12V : 'off'
3	IN LOCK lamp	0V : 'on' +12V : 'off'
7	Reduced power lamp	0V : 'on' +12V : 'off'
5	Mute	0V : drive unit muted +12V : drive unit not muted
30	Coarse-tune-initiate	0V : normal +12V : coarse-tune-initiate
14	Standby switch	0V : depressed +12V : released
16	EHT switch	0V : depressed +12V : released
12	Command level to MODE switch	+12V : 'ready' condition 0V : 'tune' or 'not ready' condition
11	TUNE select	+12V : 'tune' selected 0V : 'tune' not selected
10	READY lamp	0V : 'on' +12V : 'off'



Noise-immunity board PM.346

29. Refer to fig.8 of Chap.7 and fig.8 of Chap.1 in order to ascertain the interconnecting points between the frequency selection switches and the PM.346 board. In order to check the PM.346 board, it is necessary to apply either +12V or open-circuit to each input pin and check for an inverted level at each corresponding output pin. This is accomplished by setting the frequency selection switches to certain positions and monitoring, with an electronic voltmeter, at the pins shown in Tables 15 to 20.

TABLE 15

Noise-immunity board check : MHz x 10 switch

Switch Setting MHz x 10	Pin			
	Input	Output	Input	Output
	48	47	42	41
1	+12V	0V	-4V	+5V
2	-4V	+5V	+12V	0V
Suspect transistor	TR24		TR21	

TABLE 16

Noise-immunity board check : MHz x 1 switch

Switch Setting MHz x 1	Pin							
	Input	Output	Input	Output	Input	Output	Input	Output
	40	39	38	37	36	35	34	33
8	-4V	+5V	+12V	0V	+12V	0V	+12V	0V
7	+12V	0V	-4V	+5V	+12V	0V	+12V	0V
5	+12V	0V	+12V	0V	-4V	+5V	+12V	0V
1	+12V	0V	+12V	0V	+12V	0V	-4V	+5V
Suspect transistor	TR20		TR19		TR18		TR17	

TABLE 17

Noise-immunity board check : kHz x 100 switch

Switch Setting kHz x 100	Pin							
	Input	Output	Input	Output	Input	Output	Input	Output
	32	31	30	29	28	27	26	25
1	-4V	+5V	+12V	0V	+12V	0V	+12V	0V
2	+12V	0V	-4V	+5V	+12V	0V	+12V	0V
4	+12V	0V	+12V	0V	-4V	+5V	+12V	0V
8	+12V	0V	+12V	0V	+12V	0V	-4V	+5V
Suspect transistor	TR16		TR15		TR14		TR13	

TABLE 18

Noise-immunity board check : kHz x 10 switch

Switch Setting kHz x 10	Pin							
	Input	Output	Input	Output	Input	Output	Input	Output
	24	23	22	21	20	19	18	17
1	-4V	+5V	+12V	0V	+12V	0V	+12V	0V
2	+12V	0V	-4V	+5V	+12V	0V	+12V	0V
4	+12V	0V	+12V	0V	-4V	+5V	+12V	0V
8	+12V	0V	+12V	0V	+12V	0V	-4V	+5V
Suspect transistor	TR12		TR11		TR10		TR9	

TABLE 19

Noise-immunity board check : kHz x 1 switch

Switch Setting kHz x 1	Pin							
	Input	Output	Input	Output	Input	Output	Input	Output
	16	15	14	13	12	11	10	9
1	-4V	+5V	+12V	0V	+12V	0V	+12V	0V
2	+12V	0V	-4V	+5V	+12V	0V	+12V	0V
4	+12V	0V	+12V	0V	-4V	+5V	+12V	0V
8	+12V	0V	+12V	0V	+12V	0V	-4V	+5V
Suspect transistor	TR8		TR7		TR6		TR5	

TABLE 20

Noise-immunity board check : Hz x 100 switch

Switch Setting Hz x 100	Pin							
	Input	Output	Input	Output	Input	Output	Input	Output
	8	7	6	5	4	3	2	1
1	-4V	+5V	+12V	0V	+12V	0V	+12V	0V
2	+12V	0V	-4V	+5V	+12V	0V	+12V	0V
4	+12V	0V	+12V	0V	-4V	+5V	+12V	0V
8	+12V	0V	+12V	0V	+12V	0V	-4V	+5V
Suspect transistor	TR4		TR3		TR2		TR1	

34MHz generator board PM.344

30. Initially, check that the input at pin 8 of the board is approximately 1V p-p at 5MHz; use an oscilloscope. Carry out the voltage checks given in Table 21.

TABLE 21

34MHz generator board : voltage levels

Monitor at:	Test equipment	Measured voltage
Board pin 10	Oscilloscope	1V p-p, 1MHz squarewave
Board pin 12	Oscilloscope	4V p-p, 1MHz squarewave
TR4, collector	Oscilloscope	2V p-p
ML1, pin 6	Oscilloscope	4V p-p
ML2, pin 8	Oscilloscope	2V p-p, 2:3 mark/space ratio, 1MHz squarewave
ML4, pin 8	Oscilloscope	4V p-p, 3:2 mark/space ratio, 1MHz squarewave
ML6, pin 6	Oscilloscope	4V, 1MHz, negative-going spikes, approx. 30ns width
Board, pin 2	Multimeter	+4V d.c. *
TR5, collector	Oscilloscope	4V p-p, 5MHz squarewave
ML6b, pin 8	Oscilloscope	4V p-p, 1MHz squarewave
Board pin 8	Oscilloscope	1V p-p, 5MHz
TR3, base	Multimeter	+1.7V d.c. approx.
TR3, collector	Oscilloscope	4V p-p (approx.), 5MHz
TR1, emitter	Multimeter	+5V d.c.

\* As necessary, adjust the core of inductor L1 to obtain this value.

31. Check the v.c.o. switching stage (para.29) as follows. Set the MHz x 10 and MHz x 1 switches to each 'MHz' setting from 0 to 29 and monitor pins 20, 19 and 21 with a multimeter; refer to Table 22 for the measured results.

TABLE 22

34MHz generator board : v.c.o. switch output check

MHz settings	Output pins		
	21	19	20
0 to 7MHz	0	1	1
8 to 17MHz	1	0	1
18 to 29MHz	1	1	0

Logic '1' = +14V nom.

Logic '0' = 0V nom.

32. If the results in Table 22 are not obtained, check the input levels to the v.c.o. switching stage (fig. 1). Allow for the logic inversion in the noise-immunity board and also refer to fig.6 of Chap.7. The frequency settings of particular interest are those at 7MHz, 8MHz, 17MHz and 18MHz; Table 23 gives the input levels for these frequency settings. If these input levels are correct, a fault exists in the v.c.o. switching stage; if not, the fault may be on the noise immunity board or in the inter-wiring.

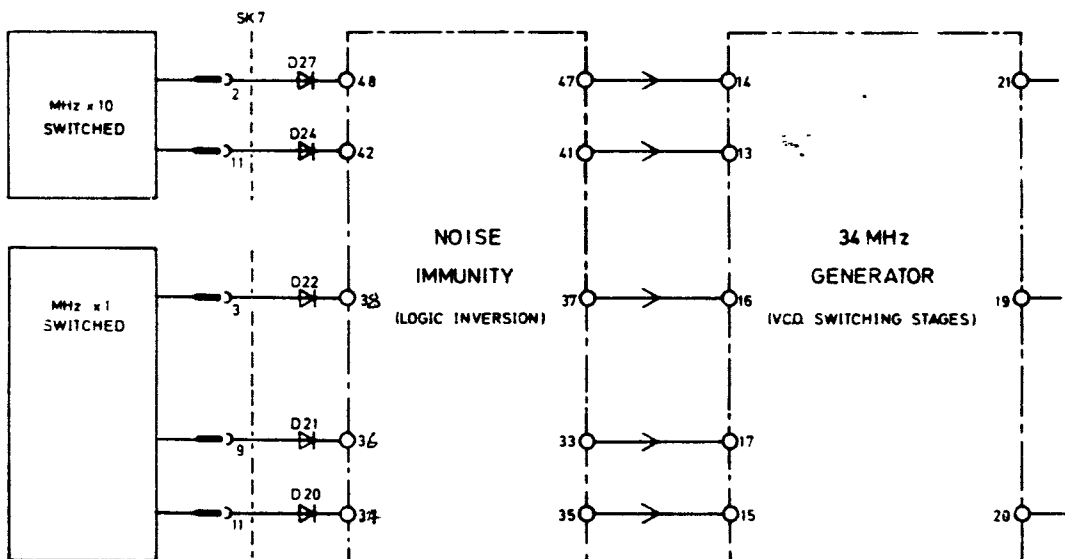


Fig.1 Input paths to v.c.o. switching stage

TABLE 23

34MHz generator board : v.c.o. switch input check

MHz setting	Input pins				
	14	13	16	17	15
7	1	1	1	0	0
8	1	1	0	0	0
17	0	1	1	0	0
18	0	1	0	0	0

Logic '1' = +5V nom.

Logic '0' = 0V nom.

H.F. loop board PS.337/3

33. Set the two MHz thumbwheel switches to the following 1MHz settings and check that the correct oscillator is being selected by monitoring at the pins shown in Table 24; if not, a fault may exist on the PM.344 board (para.27).

TABLE 24

H.F. loop board : v.c.o. selection

MHz setting	Pin	Multimeter reading
0 to 7MHz	28	0V
8 to 17MHz	27	0V
18 to 29MHz	26	0V

34. Check that the selected v.c.o. is functioning by monitoring, with an oscilloscope, for 3V p-p at TP4 on the h.f. loop board.

35. Carry out the following voltage checks throughout the board; these checks should locate a fault to a stage and, in some instances, a component.

(1) Using a multimeter, set to the 25V d.c. range, monitor the following test points (negative to 0V):-

(a) TP1: MHz switch set to 7MHz :  $+14V \pm 1V$ .

(b) TP2: MHz switch set to 17MHz :  $14V \pm 1V$ .

(c) TP3: MHz switch set to 27MHz :  $+14V \pm 1V$ .

(2) Set the MHz switches to 27. Use the multimeter to measure the following voltages with respect to chassis (0V); observe the correct polarity.

(a) Emitter TR9: -0.7V d.c.

(b) Base TR10: +2.4V d.c.

(c) Emitter TR10: +1.7V d.c.

(3) Use the oscilloscope to monitor the collector of TR9 for 600mV p-p at 52.4 to 65.4MHz.

- (4) Set the kHz controls to 9999. Monitor TP4 using the electronic voltmeter. Step the MHz switches through each position and check that the electronic voltmeter indication is 1V r.m.s.  $\pm$  2.5dB.
- (5) Monitor at TP5 for 1V r.m.s., using the electronic voltmeter.
- (6) Connect a frequency counter, in turn, to TP4 and TP5; check that the frequency at TP5 is one-half that at TP4; the MHz switch setting is arbitrary. The voltage at the collector of TR12 is a squarewave having an excursion from +0.4V to +3V (min.).
- (7) Use the oscilloscope to monitor the test points listed below.
  - (a) TP6: 442 to 474 kpps strobe pulses, negative-going, 3.5V p-p (approx.).
  - (b) TP7 and TP8: 442 to 474 kpps phase-comparator output pulses, negative-going and in phase with (a), 3.5V p-p (approx.).
- (8) Ensure that the kHz controls are set to 9999 and connect the multimeter, set to the 10V d.c. range, between TP10 (positive) and chassis (0V); check for a reading of +3.5V d.c.
- (9) Use the oscilloscope to monitor the following:
  - (a) TP12: 885 to 948kHz, approximate squarewave 4V p-p.
  - (b) ML12, pin 5: half of transfer oscillator frequency, 4V p-p.
  - (c) Board pin 13: 885 to 948kHz, 1V p-p.
  - (d) Board pin 12: logic '1' in-lock; logic '0' out-of-lock.
- (10) Use the multimeter to check the voltage at the collector of TR19 which should be between +3V and +14V d.c. when the loop is locked. When TP7 has a pulse of cyclically varying width, the voltage should be approximately +2.3V d.c.; when TP8 has a pulse of cyclically varying width, the voltage should be approximately +19V d.c.
- (11) Use the oscilloscope to check the lock indicator. When the loop is locked, TP9 and TP11 should have negative-going pulses of 1.5 $\mu$ s duration at a p.r.f. of approximately 400kHz. When the loop is out-of-lock, the pulse of cyclically varying width at TP7 or TP8 should also appear at TP12 except during the period of the negative-going 1.5 $\mu$ s pulse at TP9 and TP11.

#### Transfer loop board PS.338

36. The following in-situ checks assume that the transfer loop oscillator, on the h.f. hoop board, is functioning correctly.
37. Use an oscilloscope to check the following levels:
  - (1) TP1: 4.6 to 3.6MHz squarewave, 5V p-p.
  - (2) TP2: 115 to 52kHz squarewave, 4V p-p.
  - (3) TP3: 115 to 52 kpps, negative-going, 4V p-p, pulse width of 50ns approximately.
  - (4) TP4 and TP5: 115 to 52 kpps, 3 microsecond negative-going, and in phase with (3), 4V p-p.
  - (5) TP6: 115 to 52 kpps strobe pulse, negative-going, 4V p-p, pulse width of 300ns approximately.
  - (6) Board pin 21: 1MHz, 750mV p-p.
  - (7) Collector TR2: 1MHz, 500mV p-p.

- (8) Board pin 19: 885 to 948kHz, 1V p-p.
  - (9) ML3 pin 4: 885 to 948kHz, 1V p-p.
  - (10) Board pin 17: 4.6 to 3.6MHz, 800mV p-p.
  - (11) Junction C35/L11: 400mV p-p, 115kHz to 52kHz.
  - (12) Board pin 6: Logic '1' in-lock; logic '0' out-of-lock.
38. (1) Use the multimeter to check the voltage at board pin 4. In the 'lock' condition, this should be in the range +3V to +8V d.c. When pin 6 of ML8 has a pulse of cyclically varying width, this voltage should be approximately +11V d.c. (out-of-lock condition).
- (2) Use the oscilloscope to check the lock indicator. In the 'lock' condition the signals at TP4 and TP5 should be negative-going pulses with an excursion of +3V to +0.4V and a duration of 3 $\mu$ s. In the out-of-lock condition, the pulse of cyclically varying width at TP3, or pin 6 of ML8, should also appear at pin 6 of the transfer loop board except during the period of the negative-going 3 $\mu$ s pulse at TP4 and TP5.

#### L.F. loop board PM.349

39. Carry out the following voltage checks:
- (1) Use the multimeter to check the oscillator supply; the voltage at the emitter of transistor TR1 should measure +5V d.c.  $\pm$  0.25V.
  - (2) Use the oscilloscope to check the oscillator output at TP1 which should be a TTL squarewave signal in the frequency range 18-23MHz.
  - (3) Use the oscilloscope to check the strobe pulse at TP4 which should be negative-going pulses with a duration of 80-100ns.
  - (4) Use the oscilloscope to check the strobe pulse at TP2 which should be positive-going pulses of approximately 50ns duration. If the positive-going 50ns pulses are not obtained at TP2, the input and output pins of ML5, ML8, ML13 and ML16 should be monitored to isolate the faulty module in the divider chain.
  - (5) Use the oscilloscope to check the divide-by-five stage ML2; the TTL signal at pin 2 of ML2 should be in the frequency range 3.6 - 4.6MHz.
  - (6) Transfer the oscilloscope to pin 12 of ML1 to check the buffer stage, gate G1 of ML1; the signal should be in the frequency range 3.6 - 4.6MHz.
  - (7) Use the oscilloscope to check the divide-by-2000 stage at TP3; the signal should be a 500Hz squarewave. If the 500Hz squarewave is not obtained at TP3, the input and output pins of ML3, ML4, ML7 and ML10 should be monitored to isolate the faulty module in the divider chain.
  - (8) Use the oscilloscope to check the phase-comparator outputs. Positive-going pulses of 50ns duration should be obtained at the Q outputs (pin 5 and pin 9) of ML12A and ML12B when the loop is locked. In the out-of-lock condition, pin 5 or pin 9 should have a positive-going 50ns pulse whilst the other pin should have a pulse of cyclically varying width.
  - (9) Use the multimeter to check the supply to the varactor line driver at the emitter of transistor TR10; the voltage should be +19.5V d.c.  $\pm$  0.5V.
  - (10) Transfer the multimeter to check the varactor line driver at TP5. When the loop is locked, the voltage should be between +3.5V and +15V d.c. depending on the frequency selected. When the Q output (pin 5) of ML12A has the pulse of cyclically varying width, the voltage should be approximately +2V d.c. When the Q output (pin 9) of ML12B has the pulse

of cyclically varying width, the voltage should be approximately +18V d.c.

- (11) Use the oscilloscope to check the 1.4MHz generator; the signal at pin 9 of ML3 should be a squarewave with an excursion from +0.4V to at least +3V p-p.
- (12) Transfer the oscilloscope to the base of TR3; a sinewave signal of approximately 500mV p-p should be obtained.
- (13) Transfer the oscilloscope to pins 1 and 2 of the board. The output of the 1.4MHz generator should be approximately 640mV p-p when the generator is correctly terminated.



## Chapter 4

## REPAIR

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INTRODUCTION

1. The information in this chapter covers the removal and refitting of sub-assemblies and printed-circuit boards; where not obvious, the procedure for removing certain components is also given. It is assumed that the drive unit is placed on a bench.

2. The location of sub-assemblies and printed-circuit boards is shown in fig.2 and 3 of Chap.4.

REMOVAL AND REFITTING OF FREQUENCY STANDARD

3. (1) Remove the top cover to the chassis (10 quick-release fasteners).
- (2) Remove the four screws securing the plate on which the frequency standard assembly is mounted (fig.2, Chap.1).
- (3) Withdraw, vertically, the assembly; there is sufficient cable beneath to allow this to be done.
- (4) Remove the connector from beneath the mounting plate.
- (5) Remove the screws securing the mounting plate to the frequency standard.
- (6) Refitting is the reverse of the above procedure.

REMOVAL AND REFITTING OF BOARDSMixer and output board PM.342

4. The following transistors are physically mounted in 'cup' type heatsinks secured, and electrically insulated from, the chassis casting; TR2, TR3, TR5, TR6, TR8 to TR13 and TR15. These transistors protrude through holes in the

board and are wired to terminals on the board. Any one of the transistors is removed by unsoldering the leads and gently easing the component out of the heat-sink by gripping the leads with pliers.

5. The PM.342 board is removed as follows:

- (1) Remove the chassis top cover (10 quick-release fasteners).
- (2) Remove the eight board fixing screws.
- (3) Unsolder all connecting leads, noting the colour code and board terminal number.
- (4) Using a pair of pliers, very carefully ease out of the chassis-mounted heat-sink all the transistors referred to in para.4. This should be progressively carried out, in turn, for all the transistors until the board is free.
- (5) Raise the board vertically until it is clear of the webbs in the casting.

CAUTION...

This board must be handled with care as it may easily be damaged by bending or dropping.

- (6) Refitting is the reverse of the above instructions.

#### Control board PM.345 and low-level board PM.341

6. (1) Remove the chassis top cover (10 quick-release fasteners).
- (2) Remove all fixing screws.
- (3) Unsolder all connecting leads, noting the colour code and board terminal number.
- (4) Remove the board.
- (5) Refitting is the reverse of the above instructions.

#### Power supply board PM.343

7. Refer to fig.3 of Chap.1.
  - (1) Remove the four screws securing the cover.
  - (2) Loosen the two screws securing the bracket holding TB2, and withdraw TB2.
  - (3) Unsolder all connecting leads, noting the colour code and board terminal number.
  - (4) Withdraw the board.
  - (5) Refitting is the reverse of the above instructions.

#### Remaining boards

8. The remaining boards are all removed in the same manner. Note that only one screening cover encloses the transfer loop and h.f. loop boards.

- (1) Remove the screws securing the cover.
- (2) Remove the screws securing the board.

(3) Unsolder all connecting leads, noting the colour code and board terminal number.

(4) Withdraw the board.

**CAUTION...**

The h.f. loop board must be handled with care as it may easily be damaged by bending or dropping.

(5) Refitting is the reverse of the above instructions.

Diode board PS.581

9. Refer to fig.3 of Chap.1.

(1) Remove the cover enclosing the l.f. loop and noise-immunity boards.

(2) Remove the board securing screws.

(3) Withdraw the board on its cable harness.

(4) Unsolder all connecting leads, noting the colour code and board terminal number.

(5) Refitting is the reverse of the above procedure.

Line decoupling board PS.392

10. Refer to fig.2 of Chap.1.

(1) Remove the chassis top cover (12 securing screws).

(2) Remove the board securing screws.

(3) Unsolder all connecting leads, noting the colour code and board terminal number.

(4) Refitting is the reverse of the above procedure.

Front panel

11. (1) Disconnect SKT1 and PL1 (fig.2, Chap.1).

(2) Unsolder the lead to the front-panel R.F. MON. socket.

(3) Remove the four screws securing the front panel to the two chassis side members.

(4) Refitting is the reverse of the above procedure.

Miscellaneous components

12. The method is self-evident for the unsoldering and removal of the various chassis-mounted components. When replacing any one of the power transistors TR1 to TR4, it is necessary to also remove the appropriate heat-sink (chassis rear) before unsoldering leads.

## Chapter 5

## ALIGNMENT

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INTRODUCTION

1. This chapter gives alignment procedures for the filters contained within the drive unit. The two filters which it is possible for maintenance units to align are both on the mixer and output board PM.342. Alignment of the two sideband filters is not possible. Reference should be made to Chap.8 for the component layout and circuit diagrams for the mixer and output board; reference to illustrations in Chap.1 gives the location of the board.

TEST EQUIPMENT

2. Refer to Chap.3 for the complete list of test equipment required to service the drive unit. The items required for filter alignment are:

- (1) Electronic voltmeter 10S/6625-99-193-4355.
- (2) Signal generator (40MHz) 10S/6257379.

PRELIMINARY REQUIREMENTS

3. It is assumed that the drive unit has been placed on a bench with access to the chassis top, and with the dust cover removed. Both filter alignment procedures are most conveniently carried out in-situ; however, certain links on the board have to be removed and refitted using a soldering iron. It is not necessary to connect the drive unit to a mains voltage supply.

35.4MHz BAND-PASS FILTER ALIGNMENT

4. (1) Unsolder the wire links between terminals 1 and 2 and terminals 29 and 27 on the mixer and output board.

Note...

The two lengths of 50-ohm coaxial cable (operations (2) and (3)) required for connecting test equipment must be as short as possible in order to avoid interaction; crocodile clips must not be used for connection to the board terminals.

- (2) Using a short length of coaxial cable, and a soldering iron, connect the signal generator (50-ohm output) to terminal 2 (inner) and terminal 3 (screen) on the board.
- (3) Using a short length of coaxial cable, and a soldering iron, connect the electronic voltmeter (50-ohm input) to terminal 29 (inner) and terminal 28 (screen) on the board.
- (4) Set the signal generator frequency to 35.4 MHz with an output level of 1 volt r.m.s.
- (5) Adjust the electronic voltmeter range to obtain a reading.
- (6) Adjust the cores of L2 to L7, in turn, for a maximum reading on the electronic voltmeter; repeat until optimum results are obtained.
- (7) Ensure that the output indicated on the electronic voltmeter is not more negative than minus 7 dB relative to 1 volt. Note the voltage.
- (8) Set the signal generator to 34.0 MHz with an output level of 1 volt r.m.s.
- (9) Ensure that the output indicated on the electronic voltmeter is not less negative than minus 55 dB relative to 1 volt.
- (10) Set the signal generator to 32.6 MHz with an output level of 1 volt r.m.s.
- (11) Ensure that the output indicated on the electronic voltmeter is not less negative than minus 65 dB relative to 1 volt.
- (12) Unsolder the coaxial leads and link terminals 1 and 2 and terminals 29 and 27 using bare tin copper wire.

### 30 MHz LOW-PASS FILTER ALIGNMENT

5. (1) Unsolder the wire links between terminals 30 and 31 and terminals 19 and 20 on the mixer and output board.

Note...

The two lengths of 50-ohm coaxial cable (operations (2) and (3)) required for connecting test equipment must be as short as possible in order to avoid interaction; crocodile clips must not be used for connections to the board terminals.

- (2) Using a short length of coaxial cable, and a soldering iron, connect the signal generator (50-ohm output) to terminal 30 (inner) and terminal 32 (screen) on the board.
- (3) Using a short length of coaxial cable, and a soldering iron, connect the electronic voltmeter (50-ohm input) to terminal 20 (inner) and terminal 18 (screen) on the board.
- (4) Adjust the electronic voltmeter range to obtain a reading.

- (5) Set the signal generator frequency to 37.42 MHz with an output level of 1 volt r.m.s. Adjust the electronic voltmeter range to obtain a reading.
- (6) Adjust L9 for minimum meter reading.
- (7) Set the signal generator frequency to 35.5 MHz.
- (8) Adjust L10 for minimum meter reading.
- (9) Set the signal generator frequency to 44.17 MHz.
- (10) Adjust L11 for minimum meter reading.
- (11) Set the signal generator frequency to 30 MHz; adjust L8 for maximum meter reading.
- (12) Repeat operations (5) to (11) twice.
- (13) Sweep the signal generator frequency from 1 MHz to 30 MHz. Note the frequency which produces maximum output and note the maximum output level.
- (14) Sweep the signal generator frequency from 1 MHz to 30 MHz. Ensure that the output remains within 1 dB of the level noted in operation (13). If necessary re-adjust L8.
- (15) Set the signal generator frequency to 35.4 MHz with an output level of 1 volt r.m.s.
- (16) Ensure that the output indicated on the electronic voltmeter is not less negative than minus 55 dB relative to the level noted in operation (13).
- (17) Sweep the signal generator frequency from 35.4 MHz to 65.4 MHz and ensure that the output remains not less negative than minus 55 dB.
- (18) Unsolder the coaxial leads and link terminals 20 and 19 and terminals 30 and 31 using bare tin copper wire.

## Chapter 6

## OVERALL PERFORMANCE TESTS AND ADJUSTMENTS

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INTRODUCTION

1. This chapter gives post-repair adjustment procedures and checks for the boards within the drive unit. Following repair work to the drive unit, carry out the setting-up procedures given in Chap.2 and appropriate performance checks on the linear amplifier.

ADJUSTMENTSPreliminary procedure

2. The drive unit must be placed on a bench with its top and bottom covers removed (Chap.4).

- (1) Connect a 50-ohm dummy load to the r.f. output socket (SKT4) on the rear of the unit.
- (2) Connect the unit to a suitable mains voltage supply.
- (3) Check that both the SUPPLY and STANDBY pushbuttons are released to the 'off' positions.
- (4) Set the TUNE/MUTE/OPERATE switch to OPERATE HIGH.
- (5) Set the MODE switch to C.W.

- (6) Set the VOX/PTT/TX switch to TX.
- (7) Link pins 13 and 14 of TS1 (rear).
- (8) Set the LOCAL/EXTENDED/REMOTE switch to LOCAL SYNTH.

### Regulator board PM343

3. (1) Depress the SUPPLY pushbutton.

Note...

It is not necessary, under these conditions, to depress the STANDBY pushbutton.

- (2) Connect a multimeter to TB2 (Chap.1, fig.3) and make the adjustments given in Table 1; refer to Chap.9, fig.5.

TABLE 1

Regulator board PM343: adjustments

Connect to TB2, pins:	Adjust	Measured voltage
1 or 2 and E	R12	-7V $\pm$ 0.25V
3 or 4 and E	R9	+5V $\pm$ 0.25V
5 or 6 and E	R23	+12V $\pm$ 0.25V
7 or 8 and E	R22	+20V $\pm$ 0.25V

- (3) Disconnect the multimeter and release the SUPPLY pushbutton.

### Frequency standards (9400 and 9420)

4. The conditions of para.2 are to be set up.

- (1) Place the drive unit on its side on the bench.
- (2) Connect a frequency counter between pin 8 of the 34MHz generator board (Chap.7, fig.9) and chassis.
- (3) Connect an oscilloscope across the counter.
- (4) Depress the SUPPLY pushbutton and allow approximately 30 minutes to elapse before making the following measurements.
- (5) Check that the oscilloscope displays 800mV p-p.
- (6) Set the counter to measure 5MHz; refer to the appropriate publication
- (7) In order to display the least significant digit, utilize the 'overspill' facility.
- (8) Check that the displayed count is either 999999  $\pm$  1Hz or 000000  $\pm$  1Hz. If necessary, remove the rubber plug (top of frequency standard unit) and adjust for the correct displayed count.
- (9) Release the SUPPLY pushbutton.

### L.P. loop board PM349

5. The conditions of para.2 are to be set up.

- (1) Depress the SUPPLY pushbutton.
- (2) Set the six frequency selector switches to 000000 and depress the RESET pushbutton.



- (3) Connect a multimeter between TP5 (+) and chassis; refer to Chap.7, fig.11.
- (4) Adjust L2 on the PM349 board for a multimeter indication of +15V d.c
- (5) Reset the six frequency selector switches to 299999, depress the RESET pushbutton and check that the multimeter indication is +3.5V d.c.
- (6) Disconnect the multimeter and release the SUPPLY pushbutton.

#### H.F. loop board PS337/3

6. The conditions of para.2 are to be set up.
  - (1) Depress the SUPPLY pushbutton.
  - (2) Set the six frequency selector switches to an arbitrary setting and depress the RESET pushbutton.
  - (3) Connect an oscilloscope to TP4; refer to Chap.7, fig.15.
  - (4) Adjust R38 on the PS337/3 board for a display of 3V p-p.
  - (5) Disconnect the oscilloscope.
  - (6) Connect an electronic voltmeter to pin 22 of the PS337/3 board.
  - (7) Adjust R44 on the board for a meter indication of 225mV r.m.s. (OdBm into 50 ohms).
  - (8) Connect the electronic voltmeter to pin 18 of the board.
  - (9) Set the frequency selector switches to 299999 and depress the RESET pushbutton.
  - (10) Adjust L20 on the board for a meter indication of +8V d.c.
  - (11) Connect the electronic voltmeter to the collector of TR19.
  - (12) Make the adjustments at the given frequency settings shown in Table 2; depress the RESET pushbutton after each change in frequency.

TABLE 2

H.F. loop board PS337/3: adjustments

Frequency setting	Adjust	Measured voltage
069999	L4	+14V d.c.
179999	L5	+14V d.c.
299999	L6	+14V d.c.

- (13) Release the SUPPLY pushbutton and disconnect the voltmeter.

#### Drive unit mode levels

7. The entire following procedure must be carried out after repair and/or replacement of either the low-level board PM341 (Chap.8, fig.2) or the mixer and output board PM342 (Chap.8, fig.4). The procedure embraces the following particular adjustments:

- (1) R.F. output level of 200mW.
- (2) A.F. line input levels.
- (3) Channels 1 and 2 a.f. gain.

- (4) Vox sensitivity.
  - (5) A.F. meter sensitivity.
  - (6) R.F. meter sensitivity.
8. The drive unit must be placed on a bench and the top cover removed.
- (1) Connect a 50-ohm dummy load to the r.f. output socket (SKT4) on the rear.
  - (2) Connect the unit to a suitable mains voltage supply.
  - (3) Check that both the SUPPLY and STANDBY pushbutton are released to the 'off' positions.
  - (4) Set the TUNE/MUTE/OPERATE switch to OPERATE HIGH.
  - (5) Set the MODE switch to AM-6 and the sideband switch to UPPER.
  - (6) Set the VOX/PTT/TX switch to TX.
  - (7) Set the LOCAL/EXTENDED/REMOTE switch to LOCAL SYNTH.
  - (8) Connect an electronic voltmeter across the 50-ohm dummy load at SKT4.
  - (9) Depress the SUPPLY pushbutton.
9. (1) Adjust T6 on the PM341 board (Chap.8, fig.2) for a maximum voltmeter indication.
- (2) Adjust L2, L3, L4, L6 and L7 on the mixer and output board (Chap.8, fig.4) for a maximum voltmeter indication.
  - (3) Adjust R70 on the mixer and output board for a voltmeter indication of 1.6V r.m.s.
  - (4) Set the front-panel meter switch to R.F. and adjust R64 on the PM342 board for a front-panel meter indication of -6dB.
  - (5) Set the MODE switch, in turn, to SSB-16 and SSB-26, and check that the voltmeter reading reduces by 10dB  $\pm$  1dB and 20dB  $\pm$  1dB respectively.
  - (6) Connect an audio signal generator to the LINE 1 jack socket on the front panel; refer to fig.6, Chap.1 for method of connecting to the audio line terminals of the jack plug.
  - (7) Set the MODE switch to SSB-SUPP.
  - (8) Adjust the generator output level to 0dBm at 1kHz and 600 ohms.
  - (9) Set the METER switch to LINE 1.
  - (10) Adjust R195 on the low-level board (Chap.8, fig.2) for a front-panel meter indication of 0dBm.
  - (11) Set the front-panel SET LINE 1 control fully counter-clockwise.
  - (12) Set the METER switch to SET 1.
  - (13) Adjust the SET LINE 1 control for a front-panel meter indication of 0dBm.
  - (14) Set the METER switch to R.F.
  - (15) Increase the generator output level by 10dB.
  - (16) Adjust R73 on the low-level board for a front-panel meter reading of 200mW.
  - (17) Alternate the setting of the SIDEBAND switch between UPPER and LOWER and adjust, in turn, R175 and R176 respectively in order to obtain 200mW meter readings for each switch position.

(18) Decrease the generator output by 20dB and check that the voltmeter reading reduces by not more than 1.5dB.

10. (1) Set the VOX/PTT/TX switch to VOX.  
 (2) Set R79 on the low-level board to the maximum counter-clockwise position and check that, after 2 seconds, the drive unit output indication is muted to zero.  
 (3) Turn R79 clockwise until the drive unit de-mutes.

Note ...

For normal speech inputs, the clockwise setting of R79 may have to be increased slightly.

11. (1) Reset the generator output level to 0dB.  
 (2) Set the VOX/PTT/TX switch to TX.  
 (3) Set the MODE switch to ISB-26 and check that the output level falls by 6dB.
12. (1) Connect the generator output to the LINE 2 front-panel jack socket.  
 (2) Set the METER switch to LINE 2 and check that the front-panel meter reading is 0dBm.  
 (3) Set the METER switch to SET 2 and adjust the SET LINE 2 control for a 0dBm reading on the front-panel meter.  
 (4) Set the METER switch to R.F.  
 (5) Increase the generator output level by 10dB.  
 (6) Adjust R75 on the low-level board for a reading of -6dB relative to the 200mW front-panel meter setting.  
 (7) Set the TUNE/MUTE/OPERATE switch to TUNE.  
 (8) Set the MODE switch to C.W.  
 (9) Adjust R204 on the low-level board for a reading of 6dB below 200mW.  
 (10) Set the TUNE/MUTE/OPERATE switch to OPERATE LOW.  
 (11) Adjust R190 on the low-level board until the front-panel meter reading is -6dB relative to 200mW.  
 (12) Release the SUPPLY pushbutton.

#### 1kHz tone oscillator

13. The conditions of para. 2 are to be set up.
- (1) Depress the SUPPLY pushbutton and set the frequency selector switches to 2000000.  
 (2) Adjust R65 on the low-level board for a front-panel meter reading of 200mW.  
 (3) Connect a frequency counter across the dummy load at the r.f. output SK4.  
 (4) The frequency display should be 1.999000MHz; if necessary, adjust T1 on the low-level board.  
 (5) Release the SUPPLY pushbutton and disconnect the test equipment.

- (6) Set the Mode switch to C.W.
- (7) Check that pins 13 and 14 of TS1 (rear) are still linked.
- (8) Using an oscilloscope, monitor at TP1 on the board; the level of the displayed waveform should be within the limits of 3.0V to 5.0V p-p. limiting on one peak and folding back 1.0V (approx).
- (9) Adjust R69, if necessary, to meet the above conditions.

#### R.F. output level

14. If an r.f. output level of less than 200mW is required, then adjust R70 (low-level board) accordingly.

## Chapter 7

## CIRCUIT DESCRIPTION OF SYNTHESIZER

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INTRODUCTION

1. This chapter contains a circuit description of those boards in the drive unit which combine to provide the synthesizer function. The principle of operation of the synthesizer is contained in Chap. 1. The synthesizers are identical in the MA.1720A and MA.1720S drive units with the exception of the frequency standard which is a Type 9400 (MA.1720A) or 9420 (MA.1720S); the Type 9420 has higher stability characteristics.

2. The synthesizer consists of the following sub-assemblies:-

- (1) Frequency standard (5 MHz).
- (2) 34 MHz generator board PM.344.
- (3) L.F. loop board PM.349.
- (4) H.F. loop board PS.337/3, or PS.337/4.
- (5) Transfer loop board PS.338
- (6) Noise immunity board PM.346

The interconnection diagram in Chap. 1 shows the interconnections between all the synthesizer sub-assemblies.

3. The frequency selection switches and the noise immunity board are described in this chapter because they are an essential part of the synthesizer.

FREQUENCY STANDARD

4. The fast-warm-up frequency standard sub-assembly produces a 5 MHz high-stability output which is applied to the 34 MHz generator board.

5. This is a fourth-line repairable unit hence no technical information is given in this publication.

FREQUENCY SELECTION SWITCHES (fig. 6)

6. There are six frequency selection switches each with a +12V input line and four output lines; the output lines are at a level of +12V or open-circuit depending upon the switch settings. The binary-coded decimal output from each switch is nines-complemented and inverted for the MHz x 10 and MHz x 1 switches; an inverted BCD output is provided by the kHz x 100, kHz x 10, kHz x 1 and Hz x 100 switches. Table 1 summarises the logic output levels as related to the switch decimal settings.

7. The switch output lines are routed via a noise immunity board PM.346 to the programmed dividers on the l.f. loop board, the h.f. loop board and the transfer loop board.

TABLE 1

Frequency selection switches: logic output levels

		Switch setting (decimal)*									
		0	1	2	3	4	5	6	7	8	9
Binary	2 <sup>0</sup>	0	1	0	1	0	1	0	1	0	1
	2 <sup>1</sup>	0	0	1	1	0	0	1	1	0	0
	2 <sup>2</sup>	0	0	0	0	1	1	1	1	0	0
	2 <sup>3</sup>	0	0	0	0	0	0	0	0	1	1
Inverted binary (100 Hz, 1 kHz 10 kHz, & 100 kHz switches)	2 <sup>0</sup>	1	0	1	0	1	0	1	0	1	0
	2 <sup>1</sup>	1	1	0	0	1	1	0	0	1	1
	2 <sup>2</sup>	1	1	1	1	0	0	0	0	1	1
	2 <sup>3</sup>	1	1	1	1	1	1	1	1	1	0
Inverted 9's complemented binary (1 MHz & 10 MHz switches)	2 <sup>0</sup>	0	1	0	1	0	1	0	1	0	1
	2 <sup>1</sup>	1	1	0	0	1	1	0	0	1	1
	2 <sup>2</sup>	1	1	0	0	0	0	1	1	1	1
	2 <sup>3</sup>	0	0	1	1	1	1	1	1	1	1

\* Logic 0 = open circuit  
Logic 1 = +12V

\*\* Not used in  
MHz x 10 switch

NOISE IMMUNITY BOARD PM.346 (fig. 8)

8. The function of the noise immunity board is to prevent random operation on any of the 22 frequency selection lines by noise or r.f. signals picked up on the lines.

9. The board contains 22 identical stages (one for each frequency selection line) which accept +12V for 'select' and open-circuit for 'non select'. The input line to each circuit is taken via a 4.7k ohm resistor to the -7V rail (earth clamp diodes in the transistor base circuits prevent reverse base/emitter voltage breakdown) and thus a voltage greater than approximately 8V (relative to -7V) must be applied to the input line before the transistor will conduct.

10. The outputs of the board are taken from the collectors of transistors to the inputs of the three programmed dividers; selection of a line causes the associated transistor to conduct and apply logic '0' to the divider input.

#### 34 MHz GENERATOR BOARD PM.344 (fig. 10)

11. The main function of the 34 MHz generator board is to produce a 34 MHz sinewave output at a level of 0 dBm. The board contains the following stages, and a block diagram is shown in fig. 1.

(1) 34 MHz oscillator with output buffers and filter.

(2) Divide-by-34 stage to produce a nominal 1 MHz squarewave from one of the outputs of (1), for internal use on the board by the phase-comparator.

(3) Amplifier and squarer for the 5 MHz reference frequency input, followed by a divide-by-5 stage and output buffers.

(4) Phase detector circuits to compare the outputs of (2) and (3), produce a control voltage for locking the frequency of (1) accurately on 34 MHz.

12. Also contained on the board are logic circuits that receive inputs from the frequency-setting thumbwheel switches on the front panel, and produce control outputs for application to the appropriate oscillator selector on the h.f. loop board.

#### 34 MHz oscillator

13. TR2, TR4 and associated components form a nominal 34 MHz L-C oscillator. L1, C1 and C3 form the basic tuned circuit; frequency pulling is provided by varactor diode D2. The control voltage for D2, applied via choke L2, is derived from the phase-detector and voltage-control circuit described in para. 19 and 20.

14. The output of the oscillator is buffered by NAND gates G1-G3 in ML1, for which the supply voltage is provided by series regulator TR1 and Zener diode D1. The squarewave output from gate G3 is fed to the low-pass filter including L4 and L5, and the resultant 34 MHz sinewave output is taken off the board at pin 1. The output of gate G2 is applied as the clock input to the divide-by-34 stage.

#### Divide-by-34 stage

15. The divide-by-34 stage consists of the dual J-K flip-flop ML3, the binary decade counter ML5 (connected as a divide-by-10 stage), and NAND gates G4 and G6 in ML6.

16. The 34 MHz output from the buffer G2 in ML1 is applied in parallel to the clock inputs of both halves of ML3; the J1 output is held at logic '1' (+5V). The division factor of 34 is obtained by dividing the first 18 pulses by 3 and the next 16 pulses by 4.

$$\begin{aligned} \text{i.e.} \quad & 18 \text{ pulses} \div 3 = 6 \\ & 16 \text{ pulses} \div 4 = 4 \end{aligned}$$

Therefore, for 34 pulses in, 10 pulses appear at the output of ML3. These 10 pulses are divided by ML5 to provide the 1 MHz output at pin 2 of ML5.



17. Figure 2 illustrates the action of the circuit and shows the logic signals produced at relevant points.

#### Amplifier and squarer

18. The 5 MHz sinewave output from the frequency standard is fed onto the board at pin 8 and applied to the amplifier and squarer comprising TR3, TR5 and associated components. The output of this circuit is divided by 5 in ML2; the resulting 1 MHz squarewave (0V to +4V p-p) is fed to the inputs of NAND gates G5, G7 and G8 (connected as buffers) in ML4. The output of G5 is taken from the board at pin 10 via a 220 ohm resistor to the transfer loop board PS.338, and the output of G7 is taken via pin 12 to the l.f. loop board PM.349. The output of G8 is applied as the reference frequency to one input of the phase-comparator.

#### Phase-comparator

19. The phase-comparator consists of the dual D-type flip-flop ML7 and the NAND gate G9 in ML6. The nominal 1 MHz squarewave derived from the 34 MHz oscillator via the divide-by-34 stage is applied as the 'clock' input to one half of ML7; the reference 1 MHz squarewave derived from the 5 MHz frequency standard is applied as the clock input to the other half. Both D inputs are held permanently at logic 1. The Q outputs of both halves are applied to the inputs of NAND gate G9, and the output of G9 is connected back in parallel to the 'clear' inputs of both halves of ML7. The Q outputs are applied as control inputs to the voltage-control stage.

#### Voltage-control stage

20. The voltage-control stage consists of transistors TR6 and TR8 which together control TR7. The d.c. control voltage is developed across C23 and applied to the varactor diode D2 in the 34 MHz oscillator. R27 and C21 provide decoupling for the control voltage.

#### V.C.O. switching stages

21. The v.c.o. switching stages consist of NAND gates ML8, NOR gates ML9, ML10, and the inverting output buffers TR9-TR11. Inputs from the frequency selection switches on the front panel, routed via inverting circuits on the noise immunity board, are applied to ML8 and ML9 at pins 13-17. The logic circuits produce control outputs at pins 19-21 which are fed to the h.f. loop board to select one of the three h.f. loop oscillators.

22. A logic '0' is required as output from one (and only one) of pins 19-21 in order to select a particular oscillator; the remaining two pins must be at logic '1'.

TABLE 2

## Oscillator selection logic

Input pins					Output pins			Oscillator selected
16	15	17	13	14	21	19	20	
'1' on any pin			1	1	0	1	1	0- 7 MHz
0	0	0	1	1				8-17 MHz
or '1' on any pin			*	0	1	0	1	
Any other condition					1	1	0	18-29 MHz

'\*' = immaterial

### L.F. LOOP BOARD PM.349 (fig. 12)

23. This printed circuit board contains the circuits necessary to generate the 3.6 - 4.6 MHz frequency (f2); these consist of the following:

- (1) 18-23 MHz voltage-controlled oscillator.
- (2) Programmed divider (N1).
- (3) Divide-by-2000 stage to produce the 500 Hz reference frequency from the 1 MHz standard frequency input.
- (4) 500 Hz phase-comparator and output circuit for the control voltage.
- (5) Divide-by-5 stage to produce the 3.6 - 4.6 MHz output from (1).

24. The board also contains logic circuits to produce an 'out-of-lock' signal when the oscillator is not phase-locked to the reference frequency, and a filter and amplifier to produce a 1.4 MHz output from the 1 MHz standard frequency input. A block diagram is shown in fig. 4.

### 18-23 MHz oscillator

25. Transistor TR2 and associated components form a variable-frequency L-C oscillator, tunable over the range 18-23 MHz by the bias voltage applied to varactor diode D1 in the oscillatory circuit. The output is buffered by NAND gate G2 in ML1, and applied as the clock input to the divide-by-5 stage ML2. A squarewave output from ML2 is buffered by G1 in ML1 before being applied to the step-down transformer T1 via the low-pass filter L1, C1, C2. The 3.6 - 4.6 MHz sinewave output f2 is taken from the secondary of T1 at pins 3 and 4 of the board. Transistor TR1 forms a series stabilizer for the oscillator circuit.

### Programmed divider N1

26. This consists of the presettable decade counters ML5, ML8, ML11, ML13 and ML16, AND gates G5 and G4 of ML6, NAND gates ML15 and the dual J-K flip-flop ML9.

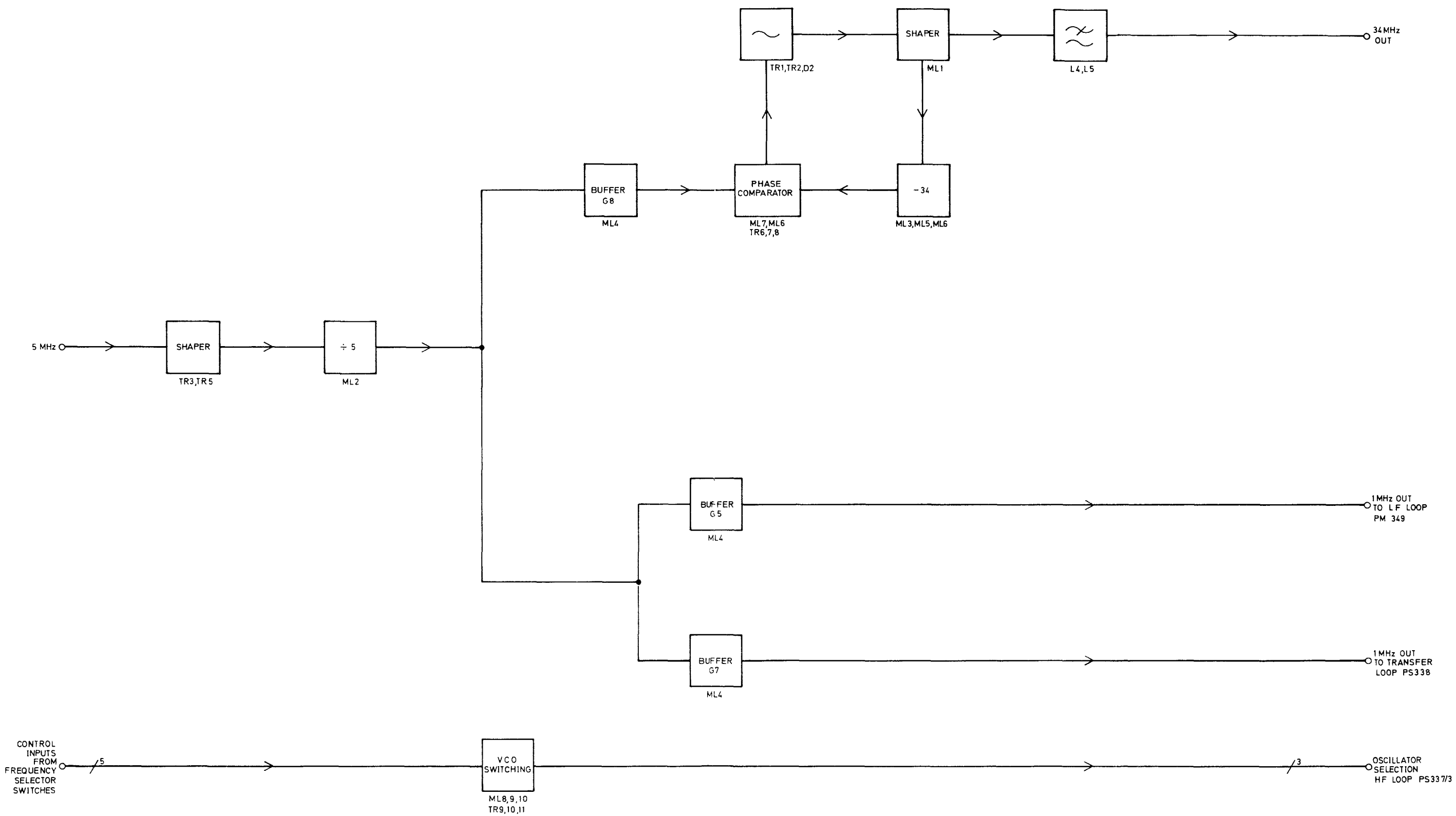


Fig. 1

34 MHz generator board PM.344 : block diagram

Fig. 1

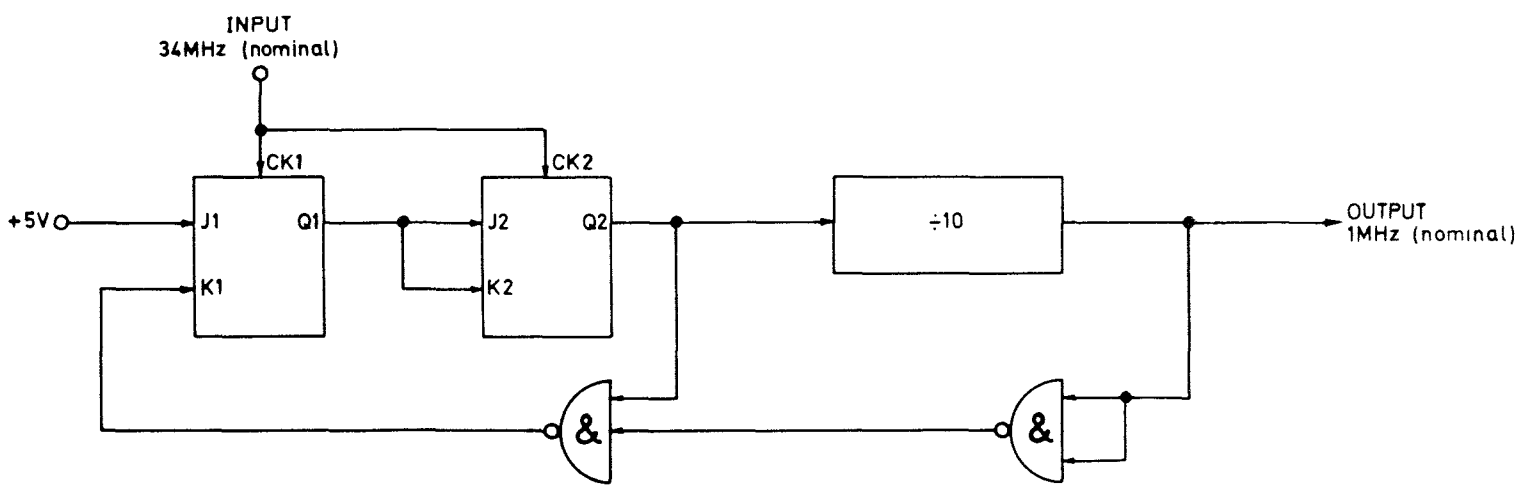
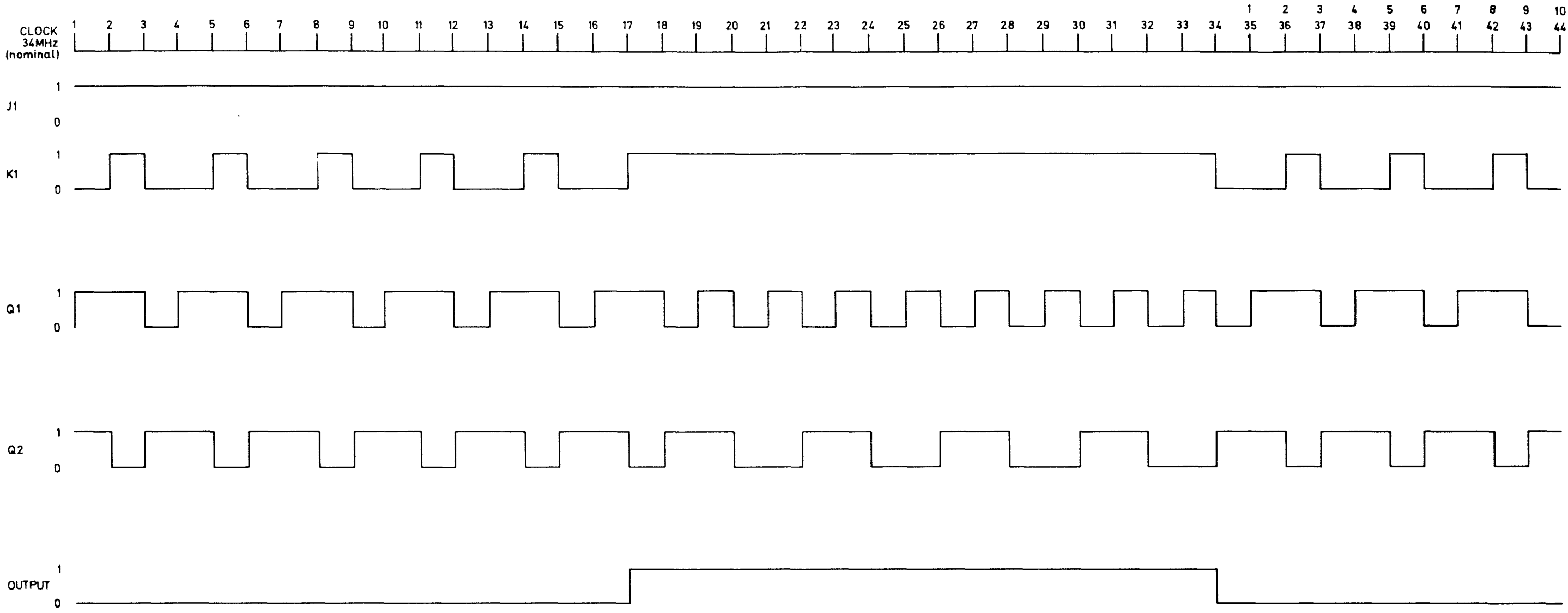


Fig. 2

Divide-by-34 stage : waveforms

Fig. 2

27. The input to the divider at ML5 pin 8 is the output of the 18-23 MHz oscillator; the output of the divider at ML16 pin 2 is applied as the sample input to one half of the phase-comparator ML12. ML9 is also clocked by the output from the v.c.o.
28. Gates ML6 and ML15 form a decoder, giving an output of logic '1' from ML8 pin 6 when a BCD count of 45997 is detected at the outputs of the counters.
29. The divider is programmable for any division ratio in the range 36001-46000 by the setting of the 'kHz' switches on the front panel; these apply the set figures (in BCD form) to the input lines of the first four counters.
30. The divider operates as follows. Assume an initial state where all counters are at 0, and where 4236 is set in BCD format on the input lines. When the clock input is applied to ML5 pin 8, the counters count up until the decoder gates detect a count of 45997.
31. At this point the J1 input of ML9a goes to logic '1', and three clock pulses later (at a count of 46000) the Q1 output of ML9a goes to '0'.
32. This is applied as the strobe input to the counters, and 'strokes-in' the data on the input lines. The counters therefore reset to 4236, count up to 46000, and continue cycling in this manner, dividing by a figure of 46000-4236.
33. In general terms, the divider is programmable to divide by 46000-XXXX, where XXXX are the digits set on the 'kHz' switches.

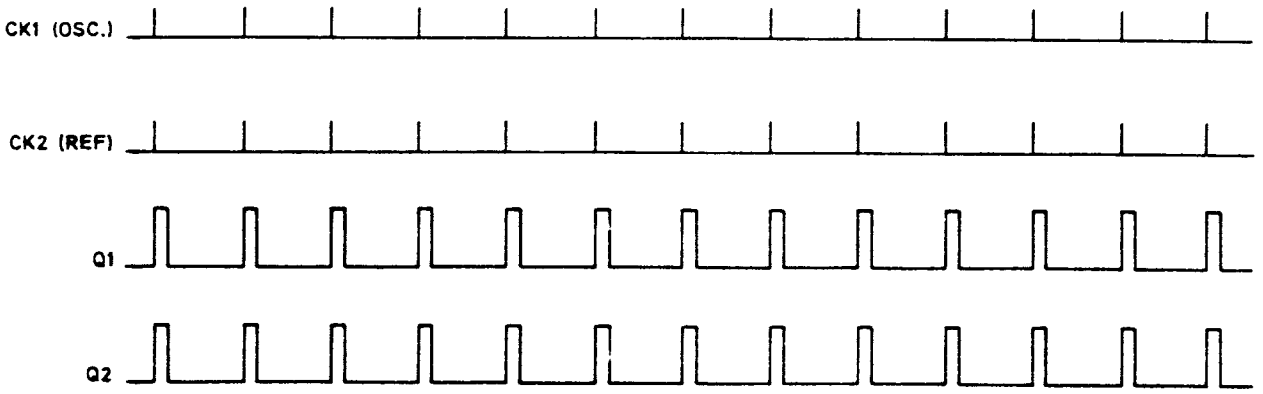
#### Divide-by-2000 stage

34. This stage consists of the three binary decade counters ML3, ML4 and ML7 connected in cascade, followed by a single divide-by-two stage ML10. The input to the stage at pin 25 is a 1 MHz squarewave (derived from the 5 MHz frequency source) from the 34 MHz generator board pin 12. The 500 Hz output from ML10 (the reference frequency) is applied to one input of the phase-comparator (ML12 and G6 of ML14).

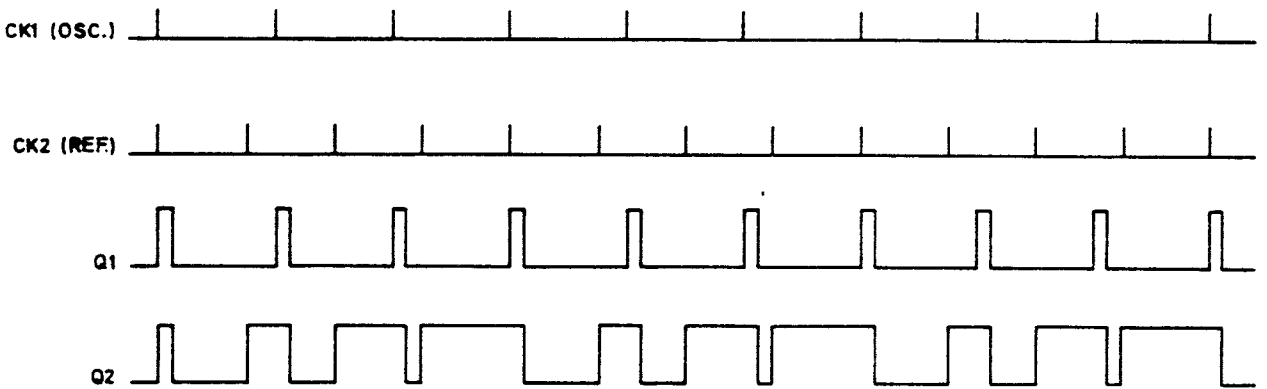
#### Phase-comparator

35. This consists of the dual D-type flip-flop ML12, NAND gate G6 in ML14, and the voltage-control circuit TR5-TR11 and associated components. The squarewave derived from the 18-23 MHz oscillator via the programmed divider is applied as the clock input to one half of ML12, and the reference 500 Hz squarewave from the 5 MHz frequency standard is applied as the clock input to the other half. Both D inputs are connected to +5V and held permanently at logic 1. The Q outputs of both halves are applied to the inputs of 'nand' gate G6 in ML14, and the output of G6 is connected to the 'clear' inputs of both halves of ML12 via the delay network R26, C25. The Q outputs are applied to the bases of TR5 and TR7 in the voltage-control circuit, and the  $\bar{Q}$  outputs are fed to the out-of-lock indicator.

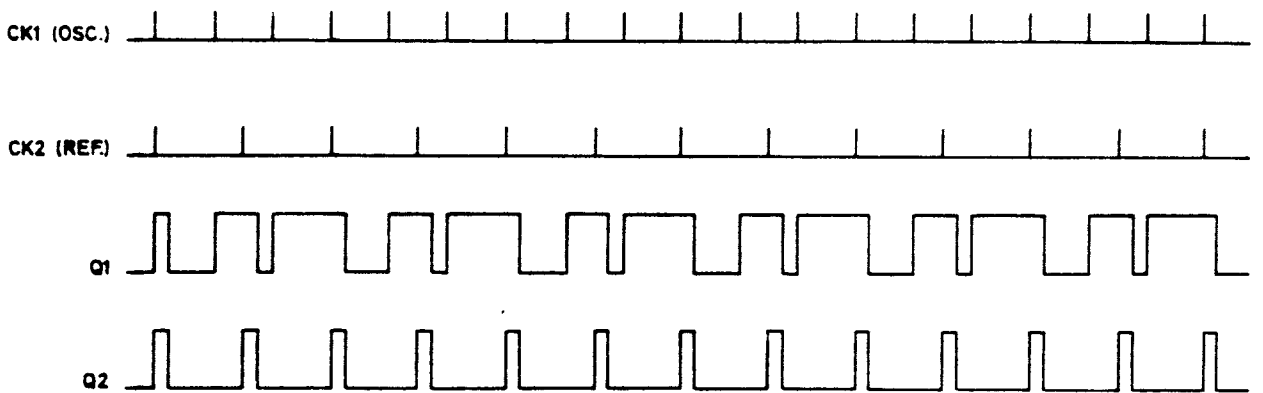
36. The operation of the phase-comparator is as follows. If the inputs are in phase, i.e. if the oscillator frequency is  $500 \times N$  Hz, the Q1 and Q2 outputs go to '1' simultaneously; gate G1 therefore gives a '0' output which, applied to the 'clear' inputs of ML12, inverts both Q outputs to '0'. The Q1 and Q2 outputs thus both consist of a train of narrow positive-going pulses at a p.r.f. of 500 Hz.



OSCILLATOR AND REFERENCE IN PHASE



OSCILLATOR LAGGING (FREQUENCY LOW)



OSCILLATOR LEADING (FREQUENCY HIGH)

Fig.3 Phase comparator - idealized waveforms

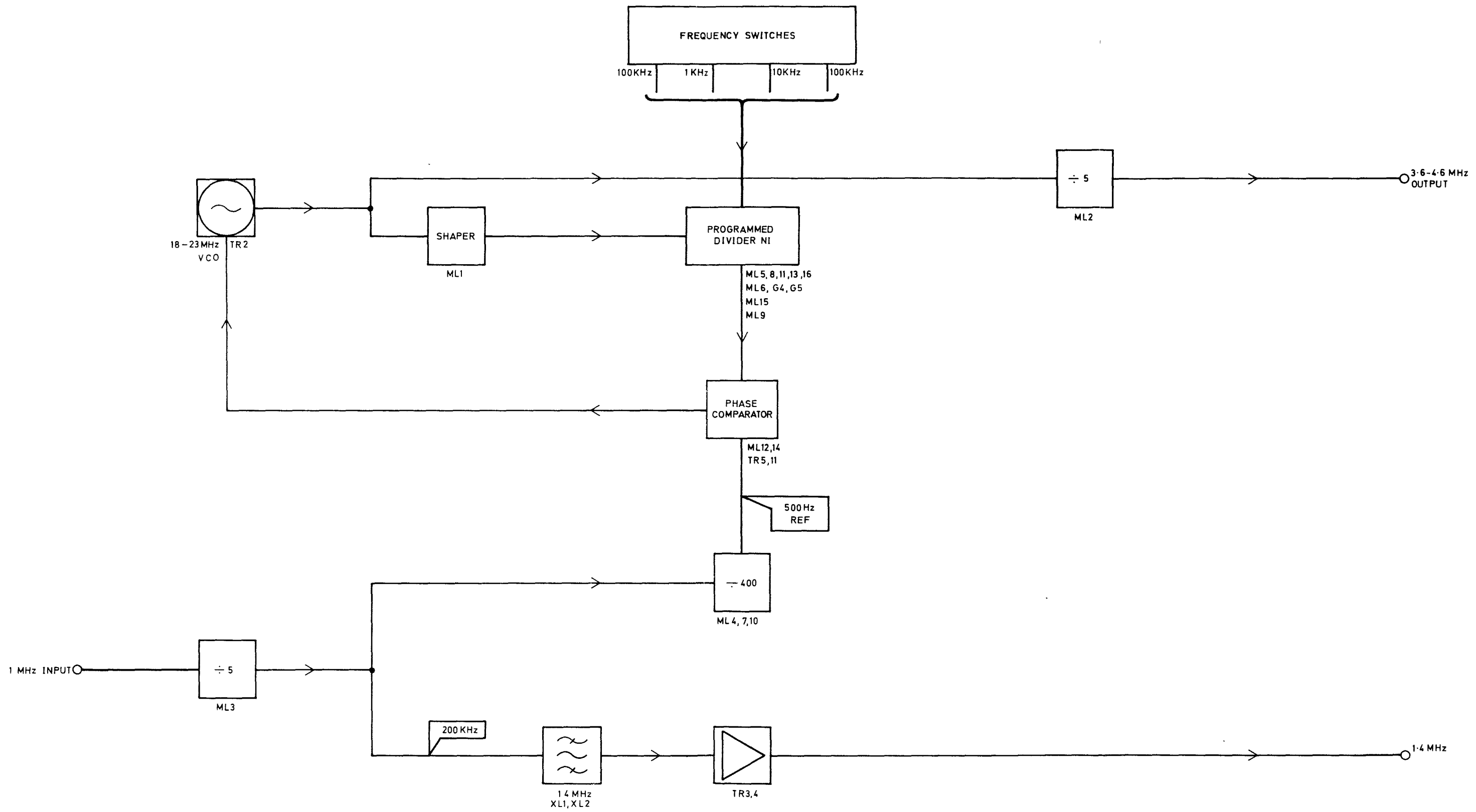


Fig. 4

L.F. loop PM.349 : block diagram

Fig. 4

37. If the oscillator is lagging on the reference, the Q1 output is a train of narrow pulses and the Q2 output is a train of wide pulses. If the oscillator is leading, the Q1 output is a train of wide pulses and the Q2 output is a train of narrow pulses.

38. These three conditions are illustrated by the idealized waveforms in fig.3.

39. The voltage-control circuit consists of transistors TR5 to TR12 and associated components, the control voltage being developed across capacitor C39.

40. If a wide pulse appears at the Q output of ML12A, this is converted by transistor TR7 into a current pulse, which will discharge capacitor C39 via transistor TR8, connected as a diode; similarly a wide pulse at the Q output of ML12B charges C39 via transistors TR5, TR6 and TR9. The voltage on C39 is fed via the source follower TR11 to the varactor diode D1 to complete the phase-lock loop; R34 and C31 ensure the loop is stable. The effect of leakage in TR6, TR7 and the varactor D1 is eliminated by TR8, TR9 and TR11. Transistor TR10 is an a.c. stabilizer to prevent unwanted noise on the +20V d.c. line reaching the varactor line.

#### Lock indicator

41. The  $\bar{Q}$  outputs of the 500 Hz phase-comparator are applied to NAND gates G9 and G10 in ML14; gate G11 on ML17 is connected as a buffer/inverter. The inputs to G10 are delayed by approximately 0.3  $\mu$ s by R38 and C31, R51 and C44 to ensure correct latching action.

42. In the in-lock condition, a train of negative-going pulses of approximately 50 ns duration will be applied to G9 and G10 in ML14. These inputs will appear as logic '0' and logic '1' inputs to G9 (logic '0' during negative pulse) but, because of the delay caused by R35 and C30, R38 and C31, the negative-going pulses will not appear at the input to G10; therefore in the in-lock condition, pins 4 and 5 of G10 will always be at logic '1'. Pin 6 of G10 will be at logic '0' which will be inverted by gate G11 in ML17 to produce a logic '1' in-lock indication at pin 24 of the board.

43. In the out-of-lock condition, one the  $\bar{Q}$  outputs from the phase-comparator will consist of a train of wide negative-going pulses whilst the other output will consist of a train of narrow negative-going pulses (para. 37). Due to the delay caused by R35 and C30 or R38 and C31, the wide negative pulse will still be present at G10 after the input to G9 has returned to logic '1'; this will have the effect of resetting the latch in G9 and G10 producing a logic '1' output at pin 6 of G10. Gate G11 in ML17 will invert this logic '1' output from G10 to produce a logic '0' out-of-lock indication at pin 24 of the board.

44. The output from the out-of-lock indicator is fed via the r.f. filter L7 and C44 to pin 24 of the board.

#### Crystal filter and amplifier

45. A divide-by-5 output of 200 kHz is taken from pin 9 to ML3 (the first component of the divide-by-2000 stage). This is passed via the 1.4 MHz crystal filter (XL1 and XL2) to the tuned amplifier TR3 and TR4. The 1.4 MHz sinewave output is at pins 1 and 2 of the board.



TRANSFER LOOP BOARD PS.338 AND H.F. LOOP BOARD PS.337/3 (fig. 14 and 16)

46. It is convenient to describe these two boards together because the v.c.o. for the transfer loop is contained on the h.f. loop board. A block diagram is shown in fig. 5.

47. The principal function of these two boards is to generate  $f_4$  (35.4 - 65.4 MHz) and  $f_3$  (885-947.8 kHz). The frequency  $f_3$  is determined by the setting of the thumbwheel frequency selector switch.  $f_4$  is phase-locked to  $f_3$  via the programmed divider such that  $f_4 = N_2 \times f_3$ .

Generation of  $f_3$

48. The circuits generating  $f_3$  are contained on two boards as follows:-

(1) Voltage-controlled oscillator (D19, TR17, TR20 on the h.f. loop board, fig. 16).

(2) Mixer and low-pass filter on the transfer loop board (fig. 14) to produce the frequency 1 MHz- $f_3$ .

(3) Programmed divider ( $N_2$ ) on the transfer loop board, producing an output  $\frac{f_2}{N_2}$  for use as the reference frequency.

(4) Phase-comparator on the transfer loop board, to lock the output of (1) at a frequency

$$1 \text{ MHz} - f_3 = \frac{f_2}{N_2}$$

Transfer loop : oscillator (fig. 16)

49. Transistor TR17, TR20 and associated components form a variable-frequency L-C oscillator, tunable by the bias voltage applied to varactor diode D19 in the oscillatory circuit. The output at frequency  $f_3$  is applied as the clock input to the divide-by-two stage ML12. A sample of  $f_3$  is fed off the board at pin 13 via the buffer amplifier TR21 and applied to the mixer on the transfer loop board.

Transfer loop : mixer and low-pass filter (fig. 14)

50. The mixer comprises the integrated-circuit ML3, together with the input buffer amplifiers TR1, TR2, TR3.

51. The 1 MHz stable signal is fed onto the board at pin 3 and applied to one input of ML3 via the buffer amplifier TR1, TR2. A sample of  $f_3$ , generated by the oscillator, is applied to the other input of ML3 via pin 19 and buffer TR3, and the combined signal is fed via the low-pass filter L11, L12 to the buffer amplifier TR6. The output frequency at the collector of TR6 is 1 MHz -  $f_3$ , which is squared and inverted in NAND gate ML7A for application to the phase-comparator.

Transfer loop : programmed divider  $N_2$  (fig. 14)

52. This consists of the presettable decade counters ML1, ML2, NAND gates ML4, ML5 and the D-type flip-flop ML6.

53. The input to the divider at pin 17 is the sine wave  $f_2$  generated by the v.c.o.; the output of the divider at ML6 pin 5 is the frequency  $f_2/N_2$ , used as the reference frequency in the generation of  $f_3$ .

54. The input signal is shaped by TR4, TR5, squared and inverted by NAND gate ML4A, and applied as the clock input to the 'units' counter ML1.

55. Gates ML4B and ML5 form a decoder, giving an output of logic '0' when a count of 37 is detected at the outputs of the decade counters. The output at ML5 pin 8 is applied to the data input of ML6, which is clocked by the input frequency  $f_2$ . The Q output of ML6 is applied:

(1) To one clock-input of the phase-comparator ML8 as the reference frequency.

(2) To the decade counters ML1, ML2 as the strobing signal (logic '0' 'strokes' in the data on the input lines).

56. The divider is programmable for any division ratio in the range 40-69 by the setting of the 'MHz' frequency selection switches on the front panel; these apply the nine's-complement of the set figure (in BCD form) via the noise immunity board to the data input lines of the divider (pins 8-15).

57. Table 3 shows the operation of the divider for various representative values of 'MHz' switch setting.

TABLE 3  
Operation of divider (transfer loop)

'MHz' setting	BCD input	Clock pulses				
		Count up (100-BCD i/p)	Commence strobe pulse ML6	Fixed count detect	End strobe pulse ML6	Total (= division ratio)
00	99	1	1	37	1	40
07	92	8	1	37	1	47
14	85	15	1	37	1	54
21	78	22	1	37	1	61
29	70	30	1	37	1	69

Transfer loop : phase-comparator (fig. 14)

58. This consists of the dual D-type flip-flop ML8 and the NAND gate ML7B. The squarewave 1 MHz- $f_3$  is applied as the clock input to one half of ML8, and the reference frequency  $f_2/N_2$  is applied as the clock input to the other half. Both D inputs are connected to +5V and held permanently at logic '1'. The Q outputs of both halves are applied to the inputs of NAND gate ML7B, and the output of ML7B is connected back in parallel to the 'clear' inputs of both halves of ML8. The Q outputs are applied as control inputs to the voltage-control circuit.

#### Transfer loop : voltage-control stage (fig. 14)

59. The voltage-control stage comprises transistors TR7-TR10 and associated components; the d.c. control voltage at TR10 collector is fed off the board at pin 4, and applied to varactor diode D2 in the oscillator via pin 18 on the h.f. loop board (fig. 16).

#### Transfer loop : lock indicator and fast lock stage (fig. 14)

60. This stage comprises two monostables, ML9, ML10, a dual D-type flip-flop ML11, and NAND gates ML4C, ML4D. Its purpose is to augment the conduction of TR7 or TR10 in the out-of-lock condition and so obtain a faster return to the locked condition; it also provides a lock-indication output signal. The action of the circuit is as follows.

61. The Q output from the phase-comparator flip-flop (ML8A) is applied to the B input (Schmitt trigger) of the monostable, ML9, and also to the D and 'clear' inputs of a D type flip-flop, ML11A. Similarly, the Q output from ML8B is applied to the B input of the monostable, ML10, and also to the D and 'clear' inputs of a second D-type flip-flop, ML11B. The two monostables, triggered when positive-going signals are applied to the respective B inputs, each produce a negative-going output pulse ( $\bar{Q}$ ), of approximately 1.5  $\mu$ s duration.

62. At the end of each output pulse, the D inputs of ML11A and ML11B are sampled by their respective clock inputs to produce the appropriate in-lock or out-of-lock  $\bar{Q}$  outputs from the flip-flops.

63. In the in-lock condition, the Q outputs from the two flip-flops, ML11A, ML11B are both at logic '1'; these signals do not, however, affect the conduction of the voltage-control transistors, TR7, TR10, due to the presence of the two diodes, D2, D3. The logic '0' output from ML4C is inverted by ML4D to produce a logic '1' in-lock signal at board pin 5.

64. If the output frequency from the mixer is low, the negative excursion of the  $\bar{Q}$  output from ML11B will be applied to TR10, via diode D3. The conduction of TR10 will, therefore, be increased rapidly to bring about a fast return to the in-lock condition. The  $\bar{Q}$  output from ML11B is also applied to ML4C to produce an alternating '01' out-of-lock signal at board pin 6.

65. Should the out-of-lock condition be due to a high mixer output frequency, the  $\bar{Q}$  output from ML11 will cause a rapid return to the in-lock condition by increasing the conduction of TR7; the Q output from ML11A is also applied to ML4C to produce an alternating '01' out-of-lock signal at board pin 6, as before.

#### H.F. loop : generation of $f^4$ (fig. 16)

66. The circuits generating  $f^4$  are contained on the h.f. loop board and consist of the following:

- (1) Voltage-controlled oscillator TR1-TR9, with a.g.c. stage TR10, TR13 and output buffer TR14.
- (2) Programmed divider N2 consisting of ML3, ML5 and associated components.
- (3) Phase-comparator ML7, to lock the output of (1) at a frequency

$$\frac{f_1}{2N_2} = \frac{f_3}{2}$$

H.F. loop : oscillator (fig. 16)

67. The frequency range of the oscillator is 35.4 to 65.4 MHz; this is provided by three switched oscillators each having the following frequency range:

- (1) Oscillator No.1 : 35.4 to 42.4 MHz
- (2) Oscillator No.2 : 42.4 to 52.4 MHz
- (3) Oscillator No.3 : 52.4 to 65.4 MHz

The oscillators are similar in operation, and the required frequency band is selected by the setting of the 'MHz' switches on the front panel. These switches apply a control voltage of 0V to one of the pins 26, 27 or 28 via the logic circuits on the 34 MHz generator board (fig. 10); this input turns on TR3, TR2 or TR1 supplying power to the associated oscillator.

68. Details of the three oscillators are as follows:-

	Selector	Oscillator	O/P buffer
Osc. 1	TR3	TR6, D8, D9, L6	TR9
Osc. 2	TR2	TR5, D6, D7, L5	TR8
Osc. 3	TR1	TR4, D4, D5, L4	TR7

69. The output of the selected oscillator is amplified in TR10 and applied to:

- (1) The a.g.c. stage TR13, which controls the oscillator source potential (R38 sets the a.g.c. level).
- (2) The squarer stage TR11, TR12.
- (3) The output buffer amplifier TR14 (potentiometer R44 sets the stage gain); the output (f4) is available at pin 20.

H.F. loop : programmed divider (fig. 16)

70. This consists of the presettable decade counters ML3, ML5, J-K flip-flops ML2B, ML9, AND gates ML4, and NAND gate ML6. ML3 is the 'units' counter and ML5 the 'tens' counter.

71. The input to the divider at ML3 pin 8 is the squarewave  $f_1/2$ , derived from the selected oscillator via the squarer stage TR11, TR12 and the divide-by-two pre-scaler ML2A; the output of the divider at ML2B pin 9 is the frequency  $f_1/2N$ , which is fed to one input of the phase-comparator ML7.

72. Gates ML4 and ML6A form a decoder, giving an output of logic '1' when a count of 35 is detected at the outputs of the decade counters. The output at ML4 pin 6 is applied to the 'J' input of ML2B, which is clocked by the input frequency  $f_1/2$ ; both Q outputs of ML2B are fed to the dual J-K flip-flop ML9 (Q to 'J',  $\bar{Q}$  to 'K'), and the Q output of ML9B is fed back to the 'K' input of ML2B. The effect of this circuit is to stretch the duration of the '1' signal at the Q output of ML2B in order to enable the programmed divider to recognise the input data.

73. The  $\bar{Q}$  output of ML2B is applied also to the decade counters ML3, ML5 as the strobing signal (logic '0' strobes-in the data on the input lines).

74. The divider is programmable for any division ratio in the range 40-69 by the setting of the 'MHz' frequency selection switches on the front panel; these apply the nines complement of the set figure (in BCD format), via the noise immunity board, to the data input lines of the divider.

75. Table 4 shows the operation of the divider for various representative values of 'MHz' switch setting.

TABLE 4

Operation of divider (h.f. loop)

'MHz' setting	BCD input	Clock pulses				
		(100-BCD i/p)	Reset counters ML2b	Fixed count detect	ML9a and ML9b	Total ( $\pm$ division ratio)
00	99	1	2	35	2	40
07	92	8	2	35	2	47
14	85	15	2	35	2	54
21	78	22	2	35	2	61
29	70	30	2	35	2	69

#### H.F. loop: phase-comparator (fig.16)

76. This consists of the dual D-type flip-flop ML7 and the NAND gate ML6A. The squarewave  $f1/2N$  from the programmed divider is applied as the clock input to one half of ML7, and the frequency  $f3/2$  (derived from the oscillator via the divide-by-two stage ML12) is applied as the reference to the clock input of the other half. Both D inputs are connected to +5V and held permanently at logic 1. The Q outputs of both halves are applied to the inputs of NAND gate ML6A, and the output of ML6A is connected back in parallel to the 'clear' inputs of both halves of ML7. The  $\bar{Q}$  outputs are applied as control inputs to the voltage-control circuit.

#### H.F. loop: voltage-control stage (fig.16)

77. The voltage-control stage consists of transistors TR16-TR19 and associated components; the d.c. control voltage at TR19 collector is applied via R82 and r.f. chokes L21, L22, L23 to the varactor diodes D4-D9.

#### H.F. loop: out-of-lock indicator (fig.16)

78. The Q outputs of the phase-comparator are applied to the out-of-lock indicator comprising ML8, ML10, ML11, ML12B and associated components. This circuit operates in the same way as that described in paras. 41 to 43; the purpose of ML12B is to lengthen the out-of-lock pulse at board pin 12. ◀

▶ HF LOOP BOARD PS.337/4

79. Some equipments are fitted with an alternative HF Loop Board type PS.337/4, in place of type PS.337/3. The circuits on the alternative board operate, in general, as described for type PS.337/3; the differences will be evident from a comparison of Fig. 16 and 17. The physical differences between the boards are shown in Fig. 15. ▶

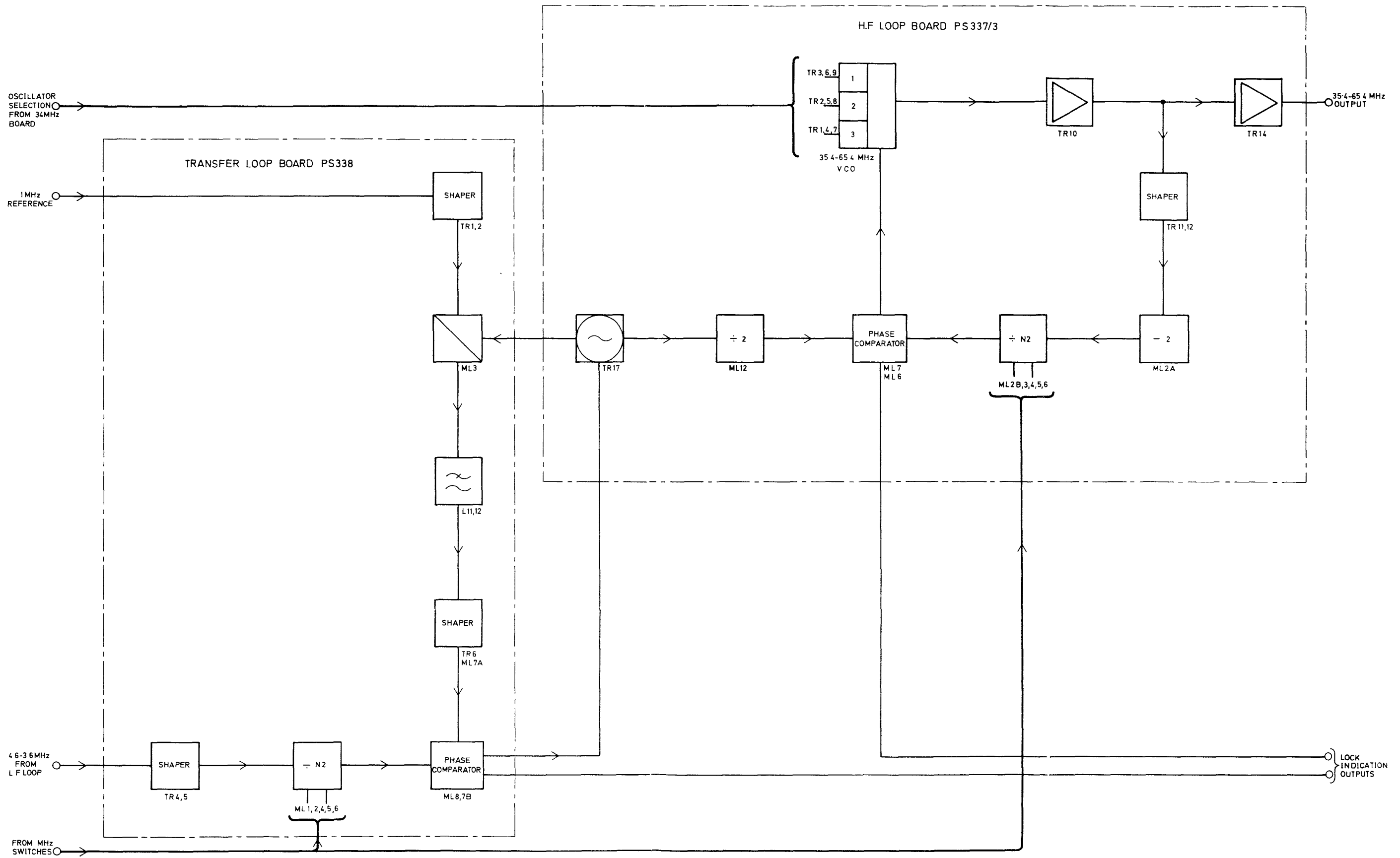


Fig. 5

Transfer loop PS.338 and h.f. loop PS.337/3 : block diagram

Fig. 5

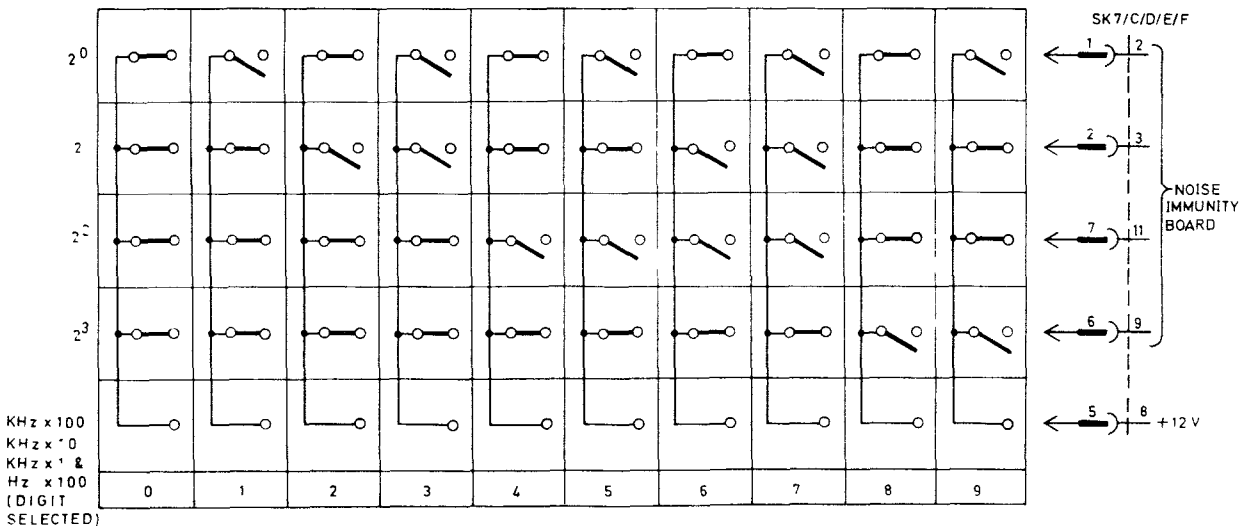
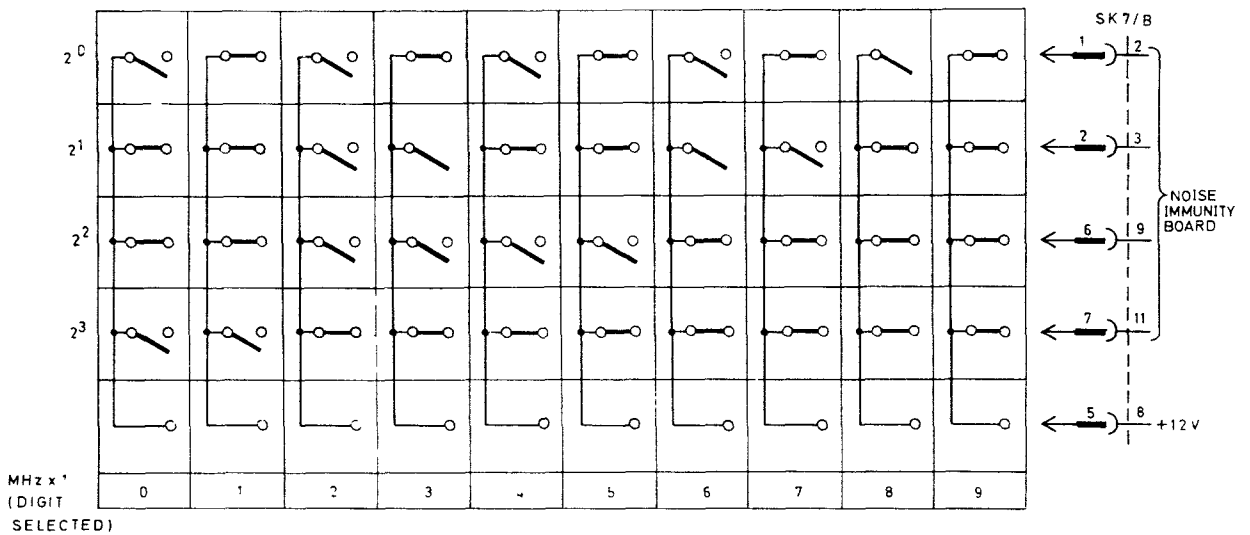
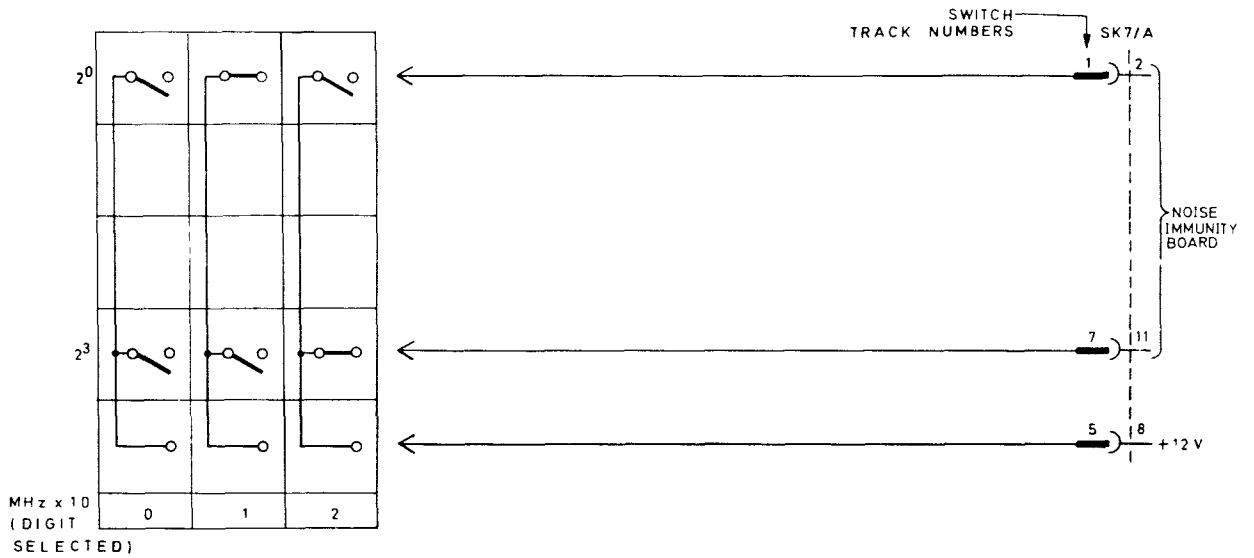


Fig. 6 Frequency selection switches : circuit



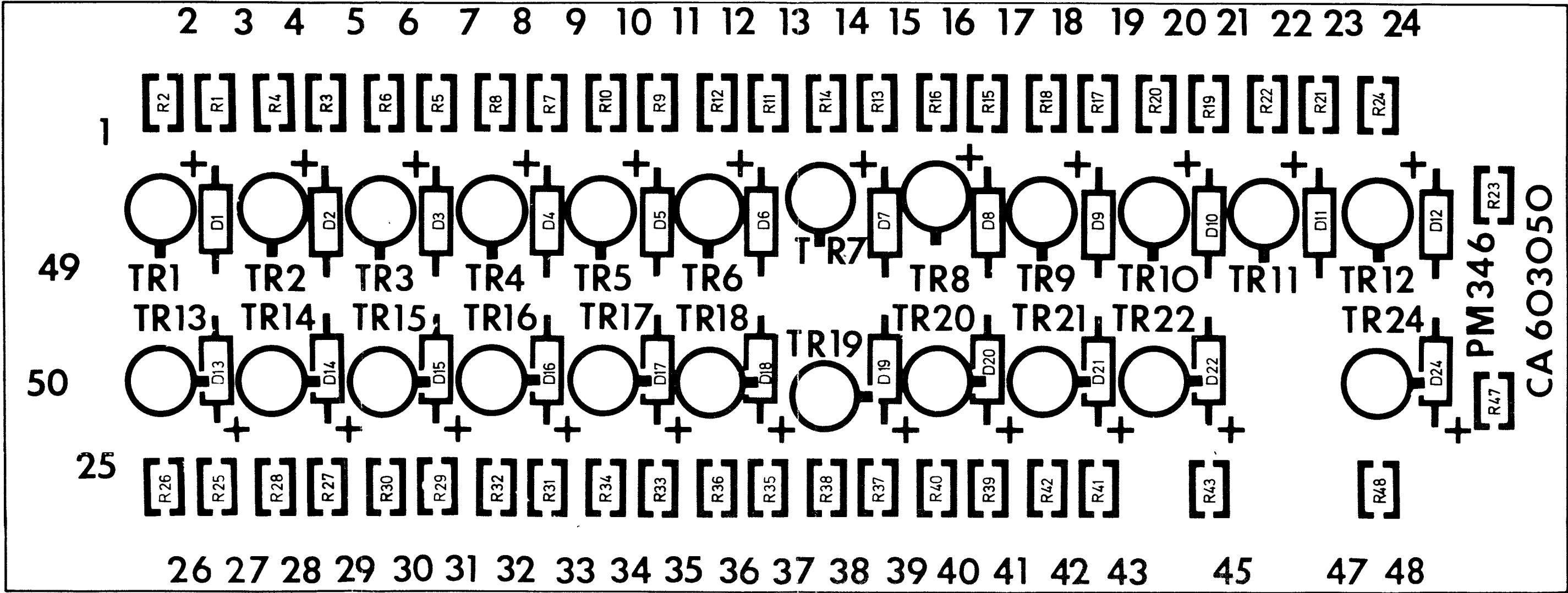


Fig. 7

Noise immunity board PM.346 : component layout

Fig. 7

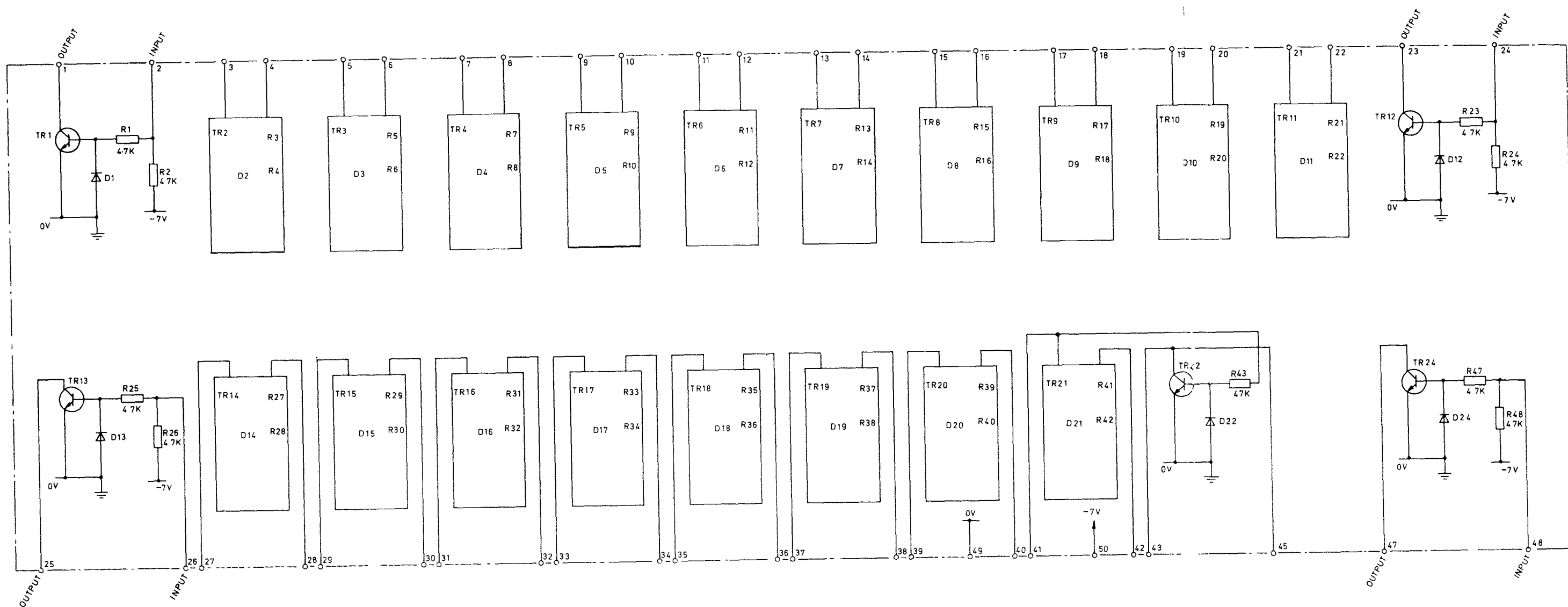


Fig. 8

Noise immunity board PM.346 : circuit

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Fig. 8

Chap.7

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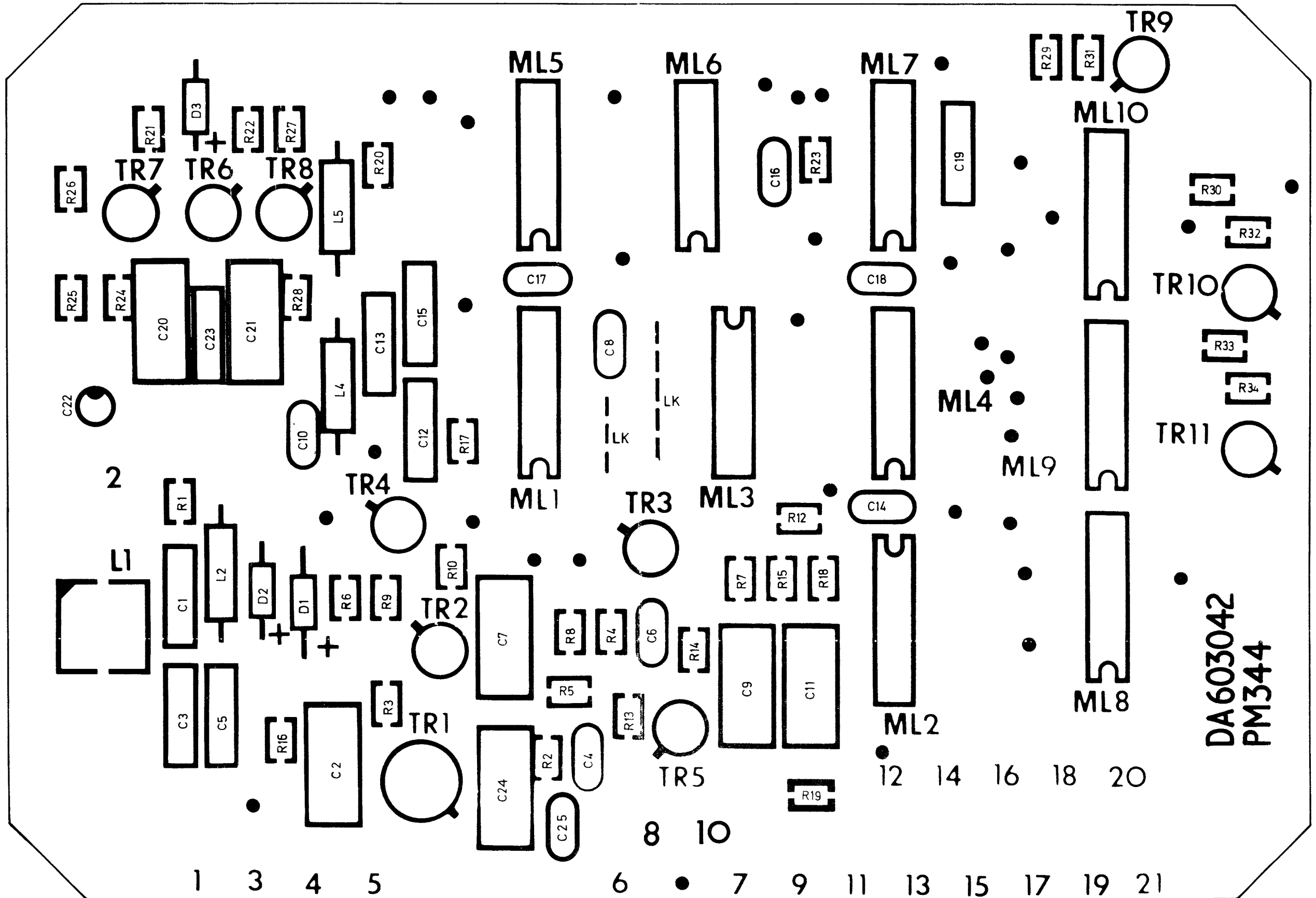


Fig. 9

34 MHz generator board PM.344 : component layout

Fig. 9

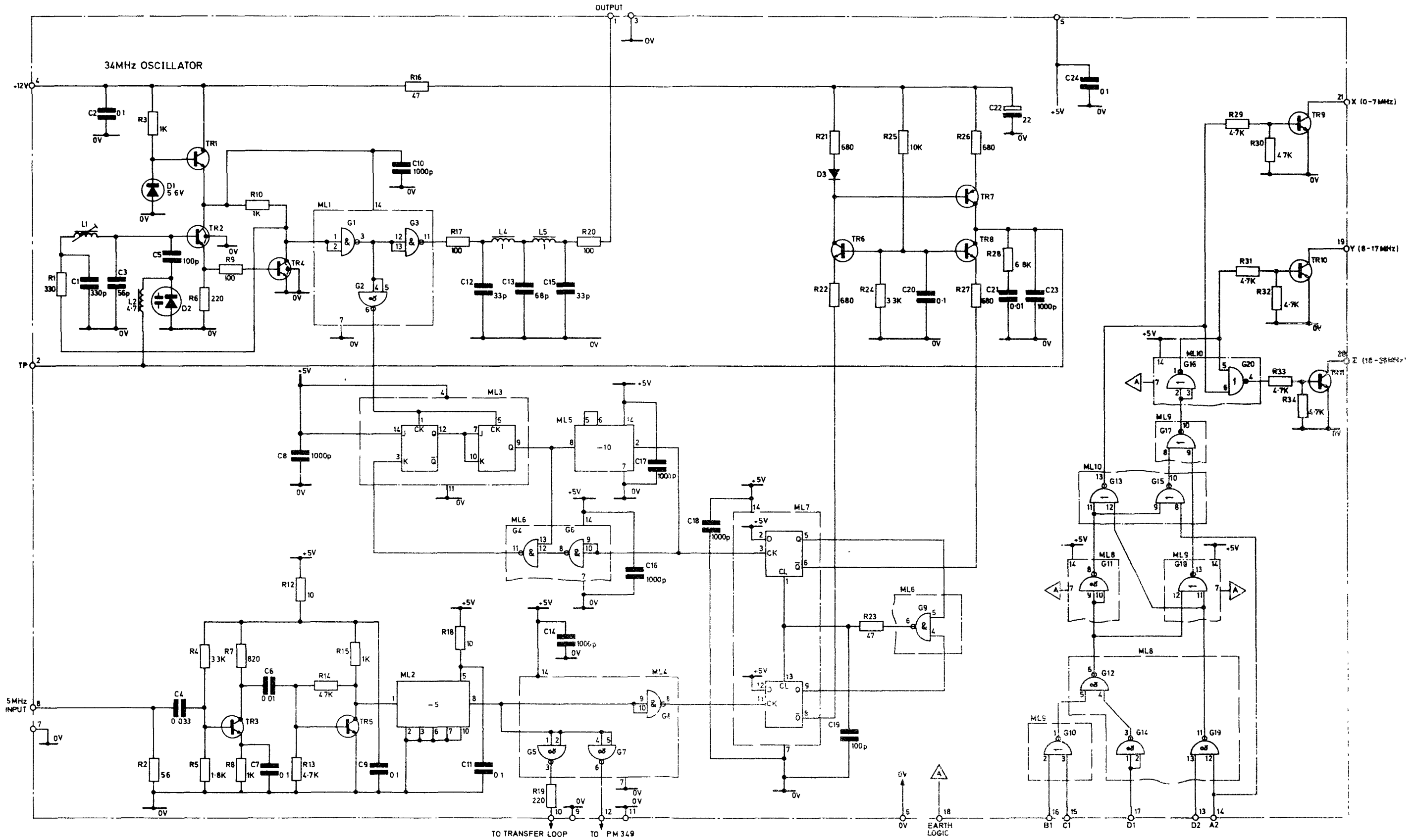


Fig. 10

34 MHz generator board PM.344 : circuit

Fig. 10



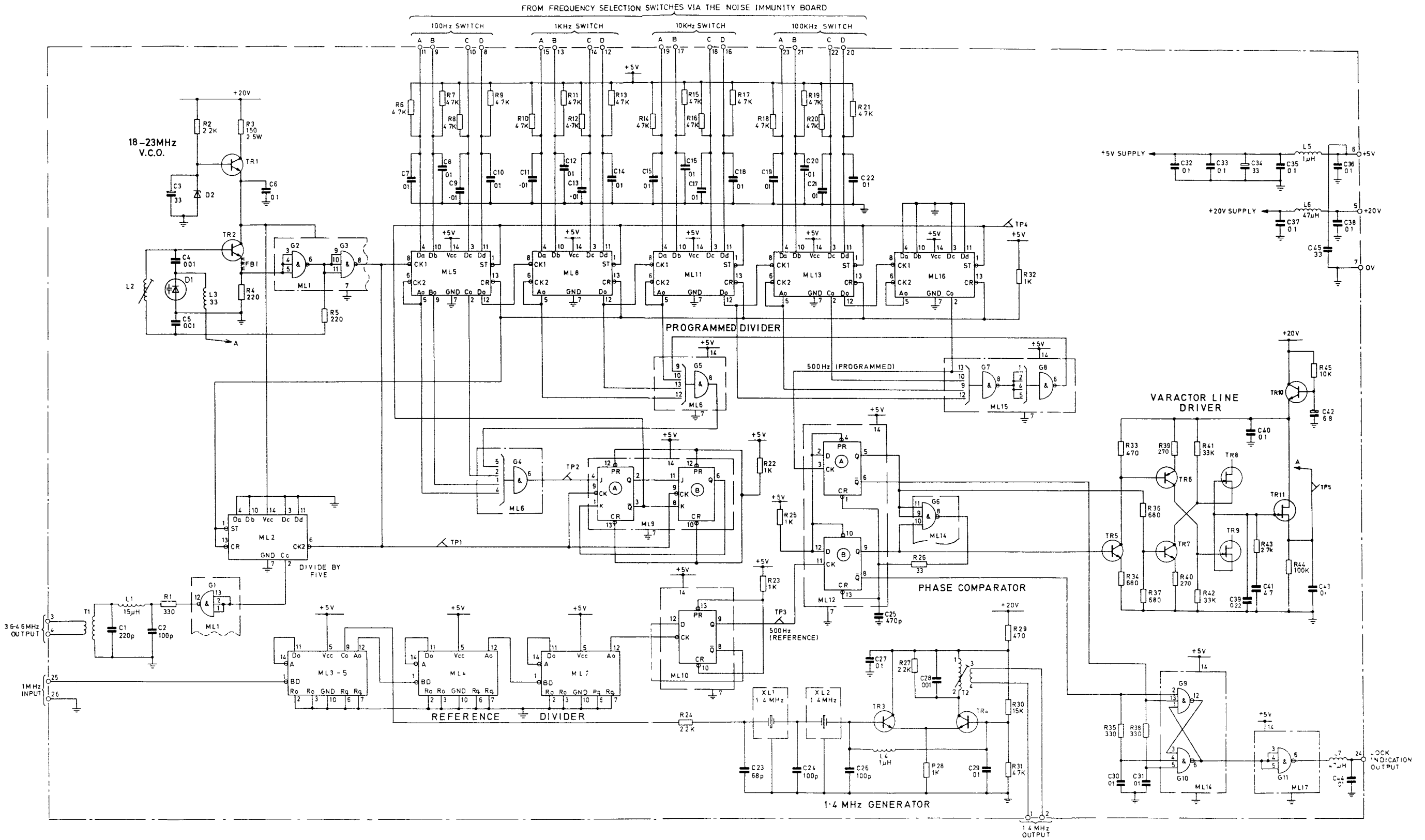
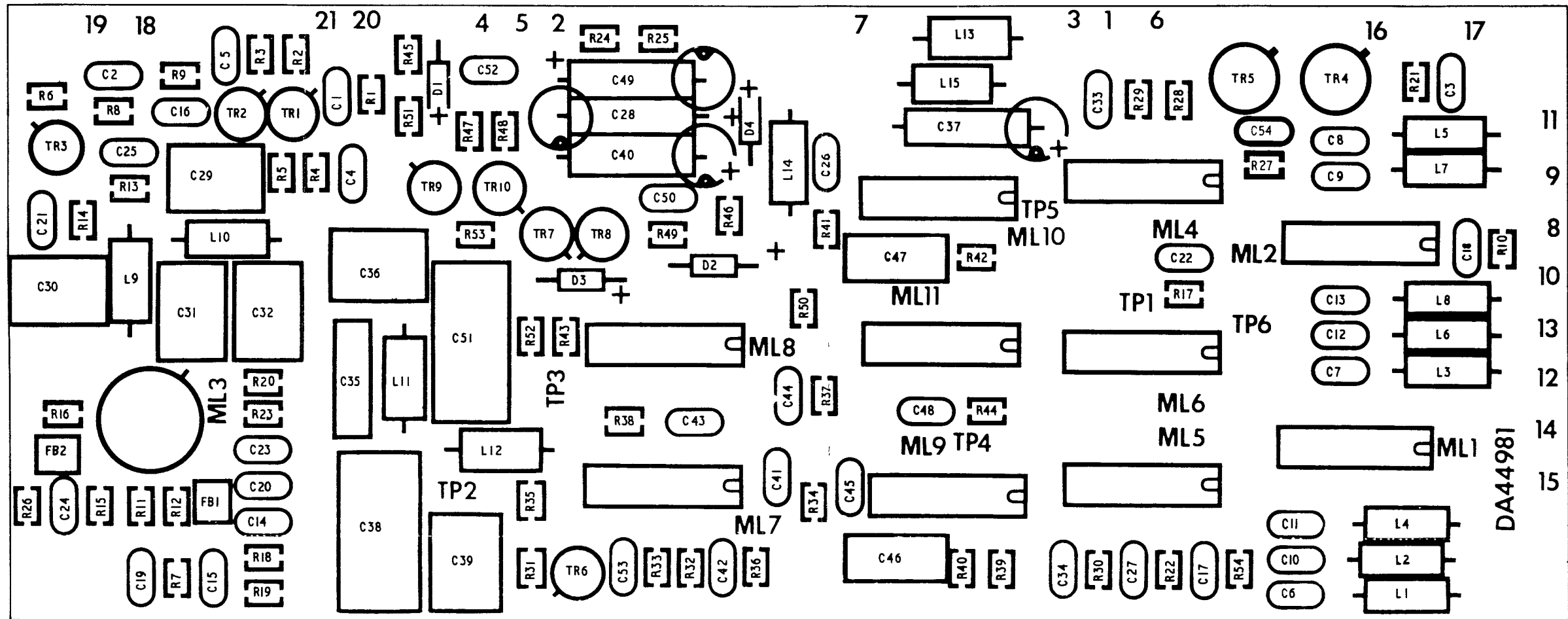


Fig.12

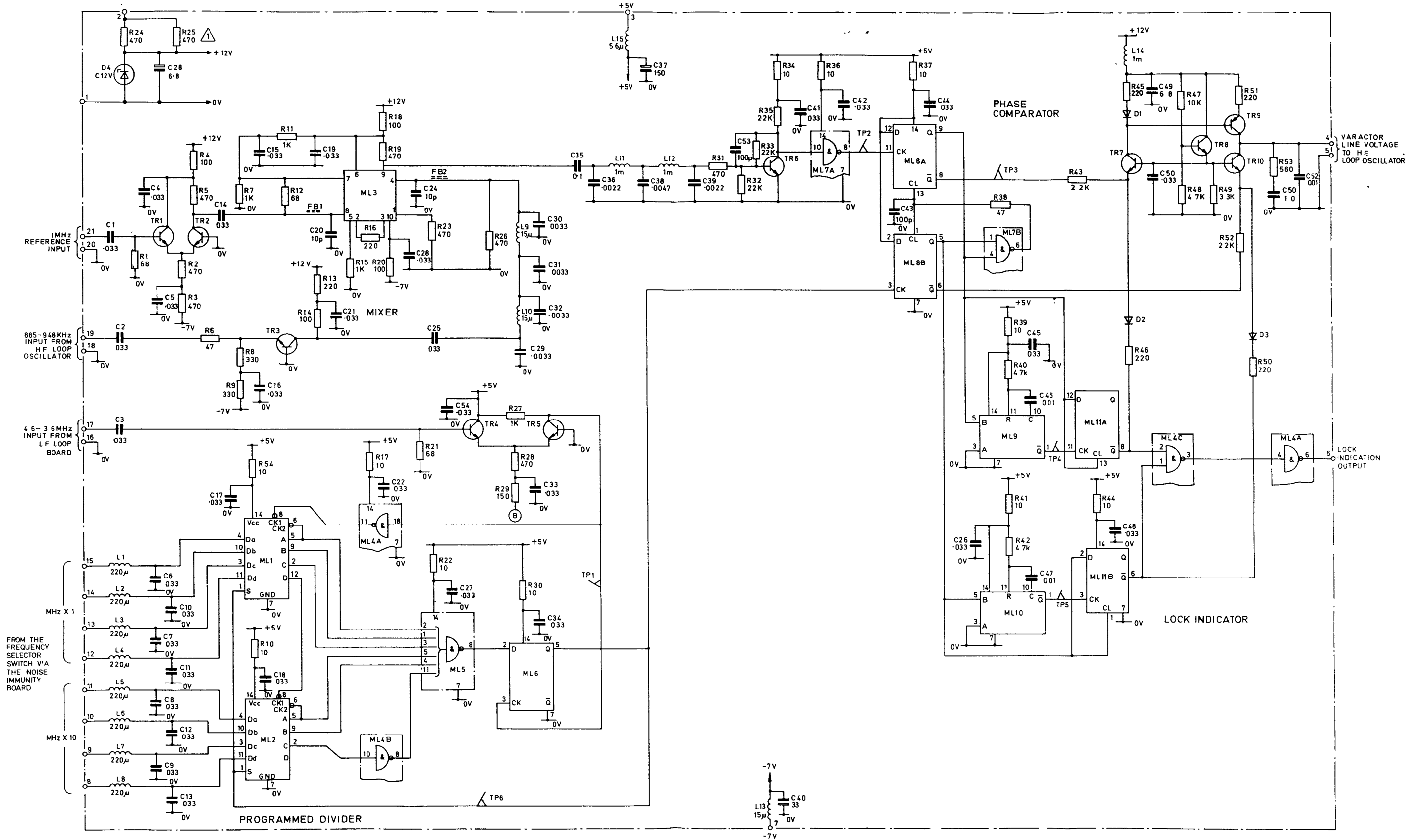
LF loop board PM.349 : circuit

Fig.12



Transfer loop board PS.338: component layout

Fig.13



REFER TO MOD No A8585

Fig. 14

Transfer loop board PS338: circuit

Fig.14



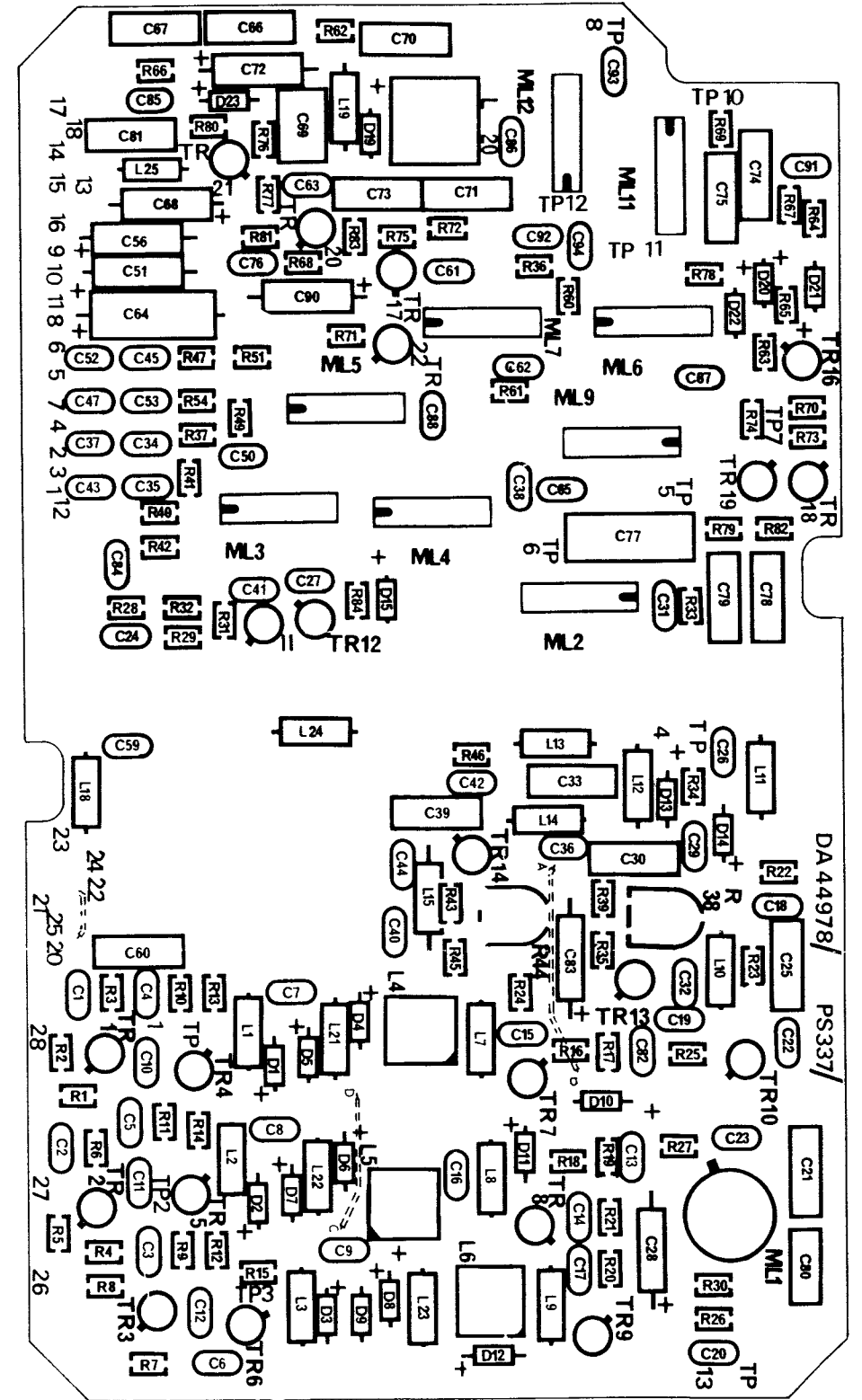
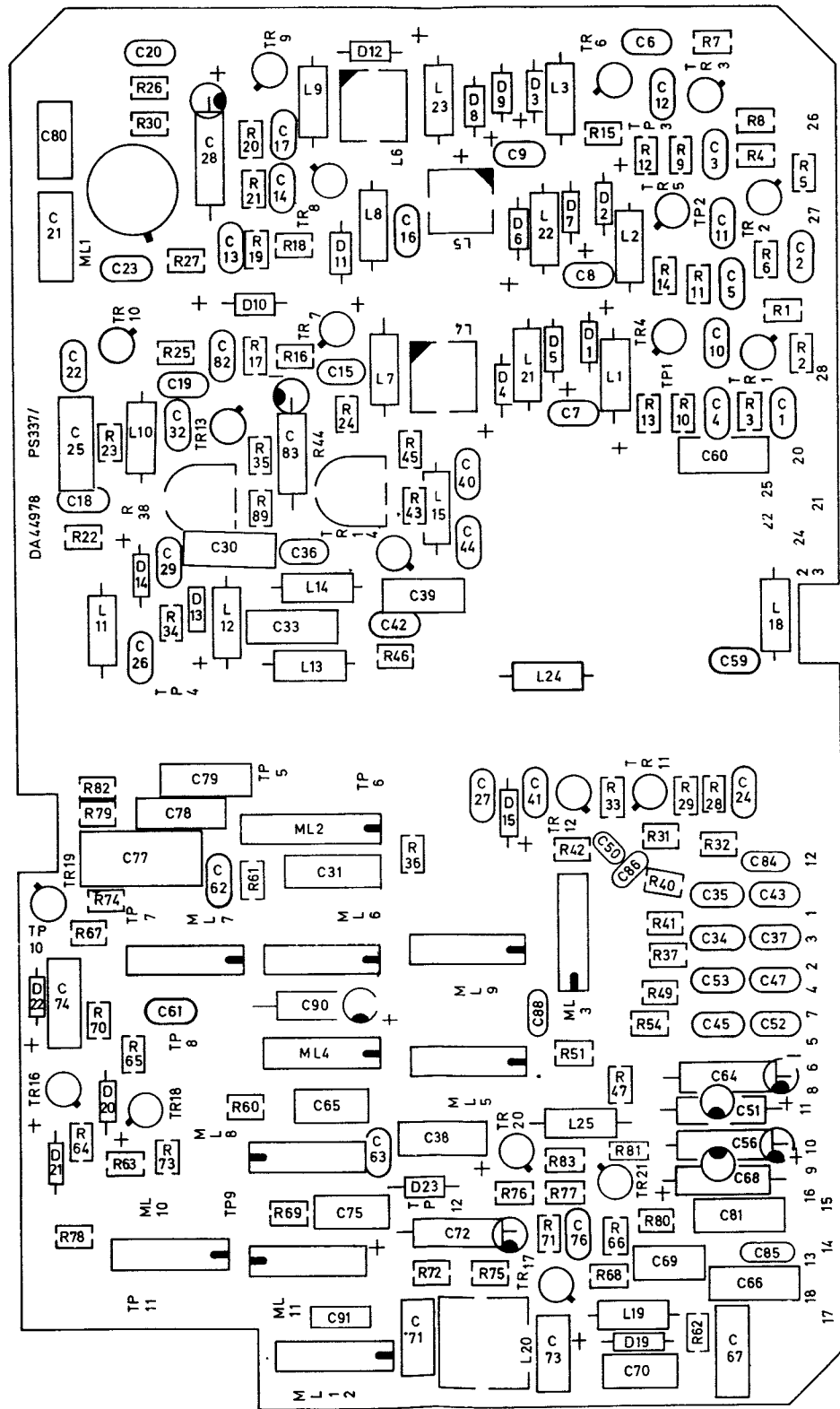
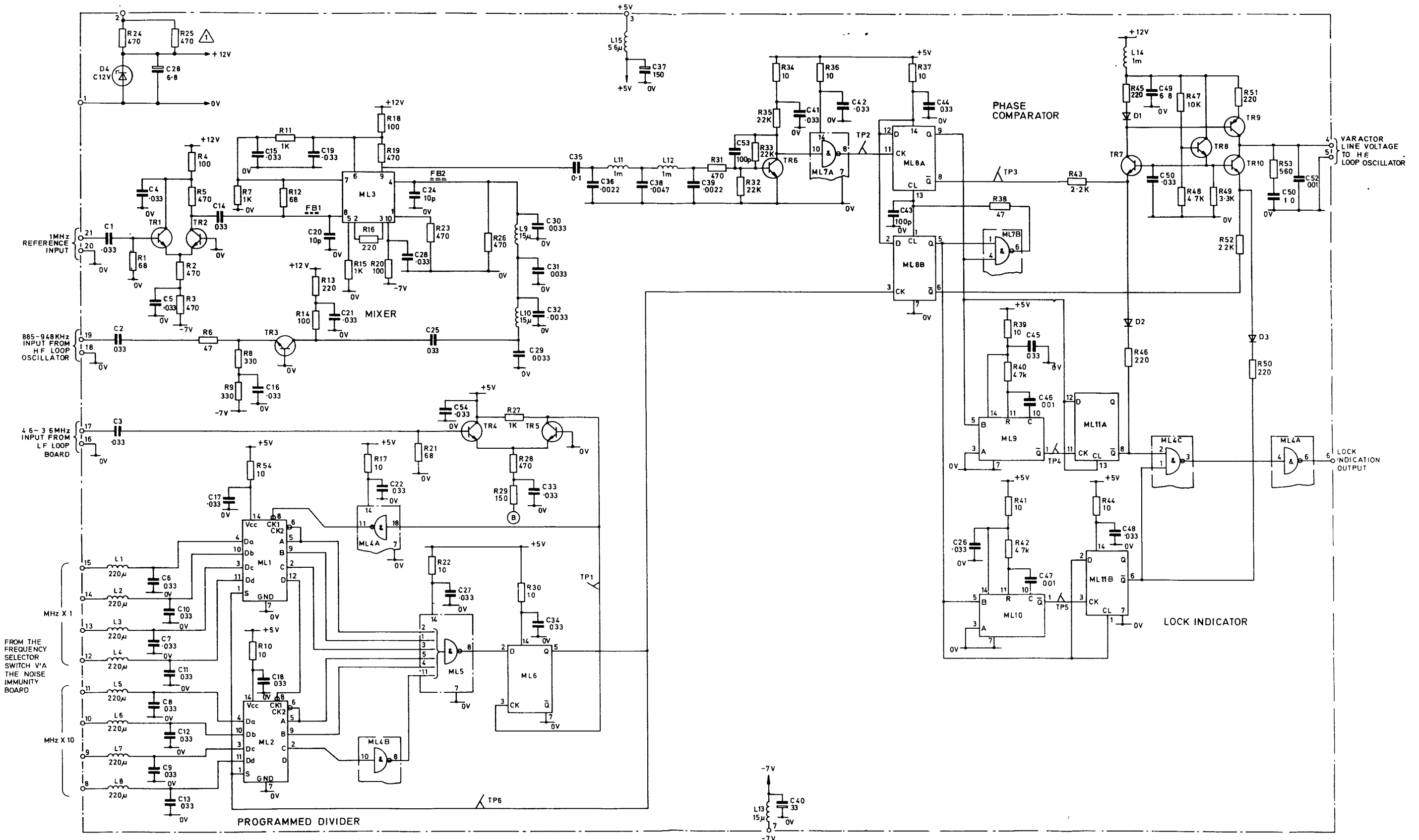


Fig. 15

HF loop boards PS337/3 and PS337/4 : component layouts

Fig. 15



REFER TO MOD No A8585

Fig. 14

Transfer loop board PS338: circuit

Fig. 14

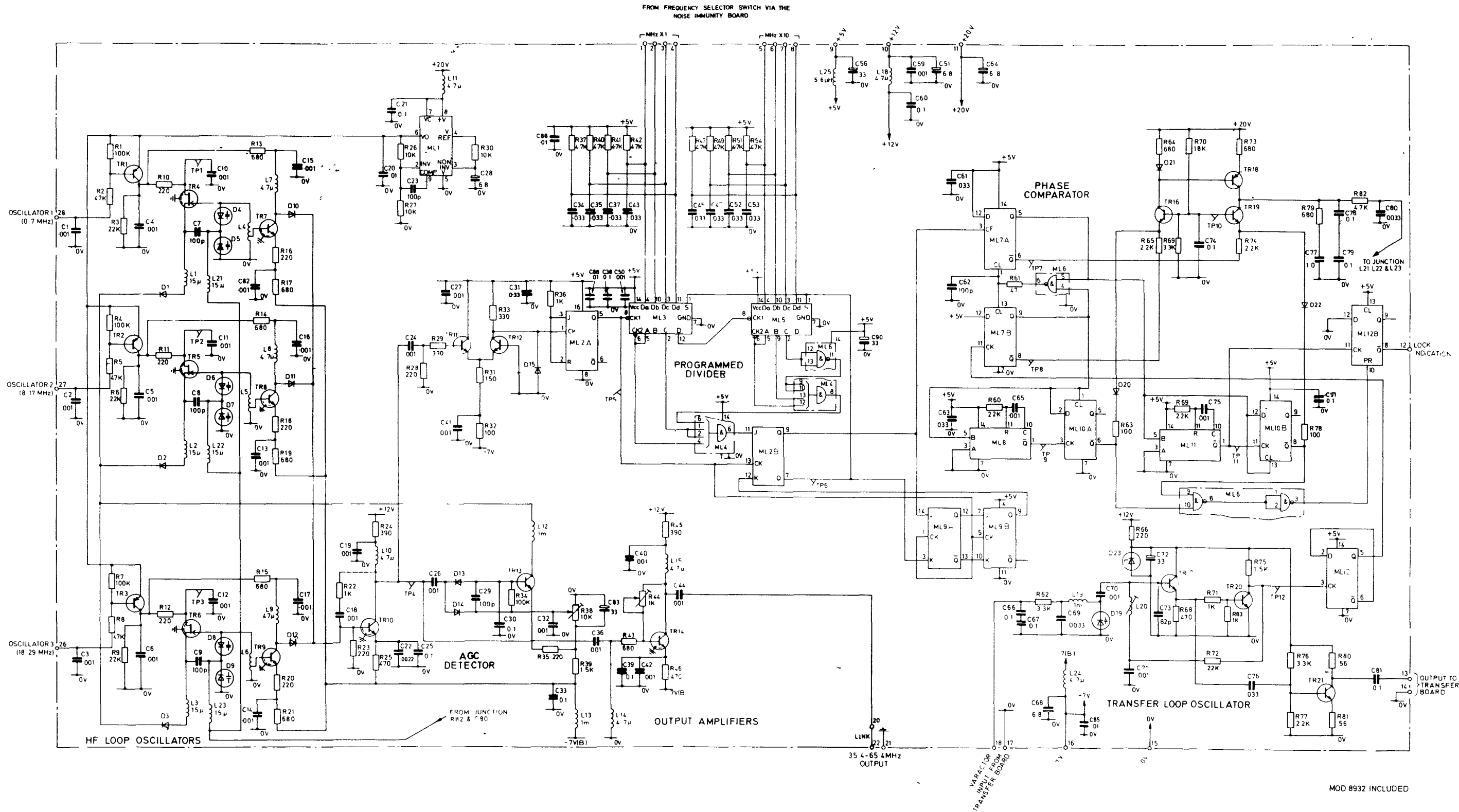


Fig. 16

HF loop board PS 337/3 : circuit

Fig.16

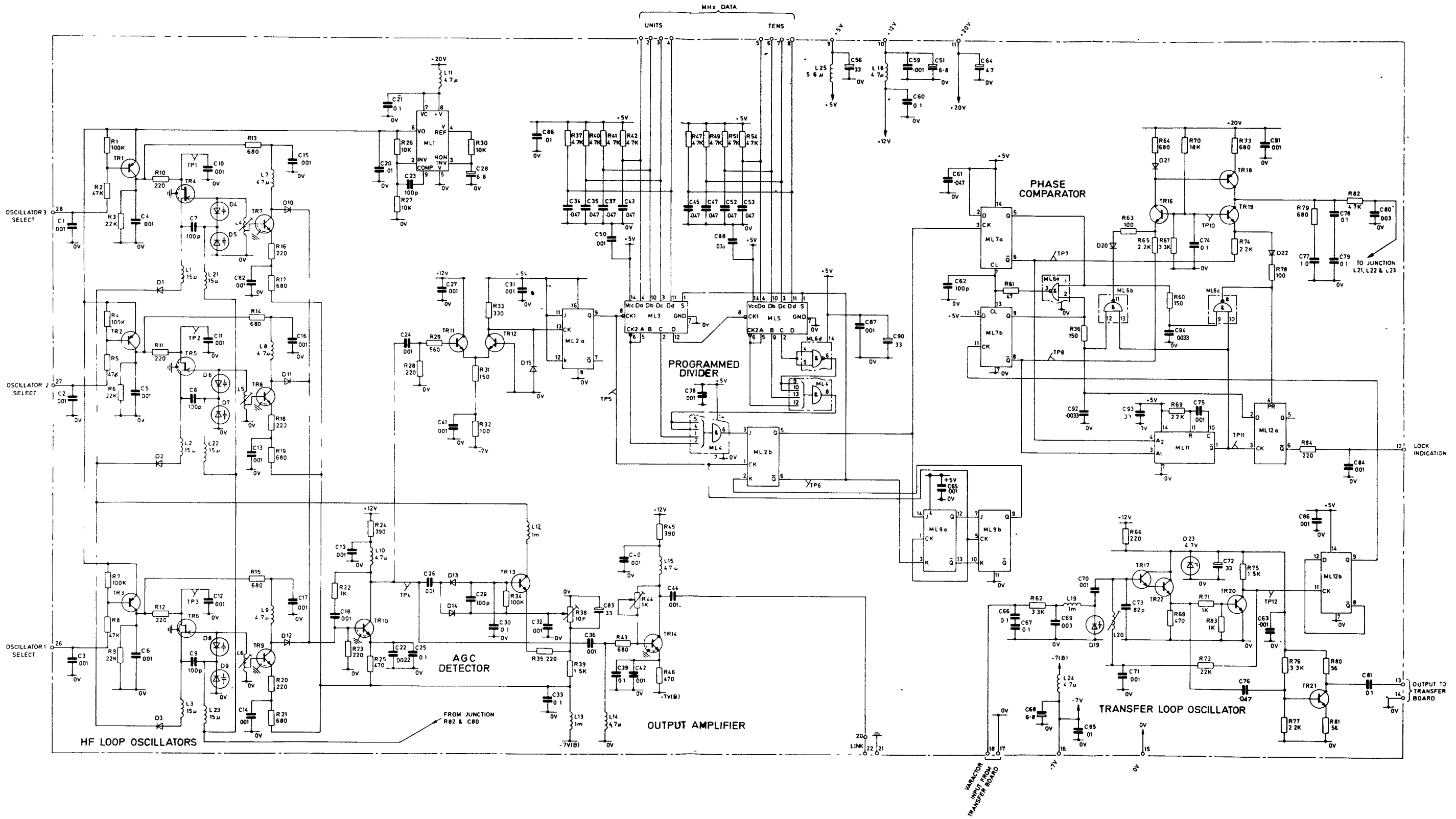


Fig. 17

HF loop board PS337/4: circuit

Fig. 17

## Chapter 8

## CIRCUIT DESCRIPTION OF A.F. AND R.F. STAGES

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INTRODUCTION

1. This chapter contains a circuit description of those boards in the drive unit which have the audio amplifier stage, the low-level modulation stage, r.f. mixing and low-level r.f. amplifier stages.

2. The a.f. and r.f. stages are identical in the two drive units but for the sideband filters which have a bandwidth of 3 kHz (MA.1720A) or 3.4 kHz (MA.1720S).

3. The two relevant boards are as follows:

- (1) Low-level board PM.341.
- (2) Mixer and output board PM.342

4. The remaining ancillary boards in the drive unit are described in Chap. 9 which includes the control board PM.345 and the front-panel switch and indicator wiring. It may be necessary to make cross-references to this chapter during the course of the following descriptions, and also to the flow circuits and interconnection diagrams contained in Chap. 1.

#### LOW-LEVEL BOARD PM.341 (fig. 1 and 3)

5. The low-level board processes all the audio and key input signals to the drive unit and produces a modulated output of 1.4 MHz which is translated to the final output frequency by the mixer and output board. The board also contains the necessary attenuation circuits and relay drivers for selection of the required sideband filters. The block diagram in fig.1 is largely self-explanatory and is also an aid to understanding fig. 3.

#### Keyed mode

6. The drive unit generates a keyed output, by keying a 1 kHz oscillator, which is then applied to one of the balanced modulators. When either the key or c.w. position is selected on the front panel, +12V is applied to the board via either pin 45 or 46, thus turning on TR9 and thence TR14, connecting +12V to the tone insertion oscillator. A +12V supply is also connected to TR1 via D18 and D12, turning on TR1 thus switching off the -7V regulator transistor TR3 and muting the channel 1 audio amplifier.

7. The keying input to the board is direct keying on pins 44 and 43; a closed key connects pins 44 and 43 and takes TR15 base to 0V. TR15 collector rises towards +12V, producing the following results:

(1) It switches on TR18, connecting the output of the L-C audio oscillator TR19 into the main audio path via R59, C29.

(2) It operates the mute delay circuit TR20-TR26. In the 'normal' state, C40 is charged to approximately 6.5V and thus TR25 and TR26 are conducting, giving a 0V output to the 'OR' gate on the control board and muting the output. Upon initiation of keying, TR20 and TR22 are turned on, discharging C40 rapidly to 0V via R84; this turns TR25 and TR26 off, allowing the collector to rise to +12V which is applied to the control board to demute the exciter. Upon cessation of keying, TR20 and TR22 are turned off, C40 charges towards +12V via R83, and when the potential on the base of TR25 reaches 6.5V, TR26 turns on taking pin 47 to 0V to mute the exciter. This ensures that so long as keying is not suspended for more than 2 seconds the exciter and any associated equipment remain active, but after this period of time they are automatically muted.

Tone oscillator

8. The tone insertion oscillator (1 kHz) consists of a tuned transformer (T1) coupled oscillator; feedback is provided by R68 and R69 in the emitter circuit of TR19; R69 provides adjustment of the feedback level. Output level adjustment is provided by R65.

RTTY mode

9. The RTTY facility is not incorporated in either the MA.1720A or MA1720S drive units.

Audio mode

10. The audio input is fed onto the board at pins 41 (audio 1) and 35 (audio 2), and is routed to pins 38 (32) via front-panel level-control potentiometers; from there the inputs are applied to similar a.f. amplifiers.

11. The audio 1 input at pin 38 drives the differential amplifier TR10, TR12 via the phase splitter TR6. The output at TR12 collector is applied to amplifier ML1, which has a gain of approximately 200 times; a.g.c. action is provided by TR16 and diodes D13, D17. A sample of the audio output from ML1 is detected by D19, D23 and the resulting signal is used to control the current through TR16 and thus through D13 and D17; as the effective impedance of D13 and D17 is dependent upon the current flowing through them, this controls the overall gain of the amplifier. A potential of -3V is required on TR16 base to turn it on, and to set the output level from the amplifier at approximately 4.5V p-p.

12. The output of ML1 is applied to the level control gates (TR28 and 32) via the 'channel 1 gain' potentiometer R73. The level control gates are brought into operation when reinserted carrier modes are selected in order to reduce the gain of the audio channel, thus preserving a constant p.e.p. level at the output.

13. The audio 2 input is similarly processed in the circuit comprising ML2 and associated components, and is applied to a 16 dB level gate via potentiometer R75.

VOX mode

14. VOX operation is available on channel 1 on single sideband modes. A sample of the output from ML1 is applied via the 'VOX sensitivity' potentiometer R79 to the amplifier TR23, TR24, the output of which operates the Schmitt trigger TR27, TR29. The output of the Schmitt switches TR33 in the mute delay circuit TR33-TR39, which operates in the same fashion as the c.w. mute delay circuit, giving a fast attack, and a 2-seconds decay time.

Production of 1.4 MHz first i.f.

15. The 1.4 MHz signal, derived from the reference oscillator, is fed onto the board at pin 16 at a level of about 0 dBm and applied to the a.g.c. amplifier TR43-TR46, which stabilises it at a level of 250 mV r.m.s. From pin 16 the signal is passed into a variable attenuator formed by R133 and TR40, the output of which is amplified by TR43 and TR44. The signal at the emitter of TR44 is amplified by TR45 and detected by D35 and D36; the resultant d.c. signal is amplified in TR46 and then applied to TR40, thus controlling the overall gain of the amplifier. The output level is adjustable by R149, and

is set to be exactly 250 mV r.m.s. at TP5. The low-impedance output from TR44 emitter is applied in parallel to:-

(1) The balanced modulator stages TR41, D33, TR47 (channel 1) and TR42, D34, TR48 (channel 2).

(2) The 1.4 MHz carrier insertion stage TR49-TR52.

16. The output from channel 1 level gates is amplified in TR34, TR37, and the low-impedance output from TR37 emitter may be applied to either of the balanced modulators according to the state of RLA and RLB. The channel 2 modulating input at TR35 base is amplified in TR35, TR38; the low-impedance output from TR38 is applied to the channel 2 balanced modulator when the i.s.b mode is selected. The gain in channel 2 is set to be 6 dB down on that of channel 1.

17. The outputs of the balanced modulators are routed via band-pass filters to the input of the feedback summing amplifier TR55, TR57 where the 1.4 MHz carrier frequency is re-inserted (via the amplifier and switch TR51) to form the first i.f. of 1.4 MHz; this is fed off the board at pin 10 at a level of 0 dBm. D45, D46, D47 form a limiter circuit arranged to operate when the level on TP6 is about 9V p-p (output level of +2 dBm) to prevent overloading of the following stages.

#### Attenuation stages

18. Attenuation gates are provided as follows, energized by +12V d.c. inputs to pins 26 (6 dB), 23 (16 dB) and 20 (26 dB).

(1) 6 dB gates:

(a) TR28, shunting the channel 1 modulating input to TR34 (attenuates signal by 6 dB).

(b) TR54, shunting the 1.4 MHz output from TR51.

(2) 16 dB gates:

(a) TR32, shunting the channel 1 modulating input to TR34 (attenuates signal by 1.5 dB).

(b) TR30, shunting the channel 2 modulating input to TR35.

(c) TR60, shunting the 1.4 MHz output from TR51.

(3) 26 dB gate: TR53, shunting the 1.4 MHz output from TR51.

19. The 'tune' attenuator TR61 is energized by +12V d.c. at pin 27, and shunts the 1.4 MHz output from TR51. Its attenuation may be adjusted by means of R204.

20. When any of the above attenuation gates are selected, +12V is applied to the base of TR49 via the appropriate diode in the chain D37-D41 and the base resistor R166. TR49 will switch on, switching off TR50 which will switch on TR52. This action will switch on the 1.4 MHz amplifier TR51, and the 1.4 MHz signal will be applied via the amplifier to the appropriate attenuator gate. The gain of this stage is controlled by R184.



Relay driver stages

21. Relays RLA and RLB are driven by TR21 and TR31 respectively; their contacts control the routing of the modulating inputs to the balanced modulators.
22. When the l.s.b. mode is selected by applying +12V to pin 30, RLA in TR21 collector is energized and contact RLA1 routes the channel 1 input to the channel 2 modulator, the output of which is taken to the u.s.b. filter.
23. When the u.s.b. mode is selected, both relays are de-energized and the channel 1 input is routed via the channel 1 modulator to the l.s.b. filter.
24. When the i.s.b. mode is selected, RLB is energized via TR31; RLA is de-energized, and the channel 1 input therefore generates the upper sideband while the channel 2 input generates the lower sideband.

Auxiliary control inputs

25. The auxiliary control functions are summarised in Table 1.

TABLE 1  
Control functions on low level board

Control input	Operation on application of +12V
Full power (pin 9)	Sets the output to maximum by switching on TR58 and setting the gain of the output amplifier to maximum.
Low power (pin 8)	Switches on TR59 and TR56 allowing output level to be adjusted by R190; this enables the output level to be set between 0 dB and -7 dB down on the normal level.
- 6 dB (pin 26)	Turns on 1.4 MHz switch (TR51) via D39; operates 1.4 MHz 6 dB gate (TR54), and 6 dB audio gate (TR28).
-16 dB (pin 23)	Turns on 1.4 MHz switch (TR51) via D37; operates 1.4 MHz 16 dB gate (TR60), and 16 dB audio gates (TR30, TR32).
-26 dB (or -20 dB) (pin 20)	Turns on 1.4 MHz switch (TR51) via D40; operates 1.4 MHz 26 dB gate (TR53).
I.S.B. (pin 29)	Operates RLB (TR31) and 6 dB audio gate via D26.
Tune (pin 27)	Mutes audio by turning off -7V regulator (TR3) via D28. Turns on 1.4 MHz switch (TR51) via D41; operates tune gate (TR61) allowing tune level to be set by R204. Also operates full-power gate (TR58) via D51, and inhibits low-power gate.
L.S.B. (pin 30)	Operates RLA (TR21).
RTTY ON (pin 21)	Not applicable.

TABLE 1 (cont.)

Control input	Operation on application of +12V
C.W.-6 (pin 45)	Switches on the tone-insertion oscillator by turning on TR14 via D4 and D10. Operates 6 dB audio gate (TR28) via D1, D2, D27, and 1.4 MHz switch (TR51) via D1, D2 and D39, and 1.4 MHz 6 dB gate (TR54) via D1, D2. Also mutes audio by turning off -7V regulator (TR3) via D4, D18 and D12.
C.W. supp. (pin 46)	Switches on the tone-insertion oscillator by turning on TR14 via D3 and D10. Mutes audio by turning off -7V regulator (TR3) via D3, D18 and D12.

### Meter amplifier

26. Transistors TR62-TR64 form a meter-drive circuit. The amplifier accepts audio inputs at approximately -30 dBm at pin 15 and, with diodes D48, D49 in the feedback network, provides 100  $\mu$ A d.c. for full-scale deflection of the front-panel meter. R195 is for initial calibration of the meter circuit.

### MIXER & OUTPUT BOARD PM.342 (fig. 5)

27. This board contains the following circuits:-

- (1) First and second mixer circuits, with associated filters and amplifiers.
- (2) Input amplifiers for the 34 MHz fixed and 35.4-65.4 MHz variable frequencies.
- (3) Muting circuit.

### Mixer and output amplifier stages

28. The 1.4 MHz first i.f. from the low-level board is fed onto the mixer and output board at pin 4 at a level of 0 dBm and into the first mixer stage T1, T2; there it is mixed with the 34 MHz stable frequency from the 34 MHz generator board to produce the second i.f. of 35.4 MHz. Unwanted frequency components are removed by the bandpass L-C filter including C7-C30, which provides 50 dB attenuation of the fundamental and 70 dB image rejection.

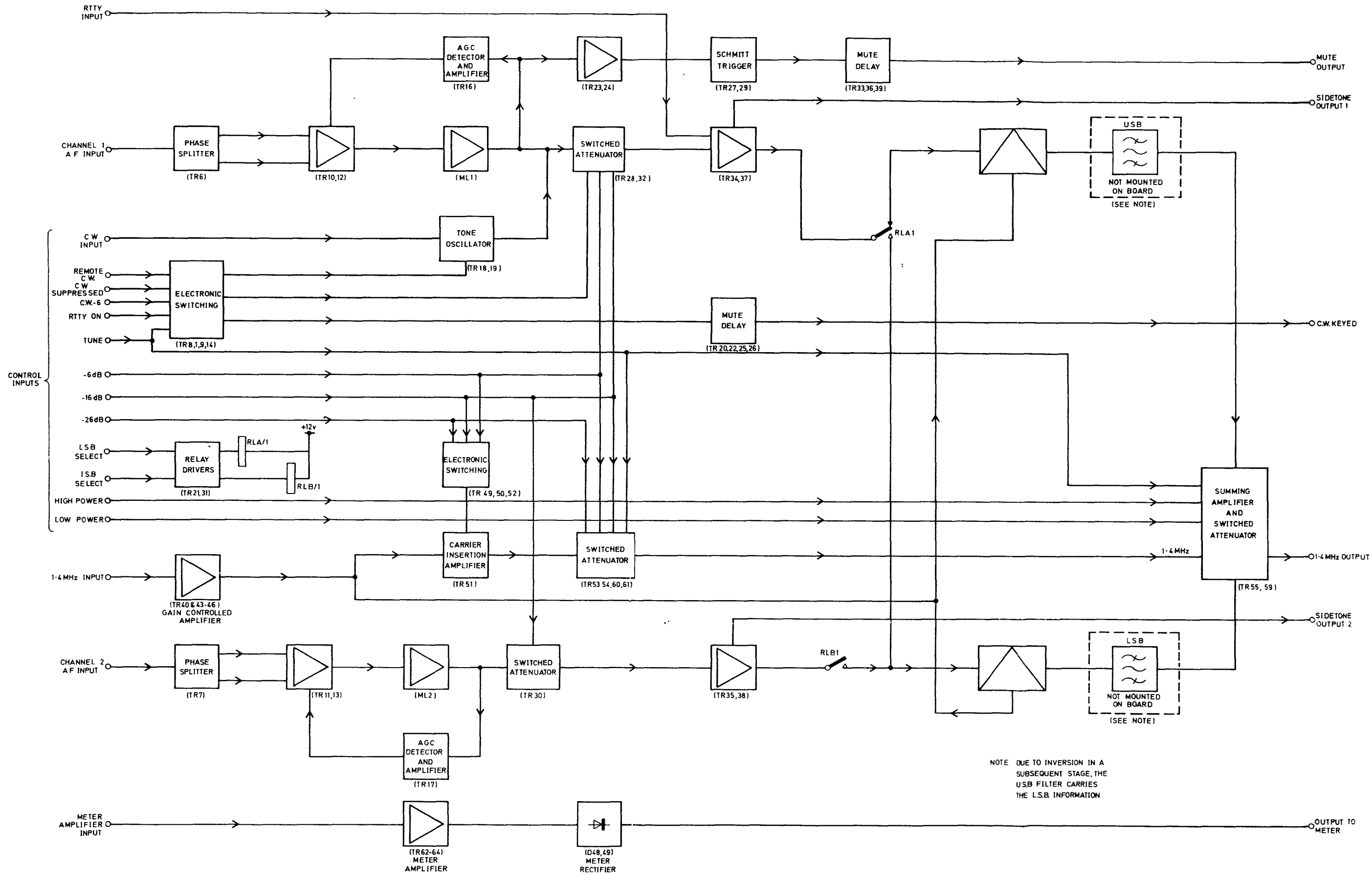
29. The signal is then amplified by TR7, TR8, filtered again in the crystal filter, (which reduces wideband noise into the final mixer and has a pass-band of  $\pm$  6 kHz centred on 35.4 MHz), and then fed into the final mixer T8, T10. There it is mixed with a signal in the range 35.4-65.4 MHz derived from the synthesizer boards, and the resulting signals are filtered by the low-pass filter L8-L10 (which has a sharp cut-off above 30 MHz). The output from the filter is a signal in the range 1-30 MHz at a level of -16 dBm; this is applied via the buffer amplifier TR14, TR15, which also incorporates a gain control R67, to the input of the five-stage wideband output amplifier TR9-TR13. The output at a level of +23 dBm is taken off the board at pin 16.

Input amplifier stages

30. The two input amplifiers, for the 34 MHz fixed frequency and the 35.4-65.4 MHz variable frequency, are similar in construction and operation.
31. The 34 MHz signal is fed onto the board via pin 7 at a level of 0 dBm and a.c. coupled into the base of the driver transistor TR1. The output of the push-pull stage TR2, TR3, is a 20V p-p sinewave to the first mixer.
32. The 35.4 - 65.4 MHz signal is fed onto the board via pin 8 at a level of 0 dBm, and a.c. coupled into the base of driver transistor TR4. The output of the push-pull stage TR5, TR6, is a 20V p-p sinewave to the second mixer.

Muting stage

33. The muting circuit TR16, TR17 controls the d.c. supply to the collectors of TR9-TR12 in the output amplifier. Transistor TR17 is normally held on by the +12V d.c. input to pin 12 from pin 5 on the control board, and TR16 is bottomed, applying +20V to the output amplifier. When TR17 base is taken down to 0V, TR16 cuts off and removes the supply to the amplifier.



NOTE DUE TO INVERSION IN A SUBSEQUENT STAGE, THE USB FILTER CARRIES THE LSB INFORMATION

Fig. 1

Low-level board PM.341 : block diagram

Fig. 1

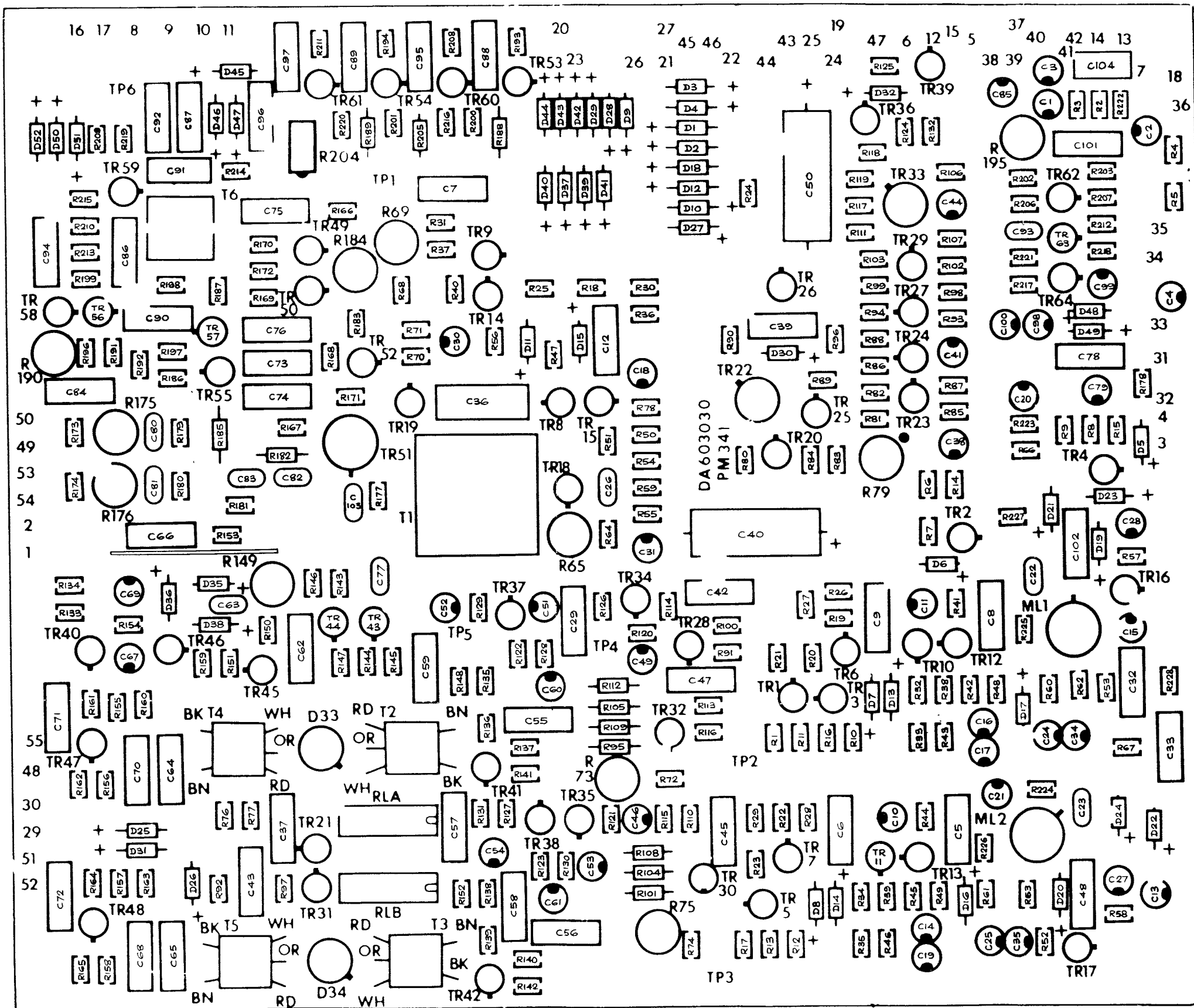


Fig. 2

Low-level board PM.341 : component layout

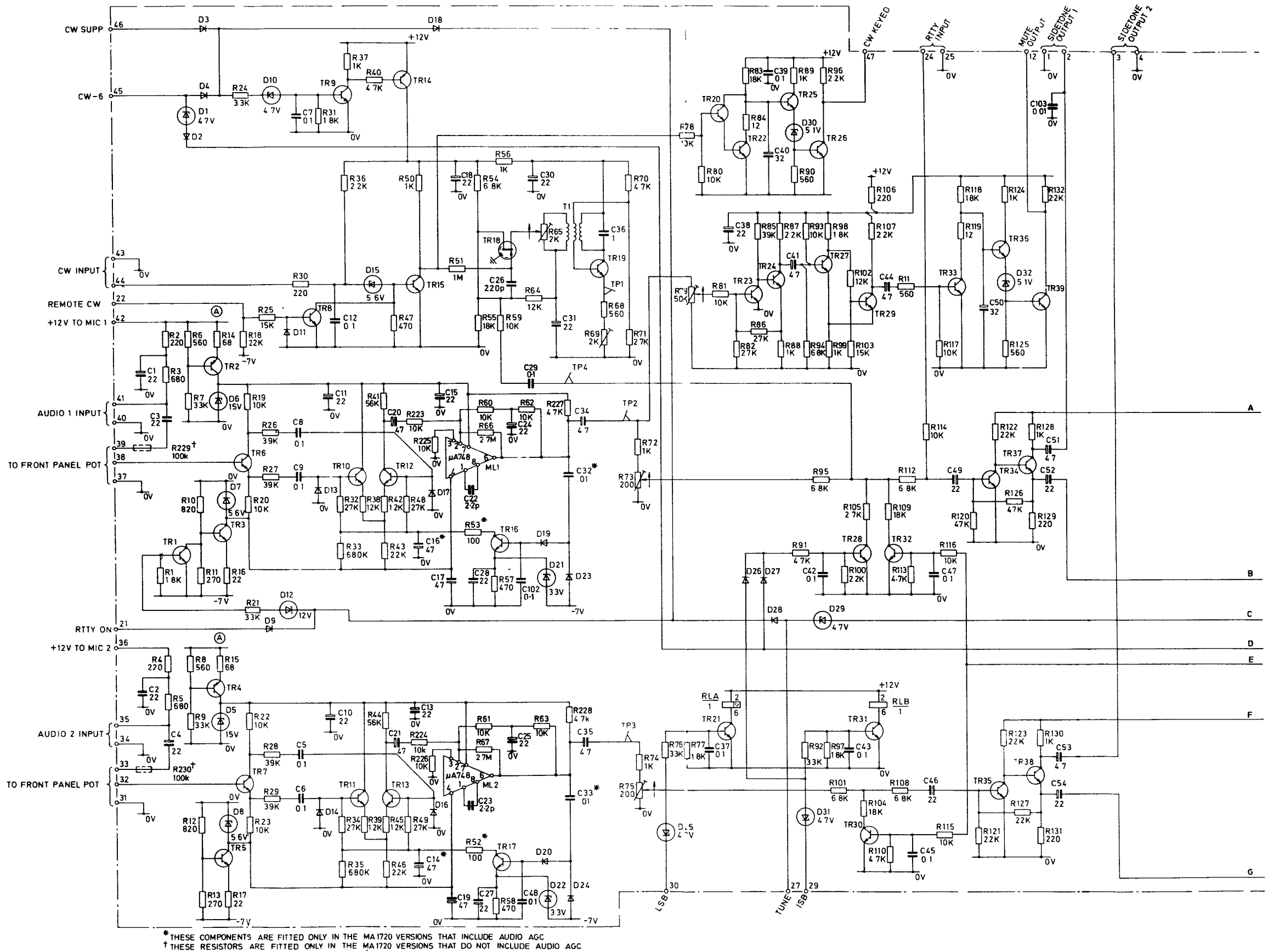


Fig. 3a

Low-level board PM.341 : circuit (Sht. 1)

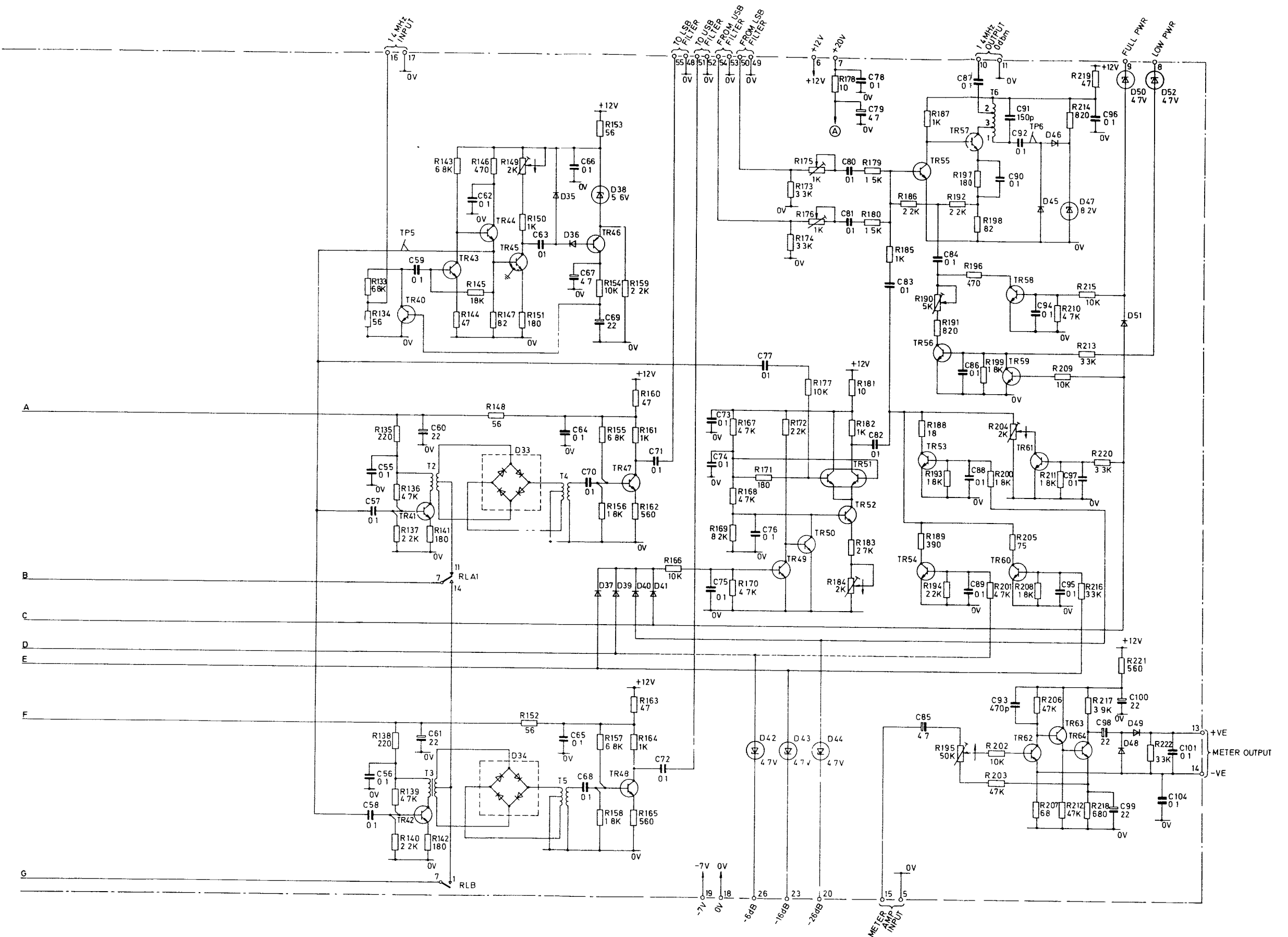
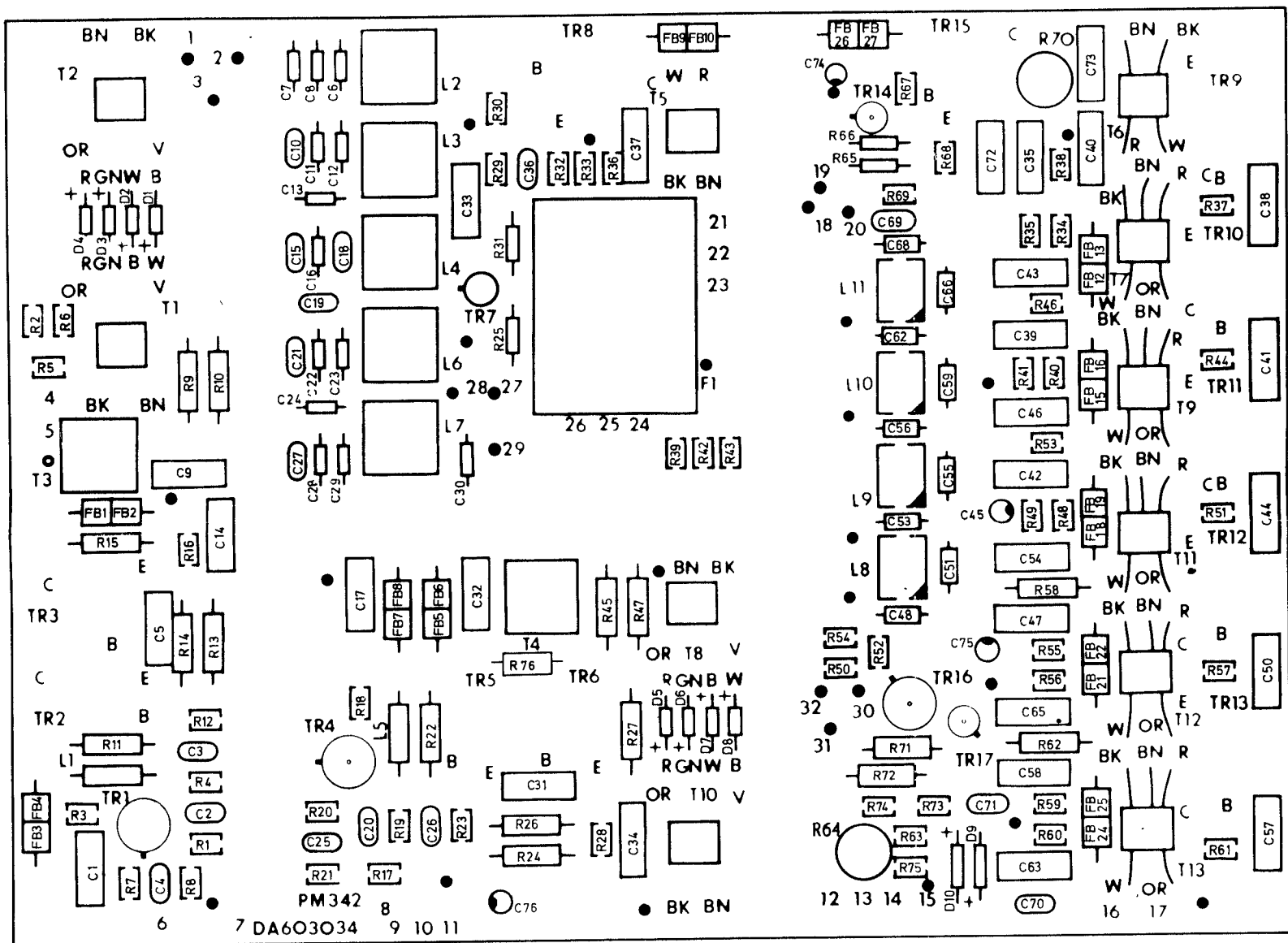


Fig. 3b

Low-level board PM.341 : circuit (Sht. 2)

Fig. 3b



Mixer and output board PM342: component layout Fig. Chap Page Nov 84 (Amdt 7)



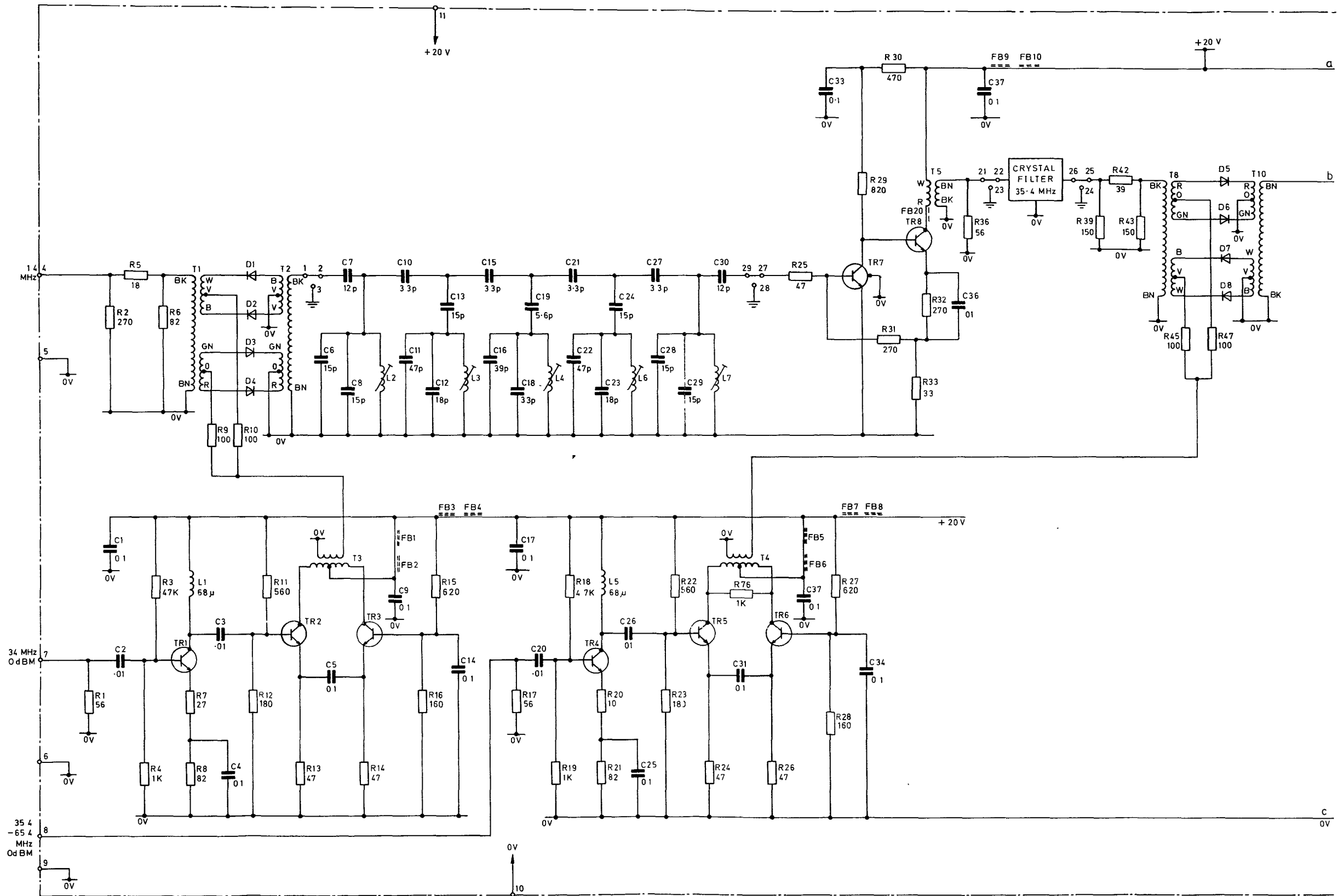


Fig. 5a

Mixer and output board PM342: circuit (sheet 1)

Fig. 5a

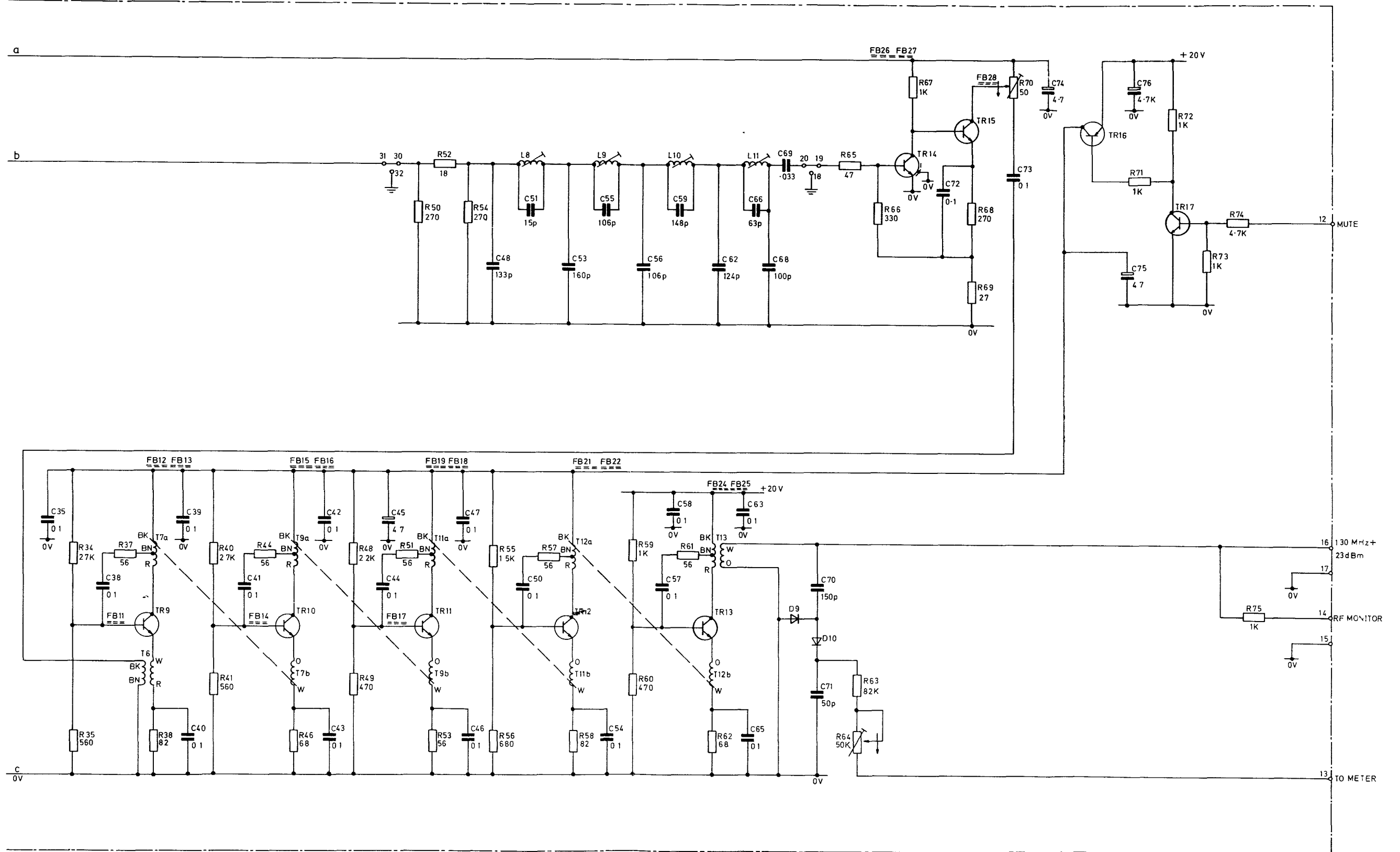


Fig. 5b

Mixer and output board PM 342: circuit (sheet 2)

Fig.5b

## Chapter 9

## CIRCUIT DESCRIPTION OF ANCILLARY STAGES

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INTRODUCTION

1. This chapter contains a circuit description of the remaining ancillary boards or sub-assemblies in the drive unit; these embrace control functions and power supplies and are as follows:

- (1) Front panel switches and indicators
- (2) Control board PM.345
- (3) Power supply unit, including power supply board PM.343

These boards and sub-assemblies are identical for both drive units.

2. In general, the control board functions are initiated by the switches on the front panel; hence, it will be necessary to cross-refer to the flow-circuits and interconnecting diagrams contained in Chap. 1. The front-panel switches also affect the operating conditions of the low-level board (Chap.8).

FRONT-PANEL SWITCHES AND INDICATORS (fig. 2)

3. In the main, the front-panel switches initiate logic command levels to solid-state switches on the following boards:

- (1) Control board PM.345
- (2) Low-level board PM.341
- (3) Mixer and output board PM.342

4. The effect of the various switch positions becomes apparent when reading the description of the control board PM.345 in this chapter, the description of the low-level board PM.341 in Chap. 8 and the drive unit functional description in Chap. 1. The circuit of the frequency selection switches is given in fig. 3 of Chap. 7.

CONTROL BOARD PM.345 (fig. 4)

5. The control board logic and switching circuits accept the inputs and produce the outputs summarised in Table 1.

TABLE 1  
Control board : inputs and outputs

Input/pin	Output/pin
Reset (+12V) 29	'Reset' to Tx (+12V) 30 Removes earth from RESET lamp 4 Removes +12V from remote 'Reset' line 32
In-lock (+5V) 25,26,27	Earth to in-lock lamp. 3 +12V to remote in-lock line 31
Mute (+12V) 24	'Mute' to mixer and output board and Tx (0V) 5
Selector switch inputs (+12V) 18,29,20,21	De-mute to mixer and output board and Tx (+12V) 5

TABLE 1 (cont.)

Input/pin		Output/pin	
Tune switch (+12V)	17	'Tune' to low level board (+12V)	11
		'Inhibit' to mode switch (0V)	12
		'De-mute' to mixer and output board and Tx (+12V)	5
Fault (0V)	1	Earth to RESET lamp	4
		+12V to remote 'reset' line	32
		'Mute' to mixer and output board and Tx (0V)	5
Reduced power (+12V)	6	Earth to REDUCED POWER lamp	7
		+12V to remote 'reduced power' line	33
Ready (0V)	8	Earth to READY lamp	10
		+12V to remote 'ready' line	34
		'Enable' to mode switch (+12V)	12
Standby (+12V)	13	Earth to 'standby' line	14
E.H.T.-on (+12V)	15	Earth to e.h.t.-on line	16
<u>Power supplies</u>			
+12V	9		
+5V	2		
-7V	28		
Earth	22		
Logic earth	23		

RESET input (pin 29)

6. Pin 29 is normally open-circuit. When the RESET button on the front panel is pressed, +12V is applied to pin 29; this turns TR2 on, with the following effects:

- (1) TR1 turns off, applying +12V to the linear amplifier as a 'Reset' command via pin 30.
- (2) The '0' at TR2 collector is inverted by G1 and used to trigger the 2-second monostable ML<sup>4</sup>, which applies a '0' for 2 seconds to G2 and G3; this resets the latch described in paras. 18 to 20.

In-lock input (pins 25, 26, 27)

7. The inputs to these pins are derived from the lock indicators associated with each of the three phase-comparators in the frequency synthesizer, with output '1' to indicate the 'in lock' condition. When all three inputs are at '1', the output of G6 is '0'; this is inverted to '1' by G8 and applied to:

- (1) TR4, which turns on and lights the 'in-lock' lamp via pin 3, and also turns TR5 on to apply +12V to the remote 'in-lock' line via pin 31.
- (2) G4 in the latch circuit, leaving the latch in the 'normal' (de-muted) condition.

#### Mute input (pin 24)

8. Pin 24 is normally open-circuit. When MUTE is selected, +12V is applied via pin 24 to TR8, turning it on and applying '0' to one of the inputs of G9; G9 therefore gives a '1' output which turns TR9 on and applies a 'mute' command of 0V to pin 5.

#### Selector switch inputs (pins 17 to 21)

9. A +12V signal on any of these inputs, applied through TR12 and G10, results in a '1' being applied to G9. If there is no +12V signal present at any of these inputs, a '0' is applied to G9, which results in a 0V 'mute' command output from pin 5 via TR9.

10. A +12V signal at pin 17 (TUNE selected), applies a +12V 'tune' signal to the low-level board via D17 and pin 11; it also switches TR17 on via Zener diode D18, removing the +12V supply to the LOCAL/EXTENDED/REMOTE switch, via TR16 and pin 12, in order to prevent selection of other modes.

#### Fault input (pin 1)

11. In normal operation, +12V is applied to pin 1; this back-biases D1, causing Zener diode D2 to conduct via R5 and turn TR3 on, thus applying logic '0' to G2. A fault condition is signalled by 0V at pin 1, resulting in a '1' input to G2 and a '0' output. This causes the output of G5 to go to '1', lighting the RESET lamp via TR6 and pin 4 and applying +12V to the remote RESET line via TR7 and pin 32. The '1' output from G5 is also applied via G7 and G9 to TR9, producing a 0V 'mute' output at pin 5.

12. If the RESET button is now pushed, the output of G5 will change to '0' only for the 2-second period of the monostable ML4; the drive unit will therefore de-mute, and the RESET lamp will extinguish for only two seconds.

#### Reduced-power input (pin 6)

13. Pin 6 is normally held at 0V. When the linear amplifier is operating at reduced power, +12V is applied, turning TR10 and TR11 on. TR10 lights the 'reduced power' lamp via pin 7, and TR11 applies +12V to the remote 'reduced power' line via pin 33.

#### Ready input (pin 8)

14. Pin 8 is held at +12V when the system is 'not ready'. When it is 'ready', the input goes to 0V, turning TR13 off, TR14 on and TR15 on. TR14 lights the 'ready' lamp via pin 10, and TR15 applies +12V to the remote 'ready' line via pin 34; TR14 also removes the drive from TR17 via D15 and D18, turning TR16 on and applying +12V via pin 1 to the LOCAL/EXTENDED/REMOTE switch.

15. In the absence of a 'ready' input (i.e. if pin 8 is at +12V), TR14 collector is at +12V which is applied to:

- (1) The 'tune' control line on the low level board via D15 and pin 11.
- (2) TR12 via Zener diode D13, D14 and R34, turning TR12 on and, via G10, applying logic '1' to pins 1 and 2 of G9.

Standby input (pin 13)

16. A +12V signal is applied to pin 13 when the front panel 'Standby On' button is depressed; this turns TR18 on and applies a 0V signal to the linear amplifier via pin 14. When 'Standby' is not selected, pin 13 is open-circuit and the output at pin 14 is +12V.

E.H.T.-on input (pin 15)

17. This facility is not used in this transmitter.

Latch circuit G3/G4

18. Gates G3 and G4 form a latch which is reset by a '0' on pin 4 of G3 and tripped by a '0' on pin 9 of G4. When the synthesizer is caused to go out-of-lock by a change in the frequency setting, a fast negative pulse is applied to pin 9 of G4 (para. 7). This trips the latch, causing a '1' on pin 11 of G5; this turns TR6 on, lighting the RESET lamp via pin 4 and applying +12V to the remote 'reset' line via TR7 and pin 32.

19. The '1' on pin 11 of G5 is inverted by G7 and applied to pin 5 of G9, causing G9 to produce a '1' output; this turns TR9 on, placing a 0V 'mute' signal on pin 5. D5 in TR9 collector protects TR9 against reverse switching pulses from a muting relay (not used in this transmitter).

20. The latch G3/G4 is reset by a '0' on pin 4 of G3, applied via pin 29, TR2, G1 and the monostable ML4 when the RESET button is pushed.

POWER SUPPLY UNIT (fig. 6)

21. The power supply board, in conjunction with external transistors and resistors, stabilizes the unregulated potentials from the transformer and rectifiers.

22. The d.c. supplies produced are as follows:-

- (1) Positive 20V  $\pm$  2V, variable, maximum current 1.5A.
- (2) Positive 5V  $\pm$  0.5V, variable, maximum current 1.5A.
- (3) Negative 7V  $\pm$  0.5V, variable, maximum current 0.5A.
- (4) Positive 12V  $\pm$  2V, variable, maximum current 1.5A.

23. Reference must be made to fig.8 of Chap.1 and fig. 1 (this Chap.) in order to locate the path from the mains input socket (rear of drive unit) via the fuse and mains on/off switching to the input of the voltage selector (fig. 6).

Power supply board PM.343

24. The four d.c. supplies are produced by four almost identical stabilizing circuits, hence, only the +5V supply is described in detail, Figure 6 shows that with the exception of large or heat-dissipating components, the majority of the components are on power supply board PM.343.

25. Each stabilizing circuit uses an integrated circuit regulator (ML1 to ML4) consisting of:-

- (1) temperature compensated reference amplifier.

- (2) error amplifier.
- (3) series-pass transistor.
- (4) current-limit transistor.

26. A simplified circuit of the regulator is shown in fig. 1. The error amplifier is used to compare the reference voltage (maximum approximately +7V) with a sample of the final stabilised output voltage (via a potential divider if greater than the reference voltage) and the output of the error amplifier is then used to control the series-pass transistor. This transistor is also controlled by a current limiting stage which itself is controlled by the current drawn from the supply by the external circuit

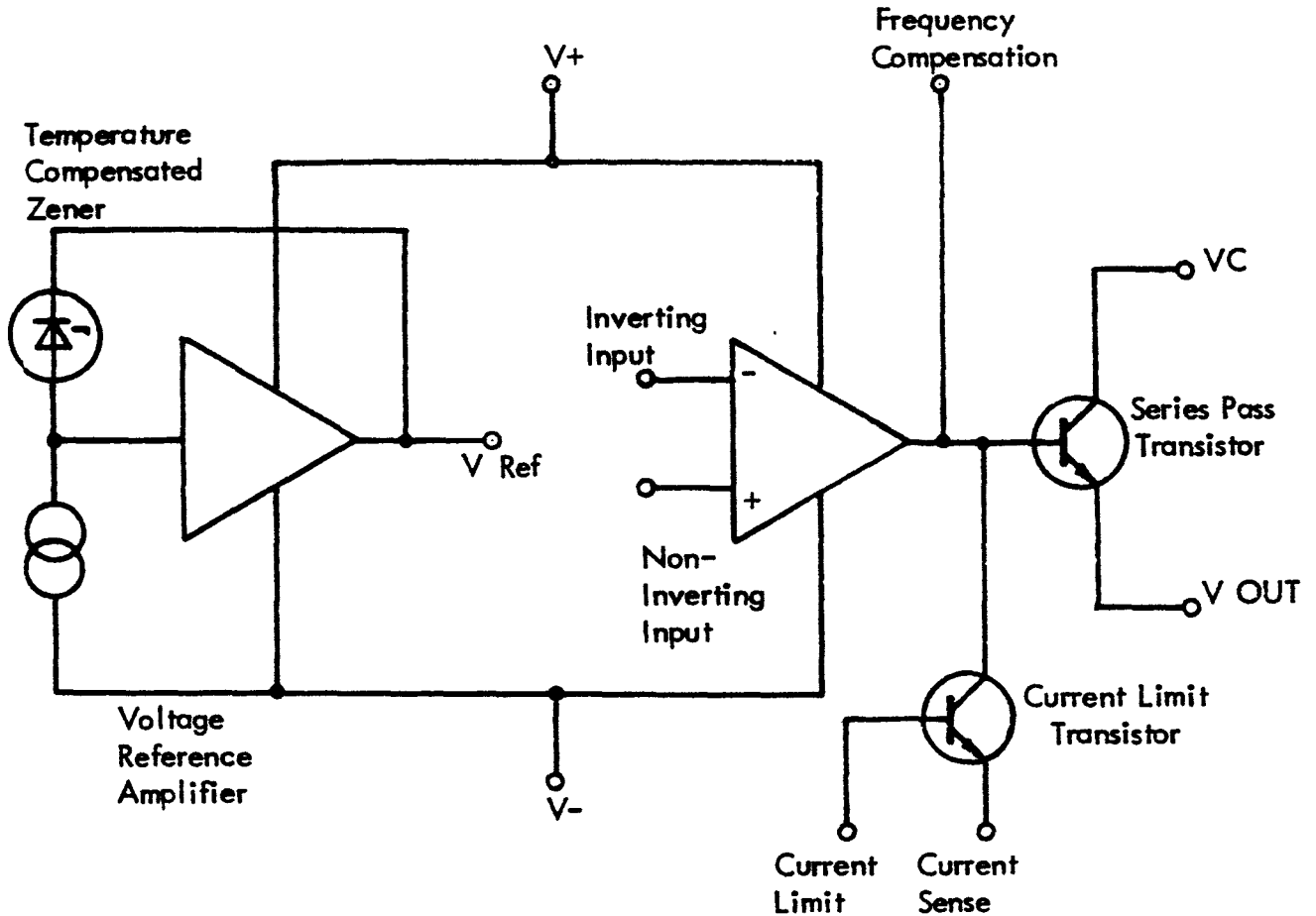


Fig.1 Integrated-circuit regulator : simplified circuit

27. The +5V regulator stage functions as follows. The voltage regulator module ML4 is fed from the unregulated output from 1D2. A reference potential is developed within ML4 and appears at pin 8. A portion of this voltage is fed via potential divider R8, R9, R10 to pin 3, the non-inverting input. Capacitor C4 provides smoothing of the reference potential.

28. Transistor 1TR1 is the series-regulator element. The +5V output appears at pin 3 of the board; C9 is the output smoothing capacitor. A sample of the 5V output is fed to the inverting input (pin 2) of ML4 and the potentials



at pins 2 and 3 are compared. The resultant output from ML4 (pin 6) is fed via TR3 and controls 1TR1 conduction in order to maintain the differential voltage at zero. Potentiometer R9 provides the output-voltage adjustment.

29. A current-limiter circuit gives overload protection. The external load current flows through 1R1 and develops a control potential across this resistor. If this control potential becomes excessive due to an excessive load current, TR3 conduction is reduced which, in turn, reduces 1TR1 conduction; hence, the output voltage is considerably reduced without causing over-dissipation in 1TR1.

► Power supply board PM372

30. Some equipments are fitted with an alternative power supply board type PM372, in place of type PM343. The minor physical differences between the type PM343 and PM372 boards are shown in Fig. 5. The mode of operation of board type PM372 is as described above for type PM343; the circuit diagram (Fig. 6) suffices for both types.

Note. References elsewhere in this publication to board type PM343 may be read as board type PM372, unless stated otherwise. ◀

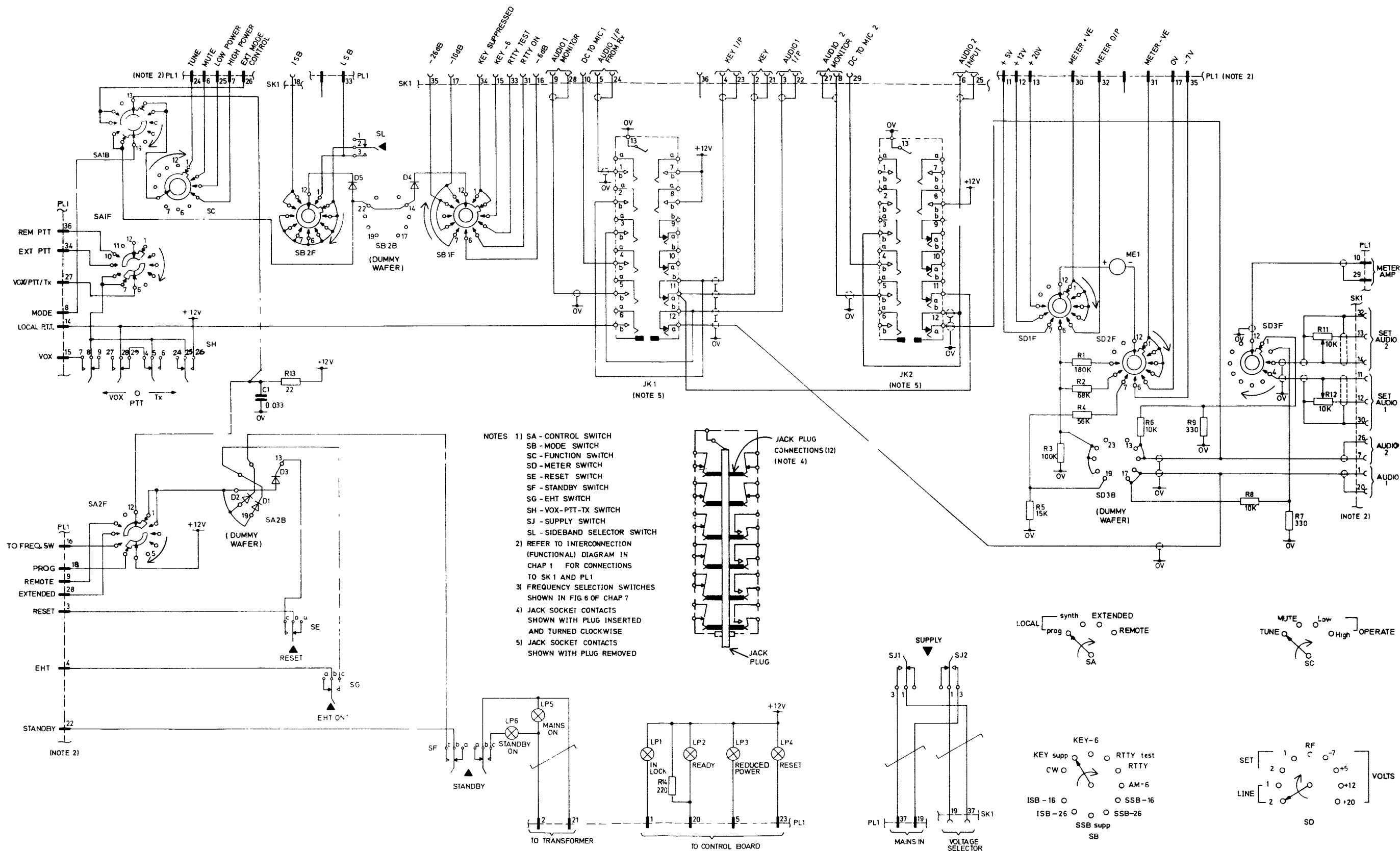


Fig. 2

Front panel : circuit

Fig. 2

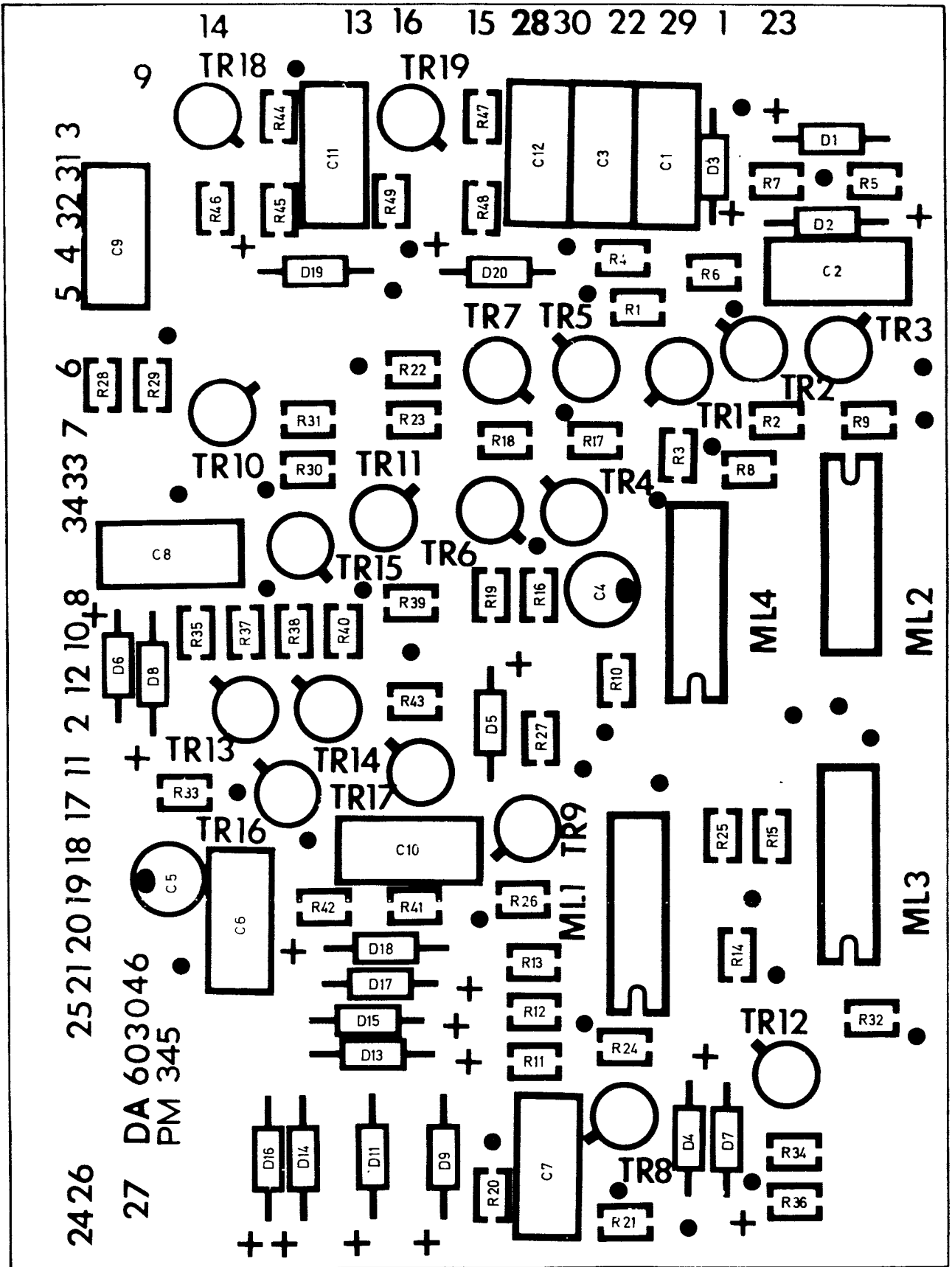


Fig. 3 Control board PM.345 : component layout

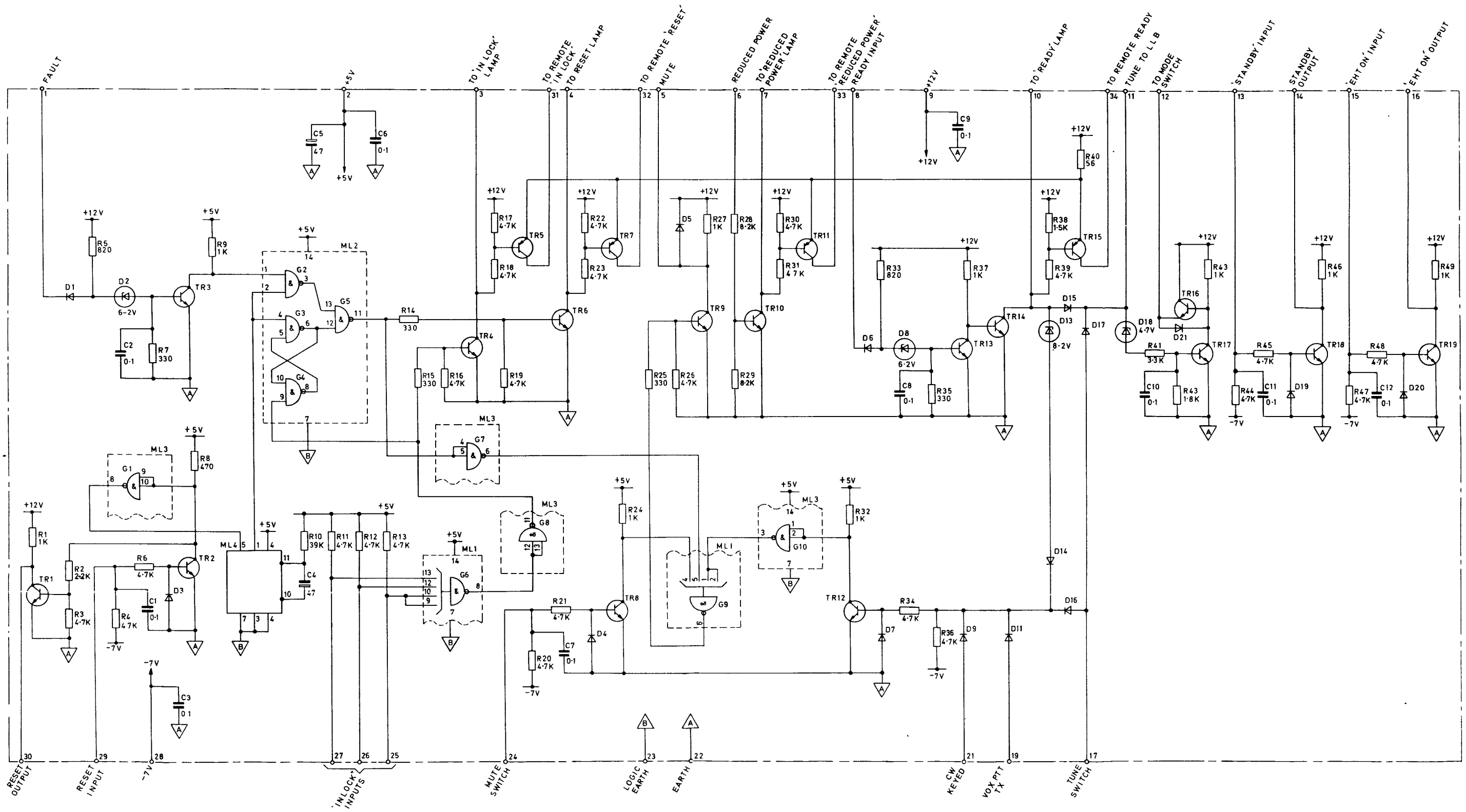
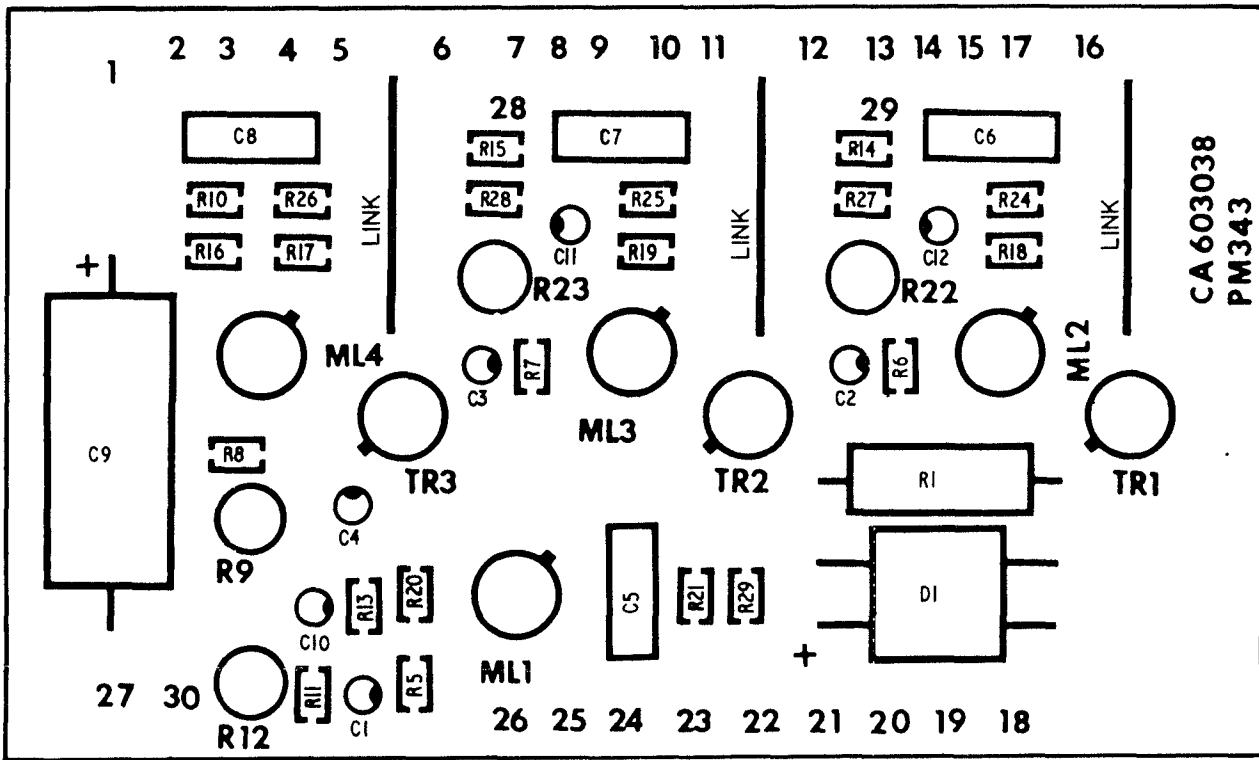
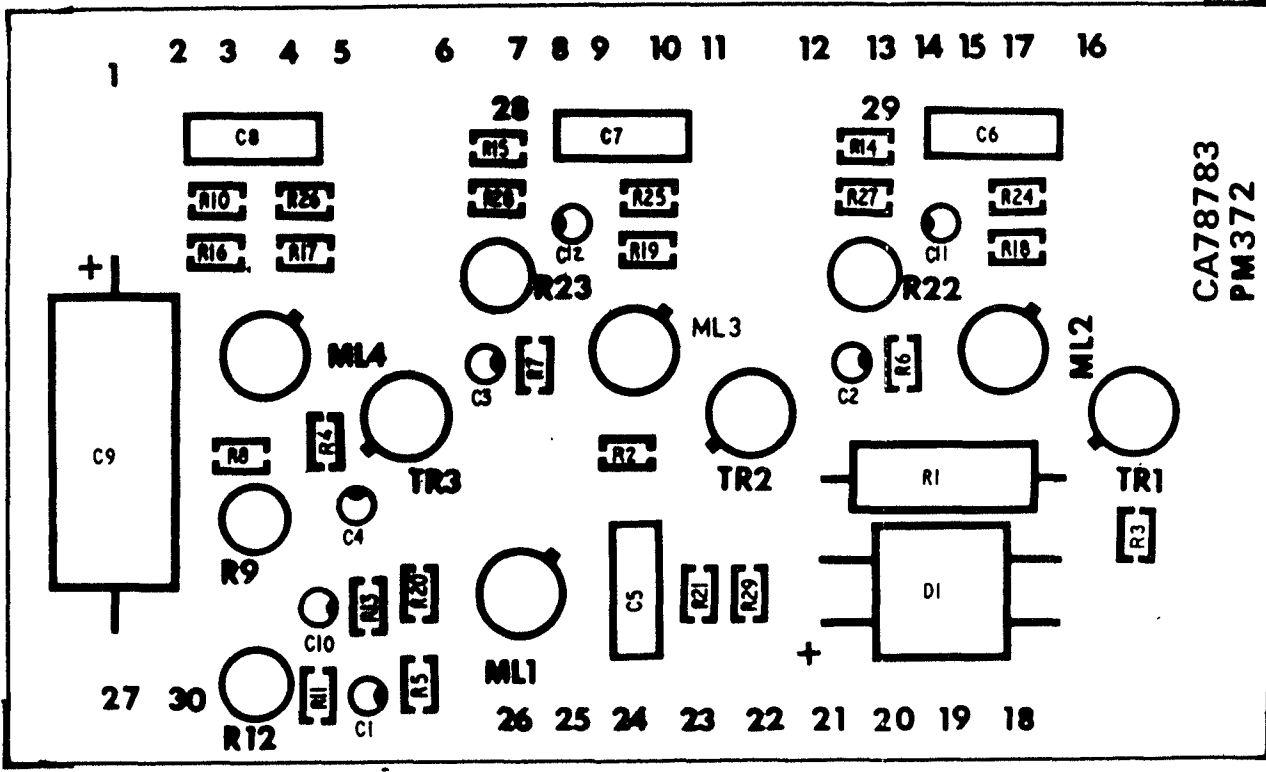
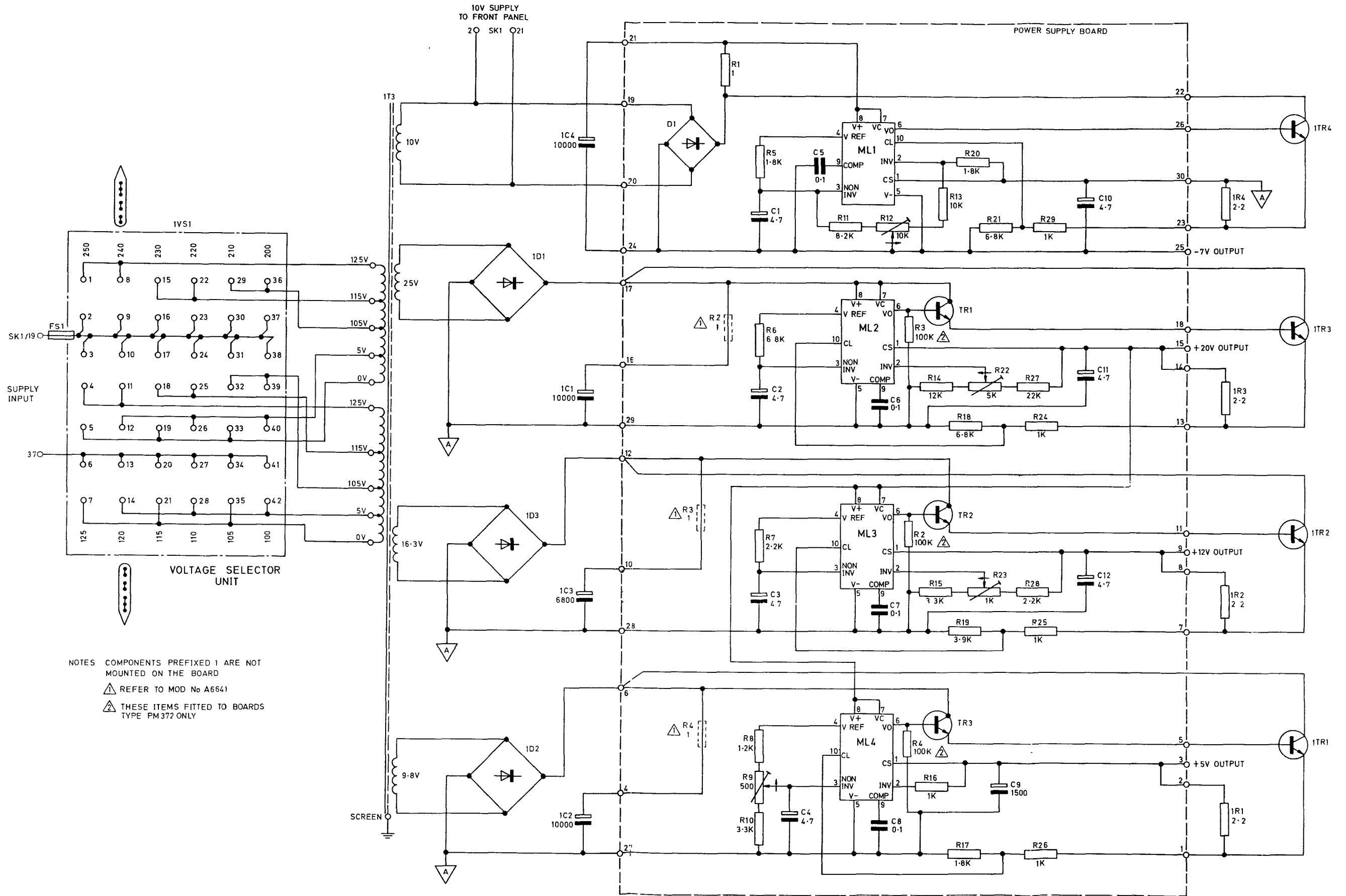


Fig. 4

Control board PM345: circuit

Fig. 4





NOTES COMPONENTS PREFIXED 1 ARE NOT MOUNTED ON THE BOARD  
 ⚠ REFER TO MOD No A6641  
 ⚠ THESE ITEMS FITTED TO BOARDS TYPE PM372 ONLY

Fig.6

Power supply unit: circuit

Fig.6

CHAPTER 1GENERAL DESCRIPTIONCONTENTS

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CHAPTER 1GENERAL DESCRIPTIONINTRODUCTION

1. The MA1720 is a solid state Transmitter Drive Unit providing 289,999 frequency channels in 100 Hz steps over the frequency range 1 to 29.9999 MHz. The output frequency is derived by frequency synthesis from a highly stable crystal-controlled 5 Mhz reference source. Channel frequency is selected by six thumbwheel switches which display the selected frequency in digital form; no other tuning action is necessary. 'Locking-in' to the selected frequency is completed in approximately 10 milliseconds; a front panel indicator illuminates when the MA1720 is 'in lock' i.e. when the tuning sequence is completed.
2. The output level of the unit may be preset by an internal control from 25 mW to 200 mW; the output impedance is 50 ohms.
3. Local, pre-programmed, extended or remote control of the associated transmitter is selected by a front panel switch on the Drive Unit.

LOCAL (SYNTH): The transmitter is controlled by the front panel settings on the MA1720.

LOCAL (PROG): The MA1720 may be operated on pre-selected frequency channels by means of a pre-programmed selector such as the Racal MA1038.

EXTENDED: Control of the MA1720 and the associated transmitter is extended to an external control panel such as the Racal MA1040.

REMOTE: Control of the MA1720 and the associated transmitter is extended to a remote control position over telephone lines or radio links by means of a remote control system such as the Racal MA1722/MA1085/MA1040 or MA1722/ MA1090. These are SCORE systems and additionally require 2 x 26LSI data modems. Control of the MA1720/MA1038 is by the LA1517/LA1518 10-channel sequential tone system.

AUDIO/KEYING INPUTS

4. Two front panel jacks are provided for connection and monitoring of line inputs, connection of a microphone or contact closure keying. LINE 1 jack is used for USB or LSB modes and both jacks are used for ISB operation; contacts are also provided on LINE 1 jack for a Press-to-Talk line, sidetone output, and connection of an output from an associated receiver. Rear panel connectors provide for connection of two 600 ohm balanced line inputs, a high impedance RTTY input, telegraph keying and external frequency standard input. Multi-way connectors enable the extended, remote or pre-programmed control facilities to be connected to the MA1720.



5. The 600 ohm balanced audio inputs may vary between -30 dBm and +10 dBm (relative to 1 mW); two front panel controls enable the input level to be set to the centre of the AGC range. The optional RTTY facility is provided by an internally fitted module; the RTTY keying input may vary between 5-0-5 volts and 80-0-80 volts (by the use of suitable dropping resistors - see Chap. 2 para.17) provided by an external supply. The maximum keying speed is 200 bauds.

#### OPERATIONAL FACILITIES

6. The unit offers a choice of upper or lower single sideband, with suppressed or reduced carrier, independent sideband or radio telegraphy. Radio teleprinter (RTTY) is available as an optional built-in facility. Details of the facilities which are selected by a front panel control switch are as follows:

SSB (Upper or Lower):	-26, -16 db or suppressed
ISB:	-16 or -26 dB carrier
Key:	-6 dB or suppressed carrier
AM:	-6 dB carrier
CW:	LSB mode with 1 kHz keyed tone
RTTY:	Tone Shift Keying
RTTY Test:	Selects Mark
VOX:	Automatic Voice Switching
PTT:	Press-to-Talk
Transmit:	Continuous transmission

NOTE: The -26 dB pilot carrier level may be changed to -20 dB by a simple modification (see Figure 11).

7. VOX (automatic voice switching) is available on Line 1 to enable a two-way conversation to be carried out without manual switching.

8. To increase the flexibility of any system in which the MA1720 Drive Unit may be employed, provision is made for muting an associated receiver and for antenna switching between the associated transmitter and receiver. The receiver output may be monitored at the drive unit and the drive unit sidetone fed to the receiver.

#### FRONT PANEL CONTROLS

9. (1) SUPPLY: Push button switch. Illuminates when supply is ON.
- (2) Frequency Selection: Six thumbwheel switches.

- (3) MODE: An eleven-position rotary switch which selects the facilities described in para. 6.
- (3) CONTROL: A four-position rotary switch for the selection of LOCAL (programmed or synthesizer), EXTENDED or REMOTE control of the MA1720 (see para. 3).
- (5) TUNE/MUTE/OPERATE: A four-position rotary switch:-
- TUNE: Provides a CW tuning signal for the associated transmitter.
- MUTE: Mutes drive to transmitter.
- OPERATE: Low: Low power operation approximately -6 dB below p.e.p. by internal adjustment.
- High: Full p.e.p. adjustment by internal preset control.
- (6) Sideband Selection: A two position switch which selects UPPER or LOWER sideband.
- (7) VOX/PTT/Tx: A three position switch which selects:
- VOX: Automatic Voice Switching
- PTT: Press-to-Talk
- Tx: Continuous transmission
- (8) STANDBY-ON: A push button switch which illuminates when depressed. Provides a local control signal (+12 V when not depressed, 0 V when depressed), via a rear panel socket, for the associated transmitter or linear amplifier.
- (9) EHT-READY: A push button switch. Provides a local control signal (+12 V when not depressed, 0 V when depressed) via a rear panel socket, for the associated transmitter or linear amplifier. The switch may be illuminated by a READY signal from the associated transmitter or linear amplifier.

- (10) RESET: A push button switch and indicator lamp. The lamp illuminates when the drive unit output is muted following a change in the selected frequency. It may also illuminate to indicate a fault condition at the associated transmitter or linear amplifier. The push button is depressed to reset the equipment to the new frequency.
- (11) METER Switch: A nine-position rotary switch used in conjunction with the front panel meter for monitoring audio line input levels, the RF output level and internal supply voltage levels.

#### FRONT PANEL INDICATORS

10. (1) IN LOCK: Illuminates when the drive unit is locked to the selected frequency.
- (2) REDUCED POWER: This lamp may be illuminated by a +12 V 'reduced power' signal from the associated transmitter or linear amplifier.

#### MONITORING

11. The front panel jacks (Line 1 and Line 2) enable the audio line inputs to the drive unit to be monitored using high impedance headphones. Line 1 monitors the Audio 1 input whilst Line 2 monitors the Audio 2 input. The audio input from an associated receiver may also be monitored at LINE 1.
12. The signal input socket SK9, which is mounted on the rear panel, provides monitor facilities for Audio 1 and Audio 2 inputs and the output of an associated receiver. The associated receiver output may also be monitored at terminal strip TS1 at the rear of the unit.
13. An RF monitor socket mounted on the front panel permits connection of test equipment to monitor the RF output of the drive unit.

#### METERING

14. A front panel mounted meter is used in conjunction with the meter switch to indicate the line input levels, line input setting levels, the internal supply voltage levels and the RF output level. A green band on the meter scale indicates the correct setting for audio levels and internal supply voltage levels.

FREQUENCY STANDARD

15. The reference frequency is generated by a 5 MHz Racal fast warm-up oscillator Type 9400 which has a stability better than 1 part in  $10^8$  over the temperature range  $-10^{\circ}\text{C}$  to  $+60^{\circ}\text{C}$ . The Racal Type 9420 5 MHz oscillator, available as an option, has a stability better than 6 parts in  $10^{10}$  over the temperature range  $-10^{\circ}\text{C}$  to  $+60^{\circ}\text{C}$ . A rear panel socket with associated switch provides for the use of an external 5 MHz frequency if required.

MECHANICAL DETAILS

16. The unit is housed in a cast alloy chassis, which is compartmented to provide screening between assemblies liable to mutual interference. The printed circuit boards are mounted on either side of the chassis.

17. Access to assemblies mounted on the upper side of the chassis is gained simply by removing the top panel which is secured by screws to the side and rear panels. Assemblies mounted on the underside of the chassis are protected by individual lids which afford easy access to each assembly; the printed circuit boards mounted on the underside of the chassis may be hinged outwards from the chassis for servicing purposes.

18. The front, side and rear panels are all constructed of steel; the rear panel carries the heat sinks for the power transistors. The front panel is connected to the main cableform via two multi-pin connectors and may be completely detached from the chassis for test purposes.

19. To facilitate cooling, slots in the chassis, the top cover, and compartment lids allow air to flow freely throughout the unit.

PRINCIPLES OF OPERATIONSYNTHESIZER

20. Figure 2 shows that the synthesizer produces the following three outputs:

- (1) 35.4 to 65.4 MHz as the final mixer injection frequency.
- (2) 34 MHz for injection into the first mixer.
- (3) 1.4 MHz for injection into the balanced modulator and for carrier re-insertion.

21. The indirect method of frequency synthesis is used where the required output frequencies (with the exception of the 1.4 MHz output) are derived from voltage-controlled oscillators which are phase-locked to an input frequency derived from the 5 MHz standard frequency source. Algebraic equations, for calculating each local oscillator frequency are given in paras. 34 to 39.

### 34 MHz Generator

22. The 5 MHz signal is divided by five, on the 34 MHz generator board, and the 1 MHz output fed to the LF loop board. This 1 MHz signal is also applied to a phase-locked loop containing a 34 MHz VCO, the output from which is fed via a band-pass filter to the first mixer on the mixer and output board (Fig. 15).

### LF Loop

23. This generates the kHz part of the synthesizer output frequency. The low-frequency loop consists of a 23 to 18 MHz VCO, a programmed divider, N1, and a phase-comparator. The phase-comparator compares the phase of the output signal from the programmed divider with that of a 500 Hz reference frequency derived from the frequency standard. Should a phase difference exist, a correction voltage is derived which is fed back to the VCO to eliminate the error.

24. The programmed divider, N1, has a variable division ratio in the range 46000 to 36001, and is controlled by the 100 Hz, 1 kHz, 10 kHz and 100 kHz frequency selector switches. A frequency setting of 9999 sets the division ratio to 36001; a setting of 0000 sets the division ratio to 46000; the division ratio for intermediate frequency settings is given by the expression  $N1 = 46000$  minus the settings of the above four frequency selector switches.

25. The programmed divider N1 is a reversible decade counter programmed to commence a counting sequence at a point dependent on the setting of the four selector switches. When the VCO has been driven to its correct operating frequency, (reset strobe) pulses occur at a rate of 500 p.p.s.

26. Consider a frequency setting of 12.3456 MHz (the required final mixer injection frequency is 12.3456 MHz plus 35.4 MHz i.e. 47.7456 MHz). Ignoring the MHz part of the frequency setting, the divider N1 is preset to start counting at 3456 and count up to 46000, a total of 42544 pulses (46000 minus 3456). The LF loop VCO frequency is now found by multiplying 42544 by the 500 Hz reference frequency, to produce 21.272 MHz.

27. The 21.272 MHz main output from the VCO is fed via a divide-by-five stage to the transfer loop. Note that the output frequency from the LF loop is in the range 4.6 to 3.6 MHz and hence the actual output is 4.2544 MHz.

28. The 1 MHz input to the LF loop is divided by five to produce 200 kHz; a 1.4 MHz crystal filter selects the seventh harmonic and this is amplified to produce a 1.4 MHz injection signal for the balanced modulators.

### Transfer Loop

29. This loop, in conjunction with the HF loop, generates the MHz portion of the output frequency. It consists of a programmed divider, N2, a phase comparator, a mixer and a VCO (HF loop board) which covers the frequency range 885 to 947.8 kHz.

30. The programmed divider, N2, has a division ratio of from 40 to 69. In contrast to the previously described programmed divider N1, the division ratio of N2 is found by adding 40 to the setting of the MHz switch. This is achieved by first converting the decimal 0 to 29 into a 'nines complement' code before application to the programmed divider which counts from the programmed starting point up to 99, and then to 39 when the reset occurs. Table 1 gives the conversion from decimal to nines complement code.

TABLE 1

Decimal to Nines - Complement BCD Conversion

Decimal	BCD				Nines Complement				Decimal
	D	C	B	A	D9	C9	B9	A9	
0	0	0	0	0	1	0	0	1	9
1	0	0	0	1	1	0	0	0	8
2	0	0	1	0	0	1	1	1	7
3	0	0	1	1	0	1	1	0	6
4	0	1	0	0	0	1	0	1	5
5	0	1	0	1	0	1	0	0	4
6	0	1	1	0	0	0	1	1	3
7	0	1	1	1	0	0	1	0	2
8	1	0	0	0	0	0	0	1	1
9	1	0	0	1	0	0	0	0	0

31. The output from the LF loop is divided by N2 and is then applied as one input to a phase-comparator. The output from the VCO is mixed with the 1 MHz reference frequency, derived from the frequency standard, and the difference frequency from the mixer is applied as the second input to the phase-comparator. Thus the output voltage from the phase-comparator drives the VCO to a frequency which is equal to 1 MHz minus the output frequency from the programmed divider, N2.

32. The division ratio for the programmed divider, N2, is obtained by adding 40 to the MHz digits of the output frequency. Thus for a frequency of 12.3456 MHz, N2 will be 40 plus 12 which equals 52. The 4.2544 MHz output from the LF loop (para. 26) is divided by 52 and the result is then subtracted from 1 MHz to give us the transfer loop output frequency.

$$\begin{aligned} \text{Transfer loop output} &= 1 - \frac{4.2544}{52} \text{ MHz} \\ &= 1 - 0.081815 \text{ MHz} \\ &= 918.185 \text{ kHz} \end{aligned}$$

HF Loop

33. As stated in para. 29, the VCO for the transfer loop is on the HF loop board. The output from this VCO is fed via a divide-by-two stage to the HF loop which contains a programmed divider N2 with the same range of division ratios as for the transfer loop. The output from this loop, which also contains a further divide-by-two stage, is 2N2 times the input frequency to the phase comparator. Hence, the output from the VCO is:

$$918.185/2 \times 2 \times N2 = 47.7456 \text{ MHz (para. 26)}$$

Loop Equations

34. The variable output frequency from the synthesizer may be worked out for any frequency setting by using a simple algebraic equation. The following paragraphs show the derivation of this equation, and should be read in conjunction with Fig. 2.

35. The 1 MHz reference frequency input to the low-frequency loop, designated f1, is expressed as: f1 = 10<sup>6</sup> Hz. The output from the LF loop (f2) is therefore:

$$f2 = \frac{10^6}{5 \times 400} \times N1 \times \frac{1}{5} \text{ Hz} \dots\dots\dots (1)$$

$$= 10^2 \times N1 \text{ Hz} \dots\dots\dots (2)$$

36. The transfer loop divides its input (equation 2) by N2 and then subtracts the result from 1 MHz. The output frequency (f3) is therefore:

$$f3 = 10^6 - \frac{10^2 \times N1}{N2} \dots\dots\dots (3)$$

37. The input to the HF loop (equation (3)) is divided by a factor of two and applied to the phase-comparator as:

$$\frac{f3}{2} = \frac{10^6}{2} - \frac{100 \times N1}{2 \times N2} \dots\dots\dots (4)$$

The final output frequency (f4) from the HF loop is found by multiplying equation (4) by 2 X N2:

$$\begin{aligned} f4 &= \frac{10^6 \times 2N2}{2} - \frac{2N2 \times 100N1}{2N2} \\ &= 10^6 N2 - 100N1 \dots\dots\dots (5) \end{aligned}$$

38. For a frequency setting of 12.3456 MHz, the division ratio for N1 was found to be 42544 (para. 26) and that for N2 was found to be 52 (para. 32). Substituting the values of N1 and N2 into equation (5), the final output frequency  $f_4$  is therefore:

$$\begin{aligned} f_4 &= 10^6 \times 52 - 100 \times 42544 \\ &= 47.7456 \text{ MHz.} \end{aligned}$$

### SSB OPERATION (Fig. 1)

39. The channel 1 and 2 modulating input signals are applied to a pair of automatic gain controlled amplifiers and thence to balanced modulators via MODE switch controlled reed relays. For SSB operation, the channel 1 input is used to generate the upper sideband via balanced modulator 1 or the lower sideband via balanced modulator 2. The channel 2 input is used to generate the lower sideband (via balanced modulator 2) in the ISB mode.

40. The 1.4 MHz signal from the frequency synthesizer is first amplified and is then applied to both balanced modulators where mixing occurs with the outputs from the gain controlled input amplifiers. The required sidebands are obtained by filtering; the output from balanced modulator 1 is applied to an LSB filter, and the output from balanced modulator 2 is applied to a USB filter, to compensate for sideband inversion which occurs in the final mixer.

41. The 1.4 MHz signal from the synthesizer is also applied to a carrier insertion stage where it is attenuated by 6, 16 or 26 dB (suppressed carrier greater than -40 dB), dependent upon the mode of emission selected; the audio signal from the gain controlled amplifier is also attenuated to ensure a constant p.e.p. output. A summing amplifier adds the SSB or ISB signals to the carrier and the resultant signal is mixed with the 34 MHz output from the synthesizer to produce an IF of 35.4 MHz.

42. The 35.4 MHz IF is fed, via a bandpass filter which attenuates the unwanted image signal, to a wideband amplifier. The output of the wideband amplifier is applied to a crystal filter which has a pass-band of  $\pm 6$  kHz centred on 35.4 MHz; the filter reduces noise to the final mixer to obtain optimum wideband noise performance.

43. In the final mixer, the 35.4 MHz IF is mixed with the 36.4 MHz to 65.4 MHz output from the synthesizer. The resultant output is applied to a low pass filter which suppresses the image signal and oscillator breakthrough, to produce the output frequency in the range 1 MHz to 30 MHz. The output of the low pass filter is applied via a buffer amplifier, which incorporates a manual gain control, to a five-stage wideband amplifier.

### SUPPRESSED CARRIER OPERATION

44. Suppressed carrier operation is similar to single sideband operation except that the 1.4 MHz carrier is not re-inserted after the sidebands have been generated.



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CHAPTER 2INSTALLATIONINTRODUCTION

1. Installation of the Drive Unit consists of making electrical connections to sockets on the front and rear panels as detailed in the following paragraphs.

FRONT PANEL CONNECTORS

2. Two front panel jack sockets provide the following:

<u>FUNCTION</u>	<u>CONNECTOR</u>
AF injection SSB (USB and LSB)	Line 1 jack
AF injection ISB (USB)	Line 1 jack
AF injection ISB (LSB)	Line 2 jack
Press-to-talk	Line 1 jack
Contact closure keying	Line 1 or Line 2 jack
Monitor AF input SSB, (USB or LSB)	Line 1 jack
Monitor AF input ISB (USB only)	Line 1 jack
Monitor AF input ISB (LSB only)	Line 2 jack
Monitor keying inputs	Line 1 jack
Monitor RTTY inputs	Line 1 jack
Monitor receiver output	Line 1 jack

Details of connections to Line 1 and Line 2 jacks are as follows:

<u>Jack Contact No.</u>	<u>Function</u>
1	Associated receiver output (Line 1 jack only)
2	See Note (3) (Line 1 jack only).
3	See Note (2).
4	Connect to pin 8 if microphone bias required.
5	Monitor audio, keying or RTTY sidetones.
6)	Press-to-talk (line 1 Jack only) normally
7)	open contacts between pin 6 and pin 7.
8	Wire to pin 4 if microphone bias required.

<u>Jack Contact No.</u>	<u>Function</u>
9	Not used.
10	Not used.
11	One of key contacts (other to earth)
12	Local audio injection
13	Common 0 V

- Notes: (1) To connect a jack plug to a jack socket, the plug is pushed in and turned fully clockwise. The socket is slotted to accept the plug in one position only. To remove the plug, reverse the above procedure.
- (2) To monitor the AF input with a headset plugged into a jack socket whilst applying the AF input to TS1 at the rear of the unit (refer to para. 11) connect pin 3 to pin 12 in the jack plug.
- (3) To monitor the key input with a headset plugged into a jack socket whilst applying key input to TS1 at the rear of the unit (refer to para.11), connect pin 2 to pin 11 in the jack plug.

### REAR PANEL CONNECTORS

3. The following connectors are provided on the rear panel:

- PL2: Supply input - connect local a.c. supply to unit.
- PL3: Extended frequency control lines - enable frequency to be selected from an extended position; also provides power and indicator connections to a Pre-programmed Selector.
- SK2: Extended/remote control lines - enable the MA1720 to be controlled from an extended or remote position.
- SK3: External frequency standard input - enables the frequency synthesizer to be referenced to a 5 MHz external frequency source.
- SK4: Output - connects the RF output of the MA1720 to the associated transmitter.
- SK6: Status/control lines to transmitter - enable the MA1720 to control a distant linear amplifier.
- SK9: Signal inputs - connects modulating inputs to the drive unit.
- TS1: Signal inputs - connects modulating inputs to the drive unit.

PL2 - Supply Input

4. Mains power supplies are connected to PL2 as follows:

Line: Pin A  
 Neutral: Pin B  
 Earth: Pin C

Note: The associated voltage tapping panel should be adjusted to suit the local mains voltage.

PL3 - Extended Frequency Control, Power, and Indicator Connections

5. The frequency of the Drive Unit may be controlled externally by applying +12 V to the extended frequency control lines according to the following code (see para. 6).

Notes: (1) +12 V is available at PL3 pin 37.

(2) The external frequency control lines may also be used as outputs, where the frequency is selected on the MA1720 frequency switches and an external indication is required. In this case, the output is the same code and voltage levels as the input.

Coding

6. (a) The 100 Hz, 1 kHz, 10 kHz, and 100 kHz inputs are in inverted 1-2-4-8 BCD, e.g.

600 Hz = 0110 (x 100 Hz decade), which when inverted becomes 1001, where 1 = +12 V, and 0 = open circuit.

(b) The 1 MHz makes use of an inverted nines complement code, e.g.

6 MHz nines complement = 3 MHz.

3 MHz = 0011 (x 1 MHz decade) which when inverted becomes 1100, where 1 = + 12 V, and 0 = open circuit.

(c) The 10 MHz input requires three sets of data only to cover the 0, 1 and 2 10 MHz decades. An inverted nines complement code is used, as for the 1 MHz decade, except that only two lines are required. From the table below it can be seen that a unique code may still be obtained by ignoring the inverted nines complement 2 and 4 levels.

10 MHz Decade	BCD				Inverted Nines Complement			
	8	4	2	1	8	4	2	1
0	0	0	0	0	0	1	1	0
1	0	0	0	1	0	1	1	1
2	0	0	1	0	1	0	0	0

Thus 0 (x 10 MHz decade) is given by 0--0, 1 (x 10 MHz decade) is given by 0--1, and 2 (x 10 MHz decade) is given by 1--0, where 1 = +12 V, and 0 = open circuit.

- (d) Using the above examples, the Table below shows how inputs or outputs would be for a frequency of 06.000600 MHz.

#### EXTENDED FREQUENCY CONTROL LINES

Pin	Function	Remarks	Para. 6 Example
9	1)	)	1
10	2)	)	0
11	4) x100 Hz	)	0
12	8)	)	1
		)	
5	1)	)	1
6	2)	)	1
7	4) x1 kHz	)	1
8	8)	) Inverted BCD	1
		)	
1	1)	)	1
2	2) x10 kHz	)	1
3	4)	)	1
4	8)	)	1
		)	
21	1)	)	1
22	2)	)	1
23	4) x100 kHz	)	1
24	8)	)	1
		)	
17	1)	)	0
18	2)	)	0
19	4) x1 MHz	)	1
20	8)	) Inverted Nines Complement	1
		)	
13	1)	)	0
	)	)	
	) x10 MHz	)	
16	8)	)	0

## POWER AND INDICATOR CONNECTIONS

	Pin
Pre-programming (+12 V indicates MA1720 is set to Pre-programmed control)	36
0 V	34
12 V (300 mA max.) Supply to pre-programmed Selector	37

SK2 - Extended/Remote Control Lines

7. Input and output connections for extended and remote control are made to SK2. Input connections are applied at +12 V to select a mode of operation (open circuit = OFF) and output connections at +12 V illuminate indicating lamps on the extended or remote control panel. Pin connections and functions are given below:

## EXTENDED/REMOTE CONTROL LINES

Pin	Function	Pin	Function
1	Blank	20	RTTY Test
2	Blank	21	RTTY
3	ISB Control	22	LSB control
4	Blank	23	Low power control
5	High Power control	24	-26 dB control
6	-16 dB control	25	-6 dB control
7	Key supp. control	26	Key -6 dB control
8	VOX control	27	Blank
9	Extended Tx lamp	28	Extended 'EHT ON'
10	Extended 'Reset'	29	Extended 'Standby ON'
11	Extended 'Tune'	30	Extended 'Reset' lamp
12	Ext. 'Reduced' power lamp	31	Extended 'Ready' lamp
13	Extended 'In lock' lamp	32	Extended Mute
14	Remote ON	33	Extended ON
15	Extended Mode Control	34	Extended 'PTT'
16	-7 V	35	0 V
17	+ 5V	36	+ 12V
18	+ 20 V	37	Remote 'PTT'
19	Local 'PTT'		

SK3 - External Frequency Standard Input

8. An external 5 MHz frequency standard with a minimum output level of 300 mV r.m.s. may be connected to SK3. The adjacent slider switch selects either internal or external standard as the reference frequency for the synthesizer.

SK4 - Output

9. SK4 is the output socket for the 1 MHz to 30 MHz modulated output of the drive unit.

SK6 - Status/Control Lines to Amplifier

10. SK6 carries the status signal and control interconnections between the drive unit and the associated amplifier. Pin connections and functions are given below.

STATUS/CONTROL LINES			
Pin	Function	Voltage	Action
1	Mains On	+ 12 V = ON 0 V = OFF	Signal present when MA1720 is switched on.
2	Fault	0 V = Fault + 12 V = Normal	Lights the 'Reset' lamp and mutes the MA1720 under fault conditions.
3	Ready	0 V = Ready + 12 V = Not Ready	Lights the 'Ready' lamp, the absence of 'Ready' signal reverts the output of the MA1720 to the 'tune' signal.
4	Reset (CTI)	0 V = Normal + 12 V = Reset	When the 'Reset' button is depressed the MA1720 is demuted and a Coarse Tune Initiate (CTI) signal is applied to the linear amplifier.
5	Reduce Power	0 V = Lamp OFF + 12 V = Lamp ON	Lights 'Reduced Power' lamp when the linear amplifier is operating on reduced power.
6	EHT ON	+ 12 V = OFF 0 V = ON	Switches on linear amplifier EHT supplies.
7	Standby	+ 12 V = OFF 0 V = ON	Sets the linear amplifier to Standby.
8	Mute	+ 12 V = Normal 0 V = Mute	Mutes linear amplifier.

Pin	Function	Voltage	Action
9		0 V	Earth
10	Not used.		
11	CTI (Reset)	0 V = Normal + 12 V = Reset	Set linear amplifier to the coarse tune Initiate condition.

### SK9/TS1 - Signal Inputs

11. Signal inputs to the drive unit may be connected to SK9 or TS1 which are connected in parallel. Connections and functions are given below.

#### Signal Input Socket SK9

Pin	Function	Pin	Function
1)	Audio 1 input	25	Screen for RTTY input
2)		15	Blank
14	Audio 1 Screen		
3)	Audio 2 input	19	Audio 1 monitor (Sidetone)
4)		20	Audio 1 monitor Screen
16	Audio 2 Screen	21	Audio 2 monitor (Sidetone)
		22	Audio 2 monitor Screen
5	KEY input	23	0 V
17	Key input Screen	24	+ 12 V
6	Audio from Receiver		
18	Receiver audio Screen		
7	Normally Closed) (Tx Condition) )		
8	Relay contacts ) (Change Over) )	See Note	
9	Normally Open )	below	
10	Normally Closed)		
11	Relay contacts ) (Change Over) )		
12	Normally Open )		
13	RTTY input )		



## Signal Input Terminal Strip TS1

Pin	Function	Pin	Function
1)	Audio 1 input	10	Normally Closed ) See
2)		11	Relay contacts ) Note
3	Audio 1 Screen	12	Normally Open ) below
		13	Key input
4)	Audio 2 input	14	Key input Screen
5)		15	Audio input from Receiver
6	Audio 2 Screen	16	Receiver audio Screen
7	Normally closed	17	RTTY input
8	Relay Contacts ) See	18	RTTY Screen
	(Change over) ) Note	19	0 V
9	Normally open ) below	20	+ 12 V

Note: Pins 7 to 12 of SK9 and TS1 are connected to a changeover relay in the MA1720 which is provided for external use only. This relay operates when the output of the MA1720 is muted (max Relay ratings: 100 V, current 1 ampere, maximum power 30 Watts).

Local Operation

12. The CW output (pin 2 on the RTTY board - PS568) should not be linked to the associated pin (pin 2) on the mounting plate. This link is made for remote operation only.

Remote Operation

13. Both RTTY and CW inputs are fed to pins 13 and 25 of SK9 or pins 17 and 18 of TS1 (RTTY input). When the RTTY board is not fitted, pins 2 and 3 on the RTTY board mounting plate must be linked.

Front Panel to Main Chassis Connections

14. So that the front panel may be detached from the main chassis, the wiring from the front panel switches, connectors, and indicators are terminated in a 37-way socket (SK1) and a 37-way plug (PL1), mounted on the rear of the front panel. These connectors mate with PL1 and SK1 respectively, on the main chassis cableform (refer to Figs. 23 and 28).



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CHAPTER 3

SETTING-UP AND OPERATION

INTRODUCTION

1. The MA1720 Drive Unit and associated transmitter may be controlled by any one of the following methods:
  - (a) Local Control - The Drive Unit and associated linear amplifier are controlled by the setting of the front panel switches.
  - (b) Extended Control - The Drive Unit and associated linear amplifier are controlled by switches on an external panel (e.g. Racal MA1040).
  - (c) Remote Control - Full operational control of the Drive Unit and associated linear amplifier is extended to a remote control terminal via telephone lines or radio links by means of a remote control system such as the Racal CSA1505 or LA7922/7923 and the MA1040 Remote Control Panel.
  - (d) Pre-programmed Control - The frequency of the Drive Unit is controlled by a Pre-Programmed Selector such as the Racal MA1038 which may be set to provide a number of frequency channels.
2. Detailed operating instructions are given in paras. 40 to 51.

INITIAL SETTING-UP

3. The setting-up procedures detailed in the following paragraphs need only be carried out immediately following installation or maintenance.
4. Check that the voltage selector on the rear panel is set correctly for the local mains voltage and that the slider switch on the rear panel is set correctly for internal or external frequency standard.
5. If RTTY operation is required, connect the linking on the RTTY Generator Board PS568 as follows:-

POLAR	NEUTRAL	REVERSE KEYING	NORMAL KEYING
Pin 12 to Pin 13 Pin 14 to Pin 16	Pin 12 to Pin 13 AND EITHER: Pin 14 to Pin 15 for positive keying OR Pin 14 to Pin 17 for negative keying	A-C	A-B

6. Set the front panel switches as follows:

SUPPLY switch to OFF  
 STANDBY switch to OFF  
 EHT switch to OFF  
 TUNE/MUTE/OPERATE switch to OPERATE HIGH  
 MODE SELECTOR switch to RTTY TEST  
 CONTROL SELECTOR switch to LOCAL

7. Operate the SUPPLY push button and check that the following lamps illuminate:

SUPPLY ON  
 RESET  
 IN LOCK

8. Set the meter switch in turn to -7V, +5V, +12V and +20V. Check that on each setting the meter reads in the centre of the green band on the meter scale; if not refer to Chapter 5, para.2.

### INITIAL CHECKS

9. Before installation, functional and mode checks of the MA1720 may be carried out using a multimeter and the front panel mounted meter. To simulate transmitter conditions, various inputs must be applied to socket SK6 on the rear panel of the unit; details are given in paras. 10 to 29.

### Functional Checks Using Multimeter

10. Ensure the RF output of the MA1720 (SK4 on the rear panel) is connected to a 50 ohm load.

11. At socket SK6 on the rear panel connect pin 9 to pin 3; this simulates the READY condition in the absence of a linear amplifier.

12. Select an operating frequency on the thumbwheel switches and press the RESET button. When the RESET lamp extinguishes the Drive Unit is demuted, and when the IN LOCK lamp illuminates the Drive Unit is locked to the selected frequency. Set the meter switch to RF and ensure there is a reading of approximately 200 mW on the meter.

13. Connect the multimeter (set to measure d.c. volts) between pin 7 of socket SK6 on the rear panel and earth (+ve lead to pin 7). Check that the multimeter measures +12V d.c. Press the STANDBY push button and check that the multimeter reads 0 V.

14. Connect the multimeter between pin 6 of socket SK6 and earth (+ve lead to pin 6). Check that the multimeter measures +12 V d.c. Press the EHT push button and check that the multimeter reads 0 V.

15. Apply +12 V d.c. to pin 5 of socket SK6 to simulate a linear amplifier operating on reduced power and check that the REDUCED POWER lamp illuminates.

NOTE: +12 V d.c. is available at pin 36 of socket SK2.

16. Remove the +12 V d.c. from pin 5 of socket 6 and connect the multimeter between pin 8 of socket SK6 and earth (+ve lead to pin 8). Check that the multimeter reads +12 V d.c. Set the TUNE/MUTE/OPERATE switch to MUTE and check that the multimeter reads 0 V. Reset the TUNE/MUTE/OPERATE switch to OPERATE HIGH.
17. Connect the multimeter between pin 4 of socket SK6 and earth (+ve lead to pin 4) and press the RESET push button. Check that the RESET lamp extinguishes and that the multimeter reads +12 V d.c.
18. Apply 0 V (earth) to pin 2 of SK6 to simulate a transmitter fault, and check that the RESET lamp illuminates.
19. Press the RESET push button and check that the Drive Unit de-mutes for 2 seconds before the RESET lamp illuminates again.
20. Remove the 0 V (earth) connection from pin 2 of socket SK6 and check that the Drive Unit is de-muted and the RESET lamp is extinguished.

#### Mode Checks

21. Set the MODE SELECTOR switch to AM-6, the VOX/PTT/Tx switch to Tx, and the TUNE/MUTE/OPERATE switch to OPERATE LOW, and check that the RF output of the Drive Unit decreases by 6 dB.
22. Set the MODE SELECTOR switch to SSB SUPPRESSED, connect a suitable microphone to LINE 1 jack and check that speech input to the microphone modulates the RF output of the Drive Unit.
23. Set the TUNE/MUTE/OPERATE switch to MUTE, and the MODE SELECTOR switch to AM-6. Check that the Drive Unit is muted when speech is applied to the microphone.
24. Set the TUNE/MUTE/OPERATE switch to OPERATE HIGH, and the VOX/PTT/Tx switch to VOX. Check that when speech input to the microphone is stopped for more than 2 seconds the Drive Unit is muted.
25. Switch the VOX/PTT/Tx switch to PTT and check that the Drive Unit is muted when the pressel switch on the microphone is not operated.
26. Remove the microphone from LINE 1 jack and set the MODE SELECTOR switch in turn to ISB-16, ISB-26, SSB SUPPRESSED, SSB-26, SSB-16, and AM-6. Check that the RF output of the Drive Unit varies in accordance with each mode selected.
27. Set the MODE SELECTOR switch in turn to CW, KEY SUPPRESSED, and KEY-6. Check that the RF output level varies in accordance with each mode selected.
28. Connect a suitable test key to LINE 1 jack and set the MODE SELECTOR switch in turn to CW, KEY SUPPRESSED and KEY-6. Check that in the 'key down' condition at each switch position the RF output of the drive unit is approximately 200 mW.
29. Remove the connection between pin 3 and pin 9 of socket SK6.

Functional Checks: MA1720 Connected to a Linear Amplifier

30. The following checks are given as a general guide only and should be carried out with the MA1720 connected to a suitable linear amplifier (e.g. Racal TA1800). Detailed checks for systems using various Racal linear amplifiers may be found in the addendum 2 of this appendix. Refer to the relevant linear amplifier or system manual for the tuning procedures and the required level of drive input required.
31. Select an operating frequency on the thumbwheel switches and press the RESET button. When the RESET lamp extinguishes the drive unit is de-muted (not muted) and when the IN LOCK lamp illuminates, the drive unit is locked to the selected frequency. Set the meter switch to RF and ensure that the level is suitable for the associated linear amplifier e.g. 100 mW with the TA1800.
32. If applicable, press the STANDBY-ON push button to switch the associated linear amplifier to the standby condition. Check that the STANDBY-ON lamp illuminates.
33. If applicable, press the EHT push button to switch on the EHT at the associated linear amplifier. If the READY signal line is connected between the MA1720 and the linear amplifier, check that the READY lamp illuminates on completion of tuning.
34. If possible, check that when the linear amplifier is operating on reduced power, the REDUCED POWER lamp on the MA1720 illuminates.
35. Restore the linear amplifier to normal operation, set the TUNE/MUTE/OPERATE switch to MUTE and check that the MA1720 and linear amplifier are muted. Reset the TUNE/MUTE/OPERATE switch to OPERATE HIGH.
36. Press the RESET push button and check that the RESET lamp extinguishes and that the linear amplifier is de-muted.
37. If possible, simulate a fault condition on the linear amplifier (e.g. break the interlock line or trip a circuit breaker) and check that the RESET lamp illuminates and that the drive unit output is muted.
38. Whilst maintaining the simulated condition, press the RESET push button and check that the drive unit de-mutes for approximately two seconds before the RESET lamp illuminates again.
39. Remove the simulated fault condition and press the RESET button. Check that the drive unit is de-muted and that the RESET lamp is extinguished.

OPERATING PROCEDURES

40. The operating procedures detailed in the following paragraphs assume that the MA1720 has been correctly connected to a suitable linear amplifier and has been set up in accordance with the preceding paragraphs.

Local Control

41. (a) Press the SUPPLY push button and check that the SUPPLY lamp illuminates.
- (b) Set the CONTROL switch to SYNTH.
- (c) Set the TUNE/MUTE/OPERATE switch to OPERATE HIGH or LOW as required.
- (d) Set the MODE switch to mode of emission required.
- (e) Set the sideband switch to UPPER or LOWER as required.
- (f) Set the VOX/PTT/Tx switch as required.
- (g) Select the required frequency on the frequency selection thumbwheel switches and check that the IN LOCK lamp illuminates (add 1 kHz to desired frequency for the CW mode).
- (h) Where applicable (see relevant system manual), press the STANDBY-ON push button (STANDBY-ON lamp should illuminate) and then press the EHT push button. The READY lamp may illuminate when the linear amplifier has completed tuning.
- (i) Press the RESET push button. When the RESET lamp extinguishes the MA1720 and associated transmitter or linear amplifier are ready for operation.
42. After a frequency change, note the state of the RESET lamp and press the RESET button if the lamp is illuminated.
43. Monitoring may be carried out as detailed in paras. 52 to 54.
44. If SSB mode is selected, the audio input levels must be set as follows:-
- (a) With AGC: Set the meter switch to SET1 and adjust the SET LINE 1 potentiometer to obtain a meter reading of 0 dB (with a continuous tone audio input).
- (b) Without AGC: As for para. 44 (a) but with a meter reading of -10 dB.
45. If ISB mode is selected, repeat para. 44 for LINE 2.

Extended Control

46. Control of the MA1720 and associated linear amplifier is extended to an external control panel, such as the Racal MA1040, the operation of which is similar to Local Control operation described in paras. 41 and 42. On the MA1720, the SUPPLY must be switched ON and the CONTROL switch set to EXT.
47. Local monitoring may be carried out as detailed in paras. 52 to 54.



Remote Control

48. Control of the MA1720 and associated linear amplifier is extended to a remote control panel, such as the Racal MA1040, via telephone lines or a radio link by means of a remote control system. The MA1720 SUPPLY must be switched ON and the CONTROL switch set to REMOTE.

49. Local monitoring may be carried out as detailed in paras. 52 to 54.

Pre-Programmed Control

50. Control of frequency selection only is extended to a Pre-Programmed Selector in which the frequency channels are pre-set on thumbwheel switches. All other front panel controls on the MA1720 must be operated as for Local Operation described in paras. 41 and 42 and the CONTROL switch must be set to PROG.

51. Monitoring may be carried out as detailed in paras. 52 to 54.

MONITORING

52. The inputs to the MA1720 may be monitored using high impedance headphones as detailed below:

<u>Facility</u>	<u>Connector</u>
Monitor AF input SSB (USB or LSB)	Line 1 jack
Monitor AF input ISB (USB only)	Line 1 jack
Monitor AF input (LSB only)	Line 2 jack
Monitor keying inputs	Line 1 jack
Monitor RTTY inputs	Line 1 jack
Monitor associated receiver output	Line 1 jack

53. The audio inputs to the Drive Unit may also be monitored at socket SK9 which is mounted on the rear panel. Details are as follows:-

<u>Facility</u>	<u>SK9 Pin No.</u>
Audio 1 monitor	19
Screen for audio 1 monitor	20
Audio 2 monitor	21
Screen for audio 2 monitor	2

54. A front panel mounted meter and an associated meter switch provide the following:-

<u>Meter Switch</u>	<u>Meter Indication</u>
LINE 1	Line 1 input level
LINE 2	Line 2 input level
SET 1	Line 1 input level (may be adjusted by front panel mounted potentiometer located above LINE 1 jack)
SET 2	Line 2 input level (may be adjusted by front panel mounted potentiometer located above Line 2 jack)
RF	RF output level
-7V	) Internal supply voltages. Correct
+5V	) level is indicated by meter
+12V	) reading in centre of the green
+20V	) band on the meter scale.

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CHAPTER 4CIRCUIT DESCRIPTION34 MHz GENERATOR BOARD PM344

1. This board (Fig. 3) provides the 34 MHz first mixer injection frequency, together with a 1 MHz reference frequency which is applied to the LF and transfer loop boards, PM349 and PS338. Also contained on this board are logic circuits that receive frequency range information from the frequency selector switches (via the noise immunity board) to select one of three oscillators on the HF loop board PS337. A block diagram of the board is given in Fig.4.1.

34 MHz Oscillator

2. TR2, TR4 and associated components form a voltage controlled 34 MHz LC oscillator. L1, C1 and C3 form the basic tuned circuit. Frequency control is provided by varactor diode D2; the control voltage for D2, applied via RF choke L2, is derived from the phase comparator and voltage control circuits described in paras. 9 to 14.

3. The output of the oscillator is buffered by NAND gates G1-G3 of ML1. The squarewave output from G3 is fed to the low-pass filter, L4 and L5, and the resultant 34 MHz sinewave output is taken to board pin 1.

4. The supply voltage for the 34 MHz VCO and also for ML1 is provided by the series regulator transistor TR1 and a 5.6 V Zener diode D1.

Divide-by-34 Stage

5. A second output from the 34 MHz oscillator is buffered by NAND gate G2 of ML1 before being applied to a divide-by-34 stage; this consists of a divide-by-two (ML5 CK1-A output) and a divide-by-17 stage (ML3, ML5 CK2-C output, G4 and G6).

6. The 17 MHz output from ML5 pin 5 is applied to the clock inputs of both halves of ML3 whilst the J1 input (ML3 pin 14) is held at logic '1' (+5 V). The division factor of 17 is obtained by dividing the first 9 input clock pulses by three and the next 8 clock pulses by four. Thus for the first 9 clock pulses, 3 output pulses are produced ( $9 \div 3 = 3$ ) and for the next 8 clock pulses, 2 output pulses are produced ( $8 \div 4 = 2$ ), making a total of 5 output pulses for 17 input pulses. These 5 pulses are then divided by ML5 to produce a 3:2 mark-to-space ratio 1 MHz squarewave output at ML5 pin 2.

7. Figure 4.2 illustrates the action of the circuit and shows the logic signals produced at relevant points.

### 1 MHz Divider

8. The output from the 5 MHz frequency standard, at board pin 8, is applied to a buffer amplifier, TR3, and then to a shaper stage, TR5. The squarewave output from TR5 is applied to a divide-by-five stage, ML2, and the resultant 1 MHz output is applied to ML4; this consists of three NAND gates, G5, G7, G8, which are used as buffers. The output from G5, at ML4 pin 3, is taken to the transfer loop board PS338 via R19 and board pin 10; the output from G7 is taken to the LF loop board PM349 via board pin 12, and the output from G8 is taken to the phase comparator, ML7.

### Phase Comparator

9. The output signal from the 34 MHz oscillator is divided to provide a frequency of 1 MHz when the oscillator frequency is correct. This frequency is compared with a reference 1 MHz frequency and any error between the two frequencies is used to develop a d.c. voltage which adjusts the oscillator frequency to eliminate the error. This voltage is generated in the phase comparator, and is applied to 34 MHz oscillator varactor diode D2 via L2.

10. The phase comparator consists of a dual D-type flip-flop, ML7, a two-input gate, G9 of ML6, and an output voltage control circuit, TR6, TR7, TR8. The action of the circuit is as follows.

11. The output from the divide-by-34 stage, at ML5 pin 2, is applied to the clock 1 input of ML7, whilst the reference frequency output, from ML4 pin 8, is applied to the clock 2 input of ML7. The D inputs of ML7, at pins 2 and 12, are both taken to the +5 V rail (logic '1'). Thus when the positive edge from ML5 pin 2 clocks ML7, the Q1 output at pin 5 changes to '1' and the Q1 output changes to '0'. Similarly, when the positive edge from ML4 pin 8 clocks ML7, the Q2 output changes to '1' and the Q2 output changes to '0'. When both Q1 and Q2 are at '1', the output from NAND gate G9 of ML6 changes to '0', clearing both ML7 flip-flops via R23 and thus resetting the Q outputs to '0' and the Q outputs to '1'.

12. Consider the case where the 34 MHz oscillator frequency is high. This will mean that the positive going edge from the divide-by-34 stage will occur before the edge from the 1 MHz reference frequency. The resultant setting and resetting of the flip-flops causes increased conduction of TR8, due to the Q1 output waveform (see Figure 4.3) as compared with the conduction of TR6; this causes the voltage at the collector of TR8 to become less positive, thereby reducing the voltage applied to the varactor diode D2, and reducing the oscillator frequency.

13. If the oscillator frequency is low, the divide-by-34 pulse will occur after the reference pulse, the Q2 output waveform will cause increased conduction of TR9 and the voltage at the collector of TR8 will become more positive. The increased voltage applied to the varactor diode causes the oscillator frequency to increase, thus correcting the error.

14. When the two frequencies are in phase the two flip-flops of ML7 are clocked at the same time, the Q1 output waveform is equal to the Q2 output waveform and the varactor line voltage remains constant.

Logic Circuits

15. The logic circuits consist of NAND gates ML8, NOR gates ML9, ML10, and the inverting output buffers TR9-TR11. Inputs from the frequency selection switches on the front panel, routed via inverting circuits on the Noise Immunity Board, are applied to ML8 and ML9 via board pins 13 to 17. The logic output levels, at board pins 21, 19 and 20, are used to select one of three oscillators on the HF loop board. Table 1 shows the output logic levels for the various combinations of control inputs.

TABLE 1

## Oscillator Selection Logic

INPUT PINS					OUTPUT PINS			OSCILLATOR SELECTED
16	15	17	13	14	21	19	20	
'1' on any pin			1	1	0	1	1	0-7MHz
0	0	0	1	1	1	0	1	8-17MHz
or '1' on any pin			*	0				
Any other condition					1	1	0	18-29MHz

\* = either 0 or 1

LF LOOP BOARD PM349

16. This board (Fig. 5) contains the low frequency loop and also the 1.4 MHz generation circuits. A block diagram of the board is given in Fig. 4.4.

18-23 MHz Voltage Controlled Oscillator

17. The 18 to 23 MHz VCO for the low frequency loop consists of transistor TR2, a tuned circuit, L2, C4, C5, and a varactor diode, D1: feedback is provided by the inverting gate G2 (ML1). The supply voltage for the VCO is provided by the series regulator transistor, TR1, and 5.6 V Zener diode D2.

18. The output from the VCO is shaped and buffered by NAND gate G3 (ML1) and is then applied to ML5 of the programmed divider and also to a divide-by-five stage, ML2. The output from ML2, in the frequency range 3.6 to 4.6 MHz, is applied to the transfer loop board PS338, via board pins 3 and 4, step-down transformer T1, a low pass filter L1, C1, C2, and NAND gate buffer G1.



Programmed Divider N1

19. The programmed divider consists of four presettable decade counters ML5, ML8, ML11, ML13, one preset counter ML16, two AND gates G4, G5 (ML6), two NAND gates G7, G8 (ML15), and a dual J-K flip-flop, ML9.

20. The decade counters have strobed parallel-entry capability such that the starting point of a count sequence may be preset. A '1' or a '0' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Ao, Bo, Co, Do), when the strobe (S) input is at '0'. The counting operation is performed on the negative-going edge of the input clock pulse.

21. The division ratio of the programmed divider, which is controlled by the 100 kHz, 10 kHz, 1 kHz and 100 Hz digits of the selected operating frequency, is given by the expression  $N1 = 46000$  minus the selected digits, i.e. the division ratio is 46000 for a setting of 0000 and 36001 for a setting of 9999. The operation of the divider is described below.

22. Binary coded decimal (BCD) frequency setting information is applied to the data inputs of ML5 (100 Hz), ML8 (1 kHz), ML11 (10 kHz) and ML13 (100 kHz). The Da, Db, Dc and Dd data inputs of ML16 are connected to the 0 V line and thus ML16 starts counting from zero.

23. To start a counting sequence, assume that a logic '0' strobe pulse is applied to the strobe (S) input of each decade counter. As described in para. 20, this causes the logic level applied to each input line (Da, Db, Dc, Dd) to be transferred to the corresponding output line (Ao, Bo, Co, Do). The negative-going edge of the clock pulse (from the VCO) is applied to the clock 1 input of ML5 and each pulse is now counted until an output from the counter of 45997 is reached i.e. until the Co output from ML16 is at '1' (binary 4), the Ao and Co outputs from ML13 are at '1' (binary 5), the Ao and Do outputs from ML11 and ML8 are at '1' (binary 9) and the Ao, Bo and Co outputs from ML5 are at '1' (binary 7). Since ML16 is preset to start counting from zero, and since the remaining counters may be preset to start counting at any number from 0 to 9, the maximum number of clock pulses that may be counted is equal to 45997.

24. Once a count of 45997 is reached, the input lines to AND gate G4 are all at logic '1' and the resulting '1' output (TP2) is applied to the J input of a dual J-K flip-flop, ML9. The VCO output is also applied to the clock inputs of ML9 (TP1) which counts a further three clock pulses before the Q output at ML9 pin 3 changes to logic '0' to strobe (reset) the decade counters. Thus three clock pulses are counted by ML9, making a total count of 46000, i.e.  $45997 + 3$ , until the reset occurs and the next counting sequence begins.

Reference Frequency Divider

25. The 1 MHz squarewave input at board pin 25 is applied to three decade dividers ML3, ML4, ML7, and a D-type flip-flop, ML10, connected to divide-by-two. The resulting 500 Hz reference frequency output (TP3) is applied to one of the clock inputs of the LF loop phase comparator flip-flop, ML12.

### Phase Comparator

26. When the 18 to 23 MHz VCO is operating at the correct frequency, the strobe pulses occur at a repetition rate of 500 pps. These pulses are applied to the phase comparator where they are compared with the 500 Hz reference frequency; any error between these two frequencies is used to develop a d.c. voltage which is applied to the VCO to eliminate the error.
27. The phase comparator consists of a dual D-type flip-flop ML12, NAND gate G6 (ML14), and a voltage control circuit, TR5 to TR11. The action of the circuit is as follows.
28. The output signal from the programmed divider N1, from ML16 pin 2, consists of positive-going pulses which are applied to the clock input of ML12A (Pin 3). The output signal from the reference divider also consists of positive-going pulses, and these are applied to the clock input of ML12B (Pin 11). The D inputs of ML12, at pins 2 and 12, are both taken to the +5 V rail (logic '1') via R25. Thus when the positive edge from ML16 pin 2 clocks ML12A, the Q output at pin 5 changes to '1' and the  $\bar{Q}$  output changes to '0'. Similarly, when the positive edge from the reference divider clocks ML12B, the Q output at pin 9 changes to '1' and the  $\bar{Q}$  output changes to '0'. When both Q outputs are at '1' the output from the NAND gate G6 (ML14), changes to '0' clearing both flip-flops of ML12 via R26 and thus resets the Q outputs to '0' and the  $\bar{Q}$  outputs to '1'.
29. Consider the case where the 18 to 23 MHz VCO frequency is high. This will mean that the positive edge from the programmed divider will occur before the positive edge from the reference divider. The resulting setting and resetting of the flip-flops causes increased conduction of TR7, due to the Q output waveform from ML12A (see Timing Diagram, Fig. 4.3) as compared with the conduction of TR5; this causes the voltage at the collector of TR7 to become less positive, allowing C39 to discharge via TR8 (connected as a diode) and reduce the voltage applied to the source follower, TR11. The output from TR11 (TP5), which is applied to the varactor diode D1 of the VCO, also reduces and causes a corresponding reduction in the VCO frequency to correct the error.
30. If the VCO frequency is low, the programmed divider output pulse will occur after the reference pulse, and the Q output waveform from ML12B will cause increased conduction of both TR5 and TR6. The voltage at the collector of TR6 becomes more positive and capacitor C39 charges via TR9 (connected as a diode). The resultant increase in the voltage applied to the varactor diode causes the VCO frequency to increase, thus correcting the error.
31. When the two signals are equal in frequency and phase the two flip-flops of ML12 are clocked at the same time, the two Q output waveforms are equal and the varactor line voltage remains constant.

LF Loop Lock Detector

32. The LF loop lock detector consists of a bistable latch G9, G10, and an output buffer, G11. The Q outputs from the phase comparator ML12 are connected directly to G9, and also to G10 via integrating components, R35, C30 and R38, C31. Under phaselocked conditions the in-phase negative-going Q output pulses from ML12, pins 6 and 8 (Q1 and Q2 of Fig. 4.3) are prevented from reaching G10 due to the time constants presented by the integrating components. Pins 4 and 5 of G10 therefore float up to logic '1' and the resulting logic '0' output, at G10 pin 6, forces the output of G11 to logic '1'. Thus for the in-lock condition a logic '1' signal is applied to board pin 24.

33. When an out-of-lock condition exists, the clock input waveforms applied to ML12 are no longer in phase and the resultant longer-duration negative-going output pulses from ML12 pin 6 or ML12 pin 8 (dependent on whether a phase lead or a phase lag exists) are sufficient in width to overcome the time constant presented by the respective integrating components. The effect of this is to produce an alternating '0' - '1' output from G11 which is inverted by G11 to produce a '0' - '1' out-of-lock signal at board pin 24.

1.4 MHz Generation

34. A divide-by-five output from ML3 provides a 200 kHz input to a 1.4 MHz crystal band-pass filter, XL1, XL2, C23, C24, C26; the seventh harmonic of the 200 kHz input is selected and this is amplified by TR3, TR4, to produce a 1.4 MHz output at the required level at board pins 1 and 2.

TRANSFER LOOP BOARD PS338

35. The transfer loop board (Fig. 9) contains the transfer loop (with the exception of the transfer loop oscillator which is contained on the HF loop board PS337), programmed divider N2 and lock indication circuits. This board, together with the HF loop board, generates the 35.4 to 65.4 MHz second mixer injection frequency. A block diagram of the two boards is given in Fig. 4.5.

36. The 4.6 to 3.6 MHz output signal from the LF loop, at board pin 17, is coupled by C3 to a shaper stage, TR4, TR5. The squarewave output is inverted by ML4a and is then applied to a programmed divider consisting of two presettable decade counters, ML1, ML2, an inverter, ML4b, a six-input NAND gate, ML5 and a D-type flip-flop, ML6.

Programmed Divider N2

37. The two decade counters, ML1, ML2, have strobed parallel-entry capability so that the starting point of a count sequence may be preset. A '1' or a '0' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Ao, Bo, Co, Do) when the strobe (S) input is at '0'. The counting operation is performed on the negative-going edge of the input clock pulse.

38. The division ratio of the programmed divider, which is controlled by the frequency switches, is given by the expression  $N2 = 40 + \text{selected MHz digits}$ , ie, when 00 MHz is selected, the division ratio is 40, and when 29 MHz is selected, the division ratio is 69. The operation of the divider is described below.

39. Frequency setting information from the MHz frequency selection switches is applied to the noise immunity board where it is converted into a BCD nines complement code (see Table 2). The nines complement coded outputs are supplied to the data inputs of the two decade counters, 'units' to ML1, 'tens' to ML2, and preset the starting point of a count sequence.

40. To start the counting sequence, assume that a logic '0' strobe pulse is applied to the strobe (S) inputs of both ML1 and ML2 (at pin 1). As described in paragraph 37, this causes the logic level applied to each input line (Da, Db, Dc, Dd) to be transferred to the corresponding output line (Ao, Bo, Co, Do). The negative going edge of the clock pulse (from the shaper stage, TR4, TR5 and the inverter ML4a) is now applied to the clock 1 input of ML1 at pin 8. Each clock pulse is now counted until a count of 37 is reached, i.e. until the Ao and Bo outputs from ML2 are both at logic '1' (binary 3) and the Ao, Bo and Co outputs from ML1 are all at logic '1' (binary 7). (The Co output from ML2 is applied to an inverter, ML4b, to inhibit binary 7.)

41. When a count of 37 is reached, the input lines to the NAND gate, ML5, are all at logic '1' and the '0' output, at ML5 pin 8, is applied to the D input of flip-flop ML6. The next clock pulse, which is applied to pin 3 of ML6, transfers the '0' at ML6 pin 2 to the Q output, at ML6 pin 5, and this is applied as the next strobe pulse to the two decade counters, ML1 and ML2, ready for the next count. The output from ML5 changes to logic '1' and the next clock pulse applied to ML6 causes the Q output to change to logic '1'; this output is applied to the phase comparator, ML8.

42. Table 3 shows the operation of the divider for various settings of the MHz switch.

### Mixer

43. ML3 is an integrated circuit mixer; the 1 MHz reference frequency signal, shaped by TR1, TR2, is applied to pin 8 and the 885 -948 kHz transfer loop oscillator output signal, from the HF loop board, buffered by TR3, is applied to pin 4 via a low-pass filter, L9, L10, C29 to C32. The difference frequency output from the mixer, 115 kHz to 52 kHz, is coupled to a low-pass filter, L11, L12, C36, C38, C39, and is then applied to a shaper stage, TR6. The squarewave output from TR6 is applied to the phase comparator, ML8 via a buffer, ML7A.

Phase Comparator

44. The phase comparator consists of a dual D-type flip-flop, ML8, a two-input NAND gate, ML7b and a voltage control circuit, TR7, TR8, TR9, TR10. It compares the output signal frequency from the programmed divider with the output signal frequency from the mixer; any error between these two frequencies is used to develop a d.c. voltage, which is applied to the transfer loop oscillator (on the HF loop board) to eliminate the error. The action of the circuit is as follows.

TABLE 2

Code Conversion

Decimal	BCD				Nines Complement				Decimal
	D	C	B	A	D9	C9	B9	A9	
0	0	0	0	0	1	0	0	1	9
1	0	0	0	1	1	0	0	0	8
2	0	0	1	0	0	1	1	1	7
3	0	0	1	1	0	1	1	0	6
4	0	1	0	0	0	1	0	1	5
5	0	1	0	1	0	1	0	0	4
6	0	1	1	0	0	0	1	1	3
7	0	1	1	1	0	0	1	0	2
8	1	0	0	0	0	0	0	1	1
9	1	0	0	1	0	0	0	0	0

TABLE 3

Programmed Divider Operation (PS338)

'MHz' Setting	Nines Complement	Clock Pulses				
		Count up to 100	Fixed Count	Strobe Pulse		Total Division Ratio
				Begin	End	
00	99	1	37	1	1	40
07	92	8	37	1	1	47
14	85	15	37	1	1	54
21	78	22	37	1	1	61
29	70	30	37	1	1	69

45. The output from the programmed divider, at ML6 pin 5, consists of negative-going pulses; these are applied to the clock input of ML8b. The output from the mixer (via the low-pass filter, shaper and buffer), at ML7a pin 8, is applied to the clock input of ML8a. The D inputs to both ML8a and ML8b are taken to the +5 V rail (logic '1'). Thus when the positive edge from ML6 pin 5 clocks ML8b, the Q2 output at pin 5 changes to '1' and the Q2 output changes to '0'. Similarly, when the positive edge from ML7a pin 8 clocks ML8a, the Q1 output changes to '1' and the Q1 output changes to '0'. When both Q outputs are at '1', the output from the NAND gate, ML7b, changes to '0', clearing both ML8 flip-flops via R38 and thus resetting the Q outputs to '0' and the Q outputs to '1'.

46. Consider the case where the frequency of the mixer output signal is high. This will mean that the positive edge from ML7a will occur before the edge from ML6. The resultant setting and resetting of the flip-flops causes increased conduction of TR7, due to the Q1 output from ML8a (see timing diagram, Fig. 4.3), as compared with the conduction of TR10; this causes the voltage at the collector of TR9 to become more positive, thereby increasing the varactor line voltage applied to the transfer loop oscillator on the HF loop board. This increases the oscillator frequency, but since this frequency is subtracted from the reference 1 MHz in the mixer, ML3, the output frequency from the mixer is reduced.

47. If the mixer output signal frequency is low, the pulse from ML7a will occur after the pulse from ML6, the Q2 output waveform from ML8b will cause increased conduction of TR10 and the voltage at the collector of TR9 will become less positive. Thus the reduced varactor line voltage applied to the transfer loop oscillator causes a reduction in oscillator frequency and a corresponding increase in the mixer output signal frequency.

48. When the two frequencies are in phase, the two flip-flops of ML8 are clocked at the same time, the Q1 output waveform is equal to the Q2 output waveform and the varactor line voltage remains constant.

#### Lock Indicator and Fast Lock Circuit

49. This circuit comprises two monostables, ML9, ML10, a dual D-type flip-flop, ML11, and NAND gates ML4c, ML4d. Its purpose is to augment the conduction of TR7 or TR10 in the out-of-lock condition and so obtain a faster return to the locked condition; it also provides a lock indication output signal. The action of the circuit is as follows.

50. The Q output from the phase comparator flip-flop, ML8a, is applied to the B input (Schmidt trigger) of the monostable, ML9, and also to the D and clear inputs of a D-type flip-flop, ML11a. Similarly, the Q output from ML8b is applied to the B input of the monostable, ML10, and also to the D and clear inputs of a second D-type flip-flop, ML11b. The two monostables, triggered when positive going signals are applied to the respective B inputs, each produce a negative going output pulse (Q), of approximately 1.5 microseconds duration.

51. From the timing diagram, Fig. 4.6, it will be seen that for the in-lock condition, the Q outputs from the two flip-flops, ML11a, ML11b, are both at logic '1'; these two signals do not, however, affect the conduction of the voltage control transistors TR7, TR10, due to the presence of the two diodes, D2, D3. The logic '0' output from ML4c is inverted by ML4d to produce a logic '1' in-lock signal at board pin 6.

52. If the output frequency from the mixer is low, as depicted by the out-of-lock waveform of Fig. 4.6, the negative excursion of the Q output from ML11b will be applied to TR10, via diode D3. The conduction of TR10 will, therefore, be rapidly increased to bring about a fast return to the in-lock condition. The Q output waveform from ML11b is also applied to ML4c to produce an alternating '0' - '1' out-of-lock signal at board pin 6.

53. Should the out-of-lock condition be due to a high mixer output frequency the Q output from ML11a will cause a rapid return to the in-lock condition by increasing the conduction of TR7; the Q output from ML11a is also applied to ML4c to produce an alternating '0' - '1' out-of-lock signal at board pin 6, as before.

#### HF LOOP BOARD PS337

54. This board (Fig. 7) provides the 35.4 - 65.4 MHz injection frequency for the second mixer; it also contains the 885 - 948 kHz transfer loop oscillator. The block diagram of the HF loop board, together with the transfer loop board, is given in Fig. 4.5.

#### Transfer Loop Oscillator

55. Transistors TR17 and TR20, together with associated components, form a variable frequency LC oscillator, tunable by the voltage applied to the varactor diode D19. The varactor line voltage at pin 18, from the transfer loop board, is applied to D19 via a filter, C66, C67, R62, C69 and L19.

56. The oscillator output signal, at the collector of TR20, is applied to the clock input of a divide-by-two stage, ML12; the output from ML12, at pin 5, is applied as one signal input to the phase comparator, ML7.

57. A second output from the oscillator is coupled by C76 to a buffer amplifier, TR21, the output from which is applied to the mixer on the transfer loop board, via C81 and pin 13.

#### HF Loop Oscillator

58. Three separate, switched oscillators are provided to cover the frequency range 35.4000 to 65.3999 MHz. Oscillator selection is controlled by the MHz frequency switches and the logic circuits on the 34 MHz generator board; an earth (0 V) is connected to the appropriate switching transistor, TR1, TR2 or TR3 (via pins 28, 27 or 26 respectively) and the supply voltage to the selected oscillator is switched on. The oscillator selected is in accordance with Table 4.

TABLE 4

## HF Loop Oscillator Selection

OSCILLATOR	FREQUENCY RANGE (MHz)	MHz SWITCH SETTING
3	35.4000 to 43.3999	0 to 7
2	43.4000 to 53.3999	8 to 17
1	53.4000 to 65.3999	18 to 29

59. The three oscillators are similar in construction and operation. Frequency is controlled by the voltage applied to a pair of varactor diodes; this voltage, derived by the phase comparator, is applied via a common line and an inductor (L21, L22, L23) to each oscillator. The gain of the selected oscillator stage is automatically controlled by peak-detecting diodes D13, D14, and the current source transistor, TR13; the automatic gain control (AGC) level is preset by R38.

60. The output from the selected oscillator transistor and associated buffer (TR7, TR8 or TR9) is amplified by TR10 and applied to:-

- (a) The AGC stage, TR13, via C26.
- (b) A programmed divider, via C24.
- (c) An output buffer amplifier stage, TR14, via C36.

#### Output Buffer Stage

61. The output buffer amplifier stage, TR14, is conventional; stage gain is preset by potentiometer R44 and the amplified output signal is taken to board pin 22 via C44.

#### Programmed Divider N2

62. The programmed divider, which is set to the same division ratio, N2, as that of the transfer loop board programmed divider, consists of a shaper stage, TR11, TR12, a divide-by-two stage, ML2a, two presettable decade counters, ML3, ML5, with associated gates, and three J-K flip-flops, ML2b, ML9a, ML9b.

63. The two decade counters, ML3, ML5, have strobed parallel-entry capability such that the starting point of a count sequence may be preset. A '1' or '0' at a data input (Da, Db, Dc, Dd) is transferred to the associated output (Ao, Bo, Co, Do) when the strobe (S) input is at '0'. The counting operation is performed on the negative-going edge of the input clock pulse.



64. The division ratio of the programmed divider, which is controlled by the frequency switches, is given by the expression  $N2 = 40 + \text{selected MHz digits}$ , i.e. when 00 MHz is selected, the division ratio is 40, and when 29 MHz is selected, the division ratio is 69. The operation of the divider is described below.

65. Frequency setting information from the frequency selection switches is applied to the noise immunity hoard where it is converted into a nines complement code (see Table 2). The nines complement coded outputs are applied to the data inputs of the two decade counters, 'units' to ML3 and 'tens' to ML5, and preset the starting point of a count sequence.

66. To start the counting sequence, assume that a logic '0' strobe pulse is applied to the strobe (S) inputs of both ML3 and ML5 (at pin 1). As described in paragraph 63, this causes the logic level applied to each input line (Da, Db, Dc, Dd) to be transferred to the corresponding output line (Ao, Bo, Co, Do). The negative-going edge of the clock pulse (from the shaper stage, TR11, TR12 and the divide-by-two ML2a) is now applied to the clock 1 input of ML3 at pin 8. Each clock pulse is now counted until a count of 35 is reached, i.e. until the Ao and Bo outputs from ML5 are both at logic '1' (binary 3) and the Ao and Co outputs from ML3 are both at logic '1' (binary 5).

67. When a count of 35 is reached, the input lines to the AND gate, ML4b are all at logic '1' and the '1' output, at ML4 pin 6, is applied to the J input of flip-flop ML2b. Both Q outputs from ML2b are fed to the dual J-K flip-flop, ML9 (Q to J, Q to K), and the Q output of ML9b is fed back to the K input of ML2b. The effect of this circuit is to produce a logic '0' strobe pulse (ML2BQ) sufficient in width for the two decade counters, ML3 and ML5. As can be seen from the timing diagram, Fig. 4.7, the strobe pulse is extended to the negative-going edge of the 39th clock pulse, at which point the counting sequence is repeated.

68. Table 5 shows the operation of the programmed divider for various settings of the MHz frequency selection switch.

TABLE 5  
Programmed Divider Operation (PS337)

'MHz' Setting	Nines Complement	Clock Pulses			Total Division Ratio
		Count up to 100	Fixed Count	Strobe Pulse Generation	
00	99	1	35	4	40
07	92	8	35	4	47
14	85	15	35	4	54
21	78	22	35	4	61
29	70	30	35	4	69

Phase Comparator

69. The phase comparator comprises a dual D-type flip-flop, ML7, a two-input NAND gate, ML6 (pins 4, 5 and 6), and a voltage control circuit TR16, TR18, TR19. It compares the output signal frequency from the transfer loop oscillator (after division by two in ML12) with the output signal frequency from the programmed divider; any error between these two frequencies is used to develop a d.c. voltage which is applied to the selected HF loop oscillator to eliminate the error. The action of the circuit, which is similar to that of the transfer loop board (PS338), is as follows.

70. The programmed divider output, which is taken from ML2b pin 5, consists of positive-going pulses; these are applied to the clock input of ML7a. The output from the divide-by-two stage, ML12b pin 9, is applied to the clock input of ML7b. The D inputs of both ML7a and ML7b are taken to the +5 V rail (logic '1'). Thus when the positive edge from ML2b clocks ML7a, the Q output at pin 5 changes to '1' and the Q output changes to '0'. Similarly, when the positive edge from ML12 pin 5 clocks ML7b, the Q output changes to '1' and the Q output changes to '0'. When both Q outputs are at '1', the output from the NAND gate, ML6a, changes to '0', clearing both ML7 flip-flops via R61 and thus resetting the Q outputs to '0' and the Q outputs to '1'.

71. Consider the case where the frequency of the selected HF loop oscillator output signal (which is applied to the programmed divider) is high. This will mean that the positive edge from ML2b will occur before the edge from ML12. The resultant setting and resetting of the flip-flops causes increased conduction of TR19, due to the Q output from ML7a (see timing diagram, Fig. 4.3), as compared with the conduction of TR16; this causes a reduction in the varactor line voltage, taken from the collector of TR18, and thus a reduction in the frequency of the selected HF loop oscillator output signal.

72. If the frequency of the selected HF loop oscillator output signal is low, the edge from ML2b will occur after the edge from ML12; the Q output from ML7b will cause increased conduction of TR16, the voltage at the collector of TR18 will become more positive and this will cause an increase in the frequency of the selected HF loop oscillator output signal.

73. When the two frequencies are equal, the two flip-flops of ML7 are clocked at the same time, the Q output waveform from ML7a is equal to that from ML7b and the varactor line voltage remains constant.

Lock Indicator and Fast Lock Circuit

(Applicable to later versions only - Issue 7 onwards)

74. This circuit comprises a monostable ML11, a D-type flip-flop ML12a, and two NAND gates ML6b, ML6c. Its purpose is to augment the conduction of TR16 or TR19 in the out-of-lock condition and so obtain a faster return to the locked condition; it also provides a lock indication output signal. The following description should be read in conjunction with the timing diagram, Fig. 4.8.

75. The Q output waveforms from the phase comparator, ML7a and ML7b, are applied to NAND gates ML6b, ML6c, via integrating components R36, C92 and R60, C94 respectively, whilst the phase comparator Q output waveforms are applied to the A inputs of a monostable, ML11.

76. Under phase-locked conditions, the in-phase positive-going Q output pulses from ML7a and ML7b are prevented from reaching NAND gates ML6c and ML6b respectively due to the time constants presented by the integrating components; pins 9 and 12 of ML6, and also the D input of ML12a, are therefore at logic '0'. The resulting logic '1' outputs from ML6 pins 8 and 11 do not, however, affect the conduction of the voltage control transistors, TR16, TR18, TR19, due to the presence of the two diodes, D20 and D22.

77. ML11 is a negative edge-triggered monostable which produces a negative-going output pulse (Q) of approximately 1.5 microsecond duration (timing components R69, C75) when either or both of the A inputs are at logic '0' with the B input at logic '1'. (The B input is not connected externally and therefore floats up to logic '1'). Under phase-locked conditions, the in-phase negative-going phase comparator output pulses applied to ML11 produce a negative-going pulse train at ML11 pin 1 which clocks ML12a (positive-edge triggered) to produce a steady logic '1' in-lock signal at board pin 12 (Fig. 4.8).

78. If the output frequency from the programmed divider is low (as depicted by the centre set of waveforms of Fig. 4.8), the longer-duration positive-going output pulses at ML7b pin 9 are sufficient in width to overcome the time constant presented by integrating components R36 and C92. The effect of this, together with the Q output waveform from ML11, is to produce a negative-going output pulse from ML6b; this is applied to TR16, via D20, and rapidly increases the conduction of TR16 to bring about a fast return to the locked condition (in practice, a rapid succession of negative-going pulses appears at ML6b pin 11 as the programmed divider output frequency increases). At the same time, the combination of the D and CK waveforms applied to ML12a produce an alternating '0' - '1' out-of-lock signal at board pin 12.

79. Should the out-of-lock condition be due to a high programmed divider output frequency (lower set of waveforms of Fig. 4.8) the resulting longer-duration positive-going output pulses at ML7a pin 5 are sufficient in width to overcome the time constant presented by R60 and C94 and the negative-going output pulse at ML6c pin 8 will cause a rapid return to the locked condition by increasing the conduction of TR19; the output pulse from ML6c is also applied to the clear input of ML12a, and the combination of this and the Q output waveform from ML11 produces an alternating '0' - '1' out-of-lock signal at board pin 12, as before.

## FREQUENCY SELECTOR SWITCHES

### General Description

80. The Frequency Selector Switch (Fig. 28) consists of six individual switches, one switch for each frequency decade.

81. Each switch accepts +12 V, and according to the value the switch is set at, routes +12 V or an open circuit to the switch output. Fig. 4.9 shows all the possible positions of the four switch sections for each of the six switches.

82. The state of any frequency selection line is either open circuit or +12 V. The MHz x 10 and MHz x 1 switches provide an inverted and 9's complement BCD output; the kHz x 100, kHz x 10, kHz x 1, and Hz x 100 switches provide an inverted BCD output. A truth table to show switch operation is given in Table 6.

TABLE 6: Frequency Selector Switches

	Switch setting (Decimal)										
	0	1	2	3	4	5	6	7	8	9	
Binary	1	0	1	0	1	0	1	0	1	0	1
	2	0	0	1	1	0	0	1	1	0	0
	4	0	0	0	0	1	1	1	1	0	0
	8	0	0	0	0	0	0	0	0	1	1
Inverted Binary 100 Hz, 1 kHz, 10 kHz and 100 kHz decades	1	1	0	1	0	1	0	1	0	1	0
	2	1	1	0	0	1	1	0	0	1	1
	4	1	1	1	1	0	0	0	0	1	1
	8	1	1	1	1	1	1	1	1	0	0
Switch setting 9's complement (Decimal)	9	8	7	6	5	4	3	2	1	0	
Inverted 9's complement Binary 1 MHz Decade	1	0	1	0	1	0	1	0	1	0	1
	2	1	1	0	0	1	1	0	0	1	1
	4	1	1	0	0	0	0	1	1	1	1
	8	0	0	1	1	1	1	1	1	1	1
Inverted 9's Complement Binary 10 MHz Decade	1	0	1	0							
	2	-	-	-							
	4	-	-	-							
	8	0	0	1							

NOTE: 1 = +12 V  
0 = open circuit

LOW LEVEL BOARD PM341Function

83. The Low Level board (Fig. 11) processes all the audio and key input signals to the exciter and produces a modulated output at 1.4 MHz which is translated to the final output frequency by the mixer and output board. The board also contains the necessary attenuation circuits and relay drives for selection of the required sideband filter.

Keyed Mode

84. The MA1720 generates a keyed output by keying a 1 kHz oscillator, TR19, which feeds one of the balanced modulators. When any of the key or CW positions are selected on the front panel, +12 V is applied to the board via either pin 45 or 46, thus turning on TR9 and thence TR14, connecting +12 V to a tone insertion oscillator, TR19, and associated switching transistors, TR15, TR18. The +12 V supply is also connected to TR1 via D18 and D12, turning on TR1 to switch off the -7 V regulator transistor TR3 and mute the channel 1 audio amplifier.

85. The keying input to the board is either direct keying between pins 44 and 43 or remote keying via the RTTY board at pin 22. For direct keying, a closed key connects pins 44 and 43 and takes TR15 base to 0 V; for remote keying a +12 V signal applied to the RTTY board applies approximately 20 V to pin 22, turning TR8 on and taking TR15 base to 0 V. TR15 collector rises towards +12 V, producing the following results:-

- (a) It switches on TR18, connecting the output of the LC audio oscillator TR19 into the main audio path via R59, C29.
- (b) It operates the mute delay circuit TR20-TR26. In the 'normal' state C40 is charged to approximately 6.5 V and thus TR25 and TR26 are conducting, giving a 0 V output to the 'OR' gate on the control board and muting the output. Upon initiation of keying, TR20 and TR22 are turned on, discharging C40 rapidly to 0 V via R84; this turns TR25 and TR26 off, allowing the collector to rise to +12 V which is applied to the control board to demute the exciter. Upon cessation of keying TR20 and TR22 are turned off, C40 charges towards +12 V via R83, and when the potential on the base of TR25 reaches 6.5 V, TR26 turns on taking pin 47 to 0 V to mute the exciter. This ensures that so long as keying is not suspended for more than 2 seconds the exciter and any associated equipment remain active, but after this period of time they are automatically muted.

Tone Insertion Oscillator

86. The tone insertion oscillator consists of a tuned transformer (1 kHz) coupled oscillator; feedback is provided by R68 and R69 in the emitter circuit of TR19; R69 provides adjustment of the feedback level. Output level adjustment is provided by R65.

RTTY Mode

87. The RTTY signal from the RTTY Board pin 9 is fed onto the board at pin 24 and routed into the audio channel via R114.

Audio Mode

88. The audio input is fed onto the board at pins 41 (audio 1) and 35 (audio 2), and is routed to pins 38 (32) via front panel level control potentiometers; from there the inputs are applied to similar AF amplifiers.

89. The audio 1 input at pin 38 drives the differential amplifier TR10, TR12 via the phase splitter TR6. The output at TR12 collector is applied to amplifier ML1, which has a gain of approximately 200 times; AGC action is provided by TR16 and diodes D13, D17. A sample of the audio output from ML1 is detected by D19, D23 and the resulting signal is used to control the current through TR16 and thus through D13 and D17, as the effective impedance of D13 and D17 is dependent upon the current flowing through them, this controls the overall gain of the amplifier. A potential of -3 V is required on TR16 base to turn it on to set the output level from the amplifier at approximately 4.5 V<sub>peak-to-peak</sub>.

90. The output of ML1 is applied to level control gates TR28, TR32, via the 'channel' 1 gain potentiometer R73. The level control gates are brought into operation when reinserted carrier modes are selected in order to reduce the gain of the audio channel, thus preserving a constant p.e.p. level at the output (para. 96).

91. The audio 2 input is similarly processed in the circuit comprising ML2 and associated components, and is applied to a 16 dB level gate TR30, via potentiometer R75.

VOX

92. VOX operation is available on channel 1 on single sideband modes. A sample of the output from ML1 is applied via the 'VOX sensitivity' potentiometer R79 to the amplifier TR23, TR24, the output of which operates the Schmidt trigger TR27, TR29. The output of the Schmidt switches TR33 in the mute delay circuit TR33-TR39, which operates in the same fashion as the CW mute delay circuit, giving a fast attack, and a 2 second delay time.

Production of 1.4 MHz First IF

93. The 1.4 MHz signal, derived from the frequency standard, is fed onto the board at pin 16 at a level of about 0 dBm and applied to the AGC amplifier TR43-TR46, which stabilises it at a level of 250 mV r.m.s. From pin 16 the signal is passed into a variable attenuator formed by R133 and TR40, the output of which is amplified by TR43 and TR44. The signal at the emitter of TR44 is amplified by TR45 and detected by D35 and D36; the resultant d.c. signal is amplified by TR46 and then applied to TR40, thus controlling the overall gain of the amplifier. The output level is adjustable by R149, and is set for exactly 250 mV r.m.s. at TP5. The low-impedance output from TR44 emitter is applied in parallel to:-

- (a) The balanced modulator stages TR41, D33, TR47 (channel 1) and TR42, D34, TR48 (channel 2).
- (b) The 1.4 MHz carrier insertion stage TR49-TR52.

94. The output from channel 1 level gates is amplified by TR34, TR37, and the low-impedance output from TR37 emitter may be applied to either of the balanced modulators according to the state of RLA and RLB. The channel 2 modulating input at TR35 base is amplified by TR35, TR38; the low-impedance output from TR38 emitter is applied to the channel 2 balanced modulator when the ISB mode is selected. The gain of channel 2 is set to be 6 dB down on that of channel 1.

95. The outputs of the balanced modulators are routed via band-pass filters to the input of the feedback summing amplifier TR55, TR57 where the 1.4 MHz carrier frequency is re-inserted (via the amplifier and switch TR51) to form the first IF of 1.4 MHz; this is fed off the board at pin 10 at a level of 0 dBm. D45, D46, D47 form a limiter circuit arranged to operate when the level at TP6 is about 9 V peak-to-peak (output level of +2 dBm) to prevent overloading of following stages.

#### Attenuation Gates

96. Attenuation gates are provided as follows, energised by +12 V d.c. inputs to pins 26 (6 dB), 23 (16 dB) and 20 (26 dB or 20 dB - see note).

##### (a) 6 dB gates

- (i) TR28, shunting the channel 1 modulating input to TR34 (attenuates signal by 6 dB).
- (ii) TR54, shunting the 1.4 MHz output from TR51.

##### (b) 16 dB gates

- (i) TR32, shunting the channel 1 modulating input to TR34 (attenuates signal by 1.5 dB).
- (ii) TR30, shunting the channel 2 modulating input to TR35.
- (iii) TR60, shunting the 1.4 MHz output from TR51.

##### (c) 26 dB gate (or 20 dB - see note)

TR53, shunting the 1.4 MHz output from TR51.

NOTE: For 20 dB carrier insertion, R188 is changed from 18 ohms to 39 ohms.

97. The 'Tune' attenuator TR61 is energised by +12 V d.c. at pin 27, and shunts the 1.4 MHz output from TR51. Its attenuation may be adjusted by means of R204.

98. When any of the above attenuation gates are selected, -12 V is applied to the base of TR49 via the appropriate diode in the chain D37-D41 and the base resistor R166. TR49 will switch on, switching off TR50 which will switch on TR52. This action will switch on the 1.4 MHz amplifier TR51, and the 1.4 MHz signal will be applied via the amplifier to the appropriate attenuator gate. The gain of this stage is controlled by R184.

#### Relay Drivers

99. Relays RLA and RLB are driven by TR21 and TR31 respectively; their contacts control the routing of the modulating inputs to the balanced modulators.

100. When 'LSB' is selected by applying +12 V to pin 30, RLA in TR21 collector is energised and contact RLA1 routes the channel 1 input to the channel 2 modulator, the output of which is taken to the USB filter.

101. When 'USB' is selected, both relays are de-energised and the channel 1 input is routed via the channel 1 modulator to the LSB filter.

102. When 'ISB' is selected, RLB is energised via TR31: RLA is de-energised, and the channel 1 input therefore generates the upper sideband while the channel 2 input generates the lower sideband.

#### Auxiliary Control Inputs

103. The auxiliary control functions are summarised in Table 7.

#### Meter Amplifier

104. Transistors TR62-TR64 form a meter drive circuit. The amplifier accepts audio inputs at approximately -30 dBm at pin 15, and with diodes D48, D49 in the feedback network provides 100 microamp d.c. for full scale deflection of the front panel meter. R195 is for initial calibration of the meter circuit.



TABLE 7

## Auxiliary Control Functions

CONTROL INPUT	OPERATION ON APPLICATION OF +12 V
Full Power (pin 9)	Sets the output to maximum by switching on TR58 and setting the gain of the output amplifier to maximum.
Low Power (pin 8)	Switches on TR56 allowing output level to be adjusted by R190 - this enables the output level to be set between 0 dB and -7 dB down on the normal level.
- 6 dB (pin 26)	Turns on 1.4 MHz switch (TR51) via D39, operates 1.4 MHz 6 dB gate (TR54), and 6 dB audio gate (TR28).
-16 dB (pin 23)	Turns on 1.4 MHz switch (TR51) via D37, operates 1.4 MHz 16 dB gate (TR60), and 16 dB audio gates (TR30, TR32).
-26 dB (or -20 dB)* (pin 20)	Turns on 1.4 MHz switch (TR51) via D40, operates 1.4 MHz 26 dB or 20 dB gate (TR53)*
ISB (pin 29)	Operates RLB (TR31) and 6 dB audio gate via D26
Tune (pin 27)	Mutes audio by turning off -7 V regulator (TR3) via D28. Turns on 1.4 MHz switch (TR51) via D41, operates tune gate (TR61) allowing tune level to be set by R204. Also operates full power gate (TR58) via D51, and inhibits low power gate.
LSB (pin 30)	Operates RLA (TR21)
RTTY ON (pin 21)	Mutes audio by turning off -7 V regulator (TR3) via D9, D12.
CW-6 (pin 45)	Switches on the tone insertion oscillator by turning on TR14 via D4 and D10. Operates 6 dB audio gate (TR28) via D1, D2, D27, and 1.4 MHz switch (TR51) via D1, D2 and D39, and 1.4 MHz 6 dB gate (TR54) via D1, D2. Also mutes audio by turning off -7 V regulator (TR3) via D4, D18 and D12.
CW supp. (pin 46)	Switches on the tone insertion oscillator by turning on TR14 via D3 and D10. Mutes audio by turning off -7 V regulator (TR3) via D3, D18 and D12.

\* Resistor R188 is changed to 39 ohms for 20 dB.

RTTY GENERATOR BOARD PS568Function

105. The RTTY Generator Board (Fig. 13) accepts either polar or neutral (positive or negative) telegraph signals (by the appropriate setting of links LK1 and LK2) and produces the mark/space output voltages in the Remote keying mode or the mark/space audio frequencies in the RTTY mode. The mark/space frequencies may vary from  $\pm 42.5$  Hz to  $\pm 425$  Hz about a 2 kHz nominal frequency. The Remote keying and RTTY outputs are both applied to the Low Level Board. The Remote keying output is taken from pin 2 of the board whilst the RTTY output is taken from pin 9.

Remote Keying

106. The keying input at pin 3 is applied via the input selection circuitry (TR1, TR2, LK1, LK2) and the voltage divider network R6, R7 to the gate of TR3; the voltage appearing at TR3 gate is limited between +4 V and -5.4 V by Zener diodes D3 and D4. TR3 switches the base of TR4, producing an output from pin 2 of approximately +20 V mark and 0 V space.

RTTY Mode (see also para. 145)

107. The input at pin 3, which may be derived from a 5-0-5 V or an 80-0-80 V supply, is applied to TR3 gate and switches TR4. The output may be taken directly from TR4 collector or via the inverting stage TR5 according to the position of link LK3 (which provides 'normal' keying in position A-B and 'reverse' keying in position A-C) and is applied via R17 to the coupled emitters of TR6 and TR7.

108. TR6, TR7, TR8, TR9 and C6 shape the input to trapezoidal form (constant-current sources being provided by TR6 and TR7) with rise and fall times of approximately 750 microseconds and amplitude of +20 V p-p; this output is then applied via R20 and TR8, TR9, to control the parameters of the pulse generator TR13, C6, C7. R27 in TR11 emitter controls the generator frequency and is set to give a p.r.f. of 4 kHz; R20 in TR10 base controls the frequency shift within the range  $\pm 42.5$  Hz to  $\pm 425$  Hz. The output of the pulse generator is coupled by C10 into the 'clock' input of the J-K flip-flop ML1, which produces a squarewave output at half the input frequency. This is fed off the board at pin 9, via the level-control potentiometer R36 and board pin 9, to pin 24 on the Low Level Board.

109. TR12 and associated components form the enable/inhibit stage for the RTTY output. When +12 V is applied at pin 7 (from SK1/31 on the front panel) Zener diode D13 conducts and turns TR12 on, applying logic '0' to the J input of ML1 and enabling the output; an open circuit at pin 7 applies logic '1' to the J input and inhibits the output. The output may also be enabled by +12 V applied from SK1/33 on the front panel via the 'RTTY TEST' pin 5 and diode D12; this also selects a 'mark' signal by applying a positive input to TR3 via R8, overriding any input on pin 3.

Pulse Generator

110. The pulse generator uses a complementary unijunction transistor TR13. At the beginning of a cycle, C6 charges via TR11 towards 0 V; when the B1-E voltage on TR13 reaches a value of approximately 8.6 V, C6 discharges via TR13 and R26, causing a voltage pulse of approximately 5 V peak to be developed across R26.

111. The frequency of oscillation is controlled by the current through TR11, which is adjustable by R27, and also by the potential at TR10 base which is determined by the setting of R20 and the switching waveform from the trapezoidal shaper.

MIXER AND OUTPUT BOARD PM342

112. This board (Fig. 15) contains the following circuits:-

- (a) First and second mixer circuits, with associated filters and amplifiers.
- (b) Input amplifiers for the 34 MHz fixed and 35.4 - 65.4 MHz variable frequencies.
- (c) Muting circuit.

Mixers and Output Amplifier

113. The 1.4 MHz first IF from the low level board is fed onto the mixer and output board at pin 4 at a level of 0 dBm and into the first mixer stage T1, T2; there it is mixed with the 34 MHz stable frequency from the 34 MHz Generator Board to produce the second IF of 35.4 MHz. Unwanted frequency components are removed by the bandpass L-C filter including C7-C30, which provides 50 dB attenuation of the fundamental and 70 dB image rejection.

114. The signal is then amplified by TR7, TR8, filtered again in the crystal filter, (which reduces wideband noise into the final mixer and has a pass-band of  $\pm 6$  kHz centred on 35.4 MHz), and then fed into the final mixer T8, T10. There it is mixed with a signal in the range 35.4-65.4 MHz derived from the synthesizer boards, and the resulting signals are filtered by the low-pass filter L8-L10 (which has a sharp cut-off above 30 MHz). The output from the filter is a signal in the range 1-30 MHz at a level of -16 dBm; this is applied via the buffer amplifier TR14, TR15, which also incorporates a gain control R70, to the input of the five-stage wide-band output amplifier TR9-TR13. The output at a level of +23 dBm is taken off the board at pin 16.

Input Amplifiers

115. The two input amplifiers, for the 34 MHz fixed frequency and the 35.4-65.4 MHz variable frequency, are similar in construction and operation.

116. The 34 MHz signal is fed onto the board via pin 7 at a level of 0 dBm and a.c. coupled into the base of the driver transistor TR1. The output of the push-pull stage TR2, TR3, is a 20 V p-p sinewave to the first mixer.

117. The 35.4 - 65.4 MHz signal is fed onto the board via pin 8 at a level of 0 dBm, and a.c. coupled into the base of driver transistor TR4. The output of the push-pull stage TR5, TR6, is a 20 V p-p sinewave to the second mixer.

#### Muting Circuit

118. The muting circuit TR16, TR17 controls the supply to the collectors of TR9-TR12 in the output amplifier. Transistor TR17 is normally held on by the +12 V d.c. input to pin 12 from pin 5 on the Control Board and TR16 is bottomed, applying +20 V to the output amplifier. When TR17 base is taken down to 0 V, TR16 cuts off and removes the supply to the amplifier.

#### NOISE IMMUNITY BOARD PM346

119. The function of the noise immunity board (Fig. 17) is to prevent random operation of any of the frequency selection lines by noise or RF signals picked up on the lines when the unit is used on extended control.

120. The board contains circuits (one for each frequency selection line) which accept + 12 V for 'select' and open circuit for 'not select'. The input line to each circuit is taken via a 4.7 k ohm resistor to the -7 V rail (earth clamp diodes in the transistor base circuits prevent reverse base/emitter voltage breakdown) and thus a voltage greater than approximately 8 V (relative to -7 V) must be applied to the input line before the transistor will conduct.

121. The outputs of the board are taken from the collectors of transistors to the inputs of the three programmed dividers; selection of a line causes the associated transistor to conduct and apply logic '0' to the divider input.

#### CONTROL BOARD PM345

122. The Control Board (Fig. 19) logic and switching circuits accept the inputs and produce the outputs summarised in Table 8.

TABLE 8

## Control Board Input and Output Signals

INPUT/PIN	OUTPUT/PIN
Reset (+12 V) 29	'Reset' to Tx (+12 V) 30 Removes earth from 'Reset' lamp 4 Removes +12 V from remote 'Reset' line 32
In lock (+5 V) 25,26,27	Earth to 'In lock' lamp 3 +12 V to remote 'In lock' line 31
Mute (+12 V) 24	'Mute' to Mixer & Output Board and TX (0 V) 5
Selector Switch inputs (+12 V) 18,19,20,21	'De-mute' to Mixer & Output Board and Tx (+12 V) 5
Tune Switch (+12 V) 17	'Tune' to Low Level Board (+12 V) 11 'Inhibit' to Mode Switch (0 V) 12 'De-mute' to Mixer & Output Board and Tx (+12 V) 5
Fault (0 V) 1	Earth to 'Reset' lamp 4 +12 V to remote 'Reset' line 32 'Mute' to Mixer & Output Board and Tx (0 V) 5
Reduced Power (+12 V) 6	Earth to 'Reduced Power' lamp 7 +12 V to remote 'Reduced Power' line 33
Ready (0 V) 8	Earth to 'Ready' lamp 10 +12 V to remote 'Ready' line 34 'Enable' to Mode Switch (+12 V) 12
Standby (+12 V) 13	Earth to 'Standby' line 14
EHT On (+12 V) 15	Earth to 'EHT On' line 16
<u>Power Supplies</u>	
+12 V 9	
+5 V 2	
-7 V 28	
Earth 22	
Logic Earth 23	

Reset Input (pin 29)

123. Pin 29 is normally open circuit. When the 'Reset' button on the front panel is pressed, +12 V is applied to pin 29; this turns TR2 on, with the following effects:

- (a) TR1 turns off, applying +12 V to the associated linear amplifier as a 'Reset' command via pin 30.

- (b) The '0' at TR2 collector is inverted by G1 and used to trigger the 2-second monostable ML4, which applies a '0' for 2 seconds to G2 and G3; this resets the latch described in paras. 135 to 137.

#### In Lock Input (pins 25, 26, 27)

124. The inputs to these pins are derived from the lock indicators associated with each of the three phase comparators in the frequency synthesizer, which output '1' to indicate the 'in lock' condition. When all three inputs are at '1', the output of G6 is '0'; this is inverted to '1' by G8 and applied to:

- (a) TR4, which turns on and lights the 'in lock' lamp via pin 3, and also turns TR5 on to apply +12 V to the remote 'In lock' line via pin 31.
- (b) G4 in the latch circuit, leaving the latch in the 'normal' (de-mute) condition (para. 135).

#### Mute Input (pin 24)

125. Pin 24 is normally open circuit. When the 'Mute' switch is operated, +12 V is applied via pin 24 to TR8, turning it on and applying '0' to one of the inputs of G9; G9 therefore outputs a '1'. This turns TR9 on and applies a 'mute' command of 0 V via pin 5 to the transmitter and to the mixer and output board.

#### Selector Switch Inputs (pins 17-21)

126. A +12 V signal on any of these inputs, applied through TR12 and G10, results in a logic '1' input to G9. If there is no +12 V signal present at any of these inputs a '0' is applied to G9, which results in a 0 V 'mute' command output from pin 5 via TR9.

127. A +12 V signal from the 'Tune' switch on pin 17, in addition to the above actions, applies a +12 V 'tune' signal to the Low Level Board via D17 and pin 11 it also switches TR17 on via Zener diode D18, removing the +12 V supply to the mode switch via TR16 and pin 12 to prevent selection of other modes.

#### Fault Input (pin 1)

128. In normal operation, +12 V is applied to pin 1; this back-biases D1, causing Zener diode D2 to conduct and turn TR3 on, thus applying logic '0' to G2. A fault condition is signalled by 0 V at pin 1, resulting in a '1' input to G2 and a '0' output. This causes the output of G5 to go to '1', lighting the 'reset' lamp via TR6 and pin 4 and applying +12 V to the remote 'reset' line via TR7 and pin 32. The '1' output from G5 is also applied via G7 and G9 to TR9, producing a 0 V 'mute' output at pin 5.

129. If the 'Reset' button is now pushed, the output of G5 will change to '0' only for the 2-second period of the monostable ML4; the drive unit will therefore de-mute, and the 'reset' light will go out, for only two seconds.

Reduced Power Input (pin 6)

130. Pin 6 is normally held at 0 V. When the linear amplifier is operating at reduced power +12 V is applied, turning TR10 and TR11 on. TR10 lights the 'reduced power' lamp via pin 7, and TR11 applies +12 V to the remote 'reduced power' line via pin 33.

Ready Input (pin 8)

131. Pin 8 is held at +12 V when the linear amplifier is 'not ready'. When it is 'ready' the input goes to 0 V, turning TR13 off, TR14 on and TR15 on. TR14 lights the 'ready' lamp via pin 10, and TR15 applies +12 V to the remote 'ready' line via pin 34; TR14 also removes the drive from TR17 via D15 and D18, turning TR16 on and applying +12 V via pin 1 to enable the 'Mode' switch.

132. In the absence of a 'ready' input (i.e. if pin 8 is at +12 V) TR14 collector is at +12 V; this is applied to:

- (a) The 'tune' control line on the Low Level Board via D15 and pin 11.
- (b) TR12 via Zener diode D13, D14 and R34, turning TR12 on and applying logic '1' via G10 to pins 1 and 2 of G9.

Standby Input (pin 13)

133. A +12 V signal is applied to pin 13 when the front panel 'Standby On' button is pushed; this turns TR18 on and applies a 0 V signal to the linear amplifier via pin 14. When 'Standby' is not selected, pin 13 is open circuit and the output at pin 14 is +12 V.

EHT On Input (pin 15)

134. A +12 V signal is applied to pin 15 when the front panel 'EHT On' button is pushed; this turns TR19 on and applies a 0 V signal to the linear amplifier via pin 16. When 'EHT On' is not selected, pin 15 is open circuit and the output at pin 16 is +12 V.

Latch Circuit G3/G4

135. Gates G3 and G4 form a latch, which is reset by a '0' on pin 4 of G3 and tripped by a '0' on pin 9 of G4. When the synthesizer is caused to go out of lock by a change in the frequency setting, a fast negative pulse is applied to pin 9 of G4 (see para. 124). This trips the latch, causing a '0' to appear on pin 6 of G3 and a '1' on pin 11 of G5; this turns TR6 on, lighting the 'Reset' lamp via pin 4 and applying +12 V to the remote 'Reset' line via TR7 and pin 32.

136. The '1' on pin 11 of G5 is inverted by G7 and applied to pin 5 of G9, causing G9 to output a '1'; this turns TR9 on, placing a 0 V 'Mute' signal on pin 5. D5 in TR9 collector protects TR9 against reverse switching pulses from the relay connected to the 'Mute' line.

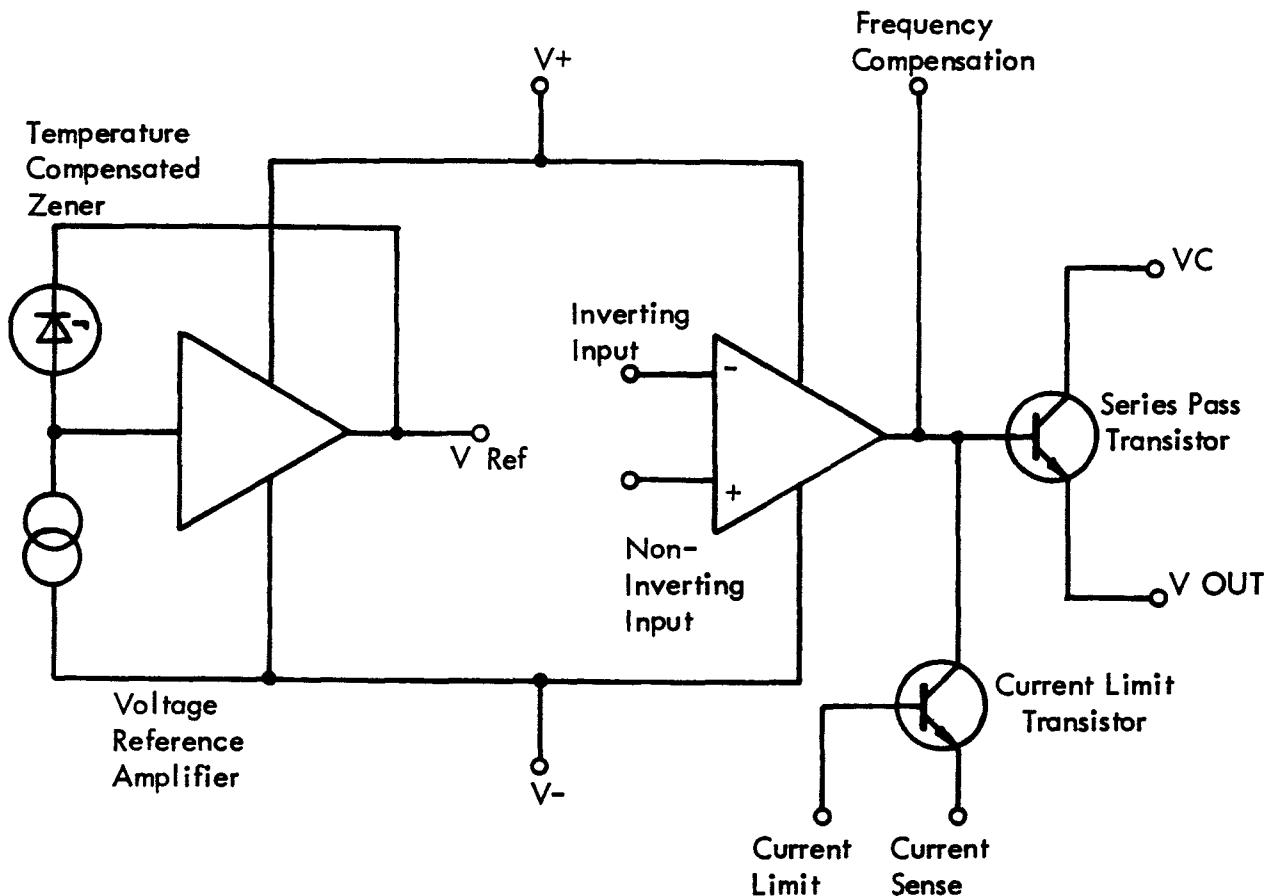
137. The latch G3/G4 is reset by a '0' on pin 4 of G3, applied via pin 29, TR2, G1 and the monostable ML4 when the 'Reset' button is pushed.

### POWER SUPPLIES

138. The power supply section of the drive unit (Fig. 21) comprises a voltage selector unit 1VS1, a mains transformer 1T3, a regulator board and four series-pass power transistors, 1TR1 to 1TR4. Stabilised supplies of -7 V, +5 V, +12 V and +20 V are provided.

### Regulator Board PM372

139. This utilises four identical integrated circuit regulators, ML1 to ML4. This device consists of a temperature compensated reference amplifier, error amplifier, series pass transistor and current limit circuitry. An equivalent circuit of the device is given below.



**Equivalent Circuit: Voltage Regulator IC**

140. The error amplifier is used to compare the reference voltage (maximum approx. +7 V) with a sample of the final stabilised output voltage (via a potential divider if greater than the reference voltage) and the output of the error amplifier is then used to control the series pass transistor. This transistor is also controlled by a current limiting stage which itself is controlled by the current drawn from the supply by the external circuitry.



-7 V Regulator

141. A 10 V secondary winding of 1T3 is connected to a full wave bridge rectifier, D1, via board pins 19 and 20. The positive output from D1 is applied to the collector of the external series pass transistor, 1TR4, via board pin 22, whereas the emitter of 1TR4 is returned to the negative output of D1 via pin 23, R29 and R21. The positive supply voltage for ML1 (V+) and also the collector voltage (VC) for the internal series pass transistor are taken from D1 via R1. The output from the reference amplifier (V REF) is applied via R5 to the non-inverting input of the error amplifier whilst the inverting input is connected to the -7 V regulated output via a potential divider R20, R13, preset voltage adjust potentiometer R12 and R11. Current feedback is provided by R29, R21 and 1R4.

+5 V Regulator

142. Bridge rectifier 1D2 is fed from a 9.8 V secondary winding of transformer 1T3. The positive output from D2 is applied to the collector of 1TR1 via board pin 6 and also to the collector of TR3. The positive supply voltage for ML4 (V+) and also the collector voltage (VC) of the internal series pass transistor are taken from the +20 V regulated supply. The reference voltage level applied to the non-inverting input of the error amplifier is preset by the potentiometer, R9, and the inverting input is taken from the 5 V output via R16. Current feedback is provided by R17, R26 and 1R1.

+12 V Regulator

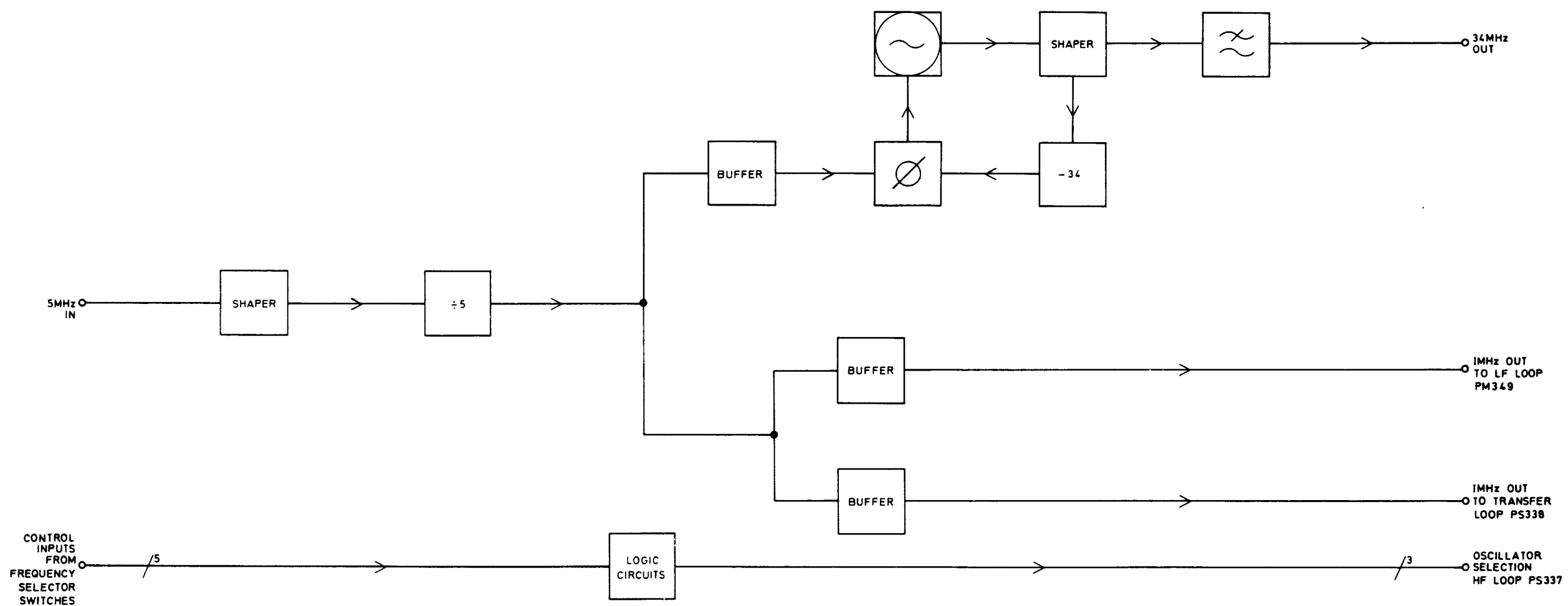
143. This supply is derived from a 16.3 V secondary winding of transformer 1T3. The positive output from the bridge rectifier, 1D3, is applied to the collector of 1TR2 via board pin 12 and also to the collector of TR2. The positive supply voltage for ML3 and the collector voltage for the internal series pass transistor are taken from the -20 V regulated supply. The reference voltage is applied via R7 to the non-inverting input of the error amplifier whilst potentiometer R23 presets the voltage level applied to the inverting input. The regulated +12 V output is taken to board pins 9 and 8, and current feedback is provided by R19, R25 and 1R2.

+20 V Regulator

144. This stage, which is similar to the +12 V regulator, is fed from a 25 V secondary winding of 1T3 and bridge rectifier 1D1. The regulated output is preset by potentiometer R22. Current feedback is provided by R18, R24 and 1R3.

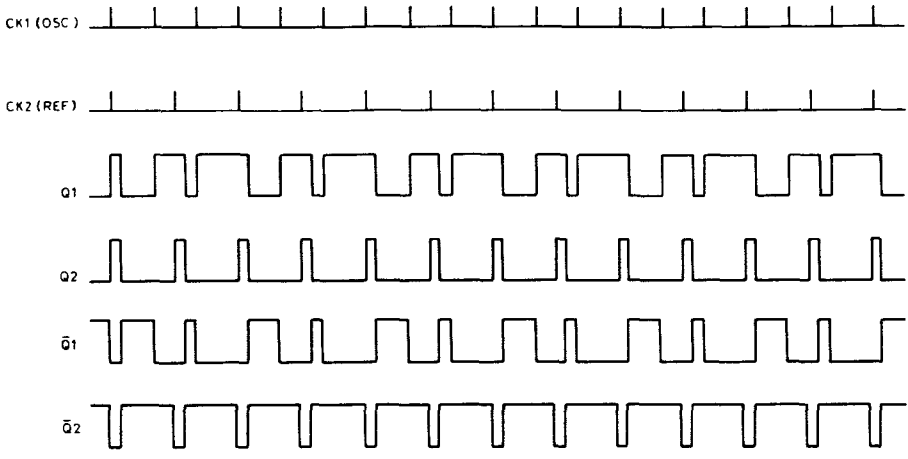
RTTY MODIFICATION KIT

145. On units built from the beginning of 1988 a replacement circuit for the obsolete TR13 of the RTTY Generator Board is included (Fig. 13A). This circuit, mounted on a supplementary board, functions in an identical manner to that described in para. 108.

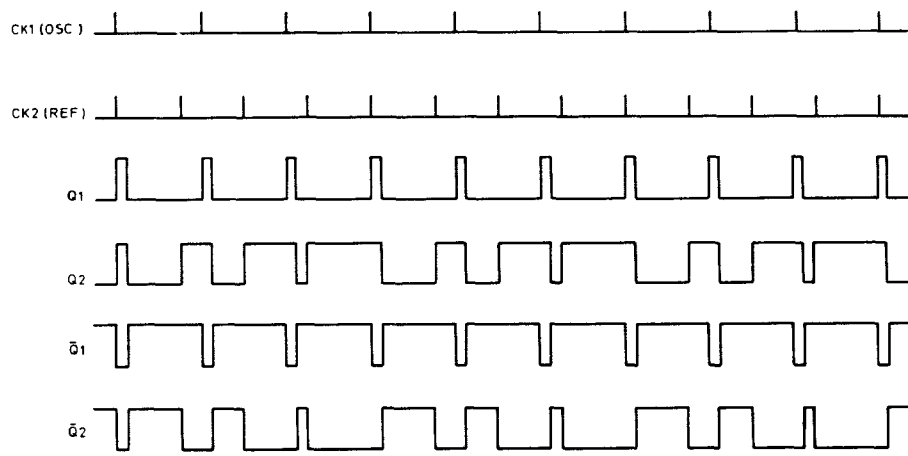


Block Diagram  
 34MHz Generator Board  
 PM344

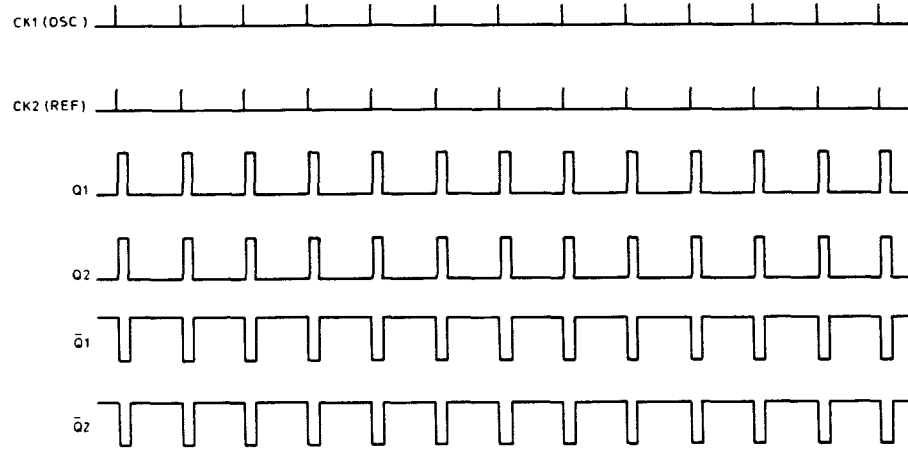
Fig 4-1



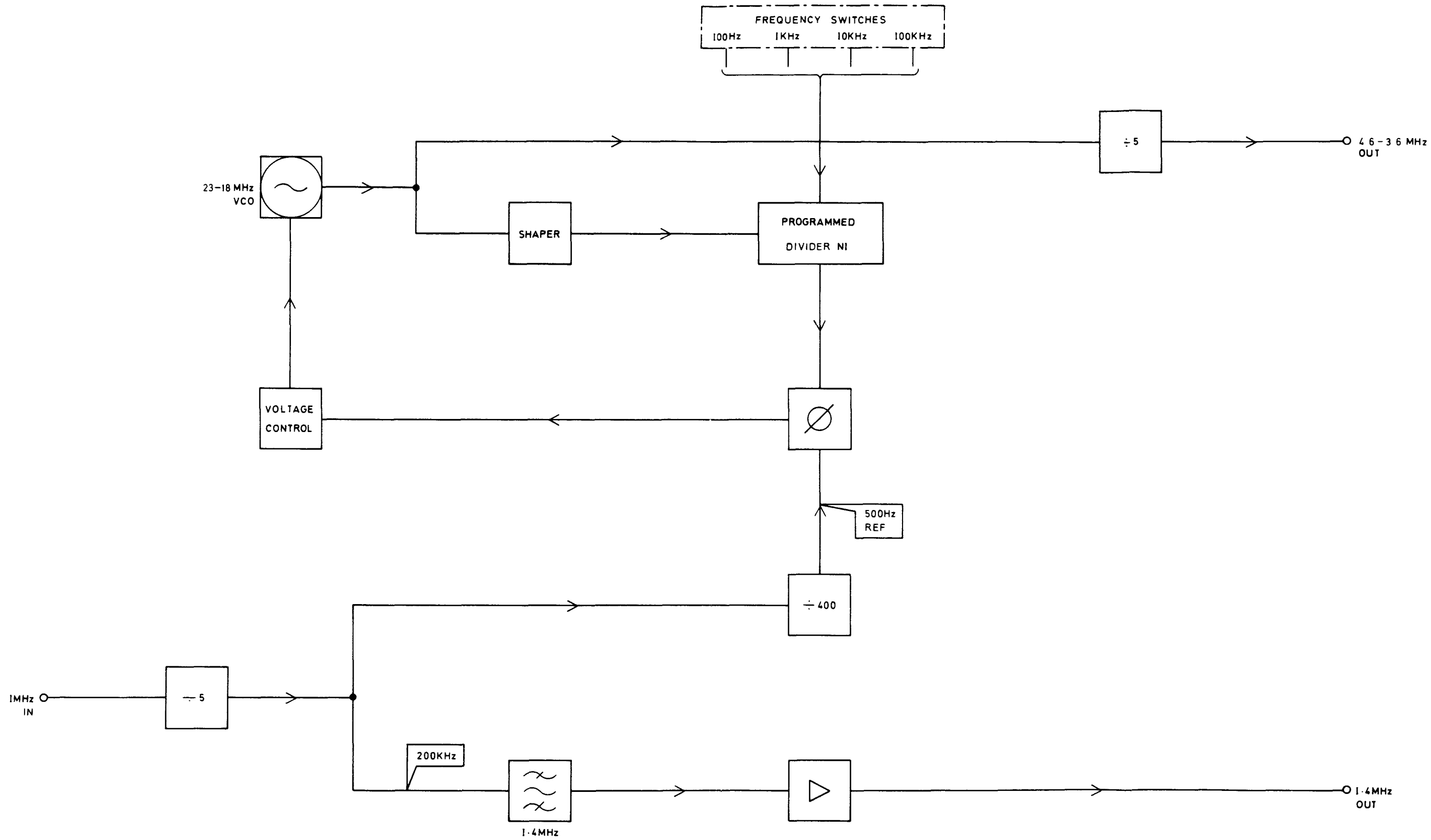
OSCILLATOR LEADING (FREQUENCY HIGH)



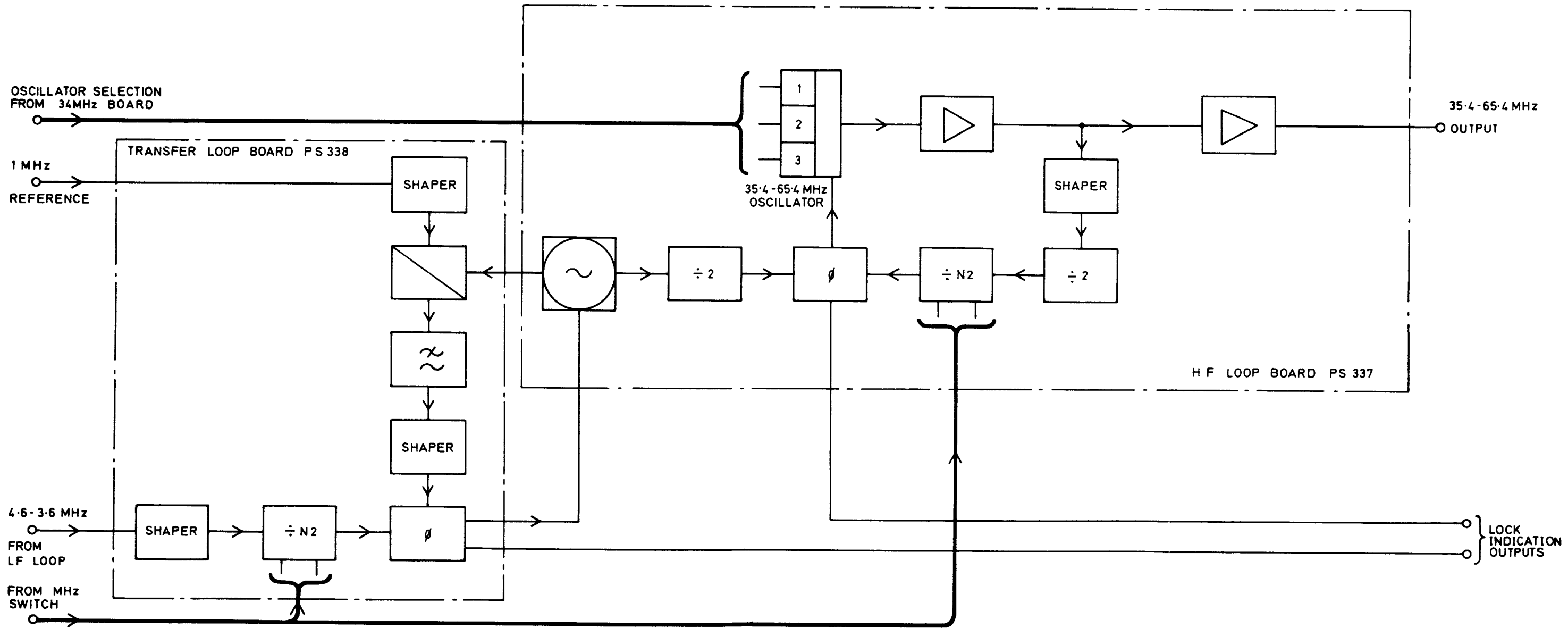
OSCILLATOR LAGGING (FREQUENCY LOW)

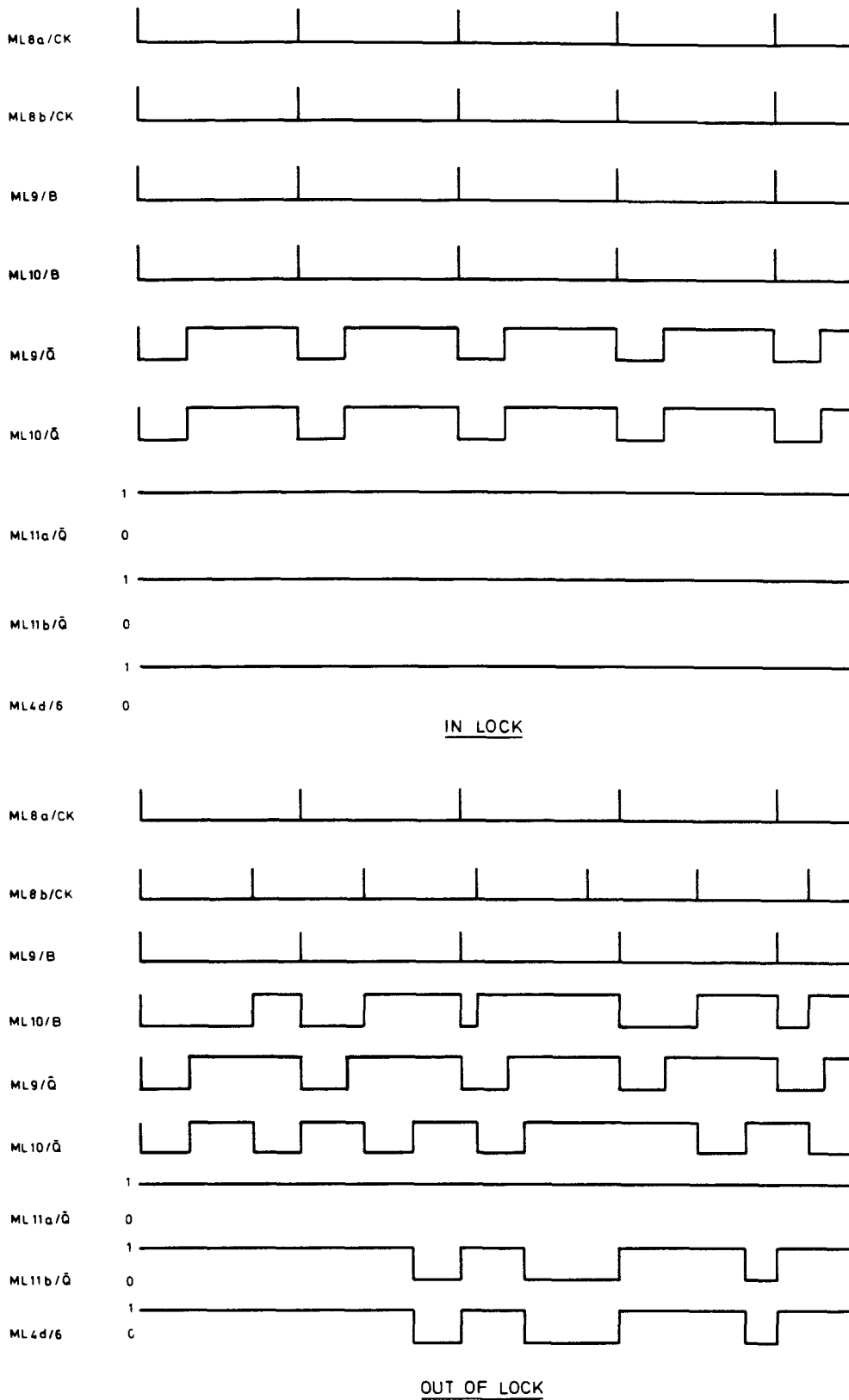


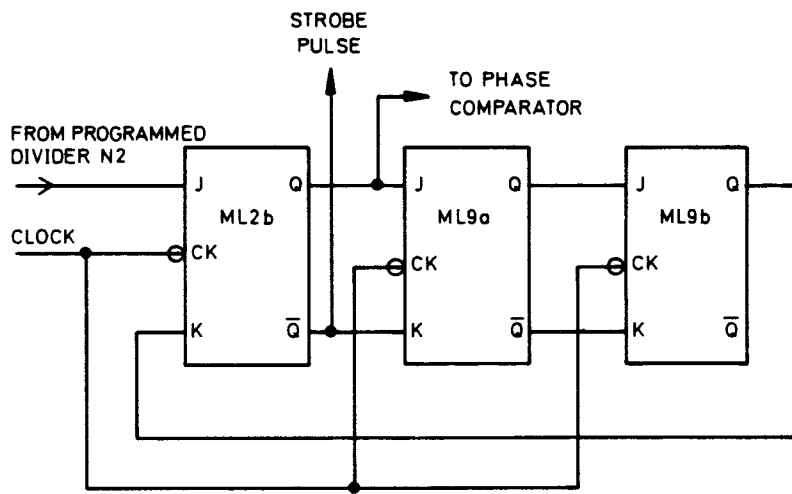
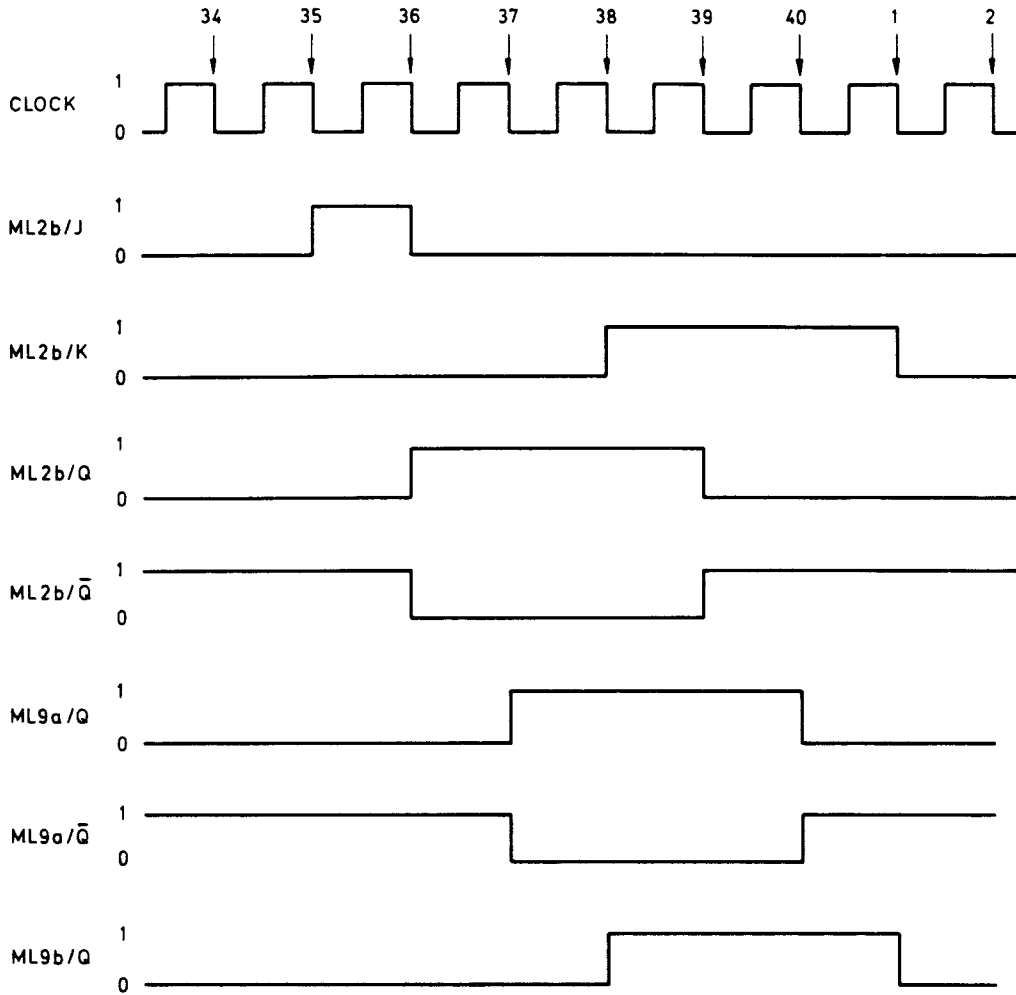
OSCILLATOR AND REFERENCE IN PHASE



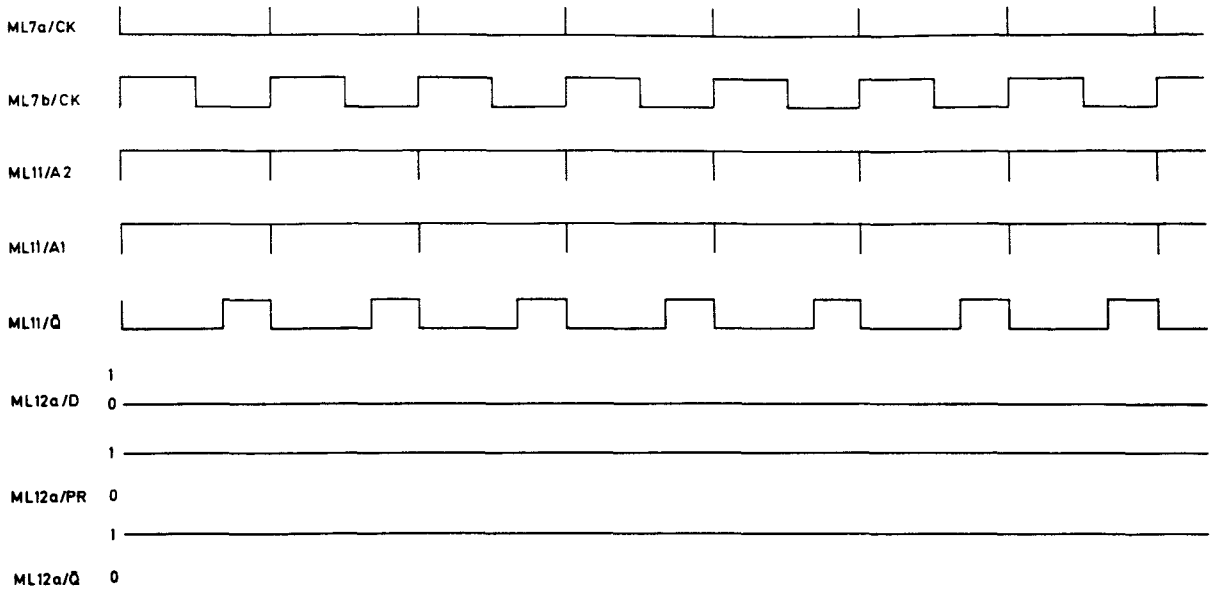
Simplified  
Block Diagram  
LF Loop PM 349 Fig 4.4



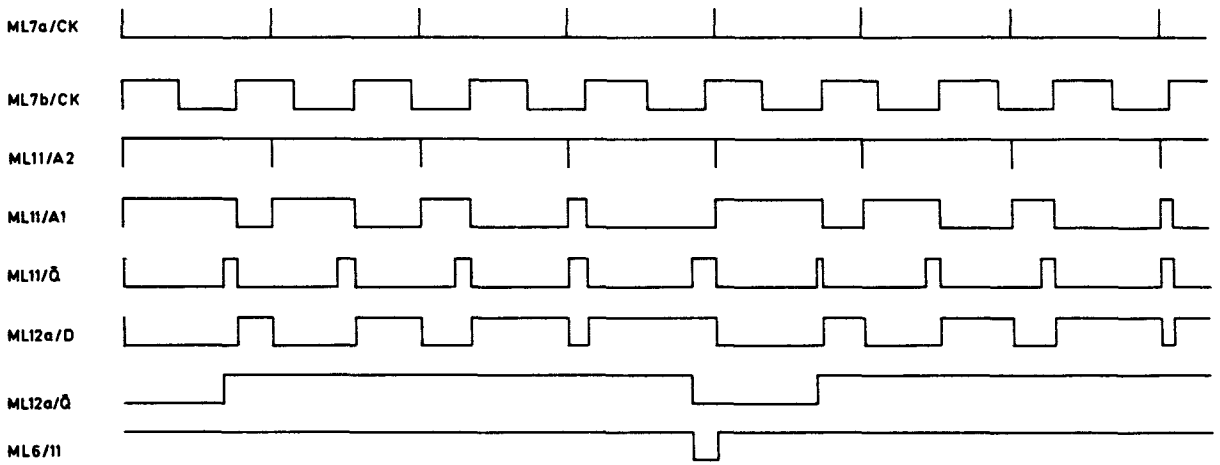




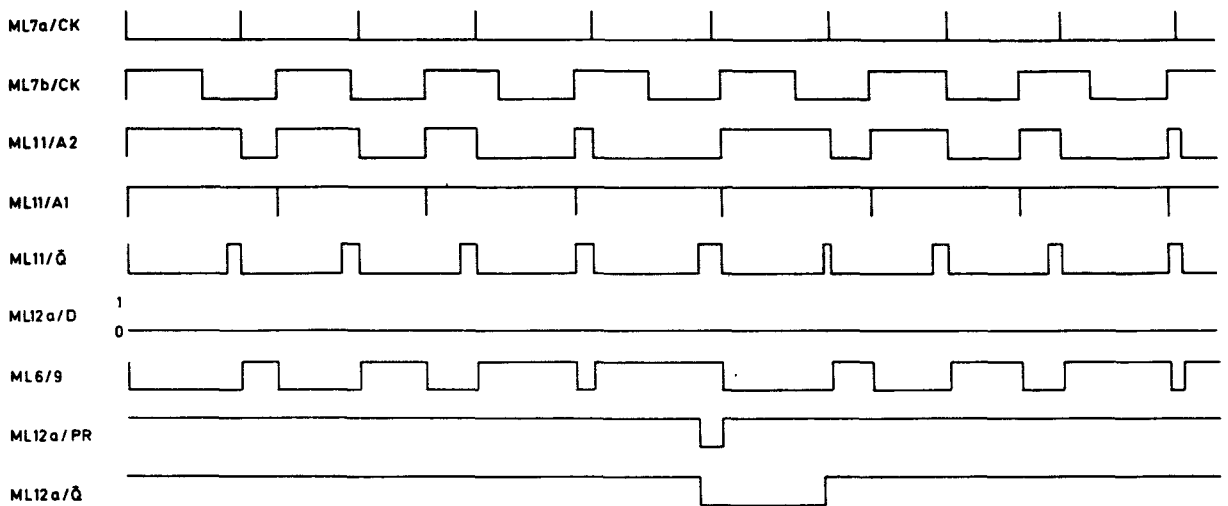
TRUTH TABLE (Each Section)		
t <sub>n</sub>		t <sub>n+1</sub>
J	K	Q
0	0	Q <sub>n</sub>
0	1	0
1	0	1
1	1	Q̄ <sub>n</sub>



IN LOCK



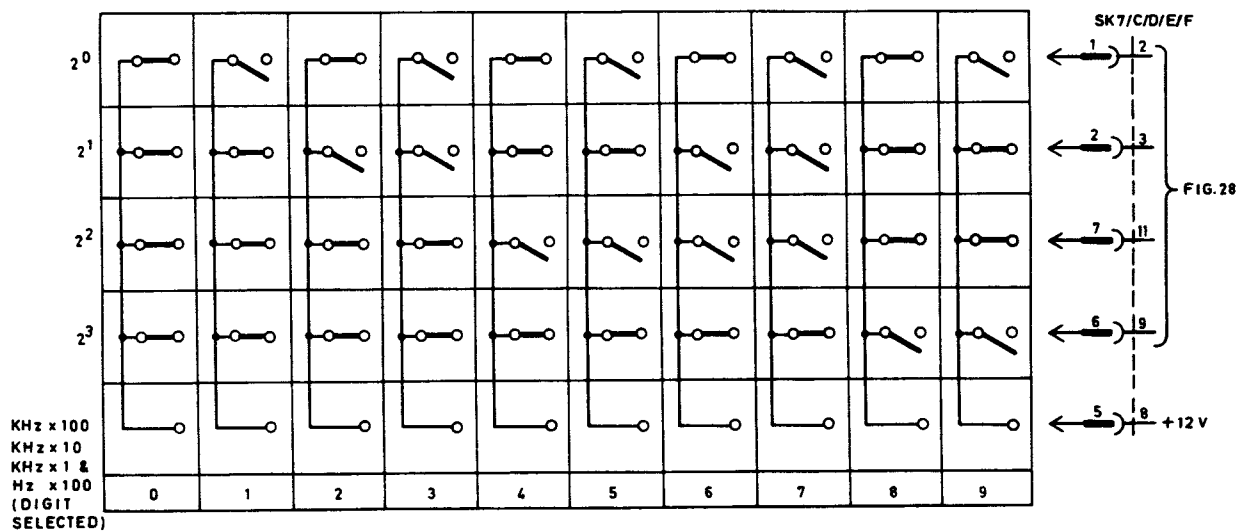
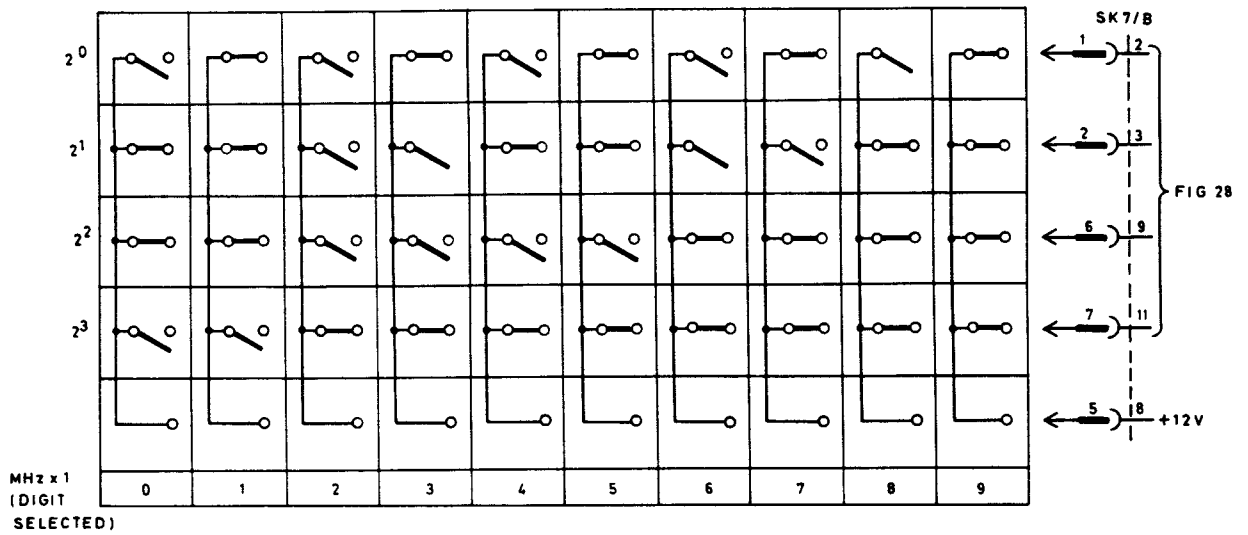
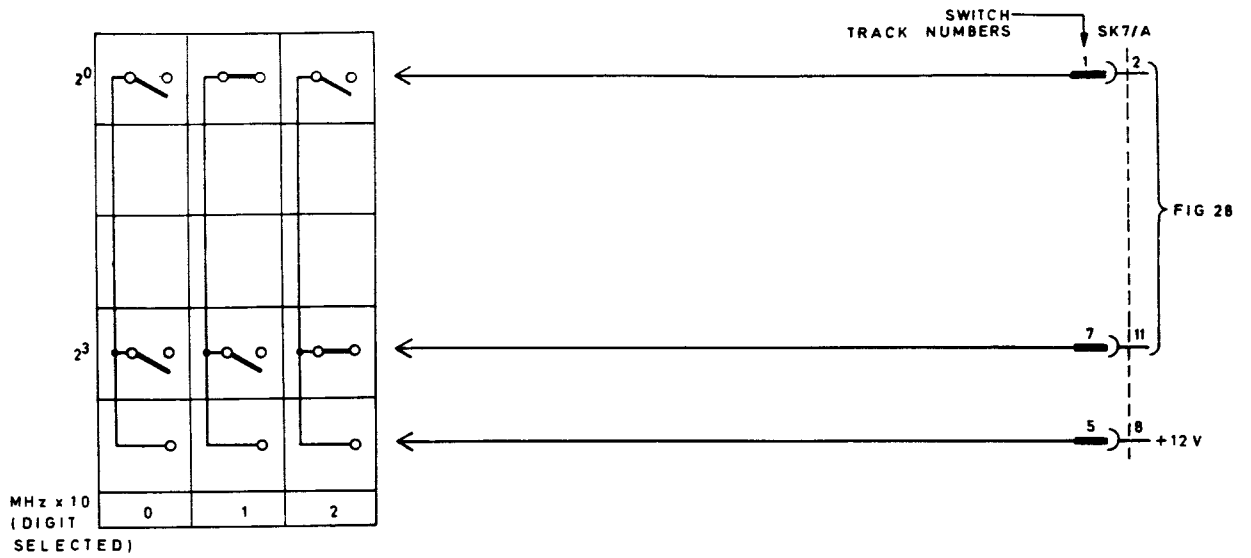
OUT OF LOCK (PROGRAMMED DIVIDER FREQUENCY LOW)



OUT OF LOCK (PROGRAMMED DIVIDER FREQUENCY HIGH)

Timing Diagram : Fast Lock and Indicator  
HF Loop PS337





Frequency Selection Switch Diagram

Fig.4-9

CHAPTER 5MAINTENANCE AND FAULT LOCATIONCONTENTS

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CHAPTER 5MAINTENANCE AND FAULT LOCATIONINTRODUCTION

1. This chapter contains the setting-up procedures for the drive unit together with information to assist in the location of a fault.

Test Equipment

2. The items of test equipment listed below are required for the following procedures and tests.

(1) Audio Signal Generator (Two Tone)

Example: Marconi Type 2005R

(2) Multimeter

20,000 ohms per volt

Example: AVO 8 or 9

(3) Digital Frequency Meter

Frequency Range: 900 kHz to 70 MHz

Example: Racal Type 9022

(4) Electronic Voltmeter

Voltage Range: 100 mV to 30 V

Example: Airmec Type 301A or Farnell Type TM6 with Probe to Type N Adaptor, 50 ohm Terminated (Type TM6/4).

(5) Oscilloscope, Dual Beam with delayed time base facility.

Bandwidth: 65 MHz or better.

Sensitivity: 100 mV/cm with high impedance probe.

Example: Tektronix 454

(6) Spectrum Analyzer, 0 - 100 MHz

Example: Hewlett Packard  
141T Display Section  
8552 IF Section  
8553 RF Section

MAINTENANCE

Note: When operating the MA1720 as an independent unit it is necessary to terminate the output with a 50 ohm load and to link pin 9 to pin 3 on socket SK6.

Setting-up Regulator Board PM372

3. Use the multimeter to measure the supplies at TB2; adjustment of a supply is by the associated potentiometer on the regulator board.

TB2	Supply	Adjustment
1 & 2	-7 V $\pm$ 0.25 V	R12
3 & 4	+5 V $\pm$ 0.25 V	R9
5 & 6	+12 V $\pm$ 0.5 V	R33
7 & 8	+20 V $\pm$ 0.5 V	R22

LF Loop Board PM349

4. Set the front panel frequency selector switches to 000000 MHz and adjust L2 on the LF Loop Board PM349 to obtain a reading of +15 V d.c. at TP5. Set the front panel frequency selector switches to 29.9999 MHz and check that the voltage at TP5 is now 3.5 V d.c.

HF Loop Board PS337

5. Connect the oscilloscope to TP4 and adjust R38 to obtain a reading of 3 V p-p.

6. Use the electronic volmeter to measure the level at board pin 22 and adjust R44 to obtain a reading of 225 mV (0 dBm into 50 ohms).

7. Set the front panel frequency switches to 29.9999 MHz and adjust L20 to obtain a reading of +8 V d.c. at board pin 18.

8. Set the front panel frequency switches to 6.9999 MHz and adjust L4 to obtain a reading of +14 V d.c. at the collector of TR19.

9. Set the front panel frequency switches to 17.9999 MHz and adjust L5 to obtain a reading of +14 V d.c. at the collector of TR19.

10. Set the front panel frequency switches to 29.9999 MHz and adjust L6 to obtain a reading of +14 V d.c. at the collector of TR19.

Setting-up Mode Levels

NOTE: The following procedure sets the drive unit RF output level to 200 mW. For systems which require a lower level of RF drive, this procedure should be carried out before finally setting the level to that required. Refer to the relevant system manual or appendix for instructions.

11. (1) Set the frequency to 10 MHz, the MODE switch to AM-6, CONTROL to LOCAL SYNTH, TUNE/MUTE/OPERATE to OPERATE HIGH, UPPER sideband, VOX/PTT/Tx to Tx, and depress the RESET push button. Connect the Electronic volmeter to SK4 and adjust T6 on the Low Level Board for maximum output.
- (2) Adjust inductor L2, L3, L4, L6 and L7 on the Mixer and Output Board for maximum output and adjust R70 on the Mixer and Output Board for an output voltage of 1.6 V r.m.s.
- (3) Set the front panel METER switch to RF and adjust R64 on Mixer and Output Board to obtain a reading of -6 dB on the front panel meter.
- (4) Set the MODE switch to SSB-16 and check that the output level falls by 10 dB  $\pm$  1 dB to that obtained in (3).
- (5) Set the MODE switch to SSB-26 and check that the output level falls by 20 dB  $\pm$  1 dB to that obtained in (3).
- (6) Set the MODE switch to SSB SUPP and use the Audio Signal Generator to insert a signal of 0 dBm into 600 ohms at a frequency of 1 kHz into LINE 1 socket on the front panel. Turn the SET LINE potentiometer on the front panel fully counter-clockwise.
- (7) Set the METER switch to LINE 1 and adjust R195 on the Low Level Board to obtain a reading of 0 dBm on the front panel meter.
- (8) Decrease the output of the Audio Signal Generator by 10 dB and ensure that the front panel meter reading falls by 10 dB  $\pm$  0.5 dB. Increase the output of the Audio Signal Generator to 0 dB.
- (9) Set the METER switch to SET 1 and adjust the SET Line 1 potentiometer to obtain a reading of 0 dB on the front panel meter (with an audio input).
- (10) Set the METER switch to RF and increase the output of the Audio Signal Generator by 10 dB. Adjust R73 on the Low Level Board to obtain a reading of 200 mW on the front panel meter.
- (11) Alternate the setting of the SIDEBAND switch between UPPER and LOWER and adjust in turn potentiometers R175 and R176 on the Low Level Board to obtain equal output levels of 200 mW for each sideband.
- (12) Decrease the output of the Audio Signal Generator by 20 dB and check that the output level does not fall by more than 1.5 dB.
- (13) Set the VOX/PTT/Tx switch to VOX and adjust R79 on the Low Level Board fully anti-clockwise, and check that the output of the MA1720 is muted after approximately 2 seconds. Adjust R79 clockwise until the MA1720 de-mutes.

NOTE: For speech input the clockwise setting of R79 may have to be increased.

- (14) Set the Audio Signal Generator output to 0 dB, set the MODE switch to ISB-26 and the VOX/PTT/Tx switch to Tx. Check that the output level falls by 6 dB.
- (15) Insert the audio signal into Line 2 jack socket, set the METER switch to LINE 2 and check that the front panel meter reads 0 dBm.
- (16) Set the METER switch to SET 2 and adjust the SET LINE 2 potentiometer clockwise until the front panel meter reads 0 dBm.
- (17) Set the MODE switch to ISB-26 and the METER switch to RF. Increase the audio output by 10 dB and adjust R75 on the Low Level Board to obtain a reading of -6 dB relative to the 200 mW setting on the front panel meter.

#### Setting-up Tone Oscillator

- 12. (1) Set the TUNE/MUTE/OPERATE switch to OPERATE HIGH.
- (2) Set the MODE switch to CW.
- (3) Set the VOX/PTT/Tx switch to Tx.
- (4) Set the FREQUENCY switches to 2 MHz and press the RESET push button.
- (5) Insert the Key into a front panel jack and earth the Key line (Key down condition).
- (6) In the Key down condition adjust R65 on the Low Level Board to obtain a reading of 200 mW on the front panel meter.
- (7) Use the Frequency Meter to measure the output frequency at socket SK4 on the rear panel. The frequency should be 1.999 MHz in the Key down condition. If necessary, adjust transformer T1 on the Low Level Board.

#### Setting-Up RTTY Facility

- 13. (1) Set the MODE switch to RTTY TEST and the SIDEBAND switch to UPPER.
- (2) Remove link LK3 on the RTTY Generator Board and use the Frequency Meter to measure the output at socket SK4 on the rear panel. The measured frequency should be 2.0020 MHz; if not adjust R27 on the RTTY Generator Board.
- (3) Replace link LK3 in the A-B position on the RTTY Generator Board.

- (4) The required frequency shift is given by adjustment of R20. For example, if a shift of  $\pm 425$  Hz is required, adjust R20 until a reading of 2.002425 MHz is obtained on the Frequency Meter. Rotate the MODE switch to the RTTY position, a reading of 2.001575 MHz should be obtained. The above adjustment will give a total shift of 850 Hz.
- (5) Remove the Frequency Meter from socket SK4 and replace with a  $50\Omega$  1 watt load. Select, in turn, RTTY USB, RTTY LSB, RTTY TEST USB and RTTY TEST LSB. Note the power output level, as indicated on the front panel meter, for each position, and set to that position which indicates the highest output level.
- (6) Adjust R36 on the RTTY Generator Board for a front panel meter indication of 200 mW.

#### Tune Level

14. Set the TUNE/MUTE/OPERATE switch to TUNE and adjust R204 on the Low Level Board for the required tune level (see relevant System Manual or Appendix).

#### Mixer Drive Level

15. (1) Set the MA1720 operating frequency to 29 MHz. Set the TUNE/MUTE/OPERATE switch to OPERATE HIGH and connect the Electronic Voltmeter to pins 8 and 9 (earth) on the Mixer and Output Board.
- (2) Adjust R44 on the HF Loop Board PS337 to obtain a reading of  $224 \text{ mV} \pm 10 \text{ mV r.m.s.}$  on the Electronic Voltmeter.

#### Final RF Output Level

16. The RF output level is now set to 200 mW. For systems which require a lower level of RF drive, refer to the relevant System Manual or Appendix for instructions.

### FAULT LOCATION

#### Procedure

17. If a fault is suspected, first check that the front panel controls are correctly set for the mode of operation required, then check the setting of the INTERNAL/EXTERNAL Frequency Standard Selector switch on the rear panel.

#### Power Supplies

18. Check the supply voltages, using the front panel meter (Chap. 3 para. 8). If necessary adjust the appropriate potentiometer on the regulator board PM343 (para. 3). If any supplies are missing, use the multimeter to check the following voltages on the regulator board PM343.

Pin 17	+29 V $\pm$ 4 V d.c.
12	+18 V $\pm$ 2 V d.c.
6	+10 V $\pm$ 2 V d.c.
19	+14 V $\pm$ 2 V d.c.

### Mixer and Output Board PM342

19. Using the oscilloscope, check RF levels at the collectors of all transistors on the Mixer and Output Board. Using the electronic voltmeter, check d.c. levels at the emitters of all transistors on the board. Representative values are given below.

<u>Transistor</u>	<u>Emitter V d.c.</u>	<u>Collector V p-p</u>
TR13	5.8	16.0
TR12	5.6	7.5
TR11	2.8	4.0
TR10	2.6	1.6
TR9	2.6	0.8
TR15	8.0	0.3
TR6	3.2 )	15-20 at 35-60 MHz
TR5	4.0 )	
TR8	6.0	1.0
TR3	3.2 )	15-20 at 35.4 MHz
TR2	4.0 )	

20. Adjustment of Low Pass Filter - If misalignment is suspected (symptom - excessive breakthrough of 2nd local oscillator, 35.4 - 65.4 MHz), the following procedure should be adopted.

- (1) Monitor the RF output from the MA1720 on the spectrum analyzer.
- (2) Set the MODE SELECTOR switch to KEY suppressed, and ensure that the MA1720 is not muted and that the key is up.
- (3) Set the frequency switches to 02.0200 MHz. Press the RESET push button and adjust L9 on PM342 for minimum output at 37.42 MHz.
- (4) Set the frequency switches to 00.1000 MHz. Press the RESET push button and adjust L10 on PM342 for minimum output at 35.5 MHz.
- (5) Set the frequency switches to 08.7700 MHz. Press the RESET push button and adjust L11 on PM342 for minimum output at 44.17 MHz.
- (6) Set the frequency switches to 29.9999 MHz, and set the TUNE/MUTE/OPERATE switch to TUNE. Press the RESET push button and adjust L8 on PM342 for maximum output at 30 MHz.

21. Using the oscilloscope, check the 1.4 MHz input to the Mixer and Output Board PM342 at pin 4. The level should be 600 mV p-p approximately. If there is no signal at this point, check the Low Level Board as in the following paragraphs.



Low Level Board PM341

22. Select CW on the MODE switch. Using the oscilloscope, check pin 16 on the Low Level Board for the presence of a 1.4 MHz signal of approximately 600 mV p-p. If there is no signal, check the 1.4 MHz Generator on the LF Loop Board as detailed in para. 68.

23. If a signal is present at pin 16, check the signal at TP5 for approximately 620 mV p-p using the oscilloscope, then check the collectors of TR41 and TR42 using the oscilloscope. A squarewave of approximately 4 V p-p should be present.

24. Using the oscilloscope, check that a sinewave of approximately 1 V p-p is present at TR57 collector.

25. Select 'KEY supp' on the MODE switch and repeat the tests in paras. 22 and 23 for the same results.

26. Select 'KEY -6' on the MODE switch. Using the electronic voltmeter, check that the voltage at pin 45 is not less than +10 V d.c., and that +5.5 V d.c. is present at TR50 collector.

27. Select 'RTTY' on the MODE switch. Using the multimeter, check that +10 V d.c. is present at pin 21. Using the oscilloscope, check that a squarewave of 50 mV p-p at a frequency of approximately 2 kHz is present at pin 24.

28. Select any SSB mode on the MODE switch and test the following points for the results shown:

TR2 collector +15 V d.c. ) using the electronic  
TR3 collector -5.6 V d.c. ) voltmeter

Pin 38 300 mV p-p audio ) using the  
TR12 collector 10 mV p-p audio ) oscilloscope  
TP2 2.5 V p-p audio )

29. Select 'ISB' on the MODE switch and test the following points for the results shown:

Pin 29 +10 V d.c. ) using the electronic  
TR4 collector +15 V d.c. ) voltmeter  
TR5 collector -5.6 V d.c. )

Pin 32 300 mV p-p audio ) using the  
TR13 collector 10 mV p-p audio ) oscilloscope  
TP3 2.5 V p-p audio )

30. To check the meter circuit, test the following points for the results shown:

Pin 15 100 mV p-p audio ) using the  
TR64 collector 1.5 V p-p squarewave ) oscilloscope

RTTY Board PS568

31. To check the operation of the RTTY Board, carry out the following tests for the results shown:

<u>MODE Switch Setting</u>	<u>Test Point</u>	<u>Reading</u>	<u>Test Instrument</u>
RTTY Test	Pin 5	not less than +10 V d.c.)	Multimeter
RTTY	Pin 5	-4 V d.c. )	
RTTY Test	TR4 collector	+15 V to +20 V d.c. )	Electronic Voltmeter
RTTY	TR4 collector	0 V )	
RTTY Test	TR5 collector	0 V )	
RTTY	TR5 collector	+15 V to +20 V d.c. )	

32. Remove the link LK3 and check the tone oscillator by monitoring TP3 with the oscilloscope. A 2 kHz squarewave with an amplitude of approximately 4 V p-p should be displayed.

33. Select 'RTTY Test' on the MODE switch. Monitor TP3 with the oscilloscope, insert link LK3 in position A-C and check that the oscillator frequency increases above 2 kHz. Change the link to position A-B and check that the oscillator frequency falls below 2 kHz.

Control Board PM345

34. (1) Connect the multimeter between pin 30 (positive lead) and pin 22 (negative lead). Operate the RESET push button and hold in position; the multimeter should indicate +12 V d.c.
- (2) If the front panel LOCK lamp is extinguished use the oscilloscope to monitor pins 25, 26 and 27; if the synthesizer is in the locked condition a constant +5 V d.c. will appear at each pin.
- (3) If the synthesizer is locked i.e. +5 V d.c. is present at pins 25, 26 and 27, use the multimeter to check for 0 V on pin 3 and +12 V on pin 31 of the Control Board.
- (4) Set the TUNE/MUTE/OPERATE switch to MUTE and use the multimeter to check for 0 V on pin 5.
- (5) Select CW Keyed on the MODE SELECTOR and check for approx. +10 V d.c. at pin 5.
- (6) Set the VOX/PTT/Tx switch to Tx and check for approx. +10 V d.c. at pin 5.
- (7) Set the TUNE/MUTE/OPERATE switch to TUNE and check for approx. +10 V d.c. at pin 5.
- (8) Depress the STANDBY push button and check for 0 V at pin 14.
- (9) Depress the EHT READY push button and check for 0 V at pin 16.

- (10) Apply in turn the inputs shown below to the pins indicated. Connect the negative lead of the multimeter to pin 22 and use the positive lead to monitor the output pins shown. Check that the specified voltages  $\pm 0.5$  V are indicated.

<u>Apply Input to Pin</u>		<u>Monitor Output from Pin</u>	
Earth	1	0 V	4
		+12V	32
		0 V	5
+12 V	6	0 V	7
		+12 V	33
Earth	8	0 V	10
		+12 V	34
		+12 V	12

#### Noise Immunity Board PM346

35. If the output frequency of the MA1720 is incorrect, a check should be made to ensure that the coding input and output logic levels at the noise immunity board are correct. The input logic levels to the board (from the frequency switches or the external frequency control lines via PL3) for any frequency may be found by reference to the following table.

		Switch setting (Decimal)									
		0	1	2	3	4	5	6	7	8	9
Binary	'1'	0	1	0	1	0	1	0	1	0	1
	'2'	0	0	1	1	0	0	1	1	0	0
	'4'	0	0	0	0	1	1	1	1	0	0
	'8'	0	0	0	0	0	0	0	0	1	1
Inverted Binary (100Hz, 1kHz, 10kHz, & 100kHz decades)	'1'	1	0	1	0	1	0	1	0	1	0
	'2'	1	1	0	0	1	1	0	0	1	1
	'4'	1	1	1	1	0	0	0	0	1	1
	'8'	1	1	1	1	1	1	1	1	1	0
Switch setting 9's complement (Decimal)		9	8	7	6	5	4	3	2	1	0
Inverted 9's complement Binary 1 MHz Decade	'1'	0	1	0	1	0	1	0	1	0	1
	'2'	1	1	0	0	1	1	0	0	1	1
	'4'	1	1	0	0	0	0	1	1	1	1
	'8'	0	0	1	1	1	1	1	1	1	1
Inverted 9's Complement Binary 10 MHz Decade	'1'	0	1	0							
	'2'	-	-	-							
	'4'	-	-	-							
	'8'	0	0	1							

NOTE: 1 = +12 V  
0 = open circuit

36. As will be seen from the circuit diagram (Fig. 17), the logic state at each output pin should be the inverted form of the input.

<u>Range</u>	<u>BCD Function</u>	<u>Input Pin</u>	<u>Output Pin</u>
100 Hz	1	8	7
	2	6	5
	4	4	3
	8	2	1
1 kHz	1	16	15
	2	14	13
	4	12	11
	8	10	9
10 kHz	1	24	23
	2	22	21
	4	20	19
	8	18	17
100 kHz	1	32	31
	2	30	29
	4	28	27
	8	26	25
1 MHz	1	40	39
	2	38	37
	4	36	35
	8	34	33
10 MHz	1	48	47
	-	-	45) Inverse
	-	-	43) of 41
	8	42	41

#### 34 MHz Generator Board PM344

37. To check this board, monitor pin 8 with the oscilloscope and ensure that the 5 MHz input is present at a level of approximately 800 mV p-p. Transfer the oscilloscope to the following points in turn and check that the specified outputs are obtained.

<u>Test Point</u>	<u>Output</u>
Pin 10	1 MHz squarewave, 1 V p-p
Pin 12	1 MHz squarewave, 4 V p-p
TR4 collector	34 MHz sinewave, more than 500 mV p-p
ML1 pin 6	34 MHz sinewave, 4 V p-p
ML2 pin 8 )	1 MHz squarewave, 4 V p-p
ML4 pin 8 )	
ML6 pin 6	-ve spikes of 4 V at 1 MHz

38. Monitor the voltage at board pin 2 with the multimeter, and check that the level is +4 V d.c. Adjust L1 if necessary.

HF Loop Board PS337

39. Set the MHz switch on the front panel to the following ranges and check that the correct oscillator is selected by monitoring the pins on the board.

<u>MHz Range</u>	<u>Pin No.</u>	<u>Reading</u>
0-7 MHz	28	0 V
8-17 MHz	27	0 V
18-29 MHz	26	0 V

40. Check that the selected oscillator is operating by using the oscilloscope to measure a 3 V p-p signal at TP4.

41. Check the shaping circuit, TR11 and TR12, by using the oscilloscope to check the signal at the collector of TR12. The squarewave signal should have an excursion from 0.4 V to at least +3 V p-p.

42. Use the oscilloscope to check the divide-by-two circuit ML2, by monitoring the input at the collector of TR12 and the output at TP5.

43. Use the oscilloscope to check the strobe pulse at TP6. The negative going pulse should be of 90 ns to 180 ns duration with a p.r.f. of approximately 400 kHz.

44. Use the delayed time base facility on the oscilloscope to check the divider ratio. Trigger the oscilloscope from TP6 and count the number of input pulses to produce one output pulse.

45. Use the oscilloscope to check the operation of the Transfer Oscillator at TP12. The squarewave pulse should have an excursion from 0.4 V to at least +3 V p-p.

46. Use the oscilloscope to check the phase comparator outputs. Negative going pulses of 30 ns duration should be obtained at TP7 and TP8 when the loop is locked. When the loop is out of lock, one test point should have the negative going 30 ns pulse whilst the other should have a pulse of cyclically varying width.

47. Use the multimeter to check the d.c. voltage at the collector of TR19. When the loop is locked the voltage should be between +3 and +14 V d.c. When TP7 has the pulse of cyclically varying width the voltage should be approximately +2.3 V d.c. When TP8 has the pulse of cyclically varying width the voltage should be approximately +19 V d.c.

48. Use the oscilloscope to check the lock indicator. When the loop is locked TP11 should have negative going pulses of 1.5 microsecond duration at a p.r.f. of approximately 400 kHz. When the loop is out of lock the pulse of cyclically varying width at TP7 or TP8 should also appear at TP12 except during the period of the negative going 1.5 microsecond pulse at TP11.

Transfer Board PS338

**NOTE:** The following checks on the Transfer Board should be carried out when the Board is used in conjunction with the oscillator on the HF Loop Board.

49. Use the oscilloscope to check the voltage at the collector of TR2 which is produced from the 1 MHz frequency standard input. The voltage level should be approximately 300 mV p-p.
50. Use the oscilloscope to check the signal at the collector of TR3 which is produced from the Transfer Oscillator input. The signal level should be approximately 1 V p-p in the frequency range 885-948 kHz.
51. Use the oscilloscope to check the mixer output at the collector of TR6. The signal should have an excursion from +0.4 V to at least +3 V p-p.
52. Use the oscilloscope to check the signal at TP1 which should have an excursion from +0.4 V to at least +3 V p-p.
53. Use the oscilloscope to check the signal at TP6 which should be a negative going pulse with an excursion from +0.4 V to at least +3 V p-p, with a duration of approximately 250-300 ns.
54. Use the delayed time base facility on the oscilloscope to check the divider ratio by triggering the oscilloscope from TP9 and counting the number of input pulses to produce one output pulse.
55. Use the oscilloscope to check for negative going pulses of 30 ns duration at TP3 and pin 6 of ML8 in the locked condition. In the out of lock condition either TP3 or pin 6 of ML8 will have negative going pulses of 30 ns duration whilst the other will have negative going pulses of cyclically varying widths.
56. Use the multimeter to check the d.c. voltage at TR10 collector. In the locked condition this should be in the range +3 V to +8 V d.c. When pin 6 of ML8 has a pulse of cyclically varying width this voltage should be approximately +11 V d.c. (out of lock condition).
57. Use the oscilloscope to check the lock indicator. In the locked condition the signals at TP4 and TP5 should be negative going pulses with an excursion of +3 V to 0.4 V with a duration of 1.5 microseconds.
58. In the out of lock condition the pulse of cyclically varying width at TP3 or pin 6 of ML8 should also appear at pin 6 of the Transfer Board except during the period of the negative going 1.5 microsecond pulse at TP4 and TP5.

#### LF Loop Board PM349

59. Use the multimeter to check the oscillator supply; the voltage at the emitter of transistor TR1 should measure +5 V d.c.  $\pm$  0.25 V.
60. Use the oscilloscope to check the oscillator output at TP1. A TTL squarewave signal in the frequency range 18-23 MHz should be obtained.
61. Use the oscilloscope to check the strobe pulse at TP4. The negative going pulses should have a duration of 80-100 ns.
62. Use the oscilloscope to check the strobe pulse at TP2. The positive going pulses should be of approximately 50 ns duration.

NOTE: If the positive going 50 ns pulses are not obtained at TP2, the input and output pins of ML5, ML8, ML13 and ML16 should be monitored to isolate the faulty package in the divider chain.

63. Use the oscilloscope to check the divide-by-five package ML2. The TTL signal at pin 2 of ML2 should be in the frequency range 3.6 - 4.6 MHz.

64. Transfer the oscilloscope to pin 12 of ML1 to check the buffer stage, gate G1 of ML1. The signal should be in the frequency range 3.6 - 4.6 MHz.

65. Use the oscilloscope to check the divide-by-2000 stage at TP3. The signal should be a squarewave at 500 Hz.

NOTE: If the 500 Hz squarewave is not obtained at TP3, the input and output pins of ML3, ML4, ML7 and ML10 should be monitored to isolate the faulty package in the divider chain.

66. Use the oscilloscope to check the phase comparator outputs. Positive going pulses of 50 ns duration should be obtained at the Q outputs (pins 5 and 9) of ML12(a) and ML12(b) when the loop is locked. In the out of lock condition pin 5 or pin 9 should have a positive going 50 ns pulse whilst the other pin should have a pulse of cyclically varying width.

67. Use the multimeter to check the supply to the Varactor Line Driver at the emitter of transistor TR10. The voltage should be +19.5 V d.c.  $\pm$  0.5 V.

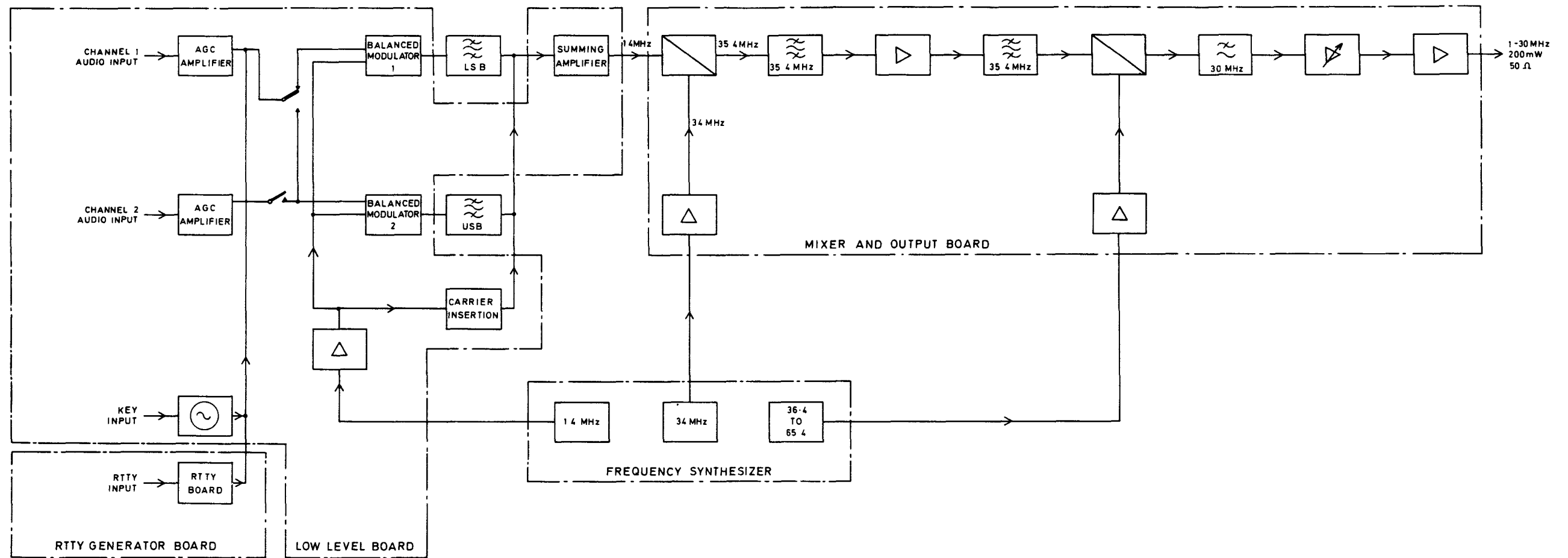
68. Transfer the multimeter to check the Varactor Line Driver at TP5. When the loop is locked the voltage should be between +3 V and +15 V d.c. depending on the frequency selected. When the Q output (pin 5) of ML12(a) has the pulse of cyclically varying width the voltage should be approximately +2 V d.c. When the Q output (pin 9) of ML12(b) has the pulse of cyclically varying width the voltage should be approximately +18 V d.c.

69. Use the oscilloscope to check the 1.4 MHz Generator. The signal at pin 9 of ML3 should be a squarewave with an excursion from 0.4 V to at least +3 V p-p.

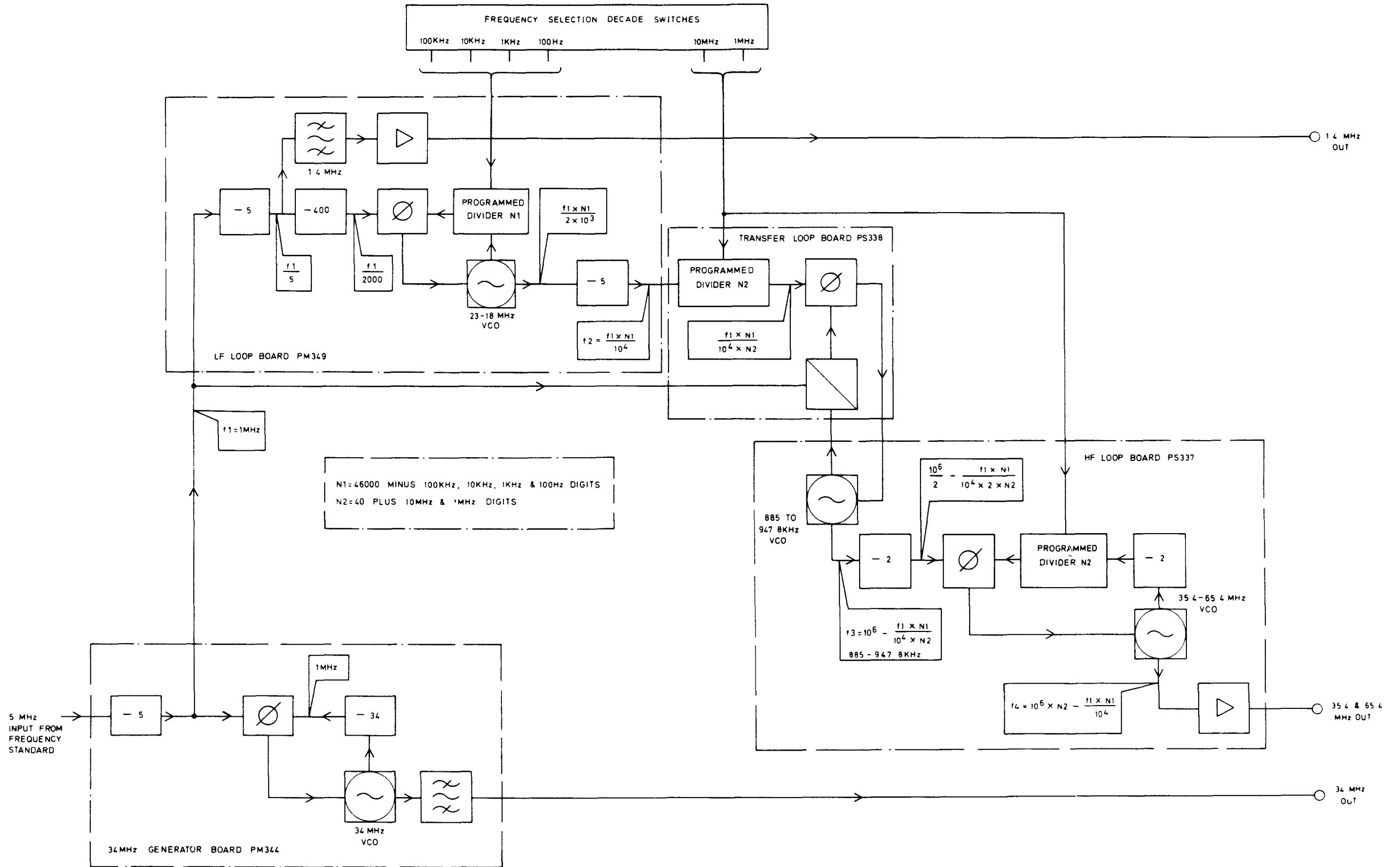
70. Transfer the oscilloscope to the base of TR3. A sine wave signal of approximately 500 mV peak-to-peak should be obtained.

71. Transfer the oscilloscope to board pins 1 and 2. The output of the 1.4 MHz Generator should be approximately 640 mV p-p when the generator is correctly terminated.

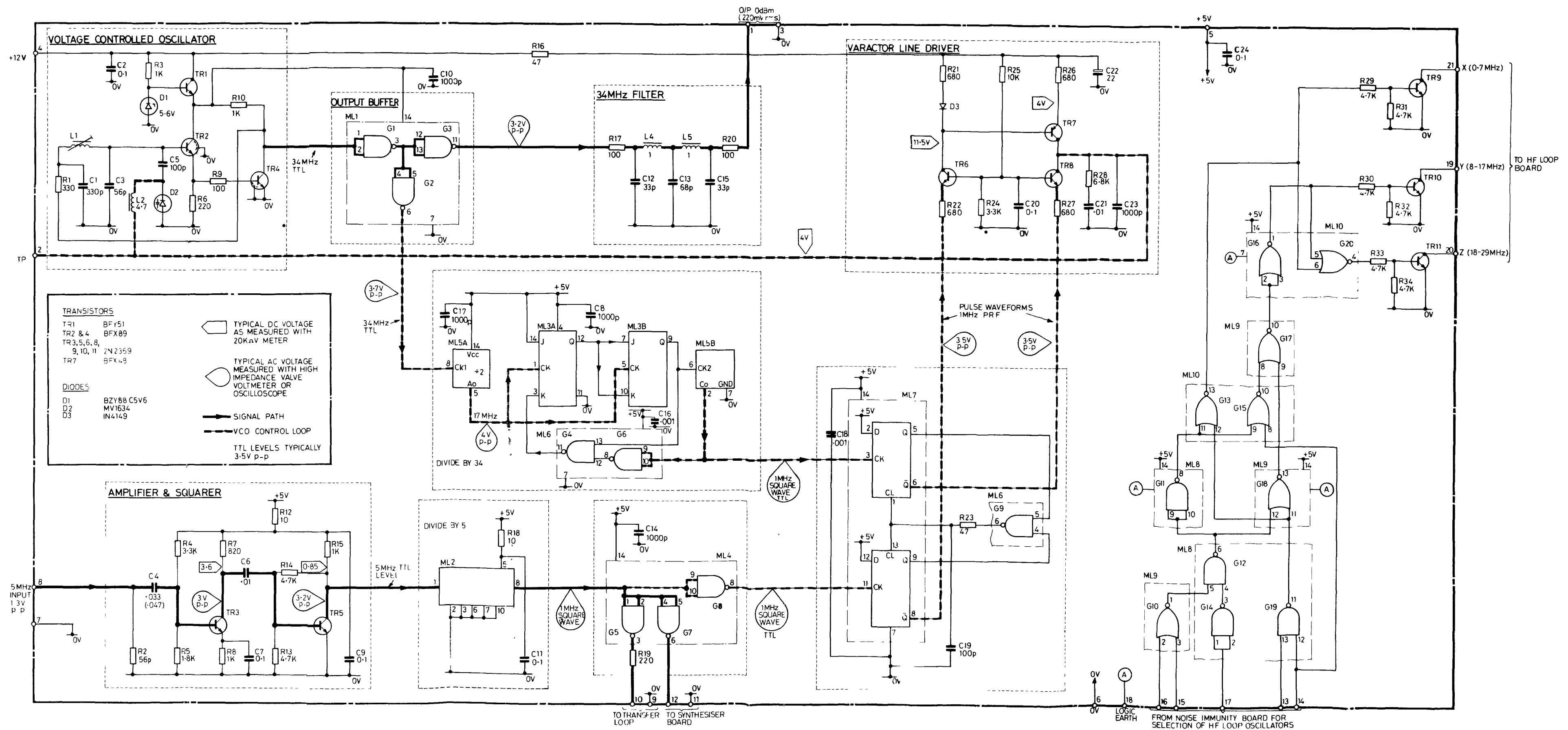


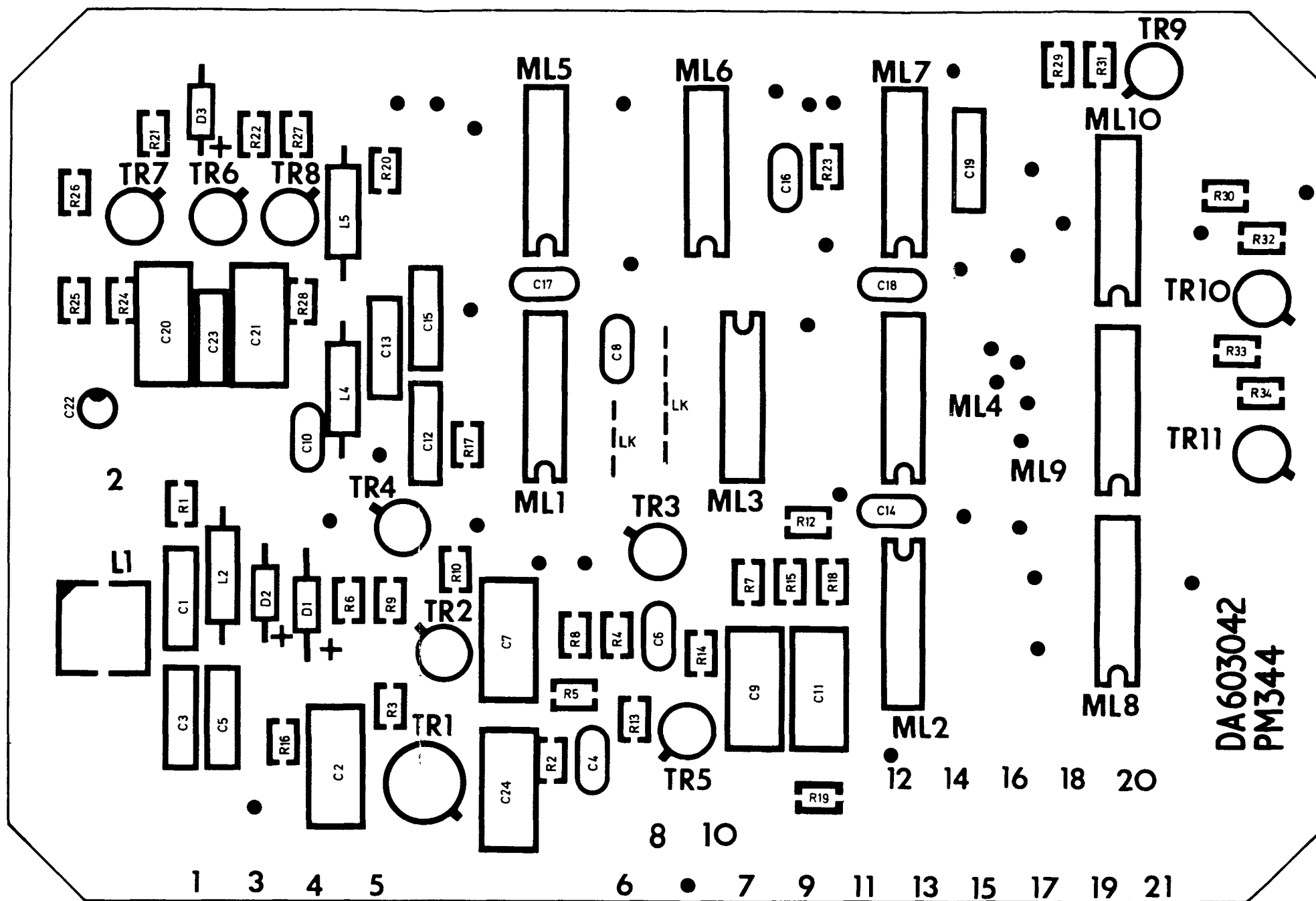


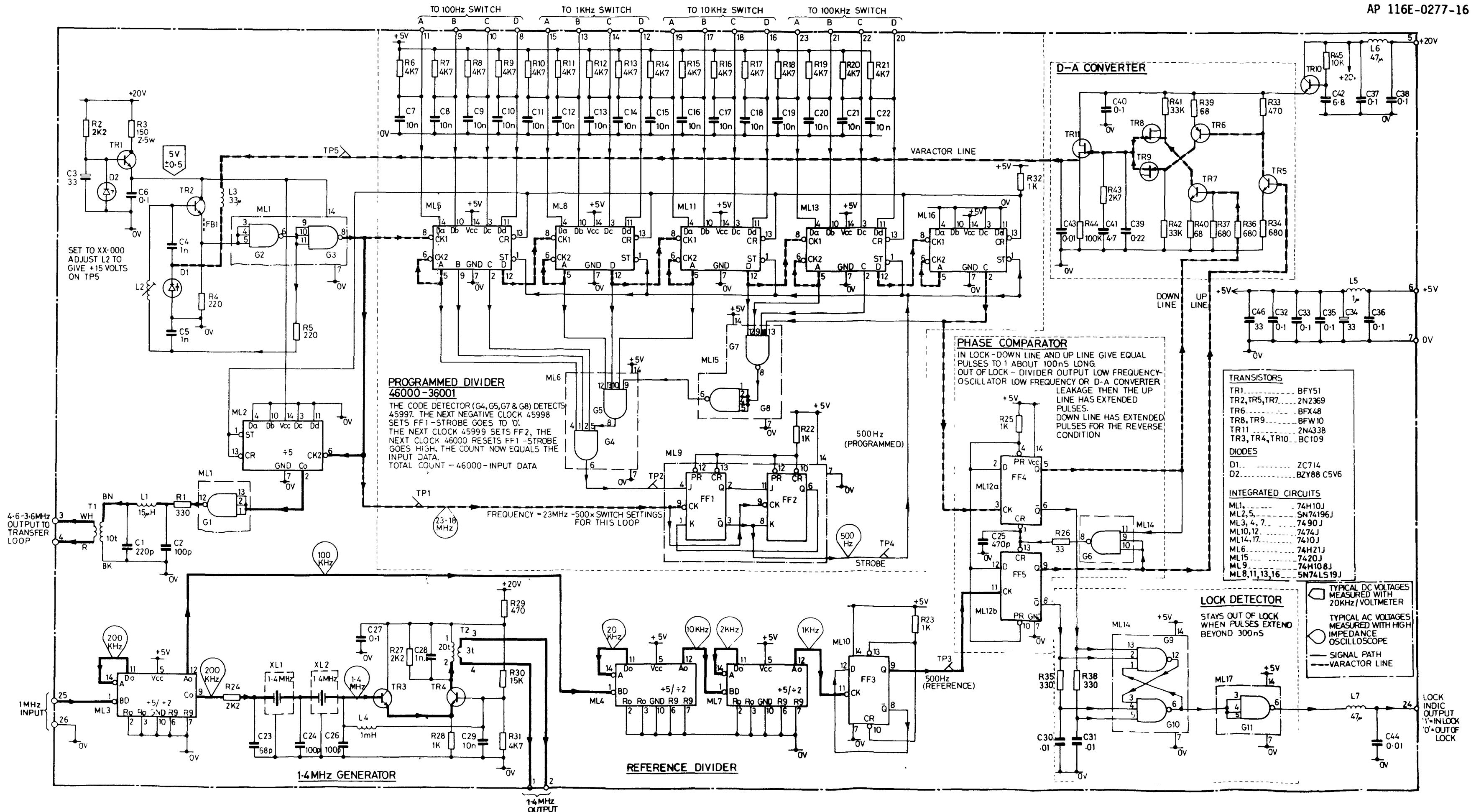
M.A.1720: Simplified Block Diagram

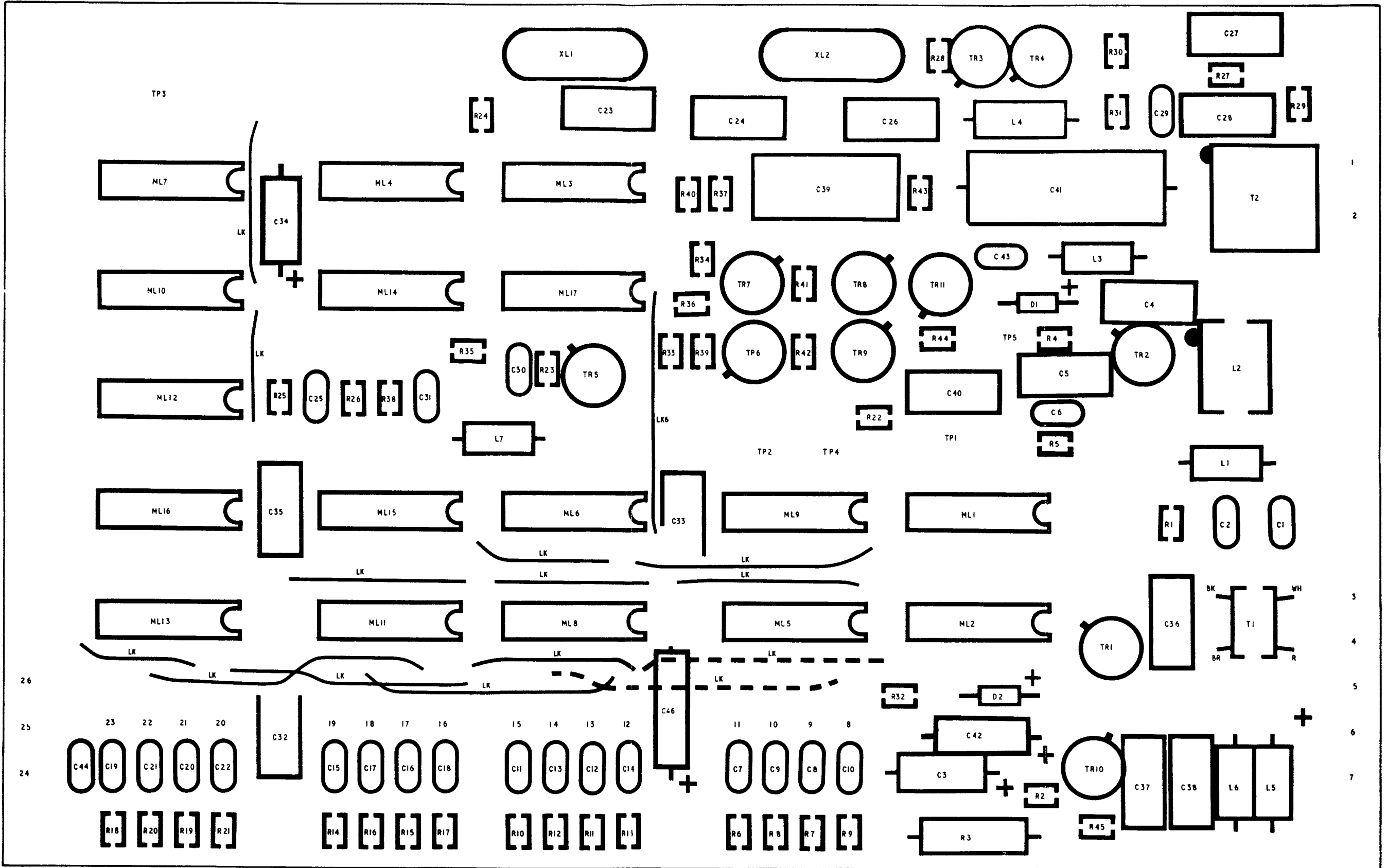


Simplified block diagram: frequency synthesizer



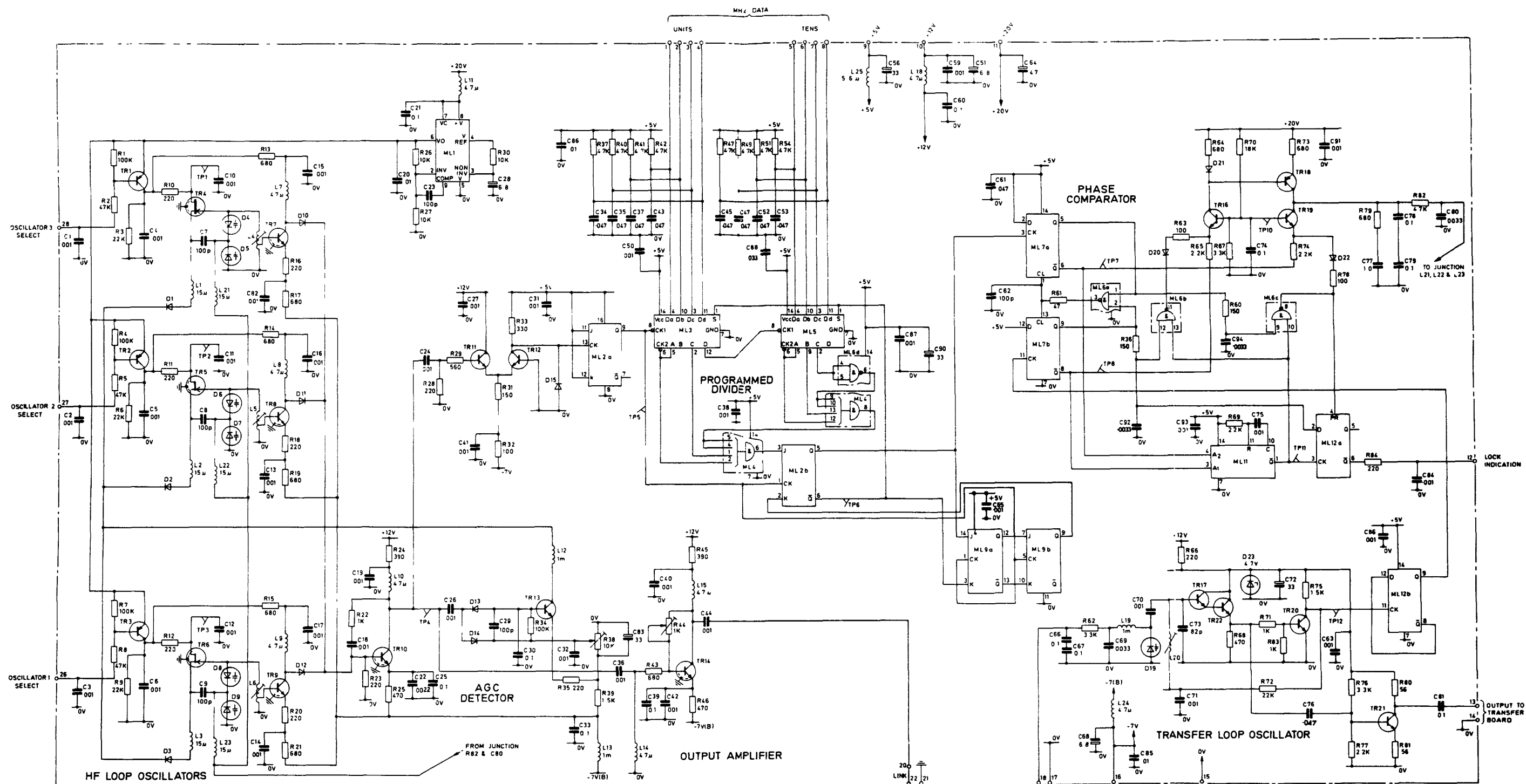






Layout : LF Loop Board PM349

Fig. 6



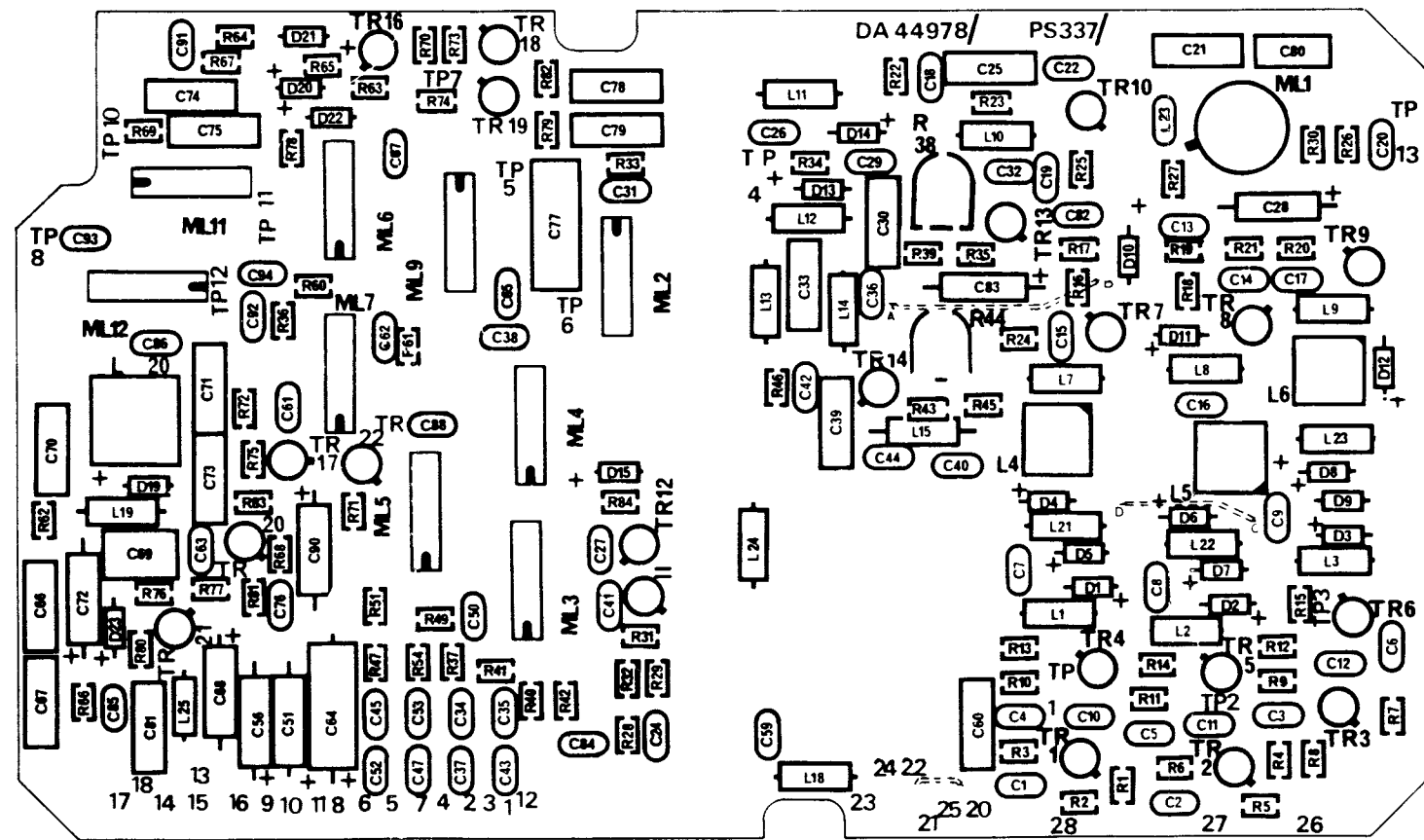
TRANSISTORS		DIODES		INTEGRATED CIRCUITS	
BFX 48	TR1, TR2, TR3, TR18	IN 4149	D1, D2, D3, D10, D11	μA723HM	ML1
BFW10	TR4, TR5, TR6		D12, D20, D21, D22	SN74S112J	ML2
BFX 89	TR10, TR14,	MV1650	D4, D5, D6, D7	SN74196J	ML3
2N2369	TR7, TR8, TR9, TR11		D8, D9, D19	SN74H31J	ML4
	TR12, TR16, TR19, TR20			SN74LS196J	ML5
				SN74H00	ML6
		HP 2800	D13, D14, D15	SN7474J	ML7, ML12
BC109	TR13, TR17, TR21, TR22			SN74121J	ML11
		BZY88C4V7	D23	SN74H03J	ML9
					ML8 AND ML10 NOT USED

W0H2085 EC44978  
5 7 0 10

Jan 92 (Amdt 8)

Circuit: HF Loop Board PS 337/3

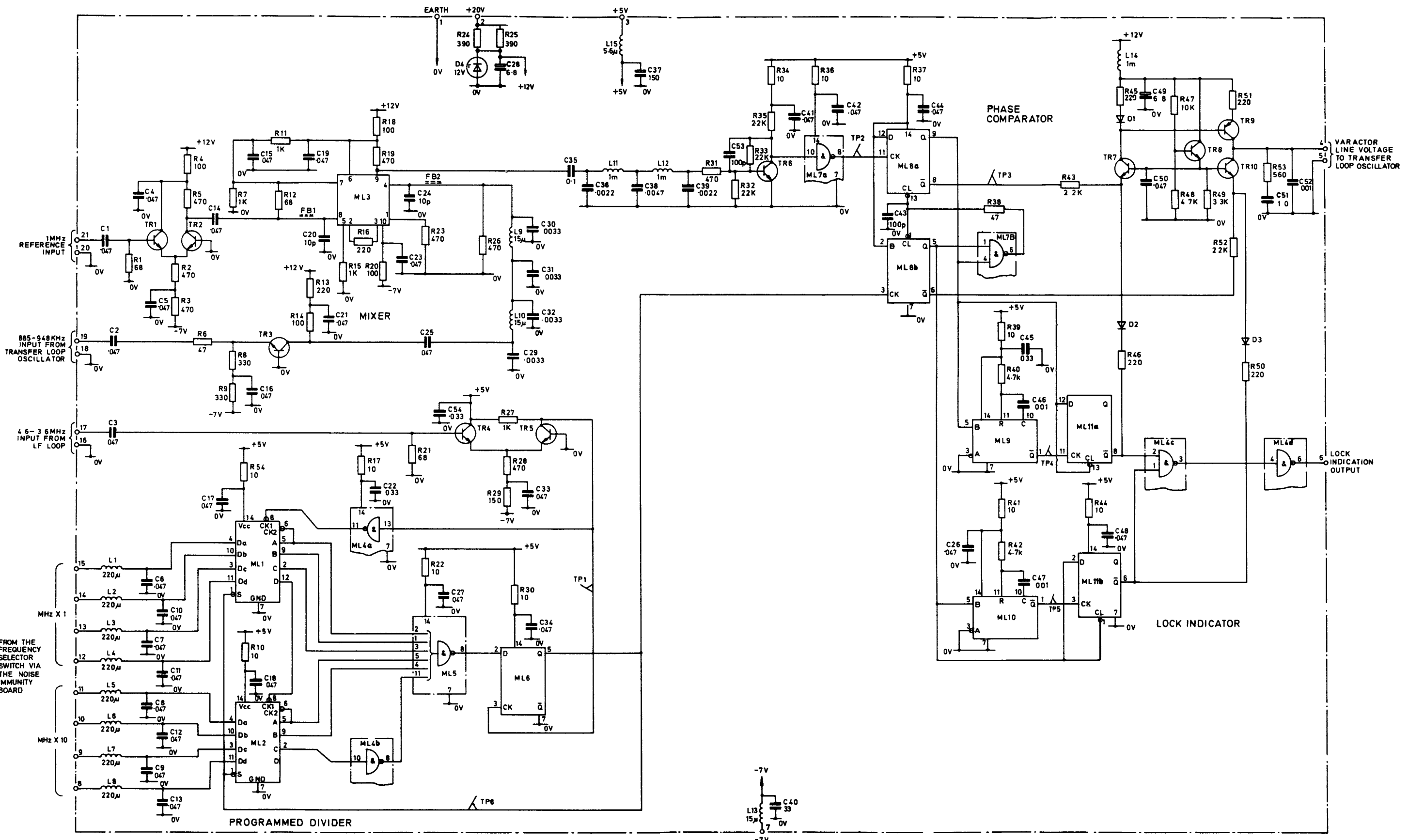
Fig 7



Layout : HF Loop Board PS337/4

Fig.8



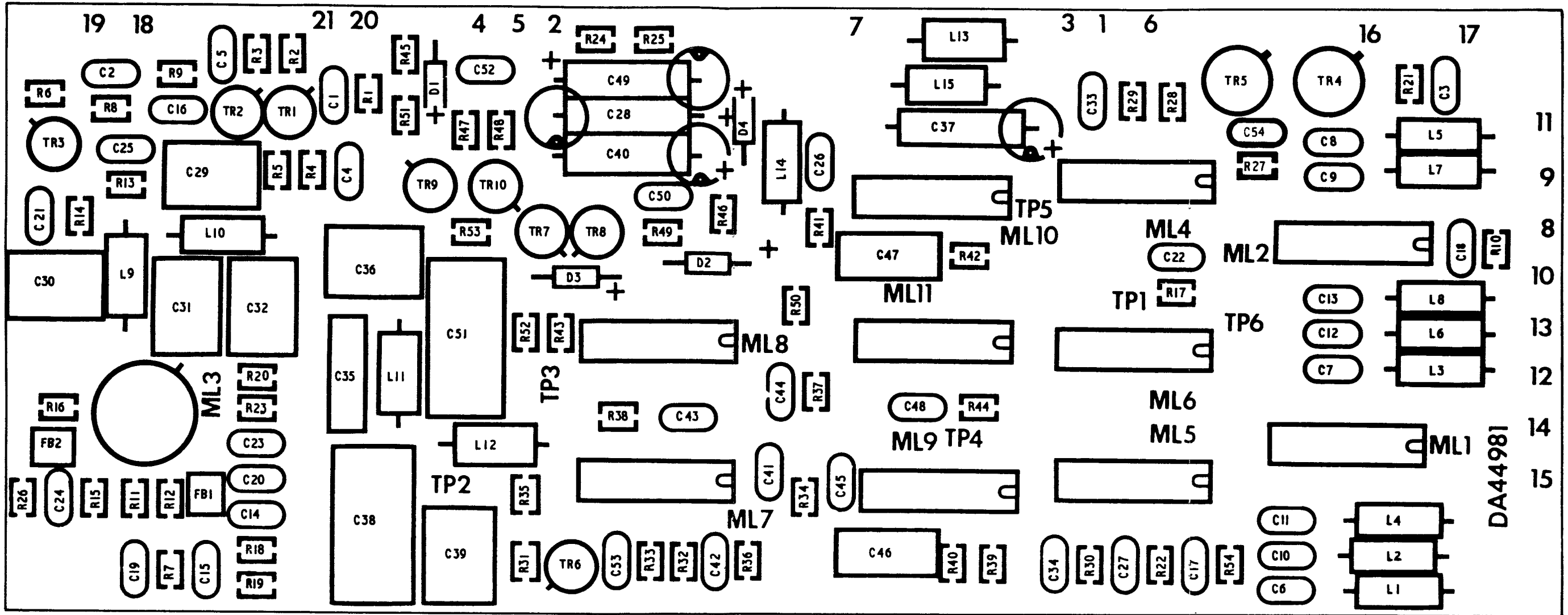


WOH2085 DC44981  
C 2 3 4 7 8

Jan 92 (Amdt 8)

Circuit: Transfer Loop PS338

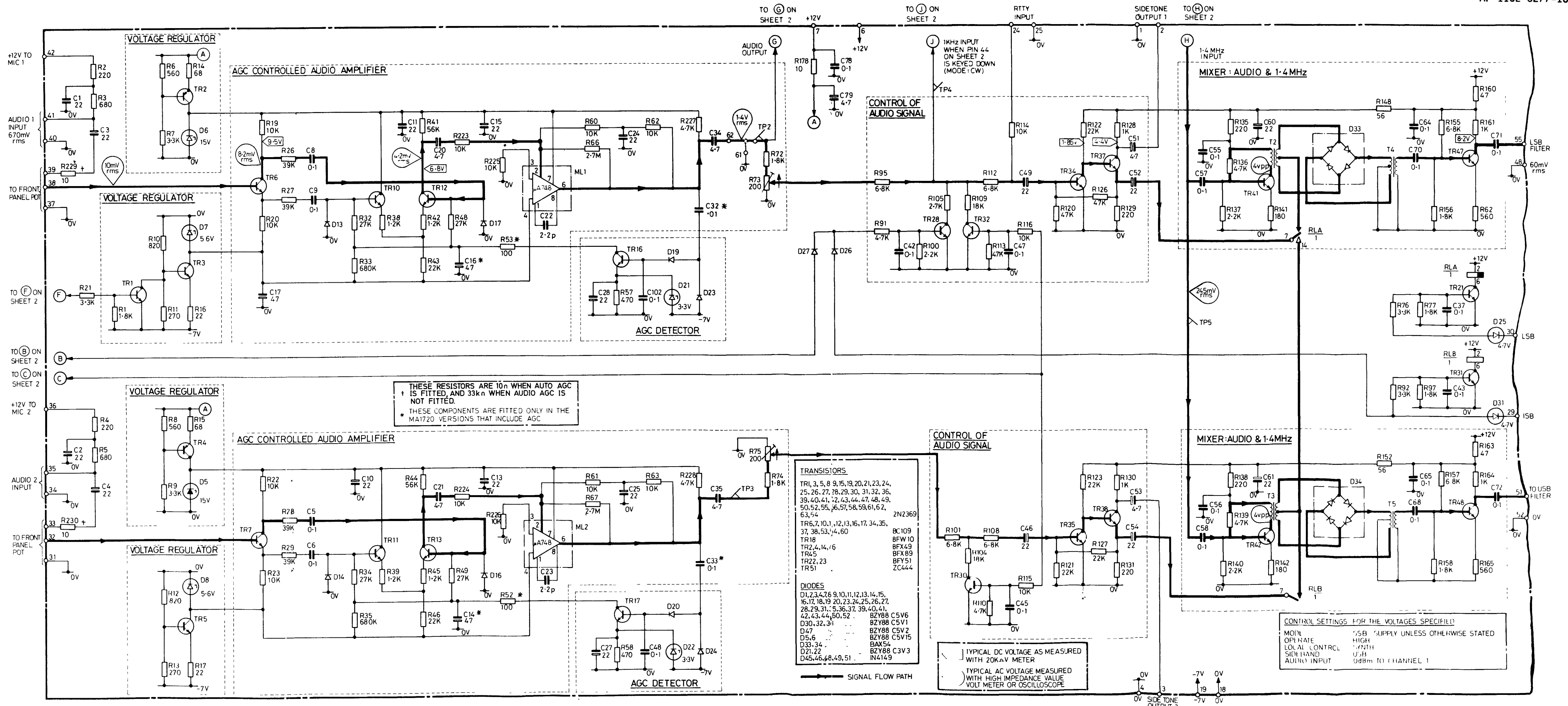
Fig. 9

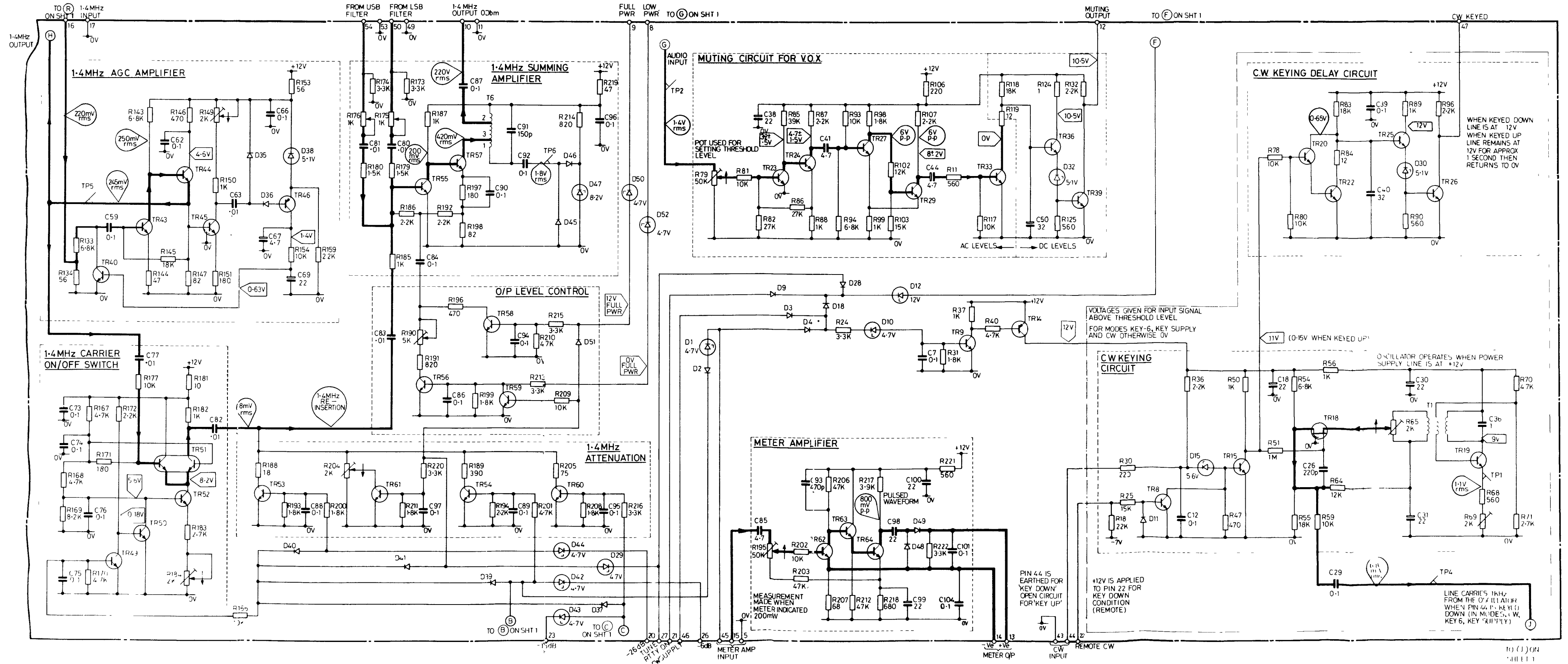


DA44981

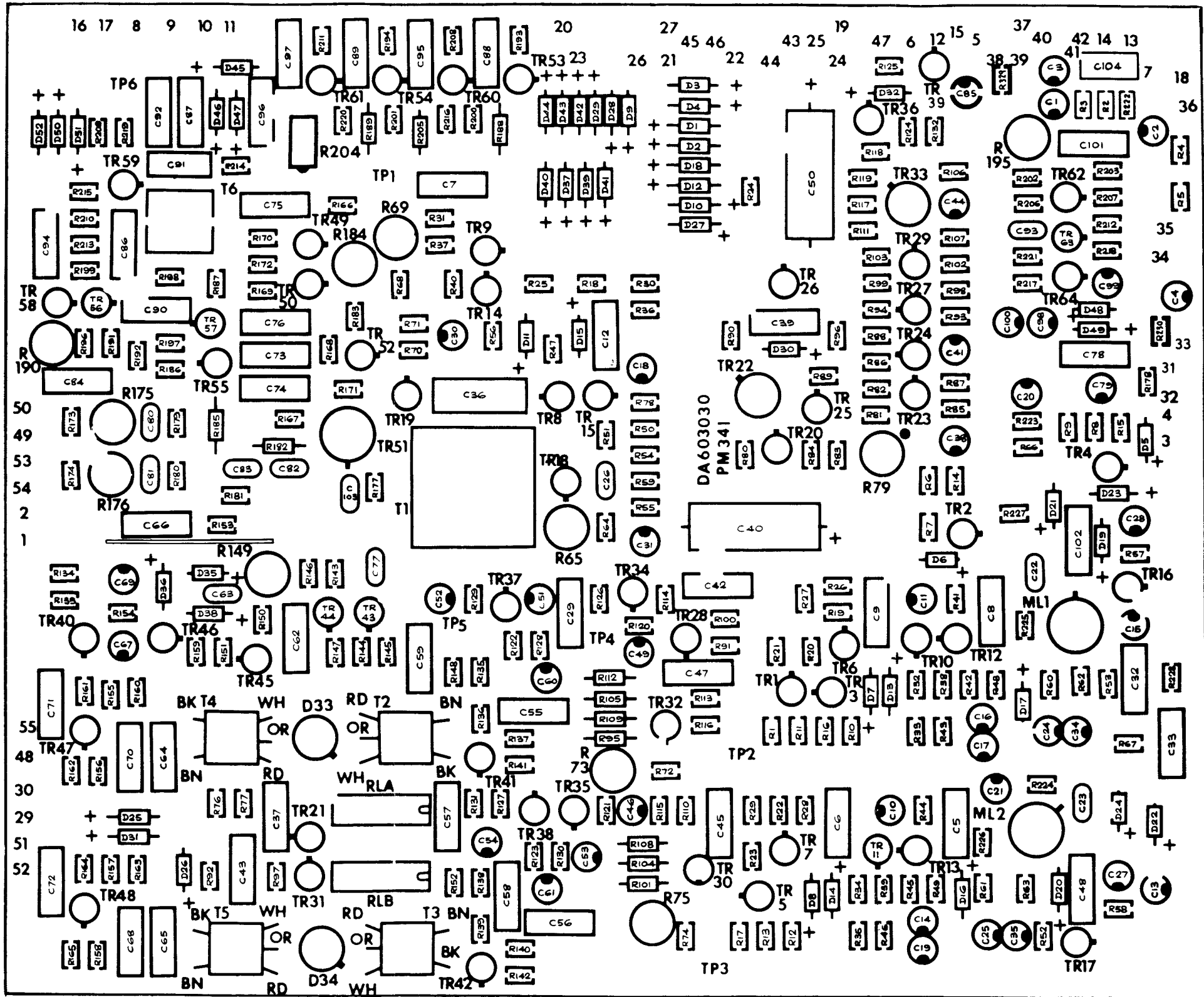
Layout: Transfer Loop Board PS338

Fig. 10





Circuit: Low Level PCB PM.341 Fig. 11 Sht. 2

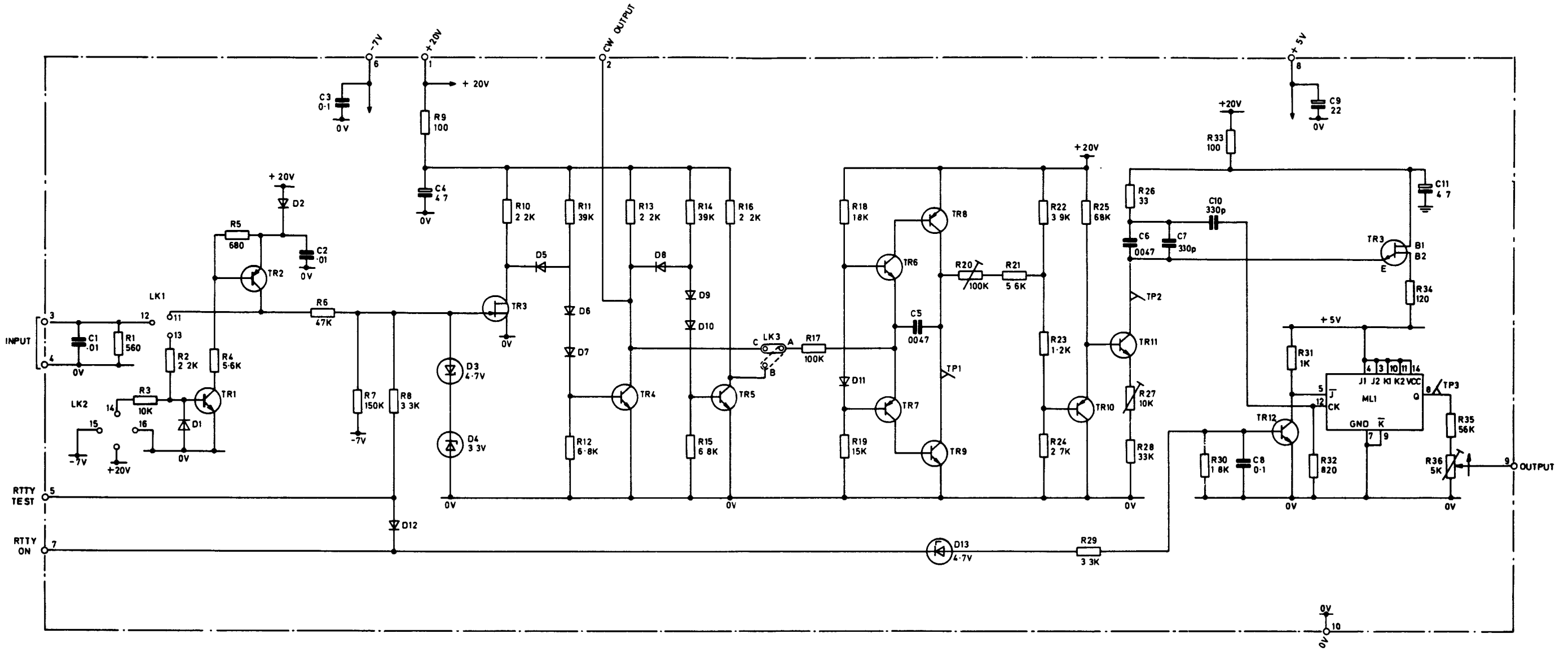


WOH 2085	DA603030	SHT 1
2	3	6

Jan 92 (Amdt 8)

Layout: Low Level Board (PM341)

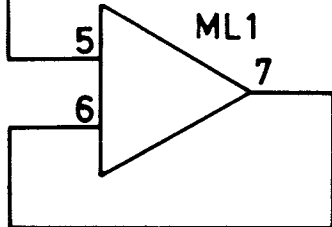
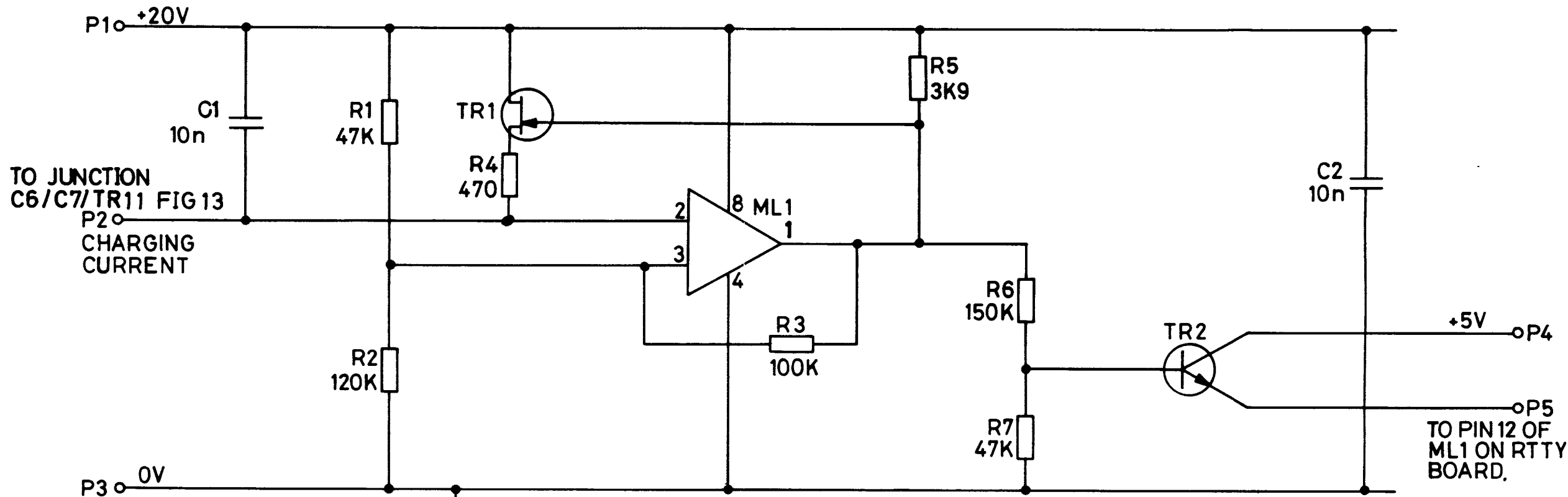
Fig. 12



LINK CONNECTION TABLE

POLAR	NEUTRAL	REVERSE	NORMAL
PIN 12 TO PIN 13	PIN 12 TO PIN 13 AND EITHER	A - C	A - B
PIN 14 TO PIN 16	PIN 14 TO PIN 15 FOR POSITIVE KEYING OR PIN 14 TO PIN 17 FOR NEGATIVE KEYING		

DIODES		TRANSISTORS	
1N4149	D1, D5, D6, D7, D8, D9, D10, D11, D12	2N2369	TR1, TR12
1N4002	D2	BC107	TR4, TR5
BZY88C3V3	D4	BFX 29	TR2
BZY88C4V7	D3, D13	2N4392	TR3
		BC109	TR6, TR9, TR11
		BFX 46	TR7, TR8, TR10
		D5K2	TR13



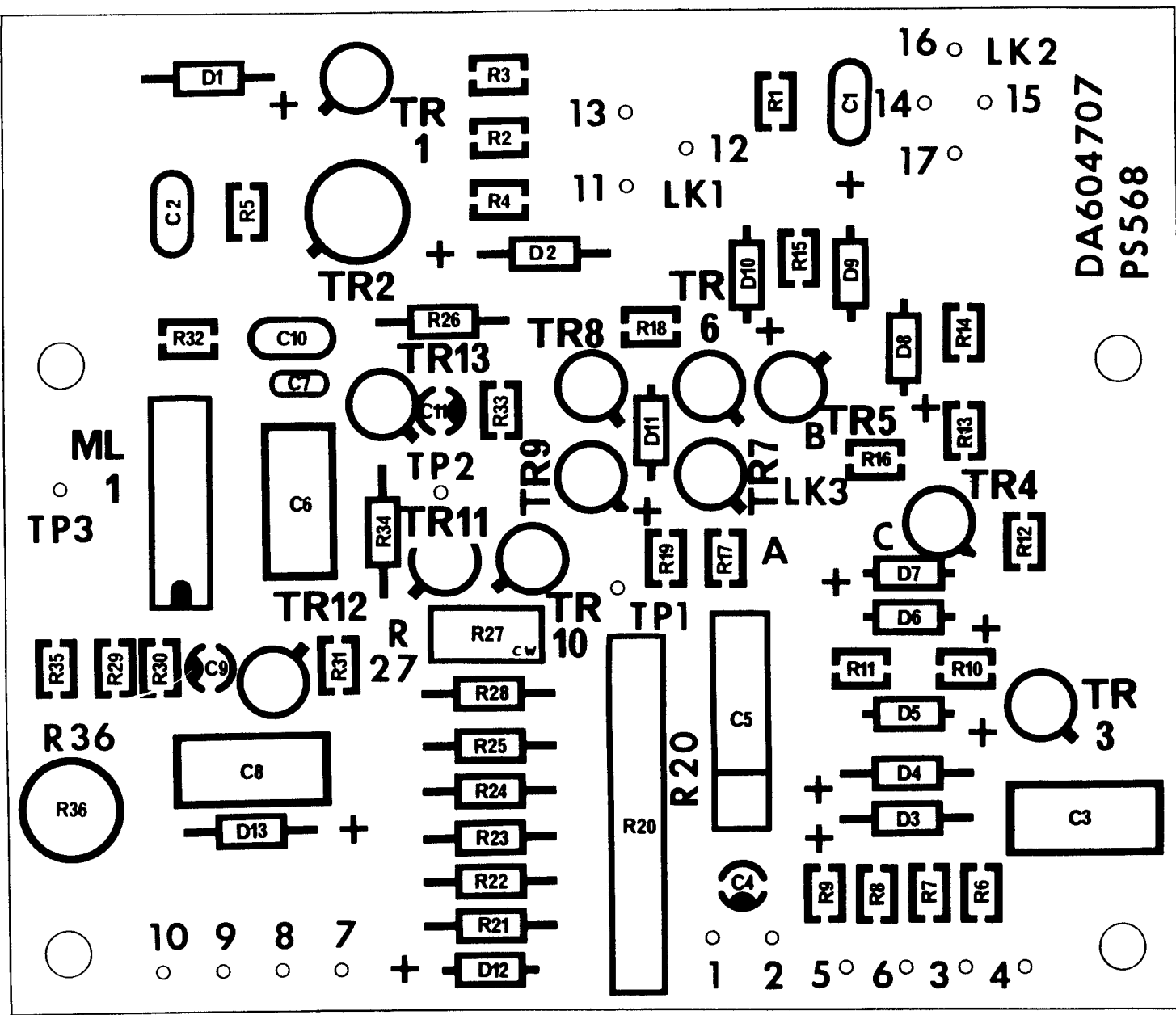
TRANSISTORS		INTEGRATED CIRCUITS	
REF	TYPE	REF	TYPE
TR1	2N4392	ML1	LM393N
TR2	BC109		

**RACAL**

WOH2085	BC88476
1	

Jan 92 (Amdt 8)

Circuit :RTTY Modification Fig.13 A

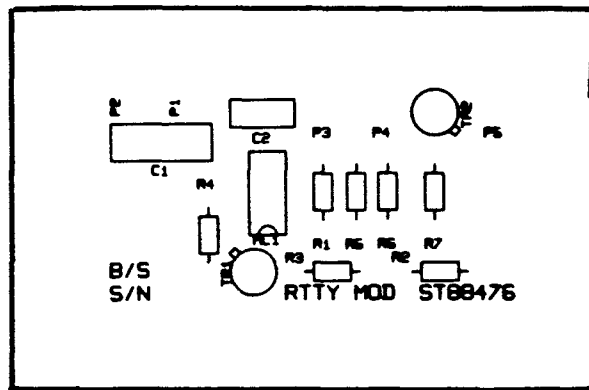


DA604707  
PS568

Layout: RTTY Generator PS568

Fig.14

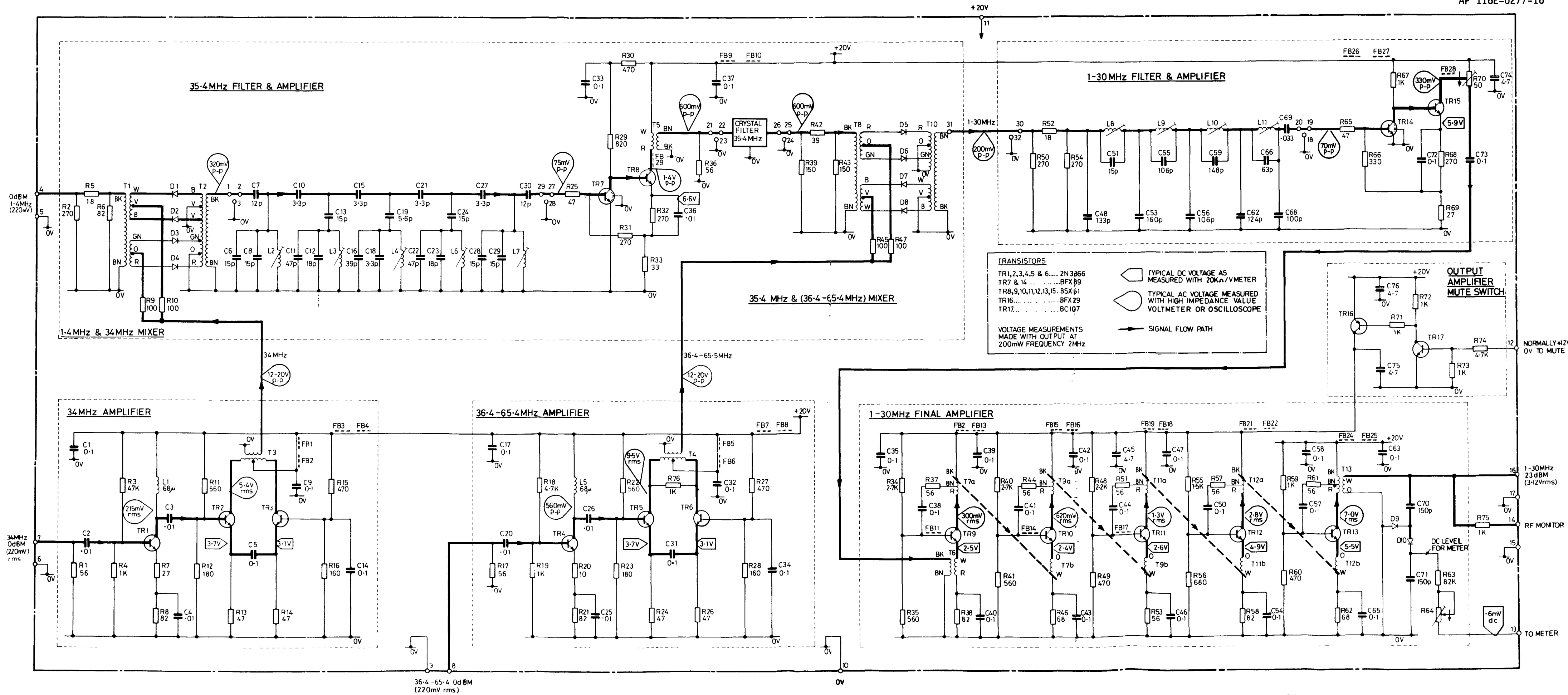


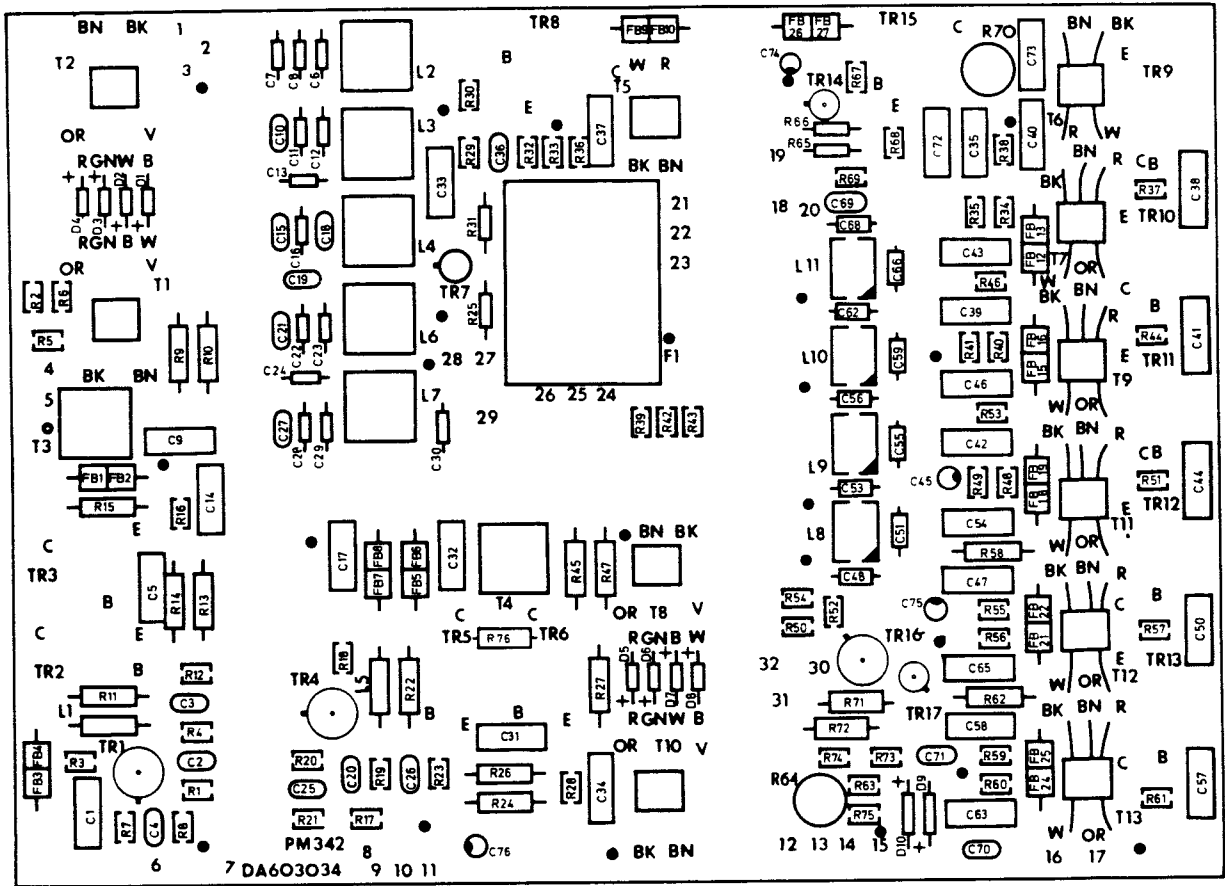


WOH2085	BA88475
1	

Jan 92 (Amdt 8)

Layout:  
RTTY Mod. Board Fig 14A



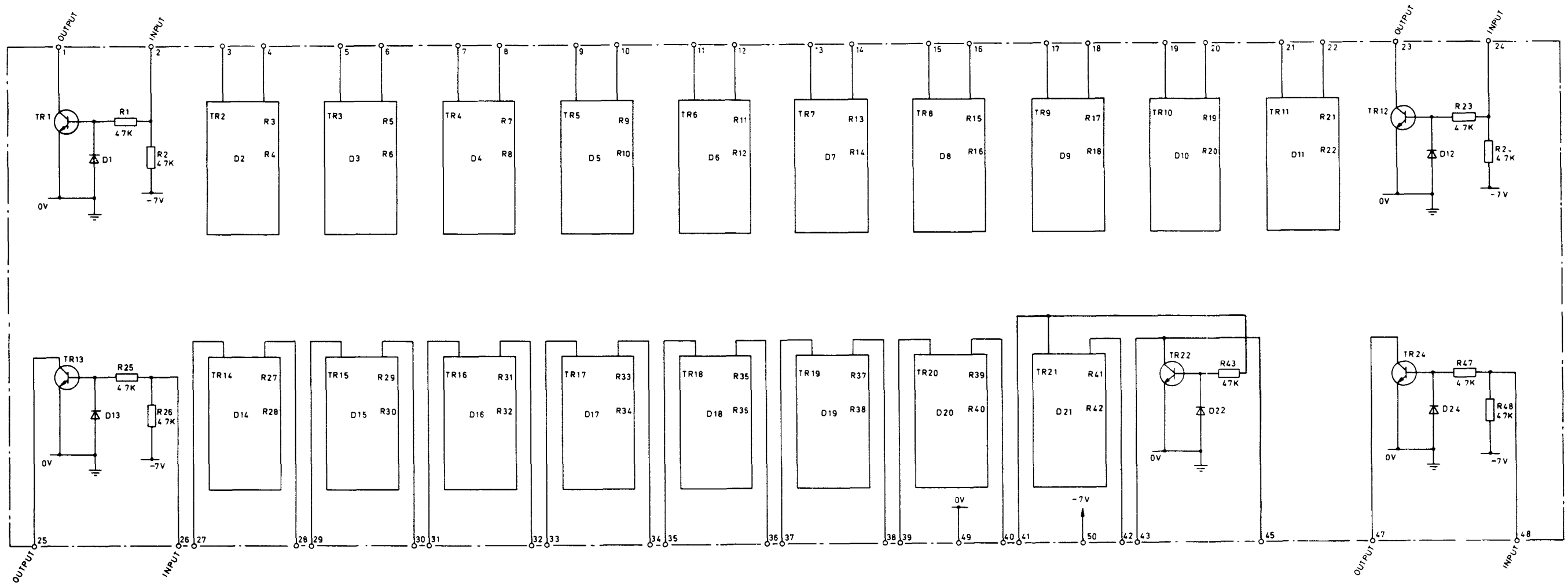


WOH2085 DA603034  
B 3

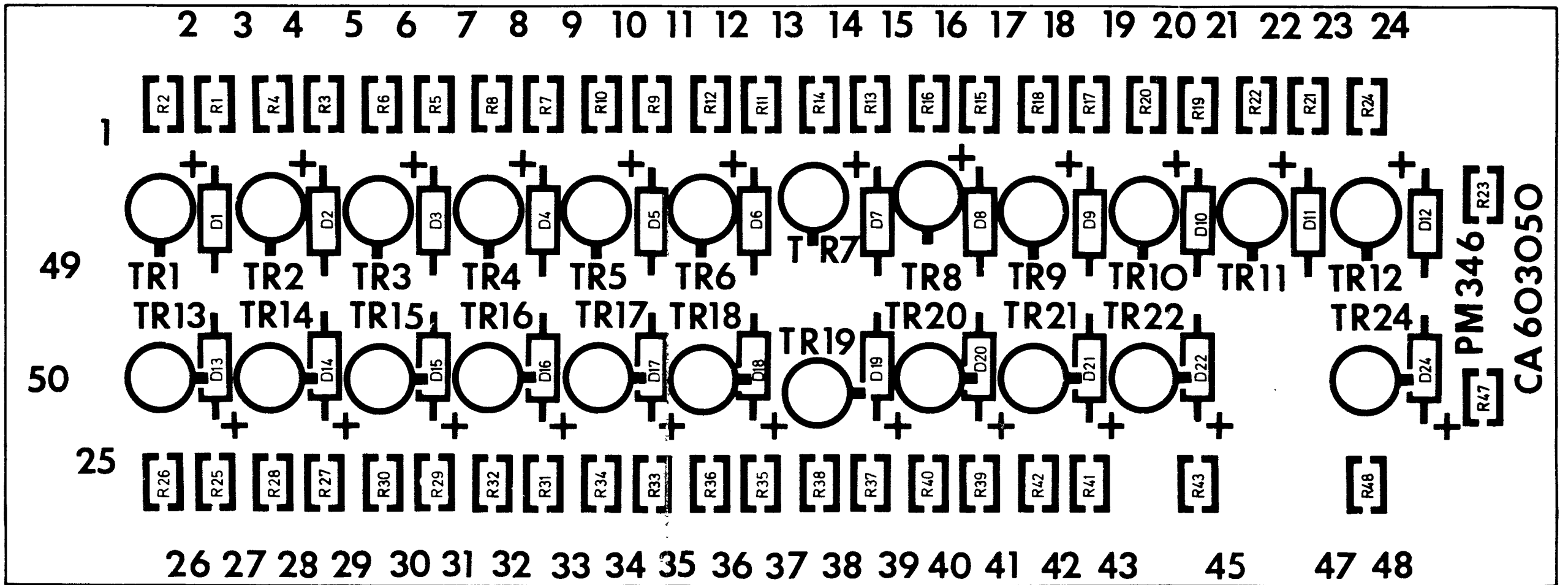
Jan 92 (Amdt 8)

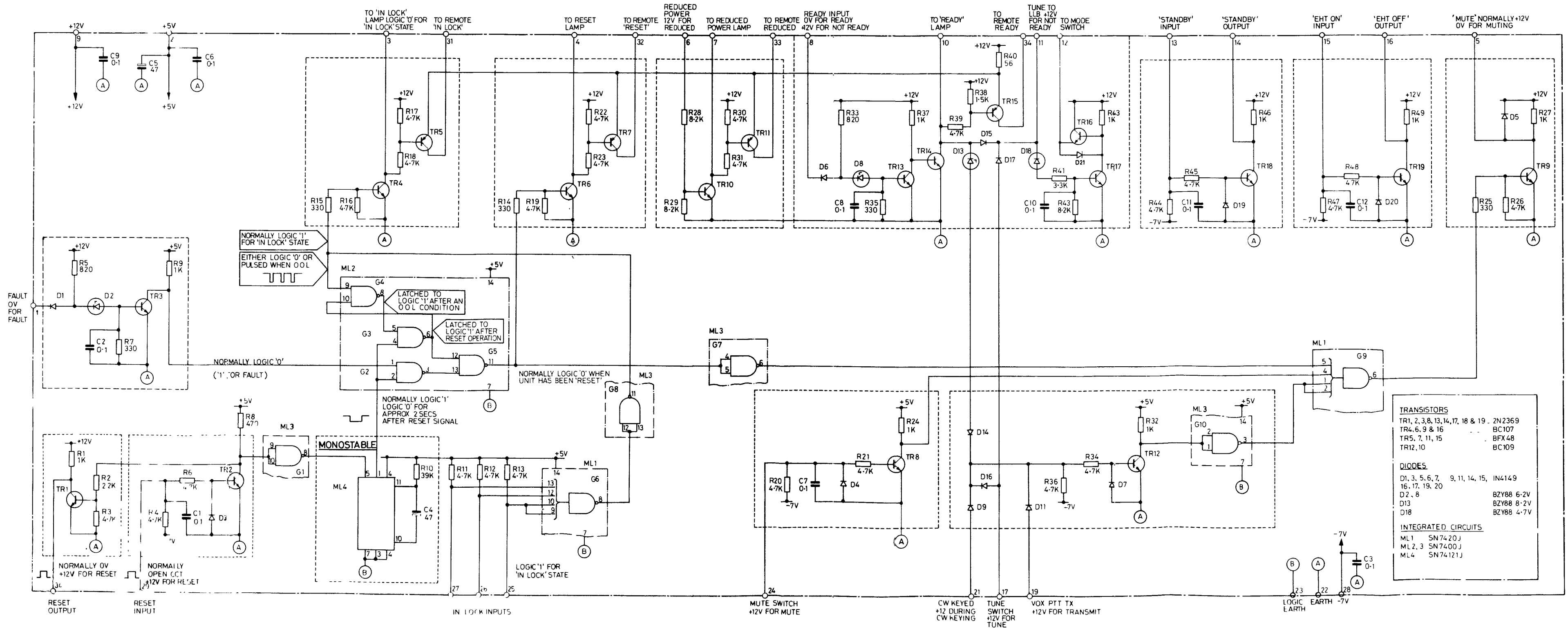
Layout: Mixer and Output Board PM342

Fig. 16



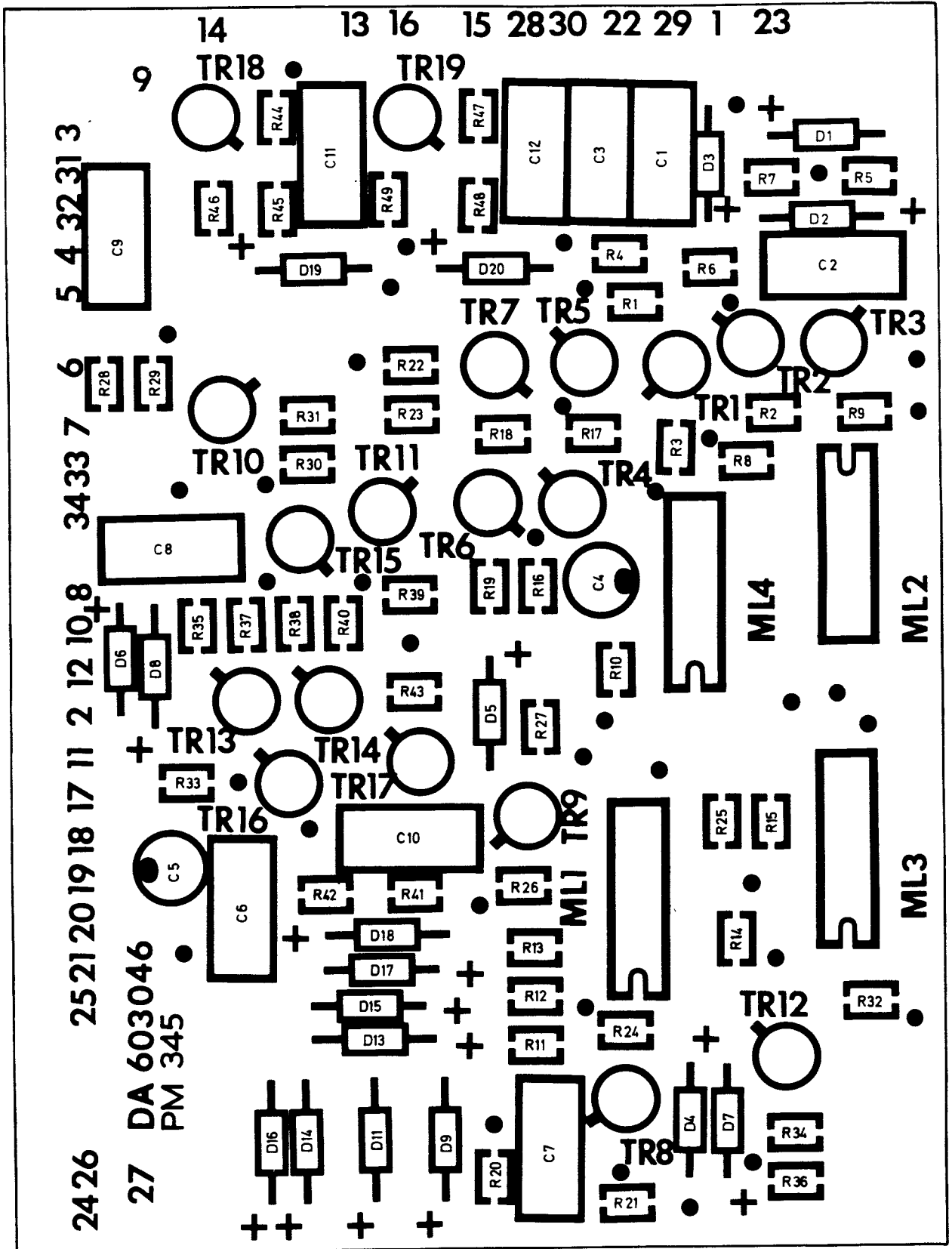
NOTE EVEN NUMBERED PINS ARE INPUTS  
 ODD NUMBERED PINS ARE OUTPUTS





Circuit :  
Control PCB PM.345

Fig.19

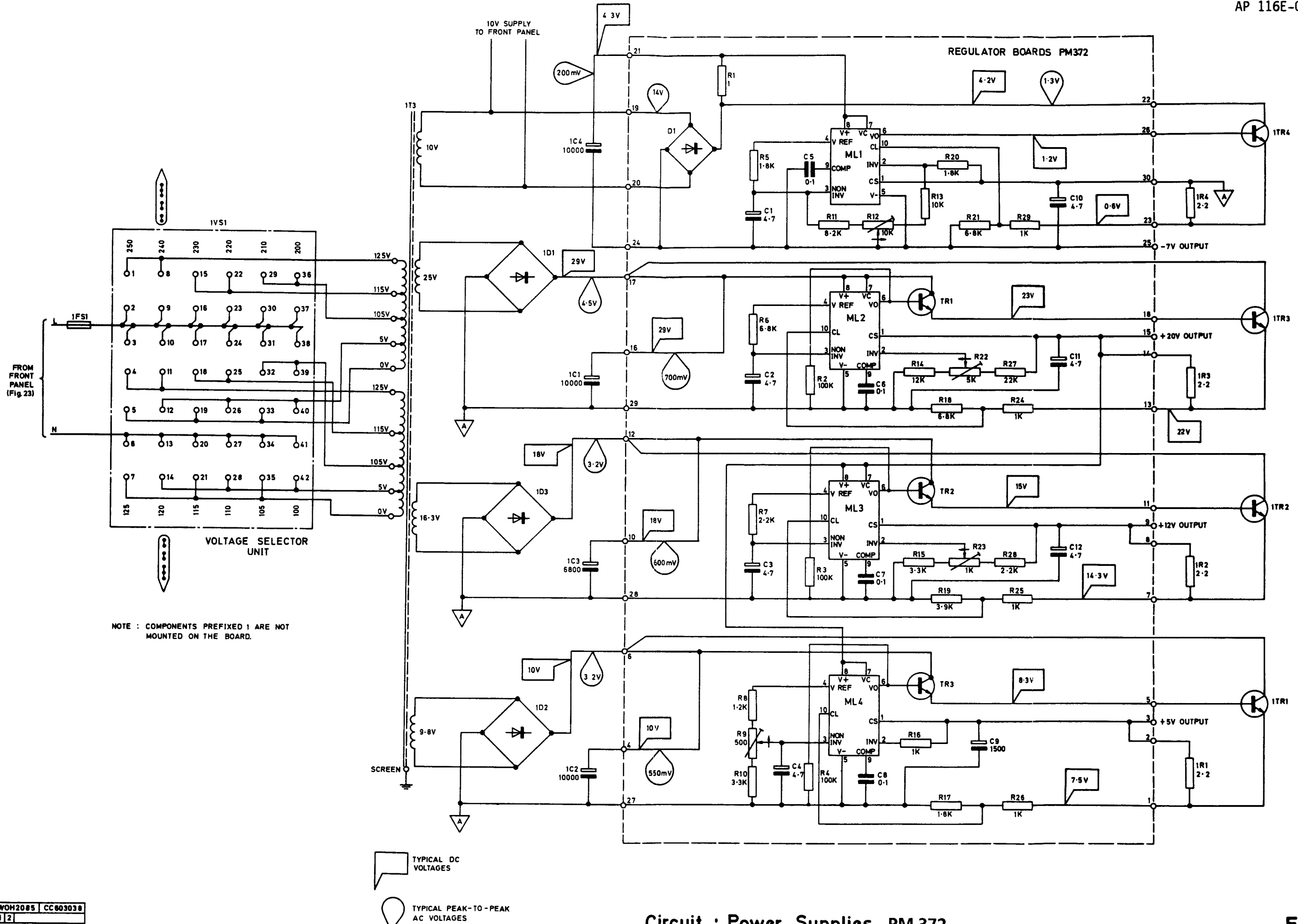


WOH2085	DA603046	SHT 1
B/L		

Jan 92 (Amdt 8)

Layout: Control Board PM345

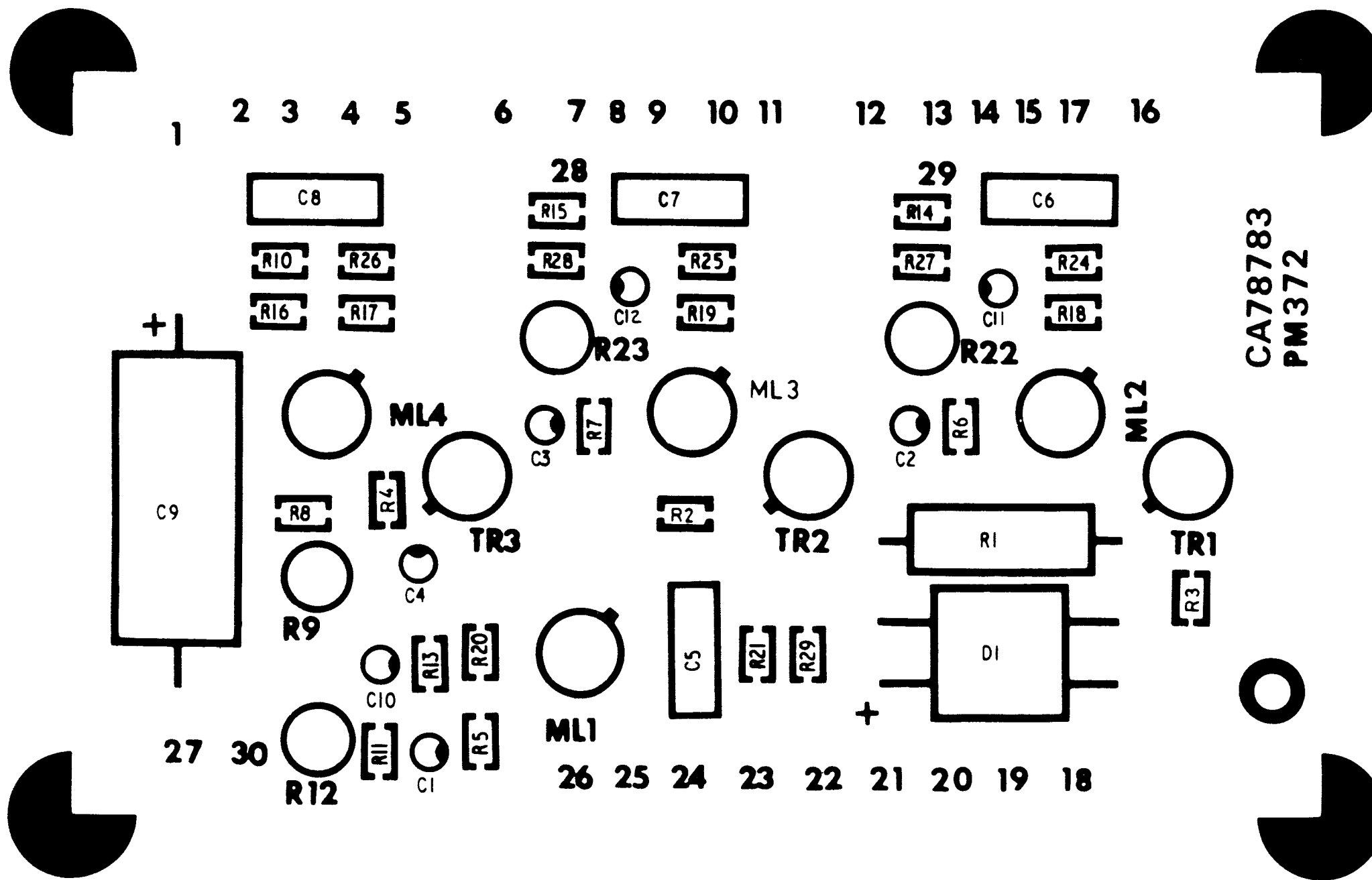
Fig. 20



Circuit : Power Supplies PM 372

Fig 21





CA78783  
PM372

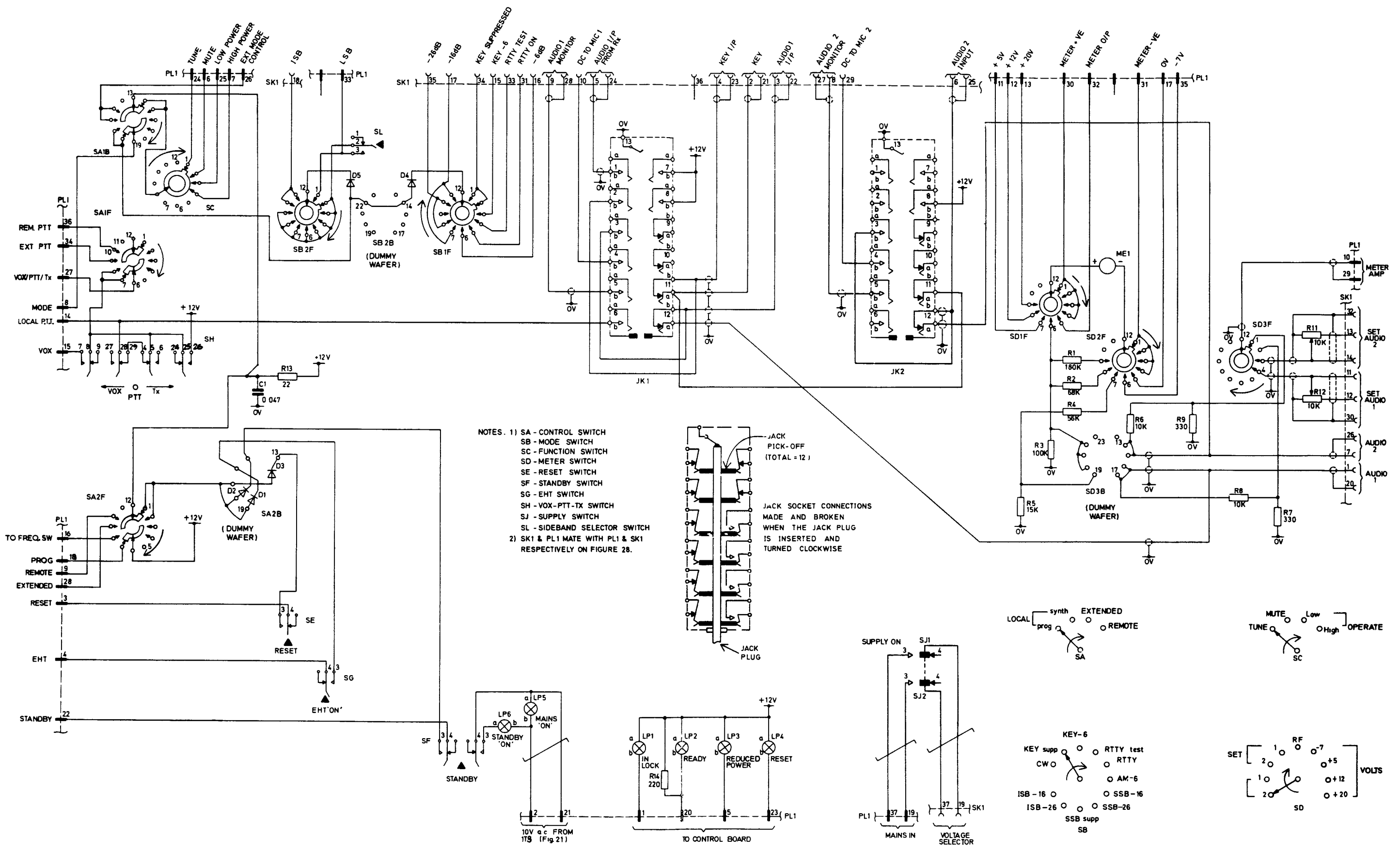
**RACAL**

WOH 2085	CA78783
2	

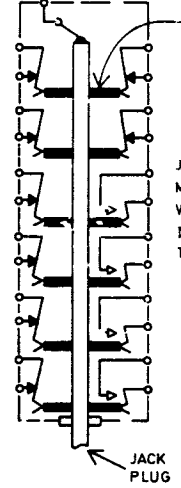
Jan 92 (Amdt 8)

Layout: Regulator Board PM372

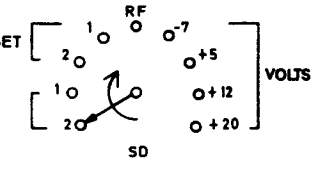
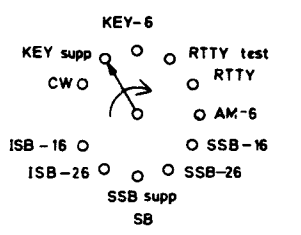
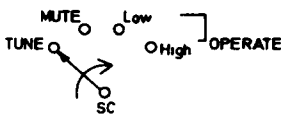
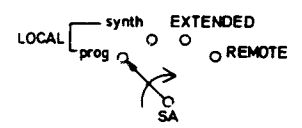
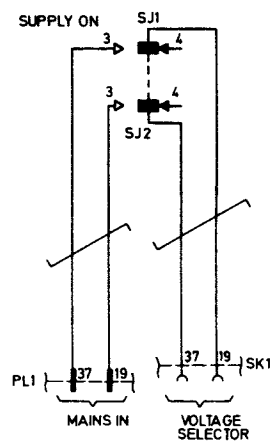
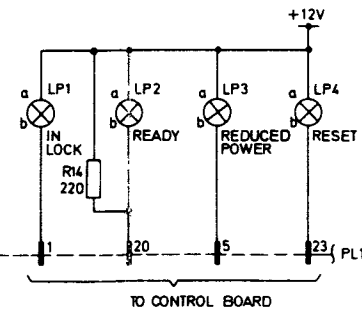
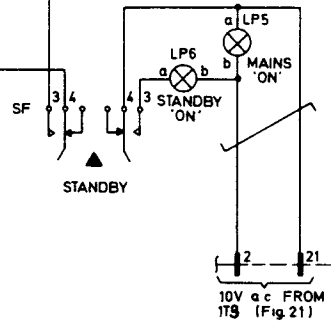
Fig.22



- NOTES. 1) SA - CONTROL SWITCH  
 SB - MODE SWITCH  
 SC - FUNCTION SWITCH  
 SD - METER SWITCH  
 SE - RESET SWITCH  
 SF - STANDBY SWITCH  
 SG - EHT SWITCH  
 SH - VOX-PTT-TX SWITCH  
 SJ - SUPPLY SWITCH  
 SL - SIDEBAND SELECTOR SWITCH  
 2) SK1 & PL1 MATE WITH PL1 & SK1 RESPECTIVELY ON FIGURE 28.

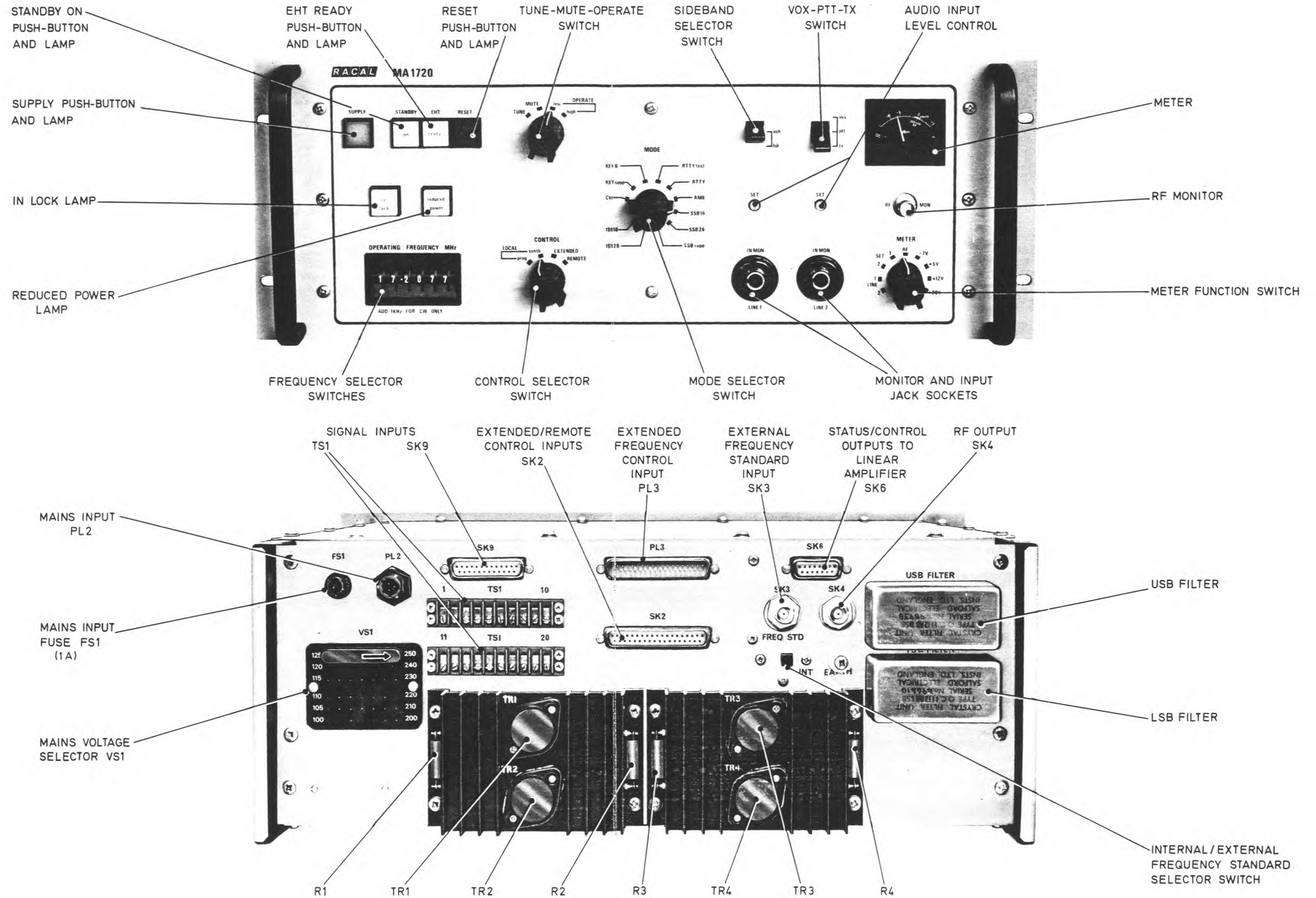


JACK SOCKET CONNECTIONS MADE AND BROKEN WHEN THE JACK PLUG IS INSERTED AND TURNED CLOCKWISE



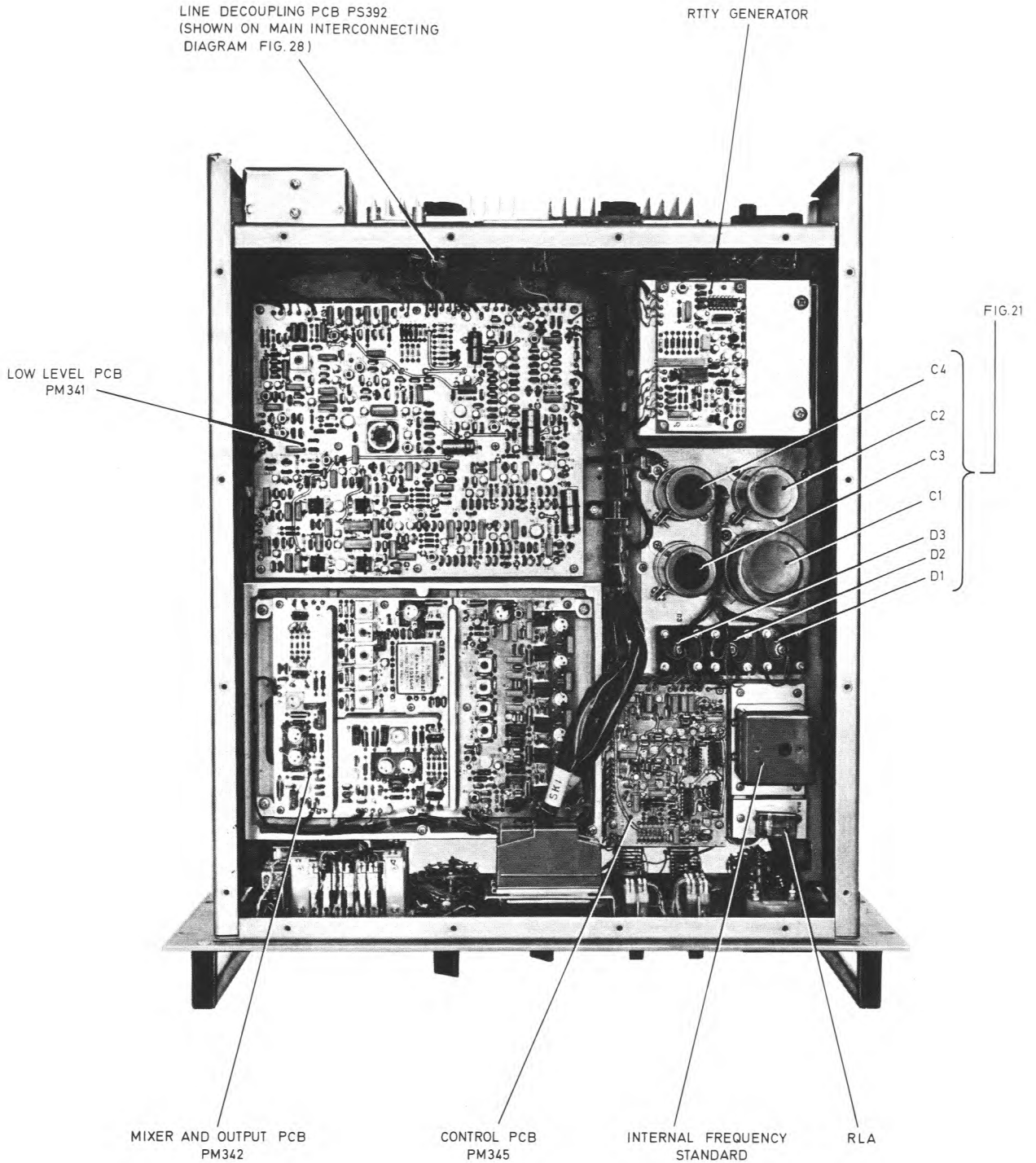
Circuit: Front Panel

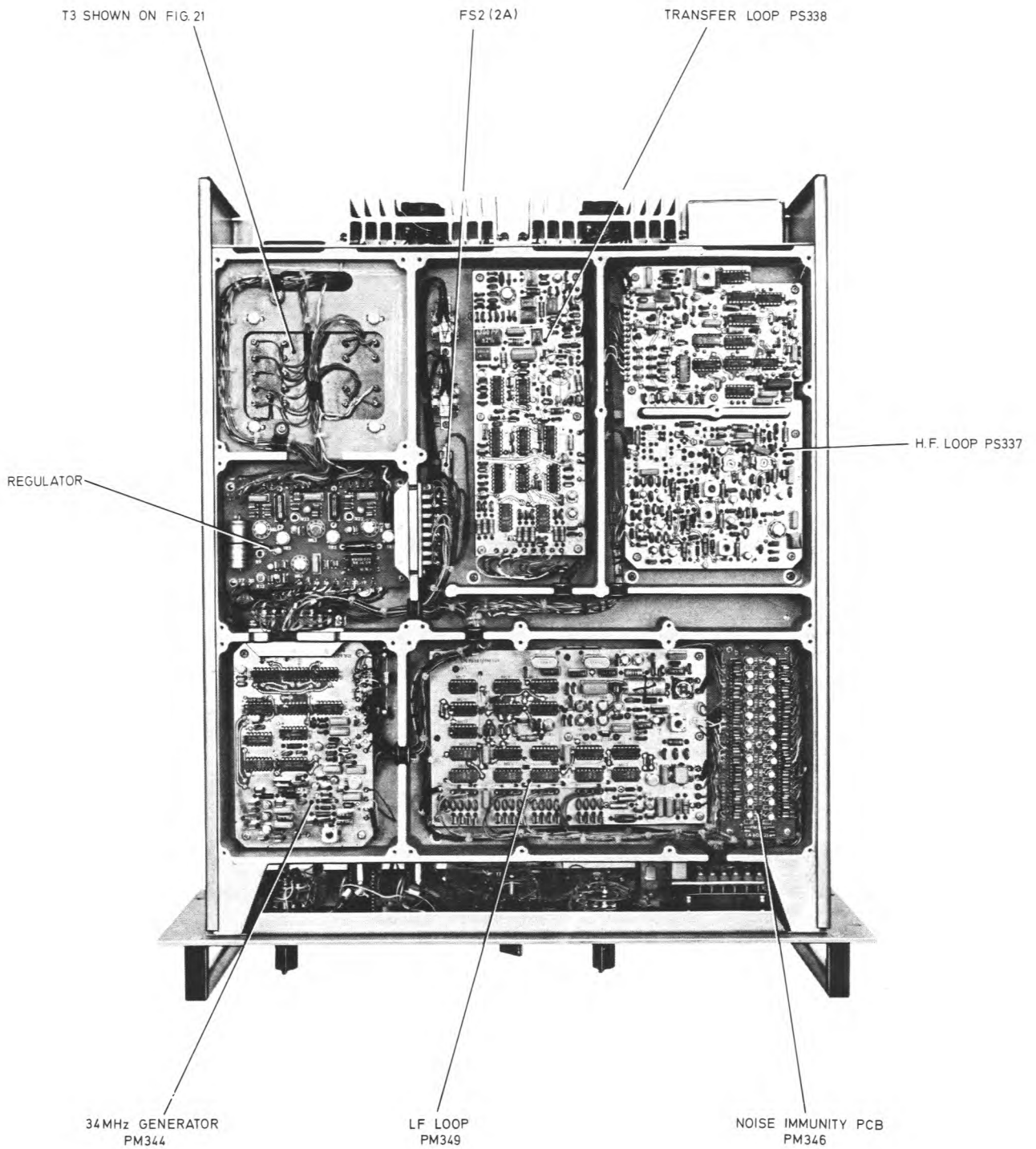
Fig. 23

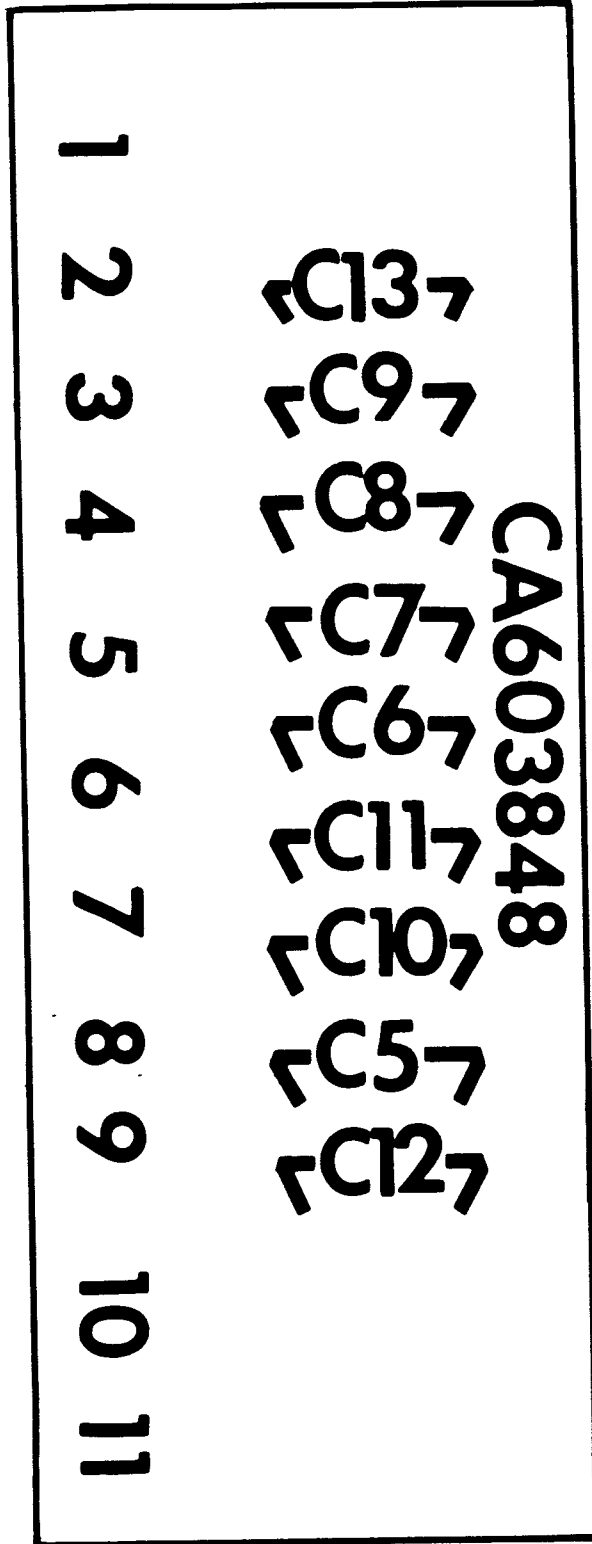


Front and Rear Panels - MA.1720

Fig.24







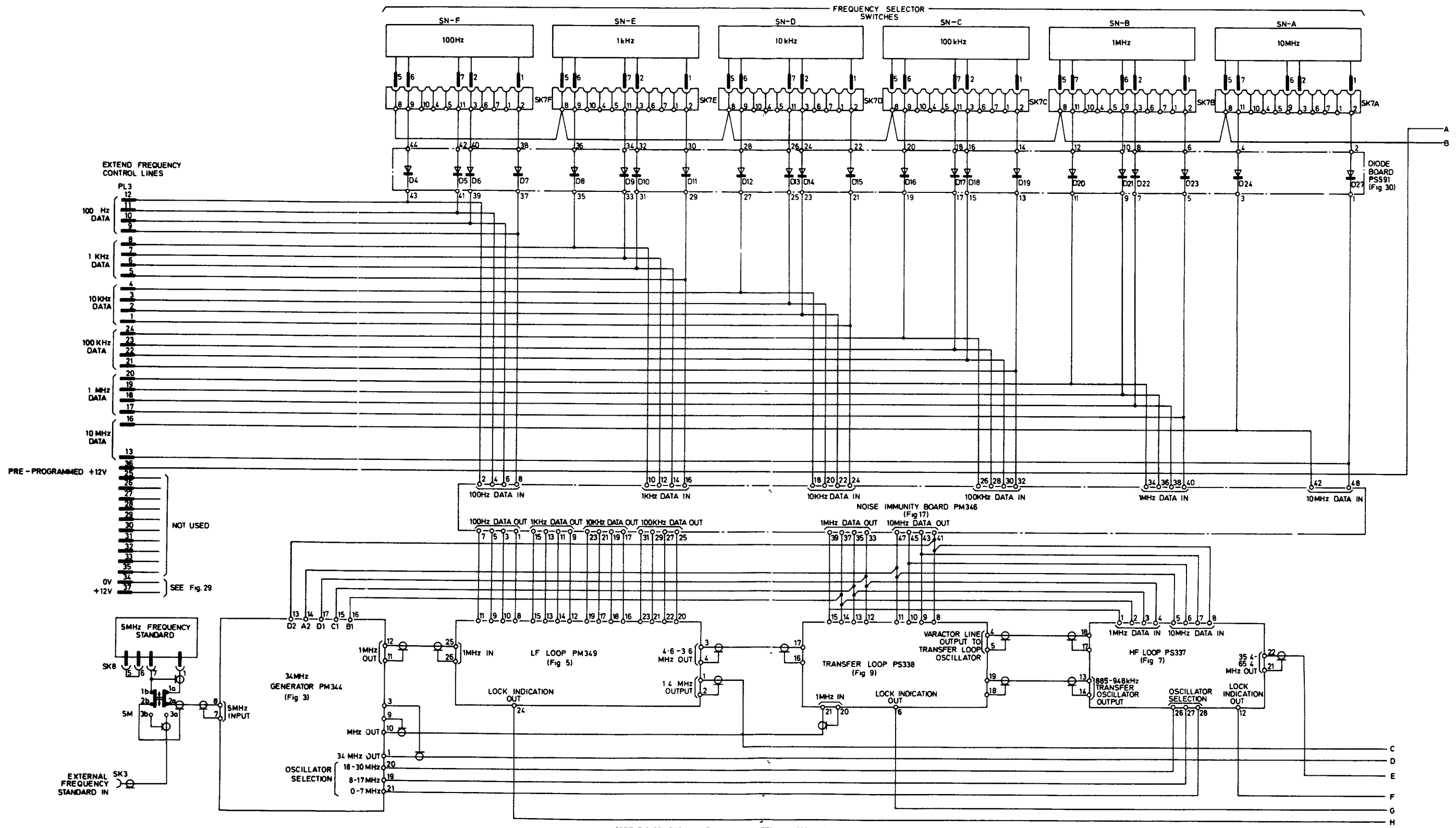
NOTE: CIRCUIT IS SHOWN ON OVERALL INTERCONNECTING DIAGRAM FIG 28

WOH2085	CD603850	SHT.3
B	PL	

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Layout: Line Decoupling  
P.C.B. PS392

Fig. 27

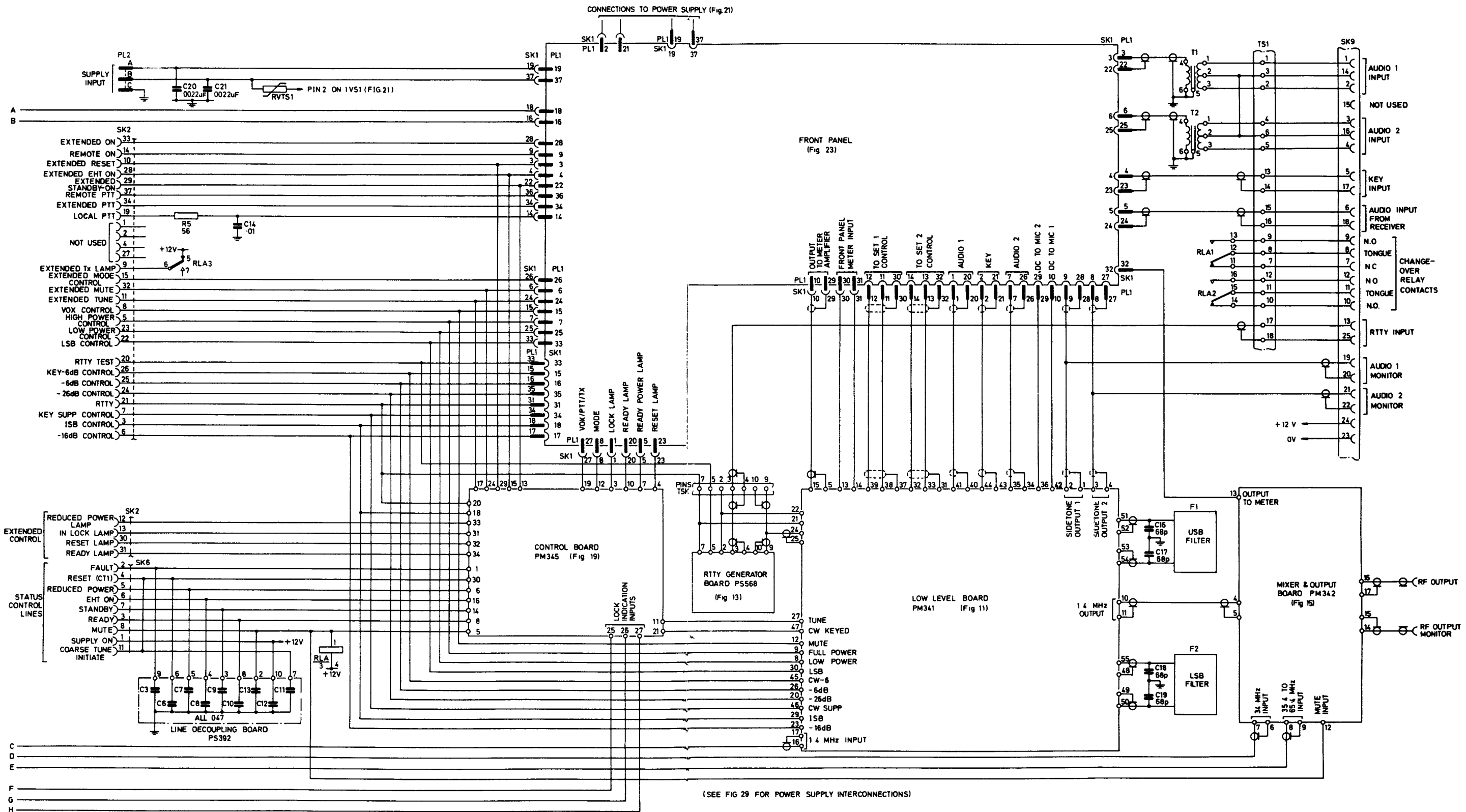


(SEE FIG 29 FOR POWER SUPPLY INTERCONNECTIONS)

WOH2085 EC603200  
8/9

Fig. 28 (Sheet 1)

Interconnection Diagram (Part 1) MA1720

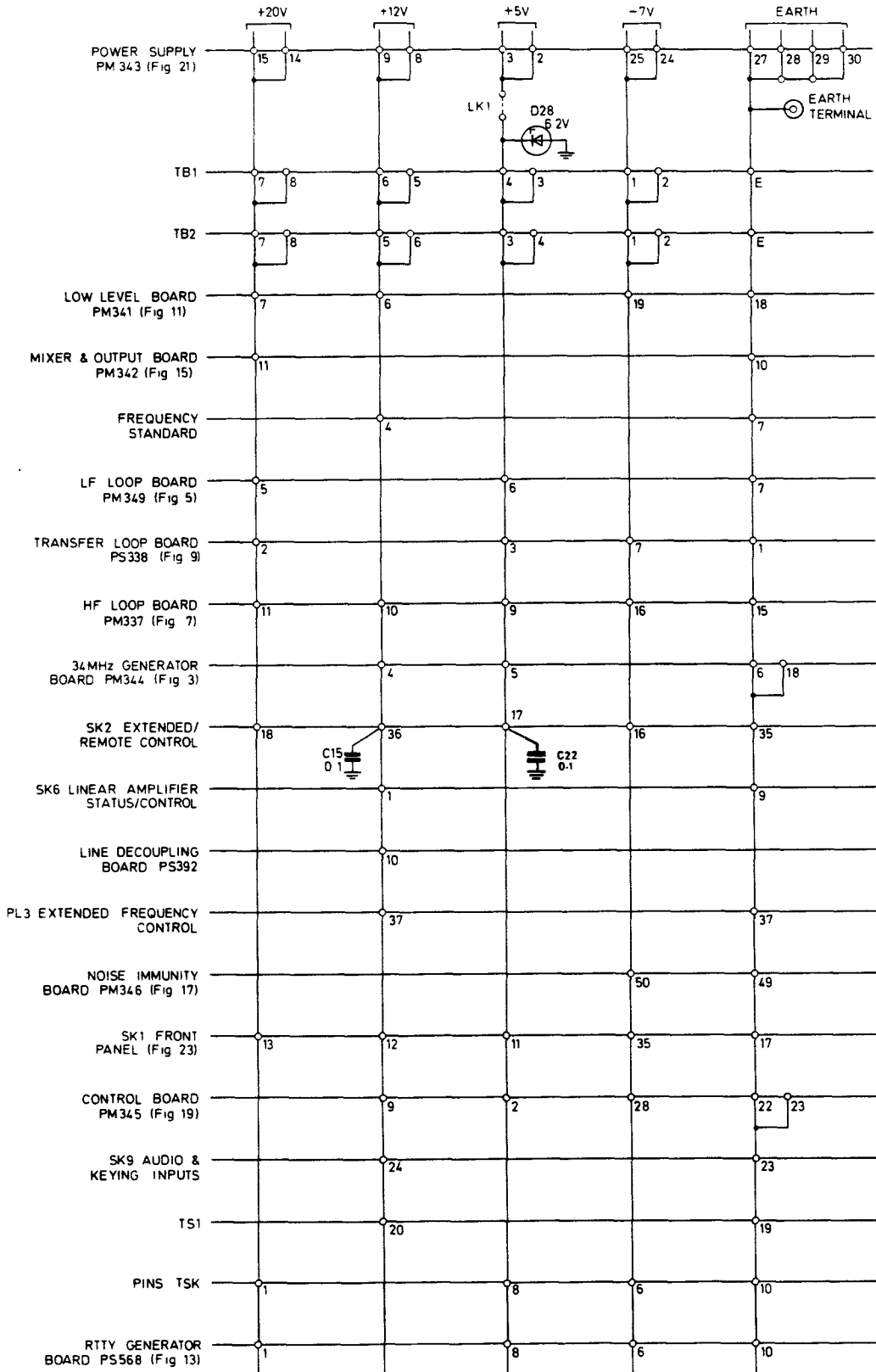


(SEE FIG 29 FOR POWER SUPPLY INTERCONNECTIONS)

Interconnection Diagram (Part 2): MA.1720

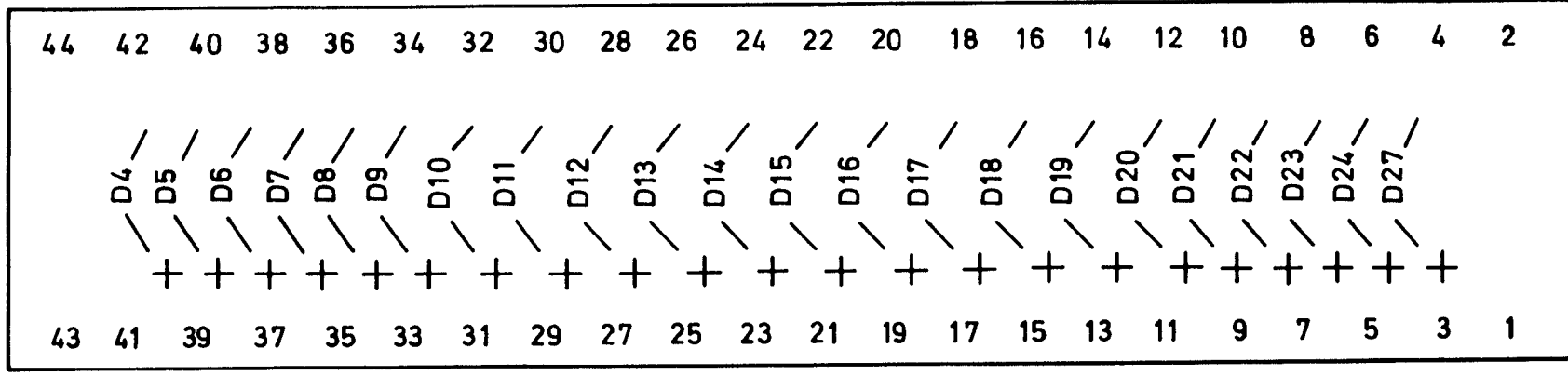
(Sheet 2) Fig. 28





WOH 2085 EC603200  
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Interconnection Diagram: Power Supplies Fig. 29



WOH2085 DA604998/3  
21

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Layout: Diode Board PS591

Fig.30

ADDENDUM 1

TO

APPENDIX 1

GENERATION OF CW SIGNAL

CONTENTS

	<u>Para.</u>
INTRODUCTION	1
CW GENERATION	2

ADDENDUM 1TOAPPENDIX 1GENERATION OF CW SIGNALINTRODUCTION

1. The operating procedures given in Chapter 3 state that the frequency selector switches must be set to 1 kHz above the required frequency for CW operation. The principles of the generation of the CW signal, and the reason for the frequency offset, are given in this appendix.

CW GENERATION

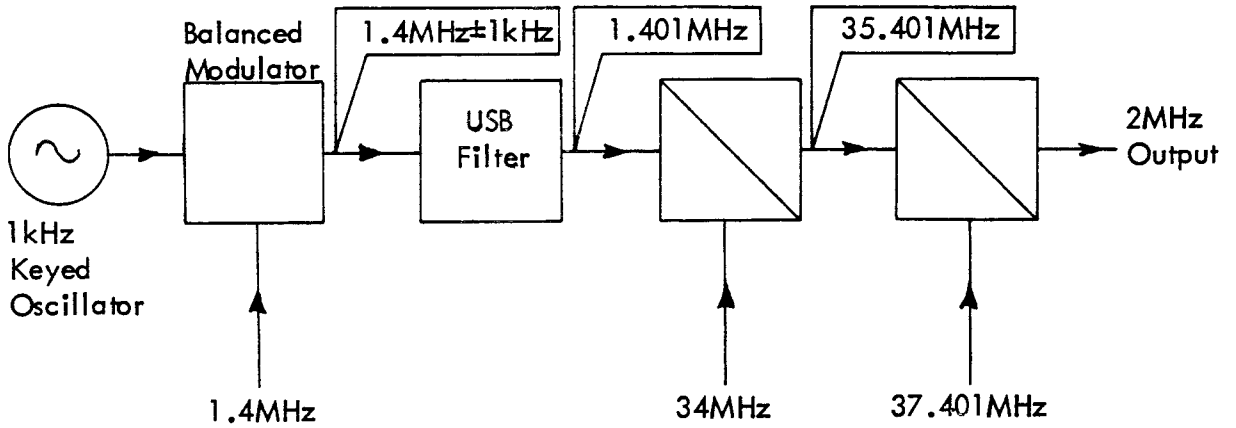
2. The CW (A1) output of the transmitter is a keyed signal at carrier frequency. In the MA1720 drive unit the CW signal is generated by a 1 kHz tone in the lower sideband. As the output signal is required to be at the carrier frequency, the selected frequency must be 1 kHz above the required output frequency.

3. A simplified block diagram with a numerical example is given below. In this example an actual output frequency of 2.0000 MHz is required; therefore the CW mode is selected and the frequency selector switches are set to 2.0010 MHz.

4. The 1 kHz oscillator frequency is mixed, in a balanced modulator, to provide a first IF of  $1.4 \text{ MHz} \pm 1 \text{ kHz}$ , i.e. 1.401 MHz and 1.399 MHz. The 1.401 MHz signal is passed by the USB filter, and mixed with 34 MHz to provide a second IF of 35.401 MHz.

NOTE: The USB filter allows the higher frequency (1.401 MHz) to be fed to the mixer and suppresses the lower frequency (1.399 MHz). Due to the inversion introduced by the final mixer the CW signal appears as a 1 kHz tone in the lower sideband.

5. The 35.401 MHz frequency is mixed with the channel frequency (which is 37.401 MHz when the selector switches are set to 2.0010 MHz), to produce the required output signal at a frequency of 2.0000 MHz.



6. The method of signal generation outlined above allows CW signals to be shaped by the sideband filter. If a shaping stage is omitted, harmonics are generated due to the rapid rise and fall of the keyed tone.

ADDENDUM 2

TO

APPENDIX 1

INTERFACE WITH TA1800 LINEAR AMPLIFIER

CONTENTS

	<u>Para.</u>
INTRODUCTION	1
INTERCONNECTIONS	2
SETTING-UP PROCEDURES	3

Illustrations

Interconnection Diagram: MA1720-TA1800

Fig. Add. 2.1

ADDENDUM 2TOAPPENDIX 1INTERFACE WITH TA1800 LINEAR AMPLIFIERINTRODUCTION

1. This addendum provides interconnection and setting-up information for the MA1720 when used in conjunction with the Racal TA1800 10 kW linear amplifier. The setting-up procedures given utilise the OPERATE-HIGH position of the switch on the MA1720 front panel. When the OPERATE-LOW position is selected the MA1720 RF output level, and hence the TA1800 RF output level, is directly controlled by a preset potentiometer (R190), providing a reduced power output from the normal 10 kW output level.

INTERCONNECTIONS

2. The interconnections are given in Fig. Add. 2.1. The mating connector for SK6 on the MA1720 is a 15-way plug, Cannon DA15P, Racal part No. 909729, with a shell junction, DA51210-1 (Racal 912683) and a retainer, DA51220-1 (Racal 914244). 1SK1 on the TA1800 is a 26-way terminal strip, whilst the mating coaxial connectors for SK4 (MA1720) and 1SK8 (TA1800) are Transradio BN1/5 (Racal 900038).

SETTING-UP PROCEDURE

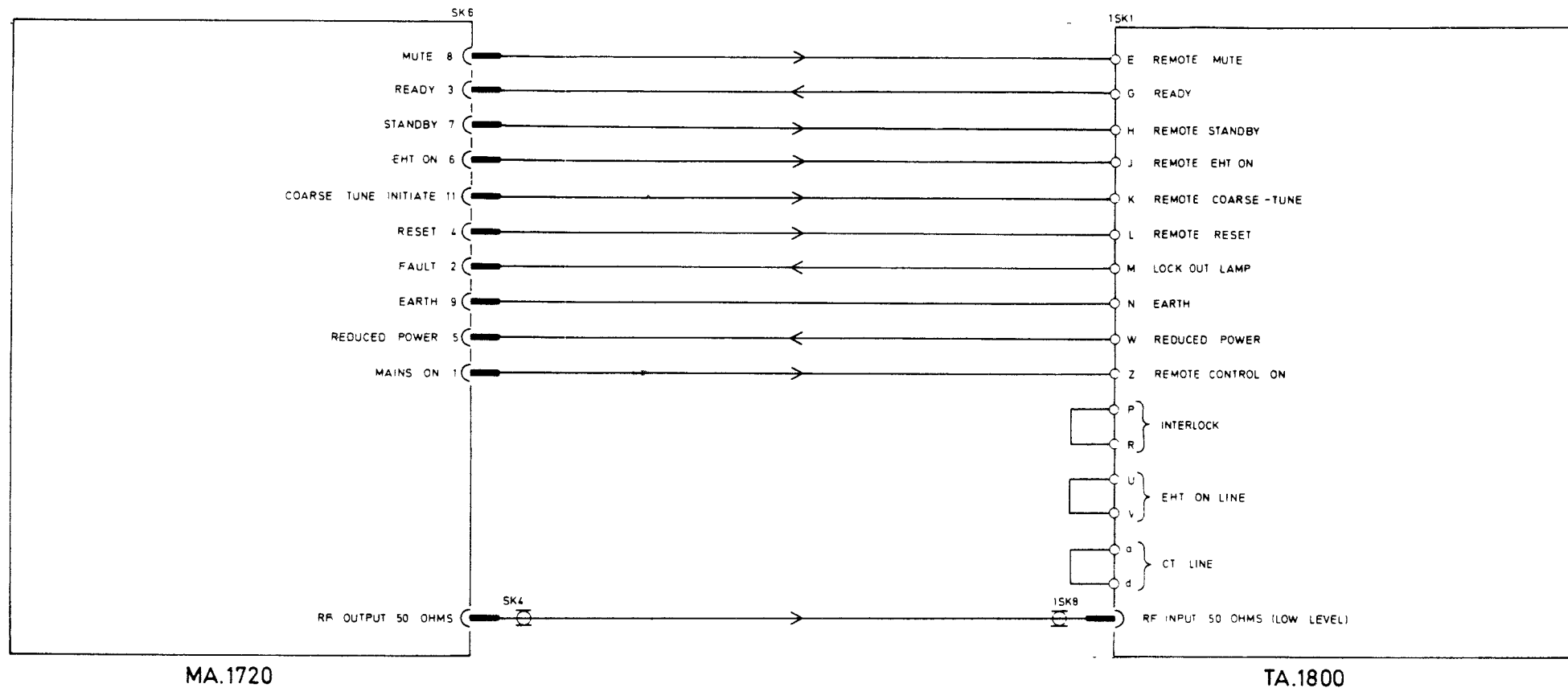
3. Before carrying out the following procedures ensure that the equipment has been correctly installed in accordance with the relevant handbooks.
4. (1) Remove the normal connection from SK6 on the MA1720, and link SK6 pins 3 and 9.
- (2) Remove the normal connection from SK4 on the MA1720, and replace with a 50 ohm dummy load (a 51 ohm 0.25 W resistor is suitable).
- (3) On the MA1720 set the MODE switch to CW and select OPERATE HIGH. Check that the READY lamp is illuminated.
- (4) Set the MA.1720 frequency selector switches to 10.0000 MHz and depress the RESET button.

- (5) Close the CW KEY (or link terminals 13 and 14 of TS1 on the MA1720).
  - (6) Set the MA1720 METER switch to RF.
  - (7) Adjust R70 on the MA1720 mixer and output board PM352 for a front panel meter indication of -3 dB (i.e. 100 mW).
- NOTE: A 0 dB meter indication equals 200 mW.
- (8) Set the MA1720 TUNE/MUTE/OPERATE switch to TUNE.
  - (9) Adjust R204 on the MA1720 low level board PM341 for a front panel meter indication of -9 dB.
  - (10) Connect the output of a two-tone audio generator to the MA1720 AUDIO 1 input (SK9 or TS1 pins 1 and 2, screen to pin 14).
  - (11) Set the audio generator for a 1000 Hz single tone output at a level of -13 dBm.
  - (12) Set the MA1720 METER switch to SET 1 and adjust the associated SET control for a front panel meter indication of 0 dB.
  - (13) Set the MA1720 to SSB SUPressed and OPERATE HIGH. Connect the RF MON socket on the MA1720 to the oscilloscope input. Set the audio generator for two tone operation. Set the frequency of the second tone for 1700 Hz and adjust the output level of the audio generator until two equal tones are present at the MA1720 output (indicated by the RF envelope falling to zero).
  - (14) Reduce the audio generator output by 6 dB i.e. for -13 dBm peak output.
  - (15) Reconnect the MA1720 RF output to the TA1800 (SK4). Do not remove the link between SK6 pins 3 and 9.
  - (16) Set the MA1720 TUNE/MUTE/OPERATE switch to TUNE.
  - (17) Connect the RF output af the TA1800 to a 10 kW (minimum) dummy load.
  - (18) Set the TA1800 CONTROL supply switch to ON and the LOCAL-REMOTE switch to LOCAL.
  - (19) At the TA1800 select FINE TUNE HOLD and AUTO.
- NOTE: The COARSE TUNE HOLD switch should be in its central position.
- (20) At the TA1800 select STANDBY ON and EHT ON.
  - (21) Check that the EHT ON lamp illuminates (after delay) followed by the FINE TUNE COMPLETE lamp.



- (22) Set the TA1800 MANUAL/AUTO switch to MANUAL.
- (23) At the MA1720 select SSB SUPressed, LOWER sideband and OPERATE HIGH.
- (24) Ensure that the audio generator is set for two-tone operation and is connected to the AUDIO 1 input.
- (25) At the TA1800 adjust the manual gain (by means of the MANUAL GAIN and MANUAL CLOCK controls) to give a PA CATHODE CURRENT meter indication of 1.75 A.
- (26) Remove the link between pins 3 and 9 on SK6 and check that the TA1800 PA CATHODE CURRENT indicates approximately 1.3 A. Note the actual meter reading.
- (27) At the TA1800 select COARSE TUNE HOLD, set the MANUAL/AUTO switch to AUTO, and then return the COARSE TUNE HOLD switch to its central position.
- (28) Adjust R65 on the TA1800 ALC 1 board PS216 for a PA CATHODE CURRENT meter indication equal to that noted at step (26).
- (29) Connect to SK6 on the MA1720 the plug removed in step (1) and set the TA1800 FINE TUNE HOLD switch to its central position.
- (30) Check that the TA1800 READY lamp illuminates.
- (31) At the MA1720 set the TUNE/MUTE/OPERATE switch to OPERATE HIGH.
- (32) Check that the output power into the dummy load is approximately 10 kW p.e.p. (5 kW mean).
- (33) Switch off the transmitter, remove all test equipment and reconnect all disturbed cables.
- (34) The transmitter is now correctly set up to provide a 10 kW output.

NOTE: For certain installations it may be necessary to re-adjust the SET 1 control to suit the particular audio line input level.



MA.1720

TA.1800