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TRANSMITTER CONTROL UNIT (Racal Type MA.1090)

TECHNICAL AND REPAIR MANUAL

BY COMMAND OF THE DEFENCE COUNCIL

Ministry of Defence

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AP 100B-01 Order 0504

MODIFICATION RECORD

The following record confirms that this publication incorporates all technical changes necessitated by the modifications listed below. Information on modification titles, classification categories and Mark applicabilities is given in Topic 2.

Mod. No.	Brief description
A9378	Replace nicad battery
TC0052	Reduce arcing on mains switch

Maintenance Manual

MA. 1090
Transmitter Control Unit

RACAL
The Electronics Group

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LETHAL WARNING

Voltages within this equipment are sufficiently high to endanger life.

Covers are NOT to be removed except by persons qualified and authorised to do so and these persons should always take extreme care once the covers have been removed.

Resuscitation instructions are given overleaf.

FIRST AID in case of Electric Shock

1. Lay victim on his back.
2. Clear victim's mouth and throat.
3. Tilt victim's head back as far as possible and raise his head.
4. Pinch victim's nostrils.
5. Take a deep breath.
6. Cover the victim's mouth with yours and blow, watching his chest rise.
   Note: Blow forcefully into adults, but gently into children.
7. Move your face away to allow victim to breathe out, watching his chest fall.
8. Repeat first five to ten breaths at a rapid rate; thereafter, take one breath every three to five seconds.
9. Keep victim's head back as far as possible all the time.

Have someone else send for a Doctor

Keep patient warm and loosen his clothing

DO NOT Give liquids until patient is conscious

HANDBOOK AMENDMENTS

Amendments to this handbook (if any), which are on coloured paper for ease of indentification, will be found at the rear of the book. The action called for by the amendments should be carried out by hand as soon as possible.

ORDERS FOR SPARE PARTS

In order to expedite handling of spare part orders please quote:-

(1) Type and serial number of equipment.

(2) Circuit reference, description, Racal part number, and manufacturer of part required.

(3) Quantity required.

NOTE: If the equipment is designed on a modular basis, please include the type and description of the module for which the replacement part is required.

RACAL
WOH8307

MA.1090 Transmitter Control Unit

MA.1090 TRANSMITTER CONTROL UNIT

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TECHNICAL SPECIFICATION

Frequency:

Freqency in the range 0.0 to 29 999.9 kHz selected by six rotary switches. Minimum increment 100 Hz. Frequency display provided by LED indicators.

Mode:

Selected by eight interlocked illuminated push-buttons as follows:-

CW (selects KEY, LSB, Supp.)
AM-6 (selects USB-6 dB)
USB-20
USB SUPP
LSB-20
LSB SUPP
ISB-20
ISB SUPP

External Entry:

Provision is made via front panel EXTERNAL socket for external frequency data entry from the MA.1083 Frequency Entry Pad. Rear panel connections are provided for external data entry from external equipment.

Transmitter Control:

Eight illuminated push-buttons are provided as follows:-

OFF:	Cancels the STANDBY and EHT ON selections.
STANDBY:	Selects the STANDBY-ON condition. Cancels OFF and EHT ON.
EHT ON:	Selects the EHT ON condition if STANDBY is already selected. Not operational when MA.1090 is used with Racal solid-state transmitters.
RESET:	Resets the transmitter trip conditions and initiates a tuning sequence.

LOW POWER: Selects the LOW POWER condition; may be cancelled by a second press.

MUTE: Cancels OPERATE and TRANSMIT, and mutes the transmitter.

OPERATE: Cancels MUTE and TRANSMIT; allows the external PTT line to control the transmit state of the transmitter.

TRANSMIT: Cancels MUTE and OPERATE. Sets the transmitter to the TRANSMIT state.

Transmitter State: Revertive indicators are provided to show the state of the transmitter. STANDBY, EHT ON, READY and TRANSMIT indicators are illuminated in green, REDUCED POWER in amber, and FAULT in red.

Status Controls: Four push-buttons designated CHECK, IN, OUT and RECALL.

CHECK: Interrogates the transmitter control settings and disables the MA.1090 front panel controls.

IN: allows data from an external source to control both the MA.1090 and the transmitter; disables the MA.1090 front panel controls.

OUT: allows the output control data to be transferred to an external control unit.

RECALL: allows subsequent recall of frequency and mode (from internal memory) without affecting the transmitter control state.

Status Indicators: Two indicators are provided; a green CONTROL ON indicator shows that control of the transmitter is available from the MA.1090. A red LINE FAULT indicator shows failure of the control link.

Serial Control System:

The SCORE (Serial Control Of Racal Equipment) format is used for the interchange of serial data. This specifies data coding and should be consulted for a more detailed specification of the serial data characteristics (Chap. 5).

Signalling Levels:

All clock and data connections are compatible with the electrical characteristics of CCITT recommendation V28 and the relevent clauses of V24.

Frame Length:

Each data frame comprises 48 bits and consists of a 16-bit preamble and a 32-bit data word.

Control Words:

The MA.1090 uses the following two words for control purposes:

WORD 1	Frequency setting
WORD 3	Mode and transmitter control

Revertive Words:

Word 0, the monitor word, is used for revertively monitored information. Words 1 and 3 may be revertively checked using the CHECK status.

Computer Word:

Word 9, the operator addressing word, is used for computer control of the MA.1090 status.

Data Transfer Rates:

Internal Clock: 19.2k bauds +4% -10%
External Clock: from 100 bauds to 20k bauds

Line Requirements:

The line connections provided conform to the following CCITT V24 descriptions:-

	V24 Designator	Description
	101	Chassis Earth
*	102	Signal Earth
*	103	Control Data output
*	104	Revertive Data input
	105	Request to send (RTS) output
	106	Ready for sending (RFS) input
*	113	Control Clock output
	114	Master Clock input
	115	Revertive Clock input
	134	Revertive Data Present input

* Denotes minimum control line requirement for basic extended control system (four lines).

Electrical Line Characteristics:	Loop Impedance: 1 kilohm max. Line Capacitance: 2500 pF max.
Transmitter Addressing:	An external unit may be connected via a rear panel connector to provide addressing facilities for up to 100 transmitters. This uses SCORE word 8, the equipment addressing word.
Control Unit Addressing:	The MA.1090 is fitted with internal address switches (00 to 99) to enable a computer to address information to a particular MA.1090 via a common highway. This uses SCORE word 9, the operator addressing word.
Computer Support:	Input and Output ports are provided for access by a computer to enter control information or to read the MA.1090 status information. These ports are also used for data exchanges between control units.
Dimensions:	Height: 178 mm Width: 483 mm Depth: 300 mm
Weight:	16 kg (approximately).
Power Requirements:	Supply voltage: 100V to 125V in 5V steps OR 200V to 250V in 10V steps Tolerance: +6% to -10% Frequency: 45 Hz to 400 Hz Power consumption: 50 VA approximately.
Environmental Conditions:	The equipment is designed to meet certain of the requirements of the British Defence Specification DEF.133, L2, for the ambient temperature range: Operating Temperature: $-10^{\circ}C$ to $+55^{\circ}C$ Storage Temperature: $-40^{\circ}C$ to $+70^{\circ}C$ Relative Humidity (non-condensing): 95% at $40^{\circ}C$.

CHAPTER 1

GENERAL DESCRIPTION

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CHAPTER 1

GENERAL DESCRIPTION

INTRODUCTION

1. The MA.1090 control unit is designed for use with an externally controlled HF transmitter assembly, such as the Racal MA.1722/MA.1720, in conjunction with, for example, the Racal TTA.1860 HF Transmitter. Frequency selection and all other functions such as mode and transmitter control, are achieved by the use serial control data which conforms to the SCORE (Serial Control Of Racal Equipment) format.

SCORE FORMAT

2. The SCORE format for serial control, as used by the MA.1090, is fully described in Chap. 5. It is based on a number of 48-bit synchronous frames, each of which contains a 16-bit preamble (synchronisation, word number identification, etc.), followed by a 32-bit data word. The total capacity of the SCORE format is sixteen 32-bit words numbered 0 to 15, each of which may be revertively checked. Of these, the MA.1090 uses word numbers 0, 1 and 3 to control the associated transmitter. Although word 0 is sent as part of the control data sequence, it does not contain any control information and is used only for revertive data. Word 1 is used to convey the frequency setting information, whilst word 3 is used for mode and transmitter control data.

3. Words 8 and 9 have been designated for equipment and operator addressing and are available for use in computer assisted control systems. Words 2, 4 and 5 of the SCORE format have been designated for HF and VHF/UHF receiver control purposes; this leaves eight undesignated words (6, 7 and 10 to 15), any or all of which may be used to expand the control system. Words 1 to 7 may be preserved in the MA.1090 internal memory for subsequent recall purposes; words 8 to 15 cannot be recalled.

ROUTINE AND NEW DATA

4. During the time that no MA.1090 front panel control settings are being changed, 'routine data' frames are sent to the associated transmitter in numerical sequence (and then repeated), at a rate determined by the clock frequency. When a front panel control setting is changed however, the routine data sequence is interrupted so that the next frame to be sent will contain the change of function information. Thus the frames are sent out of numerical sequence and priority is given to those frames containing new data. This results in the rapid transfer of the new data in order to up-date the control settings of the associated transmitter as quickly as possible.

SYNCHRONISATION

5. The 16-bit preamble at the front of each 32-bit data word contains a 6-bit sync. code consisting of a '0' followed by five consecutive '1s'. This code has to be detected at the associated transmitter for each frame before any further action may take place.

FRAME COMPARISON

6. The associated transmitter drive unit assembly contains a frame comparison circuit for error detection purposes. Each control data frame generated by the MA.1090 is sent twice and up dating of the transmitter settings may only take place provided that the two frames are identical. As the probability of two consecutive frames containing identical bit errors is small, the system provides high security against an incorrect transmitter setting.

REVERTIVE DATA

7. The format for the revertive data from the associated transmitter is the same as for the forward control data so that essentially an inverse process takes place. Frame comparison however, does not take place as the revertive data is used at the MA.1090 to provide a confidence check only, i.e. the presence or absence of the revertive data has no effect on the transmitter control functions.

CLOCK CIRCUITS

8. The clock circuits provide the timing signals required by the various parts of the system. The basic clock signal may be derived either from the internal 19.2kHz clock generator or an externally connected master clock generator.

SIGNAL-TO-LINE REQUIREMENTS

9. The signal-to-line requirements for the serial control of the associated transmitter are based on the International Telegraph and Telephone Consultative Committee (CCITT) recommendations V24 and V28; these are described in Chap. 5. Separate lines are used for data, clock and certain other control signals travelling in each direction.

PHYSICAL DESCRIPTION

10. The MA.1090 divides into three main separable assemblies, namely the front panel assembly, the power supply module and the chassis assembly.

Front Panel Assembly

11. The front panel assembly comprises the front panel together with a sub-panel module which contains the front panel board, a switch board assembly, the display board and the various front panel controls and connections. By the removal of front panel

screws the front panel assembly may be detached from the chassis assembly. Electrical connections are made via five cable and connector assemblies; three of these connect with the chassis assembly whilst the remaining two connect with the power supply module.

Power Supply Module

12. The power supply is attached to the chassis base plate with six screws, and to the rear panel with a single screw. It has an insulating top cover plate under which is located the supply voltage adjustment panel. The rear face of the module, which carries the supply input connector, the supply input fuse and four three-terminal voltage regulators mounted on a heatsink, protrudes through an aperture in the chassis assembly rear panel. Electrical connections to the remainder of the unit are made via two sockets, one for the supply on/off switching and the other for the regulated voltage outputs.

Chassis Assembly

13. The chassis assembly houses a motherboard which accomodates (via edge connectors) five printed circuit cards, namely the display processor card, the frequency card, the frequency interface card, the status card and the control processor card. Also mounted on the motherboard is an extender card which, when positioned in its stowage edge connector, provides a number of voltage and signal monitoring points. The electrical connections between the motherboard and the front panel board are made via three flexible ribbon cable and connector assemblies, whilst the external connection plugs PL1 and PL2 are mounted directly on the motherboard to protrude through apertures in the rear panel.

14. An accessory and spare fuse compartment is located in the left-hand chassis side member; it contains a push-button screen remover, a lamp remover, two spare 100 mA fuses (for the plus and minus 12V fuses FS1 and FS2 mounted on the motherboard) and a spare 1A supply input fuse. The compartment is fitted with a snap-fit cover plate. (A spare lamp is located in the non-illuminated RECALL push-button).

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CHAPTER 2

INSTALLATION INFORMATION

INTRODUCTION

1. This chapter provides information to assist in the installation of an MA.1090 into a transmitter system. The MA.1090 may be connected in a number of ways depending on the particular installation or application, ranging from a single unit controlling a single transmitter over short lines (extended control) to a computer assisted multi-address system employing several transmitters, and controlled from a remote point where the data is conveyed via a pair of data modems. Detailed installation information is therefore beyond the scope of this manual and reference should be made to the appropriate system manuals.

REAR PANEL CONNECTIONS

2. A brief description for each rear panel connection is given. Refer to Fig. 2.1 for a rear view of the MA.1090.

Power Input Socket

3. The power supply input connection mates with PL3 and is made via a 3-way socket and cable assembly. The cable connections are as follows:-

Brown	Live
Blue	Neutral
Green/Yellow	Earth

4. The 3-way socket is of the filtered inlet type (Belling Lee L.2134A, Racal No. 928265); the connections are as follows:-

L	Live
N	Neutral
⏚	Earth

Power Input Fuse

5. The power input fuse, FS1, mounted below the power input connector, is a slow-blow type, rated at 1A. The replacement is a Belling Lee L2080/1, Racal No. 922456.

NOTE: Spare fuses are located in a compartment in the left-hand member of the chassis assembly. A spare lamp is mounted in the RECALL push-button.

Earth Terminal

6. A terminal is provided on the rear panel of the MA.1090 for connection to the earthing system of the rack or cabinet.

Multi-way Plugs PL1 and PL2

7. The connections to these plugs are listed in tables 1 and 2. The actual connections required are dependant upon the particular installation and reference should be made to the respective system manual. The mating socket details are as follows:-

PL1 25-way connector, Cannon DB25S, Racal No. 915970
Shell junction, Cannon DB51213-1, Racal No. 914299
Retainer, Cannon DB5122-1, Racal No. 914245

PL2 37-way connector, Cannon DC37S, Racal No. 915656
Shell junction, Cannon DC51215-1, Racal No. 918105
Retainer, Cannon DC51222-1, Racal No. 914245

INTERNAL CONTROLS

Voltage Selector

8. The MA.1090 is fitted with a voltage selector panel which is accessible after removing the unit top cover plate and the power supply module cover plate (fig. 2.2). Ensure that the voltage selector is correctly set to suit the intended source of supply.

Earth Link

9. A two-position link, LK1, provides for isolated signal earth and chassis earth connections (position B) or common signal and chassis earth connections (position A). The location of LK1 is shown in fig. 2.2.

Operator Addressing

10. Two thumbwheel switches are mounted on the status card (fig. 2.2) for operator addressing purposes. These are for use with computer assisted systems and are described in the appropriate systems manuals.

Internal Fuses

11. Two fuses, FS1 and FS2, are fitted to the motherboard (fig. 2.2); these fuses protect the +12V and -12V supplies which are available for external use (Table 2). They are rated at 100 mA, replacement Belling Lee L754, Racal No. 915348.

MA.1090 EXTERNAL CONNECTOR

12. The EXTERNAL socket on the MA.1090 front panel is for the connection of ancillary equipment such as the Racal MA.1083 frequency entry pad. The mating connector is a 5-pin DIN plug, Farnell E43, Racal No. 918751. The connections are listed below:-

1. 0V (Earth)
2. Control Clock output
3. Serial Data input
4. External Entry Select (0V to select)
5. +12V

TABLE 1: PL1 CONNECTIONS

PL1	
1	Master Clock Input
2	Control Clock Output
3	Ready for Sending (RFS) Input
4	Revertive Clock Input
5	Revertive Data Present
6	Computer Clock
7	Computer Present
8	Exchange Clock
9	Exchange Busy
10	
11	Signal Earth
12	
13	
14	Control Data Output
15	Request to Send (RTS) Output
16	Revertive Data Input
17	
18	Computer Data
19	
20	Exchange Data
21	
22	
23	
24	Chassis Earth
25	

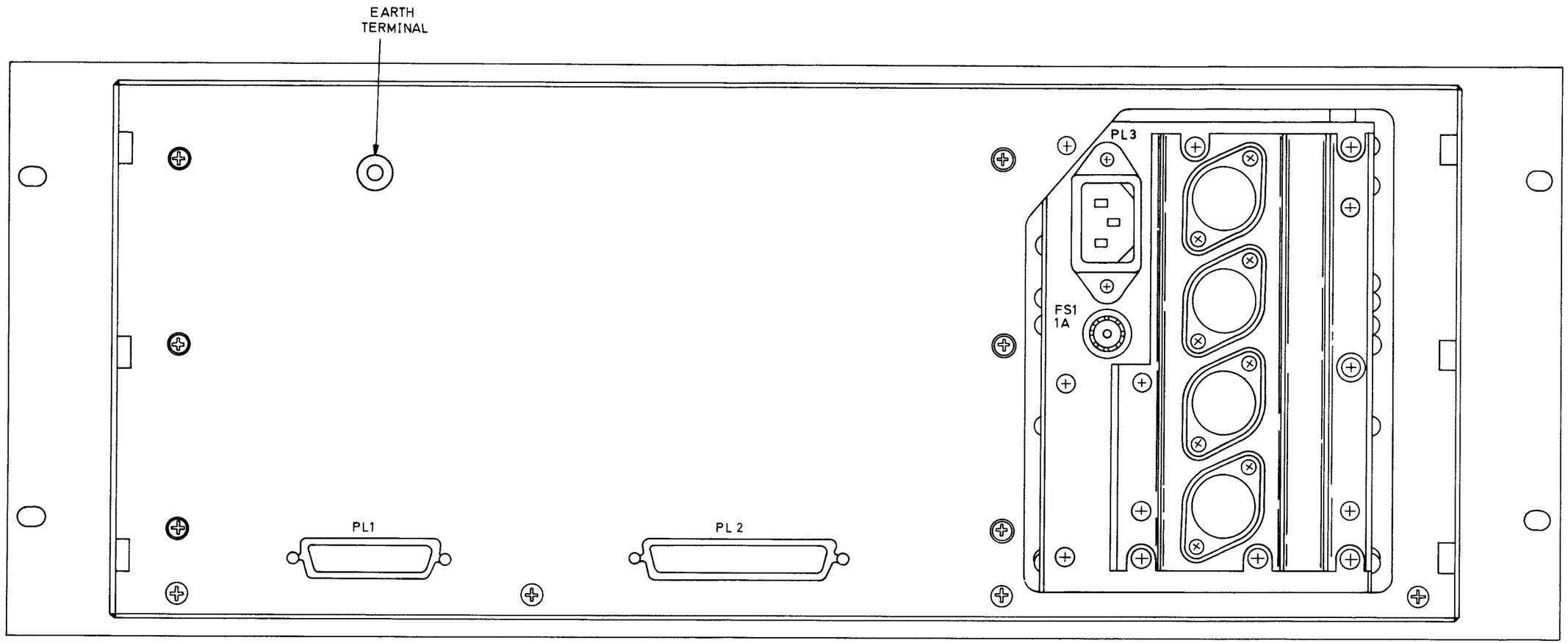
TABLE 2: PL2 CONNECTIONS

PL2		
1	Word Enable Lines	Used for Extra Word Capability
2		
3		
4		
5	Control Register Strobe	
6	Control Register Data	
7	Control Register Clock	
8	Display Register Strobe	
9	Display Register Data	
10	Display Register Clock	
11	-12V	Supply outputs available for external use. Protected by 100 mA fuses.
12	+12V	
13	0V (Earth)	
14	W	Control User Functions (Input)
15	X	
16	Y	
17	Z	
18		
19	Spare	
20	New Data	Used for Extra Word Capability
21	Word Present	
22		
23		
24	Control Register Modify - Used for Extra Word Capability	
25	Set CHECK	
26	PTT	
27		
28	External Entry/Data Inhibit	

TABLE 2 (Continued)

PL2

29	External Data	
30	Transmit	
31	Mute	
32	External Entry	
33	Auto Reset Switch	
34	D	Revertive User Functions (Outputs)
35	C	
36	B	
37	A	



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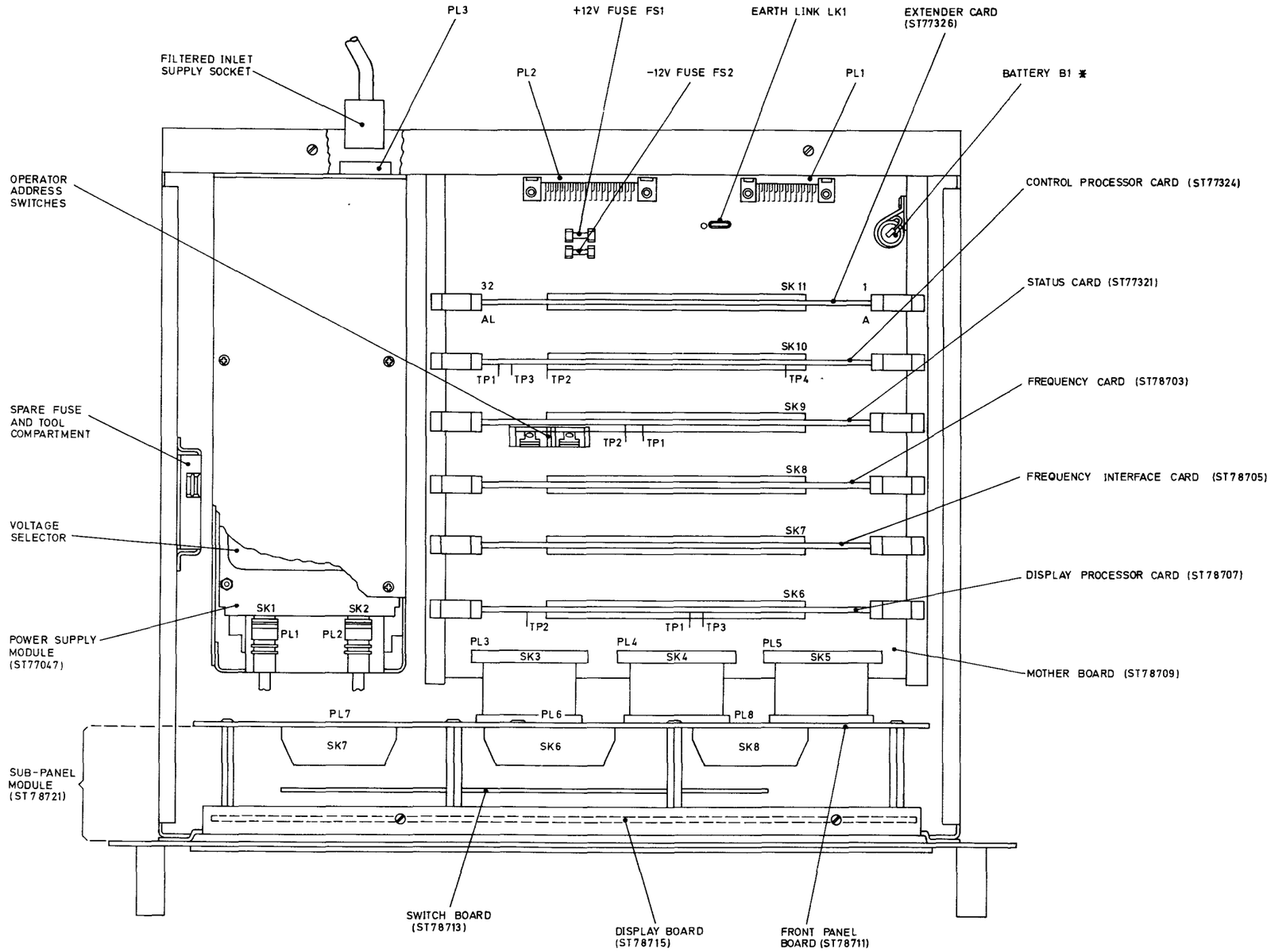
MA.1090 Control Unit:
Rear View

Fig. 2.1



* REFER TO MOD No. A9378

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Layout : MA. 1090
Plan View

Fig. 2.2

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OPERATING INFORMATION

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CHAPTER 3

OPERATING INFORMATION

INTRODUCTION

1. The operating procedures for the MA.1090 are dependent upon the particular installation in which it is employed. This chapter gives a description of each front panel control as a guide to its correct use. A front panel view of the MA.1090 is given in fig. 3.1.

FRONT PANEL CONTROLS AND INDICATORS

2. (1) SUPPLY on/off switch — A mechanically latched push-button switch which illuminates when power is applied to the MA.1090.

(2) Frequency Controls — A bank of six rotary switches is provided for the selection of the operating frequency which is then displayed by the six LED indicators.

(3) MODE - Eight illuminated push-button switches are provided for MODE selection, as follows:-

CM	(Selects KEY, LSB, suppressed)
AM-6	(Selects USB-6 dB)
USB-20	
USB SUPP	
LSB-20	
LSB SUPP	
ISB-20	
ISB SUPP	

(4) TRANSMITTER CONTROL — This section comprises eight illuminated push-button switches as follows:-

OFF: Cancels the STANDBY and EHT ON selections.

STANDBY: Selects the STANDBY condition. Cancels OFF and EHT ON.

EHT ON: Selects the EHT ON condition (if applicable) provided STANDBY is already selected.

RESET: Resets the transmitter trip conditions and initiates a tuning sequence.

LOW POWER: Selects the LOW POWER condition; may be cancelled by a second press.

MUTE: Cancels OPERATE and TRANSMIT and mutes the transmitter.

OPERATE: Cancels MUTE and TRANSMIT; allows the external PTT (Press-to-transmit) line to control the transmit state of the transmitter.

TRANSMIT: Cancels MUTE and OPERATE, sets the transmitter to the TRANSMIT state.

(5) STATUS CONTROLS

RECALL: A non-illuminated push-button which activates an internal memory to set the control unit to predetermined frequency and MODE settings without affecting the TRANSMITTER CONTROL selection.

CHECK: When CHECK is selected the front panel controls are disabled and the settings are entered into the recall store. The transmitter is interrogated and the settings are returned via the revertive data to illuminate the front panel controls and indicators. A second press cancels the CHECK status and also preserves the settings for subsequent recall (except TRANSMITTER CONTROL).

IN: The front panel controls are disabled and the settings are preserved in the recall store. Allows control settings from another MA.1090 (set to OUT) or a computer to be accepted. The IN status may be cancelled by a second press. The former frequency and MODE settings may be recovered by selecting RECALL.

OUT: This allows the control settings to be transferred to another MA.1090 set to IN.

(6) REVERTIVE INDICATORS

Eight revertively illuminated indicators are provided on the front panel, as follows:-

CONTROL ON: Illuminates in green to indicate that control of the transmitter is available from the MA.1090.

LINE FAULT: Illuminates in red to indicate failure of the control link.

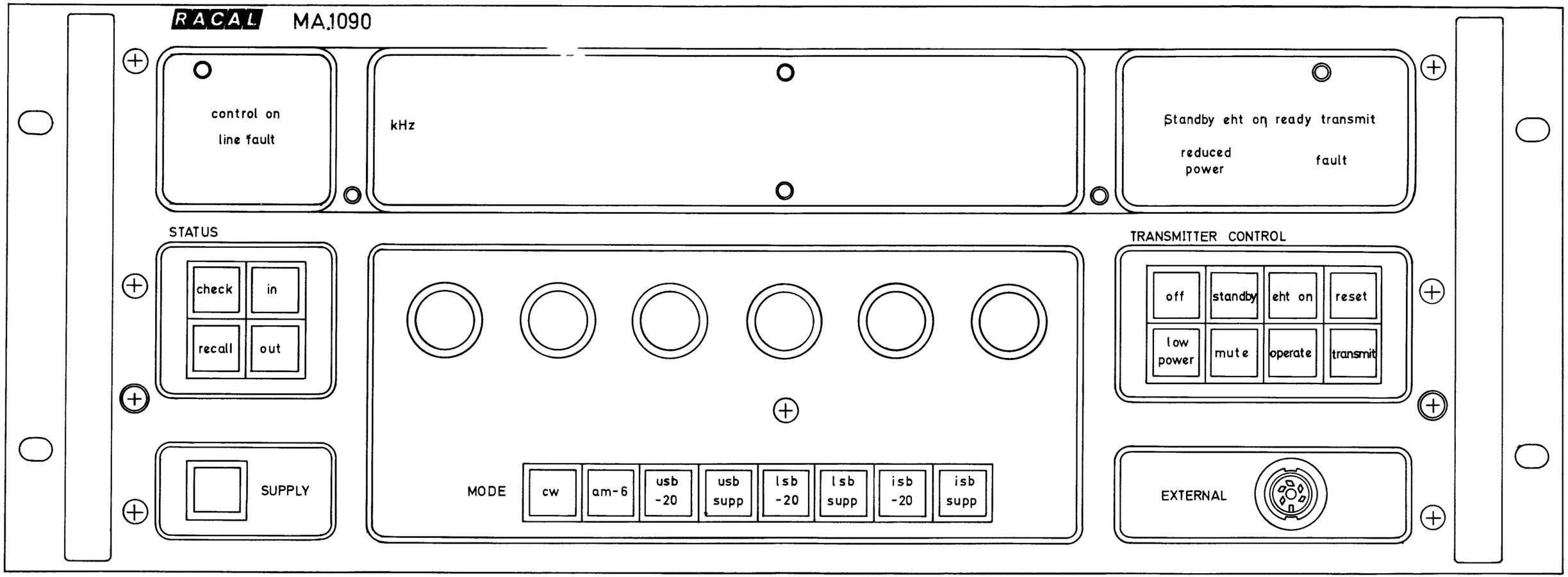
STANDBY, EHT ON, READY, TRANSMIT — Illuminate in green to indicate the state of the transmitter.

REDUCED POWER: Illuminates in amber to indicate a fault condition at the transmitter resulting in reduced output power.

FAULT: Illuminates in red to indicate a fault condition at the associated transmitter.

(7) EXTERNAL socket

Provides for the connection of an external unit such as the Racal MA.1083 frequency entry pad.



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Front Panel: MA.1090 Fig. 3.1

'POZIDRIV' SCREWDRIVERS

Metric thread cross-head screws fitted to Racal equipment are of the 'Pozidriv' type. Phillips type and 'Pozidriv' type screwdrivers are not interchangeable, and the use of the wrong screwdriver will cause damage. POZIDRIV is a registered trade mark of G.K.N. Screws and Fasteners Limited. The 'Pozidriv' screwdrivers are manufactured by Stanley Tools Limited.

CHAPTER 4

DISMANTLING AND RE-ASSEMBLY

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CHAPTER 4

DISMANTLING AND RE-ASSEMBLY

INTRODUCTION

1. This chapter provides instructions for gaining access to the printed circuits and sub-assemblies of the MA.1090. In general, the re-assembly is the reverse of the dismantling procedure.

INITIAL PROCEDURE

2. (1) Set the front panel supply push-button switch to off.

(2) Disconnect all the external cable connectors at the rear panel. (Ensure the sliding locks are released on the multi-way connectors).

(3) Remove the four screws securing the control unit to the rack or table-top cabinet.

(4) Withdraw the control unit and place it on a flat clean working surface.

(5) Remove the top cover plate, held in place with Dzus fasteners.

REMOVAL OF PRINTED CIRCUIT CARDS

3. The card guide assembly houses five printed circuit cards and the extender card. A number is printed on the component side of each printed circuit card which corresponds with the number of the mating edge connector mounted on the motherboard. Care must be taken to ensure that a removed card is replaced in the correctly numbered socket (components to the front). The socket numbers for the printed circuit cards are given in Table 1.

TABLE 1: PRINTED CIRCUIT CARD SOCKET NUMBERS

CARD	CONNECTOR
Extender	SK11
Control Processor	SK10
Status	SK9
Frequency	SK8
Frequency Interface	SK7
Display Processor	SK6

4. To remove a printed circuit card lift together the inside edges of the two card extractor levers to disengage the card from its mating edge connector, then lift the card to clear the slots cut into the card guides.

CAUTION: Do not remove or insert a card with the power applied.

LAMP REPLACEMENT

5. The illuminated push-button switches and the monitor indicators (LINE FAULT, REDUCED POWER and FAULT) accommodate a push-in type lamp (Racal No. 929284). A spare lamp is located in the non-illuminated RECALL push-button. To gain access to the monitor indicators, remove the screen and polarising filter (over the frequency display) by releasing the six knurled screws.

6. Using the screen remover located in the spare fuse compartment, place the jaws in the grooves in the opposing vertical faces of the push-button or lamp holder screen and pull out the screen. Remove the unserviceable lamp using the rubber tubing lamp remover supplied.

REMOVAL OF FRONT PANEL ASSEMBLY

7. (1) Remove the single screw from the underside of the unit securing the front sub-panel flange to the chassis base.

(2) Remove the four screws, three fitted with a nylon washer and one recessed, fitted with a spring washer, adjacent to each handle.

(3) The front panel assembly may now be disengaged from the chassis and lowered to rest on the front panel handles. Note that the control panel may be operated for maintenance purposes with the front panel assembly lowered.

(4) To completely remove the front panel assembly disconnect the three ribbon connectors from PL3, PL4 and PL5 on the motherboard, and the two connectors from the power supply module, SK1 and SK2.

REMOVAL OF POWER SUPPLY MODULE

8. (1) Remove the front panel assembly (para. 7).

(2) Remove the single screw through the rear panel adjacent to PL3.

(3) Remove the six screws, each with a spring washer, securing the module to the chassis base.

(4) Lift out the power supply module.

FRONT PANEL BOARD

9. It is necessary to remove the front panel assembly (para. 7) to gain access to the front panel board which is mounted on twelve stand-off pillars. Once the twelve securing screws, each fitted with a flat and a spring washer, are removed, the board may be hinged on the ribbon cables to reveal the switch board, the display board, the front panel push-button switches and the EXTERNAL socket. To completely remove the front panel board disconnect the three ribbon connectors from PL6, PL7 and PL8.

FRONT PANEL REMOVAL

10. (1) Remove the front panel assembly (Para. 7).

(2) Remove the collet-type frequency setting control knobs as follows:-

(a) Remove the knob end cap.

(b) Release the collet nut using an 8 mm socket or ring spanner.

(c) Remove the knob.

(3) Remove the single screw (complete with nylon washer) through the front panel above the LSB-20 push-button) attaching the front panel to the front sub-panel.

(4) Remove the front panel.

SWITCH BOARD ASSEMBLY

11. To gain access to the switch board assembly remove the front panel assembly (Para. 7) and the front panel board (Para. 9). To remove the switch board assembly, proceed as follows:-

12. (1) Remove the front panel (Para. 10).

(2) Remove the three screws, each with a spring washer, through the front sub-panel, adjacent to the frequency setting switch spindles.

(3) The switch board assembly may now be raised to hinge on the connecting cableforms.

(4) To completely remove the switch board assembly note the cableform colours before unsoldering the leads from the board pins.

DISPLAY BOARD

13. To gain access to six plug-in display integrated circuits, remove the screen and polarising filter attached to the front panel by six knurled screws. To gain access to the display board remove the front panel assembly (Para. 7) and the front panel board (Para. 9). To remove the display board proceed as follows:-

14. (1) Remove the front panel (Para. 10).

(2) Remove the switch board assembly (Para. 12).

(3) Using a 4BA spanner remove the eight hexagonal pillars, each with a spring washer, securing the display board to the front sub-panel.

(4) The board may now be raised to hinge on the connecting cableform.

MOTHERBOARD

15. Should it be necessary to gain access to the motherboard, proceed as follows:-

(1) Remove completely the front panel assembly.

(2) Remove the five printed circuit cards and the extender card.

(3) Remove the six countersunk head screws, three at each side, securing the side members to the rear panel.

(4) Remove the four domed head screws securing the lower edge of the rear panel to the chassis, and the single screw into the rear face of the power supply module.

(5) Remove the fourteen screws securing the motherboard and card guide assembly to the base of the chassis.

(6) The rear panel, motherboard and card guide assembly may now be removed as a complete sub-assembly.

CHAPTER 5

SERIAL CONTROL SYSTEM

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CHAPTER 5

SERIAL CONTROL SYSTEM

INTRODUCTION

1. This chapter describes the SCORE (Serial Control Of Racal Equipment) format, the signal-to-line requirements, and also how the control words are generated.

SCORE FORMAT

2. The SCORE format for serial control is designed to cater for numerous applications and contains ample additional capacity for expansion. It is based on a number of 48-bit synchronous frames, each of which contain a 16-bit preamble (synchronisation, word number identification, etc.) followed by a 32-bit data word. The total capacity of the system is sixteen 32-bit data words, which is equivalent to approximately 400 separate lines. All sixteen words may be revertively checked.

3. Separate lines are used for both data and clock signals travelling in each direction. These comply with CCITT V28 and the relevant clauses of V24, and are thus capatible with a wide variety of data modems (see also para. 39).

4. The SCORE data format for the control words used by the MA.1090 (word numbers 0, 1 and 3) is given in Table 1. Although word 0 is sent as part of the control sequence, it does not contain any control information and is used only for revertive data. Words 1 to 7 inclusive may be preserved in the internal memory for recall purposes; words 8 to 15 cannot be recalled. Words 2, 4 and 5 have been designated for HF and VHF/UHF Receiver control purposes whilst words 8 and 9 have been designated for equipment and operator addressing purposes (computer assisted installations). This leaves eight undesignated words (6, 7 and 10 to 15), any or all of which are available for expansion of the control system (extra word capability).

ROUTINE AND NEW DATA

5. Under static conditions, i.e. when the control data being transferred does not include change-of-function information, 'routine data' frames are sent in a continuous numerical sequence, at a rate determined by the clock frequency. When a change of function is made however, instead of allowing the transfer of the full sequence of frames to occur before the change of function is executed at the transmitter, the next frame to be sent will contain the data word carrying the change-of-function information. Thus the frames are sent out of numerical sequence and priority is given to those frames containing new data. This is achieved by the use of 'new-data' latches, where a latch is set every time a control setting is changed to indicate that the appropriate word requires transmission. The latch is reset when the new data word is transmitted.

FRAME COMPARISON

6. Error detection is accomplished (at the transmitter) by the frame comparison technique, which means that two identical frames must be received at the transmitter before a change of function can occur.

PREAMBLE

7. A 16-bit preamble is added to the front of each 32-bit data word to form one complete 48-bit frame. The preamble contains a 6-bit sync. code, a 2-bit transmit/receive (PTT) code, a control inhibit bit, a return monitor bit, a 2-bit address word security code and a 4-bit data word ident; these are described in the following paragraphs.

Sync. Code

8. The sync. code (bits 0 to 5) consists of a '0' followed by five consecutive '1s'. The maximum number of consecutive '1s' which naturally occur in serial BCD data is four, e.g., BCD7 followed by BCD8; this then makes five '1s' a unique code. For added security, the next two bits of the preamble (used for PTT) may not consist of two consecutive '1s'; this is done to 'terminate' the sync. code and so prevent the generation of a false sync. code following a link break etc.

Transmit/Receive

9. Bits 6 and 7 of the preamble are used for transmit/receive switching (PTT) where the transmit state may mute a receiver and set the associated transmitter to the transmit condition. As stated in para. 8, these two bits must not consist of two consecutive '1s'. For the transmit state bit 6 is set to a '1' and bit 7 is set to '0', whilst for the receive state, bit 6 is set to a '0' and bit 7 is set to a '1'.

Control Inhibit Bit

10. This bit of the preamble (bit 8) is used, as the name implies, to inhibit the control functions of the transmitter. When it is set to a '1', the control settings of the transmitter remain unchanged and further control instructions conveyed by the 32-bit data words are ignored. The revertive data however, is returned to the MA.1090 in the normal way. The control inhibit bit is set to a '1' in the CHECK status.

Return Monitor Bit

11. The return monitor bit is set to a '0' and is not normally used in transmitter control applications.

TABLE 1: SCORE DATA FORMAT

	BIT No.	BIT FUNCTION OR FORCED STATE	MONITOR (0)		FREQUENCY (1)		TRANSMIT MODE (3)		EQUIPMENT ADDRESSING (8)		OPERATOR ADDRESSING (9)		
PREAMBLE	0	0											
	1	1											
	2	1 SYNC											
	3	1 CODE											
	4	1											
	5	1											
	6	TRANSMIT											
	7	RECEIVE											
	8	CONTROL INHIBIT											
	9	RETURN MONITOR											
	10	ADDRESS	0		0		0		1		1		10
	11	EQUIPMENT	0		0		0		1		0		11
	12	1 DATA	0		1		1		0		1		12
	13	2 WORD	0		0		1		0		0		13
	14	3 IDENT	0		0		0		0		0		14
	15	4	0		0		0		1		1		15
DATA WORD	16		A		0		STANDBY		1		1		16
	17		B	USER FUNCTION	0	NOT USED	EHT ON		2		2		17
	18		C		0		RESET		4		4		18
	19		D		0		0		8	EQUIPMENT ADDRESS	8	OPERATOR ADDRESS	19
	20		0		0		0		10		10		20
	21		0	NOT USED	0		0	NOT USED	20		20		21
	22		0		0		0		40		40		22
	23		0		0		0		80		80		23
	24		STANDBY		1		0		FREQ.FC INH		IN		24
	25		0		2		-6	CARRIER LEVEL	MONITOR INH		DISPLAY INHIBIT		25
	26		EHT ON		4	100 Hz	-10		SLAVE		THROUGH		26
	27		CONTROL ON		8		-20		0		CHECK		27
	28		READY		1		1		0	NOT USED	PRESERVE		28
	29		0		2		2	MODE	0		STATUS INHIBIT		29
	30		0		4	kHz	4		0		OUT		30
	31		REDUCED POWER		8		8		0		MONITOR		31
	32		TRANSMIT		1		SYMMETRICAL		1		1		32
	33		FAULT		2		1	DRIVE UNIT STATE	2		2		33
	34		FC ERROR		4	10 kHz	2		4		4		34
	35		0		8		0		8	EQUIPMENT ADDRESS	8	OPERATOR ADDRESS	35
	36		0		1		HIGH PWR.		10		10		36
	37		0		2		AUTO RESET		20		20		37
	38		0		4	100 kHz	0		40		40		38
	39		0	NOT USED	8		0		80		80		39
	40		0		1		0	NOT USED	FREQ.FC INH		IN		40
	41		0		2		0		MONITOR INH		DISPLAY INHIBIT		41
	42		0		4	MHz	0		SLAVE		THROUGH		42
	43		0		8		0		0		CHECK		43
	44		0		1	10 MHz	W		0	NOT USED	PRESERVE		44
	45		0		2		X	USER FUNCTION	0		STATUS INHIBIT		45
	46		0		0	NOT USED	Y		0		OUT		46
	47		0		0		Z		0		MONITOR		47

BITS 32 TO 47 ARE A REPEAT OF BITS 16 TO 31. THIS PROVIDES HIGH SECURITY AGAINST INCORRECT ADDRESSING.

Address Security Code

12. Bits 10 and 11 are used in words 8 and 9 (in conjunction with external equipment) for equipment and operator addressing to provide added security against incorrect addressing. These two bits are set to '0' for all remaining words.

Data Word Ident

13. The last four bits of the preamble (bits 12 to 15) are used to convey the data word identification code, 0 to 15, in binary form.

DATA WORDS

14. As stated in para. 4, words 0, 1 and 3 are used by the MA.1090. These are dealt with in the following paragraphs which should be read in conjunction with Table 1. Certain words include a number of 'forced zeros' to prevent the possible occurence of five consecutive '1s' which would otherwise be mistaken for the sync. code.

WORD 0 - MONITOR

15. This word is used for revertive signalling only; although it is transferred as part of the forward control sequence it does not contain any control data.

User Functions

16. The first four bits of data word 0 provide for the revertive user functions where up to four earth (0V) signals applied to the transmitter are reproduced at rear panel connections of the MA.1090 (via the serial revertive data). The four bits are labelled A, B, C and D, and correspond with the A, B, C and D input and output connections at the transmitter and the MA.1090 respectively.

Revertive Indicators

17. The remaining operative bits of word 0 are all concerned with the revertive indicators on the MA.1090 front panel. Bit 24 is set to a '1' at the transmitter to illuminate the STANDBY indicator; similarly, bit 26, 27, 28 or 34 is set to a '1' to illuminate the EHT ON, CONTROL ON, READY or REDUCED POWER indicator respectively. Data bit 32 is set to a '1' when the transmitter is in the TRANSMIT condition, whilst bit 33 is set to a '1' to denote a FAULT condition at the transmitter. Finally, data bit 34 is set to a '1' at the transmitter following the detection of three consecutive frame comparison errors, to illuminate the LINE FAULT indicator; this indicator also illuminates if a spurious sync. code is detected in the revertive data or should a break occur in the revertive data path.

WORD 1 - FREQUENCY

18. This word is used to convey the frequency setting information to the associated transmitter, in BCD form, via data bits 24 to 45. The remaining bits are not used.

WORD 3 - TRANSMIT MODE

19. Word 3 contains the STANDBY, EHT ON and RESET selection, carrier level and MODE switching, drive unit state, high/low power switching, automatic reset and the forward user functions. Data bits 19 to 24, 35 and 38 to 43 are not used.

TRANSMITTER CONTROL

OFF, STANDBY and EHT ON Selection

20. The coding of bits 16 and 17 is controlled by the state of the OFF, STANDBY and EHT ON push-buttons; OFF sets both bits to '0', STANDBY sets bit 16 to a '1' and 17 to a '0', whilst EHT ON sets bit 17 to a '1', and 16 to a '1' only if STANDBY was previously selected.

RESET

21. Bit 18 is used for RESET. The reset push-button lamp is illuminated each time a change in frequency is made at the MA.1090; whilst this lamp is illuminated the frequency word (word 1) data is not sent to the associated transmitter (which thus remains tuned to the previously selected frequency). Once the MA.1090 has been set to display the new frequency the RESET push-button is pressed and released; the push-button lamp is extinguished, the word 1 new data latch is set, and the new frequency data is transferred to the associated transmitter. On receipt of the new frequency data the transmitter goes into the STANDBY condition, is automatically retuned to the new frequency, and then returns to the operational condition as selected at the MA.1090.

Automatic Reset

22. Bit 37 is used for automatic reset; this bit is normally set to a '1' but may be set to a '0' (when the auto-reset facility is not required) by linking pin 18 of PL2 on the MA.1090 rear panel to earth. The purpose of auto-reset is to initiate a retuning sequence at the transmitter following a frequency change at the MA.1090 (or should two consecutive frequency word frames be received which contain identical bit errors, due to line noise etc.). If the automatic reset facility is not in use, reset must be selected manually at the front panel following a frequency change.

Drive Unit State

23. The coding of data bits 33 and 34 is used to select OPERATE, MUTE or TRANSMIT, as follows:-

	BIT 34	BIT 33
OPERATE	0	0
MUTE	0	1
TRANSMIT	1	0

High/Low Power Selection

24. Bit 36 of the word 3 data is set to a '1' to select high power at the transmitter, '0' to select low power.

MODE SELECTION

25. The mode selection data is conveyed to the associated transmitter via bits 25 to 31, as tabulated below. Data bits 25, 26 and 27 are used for carrier level selection (all at '0' for suppressed carrier) whilst bits 28 to 31 are used for sideband selection. Thus for the CW mode suppressed carrier, LSB and KEY are selected, whilst -6 dB carrier level and USB are selected for AM. Since -10 dB carrier level and RTTY are not selectable by the MA.1090, data bits 26 and 30 are set permanently to '0'.

MODE	BIT NUMBER						
	31 KEY	30 RTTY	29 ISB	28 LSB	27 -20 dB	26 -10 dB	25 -6 dB
CW	1	0	0	1	0	0	0
AM-6	0	0	0	0	0	0	1
USB-20	0	0	0	0	1	0	0
USB SUPP	0	0	0	0	0	0	0
LSB-20	0	0	0	1	1	0	0
LSB SUPP	0	0	0	1	0	0	0
ISB-20	0	0	1	0	1	0	0
ISB SUPP	0	0	1	0	0	0	0

USER FUNCTIONS

26. The remaining operative bits of the word 3 data are 44 to 47; these provide for the user functions where up to four earth (0V) signals applied to the MA.1090 are reproduced at rear panel connections on the transmitter. The four bits are labelled W, X, Y and Z and correspond with the similarly marked input and output connections of the MA.1090 and associated MA.1722 respectively.

WORDS 8 and 9 - ADDRESSING

27. Word 8 is available for use by external control equipment (such as the MA.1082) for equipment addressing purposes, whilst word 9 may be detected by the MA.1090 for operator addressing purposes.

REVERTIVE DATA

28. The format for the revertive data is the same as for the control data so that essentially an inverse process takes place. Frame comparison however, does not take place and the revertive data is thus sent in single frames.

29. Provided that the control inhibit bit in the forward data preamble is not set to a '1' and that no errors occur in the control data, then the form of the revertive data is given by the following example:-

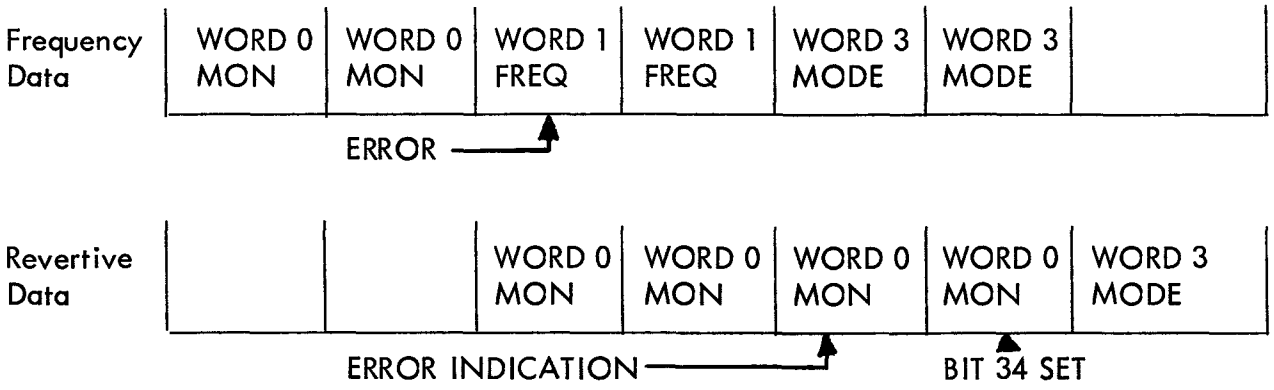
Forward Data	WORD 0 MON	WORD 0 MON	WORD 1 FREQ	WORD 1 FREQ	WORD 3 MODE	WORD 3 MODE	
Resulting Revertive Data			WORD 0 MON	WORD 0 MON	WORD 1 FREQ	WORD 0 MON	WORD 3 MODE

30. In the above example, the forward data consists of two word 0 (monitor) frames, two word 1 (frequency) frames and two word 3 (mode) frames. Since two frames have to be sent and compared before any action may take place, the revertive data resulting from the forward data given in this example is shown lagging the forward data by two 48-bit words, or 96 bits. The contents of the two blank revertive data words are dependent on the previously sent control data.

31. The two forward monitor frames are compared and, since the two frames are the same, a monitor frame is sent back. The next frame comparison however, takes place between a monitor frame and a frequency frame. The frame comparison is therefore unsuccessful and, although an error does not exist, it is arranged to send back a monitor frame. Two frequency frames are now compared, and result in a revertive frequency frame. The next two frames, frequency and mode, result in a revertive monitor frame, two mode frames result in a revertive mode frame, and so on.

Frame Comparison Failure

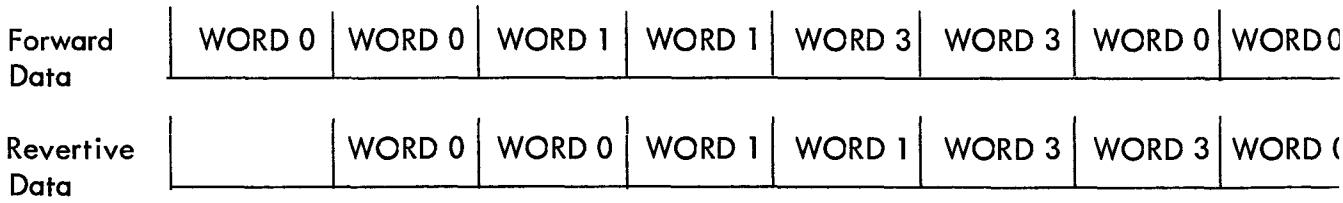
32. A frame comparison error signal is generated only on the failure of three consecutive frame comparisons, as shown in the following example.



33. In the above example, the forward data is the same as for the previous example except for a bit error in the first word 1 frequency frame. The two monitor frames result in a revertive monitor frame and the next two frames (monitor and frequency) result in a monitor frame as before. The two frequency frames are compared and this time, due to the bit error, the frame comparison is unsuccessful, resulting in a further revertive monitor frame. The next two frames (frequency and mode) being disimilar also result in a revertive monitor frame. Thus three consecutive revertive monitor frames result following the FAILURE of three consecutive frame comparisons; a frame comparison error signal is generated (i.e. bit 34 is set to a '1') and this results in the illumination of the LINE FAULT indicator on the MA.1090 front panel.

Control Inhibit

34. When the control inhibit bit (bit 8 of the preamble) is set to a '1' (CHECK status selected - para. 10), and provided that the return monitor bit (bit 9 of the preamble) is not set to a '1' (this bit is normally at '0' and is not generally used in transmitter control applications), the form of the revertive data is as shown in the following example.



35. In the above example, the control data frames are sent in numerical sequence (since the front panel controls are disabled in the CHECK status) and as no frame comparison takes place, the revertive data sequence is the same as the forward data only 48 bits later.

CLOCK CIRCUITS

36. These provide the timing signals required by the various parts of the system. The basic clock signal may be derived from one of two sources, the internal clock generator in the MA.1090 or an externally connected master clock generator.

Internal Clock

37. This is a low-stability oscillator running at 19.2 kHz (approximately) and is adequate for the majority of local and extended control applications.

External Master Clock

38. An external clock may be connected via a rear panel connector on the MA.1090, automatically overriding the internal clock. The master clock frequency may be from 100 Hz to 20 kHz, providing wide flexibility for numerous systems. This clock, which must conform to CCITT V28 and clause 114 of V24 (Para. 39), may be used for extended control systems where long lines are in use (demanding a lower clock frequency), for remote control systems using data modems, or for computer assisted systems.

SIGNAL-TO-LINE REQUIREMENTS

39. The signal-to-line requirements for the SCORE system are based on the International Telegraph and Telephone Consultative Committee (CCITT) recommendations V24 and V28, as defined in the fifth Plenary Assembly, Geneva, 1972, published by the International Telecommunications Union, 1973. The relevant parts of this document are summarised in the following paragraphs.

Recommendation V24

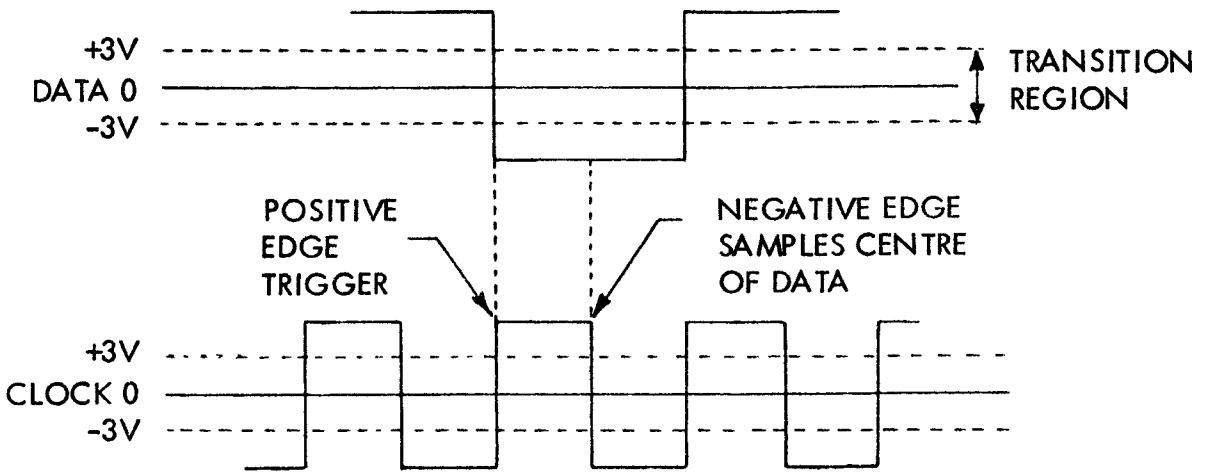
40. This is a list of definitions for interchange circuits between data terminal equipment (DTE). Separate lines are specified for data, clock and certain control signals, as listed below.

	V24	Definition
	101	Chassis Earth
*	102	0V Signal Earth
*	103	Control Data Output
*	104	Revertive Data Input
	105	Request to Send (RTS) Output
	106	Ready for Sending (RFS) Input
*	113	Control Clock Output
	114	Master Clock Input
	115	Revertive Clock Input
	134	Revertive Data Present Input

* Denote minimum control line requirements for basic extended control system.

Recommendation V28

41. Recommendation V28 specifies the electrical characteristics for unbalanced double-current interchange circuits. These are summarised below:-



(1) Binary 1 is defined as a voltage more negative than -3V.

(2) Binary 0 is defined as a voltage more positive than +3V.

(3) For timing and control circuits, binary 1 is defined as OFF, binary 0 is defined as ON.

(4) The region between +3V and -3V is defined as the transition region.

(5) All signals entering the transition region must proceed through this region to the opposite signal state and must not re-enter this region until the next significant change of signal condition.

(6) The time required for the signal to pass through the transition region during a change in state must not exceed one millisecond or 3% of one period.

(7) The maximum instantaneous rate of voltage change (slew rate) is 30V per microsecond.

(8) The maximum permissable shunt line capacitance is 2500 pF.

(9) The maximum line d.c. loop resistance is 1k

CONTROL WORD GENERATION

42. A simplified block diagram of the MA.1090 control word generation system is given in fig. 5.1. This diagram depicts the generation of words 1 and 3 both as 'routine data' words and as 'new data' words.

Routine Control Data

43. Routine control data is transferred to the associated transmitter when no new data is being generated, i.e. during the period when no control settings are being altered. The control word frame pairs are sent in numerical order (0, 1 and 3) and the complete control sequence is repeated continuously until instructed otherwise.

44. The word frame sequence is controlled by a word present 4-bit binary counter which counts sequentially from 0 to 15 and restarts at 0. The binary outputs from the word present counter are connected to the preset inputs of the new data binary counter, which is controlled by the sequence start pulse. The action of the two counters for routine control data is as follows.

45. As an arbitrary starting point, assume that the last pair of control word frames sent contained word 0, in which case the word present counter is stopped at binary 1 in readiness for the next pair of frames. The control register strobe pulse (for the next pair of frames) is inverted and then applied to the preset enable input of the new data binary counter (control processor card); the counter is preset to 1 and binary 1 is applied to the four word enable lines.

46. The control register strobe pulse is also applied to the frequency card and to the mode word circuitry on the front panel board where, after inversion, it is applied as a parallel data entry signal to the respective 32-bit output shift registers. The inverted control register strobe pulse is also applied to the reset input of the frequency word new data latch.

47. The binary 1 code on the four word enable lines is recognised by the word 1 enable detector; a logic '1' output signal is produced and this is applied as a stop signal to the word present binary counter via G1 (the output from the frequency change detector is also at logic '1'), and as an enable signal to the output gate G3 for the frequency word data contained in the 32-bit output shift register.

48. The counter clock signal, which is applied in parallel to both counters, is now disabled for a period of 32 bits; during this time however, the 32-bit frequency word is clocked out of the 32-bit output shift-register and routed via G3 to further circuitry on the control processor card which contains the preamble generator and the frame repeater.

49. The next 16 clock pulses are applied to both counters which increment. When the counters reach a count of 3, the logic '1' output from the word 3 enable detector stops the word present binary counter. The new data counter however, continuses to count searching for new data words. As, in this example, no new data is present, it counts from 3 to 15, then back to 0 and stops at 2 when the clock input signal to the two counters is again disabled for a period of 32 clock pulses. During this time the second 32-bit frequency word (word 1) is re-generated by the frame repeater (on the control processor card). When the clock signal reappears the word present counter remains stopped at binary 3 (stopped by the output from the word 3 enable detector); the new data counter however, continues to count as before, searching for new data words, and again counts from 3 to 15, back to 0 and then to 2 when the next control register strobe pulse presets it to 3.

50. The sequence is now repeated for the word 3 frame; this is followed by the all-zero word 0 frame (the word 0 circuitry is not included in fig. 1.1) and the complete routine control data sequence is then repeated starting at word 1 (words 2 and 4 to 15 are not used and therefore the word present counter will not stop at these numbers.

New Control Data

51. Every time a control setting other than frequency (i.e. a word 3 function) is altered, the new word 3 control data is required to be sent as soon as possible. The routine control data sequence is interrupted and the new data frames are inserted at the end of the routine frame currently being sent. This results in the rapid transfer of the new data frames in order to update the control settings of the associated transmitter as quickly as possible. The action of the circuit for new word 3 control data is given in para. 52. The action of the circuit when a frequency change is made is somewhat different and is described in para. 53.

52. The mode word data originating from the various front panel controls is routed to the mode word circuitry; it is also applied via G5 to the mode word new data latch such that the latch is set when a data change is detected. The next time that the new data counter reaches a count of 3 (following clock pulse 32- see para. 49), the combined outputs from the word 3 enable detector and the new data latch stop the new data binary counter at binary 3 (via G6). The next control register strobe pulse, after inversion, parallel-enables the mode word 32-bit output shift register, the new mode word data is loaded in, and is then clocked out to the control processor card via G7 and an inverting buffer. The mode word new data latch is reset via G4 (once the new data has been transferred) by the combination of the next control register strobe pulse and a '0' output from the word 3 enable detector.

53. When a frequency change is initiated at the MA.1090 front panel i.e. when the setting of any frequency switch is changed, the resulting frequency setting data is applied to the up/down counter, and also to a frequency change detector. The output from the frequency change detector changes to a '0' and this is applied to G1 to inhibit the word 1 present output signal, and to the set input of the mode word new data latch via a pulse generator and OR gate G5. Thus when a frequency change is made, the word 1 data is inhibited and the mode word new data latch is set (the reason for setting the mode word new data latch is explained in a subsequent chapter).

54. When the MA.1090 frequency switches have been set to display the required new frequency, the front panel RESET push-button is pressed; this action produces a signal which sets the frequency word new data latch, and resets the frequency change detector. The next control register strobe pulse parallel-enables the frequency word output shift register, the new frequency data is loaded in and is then clocked out to the control processor card via G3 and an inverting buffer.

55. When the new data frames have been transferred to the associated transmitter, the routine data sequence recommences where it left off(unless a further new data latch has been set).

DISPLAY REGISTER DATA

56. The display register data applied to the 32-bit input shift registers (on the frequency card and the front panel board - fig. 5.1) comes from one of the following four sources:

(1) Revertive data from the associated transmitter when CHECK is selected.

(2) Control data from the internal recall store when RECALL is selected.

(3) Control data from a computer or from another MA.1090 when IN is selected.

(4) Control data from external equipment (such as the MA.1083 frequency entry pad) connected to the front panel EXTERNAL socket.

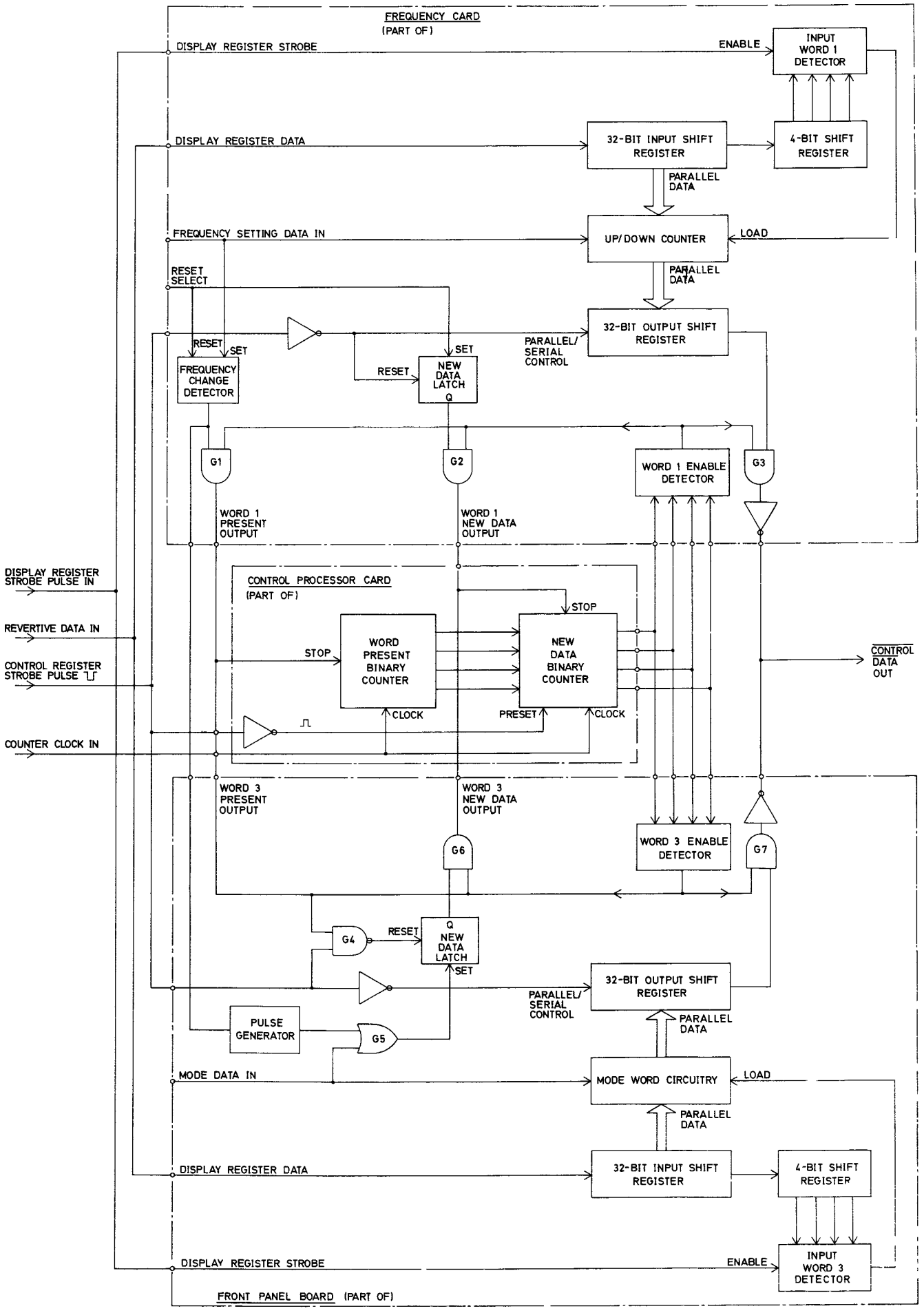
57. The display register data routing circuits are contained on the display processor card. This card (not shown in fig. 5.1) also contains the processing circuitry for the revertive monitoring data conveyed by word 0, and a pulse generator circuit which produces the display register strobe pulse at the end of each 48-bit frame.

REVERTIVE DATA

58. When the CHECK status is selected at the MA.1090, the front panel controls are disabled; further control instructions conveyed by the control data to the associated transmitter are ignored, and the actual control settings of the associated transmitter are then returned to the MA.1090 via the revertive data.

59. The revertive data is applied in parallel to the input shift registers on the frequency card and the front panel board (fig. 5.1). Since the display register strobe pulse is generated at the end of each revertive data frame, at the moment of generation, the 32 data bits of the revertive frame will be correctly positioned in the 32-bit input shift registers, and the 4-bit word identification code (bits 12 to 15 of the preamble - Table 1) will be located in the input word 1 and input word 3 detectors. If the particular word in the registers is, for example, a mode word when the display register strobe pulse enables the input word 3 detector, a load pulse is produced; this is applied to the mode word circuitry, the

parallel output data from the 32-bit input shift register is loaded in, and the actual mode word settings of the associated transmitter illuminate the appropriate push-button switches on the MA.1090 front panel.



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Simplified Block Diagram : MA.1090 Control Word Generation

Fig. 5.1

CHAPTER 6

FUNCTIONAL DESCRIPTION

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CHAPTER 6

FUNCTIONAL DESCRIPTION

INTRODUCTION

1. This chapter describes the various functions of the MA.1090 control unit in conjunction with the simplified block diagram given in fig. 6.1. This diagram uses the graphical symbol for the transmission gate, in the diagrammatical sense only, to denote electronic switching; in practice, elements other than transmission gates are used for the majority of the electronic switching circuits.

BASIC OPERATION

2. For the purposes of this description basic operation is defined as:-

(1) A STATUS push-button (CHECK, IN, OUT, RECALL) is not selected.

(2) A single MA.1090 control unit is connected to a single transmitter via the control and revertive highways.

(3) The exchange and computer highways are not in use.

(4) The EXTERNAL socket on the MA.1090 front panel is not in use.

Control Data

3. The word scanning circuits (on the control processor card) determine the control data word number sequence; for routine control data the words are sent in numerical order (0, 1, 3), whilst for new data the routine data sequence is broken by the insertion of the new data frames. Although word 0 is sent as part of the control sequence, it does not contain any control data and is used for revertive monitor purposes only (Para. 5).

4. The MA.1090 front panel control setting information is parallel-loaded, via the control circuitry, into the control output registers. The appropriate 32-bit control data word is then clocked out of the control output register (in serial form), followed by the remaining control words in the order determined by the word scanning circuits, and applied via a common line and open gate SF to the preamble generator. The 16-bit preamble is added to the front of each data word, and the resulting 48-bit frames are then repeated and applied as frame-pairs to the control highway via open gates SJ and SK.

Revertive Data

5. The revertive data from the transmitter is applied to the MA.1090 via the revertive highway and is routed via open gate SA to the monitor sync. code detector on the display processor card. This detects the presence of a correct sync. code for the monitor word (word 0) and the monitor information is routed to the front panel display via the monitor display register.

CHECK STATUS

6. When the CHECK status push-button is depressed gate SH is opened to allow the front panel settings to be preserved in the recall store (SH is then closed); these settings may subsequently be recovered by depressing RECALL (Para. 7). The MA.1090 front panel controls are disabled, the control inhibit bit of the preamble is set to a '1' (Chap. 5), and the control functions of the transmitter are held static i.e. further control instructions conveyed by the 32-bit data words are ignored. The revertive data however is returned in the normal way, as described in Para. 5, except that gate SC is now also open and the revertive data is applied to the display sync. code detector; this detects the presence of a correct sync. code in turn, for words 1 and 3, and the revertive data frames are then clocked in turn, into the display input registers on the frequency card (word 1) and the front panel board (word 3). The display input register data for each word is then applied, in parallel form, to the respective control and display circuitry and the actual transmitter settings are displayed on the MA.1090 front panel. Thus the CHECK status provides a confidence check for the MA.1090 operator in that if the MA.1090 front panel control settings remain unchanged after CHECK is selected it indicates that the transmitter has responded correctly to the instructions conveyed by the serial control data.

RECALL STATUS

7. When the RECALL push-button is depressed, gate SF is closed, gate SG is opened, gate SH (preserve function) is also opened (all on the control processor card) and gate SE (display processor card) is opened. The data contained in the recall store is clocked out via gate SG to the preamble generator and thence to the frame repeater; it is then routed, as pairs of 48-bit frames, to the control highway via gates SJ, SK, and is also routed via gate SE and the display sync. code detector to illuminate the appropriate front panel displays. At the same time, the previous front panel control settings are clocked into the recall store via the preserve gate SH for subsequent recall purposes. Thus the RECALL status may be used to rapidly set the associated transmitter to one of two sets of control settings i.e. it effectively acts as a single channel store.

OUT AND IN STATUS

8. The OUT and IN status push-buttons are used for multi-operator installations where a number of MA.1090 control panels, each connected to a transmitter, are interconnected via the exchange highway to allow the rapid transfer of control settings from one operator to another.

OUT

9. When the OUT push-button is depressed, gate SQ on the status card is opened and the control highway data (pairs of 48-bit control data frames from the frame repeater via SJ and SK) is also routed to the exchange highway (fig. 6.2). An exchange busy line is activated to prevent another operator using the OUT status.

IN

10. If the IN push-button is now depressed at control unit B (fig. 6.2) the following action results:-

(1) The preserve gate SH is opened and the present control settings are entered into the recall store (SH is then closed).

(2) Gate SD (display processor card) is opened and the data from the exchange highway is routed via open gates SM and SD to the display sync. code detector.

(3) The MA.1090 front panel controls are disabled and the exchange data output from the display sync. code detector illuminates the appropriate front panel displays.

(4) The through gate SK is closed whilst SL is opened to allow the exchange data from control unit A to control transmitter B.

11. The IN status may be cancelled by a second press, or the former control settings may be recovered by pressing RECALL.

EXTERNAL DATA

12. The EXTERNAL socket on the front panel to the MA.1090 provides for the connection of external control equipment such as the Racal MA.1083 frequency entry pad, which is used to rapidly set the transmitter to a particular operating frequency. The pad consists of a unit with numeric keys for 0 to 9 and decimal point together with an internal memory and channel selection keys for selecting one of a number of pre-determined channel frequencies.

13. Using the frequency entry pad as an example, to gain control an external entry signal is applied which opens gate SB (display processor card) and closes gate SJ (control processor card). The frequency word data from the pad is now applied to the frequency card via the display sync. code detector and SB, whilst the control data output from the frame repeater is prevented from reaching the control highway due to the closed gate SJ.

14. When the new operating frequency is correctly displayed on the MA.1090 front panel, the external entry signal is removed, gate SB closes and gate SJ opens to allow the new frequency data to be applied to the transmitter via the control highway.

COMPUTER SUPPORT

15. Many installations may be adapted for computer support. For example, the multi-operator installation mentioned in Para. 8 readily lends itself for computer assisted control as each MA.1090 contains decode circuitry for up to 100 operator addresses.

16. Data transfers from the computer to the MA.1090 are made using the computer highway, whilst the data from MA.1090 or the transmitter via the MA.1090 is conveyed to the computer via the exchange highway. The computer makes use of word 9 of the SCORE format to control the functions of the MA.1090 and, once control has been established, it may generate and send any or all of the forward data words (0, 1 and 3) together with any extra words required for ancillary control functions. The format for word 9 is given in Table 1 of Chapter 5; a brief summary of the word 9 control functions shown in fig. 6.1 is given in the following paragraphs.

Computer Present

17. When a computer is connected to the MA.1090 a link is made at a rear panel connector which opens gate SN and closes gate SM (status card). The presence of this link inhibits the IN and OUT status push-button switches on the MA.1090 front panel (to prevent interference by the MA.1090 operator), and the closure of gate SM prevents control data inputs from the exchange highway. The computer word 9 data is applied to the processing circuitry on the status card (input register, error detector, address detector, status latches and output register), whilst the transmitter control data entry from the computer (words 0, 1 and 3) is via gate SN.

IN Status

18. The IN status may be selected by the computer (word 9 status latches); the front panel controls are disabled, the computer data is accepted and displayed by the MA.1090 (via SD), and is routed to the transmitter via the control highway and gates SJ and SK.

Through

19. The computer may select the THROUGH function to route the computer data to the control highway. Gate SK is closed to block the path of the MA.1090 control data whilst gate SL is opened to complete the path between the computer highway and the control highway.

OUT Status

20. Selection of the OUT status (via word 9) opens gate SQ to route the control highway data to the exchange highway; this allows data transfers to be made from the MA.1090 to the computer.

Preserve

21. The preserve function is selected by the computer to preserve in the recall store the control settings of a particular transmitter. This may be done, for example, to preserve the control settings for subsequent recall by the MA.1090 operator following a channel change effected by a computer-assisted channel selection unit.

Monitor

22. The revertive data may be routed to the computer via the monitor gate SP and the exchange highway.

CHECK Status

23. The CHECK status is selected by the computer so that a particular transmitter may be interrogated and the control settings returned via the revertive data to be displayed on the MA.1090.

Display Inhibit

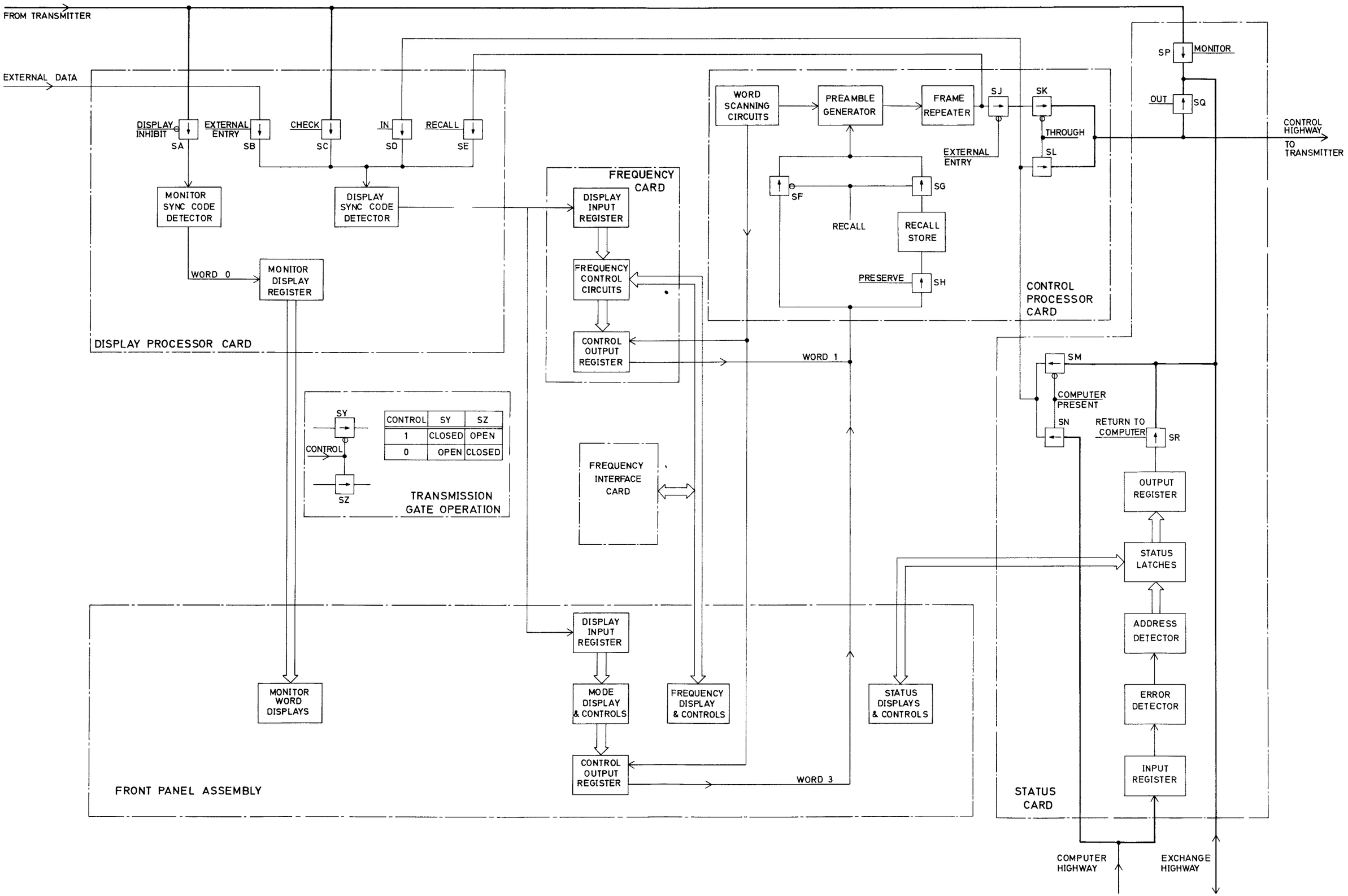
24. The display inhibit gate SA may be closed by the computer to prevent the revertive data from a transmitter under interrogation by the computer being displayed on the MA.1090, which may be controlling a different transmitter.

Status Inhibit

25. Status inhibit (not shown in fig. 6.1) is set by the computer to disable the status switches on the MA.1090 front panel and so prevent the MA.1090 operator selecting CHECK or RECALL. The IN and OUT status switches are similarly disabled when a computer is connected to the system (Para. 17).

Return to Computer

26. The return to computer gate SR is opened on command by the computer to return confirmation of the word 9 data.



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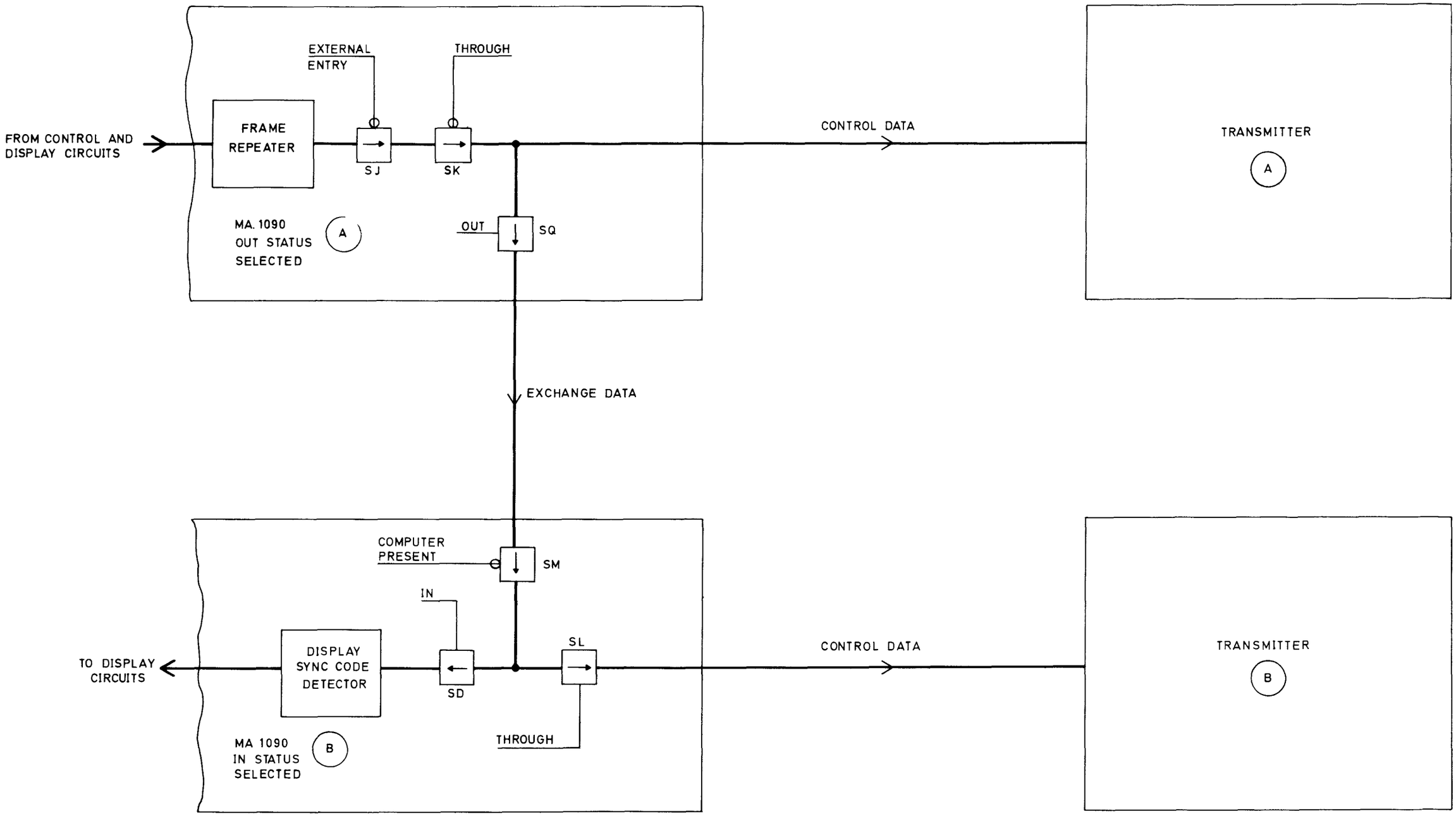
Simplified Block Diagram : MA.1090

Fig. 6-1



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Data Routing :
IN And OUT Status

Fig. 6.2

CHAPTER 7

LOGIC LEVELS

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CHAPTER 7

LOGIC LEVELS

INTRODUCTION

1. The MA.1090 uses digital integrated circuits to perform a variety of digital functions. This chapter provides an introduction to the types of devices used together with the logic levels encountered.

DIGITAL INTEGRATED CIRCUITS

2. Both TTL (transistor-transistor logic) and C-MOS (complementary metal oxide silicon) devices are used in the MA.1090. Both types of device are d.c. voltage level operated; for this reason, where an oscilloscope is used for monitoring these levels it should be set for d.c. coupling.

TTL Voltage Levels

3. Positive logic is utilised where the TTL voltage levels for the devices used in the MA.1090 are defined as follows:-

(1) Less than 0.8V at an input is a logic '0'.

(2) More than 2.4V at an input is a logic '1'.

Any voltage between these levels is a potential fault condition as the input state is then undefined.

C-MOS Voltage Levels

4. The supply and earth (0V) pins of a C-MOS device are denoted by VDD and VSS respectively. VDD is +12V except for circuitry operated from the internal battery when it is +4.5V. C-MOS voltage levels are defined as follows:-

(1) More than 70% of the supply voltage (VDD) at an input is a logic '1'.

(2) Less than 30% of the supply voltage at an input is a logic '0'.

(3) In general, the output of a C-MOS device will be VDD (supply voltage) for logic '1' and 0V for logic '0'.

NOTES: (1) Unused inputs must always be tied down to an appropriate logic voltage level (VDD or 0V). Damage may result if an unused input is left in the open-circuit condition.

(2) It is permissable to short-circuit the output of a gate to the supply (VDD) or 0V rails for short periods of time.

(3) The input/output voltage level must not generally be outside the range 0V to VDD.

(4) Some C-MOS devices are operated with VDD at +5V for buffering to TTL devices.

C-MOS HANDLING PRECAUTIONS

5. The C-MOS devices used in the MA.1090 contain circuitry to protect the inputs against damage due to high static voltages or electric fields. The following precautions however, should be taken to avoid the application of any voltage higher than the maximum rated voltages to these high impedance devices.

6. (1) Replacement C-MOS devices should not be removed from the protective packaging (metal trays, conductive plastic, conductive foam etc.) until actually required for use.

(2) The C-MOS devices used in the MA.1090 are of the dual-in-line (DIL) type, and are mounted in IC holders. A C-MOS device should not be removed from its holder whilst power is applied to the printed circuit board or card.

(3) A printed circuit board or card should not be removed from the MA.1090 whilst power is applied.

(4) All soldering and de-soldering equipment should be properly earthed.

CCITT V28 SIGNAL VOLTAGE LEVELS

7. The TTL and C-MOS output voltage levels, where necessary, are inverted and converted to plus and minus 12V signals to comply with the CCITT V28 recommendations for the serial data and clock output signals, where binary '0' is +12V and binary '1' is -12V. Similarly, the V28 revertive data and clock input signals are inverted and converted to TTL or C-MOS voltage levels, as appropriate.

NOTE: The CCITT recommendations for interchange circuits are given in Chap. 5 under the heading Signal-to-Line Requirements.

LOGIC SYMBOLS

8. The logic symbols used in this manual conform to MIL specification.

9. The '0' on an input connection, e.g.

indicates that logic '0' is the significant level, i.e. the activating input is a logic '0'. Where a '0' is not shown the activating input is assumed to be a logic '1'.

10. The '0' on an output connection indicates an inversion e.g. the '0' on the output of an AND gate converts it to a NAND gate.

11. A bar above a symbol also indicates an inversion. For example, the $\overline{Q}$ output is the inverse of the Q output.

NOTE: For some C-MOS devices, under certain conditions, $\overline{Q}$ is not the inverse of Q.

CHAPTER 8

FRONT PANEL ASSEMBLY

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CHAPTER 8

FRONT PANEL ASSEMBLY

INTRODUCTION

1. The front panel assembly comprises the front panel controls and indicators, the front panel board, the display board and the switch board. This chapter deals with the front panel assembly circuitry with the exception of the front panel board which is described in Chapter 9. The interconnection diagram of the front panel assembly is given in fig. 8.1.

PUSH-BUTTON SWITCHES

2. The SUPPLY push-button switch, S27, is a double-pole maintained-action switch where the contacts are closed on the first press and the screen remains in the depressed position until released by a further press. The remaining push-button switches, S7 to S26, are momentary-action (impulse) switches containing one pair of make contacts and one pair of break contacts which are externally wired to perform a changeover function. When a push-button is held in the depressed state, the switch contacts are maintained.

3. The push-button switch lamps, which do not move when the switches are depressed, may be replaced without affecting the switching action (Chap. 4). Screen and lamp removal tools are provided in a compartment in the left-hand side member of the unit. A spare lamp is housed in the non-illuminated RECALL push-button switch.

DISPLAY BOARD

4. The display board houses six solid state 8-pin DIL numeric indicators for the frequency display. Each indicator consists of a latch memory, matrix decoder, LED matrix driver and LED matrix. It decodes the positive logic BCD input signals from the frequency interface card (Chap. 11) via the front panel board (Chap. 9) to display the appropriate character (0 to 9) when the preset enable (PE) input is at logic '0'. A truth table is given in Table 1.

5. The indicators are mounted in sockets attached to the display board and may be removed from the front-panel side of the board after removal of the screen and polarising filter. The indicators should be handled with care as the pins are extremely brittle and will not withstand bending.

TABLE 1: NUMERIC INDICATOR TRUTH TABLE

INPUT CODING					OUTPUT
8	4	2	1	PE	
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	2
0	0	1	1	0	3
0	1	0	0	0	4
0	1	0	1	0	5
0	1	1	0	0	6
0	1	1	1	0	7
1	0	0	0	0	8
1	0	0	1	0	9
1	1	1	1	0	BLANK
X	X	X	X	1	HOLD

X denotes either 1 or 0.

Decimal Point

6. The decimal point between the 1 kHz and 100 Hz indicators (ML5 and ML6) is provided by a light emitting diode (LED) D2 which is connected to the +12Va supply via R1.

Revertive Indicators

7. The display board contains eight indicators (three lamps LP1 to LP3 and five light emitting diodes D1 and D3 to D6) which are illuminated via the (correctly coded) revertive data from the associated transmitter. The decode circuitry for these indicators is contained on the display processor card (Chap. 14).

FREQUENCY SWITCHES

8. The six frequency switches, S1 to S6, which are mounted on the switch board, are identical. They are continuously rotatable in either direction and each switch produces the coded output as given in Table 2. The coded switch data is applied to the frequency card (Chap. 10) via the frequency interface card (Chap. 11) where it is used to control a six digit up/down counter.

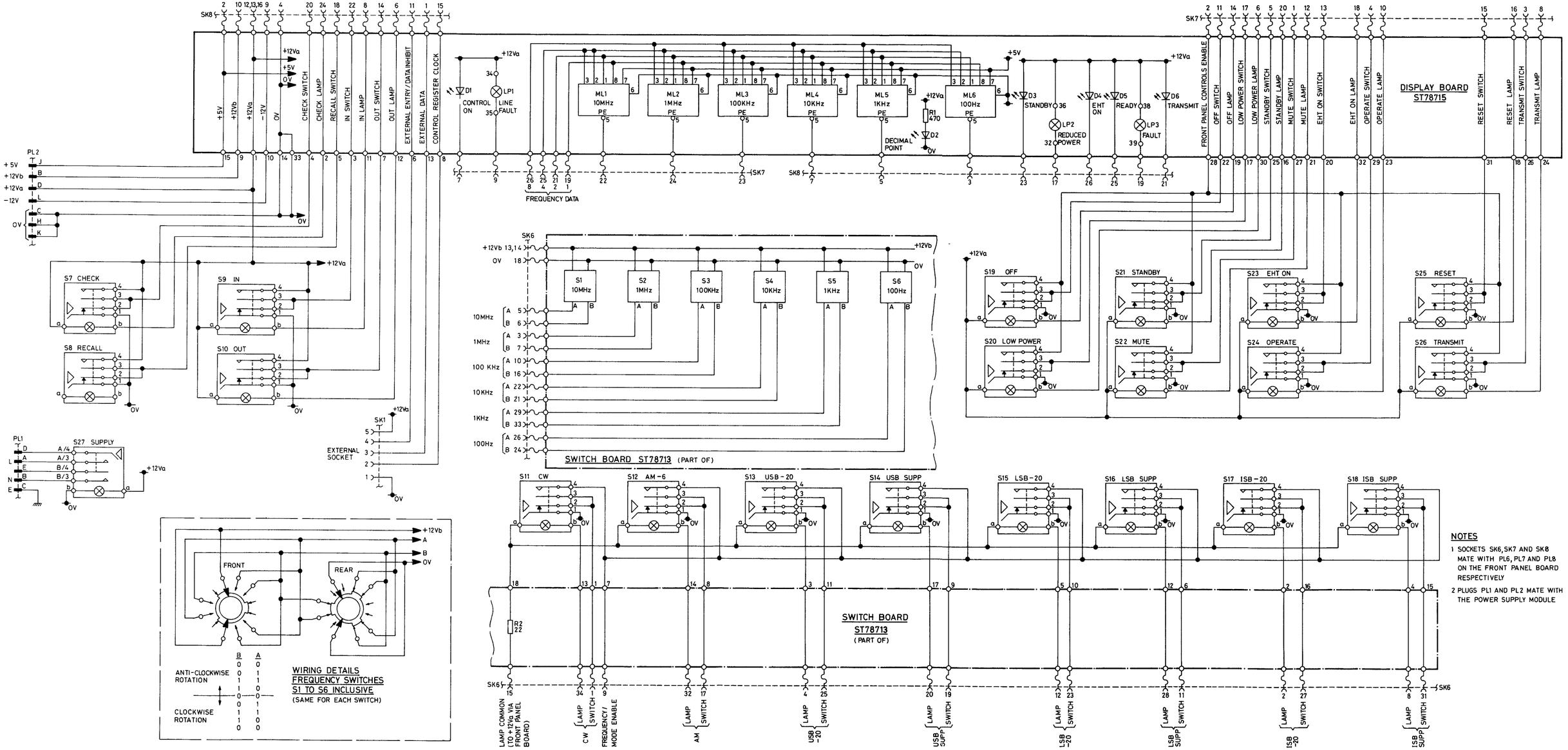
TABLE 2: FREQUENCY SWITCH OUTPUT CODING

ROTATION	B	A
ANTI-CLOCKWISE ↑	0 0 1 1	0 1 1 0
	0	0
CLOCKWISE ↓	0 1 1 0	1 1 0 0

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number	Manufacturer
		FRONT PANEL ASSEMBLY (ST 78721)				
Resistors						
R1	470	Metal Oxide		2	920758	Electrosil TR4
R2	22	Metal Oxide		2	920743	Electrosil TR4
Diodes						
D1		LED, Green (Control On)			930421	HP 5082-4955
D2		LED, Red (Decimal Point)			927748	HP 5082-4655
D3		LED, Green (Standby)			930421	HP 5082-4955
D4		LED, Green (EAT on)			930421	HP 5082-4955
D5		LED, Green (Ready)			930421	HP 5082-4955
D6		LED, Green (Transmit)			930421	HP 5082-4955
Switches						
S1		Rotary (Frequency)			CD77965	Racal
S2		Rotary (Frequency)			CD77965	Racal
S3		Rotary (frequency)			CD77965	Racal
S4		Rotary (Frequency)			CD77965	Racal
S5		Rotary (Frequency)			CD77965	Racal
S6		Rotary (Frequency)			CD77965	Racal
S7		Push-button (CHECK)			929280	Highland 31-151
S8		Push-button (RECALL)			929280	Highland 31-151
S9		Push-button (ON)			929280	Highland 31-151
S10		Push-button (OUT)			929280	Highland 31-151
S11		Push-button (CW)			929280	Highland 31-151
S12		Push-button (AM-6)			929280	Highland 31-151
S13		Push-button (USB-20)			929280	Highland 31-151
S14		Push-button (USB-SUPP)			929280	Highland 31-151
S15		Push-button (LSB-20)			929280	Highland 31-151
S16		Push-button (LSB-SUPP)			929280	Highland 31-151
S17		Push-button (ISB-20)			929280	Highland 31-151
S18		Push-button (ISB SUPP)			929280	Highland 31-151
S19		Push-button (OFF)			929280	Highland 31-151
S20		Push-button (LOW POWER)			929280	Highland 31-151

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number	Manufacturer
Switches (Contd.)						
S21		Push-button (STANDBY)			929280	Highland 31-151
S22		Push-button (MUTE)			929280	Highland 31-151
S23		Push-button (EAT ON)			929280	Highland 31-151
S24		Push-button (OPERATE)			929280	Highland 31-151
S25		Push-button (RESET)			929280	Highland 31-151
S26		Push-button (TRANSMIT)			929280	Highland 31-151
S27		Push-button (SUPPLY)			929281	Highland 31-282
Switch Screens						
		OFF			BD78044/6	Racal
		IN			BD78044/7	Racal
		OUT			BD78044/8	Racal
		CHECK			BD78044/13	Racal
		RECALL			BD78044/14	Racal
		CW			BD78044/31	Racal
		STANDBY			BD78044/75	Racal
		EHT ON			BD78044/76	Racal
		RESET			BD78044/77	Racal
		MUTE			BD78044/78	Racal
		OPERATE			BD78044/79	Racal
		TRANSMIT			BD78044/80	Racal
		LOW POWER			BD78044/81	Racal
		USB-20			BD78044/82	Racal
		USB SUPP			BD78044/83	Racal
		LSB-20			BD78044/84	Racal
		LSB SUPP			BD78044/85	Racal
		ISB-20			BD78044/86	Racal
		ISB SUPP			BD78044/87	Racal
		AM-6			BD78044/95	Racal
		Green (SUPPLY)			929283	Highland 31-951
Lamps						
LP1		Filament, 12V, 40mA (LINE FAULT)			929284	Vitality CM7354
LP2		Filament, 12V, 40mA (REDUCED POWER)			929284	Vitality CM7354
LP3		Filament, 12V, 40mA (FAULT)			929284	Vitality CM7354
LP4 to LP24		Filament, 12V, 40mA (Push-button)			929284	Vitality CM7354

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number	Manufacturer
Lampholders						
LP1		LINE FAULT			930422	Highland 31-040
		Screen, Red			930393	Highland 31-901
LP2		REDUCED POWER			930422	Highland 31-040
		Screen, Amber			930391	Highland 31-901
LP3		FAULT			930422	Highland 31-040
		Screen, Red			930393	Highland 31-901
Connectors						
PL1		Plug, 5-way			928268	Pye BMA/5/P/SW/M5H
PL2		Plug, 10-way			928270	Pye M/10/P/SW/M5H
SK1		Socket, 5-way (EXTERNAL)			918750	Farnell FE44
		Mating Plug			918751	Farnell FE43
SK6		Socket and cable assembly			BA77446/4	Racal
		Comprising:				
		PCB connector, 34-way			927425	3M's 3402-0001
		Socket, 34-way			927426	3M's 3414-3000
		Cable, flat, 34-way			927430	3M's 3365
SK7 & SK8		Connector and Cable assembly			BA77445/2	Racal
		Comprising:				
		PCB Connector, 26-way			927423	3M's 3434-0001
		Socket, 26-way			927424	3M's 3399-3000
		Cable, flat, 26-way			927429	3M's 3365
Integrated Circuits (Display Board)						
ML1		Numerical indicator			921252	HP 5082-7300
ML2		Numerical indicator			921252	HP 5082-7300
ML3		Numerical indicator			921252	HP 5082-7300
ML4		Numerical indicator			921252	HP 5082-7300
ML5		Numerical indicator			921252	HP 5082-7300
ML6		Numerical indicator			921252	HP 5082-7300
Sub-Assemblies						
		Front Panel board			ST78711	Racal
		Switch Board			ST78713	Racal
		Display Board			ST78715	Racal



NOTES

1 SOCKETS SK6, SK7 AND SK8 MATE WITH PL6, PL7 AND PL8 ON THE FRONT PANEL BOARD RESPECTIVELY

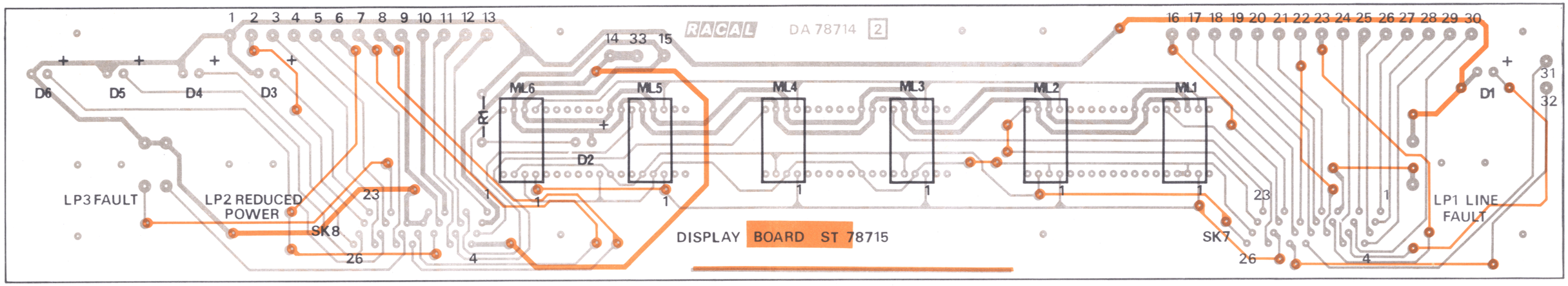
2 PLUGS PL1 AND PL2 MATE WITH THE POWER SUPPLY MODULE

RACAL

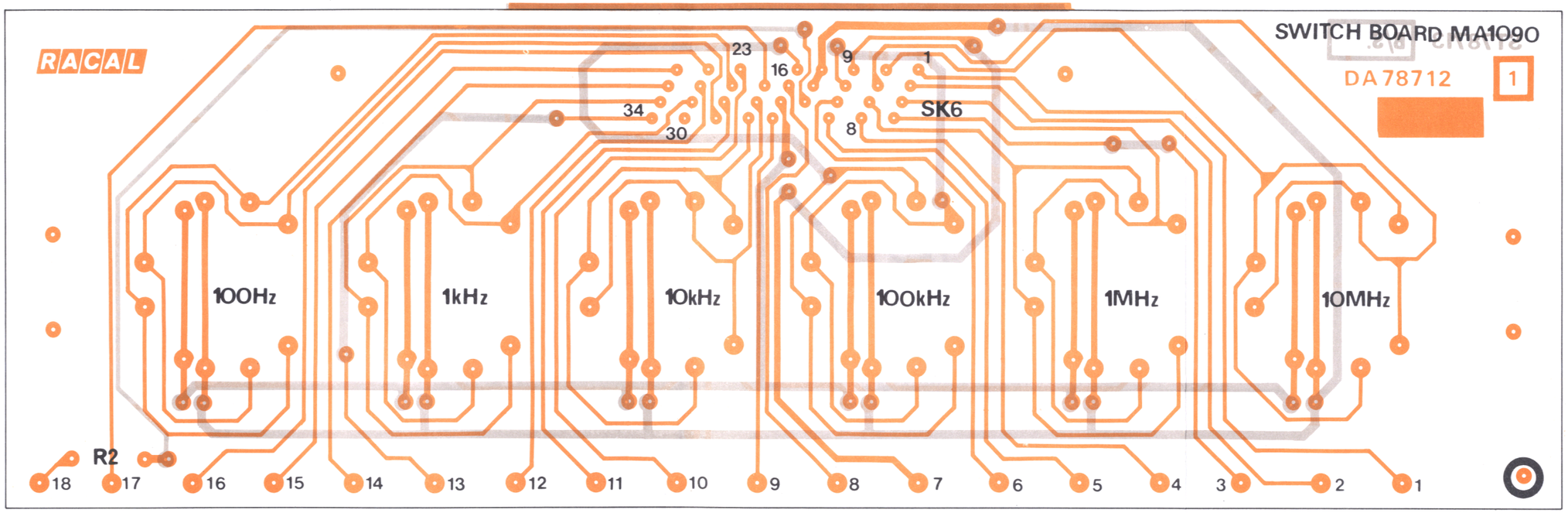
WOH8307	DC78721
2	

Interconnection Diagram : Front Panel Assembly

Fig. 8-1



Layout : Display Board Fig. 8·2



RACAL

WOH 8307	DA78712	8.3
1		1/3
WOH 8307	DA78712	8.3
1		2/3
WOH 8307	DA 78712	8.3
1		3/3

Layout: Switch Board

Fig. 8.3

CHAPTER 9

FRONT PANEL BOARD

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CHAPTER 9

FRONT PANEL BOARD

INTRODUCTION

1. The front panel board contains the word 3 (Mode word) generation circuits. It also carries a number of through connections between the front panel assembly (PL6, PL7, PL8) and the mother board (SK3, SK4, SK5).

FUNCTIONAL DESCRIPTION

2. The following functional description paragraphs should be read in conjunction with the block diagram given in Fig. 9.1.

Display Register Data

3. The inverted display register data input, at SK4 pin 31, comes from one of the following four sources:-

(1) The front panel EXTERNAL socket providing a STATUS push-button is not depressed.

(2) The revertive data highway from the transmitter when CHECK is selected.

(3) A computer (via the computer highway) or another MA.1090 control unit (via the exchange highway) when IN is selected.

(4) The control data recall store when the RECALL push-button is depressed.

Input Shift Register

4. The selected display register data is clocked into a 32-bit input shift register which consists of four cascaded eight-stage shift registers ML4, ML12, ML5 and ML3. ML4, ML12 and ML3 are dual 4-stage registers externally connected as 8-stage registers; the parallel output data from ML12 and ML3 is applied to the high/low power, drive unit state, reset and off/standby/EHT on circuits, but is only strobed into these circuits when the input word 3 detector (Para. 6) produces the required output pulse.

5. ML5 is an eight-stage shift and store register; this device has a storage latch associated with each stage for strobing data from the serial input to the parallel outputs Q1 and Q8. The data in each shift register stage is transferred to the storage register when the strobe input is at logic '1' (in this application the strobe input is permanently connected to +12 Vb), and the data in the storage register appears at the parallel outputs when the enable input is at logic '1' (Para. 6). When the enable input is at logic '0', the parallel outputs Q1 to Q8 are open circuit.

Input Word 3 Detector

6. The input word 3 detector (ML30a) produces an output pulse only when word 3 is present and correctly positioned in the register during a display register strobe pulse. The word 3 ident (bits 12 to 15 of the preamble) in the 4-stage shift register ML25b is recognised by the word detector and when the display register strobe pulse occurs an output pulse is produced. This pulse is applied to:-

(1) The enable input of ML5; the parallel outputs are enabled and these are applied to the mode circuits.

(2) AND gate G26; if the reset bit of the display register data (bit number 18) is set, then a '1' is applied via G26 to the reset circuit.

(3) AND gate G33; provided either CHECK or IN is selected (in which case the output from G34 is at '1') then a '1' is applied to G8 (for the high power bit) and to the 'drive unit state' and 'off/standby/EHT on' circuits to enable the entry of the parallel data from the input shift register. If RECALL is selected, or if the display register data is externally generated and applied via the front panel EXTERNAL socket, then the output of NAND gate G34 is at '0' and the up-dating of the high/low power, drive unit state and off/standby/EHT on' circuits is inhibited.

Power Fail Detector

7. The power fail detector circuit is powered from the internal battery supply (+12 Vb) and monitors the +12 Va supply from the power supply module. If the +12 Va supply falls to less than 10V an inhibit signal is applied to the 'drive unit state and the off/standby/EHT on' circuits to prevent data up-date.

Reset

8. When the front panel RESET push-button (connected to PL7 pin 15 - Fig. 9.1) is pressed, a +12V signal is routed via SK5 pin 5 to the frequency card where it is used to set the word 1 new data latch. Thus whilst the RESET push-button is depressed continuous word 1 frequency frames are sent.

9. When the RESET push-button is released, the reset release pulse generator (on the front panel board) produces a positive-going pulse; this is routed to the reset circuitry which applies a '1' to the P6 input of the output shift register stage ML33 (data bit 18 of the word 3 data), and also to the set input of the word 3 new data latch. The reset circuitry is described in detail in paras. 32 to 37 in conjunction with Fig. 9.2. The purpose of AND gate G35 is explained in para. 13.

Word 3 Enable Detector

10. The purpose of this stage is to detect the presence of word 3 (in inverted binary form) at the four word enable lines from the control processor card. When the presence of word 3 is detected a '1' is produced at the detector output which is routed to:-

(1) The control processor card via inverter TR12 and SK3 pin 39 to stop the word present counter at binary 3 (Chap. 12).

(2) AND gate G35 (para. 13).

(3) The new data latch ML24b and the new data signal output gate G38 (para. 11).

(4) The output gate G37 for the serial word 3 data from the output shift register (para. 14).

New Data Latch

11. The new data latch ML24b is set each time a user function change occurs, if any transmitter control push-button (LOW POWER, MUTE, OPERATE, TRANSMIT, OFF, STANDBY, EHT ON, RESET) is pressed, if any MODE push-button is pressed, or if a frequency switch position is altered (which results in the generation of the frequency switch pulse at SK4 pin 5). The next time that word 3 (in inverted binary form) is present at the word enable lines, the word 3 enable detector enables the new data latch and opens gate G38 for the word 3 new data signal; this is routed via inverter TR11 and SK3 pin 31 to the control processor card to stop the new data counter at binary 3. This ensures the word 3 frame (which contains new data) is inserted at the end of the frame currently being sent in order to update the control settings of the transmitter as soon as possible. The new data latch is reset by the control register strobe pulse when the new data word is transferred.

Frequency Display Pulse

12. The inverted control register strobe pulse, at SK3 pin 23, is applied via two inverters to a pulse generator ML23b which produces a positive-going output pulse (coincident with the positive-going edge of the inverted control register strobe pulse). This pulse is routed to the frequency display driver circuitry on the frequency interface card (Chap. 11), and also to AND gate G35 (para. 13).

13. When RESET is selected, either via the display register data or by the operation of the RESET push-button, data bit 18 is set to a '1' and is maintained at a '1' for two pairs of mode word frames. This is achieved by the use of a two-bit counter which is clocked by the output from AND gate G35.

Output Shift Register

14. The 32-bit output shift register comprises four cascaded 8-stage parallel or serial input/serial output shift registers. When the parallel/serial control input is at logic '0' the serial input is enabled and is shifted into and out of the register synchronously with the positive-going edge of the clock waveform. When the parallel/serial control input is at logic '1' the data at the parallel entry pins P1 to P8 is entered into the register independent of the clock waveform.

15. The negative-going inverted control register strobe pulse at SK3 pin 23 (from the control processor card) is inverted and then applied to the output shift register stages as a parallel data entry pulse. The parallel data is loaded in, and, provided gate G37 is opened by the word 3 enable detector output, the mode word data is clocked out of the register in serial form via G37, inverting buffer TR13 and SK4 pin 34 to the control processor card (Chap. 12).

CIRCUIT DESCRIPTION

16. The circuit diagram of the front panel board is contained on two sheets, Figs. 9.3 and 9.4. The board layout is given in Fig. 9.5.

USER FUNCTIONS (Fig. 9.3)

17. The user functions provide for up to four earth (0V) connections applied to the MA.1090 to be reproduced at the transmitter via the word 3 data. The user function connections W, X, Y and Z, at pins 14 to 17 of PL2 on the rear panel, are connected to the data inputs of a quad D-type latch ML39, and to four exclusive NOR gates G1 to G4, via SK3 pins 33, 34, 32 and 30. ML39 is clocked by the positive going control register strobe pulse, the data is latched in, and the $\overline{Q}$ outputs are taken to the remaining inputs of the exclusive NOR gates G1 to G4, and also to the output shift register stage ML40 as data bits 47, 46, 45 and 44.

18. If any user function changes, the two inputs to the respective exclusive NOR gate will be at the same logic level; this results in a logic '1' output from OR gate G5 which sets the new data latch (Fig. 9.4) via G17, G29 and G36. When the next control register strobe pulse occurs the new user functions are latched and inverted by ML39, the output from G5 changes to a '0' and the set signal is removed from the new data latch.

EXTERNAL AUTO RESET INPUT (Fig. 9.3)

19. The next operative bit of the word 3 data, in descending order, is bit 37. This bit is normally at logic '1' (+12 Va via R2, R6 and ML17), and is used at the associated transmitter to automatically initiate a re-tuning sequence following a frequency change at the MA.1090. Should the automatic reset facility not be required, bit 37 may be set to a '0' by linking pin 33 of PL2 on the MA.1090 rear panel (which connects with the front panel board via SK3 pin 28) to earth (0V).

HIGH/LOW POWER SELECTION (Fig. 9.3)

20. The front panel LOW POWER push-button switch is connected to the front panel board via PL7 pin 17. When the switch is pressed, the momentary +12V output is applied via contact bounce suppressor ML17, R15 to:-

(1) The mode word new data latch ML24b (Fig. 9.4) via G17, G29 and G36.

(2) The clock input of D-type, flip-flop ML11a; since the $\overline{Q}$ output is connected to the D input, the Q output toggles i.e. the Q output changes state for each positive-going edge applied to the clock input.

21. Thus when LOW POWER is selected at the front panel, the Q output of ML11a changes to '0'; this is applied to the P4 input of the output shift register stage ML37 (as data bit 36) and to the LOW POWER switch lamp driver TR1 via inverter ML32. ML32 is powered from the +12 Va supply so that in the event of a power failure, TR1 is turned off and thus is prevented from drawing current from the +12 Vb supply.

22. The set and reset inputs of ML11a are used to transfer the state of bit 36 of the display register data (Q4B output of ML12) to the output shift register only when either the CHECK or the IN status is selected. The selection of CHECK or IN routes the positive-going output pulse from the input word 3 detector (para. 50) to the reset input of ML11a and to one input of AND gate G8. If data bit 36 of the display register data is set to a '0' when the output pulse from the input word 3 detector occurs, then a '1' is applied to the reset input of ML11a, and a '0' is applied to the set input; the Q output is reset to '0', and this is applied to the output shift register and to the LOW POWER switch lamp driver TR1 via inverter ML32. If, however, data bit 36 of the display register data is at logic '1' then a '1' is applied to both the reset and set inputs of ML11a; this results in a '1' at the Q output, bit 36 of the output shift register data is set to a '1', and the LOW POWER switch lamp is extinguished.

DRIVE UNIT STATE (Fig. 9.3)

23. The coding of bits 34 and 33 of the output shift register data is controlled by the settings of the MUTE, OPERATE and TRANSMIT push-buttons on the front panel together with the overriding inputs from externally connected TRANSMIT and MUTE switches, or by the display register data when either CHECK or IN is selected (in which case the front panel controls are disabled - para. 28).

24. The drive unit state coding circuitry comprises two 2-input OR gates G14, G15, two D-type flip-flops ML34a, ML34b, four 2-input NAND gates G9 to G12, and a two input NOR gate G13 which is used as an inverter. An overall truth table for the coding circuitry is given in Table 1.

25. Each time the front panel TRANSMIT, OPERATE or MUTE switch is pressed (provided a STATUS push-button is not selected) a '1' is applied to the new data latch ML24b (Fig. 9.4) via OR gates G14 or G15 together with G16, G17, G29 and G36.

Lamp Driver

26. The coding of bits 33 and 34 is applied to the A and B inputs respectively of a binary to 1 to 4 decoder ML19a to illuminate the appropriate push-button switch lamp via an open-collector driver transistor TR2, TR3 or TR4. ML19a is enabled by a '0' output from the power fail detector TR5 such that should the +12 Va supply fall to less than +10V, TR5 cuts off and the enable input is removed. A conducting lamp driver transistor is thus turned off and the current drain from the +12 Vb supply is reduced.

SYMMETRICAL MODE BIT (Fig. 9.3)

27. This bit (bit 32) is not normally used in HF transmitter control applications and is set to a '0'. A '0' at the Q4A output of ML12 is applied to the D input of ML11b; this is routed to the Q output (and thence to the P8 input of ML37) by the output pulse from the input word 3 detector (para. 50) which is applied to the clock input of ML11b. The rest input applied to ML11b comes from the mode encoder (para. 39) and goes to a '1' each time a front panel MODE switch is pressed.

FREQUENCY/MODE ENABLE (Fig. 9.3)

28. The frequency/mode enable/disable circuit comprises a 3-input NAND gate G18, a two-input AND gate G19, and an inverter TR14; it is controlled by the front panel controls enable input at SK5 pin 19, the external entry/data inhibit input at SK4 pin 1 or PL8 pin 11, and the external entry input at SK5 pin 21.

29. The front panel controls enable input at SK5 pin 19 comes from the status card (Chap. 13) and is normally at logic '1' but changes to a '0' when either the CHECK or IN status is selected. The external entry/data inhibit input comes from either the front panel EXTERNAL socket (connected to PL8 pin 11) or pin 28 of PL2 on the rear panel (connected to SK4 pin 1). When this input is at logic '0', external data entry is enabled (from, for example, the MA.1083 frequency entry pad connected to the EXTERNAL socket, or from an external unit connected to PL2 on the MA.1090 rear panel), and the output data from the MA.1090 is inhibited (control processor card and display processor card - chapters 12 and 14 respectively). The external entry input at SK5 pin 21 comes from an external unit connected to PL2 pin 32 and is used to enable external data entry without inhibiting the output data from the MA.1090.

30. Provided that the CHECK or IN status is not selected then the logic '1' front panel controls enable signal at SK5 pin 19 is applied to one input of NAND gate G18, and is also routed as an enable signal to the front panel transmitter control switches (OFF, STANDBY, EHT ON, RESET, LOW POWER, MUTE, OPERATE and TRANSMIT) via PL7 pin 2. Provided also that the two external entry inputs are not active, then all the inputs to ML1 are at logic '1'; the resulting '0' at the output is applied via AND gate G19 to the base of TR14, the transistor is turned off, and a logic '1' is applied to the frequency/mode enable line.

TABLE 1: DRIVE UNIT STATE CODING

	ML34	DISPLAY DATA		ML34a	ML34b	G9			G11			G10			G12			G13
	CLOCK	BIT 34	BIT 33	$\overline{Q}$	Q	2	1	3	12	13	11	6	5	4	8	9	10	3
OPERATE	-	-	-	1	0	1	1	0	1	0	1	1	0	1	1	1	0	0
MUTE	-	-	-	1	1	1	1	0	1	1	0	1	0	1	1	0	1	0
TRANSMIT	-	-	-	0	0	1	0	1	1	0	1	1	1	0	1	1	0	1
EXT. TRANSMIT	-	-	-	X	X	0	X	1	0	X	1	1	1	0	1	1	0	1
EXT. MUTE	-	-	-	X	X	X	X	X	X	X	X	0	X	1	0	X	1	0
OPERATE		0	0	1	0	1	1	1	1	0	1	1	0	1	1	1	0	0
MUTE		0	1	1	1	1	1	0	1	1	0	1	0	1	1	0	1	0
TRANSMIT		1	0	0	0	1	0	1	1	0	1	1	1	0	1	1	0	1

X = either 1 or 0

31. Should any of the inputs applied to G18 subsequently change to a '0', then TR14 is turned on and a '0' is applied to the frequency/mode enable line.

RESET

32. A simplified diagram covering the overall reset circuitry is given in Fig. 9.2. This diagram includes the relevant circuitry on the frequency card (Chap. 10) and the control processor card (Chap. 12) is well as the circuitry on the front panel board (Figs. 9.3 and 9.4). The RESET push-button is pressed following a frequency change or to reset a trip condition at the associated transmitter.

Frequency Change

33. When a frequency change is made at the front panel, a clock signal is generated which is routed via the frequency interface card to a detector circuit on the frequency card (Fig. 9.2). This frequency change detector produces a positive-going pulse which is applied to:-

(1) A J-K fli-flop ML15a on the frequency card; the $\overline{Q}$ changes to a '0' to inhibit the inverted word present signal for the frequency word (and so inhibit the transfer of frequency data to the transmitter) whilst the Q output changes to a '1' to illuminate the RESET switch lamp via SK5 pin 7, TR15 and PL7 pin 16 on the front panel board (Fig. 9.3).

(2) The mode word new data latch ML24b on the front panel board (Fig. 9.4) via SK4 pin 5 and OR gate G36. Since the transfer of the word '1' data is inhibited, it is arranged to send a new data mode word at the end of the frame currently being sent. This is done to satisfy the requirements of externally connected multiplex equipment, and to update the frequency display.

(3) The reset input of the word present counter on the control processor card. If the word present counter is stopped at binary 1 when the frequency change is detected, the next routine control data frame to be sent to the transmitter would be a frequency frame. To prevent this from happening, the word present counter is reset to zero.

34. If the RESET push-button is now pressed, a +12V signal is applied via PL7 pin 15, contact bounce suppressor ML17, R9 and SK5 pin 5 on the front panel board (Fig. 9.3) to:-

(1) The reset input of J-K flip-flop ML15a on the frequency card; the $\overline{Q}$ output changes to a '1' to enable the output gate for the word present signal for the frequency word, whilst the Q output changes to a '0' to extinguish the RESET push-button lamp.

(2) The new data latch for the frequency word to ensure that new data frequency frames are transferred at the end of the frame currently being sent.

35. When the RESET push-button is released, a negative-going edge is applied to a pulse generator G6, G7 on the front panel board (Fig. 9.3). The positive going output pulse is applied to:-

(1) The clock input of J-K flip-flop ML24a (Fig. 9.4). The Q output changes to a '1' and this is routed to the P6 input of the output shift register stage ML33 (as data bit 18), and to the D input of a 4-stage shift register ML25a (connected as a D-type). This stage maintains bit 18 at a '1' for one pair of mode word frames (para. 36).

(2) The mode word new data latch ML24b (Fig. 9.4) via OR gate G36.

Frequency Display Pulse

36. The inverted control register strobe pulse from the control processor card is applied to the front panel board via SK3 pin 23 (Fig. 9.4) and is routed to:-

(1) The reset input of the word 3 new data latch ML24b.

(2) A pulse generator comprising D-type flip-flop ML23b (reset applied after time constant R53, C9). The positive-going output pulse is applied to the display section of the frequency interface card (Chap. 11) via SK5 pin 31, and to AND gate G35 where it is gated with the output from the word 3 enable detector. Since the output of G35 is applied to the clock input of ML25a, after the transfer of one pair of mode word frames following the generation of the reset release pulse, the Q1 output of ML25a pulses to '1' (reset applied after time constant R51, C8), ML24a is reset and data bit 18 returns to a '0'.

Reset via Display Register Data (Fig. 9.4)

37. A '1' at the Q2A output of the input shift register stage ML3 is gated (G26) with the output from the input word 3 detector to apply a '1' to the set input of ML24a; the Q output is set to a '1' and this is applied to the P6 input of the output shift register stage ML33 as data bit 18.

MODE (Fig. 9.4)

38. Data bits 31 down to 25 are used for mode selection. The eight MODE switches on the front panel are connected to the mode encoder circuit comprising OR gates G20, G21, priority encoder ML6, transmission gates ML13, ML14 and analogue latches ML16, ML17 with resistors R41 to R47. The seven bit mode selection code, either from the input shift register stage ML5 or the transmission gates, is stored in the analogue latches and is then routed to the parallel inputs of the output shift register stage ML18.

TABLE 2: MODE SELECTION CODING

MODE	ML6									ML 14a/ 1	ML 13c/ 8	BIT NUMBER						
	D5	D4	D3	D2	D1	D0	Q2	Q1	Q0			31 KEY	30 RTTY	29 ISB	28 LSB	27 -20	26 -10	25 -6
CW	0	0	0	1	0	0	0	1	0	1	0	1	0	0	1	0	0	0
AM-6	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1
USB-20	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0
USB SUPP	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
LSB-20	0	0	1	0	0	0	0	1	1	0	0	0	0	0	1	1	0	0
LSB SUPP	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0
ISB-20	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1	0	0
ISB SUPP	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

39. The one-of-eight code from the MODE switches (the output from a selected switch momentarily pulses to +12V) is converted to the required 7-bit code by the priority encoder ML6 in conjunction with G20, G21 and the transmission gates (Table 2). When any MODE push-button is pressed, the group select output at ML6 pin 14 momentarily goes to logic '1'; this output enables the transmission gates, sets the new data latch ML24b via G29 and G36, and is also used for switch contact bounce suppression (ML16 and resistors R31 to R38).

Mode Switch Lamp Decoder (Fig. 9.4)

40. The mode switch lamp decoder comprises OR gate G22, NOR gates G23, G24, G25, C-MOS-to-TTL inverting buffers ML8, and a TTL-to-decoder ML7. A truth table for the decoder is given in Table 3.

TABLE 3: MODE SWITCH LAMP DECODER

	ML7												ML9		
	INPUT				OUTPUT								PIN	PIN	PIN
	8	4	2	1	9	8	7	5	3	2	1	0	9	10	6
CW	1	0	0	0	1	0	1	1	1	1	1	1	0	1	0
AM-6	1	0	0	1	0	1	1	1	1	1	1	1	1	0	0
USB-20	0	0	1	1	1	1	1	1	0	1	1	1	0	0	1
USB SUPP	0	0	0	1	1	1	1	1	1	1	0	1	0	0	1
LSB-20	0	0	1	0	1	1	1	1	1	0	1	1	0	0	1
LSB SUPP	0	0	0	0	1	1	1	1	1	1	1	0	0	0	1
ISB-20	0	1	1	1	1	1	0	1	1	1	1	1	0	0	1
ISB SUPP	0	1	0	1	1	1	1	0	1	1	1	1	0	0	1

41. When the CW mode is selected, the decimal 8 output from ML7 is set to a '0' (Table 3); this is routed to one input of NOR gate G24, and since the remaining inputs are also at '0', the output goes to a '1' and the CW switch lamp is illuminated via inverter TR6 and PL6 pin 34. For the AM-6 mode, a '0' at the decimal 9 output of ML7 is applied to G23 and the resulting '1' at the output illuminates the AM-6 switch lamp via inverter TR7 and PL6 pin 32. The remaining mode switch lamps are illuminated directly by the appropriate logic '0' output from ML7 (Table 3).

OFF, STANDBY AND EHT ON (Fig. 9.4)

42. The remaining operative bits of the word 3 data are 17 and 16; these are concerned with the transmitter control functions OFF, STANDBY and EHT ON.

43. If control is via the display register data (IN or CHECK status), the logic levels at the Q3A and Q4A outputs of ML3 are applied to the D inputs of ML21a and ML21b respectively. When the next positive-going pulse is produced by the input word 3 detector (para. 50), which is applied to the clock inputs of ML21a and ML21b, the levels at each D input are transferred to the associated Q outputs and hence to the output shift register as bits 17 and 16.

Front Panel OFF Selection

44. When the OFF push-button is pressed, the momentary +12V signal at PL7 pin 11 is routed to the reset input of ML21b, and via OR gate G27 to the reset input of ML21a. The Q outputs, and hence bits 17 and 16 of the output data, are thus both reset to '0'. The '1' output from G27 is also used to set the new data latch ML24b (para. 49) via G29 and G36.

Front Panel STANDBY Selection

45. A momentary +12V signal from the STANDBY push-button, at PL7 pin 5, is routed to the set input of ML21b and via G27 to the reset input of ML21a. The Q output of ML21b, and hence bit 16, is set to a '1' whilst the Q output of ML21a (and data bit 17) is reset to '0'. The '1' output from G27 also sets the new data latch, as for OFF (para. 44).

Front Panel EHT ON Selection

46. The momentary +12V signal from the EHT ON push-button, at PL7 pin 13, is routed to AND gate G28; the EHT ON condition may thus only be selected if STANDBY is already selected ('1' at the Q output of ML21b). The '1' output from G28 is applied to the set input of ML21a, the Q output is set to a '1', and thus for EHT ON data bits 17 and 16 are both set to '1'.

Lamp Decoder

47. The Q outputs of ML21a and ML21b are also taken to the B and A inputs respectively of a binary to 1-of-4 decoder ML19b which controls the illumination of the OFF, STANDBY and EHT ON switch lamps via driver transistors TR8, TR9 and TR10 (Table 4). ML19b is enabled by a '0' output from the power fail detector TR5 (fig. 9.3) such that should the +12 Va supply fall to less than +10V, TR5 cuts off and the enable input is removed. A conducting lamp driver transistor is thus turned off and the current drain from the +12 Vb supply is reduced.

TABLE 4: OFF, STANDBY AND EHT ON LAMP DECODER

CONDITION	ML19b				
	INPUT		OUTPUT		
	B	A	0	1	3
OFF	0	0	1	0	0
STANDBY	0	1	0	1	0
EHT ON	1	1	0	0	1

WORD 3 ENABLE DETECTOR (Fig. 9.4)

48. This stage detects the presence of word 3, in inverted binary form, at the four word enable lines (SK3 pins 25, 27, 14 and 21) from the control processor card (Chap. 12). These lines are connected to A, B and enable inputs of a binary to 1-of-4 decoder ML30b in such a manner that when inverted binary 3 is present, the output at ML30b pin 10 goes to a '1'. This signal is applied to:-

(1) The control processor card, via output inverter TR12 and SK3 pin 29, when it is used to stop the word present counter at binary 3.

(2) The K input of the new data latch ML24b (para. 49).

(3) AND gate G35 where it is gated with the frequency display pulse to control the mode frame counter stage ML25a (para. 36).

(4) AND gate G37 to complete the path for the control register data from the output shift register, which is routed to the control processor card via inverting buffer TR13 and SK4 pin 34.

(5) AND gate G38 for the new data output from the new data latch ML24b.

NEW DATA LATCH (Fig. 9.4)

49. The new data latch consists of a J-K flip-flop ML24b. A logic '1' is applied to the set input each time a user function changes, when any frequency switch is operated, or when any MODE or TRANSMITTER CONTROL push-button is pressed; this sets the Q output to a '1' which, provided the word 3 enable output signal is present, is routed via G38, inverting buffer TR11 and SK3 pin 31, to the control processor card to stop the new data counter at binary 3. The new data latch is reset by the inverted control register strobe pulse (via two inverters of ML32) when the new data word 3 is sent, as the logic '1' word 3 enable detector output is applied to the K input of ML24b (the J input is connected to 0V).

INPUT WORD 3 DETECTOR (Fig. 9.4)

50. This circuit comprises a 4-stage shift register ML25b, AND gate G32, OR gate G31, and a binary to 1-of-4 decoder ML30a. When word 3 is correctly positioned in the input shift register, the word 3 identification code (bits 12 to 15 of the preamble) is present at the Q outputs of ML25b; the resulting logic '1' Q3 and Q4 outputs are gated by G32 to produce a '1' at the A input of ML30a, whilst the logic '0' Q1 and Q2 outputs produce a '0' (via G31) at the B input of ML30a. The negative going inverted display register strobe pulse, at SK4 pin 29, is applied to the enable input of ML30a, and a '1' is produced at the Q1 output of ML30a.

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number	Manufacturer
		FRONT PANEL BOARD (ST 78711)				
Resistors						
R1	12k	Metal Oxide		2	917952	Electrosil TR4
R2	12k	Metal Oxide		2	917952	Electrosil TR4
R3	12k	Metal Oxide		2	917952	Electrosil TR4
R4	12k	Metal Oxide		2	917952	Electrosil TR4
R5	12k	Metal Oxide		2	917952	Electrosil TR4
R6	12k	Metal Oxide		2	917952	Electrosil TR4
R7	12k	Metal Oxide		2	917952	Electrosil TR4
R8	12k	Metal Oxide		2	917952	Electrosil TR4
R9	12k	Metal Oxide		2	917952	Electrosil TR4
R10	12k	Metal Oxide		2	917952	Electrosil TR4
R11	12k	Metal Oxide		2	917952	Electrosil TR4
R12	12k	Metal Oxide		2	917952	Electrosil TR4
R13	12k	Metal Oxide		2	917952	Electrosil TR4
R14	68k	Metal Oxide		2	916478	Electrosil TR4
R15	12k	Metal Oxide		2	917952	Electrosil TR4
R16	22k	Metal Oxide		2	913493	Electrosil TR4
R17	22	Metal Oxide		2	920743	Electrosil TR4
R18	22k	Metal Oxide		2	913493	Electrosil TR4
R19	22k	Metal Oxide		2	913493	Electrosil TR4
R20	22k	Metal Oxide		2	913493	Electrosil TR4
R21	22	Metal Oxide		2	920743	Electrosil TR4
R22	22	Metal Oxide		2	920743	Electrosil TR4
R23	22	Metal Oxide		2	920743	Electrosil TR4
R24	12k	Metal Oxide		2	917952	Electrosil TR4
R25	12k	Metal Oxide		2	917952	Electrosil TR4
R26	12k	Metal Oxide		2	917952	Electrosil TR4
R27	12k	Metal Oxide		2	917952	Electrosil TR4
R28	12k	Metal Oxide		2	917952	Electrosil TR4
R29	2k7	Metal Oxide		2	916548	Electrosil TR4
R30	12k	Metal Oxide		2	917952	Electrosil TR4
R31	12k	Metal Oxide		2	917952	Electrosil TR4
R32	12k	Metal Oxide		2	917952	Electrosil TR4
R33	12k	Metal Oxide		2	917952	Electrosil TR4
R34	12k	Metal Oxide		2	917952	Electrosil TR4
R35	12k	Metal Oxide		2	917952	Electrosil TR4

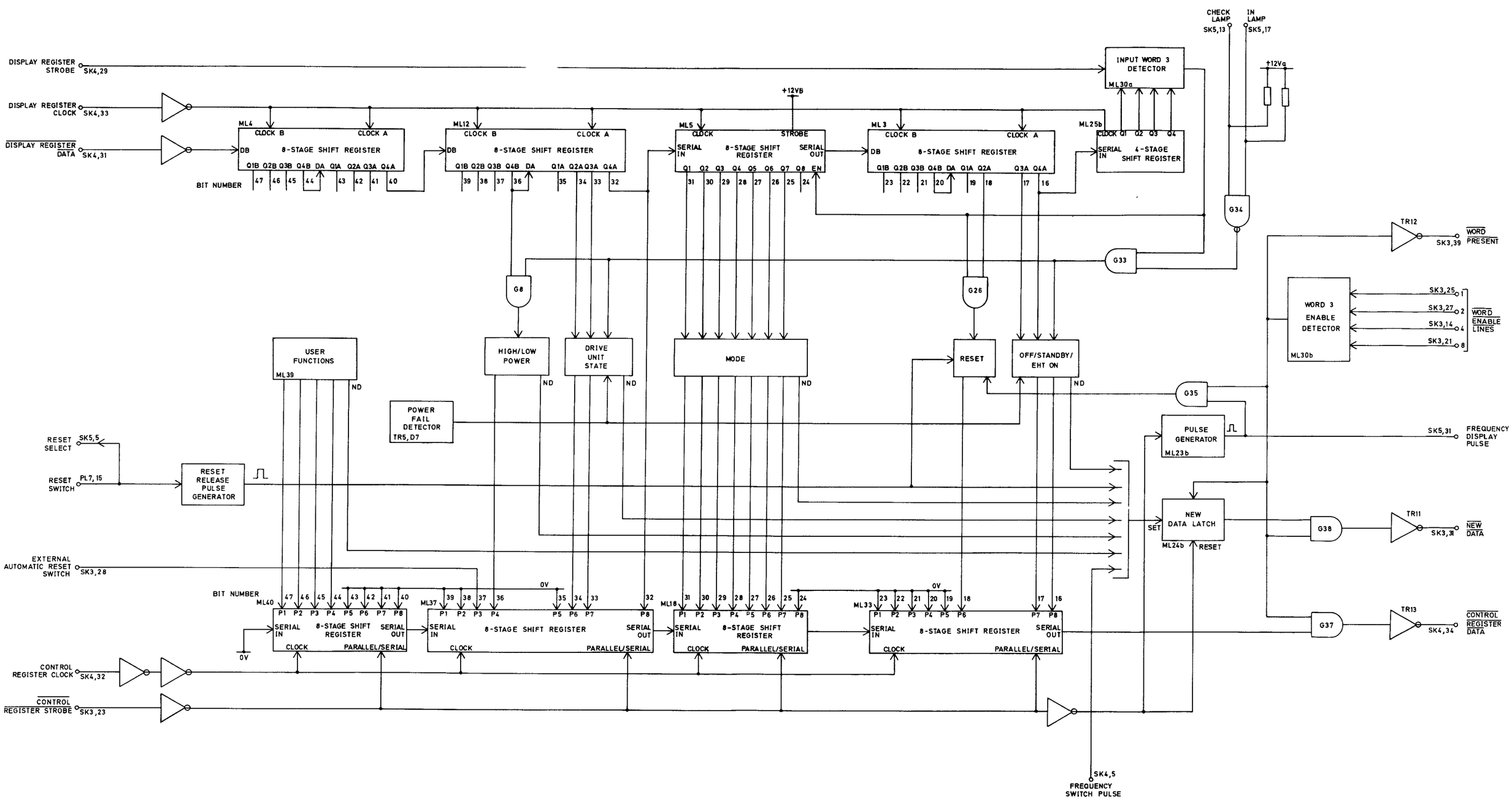
Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number	Manufacturer
Resistors (Contd.)						
R36	12k	Metal Oxide		2	917952	Electrosil TR4
R37	12k	Metal Oxide		2	917952	Electrosil TR4
R38	12k	Metal Oxide		2	917952	Electrosil TR4
R39	NOT USED					
R40	NOT USED					
R41	12k	Metal Oxide		2	917952	Electrosil TR4
R42	12k	Metal Oxide		2	917952	Electrosil TR4
R43	12k	Metal Oxide		2	917952	Electrosil TR4
R44	12k	Metal Oxide		2	917952	Electrosil TR4
R45	12k	Metal Oxide		2	917952	Electrosil TR4
R46	12k	Metal Oxide		2	917952	Electrosil TR4
R47	12k	Metal Oxide		2	917952	Electrosil TR4
R48	22k	Metal Oxide		2	913493	Electrosil TR4
R49	470	Metal Oxide		2	920758	Electrosil TR4
R50	470	Metal Oxide		2	920758	Electrosil TR4
R51	68k	Metal Oxide		2	916478	Electrosil TR4
R52	22k	Metal Oxide		2	913493	Electrosil TR4
R53	68k	Metal Oxide		2	916478	Electrosil TR4
R54	22k	Metal Oxide		2	913493	Electrosil TR4
R55	22k	Metal Oxide		2	913493	Electrosil TR4
R56	12k	Metal Oxide		2	917952	Electrosil TR4
R57	12k	Metal Oxide		2	917952	Electrosil TR4
R58	22k	Metal Oxide		2	913493	Electrosil TR4
R59	12k	Metal Oxide		2	917952	Electrosil TR4
R60	12k	Metal Oxide		2	917952	Electrosil TR4
R61	22k	Metal Oxide		2	913493	Electrosil TR4
R62	22	Metal Oxide		2	920743	Electrosil TR4
R63	22	Metal Oxide		2	920743	Electrosil TR4
R64	22	Metal Oxide		2	920743	Electrosil TR4
R65	22k	Metal Oxide		2	913493	Electrosil TR4
R66	12k	Metal Oxide		2	917952	Electrosil TR4
R67	12k	Metal Oxide		2	917952	Electrosil TR4
R68	12k	Metal Oxide		2	917952	Electrosil TR4
R69	12k	Metal Oxide		2	917952	Electrosil TR4
R70	12k	Metal Oxide		2	917952	Electrosil TR4

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number	Manufacturer
Resistors (contd.)						
R71	12k	Metal Oxide		2	917952	Electrosil TR4
R72	12k	Metal Oxide		2	917952	Electrosil TR4
R73	12k	Metal Oxide		2	917952	Electrosil TR4
R74	22k	Metal Oxide		2	913493	Electrosil TR4
R75	12k	Metal Oxide		2	917952	Electrosil TR4
R76	12k	Metal Oxide		2	917952	Electrosil TR4
R77	12k	Metal Oxide		2	917952	Electrosil TR4
R78	12k	Metal Oxide		2	917952	Electrosil TR4
R79	22k	Metal Oxide		2	913493	Electrosil TR4
R80	22k	Metal Oxide		2	913493	Electrosil TR4
R81	1k8	Metal Oxide		2	911148	Electrosil TR4
R82	22	Metal Oxide		2	920743	Electrosil TR4
R83	12k	Metal Oxide		2	917952	Electrosil TR4
R84	12k	Metal Oxide		2	917952	Electrosil TR4
R85	12k	Metal Oxide		2	917952	Electrosil TR4
R86	12k	Metal Oxide		2	917952	Electrosil TR4
R87	12k	Metal Oxide		2	917952	Electrosil TR4
R88	68k	Metal Oxide		2	916478	Electrosil TR4
R89	12k	Metal Oxide		2	917952	Electrosil TR4
R90	56k	Metal Oxide		2	913497	Electrosil TR4
R91	56k	Metal Oxide		2	913497	Electrosil TR4
Capacitors			V			
C1	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C2	15	Tantalum	20	20	910060	Union Carbide K15J20S
C3	1n	Disc Ceramic	500	20	915243	Erie 831/K2600
C4	1n	Disc Ceramic	500	20	915243	Erie 831/K2600
C5	1n	Disc Ceramic	500	20	915243	Erie 831/K2600
C6	1n	Disc Ceramic	500	20	915243	Erie 831/K2600
C7	1n	Disc Ceramic	500	20	915243	Erie 831/K2600
C8	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C9	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C10	0.1	Polyester	100	10	920566	Waycom MKS 4
C11	100p	Disc Ceramic	500	10	917417	Erie 831/N3300

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number	Manufacturer
Diodes						
D1		Silicon			914898	STC 1N4149
D2		Silicon			914898	STC 1N4149
D3		Silicon			914898	STC 1N4149
D4		Silicon			914898	STC 1N4149
D5		Silicon			914898	STC 1N4149
D6		Silicon			914898	STC 1N4149
D7		Zener, 10V, 400mW			917217	Mullard BZY88C10V
D8		Silicon			914898	STC 1N4149
D9		Silicon			914898	STC 1N4149
D10		Silicon			914898	STC 1N4149
D11		Silicon			914898	STC 1N4149
D12		Silicon			914898	STC 1N4149
D13		Silicon			914898	STC 1N4149
D14		Silicon			914898	STC 1N4149
D15		Silicon			914898	STC 1N4149
D16		Silicon			914898	STC 1N4149
D17		Silicon			914898	STC 1N4149
D18		Silicon			914898	STC 1N4149
Transistors						
TR1		NPN Silicon			923217	2N2222A (CV7770)
TR2		NPN Silicon			923217	2N2222A (CV7770)
TR3		NPN Silicon			923217	2N2222A (CV7770)
TR4		NPN Silicon			923217	2N2222A (CV7770)
TR5		NPN Silicon			923217	2N2222A (CV7770)

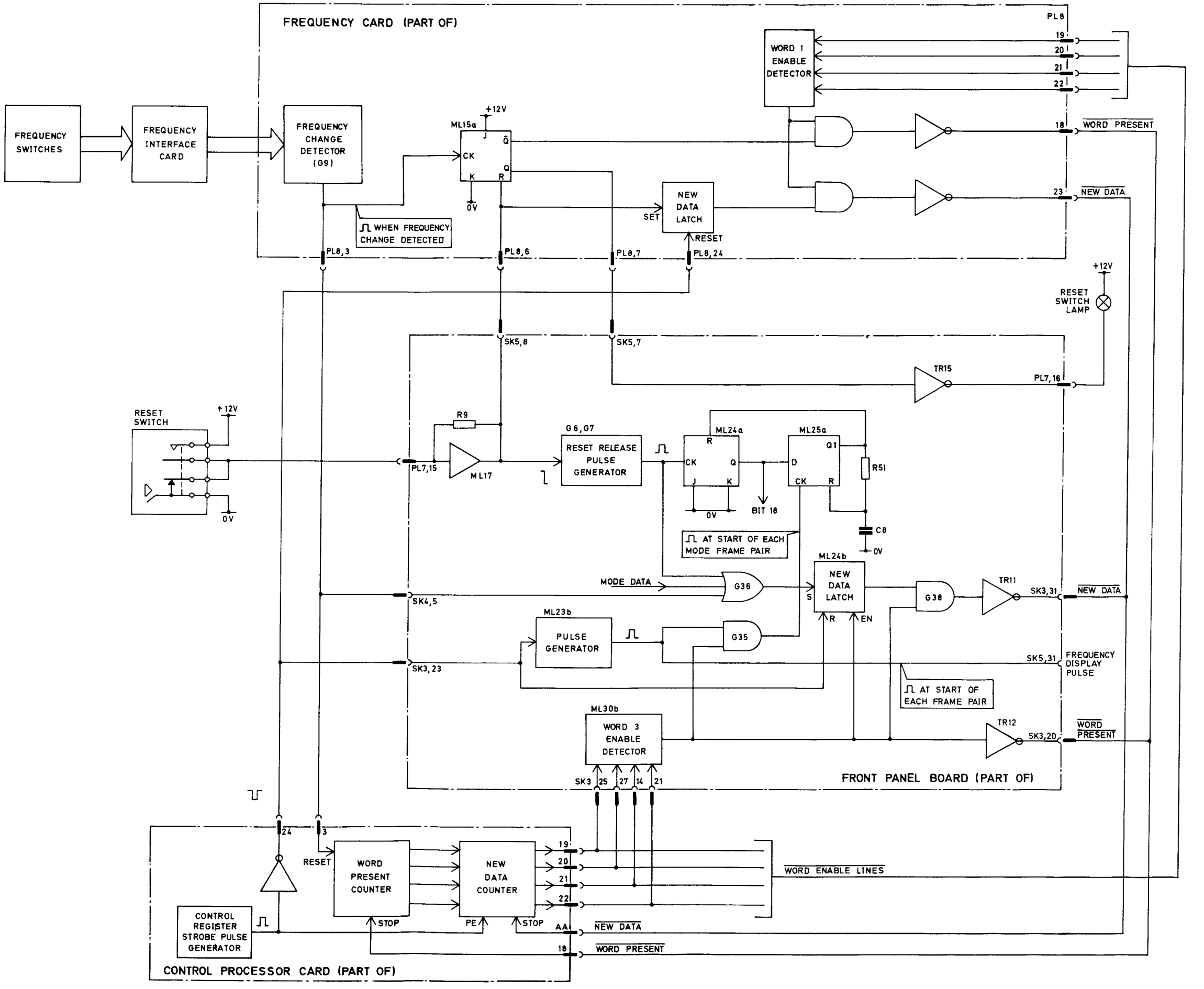
Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number	Manufacturer
Transistors (Contd.)						
TR6		NPN Silicon			923217	2N2222A (CV7770)
TR7		NPN Silicon			923217	2N2222A (CV7770)
TR8		NPN Silicon			923217	2N2222A (CV7770)
TR9		NPN Silicon			923217	2N2222A (CV7770)
TR10		NPN Silicon			923217	2N2222A (CV7770)
TR11		NPN Silicon			923217	2N2222A (CV7770)
TR12		NPN Silicon			923217	2N2222A (CV7770)
TR13		NPN Silicon			923217	2N2222A (CV7770)
TR14		NPN Silicon			923217	2N2222A (CV7770)
TR15		NPN Silicon			923217	2N2222A (CV7770)
TR16		NPN Silicon			923217	2N2222A (CV7770)
Integrated Circuits						
ML1		Triple 3-input NAND gate			930978	RCA CD4023 BE
ML2		Quad exclusive OR gate			930856	RCA CD4070 BE
ML3		Dual 4-stage shift register			930973	RCA CD4015 BE
ML4		Dual 4-stage shift register			930973	RCA CD4015 BE
ML5		8-stage shift register			929324	RCA CD4094 BE
ML6		Priority encoder			929702	RCA CD4532 BE
ML7		BCD to decimal decoder			923940	Texas BN7445J
ML8		Triple 3-input NOR gate			930030	RCA CD4049 BE
ML9		Hex. inverting buffer			930033	RCA CD4025 BE
ML10		Quad 2-input AND gate			919322	RCA CD4081 BE
ML11		Dual D-type flip-flop			926860	RCA CD4013 BE
ML12		Dual 4-stage shift register			930973	RCA CD4015 BE
ML13		Quad transmission gate			930148	RCA CD4066 BE
ML14		Quad transmission gate			930148	RCA CD4066 BE
ML15		Quad 2-input OR gate			930038	RCA CD4071 BE
ML16		Hex. non-inverting buffer			930034	RCA CD4050 BE
ML17		Hex. non-inverting buffer			930034	RCA CD4050 BE
ML18		8-stage shift register			930977	RCA CD4021 BE
ML19		Dual binary to 1-of-4 decoder			928189	RCA CD4555 BE
ML20		Quad 2-input OR gate			930038	RCA CD 4071 BE

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number	Manufacturer
Integrated Circuits (Contd.)						
ML21		Dual D-type flip-flop			926860	RCA CD 4013 BE
ML22		Dual 4-input OR gate			929319	RCA CD 4072 BE
ML23		Dual D-type flip-flop			926860	RCA CD 4013 BE
ML24		Dual J-K flip-flop			930981	RCA CD 4027 BE
ML25		Dual 4-stage shift register			930973	RCA CD 4015 BE
ML26		Quad 2-input OR gate			930038	RCA CD 4071 BE
ML27		Quad 2-input AND gate			929322	RCA CD 4081 BE
ML28		Hex. Inverting buffer			930033	RCA CD 4049 BE
ML29		Quad 2-input AND gate			929322	RCA CD 4081 BE
ML30		Dual binary to 1-of-4 decoder			928189	RCA CD 4555 BE
ML31		Quad 2-input NOR gate			930027	RCA CD 4001 BE
ML32		Hex inverting buffer			930033	RCA CD 4049 BE
ML33		8-stage shift register			930977	RCA CD 4021 BE
ML34		Dual D-type flip-flop			926860	RCA CD 4013 BE
ML35		Dual 4-input OR gate			929319	RCA CD 4072 BE
ML36		Quad exclusive NOR gate			926534	RCA CD 4077 BE
ML37		8-stage shift register			930977	RCA CD 4021 BE
ML38		Quad 2-input NAND gate			930028	RCA CD 4011 BE
ML39		Quad D-type latch			930861	RCA CD 4042 BE
ML40		8-stage shift register			930977	RCA CD 4021 BE
Connectors						
PL6		Plug, 34-way			927794	3M's 3431-2003
PL7		Plug, 26-way			928473	3M's 3423-2003
PL8		Plug, 26-way			928473	3M's 3423-2003
SK3, SK4, SK5		Cable and connector assembly			BA77446	Racal
		Comprising:				
		34-way PCB connector			927425	3M's 3402-0001
		34-way socket			927426	3M's 3414-3000
		Cable, flat, 34-way			927430	3M's 3365
Miscellaneous						
		14-pin DIL IC socket			927053	Texas C83-14-02
		16-pin DIL IC socket			927054	Texas C83-16-02



RACAL
WOH8307

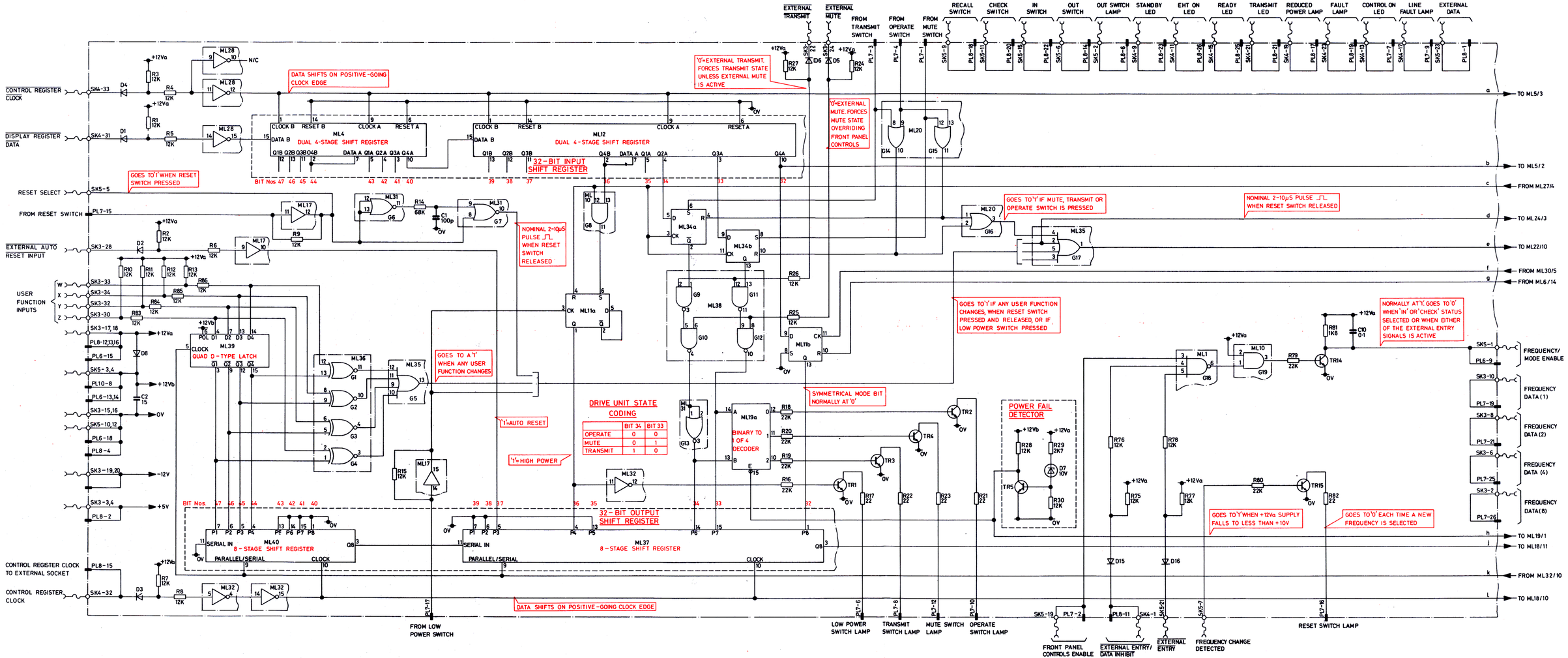
Simplified Block Diagram : Front Panel Board **Fig. 9-1**



RACAL
WOH8307

Simplified Diagram : Reset Operation

Fig. 9·2



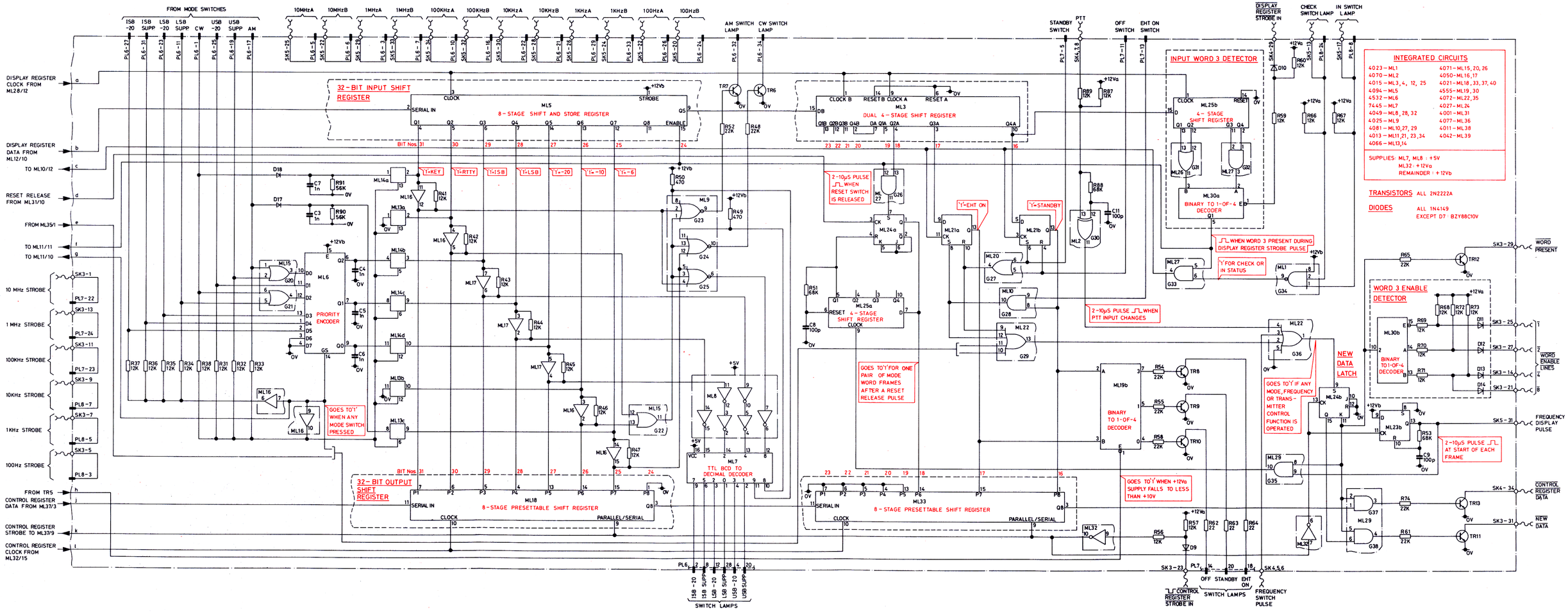
RACAL

WOH8307	DC78711	9-3
1		1/2

WOH8307	DC78711	9-3
1		2/2

Circuit : Front Panel Board (Sheet 1)

Fig. 9-3



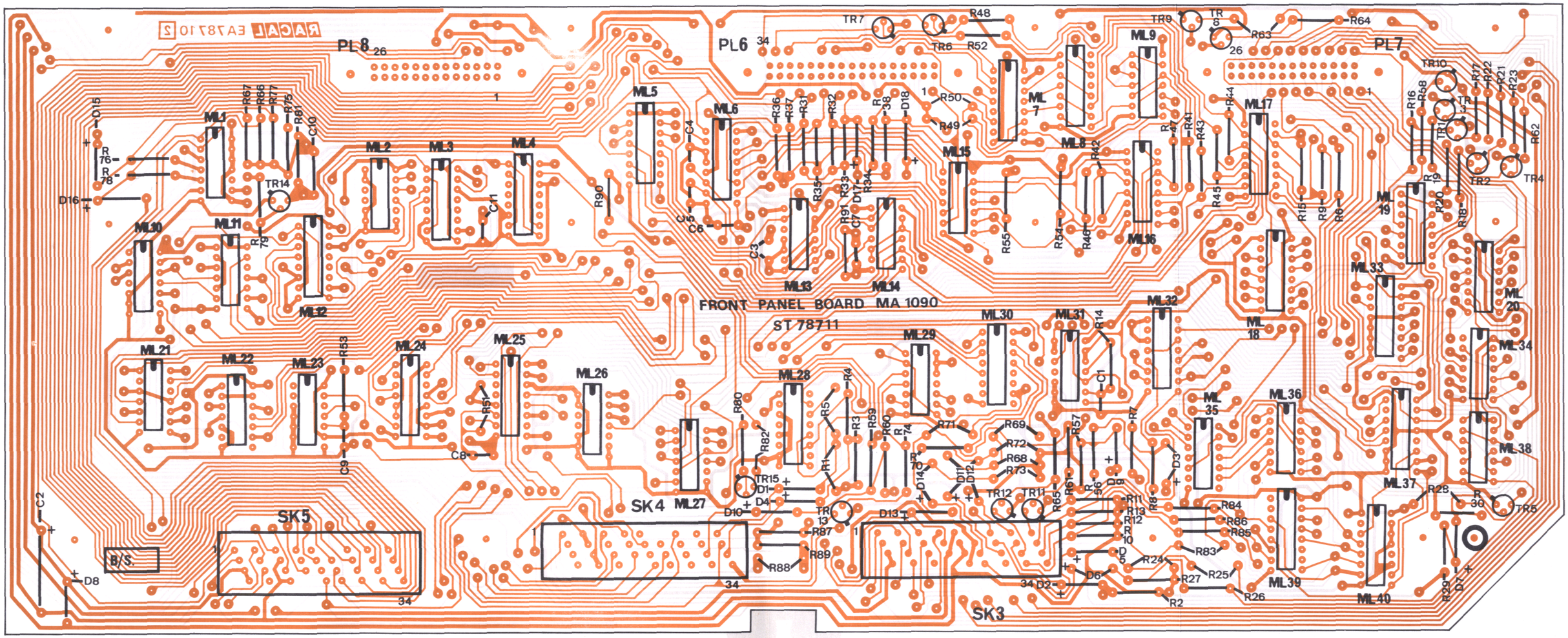
RACAL

WOH8307	DC78711	9-4
1		1/2

WOH8307	DC78711	9-4
1		2/2

Circuit : Front Panel Board (Sheet 2)

Fig. 9·4



Layout : Front Panel Board

Fig. 9·5

CHAPTER 10

FREQUENCY CARD

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CHAPTER 10

FREQUENCY CARD

INTRODUCTION

1. The frequency card generates the frequency setting data which is conveyed to the associated transmitter via word 1 of the SCORE format. It also accepts the display register data for subsequent display and control purposes.

FUNCTIONAL DESCRIPTION

2. The following functional description paragraphs should be read in conjunction with the block diagram of the frequency card given in Fig. 10.1.

Display Register Data

3. The inverted display register data at board connector pin AF comes from one of the following five sources via the display processor card.

(1) External equipment connected to the front panel EXTERNAL socket (such as the MA.1083 frequency entry pad) provided a STATUS is not selected.

(2) External equipment connected to PL2 on the rear panel provided a STATUS is not selected.

(3) The associated transmitter, via the revertive data highway, when CHECK is selected.

(4) A computer (via the computer data highway) or another MA.1090 (via the exchange highway) when IN is selected.

(5) The control data recall store (on the control processor card) when the RECALL push-button is pressed.

32-Bit Input Shift Register

4. The selected display register data is clocked into a 32-bit input shift register (by the display register clock signal at board connector pin AH), which comprises eight 4-stage shift registers connected in cascade. The parallel output from the input shift register is applied to six up/down counter stages (one for each digit of the operating frequency) but is only strobed into these stages when the word 1 detector (para. 5) produces the required preset enable pulse.

Word 1 Detector

5. The word 1 detector produces the preset enable pulse for the up/down counters only when word 1 is present and correctly positioned in the input shift register during a display register strobe pulse. The word 1 identification code (bits 12 to 15 of the preamble) is recognised by the word detector and when the display register strobe pulse occurs (at board connector pin 27) the preset enable pulse is produced.

Power Fail Detector

6. The power fail detector is powered from the internal battery supply (+12 Vb) and monitors the +12 Va output from the power supply module. Should the +12 Va supply fall to less than +10V (approximately), the output from the detector rises to logic '1' and this is routed to:-

(1) The reset input of the word 1 detector to inhibit the generation of the preset enable pulse.

(2) The up/down counters via G11 as a disable input.

Up/Down Counters

7. The clock and up/down signals for the six up/down counters are produced on the frequency interface card (Chap. 11) and are controlled by the six frequency switches on the front panel.

8. The BCD frequency setting data output from the six up/down counters (originating either from the frequency switches or the display register data) is applied in parallel form to the 32-bit output shift register (para. 16). The 10 MHz digit data is also applied to a most significant digit detector; this produces a 3-bit code which is routed to the frequency interface card (Chap. 11).

9. The clock signals for the up/down counters (originating from the six frequency switches on the front panel) are also applied to a NAND gate G9; each time a frequency switch is operated, a nominal 2 μs positive-going pulse is produced at the output of G9, which is routed to:-

(1) The word 3 new data latch on the front panel board (Chap. 9) via board connector pin 3.

(2) A frequency change detector (para. 11).

Frequency/Mode Enable

10. The frequency/mode enable input, at board connector pin 5, comes from the front panel board; this input is normally at '1' and goes to a '0' when IN or CHECK is selected, when the front panel EXTERNAL socket is in use, or when equipment connected to the external input pins of PL2 on to the rear panel is in use. A '0' at board connector pin 5 is inverted by ML18 and is then applied via OR gate G8 to the reset input of the frequency change detector (para. 11), and to the up/down counters via OR gate G11 as a disable input.

Frequency Change Detector

11. The up/down counter clock signals (originating from the six frequency switches on the front panel) are also applied to a NAND gate G9. A nominal 2 μs positive-going pulse is produced at the output of G9 each time any frequency switch is operated; this pulse is applied to the frequency change detector with the following results:-

(1) The Q output changes to a '1': this is routed to the front panel board (via board connector pin 7) where it switches on the lamp driver transistor for the front panel RESET switch lamp.

(2) The $\overline{Q}$ output changes to a '0', and this is applied to AND gate G14 to inhibit the word present output from the word 1 enable detector (para. 13).

12. The frequency change detector is reset via OR gate G8 when the front panel RESET push-button is pressed and released, or when the frequency/mode enable input changes to a '0' (para. 10).

Word 1 Enable Detector

13. The purpose of this stage is to detect the presence of the word 1 identification code (in inverted binary form) at the four word enable lines from the control processor card (Chap. 12). When the presence of word 1 is detected, a word present signal is generated; this is routed to:-

(1) The enable input of the new data latch (para. 14);

(2) AND gate G12 for the serial data output from the 32-bit output shift register (para. 17);

(3) AND gate G13 for the output signal from the new data latch (para. 14);

(4) AND gate G14 where it is gated with a '1' output from the frequency change detector (frequency change not detected) to produce an inverted (TR2) word present output a board connector pin 18. This is routed to the control processor card to stop the word present counter at binary 1 (Chap. 12).

New Data Latch

14. The new data latch for word 1 is set each time the front panel RESET push-button is pressed and released (the RESET circuitry is fully described in Chap. 9). When the RESET push-button is released, a positive-going pulse at board connector pin 6 (from the front panel board) is applied to the reset input of the new data latch. The next time that the word 1 ident. is detected at the four word enable lines, the combined outputs (G13) of the word 1 enable detector and the new data latch produce a new data signal which is applied to the control processor card (via inverter TR3 and board connector pin AA) to stop the new data counter at binary 1 (Chap. 12). This ensures that the word 1 frame is inserted at the end of the frame currently being sent.

15. The positive-going pulse at board connector pin 6 is also applied via OR gate G8 to the reset input of the frequency change detector; the $\overline{Q}$ output is reset to a '1' and this is applied to AND gate G14 to open a path for the next word 1 routine data word present signal.

Output Shift Register

16. The 32-bit output shift register comprises four 8-stage parallel or serial input/serial output shift registers connected in cascade. When the preset enable input is at logic '0', the serial input (in this case 0V) is enabled and clocked into the register whilst the data is clocked out. When the preset enable input is at logic '1', the parallel frequency setting data from the up/down counters is loaded into the register independently of the clock waveform.

17. The inverted control register strobe pulse from the control processor card, at board connector pin AB, is inverted and then applied to the output shift register as a parallel data entry enable pulse. The frequency setting data is loaded in and, provided the output from the word 1 enable detector is present, the frequency word is clocked out of the register in serial form and routed via G12, inverting buffer TR4, and board connector pin AC to the control processor card.

18. The serial frequency data from the output shift register is also routed (via board connector pin 8) to the frequency interface card (Chap. 11) where it is used for frequency display purposes.

CIRCUIT DESCRIPTION (Fig. 10.3)

32-BIT INPUT SHIFT REGISTER

19. The 32-bit input shift register comprises eight 4-stage shift registers, ML1a, ML2b, ML2a, ML3b, ML3a, ML4b, ML4a and ML5b, which are cascaded by connecting the Q4 output from one register to the D input of the next. The logic level present at a data input (D) is transferred into the first register stage, and shifted over one stage at each positive-going transition of the applied clock waveform.

WORD 1 DETECTOR

20. This circuit comprises a 4-stage shift register ML5a, a four input OR gate G10, and a binary to 1-of-4 decoder ML24b. When word 1 is correctly positioned in the input shift register, the word 1 identification code (bits 12 to 15 of the preamble) is present at the Q4 to Q1 outputs of ML5a. The logic '1' Q4 output is applied to the A input of ML24b, whilst the logic '0' Q3 to Q1 outputs result in a '0' output from G10 which is applied to the B input of ML24b. When the next display register strobe pulse occurs (at board connector pin 27), ML24b is enabled and the logic '1' Q1 output is applied to the preset enable inputs of the up/down counter stages (para. 22). The up/down counters are thus preset in accordance with the frequency setting data contained in the input shift register, and this data (at the Q1 to Q4 outputs of ML9 to ML13, and the Q outputs of ML6) is applied to the parallel data input pins of the output shift register stages.

POWER FAIL DETECTOR

21. The power fail detector is powered from the internal battery supply (+12 Vb) and monitors the +12 Va output from the power supply module via a potential divider R15, 10V zener diode D5 and R16. Should the +12 Va supply fall to less than +10V, TR1 cuts off, resulting in a '1' at the collector. This is routed to the reset input of ML5a to inhibit the generation of the preset enable output, and via OR gate G11 to the carry-in inputs of the up/down counters as a disable input.

UP/DOWN COUNTERS (100 Hz to 1 MHz Digits)

22. Five presettable BCD counters, ML9 to ML13, are used to generate the frequency setting data for the digits 100 Hz to 1 MHz. The BCD number at the parallel inputs P1 to P4 presets each counter when the preset enable input is at logic '1'. When the carry-in input is at logic '0', the counter advances up (up/down input at '1') or down (up/down input at '0') on each positive-going transition of the applied clock waveform. The timing diagram for a single counter is given in Fig. 10.2.

23. The up/down and clock signals for each counter are produced on the frequency interface card (Chap. 11) and are derived from the outputs of the frequency switches on the front panel. The counters are disabled (via the carry-in input) if the output from G11 goes to a '1' due to a power-fail condition (para. 21) or if the frequency/mode enable input goes to a '0' (para. 29).

10 MHz DIGIT UP/DOWN COUNTER

24. This circuit comprises a dual J-K flip-flop ML6, two exclusive OR gates G1, G6, and two AND gates G3, G7. The display register data 10 MHz digit output from the 32-bit input shift register, at the Q3 and Q4 outputs of ML1a, is applied via AND gates G3 and G7 to the set inputs of ML6a and ML6b respectively, whilst the preset enable pulse output from the word 1 detector (para. 20) is applied to the remaining inputs of G3 and G7, and also to the reset inputs of ML6a and ML6b. If, for example, the Q3 output from ML1a is at logic '0' when the preset enable pulse occurs, a '0' is applied to the set input of ML6a

(which has no effect), a '1' is applied to the reset input, and the resulting '0' Q output is applied to the output shift register as data bit 45. If the Q3 output from ML1a is at logic '1' when the preset enable output occurs, then both the set and the reset inputs are activated, and data bit 45 is set to a '1' (Table 1).

Counting Action

25. The 10 MHz up/down input at board connector pin D ('1' for up, '0' for down) is applied to exclusive OR gates G2, G6, whilst the $\overline{Q}$ output from ML6b is applied to the remaining input of G2, and the Q output of ML6a is applied to the remaining input of G6. The 10 MHz clock signal, at board connector pin C, is gated (G1) with the inverted frequency/mode enable input at board connector pin 5 (para. 29), such that when this input is at '0' the 10 MHz clock signal is inhibited.

26. Assume that the counter is in the 00 state (ML6a and ML6b Q outputs at '0'), and that the up/down line is at logic '1' (count up). The logic '1' $\overline{Q}$ output from ML6b, together with the '1' up/down signal, results in a '0' output from G2 which is applied to the J input of ML6a, whilst the logic '0' Q output from ML6a together with the '1' up/down signal results in a '1' at the J input of ML6b. The K inputs of ML6a and ML6b are both taken to +12 Vb (logic '1').

27. From Table 1 it can be seen that after the next clock pulse, the '0' at the J input of ML6a causes the Q output to remain at '0', whilst the '1' at the J input of ML6b causes its Q output to change to a '1'; the $\overline{Q}$ output of ML6b thus changes to a '0', and since this is applied to G2, the J input of ML6a changes to '1'. After the next clock pulse, the Q output of ML6a changes to a '1' whilst the Q output of ML6b changes to a '0'. The '1' at the $\overline{Q}$ output of ML6b results in a '0' at the J input of ML6a, whilst the '1' at the Q output of ML6a results in a '0' at the J input of ML6b.

28. To complete the cycle in the count-up mode, when the next clock pulse occurs, and with both J inputs at '0', the Q output of ML6a changes to '0', and the counter is reset to the 00 state. In the count down mode, the level on the up/down line changes to a '0', and the reverse process takes place, i.e. the counter output changes from 00 to 10, then to 01 and back to 00 (Table 2).

TABLE 1: J-K FLIP-FLOP TRUTH TABLE

PRESENT STATE					CLOCK	NEXT STATE		
INPUTS				OUTPUT		OUTPUTS		
J	K	S	R	Q		Q	Q	
1	X	0	0	0	⌐	1	0	
X	0	0	0	1	⌐	1	0	
0	X	0	0	0	⌐	0	1	
X	1	0	0	1	⌐	0	1	
X	X	0	0	X	⌐			NO CHANGE
X	X	1	0	X	X	1	0	
X	X	0	1	X	X	0	1	
X	X	1	1	X	X	1	1	

X equals don't care condition.

TABLE 2: 10 MHz DIGIT COUNTER TRUTH TABLE

ML6a Qn	ML6b Qn	Up/down	ML6a J	ML6b J	Clock	ML6a Qn + 1	ML6b Qn + 1
0	0	0	1	0	⌐	1	0
0	1	0	0	0	⌐	0	0
1	0	0	1	1	⌐	0	1
0	0	1	0	1	⌐	0	1
0	1	1	1	1	⌐	1	0
1	0	1	0	0	⌐	0	0

Frequency/Mode Enable

29. The frequency/mode enable input, at board connector pin 5, is normally at logic '1'; it is set to a '0' (via circuitry on the front panel board) when CHECK or IN is selected, when the front panel EXTERNAL socket is in use, or if external equipment connected to PL2 on the rear panel is in use. A '0' at board connector pin 5 is inverted by ML18 and is then applied to:-

(1) The reset input of the frequency change detected latch ML15a (para. 30) via OR gate G8;

(2) OR gate G1 to disable the 10 MHz clock input;

(3) The carry-in inputs of the up/down counters ML9 to ML13 via G11 to inhibit the counting action.

FREQUENCY CHANGE DETECTOR

30. The six clock signals for the up/down counters are also routed to a NAND gate G9 such that a nominal 2 μs positive-going pulse is produced at the output of G9 each time a frequency switch (on the front panel) is operated. A positive-going pulse at board connector pin 3 is used to set the mode word new data latch on the front panel board, and to reset the word present counter on the control processor card. It is also applied to the clock input of J-K flip-flop ML15a. The Q output changes to a '1', and this is routed to the front panel board to switch on the lamp driver stage for the RESET push-button lamp; the $\overline{Q}$ output changes to a '0', and this is routed to AND gate G14 to inhibit the word present signal for word 1. ML 15a is reset when the front panel RESET push-button is pressed ('1' at board connector pin 6) or when the frequency/mode enable input (at board connector pin 5).

NOTE: A detailed circuit description of reset operation, involving circuitry on the frequency card, the front panel board and the control processor card, is given in Chap. 9, in conjunction with Fig. 9.2.

MOST SIGNIFICANT DIGIT DETECTOR

31. The output signals from the 10 MHz up/down counter (Q outputs of ML6a and ML6b) are applied to an OR gate G5 such that the output goes to a '0' when the 10 MHz digit is set to zero. This output, at board connector pin F, is routed to the frequency interface card (Chap. 11) where it is used to blank the 10 MHz digit display.

WORD 1 ENABLE DETECTOR

32. This stage detects the presence of word 1 (in inverted binary form) at the four word enable lines (board connector pins 19 to 20). These lines are connected via diodes D7 to D10 to the enable, A and B inputs of a binary to 1-of-4 decoder ML24a in such a manner that when inverted binary 1 is present, the word 1 enable signal is produced at the Q3 output. This signal is routed to:-

(1) The K input of the new data latch ML15b (para. 33).

(2) AND gate G12 for the serial data output from the 32-bit output shift register.

(3) AND gate G13 for the output signal from the new data latch (para. 33).

(4) AND gate G14 where it is gated with a '1' from the $\overline{Q}$ output of ML15a (frequency change not detected); a '1' output is inverted by TR2 and is then routed via board connector pin 18 to the control processor card to stop the word present counter at binary 1 (Chap. 12).

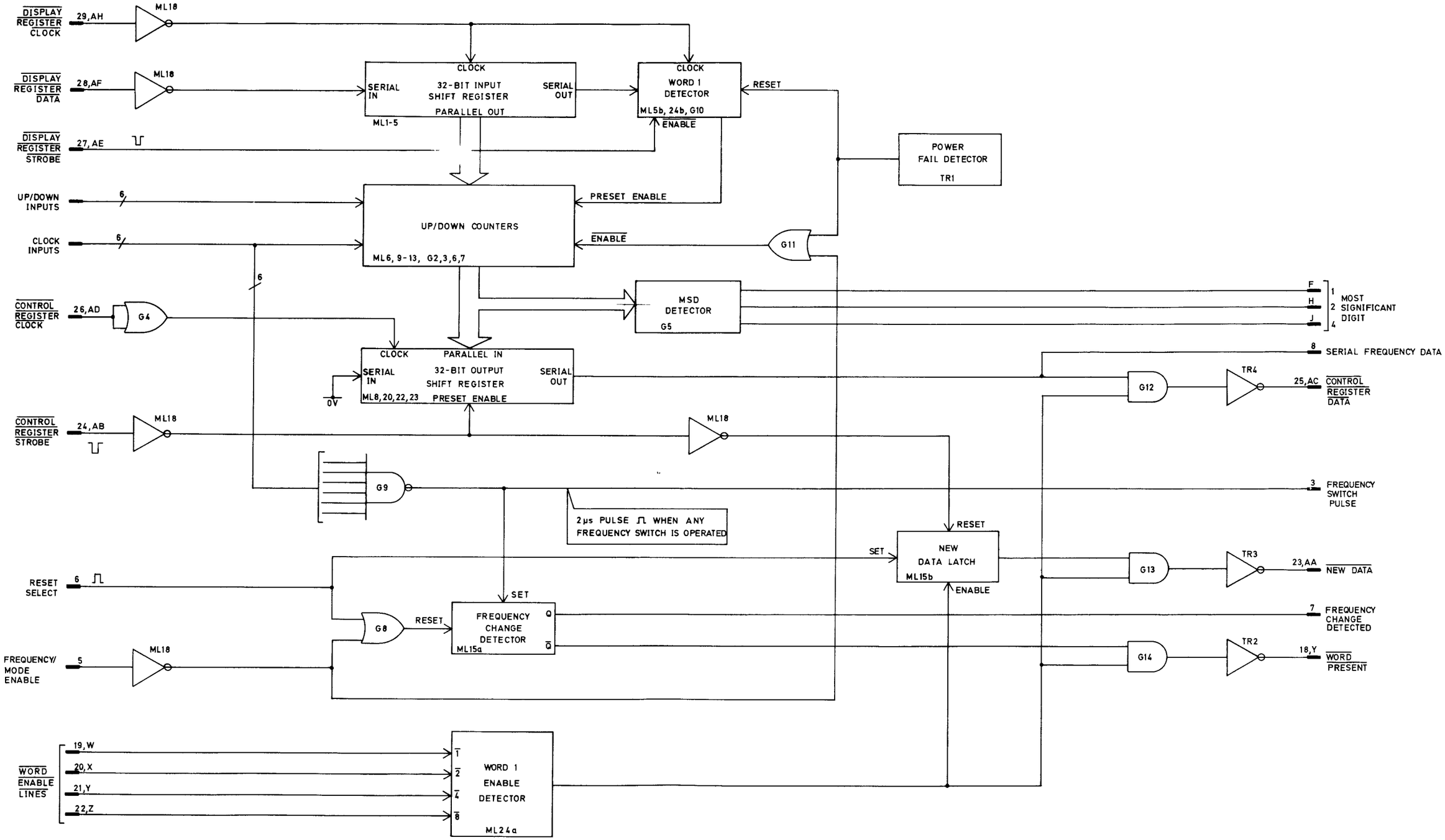
NEW DATA LATCH

33. The new data latch consists of a J-K flip-flop ML15b. A '1' is applied to the set input each time the front panel RESET push-button is pressed; this sets the Q output to a '1', which, provided the word 1 enable detector output is present, is routed via G13, inverting buffer TR3 and board connector pin AA, to the control processor card to stop the new data counter at binary 1. Since the word 1 enable detector output is applied to the K input of ML15b, the Q output is reset to zero by the next inverted control register strobe pulse, which is applied to the clock input (Table 1).

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number	Manufacturer
		FREQUENCY CARD (ST 78703)				
Resistors						
R1	12k	Metal Oxide		2	917952	Electrosil TR4
R2	12k	Metal Oxide		2	917952	Electrosil TR4
R3	12k	Metal Oxide		2	917952	Electrosil TR4
R4	12k	Metal Oxide		2	917952	Electrosil TR4
R5	12k	Metal Oxide		2	917952	Electrosil TR4
R6	12k	Metal Oxide		2	917952	Electrosil TR4
R7	12k	Metal Oxide		2	917952	Electrosil TR4
R8	12k	Metal Oxide		2	917952	Electrosil TR4
R9	12k	Metal Oxide		2	917952	Electrosil TR4
R10	12k	Metal Oxide		2	917952	Electrosil TR4
R11	12k	Metal Oxide		2	917952	Electrosil TR4
R12	12k	Metal Oxide		2	917952	Electrosil TR4
R13	22k	Metal Oxide		2	913493	Electrosil TR4
R14	12k	Metal Oxide		2	917952	Electrosil TR4
R15	2k7	Metal Oxide		2	916548	Electrosil TR4
R16	12k	Metal Oxide		2	917952	Electrosil TR4
R17	22k	Metal Oxide		2	913493	Electrosil TR4
R18	12k	Metal Oxide		2	917952	Electrosil TR4
R19	22k	Metal Oxide		2	913493	Electrosil TR4
R20	12k	Metal Oxide		2	917952	Electrosil TR4
Capacitors			V			
C1	0.1	Polyester	100	10	920566	Waycom MKS 4
C2	0.1	Polyester	100	10	920566	Waycom MKS 4
Diodes						
D1		Silicon			914898	STC 1N4149
D2		Silicon			914898	STC 1N4149
D3		Silicon			914898	STC 1N4149
D4		Silicon			914898	STC 1N4149
D5		Zener, 10V, 400mW			917217	Mullard BZY88C10V

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number	Manufacturer
Diodes (Contd.)						
D6		Silicon			914898	STC 1N4149
D7		Silicon			914898	STC 1N4149
D8		Silicon			914898	STC 1N4149
D9		Silicon			914898	STC 1N4149
D10		Silicon			914898	STC 1N4149
Transistors						
TR1		NPN Silicon			923217	2N2222A (CV7770)
TR2		NPN Silicon			923217	2N2222A (CV7770)
TR3		NPN Silicon			923217	2N2222A (CV7770)
TR4		NPN Silicon			923217	2N2222A (CV7770)
Integrated Circuits						
ML1		Dual 4-stage shift register			930973	RCA CD 4015BE
ML2		Dual 4-stage shift register			930973	RCA CD 4015BE
ML3		Dual 4-stage shift register			930973	RCA CD 4015BE
ML4		Dual 4-stage shift register			930973	RCA CD 4015BE
ML5		Dual 4-stage shift register			930973	RCA CD 4015BE
ML6		Dual J-K flip-flop			930981	RCA CD 4027BE
ML7		Quad 2-input AND gate			929322	RCA CD 4081 BE
ML8		8-stage shift register			930977	RCA CD 4021 BE
ML9		Presettable Up/Down Counter			931008	RCA CD 4510BE
ML10		Presettable Up/Down Counter			931008	RCA CD 4510BE
ML11		Presettable Up/Down Counter			931008	RCA CD 4510BE
ML12		Presettable Up/Down Counter			931008	RCA CD 4510BE
ML13		Presettable Up/Down Counter			931008	RCA CD 4510BE
ML14		Quad exclusive OR gate			930856	RCA CD 4070BE
ML15		Dual J-K flip-flop			930981	RCA CD 4027BE
ML16		Quad 2-input OR gate			930038	RCA CD 4071 BE
ML17		Dual 4-input OR gate			929319	RCA CD 4072BE
ML18		Hex. inverting buffer			930033	RCA CD 4049BE
ML19		Quad 2-input AND gate			929322	RCA CD 4081 BE
ML20		8-stage shift register			930977	RCA CD 4021 BE

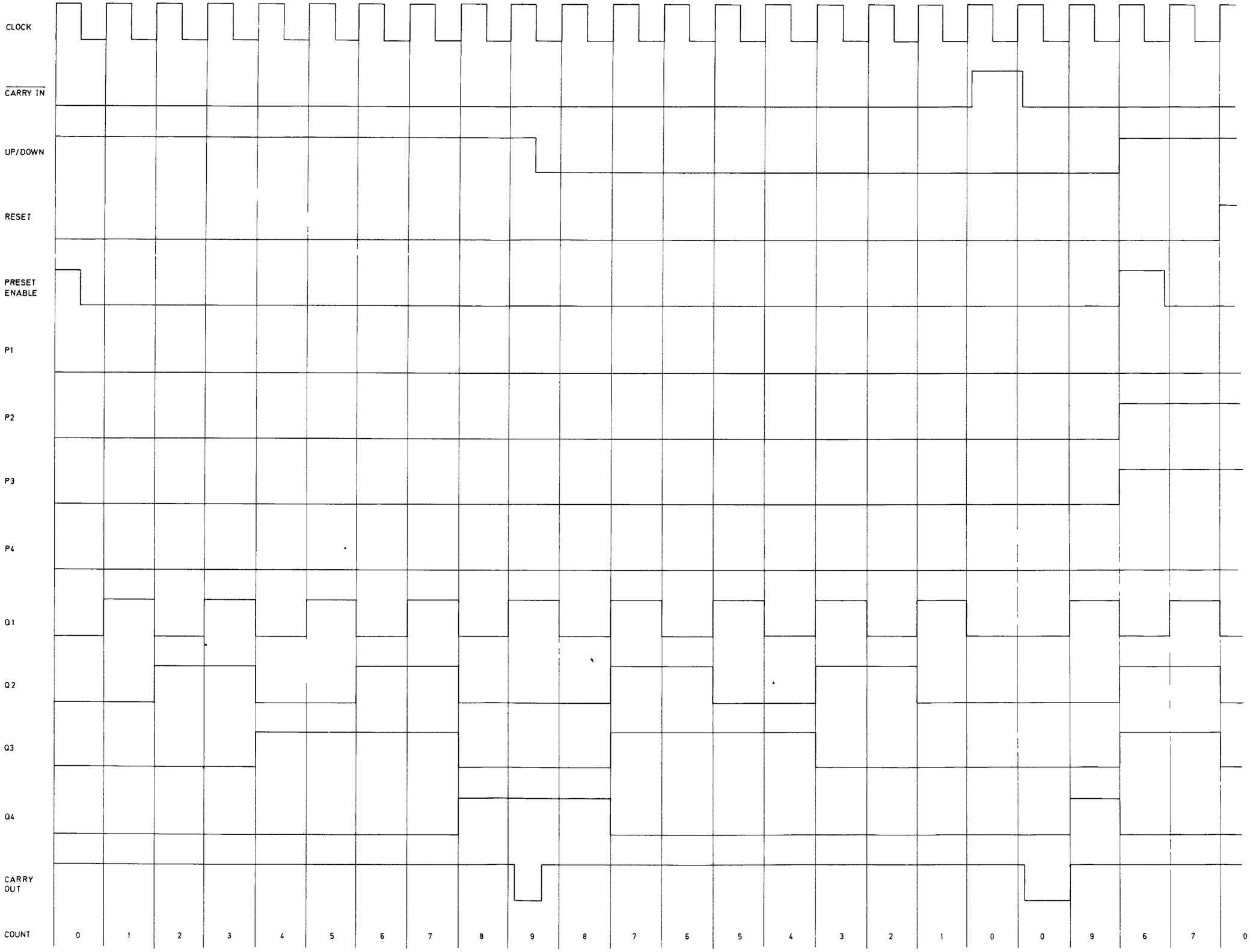
Cct. Ref.	Value	Descrtiption	Rat.	Tol. %	Racal Part Number	Manufacturer
Integrated Circuit (Contd.)						
ML21		8-input NAND gate			929317	RCA CD 4068 BE
ML22		8-stage shift register			930977	RCA CD 4021BE
ML23		8-stage shift register			930977	RCA CD 4021BE
ML24		Dual binary to 1-of-4 decoder			928189	RCA CD 4555BE
Connectors						
		14-pin DIL IC socket			927053	Texas C83-14-02
		16-pin DIL IC socket			927054	Texas C83-16-02



RACAL
WOH8307

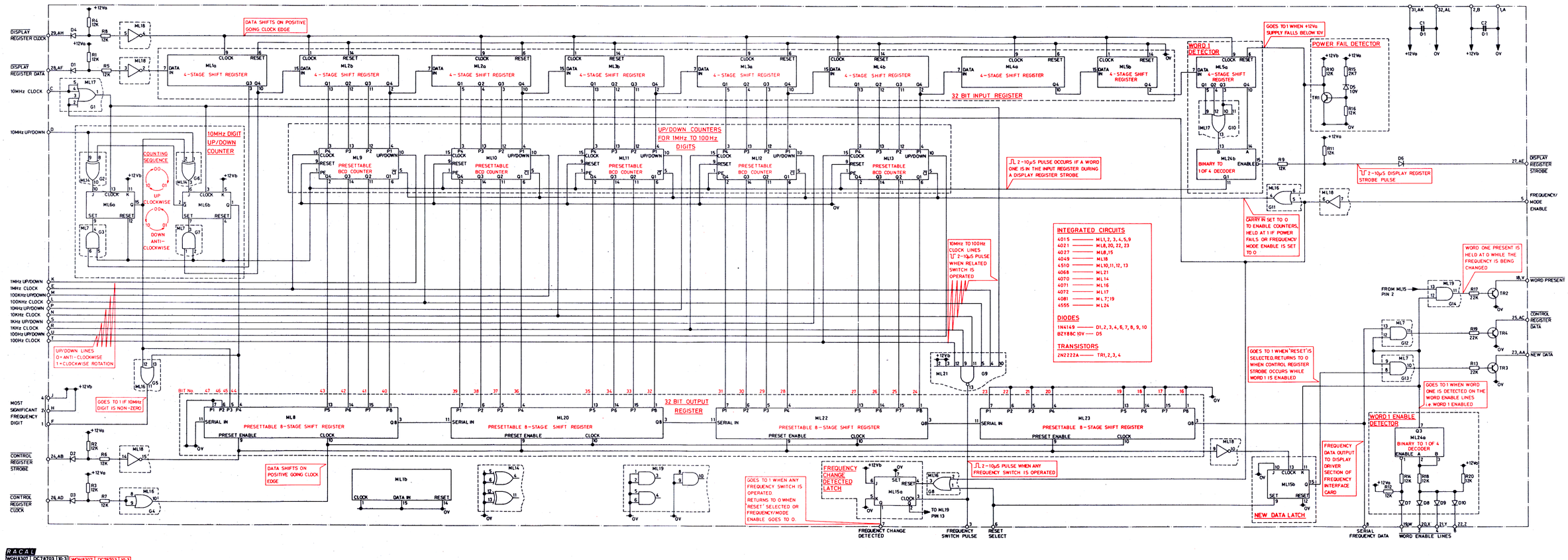
Simplified Block Diagram : Frequency Card

Fig. 10·1



RACAL
WOH8307

Timing Diagram
Single Up/Down BCD Counter Fig.10·2

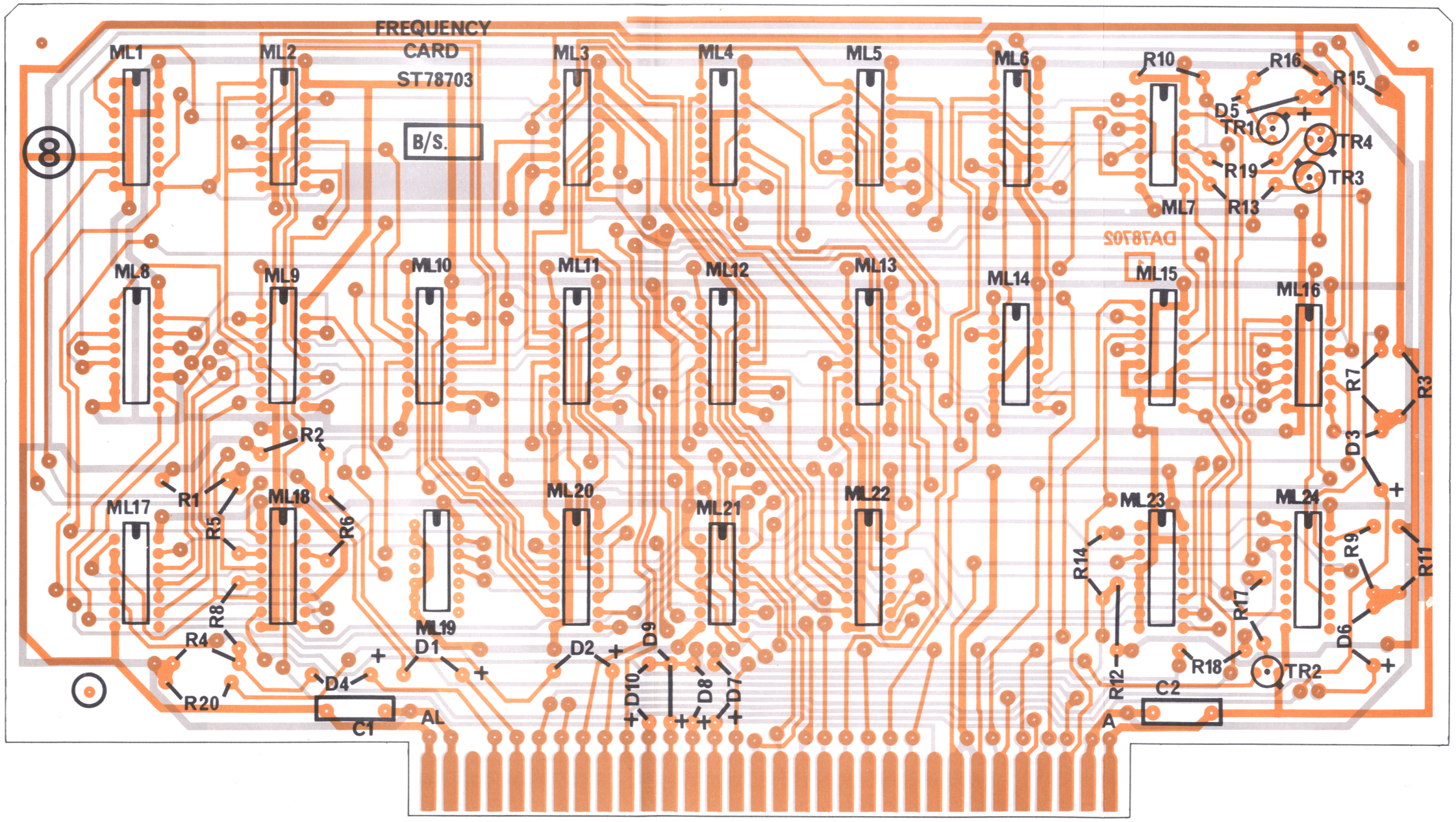


RACAL

WOH8307	DC78703	10-3	1/2
WOH8307	DC78703	10-3	2/2

Circuit : Frequency Card

Fig. 10-3



WOH 8307	DA78702	10.4
1		1/3
WOH 8307	DA78702	10.4
1		3/3
WOH 8307	DA78702	10.4
1		2/3

Layout: Frequency Card Fig. 10.4

CHAPTER 11

FREQUENCY INTERFACE CARD

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CHAPTER 11

FREQUENCY INTERFACE CARD

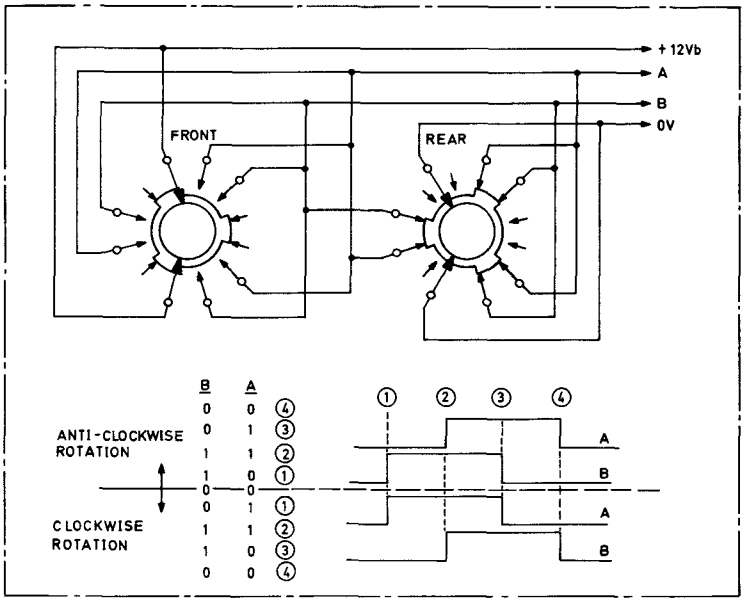
INTRODUCTION

1. The frequency interface card converts the A and B outputs from each of the six front panel frequency switches into the clock and up/down signals required by the up/down counters on the frequency card. It also contains the driver circuitry for the six solid state numeric indicators mounted on the display board.

CIRCUIT DESCRIPTION (Fig. 11.2)

CLOCK AND UP/DOWN SIGNAL GENERATION

2. Fig. 11 (i) shows the wiring of the front panel frequency switches (same for each switch) and the resulting A and B output signals for both clock-wise and anti-clockwise rotation. From the waveform diagrams of Fig. 11 (i) it can be seen that waveform A leads waveform B by 90 degrees for clockwise rotation, whilst waveform B leads waveform A by 90 degrees for anti-clockwise rotation.



RACAL Frequency Switches : Output Waveforms Fig. 11 (i)

3. Each switch wafer has three pairs of contacts connected in parallel, and two parallel-connected wiper connections. This provides high reliability and minimises the effects of switch contact bounce. A contact bounce suppression circuit is included in the A and B output line from each switch (ML14, ML15 and shunt resistors R4 to R15).

4. Since the clock and up/down signal generation circuit for each digit of the operating frequency is the same, only that for the 100 Hz digit is described. The circuit comprises four exclusive OR gates G12, G18, G29, G30, and a D-type flip-flop ML17a. A timing diagram is given in Fig. 11.1 at the end of the chapter.

5. The clock pulse generator G18, with delay components R27, C16, provides a positive-going output pulse for each transition of the input signal (from G12); one output pulse is therefore produced for each detent position of the switch. The output from G18 is applied to the clock input of ML17a, and via inverting exclusive OR gate G29 to the 100 Hz up/down counter on the frequency card (Chap. 10).

6. ML17a produces the up/down signal; for clockwise rotation the two inputs to exclusive OR gate are in anti-phase producing a '1' at the output, whilst for anti-clockwise rotation, the two inputs are in-phase, producing a '0' at the output.

DISPLAY DRIVER CIRCUITRY

8. A 2 to 10 microsecond frequency display pulse is generated on the front panel board (Chap. 9) when any word is about to be sent. This positive-going pulse, at board connector pin F, resets the binary up-counter ML1b, forcing the Q1B to Q4B outputs to logic '0'. The logic '0' Q4B output is applied, as a count enable signal, to the clock inputs of ML1a and ML1b, whilst the '0' Q3B, Q2B and Q1B outputs are inverted by ML2 to set the input code at the C-B-A input pins of ML10 to binary 7.

9. The inverted control register clock input, at board connector pin 26, is applied via inverting NAND gate G2 to the clock input of a 4-stage shift register ML4a and to the enable input of ML1a. When ML1a reaches a count of four, the first four bits (16 to 19) of the serial frequency data (in inverted form) are positioned in ML4a; the Q3A output of ML1a pulses to '1' (ML1a is reset after time constant R3, C3), and this is applied to the D input of ML10 via inverting buffer ML2. ML10 is enabled and the binary 7 at the C-B-A input pins causes the octal 7 output (ML10 pin 9) to change to logic '0'. Since, however, the frequency display does not include the 1 Hz digit, the octal 7 output is not used.

10. The count-of-four output pulse from ML1a is also applied to the enable input of ML1b; since the clock input is held at logic '0' (Q4B output), the counter increments. The Q1B output changes to logic '1' and binary 6 is applied to the C-B-A input pins of ML10 via the inverters of ML2.

11. When ML1a reaches a further count-of-four, the next four bits of the serial frequency data (bits 20 to 23) are positioned in ML4a. The Q3A output pulse from ML1a enables ML10 and the binary 6 at the C-B-A input pins causes the octal 6 output to change to a '0'; this output is also unused since the frequency display does not include the 10 Hz digit.

12. The second count-of-four output pulse from ML1a causes ML1b to increment; this results in binary 5 at the C-B-A input pins of ML10 so that when the next count of four pulse is generated, the 100 Hz numerical indicator is enabled for the 100 Hz digit data contained in ML4a (bits 24 to 27 of the serial frequency data). This process is continued for the remaining numerical indicators until a count of 32 is reached; the Q4B output changes to a '1', and the counting action of both counters is stopped until the arrival of the next frequency display pulse when the whole process is repeated.

10 MHz Digit Zero Blanking

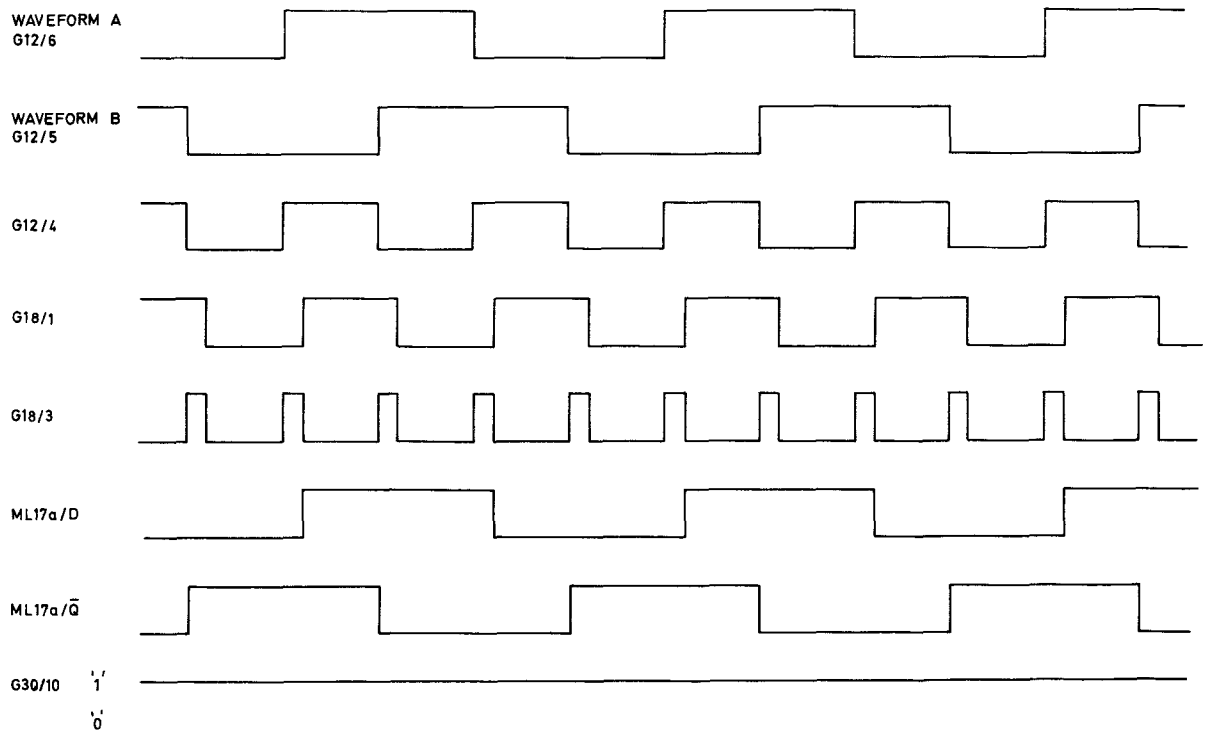
13. The 10 MHz digit zero blanking circuit uses a magnitude comparator ML9; this device is arranged to produce a logic '1' output at pin 13 when the A2-A1-A0 binary input code is numerically greater than the B2-B1-B0 binary input code. The B2-B1-B0 code, which is produced on the frequency card (Chap. 10), is set to binary 7 (1-1-1) for frequencies of 10 MHz and above, and to binary 6 (1-1-0) for frequencies below 10 MHz.

14. Since the A2-A1-A0 input applied to ML9 is set to binary 7 to enable the 10 MHz digit numerical indicator, for frequencies below 10 MHz, i.e. binary 6 at the B inputs, a '1' is applied to the reset input of ML4a; the Q1 to Q4 outputs are reset to '0', and a '1-1-1-1' blanking code is produced at the display output, via ML3 and ML11, which is then applied to the 10 MHz numerical indicator.

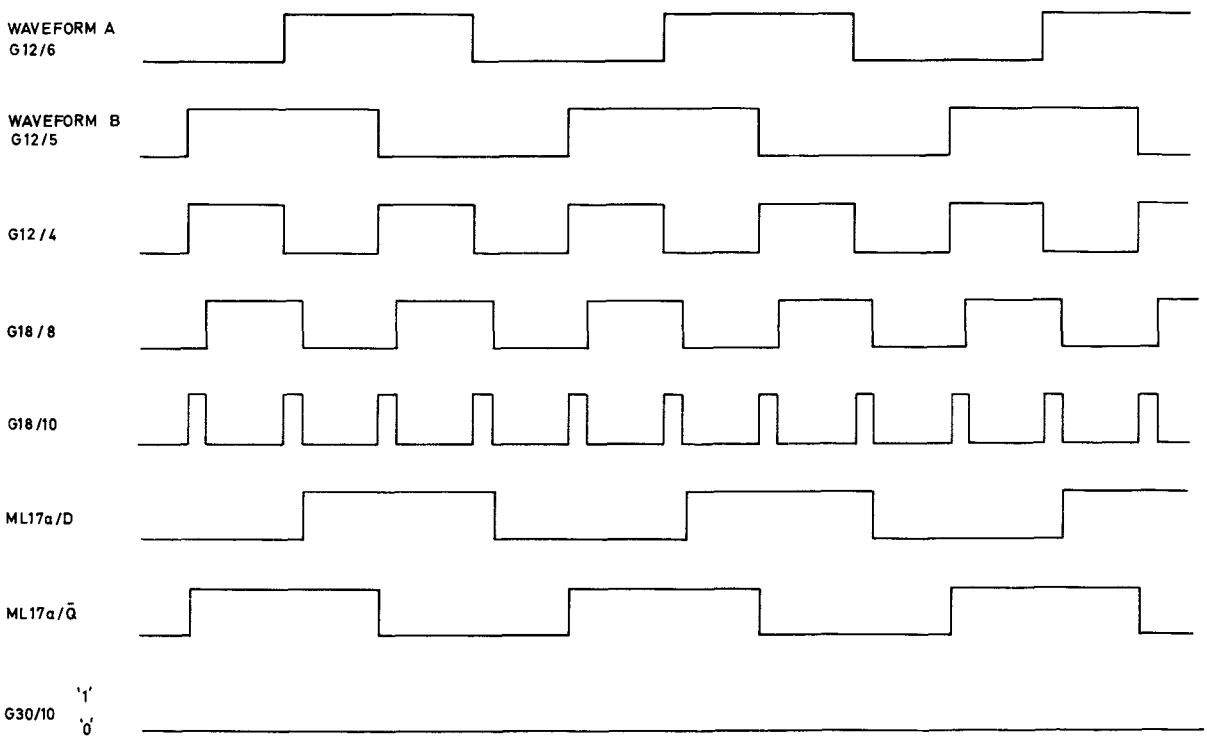
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number	Manufacturer
		FREQUENCY INTERFACE CARD (ST 78705)				
Resistors						
R1	12k	Metal Oxide		2	917952	Electrosil TR4
R2	12k	Metal Oxide		2	917952	Electrosil TR4
R3	68k	Metal Oxide		2	916478	Electrosil TR4
R4	12k	Metal Oxide		2	917952	Electrosil TR4
R5	12k	Metal Oxide		2	917952	Electrosil TR4
R6	12k	Metal Oxide		2	917952	Electrosil TR4
R7	12k	Metal Oxide		2	917952	Electrosil TR4
R8	12k	Metal Oxide		2	917952	Electrosil TR4
R9	12k	Metal Oxide		2	917952	Electrosil TR4
R10	12k	Metal Oxide		2	917952	Electrosil TR4
R11	12k	Metal Oxide		2	917952	Electrosil TR4
R12	12k	Metal Oxide		2	917952	Electrosil TR4
R13	12k	Metal Oxide		2	917952	Electrosil TR4
R14	12k	Metal Oxide		2	917952	Electrosil TR4
R15	12k	Metal Oxide		2	917952	Electrosil TR4
R16	68k	Metal Oxide		2	916478	Electrosil TR4
R17	68k	Metal Oxide		2	916478	Electrosil TR4
R18	68k	Metal Oxide		2	916478	Electrosil TR4
R19	68k	Metal Oxide		2	916478	Electrosil TR4
R20	68k	Metal Oxide		2	916478	Electrosil TR4
R21	68k	Metal Oxide		2	916478	Electrosil TR4
R22	68k	Metal Oxide		2	916478	Electrosil TR4
R23	68k	Metal Oxide		2	916478	Electrosil TR4
R24	68k	Metal Oxide		2	916478	Electrosil TR4
R25	68k	Metal Oxide		2	916478	Electrosil TR4
R26	68k	Metal Oxide		2	916478	Electrosil TR4
R27	68k	Metal Oxide		2	916478	Electrosil TR4

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number	Manufacturer
Capacitors			V			
C1	0.1	Polyester	100	10	920566	Waycom MKS 4
C2	0.1	Polyester	100	10	920566	Waycom MKS 4
C3	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C4	15	Tantalum	20	20	910060	Union Carbide K15J20S
C5	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C6	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C7	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C8	100p	Disc Ceramic	500	10	917417	Eire 831/N3300
C9	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C10	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C11	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C12	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C13	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C14	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C15	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C16	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
Diodes						
D1		Silicon			914898	STC 1N4149
Integrated Circuits						
ML1		Dual binary up-counter			930047	RCA CD 4520 BE
ML2		Hex. inverting buffer			930033	RCA CD 4049 BE
ML3		Hex. non-inverting buffer			930034	RCA CD 4050 BE
ML4		Dual 4-stage shift register			930973	RCA CD 4015 BE
ML5		Quad exclusive OR gate			930856	RCA CD 4070 BE

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number	Manufacturer
Integrated Circuits (Contd.)						
ML6		Dual D-type flip-flop			926860	RCA CD 4013 BE
ML7		Quad exclusive OR gate			930856	RCA CD 4070 BE
ML8		Quad exclusive OR gate			930856	RCA CD 4070 BE
ML9		Magnitude Comparator			931044	RCA CD 4585 BE
ML10		4-to10 Line decoder			919506	Texas SN 7442J
ML11		Quad 2-input NAND buffer			927662	Texas SN 7437J
ML12		Quad 2-input NAND gate			930028	RCA CD 4011 BE
ML13		Quad exclusive OR gate			930856	RCA CD 4070 BE
ML14		Hex. non-inverting buffer			930034	RCA CD 4050 BE
ML15		Hex. non-inverting buffer			930034	RCA CD 4050 BE
ML16		Dual D-type flip-flop			926860	RCA CD 4013 BE
ML17		Dual D-type flip-flop			926860	RCA CD 4013 BE
ML18		Quad exclusive OR gate			930856	RCA CD 4070 BE
ML19		Quad exclusive OR gate			930856	RCA CD 4070 BE
Connectors						
		14-pin DIL IC socket			927053	Texas C83-14-02
		16-pin DIL IC socket			927054	Texas C83-16-02



CLOCKWISE ROTATION
A LEADS B

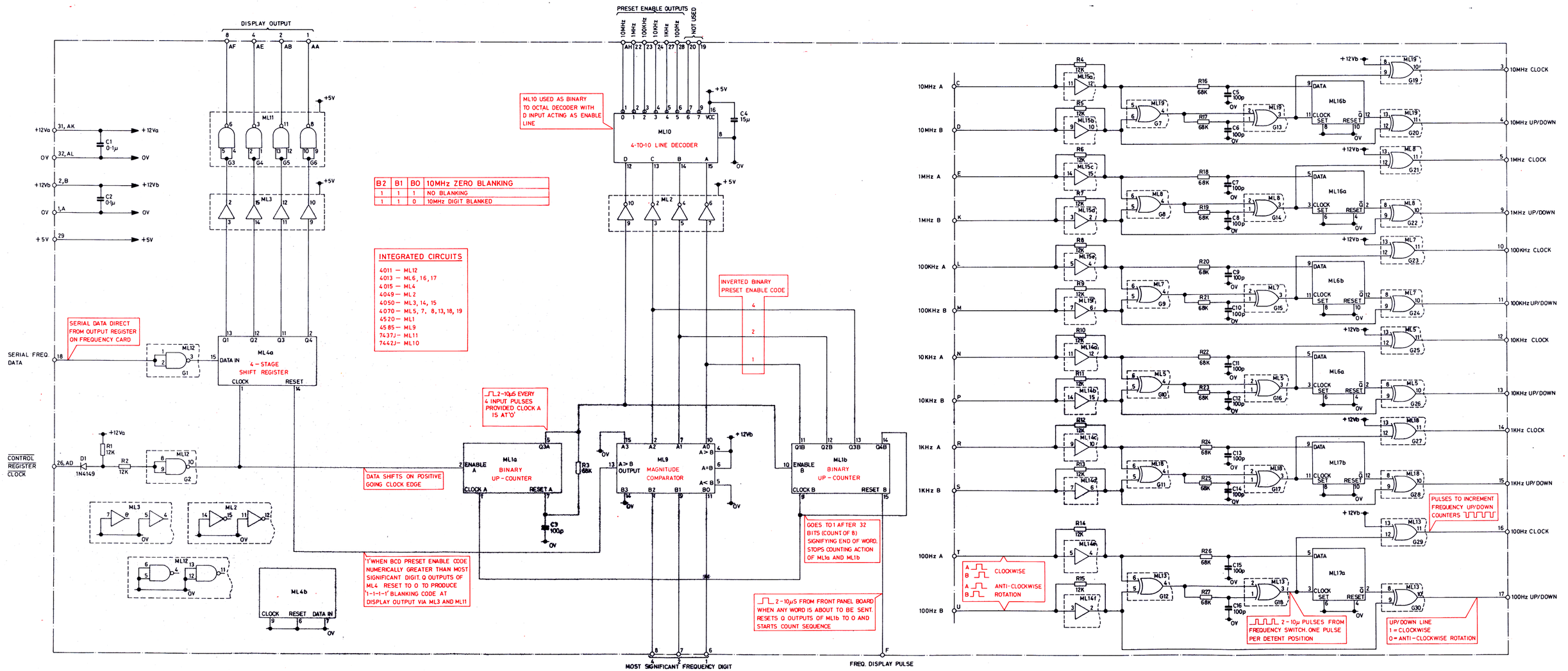


ANTI-CLOCKWISE ROTATION
A LAGS B

RACAL
WOH8307

Timing Diagram : Clock & Up/Down Signal Generation

Fig. 11·1

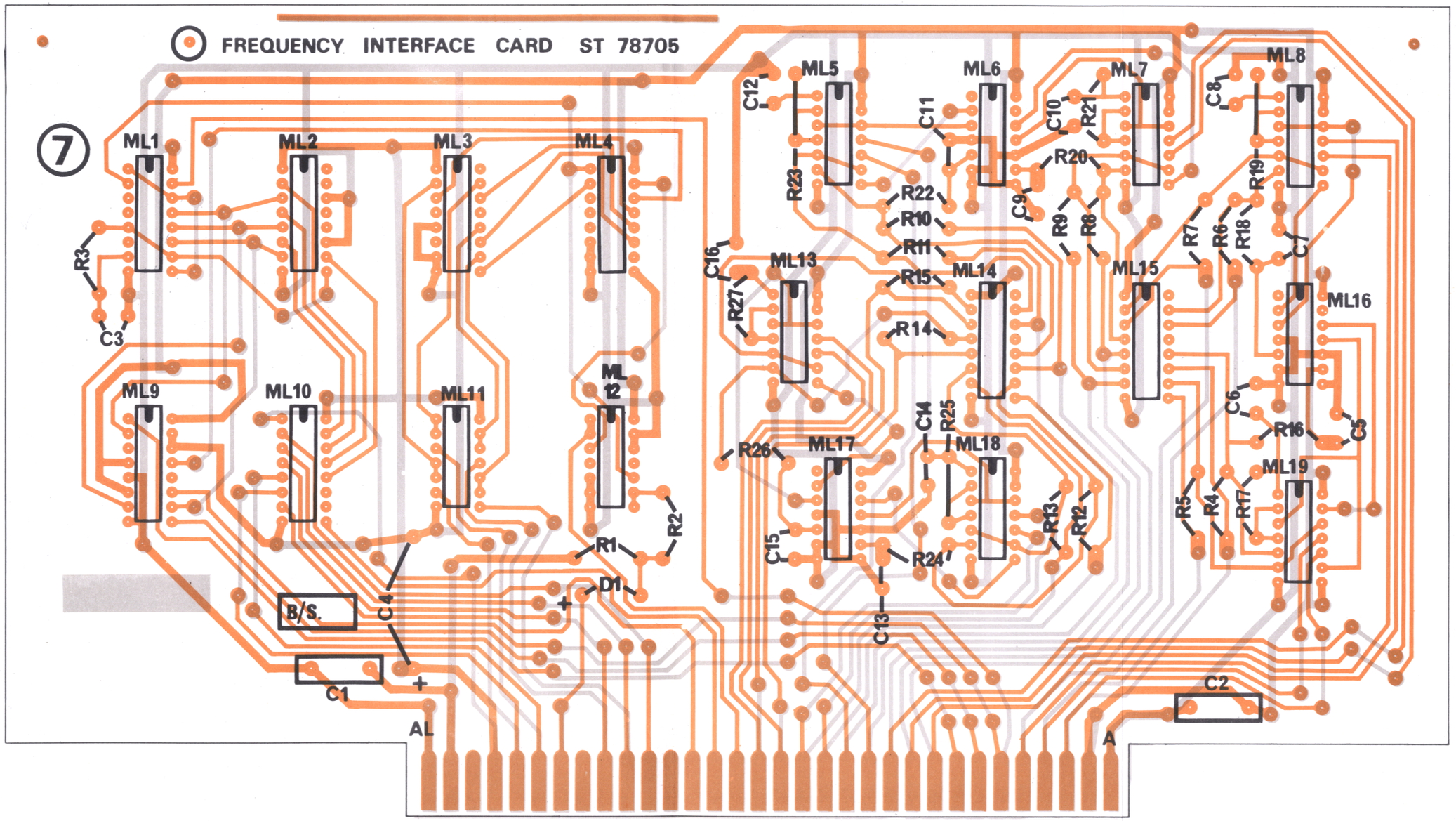


RACAL

WOH8307	DC78705	11-2	WOH8307	DC78705	11-2
1		1/2	1		2/2

Circuit :
Frequency Interface Card

Fig. 11-2



WOH 8307	DA78704	11.3
1		1/3
WOH 8307	DA78704	11.3
1		3/3
WOH 8307	DA78704	11.3
1		3/3

Layout : Frequency Interface Card

Fig. 11. 3

CHAPTER 12

CONTROL PROCESSOR CARD

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CHAPTER 12

CONTROL PROCESSOR CARD

INTRODUCTION

1. The control processor card, as its name implies, carries control circuits for various functions of the MA.1090. These include the 19.2 kHz clock generator, the word scanning circuits, the preamble generator, the frame repeater and the recall store, together with timing and data routing circuits.

FUNCTIONAL DESCRIPTION

2. A simplified block diagram of the control processor card is given in fig. 12.1; this diagram contains the essential blocks for routine data only, i.e. the new data circuitry has been omitted and is dealt with in paras. 32 to 38. The block diagram for the word scanning circuits (para. 21) is given in fig. 12.2 whilst that for the recall and preserve circuitry (para. 39) is given in fig. 12.3. The circuitry included for use with multiplex installations is described in para. 75.

CLOCK GENERATOR (Fig. 12.1)

3. The clock generator produces a 19.2 kHz squarewave output which is used as the reference clock signal for the whole of the unit. If an externally generated clock signal is applied to board pin 5 (via PL1 pin 1 on the rear panel) the internal clock generator is automatically inhibited.

COUNTER AND CONTROL (Fig. 12.1)

4. The output signal from the clock generator is applied to the clock input of a 7-stage binary counter ML33. The Q1 to Q5 outputs are used to address the recall memory, the Q5 and Q6 outputs are applied to the counter control circuit (which generates the counter reset signal), and the Q6 output opens gate G4 for the clock signal which is applied to the word scanning circuits. The action of the circuit is described in the following paragraphs which should be read in conjunction with the truth table for the 7-stage binary counter given in Table 1.

5. The counter is reset by a logic '1' level pulse at the reset terminal, which sets the Q1 to Q6 outputs to logic '0'. The counter is then advanced one count on the negative-going transition of each input clock pulse. The Q6 output changes to a '1' at the negative-going edge of clock pulse 32 (Table 1) and is maintained in this state until clock pulse 48, when the counter is reset by the combination of the Q5 and Q6 outputs. Thus the Q6 output opens gate G4 for a total of 16 clock pulses which are applied to the word scanning circuits (para. 7).

TABLE 1: 7-STAGE BINARY COUNTER TRUTH TABLE

CLOCK INPUT	BINARY OUTPUT						CLOCK INPUT	BINARY OUTPUT					
	32 Q6	16 Q5	8 Q4	4 Q3	2 Q2	1 Q1		32 Q6	16 Q5	8 Q4	4 Q3	2 Q2	1 Q1
RESET	0	0	0	0	0	0	27	0	1	1	0	1	1
1	0	0	0	0	0	1	28	0	1	1	1	0	0
2	0	0	0	0	1	0	29	0	1	1	1	0	1
3	0	0	0	0	1	1	30	0	1	1	1	1	0
4	0	0	0	1	0	0	31	0	1	1	1	1	1
5	0	0	0	1	0	1	32	1	0	0	0	0	0
6	0	0	0	1	1	0	33	1	0	0	0	0	1
7	0	0	0	1	1	1	34	1	0	0	0	1	0
8	0	0	1	0	0	0	35	1	0	0	0	1	1
9	0	0	1	0	0	1	36	1	0	0	1	0	0
10	0	0	1	0	1	0	37	1	0	0	1	0	1
11	0	0	1	0	1	1	38	1	0	0	1	1	0
12	0	0	1	1	0	0	39	1	0	0	1	1	1
13	0	0	1	1	0	1	40	1	0	1	0	0	0
14	0	0	1	1	1	0	41	1	0	1	0	0	1
15	0	0	1	1	1	1	42	1	0	1	0	1	0
16	0	1	0	0	0	0	43	1	0	1	0	1	1
17	0	1	0	0	0	1	44	1	0	1	1	0	0
18	0	1	0	0	1	0	45	1	0	1	1	0	1
19	0	1	0	0	1	1	46	1	0	1	1	1	0
20	0	1	0	1	0	0	47	1	0	1	1	1	1
21	0	1	0	1	0	1	RESET	1	1	0	0	0	0
22	0	1	0	1	1	0		MULTIPLEX ONLY					
23	0	1	0	1	1	1	49	1	1	0	0	0	1
24	0	1	1	0	0	0	50	1	1	0	0	1	0
25	0	1	1	0	0	1	51	1	1	0	0	1	1
26	0	1	1	0	1	0	52	1	1	0	1	0	0

6. The combination of the Q5 and Q6 outputs from the counter (at clock pulse 48) also produces the start-of-frame pulse; this is applied to the control register strobe pulse generator ML2a and to the frame counter ML25b (para. 8), whilst the inverted form of the start-of-frame pulse is applied to the clock input of a quad D-type latch for the status input signals RECALL, PRESERVE, CHECK and THROUGH.

WORD SCANNING

7. The word scanning circuits are described in detail in paras. 21 to 31 in conjunction with fig. 12.2; briefly, as far as routine control data is concerned and ignoring the preserve circuitry, the routine data word numbers, i.e. words 0, 1 and 3, are sequentially applied, in binary form, to the four word enable lines. These lines are connected to the preamble generator to set the data word ident (bits 12 to 15); they are also applied via inverters TR3, TR5, TR6 and TR7, and board pins 19 to 22, in parallel to the frequency card (word 1) and the front panel board (word 3).

CONTROL REGISTER STROBE PULSE GENERATOR AND FRAME COUNTER (Fig. 12.1)

8. The control register strobe pulse generator consists of a D-type flip-flop ML2a, where the level at the D input is set by the Q output of the frame counter D-type flip-flop ML25b. Prior to the start-of-frame pulse from the counter control circuit (para. 6), the Q output of ML25b is at logic '1'. This is inverted by NOR gate G33 and again by NAND gate G30 to set the D input of ML2a to a '1'. The start-of-frame pulse is applied to the clock input of ML2a, and the Q output changes to a '1' for a period of time determined by the time constant components R38 and C11 (5 μs nominal) after which time the stage is reset. This positive-going pulse resets the frame counter ML25b, and the Q output changes to a '0'; this is applied via G33 and G30 to the D input of ML2a so that when the second start-of-frame pulse is applied to the clock input no change occurs in the state of the Q and $\overline{Q}$ outputs. For routine data therefore, the strobe pulse is only generated at the start of a pair of 48-bit frames. This pulse is applied as a parallel entry enable pulse to the 16-bit preamble generator (para. 10), and via inverting buffer TR8 and board pin 24 to the 32-bit output shift register stages on the frequency card (word 1) and the front panel board (word 3). The inverted control register strobe pulse is taken from the $\overline{Q}$ output of ML2a and is applied to the word scanning circuits (para. 21).

9. The second start-of-frame pulse is applied to the clock input of ML25b and the '1' at the D input is transferred to the Q output. Thus for routine control data the Q output is at a '0' for the first of a pair of 48-bit frames, and at a '1' for the second. This signal is used to control the output of the frame repeater ML28 via an analogue multiplexer ML15b (para. 11).

PREAMBLE GENERATOR (Fig. 12.1)

10. The preamble generator comprises two 8-stage shift registers ML26, ML27. The 16-bits of the preamble are applied to the parallel input terminals and are loaded into the registers by the application of the control register strobe pulse.

FRAME REPEATER AND CONTROL (Fig. 12.1)

11. The frame repeater consists of a 48-stage shift register ML28, where the serial data output is controlled by the analogue multiplexer ML15b; this device acts as a single-pole changeover switch where a logic '0' at the control input connects the D0 terminal to the common terminal, and a logic '1' at the control input connects the D1 terminal to the common terminal. The level at the control input is governed by the output signal from the frame counter (paras. 8 and 9); since this is a '0' for the first of a pair of 48-bit frames, the 16-bit preamble, followed by the 32-bit control register data word (at board pin 25 and routed via G22 and the recall and preserve circuitry), is clocked into the frame repeater stage ML28 and at the same time is routed through ML15b, D0 to common.

12. For the second 48-bit frame (of the pair), the frame counter output signal changes to a '1' and the content of the frame repeater is clocked out and routed through ML15b, D1 to common.

EXTERNAL ENTRY SELECT (Fig. 12.1)

13. The serial control register data output from the common terminal of ML15b is routed via a further analogue multiplexer ML15c, which is controlled by the logic level at the external entry select input line connected to board pin J. When the front panel EXTERNAL socket is not in use, the +12V at the input of ML18 is inverted to produce a '0' at the control input of ML15c; this connects the D0 terminal to the common terminal and the serial data is routed through to the AND/OR select gate ML30 (para. 15).

14. When the EXTERNAL socket is in use and data is being entered (from, for example, the MA.1083 frequency entry pad), the external entry select line is connected to 0V (logic '0'); this results in a '1' at the control terminal of ML15c, and the 0V input at the D1 terminal is connected to the common terminal. The control register data output from ML15b is thus inhibited whilst external data is being entered.

AND/OR SELECT GATE (Fig. 12.1)

15. The AND/OR select gate ML30 is controlled by the THROUGH status input signal at board pin L; this input is set to a '1' when the IN status is selected at the front panel, or by the computer via the word 9 data, to route the transfer data and clock signals at board pins T and U to the control highways.

16. When the inverted start-of-frame pulse clocks the quad D-type latch ML17, the logic '1' THROUGH signal at the Q3 output sets the KA input of ML30 to a '0' and the KB input to a '1'; this connects the B1 and B2 inputs to the D1 and D2 outputs respectively, and the transfer data and clock signals are routed via ML30 and the level conversion output stages (para. 19) to the control data and clock highways.

17. When the THROUGH status bit is not set to a '1', the KA input of ML30 is set to a '1' and the KB input is set to a '0'; this connects the A inputs to the D outputs, and the control register data from ML15c, together with the control clock signal from G17, are applied to the control highways via the level conversion stages.

18. The control data and clock signals are also applied via board pins R and S to the display processor card when the RECALL status is selected, and to the status card, where they are routed to the exchange highways when the OUT status is selected.

LEVEL CONVERSION STAGES (Fig. 12.1)

19. The two level conversion output stages convert the C-MOS logic level clock and data signals to plus and minus 12V signals (to comply with the recommendations of CCITT V28 - Chap. 5), where +12V represents logic '0' and -12V represents logic '1'. The two stages are enabled by a '0' output signal from the power fail detector (para. 20).

POWER FAIL DETECTOR (Fig. 12.1)

20. The power fail detector, TR16, is powered from the internal battery supply (+12 Vb) and monitors the +12 Va supply from the power supply module via R51 and 10V zener diode D13; should the +12 Va supply fall to less than 10 volts, TR16 cuts off, and the level conversion stages are disabled.

WORD SCANNING CIRCUITS

21. A simplified diagram of the word scanning circuits is given in fig. 12.2. This diagram does not include the PRESERVE and RECALL elements which modify the action of the routine and new data circuits described in the following paragraphs. For details of the PRESERVE and RECALL circuitry refer to para. 39.

Routine Control Data

22. Routine control data is transferred to the transmitter when no new data is being generated, i.e. during the period when no control settings are being altered. The control word frames are sent in pairs in numerical order (0, 1, 3) and the sequence is then repeated continuously.

23. The frame sequence is controlled by the word present counter ML13; this is a 4-bit binary up/down counter which is set to count up by taking the up/down line to +12V. When the carry-in input is at logic '0', the counter advances on the positive-going transition of the clock input; it counts sequentially from 0 to 15 and then restarts at 0. When the carry-in input is at logic '1' the counting action is stopped. A logic '1' at the preset enable (PE) input presets the counter to the number applied to the binary inputs, P1 to P4. (The word present counter is preset to binary '1' by the start-of-preserve pulse, see para. 44).

24. The Q1 to Q4 binary output from the word present counter is connected to the preset inputs of the new data counter ML12, which is controlled by a sequence start pulse derived from the inverted control register strobe pulse. The action of the two counters for routine control data is as follows.

25. As an arbitary starting point, assume that the last pair of control word frames sent contained word 1, in which case the word present counter is stopped at binary 3 in readiness for the next pair of frames (the inverted word present signal from the front panel board is at logic '0'; this is inverted by G2 and sets the Q output of ML7a to a '1' which stops the counting action of ML13).

26. Since no new data is present, the inverted new data line, at board pin AA, is at logic '1'; this is inverted by G3, the D input of ML7b is at logic '0' and the new data counter ML12 is enabled by the logic '0' Q output of ML7b.

27. The next control register strobe pulse is applied to the reset input of ML7b; this has no effect however, since the Q output is already at logic '0'. The inverted control register strobe pulse is applied to NOR gate G5 and the resulting '1' output resets ML7a; this sets the Q output to a '0' and the word present counter is enabled. The '1' output from G5 is also applied to the preset enable input of the new data counter which is then preset to binary 3.

28. The clock signal, which is applied in parallel to both counters, is disabled (when the control register strobe pulse is generated) for a period of 32 bits; during this time the mode word is clocked out of the 32-bit output shift register on the front panel board and is routed via board pin 25 and G22 (fig. 12.1) to the serial input of the preamble generator.

29. The next clock pulses are applied to both counters which count up from 3 to 15 and then to 0; the word present counter is then stopped by the '1' output from the word 0 detector (G18, G20, G21) which is applied to the carry-in input via NAND gates G1 and G2 and the D-type flip-flop ML7a (the resulting '0' $\overline{Q}$ output from ML7a maintains the '1' at the D input via G2). The new data counter however, continues to count, searching for new data words. As, in this example, no new data is present, it counts from 0 to 3 when the clock input signal to the two counters is again disabled for a period of 32 clock pulses. During this time the second 32-bit mode word is clocked out of the frame repeater stage ML28 (fig. 12.1).

30. When the clock signal reappears the word present counter remains at 0 (stopped by the logic '1' Q output from ML7a); the new data counter, however, continues to count as before, searching for new data words. It counts from 3 to 15, back to 0 and then to 3, when the next sequence start pulse presets it to 0.

31. The control sequence is now repeated for words 0 and 1 and the complete sequence is then repeated starting again at word 3 (words 2 and 4 to 15 are not used and therefore the word present counter does not stop at these numbers).

New Control Data

32. Every time a control setting is altered at the front panel controls, new control data is required to be sent as soon as possible. The routine control sequence is interrupted and the new data frames are inserted at the end of the routine frame currently being sent. The action of the circuit for new control data is as follows.

33. Using the frequency word as an example, when the RESET push-button is pressed, a signal is routed to the set input of the frequency word new data latch. The next time that the new data counter applies binary 1 to the word enable lines, the inverted new data signal (logic '0') from the frequency card, at board pin AA, is inverted by G3 and applied as a '1' to the D input of flip-flop ML7b. At the same time the logic '0' inverted word present signal from the frequency card at board pin 18, is inverted by G2 and applied as a '1' to the D input of flip-flop ML7a. At the positive-going transition of the next clock pulse, which is applied to both flip-flops, the logic '1' Q output from ML7b stops the new data counter at binary 1 and the logic '1' Q output from ML7a stops the word present counter at whatever number it is set to.

34. If the inverted new data signal at board pin AA occurs during the transmission of the second frame of a pair of frames, then the next control register strobe pulse resets ML7b, the Q output changes to a '0' and the stop signal is removed from the new data counter ML12. The '1' output from G3 however, closes NOR gate G5 and thus prevents the production of the sequence start pulse, which would otherwise reset ML7a and preset enable ML12.

35. The control register strobe pulse, which is applied in parallel to all the data cards via board pin 24, resets the new data latch on the frequency card (whilst word 1 is enabled - Chap. 10). This removes the logic '0' inverted new data signal at board pin AA, the output of NOR gate G3 changes to a '0', and NOR gate G5 is opened for the next inverted control register strobe pulse (unless, in the mean time, a further new data latch is set).

36. The clock signal is disabled for a period of 32-bits, and during this time the new data frequency word is clocked out of the 32-bit output shift register on the frequency card. The next sixteen clock pulses are applied to the clock input of the new data counter, which counts up from 1, searching for further new data words. If no further new data words are present the counter counts from 1 to 15, back to 0 and then to 1, when the clock input is again disabled for 32-bit periods, and the second frequency word frame is clocked out of the frame repeater.

37. When the clock signal reappears the word present counter remains in the stopped condition (the '0' at the $\overline{Q}$ output of ML7a maintains the '1' at the Q output via G2) but the new counter continues to count as before, searching for further new data words. It counts from 1 to 15, back to 0 and then to 1 when the next sequence start pulse presets it to the binary number held in the word present counter. The routine control data sequence now recommences at the point where it was interrupted by the new data frequency word, and continues until it is again interrupted by a further new data word.

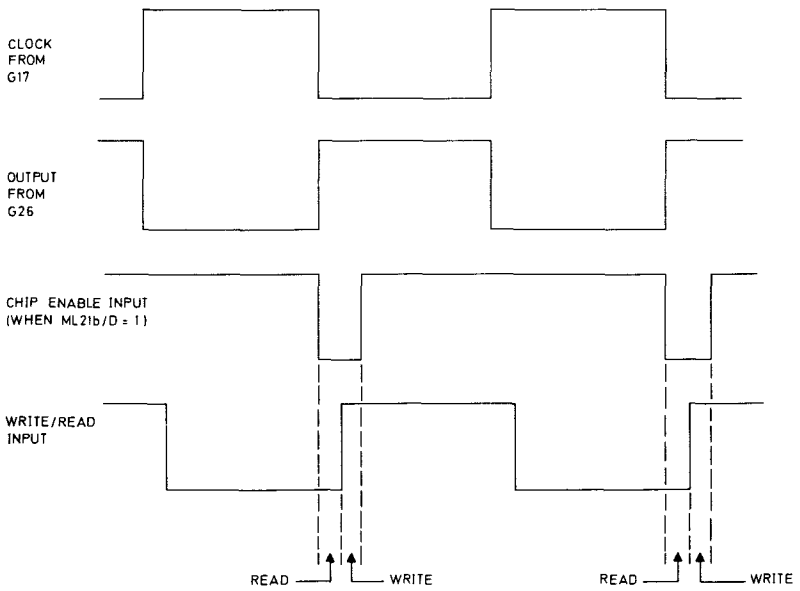
38. If the inverted new data signal at board pin AA occurs during the transmission of the first frame of a pair of frames, then the frame counter has already counted one frame and the next control register strobe pulse is not due to occur until two frames have been counted. To overcome this, the inverted new data signal is also used to reset (via the D input) the frame counter and to generate the control register strobe pulse after the completion of the frame currently being sent; this circuitry (ML3a, G32) is shown in fig. 12.3. After the new data frames have been transferred, the routine control data sequence recommences with the second frame of the interrupted pair of frames.

RECALL AND PRESERVE CIRCUITRY (Fig. 12.3)

RECALL STORE

39. The recall store consists of a 256-bit static random access memory (RAM) ML22, which is arranged to store bits 16 to 47 inclusive for words 1 to 7 inclusive. Information at the data-in terminal is written into the memory location selected by the address inputs (A0 to A7) when the chip enable input is at logic '0' and the write/read input is at logic '1'. Information is read from the memory location selected by the address inputs when both the chip enable and the write/read inputs are at logic '0'. When the chip enable input is at logic '1', the data-out terminal is held in the high-impedance OFF state.

40. The clock signal from G17 is applied to the write/read input via a delay circuit, G24, G25; it is also applied via inverting exclusive OR gate G26 to the clock input of ML21b which routes a '0' to the chip enable input when a '1' is produced by the preserve enable circuit (para. 46). From the timing diagram for the chip enable and write/read inputs given in fig. 12 (i), it can be seen that for the first half of each logic '0' chip enable period, the read function is performed, and for the secondhalf, the write function is performed.



RACAL Timing Diagram : Chip Enable & Write/Read Inputs Fig. 12(i)

41. The delayed clock signal is also applied to the clock input of ML21a, so that when the RECALL status is latched ('1' from ML17 applied to the control input of the analogue multiplexer ML15a, which connects the D1 terminal to the common terminal), each addressed data bit is temporarily stored by ML21a during the read period before being over-written in the memory during the write period.

PRESERVE CIRCUITRY

42. The PRESERVE input, at board pin P, is from the status card (Chap. 13) and is set to a '1' by the computer (via the word 9 data), when the IN, RECALL or CHECK status is selected at the front panel, or by the EXTERNAL SET CHECK input (at PL2 pin 25 on the rear panel).

43. When the quad latch ML17 is clocked by the inverted start-of-frame pulse (para. 6), the logic '1' PRESERVE input at the D4 terminal is maintained at the Q4 output, and a '0' is maintained at the $\overline{Q4}$ output.

44. The logic '1' Q4 PRESERVE signal is applied to the following:-

(1) G3 (fig. 12.2) to force the output to a '0' and so override the new data circuitry (para. 33).

(2) The reset input of ML3a; the $\overline{Q}$ output is held reset at a '1', this forces the output of G32 to a '0' and an inverted new data input signal is prevented from resetting the frame counter (ML25b) and generating the control register strobe pulse (para. 38 and fig. 12.1).

(3) G27, via a nominal 5 μs delay circuit (R14, C4), together with the logic '0' $\overline{Q4}$ output from ML17. The resulting 5 μs positive-going output pulse is applied to:-

(a) The set input of ML2a (fig. 12.1) to generate the control register strobe pulse.

(b) The preset enable input of the word present counter ML13 (fig. 12.2) as the start-of-preserve pulse; ML13 is preset to binary 1, and the inverted control register strobe pulse is inverted again by G5 (fig. 12.2) to produce the sequence start pulse. This is applied to the preset enable input of the new data counter ML12, which applies binary 1 to the four word enable lines. The sequence start pulse also resets ML7a, the Q output is reset to a '0', and this is applied to the carry-in input of ML13. Similarly, ML7b is reset by the control register strobe pulse and the '0' at the Q output is applied to the carry-in input of ML12.

(4) The D input of ML3b (fig. 12.3); when the word number present on the four word enable lines eventually reaches binary 8 (signifying that the words in use in the range 1 to 7 have been preserved in the recall store), ML3b is clocked by the resulting '1' at the '8' level word enable line, the '1' at the D input is transferred to the Q output, and a 5 μs (nominal) positive-going pulse is produced (reset applied via R1, C1). This is routed via board pin N to the status card to reset the preserve status.

45. At the same time, the logic '0' $\overline{Q4}$ output from ML17 is applied to the following:-

(1) G11 (fig. 12.2). The remaining input to this gate is from the $\overline{Q}$ output of ML7a. When the word detector on the frequency card detects the presence of binary 1 at the four word enable lines, a logic '0' word present signal is generated, and this is applied to G2 via board pin 18 (fig. 12.2). The resulting '1' output from G2 is applied to the D input of ML7a and this is transferred to the Q output by the first of the 16 applied clock pulses (para. 5) Thus a '1' is applied to the carry-in input of ML13 to prevent any counting action, and the '0' $\overline{Q}$ output from ML7a is applied to G11. The resulting '1' output sets ML7b, the '1' Q output stops ML12 counting up, and the binary 1 at the four word enable lines is maintained.

(2) G28 (fig. 12.3) together with the '0' Q2 output from ML17; ML2b is set, the '0' $\overline{Q}$ output is applied to G30 (fig. 12.1) and results in a '1' at the D input of ML2a. This ensures that a control register strobe pulse is generated for each frame (by the start-of-frame pulse) instead of one pulse for each pair of frames (para. 8).

(3) The preserve enable circuit G14, G15, G16, which produces a '1' output for the correct input conditions (para. 46).

Preserve Enable Circuit (fig. 12.3)

46. This circuit comprises three NOR gates G14, G15, G16, and produces a '1' output to ML21b (para. 40) when the four input signals are at logic '0'; these inputs are listed below:-

(1) The $\overline{Q4}$ output from ML17, signifying that the preserve status has been selected.

(2) The Q6 output from the binary counter ML23; this output is at logic '0' for a total of 32 clock pulses (0 to 31, table 1) which correspond to data bits 16 to 47.

(3) The Q output from the frame counter ML25b (fig. 12.1). This output is at logic '0' whilst the first of a pair of frames is being sent; since the control register data at board pin 25 consists of all-zeros whilst the second frame is being re-produced by the frame repeater ML28, it is essential that the

preserve sequence commences coincident with the arrival of the first data frame.

(4) The binary 8 word enable line, which is at logic '0' for words 1 to 7 inclusive.

Memory Addressing (Fig. 12.3)

47. The inverted word 1 control register data at board pin 25 (from the frequency card) is inverted by G22 and is then applied to the data-in terminal of ML22, and to the D0 input of ML15a. Since the RECALL status is not selected, a '0' is applied to the control input of ML15a (ML17 Q2 output); this connects the D0 terminal to the common terminal, and the word 1 data is thus applied to the D input of ML21a.

48. The binary 1 at the word enable lines is routed to the A0, A2 and A1 address lines of ML22, to select the word 1 memory location, whilst the Q1 to Q5 binary outputs from ML23 select the bit location for each of the 32 word 1 data bits (16 to 47) via the memory address lines A3 to A7. Thus after the application of 32 clock pulses to ML23, the word 1 data is stored in the memory and has also been clocked out of ML21a to the 16-bit preamble generator (fig. 12.1).

49. At the negative-going edge of clock pulse 32, the Q6 output from ML23 changes to a '1' (Table 1). This is applied to the preserve enable circuit G14, G15, G16, to remove the '1' enable output (fig. 12.3), and is also applied to G4 (fig. 12.1) to allow the application of 16 clock pulses to the word scanning circuits (fig. 12.2). The word present counter ML13, and the new data counter ML12 (fig. 12.2), both count up until binary 3 is applied to the four word enable lines. The logic '0' word present signal is generated on the front panel board, and this is applied to G2 (fig. 12.2); the resulting '1' output is applied to the carry-in input of ML13 via ML7a, the '1' output from G11 sets ML7b, and the '1' Q output is applied to the carry-in input of ML12. Thus both counters are stopped and the binary 3 at the word enable lines is maintained.

50. When the binary counter ML23 reaches a count of 48, the start-of-frame pulse is produced and the counter is reset (para. 6). The control register strobe pulse is produced, as is the logic '1' preserve enable signal, and the word 3 data is both preserved in the recall store and routed via ML21a to the preamble generator, as described above for the word 1 data.

51. The sequence is then repeated for any remaining operational words up to 7 (i.e. any undesignated words used for external control functions) where the counters are stopped at the appropriate number by the inverted word present signal. The preserve reset signal is then generated (when the number applied to the four word enable lines reaches binary 8 - para. 44 (4)), and the logic '1' PRESERVE input at board pin P is reset to logic '0'.

RECALL CIRCUITRY (Fig. 12.3)

52. Since the PRESERVE status is automatically selected when the front panel RECALL push-button is pressed, the circuit operation is similar to that described in paras. 42 to 51 with the following exceptions.

(1) The logic '1' Q2 output from ML17 is applied to G28 to remove the set input to ML2b (para. 45 (2)); this prevents the generation of the control register strobe pulse for each frame (the initial control register strobe pulse is still generated via G27 - para. 44 (3)); up-dating of the control register data from the control word cards is prevented, and hence the existing front panel settings are preserved in the recall store.

(2) The logic '1' Q2 output from ML17 is also applied to the control input of the analogue multiplexer ML15a; the D1 terminal is connected to the common terminal, and each data bit output from the memory is transferred to ML21a before the addressed location is overwritten with the front panel setting data from G22.

CIRCUIT DESCRIPTION

53. The operation of the various circuits on the control processor card are described in the preceding paragraphs in conjunction with figs. 12.1 to 12.3. The following paragraphs should be read in conjunction with fig. 12.4.

CLOCK GENERATOR

54. ML19 is connected as an astable (free-running) multivibrator and produces a 19.2 kHz square wave signal (timing components C6, R15) at the Q output when the astable input (pin 5) is maintained at logic '1'.

55. If an externally applied master clock is in use, it is routed via board pin 5 to a Schmitt trigger circuit TR2, ML18; the negative-going excursion of the waveform at the collector of TR2 keeps C3 discharged via D5, and ML19 is inhibited.

56. The clock output signal from either ML19 or the Schmitt trigger is inverted by G13, inverted again by G17 (the collector of TR4 is normally at 0V - para. 76) and is then applied as the reference clock for the whole of the unit via inverting buffer ML16, open collector output inverter TR15, and board pin 26.

CONTROL DATA MODIFY

57. The control register data from the word cards is applied via a common connection to board pin 25, and is then applied to an exclusive OR gate G22; the remaining input to this gate is normally at logic '1' (+12V via R49, R45) but may be pulled down to 0V via the control data modify line at board pin 11, which is routed from PL2 pin 24 on the rear panel.

58. This facility, which is not normally used with the MA.1090, is provided so that external equipment using the extra word facility may modify the control register data to suit a particular requirement.

COUNTER CONTROL CIRCUIT

59. The counter control circuit comprises NAND gates G6, G8, NOR gates G9, G10, G12, and a D-type flip-flop ML25a; it produces the reset signal for the 7-stage binary counter ML23, and also the start-of-frame pulse (paras. 5, 4 and 6).

60. The input to G10 at ML24 pin 13, which comes from the ready for sending circuit (para. 76), is normally at logic '1' and results in a '0' at the output which is applied to G9. The remaining input to G9 changes to '0' when the binary counter reaches a count of 48 (Q5 and Q6 outputs both at logic '1', gated by G6 - Table 1) a '1' is applied to the set input of ML25a, and a positive-going 5 μs (nominal) pulse is produced (reset applied via R23, C10). ML23 is reset (Q1 to Q6 outputs reset to '0'), the inverted start-of-frame pulse is produced from G8, and the start-of-frame pulse is produced via inverting NOR gate G12.

WORD DETECTOR

61. The word detector uses three NOR gates G18, G20, G21; it produces a '0' output from G21 when binary 0 or binary 1 is present at the four word enable lines, and a '1' at the output of G18 when the four word enable lines are at zero.

62. When the four word enable lines are at zero, the '1' output from G20 is inverted by G21; this is inverted again by G18 and the word present counter ML13 is stopped at a count of zero via G1, G2 and ML7a (para. 23). When binary 1 is applied to the four word enable lines, the output from G21 is still at logic '0' and this is applied to G23 as a word 1 present signal.

PREAMBLE GENERATOR

63. The preamble generator comprises two cascaded 8-stage shift registers ML26, ML27. These are parallel or serial input/serial output devices. When the parallel/serial control input is at logic '0', data is serially shifted into and out of the register synchronously with the positive-going transition of the applied clock waveform; when the parallel/serial control input is at logic '1', the data at the parallel input pins P1 to P8 is loaded into the register independently of the applied clock waveform.

64. The sync. code (a '0' followed by five '1's) is set at the P3 to P8 inputs of ML27, whilst the transmit/receive (PTT) bits at the P1 and P2 inputs are set according to the level applied to board pin 8 ('0' for transmit, '1' for receive). Bit 8 of the preamble, at ML26 P8 (control inhibit bit) is set to a '1' by the Q1 output from the quad D-type latch ML17 when the CHECK status is selected.

65. The return monitor bit (bit 9 of the preamble, at the P7 input of ML26, is not used in the MA.1090. Since the frequency frame comparison input, at board pin 4, is also unused, a '1' is applied to NOR gate G23 (+12 Va via R21, R22) and a permanent '0' is routed to the P7 input of ML26, and to the D input of ML2b.

66. The address bits of the preamble (bits 10 and 11) are both set to logic '0' (ML26, P5 and P6) whilst the four data word ident bits are set to the binary number present at the four word enable lines.

FRAME REPEATER

67. The frame repeater uses a variable length shift register ML28 which is set to 48 bits (equal to the sum of the enabled length control subscripts plus 1). It stores the first of a pair of 48-bit frames (which is also routed via analogue multiplexer ML15b, D0 to common); the frame counter ML25b then applies a '1' to the control input of the ML15b, and the content of ML28 is clocked out via ML15b, D1 to common, as the second 48-bit frame.

3-STATE V28 LINE DRIVERS

68. The data and clock output signals from the AND/OR select gate ML30 (para. 15) are applied to a pair of C-MOS to V28 level conversion stages ML29a, TR9, TR11, TR12 and ML29b, TR10, TR13, TR14. ML29 is a dual binary to 1-of-4 inverter; each section has two select inputs (A and B), an enable input and four mutually exclusive outputs ($\overline{Q0}$ to $\overline{Q4}$). When the enable input is at logic '1', the outputs remain at logic '1' regardless of the state of the A and B select inputs. A truth table for each half of ML29 is given in Table 2.

69. ML29a is enabled by the logic '0' output from the power fail detector (para. 20). In the event of a supply failure, the enable signal is removed, the $\overline{Q0}$ and $\overline{Q3}$ outputs are forced to logic '1' and the two PNP transistors TR9, TR11 are held off.

70. From Table 2 it can be seen that a logic '1' at the A and B inputs results in a '1' at the $\overline{Q0}$ output and a '0' at the $\overline{Q3}$ output; TR11 is held off whilst TR9 conducts and turns on TR12 to produce a -12V output at board pin 6 via D8 and R46. A '0' at the A and B inputs results in a '0' at the $\overline{Q0}$ output and a '1' at the $\overline{Q3}$ output; this time TR9 is held off, and TR11 is turned on to produce a +12V output at board pin 6 via D7 and R46.

TABLE 2: BINARY TO 1-OF-4 INVERTER TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	B	A	$\overline{Q3}$	$\overline{Q2}$	$\overline{Q1}$	$\overline{Q0}$
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

X = don't care

71. Resistor R36 and capacitor C14 provide a short time constant to allow one transistor to switch off before the other is driven on, and so prevent the destruction of both TR11 and TR12.

72. The level conversion stage for the clock output signal from ML30 is similar to that described above; a '0' at the $\overline{Q0}$ output turns on TR13 for a +12V output, whilst a '0' at the $\overline{Q3}$ output is inverted by TR10 to turn on TR14 for a -12V output. The control highway clock signal is not inverted however, due to the presence of inverter ML16 in the A2 input circuit of ML30.

CLOCK DELAY CIRCUITS

73. The clock signal from G17 is applied to the write/read input of the memory, ML22, via a delay circuit G25, G24, and to the chip enable input of the memory via G26 and ML21b when a '1' is produced by the preserve enable circuit (paras. 40 and 46).

74. The clock input signal to G25 is delayed by approximately 2 μs by the time constant presented by R35, C13, and the inverted output from G25 is applied to a buffer G24 which imparts a fast rise-time to the output waveform. ML21b produces a nominal 5 μs negative-going chip enable pulse, as the reset is applied after the time constant presented by R32, C12 has been overcome.

MULTIPLEX INSTALLATIONS

75. Externally connected multiplex equipment may be used to allow up to eight MA.1090 control units to control a similar number of remotely located transmitters over a single data link using a pair of data modems. For routine data, the time sharing technique is used whereby a ready for sending (RFS) signal is sent in turn to each MA.1090, and one 48-bit frame from each MA.1090 is sent in turn to each respective transmitter. The multiplex equipment generates a 4-bit code which is added to the front of each frame, and this code is used by the multiplex equipment at the transmitter location to route each data frame to the correct transmitter.

76. The multiplex equipment routes a negative voltage (more negative than approximately -3V) to the RFS input at each MA.1090 (routed from PL1 pin 3 on the rear panel to board pin M). This turns off TR4, the resulting '1' at the collector inhibits the clock output from G17, and is also inverted by ML16 to produce a '0' at one input of G10. The remaining input to G10 is from the Q3 output of the 7-stage binary counter; from Table 1 it can be seen that at clock pulse 52, the Q3, Q5 and Q6 outputs are all at logic '1', and the counter is reset via G9 and ML25a. Thus whilst the negative RFS input is applied, the binary counter produces the start-of-frame pulse for each 52 bit frame (to accommodate the additional 4-bit code generated by the multiplex equipment) and the transfer of data frames is prevented by inhibiting the clock signal.

77. When data is to be sent, the multiplex equipment applies a positive voltage to each RFS line, in turn, for a period of 47 and one half clock periods after the start-of-frame pulse. Thus the start-of-frame pulse is produced for each 52-bit frame, and one 48-bit data frame plus the 4-bit code is transferred, in turn, from each MA.1090.

78. When new control data is generated at any of the MA.1090 control units, a request to send (RTS) signal is generated by that unit; this is routed to the multiplex equipment, and the RFS signal changes from a negative voltage to a positive voltage for that particular control unit out of sequence so that the new data is sent as quickly as possible. The logic '1' RTS signal at board pin 10 is produced when a '0' is applied to any of the input lines to NOR gate G31; when PRESERVE, THROUGH or EXTERNAL ENTRY is selected, the output from G29 changes to a '0', and the inverted new data signal at board pin AA is routed to G31 via D2 and R11. The remaining input to G31 is from the Q output of ML3a; the inverted new data input at board pin AA is reset during the transmission of the first of a pair of data frames, but since it is also applied to the D input of ML3a, the RTS output signal is maintained for the second frame of the pair.

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number	Manufacturer
		CONTROL PROCESSOR CARD PM681 (ST 77324)				
Resistors						
R1	68k	Metal Oxide		2	916478	Electrosil TR4
R2	2.7k	Metal Oxide		2	916548	Electrosil TR4
R3	5.6k	Metal Oxide		2	918128	Electrosil TR4
R4	68k	Metal Oxide		2	916478	Electrosil TR4
R5	2.7k	Metal Oxide		2	916548	Electrosil TR4
R6	12k	Metal Oxide		2	917952	Electrosil TR4
R7	12k	Metal Oxide		2	917952	Electrosil TR4
R8	22k	Metal Oxide		2	913493	Electrosil TR4
R9	1.8k	Metal Oxide		2	911148	Electrosil TR4
R10	12k	Metal Oxide		2	917952	Electrosil TR4
R11	12k	Metal Oxide		2	917952	Electrosil TR4
R12	12k	Metal Oxide		2	917952	Electrosil TR4
R13	68k	Metal Oxide		2	916478	Electrosil TR4
R14	68k	Metal Oxide		2	916478	Electrosil TR4
R15	120k	Metal Oxide		2	915373	Electrosil TR4
R16	5.6k	Metal Oxide		2	918128	Electrosil TR4
R17	22k	Metal Oxide		2	913493	Electrosil TR4
R18	27k	Metal Oxide		2	913494	Electrosil TR4
R19	68k	Metal Oxide		2	916478	Electrosil TR4
R20	22k	Metal Oxide		2	913493	Electrosil TR4
R21	12k	Metal Oxide		2	917952	Electrosil TR4
R22	12k	Metal Oxide		2	917952	Electrosil TR4
R23	68k	Metal Oxide		2	916478	Electrosil TR4
R24	12k	Metal Oxide		2	917952	Electrosil TR4
R25	22k	Metal Oxide		2	913493	Electrosil TR4
R26	22k	Metal Oxide		2	913493	Electrosil TR4
R27	22k	Metal Oxide		2	913493	Electrosil TR4
R28	68k	Metal Oxide		2	916478	Electrosil TR4
R29	22k	Metal Oxide		2	913493	Electrosil TR4
R30	12k	Metal Oxide		2	917952	Electrosil TR4

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number	Manufacturer
Resistors (Contd.)						
R31	12k	Metal Oxide		2	917952	Electrosil TR4
R32	68k	Metal Oxide		2	916478	Electrosil TR4
R33	12k	Metal Oxide		2	917952	Electrosil TR4
R34	12k	Metal Oxide		2	917952	Electrosil TR4
R35	22k	Metal Oxide		2	913493	Electrosil TR4
R36	22k	Metal Oxide		2	913493	Electrosil TR4
R37	22k	Metal Oxide		2	913493	Electrosil TR4
R38	12k	Metal Oxide		2	917952	Electrosil TR4
R39	12k	Metal Oxide		2	917952	Electrosil TR4
R40	12k	Metal Oxide		2	917952	Electrosil TR4
R41	12k	Metal Oxide		2	917952	Electrosil TR4
R42	12k	Metal Oxide		2	917952	Electrosil TR4
R43	12k	Metal Oxide		2	917952	Electrosil TR4
R44	12k	Metal Oxide		2	917952	Electrosil TR4
R45	12k	Metal Oxide		2	917952	Electrosil TR4
R46	180	Wirewound	2.5	5	913602	Welwyn W21
R47	180	Wirewound	2.5	5	913602	Welwyn W21
R48	12k	Metal Oxide		2	917952	Electrosil TR4
R49	12k	Metal Oxide		2	917952	Electrosil TR4
R50	22k	Metal Oxide		2	913493	Electrosil TR4
R51	470	Metal Oxide		2	910758	Electrosil TR4
R52	12k	Metal Oxide		2	917952	Electrosil TR4
R53	12k	Metal Oxide		2	917952	Electrosil TR4
Capacitors			V			
C1	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C2	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C3	6.8	Tantalum	35	20	910129	Union Carbide K6R8J35S

Cct. Ref.	Value	Description	Rat.	Tol %	Racal Part Number	Manufacturer
Capacitors (Contd.)			V			
C4	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C5	0.1	Polyester	100	20	914173	STC PMT2R0.1 M100
C6	100p	Silver Mica	400	2	920264	STC 454-62
C7	6.8	Tantalum	35	20	910129	Union Carbide K6R8J35S
C8	6.8	Tantalum	35	20	910129	Union Carbide K6R8J35S
C9	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C10	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C11	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C12	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C13	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C14	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C15	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C16	.0022	Disc Ceramic	500	25	917438	Erie 831/K7004
C17	.0022	Disc Ceramic	500	25	917438	Erie 831/K7004

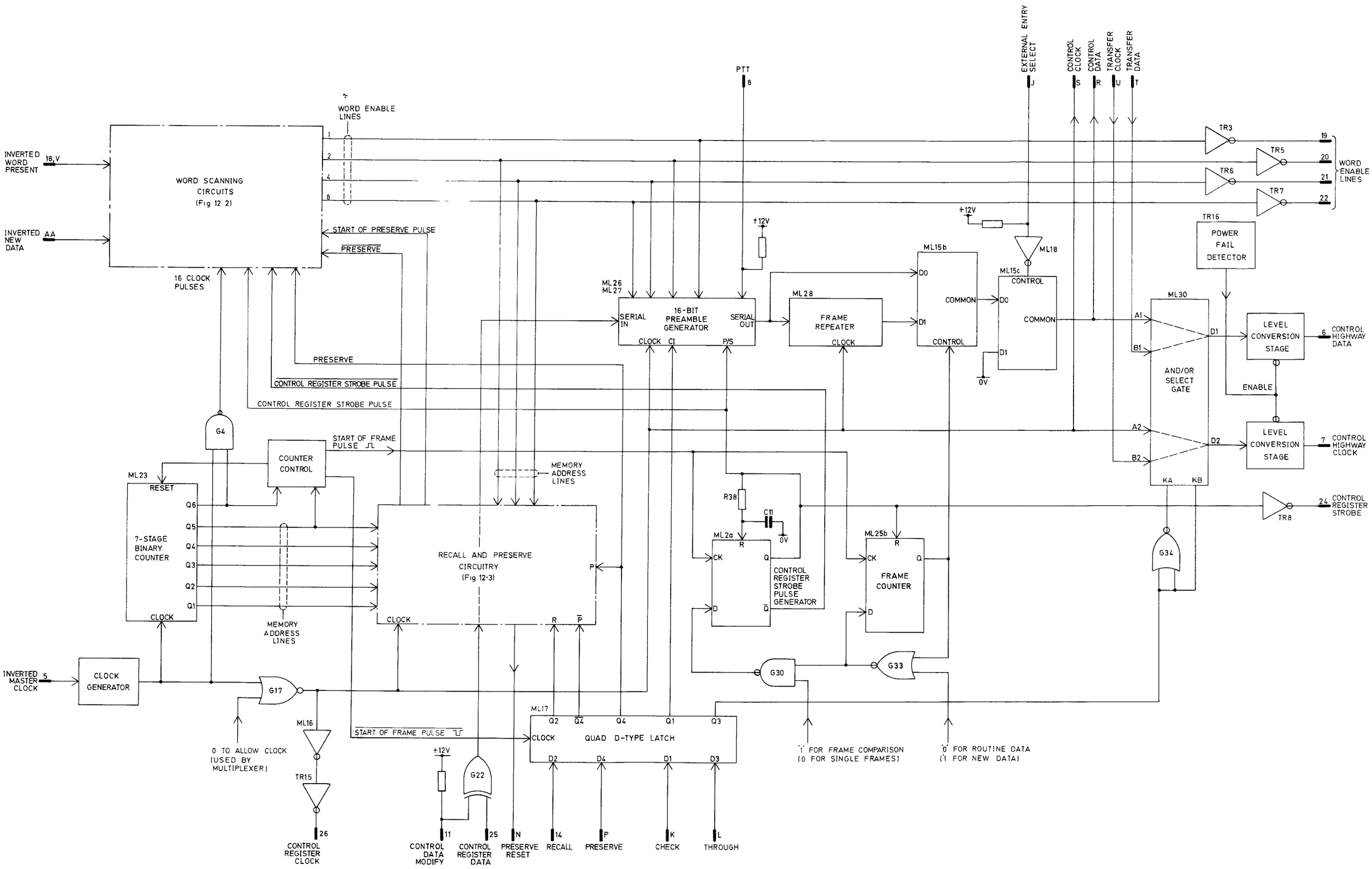
Diodes

D1	Silicon	914898	STC 1N4149
D2	Silicon	914898	STC 1N4149
D3	Silicon	914898	STC 1N4149
D4	Silicon	914898	STC 1N4149
D5	Silicon	914898	STC 1N4149

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number	Manufacturer
Diodes (Contd.)						
D6		Silicon			914898	STC 1N4149
D7		Silicon			914898	STC 1N4149
D8		Silicon			914898	STC 1N4149
D9		Silicon			914898	STC 1N4149
D10		Silicon			914898	STC 1N4149
D11		Silicon			914898	STC 1N4149
D12		Silicon			914898	STC 1N4149
D13		Zener, 10V, 400mW			917217	Mullard BZY88C10
Transistors						
TR1		PNP Silicon			915568	Mullard BCY70
TR2		NPN Silicon			914900	Mullard BC109
TR3		NPN Silicon			914900	Mullard BC109
TR4		NPN Silicon			914900	Mullard BC109
TR5		NPN Silicon			914900	Mullard BC109
TR6		NPN Silicon			914900	Mullard BC109
TR7		NPN Silicon			914900	Mullard BC109
TR8		NPN Silicon			914900	Mullard BC109
TR9		PNP Silicon			915568	Mullard BCY70
TR10		PNP Silicon			915568	Mullard BCY70
TR11		PNP Silicon			927707	ITT BC160-16
TR12		NPN Silicon			927706	ITT BC140-16
TR13		PNP Silicon			927707	ITT BC160-16
TR14		NPN Silicon			927706	ITT BC140-16
TR15		NPN Silicon			906842	Mullard 2N2369
TR16		NPN Silicon			914900	Mullard BC109

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number	Manufacturer
Integrated Circuits						
ML1		Quad 2-input NAND gate			930028	RCA CD4011BE
ML2		Dual D-type flip-flop			926860	RCA CD4013BE
ML3		Dual D-type flip-flop			926860	RCA CD4013BE
ML4		Quad 2-input NOR gate			930027	RCA CD4001BE
ML5		Triple 3-input NOR gate			930030	RCA CD4025BE
ML6		Triple 3-input NAND gate			930978	RCA CD4023BE
ML7		Dual D-type flip-flop			926860	RCA CD4013BE
ML8		Quad 2-input NOR gate			930027	RCA CD4001BE
ML9		Triple 3-input NOR gate			930030	RCA CD4025BE
ML10		Quad 2-input NOR gate			930027	RCA CD4001BE
ML11		Not used				
ML12		Binary Up/Down counter			929329	RCA CD4516BE
ML13		Binary Up/Down counter			929329	RCA CD4516BE
ML14		Quad 2-input NAND gate			930028	RCA CD4011BE
ML15		Analogue Multiplexer			930036	RCA CD4053BE
ML16		Hex inverting buffer			930033	RCA CD4049BE
ML17		Quad D-type latch			930861	RCA CD4042BE
ML18		Hex inverting buffer			930033	RCA CD4049BE
ML19		Mulitvibrator			930992	RCA CD4047BE
ML20		Quad exclusive OR gate			930856	RCA CD4070BE

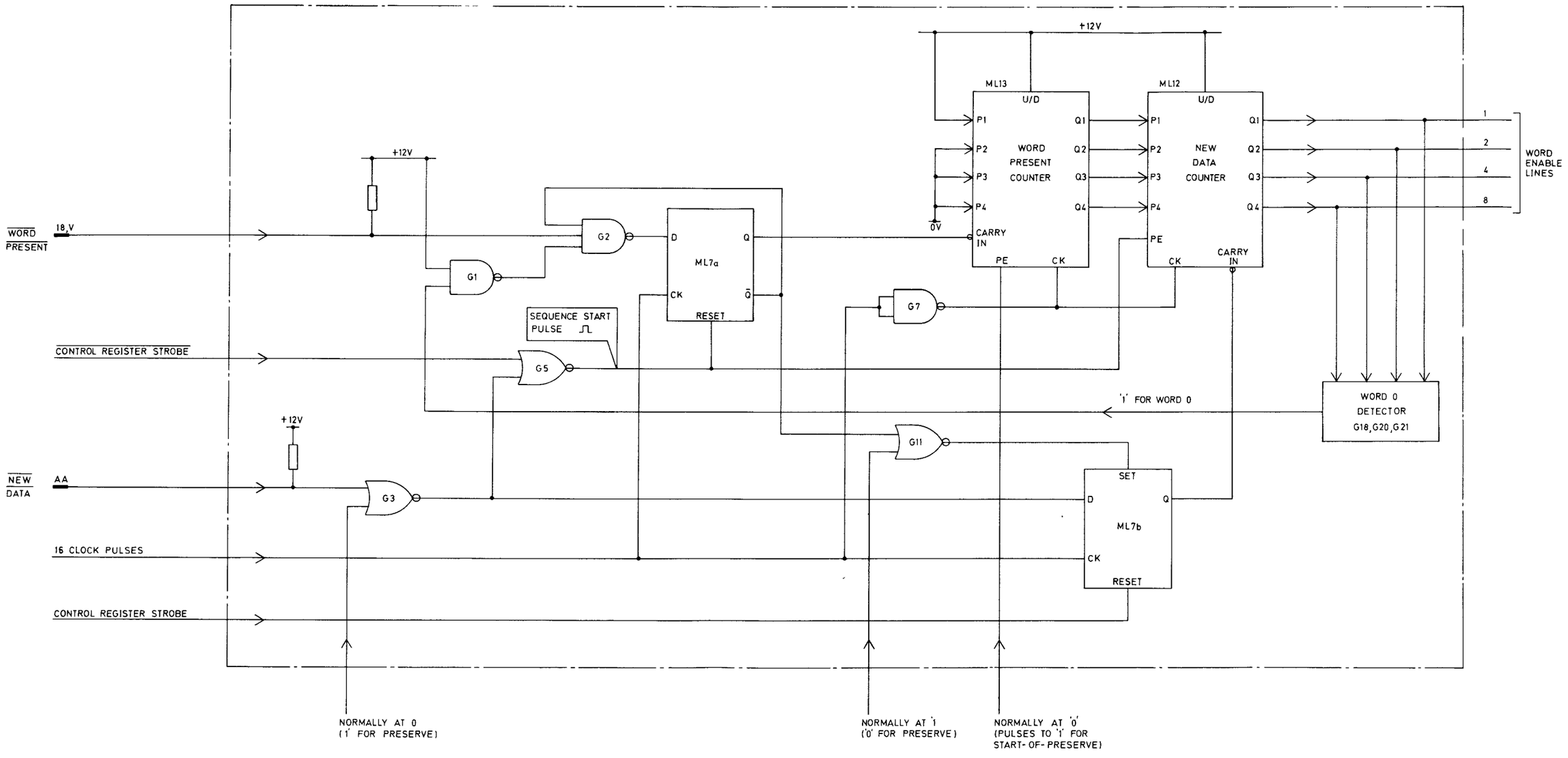
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number	Manufacturer
Integrated Circuits (Contd.)						
ML21		Dual D-type flip-flop			926860	RCA CD4013 BE
ML22		Random access memory			927799	Fairchild 34720
ML23		7-stage binary counter			930979	RCA CD4024 BE
ML24		Quad 2-input NOR gate			930027	RCA CD4001 BE
ML25		Dual D-type flip-flop			926860	RCA CD4013 BE
ML26		8-stage shift register			930977	RCA CD4021 BE
ML27		8-stage shift register			930977	RCA CD4021 BE
ML28		Variable length shift register			927076	Motorola MC14557
ML29		Dual binary to 1-to-4 inverter			929333	RCA CD4556 BE
ML30		Quad AND/OR select gate			930976	RCA CD4019 BE
Miscellaneous						
		14-pin DIL IC socket			927053	Texas C83-14-02
		16-pin DIL IC socket			927054	Texas C83-16-02



RACAL
WOH8307

Simplified Block Diagram Control Processor Card

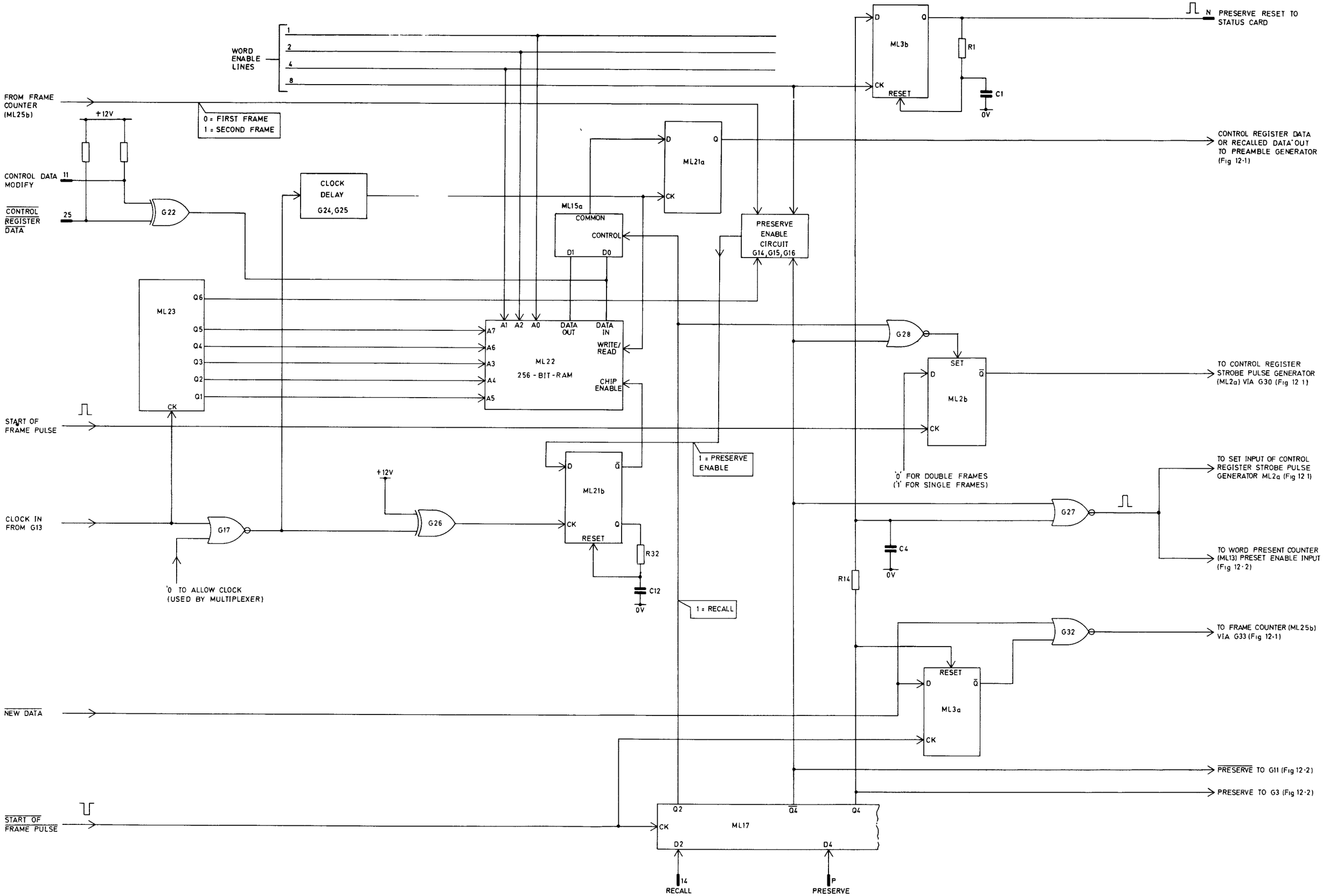
Fig.12·1



RACAL
WOH8307

Simplified Block Diagram Word Scanning Circuits

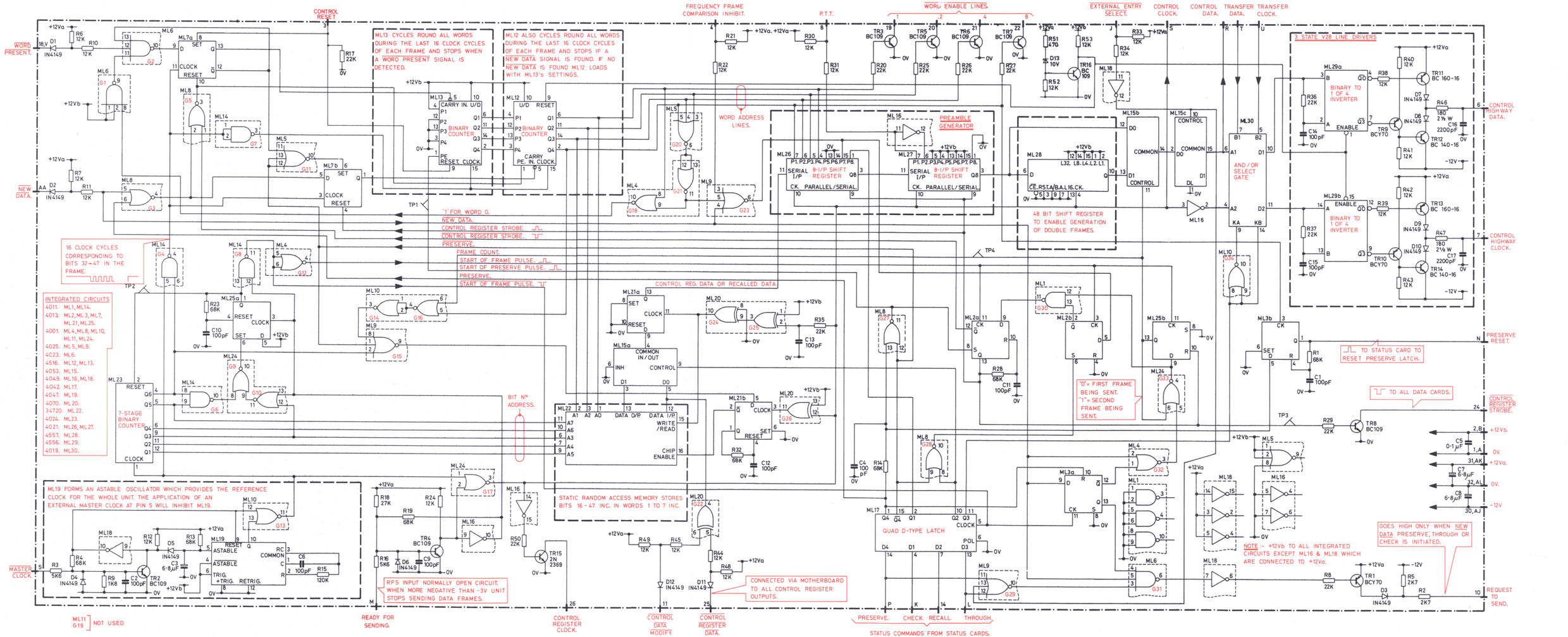
Fig. 12·2



RACAL
WOH8307

Simplified Diagram Recall & Preserve Circuitry

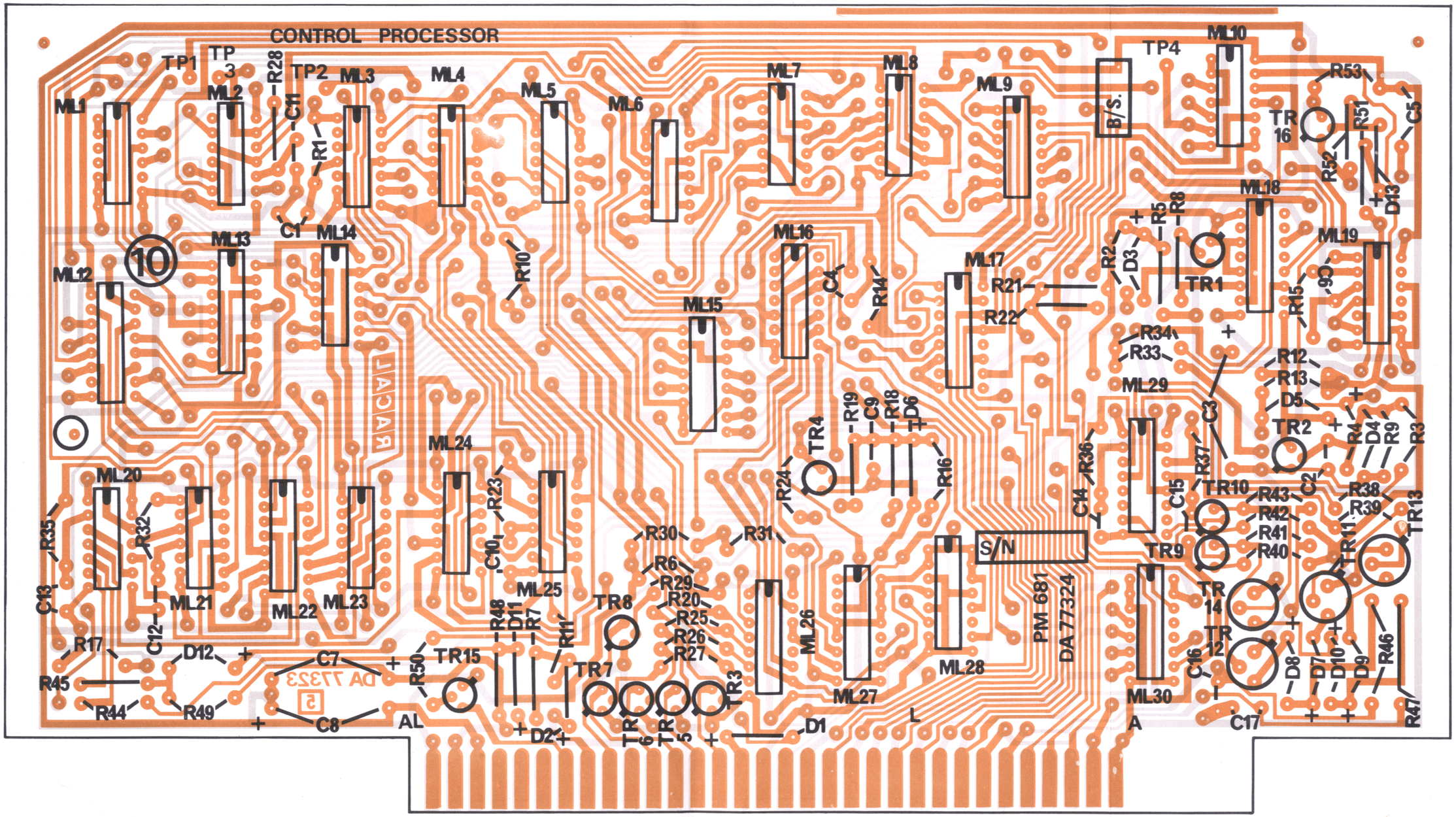
Fig.12-3



RACAL

WOH8307	DC77324	12·4		WOH8307	DC77324	12·4	
6		1/2		6		2/2	

Circuit :
Control Processor Card Fig.12·4



RACAL			
WOH8307	DA77324	12·5	
5		1/3	

WOH8307	DA77324	12·5	
5		2/3	

Layout :
Control Processor Card

Fig. 12·5

CHAPTER 13

STATUS CARD

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CHAPTER 13

STATUS CARD

INTRODUCTION

1. The status card contains the word 9 computer highway data and clock circuitry, together with the exchange and transfer data and clock routing circuits. It also carries the circuitry for the front panel STATUS switches (OUT, RECALL, CHECK and IN).

FUNCTIONAL DESCRIPTION

2. The following functional description paragraphs should be read in conjunction with the block diagram of the status card given in fig. 13.1. The circuit diagram is given in fig. 13.2.

COMPUTER PRESENT

3. When the MA.1090 is used with a computer, an earth connection is made to pin 7 of PL1 on the rear panel; this is routed to a quad AND/OR select gate, ML9, via board pin 9, and is inverted by G1 to apply a '1' to the KA input. This enables the A1 to A4 inputs, connecting them to the D1 to D4 outputs respectively. Conversely, when a computer is not connected, the KB input is at logic '1' and the B inputs are connected to the respective D outputs.

WORD 9 INPUT SHIFT REGISTER

4. The computer highway data and clock signals, at board pins 4 and 5, are applied to the input shift register, ML14, ML4, via line receivers (ML28) and low-to-high level (5V to 12V) translators ML18. After the application of 16 clock pulses, the first eight bits of the preamble (bits 0 to 7) are located in ML4, and the remaining eight bits (8 to 15) are located in ML14. If the sync. code and word 9 detector is presented with the correctly coded data, the detector output signal is applied to the control inhibit latch ML16b; if the control inhibit bit of the preamble (bit 9) is set to a '1' by the computer, the output signal from the control inhibit latch is set and inhibits the strobing of the status latches.

5. The sync. code and word 9 detector output signal also enables a 16/32 period counter, ML11, G21, such that a '1' output is produced for 16 clock periods which is applied as a parallel input enable pulse to the 8-stage shift register ML3; the next 16 bits of the word 9 data, i.e. bits 16 to 31, are now positioned in the input shift register ML14, ML4, and the BCD outputs from the two address switches, SA and SB, are loaded into the 8-stage shift register ML3.

ADDRESS COMPARISON DETECTOR

6. Since the data bits 32 to 47 of word 9 are a repeat of bits 16 to 31, the next eight bits from the computer contain the 8-bit address; this data is clocked into the 8-stage shift register, ML14, and is also applied to the exclusive OR gate G17 where it is compared with the MA.1090 address output from ML3. If the two sets of address data are the same, the computer is addressing the correct MA.1090 control unit; if the two sets of address data are not the same, the output from G17 changes to a '1' and the status load pulse generator is inhibited via the error latch.

7. At the end of the address comparison, ML3 contains data bits 24 to 31 of word 9 (from ML14); this data is then compared (by G17) with bits 40 to 47 of the word 9 data from the computer.

FRAME COMPARISON DETECTOR

8. The frame comparison, which takes place at the same time as the address comparison, is performed by the exclusive OR gate G23; it compares data bits 16 to 31 from the input shift register, ML14, ML4, with data bits 32 to 47 of the word 9 data from the computer. If the two sets of data do not compare, the output from G23 changes to a '1' which inhibits the generation of the status load pulse via the error latch.

WORD 9 OUTPUT SHIFT REGISTER

9. The word 9 output shift register comprises four 8-stage shift registers, ML6, ML2, ML1 and ML10; ML10 and ML1 generate the 16-bit preamble, whilst ML2 and ML6 contain the 16 bits of word 9 data which are repeated by feeding the serial output from ML2 back to the serial input of ML6.

10. The end of a successful address and frame comparison codincides with the count-of-32 output from the 16/32 period counter, ML11, G21; this enables the status load pulse generator and the output is applied as a parallel input enable pulse to the output shift register stages. The data at the parallel inputs is loaded into the register and is then serially clocked out, by the control clock signal at board pin U, to the computer via ML19, the level conversion circuits and the exchange highway (para. 11).

11. The status load pulse also enables a 48-period counter, ML23; the output from the counter goes to a '1' for 48 clock periods to enable the two level-conversion stages via G24; it is also applied to the B input (binary 2) of the dual 4-way data selector ML19 to enable the channel 2 input. The word 9 data from the output shift register is returned to the computer, together with the control clock signal, via the level conversion stages and the exchange highways.

MONITOR

12. If the MONITOR bit (bit 31, and repeated as bit 47) is set to a '1' by the computer, the revertive data and clock signals, at board pins N and P, are routed to the computer via the exchange highway after the word 9 data has been returned. The MONITOR bit output from the status latches is applied to NOR gate G24 to enable the level conversion stages; once the return of the word 9 data to the computer has been completed, the A and B inputs to the data selector ML19 are both at '0', the channel 0 input is enabled and the revertive data and clock signals are routed to the computer.

COMPUTER OUT STATUS

13. The computer may select the OUT status, via bit 30 (repeated as bit 46) of the word 9 data, so that the control data from the MA.1090 may be examined by the computer.

14. The logic '1' OUT signal from the status latches illuminates the OUT push-button lamp via driver stage TR1 and board pin K; it is also applied to NOR gate G24 and to the A input (binary 1) of the dual 4-way data selector such, that following the return of the word 9 data to the computer, the control data and clock signals at board pins T and U are routed via ML19 (channel 1 input) and the enabled level conversion stages to the exchange highways. Thus when OUT is selected, the control data and clock signals are routed via the exchange highway to the computer.

STATUS INHIBIT

15. The STATUS INHIBIT bit of the word 9 data (bit 29, repeated as bit 45) is set to a '1' by the computer to disable the front panel CHECK and RECALL switches via the status latches. The IN and OUT status switches on the front panel are similarly disabled by the computer present signal (para.28).

COMPUTER PRESERVE SELECT

16. The PRESERVE bit (bit 28, repeated as bit 44) is set to a '1' to preserve in the recall store the front panel settings. This could be done, for example, to preserve the front panel settings for subsequent recall by the MA.1090 operator, following a channel change effected by a computer-assisted channel storage system.

17. The PRESERVE output signal from the status latches is applied via board pin 15 to the control processor card; the front panel control settings are preserved in the recall store (on the control processor card - Chap. 12) and a reset signal is then produced which is applied to the preserve latch via board pin 14 on the status card.

COMPUTER CHECK STATUS

18. When bit 27 (repeated as bit 43) is set to a '1', the front panel controls are disabled by the removal of the front panel controls enable signal at board pin S. The CHECK output signal from the status latches illuminates the front panel CHECK push-button, and is also applied via board pin 12 to:-

(1) The control processor card to set the control inhibit bit of the preamble (bit 9) to a '1' and so inhibit the control of the associated transmitter.

(2) The display processor card to allow the entry of the revertive highway data from the transmitter for subsequent display on the MA.1090 front panel.

19. Thus when the CHECK status is selected by the computer, the front panel controls are disabled, the transmitter is interrogated and the control settings are returned via the revertive data to illuminate the front panel controls. If the MONITOR bit is also set, the revertive data from the transmitter is also routed to the computer (after the return of the word 9 data) via the exchange highway (para. 12). The PRESERVE bit may also be set in conjunction with the CHECK status to preserve the front panel settings for subsequent recall by the MA.1090 operator (para. 16).

COMPUTER THROUGH SELECT

20. Data bit 26 (repeated as bit 42) is set to '1' to route the transmitter control data produced by the computer to the transmitter through the MA.1090 (via the control highway) without being displayed on the MA.1090. Since the computer data is not routed via the frame repeater on the control processor card (Chap. 12) the data sequence must contain double frames. The THROUGH bit may be set in conjunction with the IN status (para. 23) in which case the computer data will also be displayed by the MA.1090.

21. The THROUGH output signal from the status latches is applied to the control processor card via the AND/OR select gate ML9 (A3 to D3) and board pin 13; the computer data and clock signals, at board pins 4 and 5, are then routed, via line receivers ML28, low-to-high voltage translators ML18, AND/OR select gate ML9 (A1 to D1 and A2 to D2) and board pins 16 and 17, to the control highways via the control processor card.

DISPLAY INHIBIT

22. The DISPLAY INHIBIT bit of the word 9 data from the computer (bit 25, repeated as bit 4) is set to a '1' to prevent the revertive data from a transmitter under interrogation by the computer being displayed on the MA.1090, which may be controlling a different transmitter. The DISPLAY INHIBIT output signal from the status latches is applied to the display processor card (Chap. 14) via board pin M, where it inhibits the display output shift register.

COMPUTER IN STATUS

23. The computer may set a particular MA.1090 to the IN status (via the word 9 data) to allow the computer data to be accepted and displayed, and then routed to the transmitter via the control highway. The front panel controls are disabled by the removal of the front panel controls enable signal at board pin S, and the IN push-button lamp is illuminated via lamp driver TR3 and board pin H.

24. The IN signal from the status latches is also applied to the display processor card (Chap. 14) via board pin R to allow the entry of the transfer data and clock signals from the status card at board pins 16 and 17 (para. 25).

25. The computer present input, at board pin 9, enables the A inputs applied to the AND/OR select gate ML9; the computer highway data and clock signals, at board pins 4 and 5, are routed to the display processor card via line receivers ML28, low-to-high level translators ML18, the AND/OR select gate ML9 (A1 to D1 and A2 to B2), and board pins 16 and 17. Thus the computer data is displayed on the MA.1090 and is eventually routed to the transmitter via the control highway.

26. As mentioned in para. 20. the THROUGH bit of the word 9 data may also be set; the transfer data is then routed immediately through the MA.1090 to the transmitter via the control processor card and the control highway, and is also displayed on the MA.1090 via the display processor card.

27. The PRESERVE function may be selected in conjunction with the IN status to preserve the front panel settings for subsequent recall by the MA.1090 operator.

FRONT PANEL STATUS SWITCHES

28. The four status switches on the front panel (OUT, IN, RECALL and CHECK) are connected to board pins J, F, C and D respectively. The OUT, RECALL and CHECK switches are connected directly to a switch encoder circuit (ML21, ML26, ML27), whilst the IN switch is connected to the B4 input of the AND/OR select gate ML9, and is only connected to the switch encoder (B4 to D4) when a computer is not connected. When a computer is connected, the output from the IN switch is disabled (B4 input of ML9 disconnected from the D4 output) and the earth at board pin 9 is applied to the status latches to inhibit the front panel IN and OUT switches (this prevents interference by the MA.1090 Operator).

29. The external set check input, at board pin 10, is routed from PL2 pin 25 on the rear panel and is set to 0V (earth) by, for example, multi-address equipment, to set the MA.1090 to CHECK.

SWITCH ENCODER

30. This circuit uses a priority encoder where the status priorities are as given in Table 1. These priorities are used to set the required status latches and do not effect status switch selection, unless two switches are pressed simultaneously, when that with the higher priority overrides the other.

31. The status latches are reset following a power failure by the output from the power fail detector (para. 43). When a computer is connected, the encoder (and hence the front panel switches CHECK and RECALL) may be inhibited via the status inhibit (SI) bit output from the word 9 data (para. 15). The IN and OUT switches are also inhibited when the computer present input is made (para. 28).

32. Table 1 also shows the functions selected by each status switch; these are described in the following paragraphs under the appropriate status heading.

TABLE 1: STATUS PRIORITIES

PRIORITY NUMBER	STATUS	FUNCTIONS			
		PRESERVE	FRONT PANEL CONTROLS ENABLES	EXCHANGE BUSY	THROUGH
1	OUT		ON	ON	
4	IN	SET	OFF	OFF	SET
5	RECALL	SET	ON	OFF	
6	CHECK	SET	OFF	OFF	
7	EXTERNAL SET CHECK	SET	OFF	OFF	

NOTES: 1. Priorities 0, 2 and 3 not used.

2. Highest number present dictates priority.

FRONT PANEL OUT STATUS

33. When OUT is selected at the front panel, the logic '0' exchange busy signal from the status latches is routed to pin 9 of PL1 on the rear panel (via board pin 8); this is connected in parallel to each control unit in a multi-operator installation and prevents a second operator selecting the OUT status.

34. The logic '1' OUT signal from the status latches illuminates the OUT push-button via driver stage TR1 and board pin K; it is also applied to NOR gate G24 and to the A input (binary 1) of a dual 4-way data selector ML19; the resulting logic '0' output from G24 enables the two level conversion stages, whilst the '1' input to ML19 routes the control data and clock signals (channel 1 input), at board pins T and U, to the exchange data and clock highways via ML19, level conversion stages and board pins 6 and 7.

35. Thus when OUT is selected, the control data and clock signals are routed via the exchange highways to a number of additional control units which will accept the data when set to IN.

FRONT PANEL IN STATUS

36. The output signal from the front panel IN switch is applied via the AND/OR select gate ML9 (B4 to D4) and the switch encoder to the status latches. This disables the front panel controls by removing the front panel controls enable signal (at board pin S), and also produces the PRESERVE signal; this is routed to the control processor card, via board pin 15, and the front panel control settings are preserved in the recall store (Chap. 12). The preserve latch is then reset by the input signal at board pin 14.

37. The IN signal from the status latches is applied to:-

(1) The IN push-button lamp via the lamp driver stage TR3 and board pin H.

(2) The display processor card via board pin R to allow the entry of the transfer data.

(3) The control processor card via ML9 (B3 to D3) and board pin 13 (as the THROUGH signal) to allow the entry of the transfer data.

38. The exchange data and clock signals, at board pins 6 and 7 respectively, are routed to the display processor and control processor cards, via line receivers ML28, low-to-high voltage translators ML18, the AND/OR select gate ML9 (B1 to D1 and B2 to D2), and board pins 16 and 17. The control data from another MA.1090 (set to OUT) is thus routed via the control processor card and the control highway to the transmitter, and is displayed on the MA.1090 via the display processor card.

RECALL STATUS

39. The RECALL status may only be selected at the front panel; the output from the RECALL switch, at board pin C, is applied to the status latches via the switch encoder, and the resulting PRESERVE and RECALL output signals are applied to the control processor card via board pins 15 and N respectively. The previously stored control settings are recovered from the recall store and are replaced with the existing front panel settings; the preserve and recall status latches are then reset by the preserve reset input at board pin 14.

FRONT PANEL CHECK STATUS

40. When the CHECK status is selected at the front panel, the front panel controls are disabled by the removal of the front panel controls enable signal at board pin S, and the existing front panel settings are preserved in the recall store (PRESERVE output at board pin 15). The CHECK push-button lamp is illuminated via lamp driver stage TR4 and board pin E, and the logic '1' check output signal at board pin 12 is applied to:-

(1) The control processor card to set the CONTROL INHIBIT bit of the preamble (bit 8) to a '1' and so inhibit the control of the associated transmitter.

(2) The display processor card to allow the entry of the revertive highway data from the transmitter for subsequent display on the MA.1090 front panel.

41. Thus when the CHECK status is selected at the front panel, the controls are disabled and the settings are preserved in the recall store. The transmitter is interrogated and the control settings are returned via the revertive data to illuminate the front panel controls.

EXTERNAL SET CHECK

42. The MA.1090 may be set to the CHECK status (as described above) by the application of a 0V (earth) signal to PL2 pin 25 on the rear panel. This facility is used, for example, by an address selection unit where a single MA.1090 control unit is used to control a number of transmitters. The MA.1090 is set to the CHECK status, the control settings of the addressed transmitter are displayed, and the previous control settings are preserved for subsequent recall by the MA.1090 operator.

POWER FAIL DETECTOR

43. The power fail detector TR12, which is powered from the +12 Vb battery supply, monitors the +12 Va output from the power supply module. If the level of the +12 Va supply falls below approximately 10 volts a reset signal is produced which is applied to the various non-essential circuits to limit the drain from the battery supply.

CIRCUIT DESCRIPTION

44. The circuit diagram for the status card is given in fig. 13.1, whilst the card layout is given in fig. 13.2.

WORD 9 INPUT SHIFT REGISTER

45. The computer highway data and clock signals, at board pins 4 and 5, are applied to the word 9 input shift register ML14, ML4, via line receivers ML28 (2A and 1A inputs to 2Y and 1Y outputs) and +5V to +12V converters ML18 (11 and 10 inputs to Z1 and Z0 outputs).

46. ML14 and ML4 are dual 4-stage static shift registers, which are cascaded to form a 16-stage shift register (the serial output from ML14 is taken from pin 10 and is applied to the data A input of ML4). The logic level present at the data input is transferred into the first register stage, and shifted over one stage, at each positive-going clock transition.

SYNC. CODE AND WORD 9 DETECTOR

47. The sync. code and word 9 detector consists of an 8-input NAND gate G19 and an 8-input NOR gate G18. When the first 16 bits of the word 9 data from the computer has been clocked into the input shift register, the 16 bits of the preamble (bits 0 to 15) are present at the parallel outputs. A logic '1' is produced at the output of G18 at the negative-going edge of the sixteenth clock pulse if:-

(1) Data bits 0 to 5, at the Q4B, Q3B, Q2B, Q1B, Q4A and Q3A outputs of ML4, constitute a correct sync. code (0 followed by five ones).

(2) The transmit/receive bits (bits 6 and 7) at the Q2A and Q1A outputs of ML4 are both at logic '0'.

(3) The address security bits (bits 10 and 11), at ML14 pins 4 and 5, are set to '1' and '0' respectively.

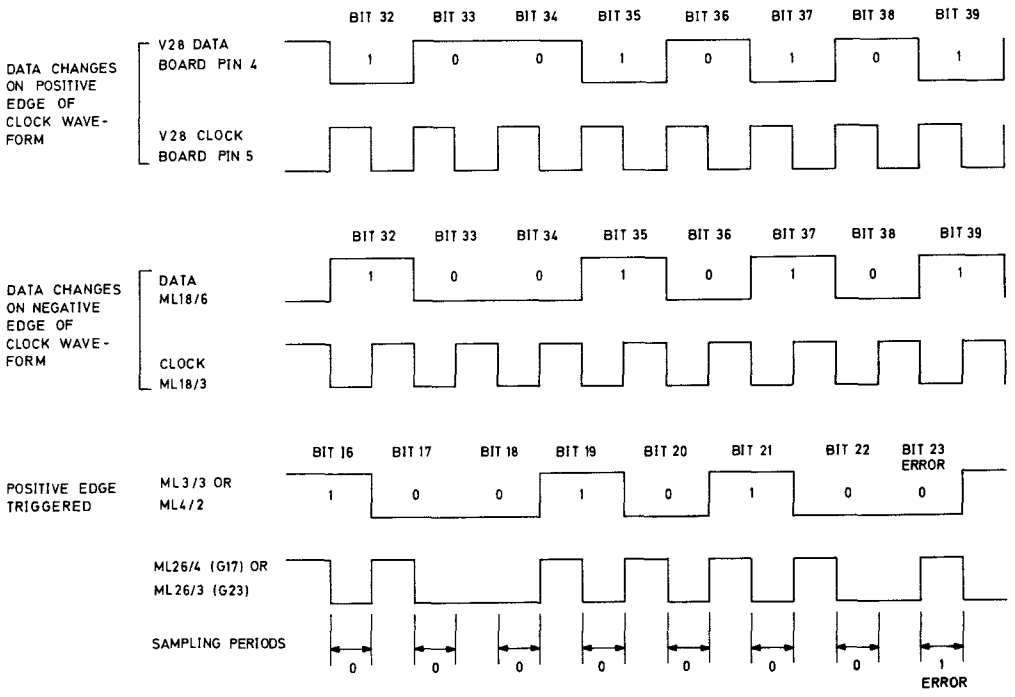
(4) The 4-bit data word identification code (bits 12 to 15) at ML14 pins 2, 11, 12 and 13 are set to BCD 9 (1011).

CONTROL INHIBIT

48. During the time that the preamble is located in the 16-stage input shift register, the CONTROL INHIBIT bit of the preamble (bit 8) is present at ML14 pin 10, and is applied to the D input of flip-flop ML16b. If this bit is set to a '1' when the '1' output is produced from the sync. code and word 9 detector, the $\overline{Q}$ output from ML16b changes to a '0'; this is applied to AND gate G16 to inhibit the strobe pulse which loads the status latches (para.67.

ADDRESS COMPARISON DETECTOR

49. The logic '1' output signal from the sync. code and word 9 detector is applied to the reset inputs of a dual binary up-counter ML11. This resets the Q outputs to '0' and the resulting '1' output from NOR gate G21 holds the error latch ML22a in the reset condition; it is also applied as a parallel input enable signal to the 8-stage shift register ML3, and the address number (00 to 99) set on the two BCD switches, SA and SB, is loaded in.



RACAL Timing Diagram : Data & Clock Signals Fig.13(i)

50. The computer highway clock signal is applied to the enable input of ML11b, which will count up at each negative-going transition of the clock waveform, provided the clock input terminal (pin 9) is maintained at logic '0'. After a count of 16, the Q4 output at ML11b pin 14 changes from a '1' to a '0'; this clocks ML11a via the enable input and the Q1 output, at ML11a pin 3, also changes to a '1'. The resulting '0' output from G21 removes the reset from the error latch ML22b, and is also applied as a serial input enable signal to the 8-stage shift register ML3.

51. The first 16 data bits of word 9 following the preamble, i.e. data bits 16 to 31, are now positioned in the input shift register ML14, ML4. The next 8 bits of the word 9 data from the computer (32 to 39) contain the address, and these are applied to the exclusive OR gate G17 where they are compared sequentially with the address switch data contained in the 8-stage register ML3. If during the sampling periods- fig. 13 (i), the two sets of address data are the same, the output of G17 is maintained at logic '0' and signifies that the computer is addressing the correct MA.1090 control unit; if the two sets of address data do not compare, the output from G17 changes to a '1' and is applied to the error latch ML22b via G22 (para. 54).

52. At the completion of the address comparison, data bits 24 to 31 of the word 9 data are contained in ML3; these are now compared (by G17) sequentially with data bits 40 to 47 from the computer.

FRAME COMPARISON DETECTOR

53. The frame comparison takes place at the same time as the address comparison. Data bits 32 to 47 from the computer are compared sequentially with data bits 16 to 31 from the input shift register by the exclusive OR gate G23. If during the sampling periods - fig. 13 (i), the two sets of word 9 data are the same, the output of G23 remains at logic '0'; if the two sets of data do not compare, the output of G23 changes to a '1' and this is applied to the error latch ML22b via G22 (para. 54).

ERROR LATCH

54. The error latch consists of a D-type flip-flop ML22b; it is held in the reset condition for 16 clock periods by the output from G21 (para. 48) and thus at the start of the address and frame comparisons, the Q output is at logic '0' and the $\overline{Q}$ output is at logic '1'. If a bit error is detected by either the address comparator or the frame comparator, the data input to ML22b changes to a '1'; this is transferred to the Q output at the next positive-going transition of the clock input and the error is latched by the logic '1' Q output (which maintains a '1' at the data input via G22).

STATUS LOAD PULSE

55. At the completion of the address and frame comparisons, the binary up-counter ML11 has reached a count of 32. The Q1 output from ML11a changes to a '0' whilst the Q2 output changes to a '1'; the time constant presented by R28 and C7 however, maintains the '1' input at G21 pin 8 for approximately 2 μs to ensure that the error latch ML22b is not prematurely reset. The logic '1' output from ML11a pin 4 is applied to the clock input of D-type flip-flop ML22a, and the level at the data input is transferred to the Q output. Provided no errors were detected by the address and frame comparators, the data input to ML22a is at logic '1' and the nominal 5 μs status load pulse is produced at TP2 (ML22a is reset via time constant components R27, C6).

56. The status load pulse is applied to the status latches to load in the status information from the word 9 data (para. 67) and is also applied as a parallel input enable pulse to the word 9 output shift register (para. 58).

WORD 9 OUTPUT SHIFT REGISTER

57. The word 9 output shift register comprises four 8-stage shift registers ML6, ML2, ML1 and ML10. These devices are parallel or serial input/serial output registers. When the parallel/serial control input is at logic '0', data is serially shifted into the 8-stage register synchronously with the positive-going transition of the applied clock waveform; when the parallel/serial control input is at logic '1', the data at the parallel input lines is loaded into the 8-stage register independently of the applied clock waveform.

58. The status load pulse, which is applied as a parallel entry enable pulse to each of the four register stages, loads into ML10 and ML1 the 16 bits of the preamble set at the parallel inputs; the address number set by the two BCD switches, SA and SB, is loaded into ML2, and the status information from the status latches is loaded into ML6. The 16 bits of the data word are repeated by applying the serial output from ML2 back to the serial input of ML6.

59. The status load pulse is also applied to the reset inputs of a dual binary up-counter; ML23; this sets the Q outputs to '0' and the resulting '1' output from G20 enables ML23b and the two level-conversion stages (para. 59) via G24. The '1' output from G20 is also applied to the B input of a dual 4-way data selector ML19; the binary number, i.e. 0, 1, 2 or 3, applied to the A and B inputs enables the correspondingly numbered input channel which is routed to the output at pins 7 and 9. Thus a '1' at the B input enables the channel 2 input and the word 9 data is clocked out of the register, together with the control clock signal at board pin U, via ML19, the two level-conversion output stages (enabled via G24) and board pins 6 and 7, to the computer via the exchange highways.

60. If the OUT bit of the output shift register data is set to a '1' (para. 69), the '1' output from G20 together with the '1' output from ML6 pin 6, which are applied to the A and B inputs of ML19, enable the channel 3 input; since; however, the channel 2 and channel 3 inputs are connected in parallel, this still results in the return of the word 9 data to the computer.

LEVEL CONVERSION OUTPUT STAGES

61. The data output signal from ML19 pin 9 is applied to the A and B inputs of a binary 1-of-4 decoder, ML20a, which drives the output transistors TR8, or TR9 via an inverter TR6. The stage converts the C-MOS logic level input signal, i.e. +12V for logic '1' and 0V for logic '0', into CCITT V28 signal levels, i.e. -12V for logic '1' and +12V for logic '0', before application to the exchange highway.

62. ML20a is enabled by the logic '0' output from G24. When the enable signal is not present, the $\overline{Q0}$ and $\overline{Q3}$ outputs are forced to logic '1' and the two PNP transistors TR6 and TR8 are held off.

63. The truth table for ML20a is given in Table 2. A logic '1' at the A and B inputs results in a '1' at the $\overline{Q0}$ output and a '0' at the $\overline{Q3}$ output; TR8 is held off whilst TR6 conducts and turns on TR9 to produce a -12V output at board pin 6 via D6 and R38. A '0' at the A and B inputs results in a '0' at the $\overline{Q0}$ output and a '1' at the $\overline{Q3}$ output; this time TR6 is held off and TR8 is turned on to produce a +12V output at board pin 6 via D5 and R38.

64. Resistor R30 and capacitor C9 provide a short time constant to allow one transistor to switch off before the other is driven on; this prevents the simultaneous conduction of both TR8 and TR9.

65. The level conversion stage for the clock output signal, from ML19 pin 7, is similar to that described above except that no inversion takes place ($\overline{Q0}$ and $\overline{Q3}$ connection reversed). Thus a positive-going transition at the output of ML19 results in a positive-going transition in the output signal at board pin 7.

TABLE 2: BINARY TO 1-OF-4 DECODER

INPUTS			OUTPUTS			
$\overline{E}$	B	A	$\overline{Q3}$	$\overline{Q2}$	$\overline{Q1}$	$\overline{Q0}$
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

X = don't care

COMPUTER PRESENT INPUT

66. As stated in para. 3, an earth is applied to board pin 9 when a computer is connected to the system; this results in a '0' at the KB input, and a '1' (via G1) at the KA input, of the quad AND/OR select gate ML9. The A input signals (A1 to A4) are then routed to the corresponding D outputs (D1 to D4). The earth signal also inhibits the front panel selection of the IN and the OUT status via AND gate G2.

STATUS LATCHES

67. The word 9 data status bits from the input shift register stage ML14 are loaded into the status latches by the status load pulse output at TP2 which is applied via G16 and G14; this opens AND gates G3, G5, G9 and G12 for the IN, OUT, CHECK and PRESERVE bits respectively, resets the IN, OUT and CHECK latches ML8a, ML8b and ML17a respectively, and is applied to the clock input of a quad D-type latch ML5 for the MONITOR, STATUS INHIBIT, THROUGH and DISPLAY INHIBIT status bits.

MONITOR

68. The MONITOR bit output, at ML14 pin 13, is applied via latch ML5 (pin 14 to pin 1) to the output shift register ML6, and also to NOR gate G24; this enables the level conversion output stages, and, once the word 9 data has been returned to the computer, the binary 0 input at the A and B inputs of ML19 enables the channel 0 input. The revertive data and clock signals, at board pins N and P respectively, are then routed to the computer via ML19, the level conversion output stages and the exchange highways.

COMPUTER OUT STATUS

69. The OUT bit, at ML14 pin 12, is applied via G5 to the set input of the OUT latch, J-K flip-flop ML8b; this sets the Q output to a '1' and this is applied to:-

(1) TR2 via R12 which produces the logic '0' exchange busy signal output at board pin 8.

(2) The open-collector lamp driver transistor TR1 which illuminates the OUT push-button on the front panel via board pin K.

(3) The word 9 output shift register stage ML6.

(4) NOR gate G24 to enable the two level conversion output stages.

(5) The A input (binary 1) of the data selector ML19 to enable the channel 1 input.

70. Once the word 9 output shift register data has been returned to the computer (para. 59), the control highway data and clock signals at board pins T and U are routed via ML19 (channel 1 input) and the enabled level conversion stages to the exchange highways.

STATUS INHIBIT

71. The STATUS INHIBIT bit output from the word 9 input shift register (ML14 pin 11) is routed via latch ML5 (pin 13 to pin 11) to the output shift register stage ML6. The inverse of the STATUS INHIBIT output from ML5, i.e. the 0V output at ML5 pin 12, is routed as a disable signal to the priority encoder ML27 which forms part of the status switch

encoder circuit (para. 81). Thus the STATUS INHIBIT bit prevents the front panel selection of the CHECK status and the RECALL status (the selection of the IN status and the OUT status at the front panel is prevented by the computer present connection at board pin 9 - para. 66).

COMPUTER PRESERVE SELECT

72. A logic '1' PRESERVE bit, at ML14 pin 2, is applied via AND gate G12 and OR gate G11 to the set input of the preserve latch ML17b; the Q output changes to a '1' and this is applied to:-

(1) The control processor and display processor cards via board pin 15.

(2) The word 9 output shift register stage ML6.

73. Once the preserve function has been accomplished a preserve reset signal is generated (on the control processor card) which is applied to the preserve latch via board pin 14.

COMPUTER CHECK STATUS

74. The CHECK bit output from ML14 is applied to the set input of the check latch ML17a via AND gate G9. The Q output changes to a '1', and this is applied to the output shift register stage ML6, and illuminates the CHECK push-button lamp via TR4 and board pin E; it is also applied via board pin 12 to:-

(1) The control processor card to set the CONTROL INHIBIT bit of the preamble (bit 8) to a '1' and so inhibit the control of the associated transmitter.

(2) The display processor card to allow the entry of the revertive highway data from the transmitter for subsequent display on the MA.1090 front panel.

75. The $\overline{Q}$ output from ML17a changes to a '0'; this is routed via AND gate G10 to NAND gate G13 and the resulting '1' output is inverted by TR5 to remove the front panel controls enable signal at board pin S.

COMPUTER THROUGH SELECT

76. A logic '1' THROUGH bit at ML14 pin 4 is routed via ML5 (pin 7 to pin 10) to the output shift register stage ML6, and to the control processor card via the AND/OR select gate ML9 (A3 to D3) and board pin 13. The control data and clock signals generated by the computer, and transferred via the computer highways at board pins 4 and 5, are then routed as transfer signals to the control processor card (and eventually to the control highways) via the line receivers ML28, the low-to-high voltage translator ML18, the AND/OR select gate ML9, and board pins 16 and 17.

DISPLAY INHIBIT

77. The DISPLAY INHIBIT bit output from ML14 is routed via ML5 (pin 4 to pin 2) to the display processor card via board pin M, where it inhibits the display output shift register (Chap. 14), and is also applied to the word 9 output shift register stage ML6.

COMPUTER IN STATUS

78. When the computer selects the IN status the logic '1' IN signal from ML14 sets the IN latch ML8a via AND gate G3. The resulting logic '1' Q output from ML8a is routed to:-

(1) The display processor card via board pin R to allow the entry of the transfer data and clock signals at board pins 16 and 17 (para. 80).

(2) Lamp driver stage TR3 to illuminate the IN push-button on the front panel via board pin H.

(3) The word 9 output shift register stage ML6.

79. The $\overline{Q}$ output signal from ML8a is routed via AND gate G10 to NAND gate G13 and the resulting logic '1' output is inverted by TR5 to remove the front panel controls enable signal at board pin S.

80. The computer highway data and clock signals, at board pins 4 and 5, are now routed as transfer signals to the display processor card via line receivers ML28, low-to-high level translators ML18, the AND/OR select gate ML9 and board pins 16 and 17.

STATUS SWITCH ENCODER

81. The front panel status switches, OUT, IN, RECALL and CHECK, together with the external check set input from the rear panel, are connected to an encoder circuit comprising two exclusive OR gates G6, G7, NOR gate G8, and a priority encoder ML27. The status priorities dictated by ML27 are shown in Table 3; as mentioned in para. 30, these priorities are used to set the status latches and do not affect status switch selection unless two switches are pressed simultaneously, when that with the higher priority overrides the other.

82. The priority encoder, ML27, is enabled by a logic '1' input applied to pin 5; this comes from the quad latch, ML5 pin 12, and is maintained at a '1' unless the STATUS INHIBIT bit of the word 9 data is set, in which case it changes to a '0' and disables ML27. The truth table for the applicable states of the priority encoder is given in Table 3.

TABLE 3: PRIORITY ENCODER TRUTH TABLE

INPUT		OUTPUT			
PRIORITY NUMBER	STATUS	GROUP SELECT	Q2	Q1	Q0
1	OUT	1	0	0	1
4	IN	1	1	0	0
5	RECALL	1	1	0	1
6	CHECK	1	1	1	0
7	EXTERNAL SET CHECK	1	1	1	1

FRONT PANEL OUT STATUS

83. The momentary +12V output from the OUT switch at board pin J is applied to the D1 input of ML27 and to AND gate G4; the remaining input to G4 is also at logic '1' (+12 Va via R8 and R9 provided the exchange busy signal is not present), and a '1' is applied to the J input of the OUT latch ML8b.

84. The logic '1' Q0 output from ML27 is used for switch contact bounce suppression (via R13) whilst the logic '1' group select output is applied to the clock input of the OUT latch ML8b via G2 (the other input to G2 is from the +12 Va rail via R1 and R2 when the computer present connection is not made). The Q output from ML8b changes to a '1' and this is applied to:-

(1) Lamp driver stage TR1 to illuminate the OUT push-button via board pin K.

(2) NOR gate G24 to enable the two level conversion output stages.

(3) The A input (binary 1) of the data selector ML19 to enable the channel 1 input for the control data and clock signals at board pins T and U, which are routed to the exchange highways.

(4) Inverter stage TR2 which produces the logic '0' exchange busy signal at board pin 8; this is connected in parallel to pin 8 on each status card (via the rear panel connectors) for each MA.1090 control unit in a multi-operator installation to prevent a further operator selecting the OUT status.

85. The logic '0' exchange busy output from TR2 is also applied to the J input of the OUT latch ML8b via AND gate G4; when the OUT push-button is pressed a second time the Q output from ML8b changes to logic '0' and the OUT status is cancelled.

FRONT PANEL IN STATUS

86. The momentary +12V output from the IN switch at board pin F is applied via the AND/OR select gate ML9 (B4 to D4) to the J input of the IN latch ML8a, and to the D4 input of the priority encoder ML27. Resistor R7 is included for switch contact bounce suppression purposes.

87. The logic '1' Q2 output from ML27 (Table 3) is applied to the clock input of the preserve latch ML17b; the logic '1' at the J input (when the CHECK status is not selected, and prior to the selection of the IN status, the $\overline{Q}$ outputs from ML17a and ML8a are both at '1') is transferred to the Q output and is routed to the control processor card via board pin 15. The front panel control settings are preserved in the recall store and the preserve reset signal is then generated (on the control processor card) which is applied to ML17b via board pin 14.

88. The logic '1' group select output from ML27 is applied to the clock input of the IN latch, via AND gate G2; this sets the Q output to a '1' and the $\overline{Q}$ output to a '0'. The logic '1' Q output is applied to:-

(1) The control processor card via ML9 (B3 to D3) and board pin 13 as the THROUGH signal to allow the entry of the transfer data and clock signals.

(2) The display processor card via board pin R to allow the entry of the transfer data and clock signals.

(3) Lamp driver stage TR3 to illuminate the IN push-button lamp.

89. The logic '0' $\overline{Q}$ output from ML8a is applied via AND gate G10 to NAND gate G13 and the resulting '1' output turns on TR5 which disables the front panel controls, by removing the front panel controls enable signal at board pin S.

90. The exchange data and clock signals, at board pins 6 and 7 are routed to the display processor and control processor cards via line receivers ML28, low-to-high voltage translators ML18, the AND/OR select gate ML9 (B1 to D1 and B2 to D2), and board pins 16 and 17.

91. When the IN push-button is pressed a second time, the Q output from ML8a changes to a '0', the $\overline{Q}$ output changes to a '1', and the IN status is cancelled (the truth table for a J-K flip-flop is given in Table 4).

RECALL STATUS

92. The RECALL status may only be selected at the front panel. The momentary +12V signal at board pin C is applied via the switch contact bounce suppression circuit G6/R16 to the D5 input of the priority encoder ML27, and to the clock input of the recall latch ML16a. The data input at ML16a pin 9 is at logic '1' (except when a computer is connected and the STATUS INHIBIT bit is set) and the resulting logic '0' $\overline{Q}$ output is applied to the control processor card via board pin 11.

93. The logic '1' Q output from ML16a is applied via G11 to the set input of the preserve latch ML17b, setting its Q output to logic '1'; this is applied to the control processor card via board pin 15, and the present front panel control settings are preserved in, whilst the former settings are recovered from, the recall store. The preserve reset signal is then produced which is applied to the preserve and recall latches via board pin 14.

FRONT PANEL CHECK STATUS

94. The output signal from the CHECK switch at board pin D is applied to the D6 input of the priority encoder ML27, via the switch contact bounce suppression circuit G7/R15. The Q1 output applies a '1' to the J input of the check latch ML17a, the logic '1' Q2 output is applied to the clock input of the preserve latch ML17b, and the logic '1' group select output is applied to the clock input of the check latch ML17a; this sets the Q output to a '1' and the $\overline{Q}$ output to a '0' (the K input is at logic '1' via R17 and R18).

95. The resulting logic '1' Q output from the preserve latch is routed to the control processor card via board pin 15 to preserve the present front panel settings in the recall store. The preserve reset signal is then produced which is applied to the preserve latch via board pin 14.

96. The logic '1' Q output from the check latch is applied to the lamp driver stage TR4 to illuminate the CHECK push-button lamp via board pin E, and is also applied via board pin 12 to:-

(1) To the control processor card to set the CONTROL INHIBIT bit of the preamble (bit 8) to a '1' and so inhibit the control of the associated transmitter.

(2) The display processor card to allow the entry of the revertive highway data from the transmitter for subsequent display on the MA.1090 front panel.

97. The logic '0' $\overline{Q}$ output from the check latch is routed via AND gate G10 to NAND gate G13 and the resulting logic '1' disables the front panel controls via TR5 and board pin S.

98. If the CHECK push-button is pressed a second time, since both the J and K inputs of the check latch are at logic '1', the Q output changes to a '0', the $\overline{Q}$ output changes to a '1', and the CHECK status is cancelled.

EXTERNAL CHECK SET

99. A 0V input at board pin 10 is applied via D3, R17 and G8 to the D7 input of the priority encoder ML27, and this sets the Q1, Q2 and group select outputs from ML27 at logic '1', as for the front panel CHECK status (paras. 94 to 97). The 0V input at board pin 10 is also applied to the K input of the check latch and this ensures that if the CHECK status is already selected it is not switched off by the application of the external check set input (See Table 4).

POWER FAIL DETECTOR

100. The power fail detector stage, TR12, is powered from the +12 Vb battery supply and monitors the +12 Va output from the power supply module; if the level of the +12 Va supply falls below approximately 10V a '1' output is produced which is applied to:-

(1) The status latches via G14 as a reset signal.

(2) NOR gate G8 to inhibit the external check set input.

(3) The reset inputs of the word 9 input shift register stages ML14 and ML4.

(4) The set input of the error latch ML22b to inhibit the generation of the status load pulse.

TABLE 4: J-K FLIP-FLOP TRUTH TABLE

PRESENT STATE					CLOCK	NEXT STATE		
INPUTS				OUTPUT		OUTPUTS		
J	K	S	R	Q		Q	$\overline{Q}$	
1	X	0	0	0	⌒	1	0	
X	0	0	0	1	⌒	1	0	
0	X	0	0	0	⌒	0	1	
X	1	0	0	1	⌒	0	1	
X	X	0	0	X	⌣			NO CHANGE
X	X	1	0	X	X	1	0	
X	X	0	1	X	X	0	1	
X	X	1	1	X	X	1	1	

X = don't care

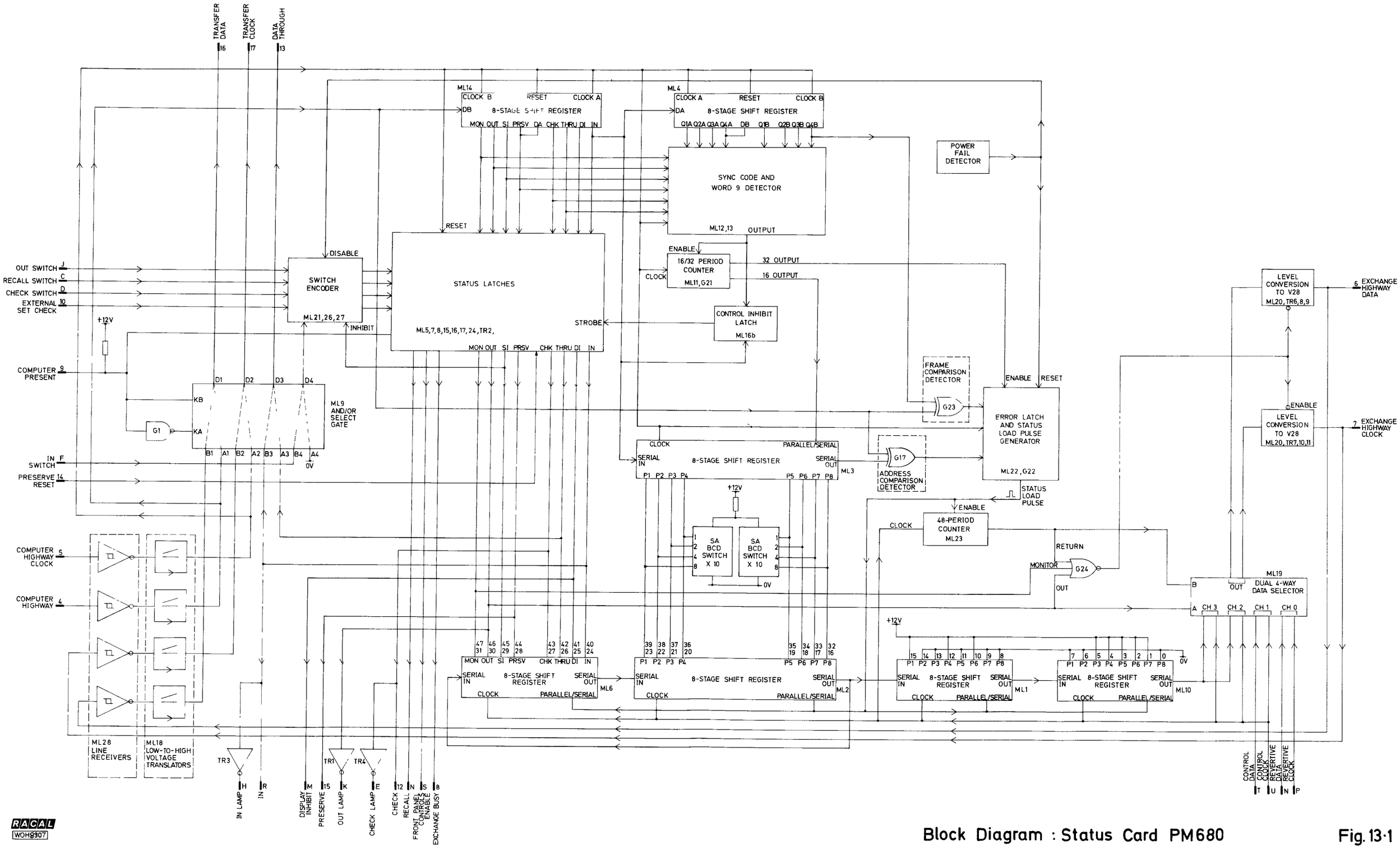
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number	Manufacturer
		STATUS CARD PM.680 (ST77321)				
Resistors						
R1	12k	Metal Oxide		2	917952	Electrosil TR4
R2	12k	Metal Oxide		2	917952	Electrosil TR4
R3	1.8k	Metal Oxide		2	911148	Electrosil TR4
R4	1.8k	Metal Oxide		2	911148	Electrosil TR4
R5	1.8k	Metal Oxide		2	911148	Electrosil TR4
R6	1.8k	Metal Oxide		2	911148	Electrosil TR4
R7	22k	Metal Oxide		2	913493	Electrosil TR4
R8	12k	Metal Oxide		2	917952	Electrosil TR4
R9	12k	Metal Oxide		2	917952	Electrosil TR4
R10	22	Metal Oxide		2	920743	Electrosil TR4
R11	22k	Metal Oxide		2	913493	Electrosil TR4
R12	22k	Metal Oxide		2	913493	Electrosil TR4
R13	22k	Metal Oxide		2	913493	Electrosil TR4
R14	22k	Metal Oxide		2	913493	Electrosil TR4
R15	22k	Metal Oxide		2	913493	Electrosil TR4
R16	22k	Metal Oxide		2	913493	Electrosil TR4
R17	12k	Metal Oxide		2	917952	Electrosil TR4
R18	12k	Metal Oxide		2	917952	Electrosil TR4
R19	22k	Metal Oxide		2	913493	Electrosil TR4
R20	22k	Metal Oxide		2	913493	Electrosil TR4
R21	22k	Metal Oxide		2	913493	Electrosil TR4
R22	22	Metal Oxide		2	920743	Electrosil TR4
R23	1.8k	Metal Oxide		2	911148	Electrosil TR4
R24	22	Metal Oxide		2	920743	Electrosil TR4
R25	12k	Metal Oxide		2	917952	Electrosil TR4
R26	22k	Metal Oxide		2	913493	Electrosil TR4
R27	68k	Metal Oxide		2	916478	Electrosil TR4
R28	22k	Metal Oxide		2	913493	Electrosil TR4
R29	22k	Metal Oxide		2	913493	Electrosil TR4
R30	22k	Metal Oxide		2	913493	Electrosil TR4
R31	270	Metal Oxide		2	910391	Electrosil TR4
R32	270	Metal Oxide		2	917952	Electrosil TR4
R33	12k	Metal Oxide		2	917952	Electrosil TR4

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number	Manufacturer
Resistors			W			
R34	12k	Metal Oxide		2	917952	Electrosil TR4
R35	12k	Metal Oxide		2	917952	Electrosil TR4
R36	12k	Metal Oxide		2	917952	Electrosil TR4
R37	12k	Metal Oxide		2	917952	Electrosil TR4
R38	180	Wirewound	2.5	5	913602	Welwyn W21
R39	180	Wirewound	2.5	5	913602	Welwyn W21
R40	2.7k	Metal Oxide		2	916548	Electrosil TR4
R41	12k	Metal Oxide		2	917952	Electrosil TR4
R42	12k	Metal Oxide		2	917952	Electrosil TR4
Capacitors			V			
C1	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C2	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C3	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C4	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C5	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C6	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C7	100p	Disc Ceramic	500	10	917438	Erie 831/N3300
C8	2200p	Disc Ceramic	500	25	917438	Erie 831/K7004
C9	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C10	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C11	6.8	Tantalum	35	20	910129	Union Carbide K6R8J35S
C12	6.8	Tantalum	35	20	910129	Union Carbide K6R8J35S
C13	2200p	Disc Ceramic	500	25	917438	Erie 831/K7004
C14	2200p	Disc Ceramic	500	25	917438	Erie 831/K7004
C15	2200p	Disc Ceramic	500	25	917438	Erie 831/K7004
C16	0.1	Polyester	100	20	914173	STC PMT2R0.1M100

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number	Manufacturer
Diodes			V	mW		
D1		Silicon			914898	STC 1N4149
D2		Silicon			914898	STC 1N4149
D3		Silicon			914898	STC 1N4149
D4		Zener	4.7	400	914067	Mullard BZY88C4V7
D5		Silicon			914898	STC 1N4149
D6		Silicon			914898	STC 1N4149
D7		Silicon			914898	STC 1N4149
D8		Silicon			914898	STC 1N4149
D9		Zener	10	400	917217	Mullard BZY88C10
Transistors						
TR1		NPN Silicon			914900	Mullard BC109
TR2		NPN Silicon			914900	Mullard BC109
TR3		NPN Silicon			914900	Mullard BC109
TR4		NPN Silicon			914900	Mullard BC109
TR5		NPN Silicon			914900	Mullard BC109
TR6		PNP Silicon			915568	Mullard BCY70
TR7		PNP Silicon			915568	Mullard BCY70
TR8		PNP Silicon			927707	ITT BC160-16
TR9		NPN Silicon			927706	ITT BC140-16
TR10		PNP Silicon			927707	ITT BC160-16
TR11		NPN Silicon			927706	ITT BC140-16
TR12		NPN Silicon			914900	Mullard BC109

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number	Manufacturer
Integrated Circuits						
ML1		8-stage shift register			930977	RCA CD4021 BE
ML2		8-stage shift register			930977	RCA CD4021 BE
ML3		8-stage shift register			930977	RCA CD4021 BE
ML4		Dual 4-stage shift register			930973	RCA CD4015 BE
ML5		Quad D-type latch			930861	RCA CD4042 BE
ML6		8-stage shift register			930977	RCA CD4021 BE
ML7		Quad 2-input AND gate			929322	RCA CD4081 BE
ML8		Dual J-K flip-flop			930981	RCA CD4027 BE
ML9		Quad AND/OR select gate			930976	RCA CD4019 BE
ML10		8-stage shift register			930977	RCA CD4021 BE
ML11		Dual binary up-counter			930047	RCA CD4520 BE
ML12		8-input NOR gate			928000	RCA CD4078 BE
ML13		8-input NAND gate			929317	RCA CD4068 BE
ML14		Dual 4-stage shift register			930973	RCA CD4015 BE
ML15		Quad 2-input AND gate			929322	RCA CD4081 BE
ML16		Dual D-type flip-flop			926860	RCA CD4013 BE
ML17		Dual J-K flip-flop			930981	RCA CD4027 BE
ML18		Quad voltage translator			927798	Texas 34104
ML19		4-way data selector			927230	Motorola MC14539
ML20		Dual binary to 1-of-4 inverter			929333	RCA CD4556 BE
ML21		Triple 3-input NOR gate			930030	RCA CD4025 BE
ML22		Dual D-type flip-flop			926860	RCA CD4013 BE
ML23		Dual binary up-counter			930047	RCA CD4520 BE
ML24		Quad 2-input NAND gate			930028	RCA CD4011 BE
ML25		Triple 3-input OR gate			928190	RCA CD4075 BE
ML26		Quad exclusive OR gate			930856	RCA CD4070 BE
ML27		Priority encoder			929702	RCA CD4532 BE
ML28		Quad line receiver			931220	Texas SN75189A N

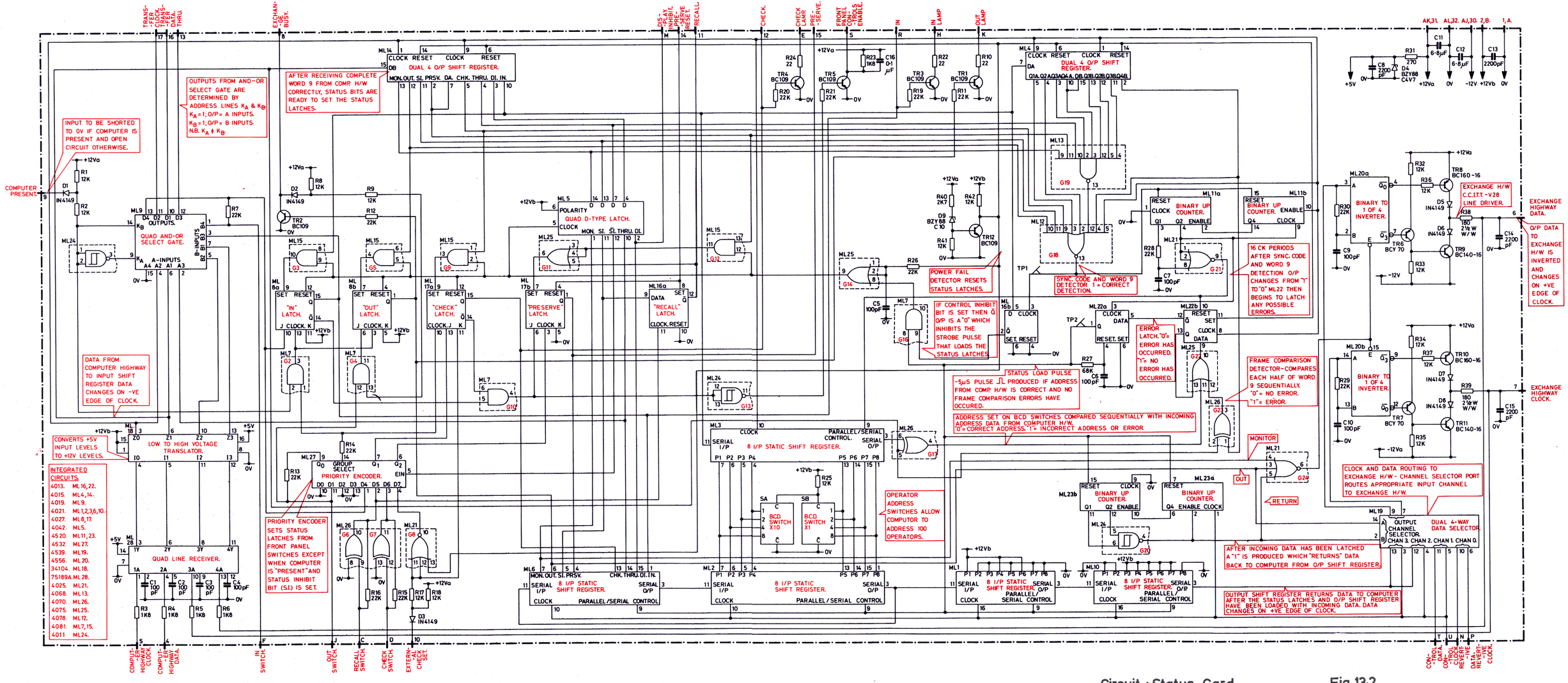
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number	Manufacturer
Miscellaneous						
SA		BCD Strip switch			927797	Waycom 1A-21-30-56-G/F
SB		BCD Strip switch			927797	Waycom 1A-21-30-56-G/F
		14-pin DIL IC socket			927053	Texas C83-14-02
		16-pin DIL IC			927054	Texas C83-16-02



RACAL
WOH8307

Block Diagram : Status Card PM680

Fig. 13·1



Circuit : Status Card

Fig. 13-2

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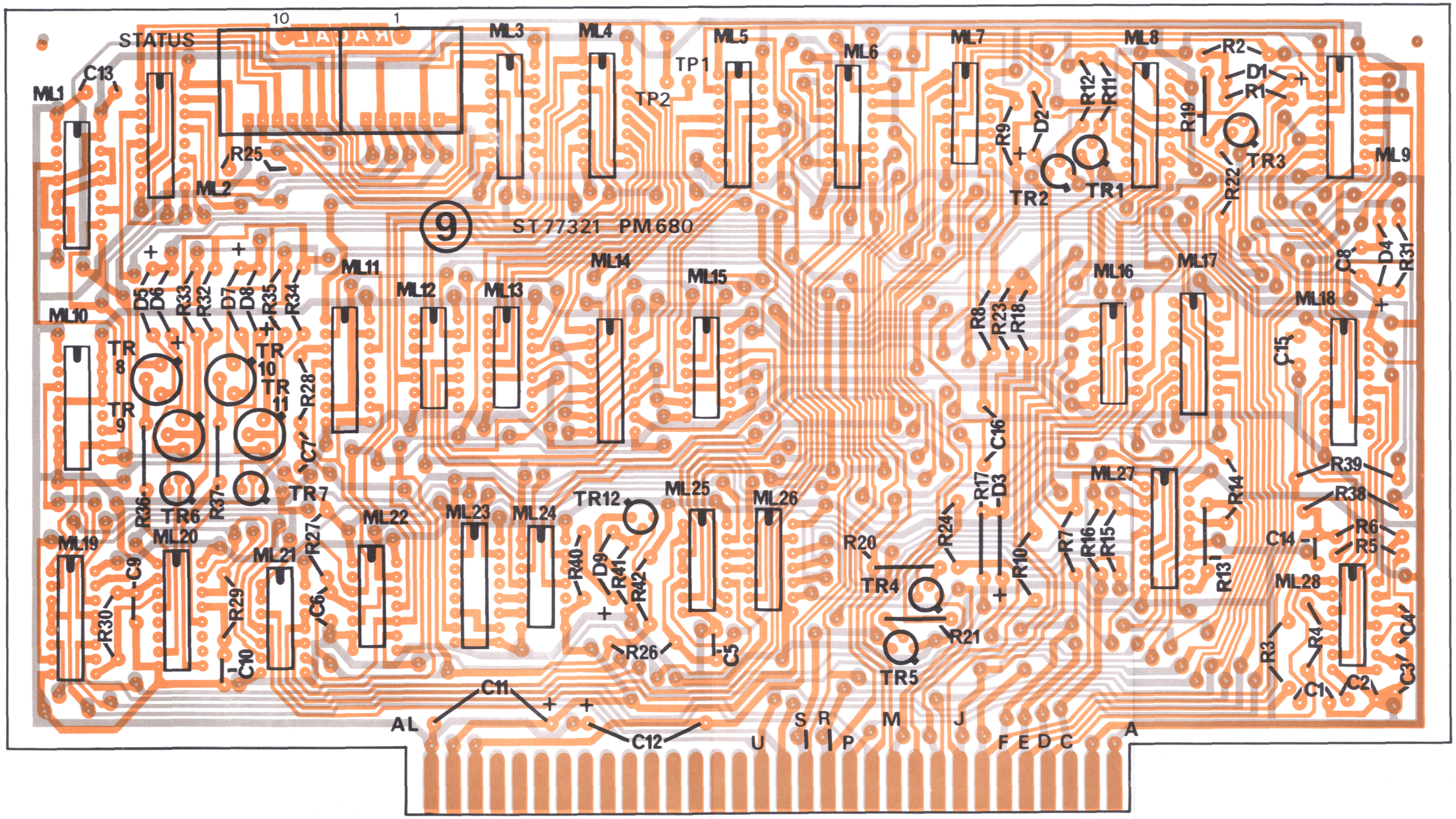

Layout : Status Card

Fig.13·3

CHAPTER 14

DISPLAY PROCESSOR CARD

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CHAPTER 14

DISPLAY PROCESSOR CARD

INTRODUCTION

1. The display processor card contains the revertive monitor word (word 0) circuitry; it also contains the data and clock selection circuitry for the display register data and clock signals applied to the front panel board and the frequency card, and it generates the display register strobe pulse.

FUNCTIONAL DESCRIPTION

2. The following functional description paragraphs should be read in conjunction with the block diagram of the display processor card given in Fig. 14.1.

Clock Selection

3. In extended control installations, a revertive clock connection between the MA.1090 and the transmitter is not normally required. In the absence of the revertive clock input (board connector pin 24) the control clock (board connector pin 17) is automatically selected in place of the revertive clock by a selection circuit G1 to G3.

4. The revertive data present input (board connector pin 25) is normally open-circuit. In certain multi-equipment installations, a negative signal may be applied to this input to inhibit the revertive data by disabling the revertive clock signal.

Display Register Data

5. The inverted display register data, at board connector pin 28, comes from one of the following five sources:-

(1) External data at board connector pin C from either:-

(a) External equipment connected to pin 29 of PL2 on the MA.1090 rear panel, or

(b) External equipment connected to the EXTERNAL socket on the front panel, provided, in each case, that the external entry/data inhibit input (board connector pin 18) is preset.

(2) Revertive data, at board connector pin 23, from the associated transmitter, when CHECK is selected.

(3) Transfer data at board connector pin 20, from a computer via the computer highway, or another MA.1090 control unit, via the exchange highway, when the IN status is selected.

(4) Control data at board connector pin 16, from the internal recall store, when RECALL is selected.

6. These data input signals, together with the associated clock signals (the control clock is used for external data, and also for the revertive data when the revertive clock is not present) are applied to the data and clock selection circuit (ML11, 12, 18, G5, G7); this circuit contains a priority encoder which controls a dual 4-channel data multiplexer. The external entry/data inhibit, external entry select, CHECK, IN, PRESERVE and RECALL select signals (at board connector pins 11, D, 21, 14, 15 and 22) are applied to the priority encoder and the resulting clock and data output signals from the multiplexer are as shown in Table 1. This Table also shows the priority of each select signal, i.e. the external entry/data inhibit and external entry select inputs have the lowest priority, and RECALL has the highest priority.

TABLE 1: DATA AND CLOCK SELECTION

PRIORITY ENCODER LEVEL*	SELECT SIGNAL	DATA INPUT
1	EXTERNAL	EXTERNAL
3	CHECK	REVERTIVE HIGHWAY
5	IN	TRANSFER HIGHWAY
6	PRESERVE	OUTPUT INHIBITED
7	RECALL	CONTROL HIGHWAY

* 2 and 4 not used

Preserve

7. The PRESERVE input is generated each time CHECK, IN or RECALL is selected (it may also be generated by a computer via the word 9 circuitry on the status card - Chap. 13). When CHECK is selected the front panel controls are disabled and the outputs from the data and clock selection circuit are inhibited whilst the existing front panel settings are preserved in the recall store (on the control processor card). The PRESERVE function is then reset, and the CHECK select signal then routes the revertive highway clock and data signals to the display input registers on the front panel board and the frequency card. The action of the circuit is similar when IN is selected except that once the front panel settings are preserved in the recall store and the PRESERVE input is reset, the transfer highway data is

routed to the display input registers. Thus the PRESERVE input overrides the CHECK and IN select inputs until the front panel settings are preserved in the recall store.

8. When RECALL is selected, the existing settings are preserved in the recall store whilst the previous settings are recovered from the recall store and routed via the control data highway to the display input registers; the PRESERVE and RECALL select inputs are then both automatically reset.

Display Register Strobe

9. A negative-going nominal 5 μs display register strobe pulse, at board connector pin 27, is routed to the word detectors on the front panel board (word 3) and the frequency card (word 1); this pulse is generated at the end of each 48-bit frame from the data and clock selection circuit (provided one of the input select inputs is active) only when a correct sync. code is detected. The action of the circuit is as follows.

10. The first eight bits of the frame clocked into the 8-stage shift register ML10 should consist of the sync. code (a '0' followed by five ones) and a 2-bit transmit/receive code ('0' - '1' or '1' - '0'). If these eight bits are correct, a counter enable pulse is produced by the display sync. code detector (G8, 9, 10, 13, 14 and ML2a) which is applied to a 40-period counter ML1. At the end of the next forty clock bits, a pulse is generated by ML26 which is inverted by the output buffer stage TR13 to become the display register strobe pulse.

Revertive Monitor Word

11. The revertive data from the transmitter is routed to a 32-bit register ML16, ML22, ML21, ML20, via board connector pin 23 and a Schmitt trigger stage TR4, ML3. When the word 0 detector (para. 12) detects the presence of word 0 during the end-of-frame pulse output from ML6a (para. 13), a monitor load pulse is produced (G22); this is applied to the strobe inputs of the shift register stages and the monitor word data is latched at the parallel outputs. The monitor load pulse is inhibited if the display inhibit input (board connector pin 11) is set to a '1' (para. 14).

Word 0 Detector

12. When the monitor word is correctly positioned in the 23-bit input shift register, the four-bit identification code for word 0 (bits 12 to 15 of the preamble) is located in the 4-stage shift register ML13a. If these four bits are all at '0', denoting the presence of word 0, the word 0 detector produces a logic '0' output which is applied to NOR gate G22.

End-of-frame Pulse

13. The end-of-frame pulse generation circuit is similar to the display register strobe pulse generator described in para. 9. If the first eight bits of the frame clocked into the 8-stage shift register ML16 are recognised as a correct sync. code, a counter enable pulse is produced; this starts the 40-period counter ML15, and at the end of the next forty clock bits, a negative-going end-of-frame pulse is produced which is applied to G22.

Display Inhibit

14. The display inhibit input, at board connector pin 11, is set to a '1' by a computer (via the word 9 circuitry on the status card - Chap. 13) to, for example, prevent the revertive data from a transmitter under interrogation by the computer being displayed on the MA.1090, which may be controlling a different transmitter. The display inhibit bit is applied to G22 via a 2-stage shift register ML13b to delay its application by two frames; this allows two frames to be processed before the output of G22 is forced to logic '0' to inhibit the monitor load pulse.

Revertive Indicators

15. Data bits 34, 33, 32, 31, 28, 27, 26 and 24 of the word 0 data are all associated with the revertive indicators on the front panel, namely LINE FAULT, TRANSMIT, REDUCED POWER, READY, CONTROL ON, EHT ON and STANDBY.

16. The line fault decode circuit G16, G21, ML3, causes illumination of the LINE FAULT indicator, via TR7 and board connector pin X when either:-

(1) The frame comparison error bit (bit 34) is set to a '1' at the transmitter following the detection of three consecutive frame comparison errors, or

(2) A spurious monitor sync. code is detected, or

(3) The monitor sync. code detector produces a '1' output to the fault decode circuit following a break in the revertive data (caused by, for example, a line break).

Revertive User Functions

17. The remaining operative bits of the word 0 data, 19 down to 16, provide for the revertive user functions where up to four earth (0V) signals applied to the transmitter are reproduced at pins 34 to 37 of PL2 on the rear panel via open-collector transistors TR16, TR17 and TR18, TR19, and board connector pins 26, AB, AC and AD respectively.

CIRCUIT DESCRIPTION

18. The circuit diagram of the control processor card is given in Fig. 14.2; the layout is given in Fig. 14.3.

Clock Selection

19. When the revertive highway clock signal is present, at board connector pin 24, the V28 signal levels are converted to C-MOS levels by a Schmitt trigger TR3 and feedback components ML3, R5. Capacitor C6 is kept discharged via D6, resulting in a '1' output from G2 which opens G1 for the output signal from the collector of TR3.

20. When the revertive highway clock signal is not present, the non-conductive state of TR3 results in a '1' at pin 6 of G1 and also at pin 1 of G1; the gates are opened and the control clock signal (board connector pin 17) is allowed through for use in place of the revertive clock.

21. Gate G3 is controlled by the revertive data present input at board pin 25. This input is normally an open-circuit to open gate G3 for the clock signal from G1. In certain multi-equipment installations, however, the revertive data is inhibited by disabling the revertive clock; this is achieved by applying a negative voltage signal to board connector pin 25 which turns off TR2 and results in a logic '1' at pin 9 of G3.

22. The revertive clock signal from G3 is applied to the status card via inverting buffer G4 and board connector pin 13, to the monitor word input shift register (para. 33), the word 0 detector (para. 30), to the data and clock selection circuit (para. 23), and to the monitor sync. code detector and counter.

Data and Clock Selection

23. The display register data and clock signals applied to the front panel board and the frequency card (via board connector pins 28 and 29) are selected from a number of sources by the data and clock selection circuit; this comprises two R/S latches ML18, a priority encoder ML12, NAND gate G5, NOR gate G7, and a dual 4-channel data multiplexer ML11. The CHECK, IN, PRESERVE and RECALL select inputs, at board connector pins 21, 14, 15 and 22 respectively, are from the status card (Chap. 13), the external entry select input, at board connector pin D (this input is not normally used) comes from PL2 pin 32 on the rear panel, whilst the external entry/data inhibit input, at board connector pin 18, comes either from the EXTERNAL socket on the front panel or PL2 pin 28 on the rear panel.

24. The 8-bit priority encoder ML12, which is permanently enabled by the logic '1' at pin 5, encodes the highest priority input to a 3-bit binary code. The eight inputs D0 to D7 each have an assigned priority where D7 is the highest priority and D0 the lowest. Table 2 shows the 3-bit output code for each of the five data select input signals. Ignoring the PRESERVE select input for the moment, it can be seen from this table that the Q0 output is at '1' for all the remaining select inputs, whilst the Q1 and Q2 outputs provide a unique 2-bit code i.e. binary 0, 1, 2 and 3 for EXTERNAL, CHECK, IN and RECALL respectively. The Q0 output is inverted by NOR gate G7 and applied to the inhibit pins of the data multiplexer ML11 ('1' to inhibit), whilst the 2-bit binary code output from Q1 and Q2 is applied to the A and B input pins of ML11 to select the similarly numbered outputs, i.e. binary 0 selects X0 and Y0, binary 1 selects X1 and Y1, and so on.

25. As stated in para. 7, the PRESERVE select input is generated each time CHECK, IN or RECALL is selected (or it may be selected by a computer). For CHECK and IN, the Q0 output from ML12 goes to logic '0' (Table 2) and inhibits ML11 until the front panel settings are preserved in the recall store; the PRESERVE select input is then reset and allows selection of the revertive highway data and clock (X1 and Y1) if CHECK was selected, or the transfer highway data and clock (X2 and Y2) if IN was selected. When RECALL is

selected, since RECALL has a higher priority than PRESERVE, the previous front panel settings are recovered from the recall store via the control highway whilst the existing front panel settings are entered into the recall store via circuitry on the control processor card (Chap. 12).

TABLE 2: PRIORITY ENCODER OPERATION

DATA SELECT INPUT	ENCODER PRIORITY	3-BIT OUTPUT CODE		
		Q2	Q1	Q0
EXTERNAL	1	0	0	1
CHECK	3	0	1	1
IN	5	1	0	1
PRESERVE	6	1	1	0
RECALL	7	1	1	1

Display Sync. Code Detector

26. The selected data and clock signals from ML11 (X out and Y out) are routed to the front panel board and the frequency card via open collector inverting buffer stages TR15, TR14, and board connector pins 28 and 29 respectively. The data is also clocked into the display sync. code detector which comprises a dual 4-stage shift register ML10 (connected as an 8-stage register), NAND gates G8, G9, G10, NOR gates G13, G14, and a J-K flip-flop ML2a.

27. When the first six bits of a correct sync. code, i.e. a '0' followed by five consecutive '1s', are clocked into ML10, the inputs to NAND gates G8 and G9 are all at logic '1'; the resulting '0' outputs are applied to NOR gate G13 and this results in a '1' at the J input of ML2a. At the same time, the '0' at the Q2A output of ML10 results in a '1' at the output of G10; this is inverted by G14, a '0' is applied to the K input of ML2a, and, after the next clock pulse, the Q output of ML2a changes to a '1' to reset the 40-period counter ML1. After the next clock pulse the eight bits of the sync. code are positioned in ML10. If the code is correct (a '0' and five '1s' followed by '0'-'1' or '1'-'0'), the resulting parallel outputs from ML10 cause a '0' at the J input and a '1' at the K input of ML2a. Thus if a correct sync. code is detected, the Q output from ML2a changes to a '0' and the 40-period counter is restarted by the removal of the reset input. If a further sequence of five '1s' occurs during the next 40 bits, then the Q output of ML2a goes to a '1' and the 40-period counter is again reset. The set input of ML2a is normally at logic '0' and goes to a '1' following a power failure (para. 43).

Display Register Strobe

28. ML1 is a dual BCD up-counter where ML1a produces a '1' at the Q4 output for ten input pulses, and ML1b produces a '1' at the Q3 output for four input pulses. The input pulses are applied to the enable inputs and counting is enabled by the application of a '0' to the clock inputs. Thus 40 clock periods after the detection of a correct sync. code, the Q3 output from ML1b clocks the J-K flip-flop ML2b which generates a nominal 5 μs end-of-frame pulse (reset applied after time constant R41, C8); this pulse is used to reset the CHECK and RECALL R/S latches ML18, and is inverted by the open-collector output buffer stage TR13 to produce the display register strobe pulse at board connector pin 27. This is then routed to the word detectors on the front panel board (word 3) and the frequency card (word 1).

Monitor Word Sync. Code Detector

29. The monitor word sync. code detector is similar to the display sync. code detector (para. 26). It comprises a dual 4-stage shift register ML16 (connected as an 8-stage register), NAND gates G11, G12, G15, NOR gates G17, G18, and J-K flip-flop ML6b. A '0' is produced at the Q output of ML6b when a correct sync. code is received, and the reset input is removed from the 40-period counter ML15. If a further sequence of five '1s' occurs during the next 40 bits of data, the Q output of ML6b changes to a '1' and resets the 40-period counter.

Monitor Load Pulse

30. The 40-period counter ML15 is similar to that used for the generation of the display register strobe pulse (para. 28); the Q3 output at ML15a pin 5 goes to a '1' forty clock periods after detection of a correct sync. code (unless a further sequence of five '1s' occurs in the data) and ML6a generates a negative-going nominal 5 μs output pulse (reset applied from the Q output after time constant R42, C9). This is applied to NOR gate G22, and also to the clock input of ML13b which is connected as a 2-stage shift register. The display inhibit input, at board connector pin 11 (para. 32) is normally set to a '0' and the resulting '0' output at ML3b pin 12 is also applied to NOR gate G22.

30. The remaining input to NOR gate G20 comes from the word 0 detector ML13a, G23. When a monitor word is present and correctly positioned in the 32-bit input shift register (ML16, ML22, ML21, ML20), the word 0 identification code (bits 12 and 15 of the preamble) is present at the Q outputs of ML13a; the resulting '0' output from G23 is applied to G22 and a positive-going monitor load pulse is produced which is applied to the strobe inputs of the shift register stages ML20 to ML22 (para. 33).

Display Inhibit

32. As stated in para. 14, the display inhibit input, at board connector pin 11, is set to a '1' by a computer; since it is applied to the data input of a 2-stage shift register ML13b, it only appears at the Q2 output (to inhibit the monitor load pulse) following the application of two end-of-frame pulses from ML6a. This allows two frames to be

processed before the display inhibit takes effect, and when the display inhibit bit is reset to '0', a further two frames are inhibited before the MA.1090 again displays revertively-monitored information.

Monitor Word Shift Register

33. The revertive data monitor word is clocked into a 32-bit shift register comprising the dual 4-stage register ML16 (which is also part of the monitor word sync. code detector), and three 8-stage tri-state output latched register stages ML22, ML21, ML20. These devices have a storage latch associated with each stage for strobing data from the serial input to the parallel outputs Q1 to Q8. The data in each shift register stage is transferred to the storage register when the strobe input is at logic '1' (monitor load pulse). The parallel outputs assume one of three states and are controlled by the enable input (pin 15); when this is at logic '1' the two state (i.e. logic '1' or logic '0') data in the storage register appears at the parallel outputs, whilst if the enable input is at logic '0', the parallel outputs are open-circuit. In this application however, the monitor load pulse is applied to the strobe input and the enable input is connected to +12 Va to maintain the parallel outputs until the power is removed.

Line Fault Indicator

34. The illumination of the LINE FAULT indicator on the front panel is controlled by a decode circuit comprising NAND gates G16, G19, inverting NOR gate G20, OR gate G21 and lamp driver stage TR7. The three conditions given in para. 16, which result in the illumination of the LINE FAULT indicator, i.e. frame comparison error bit, spurious monitor sync. code and loss of revertive data, are described in the following paragraphs.

Frame Comparison Error Bit

35. The frame comparison error bit (bit 34) of the word 0 data, at ML22 pin 13, is set to a '1' at the transmitter following the detection of three consecutive frame comparison failures; this is inverted by NAND buffer G16 and is then applied to OR gate G21 via a fast attack - slow decay time constant circuit comprising inverter ML3, D9, R26 and C7. Thus a short-duration '1' output at ML22 pin 13 rapidly charges C7 via D9 and the illumination of the LINE FAULT lamp is maintained for approximately half a second.

Spurious Sync. Code

36. If the monitor sync. code detector detects a spurious sync. code, due either to corrupted data or a break in the revertive data input at board connector pin 23 which results in a maintained '1' output from the Schmitt trigger stage TR4, then the inputs to NAND gate G19 will all be at logic '1'; the resulting '0' output is inverted by G20 and a '1' is applied to OR gate G21.

Revertive Data Failure

37. Should a break occur in the revertive data which results in a maintained '0' output from the Schmitt trigger stage TR4, then the 40-period counter ML15 is not reset by a '1' output from the sync. code detector. When a count of eighty is reached (after the last valid sync. code), the Q4 output of ML15a goes to a '1' and this is routed to G21 to illuminate the LINE FAULT indicator.

38. Resistor R25 is included to pull the Q6 output of ML22 down to 0V should a power failure occur; this inhibits the line fault decode circuit and so reduces the current drain from the +12 Vb battery supply.

Fault Indicator

39. The fault bit (bit 33) of the word 0 data is set to a '1' at the transmitter following an out-of-lock condition in the synthesizer section of the transmitter drive unit. This turns on the lamp driver stage TR5 and the front panel FAULT indicator is illuminated.

Reduced Power Indicator

40. The reduced power indicator on the MA.1090 front panel is illuminated via lamp driver stage TR8 when a fault condition at the transmitter causes a reduction in the transmitter output power level. The information is conveyed by data bit 31 which appears at the Q1 output of ML21.

Ready, Control On, EHT On and Standby Indicators

41. These front panel indicators are illuminated via bits 28, 27, 26 and 24 of the word 0 data and lamp driver stages TR9 to TR12 respectively.

Revertive User Functions

42. The remaining operative bits of word 0 i.e. bits 19 down to 16, at ML20 pins 14, 13, 12 and 11, are concerned with the revertive user functions. When any of these bits are set to a '1', the respective open-collector transistors TR16 to TR19 provide a 0V output to external equipment connected to pins AD, AC, AB on 26 via PL2 on the rear panel.

Power Fail Detector

43. The power fail detector TR1 is powered from the internal battery supply (+12 Vb) and monitors the +12 Va output from the power supply module. Should the +12 Va supply fall to less than approximately +10V, TR1 cuts off and a '1' is routed to:-

(1) The reset inputs of ML10 and the set input to ML2a to inhibit the generation of the display register strobe pulse;

(2) The reset inputs of ML16 and the set input of ML6b to inhibit the generation of the monitor load pulse.

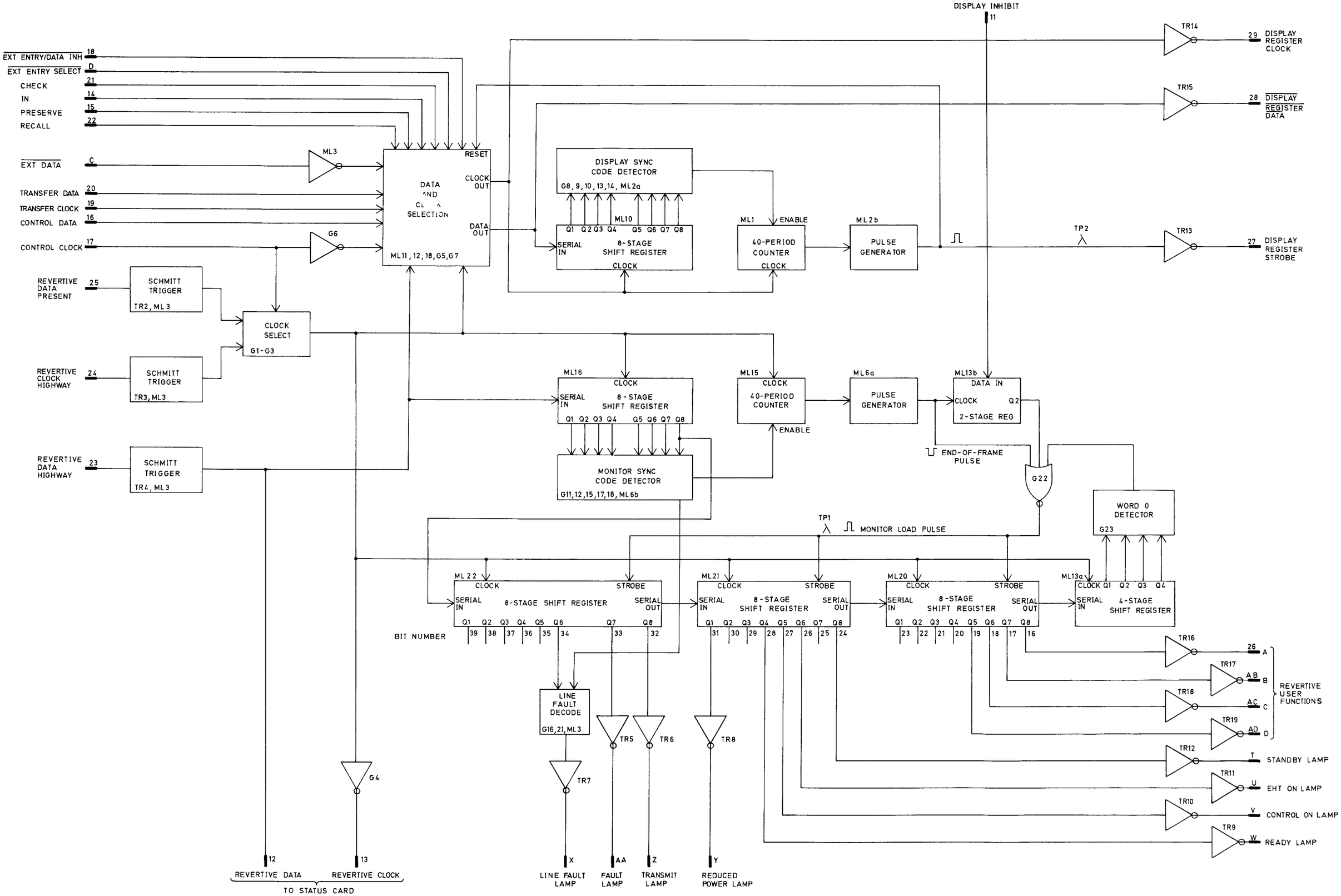
44. The purpose of the power fail detector is to switch off various non-essential circuits and so reduce the current drawn from the internal battery during a power failure.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number	Manufacturer
		DISPLAY PROCESSOR CARD (ST 78707)				
Resistors						
R1	5k6	Metal Oxide		2	918128	Electrosil TR4
R2	5k6	Metal Oxide		2	918128	Electrosil TR4
R3	5k6	Metal Oxide		2	918128	Electrosil TR4
R4	22k	Metal Oxide		2	913493	Electrosil TR4
R5	68k	Metal Oxide		2	916478	Electrosil TR4
R6	68k	Metal Oxide		2	916478	Electrosil TR4
R7	2k7	Metal Oxide		2	916548	Electrosil TR4
R8	12k	Metal Oxide		2	917952	Electrosil TR4
R9	68k	Metal Oxide		2	916478	Electrosil TR4
R10	12k	Metal Oxide		2	917952	Electrosil TR4
R11	1k8	Metal Oxide		2	911148	Electrosil TR4
R12	1k8	Metal Oxide		2	911148	Electrosil TR4
R13	12k	Metal Oxide		2	917952	Electrosil TR4
R14	68k	Metal Oxide		2	916478	Electrosil TR4
R15	12k	Metal Oxide		2	917952	Electrosil TR4
R16	12k	Metal Oxide		2	917952	Electrosil TR4
R17	12k	Metal Oxide		2	917952	Electrosil TR4
R18	12k	Metal Oxide		2	917952	Electrosil TR4
R19	12k	Metal Oxide		2	917952	Electrosil TR4
R20	12k	Metal Oxide		2	917952	Electrosil TR4
R21	12k	Metal Oxide		2	917952	Electrosil TR4
R22	12k	Metal Oxide		2	917952	Electrosil TR4
R23	22k	Metal Oxide		2	913493	Electrosil TR4
R24	22	Metal Oxide		2	920743	Electrosil TR4
R25	22k	Metal Oxide		2	913493	Electrosil TR4
R26	120k	Metal Oxide		2	915373	Electrosil TR4
R27	22k	Metal Oxide		2	913493	Electrosil TR4
R28	22	Metal Oxide		2	920743	Electrosil TR4
R29	22k	Metal Oxide		2	913493	Electrosil TR4
R30	22k	Metal Oxide		2	913493	Electrosil TR4
R31	470	Metal Oxide		2	920758	Electrosil TR4
R32	22k	Metal Oxide		2	913493	Electrosil TR4
R33	22	Metal Oxide		2	920743	Electrosil TR4
R34	22k	Metal Oxide		2	913493	Electrosil TR4
R35	22k	Metal Oxide		2	913493	Electrosil TR4

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number	Manufacturer
Resistors (Contd.)						
R36	470	Metal Oxide		2	920758	Electrosil TR4
R37	22k	Metal Oxide		2	913493	Electrosil TR4
R38	470	Metal Oxide		2	920758	Electrosil TR4
R39	470	Metal Oxide		2	920758	Electrosil TR4
R40	470	Metal Oxide		2	920758	Electrosil TR4
R41	68k	Metal Oxide		2	916478	Electrosil TR4
R42	68k	Metal Oxide		2	916478	Electrosil TR4
R43	22k	Metal Oxide		2	913493	Electrosil TR4
R44	22k	Metal Oxide		2	913493	Electrosil TR4
R45	22k	Metal Oxide		2	913493	Electrosil TR4
R46	22k	Metal Oxide		2	913493	Electrosil TR4
R47	22k	Metal Oxide		2	913493	Electrosil TR4
R48	22k	Metal Oxide		2	913493	Electrosil TR4
R49	22k	Metal Oxide		2	913493	Electrosil TR4
Capacitors			V			
C1	0.1	Polyester	100	10	920566	Waycom WIMA MKS 4
C2	0.1	Polyester	100	10	920566	Waycom WIMA MKS 4
C3	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C4	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C5	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C6	6.8	Tantalum	35	10	919480	Union Carbide K6R8J35KS
C7	6.8	Tantalum	35	10	919480	Union Carbide K6R8J35KS
C8	100p	Disc Ceramic	500	10	917417	Erie 831/N3300
C9	100p	Disc Ceramic	500	10	917417	Erie 831/N3300

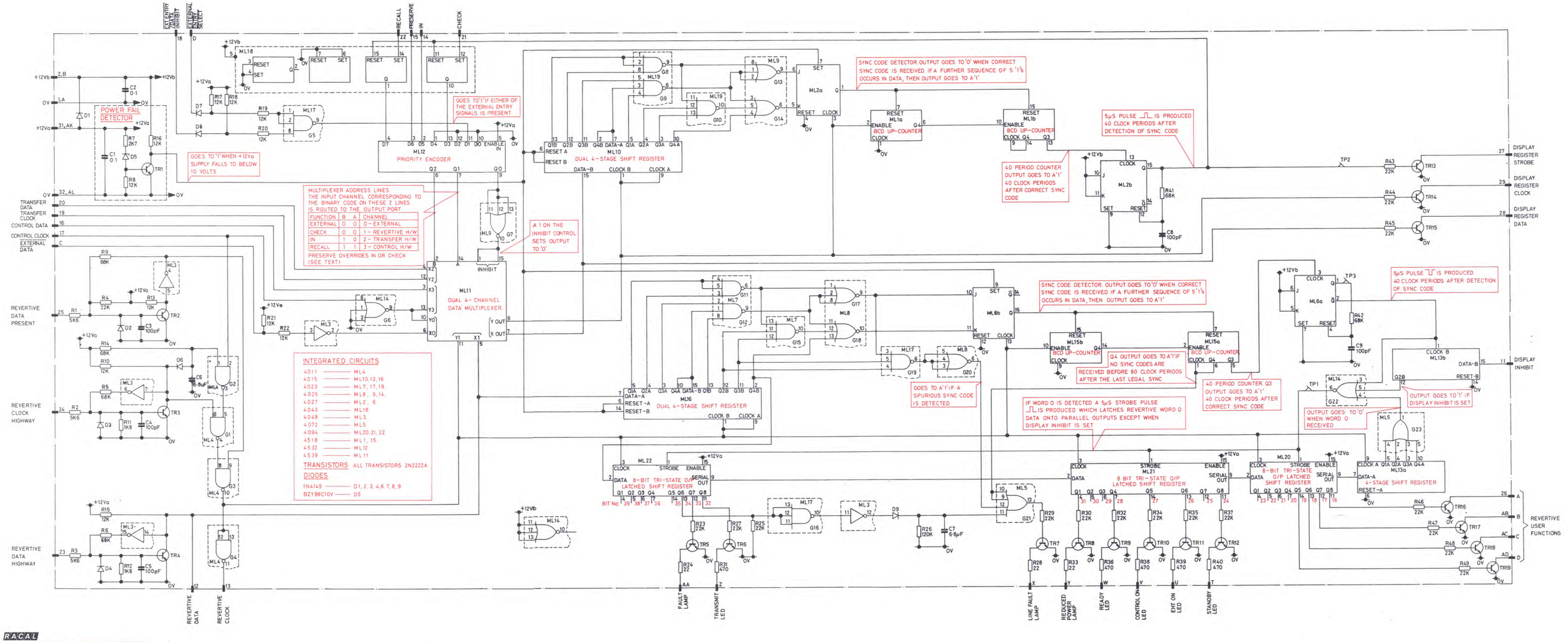
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number	Manufacturer
Diodes						
D1		Silicon			914898	STC 1N4149
D2		Silicon			914898	STC 1N4149
D3		Silicon			914898	STC 1N4149
D4		Silicon			914898	STC 1N4149
D5		Zener, 10V, 400mW			917217	Mullard BZY88C10V
D6		Silicon			914898	STC 1N4149
D7		Silicon			914898	STC 1N4149
D8		Silicon			914898	STC 1N4149
D9		Silicon			914898	STC 1N4149
Transistors						
TR1		NPN Silicon			923217	2N2222A (CV7770)
TR2		NPN Silicon			923217	2N2222A (CV7770)
TR3		NPN Silicon			923217	2N2222A (CV7770)
TR4		NPN Silicon			923217	2N2222A (CV7770)
TR5		NPN Silicon			923217	2N2222A (CV7770)
TR6		NPN Silicon			923217	2N2222A (CV7770)
TR7		NPN Silicon			923217	2N2222A (CV7770)
TR8		NPN Silicon			923217	2N2222A (CV7770)
TR9		NPN Silicon			923217	2N2222A (CV7770)
TR10		NPN Silicon			923217	2N2222A (CV7770)
TR11		NPN Silicon			923217	2N2222A (CV7770)
TR12		NPN Silicon			923217	2N2222A (CV7770)
TR13		NPN Silicon			923217	2N2222A (CV7770)
TR14		NPN Silicon			923217	2N2222A (CV7770)
TR15		NPN Silicon			923217	2N2222A (CV7770)

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number	Manufacturer
Transistors (Contd.)						
TR16		NPN Silicon			923217	2N2222A (CV7770)
TR17		NPN Silicon			923217	2N2222A (CV7770)
TR18		NPN Silicon			923217	2N2222A (CV7770)
TR19		NPN Silicon			923217	2N2222A (CV7770)
Integrated Circuits						
ML1		Dual BCD up-counter			928002	RCA CD 4518BE
ML2		Dual J-K flip-flop			930981	RCA CD 4027BE
ML3		Hex. inverting buffer			930033	RCA CD 4049BE
ML4		Quad 2-input NAND gate			930028	RCA CD 4011BE
ML5		Dual 4-input OR gate			929319	RCA CD 4072BE
ML6		Dual J-K flip-flop			930981	RCA CD 4027BE
ML7		Triple 3-input NAND gate			930978	RCA CD 4023BE
ML8		Triple 3-input NOR gate			930030	RCA CD 4025BE
ML9		Triple 3-input NOR gate			930030	RCA CD 4025BE
ML10		Dual 4-stage shift register			930973	RCA CD 4015BE
ML11		Dual 4-channel MUX			931025	RCA CD 4539BE
ML12		Priority Encoder			929702	RCA CD 4532BE
ML13		Dual 4-stage shift register			930973	RCA CD 4015BE
ML14		Triple 3-input NOR gate			930030	RCA CD 4025BE
ML15		Dual BCD Up-counter			928002	RCA CD 4518BE
ML16		Dual 4-stage shift register			930973	RCA CD 4015BE
ML17		Triple 3-input NAND gate			930978	RCA CD 4023BE
ML18		Quad R/S Latch			930855	RCA CD 4043BE
ML19		Triple 3-input NAND gate			930978	RCA CD 4023BE
ML20		8-stage shift register			929324	RCA CD 4094BE
ML21		8-stage shift register			929324	RCA CD 4094BE
ML22		8-stage shift register			929324	RCA CD 4094BE
Connectors						
		14-pin DIL IC socket			927053	Texas C83-14-02
		16-pin DIL IC socket			927054	Texas C83-16-02



RACAL
WOH 8307

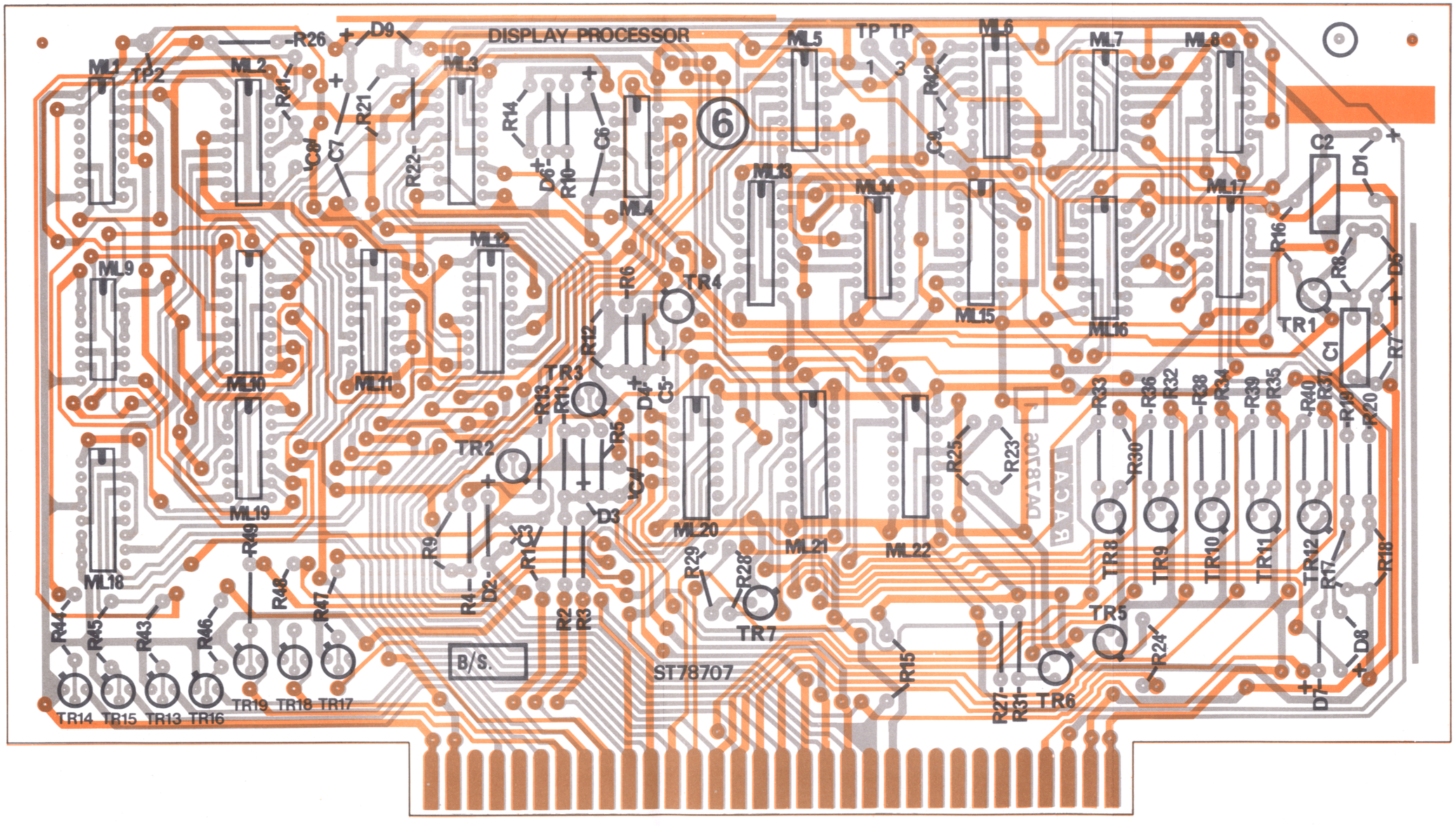
Block Diagram :
Display Processor Card **Fig. 14-1**



RACAL

WOH8307	DC78707	14-2	1/2
WOH8307	DC78707	14-2	2/2

Circuit : Display Processor Card Fig.14-2



RACAL		
WOH 8307	DA78706	14.3
1		1/3
WOH 8307	DA78706	14.3
1		2/3
WOH 8307	DA78706	14.3
1		3/3

Layout: Display Processor Card

Fig. 14.3

CHAPTER 15

POWER SUPPLIES

CONTENTS

	Para.
INTRODUCTION	1
MS685 POWER SUPPLY MODULE	2
BATTERY SUPPLY	5
COMPONENTS LIST	

ILLUSTRATIONS

	Fig.
Circuit: Power Supply Module MS685	15.1
Layout: Power Supply Module MS685	15.2

CHAPTER 15

POWER SUPPLIES

INTRODUCTION

1. The power supply module MS685 provides two regulated outputs at +12V (a and b), a +5V output and a -12V output. The +12 Vb output is used to trickle charge a 5V (nominal) internal battery, which is used to maintain power to various circuits in the event of a supply failure.

MS685 POWER SUPPLY MODULE

2. The circuit diagram of the power supply module is given in fig. 15.1. The supply input at PL3 is routed via FS1 and SK1 to the SUPPLY ON/OFF switch on the front panel and is then applied via the voltage selector panel VS1 to transformer T1.

3. Bridge rectifier D7 feeds the 3-terminal voltage regulator integrated circuits ML1, ML2 for both the +12 Va and +12 Vb supplies, D8 feeds the +5V regulator, and D9 feeds the -12V regulator. These three-terminal regulators contain a current limiting circuit to limit the peak output current to a safe value. If the internal power dissipation becomes too high for the heat sinking provided, a thermal shut-down circuit takes over to prevent the device overheating.

4. Diode D2 is included to prevent the battery discharging via the power supply when it is switched off or during a temporary supply failure, D2 compensates for the resultant voltage drop (across D2), whilst diodes D3 to D6 protect against input voltage reversal.

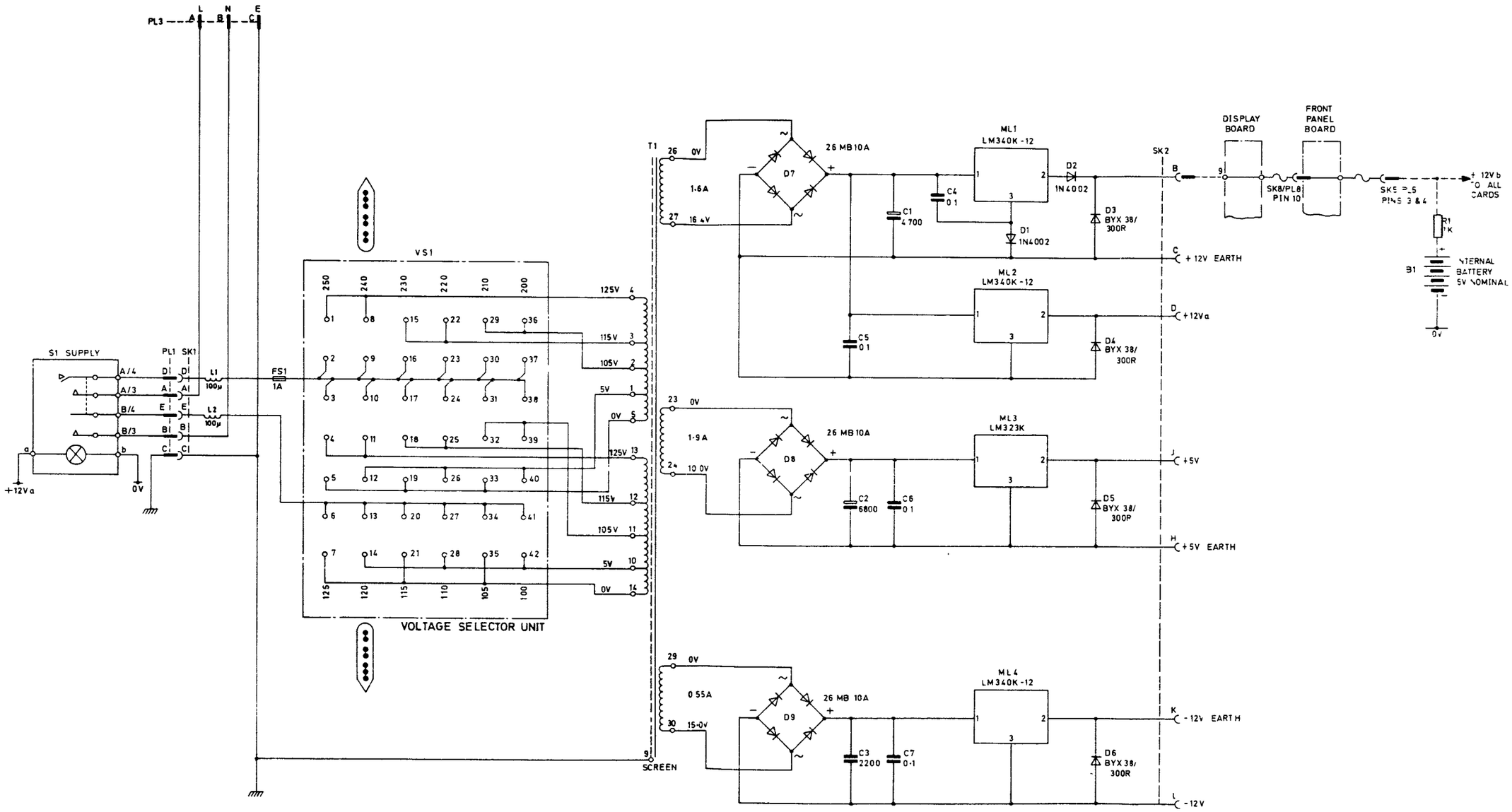
BATTERY SUPPLY

5. The +12V output from ML1, at SK2 pin B, is applied to the battery via links on the display driver and front panel boards, SK5/PL5 and resistor R1 (mounted on the mother board). The nickel cadmium battery has a capacity of 70 mA/hours; since between 0.5 mA and 1.0 mA is drawn from the battery when the MA.1090 is switched off or during a supply failure, the battery is fully discharged in approximately 70 hours. The battery is then re-charged in a few hours when the power is restored.

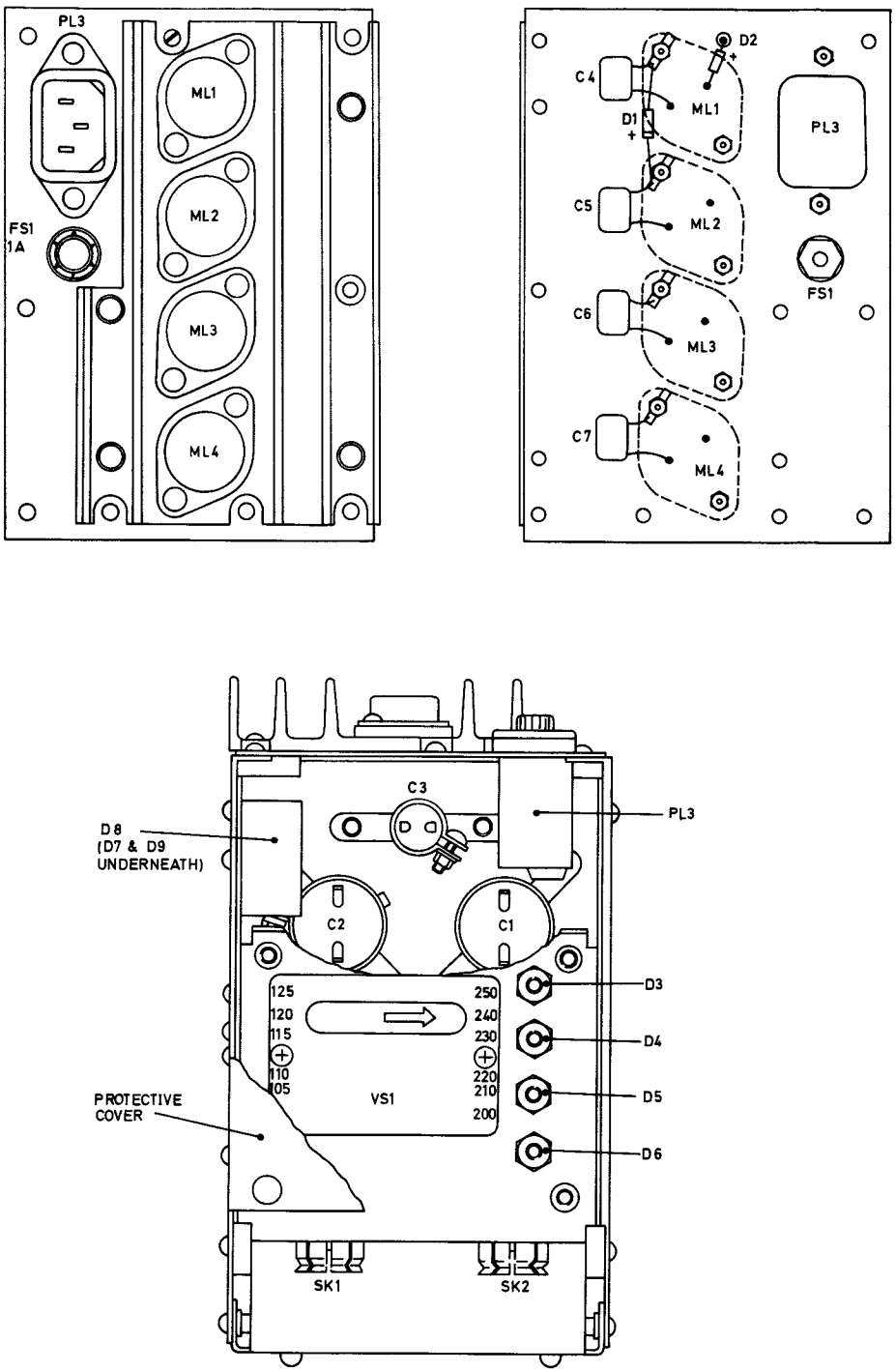
6. Since the current drain from the battery is very low, the life of the battery is approximately the same as its shelf life, and it should be replaced at two-yearly intervals (one-year intervals in critical situations).

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number	Manufacturer
		POWER SUPPLY MODULE MS685 (ST 77047)				
Capacitors			Volts			
C1	4700	Electrolytic	40	+50 -10	922804	Mullard 071-17472
C2	6800	Electrolytic	25	+50 -10	924979	Mullard 071-16682
C3	2200	Electrolytic	25	+50 -10	917962	Mullard 071-16222
C4	0.1	Polycarbonate	160	20	932055	Ashcroft A2 B1015A
C5	0.1	"	160	20	932055	"
C6	0.1	"	160	20	932055	"
C7	0.1	"	160	20	932055	"
Transformers						
T1		Sypply transformer			CT77219	Racal
Diodes						
D1		Silicon			911460	STC 1N4002
D2		Silicon			911460	STC 1N4002
D3		Recitifer			912407	Mullard BYX38/300R
D4		Rectifier			912407	Mullard BYX38/300R
D5		Rectifier			912407	Mullard BYX38/300R
D6		Rectifier			912407	Mullard BYX38/300R
D7		Bridge rectifier			930088	IR 26MB-10A
D8		Bridge rectifier			930088	IR 26MB-10A
D9		Bridge rectifier			930088	IR 26MB-10A

Cct. Ref.	Value	Description	Rate	Tol. %	Racal Part Number	Manufacturer
Integrated Circuits						
ML1		Voltage regulator			923014	National LM340K12
ML2		Voltage regulator			923014	National LM340K12
ML3		Voltage regulator			927558	National LM323K
ML4		Voltage regulator			923014	National LM340K12
Fuses						
FS1	1A	Anti-surge			922456	Belling Lee L2080/1
		Fuse Holder			922465	Belling Lee E6011B
Connectors						
PL3		Plug, 3-way filtered entry			928477	Belling Lee L2133B/S
		Mating socket			928266	Belling Lee L1497
Earlier version:						
		Plug 3-way			915655	Amphenol (62GB57A-8-3.3P)
		Mating socket			919694	Amphenol (62GB56T-8-3.3S)
		Clamp, strain relief			920884	Amphenol (62GB585-8-35
SK1		Socket, 5-way			928267	Pye BMA/5/S/N/SS
		Mating Plug			928268	Pye BMA/5/P/SW/M5H
SK2		Socket, 10-way			925690	Pye M10/S/N/LR
		Mating Plug			928270	Pye M10/PSW/M5H
Miscellaneous						
VS1		Voltage selector			906385	McMurdo B279002/A
B1		Battery			927407	GE W115/5006



Circuit : Power Supply Module MS685 Fig.15.1



Component Layout
Power Supply Module MS685

Fig.15.2

CHAPTER 16

MOTHERBOARD

CONTENTS

	Para.
INTRODUCTION	1
EXTERNAL CONNECTIONS	2
COMPONENTS LIST	

ILLUSTRATIONS

	Fig.
Circuit: Motherboard	16.1
Layout: Motherboard	16.2

CHAPTER 16

MOTHERBOARD

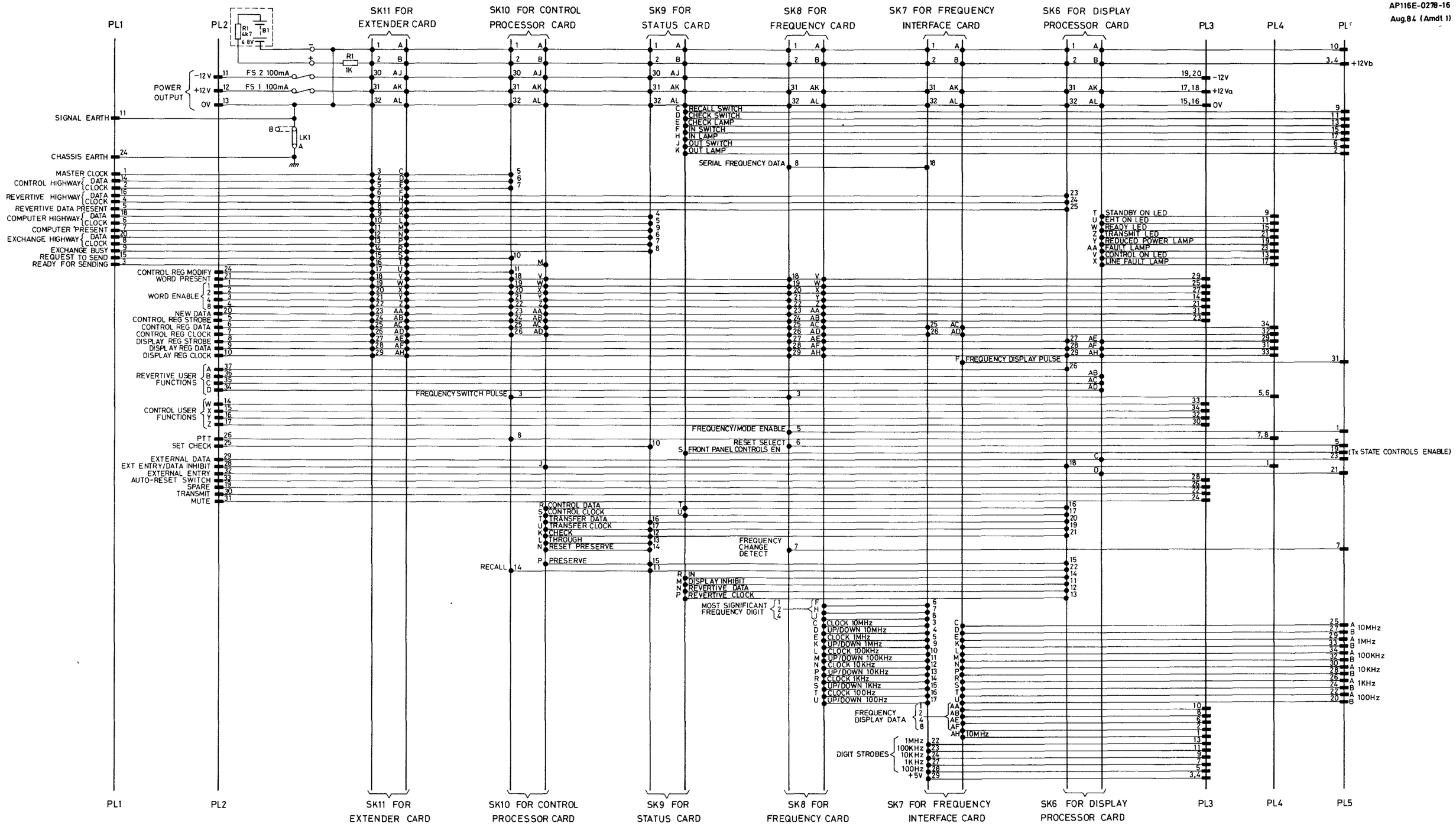
INTRODUCTION

1. The motherboard is mounted on the base plate of the control unit and accommodates, in edge connectors, the five printed circuit cards and the extender card. Also attached to the motherboard are the two multi-way plugs, PL1 and PL2 (which protrude through apertures in the rear panel), to which the external connections are made, two 100 mA fuses for the externally available plus and minus 12V supplies, and the earth link LK1. The circuit of the motherboard is given in fig. 16.1 , the layout is given in fig. 16.2.

EXTERNAL CONNECTIONS

2. The external connections to the MA.1090 are made via the 25-way plug PL1 and the 37-way plug PL2 at the rear of the unit. The connections required are dependent on the particular installation and reference should be made to the appropriate systems manual. The connections to PL1 and PL2 are given in Tables 1 and 2, Chap. 2.

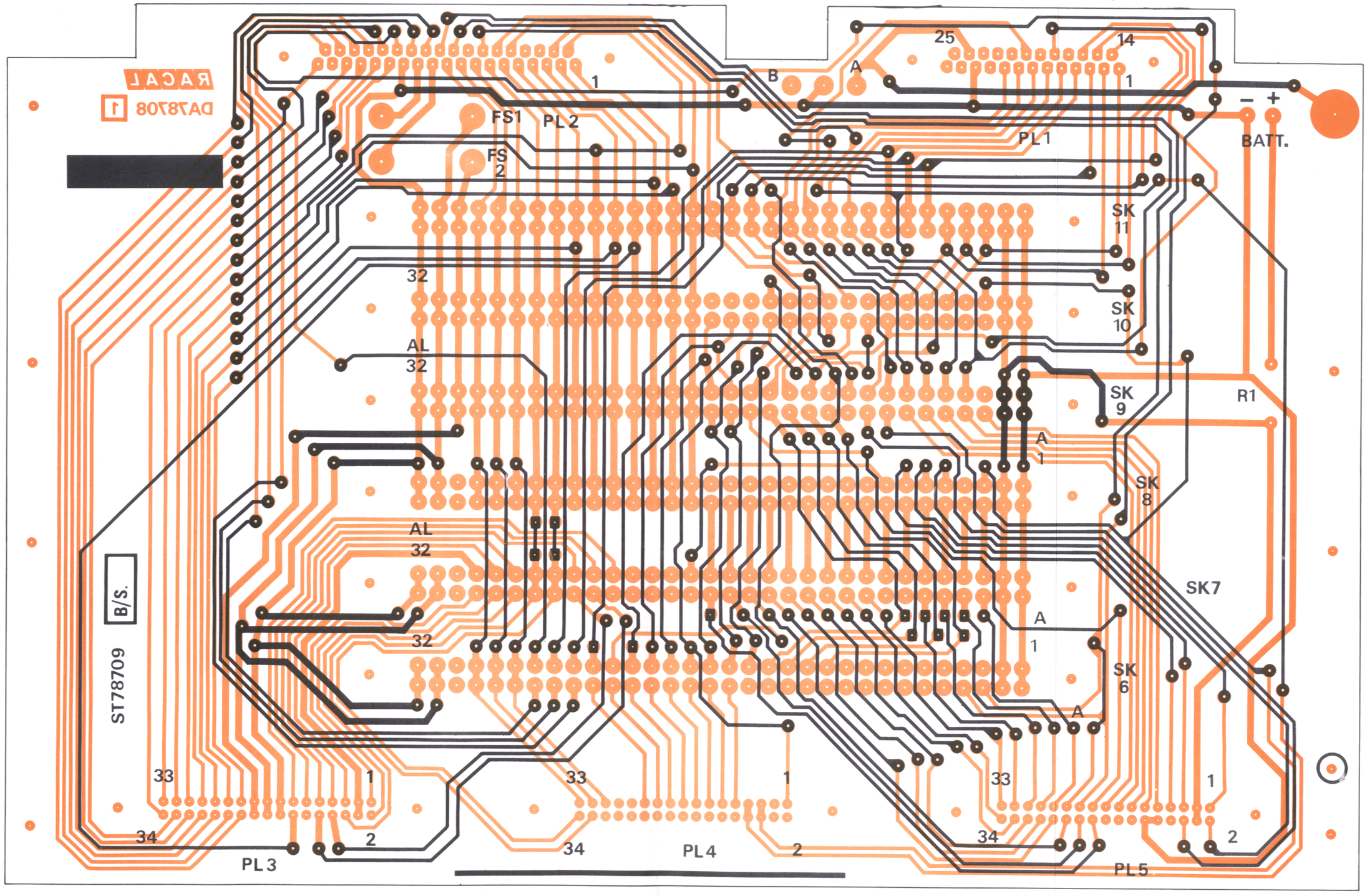
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number	Manufacturer
		MOTHERBOARD (ST 78709)				
Resistors						
R1	1k	Metal Oxide		2	913489	Electrosil TR4
Fuses						
FS1	100mA	Fuselink size 00			915348	Belling Lee L754
FS2	100mA	Fuselink size 00			915348	Belling Lee L754
		Fuseholder			908352	Belling Lee L1383
Connectors						
PL1		Plug, 25-way			928763	Cannon DB25P11BON
		Mating socket			915970	Cannon DB25S
		Shell junction			914299	Cannon DB51213-1
		Retainer			914245	Cannon DB51221-1
PL2		Plug, 37-way			928764	Cannon DC37P-1BON
		Mating socket			915656	Cannon DC37S
		Shell junction			918105	Cannon DC51215-1
		Retainer			914246	Cannon DC51222-1
PL3		Plug, 34-way			927794	3M's 3431-2003
PL4		Plug, 34-way (modified)			AD77779	Racal
PL5		Plug, 34-way			927794	3M's 3431-2003
SK6		Edge connector, 64-way			929985	Ferranti EWD/32/32/F
SK7		Edge connector, 64-way			929985	Ferranti EWD/32/32/F
SK8		Edge connector, 64-way			929985	Ferranti EWD/32/32/F
SK9		Edge connector, 64-way			929985	Ferranti EWD/32/32/F
SK10		Edge connector, 64-way			929985	Ferranti EWD/32/32/F
SK11		Edge connector, 64-way			929985	Ferranti EWD/32/32/F
LK1		Shorting Plug			927090	Cambion 461-2871-02-03-12



RACAL
WOH8307 | DC78709
1

Circuit : Mother Board

Fig.16-1



RACAL

WOH 8307	DA 78708	16.2
1		1/2
WOH 8307	DA 78707	16.2
1		2/2

Layout: Mother Board

Fig. 16.2

CHAPTER 17

PARTS LIST

PREFACE

This chapter gives parts list information for assemblies and chassis mounted components. Detailed components lists for the printed circuit boards and assemblies are given at the end of the respective chapters.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number	Manufacturer
CHASSIS MOUNTED COMPONENTS						
B1		Battery			927407	KPP Products W115/5006
Spare Fuses						
1A	1A	Anti-surge			922456	Belling Lee L2080/1
	100mA	Size 00			915348	Belling Lee L754
Miscellaneous						
		Lamp screen remover			925712	Highland 02-905
		Lamp remover			925713	Highland 02-906
		Push-bit plastic feet			921253	Moulded Fastener 0350-3718
		Knob, FREQUENCY/			927731	Sifam K210250
		Knob cap			927734	Sifam C210
ASSEMBLIES						
Power supply module MS685 (Chap.15)					ST77047	Racal
Motherboard (Chap.16)					ST78709	Racal
Display Processor Card (Chap.14)					ST78707	Racal
Frequency Card (Chap.10)					ST78703	Racal
Frequency Interface Card (Chap.11)					ST78705	Racal
Status Card (Chap.13)					ST77321	Racal
Control Processor Card (Chap.12)					ST77324	Racal
Extender Card					ST77326	Racal
Front Panel Assembly (Chap.8)					ST78721	Racal
Comprising:						
		Front Panel Board			ST78711	Racal
		Switch Board			ST78713	Racal
		Display Board			ST78715	Racal

ALTERNATIVES

Certain recommended alternative components are listed below. These alternative components may be used when the appropriate item given in the components list is no longer available.

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number	Manufacturer
MOTHERBOARD (Chap.16, Components 1)						
SK6 - SK11		Edge connector, 64 - way			929985	Ferranti EWD32/32FT