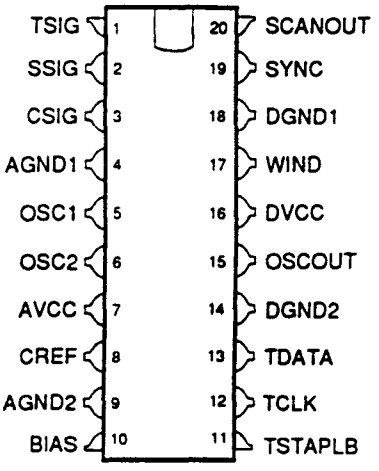
TEXAS INSTRUMENTS

Consumer Products Family

Teletext DATA SLICER CF72306

TELETEXT DATA SLICER CF72306

- **Forms a custom 2-chip solution when used with an ASICTEXT decoder**
- **Low power 1μm CMOS (<100mW)**
- **Standard 20 pin/300mil package**
- **Tolerates a range of video distortions**
- **Operates with 13.875 MHz fundamental mode crystal**



CF72306
20-PIN/300 Mil N PLASTIC

description

The CF72306 is a new device comparable with the CF72303 data slicer currently in production by TI. The CF72306 teletext data slicer is the analogue component of the Texas Instruments (TI) teletext system. The TI teletext system is a two-chip solution to the teletext function and comprises a data slicer and a digital decoder.

The data slicer performs the functions of composite sync separation, teletext data extraction and data clock regeneration from the received video signal and passes clock, data and composite sync signals to the digital decoder chip.

The CF72306 data slicer has the following features that distinguish it from the CF72303 data slicer:

(a) The sync-separator slicing level is adaptive so that it can operate with a range of video amplitudes and signal distortions.

(b) The data-slicer uses an adaptive signal recognition and clock-phasing algorithm so that it can operate with a wide range of clock run-in amplitudes.

(c) The external 55.500MHz third overtone-mode crystal has been changed to a 13.875MHz fundamental mode crystal with the specification given below.

13.875MHZ Crystal Specification

- Oscillation Mode ..... Fundamental Parallel
- Frequency 13.8750MHz
- Crystal Frequency Stability ..... ±150ppm *
- Maximum Crystal ESR (steady-state) ..... 60 Ohms
- Maximum Crystal ESR (start-up) ..... 120 Ohms
- Maximum Shunt Capacitance ..... 7 pF
- Maximum Motional Capacitance ..... 30 fF
- Crystal Load Capacitance ..... 18 pF
- Free Air OperatingTemperature Range ..... 0 to 70 °C
- Drive Level ..... 1mW max.
- Ageing ..... ±5ppm max for first year

* Includes temperature stability and manufacturing tolerance.

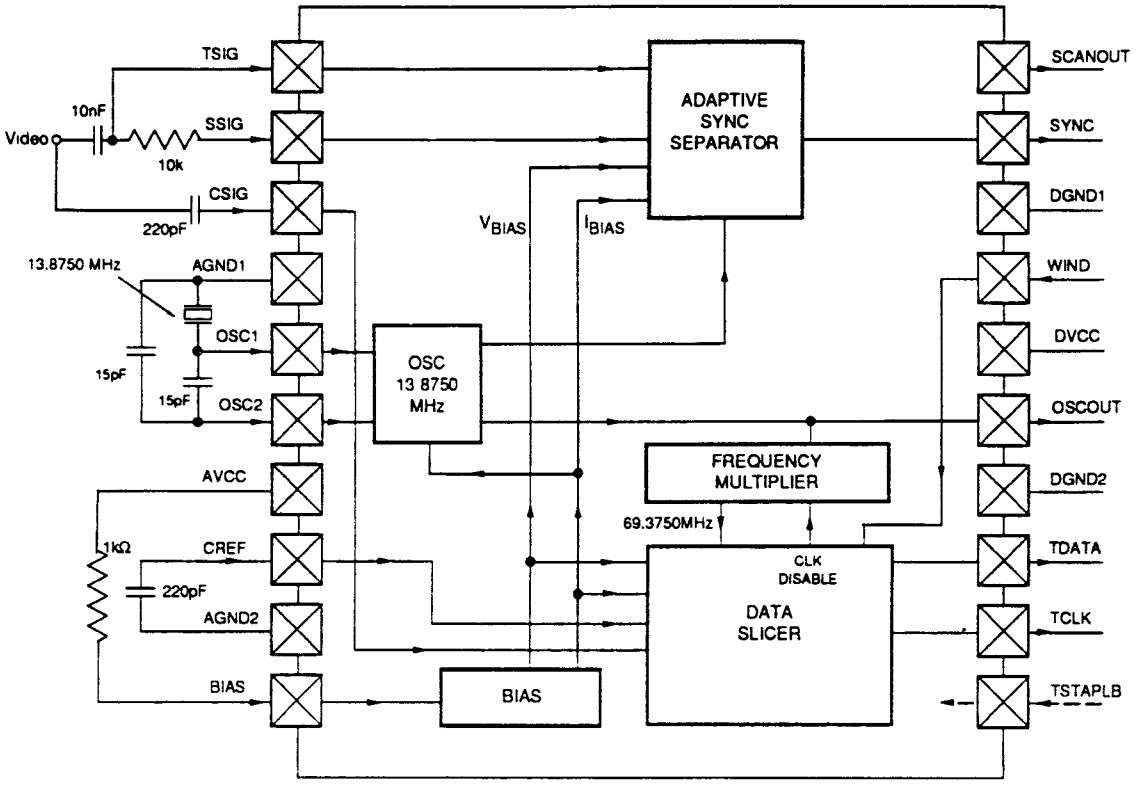


Fig. 1: CF72306 Internal Block Diagram

An internal block diagram of CF72306 is shown in Fig. 1 above.

pin description

PIN	SIGNAL	DESCRIPTION	I/O	TYPE
1	TSIG	Video Sync Input 1	I	Analogue
2	SSIG	Video Sync Input 2	I	Analogue
3	CSIG	Video Data Input	I	Analogue
4	AGND1	Analogue Ground		Power
5	OSC1	13.875 MHz Oscillator	I	Analogue
6	OSC2	13.875 MHz Oscillator	I	Analogue
7	AVCC	Analogue Vcc		Power
8	CREF	Video Data Reference Input	I	Analogue
9	AGND2	Analogue Ground		Power
10	BIAS	Internal Reference	I	Analogue
11	TSTAPLB	Test/Application	I	Digital
12	TCLK	Teletext Clock	O	Digital
13	TDATA	Teletext Data	O	Digital
14	DGND2	Digital Ground		Power
15	OSCOUT	Oscillator Output	O	Digital
16	DVCC	Digital Vcc		Power
17	WIND	Timing Signal	I	Digital
18	DGND1	Digital Ground		Power
19	SYNC	Separated Sync Output	O	Digital
20	SCANOUT	Test Scan Output	O	Digital

Signal pins = 14 Power pins = 6

Composite video input description

The composite video input to the CF72306 has the following form in the nominal case.

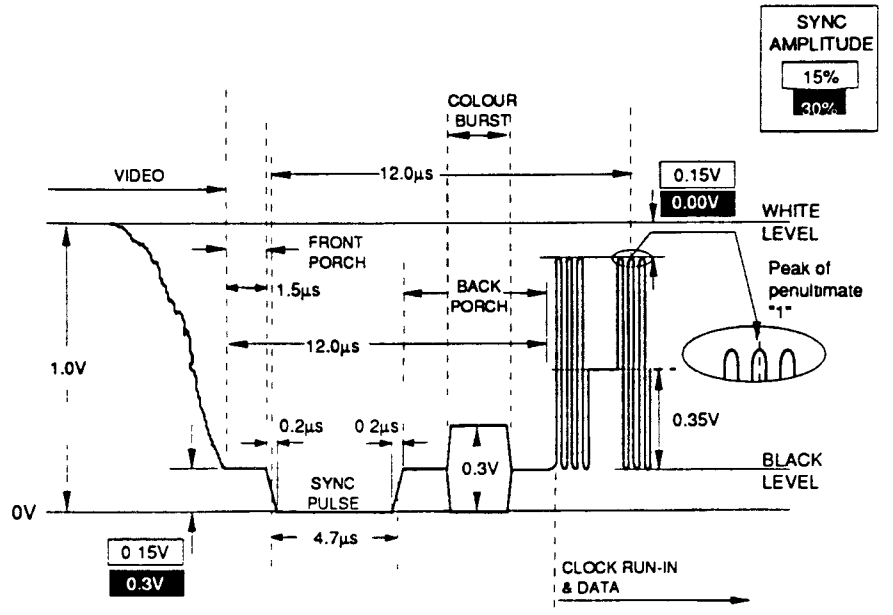


Fig 2.1: Nominal Composite Video

The composite video input to the CF72306, when subject to the worst case amplitude tolerances resulting from both low and high frequency distortions, has the forms shown in the following four diagrams. Parameter values are shown in Table 2.2.

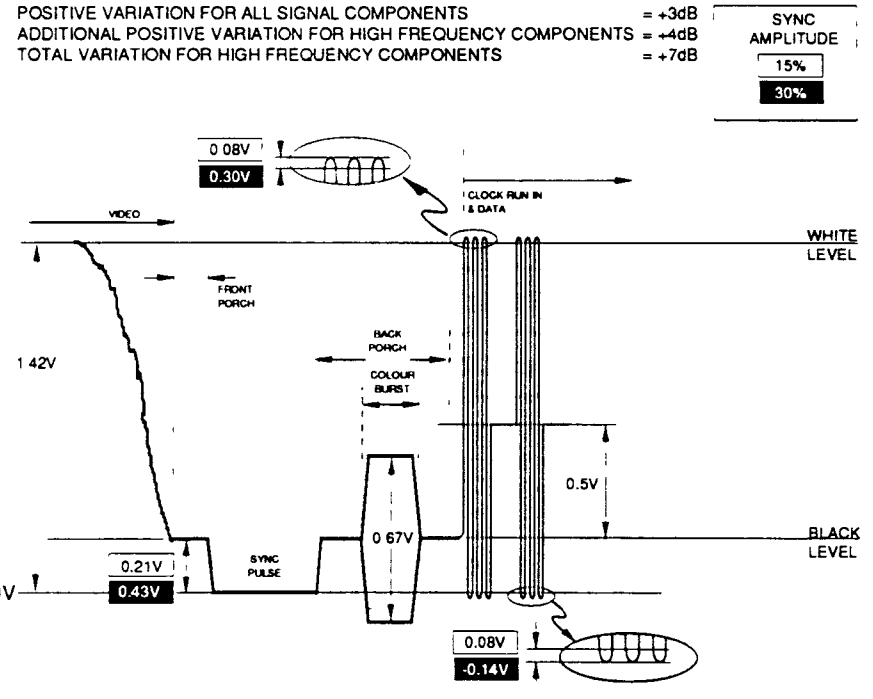


Fig 2.2: Worst Case Composite Video Waveform with conditions as given at top of diagram

Composite video input description-continued

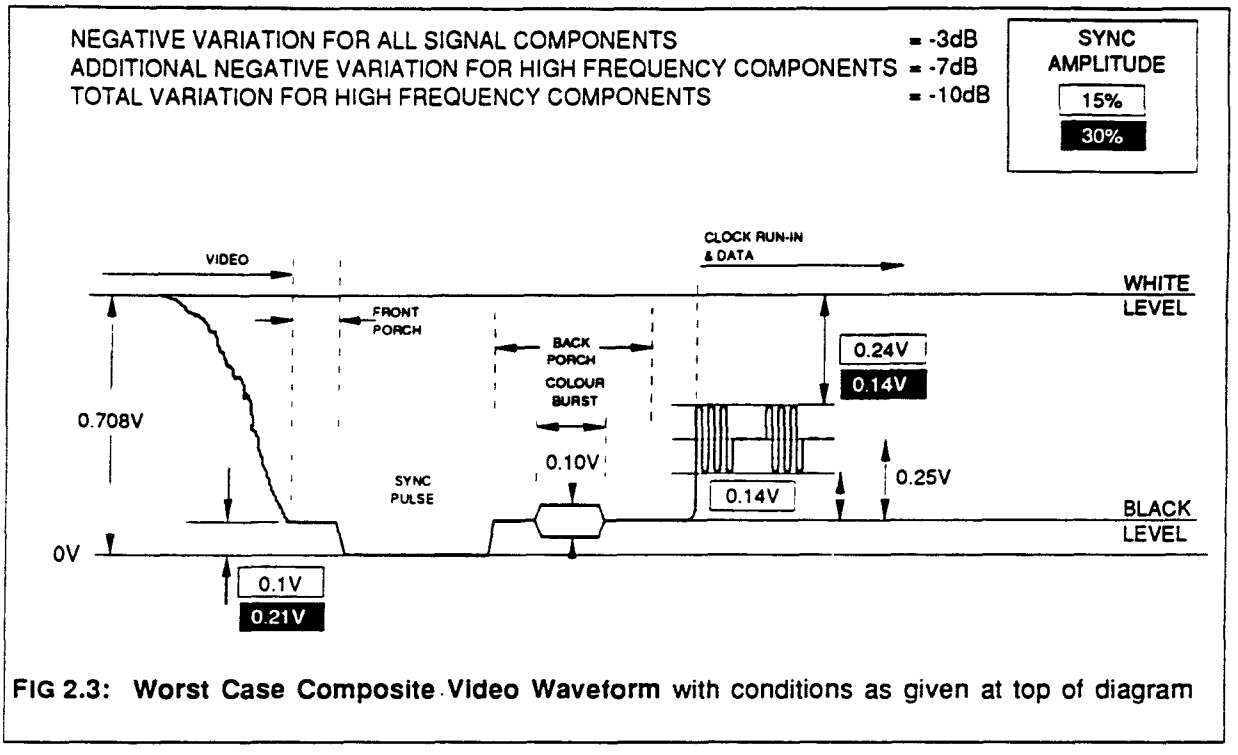


FIG 2.3: Worst Case Composite Video Waveform with conditions as given at top of diagram

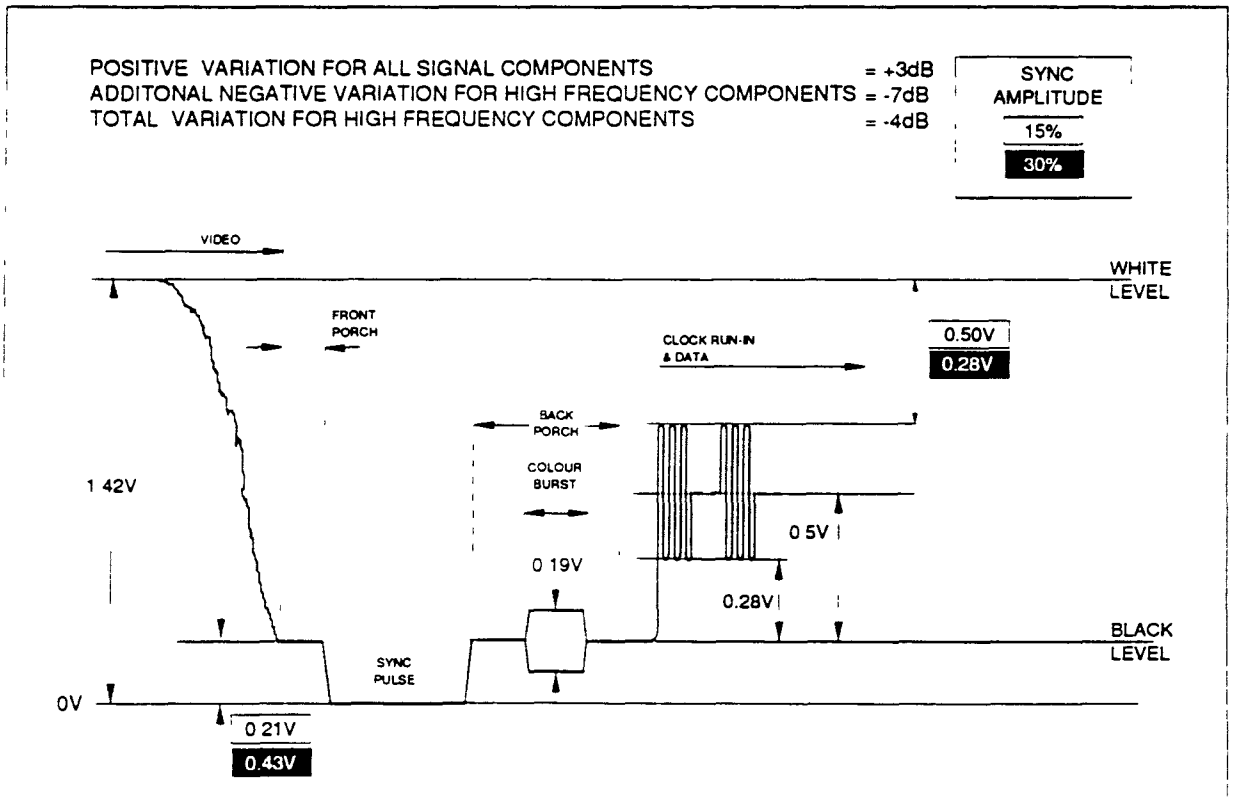


Fig 2.4: Worst Case Composite Video Waveform with conditions as given at top of diagram

Composite video input description-continued

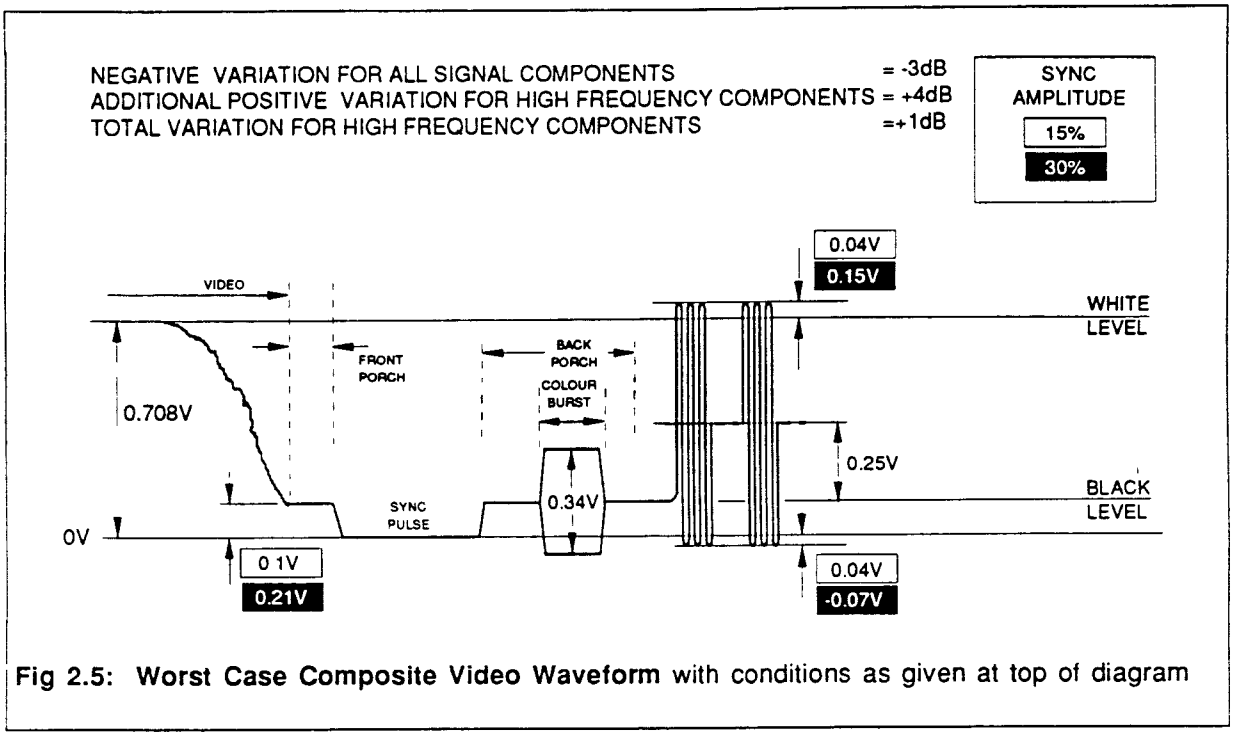


Fig 2.5: Worst Case Composite Video Waveform with conditions as given at top of diagram

The composite video input to the CF72306 has the following timing specification All amplitudes in this figure have nominal reference values as shown in Figure 2.1.

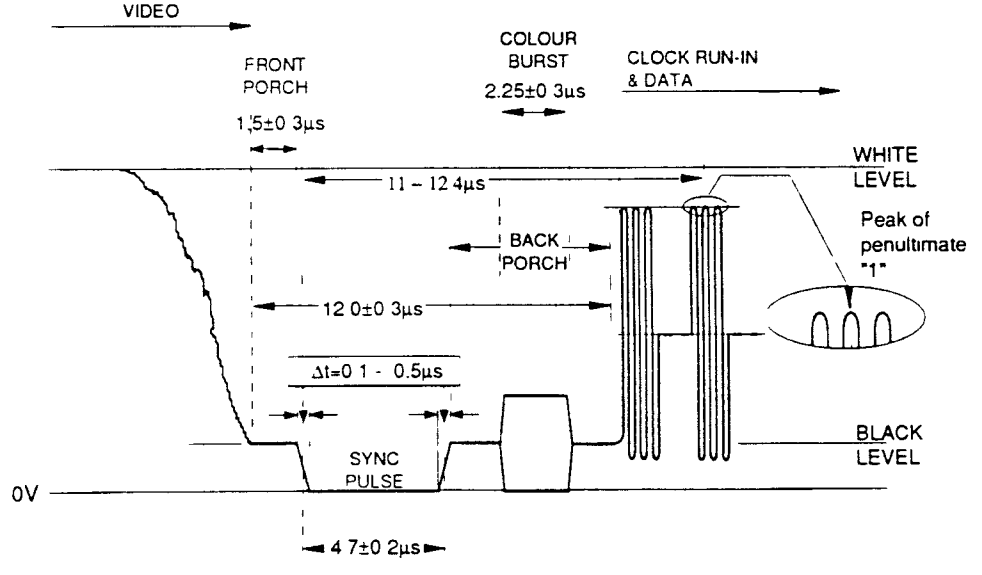


Fig 2.6: Composite Video Timing Information

VIDEO INPUT SPECIFICATION

PARAMETER	MINIMUM	NOMINAL	MAXIMUM	UNIT	Notes
Composite Video Amplitude (peak-to-peak)	0.708	1.0	1.42	V	
Source Impedance	-	-	350	Ω	
Sync Amplitude	10	-	43	% Nominal video	1
Sync Duration	4.5	4.7	4.9	µs	2
Sync Transition Times	0.1	0.2	0.5	µs	3
Front Porch	1.2	1.5	1.8	µs	
Under/Overshoots	-	-	20	% Nominal Video	4
Time between -ve sync & penultimate '1' of Clock Run-in	11	12	12.4	µs	5
Line Blanking	11.7	12.0	12.3	µs	6
Colour Burst Amplitude (peak-to-peak)	9	30	67	% Nominal video	
Colour Burst Frequency	-	4.43	-	MHz	
Colour Burst Duration	1.95	2.25	2.55	µs	
Clock Run-in Amplitude	22	70	157	% Nominal video	7
Number of Complete & Consecutive Clock Run-in cycles	5	-	8		8
Bit rate	6.9373	6.9375	6.9377	Mbps	
Data "one" level	19	66	161	% Nominal video	
Data "zero" level	-6	0	6	% Nominal video	9

Note 1: Minimum value is: low frequency -3dB and 15% sync.
Maximum value is: low frequency +3dB and 30% sync.

Note 2: As measured at 50% of the total sync amplitude.

Note 3: As measured at 10% and 90% of the total sync amplitude.

Note 4: Under/Overshoots are of order 100ns duration.

Note 5: As measured at 50% of the negative sync transition and the peak of the penultimate "1".

Note 6: As measured at 50% of the negative and positive edges of adjacent peak white components which are respectively before and after a sync pulse.

Note 7: Clock Run-in envelope - Raised cosine filter with centre frequency at 3.46875MHz. Skew-symmetrical about 0.5 x bit-rate and substantially reduced at 5MHz.

Note 8: A clock run in cycle is complete if it's amplitude equals or exceeds 22% of composite video.

Note 9: With the black level as a zero reference.

TABLE 2.1.

absolute maximum ratings

Supply Voltage, Vcc 6.5V
Input Voltage ..... Vcc + 0.5V
Current Any signal pin ..... ±20mA
Current Vcc or GND ..... ±50mA
Operating free air temperature range ..... 0°C to 70°C
Storage Temperature range ..... -65°C to 150°C
Thermal Resistance θja ..... 150°C/W

recommended operating conditions

Symbol	Parameter	Test Conditions	min	nom	max	unit
V_{cc}	Supply Voltage	V_{ih}=min V_{il}=max	4.5	5.00	5.5	V
V_{ih}	High Level Input Voltage	WIND	0.7V_{cc}		V_{cc}	
V_{il}	Low Level Input Voltage	WIND			0.2V_{cc}	
I_{ih}	Input Current High	WIND,OSC1,OSC2,TSTAPLB V_{cc}=max BIAS 1KΩ to V_{cc}	 -1		 +1	 µA
I_{il}	Input Current Low	WIND,OSC1,OSC2,TSTAPLB V_{cc}=max BIAS 1KΩ to V_{cc}	 -1		 +1	 µA
f_o	Operating Freq.			13.8750(*)		MHz
V_{oh}	Output Voltage High	TCLK, TDATA, SYNC, OSCOUT (Note 1) V_{cc}=min I_{oh}=30µA =300µA =3mA	 V_{cc}-100mV V_{cc}-200mV 3.76			 V
V_{ol}	Output Voltage Low	TCLK,TDATA, SYNC, OSCOUT (Note 1) V_{cc}=min I_{ol}=30µA =3mA			 100 500	 mV mV

(*) 2 X (Teletext data rate - 6.9375 MHz)

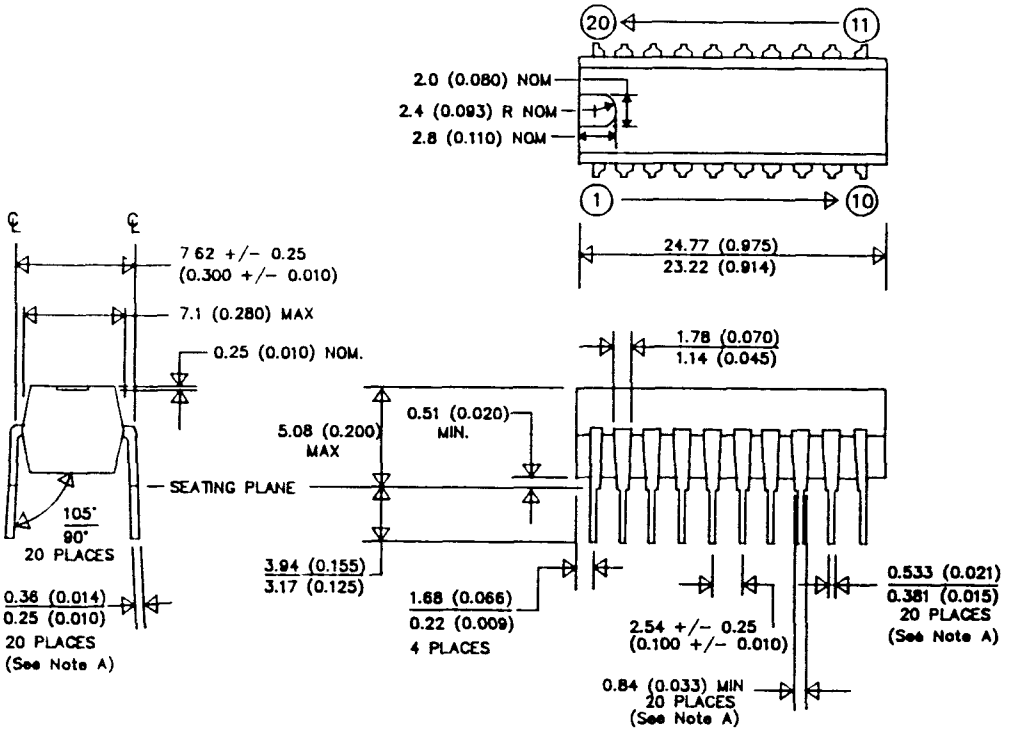
Note 1: It is recommended that PCB track capacitance on OSCOUT should not exceed 22pF.

Note 2: It is recommended that PCB track capacitance on TCLK and TDATA should not exceed 33pF.

20-Pin Plastic Dual-In-Line Package

(20-Pin N Plastic)

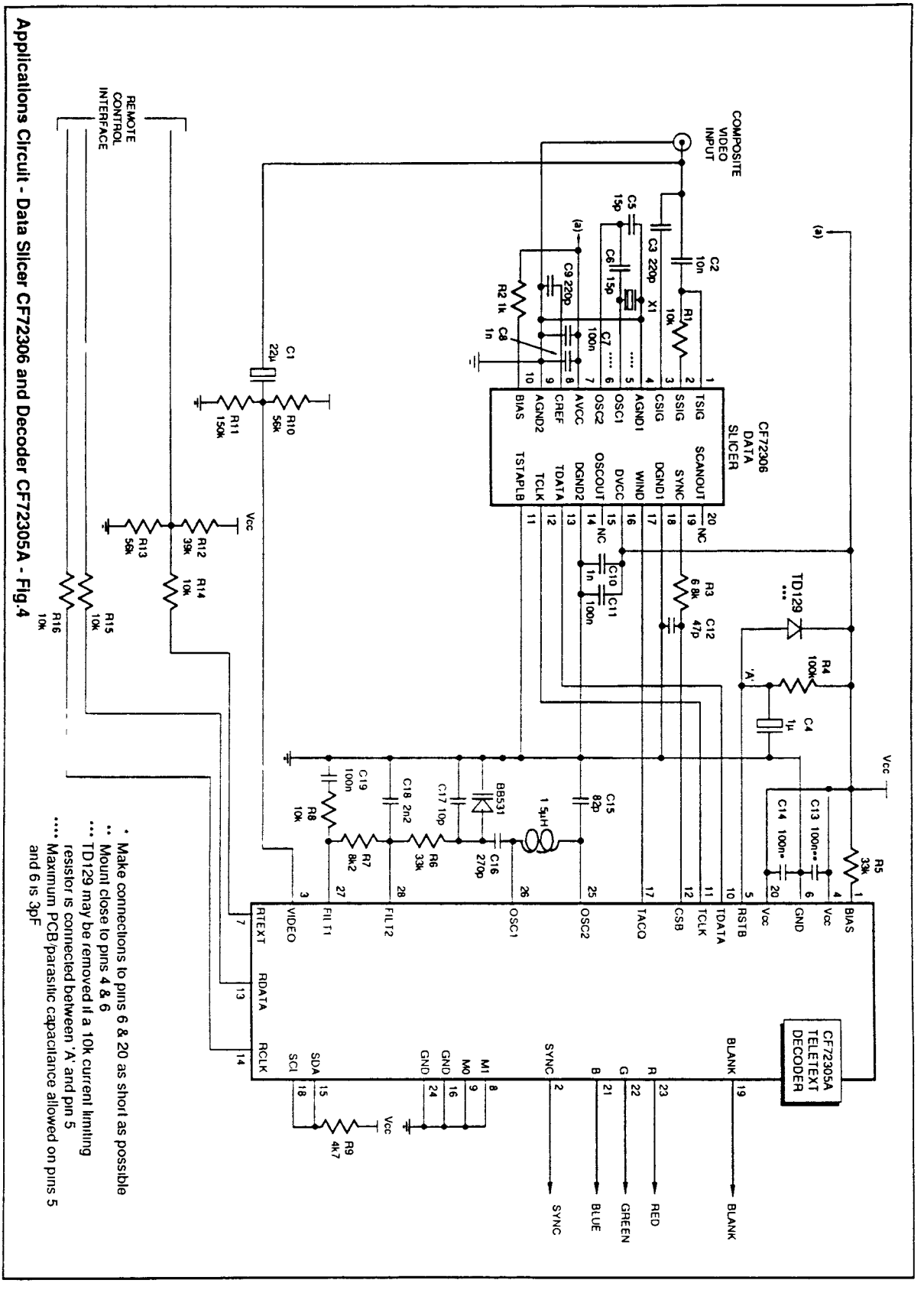
Dimensions in millimetres(inches)



NOTE : A This dimension does not apply for solder-dipped leads.

Fig. 3:

applications information



Applications Circuit - Data Slicer CF72306 and Decoder CF72305A - Fig.4

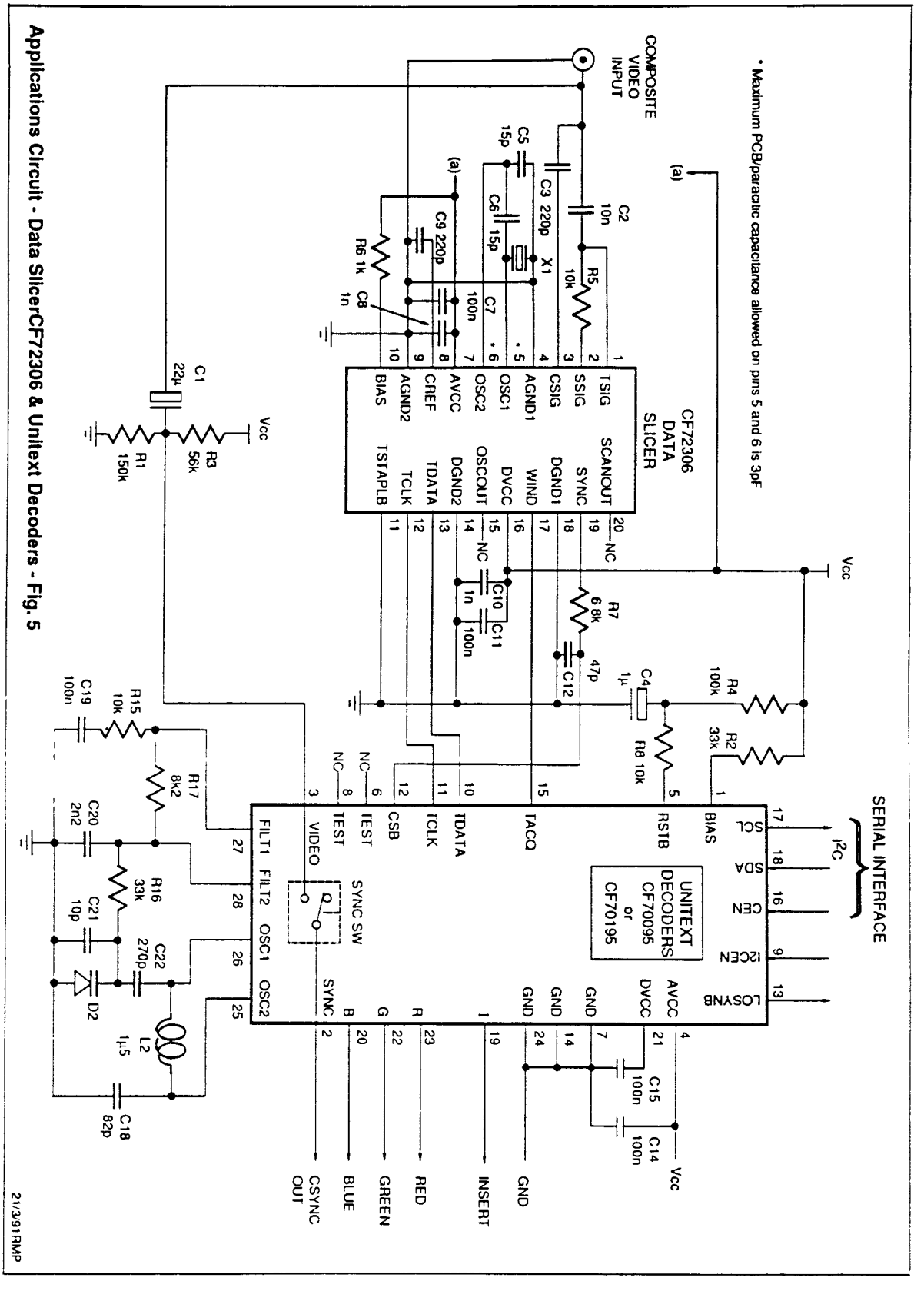
* Make connections to pins 6 & 20 as short as possible

** Mount close to pins 4 & 6

*** TD129 may be removed if a 10k current limiting resistor is connected between 'A' and pin 5

**** Maximum PCB parasitic capacitance allowed on pins 5 and 6 is 3pF

applications information-continued



Applications Circuit - Data SlicerCF72306 & Unitext Decoders - Fig. 5

Supplementary Applications Information (required for stand-alone applications)

The following information will be required when the Data Slicer is not used in conjunction with a Texas Instruments single or multi-page teletext decoder:-

1. TDATA and TCLK outputs are static low when WIND input is static low or when the VIDEO input contains invalid teletext clock run in data.
2. Phase Relationship Between TDATA and TCLK signals

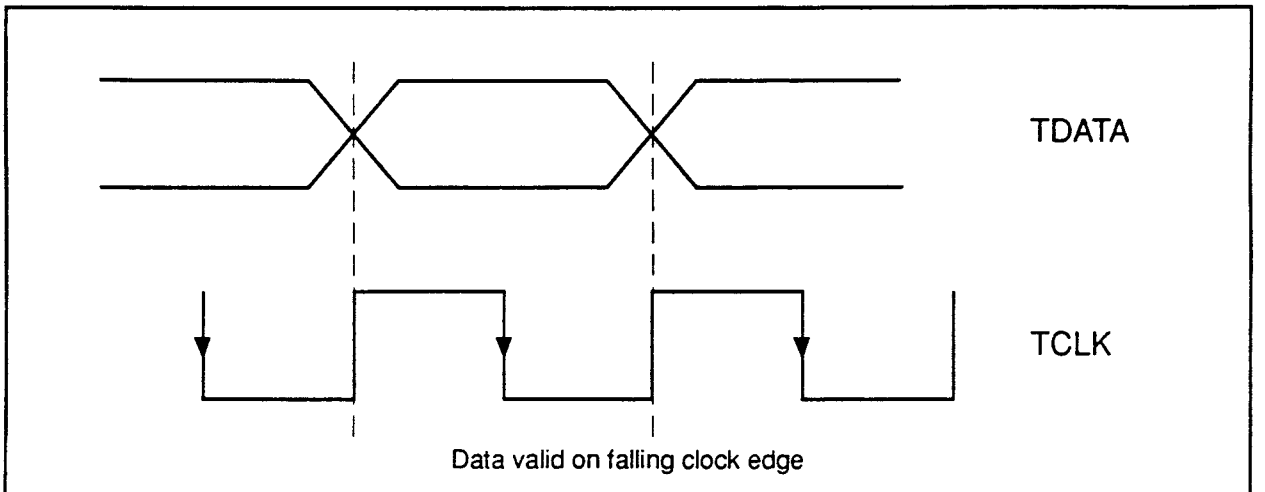


Fig.6: TDATA and TCLOCK Timing

3. Window Signal Timing

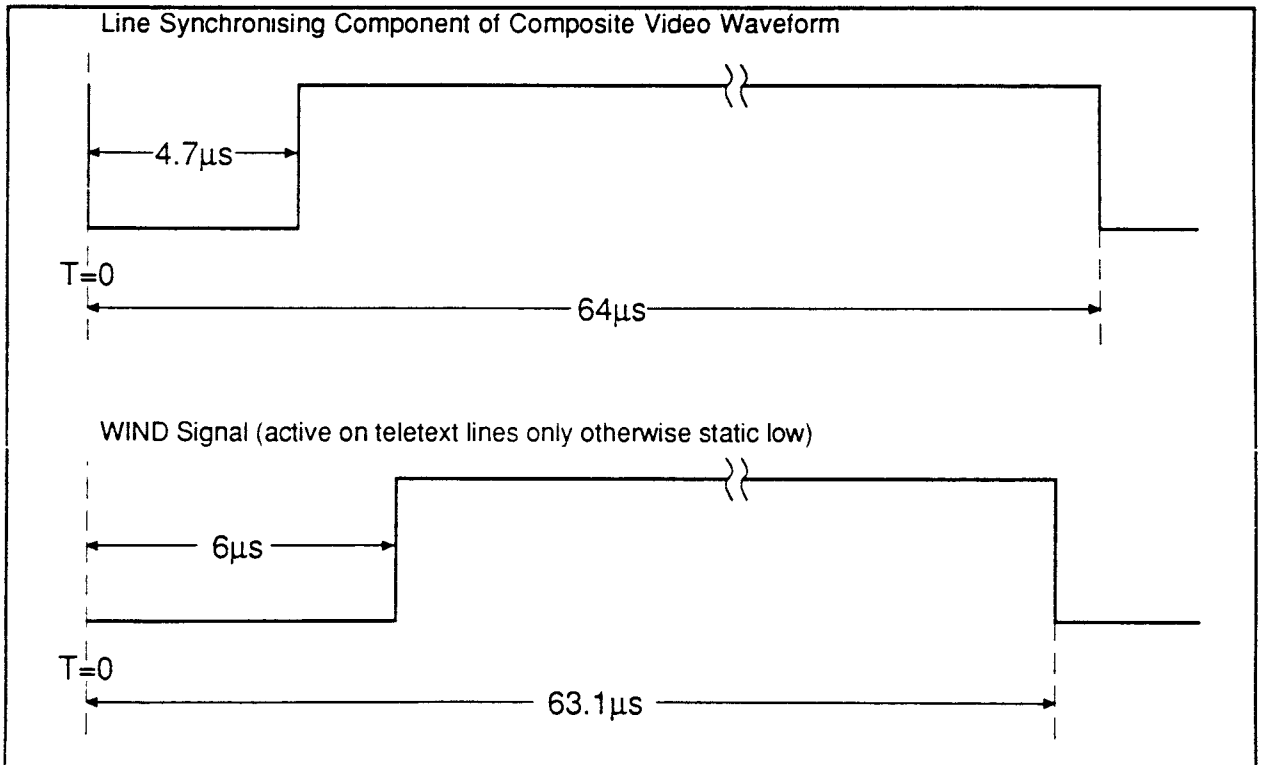


Fig.7: Window Signal Timing

Notes:-

1. T=0 Above can be coincident with or up to 1.5µs later than negative video line SYNC edge.
2. All timings may sustain a tolerance of +/- 5%

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