TEXAS INSTRUMENTS

Consumer Products Family

Universal Teletext Decoders 'UNITEXT' CF70095 & CF70195

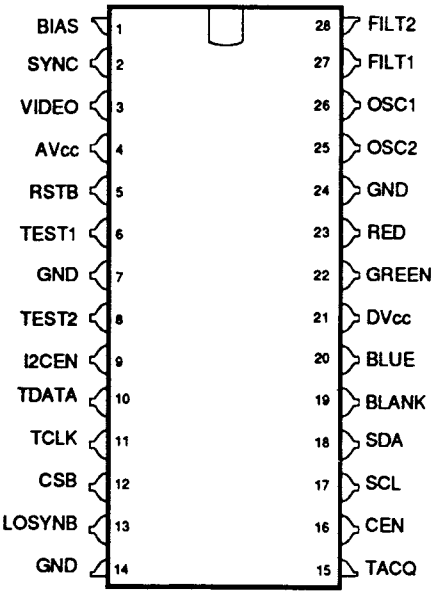
This revision replaces 4Q/91 release

CONTENTS

CHANGES

This release, 1Q/92, of CF70095/70195 datasheet contains revised values for the Iol and Vol perameters for the following signals:- LOSYNB, TACQ, SCL, SDA, BLUE, RED, GREEN, SYNC, BLANK and CEN. (See page 9).

- **Europe-wide solution**
- **Built-in "intelligent" teletext processing**
- **Single page on-chip display RAM**
- **I²C or simple serial interface control options**
- **Full level 1.5 Spanish language processing**
- **Full screen on-screen-display capability**
- **Automatic ghost row processing (Packets 8/30,X/26,X/27)**
- **Packet 8/30 status display**



- **Advanced 1µm CMOS Technology**

1.DESCRIPTION

The CF70095 and CF70195 UNITEXT devices are single-page "intelligent" teletext decoders. When used with an Analogue Interface device (Texas Instruments' CF72308 or CF72306), they provide a flexible teletext solution covering the following European languages :-

CF70095	CF70195
English	English
German	Polish
Swedish/Finnish/Hungarian	Czechoslovakian
Italian	German
French	Swedish/Finnish/Hungarian
Spanish (including automatic packet 26 processing)	Serbo-Croat

The UNITEXT devices have an on-chip micro-coded processor which takes care of all teletext processing requirements, including the ghost row processing. Control of their operation is done at a high level using simple commands.

In addition to its teletext capability, the UNITEXT decoders can be used for locally generated on-screen-display. The extent of the display is under the control of the TV microprocessor and may use the complete teletext screen of 25 rows of 40 characters. The screen display may use any of the teletext alphanumeric symbol and graphics characters (including all the national language characters).

A further OSD mode is available which permits messages of up to 22 characters to be displayed at the same time that the stored teletext page is being updated.

1.DESCRIPTION

External control of the UNITEXT is via either an I²C slave transceiver or a simple serial interface.

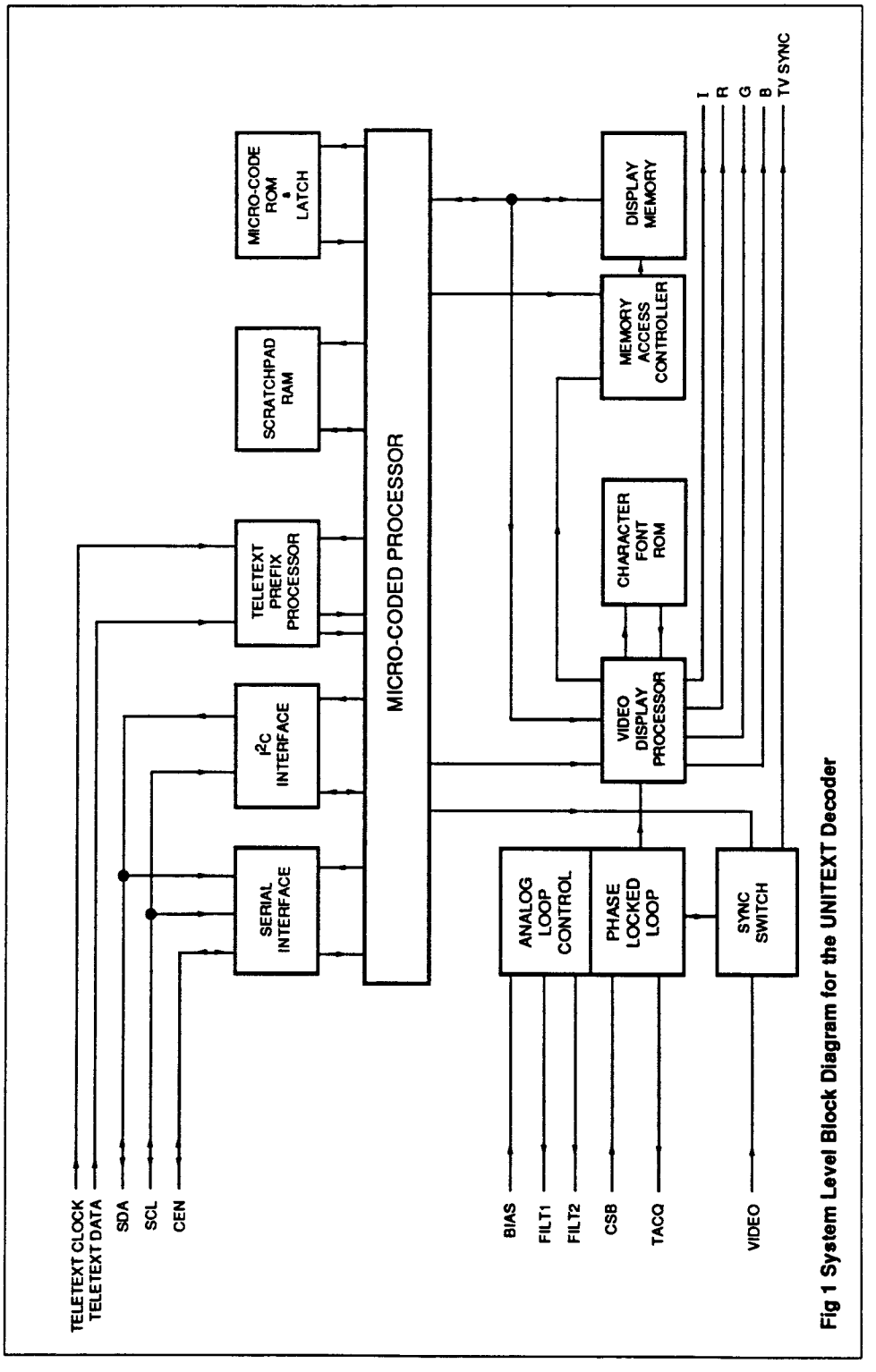


Fig 1 System Level Block Diagram for the UNITEXT Decoder

1.DESCRIPTION-continued

It is possible to read status information and received teletext data via the I^2C bus. For example, the C12, C13, C14 language bits can be read from a teletext header to ascertain in what language locally generated messages should be displayed.

In the UNITEXT decoder, serial clocked teletext data from the Analogue Interface is made available in parallel form by the prefix processor - see Figure 1. Under the control of the micro-coded processor, the prefix processor can check the parallel data for parity errors and perform Hamming code error detection and correction. Corrected data is then passed on to the processor which operates at 11 MIPS and allows real time processing of the teletext data under microcode control. Because only a small amount of fixed hardware processing is done, great flexibility in handling of the data packets is possible and sufficient spare processing capacity exists for non-teletext functions such as a full-screen on-screen display capability.

The memory access control routes the data from the teletext controller into the display memory and arbitrates memory access requests from the controller and the video display processor(VDP).

The character font ROM holds the required fonts in 10 X 12 pixel format. An RGB output is produced according to serial control display attributes along with a BLANK(fast blanking) signal which allows the display to be viewed in modes TEXT, MIX or BOX(subtitle/newsflash).

All system timing functions are produced in the PLL & TV sync timing block including the 11MHz display pixel clock. The display sync signals generated are flexible and can be software controlled to provide non-interlaced text displays with locked or unlocked field sync.

2.PIN DESCRIPTION

Pin1 - BIAS

Sets the internal bias for the chip. A 33k resistor should be connected from Pin 1 to Vcc.

Pin 2 - SYNC

This pin works in two modes. When the UNITEXT device is not in text mode, the VIDEO input is connected to SYNC via the internal sync switch. The output is intended to drive only the timing circuits of the TV and does not have full video bandwidth specification. In TEXT mode the output delivers composite sync pulses from the internal sync generator. The sync pulse format is selected by the commands 50 to 5F (see Ref 2, UNITEXT Software Applications Guide).

Pin 3 - VIDEO

This pin is connected to the internal video switch. It is connected to Pin 2 when the device is not in text mode. This input should be AC coupled.

2.PIN DESCRIPTION - continued

Pins AVcc

Analogue power supply pin 5V±10%. This pin should be decoupled to ground (pin 24) with a 100nF capacitor as close as possible to the package pins.

Pin 5 - RSTB

Active low reset. To facilitate power-on-reset, the pin should be connected to DVcc (pin 21) through a 100k resistor and to ground through a 1µF electrolytic capacitor.

Pins 6 & 8 - TEST1 & TEST2

No connection should be made to these internal test pins.

Pins 7, 14 , 24 - GND

All three grounds should be connected together.

Pin 9 - I^2C EN - I^2C Enable

This input selects how the UNITEXT device is controlled

Logic 0	-	Simple Serial Bus
Logic 1	-	I^2C Bus

Pin 10 - TDATA

Schmitt trigger input. Teletext data from the Analogue Interface.

Pin 11 - TCLK

Schmitt trigger input. Teletext clock from the Analogue Interface.

Pin 12 - CSB

Schmitt trigger input. This pin receives active-low composite sync from Analogue Interface. The signal is used to lock the timing circuit to the incoming teletext data.

Pin 13 - LOSYNB

Open drain output. The signal is low when just text is displayed on the screen and a bad incoming video is detected. It is intended for connection to the TV audio mute circuit but, if not required, Pin 13 should be connected to Vcc via a 1kΩ resistor.

Pin 15 - TACQ - Text ACQuisition Window

This output is high during lines 2 to 22 of the video signal and should be connected to the window signal input of the Analogue Interface.

Pin 16 - CEN

Open drain output and input. This is a control signal for the simple serial interface. This line should be tied low if the UNITEXT device is to be controlled via the I^2C bus.

Pin 17 - SCL

Open drain output and input. Serial clock line for the I^2C and simple serial interface.

2.PIN DESCRIPTION - continued

Pin 18 - SDA

Open drain output and input. Serial data line for the I^2C and simple serial interface.

Pin 19 - BLANK-Fast Blanking Signal

Open drain output. This signal is high for the whole TV line in TEXT mode and also in MIX mode during foreground colour.

Pin 20 - BLUE

Open drain output. Teletext display.

Pin 21 - DVcc

Digital power supply pin 5V±10%. This pin should be decoupled to ground (pin 7) with a 100nF capacitor as close as possible to the package pins.

Pin 22 - GREEN

Open drain output. Teletext display.

Pin 23 - RED

Open drain output. Teletext display.

Pin 25 - OSC2

VCO analogue output.

Pin 26 - OSC1

VCO analogue input.

Pin 27 - FILT1-Time constant filter

Analogue input. Determines the pull-up and hold ranges of the PLL.

Pin 28 - FILT2-Time constant filter

As FILT1, also, a current limited 2.5MHz source forces the VCO control voltage to Vcc/2 when no sync input signal is present.

3.INTERFACING

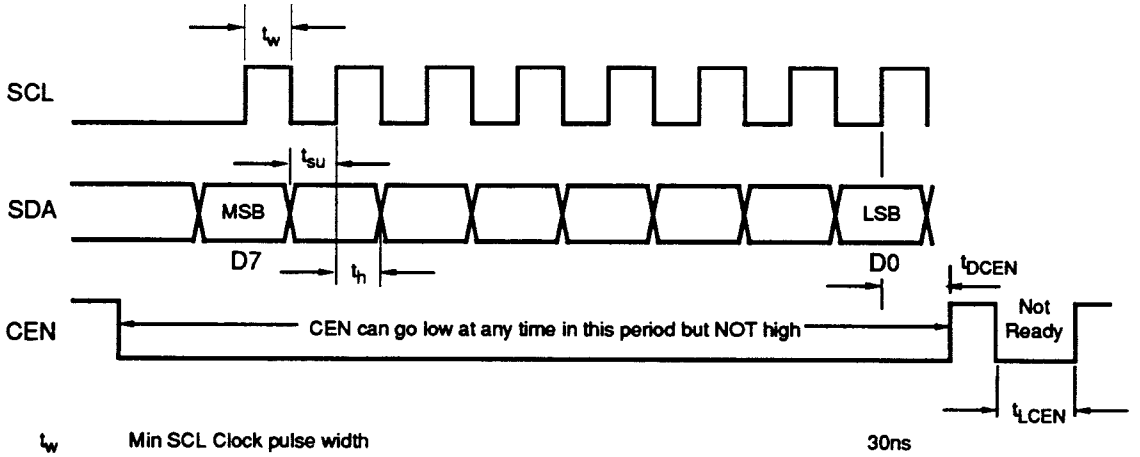
UNITEXT provides two options for control interfacing, a 'simple serial interface' and an I^2C interface.

The purpose of the simple serial interface is to enable easy connection of UNITEXT to systems which do not use an I^2C interface, thus avoiding the overheads associated with a full I^2C bus implementation. The interface provides a straightforward data, clock and handshake line arrangement. The handshake line allows the clock and data lines to be multiplexed with other functions so that only one dedicated control line is necessary. The bus is unidirectional, so data can be passed from the controller to UNITEXT. This means that status information and teletext data can not be read from UNITEXT using the simple serial interface.

3.1 Simple Serial Interface ($I^2CEN=0$)

The simple serial interface consists of an 8-bit serial shift register and some handshake logic. To send data to the interface, the CEN line must be checked for a high state (indicating 'ready'). The data bit is then placed on the SDA input and the SCL input is then clocked (the data is clocked into the shift register on the low to high transition). After 8 bits of data have been clocked into the register, the CEN input is then taken high to tell the handshake logic that data is ready. Up to 100ns later , the handshake logic will pull the CEN low to indicate to the external controller that the UNITEXT decoder is not yet ready - as soon as the data has been processed by the micro-coded processor, the CEN line is released to indicate 'ready'.

The CEN pin is an open drain output (as well as being an input), and can be held in any state whilst the data is being clocked into the register, except that it must not go from low to high during this time. This means that the CEN pin can be used as a chip select or simply clocked at the end of a data stream by an open collector type output.



t_w	Min SCL Clock pulse width	30ns
t_{su}	Min SDA set up time before SCL low-to-high transition	30ns
t_h	Min SDA hold time after SCL low-to-high transition	5ns
t_{DCEN}	Min time between last SCL low-to-high transition & CEN low-to-high transition	100ns
t_{LCEN}	Min CEN low pulse period	40ns

Fig 2 UNITEXT Serial Interface Timing

3.2 I²C Interface (I²CEN=1)

When the I²C interface is enabled, UNITEXT operates as a slave transceiver following standard I²C bus protocols. No special handshake procedures are required other than normal I²C protocols.

3.2.1 Data Transfer to UNITEXT

This is the mode used to send UNITEXT command and data bytes. The bus master initiates the data transfer by placing a 'start' condition on the bus and then sends the UNITEXT bus address with the R/W bit set to zero (00100010). Data bytes are then transferred to UNITEXT which acts as a slave receiver. The transfer can be any number of bytes long. The bus master terminates the transfer by placing a 'start' or 'stop' condition on the bus.

3.2.2 Data Transfer from UNITEXT

This mode is used to read the status word and received teletext data from UNITEXT. The bus master initiates the data transfer by placing a 'start' condition on the bus and then sends the UNITEXT bus address with the R/W bit set to one (00100011). UNITEXT then becomes a slave transmitter. The transfer can be any number of bytes long. The bus master terminates the transfer by placing a 'start' or a 'stop' condition on the bus. During the transfer, UNITEXT will continue to send data as long as the master acknowledges each byte and continues to issue clock pulses. If the master issues clock pulses after not acknowledging, UNITEXT will transmit FF(hex).

3.2.3 Handshaking

Handshaking is carried out on the bit level as described in Ref 1 (I²C Bus Specification) Section 6.3 'Use of the clock synchronising mechanism as a handshake'. When UNITEXT is not ready to service the I²C interface immediately, it can delay the leading edge of certain clock pulses by holding SCL low.

The length of the clock pulse delay depends on the current activity of the on-chip processor. The delay will be increased if the processor is involved in real time processing of received teletext data or if the previous byte is still being processed.

If a clock pulse is delayed, the delay period is typically less than 10µs, but can be up to 1.75ms. This because some 'long' instructions can take up to 1.75ms to execute, and during execution the on-chip processor can not service the I²C interface. The 'long' instructions are detailed in Ref 2 (UNITEXT Software Applications Guide) Section 5.1. If more than 1.75ms has passed since the last 'long' instruction was sent, the clock pulse delay will be less than 0.8ms

For successful implementation of the the bit protocol, the bus master must poll the SCL line after releasing it to check for a high level. This is true for all transfers on the bus and is because the first clock pulse of a data transfer from the master to another slave may be delayed if it occurs less than 1.75ms after UNITEXT is deselected.

References

1. I²C Bus Specification from Philips Electronic Components & Materials.
2. UNITEXT Software Applications Guide from Texas Instruments

4. ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Vcc 6.5V
Input Voltage ..... Vcc + 0.5V
Current Any signal pin ..... ±20mA
Current Vcc or GND ..... ±50mA
Operating free air temperature range ..... 0°C to 70°C
Storage Temperature range ..... -65°C to 150°C
Latch up ..... 250mA @ 25°C

5. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	min	nom	max	unit
Vcc	Supply Voltage	V_{ih} = min, V_{il} = max	4.5	5.00	5.5	V
V_{ih}	High Level Input Voltage	All inputs except SDA & SCL.	0.7Vcc			V
V_{il}	Low Level Input Voltage	All inputs except SDA & SCL.			0.2Vcc	V
V_{ih}	High Level Input Voltage	SDA & SCL	3.0			V
V_{il}	Low Level Input Voltage	SDA & SCL			1.5	V
V_{ik}	Ground Clamp Voltage	Vcc = max All pins @ -20mA			-1.5	V
V_{ok}	Vcc Clamp Voltage	Vcc = 0V All pins except LOSYNB, RED, GREEN, BLUE, BLANK @ +20mA			1.5	V
I_{ih}	Input Current High	Vcc = max TEST1, TEST2 = 0V			±1	µA
I_{il}	Input Current Low	Vcc = max TEST1, TEST2 = 0V			±1	µA
V_{bias}		Vcc = max BIAS = 33kΩ to Vcc	0.8		1.5	V

5. RECOMMENDED OPERATING CONDITIONS-continued

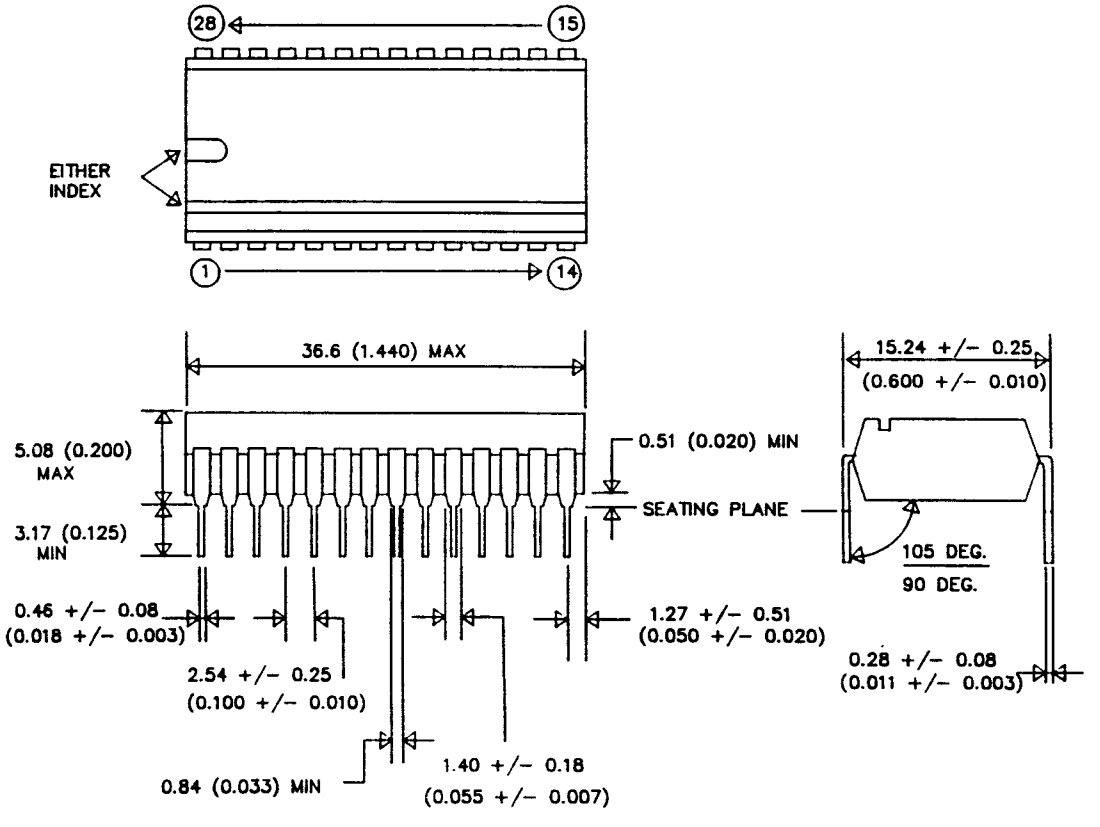
Symbol	Parameter	Test Conditions	min	nom	max	unit
V_{oh}	Output Voltage High	Vcc = min TACQ Ioh =60uA =600uA =6mA OSC2 Ioh =5uA =50uA =500uA	 Vcc-100mV Vcc-200mV 3.76 Vcc-100 mV Vcc-200 mV 3.76			 V V
V_{ol}	Output Voltage Low	LOSYNB, CEN, TACQ, RED, BLUE, GREEN, BLANK Vcc = min I_{ol} =40uA =4mA OSC2 Vcc = min I_{ol} =5uA =500uA SDA, SCL Vcc = min I_{ol} =30uA =3mA			 100 500 100 400 100 400	 mV mV mV mV mV mV
I_{off}	Open N-Drain High-Z Leakage	Vcc = max Pins =LOSYNB,SCL, SDA,BLUE,RED, GREEN,BLANK,CEN Vo = Vcc or 0V			 5	 µA
I_{cc}	Supply Current	Vcc = max Quiescent(BIAS=0V) Active(at f_o)			 10 18	 µA mA
f_o	Operating Freq			22		MHz
R_{on}	Analogue Switch on resistance	Vcc = nom VIDEO=2.5V	 10		 100	 Ω

5.RECOMMENDED OPERATING CONDITIONS-CONTINUED

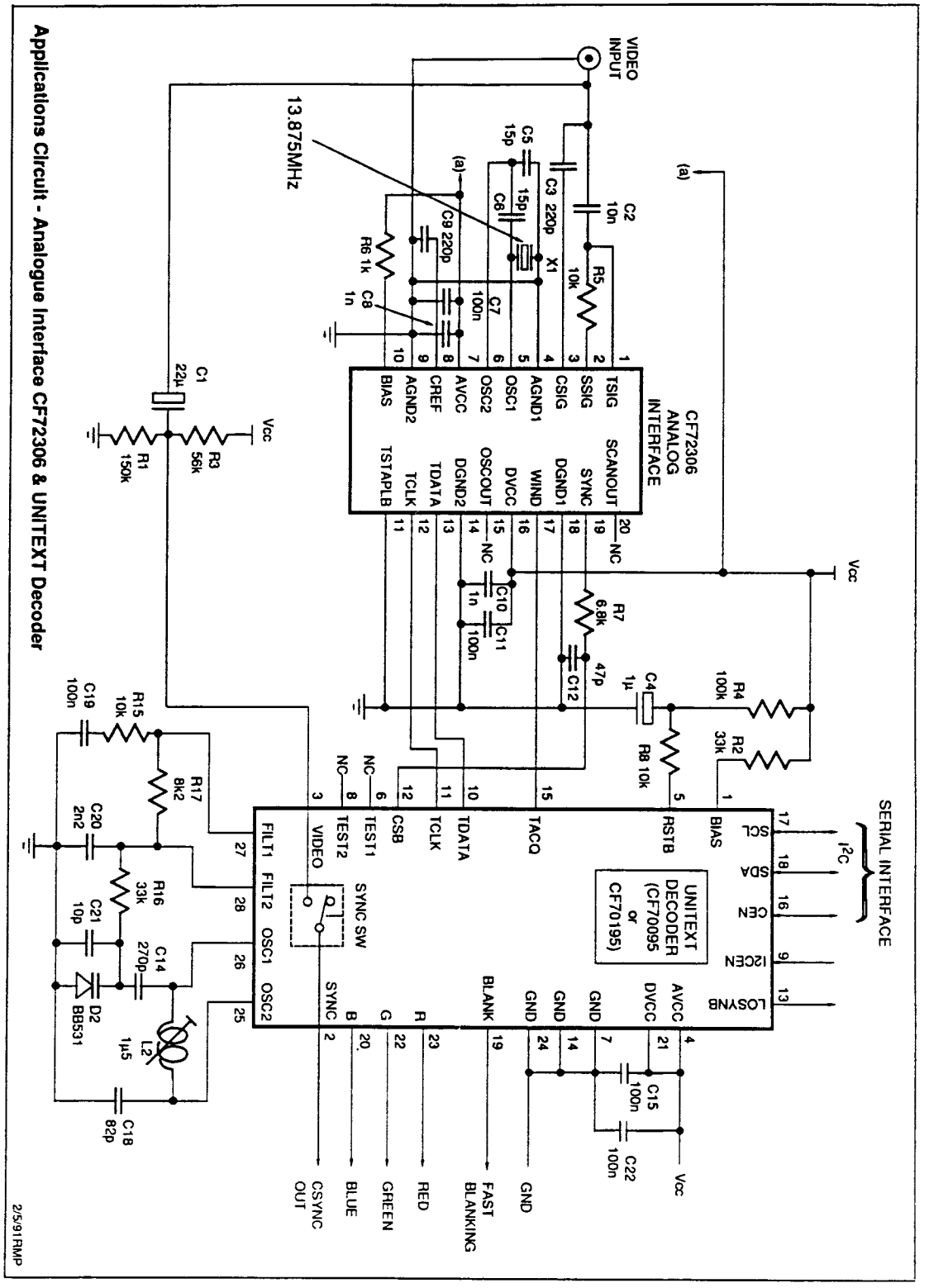
Symbol	Parameter	Test Conditions	min	nom	max	unit
V_{sync}	Sync	Vcc = min				
		Voh (I_{SYNC} = -100µA)	1.8		3.7	V
		Vol (I_{SYNC} = 100µA)	2.0		3.9	V
		Height	0.3		0.7	V
V_{osc}	Osc. Voltage	OSC1 @ 100uA	2.5		3.1	V
		OSC1 @ -100uA	1.6		2.2	V
		OSC2 @ 100uA	0.7		1.0	V
		OSC2 @ -100uA	3.6		4.25	V
		Amplitude OSC2 - OSC1	1.0		2.0	V

6.PACKAGING

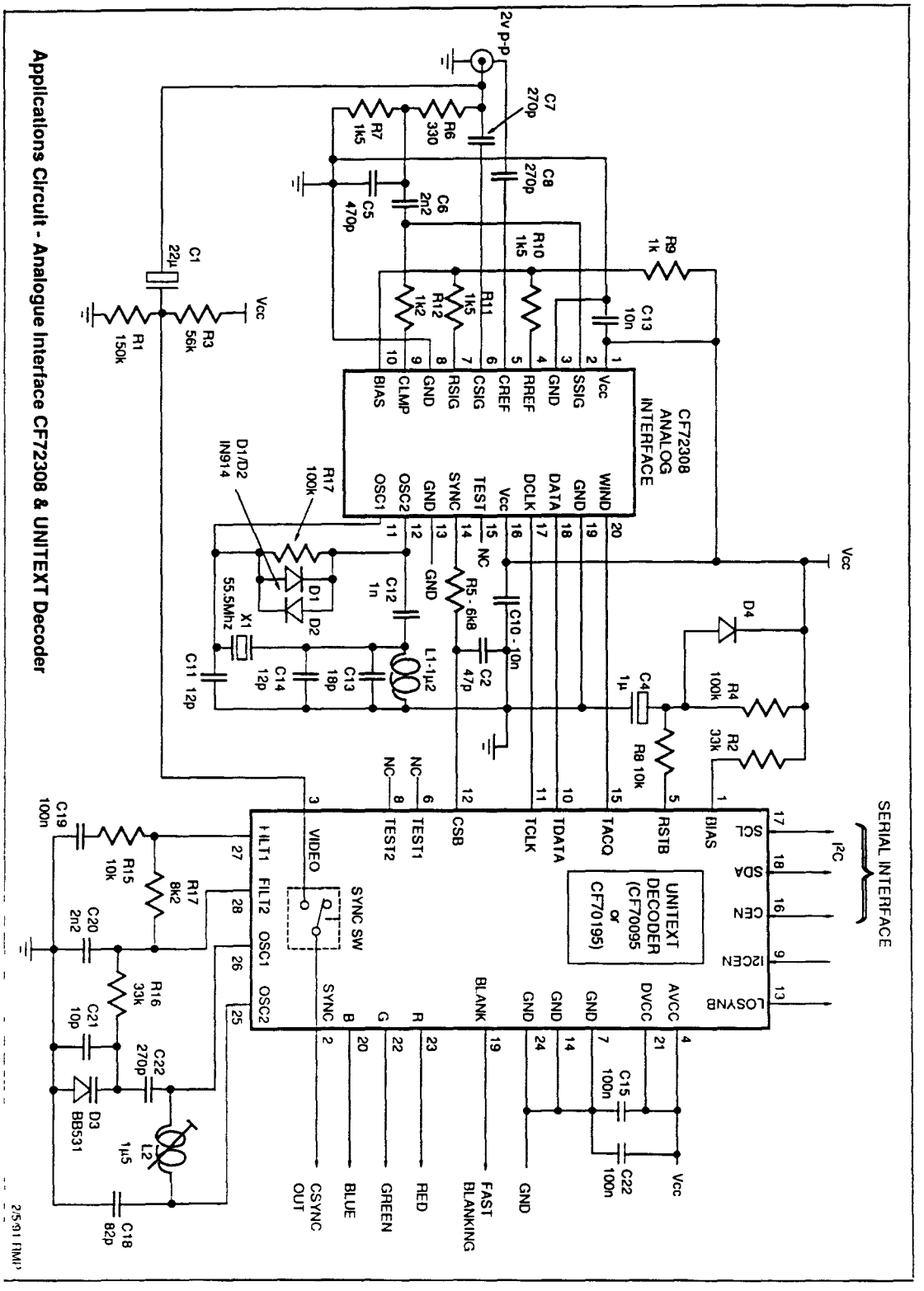
28-Pin Dual-in-Line Plastic Wide Body - Dimensions in Millimetres(Inches)



7.APPLICATIONS INFORMATION



7.APPLICATIONS INFORMATION-continued



CHARACTER FONT DIAGRAMS

The following four pages carry the character font diagrams used in both CF70095 and CF70195 devices.

The drawings have been derived using graphing software from the content of the character ROMs used in the two devices and are shown together with their ROM addresses.

The fonts marked by the bracket shown below appear at the indicated address of the National Option spaces in the diagrams

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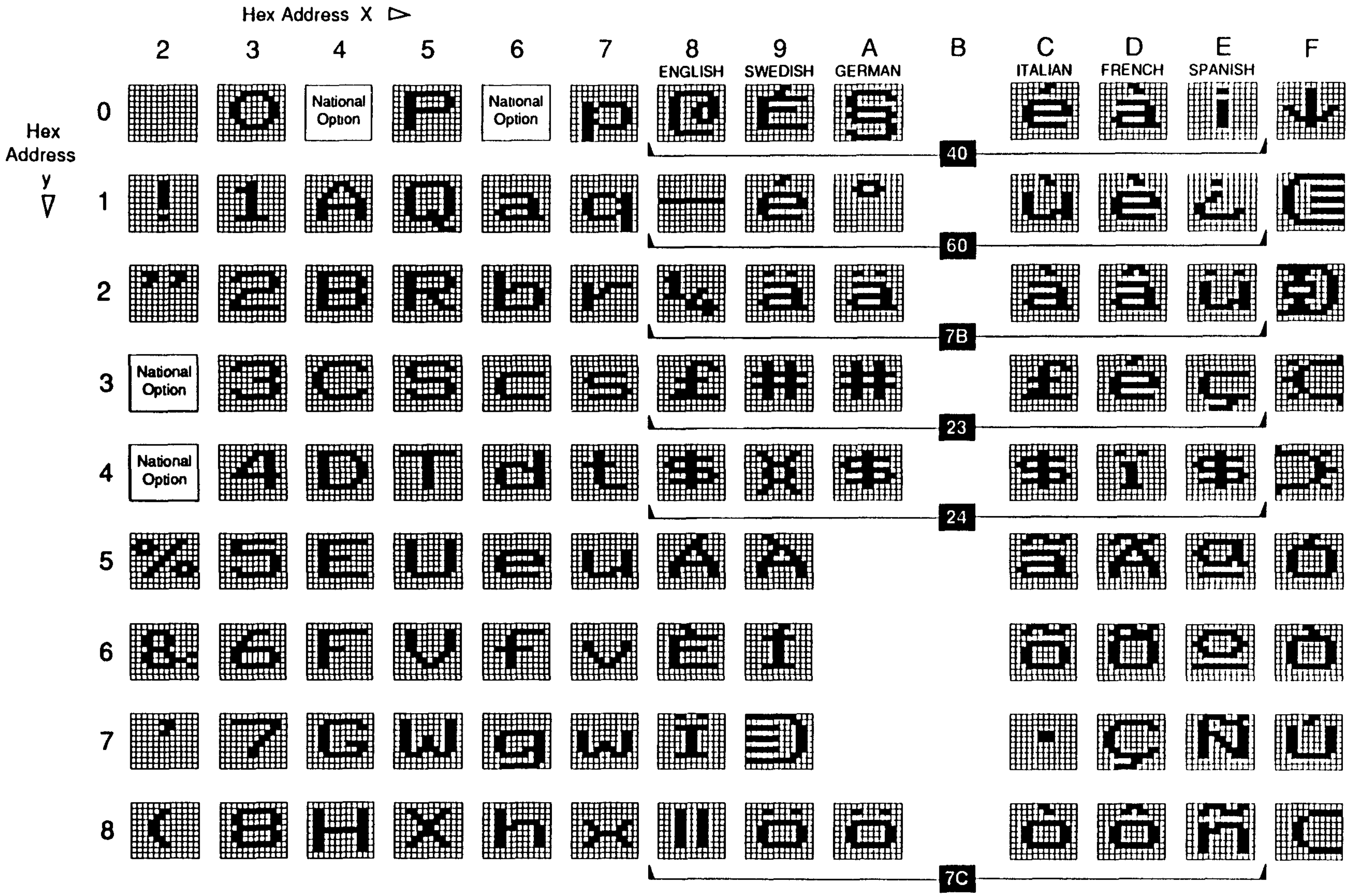
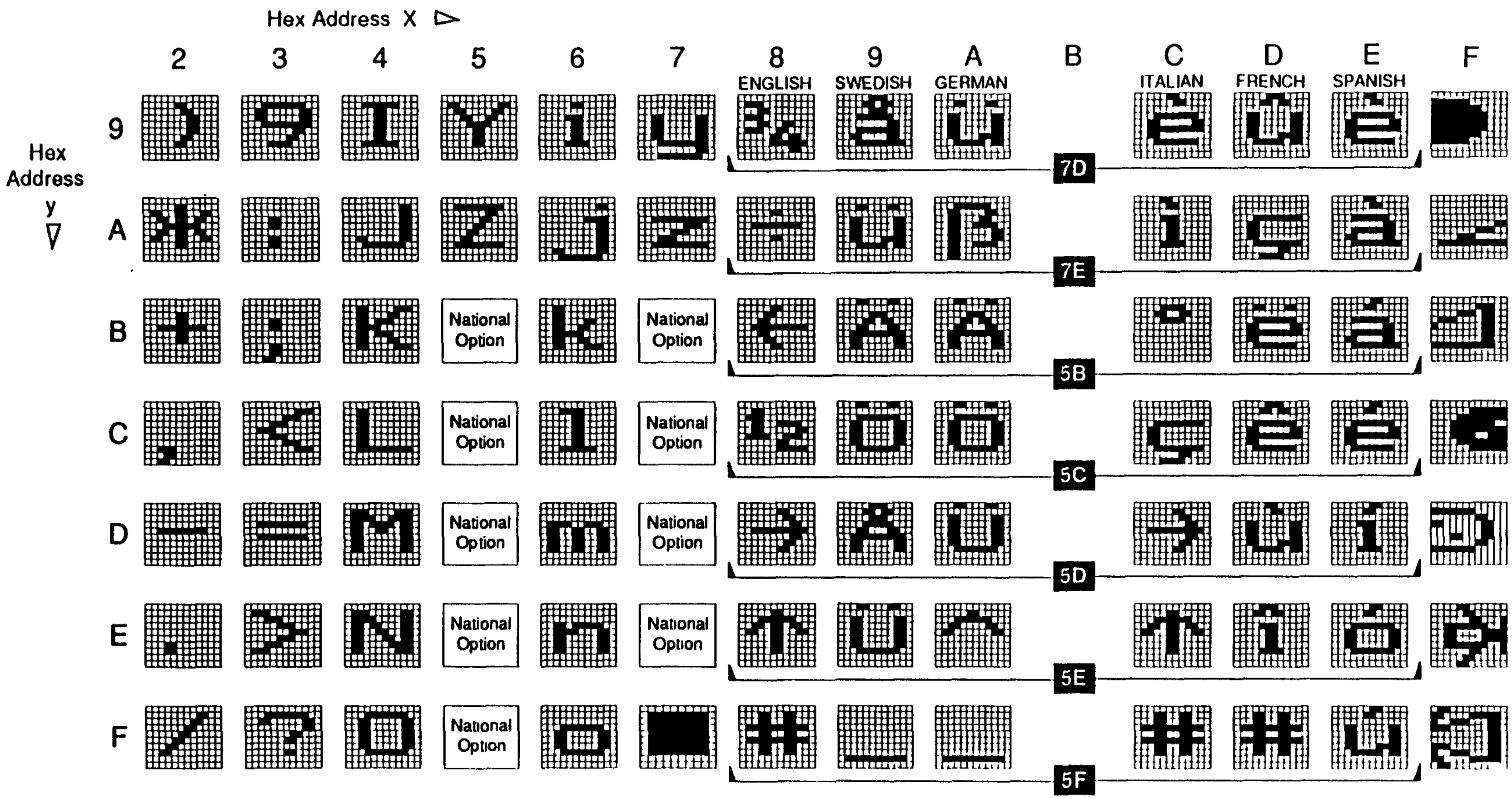
UNITEXT CHARACTER SET - WESTERN EUROPEAN for CF70095



1Q/92

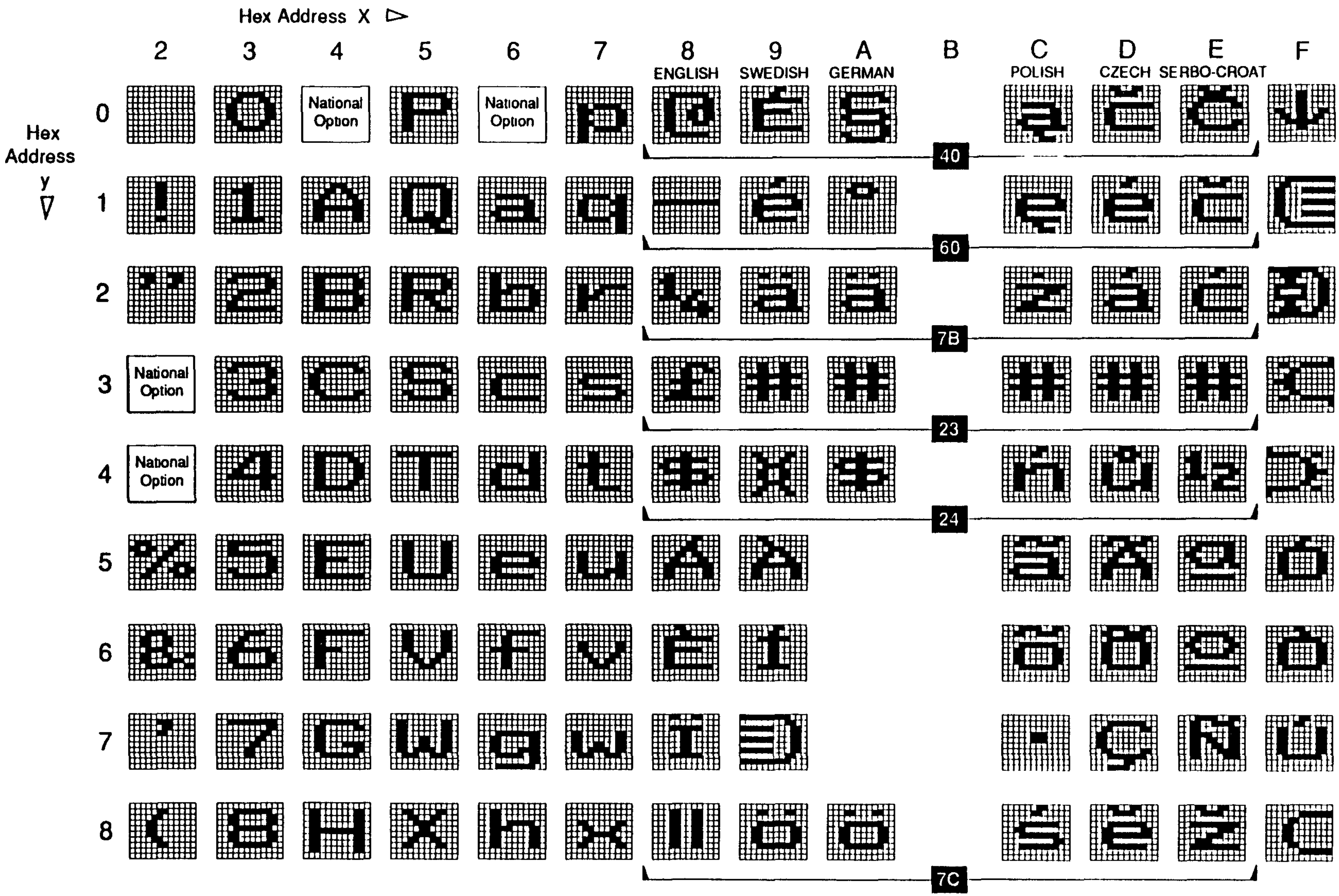
TEXAS INSTRUMENTS

UNITEXT CHARACTER SET - WESTERN EUROPEAN for CF70095 - continued



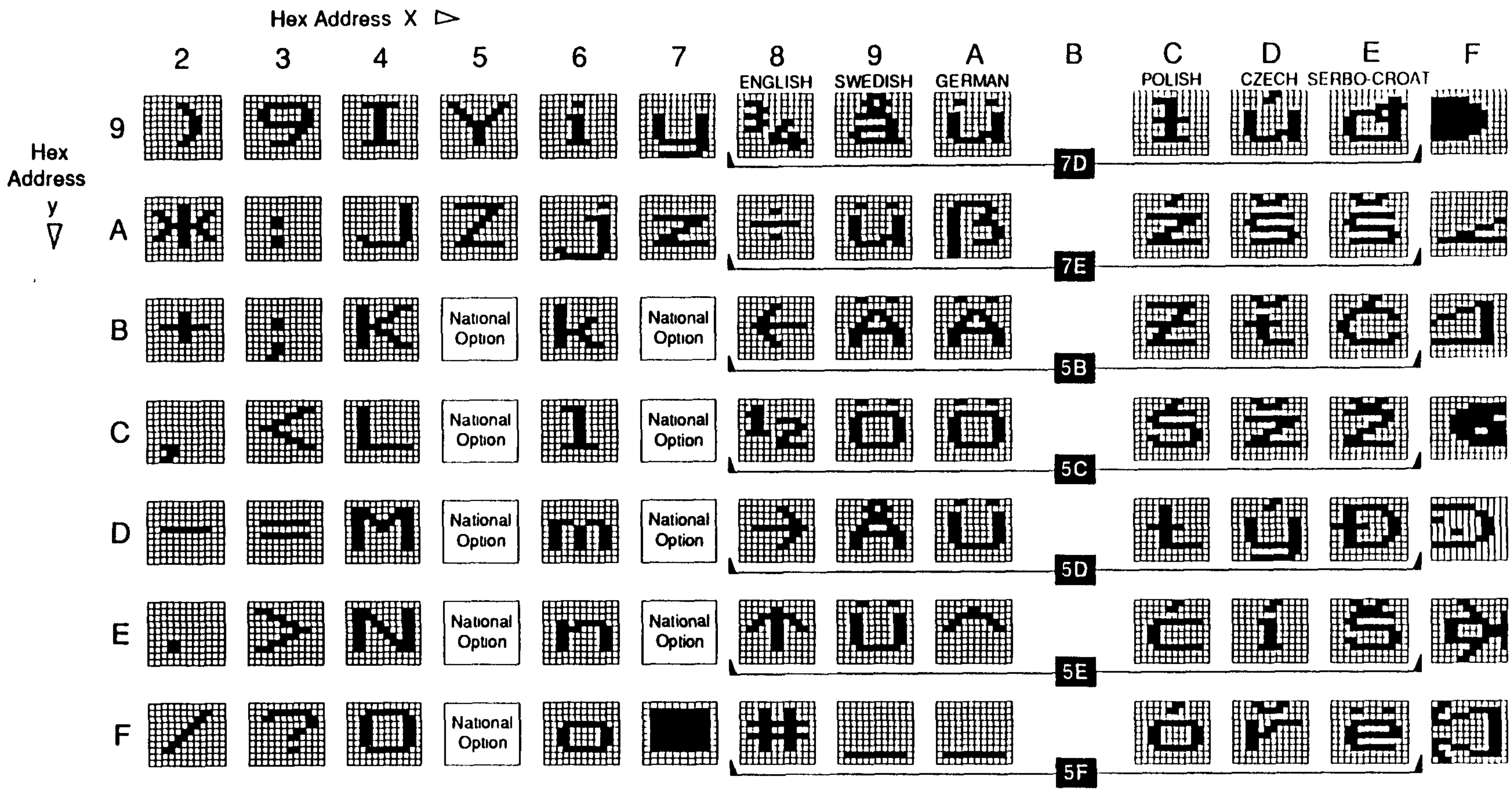
TEXAS INSTRUMENTS

UNITEXT CHARACTER SET - EASTERN EUROPEAN for CF70195



TEXAS INSTRUMENTS

UNITEXT CHARACTER SET - EASTERN EUROPEAN for CF70195



TEXAS INSTRUMENTS