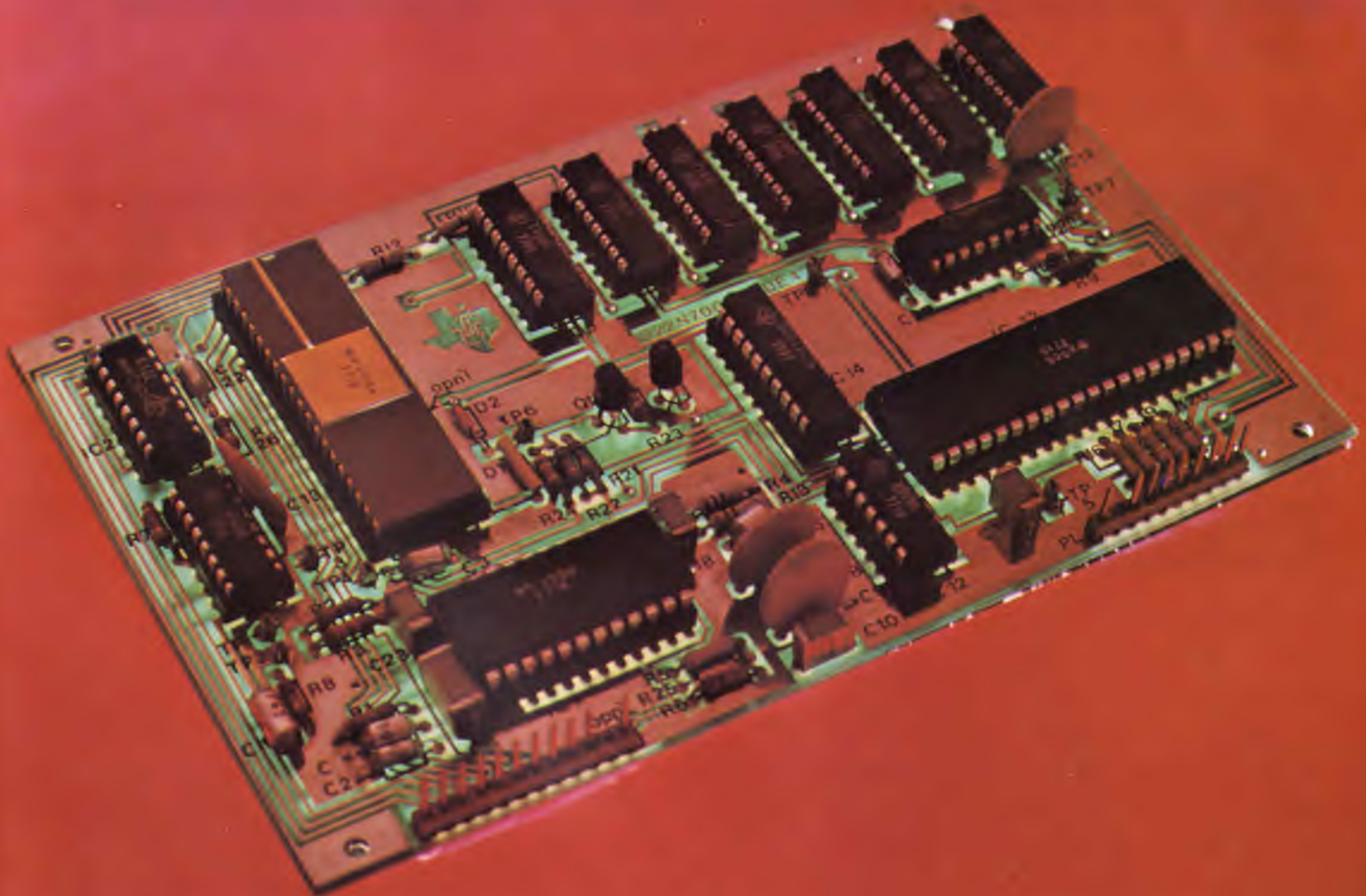




The TIFAX XM 11 Teletext Decoder



Application Report B183

The TIFAX XM 11 Teletext Decoder

by
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INTRODUCTION

A number of factors were considered during the conception of a decoder design to enable the reception of Teletext signals, in particular the BBC's CEEFAX and the IBA's ORACLE services, to be decoded and displayed on a domestic television receiver. The first and most important of these was the intention that, as the product was destined for the consumer market, it must be low cost and simple to use. This could have involved a trade-off between cost and features, and certainly meant that the number of integrated circuits (i.c.s) used would be optimized so that the overall function cost was a minimum. Related to this latter fact was the early decision to supply a complete fully functional module rather than individual i.c.s. This speeds the introduction of the whole Teletext System, does not involve the equipment manufacturer in expensive involved i.c. incoming inspection equipment, and, provided the module interfacing is designed for simple insertion, does not involve him in lengthy design time. Another important consideration was the decision to use processes, after a detailed review of the whole of the company's technologies, which were standard at the time of first production units. For example, charge coupled devices (c.c.d.s) will probably be an ideal process for the Teletext decoder of the future, but, without volume production experience, they would almost certainly introduce complications into the product manufacture and impose unjustified risks.

Another deliberation was whether or not to use a standard microprocessor in the system. Use of such a microprocessor would have required a minimum development investment and would have provided flexibility by means of its program read-only-memories (i.o.m.s). More functions could be easily added, it requires little buffering and will store many logic states. However, Teletext needs none of the latter features but requires a large number of functions to be performed in a fast throughput time and requires additional peripheral dedicated parts, e.g. data slicer, error correction, character rounding logic. Thus the microprocessor is first, not fast enough, and secondly, with the necessary special peripherals, is not economic when compared with a dedicated i.c. design for high volume consumer usage. Therefore the dedicated large scale integrated (l.s.i.) approach was taken for the decoder.

L.s.i. is implemented by gates interconnected to perform functions. Thus a breakdown of the system into speed required per gate level was required and an examination made of all the possible processes available to give the rudimentary divisions for the dedicated i.c.s. Further constraints in the equation for i.c. partitioning are; the minimum acceptable yield relating to maximum bar size, the number of package pins available; and the necessary interconnections between and on i.c.s. All these factors, combined with the desire to have an electrically compatible system, resulted in the use in the module of the low power Schottky transistor-transistor logic (l.p.S.t.t.l.) process extensively, but combined with integrated injection logic (i²l), n-channel MOS (n.m.o.s.), and special bipolar linear processes.

SPECIFICATION

The TIFAX XM-11 is a sub-assembly module, designed to perform full teletext decoding from a composite video signal,¹ and to provide decoded signals suitable for driving the video output stages of t.v. receivers. The decoder is programmed using a scanning matrix keyboard, and may be interfaced with remote control circuitry.

It features:-

- ★ A full alphanumeric character set, upper and lower case letters,
- ★ 64 Graphics characters,
- ★ Six colours plus white display,
- ★ Flashing characters,
- ★ Boxed characters,
- ★ Concealed/unconcealed display,
- ★ Newsflash and subtitle facilities,
- ★ Update capability,
- ★ Time accessed page acquisition,
- ★ Suppress header and page capability.

Also for added legibility and ease of use, it has:

- + Character rounding,
- + Picture, text, and text-superimposed on picture, modes of display,
- + Keyboard entered page and time displayed on the screen,
- + Rolling page number displayed,
- + Freeze display.

It is designed to:

- Employ only a 5V power supply (typical consumption $\approx 800\text{mA}$)
- Allow for an increase in the number of data lines,
- Require the minimum number of connections with the t.v., (The open collector output stages have sufficient voltage and current capability to directly drive t.v. video output stages),
- Allow additional keyboards by simply wiring in parallel,
- Perform all code checking and correcting.

Brief Data

VCC	+5V
Composite video input	1.0-2.7V pk to pk
Line flyback pulse input	-30 to -100V w.r.t. earth
Keyboard entry	4 x 5 scanning matrix
Outputs (R,G,B, Mono-chrome and Blanking)	0 to 15V 20mA maximum sink source.

SYSTEM DESCRIPTION

Figure 1 shows a block diagram of the complete system.

In the Data Slicer the digital information is extracted from the video signal and fed to the Clock Sync to provide

synchronisation of the 6.9375MHz internal clock and to the Serial to Parallel Converter. Video is taken to the Sync. Separator where the composite sync. signal is extracted and fed to the Field Sync. The Line Flyback pulse is passed through a Monostable and taken to both Field Sync. and Line Sync. which provide their appropriate timing signals, i.e. Field Sync., Odd and Even Field pulses and Line Sync. pulses. The data, now in parallel form, is passed from the Serial to Parallel block to the Framing Code Detect, where, if Teletext information is detected, a signal is passed to Character Clock for it to generate timing signals mainly for character control. 8-bit byte information is passed through and corrected in Hamming Code Correct to the Page Decode.

User commands are given to the decoder via a keyboard (either cable connected or remote control) and decoded in Keyboard Decode. Page/Time decoder ascertains whether the requested page is to be selected by Time code or page number only, and the relevant Page and (optional) time are stored in the Keyboard Memory. When the incoming data matches the information in the Keyboard Memory, Page Decode generates a 'write enable' signal from Page Clear allowing the page to be written into the Memory at addresses generated by Row Count and Character Count.

All information is written into the memory during the frame blanking period. For its read out and display during the active video time, the required page passes line by line through the data latch, which stores it for sufficient time for previous commands to be acted upon, to the Data

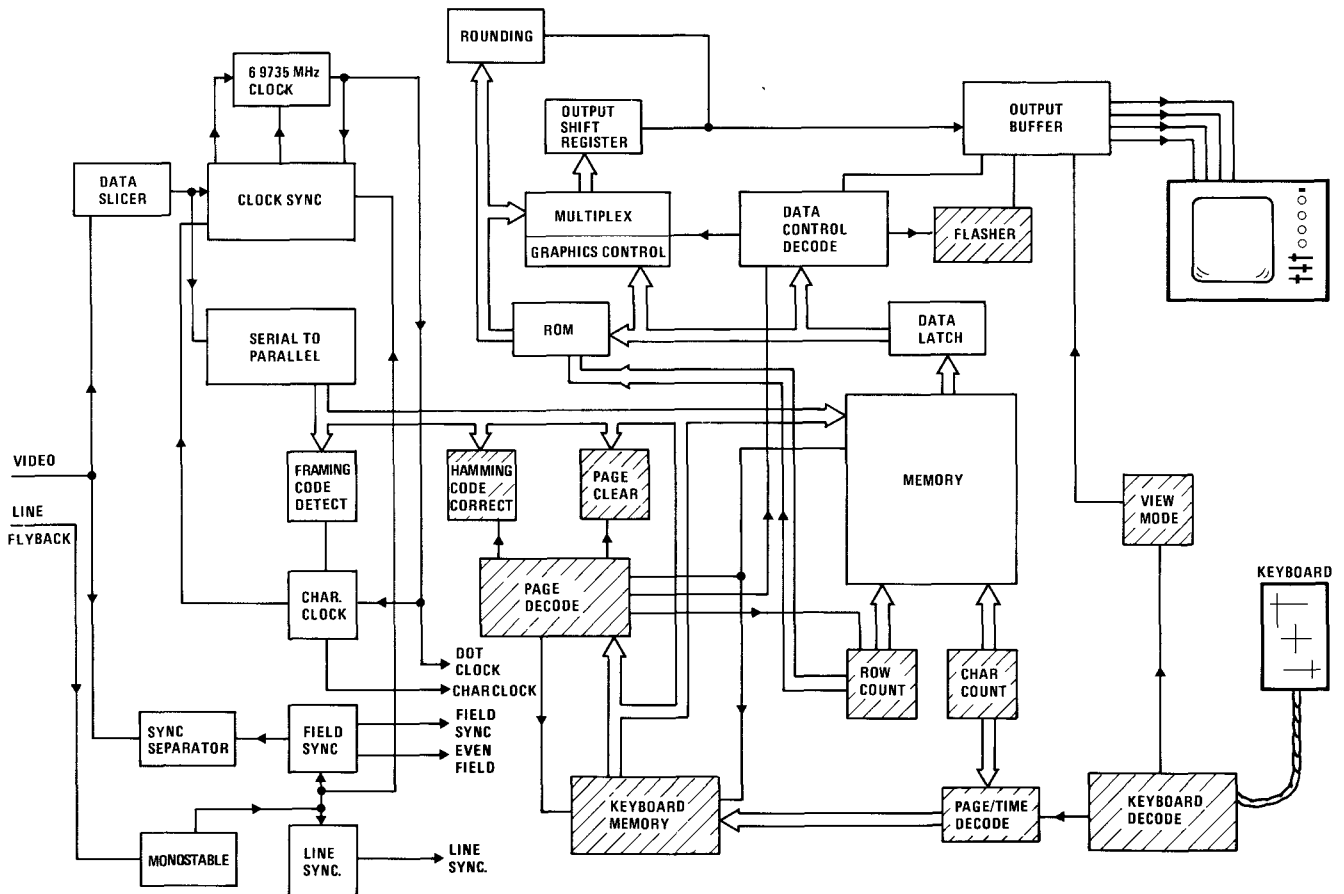


FIGURE 1. Decoder Block Diagram

Control Decode. This allows it to go into Graphics Control if graphics or address the R.O.M. for alpha-numeric information stored there. Under direction of Row Count, letters or characters come from the R.O.M., the former passing through Rounding, and the latter through Graphics Control, via the Multiplexer and Output Shift Register to the Output Buffer. Under command of Data Control Decode, which also controls the Flasher, and View Mode, which ensures the called for display mode, the Output Buffer gives the correct information to the video drivers of the t.v. set.

I.C. DESCRIPTIONS

Linear I.C. (TX005, IC1)

A block diagram of the linear i.c. is shown in Figure 2. Although the input data spectrum only extends to 5.5MHz, the gain bandwidth product of the linear section needs to be in excess of 500MHz in order to obtain t.t.l. compatible waveforms. This dictated a non saturating low impedance circuit design, made with a special bipolar linear process, which together with power dissipation limitations resulted in an optimum supply rail of 5V. The i.c. performs three functions, i.e. data slicing, sync separation, and clock generation.

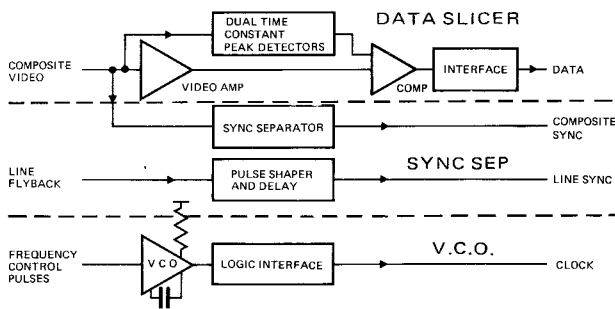


FIGURE 2. Linear I.C. Block Schematic

The Data slicer section extracts the digital information from the composite video signal and provides t.t.l. compatible signals. Using Dual Time Constant Peak Detectors black and peak white are picked out with a long time constants and the overall slicing level is adjusted to a mean level. Using a short time constant the peak 'one' and 'zero' levels are detected and the slicing level further adjusted over this short period to an optimum slicing level. Thus, when the video signal from the amplifier is compared with this continually updated slicing level in the Comparator, the most accurate signal output is obtained. The use of a level adaptive to changes in signal amplitude and distortion results in an excellent system error performance when compared with a non adaptive slicer. In the interface block the data is squared up and converted to t.t.l. levels.

The Sync Separator section removes from the composite video signal the composite sync. signal and converts it to t.t.l. compatible levels for use in the module. In this section also the line flyback pulse is passed through a pulse Shaper and Delay circuit and converted to provide Line Sync at system compatible t.t.l. levels.

The third section generates the Clock signal using a VCO (voltage controlled oscillator). In the display mode the ≈ 7 M Bit signal is counted down by 444 in IC3, the Clock Control I.C., and compared there with Line Sync. Pulses giving the frequency error are fed back to this section of IC1. Here they are integrated and the appropriate error signal voltage controls the V.C.O., whose output is again made t.t.l. compatible, and used as the system Clock. Locking thus to line flyback pulse results in a jitter free display. During the field blanking interval, the clock runs at the same frequency but is phase locked to incoming data.

Serial/Parallel Converter I.C. (X904, IC2)

This i.c. accepts the serial 6.9375 M Bit, now squared up, digital signal from IC1 and clocks it sequentially into a shift register. When it finds a match to the 'hard wired' Framing Code signal (11100100) it recognises Teletext information and synchronises the byte clock to the incoming data by counting thereafter each 8 bits. Each byte or 8-bit word is then read out of the register in parallel form. The i.c. is made using the l.p.S.t.t.l. process.

Clock Control I.C. (X905, IC3)

The clock control i.c. (also in l.p.S.t.t.l.) counts down the data clock to provide the byte clock and the line rate for the system. (For byte clock this involves counting by 8 for the incoming data words, and by 7 for displaying the R.O.M. information.) It also produces all clocks required in the rest of the module. As mentioned in the description of the Linear i.c. (IC1), after counting down by 444 this i.c. also performs a comparison with Line Sync to provide frequency error pulses for the V.C.O. in IC1.

Computational Logic I.C. (TX004, IC4)

This i.c. performs all the housekeeping functions of the system. The areas which it controls are shown hatched in Figure 1, and cover both data acquisition and display. As can be seen, it Hamming checks and corrects control information and parity checks display data bytes. It decodes the keyboard entered information, page number and time code, stores this in a keyboard memory and compares it with the incoming information. Once a match is made with the requested page it forwards this page into the memory, defining both the positioning in there and giving the addresses for later displaying of the page. In it also is the generated character blanking to define the display margins. Other miscellaneous functions controlled by it are the view mode and flashing facility.

In order to contain such a complex amount of circuitry and meet the speed requirements of the system this i.c. is fabricated in i^2l . Production n.m.o.s. could not meet such stringent requirements. The chip size is relatively large, considerable area being taken up by the necessary complex of interconnections.

Memory ICs (TX009s IC5 to 11)

A Teletext fully populated page of text requires a storage of $40 \times 24 \times 7$ bit words i.e. 6720 bits. Although the display character rate is $1\mu s$, random access to any

location is required within 350ns to allow for delays in the system. Reading and writing operations are mutually exclusive. The ideal memory implementation² would be a row addressable store, i.e. one that has random access to any of the 24 displayed rows and serial access to the 40 words by 7 bits data in each row. This, with a 1 out of 24 decoder, 5-bit Row Address and 7-Bit data input/output bus, would minimise the number of package pins and have the best possible organization. Such an organization and the best technology to implement it, i.e. c.c.d., was not available as a production item. Random Access Memories (r.a.m.s) were being developed with 4k and the more ideal 8k-bit storage capacity. To position 40 characters by 24 rows, i.e. 960 positions, a 10-bit address word is required ($2^{10} = 1024$). This word address must be derived from the display row and 'position along a row' addresses. The number of package pins is further minimized by the system using a 7-bit data input/output bus. The 4k and 8k r.a.m.s. being developed, mainly for the computer market, did not have this organization suitable for a Teletext i.c., and also operated from a number of supplies. By using, selected for speed, standard 1k static n.m.o.s. r.a.m.s. for the memory the required organization (1k words by 7 bits) is achieved; only a single 5V supply being necessary. Also the cost of such volume production devices is well down the 'learning curve' and long term cost reduction is likely.

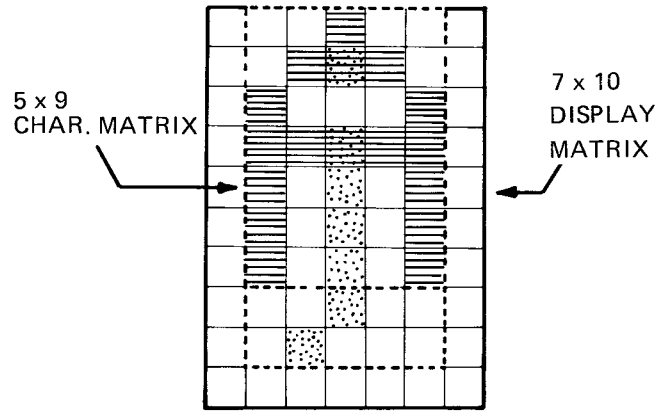


FIGURE 3. Alphanumeric Cell

R.O.M. (SN74S262 IC14)

In order to give good legibility of the alphanumeric characters, they are stored in the r.o.m. in a 5 by 9 matrix, as illustrated by the letters A and j in Figure 3, rather than the more common 5 by 7 matrix. Using the 5 x 9 format gives more design flexibility, particularly with characters whose 'tail' will normally come beneath the line, e.g. j, no repositioning in the matrix being necessary.

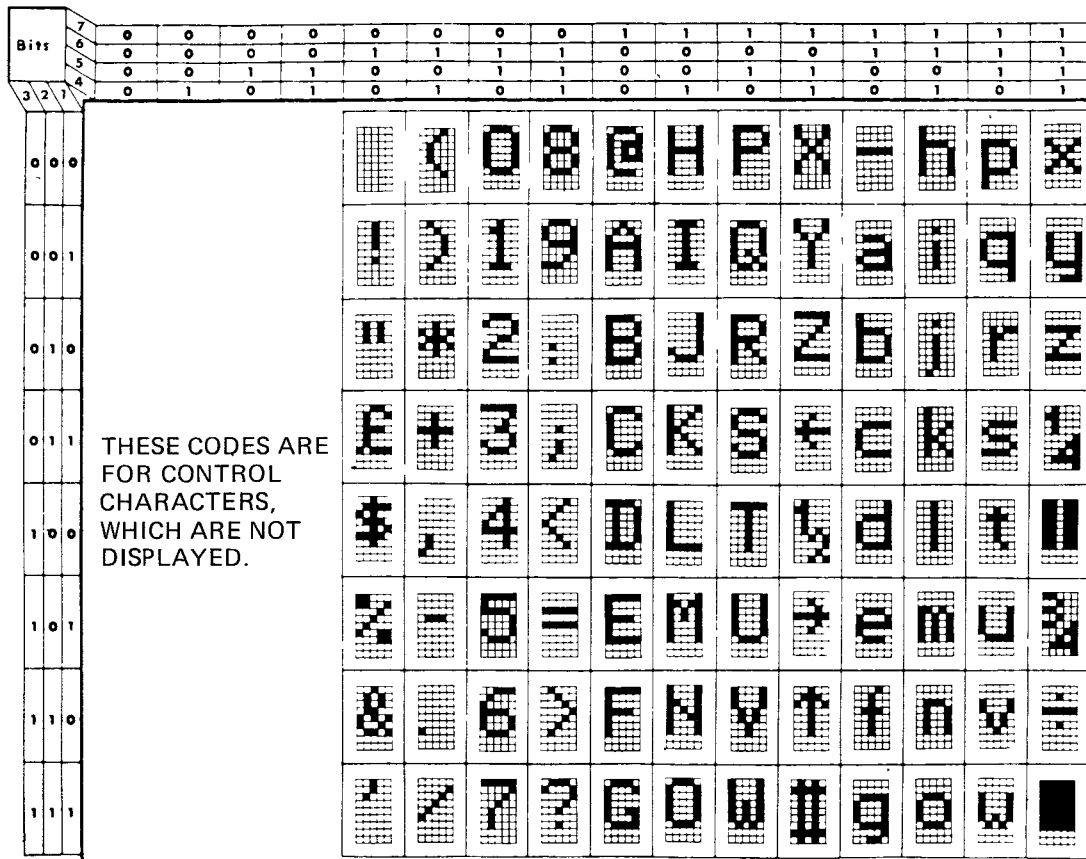


FIGURE 4. R.O.M. English Fount

Characters such as $\frac{3}{4}$ can also be more easily formed and legibly displayed. Thus to store 128 characters (96 of which are displayed and 32 used as control characters) the r.o.m. must be capable of storing $128 \times 5 \times 9 = 5760$ bits. The characters in the r.o.m. can be easily changed, to be suitable for another language for example, by using a different mask during the last stage of the i.c. manufacture, viz. the SN74S263 with Swedish character font. The English font in the '262 is shown in Figure 4.

The organization of the r.o.m. is shown in Figure 5. It features static operation, not requiring any clocks, i.e. the output data remains valid as long as the 7-bit character input address (plus chip enable) remains unchanged. Through the 128 to 1 decoder, the correct character word (of 45 bits) is chosen from the memory. Under control of the row address (4 bits/lines) the output character appears as a 9 word sequence on each of the 5 character row outputs. The device can operate with the row address fixed while the character address changes (scanned display) as in the TIFAX module, or the character address may remain fixed while the row address changes (x-y or character scan).

In the module the sequence for a page display is as follows: The first character of the first display row A, say, has its address presented to the r.o.m. The character row address will be calling for the first (or top) of the 9 character rows. The 5 output lines will therefore provide the top line of the letter (A) which will be displayed as the first t.v. line (both odd and even field) scans across the screen at the correct position. After 5 dot positions plus two blanks for character separation, the computational logic i.c. (IC4) calls for the next display row letter address, B say, to be set up at the r.o.m.s. input. Display of the top row of this letter will then occur as the t.v. lines (odd and even) continue their scan of the screen, the row address not having changed. This sequence continues until the whole 40 character positions have been scanned and displayed. Then IC4 calls for a character row address change to the next one down, recalls character A for the r.o.m. input select, and the scan of the next t.v. line (odd and even) displays the next character row of A,B, etc. The scanning is continued for all nine character rows and a tenth is scanned blank for

spacing between display rows. IC4 then calls up the next display row of characters and the sequence is continued for all 24 display rows.

The outputs of the Teletext r.o.m. are of the totem-pole configuration. (As they are mask programmable, they could be made open-collector or tri-state making it possible to wire-OR the outputs of several r.o.m.s. The facility of two chip enables provides for the possibility of selecting one out of four r.o.m.s.) Invalid row addresses (— 4 bits gives 16 possibilities, only 10 of which are used) are automatically blocked out in the r.o.m. generating a blank on the screen.

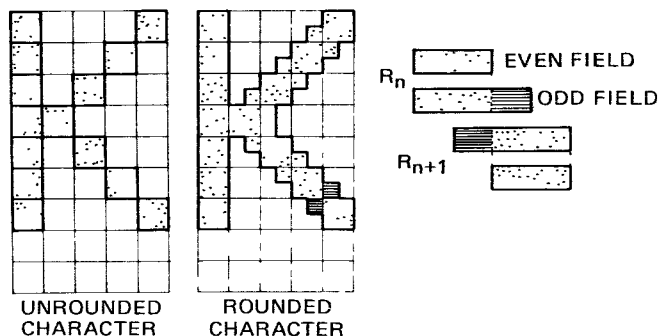


Figure 6. Rounding Characters

In a scanned display system using line interlacing a repeat of the display pattern is given on alternate t.v. lines, as explained. This results in coarsely stepped diagonals which appear fainter than verticals or horizontals. A system which looks at the preceding or succeeding character row and interpolates intermediate extensions to the display by reducing the coarseness of diagonals, known as character rounding, makes the display more legible and acceptable. This is illustrated with the letter K in Figure 6. Practically this can be achieved by comparing the two character rows by using (i) two r.o.m.s, one generating the row being displayed and the other the row above or below; (ii) a single display r.o.m. with a single line store; or (iii) a single fast r.o.m. that can be accessed twice per character interval. The latter is used in the TIFAX module as it results in the minimum amount of storage and package pins required, and reduces circuit complexity and component cost. Thus the '262 has a typical character access time of 180ns which allows access twice per character row. Using a 1.p.S.t.t.l. process allows its power consumption to be kept down to 250mW.

Output Logic IC (X908 IC13)

The output logic i.c. performs a number of functions concerned with the decoding, routing and display of information. A block diagram of its internal arrangement is shown in Figure 7.

Under control of the computational i.c. (IC4) the data from the memory comes into the output logic i.c. and

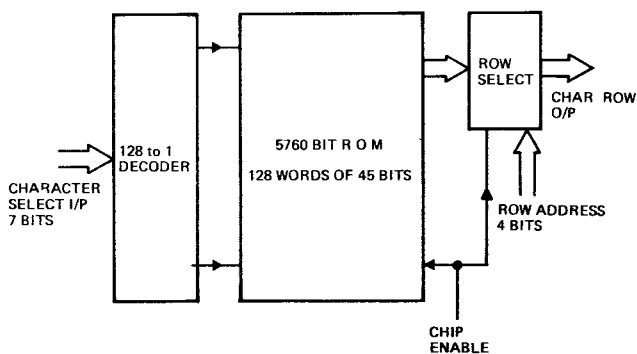


FIGURE 5. Organization of the R.O.M.

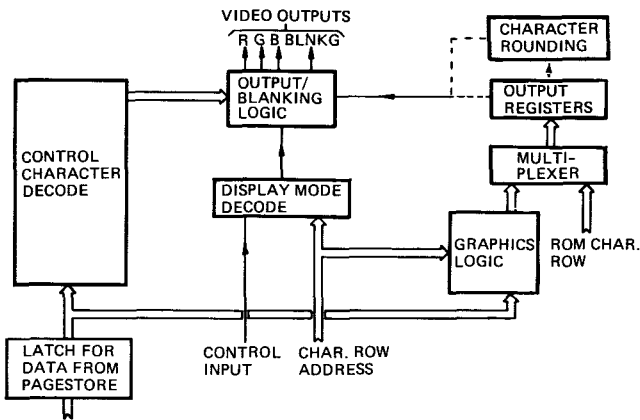


FIGURE 7. Display Logic

is stored in a latch. Seven-bit character select address information is fed from here out of the i.c. to the r.o.m. and, internally, to the graphics generator logic and to the control character decode. The latter determines whether the information in the latch is a control character or not. If not, it next determines whether the system at that time is in a graphics mode or not. The specification calls for the information to be in alphanumeric white unless directed to the contrary. Thus, assuming no previous control characters, the i.c. will not be calling for a graphics mode and the character row outputs from the r.o.m. will be allowed to pass through the multiplexer into the output registers. If the next character is a control character, say, the control decode determines what type of control, e.g. graphics, colour, flash, box, etc. If graphics it will call for the correct symbols to be passed through the multiplexer to the output registers.

The 7 by 10 (including isolation borders) matrix size is also used for displaying the graphics characters by dividing it into six separately controlled sections, as denoted by B1, B2, B3, B4, B5 and B7 in Figure 8. The illumination of any particular section(s) is determined by using 6 bits of the 7-bit character select address. One bit is assigned to

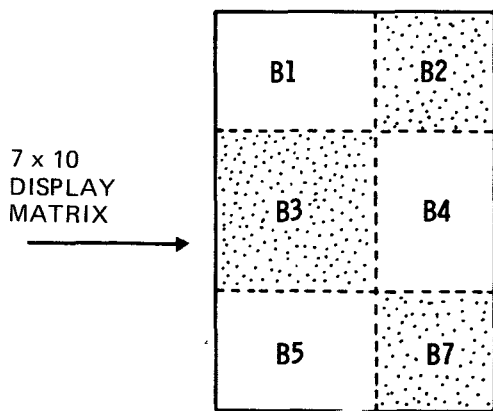


FIGURE 8. Graphics Cell

each section and if it is a 'one' its section will be illuminated in a scanning fashion similar to the character scanning.

The information from the multiplexer to the output registers is in parallel form and it is converted to a serial output form in the parallel-in serial out (p.i.s.o.) register. The serial information is passed to the character rounding i.c. (X909) to be rounded, although this operation can be omitted if required. Adjusted information then goes into the output/blanking section of the i.c.

A control input from IC4 informs the display mode decode section of the type of information required, e.g. picture, text, or text on picture. After decoding, the correct signals are applied to instruct the output/blanking logic, where t.v. compatible video outputs (R,G,B and blanking) are generated. Other functions, such as flashing, will also be carried out in this latter section, under direction of the control character decode.

Rounding I.C. (X909 IC12)

In this device are a parallel-in parallel-out (p.i.p.o.) register 1, a p.i.s.o. register 2, and rounding logic gates, as shown in the boxed section of Figure 9. At the start of character clock, character line address R_{n-1} on an even field and R_{n+1} on an odd field is presented to the r.o.m. Approximately half way through this period on a positive going edge the r.o.m. output passes to the p.i.p.o. register in the X909 rounding i.c., and the p.i.s.o. register in the X908 output logic i.c. A little later the line address R_n is presented to the r.o.m. Just prior to the end of the character clock period, line R_{n+1} is transferred from the p.i.p.o. register to the p.i.s.o. register on the X909, and line R_n dot output from the r.o.m. goes to the p.i.p.o. register in the X909 and the p.i.s.o. register in the X908. The latter can then be compared with the information in the p.i.s.o. register of the rounding i.c. in the rounding logic gates, amended if necessary, and fed back to the output stages of the X908.

Delay I.C. (IC15)

In order to ensure the correct propagation delays in the system a further i.c. (IC15) is added in the module. This device may become redundant with further development of the other i.c.s.

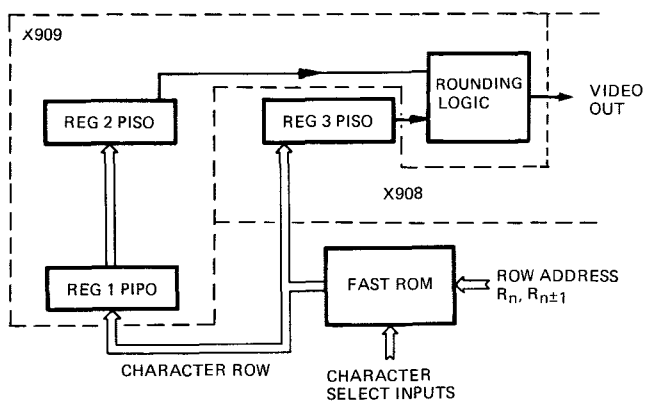


FIGURE 9. Character Rounding with a fast R.O.M.

MODULE

A block diagram of the complete module is given in Figure 10.

Summarizing, the i.c.s and all necessary passive components fit on a 160 x 100mm Eurosize printed circuit board. The only connections necessary are the two inputs, composite video and line flyback; eight connections to the keyboard; five outputs R,G,B, Blanking and Monochrome (not required with a colour receiver); and the 5V power supply.

INCORPORATION IN A T.V. RECEIVER

General

The XM-11 module is designed to reduce to a minimum the amount of redesign necessary in order to incorporate a Teletext facility into a standard t.v. receiver. However, certain areas of existing t.v. designs may need attention on the part of the t.v. manufacturer, viz mec-

hanical design, video output amplifiers, i.f. amplifier, keyboard design, and power supply.

Figure 11 shows the pin connections to the TIFAX XM-11 module and Table 1 gives the connections. Figure 12 shows a block diagram of a colour t.v. receiver incorporating the decoder.

Table 1. External Connections to Module

PL1		PL2	
Pin No.		Pin No.	
1	Keyboard I/P 1	13	Ground
2	Keyboard I/P 4	14	Polarising Key
3	Keyboard I/P 3	15	Line F/B Input
4	Keyboard I/P 2	16	Video Input
5	Keyboard Strobe 1	17	Blue Output
6	Keyboard Strobe 2	18	Green Output
7	Keyboard Strobe 3	19	Red Output
8	Keyboard Strobe 4	20	Monochrome Output
9	No connection	21	Blanking Output
10	Power Supply 1 (+5V)	22	Power Supply 2 (+5V)
11	Polarising Key		
12	Ground		

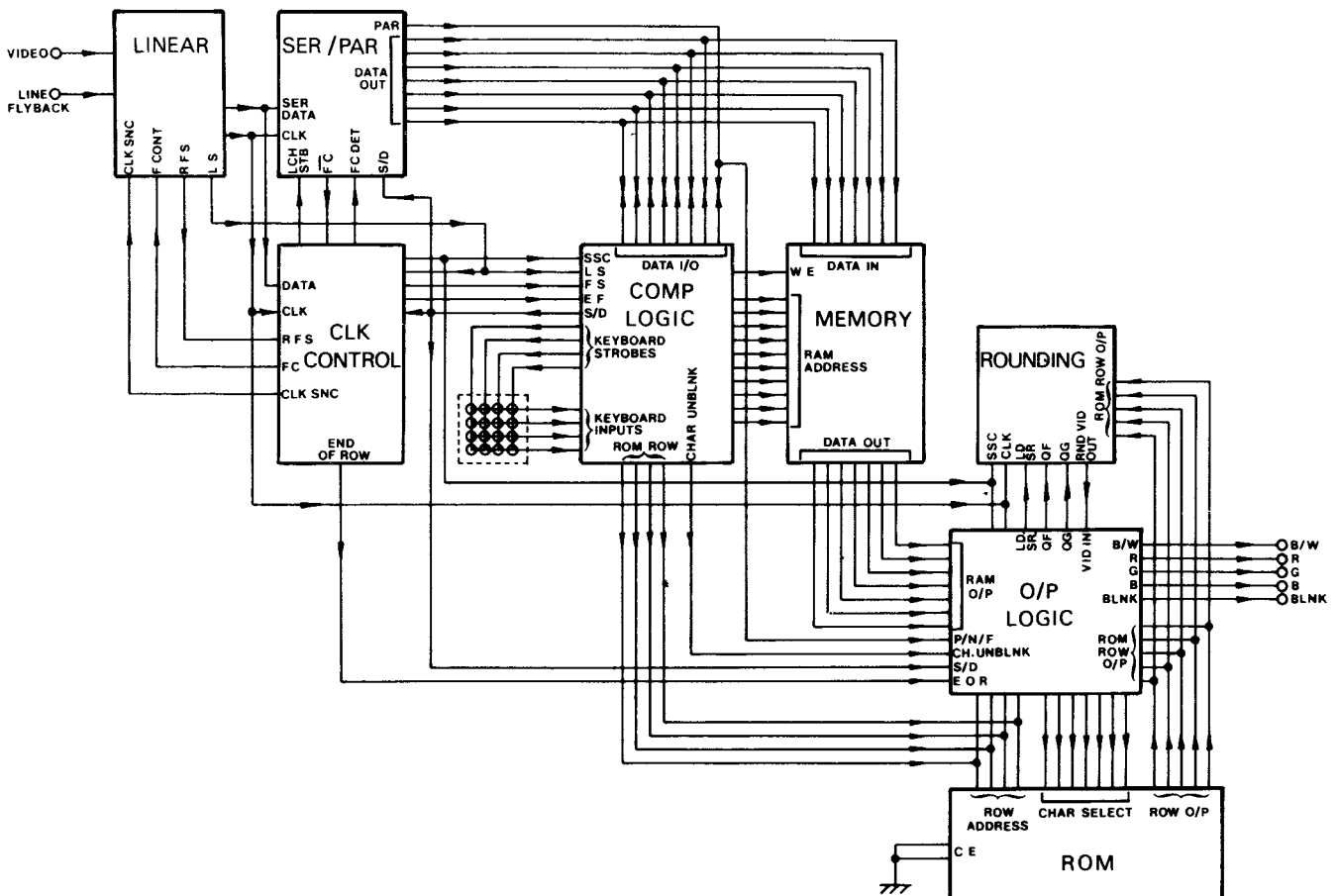


FIGURE 10. Block Diagram of Complete Module

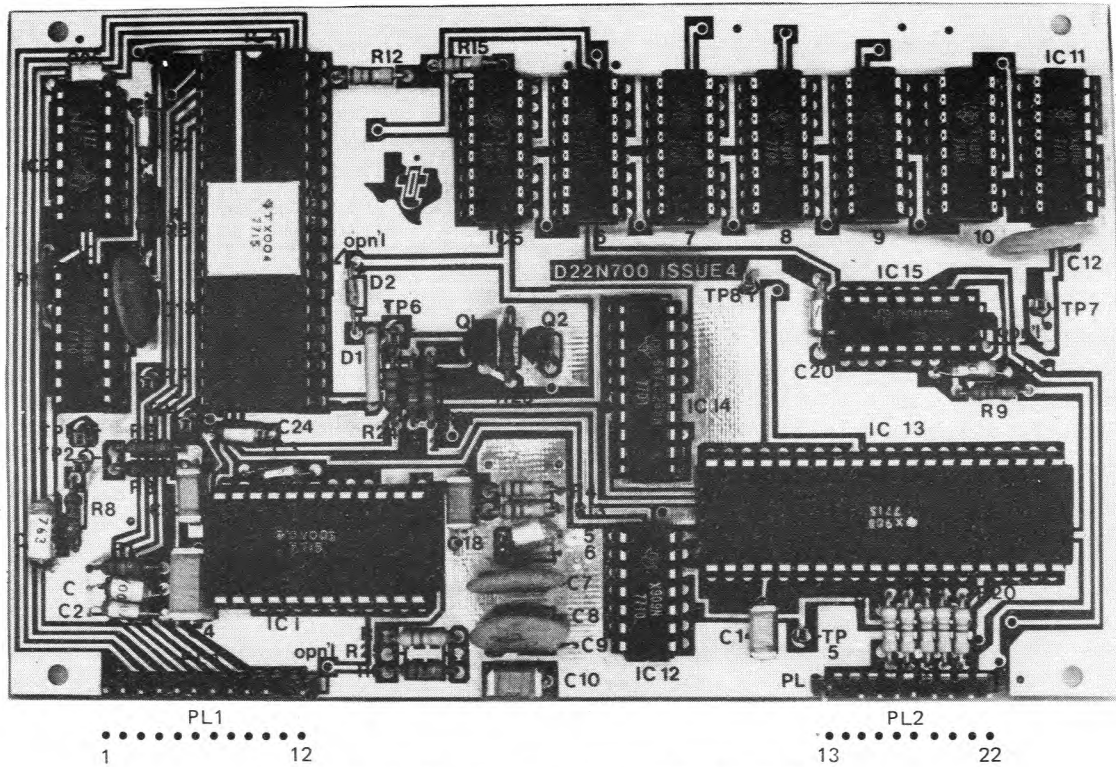


FIGURE 11. Pin Connections to TIFAX XM-11 Module

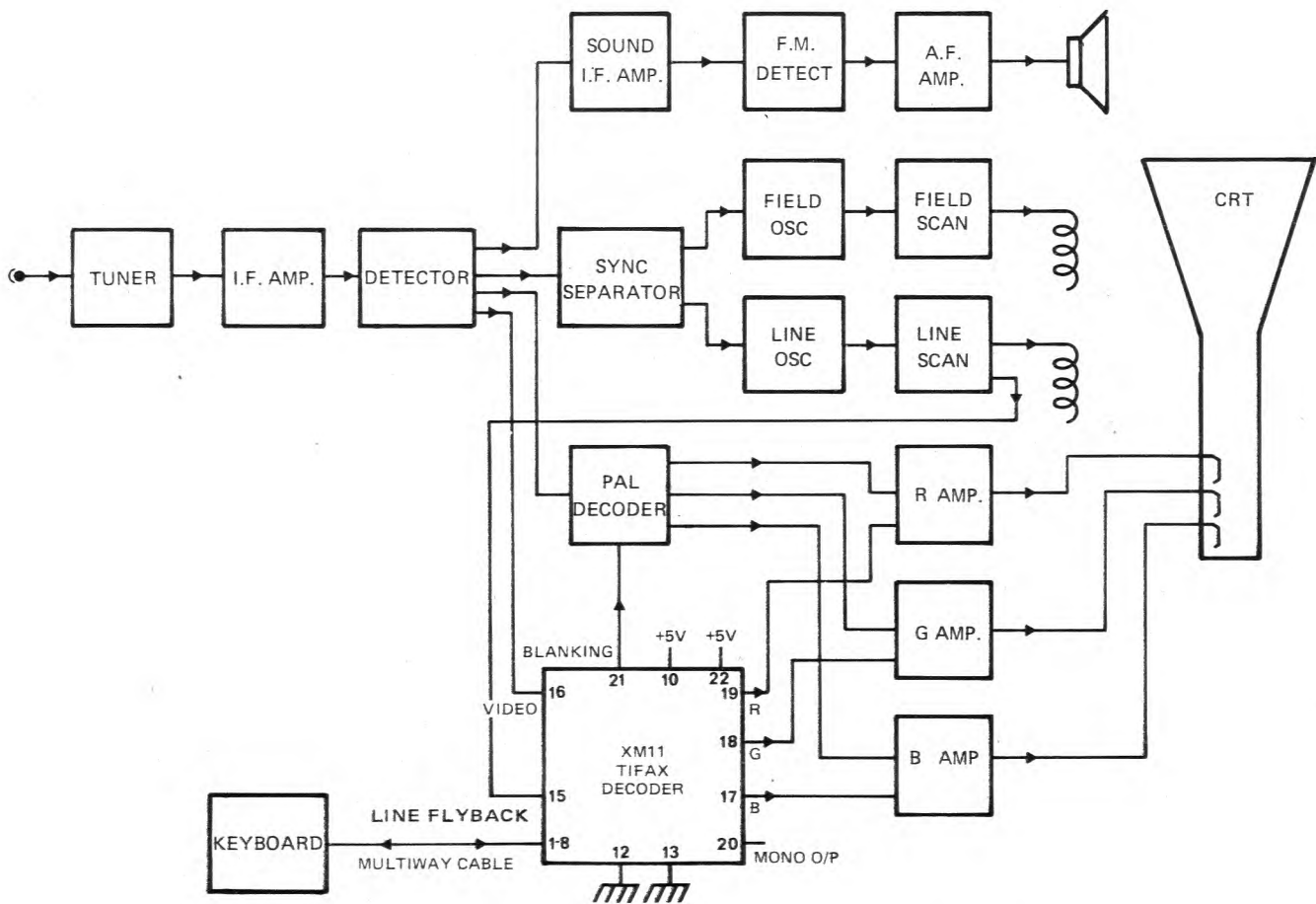


FIGURE 12. Block Diagram of Colour T.V. Receiver Incorporating XM-11 TIFAX Decoder

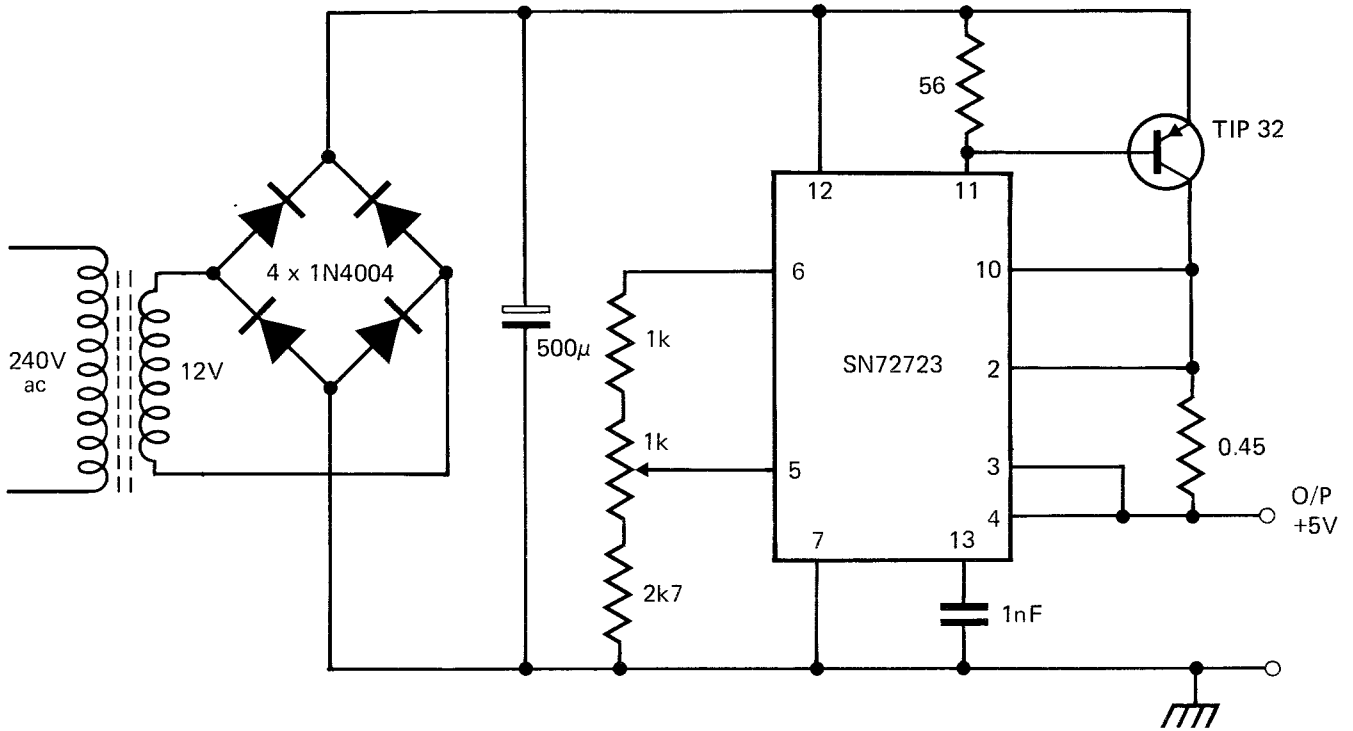


FIGURE 13. 5V Regulated Power Supply

Power Supply

Requirements: The decoder requires only a +5V supply, but this is brought out on two pins (plug 1 pin 10, and plug 2 pin 22) supplying different parts of the circuit. The main supply to the decoder is via plug 2 pin 22, which will draw a current of 900mA maximum (750mA typical). This supply may be to a standard t.t.l. specification, i.e. $\pm 0.25V$ and ripple less than 100mV. The other +5V connection, via plug 1 pin 10, feeds the linear portion of the decoder circuits. These circuits are more sensitive to ripple, which must be kept less than 10mV. Nominal tolerance on this supply voltage is the same as the main supply ($\pm 0.25V$).

A suitable power supply is shown in Figure 13. Alternatively the supply can be generated from the line output transformer.

Precautions: The maximum supply voltage is 6.5V. While the circuits will probably not function correctly under this condition, no permanent damage will be caused by the application of voltages up to 6.5V. Voltages in excess of 6.5V may cause permanent damage, and it is recommended that protection be provided to guard against excess d.c. voltage caused, for example, by the failure of the voltage regulator. Damage may also be caused by voltage spikes on the supply line, and it is recommended that some protection be provided against transients which cause the supply to exceed 6.5V, even for a very short time.

A possible protection circuit is shown in Figure 14. Voltage transients are shorted to earth through transistor VT2, which should have a sufficient large dissipation rating

to be able to withstand the energy from the suppressed spikes. Under normal operation there is no dissipation at all. This circuit should be mounted as close to the TIFAX unit as possible with a minimum length of connection to the module. Other configurations are possible, and any circuit which will act in less than $0.5\mu s$ may be used.

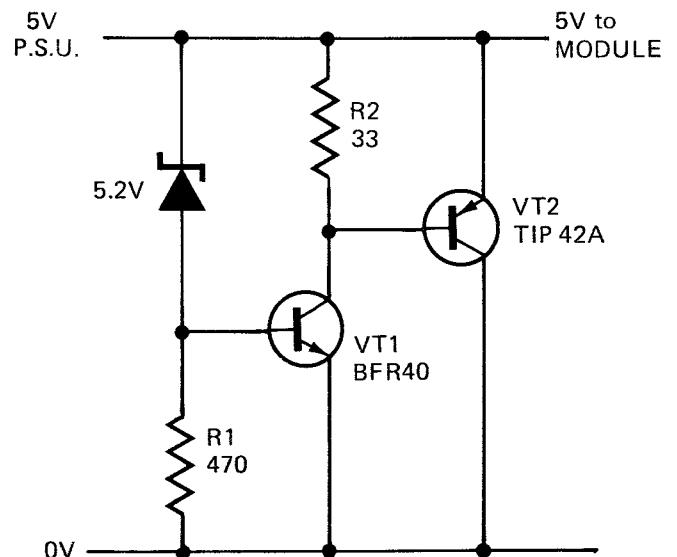


FIGURE 14. Transient Protection Circuit

Composite Video Signal Input & I.F. Requirements

General: The nominal input level required is 1-2.7V peak to peak with negative going synchronising pulse, as shown in Figure 15. It is essential that the sync pulses are retained in the video signal, since the decoder uses these pulses for an internal clock. Care should be taken not to crush the sync. pulses.

An i.f. amplifier and filter designed for good teletext performance will give excellent picture quality, but the converse is not necessarily true. The required response of the video signal, which will be defined mainly by the i.f. circuitry is a complex subject but the following brief explanation summarises the critical parameters.

I.F. Amplitude Response: To obtain good picture quality, amplitude response is of prime importance, and an i.f. amplifier designed for good picture quality will probably have adequate amplitude performance for teletext. The response should ideally be flat over a video bandwidth of 5.5MHz. However, teletext components above 4MHz are of less significance and a slight roll-off in response between 4MHz and 5.5MHz will probably not be detrimental.

I.F. Phase Response: An amplitude response as described above will not give error-free teletext reception if the phase response is not good enough. The phase requirements for teletext are compatible with normal video, but are often neglected in i.f. amplifier design, since the requirements for good picture quality are less critical.

When the signal passes through the i.f. filter and amplifier, it is delayed by a time t_d where:

$$t_d = d\phi/df \quad \text{with } \phi = \text{phase} \\ \text{and } f = \text{frequency}$$

For a narrow bandwidth, the value of t_d is given in Figure 16 by the expression

$$t_d = 2.778 \times (\phi_2 - \phi_1) / (f_2 - f_1)$$

where

t_d is in ns

ϕ is in degrees

f is in MHz

The actual value of delay time t_d is not important if it is constant over the whole bandwidth. In order to achieve this the phase/frequency characteristic must be linear over the bandwidth in question. Non-linearities in this characteristic will result in a varying group delay, degrading the data and possibly introducing errors after decoding. The effects of phase and amplitude distortion on a data signal may be seen in Figure 17.

Measurement of Group Delay: In Figure 18 a low frequency signal f_1 is used to modulate a carrier frequency f_2 that is variable over the i.f. bandwidth. The low frequency is chosen as a compromise between the bandwidth over which group delay may be regarded as constant, and the resolution of the phase comparator (100kHz is probably suitable in most cases). Group delay is measured as a phase difference between the 100kHz reference and the detected 100kHz output. By taking measurements with the carrier frequency varied over the i.f. pass band, the group delay characteristic may be plotted.

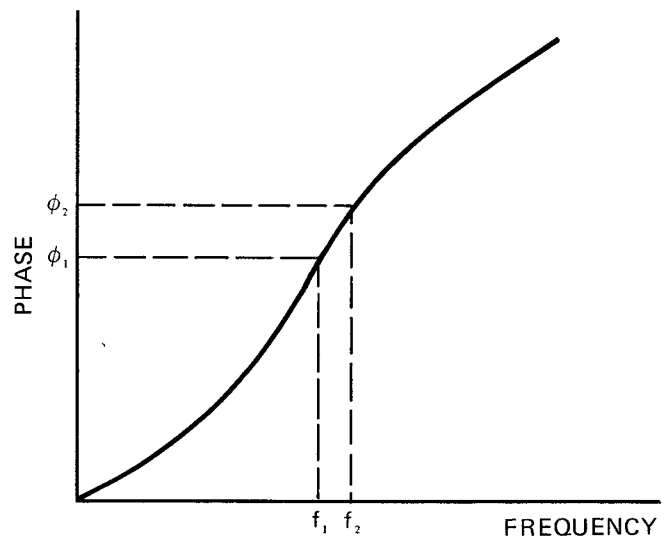


FIGURE 16. Group Delay Definition

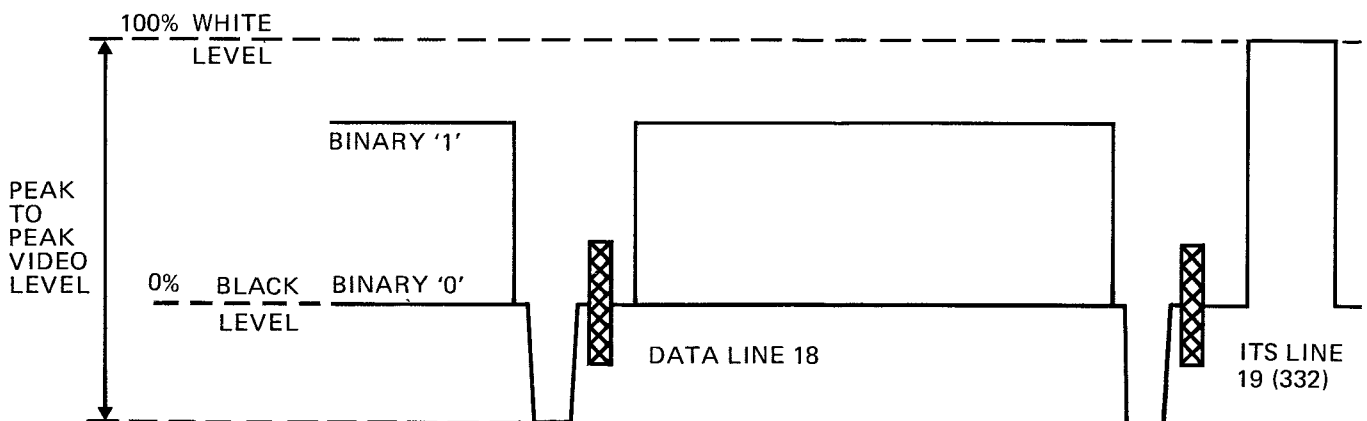


FIGURE 15. Video Input Waveforms

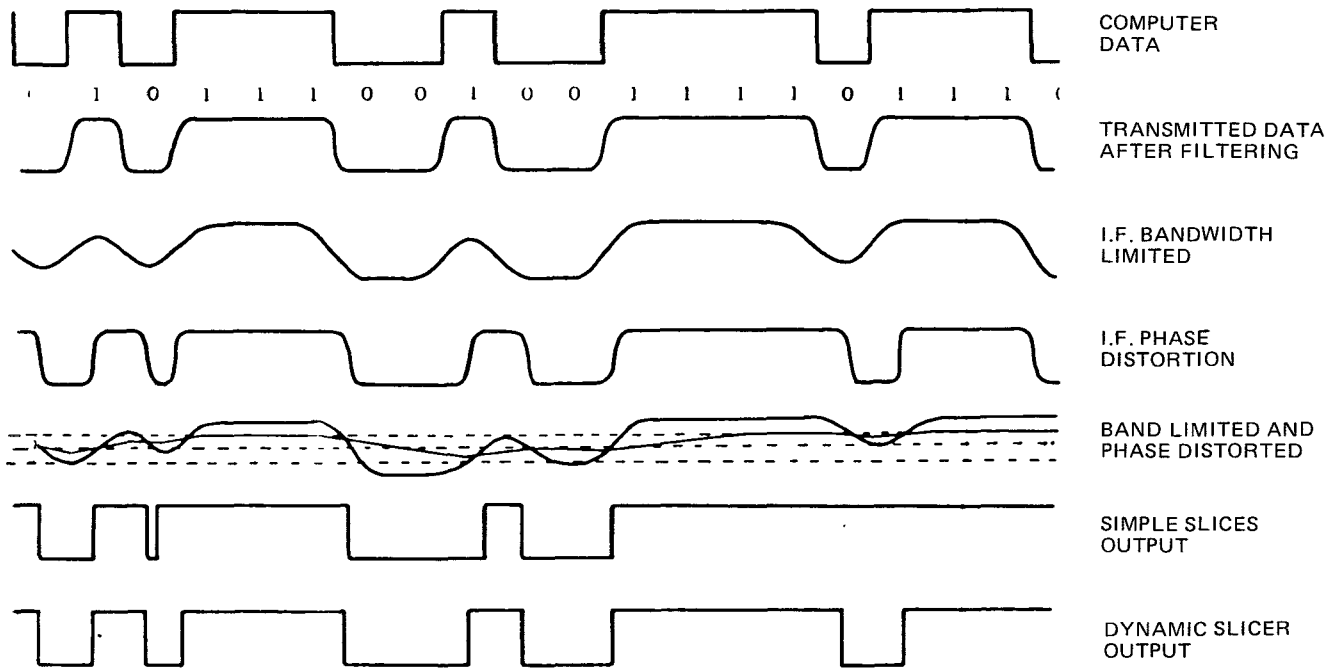


FIGURE 17. Effect of Phase and Amplitude Distortion

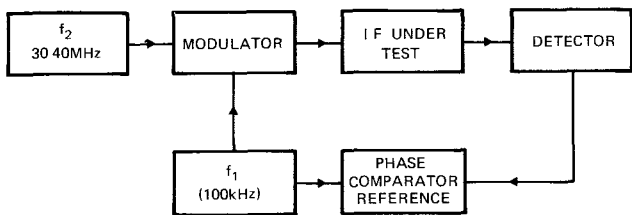


FIGURE 18. Group Delay Measurement Using Modulated Wave Amplitude

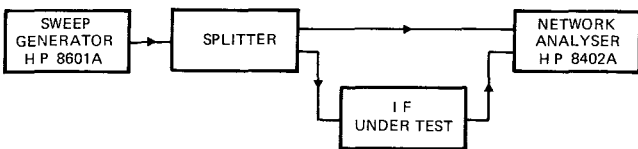


FIGURE 19. Group Delay Measurement Using Network Analyser

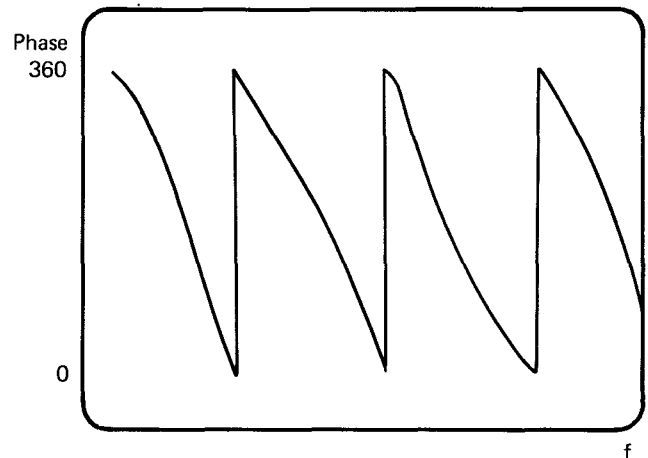


FIGURE 20. Network Analyser Display

At any given value of f_2 :

$$t_d = (10^9/f_1) \times (\phi/360) \quad \text{ns}$$

The method may be extended to include modulation up to u.h.f.

Figure 19 shows an alternative method of measuring group delay using a Hewlett Packard Network Analyser. This method is extremely simple to set up but suffers from the disadvantage that phase distortion in the demodulator and video circuits of the television is not included. The network analyser displays the phase/frequency characteristic of the i.f., a typical display is shown in Figure 20. Group delay is calculated from the slope of the phase/frequency curve.

Practical Receivers: A number of different television receivers have been evaluated for group delay characteris-

tics and the teletext error rates compared for a given signal level. The receivers tested had group delay variations of 100-400ns. The error rate is dependent not only on the magnitude of the variation, but also on its characteristics with frequency. For example, two receivers had similar variations of group delay magnitude, but one had a peak at low video frequencies and the other a peak at high frequencies. Distortion at the low frequency end of the video spectrum produces considerably more errors than distortion at high frequencies, due to the fact that the data energy content is higher at low frequencies.

It is not possible at this time to give absolute rules for i.f. group delay performance. Experience at this stage indicates that a very low error rate can be achieved with t_d varying up to 100ns, with relatively little dependence on

the shape of the t_d versus frequency graph. With variations in t_d of up to 250ns, error rate will be dependent on the shape of the graph of t_d against frequency as previously described. If the variation in group delay exceeds 250ns, a significant number of errors will almost certainly be produced. The levels of group delay variation quoted above are those in the presence of a good signal/noise ratio and amplitude response. In poor signal strength areas, or if the amplitude response is not sufficiently flat, significant errors may be produced by lower values of group delay variation, and it is felt that a group delay variation of 50ns should be regarded as a target specification.

Methods of Improving IF Phase Response: If measurements on the i.f. show that the characteristics will result in poor teletext reception, several different approaches are possible to improve the signal.

1. Redesign of LC filter network.

It may be possible to improve the i.f. group delay by modification of the filter networks. It is quite possible to design an LC block filter with excellent group delay characteristics – providing that group delay is considered as a design parameter. The problem is usually that there is little need to consider group delay for colour television receivers and it therefore is neglected in the design.

2. Video Correction of Phase Response.

It is, in theory, possible to synthesise any desired phase response by the use of all-pass filters, derived from lattice sections (Figure 21). The phase-shift introduced by this network is given by

$$\tan \beta/2 = -j \sqrt{(Z_a/Z_b)}$$

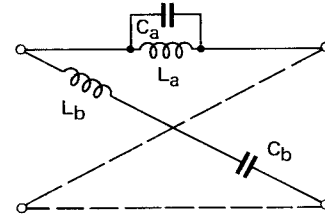
Phase response of this network configuration with varying LC ratios are shown in Figure 22. However, the network in Figure 21 requires a balanced input and is complex in terms of components.

If $\omega \cdot L_a > R_0$, it is possible to transform the lattice network of Figure 21 to a bridged T as

shown in Figure 23. Details of this transformation can be obtained along with much other valuable information on phase correcting networks.³

3. SWF Filter.

Another possible way to provide a phase-linear i.f. is by use of a surface-wave filter. This type of device has the advantage that its phase



$L_a C_a$ and $L_b C_b$ are reciprocal impedances

i.e. $L_a = R_0^2 C_b$

$C_a = L_b / R_0^2$

where R_0 = characteristic impedance.

FIGURE 21. Lattice Filter Section

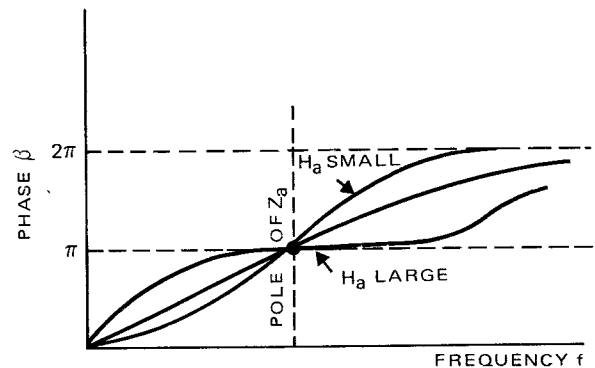


FIGURE 22. Phase Response of All-pass Lattice Network

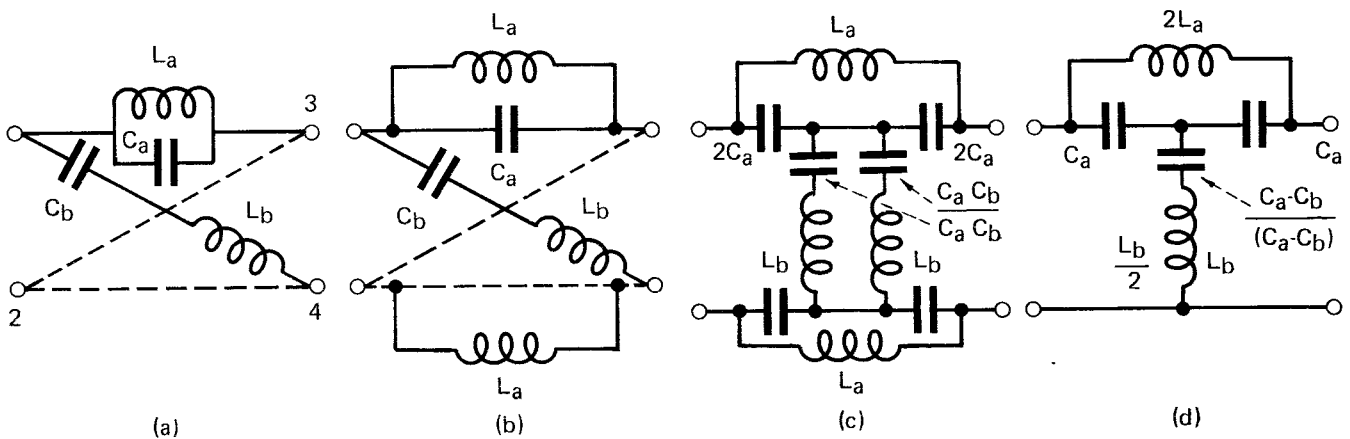


FIGURE 23. Transformation of Lattice Network to Bridged-T Network

response can be tailored separately to the amplitude response. It is probably, however, only to be considered for use in new designs. It will give a response that is not only superior but also much more reproducible, and cannot be mis-aligned by service engineers with inadequate equipment.

Eye Height. The most useful indication of data quality is given by 'eye height'. A basic system diagram for eye-height measurement is shown in Figure 24.

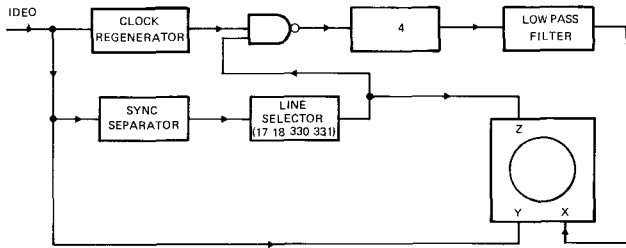


FIGURE 24. Measurement of Eye Height

It is necessary to regenerate the clock from the incoming data. This clock frequency is divided by four, and harmonics removed by a low pass filter to give a sinusoidal waveform. The latter is used as the timebase for the oscilloscope. Four clock periods are displayed. Video is applied to the Y input, and the display is gated on the oscilloscope Z input to ensure display only during data. The display is of the form shown in Figure 25.

The Eye Height is expressed as the percentage $(h/H) \times 100$. The name 'eye height' for this percentage is derived from the fact that the shape of the hole in the middle of the display, which gives the difference between the highest level of a logic '0' and the lowest level of a logic '1', approximates to the shape of an eye. Distortion of the signal will reduce the difference between these two levels. In order to measure eye height it is necessary to integrate the display to include all possible combinations of data. This may be done either with a storage oscilloscope or a scope camera.

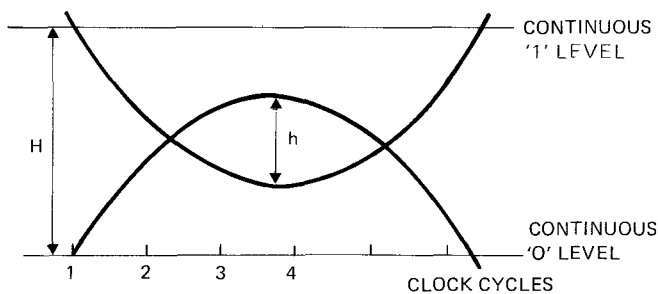


FIGURE 25. 'Eye Height' Display Form

Demodulator. The type of demodulator used will also affect data quality. T.v. signals are transmitted using a vestigial sideband signal. At high modulation frequencies this behaves like a single sideband signal, and has an envelope given by

$$E = (1 + m \sin pt + m^2/4)^{1/2}$$

where m = modulation depth

p = angular frequency of video sinewave

$$= 1 + \frac{1}{2}m (\sin pt + m/4) - \frac{1}{8}m^2 (\sin pt + m/4)^2 \dots$$

As long as $m \ll 1$ this is close to the original video waveform. However, Teletext is modulated to 40% ($m = 0.4$) and t.v. receivers contain filters that reduce the carrier level by 6dB making the effective modulation index 80% ($m = 0.8$). The effect of this on the demodulated waveform may be seen in Figure 26, where there is a change in instantaneous level of up to 10%. The effective modulation depth is reduced by adding a large carrier component to the signal, as is done in a synchronous demodulator.

Thus it is advisable to use a synchronous demodulator if at all possible. Receivers using envelope detectors may give reasonable results with good signal conditions but immunity to signal degradation of any sort will be reduced.

Connection to Module. The video signal may be taken from any suitable point after the detector, preferably using a buffer to avoid loading the existing receiver circuits. The video connection should be made using a screened cable, which should be reverse terminated to reduce reflections as shown in Figure 27. Use of the 56 ohm resistor may not be necessary if the connecting cable is short.

The video input level to the XM-11 should be capable of adjustment over the range 1.0 to 2.7V. At any one power supply voltage there is a wide range of video input level over which the module will give acceptable performance, but this range differs for different power supply voltages and for different modules. The extent of the range will be dependant on the quality (eye-height) of the data signal.

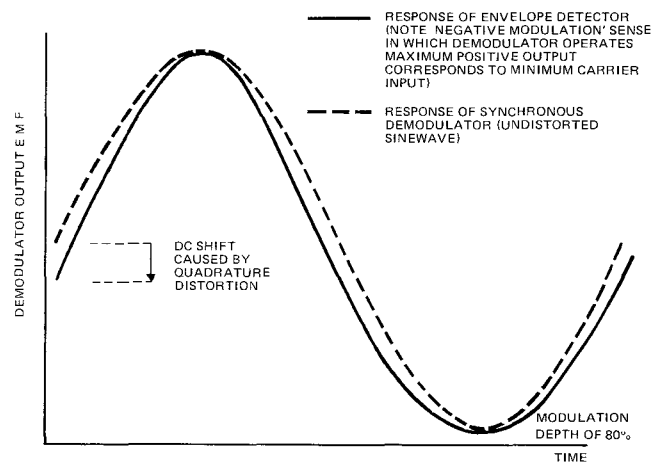


FIGURE 26. Response of Envelope and Synchronous Demodulators to a Sinusoidally - Modulated Single-Sideband Signal.

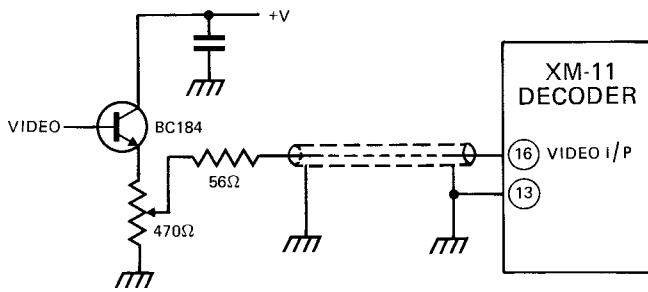


FIGURE 27. Video Output Interface Circuit

For operation at severely degraded eye heights each module will have an optimum video input level which will be dependant on the power supply voltage, the module itself and the characteristics of the video and i.f. circuits of the t.v.

Line Flyback Pulse

The line flyback pulse may be conveniently taken from a low voltage supply winding on the line transformer. A 20-30V supply winding will have a negative pulse of about 200V on it (see Figure 28). The actual value is not

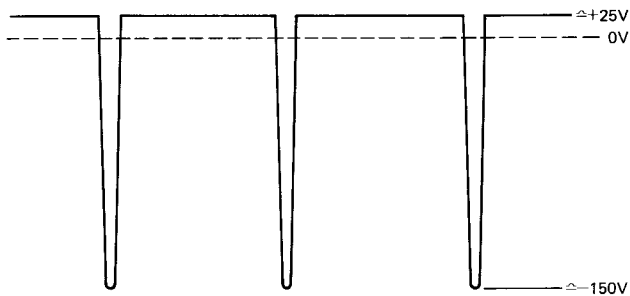


FIGURE 28. Line Flyback Pulse Waveform

critical, but the pulse must be negative with respect to ground, and an external resistor must be used to limit the pulse current to about 3mA. The pulse should be fed to the module using a screened cable, which is earthed only at the receiver end, to avoid earth loops with the video earth. This cable will capacitively load the output resulting in a CR time constant which will delay the pulse, resulting in a displacement of the display on the screen. This problem may be overcome by putting half the resistance at each end of the cable and using a speed-up capacitor as shown in Figure 29. The value of the speed up capacitor may be optimised by viewing the position of the text on the screen. The module line flyback input has an input resistance of about 22kΩ, and calculations of series resistance should allow for this.

The line flyback pulse is used to synchronise the teletext display as this results in less jitter than a system which generates a line pulse from the video input signal.

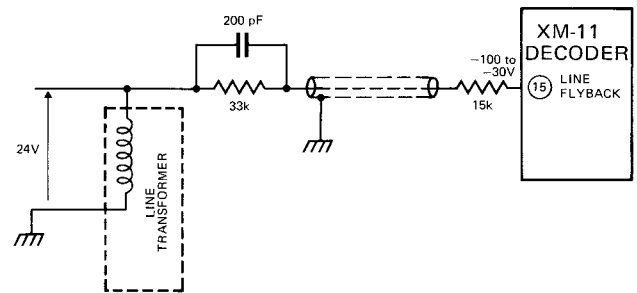


FIGURE 29. Line Flyback Pulse Interface

However, in some applications of the decoder, line flyback may not be available. In this situation, a line pulse must be generated separately. The decoder acts only on the first falling edge of the negative pulse, which should occur within 0.5μs of the end of the active video signal. Mark/space ratio is not critical provided that the negative pulse is at least 8μs wide. If the line flyback input is generated in this fashion, it is possible that a large negative pulse is not easily obtained (a pulse of at least -25V w.r.t. earth is required). Provision is made on the board for the addition of a resistor (R25) which may be used to reduce the input resistance by shunting the 22kΩ input resistor, and hence the required voltage.

The line flyback input must be provided even if the module is used to capture data only. This is possible if a 'standby' mode of operation is incorporated for the capture of time coded pages when the user is not actually watching television, and only the small signal circuits are under power.

Keyboard Connections

Control instructions are given to the decoder by using the 4 input wires and 4 output wires in a scanning matrix, as shown in Figure 30, and decoded according to the

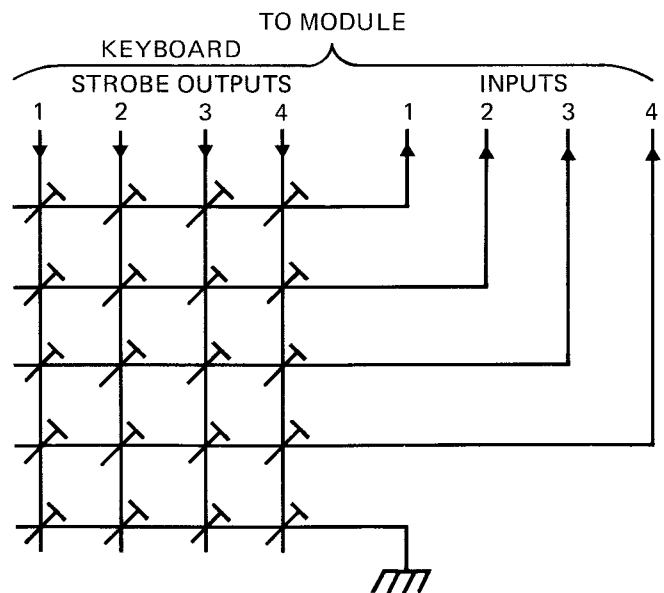


FIGURE 30. Keyboard Matrix

Table 2. Keyboard Matrix Decoding

Lines	Outputs	1	2	3	4
Inputs		0	4	8	Text
1		0	4	8	Text
2		1	5	9	Mix
3		2	6	Page	Pict.
4		3	7	Time	Update
E	Reveal	N/A	N/A	N/A	N/A

matrix in Table 2. All strobe outputs, and inputs are normally held at a t.t.l. high level by means of 5kΩ internal pull up resistors. During one t.v. line in each field, each output has a negative pulse approximately 12ns in duration. These pulses are time-shared, as shown in Figure 31.

The pulses in Figure 31 are repeated on each output at field rate, i.e. every 20ms. In order to give a command to the decoder, one of the output pulses must be transferred to one of the input lines for at least 2 and preferably 3 field periods in order to allow the internal 'de-bounce' circuitry to function correctly. Similarly there should be a time interval of 2 or 3 field periods between instructions.

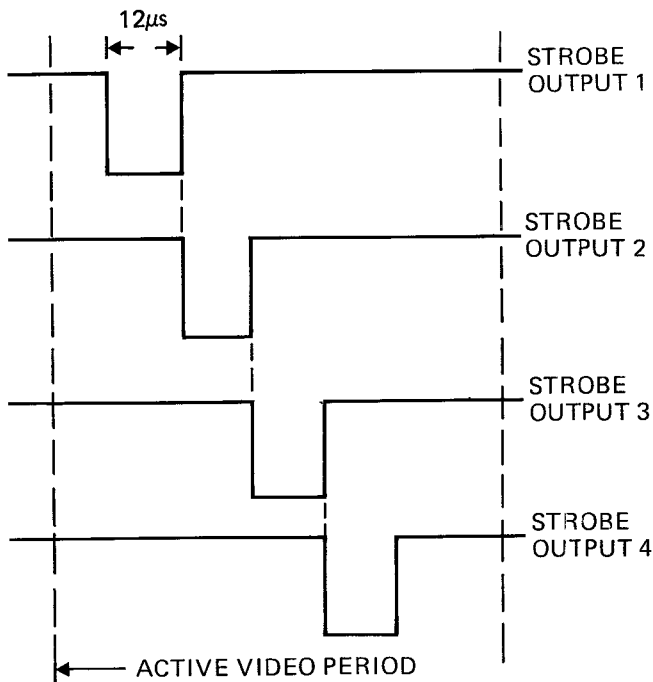


FIGURE 31. Keyboard Strobe Pulses

The 'Reveal concealed display' command operates in a different manner however. Instead of transferring a pulse from an output to an input, strobe output 1 must be held at a t.t.l. 'low' level for 3 fields.

The simplest way of controlling the keyboard matrix is by use of a hardwired keyboard using mechanical switches.

It may also be possible to use solid state analogue switches instead of mechanical switches. However, the maximum allowable series resistance in the keyboard lines is 100Ω and many devices of this type do not achieve this. The switches should be connected to the module using an 8 cored screened cable. Up to 1nF of capacity may be connected to each of the keyboard connections corresponding to about 6m of typical multiway cable. Care should be taken to insulate the connections from the possibility of static discharge. (With the prevalence of synthetic carpets nowadays, it is quite possible for the operator to charge to -25kV and if applied to the keyboard connections this voltage is likely to cause failure of the module.)

Many available keyboards do not have a matrix arrangement, but instead each contact connects one line to a common terminal, thus the keyboard has (n+1) connections, where n = number of keys). This arrangement can be used with a transistor at each matrix point as shown in Figure 32 for one of the keyboard strobe outputs.

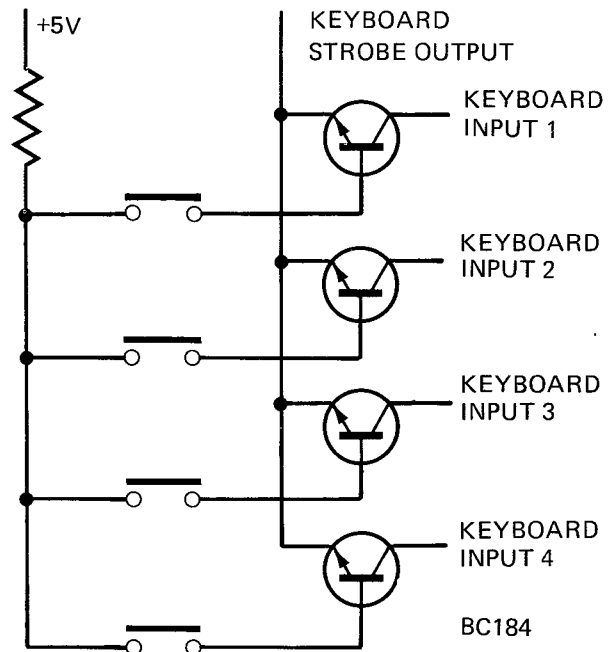


FIGURE 32. Use of n-Line to Common Keyboard

A similar arrangement can be used for initialization at switch-on. When first switched on the decoder may start in either picture or mix modes. In order to ensure initialization in the picture mode the circuit in Figure 33 may be used.

Remote Control. The keyboard connections to the TIFAX XM-11 module have operating conditions compatible with standard t.t.l. making it relatively straightforward

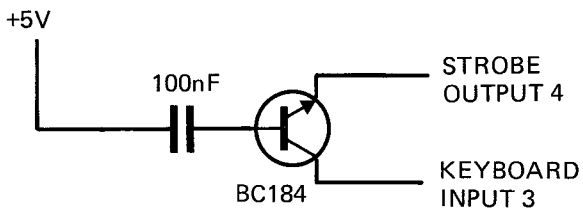


FIGURE 33. Picture Initialization Circuit

to interface with any remote control system, either ultrasonic or infra-red. Most remote control systems generate a 5 bit word for each control function; this must be decoded to transfer strobe output pulses to the keyboard inputs. The first 6 ns of the strobe output pulse are not active, giving a margin for propagation delays of external circuitry.

If remote control is used, it will probably be combined with the normal t.v. functions. In order to keep the number of buttons on the keyboard to a minimum, and also since many remote control systems have only 30 channels, some multiplexing will be necessary. The number keys 0-9 will probably be used for teletext control and channel change with an inhibit circuit to prevent channel change during teletext control. Many arrangements are possible and choice is very much up to individual preference.

Blanking Output

The blanking output must inhibit the picture drive to the video output stages. When operating in the 'Text' mode, the blanking output is 'high' at all times during display of a full page of text. If the page selected consists of a boxed display, such as a newflash, or subtitles, the decoder automatically switches to a picture display and the blanking signal is 'high' only during that part of the scan necessary to produce the box.

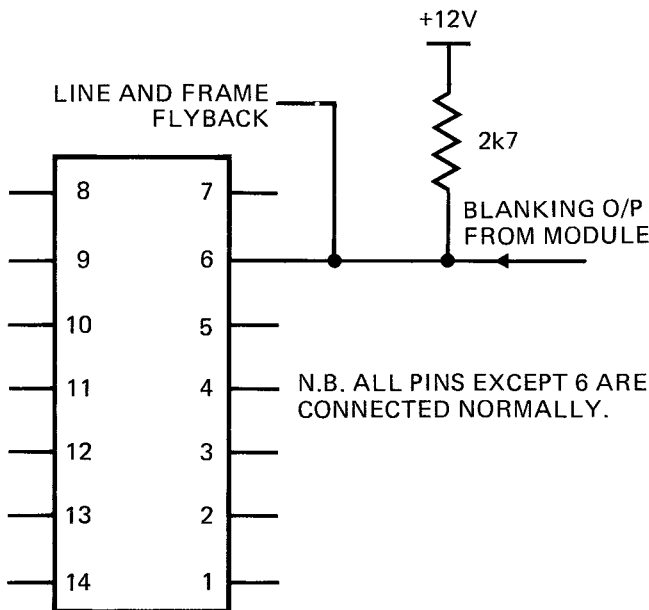


FIGURE 34. SN76227 Blanking Interface

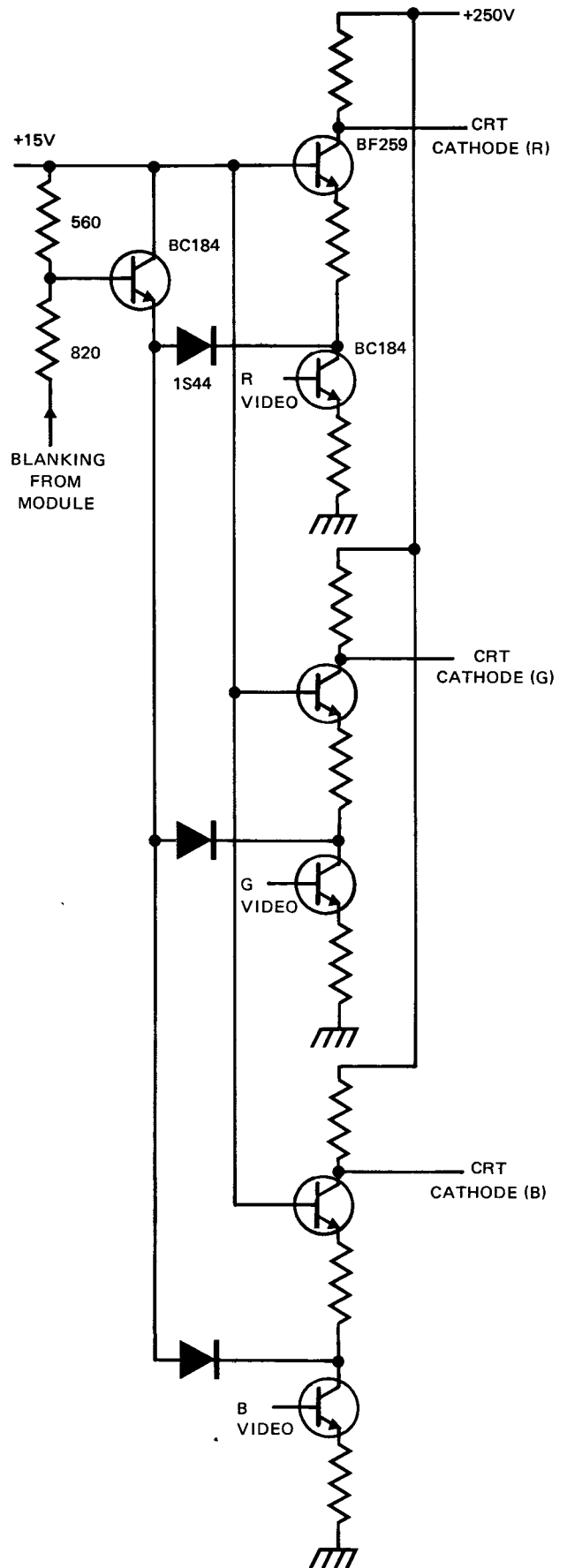


FIGURE 35. Blanking Interface with Cascode Video Output Stages

The blanking output of the module consists of an open collector transistor with a 470Ω resistor in series with it. The resistor is included to protect the output transistor. In some applications (e.g. driving standard t.t.l.) the resistor may make circuit design difficult. Provision is made on the board for the addition of a shorting link across the output resistor (R20). However, it is recommended that the resistor is left in circuit if possible.

In receivers using the SN76227 i.c. (double balanced chroma demodulator) the blanking signal may be applied to the blanking input on the i.c. (pin 6). A suitable interface circuit is shown in Figure 34. In receivers that do not use the SN76227 it may be necessary to blank each of the R.G.B. video amplifiers separately. If this is done, the three blanking signals must be fed through diodes to avoid interconnecting the video amplifiers. An example of blanking interface circuitry into a cascode output stage is shown in Figure 35.

Receivers with colour difference outputs will probably need the luminance signal blanked in addition to the difference signals. This is a particularly suitable application for the use of analogue switches which are another popular method of blanking.

An extension of the blanking function may be used to facilitate the 'Mix' mode of operation. This mode of display has two problems associated with it. The first is that circuit design can become complicated in order to avoid saturation when text and normal video are summed together. The second problem concerns the legibility of the display being very dependent on the picture content. The Teletext characters, which are all white in the 'Mix' mode, cannot be seen against a light background.

The blanking output of the XM-11 may be summed with the Monochrome output, and presented to the t.v. as a composite blanking signal. In the 'Mix' mode, this will create character shaped 'holes' in the picture. This avoids the problem of saturation, and also, provided that circuit timing is correct, gives a black 'shadow' to the characters which considerably improves the legibility.

Video Output Interface

Colour Receivers. The RGB outputs of the module consist of open collector transistors with 470Ω series resistors. Provision is made on the board for the addition of wire links to short out the resistors (R16, R17, R18) for applications where their inclusion presents design problems. However, as with the blanking output, it is recommended that the resistors are left in circuit where possible.

The RGB outputs may be very easily interfaced into cascode video amplifiers. The configuration shown in Figure 36, shows the simple modification necessary for each video amplifier in this arrangement. Blanking may be achieved as described earlier.

The open collector outputs of the TIFAX module give an extremely flexible configuration capable of driving a variety of different circuits. A simple method of interfacing with a common emitter output stage is shown in Figure 37. The video input must be blanked as described earlier. In Figure 37, transistor VT2 must be a high voltage video

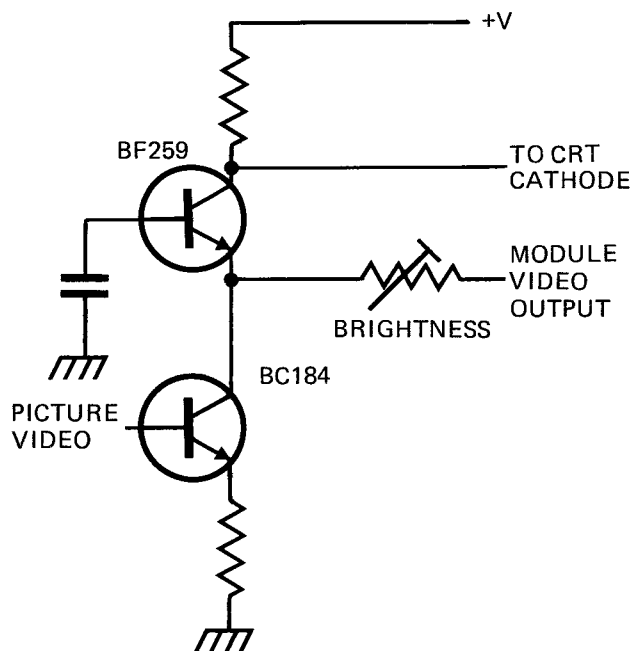


FIGURE 36. RGB Cascode Video Output Interface

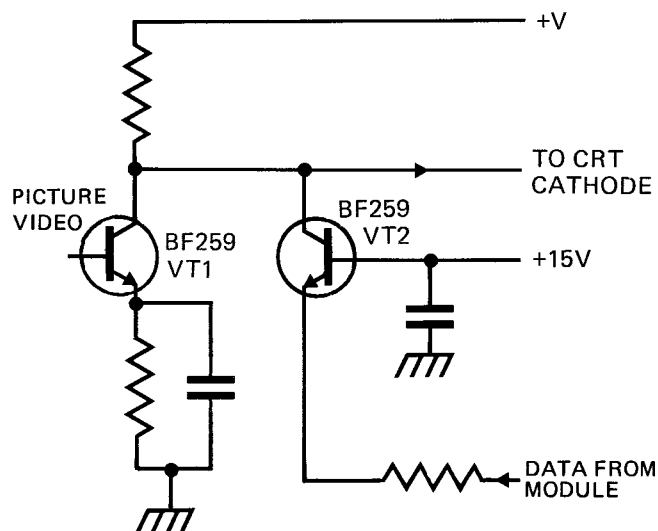


FIGURE 37. Common Emitter Output Interface

transistor. This method does add some extra capacity at the c.r.t. cathode drive point, but in practice does not give any visible degradation of picture quality on receivers with good h.f. response that are modified in this way.

As mentioned earlier, long wires and earth returns in the video output interface can give problems in sensitive parts of the receiver due to pickup of radiation at video frequencies. This problem can be overcome at the expense of circuit complexity by using separate logic and video earth paths as shown in Figure 38. In this circuit the logic earth and thus the logic circulating current is separated from the video current, substantially reducing the effect of the long earth path. An additional feature of this circuit is the use of feedback via resistor R_F to define the full white level in the Mix mode.

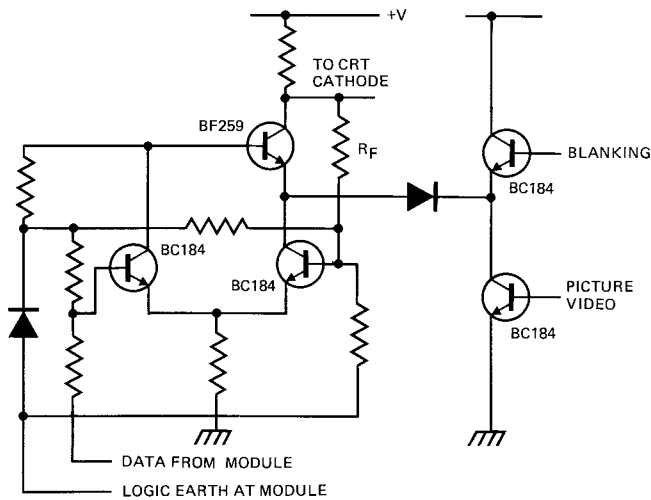


FIGURE 38. Cascode Video Output Interface
(Separate Video and Logic Earth Paths)

Monochrome Receivers. A separate output is available for feeding the video output stages of monochrome receivers, which operates in a similar manner to the RGB outputs. All colour information is removed, however, and all characters and graphics will be displayed in white against a black background. Black characters on a white background can be achieved with simple additional circuit. Blanking of the picture video is still required, and will probably need applying to the output stage. A typical monochrome video output interface is shown in Figure 39.

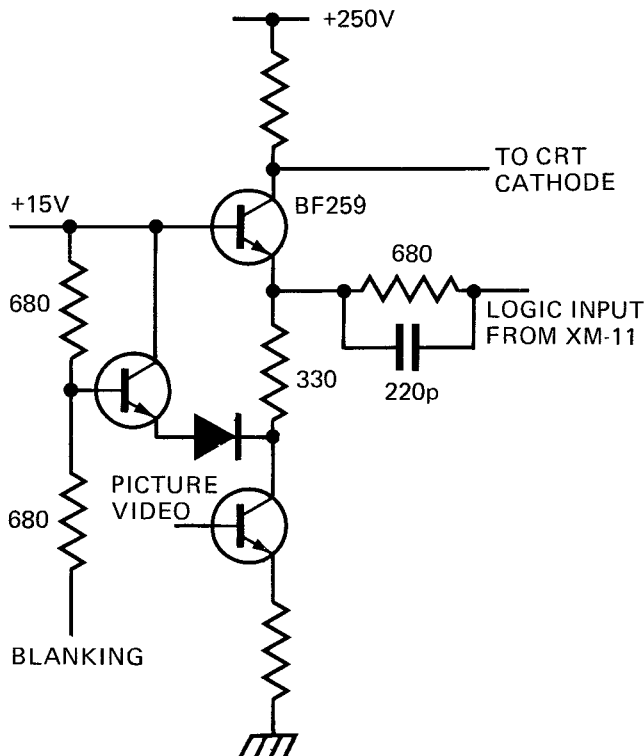


FIGURE 39. Monochrome Output Interface

Sound Muting

It may be considered desirable to mute the t.v. sound signal during display of teletext. This may be conveniently achieved by deriving a muting voltage from the XM-11 decoder blanking output. Other methods are possible (e.g. use of the keyboard 'Text' instruction) but use of the blanking signal has the advantage that it is easy to retain sound during boxed displays such as newflash or subtitles.

A simple RC time constant as shown in Figure 40 will give a d.c. output proportional to the blanking signal mark/space ratio. During display of picture, or when text is superimposed on picture, there is no blanking output.

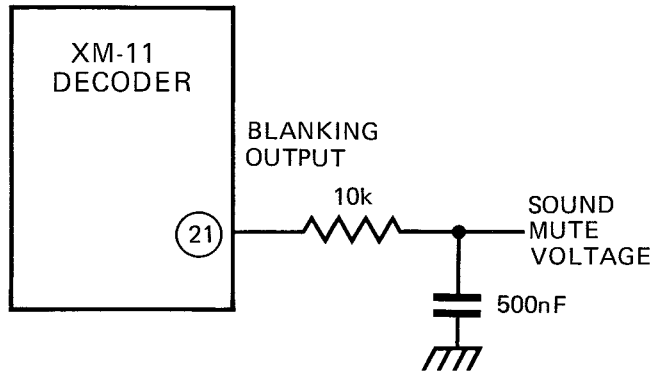


FIGURE 40. Sound Muting

During display of a full page of text the blanking output is 'high' for approximately 80% of the time. If a boxed display is present when in the 'Text' mode, the blanking output will be high only during that part of the scan necessary to produce the box. Thus if the box is $\frac{2}{3}$ of the picture width and $\frac{1}{6}$ of the picture height, the blanking voltage will be high for a percentage of time given by:

$$80 \times \frac{1}{6} \times \frac{2}{3} \approx 9\%$$

A simple level sensitive switch may be used to ensure that sound is muted only when a full page of text is displayed.

REFERENCES

1. *Specification of Standard for Broadcast Teletext Signals*; BBC, IBA and BREMA; January 13, 1976.
2. B. Norris & R. Parsons; "Teletext Data Decoding - The L.S.I. Approach"; *IEE Transactions on Consumer Electronics*, August 1976, Vol. CE/22 No. 3, pp. 247-252.
3. F. E. Terman, *Radio Engineers Handbook*, McGraw-Hill Book Co., New York & London, Section 3, pp. 135-, 1943.
4. *Broadcast Teletext Specification*; BBC, IBA and BREMA; September 1976.

ASSOCIATED PRODUCTS

The DM-11 Direct Memory Access Module

The DM-11 module provides all the facilities of the XM-11, but has the additional feature that a signal on a single control pin effects a complete changeover from the Teletext mode to an external data mode of operation. The page memory is then made directly accessible to seven bit parallel data. Memory addressing is in the form of a six bit column address and a five bit row address. External data may be written into the memory and stored data may be read out. In addition status signals are provided to enable proper timing of read/write operations and cursor generation/insertion.

This module may be used to display from Viewdata, data from cassette recorders, microprocessors, games etc.

The XM-11 DH TIFAX Module with Double Height Character Facility

Since the design of the XM-11, several new control characters have been added to the Teletext specification,⁴ including the facility for displaying double height characters. In most applications this feature is not essential, particularly since the change in the specification is made in such a way as to ensure compatibility with decoders not reacting to the double height control. However, where the Teletext system is used primarily for sub-titling, the use of double height characters becomes more important. For this type of application, the XM-11 DH module has the ability to decode the double height control character when transmitted. The subsequent letters/numbers or graphics are then displayed in double height format until the normal height control character is received or until the end of the row.

Alternative Character Founts

As stated, the r.o.m. used in the TIFAX range of products is mask programmable to allow for alternative character founts for use in countries other than the U.K. A version of the r.o.m. which generates a Swedish set of characters is available (SN74S263) and others will be produced when required.

Remote Control Interface I.C.

A mask-programmable i.²l. i.c. is available, development number TX010, which is designed as a remote control interface for the XM-11 module. This will allow operation with any system using a 5 bit control word. It operates from a 5V supply, has a low power consumption – typically 40mW, and is available in a 16 or 18 pin d.i.l. package. Its open collector outputs allow the device to be wired in parallel with an existing keypad if required. A latched output (Channel Change Enable), is provided to ensure that channel changes are avoided during the selection of pages of text. The output is set to a logic 'low' when either 'Text' or 'Mix' is selected. The latch is reset to logic 'high' by either 'Picture' or 'Update' and the i.c. incorporates a power-on reset circuit.

Microprocessor Control of T.V. Peripheral Circuits

It is apparent that microprocessors now present a viable and economic solution for the control of t.v. peripherals. For example, the TMS 1100 microprocessor can be programmed to remotely perform the following functions:

- ★ Channel selection
- ★ Band select
- ★ Programmed viewing
- ★ Channel Tune Up/Down
- ★ Display time and channel number
- ★ Clock set
- ★ Colour Up/Down
- ★ Volume Up/Down
- ★ Brightness Up/Down
- ★ Reset
- ★ Sound Mute
- ★ Cancel program

The XM-11 module may be combined with such a system using the remote control interface i.c.

PRODUCT SUMMARY

Product	Description	Ordering Code
XM-11	Standard TIFAX module meeting January '76 Teletext Specification.	N700
XM-11/S	TIFAX module with Swedish character R.O.M.	N705
XM-11 DH/E	TIFAX module with double height character facility and standard English characters.	N706
XM-11 DH/S	TIFAX module with double height character facility and Swedish characters.	N703
DM-11	Direct memory access module	N702



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