Wireless World Teletext decoder

1 — The background

by Philip Darrington

The first of a series of articles on the Teletext television information display system and the construction of a decoder for use with domestic television receivers.

In succeeding articles of this series we shall describe the design and construction of the *Wireless World* Teletext Decoder. But, before we do that, it seems only sensible to make sure that readers are up to date with current activity in the field and have an idea of other systems which have been proposed. We will also describe the basic operation of Teletext and mention the techniques used to decode the transmissions for display on a domestic television receiver.

In the early years of "wireless", the vision of millions of people being entertained by transmissions was just not credible. Television was thought to be sheer science fiction and wireless itself was for the transmission of vital information. Even if it had been possible to communicate phonically, that was not the idea at all – ships were the real users of radio and if amateurs could derive pleasure from listening to marine morse traffic or Eiffel Tower time signals, so much the better.

Then, of course, radio telephony was developed and the entertainment possibilities were recognized. It is now an extraordinary and rather depressing fact that out of the few thousand megahertz available for radio transmission, nearly 600MHz are taken up by broadcasting stations, most of which put out entertainment of one sort or another. Sound is reasonably restrained in its use of bandwidth, but television occupies 566MHz – a staggering figure, particularly as the television signal contains so much redundancy. Anything designed to make better use of this signal is to be welcomed and Teletext is one way of doing that, in that a previously unused part of the waveform is used to transmit more information.

Many ways of using television transmissions to better effect have been proposed[1, 2]. Since the early sixties, test signals inserted in the field blanking interval have been in common use, and have been supplemented by coded data transmitted on lines 16 and 329 of each frame[3]. It apparently did not, at the time, occur to ORTF, who originally used the system, that the technique could be developed to allow the transmission of visible information, but the system was used for switching remote transmitters, identification for remote supervision purposes, etc.

Other systems of transmission aimed at "still" display, with or without sound and in colour or monochrome depend on the exclusive use of a television or sound channel. For instance, the NHK "A" system[4] is able to carry over 50 channels of colour still pictures, with sound, in the bandwidth of one normal television channel. The pictures are transmitted at the rate of one still per frame, together with a code to enable a magnetic disc memory in the receiving equipment to record a selected frame, which is then continuously replayed. Sound is multiplexed with video information and transmitted in the frame intervals.

The NHK "B"[4] system falls into the multiplexed television channel category, using uncoded signals. Three unused lines per field are used to transmit three lines of a still picture, which is magnetically recorded at the receiver. Sound is transmitted by the use of additional sound carriers at low level, spaced further in the spectrum from the vision channel than the original sound carrier.

In 1971, W. D. Houghton of RCA described the Homefax[5] system in which additional information was multiplexed with a broadcast television waveform to produce "hard copy" from an electro-optical printer, using a cathode-ray tube to produce the "printing" on Electrofax paper. The information, uncoded, was carried in an unused vertical interval line and transmitted in the normal way – each of these lines producing part of one line of a row of print on the receiver paper. Transmission tests of this system had been carried out in 1967, and improvements were being carried out in 1970. A method of data transmission not using the vertical blanking interval[6] was described by P. T. King of Hazeltine Research, Inc., at the SMPTE Technical Conference in 1973. In this system, known as an "add-on" type, a low-level subcarrier was inserted on the vision signal at an odd multiple of half the line frequency, a method which is well known in colour television circles as a method of avoiding interference between two signals in a common waveform. The added signal is shifted in phase from line to line and the visible effects are reduced. The actual frequency is chosen to be between 2 and 3MHz in the NTSC standard, because radiated energy is at a minimum in that region in a typical picture. The data signal is biphase modulated at 21 kilobits per second and at the receiver is synchronously detected, the data decoded and used to operate a character generator, which can, for example, produce subtitles in languages using the characters available.

These two techniques – the use of previously blank lines in the vertical blanking interval and the provision of a character generator at the receiving end – paved the way for Teletext. A system of this kind is able to carry more information, more flexibly, by leaving the receiver to do rather more of the work than an analogue or uncoded digital system. If the transmitted signal is made to carry instructions to the receiver on what to do, the receiver can then hold much of the information in store, releasing it when commanded to do so.

Peter Hutt of the IBA described an embodiment of this principle in a paper read to the IPC, 1972[7]. The system was named SLICE and was primarily intended for the labelling of programmes with a source identification. The information was carried on lines 16 and 329 in the form of 112 binary digits per line and, at the receiver, was read

into a memory where a complete message was assembled. SLICE was the fore-runner of ORACLE and CEEFAX. (Hutt mentioned the possibility of a domestic information service in his paper.)

Teletext

ORACLE was developed by the Independent Broadcasting Authority in the light of its experience with SLICE and the BBC announced their own system, which was very similar and bore the name CEEFAX. (ORACLE is an acronym — Optional Reception of Announcements by Coded Line Electronics — CEEFAX is See Facts as pronounced by an adenoidal dyslexic.) There is little profit in trying to decide which organization hit upon the idea first, or which was on the air first, as the two were quickly and sensibly to agree on a common standard of transmission, in conjunction with BREMA[8]. Both names will probably continue to be used for each organization's broadcasts, but the generic term "Teletext" is now common, and will be used henceforth. Teletext has been broadcast on the present standard since September 1974 — the beginning of a two-year experimental period. The system uses a multiplex-with-vision type of transmission and uses lines 17 and 18/330 and 331 to carry coded information. There is no accompanying Teletext sound.

Before proceeding further, a look at the facilities offered by a Teletext transmission and a résumé of some of the specification will be a help when considering the equipment needed in the receiver. Briefly, the Teletext page consists of 23 rows of 40 characters each, plus a page header, which is only partly displayed. As seen in Fig. 1, the header gives the name of the service (Ceefax or Oracle), the page number, the date and the time. The time display is continually changing and is always visible.

Visible characters are either capitals or lower-case letters assembled on a 7 × 5 dot matrix and in one of six colours or white: diagrams or low-resolution "pictures" can be assembled by the use of a block of cells on a 3 × 2 pattern, each of which can be "on" or "off", in colour. A variety of other symbols (commas, brackets, @, £, etc.) can also be shown, and the set of characters is known as the ISO-7 code, which is a version of the ASCII code with some of the "National usage" characters substituted. Characters can be made to flash on and off, though our own feeling is that this will be used rather less when the service is finally in use than it is now, if it infuriates other people as it does the writer.

The Teletext editing teams can use the pages in three different ways, the norm being single pages which appear when selected by the viewer at any time and which are up-dated perhaps once or twice a day. A second type is one of a group of, perhaps, four such pages which change at about one minute intervals. They will usually be on a related topic, such as sport, and are identified by the letters A B C or D, the relevant letter being in a different colour so that the viewer knows which point in the set of pages has been reached. This type is really the same as the first variety, but pages are changed automatically at minute intervals. The third kind of page can be selected by the time-code on the header, so that it can be received, placed in store and read out at a convenient time.

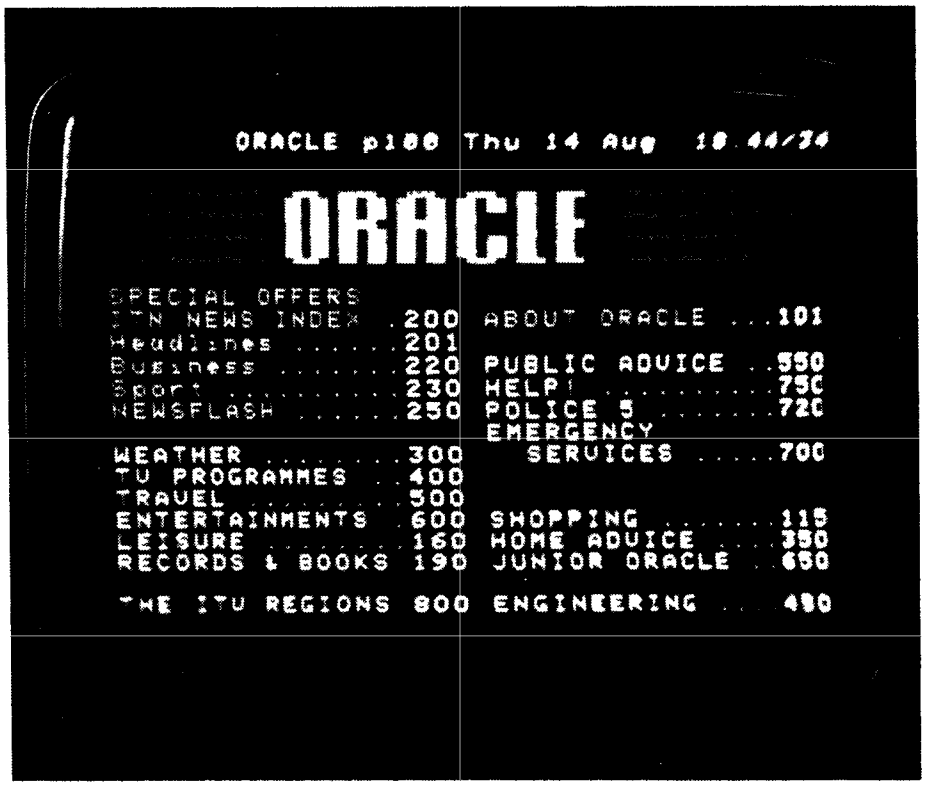


Fig. 1. The main index page (p. 100) of ORACLE for August 14, 1975, produced by the W.W. decoder on a Thorn colour receiver.

The data to be displayed can be presented as a complete page or, in the case of news flashes or subtitles, can be inserted in a blank rectangle on the screen, leaving the rest of the picture visible. The full page can be superimposed on the picture, but in our experience this is a good way to ruin one's eyesight.

A typical magazine has the capacity of 100 pages. Four lines are transmitted per television frame and there are 24 lines per Teletext page. A full magazine would therefore take 600 frames or 24 seconds to cycle. The BBC and IBA appear to differ on what they consider acceptable access times; the BBC suggest a typical time of 12 seconds (for an unspecified number of pages) while a recent check on Oracle gave an access time of 28 seconds for well over 100 pages. The theoretical time can be reduced considerably by not transmitting blank lines, a practice which is already followed by the IBA and which the BBC intend to change to shortly (they already omit blank lines at the bottom of a page).

To select a Teletext page, one first switches the signal path through the decoder, selects a page by means of thumbwheel switches or a set of push-buttons and waits for the selected page to be assembled.

Teletext signal

The method of transmission of the Teletext data is of interest at this point. As has been said, the data signals are carried by lines 17 and 18 and the corresponding lines in the alternate field, 330 and 331. The choice of lines is influenced by the need to avoid the early part of the vertical blanking interval and the few lines near the start of the video signal (lines 23 and 336). If early lines were used, it is possible that data would appear on the field flyback on some receivers and if lines later than 18/331 carried the information, receivers with incorrect picture height adjustment or with a downward-shifted picture might show the data as an extremely "busy" pattern of dots at the top of the screen – this sometimes occurs even with the present line allocations. A further reason for avoiding lines 19/332, 20/333 is that they are currently used for insertion test signals, which are often visible but, being static, are not obtrusive.

A form of binary code is used for the data, known as non-return-to-zero, which possesses the advantage over a complemented-element code of a reduced bandwidth requirement. As its name suggests, the resulting waveform is not a continuous train of pulses, but rather a series of voltage levels. A

typical sequence is shown in Fig. 2(b), where it is seen that a "1" level does not automatically return to zero at the end of the pulse and if the succeeding level is also 1, the voltage merely stays up — similarly with a succession of "0". One result of this is seen in Fig. 2(c) where a train of the form 0 1 0 1 0 1 etc. turns out to be a square wave at half the repetition frequency of the clokc. As transmitted the pulses are "raised-cosine" in form and the square wave becomes a half-clock-frequency sinusoid.

The diagram in Fig. 3 shows one line of the complete picture frame. A complete line occupies 64μs, of which about 12μs are taken up with the synchronizing pulse, back porch with colour burst and front porch. The first 40 of the 360 bits are concerned with clock synchronization (in a manner similar to that of the colour burst), a series of bits which constitute a "start" sequence and 16 bits for control and row address information. The rest of the line contains 320 bits for display and control. Figure 4 shows the layout of information in the line.

Coding

All transmission paths are subject to errors, and television has its share. Noise can be a problem, but the type of distortion caused by multipath propagation is perhaps the deadliest source of error. Both BBC and IBA have done work on this in the U.K., Sweden and Germany, and have come to the conclusion that Teletext transmissions are fairly robust, but require a good performance in the receiver. This relative invulnerability to attack is assisted by the application of code protection — additional bits of information transmitted with the data.

Code protection is applied in two levels. Data bits which are intended for addressing and control are heavily protected, while those used to produce the displayed characters are protected rather less. The transmitting authorities consider that the occasional error in, or rejection of, a character is not serious as it will quite probably be corrected on the succeeding transmission of the page, but that an error in an address would lead to complete nonsense and must be avoided in the presence of the average amount of noise and ghosting.

The character code is basically 7-bit ISO-7 and is protected quite simply by means of a parity bit, giving odd parity. This means that if the total of "1s" in the basic 7 bits is odd, the parity bit is "0". An even total of "1"s in the 7 bits dictates a "1" parity bit to maintain an odd overall total. On examination at the receiver, any byte (the name for a "word" of 8 bits) with an even number of "1"s is seen to contain one error and is rejected. Previously-correct words in a display will not, therefore, be overwritten by an incorrect one and the effect is a reduction in errors in succeeding pages. Double errors, preserving odd parity, are not rejected and will be written.

Address data bits, on the other hand, are more heavily protected by being transmitted in a type of code which will detect 2, 4 or 6 errors in the byte and will detect and *correct* a single error. This type of code was described by R. W. Hamming in a classic paper[9] in 1950, and is known as the Hamming code. It takes the form of four parity bits in positions 1, 3, 5 and 7 of the eight-bit byte (the addresses are in a four-bit code). Three of the parity checks are associated with groups of three of the four message bits and the overall parity check covers all message and parity bits. Failure of the overall parity indicates an error and the position of the error is identified by the checks on the groups of three bits. If the overall parity appears true, but the individual checks show that a correction is required, there will have been a double error and the byte will be rejected as unusable.

Figs. 3 and 4 indicate that the bits at the beginning of the line are not concerned with the displayed message. Three groups of bits are transmitted, of which one is two bytes (16 bits) designed to lock the receiver's clock in frequency and phase with the transmission, in a similar manner to the way in which the colour burst dictates phase in a colour receiver. The 16 bits are termed the *clock run-in* and consist of a train of 1 0 1 0 1s. It is a penalty of the n.r.z. code used that this run-in is necessary, as it entails a code which is not self-clocking. In other words, unless the data are of the 101010 variety, which conveys no information, the transitions do not occur at every interval, and the data pulses themselves could not be used as a clock source, if it were not for the choice of odd parity for the protection code, ensuring at least one transition per character, which can be used to refresh the clock generator. The 16-bit burst of 3.5MHz is also detected and used to identify the transmission as Teletext and not some other data system such as SLICE (IBA), ICE (BBC) or insertion test signals.

The second group of 8 bits forms the framing code, which is always the same and is used to indicate the start of the first 8-bit word. The order of bits used is 11100100 – an arrangement which is designed to avoid errors. A common way to detect the framing code is to pass all data through an 8-bit shift register and to examine the parallel outputs of the register. There will be only one step, when the register contains all eight bits of the framing code, when the above order of bits is present at the outputs of the shift register and gives a positive comparison with the "permanent" word used for detection. The framing code is shown in progress through the shift register in Fig. 6, which indicates that, even in the presence of bits from the clock run-in (c.r.i.) and succeeding information, a maximum of 5 bits "look like" the framing code. By means of more or less extensive circuitry, the framing code detector can be made to recognize the code in the presence of one error.

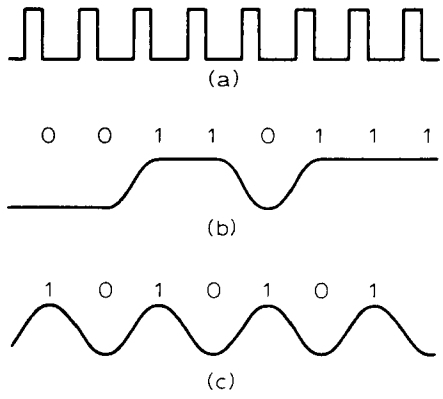
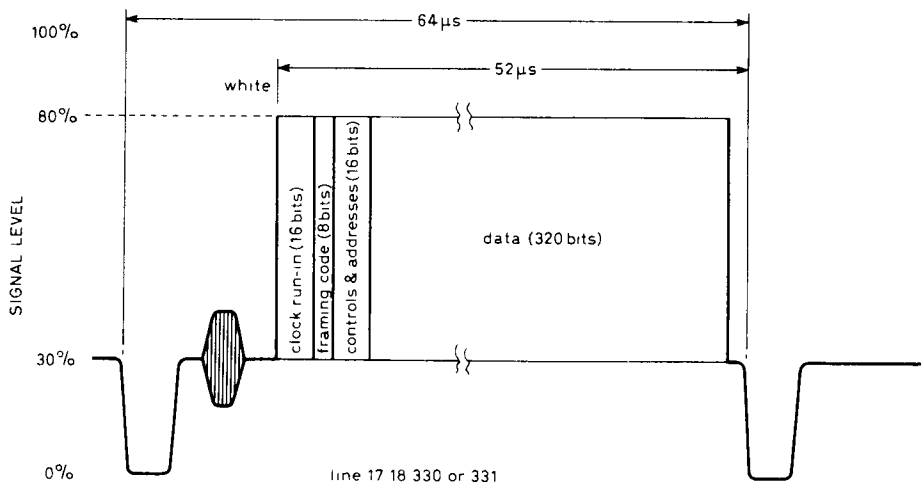


Fig. 2. The non-return-to-zero method of transmitting binary information is at (b) with the attendant clock at (a). A succession of 101010 etc. gives a half-clock frequency waveform and, if the pulse shape is a raised cosine, as used in Teletext, the result is a sinusoid at 3.5 MHz.

Fig. 3. A line of Teletext data. Sync. pulses are the 30% pulses and the colour burst is on the back porch.



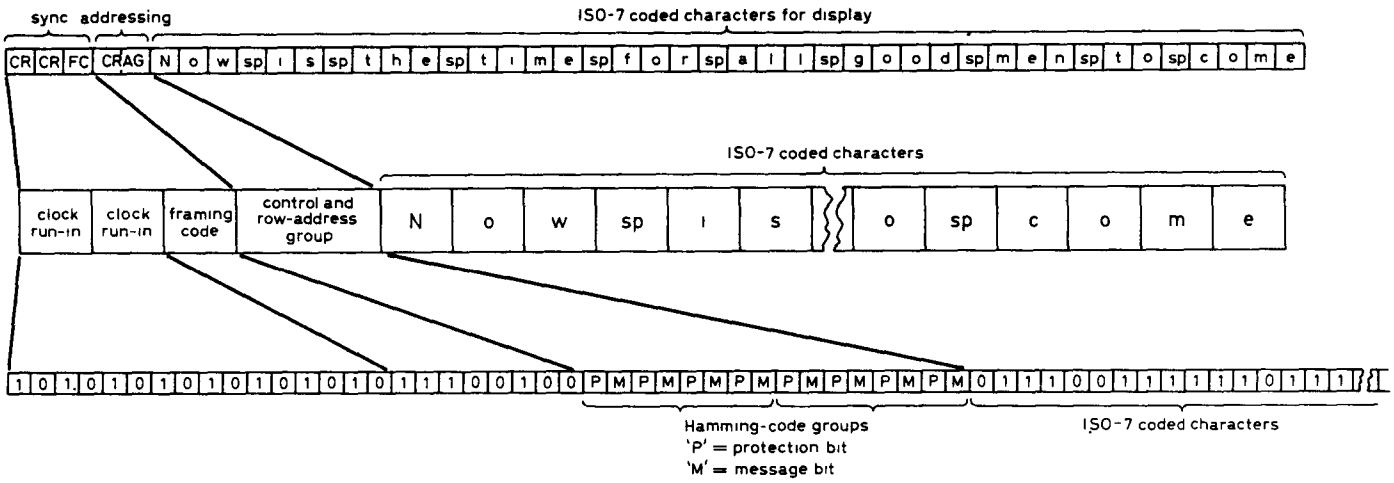


Fig. 4. A row of data It is seen that each group of 8 bits (1 byte) has a separate function. Clock run-in and Control and Row address each have two groups.

Row addressing. The 16 bits following the framing code are concerned with the identification of the following data. Each of the 24 rows of characters must be identified and this is done by numbering each with a row number from 0-23 and a magazine number (1 to 8). The bottom line of Fig. 4 shows the layout of bits in the 16-bit group and also indicates the fact that these are protected by being Hamming-coded. As, at the moment, we are not concerned with protection, the bits marked "P" can be ignored, and the groups become 4-bit words. In fact, this is an artificial distinction, because they form one word of three bits and one of five. The first group of three message bits (marked "M") identifies the magazine, and the remaining five contain the row address in a pure binary code (00001 is Row 1, 10111 is Row 23). The least significant bit is transmitted first.

Data. The rest of the line is filled with data for display, the previous bits not, of course, being visible on the screen. Fig. 5 shows the complete set (in use until Sept. 1, 1975) of available characters and blocks for graphic displays, together with the address code (bits 1-7). Bit 8 is the parity bit and plays no part in the display. A slightly modified table will be used exclusively after September, 1976, and the system is now in transition between the two.

Decoding

The circuitry for decoding Teletext transmissions is extra to that in an ordinary receiver and is mainly digital in nature. When the services are established and commercial receivers are sold (several firms already have models), the decoders will be built in, but before that happens, many viewers will want to convert their existing receivers, an add-on unit being the obvious solution, with video signals into and out of the decoder. U.h.f. input and output will probably not be used, the cost of a colour modulator, for instance, being prohibitive.

The extra circuitry needed can be considered in three groups; data acquisition, storage and output processing. The detected vision signal is taken from the television receiver, having been disconnected from the video amplifier, and taken to the decoder, where clock regeneration, framing-code detection, parity checking, serial-to-parallel conversion and page selection are carried out. The selected and organized information is then passed to a store (either a multitude of shift registers or a random-access read/write memory) until the selected page is assembled. When this has been done, the store addresses the character generator in the output processor (a read-only memory containing the ISO-7 characters) which indirectly drives the guns of the display tube.

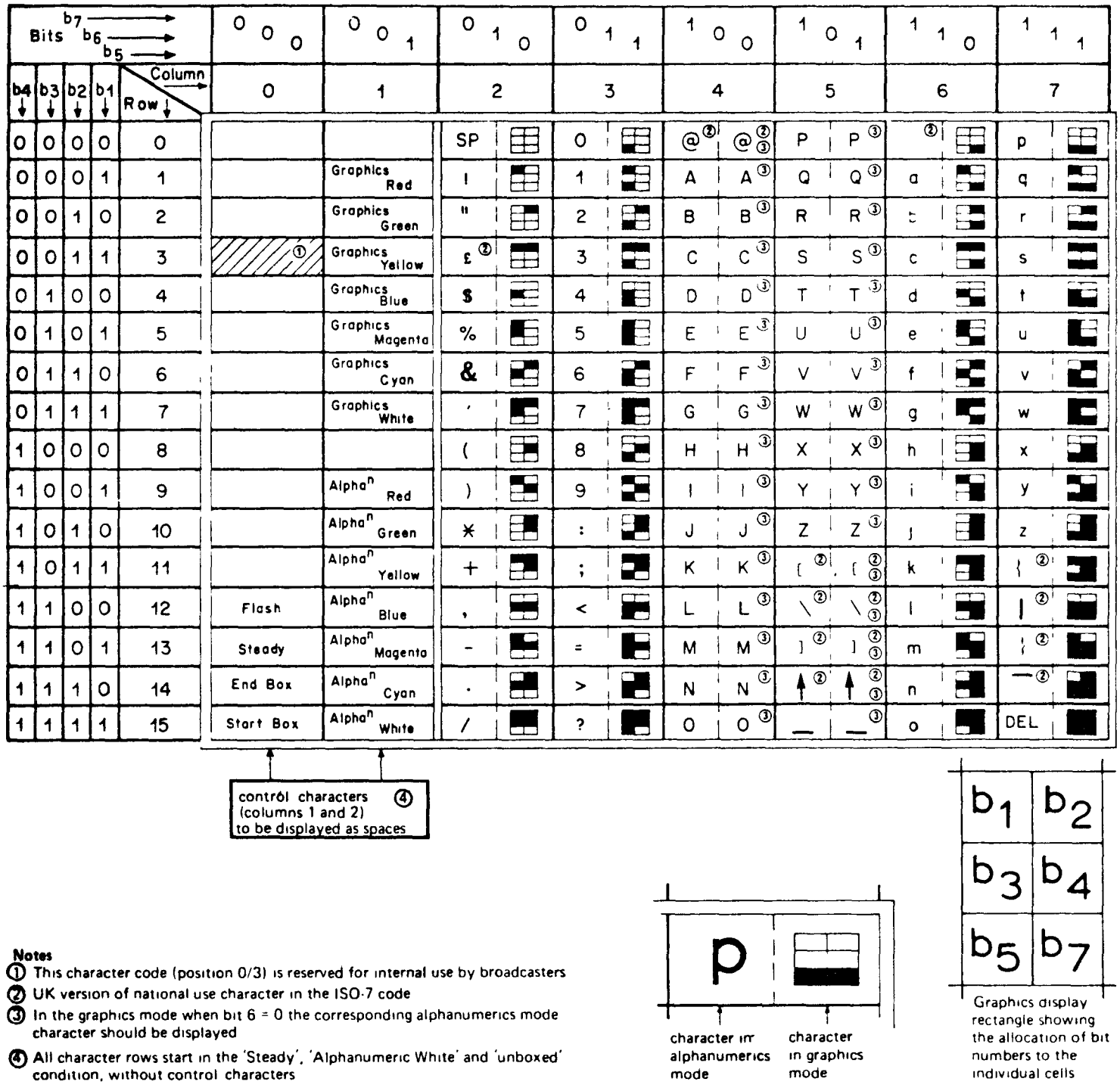
Input processor. This preliminary canter through the decoder is, of course, grossly over-simplified and a closer look at the sections is necessary, the first of these being the video processor which operates on the video signal to derive data and clock pulses. As has been said, the n.r.z. code in which data are transmitted, is not a self-clocking code and the decoder must contain its own clock. The clock run-in contained in the Teletext signal can operate as either a locking sequence for an oscillator which is continuously running, but which drifts out of phase with the Teletext clock between lines, or can be used to excite a passive oscillatory circuit which then rings for at least the duration of the Teletext line, being automatically in phase and frequency synchronization with the signal when the LC circuit is properly tuned. Each transition of the data "refreshes" the tuned circuit.

The diagrammatic input processor of Fig. 7 shows that the data is first passed through a serial-in, parallel-out store — the shift register, which is clocked at data rate. The register is 8 bits long and can contain one word, complete with its parity bit (4 parity bits in the case of Hamming-protected words). The 8 bits, in parallel, are examined by the framing-code detector for coincidence with the 11100100 "start" sequence which, when detected, resets a "divide-by-eight" counter to zero. The output of the counter is a pulse at one-eighth the rate of the clock and is used to identify correctly-framed words of 8-bit words in the shift register. In other words, framing-code detection indicates a reference point and the counter produces a pulse every eighth clock period which transfers the group of eight bits currently in the shift register, through latches, to the data lines. The output if the latch only changes when the counter indicates that the eight bits being presented to it are, in fact, a word. Complete characters are therefore presented on the eight, parallel data lines in serial form, reducing the 6.9375MHz rate to 867kHz.

The parallel data presented to the latches are also examined by the Hamming-code checker which, as was seen, can correct one error and detect 2, 4 or 6 errors in address and time information. Following this block, an 8-bit latch finds and holds the 3-bit magazine address and 5-bit row address, referred to in Fig. 4, after a two-character holding time, inserted to allow the two four-bit words (or one three-bit word and a five-bit word) to be assembled.

Parity checks on character words are performed by the parity block, operating from the main data line, its output determining the acceptability or otherwise of a word.

The rest of the input processor is concerned with the selection of a page by the viewer, who will be provided with three thumbwheel switches or a keyboard with ten number keys and keys for several other functions. A page having been "dialled in", the row address latch block examines the row address words until row zero is detected — the page header — when the selector will examine the following address information to compare it with the required page keyed in by the viewer. On detection of the required page code,



Notes

① This character code (position 0/3) is reserved for internal use by broadcasters

② UK version of national use character in the ISO-7 code

③ In the graphics mode when bit 6 = 0 the corresponding alphanumerics mode character should be displayed

④ All character rows start in the 'Steady', 'Alphanumeric White' and 'unboxed' condition, without control characters

Fig. 5. Characters possible in a Teletext display. Graphics are not in the ROM, being produced directly by the data bits.

the data which follows is written into the store, assuming that the parity checker is in agreement.

The outputs of the input processor are taken to the store and are (a) the 7-bit data (b) the "write" or "reject" command to the store (c) the row address and (d) the character address.

Store. Storage can take many forms, but the most convenient way to store the data while the page is assembled is the random-access memory, which is an array of semiconductor devices, often bistable circuits, set to "1" or "0" by input signals and which can be interrogated non-destructively when required by examining any desired location in the memory. No "order" is entailed: data can be lodged at any part of the memory.

Data are stored in 7-bit code as received from the 7-bit latch driving the data line in Fig. 7.

Display. The display of characters depends on the use of a large-scale integrated circuit — another form of store called a read-only memory. This is again an array of memory cells, but this time the pattern of bits read out of a given address in the memory is not under the control of the user. The form of the data is decided at the time of manufacture to perform a variety of functions, but the one in a Teletext decoder is a character generator, arranged to contain the characters shown in Fig. 5. Bits 1-7 in the configurations shown on the left, control the selection of display at the output. Bits 1-4 determine which row of character bits should be read out, while bits 5-7 indicate the column. For example, if the seven bits from the store were 0011010, bits 7, 6 and 5 (001) indicate that one of the undisplayed control characters in column 1 should be generated and bits 4, 3, 2 and 1 show that ROW 10 — alphanumerics, green — is required. The use of this invisible control character means that the visible, succeeding character shall be a green alphanumeric one, as opposed to the graphics alternative in columns 2, 3, 6 and 7. The next group of

bits could be 1101001, in which case the result would be a green, lower-case "i" on the screen. A control character is not displayed, so that whenever the mode is changed — from alphanumerics to graphics or from picture to insert or from white to red — a space must appear.

There is one exception to this, and the space can be avoided when an alphanumeric character is needed close to graphics, with no control character space. Although the graphics characters are shown in Fig. 5, it is not meant to imply that they are contained in the ROM. Only the alphanumeric characters are held in the memory, the graphics being generated directly by the 7-bit code as received, as shown in Fig. 5. The area occupied by a character and its surrounding space can be separated into six "cells" which each have a bit of data allocated to them. All codes intended for display as graphics have a 1 as bit 6. However, if, while in the graphics mode, a code occurs with a 0 as bit 6, then those characters in columns 4 and 5 of Fig. 5 will be displayed — a limited selection of alphanumerics, termed "blast-through" alphanumerics.

Fig. 8 shows the output processor, complete with character generator and timing circuits, synchronized by line and field sync pulses. Characters are built up from dots at the 7MHz clock frequency and a dot clock is therefore required. The number of elements or dots in the width of a character is six (5 in the character and a space) and a

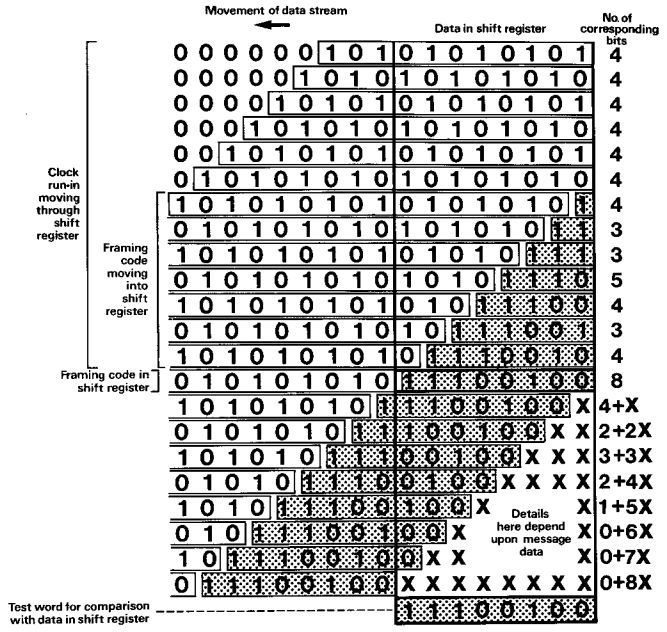


Fig. 6. The framing code in progress through the shift register, and in position on the 10th row down. At no time other than at coincidence are more than 5 bits in the register in correspondence with the reference word 11100100.

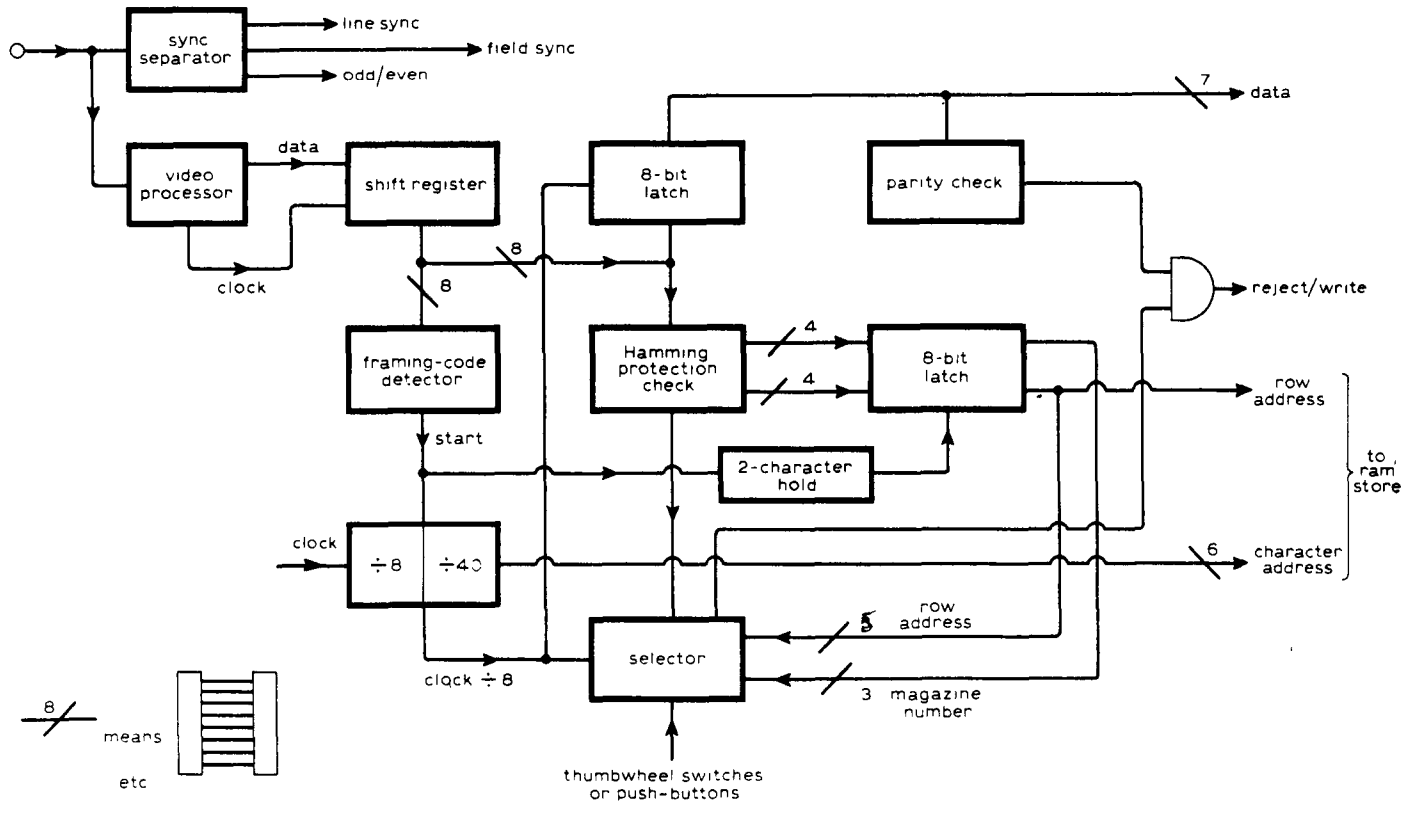
6-counter produces an output at each character. These two outputs are used to serialize the outputs of the ROM, and a 40-counter with a 6-line output is applied to the store, instructing it to provide successive character codes to the ROM which generates the pattern for each new character.

Line sync is also applied to a "divide-by-10" counter, which ensures that the store addresses the ROM for 10 lines in each character, giving 7 scanning lines for the character and 3 scanning lines space between characters. A 24-counter addresses the 24 rows of data in the store.

A further block in the display circuitry is the controls decoder which recognizes the control characters in columns 0 and 1 of Fig. 6, to produce RGB drives, blanking to provide a box for inserts and a "flashing" instruction. Graphics are produced, under command from the controls decoder, by the graphics generator on the principle previously mentioned and illustrated in Fig. 5.

Finally, the interpolator can be used to obtain a slightly improved appearance to characters which include a diagonal (Y, Z, K, etc.). The principle is to take advantage of the fact that interlacing effectively provides 14 lines

Fig. 7. The input processor block diagram.



in a character, not 7, and to "fill in" the steps produced by the 7 stored lines. An odd/even field command can be derived and used to synchronize the interpolator, which is also used to make the flashing signal effective.

That is the principle of the decoder, very briefly. In a short article, it is not possible to cover all aspects and it was not the intention. Forthcoming articles will describe the circuit in detail and provide complete information on the construction of a decoder that will differ from this general picture in several respects. Many savings in cost have been found possible by circuit changes which have also made possible a unit which is much smaller than envisaged.

(To be continued)

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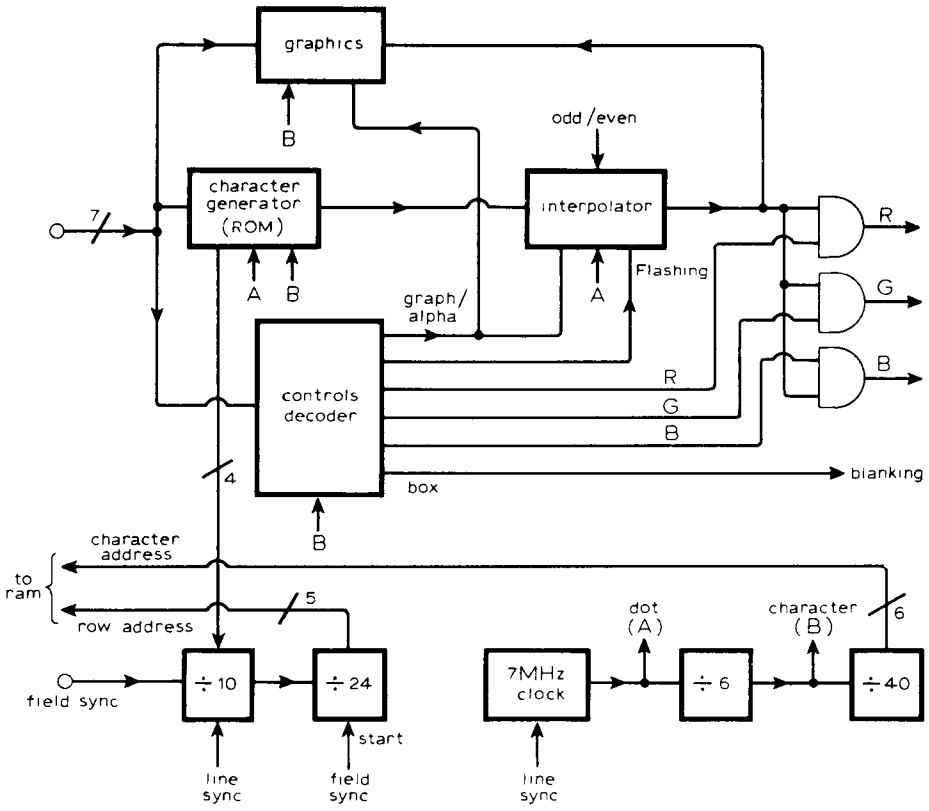


Fig. 8. A typical output processor.

Fig. 9 An example of the use of graphics.

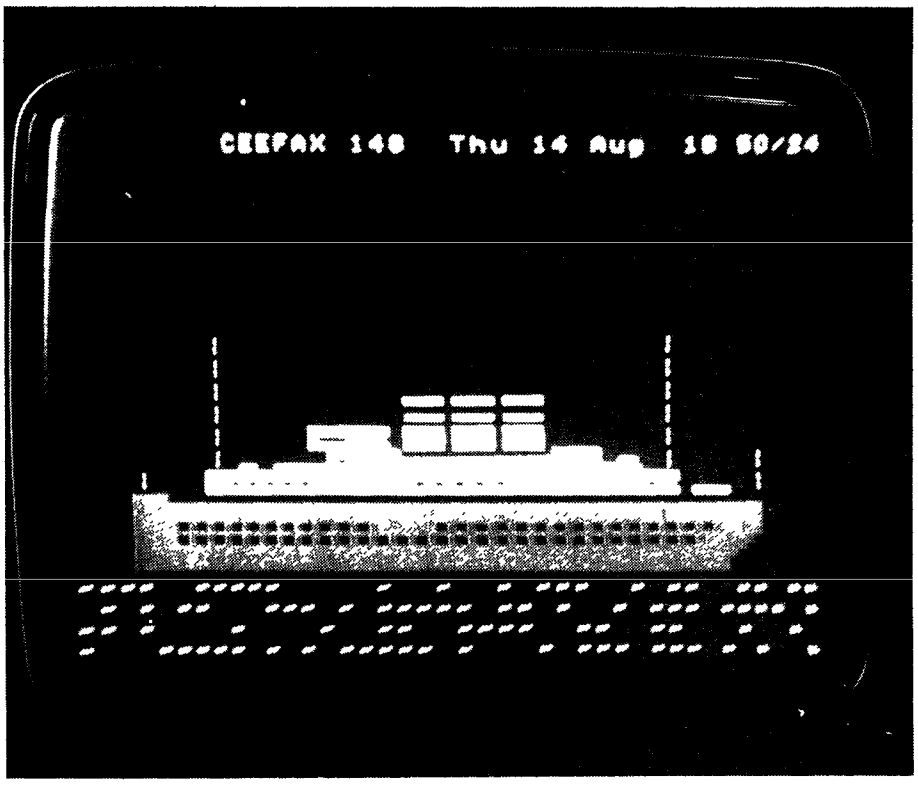
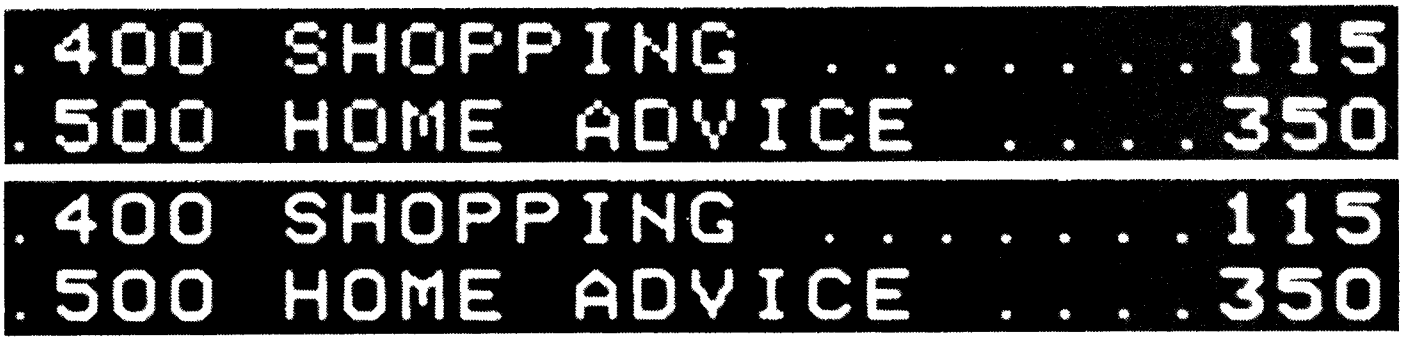


Fig. 10. Extracts from an Oracle index page, showing the normal appearance at (top) and the effect of character rounding (bottom). This is an IBA photograph taken from the screen of a studio monitor. On a domestic receiver, the effect is not as pronounced.



Wireless World Teletext decoder

2—The decoder system

by J. F. Daniels*

This article describes the facilities offered by the Wireless World decoder and also covers, in general terms, the methods of installation in a commercial colour receiver. The problems likely to be encountered with such a project are also discussed.

When contemplating the design of a project as complex as this one, there are many factors which have to be considered. For instance, to build a single Teletext decoder with cost and size virtually no object and expensive test equipment available is comparatively easy, but this is of little interest to the home constructor. What is needed is something which can be built relatively cheaply, can be mounted in a small, attractive cabinet, and can be installed and made to work with only the minimum of adjustments, preferably requiring only a cheap multimeter.

This design will fulfil these requirements. This does assume, however, that the unit is constructed without any wiring errors and with no faulty components – in a unit using around 85 i.cs and their interconnexions, there is some room for error!

Not to be too discouraging at such an early stage, however, it should be pointed out that printed circuit boards will be made available, from normal sources, which should eliminate most wiring error problems. Further, digital i.cs tend to be very reliable, in my experience anyway, as long as they are not obtained from one of the sources of unmarked, untested devices. The use of such i.cs in this project must be strongly discouraged, as even if they appear satisfactory on a d.c. test, they may well be out of tolerance on delay time or fan-out, which could have disastrous effects in some parts of the circuit, where correct delay time through i.cs is an important factor.

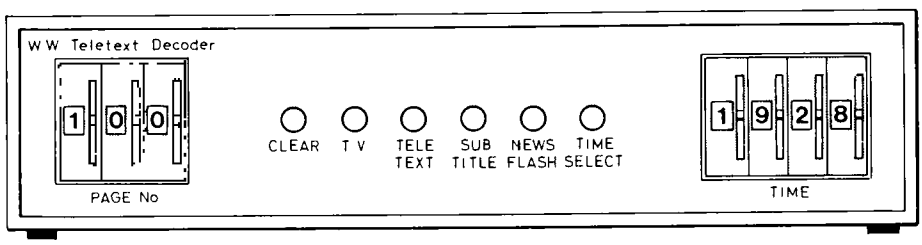
For the constructor who has access to an oscilloscope, waveform diagrams will be given at various points in the circuit to help those wishing fully to understand the circuit operation.

It is not intended, in this series of articles, to give full constructional details, and the choice of suitable box, and method of mounting p.c.bs etc. is left to the individual constructor. Details of how the unit may be connected into various types of commercial colour receiver will, however, be fully covered and this should leave only problems of a mechanical nature to the individual.

The cost of the decoder will be in the region of £85, and although this may seem a great deal of money to pay, people who have seen the resulting display of pages on the TV screen agree that the service is well worth while and has great potential for the future. The *Wireless World* decoder will be capable of utilising most of the features currently offered by the system, including display in six colours and white, alphanumeric characters, graphic characters, and flashing display. Two circuit options will be described; one which includes both upper and lower case characters, and another, slightly simpler circuit, with upper case characters only — a worthwhile option for cost conscious contructors. The circuit does not include any form of interpolation (character rounding) because it was thought that the extra cost of about £15-20 was not justified in a discrete-component decoder of this type.

Before going on to describe some problems, which can be encountered when dealing with commercial TV receivers, it is necessary to describe in more detail the performance of the Teletext decoder.

Fig. 1. Suggested front panel layout of the Wireless World *Teletext decoder.*



Operation

The decoder can be built into a box measuring about 8.5 × 10.5 × 2in, which is a convenient size to rest on top of a normal domestic TV receiver. The power supply is not included in this box for a number of reasons, some electrical, but mainly to keep down the size and heat dissipation in the decoder unit. Space can usually be found in the cabinet of most domestic TV receivers to take the decoder power supply.

The front panel of the decoder carries two sets of thumbwheel switches, and various other function switches. In the latest version, the function switches take the form of a row of pushbuttons as shown in Fig. 1. The bank of three thumbwheel switches are for magazine and page number selection, the one on the left being for magazine number; the other two for page number tens and units. The bank of four thumbwheel switches are for the selection of timed pages, which may only be transmitted for a one-minute period during each day, and therefore require selection by means of time code and storing, for viewing later. The switches can be set to any given time during a 24-hour period, and in this mode of operation a page will only be written into the store at the time shown on the thumbwheel switches. It should be pointed out here that at the time of writing, no pages are being transmitted in this manner, although the operation of the circuitry can easily be checked, because all pages carry time coding information. However, a cost saving of the order of £6 could be made by omitting this facility.

*Designer of the Teletext decoder

The row of pushbutton switches mainly controls the form of display on the TV screen. The four in the centre are all interlocked, latching pushbuttons, the one of the left is an individually-operating, momentary-action type and the right-hand one is individually latching. The "TV" button merely selects the picture on the screen in the normal manner, although the decoder will still be operative and can store pages in the usual way, ready for instant viewing when the "Teletext" button is pushed. The latter merely replaces the picture with the video output of the decoder and, in this mode, all the normal features of Teletext display are available.

The page header contains a continuously changing time indication in the top right-hand corner, but a fixed page number display — the number of the page selected. When a different page is required on the display, the momentary-action, left-hand button marked "clear" is pushed. This clears all the information from the display except for the page header row, which then starts "rotating" i.e., reading out all the page headers as they are transmitted until the new page number selected is reached, whereupon the new page is read out into the screen.

The next button is marked "subtitle" and is used to select the "insert" mode of operation. When this button is selected, the TV picture is displayed on the screen until the subtitle page, the number of which has been selected on the thumbwheel switches, is detected, when the subtitle message will be read out in a box inserted in the picture. If a new subtitle, or indeed a continuous stream of different subtitles is transmitted, the displayed subtitles will automatically change as they are transmitted. This may be a very useful facility for the future, as subtitles take up very little transmission time in the Teletext waveform, consisting of only a few rows of information. However, at the present time they are only transmitted in test form.

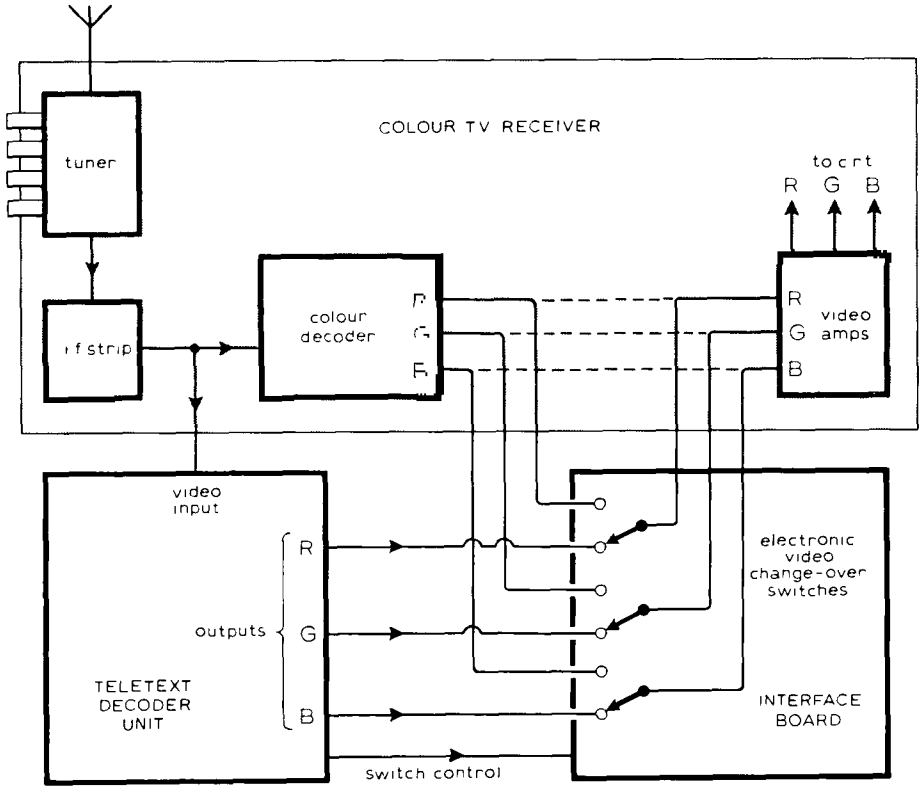
The operation of the "newsflash" button is somewhat similar to the subtitle button, but with an added facility. After selecting the newsflash page number on the thumbwheel switches, the current newsflash — which may have first been transmitted some time ago — is displayed in a box in the TV picture in the normal manner. If, however, the clear button is then pushed, the picture returns to normal, and no data are then displayed until a new newsflash is transmitted, whereupon this is displayed in the usual way in its box. If the current newsflash is required to be seen again, after pushing the clear button, the newsflash button is simply released and reselected.

The next button, marked "time" brings the time-select thumbwheel switches into operation, when the selected page will only be written into the decoder store during the one-minute period displayed on the thumbwheel switches. This page will then be held in the store until either the clear button is depressed or a different mode of operation is selected. This button is not interlocked with the other buttons so that time-selected pages can be written into the store while watching a TV programme — possibly for later reading during the commercials! The time selection facility is not operative when subtitle or newsflash buttons are selected.

No facility is provided for superimposing the complete Teletext display on the picture, as in the author's opinion this gives a meaningless display which makes both the picture and the Teletext display difficult to interpret.

These, then, are the basic facilities offered by the *Wireless World* decoder. Without doubt, as the Teletext system progresses, more facilities will be offered by the service, and it should not be difficult to add extra facilities to the decoder as required.

Fig. 2. Suggested method of connexion into a domestic colour receiver, using an interface board containing three simple electronic video switches.



Installation

There is really only one satisfactory way to connect the decoder to a domestic colour receiver if all the facilities described earlier are required, and this is shown in Fig. 2. It can be seen from the diagram that there are only four points of connexion into the set: a feed of composite video from the output of the receiver i.f. strip, and feeds of red, green and blue (or possible R-Y, G-Y and B-Y) to and from the inputs to the receiver video amplifiers. It is possible that a fifth connexion, from the set's flywheel oscillator, will be required if the set is in use in a low signal area and displays a noisy picture, as this can be used to remove horizontal jitter on the Teletext display caused by the noise on the video signal. However, this possibility will be considered later during the circuit description.

The interface board is a small video switch unit, mounted inside the receiver, fairly close to the video amplifiers, and serves to switch electronically between the picture and the Teletext display, when commanded by either the function switches, or by "hole-cutting information from the decoder. The design of this unit will vary slightly, depending on the type of receiver used, some sets having, R, G and B feeds to the video amplifiers and others using colour difference signals (R-Y, G-Y and B-Y). If the facility of putting newsflashes and subtitles in boxes is not required, then this unit could probably be replaced by a three pole change-over relay, controlled solely by the function switches.

This, then, is the only practical way in which a decoder can be installed into an existing TV set, if a coloured display is required and this is the only method that will be described in detail in this series of articles. However, for those who rent a colour set, there is another, somewhat less attractive possibility, shown in Fig. 3. Here, a separate tuner and i.f. strip are used to provide video for the Teletext decoder. The R, G and B outputs of the decoder are then matrixed together, and fed to a u.h.f.

modulator. This in turn feeds the aerial socket of the receiver, which is tuned in to the modulator on an unused channel. This will, of course, only give a monochrome display, but would at least have different shades of grey to represent different transmitted colours.

It is not practical to modulate the decoder display into PAL colour form, partly because of the high cost of a colour coder, but mainly because the results woule be unsatisfactory due to the fact that the bandwidth of the PAL system would be insufficient to cope with the Teletext display waveform.

Data signal

Before starting a description of the decoder block diagram, there are two more important points to be made to prospective constructors. Firstly, there is the question of obtaining a suitably undistorted data signal from the TV receiver.

Distortion of the data waveform can be caused in a number of ways; poor bandwidth or non-linear phase response in the receiver i.f. strip; reflections (ghosting) on the picture, caused either by external multipath interference or aerial mismatching; co-channel interference; and finally noise. All these can cause errors to be made in the data display and, in extreme cases, prevent operation of the decoder at all.

Generally speaking, however, satisfactory results can be expected from the majority of colour sets displaying a ghost-free picture. Noise on the picture, unless of sufficient amplitude to be objectionable, is unlikely to be a problem, as the decoder employs circuits capable of detection and correction of errors caused by noise spikes.

Secondly, the performance of the decoder in the presence of interference in various forms is determined almost solely by the performance of the front end, i.e., the circuitry which separates the data from the video waveform, and converts it into t.t.l.-compatible form. It is proposed to describe first a fairly simple data separator, which is extremely easy to set up and which will be adequate under good reception conditions. This will enable the rest of the digital circuitry to be tested and set up. In a later article a more complex form of data separator will be described which will give an improved performance under adverse signal conditions although it will be rather more difficult to set up initially.

Safety

The most important problem of all is one of safety. If the decoder is to be installed in the manner to be described rather than by using a u.h.f. modulator, as mentioned earlier, then a direct connexion must be made to the receiver chassis, which could under some circumstances be live.

There is only one way to prevent the decoder itself from becoming live, and that is to use a mains isolating transformer in the mains supply to the TV receiver, and I would strongly recommend this course of action for anyone who does not regularly work with live equipment. If, however. the constructor feels absolutely confident that he can carry out the installation without electrocuting himself, then there are two important points to note. The first is to ensure that the receiver chassis is connected to the neutral side of the mains and not the live — this should be a simple matter of connecting the plug the correct way round but it must be checked with a multimeter. The second is to make sure that the decoder cabinet (if made of metal) or any metallic parts on it such as switches, etc. are not connected to the decoder electrical earth.

A three core mains lead must be used, with the earth connexion taken to the decoder cabinet, if this is made of metal. Probably the best solution, though, is to use a wooden cabinet and ensure that the thumbwheel switches and pushbutton switches are suitably insulated from their electrical contacts. The earth connexion should only be made after the decoder has been tested and set up, as it could create a hazard while actually working on the decoder. Of course, after testing is finished, when the earth is connected, protection is ensured against the decoder box becoming live due to faulty insulation.

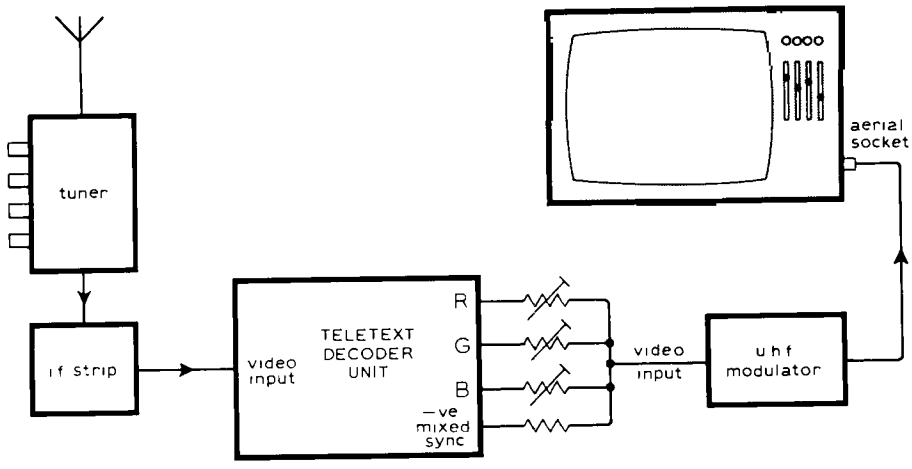


Fig. 3. Alternative arrangements for rented television sets. This has the disadvantage that only a black and white display will be obtained.

Construction

Prototype decoders were constructed on 12 × 7in pieces of ordinary Veroboard 0.1in matrix sheets. There is no reason why this method of construction should not be used, apart from the fact that it is very laborious, and wiring errors can easily be made.

For those who have less time to spare, printed circuits will be available in the form of two large p.c.bs for the digital circuitry, and a smaller p.c.b. for the analogue circuits. The overall size of the unit has been kept down by splitting up the boards in this way.

The large boards measure 9½ × 5½in,, and are arranged to mount one above the other, spaced about ½in apart. The analogue board measures 5½ × 3in and is spaced ½in above the digital boards. This gives an overall size for the decoder electronics of about 9½ × 5½ × 1½in. The digital boards, which each hold about 40 i.c.s, are double sided, but for cheapness do not have plated-through holes. The "plating through" process is carried out by the constructor, using tinned copper wire soldered on both sides of the board.

This simplified block diagram in Fig. 4 shows the main functions contained in the decoder, only the main data paths being shown for simplicity. The heart of the circuit is contained in the clock and line divider blocks, and there are many waveforms from these sources which are distributed to the rest of the circuit blocks. This initial description is only intended as a guide to circuit operation, so that an overall picture can be obtained, before starting a detailed description of each circuit block.

The function of the analogue board is to take the composite wide-band video signal from the receiver i.f. strip, and produce from it t.t.l.-compatible mixed syncs, data, and clock waveforms. The single clock line includes the outputs of two clock generators, one derived from the incoming data, and another free-running oscillator used during the display time. Switching between the oscillators is achieved by using a waveform from the line divider circuits, which switches from the display oscillator to the "data locked" oscillator during part of the field blanking interval (between lines 10 and 20). The free-running oscillator has a preset frequency adjustment which controls the width of the Teletext display, and is also triggered by a line blanking wavefrom to ensure that it starts up in the same phase at the start of each television line.

Clock and data waveforms from the analogue board are fed to the serial-to-parallel converter, which in turn feeds the data latches and the framing-code detector. The output of the framing code detector is used to reset the clock

dividers, and a ÷8 clock waveform is in turn used to operate the data latches.

It should be explained at this point that the clock and line dividers perform the dual role of data aquisition and data display dividers, and this constitutes quite a saving in circuit components.

Bits 1-7 from the data latches are fed straight to the inputs of the data store, while all eight bits are fed to the parity checker and Hamming-code corrector. The output of the Hamming corrector consists of bits 2, 4, 6 and 8, suitably corrected in the case of a single error, and also an output which indicates an even number of errors. If an even error is detected during a row address group, then the even error output of the Hamming corrector is used to inhibit any data from being written into the store on this row.

Bits 2, 4, 6 and 8 from the Hamming corrector are fed to the row and page recognition circuitry, and also to the line divider circuits. The line divider circuits count line syncs during the display period, but when data lines are detected during field blanking, the counters are preset to the correct row number, indicated by the Hamming-corrected bits. The five-bit row-address output of the line dividers is fed, together with the six-bit column-address output of the clock dividers, to the code convertor circuit. ("Column address" refers to the 40 vertical character columns and "row address" to the 24 horizontal character rows.)

The divider circuits are both arranged so that the data on these eleven wires is correct during both data aquisition and data display, and this obviates the necessity of complicated switching in the address inputs to the store. The code convertor is required for the following reason: the 1024-bit random-access memories are arranged in a 32 × 32 matrix which can, of course, be addressed in any of its store positions by a 10-bit address input. Our display matrix, though, is arranged in a 40 × 24 pattern as previously described, and this requires an 11-bit (6 + 5) code to address each individual position. However, there are many unused positions which can be addressed by the 11-bit code and by a suitable rearrangement of the addresses, the 11-bit code can be reduced to 10 bits, without actually losing any of the 40 × 24 matrix positions. A simple calculation showing that 40 multiplied by 24 comes to less than 1024 indicates this possibility.

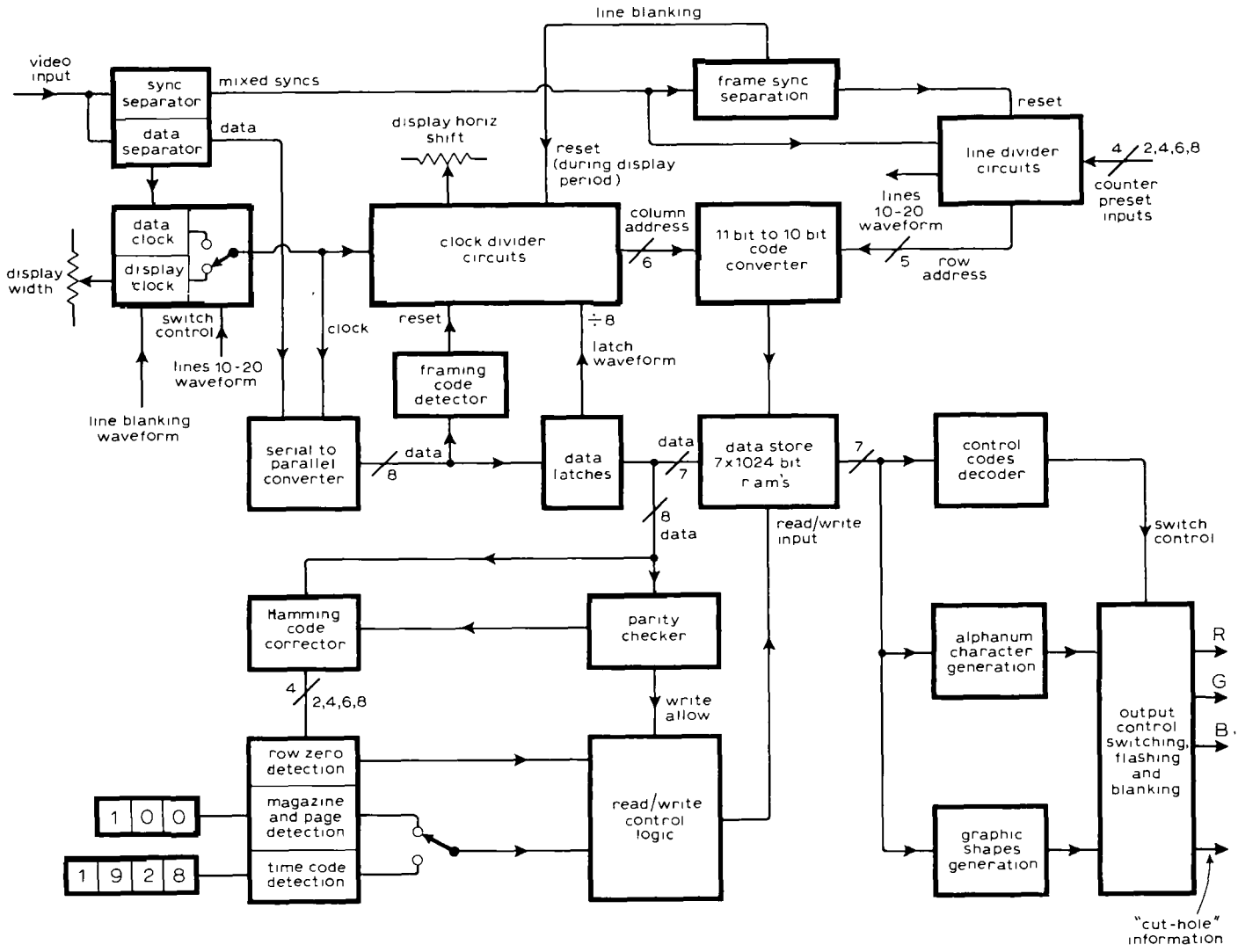
Fig. 4. Teletext decoder simplified block schematic.

The data store consists of seven 1024-bit random-access memories, addressed in parallel – one for each of the seven bits of data. The other input to the store is the read/write input. This input is normally in the read condition, when data already in the store is read out onto the screen, but changes to the write condition during Teletext data lines 17 and 18, when instructed to do so by the read/write control logic.

The seven-bit output of the data store is fed in parallel to three circuit blocks, as shown. Alphanumeric characters and graphic characters are generated for each of the 960 display positions on the screen. The control codes decoder decides which will actually be displayed, what colour it should be, and whether or not it ought to be flashing or boxed. It does this by suitable switching in the output control unit, which also blanks control characters.

This, then, is a necessarily brief introduction to the *Wireless World* Teletext decoder. In the following articles, detailed descriptions of each of the circuit blocks will be given, with waveform diagrams and explanations where these are relevant. Finally, circuits will be given for various types of "interface" board.

(To be continued)



Wireless World Teletext decoder

3 — Line and clock dividers

by J. F. Daniels

Last month we looked briefly at the overall operation of the decoder by considering a simplified block schematic diagram. I also mentioned that the heart of the circuit lay in the design and operation of the clock and line divider circuits. This month we shall look in greater detail at the operation of these two circuit blocks, as these together provide most of the waveforms used elsewhere in the decoder circuitry. We shall begin by looking at the operation of the line dividers.

The main function of this part of the circuit is to provide row-address information for the store during the operation of writing data into the store and when reading it; i.e., when the data is displayed as characters on the screen. Other outputs are also obtained from this part of the circuit, namely separated field syncs, line address information for the character generater read-only memory, the vertical component of the display blanking waveform and a field blanking waveform which goes to "1" during the period from lines 11 to 21 and 324 to 334. This latter waveform is used extensively elsewhere in the decoder to discriminate between data acquisition and data display: i.e., data is only "looked for" during the periods just mentioned. If all 625 lines were examined for data, false framing codes would be detected at random during the video information, and cause lines of "rubbish" to be read into the store. It would of course be possible to look for data only on lines 17-18 and 330-331, but it is possible that broadcasters may change the positions, or increase the number, of data lines transmitted, and so the above method was adopted to avoid later modification in this respect.

It may appear, from a quick glance at the circuits, that the i.cs are numbered somewhat erratically, but this is

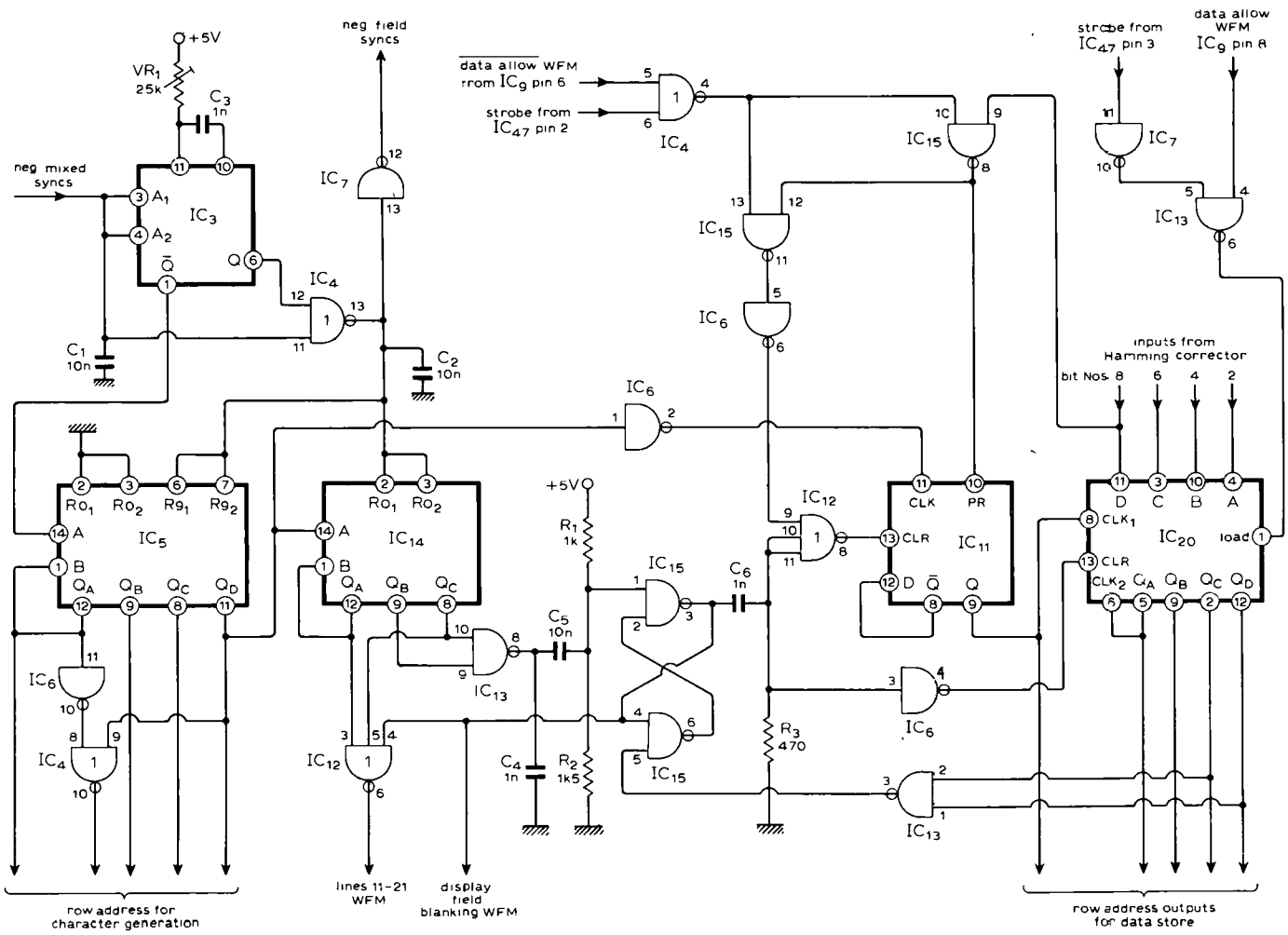


Fig. 1. The line divider circuitry. IC_3 is a 74121 monostable, IC_5 and IC_{14} are 7490 decimal counters, IC_{11} is a 7474 dual D-type edge-triggered flip-flop and IC_{20} is a 74177 / 74197 binary counter.

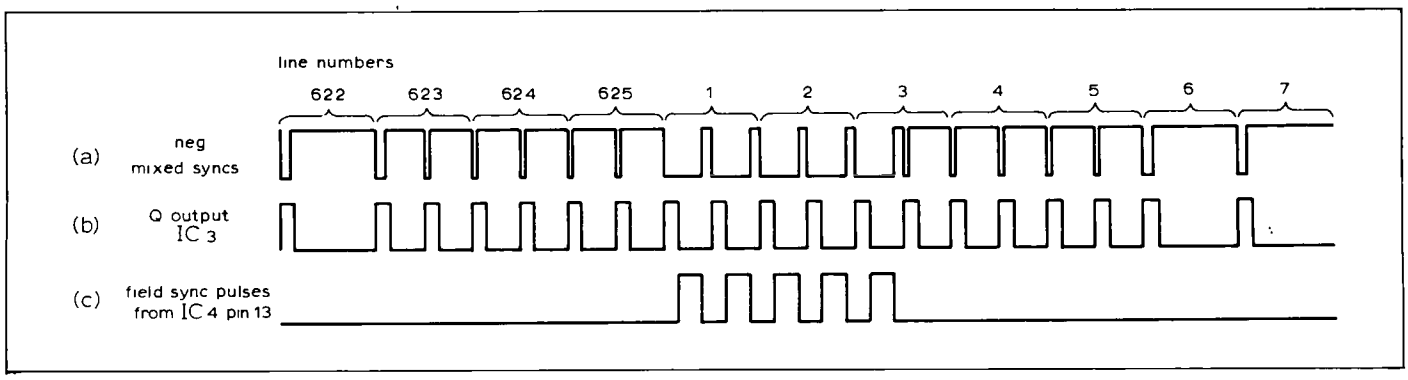


Fig. 2. Waveforms from Fig. 1, showing the detection of broad pulses.

because they are designated according to their position on the p.c. boards – $IC_{1\text{-}40}$ being on the uppermost board and $IC_{41\text{-}80}$ on the lower circuit. During circuit descriptions, multigate i.cs will be referred to by their IC number, and output pin number. For example (7, 12.) indicates the inverter gate for field sync pulses in Fig. 1.

Line dividers

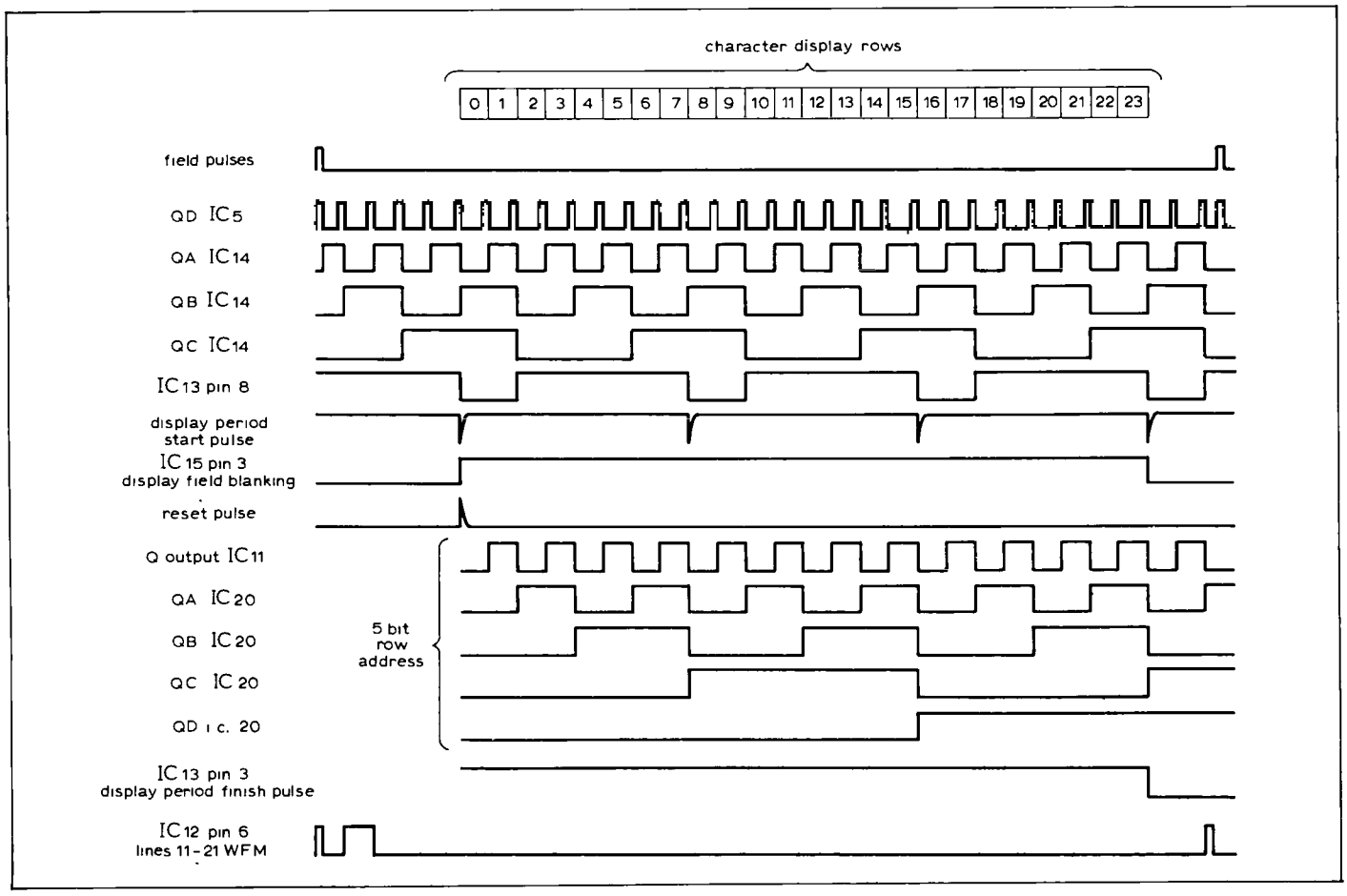
Negative-going mixed syncs from the analogue board trigger monostable 3, which is adjustable by means of a preset potentiometer. Elswhere in the circuit the variable width of the output pulse is used to shift the display horizontally, but for this part of the circuit the output pulse width is not critical, so long as the pulse is wider than the input sync pulse. By gating together the input and output waveforms of this i.c. in a NOR gate (4,13), the broad pulses during the field blanking interval are separated from the mixed sync waveform. Capacitor C_2 removes spikes which are caused by the delay through IC_3. The method by which the broad-pulse separation is achieved is more clearly shown by Fig. 2. waveforms (a), (b) and (c).

The broad pulses are used to reset the first part of the line-divider chain, which consists of two i.cs forming a divide-by-80 circuit. The first i.c., a divide-by-10 counter, provides line-address information for the character generater r.o.m. and sets the height of each "character box" at 10 lines per field.

In the "upper case only" version of the decoder, only seven of these lines are used for the display of alphanumeric characters, and gates (6,10) and (4,10) serve to inhibit character generation during three of the ten lines. These gates are not required when the upper and lower case version is built, as the blanking of unused character lines is achieved in a later part of the decoder.

The operation of the rest of the circuit is best understood by referring to Fig.3, which shows some of the more important waveforms through the circuit. The divide-by-8 counter IC_{14} is fed with one pulse every 10 lines from IC_5 and its outputs Q_B and Q_C are gated in (13, 8) to provide a start pulse for the display period at line 51 (also 364). C_4 removes any spikes caused by timing differences between the Q_B and Q_C outputs of the counter, and C_5, R_1 and R_2 shorten the pulse into a narrow negative spike to set the vertical display-blanking flip-flop, formed from gates (15, 3) and (15, 6). The positive transition at the output of gate (15, 3) is coupled via C_6 and R_3 into gates (12, 8) and (6, 4), which has the

Fig. 3. Waveforms in the circuit of Fig. 1.



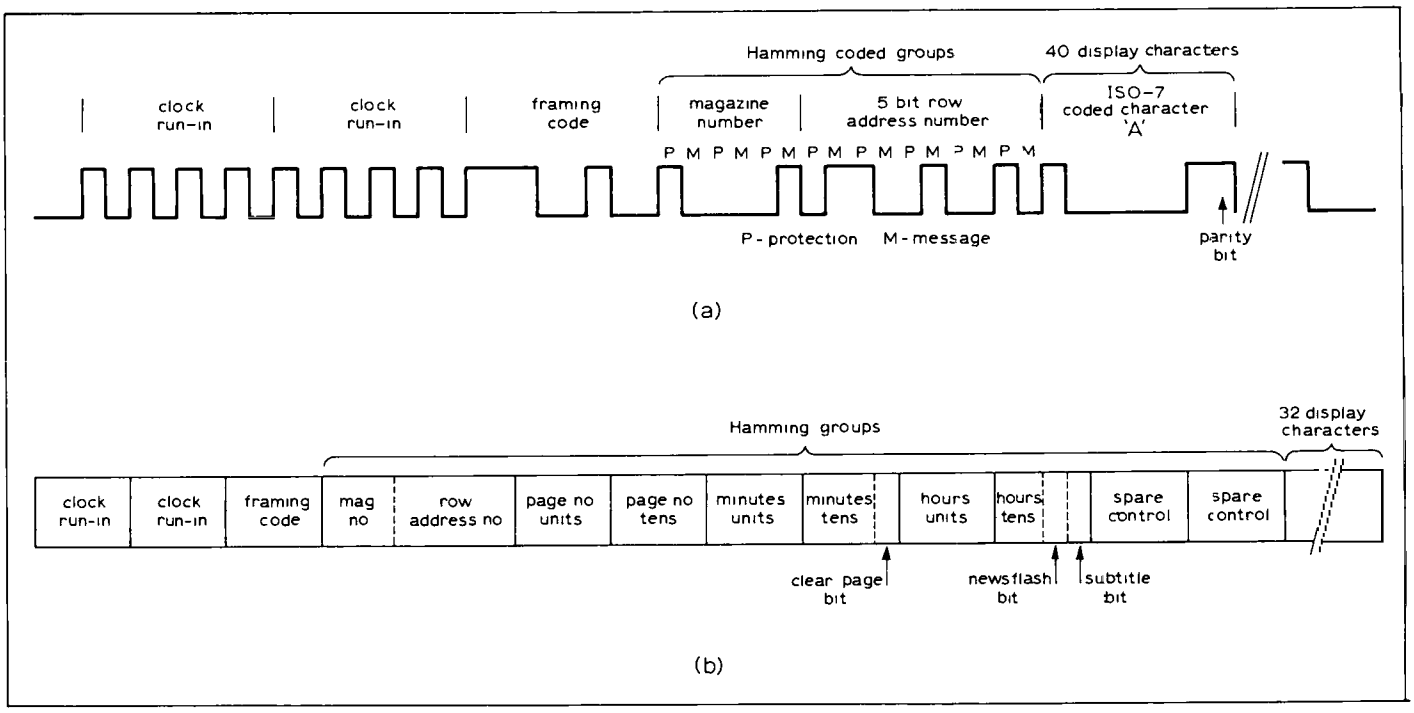


Fig. 4. Layouts of typical rows of data bits. A display row (row 5 of magazine 1) is shown at (a) and at (b) is a page-header row.

effect of setting the outputs of the 5-bit counter, formed from ICs 11 and 20, to zero. From this point onwards, the 5-bit counter counts through the character-display rows until the counter reaches 24 (the end of the page display). This point is detected by gate (13, 3) and its output is used to reset the vertical display-blanking flip-flop.

During lines containing data the 5-bit counter is preset to the correct row number, which is available in binary form at the output of the Hamming corrector during the control and row address groups, at the start of each data line.

The time at which this data is entered into the presettable counter is controlled by gates (4, 4) and (13, 6). The least significant bit of the row address arrives first, and a strobe pulse from the clock divider circuits (to be described later in this article) set IC_{11} at the appropriate time. The next data group to arrive contains the remaining four bits of row address information and this is written into IC_{20}, again at a time determined by a strobe pulse from the clock divider circuits. The other inputs to gates (4, 4) and (13, 6) are waveforms which only allow the strobe pulses to set the counters during lines which have been confirmed as containing valid information. These waveforms are used in a number of places in the decoder and we shall call them data allow (DA), for a waveform going to "1" when a framing code is detected and returning to "0" at the end of that line and $\overline{DA}$ for its inverse.

A 3-input NOR gate (12, 6), provides the field blanking waveforms which goes to "1" during lines 11 – 21 (324 – 334), by gating together the Q_A and Q_C outputs of IC_{14} together with the vertical display-blanking waveform. It can be seen from the waveform diagram in Fig.3. that this waveform also goes to "1" during the equalizing and broad pulses. This is of little consequence, however, as no video is present on these lines so that no false framing codes could be detected here.

Before continuing with a description of the clock divider circuits, it would be as well to consider in greater detail how each of the data rows is made up.

Data row format

Display row. The data bits are transmitted in groups of eight, and each line of data contains 45 of these groups, or bytes. The first five groups have the same function on all rows and a typical row is shown in Fig. 4(a). The following 40 groups consist of 1S0-7 coded characters, the eighth bit in each group being used as an odd parity bit. The magazine number and row address information are coded in a different manner from the display data, being more heavily protected in a form of Hamming coded. Only four useful bits of data can be extracted from each of these eight-bit groups, but a single error in the group can be corrected and an even number of errors i.e., 2, 4 or 6 bits in error, can be detected.

Page header row. The page-header row (row zero) contains eight more of these Hamming protected groups following the row address number, and only 32 groups of 1S0-7 coded data for display, as shown in Fig. 4(b). The two groups immediately following the row address number contain the page number units and tens respectively and these together with the three bits allocated to the magazine number, enable any combination of page numbers between 100 and 899 to be selected.

The next four groups contain information indicating the time of day. The first group contains four bits of "minutes units" information and the second, three bits for the minutes tens. The spare bit in this second group is used as a "clear page" control, which goes to "1" whenever the following page contains new information and the old page must be erased from the store. The next group contains a 4-bit "hours units" message and the fourth group contains a 2-bit "hours tens" indication. There are two unused bits in this group, the first being used to indicate a newsflash page, and the second a subtitle page.

Clock dividers

There are two more groups of Hamming-protected data before the page header display starts, and these will eventually contain more control information.

The clock-divider circuit block provides a large number of pulses and waveforms for use elsewhere in the decoder, as follows: a display line-blanking waveform which goes to "1" during the 40-character-wide display period; the "data allow" waveform which goes "1" on detection of a framing code and returns to zero 42 bytes later; 6-bit column-address for addressing the store, which is used when writing data into the store, and when reading from display; strobe pulses which discriminate between the Hamming-coded words in normal rows and in the page header row and finally, groups of pulses used elsewhere for the formation of the vertical elements of the alphanumeric characters.

Figure 5 shows the clock-divider circuit diagram, and Fig. 6 the associated waveform diagrams.

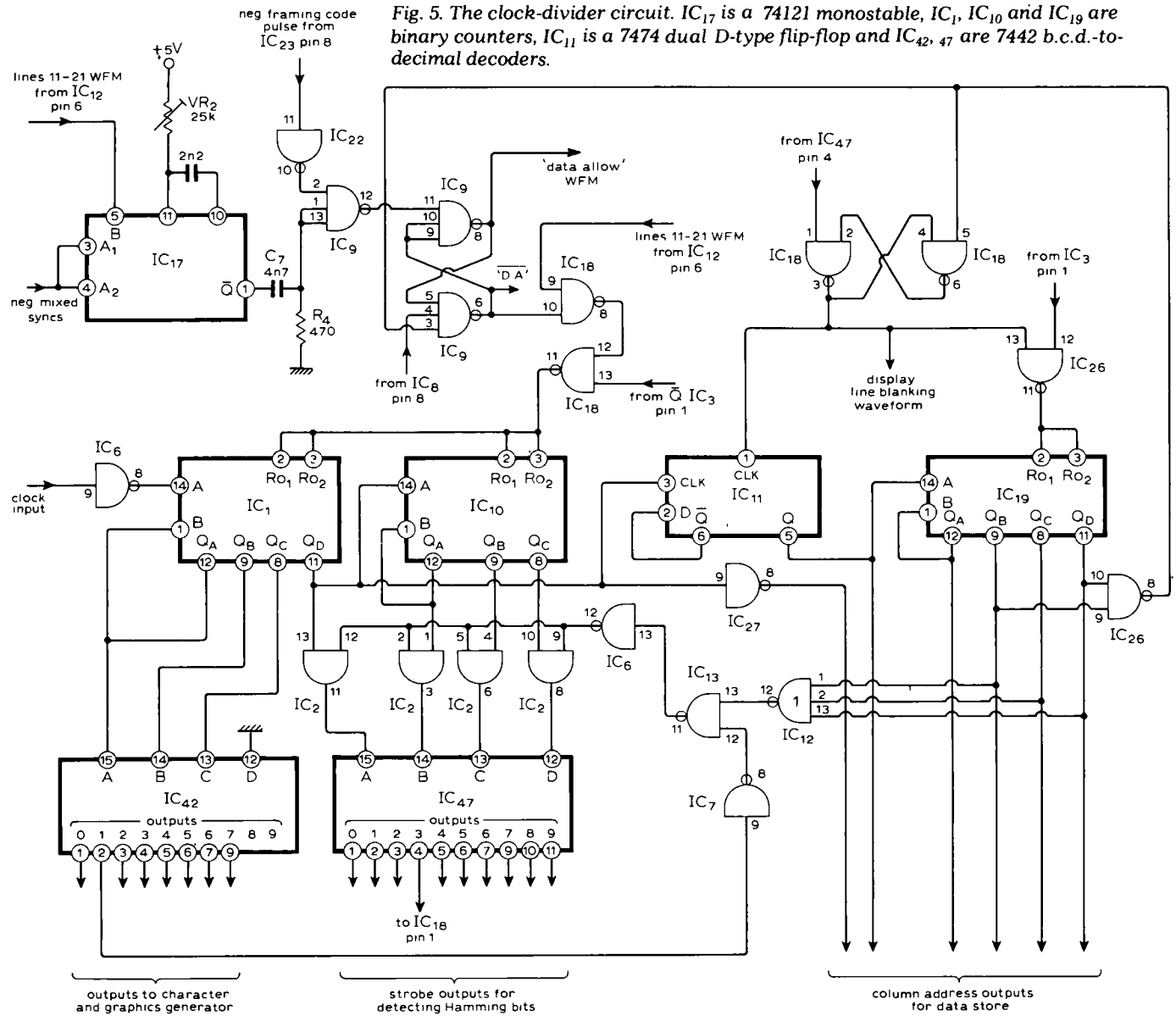
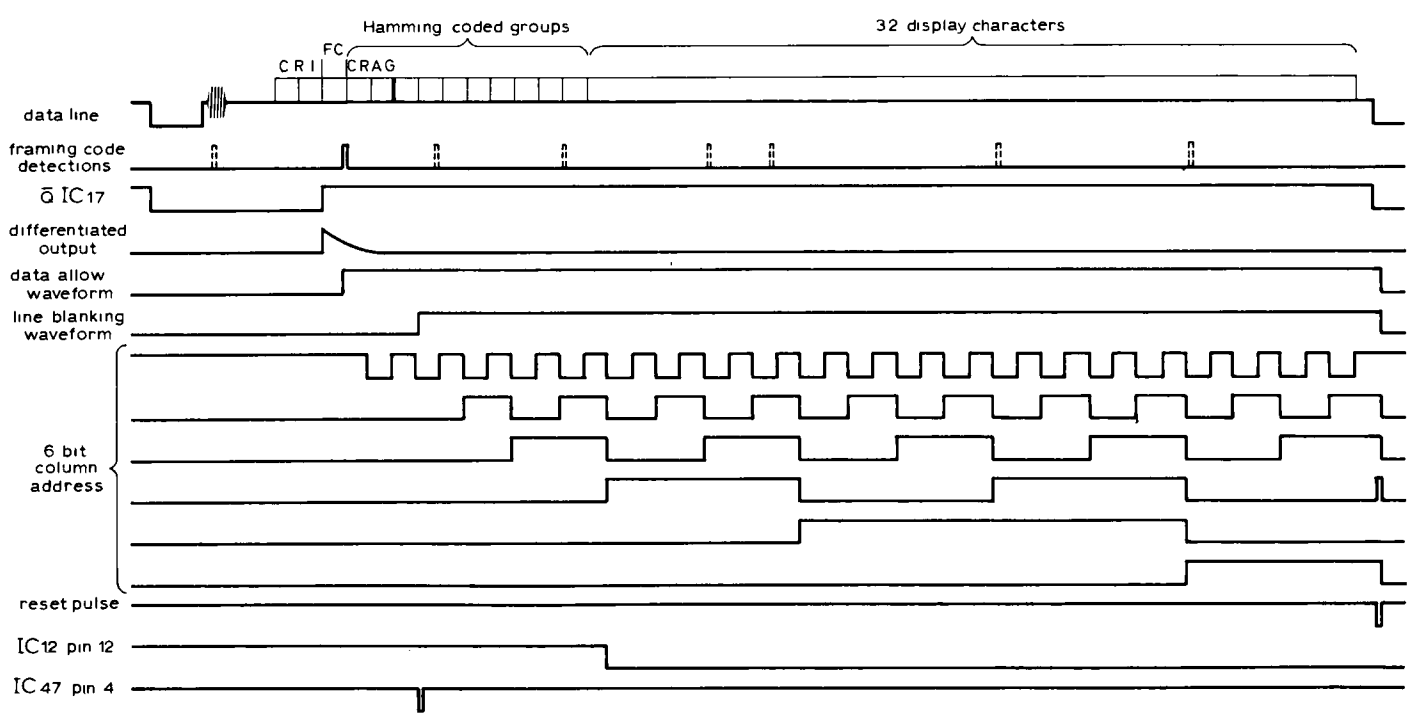
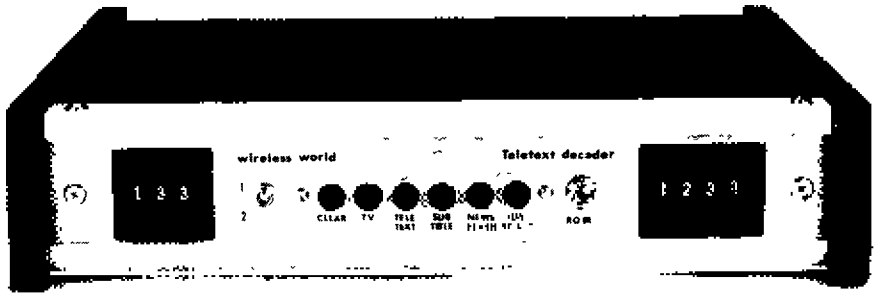


Fig. 5. The clock-divider circuit. IC_{17} is a 74121 monostable, IC_1, IC_{10} and IC_{19} are binary counters, IC_{11} is a 7474 dual D-type flip-flop and $IC_{42, 47}$ are 7442 b.c.d.-to-decimal decoders.

Fig. 6. Waveforms seen in the circuit of Fig. 5 during data lines.



Write mode. Detected framing code pulses, which are one clock pulse wide (144ns) and negative-going, are inverted in gate (22,10) and fed into gate (9,12) together with the differentiated output of monostable 17. This is the "framing-code allow" monostable and its differentiated output is about 2μs wide and timed to occur at the time of the frame code, ie, about 15μs after the start of line syncs. In this way, only valid framing codes are allowed through gate (9,12). This method was used to avoid allowing through random framing codes detected in the colour burst, which can occur with certain types of data-slicing circuit. The monostable triggering is inhibited by means of the B input on all except lines 11-21. The valid framing codes are then used to trigger the "data allow" flip-flop made up from gates (9,8) and (9,6). During lines 11-21, the first two clock-divider i.cs are held in the reset condition until the DA-waveform, goes to "1" (18,8 and 18,11) i.e., until the frame code occurs. It should be noted that i.cs of the 74H series are specified for gates 22 and 9. Although all the prototype decoders worked satisfactorily with ordinary gates here, it would be possible under worst-case conditions for the time delay between detecting the framing code and removing the reset from the dividers to exceed the maximum permissible time of 144ns. By using 74H series gates, the time delay will always be less than 144ns, even under worst-case conditions of supply voltage and gate delay.



The final prototype decoder, which measures about 40 × 22.5 × 6cm. The ROLL switch enables pages to be viewed in rapid succession. We understand that a complete kit of parts for the decoder will be available from Catronics Ltd, 39 Pound Street, Carshalton, Surrey.

A second binary-to-decimal decoder IC_{47} is connected to the outputs of the second clock-divider i.c. after they have passed through the four AND gates of IC_2. These gates serve to allow the outputs of IC_{47} only during the "allow" waveform at the output of gate (6,12). This waveform consists of narrow, positive-going pulses derived from decoder 42, gated with a waveform which only allows the pulses for the first 13 bytes of data. The output pulses of decoder 47 then become narrow, negative-going pulses, timed to occur one during each byte of data from byte 3 to byte 12: i.e., decoder 47 output 1 occurs during byte 4 – output 9 during byte 12. These pulses are used to time each group of Hamming coded bits in the row and page recognition circuitry, and for presetting the line divider i.cs as mentioned earlier.

Read mode. Resetting of the clock dividers in during the "read" mode is

The newest character code, which is now in use Reference 1 indicates that these undefined control characters will be allocated in order of decreasing serial number. Codes referenced 2 are to assist compatibility with standard data codes All character rows start in the "steady, alphanumeric white" condition, unboxed and unconcealed unless control characters indicate the contrary.

Bits				b7 b6 b5	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4	b3	b2	b1	Column → / Row ↓	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL (2)	DLE (2)		0	@ @	P P	—	p
0	0	0	1	1	Alpha Red	Graphics Red	!	1	A A	Q Q	a	q
0	0	1	0	2	Alpha Green	Graphics Green	"	2	B B	R R	b	r
0	0	1	1	3	Alpha Yellow	Graphics Yellow	£	3	C C	S S	c	s
0	1	0	0	4	Alpha Blue	Graphics Blue	$	4	D D	T T	d	t
0	1	0	1	5	Alpha Magenta	Graphics Magenta	%	5	E E	U U	e	u
0	1	1	0	6	Alpha Cyan	Graphics Cyan	&	6	F F	V V	f	v
0	1	1	1	7	Alpha White	Graphics White	'	7	G G	W W	g	w
1	0	0	0	8	Flash	Concealed Display	(	8	H H	X X	h	x
1	0	0	1	9	Steady	(1)	)	9	I I	Y Y	i	y
1	0	1	0	10	End Box	(1)	*	:	J J	Z Z	j	z
1	0	1	1	11	Start Box	ESC (2)	+	;	K K	← ←	k	¼
1	1	0	0	12	(1)	(1)	,	<	L L	½ ½	l	‖
1	1	0	1	13	(1)	(1)	-	=	M M	→ →	m	¾
1	1	1	0	14	SO (2)	(1)	.	>	N N	↑ ↑	n	÷
1	1	1	1	15	SI (2)	(1)	/	?	O O	# #	o	

Wireless World Teletext decoder

4 — Framing code detector, error circuits and storage

by J. F. Daniels

Discussion of the serial-to-parallel convertor, framing code detector, data latches, Hamming corrector, data store and code converter completes the description of the circuitry contained on digital board one.

Fig. 1 shows the serial-to-parallel converter, data latches and framing-code detector. IC_{21} is an 8-bit, serial-in, parallel-out shift register, which presents all eight bits of data in one "byte" to the inputs of the data latches at the same time. A strobe pulse is applied to the data latches, which causes the eight bits of data to be stored in the latches until the next strobe pulse arrives, eight clock periods later. A 7428 buffer i.c. is used for driving the strobe inputs of the latches, as the fan-in requirement of 16 could not be met by the more common 7402, two-input NOR gate. The timing of the strobe pulse is quite critical and it must, of course, occur only when the eight bits of data in each byte are correctly positioned in the 74164 shift register. The detection of the framing-code pulse initially sets the timing of the latch strobe pulses, and subsequently they are derived from a ÷8 output of the clock divider circuit (IC_{42}, pin 1).

Framing code detection

The framing-code detection circuit consists of only four inverter gates and a single 8-input NAND gate (23, 8). The output of this gate goes to "0" only when the eight outputs of the shift register are in a condition that causes all "1"s to be present at the gate input. It is possible, with the use of more complex circuitry, to detect the framing code in the presence of a single error, as was explained in the introductory article. However, this added complication will also increase the number of false framing code detections, and this can in some circumstances be more troublesome than the occasional missed framing code. This simple detector was found to be perfectly adequate.

Error detection and correction

Before continuing with a description of the parity and Hamming-code correc-

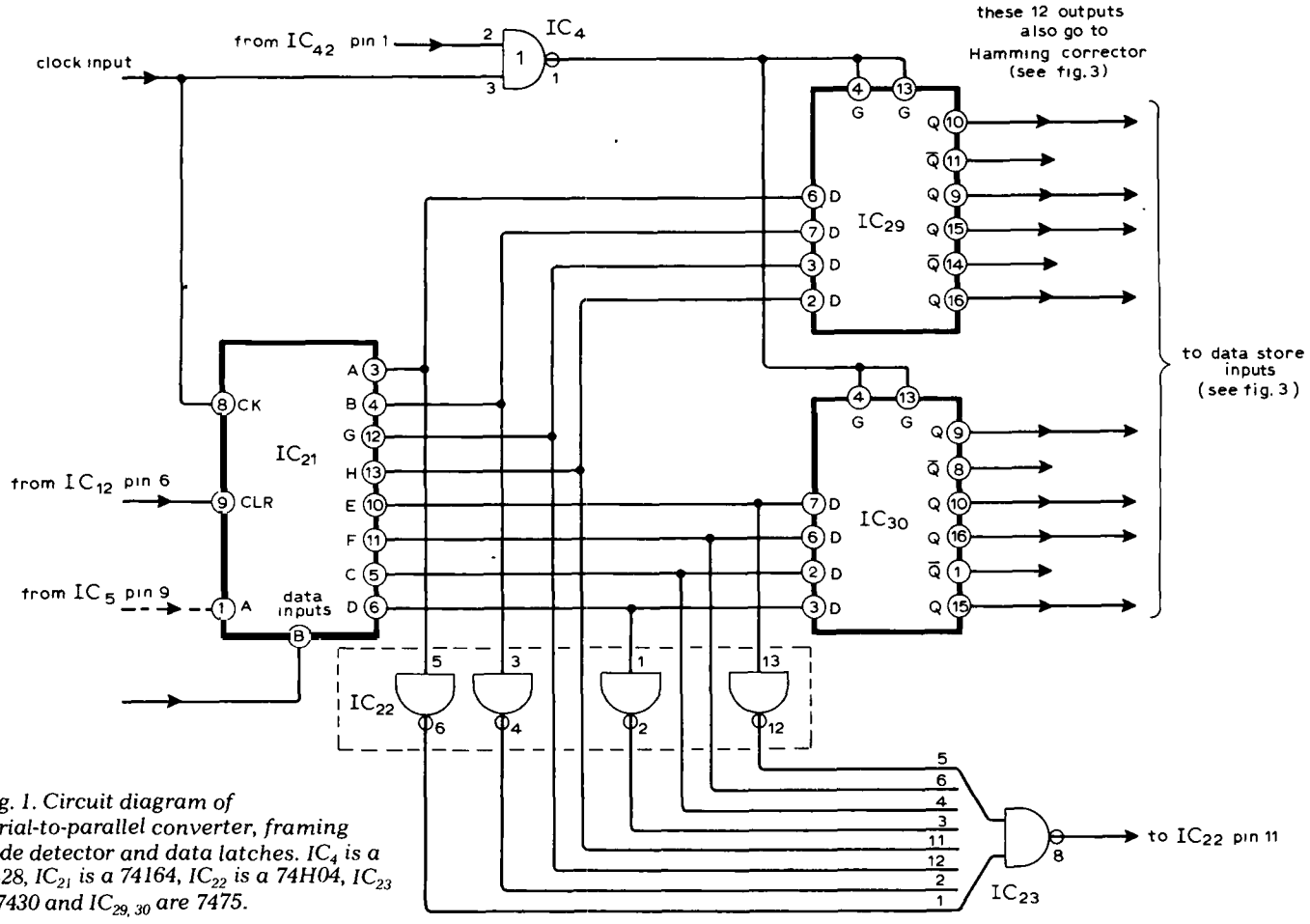


Fig. 1. Circuit diagram of serial-to-parallel converter, framing code detector and data latches. IC_4 is a 7428, IC_{21} is a 74164, IC_{22} is a 74H04, IC_{23} a 7430 and $IC_{29, 30}$ are 7475.

D	C	B	A	
0	0	0	0	error free reception
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	reject even order error
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	invert bit 7
1	0	0	1	" " 1
1	0	1	0	" " 3
1	0	1	1	" " 8
1	1	0	0	" " 5
1	1	0	1	" " 6
1	1	1	0	" " 4
1	1	1	1	" " 2

A,B,C & D are parity checks over the following bit no's

A checks on bits 1 2 6 8
B " " " 2 3 4 8
C " " " 2 4 5 6
D " " " 1 2 3 4 5 6 7 8

0 = parity check correct
1 = " " incorrect

Fig. 2. Table showing the results of four possible parity checks carried out over the Hamming coded groups, and the action required for each combination of results.

tion circuits, it would be as well to explain in more detail some of the effects that can be caused by noise and distortion in the received signal, and what can be done about correcting them.

Below I have listed five different types of possible error in the data display, and I have put them in what I would consider to be in order of decreasing annoyance value:

a) a row of complete "rubbish", i.e. random characters across a complete display row;

b) a row which begins correctly with intelligible data but which becomes rubbish somewhere across the row;

c) a row which is correct in terms of the data it contains but which takes up the position of another row in the display; this may leave a blank row where it should have been situated;

d) a row which should contain information, but which is displayed blank;

e) words which have individual letters incorrect, or missing – other than those caused by typing errors!

Apart from the Hamming correction circuits, which can be considered an instantaneous form of correction, another type of correction can be used which relies on the fact that the pages of information are transmitted cyclically, repeating every 15 seconds or so. If information is written into the data store every time the selected page is received – and not just the first time it arrives after being selected – then some errors such as missed rows, missed letters, etc., can be corrected. Bearing this in mind, we can now consider the types of error mentioned earlier, their causes, and whether they can be corrected by subsequent detections of the correct page.

Rows of complete rubbish are almost always caused by the detection of false framing codes. These arise in several ways. On normal data rows, for instance, a framing code detection will result whenever the sequence of data bits is 11100100. This will occur more often than might be expected since this sequence may occur across "byte barriers" e.g. the letters p , r will be represented by the data bits 00001110 01001111. It can be seen from this that the last four bits of the first group and the first four of the second group combine to form a framing code sequence.

This simple example shows how frequently these framing code detections might occur. The false detection, does not, however, cause any serious problems, as there are two fairly simple ways of overcoming it, both of which are used in this design. Firstly, the output of the framing code detector is gated with a pulse, derived from monostable 17, which only allows through framing codes that occur at the expected position on the television line. This gating pulse is sufficiently wide to allow for expected differences between TV channels, but not so wide as to allow through framing codes caused by byte barriers. Any framing codes which may occur before the correct one are also eliminated in this manner. (It is possible that framing codes may be detected in the colour burst with some types of data separator circuit.) Secondly, the reset waveform to the clock dividers consists not simply of framing code detections, but of the Data Allow latch waveform, which is derived as explained last month. This allows only the first framing code detected on any data line to set the initial timing of the latch enable pulses and ignores subsequent framing code detections on that line.

False framing codes which may be more of a problem, are those that can be detected on lines other than 17, 330 and 18, 331. It has already been pointed out that data is only "looked for" during lines 11, 21, 324, 334, and in this way

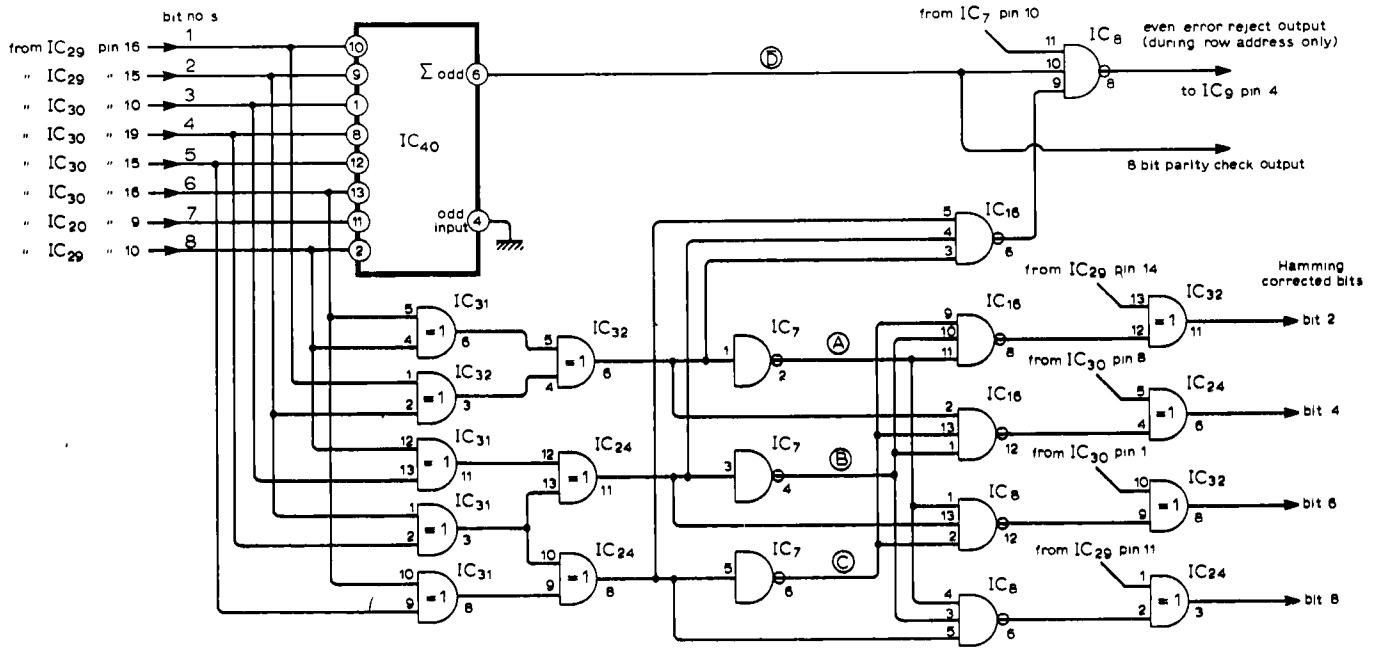


Fig. 3. Circuit diagram of the Hamming corrector. IC_7 is a 7404, $IC_{8,16}$ are 7410, $IC_{24,31,32}$ are 7486 and IC_{40} is a 74180.

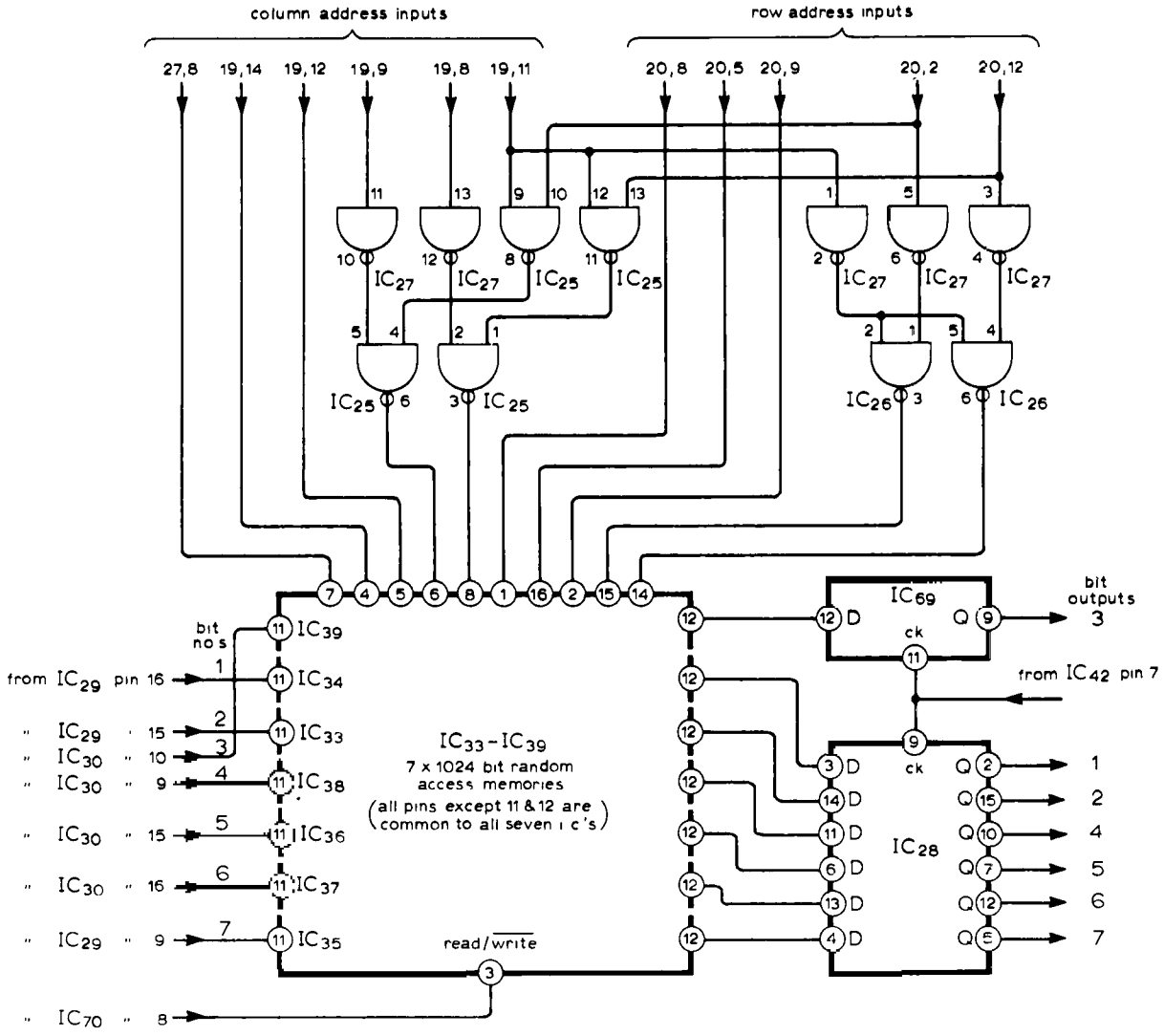


Fig. 4. Circuit diagram of the code converter and data store. $IC_{25,26}$ are 7400, IC_{27} is 7404, IC_{28} is a 74174, IC_{69} is a 7474 and the r.a.ms are 2602B or 2102B.

detections during separated picture information are avoided. However, lines 16 and 329 carry another form of data, and lines 19, 332 and 20, 333 carry insertion test signals. Despite the precautions already taken it is still possible under some circumstances to detect a framing code at the correct time on one of these lines. It is this type of false detection that can cause lines of complete rubbish to be written into the display, and it is this type of error that is most objectionable. The simplest way of overcoming it in this design is to not look for framing codes on lines 16, 329, 19 & 20, 332 and 333 and this can be easily accomplished by inhibiting the entry of data into the 74164 shift register on these lines. This is achieved by feeding the QB output of IC_5 into the second data input of the shift register (shown dotted in Fig. 1). This solution to the problem has the disadvantage that if the allocation of lines in the vertical interval is changed in the future, a modification to the circuit may be required. For this reason the connexion is not included on the p.c.bs, but may be added by means of a wire link if it is found to be necessary.

A second type of error, which is also quite disturbing but which is due to an entirely different cause, is apparent in rows which begin correctly with intelligible data, but turn to rubbish at some point across the line. For this to happen, the framing code must have been correctly detected, but somewhere across the line the divide-by-eight counter generating the latch strobe pulses gets out of step with the data bytes, and this causes the information to turn to rubbish. The most likely causes of this are that the clock oscillator is slightly off frequency, or that some particularly severe noise in the data line causes the clock generator to mistrigger.

The third type of error is the row which appears in the wrong position in the display. This probably has the secondary effect that the position it should have occupied in the display will be left blank, thus effectively making two rows of the display incorrect. This type of error is fairly uncommon in decoders employing Hamming correction, as single errors in the row address will be corrected automatically. Even if an even number of errors are present (2, 4, or 6), the row will still not be written into the wrong position, as even errors can be detected, and in this design they cause the Data Allow waveform to return to "0", preventing any data being written into the store on that row. This means that only errors totalling 3, 5 or 7 bits in the row address group will cause rows to appear in the wrong position on the screen, and this is rather unlikely, except in cases of severe interference (car ignition interference, etc).

The types of error dealt with so far are all very undesirable for the simple reason that they may occur in the display at any time, even if the page is read out correctly the first time, and it is for this reason that the extensive precautions described above are taken to prevent their occurrence. The remaining types of error to be described are less annoying because they are self correcting, i.e., a page may be read out which has errors such as rows or letters missing, but these will be corrected when the selected page is next transmitted in 15-20 seconds time. This is another good reason for having a short

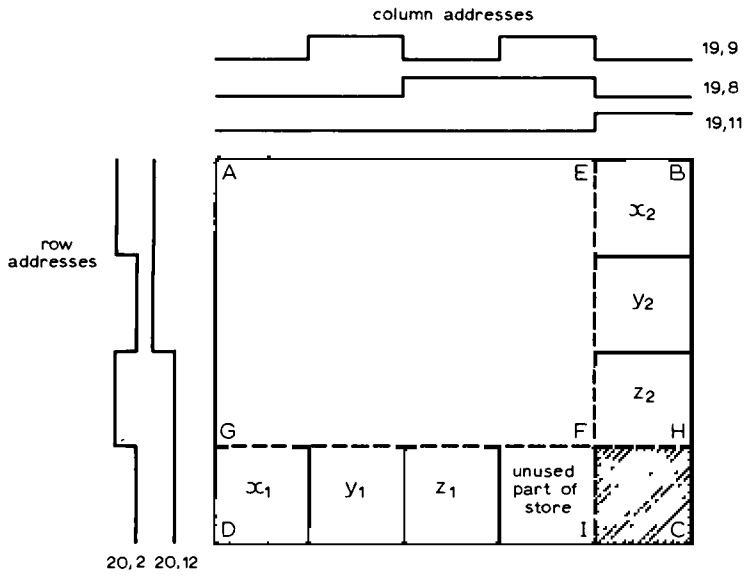


Fig. 5. Diagram showing the operation of the code converter circuit (see text for explanation).

page-access time, since corrections will be made faster.

A blank row in the display may be caused either by an even error detected in the row address group, or by a missed framing code. In either case this type of error cannot cause an already correct page to be made incorrect, and correct information will almost certainly be taken the next time the page is transmitted.

Nothing has yet been said about the parity bit contained in each of the display character groups. This is used in the following way: a parity check is made on each 8-bit data byte before it is written into the store, and if the check is satisfactory the seven bits of the character code are written in the normal manner. If, however, the check shows the parity to be incorrect, nothing is written into the store during that byte. (Anything already in the store at that address location will therefore be unaffected, as only the action of writing removes already-stored information.) This has the effect that when a page is first read out onto the screen, any parity errors will cause characters to be missing from the display. These letters will then be filled in 15 seconds or so later, when the page is next written into the store. Incorrect characters will only be read into the display if more than one error is present in the data word in such a way that the byte-parity is still correct

This, then, is a brief resumé of the more common types of error that can be encountered in the teletext display, and we will now continue the circuit description by looking at the operation of the Hamming corrector circuit.

Hamming correction

It has already been explained that the Hamming-coded bytes contain four message bits and four parity bits. The use of four parity bits enables four separate parity checks to be carried out over the byte and in this way it is possible to determine which one, if any, of the bits is incorrect. If one of the message bits is found to be incorrect, then it is simply inverted, and hence corrected. The table in Fig. 2 shows the parity checks that are carried out and the action taken if one or more of the checks fails. The actual circuit, shown in Fig. 3 does not need to be quite as complicated as the table suggests because there is nothing to be gained by correcting the odd numbered bits (parity bits) and in fact only the message bits are corrected.

Gates (32, 6), (24, 11) and (24, 8) indicate parity checks A, B and C respectively as shown in the table, and the results of these checks are fed into the four three-input NAND gates, (16, 12), (16, 8), (8, 12) and (8, 6). The output condition of these gates determines whether or not the bits from the $\overline{Q}$ outputs of the 7475 latches will be inverted or passed through the exclusive-OR gates unchanged. (Normally the $\overline{Q}$ outputs are inverted by these gates, but if an error is detected, the errant bit is passed through unchanged).

The 74180 eight-bit parity checking i.c. performs a dual function in this circuit. Firstly it is used simply as a parity checker for the ISO-7 coded characters, to determine whether they should be written into the store. Secondly, it is used in conjunction with gate (16, 6) to detect even-order errors during the Hamming-coded bytes. The input to gate (8, 8) from IC_7, pin 10 restricts the detection of even-order errors to the row address group only. As explained earlier an even-order error detected at the output of gate (8, 8) returns the Data Allow waveform to "0", thus preventing the writing of information into the store on that row.

Data store and code converter

The data store consists of seven 1024-bit static random-access memories (r.a.ms). These are m.o.s. devices, but are extremely easy to use, as they have fully t.t.l.-compatible inputs and outputs and require no external pull-up resistors. The printed-circuit boards are designed in such a way that holders may be used for these i.cs to reduce the possibility of damage by "leaky" soldering irons etc. The outputs of these i.cs are only capable of driving one t.t.l. load and must therefore be suitably buffered to obtain the normal t.t.l. fan-out of 10. They also have a somewhat variable access time, which depends on device type, temperature, and the particular 'location' in the store which is being addressed. Although the specification states that the access time will always be less than 1μs, it is important in this circuit that the bits are all time coincident at the output of the store, and this is achieved by using t.t.l. D-type latches on the outputs of the r.a.ms. These D-type latches perform the dual function of providing bit outputs that are time-coincident and with a full fan-out of 10 t.t.l. loads.

The read/write input of the store is normally at the "1" level during the display of data on the screen. When new information is written into the store,

To help readers to buy components, we print here a list of i.cs used in the decoder. The full parts list will follow later. IC_{85-90} are required for a two-r.o.m. character generator, also described later.

1 7493	31 7486	61 7412
2 7408	32 7486	62 7410
3 74121	33 2602B	63 7404
4 7428	34 2602B	64 7474
5 7490	35 2602B	65 –
6 7404	36 2602B	66 7404
7 7404	37 2602B	67 7404
8 7410	38 2602B	68 –
9 74H10	39 2602B	69 7474
10 7493	40 74180	70 7410
11 7474	41 7402	71 7400
12 7427	42 7442	72 7474
13 7400	43 7402	73 2513 (u.c.)
14 7493	44 7410	74 7403
15 7400	45 7420	75 7403
16 7410	46 7402	76 –
17 74121	47 7442	77 –
18 7400	48 7442	78 7474
19 7493	49 7400	79 7474
20 74177	50 7400	80 7474
21 74177	51 7474	81 75107
22 74H04	52 7474	82 7403
23 7430	53 7474	83 7400
24 7486	54 7402	84 7410
25 7400	55 7474	85 2513 (l.c.)
26 7400	56 7474	86 7483
27 7404	57 7400	87 7421
28 74174	58 7410	88 7400
29 7475	59 7404	89 7402
30 7475	60 7412	90 7403

Wireless World Teletext decoder

5—Selection, control logic, control codes decoding and display

by J. F. Daniels

Last month's article concluded the description of the circuitry on digital board 1. This month we continue the description by looking at board 2, which contains the page and time selection circuits, read/write control logic, control codes decoding, graphic and alphanumeric display circuits.

Page and time detection

This part of the circuit indicates when the selected page is reached in the transmission sequence, and it does this by looking at the Hamming-coded information contained in the page header (row address zero) of every page. When a page header is found which contains the same page number as that selected on the thumbwheel switches, an output pulse is obtained which lasts for the length of the data line. If the time-coded mode of operation is selected, a comparison is also made between the transmitted time and the setting of the time-selection thumbwheel switches. The pulse is fed to the read/write control logic which initiates the sequence of writing data into the memories. Before we look at the writing operation in more detail we will consider how this pulse is obtained.

The method of achieving the detection of page number and time coding information is by means of a chain of D-type flip-flops, IC numbers 55, 79, 80, 72 and 64. It should be remembered from an earlier article describing the clock-divider circuits, that IC_{47} produces clock pulses timed to occur during each of the Hamming-coded groups in the page header. (IC_{47}, pin 2 is a strobe pulse during the magazine number group – IC_{47}, pin 10 a strobe pulse occurring during the hours tens group.)

The first of the flip-flops (IC_{55}) is used to define which of the rows are page headers. The first half detects the least significant bit, and the second half the other four, by being fed with output zero of the b.c.d.-to-decimal decoder, IC_{48}. This i.c. is employed very usefully to provide decimal outputs of all the b.c.d.-coded addresses, and these outputs may be fed to all the decimal thumbwheel switch inputs in parallel. It will be noticed that the inputs to this i.c. are not fed directly by the Hamming corrector output, the D input being fed via gates (71, 8) and (63, 8). This is necessary because of the Clear Page bit which may occur during the minutes tens group. If the extra gating was not employed then correct time detection of pages which included a clear bit would not be obtained. The hours tens group does, of course, also contain extra bits to indicate newsflash and subtitle pages, but it is unlikely that either of these types of page will ever need to be time selected, and so no precautions have been taken in this respect.

The action of the chain of flip-flops is initiated by the preset input of IC_{55} which is fed by the Data Allow waveform. By doing this, only valid data rows are interrogated. IC_{55}, pin 8 goes to 1 only during page headers and this waveform is gated with the output of the magazine number flip-flop, to allow operation of the fourth flip-flop, the page units detector.

The wiring of the thumbwheel switch for magazine number detection is slightly different to the rest of the thumbwheel switches. This is because maagazine number eight is coded 000 – or 0 in decimal terms, and there is no magazine number 0 or 9. This switch is wired normally from inputs 1-7, but input 8 must be fed from IC_{48}, pin 1, not pin 10, and inputs 0 and 9 should be left unconnected, as these are unused positions on the switch. From the page units detection flip-flop through to the hours tens flip-flop the i.c.s. form a simple repetitive chain and the output pulse is obtained either from IC_{80}. pin 8 in the normal mode, or IC_{64}, pin 8 in the time-selection, mode of operation.

Read/write logic

This part of the circuit performs a large number of different functions, and before attempting to describe the circuit operation, these will be summarised as follows.

- The basic function is to provide write pulses to the random-access memory store during transmissions of the selected page, in order that the page may be written into the store. As explained in an earlier article, the page is written into the store every time it is received, and not just the first time, in order that any errors may be corrected, and also so that self-changing, and updated pages will be automatically written into the store.
- It must provide a constantly changing time indication in the top right hand corner of the display, and also a continuously changing page header during the time between the "clear" button being pushed and the receipt of the selected page.
- It should detect the clear-page bit, if it is present in the page header of the selected page, and then erase the stored information before writing the new page into the store.
- Finally, in the "auto newsflash" mode of operation, newsflashes selected on the thumbwheel switches must not be written into the store until one is detected that contains a clear-page bit, indicating an updated newsflash.

The circuitry to achieve the above functions is shown in Fig. 1, together with the page and time-selection circuits.

Page selection. The pulse from the page detection circuitry (which goes to 1 during the page header of the correct page) is used to preset the D-type flip-flop IC_{79} after being gated in (71, 6) with the output of inverter (63, 4). This waveform is an inversion of that appearing at gate (12, 12) and was shown in the clock-divider waveform diagrams in Part 2 of the series. It only goes to 1 after the Hamming bits of the page header row address have finished, and it is gated here with the page detection pulse in order to prevent the Hamming bits from being written into the store.

The action of presetting IC_{79} sets the Q output to 1, and this is then gated in (45, 8) with the output of the parity checker, the Data -Allow waveform and the line-blanking waveform. The output of the parity checker is normally at 1 for valid bytes of data, but if a parity error is detected it goes to 1, inhibiting the write pulses. The Data-Allow waveform is gated in at this point to ensure that only valid data lines are written into the

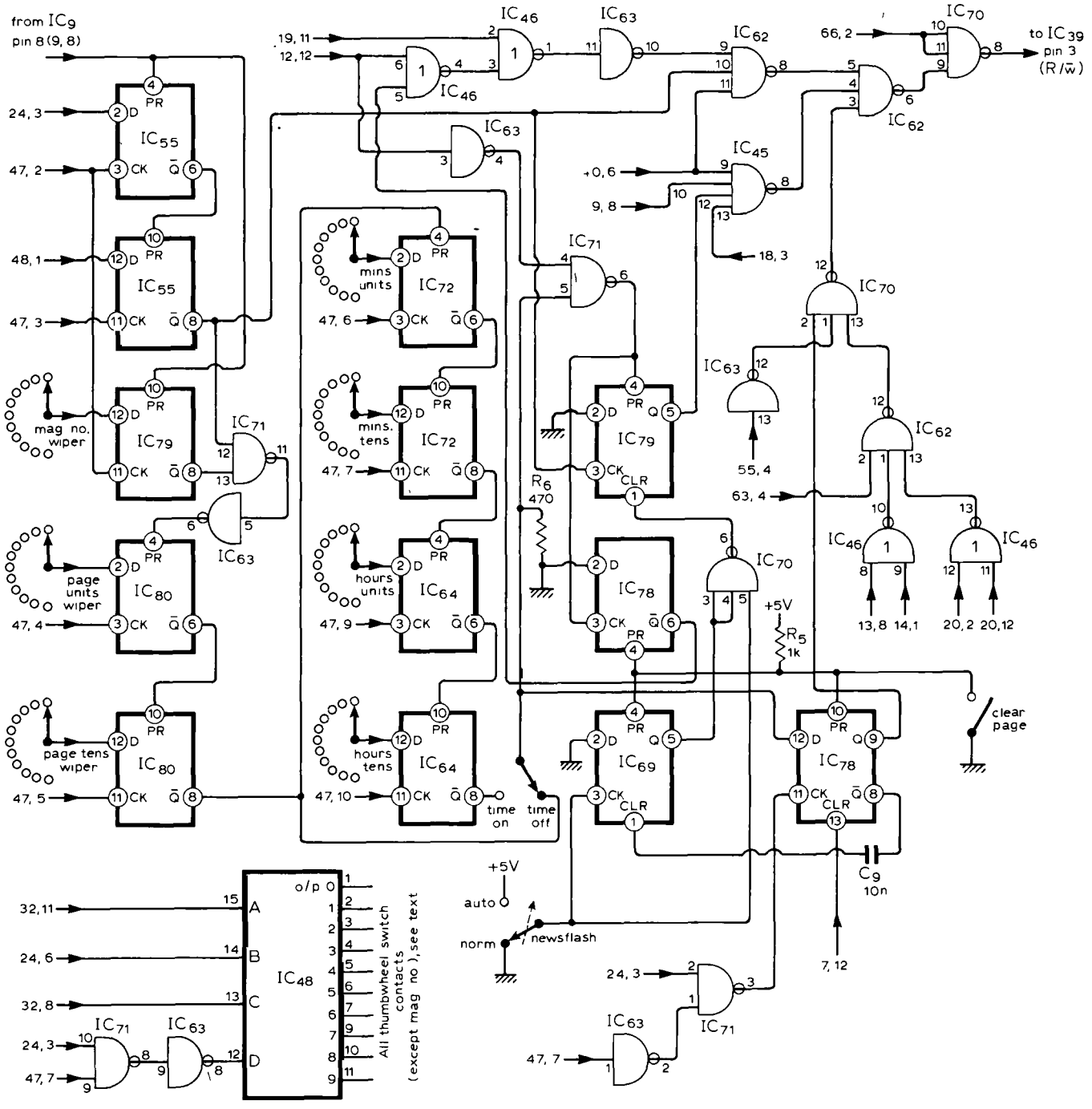
store, and the line blanking waveform further restricts the writing action by inhibiting writing during the framing code and control and row address group bytes. Gate (45, 8) will therefore go to 0 when we require to write information into the store. This, in turn, sets (62, 6) to 1, which allows the write pulses (from 66, 2) through gate (70, 8) and into the read/write input of the store.

This process initiates the writing of information into the store, but it must also be stopped at the end of the page, an operation which is not quite as straightforward as it might appear. The difficulty arises because there is nothing to indicate that the page transmission has finished. Detection of row number 23 to stop the writing action is not feasible because this may be a blank row, in which case it may not be transmitted. The same reason rules out a "stop" signal after a count up to 24 rows. It is possible that more than 24 rows may be transmitted in any given page, as there may be more than one page header containing the correct page number transmitted at any time during the transmission of the page. This may be done to update the time information in the top right hand corner of the display at regular seconds intervals. This last piece of information also precludes another possible way of ending the writing sequence, that of using the detection of the next page header after the correctly detected one.

Fig. 1. Page and time detection circuits and read/write control logic.

(At the present time the BBC quite often transmit two page headers consecutively, and the reason for this will be dealt with later in the article.)

The only way to end the writing sequence is to detect a "wrong" page header, meaning a header of any page other than the one selected on the thumbwheel switches, and this is done by clocking IC_{79} with page header detections, while the D input is held at 0. This returns the Q output to 0 and stops the writing sequence. It may not seem obvious why this does not still stop the writing action even if a second 'correct' page header is transmitted. The reason is that the preset input will always overide the action of the clock input (which only operates on positive-going edges), and the preset input will always be present during the correct page header detections.



It will be noticed from the circuit diagram that the clear input of IC_{79} is fed from the output of (70, 6). However, this only has any effect in the auto-newsflash mode of operation which will be dealt with later. During normal operation the clear input is held at 1 because one input of (70, 6) is held at 0 by the auto/normal switch.

Time display. Having looked at the operation of writing normal pages into the store let us now look at how the continuously changing time information is obtained in the top right hand corner of the screen, and also how the page header is made to "rotate" when the Clear button is pushed. The QD output of counter 19 is very useful in this respect because it goes to 1 only during the last eight bytes of data on each line, which happen to coincide with the point at which the time display information is transmitted on the page header.

This waveform is fed through gates (46, 1) and (63, 10) into gate (62, 6) where it causes the output to go to 1 (so enabling the write pulses) only during parity-correct information. The action of pushing the clear button presets IC_{78}, which is a D-type flip-flop. This sets the $\overline{Q}$ output to 0 which is fed to one input of the two-input NOR gate (46, 4). Here it is gated with the waveform which inhibits writing during the Hamming-coded bytes and is then fed into (46, 1) where it causes the whole of the page header information to be written, instead of just the time information as before.

Page clearing. Another function performed by this part of the circuit is the action of clearing the page when a clear bit is detected in the Hamming bytes at the start of the page header. The clear bit is transmitted during the header of any page which contains new information, i.e. during automatically-changing page, every time it cycles on to the next one of the group, or whenever a single page is transmitted for the first time with updated information.

In order to effect the operation of clearing the page, the store must be filled with 'space' characters, by writing them into the store at all the positions used for display purposes. Now the most convenient way to do this is to use the display period to write in these space characters as the store automatically cycles through all its positions during this time. In fact the system specification allows us to do this as it states that:– "A clear page command for a particular page, and new information for that page will not be transmitted in the same field blanking interval to allow time for the receiver store to be cleared" (hence the need to transmit two page headers in succession occasionally).

Detection of the clear page bit is achieved in gate (71, 3), where bit 8 from the Hamming corrector is strobed by a pulse from IC_{47}, pin 7. The resulting, short, negative-going pulse is used to clock IC_{78}, pin 11, and if the D input is at 1, which it will be during correct header detections, the Q output will also go to 1.

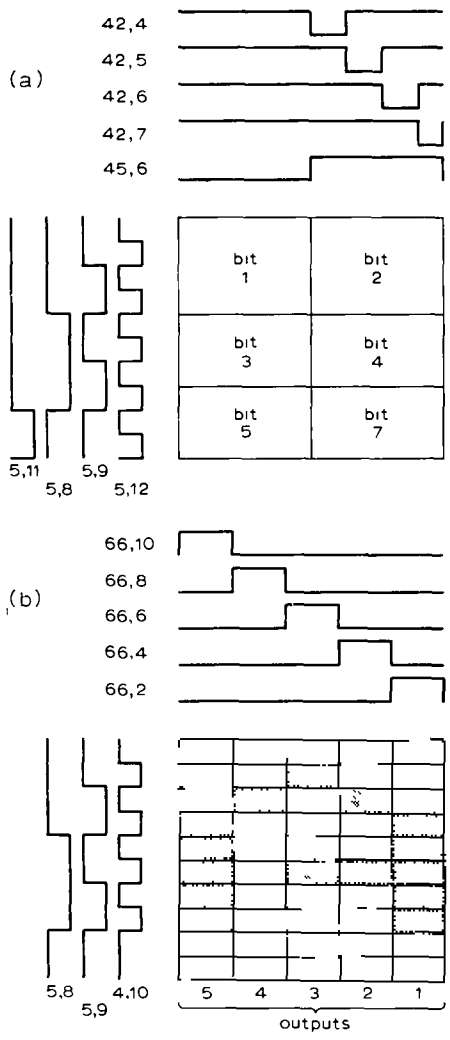


Fig. 2 (a) Graphic character segments are of unequal sizes to avoid gaps between characters. Alphanumeric generation is shown at (b), which does not include the three vertical columns for gaps between characters.

Now there is one slight problem which prevents us using this output directly to initiate the writing action during the display period. This problem is that the header which contained the Clear Page bit will be erased from the store by the action of writing during the display period and the page will then be displayed with no header, except for the time information which will, of course, reappear almost instantly. In this design that is prevented from happening by inhibiting the Clear Page action during the part of the display normally occupied by the header, that is, all the displayed header row except the part occupied by the Hamming coded bytes, which are still erased.

This is achieved with gates (46, 10), (46, 13) and (62, 12) which gate out a waveform corresponding to the display header position on the screen. This waveform is gated with (78, 9) and also the inverse of the Data Allow waveform in (70, 12) to provide the Clear Page action. The inverse of the Data-Allow waveform is gated in at this point to prevent the Clear Page action taking place on valid data rows. The Clear Page action can also be initiated by operation of the Clear Page button which presets IC_{78}, which again sets the Q output to 1. IC_{78} is cleared by negative-going frame sync pulses obtained from (7, 12) which stops the clearing action at the end of the display period.

The operation of deriving the space character codes to be written into the store is achieved in the serial-to-parallel convertor, IC_{21} (74164). In fact, a space character code is not used in this design, merely a set of eight zeroes, obtained by clearing the shift register outputs during the display period. It will be seen from the code table that this is in fact a NUL control character, which is not designated to any particular function, and is in fact inhibited from doing anything in the control codes decoder. (To be described later in this article.) It will of course be displayed as a space character, as are all control characters.

Newsflash. The only other function of this part of the circuit is to provide the Auto Newsflash facility, which is merely a method of preventing any newsflash (or any other pages) being written into the store, until one is found which contains a Clear Page bit.

When one of these "new newsflashes" is detected, the decoder reverts to normal operation, i.e., it writes all the succeeding newsflash pages into the store as well as the one containing the clear bit. In this way errors can still be corrected as described last month.

Normally the auto mode is inhibited by means of gate (70,6), the output of which is held at 1 by virtue of the auto/normal switch. When the auto mode is first selected the positive transition at the clock input of IC_{69} sets the Q output to 0 and this still allows the first newsflash received to be read into the store, regardless of whether it contains a clear bit. However, if the Clear Page button is pushed, this presets IC_{69} Q output to 1 and the output of gate (70,6) goes to 0. This clears IC_{79} and thus prevents any further pages from being written into the store. The Clear Page bit detection circuitry, however, still works as usual and if a newsflash is detected which contains a clear bit, IC_{69} is cleared by a pulse from C_9. This sets the circuit back to normal operation, and all the succeeding newsflash pages are read into the store until such time as the Clear Page button is pushed again.

Graphics generation

Figure 2(a) shows the way in which graphics characters are formed. Bits 1, 2, 3, 4, 5 and 7 each represent one sixth of the graphic shape, and it is intended that when a bit is 1 its corresponding

section of the graphics rectangle should be 'illuminated'. The decision as to how much area shall be occupied by each of the bits is left to the circuit designer, and a number of possibilities will be considered here. If rectangles of equal size were chosen for each of the six bits of information, then the best arrangement would be for the bits each to occupy three lines on each TV field and three out of the four available vertical columns. (The actual size of the complete character box available is ten lines per field and eight clock pulses wide in the horizontal direction.)

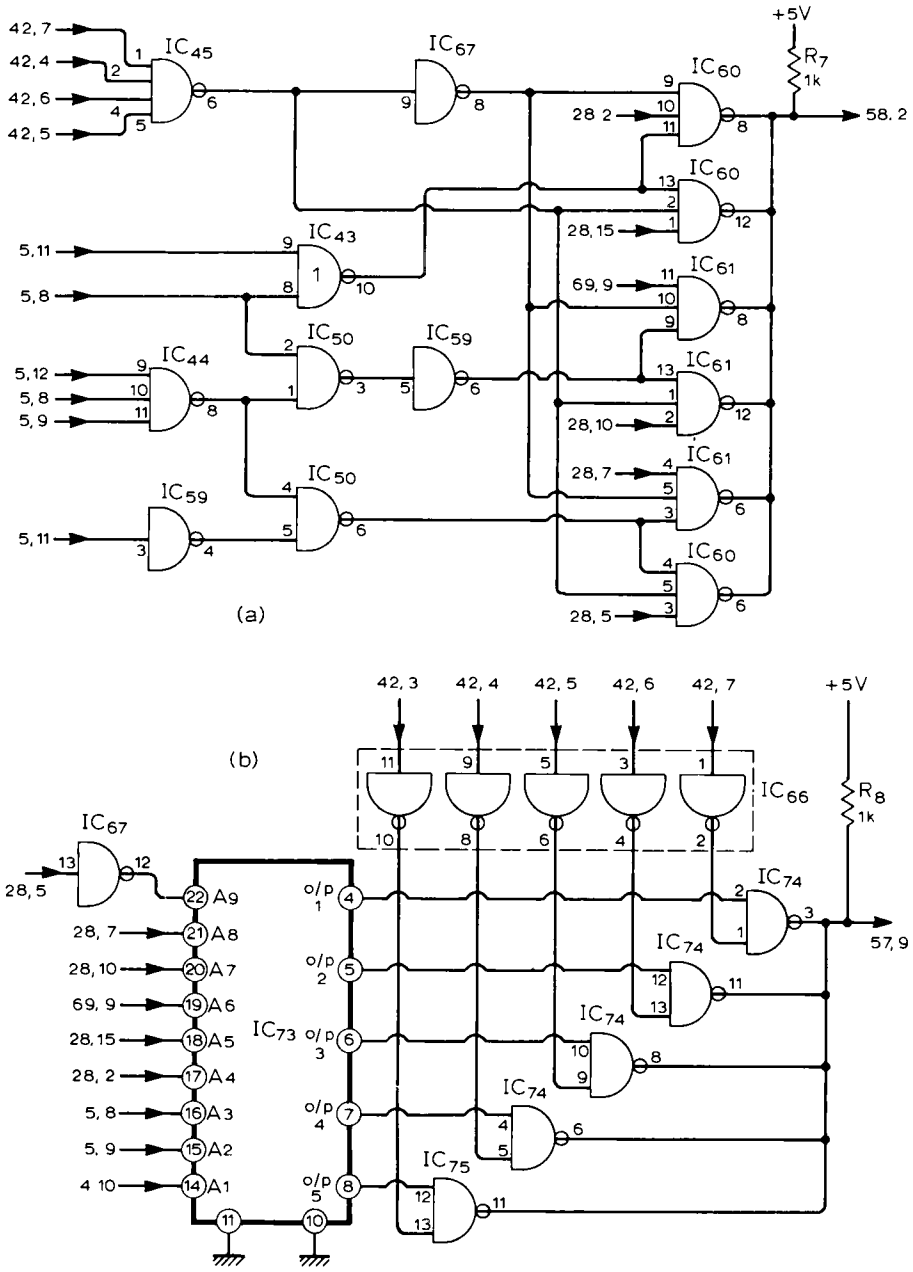
This arrangement would, however, give gaps between each of the graphics characters in the vertical direction, as only nine out of the ten available lines would be used, and in the horizontal direction, as only six out of the eight available clock pulses would be used. Now, although this method would give characters with equal size components, the effect of having gaps between each of them would be most undesirable for displays where large areas of colour were intended to be shown.

In fact the effect of having unequal size rectangles forming the graphics characters is far less disturbing than the effects caused by having gaps between them, and this design uses the format shown in Fig. 2(a) which uses four TV lines per field for bits 1 and 2 and three lines for each pair of the other four bits. In the horizontal direction the bits are equal in width, each one being formed from four out of the eight clock pulses. The reason for making bits 1 and 2 larger than the other pairs of bits, was purely one of simplicity, requiring fewer gates than any other arrangement.

The circuit for generating the graphics characters is shown in Fig (3a). Six, three-input open collector NAND gates are used, one for each bit of the displayed character. One input of each of these gates is fed with the bit information from the output of the r.a.m. store, and the other inputs are fed, one with the horizontal gating waveform, and the other with the vertical gating waveform. The six outputs are added together by the open-collector connexion of the gates and the output at this point is negative-going graphics information. The horizontal gating waveform for the right hand half of the graphics character is obtained at the output of gate (45,6) and the waveform for forming the left-hand half of the characters is simply the inverse of this waveform.

The vertical gating waveform for bits 1 and 2 is obtained by gating two of the line divider waveforms, (5,11) and (5,8) together in NOR gate (43,10). Bits 3 and 4 require the slightly more complicated gating arrangement, achieved with gates (44,8), (50,3) and (59,6), and finally the waveform for bits 5 and 7 is obtained from gate (50,6).

Fig. 3(a) Circuit of the graphics generator. The r.o.m. character generator is at (b).



Alphanumeric characters

The generation of alphanumeric characters is similar in many respects to the graphics characters, the main difference being that each of the alphanumeric characters is formed from thirty-five small squares situated in the character cell. In fact, the character cell is divided into a total of fifty squares, as shown in Fig. 2(b). (This does not include the gaps between characters in the horizontal direction, which take up three extra columns).

The top row of five squares is normally left blank to give a space between rows of characters, and the two lines of five empty squares at the bottom of the character cell are used when lower case characters, which normally descend below the line (g, j, p, q, and y), are generated.

Figure 3(b) shows the circuit diagram of the alphanumeric character generator. It is not practical to use the same approach as in graphics generation using discrete i.cs to form the characters, because this would result in an extremely large number of components. Special i.cs are in fact manufactured to perform the function of character generation, and these are called read-only memories or r.o.ms. The one shown in the circuit diagram is manufactured by Signetics and contains information for sixty-four different characters, including all the upper-case alphabet and various other characters such as brackets, numerals etc.

There are five outputs from the i.c., one for each column of the character, as indicated in Fig. 2(b), and nine address inputs. Three of the address inputs (called row addresses) are used to define which of the horizontal rows of the character is to be displayed, and the other six inputs are used to decide which of the sixty-four characters will

be displayed. The row address inputs are fed from the line divider outputs (5,9) and (5,8), also (4,10) which has been gated to inhibit the output during the last two lines of the character cell. It does this by making the row address "000" during the last two rows, and in this particular r.o.m. the output is always '0' when this row address is present.

The other six address inputs are fed directly from the r.a.m. store outputs. A quick look at the code table might indicate that bit numbers 1-6 should be used here, but as this i.c. is capable of producing upper-case only characters, this would result in lower-case alphabet letters appearing as numerals and various other odd symbols. If, however, bit 6 is replaced with bit 7 inverted, the desired effect of lower-case letters appearing as capitals is achieved.

The outputs of the i.c. are gated with their respective vertical column information in five 2-input open-collector NAND gates, where they are added together to form negative-going alphanumeric characters.

Control-codes decoding and output

This part of the circuit, shown in Fig. 4, performs several functions.

- To detect all the various control codes that are transmitted, for colour, graphics, flashing and boxing information and to switch the output gates to the correct state.
- To provide switching between the graphic and alphanumeric information in the "alphanumeric blast through" mode.
- To add line and field blanking information to the output waveform, and also to blank out the control characters, which of course are not intended for display.

There is also a problem caused by the fact that the standards of transmission have been changed recently, in terms of the position in the code table of some of the control characters. (On February 2, 1976, BBC1 began to transmit the new standard, BBC2 reverting to the old standard.) This problem is overcome by providing three links on the printed board which can be changed according to which type of transmission is being received.

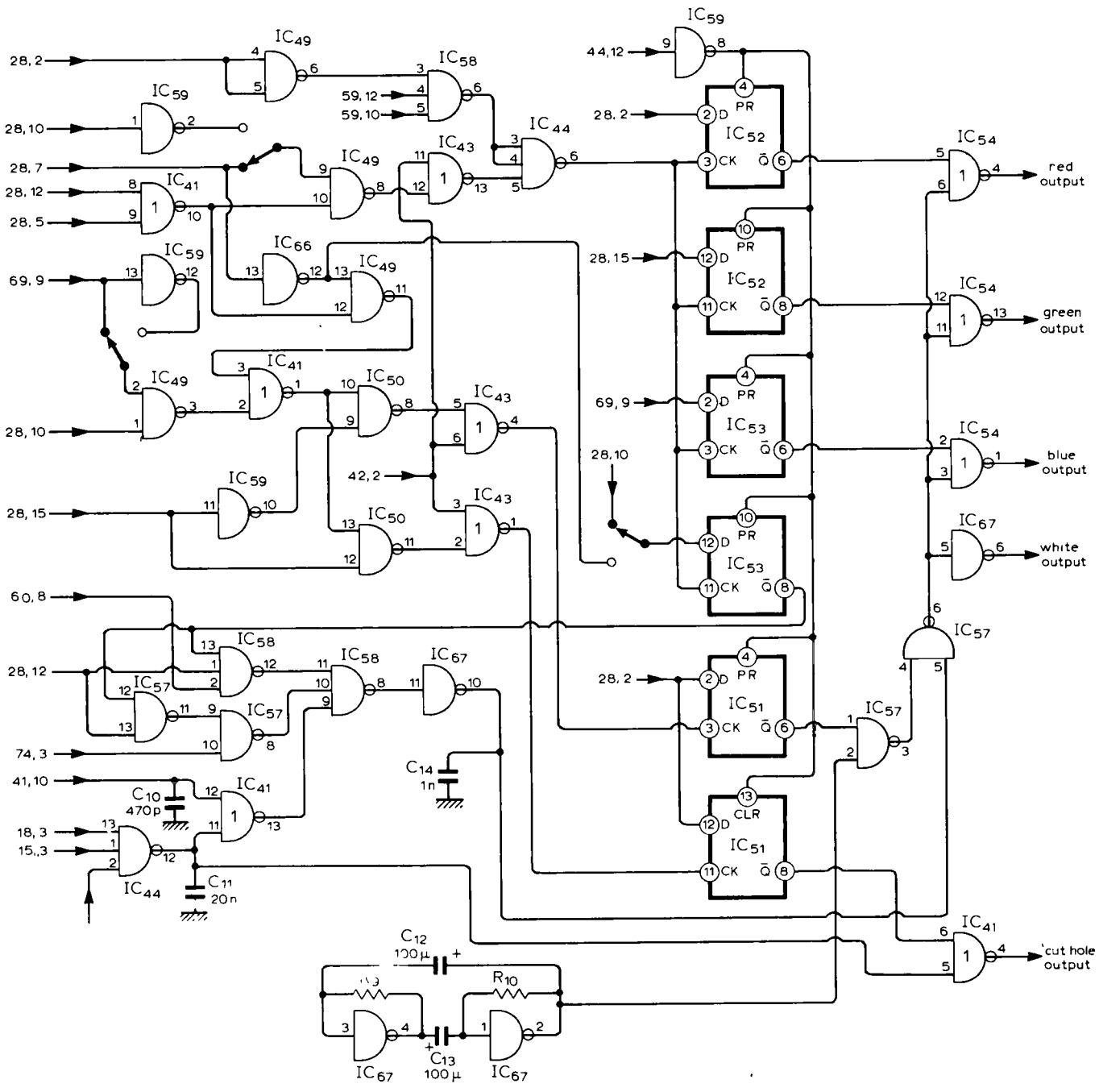
(To be continued)

Fig. 4. The control codes decoder and output circuit.

Corrections

In the list of i.cs, published last month, IC_2, was incorrectly given. It should be 74164.

On page 48, Fig. 3, the connexion to IC_{40}, pin 8 should come from IC_{30}, pin 9, not pin 19.



Wireless World Teletext decoder

6--Lower-case characters and analogue circuits

by J. F. Daniels

The control-codes detection is based on six D-type flip-flops. The first three of these (52,6), (52,8) and (53,6) detect codes which mean "go to red display, green display and blue display" respectively. The fourth one dictates whether the display should be in the alphanumeric or graphics mode, and the fifth one (51,6) indicates when characters should be flashing. The final one is used to derive a wavefrom to switch between the TV and Teletext displays during the insert or boxed mode.

The Teletext specification says that all rows should begin in the steady, alphanumeric white, unboxed condition, and this is achieved by presetting the outputs of the six flip-flops to the required state with the output pulse from (59,8), which is a combined line and field blanking waveform.

Considering first the codes which indicate a change in colour of the display, it can be seen from the code table that bit 1 is always at 1 when a red output is required, bit 2 is at 1 when a green output is required and bit 3 is at 1 when a blue display is required. Combinations of these three bits will also give the complementary colours correctly such as yellow when bits 1 and 2 are both at 1, and also white when all three bits are at 1. The way in which this is achieved in the decoder is to feed bits 1, 2 and 3 respectively to the D inputs of the three flip-flops, (52,6), (52,8) and (53,6) and feed the clock inputs in parallel, with clock pulses occurring only during the fourteen colouring codes in the code table

The clock pulse gating is achieved in (41,10), (49,8), (43,13), (44,6), (58,6) and (49,6). The actual clock pulses are narrow negative-going pulses obtained from decoder (42,2) and are fed into gate (43.13). The other gates merely serve to inhibit the clock pulses at all times other than when a change in colour of the display is required. The input to IC_{49}, pin 9 can be changed by means of the link, from IC_{28}, pin 7 to IC_{59}, pin 2, altering the Clock-pulse-allow waveform to cater for the new code allocations.

The changeover between graphics and alphanumeric operation is obtained in a very similar way to that already described for colours. Flip-flop (53,8) obtains its clock pulses from the same place as the colour changing i.cs and its D input is fed either from (66.12) or (28.10) according to which transmission standard is being received.

Flashing and boxing codes are dealt with, again in a similar way to that already described. Clock pulses are only allowed during the two code positions allocated to flashing and boxing respectively. The D inputs are fed with bit 1 information, and in this way the output of each flip-flop is set either to the on or off condition depending upon which of the control codes is received. Normally, of course, the flip-flops are set to the off condition by the line-blanking waveform, and then somewhere along the character row a flashing code may be received which will set the flip-flop to the on condition. A further code may be received to turn off the flashing or, if no code is received, the line-blanking waveform will again set the flip-flop to the off condition at the end of the row.

Switching between the alphanumeric and graphic displays (both types of character are actually generated for each character box in the display) is achieved with gates (57,8), (57,11), (58,8) and (58,12). Alphanumeric characters are fed into IC_{58}, pin 2 and graphic characters into IC_{57}, pin 10. A feed of bit6 is also connected into IC_{58}, pin 1 and IC_{57}, pin 13. This is to enable the "blast through" mode of operation, in the following manner. Normally when graphics are being displayed, bit 6 is in the 1 condition. If, however, bit 6 is made 0 as for instance in the transmission of upper-case letters, this can be made to switch away from the graphics mode, and into the alphanumeric mode for the duration of the character. In this way switching between graphics and alphanumerics can be obtained very economically, without the need for a separate control character (which would be displayed as a space). The slight disadvantage of this is that only upper-case characters in columns 4 and 5 of the code table may be displayed in this way.

Gate (58,8) is fed with the outputs of gates (57,8) and (58,12), containing the graphics and alphanumeric characters respectively. A third input to this gate is fed with a composite blanking waveform which contains both line and field blanking, and also information to blank the control characters. Gate (44,12) adds together the line and field blanking waveforms, and a third blanking input is provided here which may be used to blank the Teletext display output while watching TV programmes. (It is possible that the Teletext waveform could break through onto the TV picture under some circumstances, if the leads were not properly screened, for instance.) The output of this gate is delayed by capacitor C_{11} to allow for delays in the r.a.ms and r.o.m. This output is added to the control-character blanking waveform in gate (41,13) and the output of this gate is then fed into (58,8) where it serves to blank the video display waveform.

The output of (58,8) is then inverted and gated with the output of the flashing oscillator formed from (67,2) and (67,4). This flashing oscillator is allowed by the D type flip flop (51,6) and gates the display waveform in (57,6). At this point the composite display waveform exists in monochrome form, and then the colours are incorporated by gating this monochrome waveform in the 2-input NOR gates (54,4), (54,13) and (54,1). The three D-type flip-flops enable or disable these gates to form the red, green and blue outputs.

Finally the output of the flip-flop (51,8) is gated with the line and field blanking waveforms to give an output which can be used as a switching waveform when a "boxed" display is wanted.

Lower-case characters

The character-generation circuit already described is capable of generating only upper case, or capital letters. Although this does not detract in any way from the information-carrying capabilities of the system, some people may consider it worthwhile to add the extra circuitry required to display lower case characters.

The method is exactly the same as that described last month for upper case characters, except that some lower case letters, i.e. g,j,p,q,y, drop below the line of normal characters. Provision has already been made for this as the character box is ten lines high and only the top eight lines are used for the upper-case characters and a space line between characters. This leaves two unused lines available to display lower-case descenders.

The same type of r.o.m. is used to contain the lower-case characters, the only difference being that the lower-case memory only contains the thirty two characters in columns six and seven of the code table, the other thirty two spaces being left blank. The complication arises from the fact that characters stored in the memory can only occupy up to eight lines of the display, as the row-address information to the r.o.m. consists of only three bits of information. Fortunately, however, none of the characters having descenders contains information in the top two rows of the character box, and this enables the character to be stored in the r.o.m. two rows higher than its intended display position, as shown in Fig. 1. This means that when the row addresses are applied to the r.o.m. they must be changed for those characters which have descenders, in order to lower the display position by two TV lines.

Figure 2 shows the extra circuitry needed to produce lower-case characters, and in practice these additional i.cs are mounted on a small board which fits above digital board 1 at the opposite end to the analogue board. I.cs 87, 88, 89, and 90 are used to detect the characters which require lowering by two rows, and this information is available at gate (89,4) where a 0 denotes a normal character and a 1 indicates a character that should be lowered by two rows.

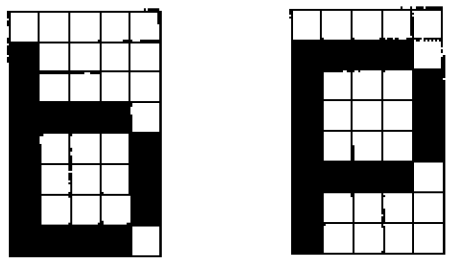


Fig. 1. Lower-case letters with "tails" are stored in the same memory rows as ordinary letters. Row addresses are changed during readout to lower the letters by two rows.

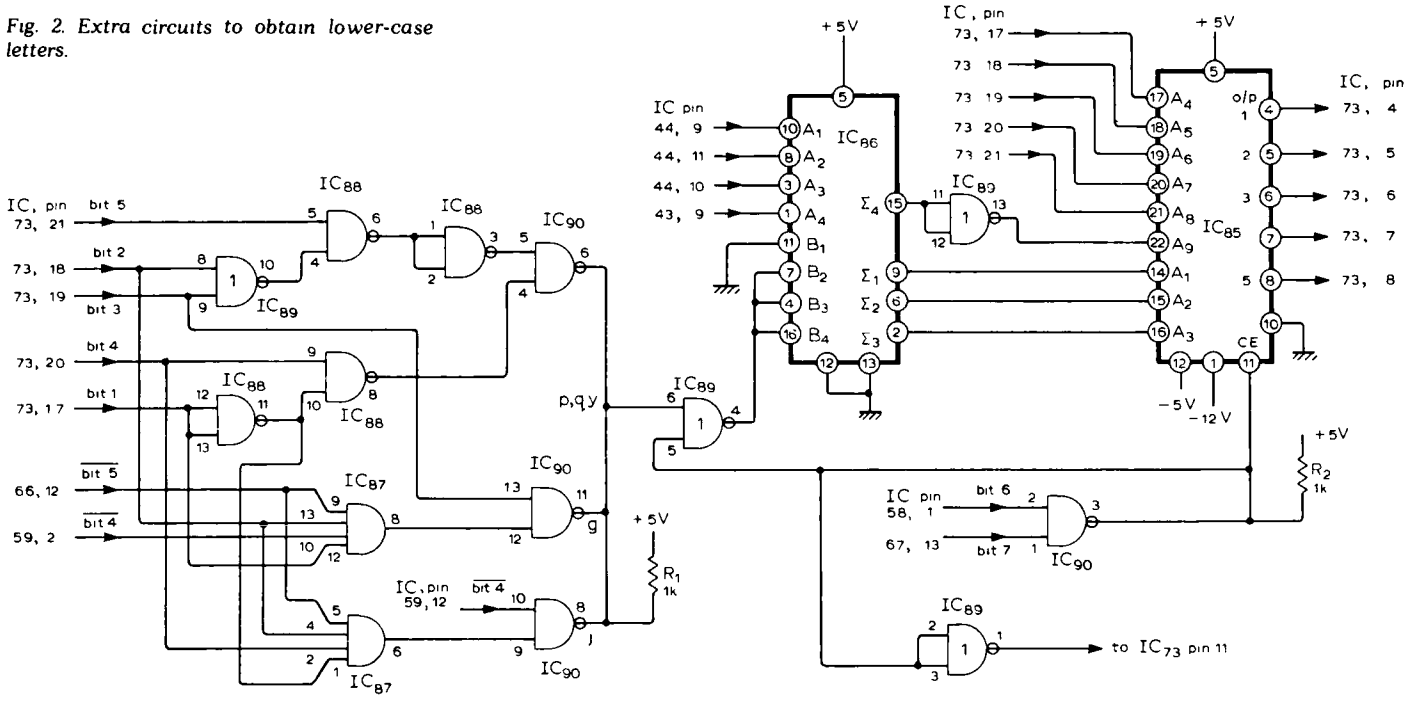
The character generator, IC_{85} is of the same type as the upper case one, a 2513, but its suffix CM3021 indicates that it is programmed with lower case characters. (The upper-case version is suffixed CM2140). Switching between the outputs of the two character generators is facilitated by their "tri-state" outputs. This means that as well as having the normal states of 0 and 1 at the output pins, a third condition can be obtained where the output pin is effectively open-circuited from the rest of the i.c. This third state is controlled by the "chip enable" input, and by suitable control of this input, any number of 2513's may be connected to the same five output rails. In this circuit, switching between the two r.o.m.s is controlled by gate (90,3). The output of this gate goes to 0 only during columns 6 and 7 of the code table, enabling IC_{85}, and the inverse of this waveform is fed to the chip enable pin of the upper-case character generator IC_{73}, enabling it during columns 0-5 of the code table.

The row addresses to IC_{85} are fed from IC_{86}, which is a four-bit binary full adder, type 7483. The A inputs are fed with the four-bit row-address information from the line counter IC_5, and the B inputs are fed either with a binary zero, during normal characters, or the binary number fourteen during characters which require descending by two rows. Sum outputs one, two and three are fed to the row address inputs of the r.o.m. and these will change for a descended character in such a way that the character will be lowered by two TV lines. Sum output four can be used as a blanking waveform to inhibit the generation of characters during the top two rows of the character box, when a descended character is displayed. The blanking is achieved by means of gate (89,13) which switches the character generator to one of the blank character spaces during the required blanking period. This method of achieving the blanking is extremely useful, as the delay applied to the blanking waveform will be similar to the delay of the character read-out of the r.o.m. (about 400ns). If the blanking had to be added externally to the r.o.m. then some means of delaying the waveform by a suitable amount would have to be found. A useful feature of the lower-case circuitry is that only one track on the upper-case printed board has to be cut when adding the extra board (the chip-enable pin of IC_{73}) and all the connections to the existing boards may be made to the underside of digital board two, which entails a minimum amount of disturbance to the existing upper-case circuitry. For this reason also, I would suggest that the decoder should be built and tested as an "upper-case only" unit initially. The lower-case board can be added later as there is no extra line-up procedure required when this board is fitted.

Analogue board

This board serves three main functions, namely to provide feeds to the digital boards of mixed syncs, separated data,

Fig. 2. Extra circuits to obtain lower-case letters.



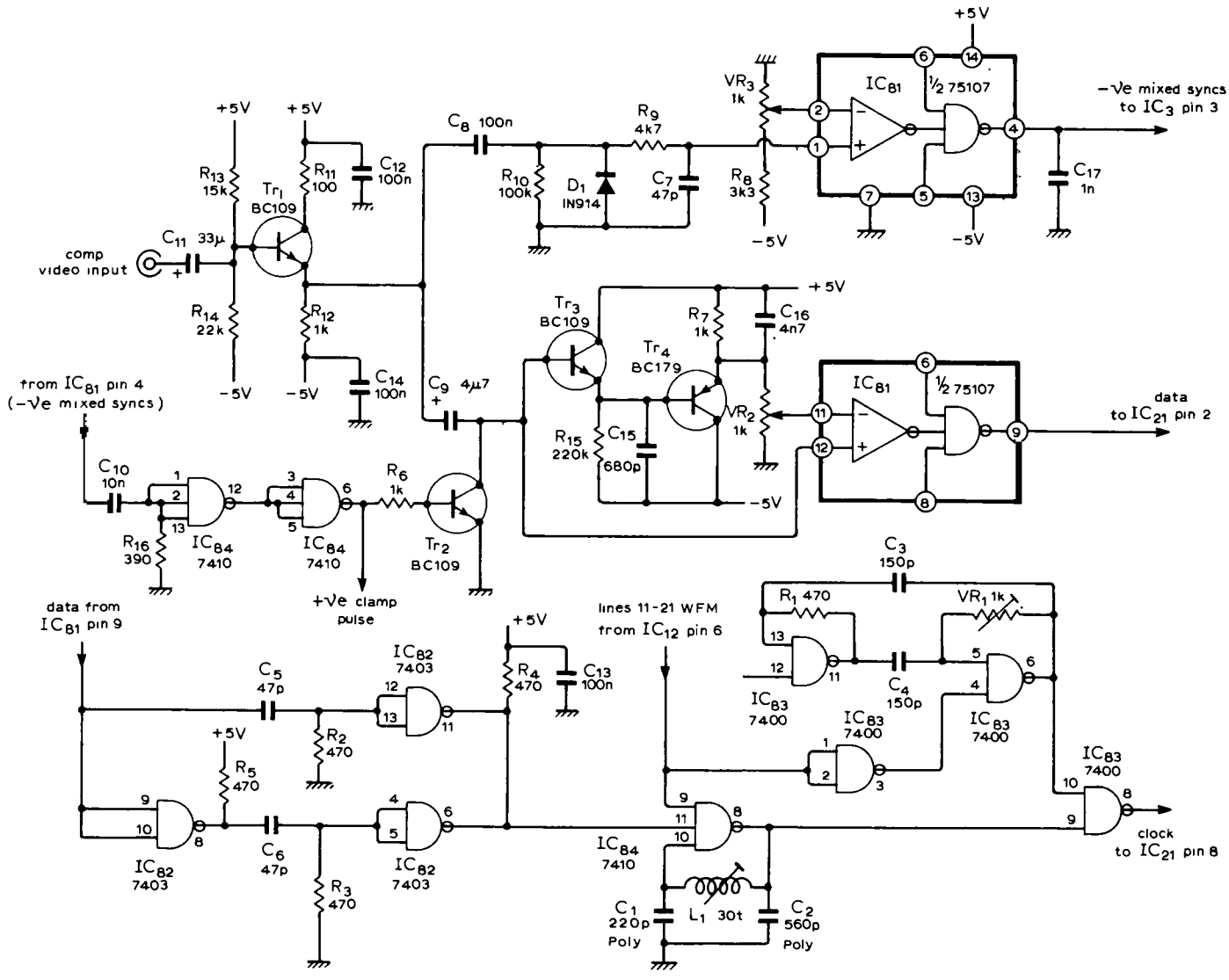


Fig. 3. The analogue circuitry to produce syncs, data and clock.

and a switched clock waveform which is suitable both for the writing of data into the store and for reading it out during the display period. The input to the analogue board, the circuit of which is shown in Fig. 3, should consist of a composite positive-going video waveform of between about 1 volt and 5 volts peak to peak. Tr_1 is an emitter-follower buffer which provides a suitable low-impedance source to drive the d.c. restorer formed from C_8, R_{10} and D_1. This restores the sync tips of the video waveform to a potential of about −1 volt. Chrominance information is then removed by the low-pass filter R_9, C_7, and the remaining video signal is fed to the positive input of a difference amplifier. The negative input is connected to a potentiometer which controls the point at which the video waveform is sliced. The best setting will depend on the amplitude of the video waveform, but the range of the potentiometer should be great enough to cover the whole of the sync portion of the video waveform and enable separated syncs to be obtained at the output of the difference amplifier. This i.c. is in fact a high-speed dual line receiver with fully t.t.l.-compatible outputs and is ideal for use in this type of circuit.

A mixed sync waveform could, of course, be obtained from the TV receiver in which the decoder is to be installed, but it was felt that it would be better to include one in the decoder if only to reduce the number of connections to the TV set. It also has another advantage in that the decoder may be fed from a "video ring main" where a separate feed of syncs may not be available.

As well as feeding the digital boards, the feed of mixed syncs is used to generate a clamp-pulse waveform which is used both on the analogue board and the video switching interface board in the TV receiver. The positive going trailing edge of the line sync waveform is differentiated by C_{10} and R_{16} and coupled into gate (84,12). The resulting negative-going pulse is inverted by gate (84,6) and a positive going clamp pulse is obtained which is about 4µs wide, and occurs during the back porch of the video waveform.

This pulse is used in the analogue board to clamp the video waveform before slicing the Teletext-data in a similar way to that used in the sync separator. Before describing this in great detail, however, it would be as well to discuss some of the problems involved in successfully slicing the data signal.

Data slicing

In the simplest possible system, the video waveform could be fed via a capacitor into the positive input of a differential amplifier and by varying the direct voltage level on the negative input by means of a potentiometer, sliced video and data would be obtained at the output. The fact that picture information is sliced, and present at the output, is immaterial as precautions against this causing trouble have been taken elsewhere in the digital circuitry. However, because of the nature of the video waveform, the varying picture information will cause the average voltage of the signal to vary, and thus alter the position at which the video (and data) is sliced. If the data information were transmitted as perfect square-shaped pulses this would not matter because the output mark/space ratio of the data information would remain unaltered. However, the data cannot be transmitted in this way because the bandwidth requirements would become infinite, and the transmission system must be tailored to suit the normal TV band-

width of 5.5 MHz. The data is in fact transmitted in the form of raised cosine pulses, and this implies that the data must be sliced fairly close to the halfway point between its positive and negative peaks, if the mark/space ratio of the received data is to be close enough to the original for correct decoding. This is the case even if the received signal is completely undistorted by the receiver tuner and i.f. strip. In cases where the receiver i.f. amplifier has insufficient bandwidth or large group-delay errors, or the aerial is mismatched into the receiver, the setting of the slice level will be even more critical and in very severe cases of "ghosting" or i.f. misalignment it may be impossible to find a suitable point at which to slice the video waveform and obtain error-free readouts. The simple system described above could only be adjusted to give satisfactory results during periods of static transmission such as test card, where the picture information is constant and the slice level would remain unaltered.

One way to overcome the problem of changing level of the video waveform would be to use the d.c.-restored video present at the cathode end of D_1. However, a better system is to clamp the video during the back porch, and this method is used in this design. Tr_2 is

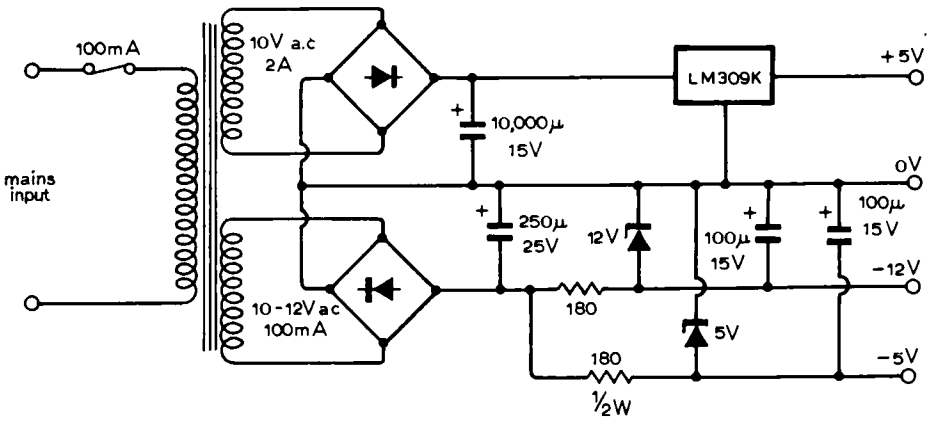


Fig. 4. A suggested power supply circuit.

turned on during the back porch by the clamp pulse, thus holding black level to approximately 0 volts regardless of the average level of the signal. Purists may point out that the clamp action will be upset by the colour burst. In practice, however, this only becomes a problem if large variations in level of the chrominance information occur, which will in turn cause the clamping point to vary slightly. If this is really a problem that cannot be solved by improving the aerial installation, then a 4.43MHz tuned circuit should be included in series with the collector of Tr_2. It has not been included as a standard feature in the circuit, partly because it has not proved niecessary, but mainly because it would be rather difficult to set up correctly without expensive test gear.

The system described so far, consisting of a clamped video signal, sliced by means of a differential amplifier having a variable voltage level at its second input, is capable of giving very good results under most reception conditions. The slice level setting can be fairly critical under adverse conditions, however, and although the black level end of the waveform is maintained at a fixed level by the clamp, variations in amplitude of the video signal will also cause unwanted movement of the data level.

Small variations between the signal amplitude of different TV channels which may occur with some types of i.f. strip can be enough to prevent correct decoder operation. A more likely cause of video amplitude variations will occur in TV sets where the contrast control operates in the a.g.c. line. In this type of set the detected video information will vary as the contrast control is changed and nowhere in the circuit will a video waveform be available that does not vary with contrast control changes. It is obviously undesirable to have to alter the slice level whenever the contrast control is adjusted and some form of compensation must be provided to automatically keep the slice level correct. One method would be to have a variable gain video amplifier which was automatically adjusted to keep the data amplitude constant. However, this

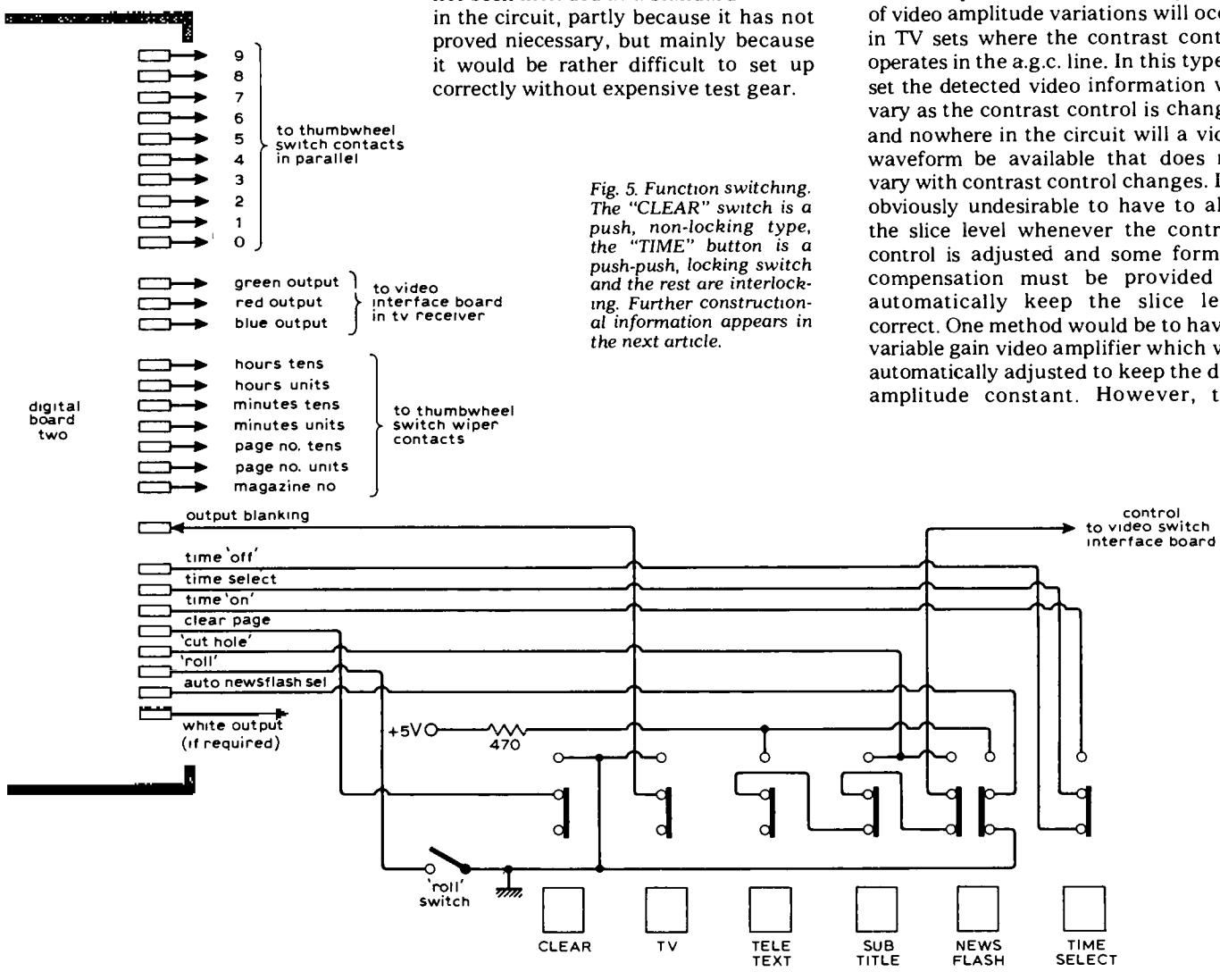


Fig. 5. Function switching. The "CLEAR" switch is a push, non-locking type, the "TIME" button is a push-push, locking switch and the rest are interlocking. Further constructional information appears in the next article.

would undoubtedly be expensive, and a much simpler way of achieving the same end is to alter the slice level automatically, to enable it to follow the varying data amplitude. This is done by detecting the data amplitude with a peak-detector circuit and then using this information to set the slice level midway between the data peaks and black level.

Tr_3 forms the positive-data peak detection circuit with the decay time set by the time constant R_{15}, C_{15}. This time constant is made fairly long compared to the data bytes to prevent too much decay during the worst case condition of fourteen consecutive zeros. TR_4 then serves to offset the base-emitter voltage drop of Tr_3 and the shorter time constant R_7, C_{16}, increases the rise time of the peak detector circuit to reduce the effect of large noise spikes. The actual slice level is adjustable by means of VR_2 over the full range from 0 volts to the positive data peak level. Although theoretically this potentiometer should be in its mid position for correct data slicing, non-linearity distortion introduced by certain types of vision detector circuit will mean that the best results may be obtained if the slice level is not mid-way between the positive and negative peaks of the data. The difference amplifier used to perform the actual data slicing is the other half of the dual line receiver, IC_{81}.

Clock generation

It has already been explained that the clock waveform generated on the analogue board consists of the outputs of two oscillators, one locked to the incoming data, and the other adjustable in frequency to enable the display width to be adjusted. Switching between the two clock generators is performed by the 'lines 11-21' waveform. Gates (83,11) and (83,6) are cross coupled to form a free running oscillator. Oscillation is inhibited during lines 11-21 by the waveform present at gate (83,3), and by also inhibiting oscillation at the start of each TV line – Q of monostable 3 is fed into gate (83,11) – the oscillator is phase-locked to the TV lines. This ensures that the characters will have "clean" verticals. If the oscillator was merely free running the phase would alter at random from one TV line to the next, and ragged verticals would result. VR_1 adjusts the frequency of oscillation and forms the display width control.

Gate (84,8) forms the active part of the data clock oscillator. The frequency of oscillation is determined by L_1, C_1 and C_2. The waveform on pin 9 of the i.c. only allows oscillation to take place during lines 11-21, and at all other times the gate output is held at 1 allowing the display clock through gate (83,8) to the output line. The oscillator is locked to the incoming data by means of narrow negative going spikes fed into the third input of (84,8). These spikes occur at every data transition, gate (82,11) providing the spikes derived from positive-going data transitions, and gate (82,6) spikes derived from negative-going data transitions. Although the oscillator circuit may appear rather crude, it has been found to give excellent results in practice. The main point in its favour is that it is extremely easy to set up, as there is only one adjustment, that being L_1. The specified coil former is the Neosid A6 assembly, but in practice equally good results will be obtained with any former of approximately 3/16in diameter, containing an adjustable ferrite core, so long as it can be tuned in to the correct frequency of about 7MHz. The frequency stability of the circuit has been found to be perfectly adequate so long as polystyrene capacitors are used for C_1 and C_2. The preferred method of adjusting the oscillator frequency will be dealt with later in the article, as will the rest of the decoder line up.

Power supply

The power requirements of the decoder are fairly modest. Five volts for the t.t.l. circuitry is required at approximately 1.3A, and this can most conveniently be obtained from a three-terminal regulator of the LM309K variety. The input voltage to the regulator must not be too great, however, as the device will be working fairly close to its limits and may exceed its maximum power dissipation figure. For this reason, the regulator must be mounted on a suitable heatsink.

A negative five-volt supply is required at a current of about 25mA, and a negative 12-volt supply for the character-generator i.c. at only a few milliamps. Both negative supplies may be derived from simple zener-diode type stabilizers, and a suitable power supply circuit is shown in Fig. 4.

Constructors should see that the connecting wires between the power supply and the decoder are of a suitable gauge to prevent excessive voltage drop of the plus five-volt rail. At a current of something greater than one amp, it only takes a few feet of thin connecting wire to cause a voltage drop of greater than 0.25 volts which will be sufficient to bring the five-volt rail outside the recommended specification for t.t.l. devices.

(To be continued)

The next article in this series will give constructional details of the teletext decoder. Subsequently there will be an article on interfacing the decoder with various colour television sets in common use.

Who thought up the synchronous satellite?

Dr Harold A. Rosen, a vice-president of Hughes Aircraft Company and a pioneer developer of synchronous communications satellites, has won the first L.M. Ericsson International Prize for "proposing the introduction of geostationary communications satellites and for his scientific and technological contributions to their development, design and operation." The prize, of 100,000 Swedish crowns (about £11,000) will be presented by King Carl XVI Gustaf at ceremonies in Stockholm in May. To be awarded every three years, the prize honours the memory of Lars Magnus Ericsson, founder of the L.M. Ericsson Telephone Company.

Dr Hakan Sterky, chairman of the prize committee, says "Dr Rosen proposed that a single satellite could be orbited at an altitude where it matches the earth's rotation and appear to be stationary, thereby simplifying connection with earth stations and providing 24-hour-a-day service". British readers, in particular, will be surprised that no acknowledgement is made to Arthur C. Clarke, who is widely considered to be the originator of the idea of satellites in synchronous orbit. Clarke pointed out in the October 1945 issue of *Wireless World* (eleven years before Dr Rosen joined Hughes) that a space-station orbit with a radius of 42,000km "has a period of exactly 24 hours. A body in such an orbit, if its plane coincided with that of the earth's equator, would revolve with the earth and would thus be stationary above the same spot on the planet. It would remain fixed in the sky of a whole hemisphere and unlike all other heavenly bodies would neither rise nor set." Further, a satellite in this orbit "could be provided with receiving and transmitting equipment . . . and could act as a repeater to relay transmissions between any two points on the hemisphere beneath . . ." (See "Extra-terrestial relays", October 1945, pp. 305-308).

Hughes Aircraft state that all of the Intelsat communications satellites "are a result of Dr Rosen's synchronous-orbit concept." This is strange in view of the fact that it was a vice-president of Hughes Aircraft Company, Dr F. P. Adler, who gave public acknowledgement to Clarke's proposal more than a decade ago (June 1965 issue, p.269). Moreover, L. M. Ericsson have indicated that they know of Clarke (although they do not seem to be aware of the thoroughness of his 1945 proposal). Readers may be forgiven for questioning whether it really was Dr Rosen's concept.

Wireless World Teletext decoder

7 — Construction and interfacing with the television receiver

by J. F. Daniels

Construction techniques

Many different methods of construction are possible because the circuit is fairly non-critical in terms of i.c. layout. High-frequency decoupling should be used on the power supply rails, and about one 0.047μF capacitor for every ten i.cs should be adequate. Extra decoupling should be employed close to the two clock oscillators and also on the plus and minus five volt rails close to IC_{81}, the dual difference amplifier.

For those constructors who intend to use the p.c. boards available from Catronics Ltd, the following hints on construction may be useful. The first thing to do is to make up the through connection holes using tinned copper wire. As there are a great many of these to do, the following method will probably be found to be the quickest. Support the board, component side down, about ¼in above a flat surface. Take a long length of suitable tinned-copper wire and push it through a hole that requires connecting through until it rests on the surface under the board. Solder it on the upper surface of the board and cut off with side cutters. Continue by soldering all the wires on the same side of the board, and then turn it over and solder the other side. The underside of the board is done first because it is easier to differentiate between connecting holes and i.c. holes on this side. Holes for capacitors and resistors are distinguished by the fact that they have larger "roundels".

After the connecting process has been carried out on the two digital boards, the i.c.s. may be mounted, and care should be taken here to ensure that no pins are left unsoldered. Only some pins require soldering on the upper surface of the boards and these are indicated by roundels. Where space permits these roundels have extra tabs to increase the soldering area. Great care should be taken when soldering the m.o.s. random-access memories on board one, and similarly the read-only memory on board two. Although all the inputs are protected to a certain extent against static charges, care should be taken to ensure that the soldering iron tip is adequately earthed. The printed-circuit boards have been designed in such a way that i.c. holders may be used for the m.o.s. devices to avoid soldering on the top surface of the board and this is probably the safest, if slightly more expensive solution.

Capacitors, resistors and preset potentiometers can then be added. Some of these components may require soldering on both sides of the board and the best rule to follow is: wherever there is a roundel, solder it!

When both of the digital boards have been completed they should be joined together by wire links along the rear edge of the boards. These links are best made from lengths of insulated stranded wire, each one being about two inches long. This enables the boards to be "opened out" if access is required to the i.cs on the lower board. At this stage the four power supply leads may be connected to the lower board. (Note that the two leads for the −5 and −12 volt supplies only go to the lower board, and no links are used to the upper digital board at this point.)

The analogue board may now be constructed. This is only a single sided board and a number of wire links are required as shown on the layout diagram. The analogue board is intended to be mounted above the upper digital board at the right hand end. Three wire links are needed at the upper (short) edge to the lower digital board, for the plus 5, minus 5 and 0 volt rails, and five more links at the top end of the right hand edge are connected to adjacent pads on the uppermost digital board. These links to the analogue board should be long enough to allow removal of this board, to allow "unfolding" of the two digital boards.

Connections to all the decoder function switches are made to the right-hand edge of the lower digital board and this board projects further than the other boards at this end to facilitate connection of the leads. The suggested method of connecting the function switches as shown in Fig. 5 (April).

If lower-case characters are being included in the decoder the extra board should be made up in a similar way to the two larger boards. The extra board is intended to be mounted above the upper digital board at the left-hand end, opposite the analogue board. Wires should then be connected from this board to the underside of the lower digital board. It is advisable, however, to get the decoder working and lined up before adding the lower case board, as any faults will be located more easily if the lower case board is not present.

Video switching and interface

This board is mounted in the TV receiver and must be capable of switching the red, green and blue outputs of the Teletext decoder into the receiver in place of the TV picture. Before describing some typical receiver and video switching circuits, it would be as well to examine the problems which will arise, and describe ways of overcoming them.

Let us assume that we have an "ideal" receiver which we wish to modify. This receiver will have three identical video amplifiers for the red, green and blue signals and the amplifiers will have capacitor-coupled inputs, i.e., the amplifier will be internally biased and clamping of the three signals will take place at the c.r.t. cathode. The amplifiers will require an input of about 4V pk-pk and have a flat amplitude frequency response up to at least 5.5MHz.

If a receiver with this type of amplifier were being modified, a simple method would be to use a three-pole changeover relay to disconnect the amplifier inputs from the red, green and blue picture information and connect the outputs of the Teletext decoder. Although this method would produce a perfectly acceptable Teletext display, it would have the disadvantage that newsflashes and subtitles could not be shown in boxes, as intended.

In order to display boxed information, the video switches must operate very rapidly, preferably with a switching time of less than about 300ns. This, however, is not the complete answer, because if switching is attempted between the decoder output and capacitor-coupled or "floating" picture information, the background brightness and colour of the display box will change, depending upon the average level of each of the three picture waveforms. This can be overcome fairly easily by clamping the three TV waveforms and the three Teletext output waveforms to the same potential prior to switching. The output of the video switches can then be capacitor-coupled into the output amplifiers as before.

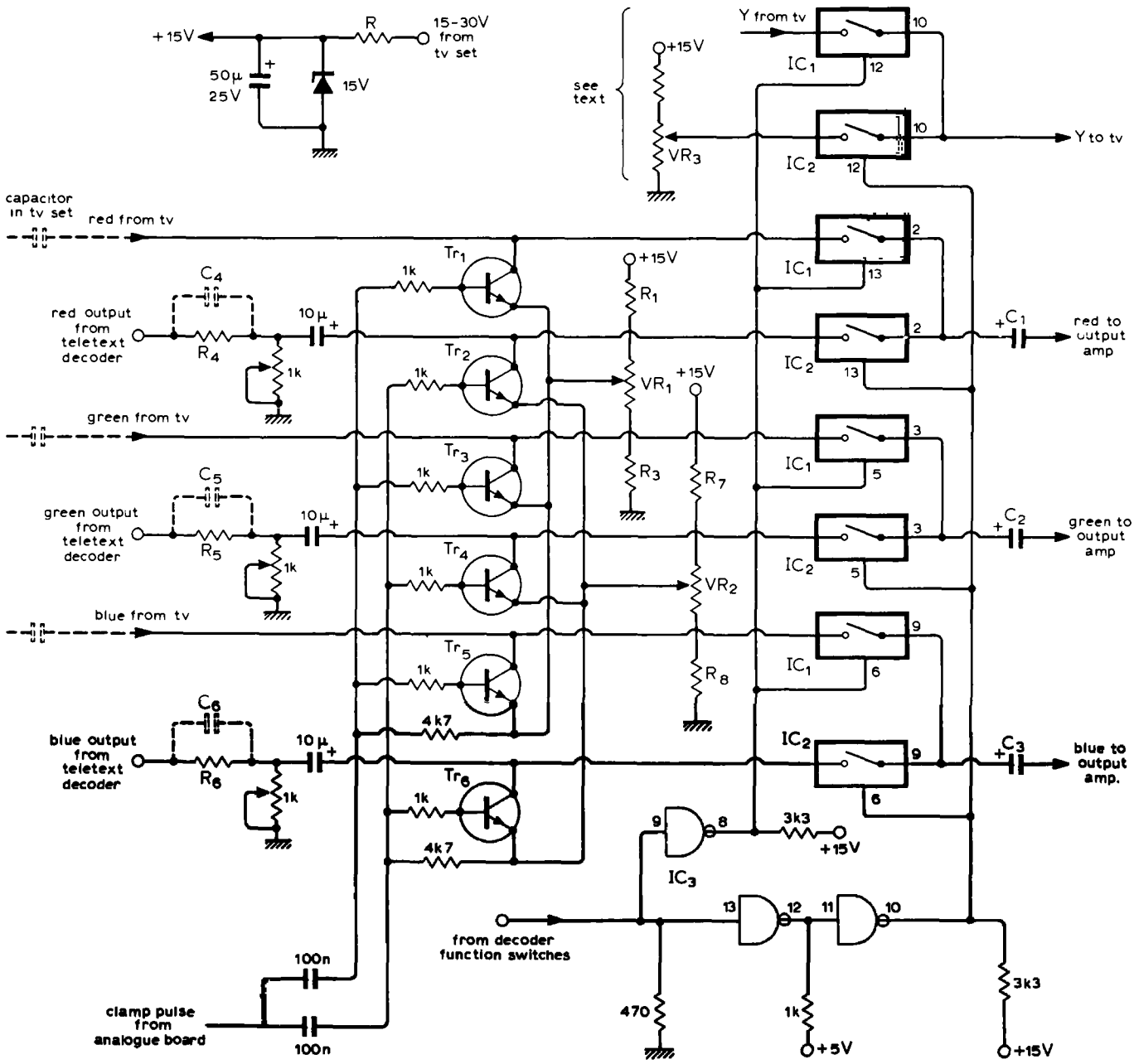
Figure 1 shows a basic video switching circuit, and this will be described initially. Alterations to the basic circuit

will then be considered in conjunction with different TV receiver designs. The actual switching elements are contained in $IC_{1,2}$, and these are c.m.o.s. CD4016 analogue switches, each with its own control input. When the control input is at the 0 level, the input and output terminals are effectively open circuited, and when at a 1 level, the input and output terminals represent a resistance of approximately 300 ohms. The device will pass frequencies up to about 10MHz, which is ideal for our purpose, and as long as a fairly high supply voltage is used, it is quite linear in operation. The slight disadvantage is that, being an m.o.s. device, the switch time is not particularly fast, and this can cause slightly coloured edges on the inserted box. However the advantages of simplicity and cheapness outweigh this slight disadvantage.

The typical switch arrangement shown in Fig. 1 uses two CD4016 i.cs. The control inputs are fed from the outputs of two high-voltage open-collector t.t.l. gates, because correct operation of the switches requires that the control-input voltage must approach the supply voltage. The input from the decoder function switches is normally held at 0 by a 470Ω resistor, ensuring that the switches are left in the TV position if the decoder is not connected to the switch board. Resistors $R_{4,5,6}$ are chosen to reduce the amplitude of the Teletext signals to the same as that of the TV signals, and capacitors $C_{4,5,6}$ may be added to boost the h.f. response if this is found to be necessary. (Because of the high frequency components contained in the verticals of the alphanumeric characters, some commercial receivers may not have a sufficiently good h.f. response to display them adequately. Later in this article a simple modification to the Teletext circuit will be described which reduces the h.f. requirement of the video amplifiers by effectively increasing the width of character verticals.)

The three capacitor-coupled video signals are clamped to the potential which is set by R_1, VR_1 and R_3. Similar, the Teletext signals are clamped to a voltage set by R_7, R_8 and VR_2. In this particular arrangement the actual clamp voltage is arbitrary but would probably be best set to about 3V. Two separate potentiometers are used so that the black level of the Teletext signals can be varied independently of the picture brightness, and thus the background brightness of the inserted box may be adjusted. The reason for not clamping to 0 volts is that the c.m.o.s. switches are not particularly linear when the input signal approaches the extremities of the supply voltage, and raising the potential of the signals ensures linear operation of the switches. After the video switches, capacitors $C_{1,2,3}$ remove the d.c. component of the waveforms before they are fed into the receiver video output amplifiers. (It

Fig. 1 The basic video switching circuit.



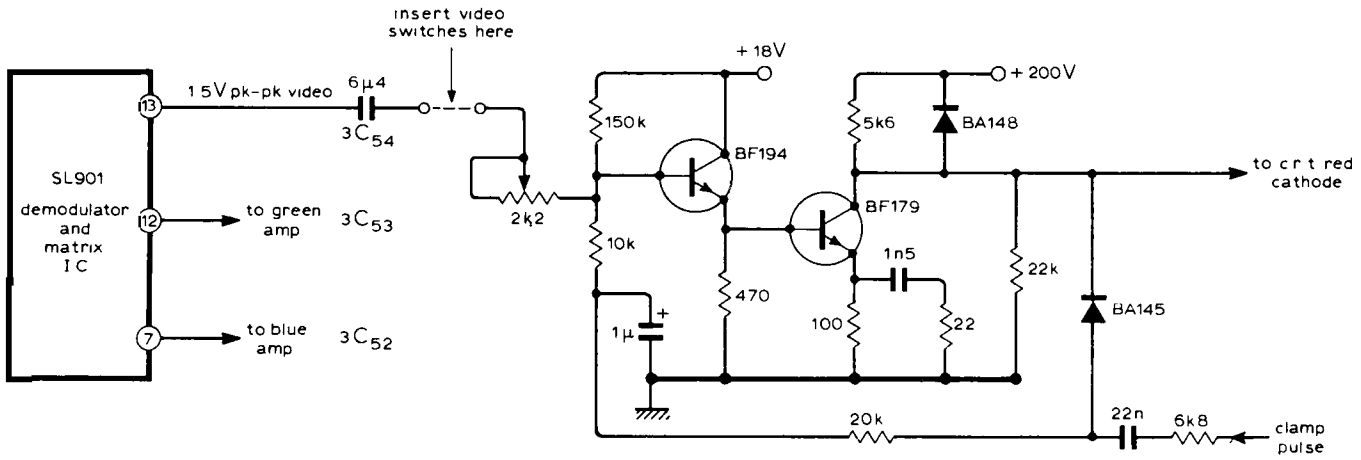


Fig. 2 Video output circuitry of the Bush CTV182S, CTV184S and CTV187CS

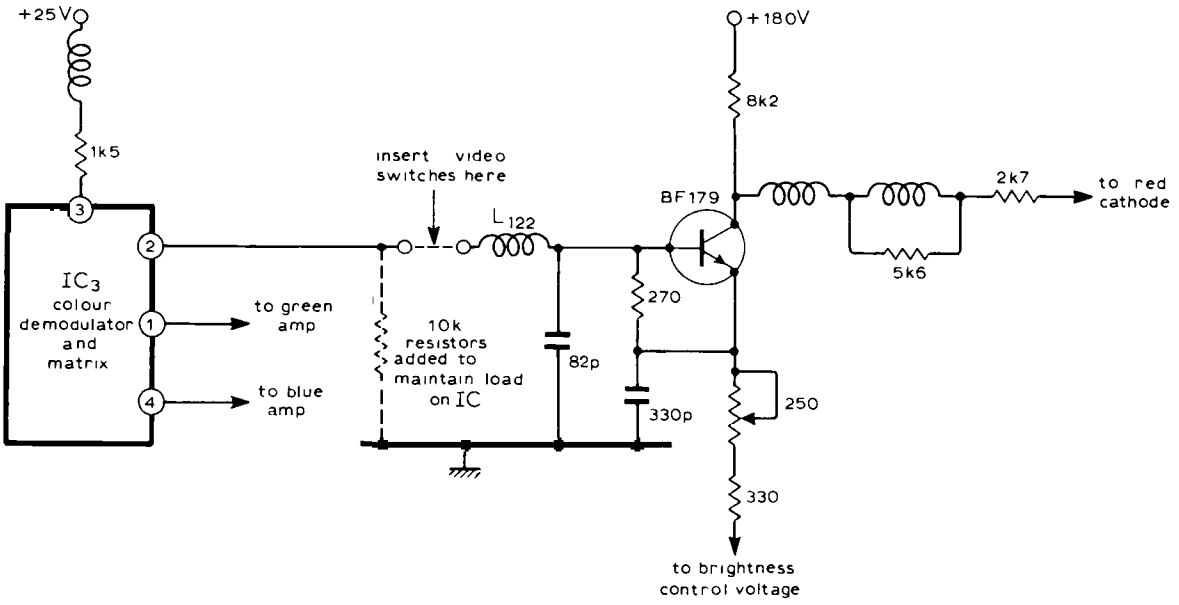
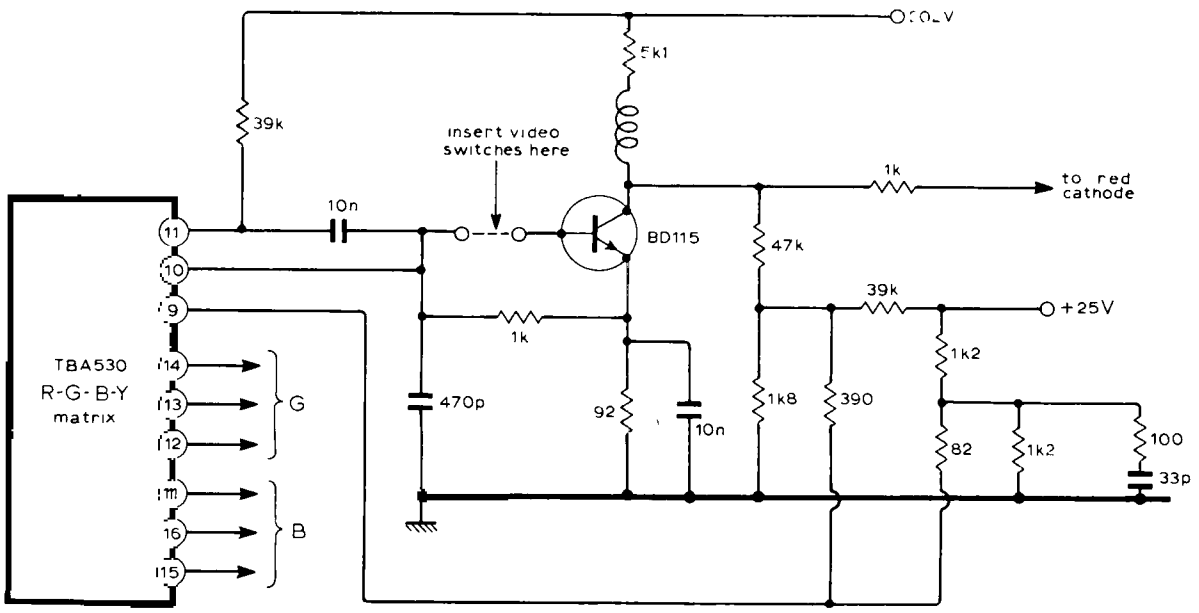


Fig 3 The BRC 8000 shown above, while below is the Philips G8 video output.



should be noted that the polarity of these and the input electrolytics will depend on the individual receiver design and may. not be as shown.) Figure 1 shows a fourth pair of switches which are not required when modifying a receiver of the type described. They are useful, however, when modifying a set which has colour-difference amplifiers (R-Y, G-Y and B-Y), as they can be used to switch off the luminance signal, which would otherwise be present while watching the Teletext display.

Figure 2 shows the circuit of one of three identical output amplifiers used in Bush models CTV182S, 184S, 187S, 192, 194, 196, 197C, 199 and 1026. For sets which have output amplifiers of this type, i.e., capacitor-coupled, positive-going R, G and B video inputs of less than about 5 volts peak to peak, the circuit just described will be adequate. Other receivers using similar amplifiers are: Murphy CV1916S, 1917, 2211S, 2212, 2213, 2610, 2611 and CT2516CS; Alba CS1919; Decca CS1910, 2211, 2213, 2611; ITT/KB CK600, CK500, CK701, CK822, CVC5, Colourscope 20 and Studio 100, and probably quite a few others.

Next will look at some receivers which differ from those just described by virtue of the fact that the output amplifiers are directly-coupled. The amplifiers still carry the R, G and B signals, but instead of being clamped at the tube cathodes, the signals are clamped earlier in the circuit and directly-coupled from this point through to the tube cathodes. Two circuits are shown in Figure 3; the first is a type used in the BRC8000 chassis, which is used by a number of different manufacturers, and the second is a circuit using Mullard i.cs used in the Philips G8 chassis, which is also quite widely used.

Because these sets have directly-coupled amplifiers, the easiest course of action is to remove the capacitor coupling in the original video switch circuit (remove $C_{1,2,3}$) and this means that in the TV mode the only change in operating conditions will be the addition of the effective resistance of the c.m.o.s. switch, about 300Ω, which will almost certainly be negligible. Since the TV signal is effectively clamped at this point in the circuit, we no longer require Tr_1, Tr_3 and Tr_5. The Teletext input circuitry can remain unchanged and VR_2 should be adjusted to make the Teletext signal black level about the same as that of the TV signal at this point. VR_2 effectively forms a Teletext brightness control.

It should be noticed that three 10kΩ resistors are required on the output pins of the matrix i.c. in the BRC8000 circuit. These resistors form the emitter load for the output transistors in the i.c. when Teletext is selected, to prevent the signal voltage at this point rising towards the positive supply rail and upsetting the operation of the c.m.o.s. switches. (The input signals to the c.m.o.s. switches must not be allowed to go outside the limits of the supply voltage to the i.c., as incorrect operation will result, with possible breakthrough on switches which are supposed to be in the off condition.)

Other receivers using the BRC8000 chassis are the Ferguson 3712, Alba 8000 and Marconiphone 4712 to name a few. Similar output stages are also used in Decca models CS2030, 2230, 2630 and 2631.

The three types of output stage just described cover the majority of the more modern British-made sets. However, there are still many older types of receiver giving good service and it was the tendency until fairly recently to drive the grids of the TV tube with colour-difference, valve video output stages. (All the circuits so far described feed the cathodes of the tube with the red, green and blue signals.)

This older type of circuit had three identical valve output stages, each one usually consisting of a triode-pentode valve of the PCL84 type. The pentode section was used to drive the tube grids with either the R-Y, G-Y or B-Y signals, and the triode section was used to clamp this signal at the tube base. The cathodes of the tube were effectively joined (sometimes potentiometers were used to vary the amount of drive to each cathode), and fed with the luminance output signal from a separate pentode valve.

A typical circuit used in the Pye CT70 series chassis is in Fig. 4. All three output stages are identical, and they are fed from three transistors, two of which are used as R-Y and B-Y amplifiers, the third being used to derive a a G-Y signal from the other two. Although it might be possible to drive the basis of these transistors, the three circuits are not identical at this point and trouble might be experienced with the green channel. The best place to feed the signal in is almost certainly at the grid of the pentode valve as shown in the diagram. The only disadvantage of feeding in here is that the Teletext signal must be negative-going at this point to produce the correct display.

There is no reason why the Teletext signals should not simply be inverted, using three ordinary t.t.l. inverters, prior to the attenuating resistors R_4, R_5 and R_6. The six capacitor-coupled signals can then be clamped using Tr_{1-6} as before, but the clamp potentials should be greater than before, at about 6V, as the signals are now negative-going at this point. Capacitors C_1, C_2 and C_3 should be used to couple the switch outputs as before, and these capacitors can be considerably smaller than before as they are feeding valve grids. The Teletext tisplay will now appear on the screen, but it will be superimposed on a black and white TV picture because the luminance signal is still connected to the tube cathodes. Some means must be found of switching off the luminance signal and for this purpose we can use the two remaining c.m.o.s. switches. By connecting them as shown in Figure 1 it is possible to insert the switch in series with the luminance chain at some suitable low-voltage point. VR_3 may be used to adjust the d.c. conditions during switching to keep the black-level correct.

Other sets using this type of output stage are as follows: Bush CTV25 and CTV167; Murphy CV2510 and CV2511; Baird 700 series and 710 series; Decca CTV25; Pye CT79, CT152 and CT153; Dynatron CTV1, CTV1CH and CTV2; Ekco CT102 and CT104; Ferranti CT1166 and 1167; Invicta CT7050; GEC 2040, 2041, 2073, 2100, 2103 and 2107.

Before leaving the subject of modifying TV receivers, the BRC2000-3000 series of receivers, which do not really fall into any of the previous categories, should be examined. Figure 5 shows a video amplifier used in the earlier 2000-series chassis, but the later 3000- and 3500-series used a configuration very similar to this and for our purposes can be considered the same. The three video amplifiers are basically identical, with one important difference. The R-Y and B-Y circuits are both as shown in the diagram, but the input capacitor of the G-Y amplifier is connected to the +30V rail, effectively earthing this point to a.c. and turning the first transistor into a common-base stage. The emitter of this transistor is fed with different amounts of R-Y and B-Y signals to form the G-Y signal.

The best approach to modifying this type of receiver is to treat the three amplifiers as identical capacitor-coupled amplifiers and put the three video switches in the base circuit of the input transistors. Extra capacitors should be used in series with the inputs to the video switches, since the colour-difference signals are close to the 30V rail at this point and outside the range of the 15V supply rail permissible for the c.m.o.s. switches. The luminance chain must also be broken before it feeds the bases of the output transistors and this can most easily be done at the input to the luminance emitter follower (not shown in the diagram). As it stands, this circuit will then produce reasonably acceptable results although, because a certain proportion of the red and blue signal is still being fed into the G-Y amplifier, the green Teletext display appears rather too bright in relation to the red and blue signals. The solution to this problem is to use two extra c.m.o.s. switches, one in the R-Y feed to the G-Y amplifier and the other in the B-Y feed to this amplifier. These switches should be wired so that they are in the open-circuit condition during the Teletext mode of operation. Resistors $R_{4,5,6}$ on the switching board will need to be about 10kΩ for this type of receiver, and $C_{4,5,6}$ about 10–15pF.

The 12–15 volts required for the c.m.o.s. switches can easily be obtained from the video amplifier power rail in

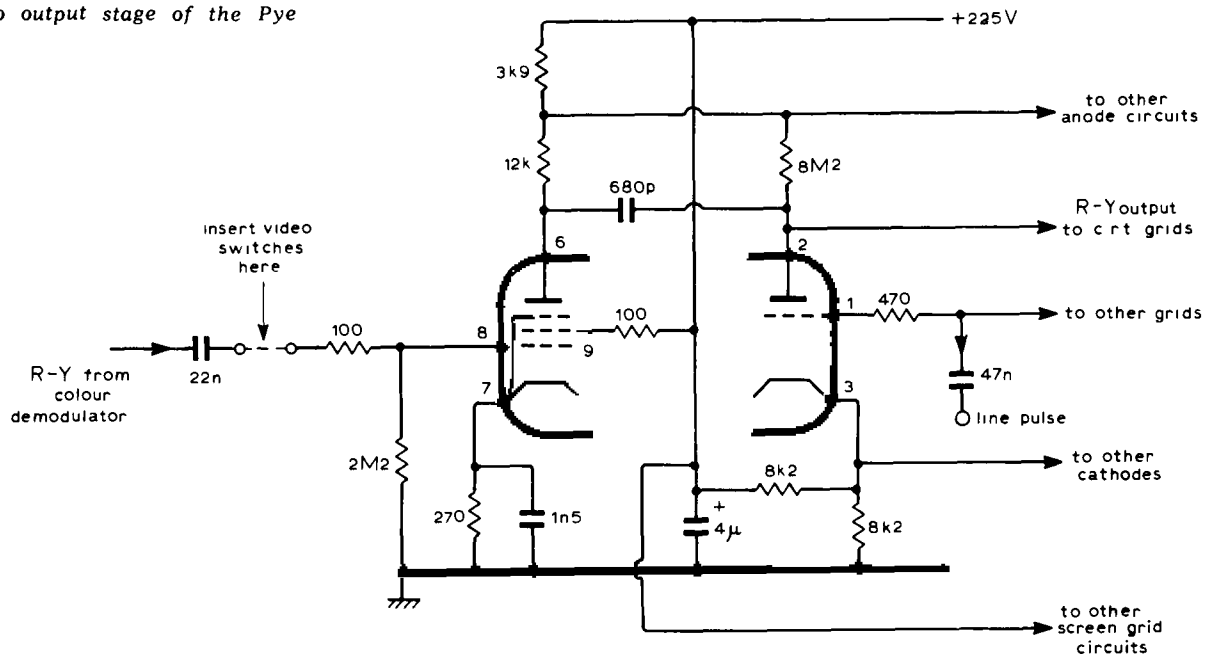


Fig. 4 Video output stage of the Pye CT70/71.

the TV set, using a simple zener diode stabiliser if the rail is higher than 15V. Most sets have a supply of between 12V and 30V and the current drawn by the switching circuit is minimal.

This concludes the description of colour-receiver output stage modifications, but there remains the problem of obtaining a suitable video signal from the set to feed into the Teletext decoder.

There should be no serious problems here, but since the signal that is fed into the decoder will determine whether or not it operates correctly, it is rather important to get this bit right. The signal into the decoder should be a positive-going video signal of between about 1V and 5V peak to peak, not limited in frequency by chrominance, or other filters. The signal should preferably be taken from a low-impedance point in the circuit, to reduce any losses in the coaxial cable feeding the signal to the decoder. A large number of modern receivers employ i.c. synchronous demodulators of the MC1330 type; these are ideal, providing around 2V of positive-going video output signal. Some older sets such as the BRC 3000 series employ separate luminance and chrominance detectors and in this type of receiver the luminance detector output should be used. This is not normally restricted in bandwith sufficiently to upset the operation of the decoder. If a suitable positive-going video signal does not exist, then a small transistor invertor may be needed.

To round off the series of articles, the final part will include a description of setting-up the decoder and a suggestion for reducing the effects of restricted bandwidth in the television receiver. We also hope, at a later date, to publish a modification to allow a new, combined upper- and lower-case character generator to be used. In addition, we will try to include information on modification to the circuit to enable it to be used with the Post Office Viewdata service.

Lack of space will prevent the publication of printed-circuit board layout and component disposition, but we have them at this office and will send copies to anyone who cares to write and ask for them. Please send a large, stamped and addressed envelope.

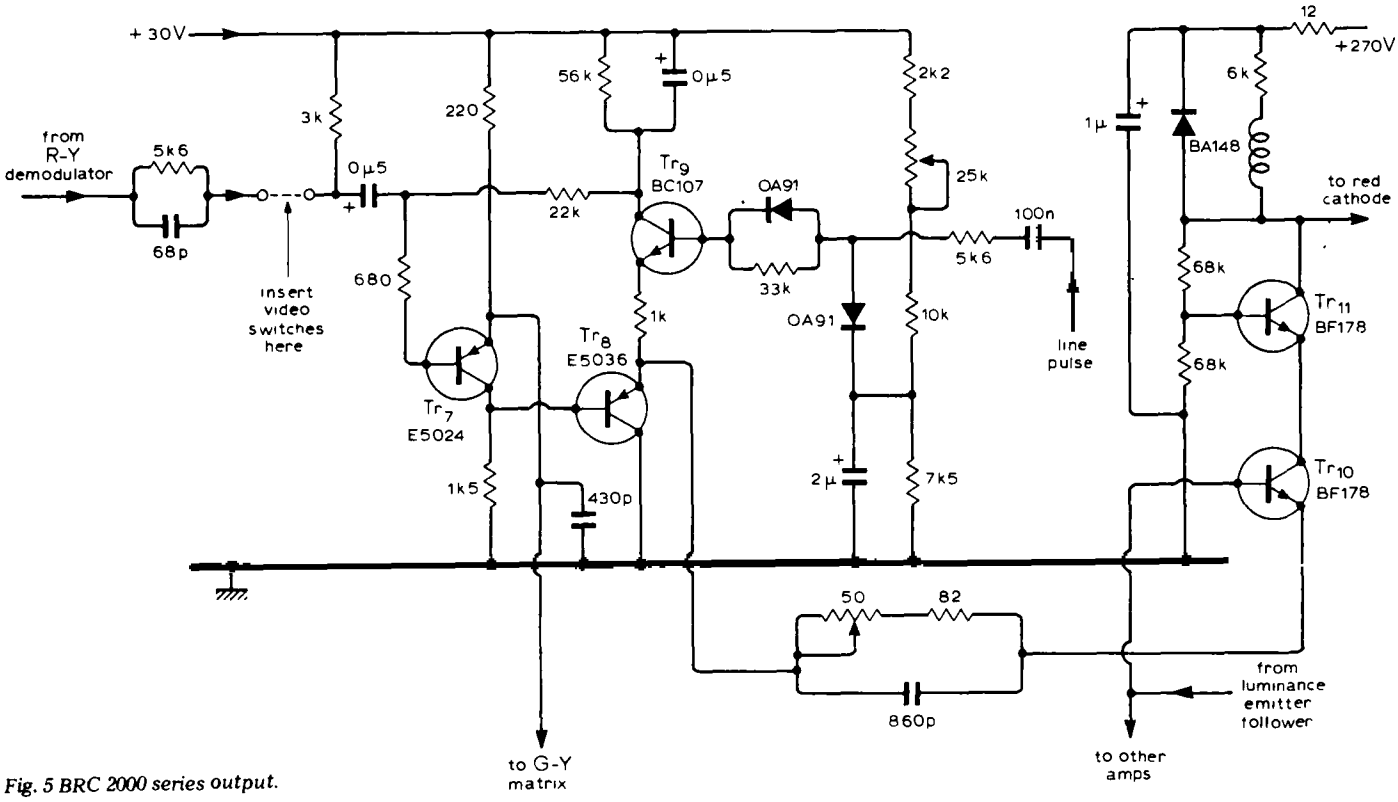


Fig. 5 BRC 2000 series output.

Wireless World Teletext decoder

8 — Modifications and lining up

by J. F. Daniels

Most constructors will probably want to use the decoder with a colour television receiver, but for those who use a black-and-white set, a few words on interfacing are needed.

Monochrome receivers

If a black-and-white receiver is to be modified then there are two options open to the constructor. The decoder may be wired in, in a similar manner to that described for the colour receiver, or a separate tuner and i.f. strip may be used, the output of the decoder being fed via a u.h.f. modulator into the receiver's aerial socket. This second method has the advantage that the decoder may be electrically isolated from the TV set. Whichever system is used, the best display will be obtained by mixing the red, green and blue outputs of the decoder together by means of variable resistors, the resistances of which may be varied to give the desired grey levels for different transmitted colours. Mixed syncs must also be added at this point to lock the scan circuits in the TV set. The problem most likely to be encountered with black and white sets, especially the older ones, is lack of bandwidth in the i.f. strip – a good reason for using the extra i.f. and modulator approach.

Character verticals

The following modification to the decoder circuitry has been found advantageous because it reduces the h.f. response requirements of the receiver video amplifier output stages. Fig. 1 shows the circuit, which uses existing "spare" i.c. gates. The extra gates are wired in series with the output of gate (57, 6). Gates (75, 8) and (75, 3) pass the signal through unchanged, but gate (75, 6) adds to the original signal a pulse derived from the trailing edge of the display character components. VR_3 can be adjusted to give the best character appearance, and the setting of this control will depend on the frequency response of the receiver video amplifiers. At zero resistance setting, the signal passes through this stage unchanged, but as the resistance is increased the width of the character verticals gradually increases until the appearance of the characters is obviously distorted. A suitable control setting should be found which gives the best character appearance.

Upper and lower-case characters

Texas Instruments have recently announced a new character generator i.c., the X887, which has been developed as part of their Tifax decoder module, and as the i.c. was specifically designed for Teletext decoders, it has a number of advantages over the 2513.

Firstly, it contains a complete set of upper and lower-case characters, which includes all those characters defined in the latest Teletext code table. Secondly it has provision for a four-bit row-select input code which means that all ten rows of the characters may be addressed independently, and no shifting of address codes is required for characters with "tails". Thirdly, it only requires a +5V supply, which means that the decoder power supply may be simplified as the −12V rail is now unnecessary.

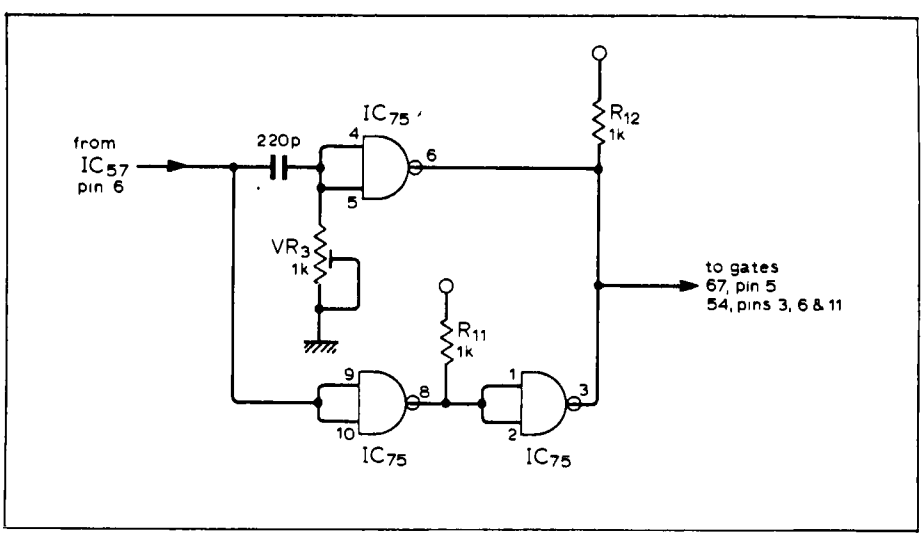
Fig. 1. This modification reduces the degrading effect of poor video frequency / amplitude response in the television receiver. The effect is to broaden vertical components of characters.

The circuit arrangement using the new i.c. is shown in Fig. 2 and is almost identical to the original circuit using the upper-case 2513. The differences are that all seven bits are now fed to the character-select inputs and the four-bit row-select inputs are fed from the Q_A, Q_B, Q_C and Q_D outputs of IC_5 directly. The Y_1-Y_5 outputs feed, as before, into the five open-collector gates, although the timing of the strobe pulses from IC_{42} has been changed slightly to allow for the faster access time of the X887.

The cost of the X887 is around £20, which makes it rather expensive compared with the 2513, but if a decoder with the lower-case facility is required, then the X887 is the obvious choice.

Line-up procedure

The following line-up procedure has been devised after lining up six decoders, but it does assume that the decoder has no faults and is being fed with a suitable video signal as described earlier. It would also be advisable to check that data is actually being transmitted on the selected TV channel, since the system is still in its experimental period and transmissions may be interrupted occasionally. To check the transmissions are present, reduce the height of the TV picture, or offset the vertical-hold control and look for lines of constantly-changing white dots and



dashes across the full width of the TV line in the field blanking interval.

The line-up procedure requires no test gear, but the power supply rails should be checked with a multimeter prior to following these instructions.

Set the six preset potentiometers (three on the analogue board, two on digital board 1 and one on digital board 2) to mid-position. A screen full of random characters will probably be obtained, because the flip-flops in the r.a.m.s take up random states at switch-on. Do not, however, push the clear-page button at this stage.

Adjust VR_3 on the analogue board (set sync separator) to give a display that is free from vertical jitter. Turning the potentiometer too far in one direction will cause the display to jitter vertically and move down the screen. Turning it too far the other way will make the display disappear altogether.

Adjust VR_1 on the upper digital board (horizontal shift), and VR_1 on the analogue board (display width) to give a correctly-centred and suitably proportioned display.

Connect a link between pins 13 and 14 of IC_9. This disables the "framing-code allow" monostable, and this is essential during the first part of the setting up procedure.

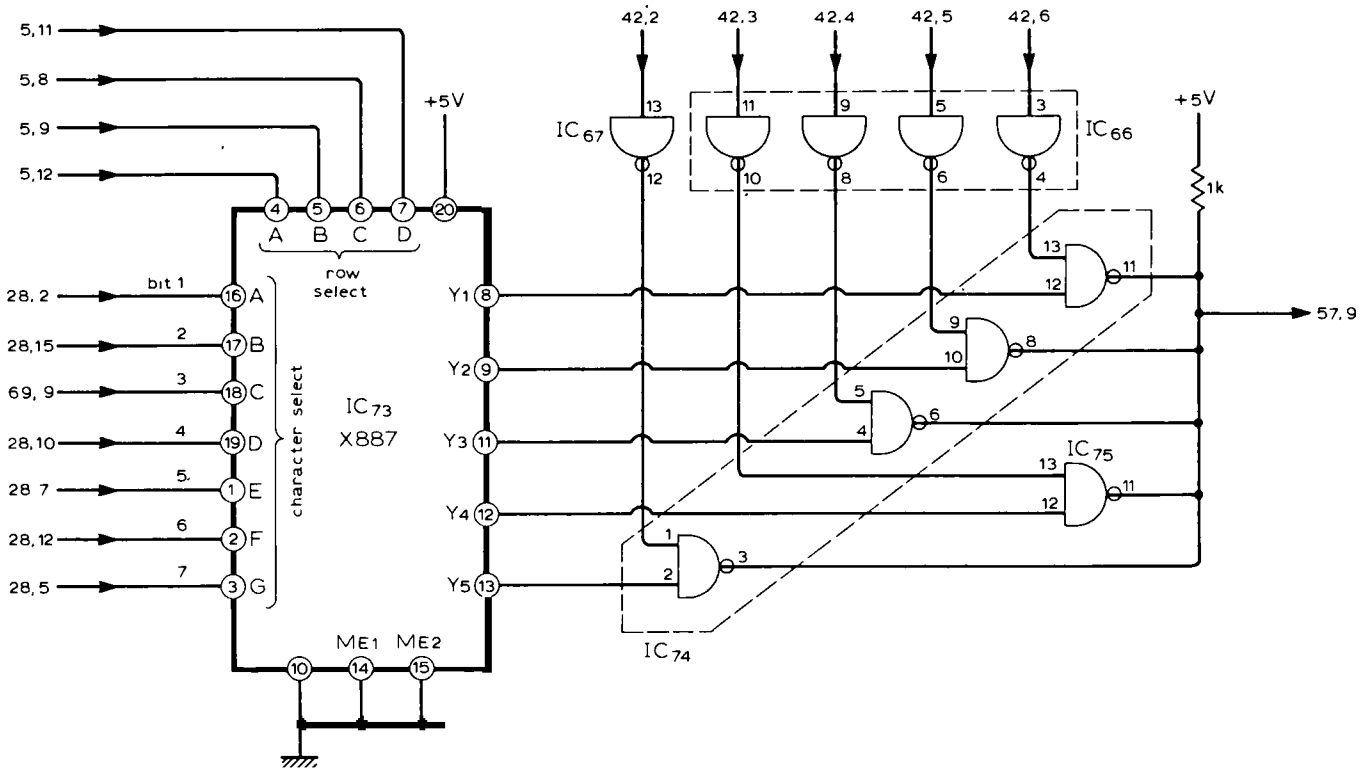
Switch the decoder to the "roll" mode and adjust L_1 to give the maximum amount of "movement" of the display. The characters should start changing at random and this may appear to be happening on consecutive rows from top to bottom of the screen, giving a "rolling-through" appearance. If so, adjust the coil for the most consistent rolling-through action. If the coil former being used is not the specified one, then the oscillation frequency can be checked as follows: – disconnect the uppermost wire link to the analogue board, (lines 11-21) and adjust L_1 to give a display of approximately the correct width. (Disconnecting this link inhibits the display oscillator and makes the data oscillator operate the whole time, so the characters will appear rather ragged). If this is outside the range of adjustment of L_1, adjust the value of C_2 until the width of the display is approximately correct. Reconnect the link to the analogue board.

Adjust VR_2 on the analogue board (slice level) to improve the rolling through action and some correct pages may now be observed changing very rapidly. Continue adjusting L_1 and VR_2 alternately to give the best rolling action. (N.b., when the roll mode is selected the decoder reads out each data row as it is transmitted, and this enables the effect of each adjustment to be observed, instantaneously, rather than having to wait for up to 15 seconds, which would be the case if pages were selected in the normal way.

Remove the link from IC_9, pins 13 and 14. The rolling-through action will probably cease. Adjust VR_2 on digital board 1 carefully, until the rolling-through action begins again. This control has an "on-off" action, unlike those previously adjusted, and is necessarily quite critical in its setting. The adjustment should be checked on different TV channels, since there may be slight differences in the position of the framing code between different channels.

Switch off the roll mode and select a clock-cracker page (at the time of writing page 899 on Oracle or page 140 on Ceefax). This page is used to accurately check the frequency of the data oscillator, and consists of 14 consecutive 1s followed by two 0s repeatedly across each row of the page. This means that the data oscillator gets the least possible amount of locking information on each line and so must free run at the correct frequency for almost two bytes of data. If L_1 is not quite correctly adjusted, a regular pattern will appear on the left-hand side of the screen which will gradually disappear or turn to "rubbish" on the right-hand side. L_1 should be adjusted a quarter of a turn at a time, until the page readout produces a pattern which is even over the whole screen. The two photographs in Fig. 3 show a correct and incorrect clock-cracker readout. These photographs were taken from the output of a decoder which had a lower-case character generator installed, and the characters displayed when an upper-case-only decoder is used are

Fig. 2. The revised character generator, which uses the Texas X887 to display both upper and lower-case characters, as well as the complete Teletext symbol set.



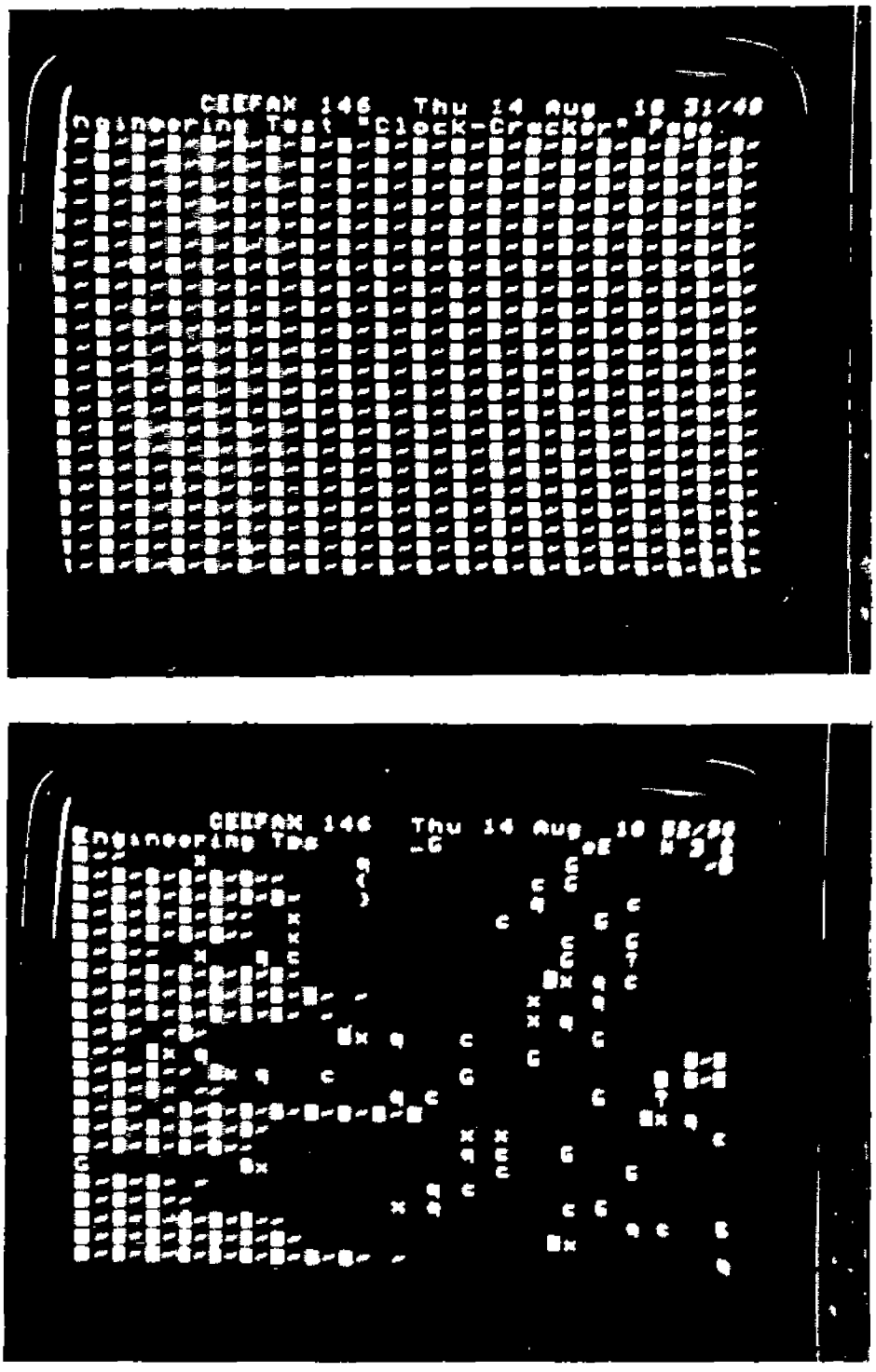


Fig. 3. The "clock-cracker" page, with L_1 (April issue, p.66) correctly adjusted is shown at (a), while the result of incorrect tuning is seen in (b).

different to those shown. The principle of adjustment is, of course, the same.

Finally adjust the slice level control (VR_2 on the analogue board) to give the most error-free page readouts, selecting pages' in the normal manner If the contrast control on the TV set alters the amplitude of the signal being fed to the decoder, check that both the sync separater and the data slicer work satisfactorily over the required range of the control.

Check that the decoder function switches operate correctly and adjust VR_3 on the lower digital board to give the most pleasing character appearance.

Fault finding

Experience with a number of decoders has shown that faults are almost invariably caused by i c pins being left unsoldered, especially on the top side of the p c. boards, or missed connected-through holes, so it is best to check the boards very carefully before attempting the line-up procedure

Faulty or suspect t t l gates can be checked fairly easily by means of d.c. tests (remember that t.t l. outputs can be shorted to the 0V rail for "in-circuit" testing of following gates, but must not be connected directly to the +5V rail.) If an oscilloscope is not available, suspect counters can only really be checked by substitution Faulty r a ms can easily be detected by spotting an abnormally large number of spelling mistakes on each page and by consulting the code table, the bit which is common to all the incorrect letters can usually be located

Installation

A few final hints on wiring the decoder into a domestic receiver may be of some use. Coaxial cable must be used for the video input feed to the decoder, and this should be kept as short as is practical. The other feeds to the decoder will be +5V, −5V, −12V and 0V From the decoder to the receiver there will be red, green and blue output signals, the video switch control wire, and the clamp pulse feed. These last nine feeds may be combined in a single multicore type of screened cable. Screening is necessary to prevent pick-up of the high frequency display components of the output waveforms in the receiver sound or video stages.

Finally it must be stressed again that great care must be taken when connecting the decoder into the TV receiver, to ensure that every possible safety precaution is taken. The decoder box must be effectively earthed, not connected to the TV chassis, and there must be no exposed connections that are at anything other than earth potential. An isolating transformer (which allows the receiver chassis to be earthed) must be used while lining up the decoder, but if the above precautions are observed, this will not be necessary once the decoder is installed in its box.

Acknowledgments

I would like to thank Mullard Ltd for their help with character generator i.cs and also my colleagues, Dave Beavan Norman Riggs and Arnie Tidder for their helpful suggestions and help with building the prototype decoders