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Colin Hinson

In the village of Blunham, Bedfordshire.

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SECTION I

GENERAL DESCRIPTION

1-1 SCOPE OF MANUAL.

This manual describes preventive and corrective maintenance procedures for the Silent 700® KSR/ASR Electronic Data Terminals manufactured by the Digital Systems Division of Texas Instruments Incorporated. Information is presented herein for maintaining and servicing the following Silent 700 models: 732 KSR, 732 ASR, 733 KSR, and 733 ASR.

The maintenance information in this manual is intended to help service personnel solve minor maintenance problems in the field and assist analysis of major troubles at regional TI service centers. A general description of each model and module of the 732/733 KSR/ASR Electronic Data Terminal series is included in this manual along with necessary interfacing information. A general theory of operation for each terminal function (the PC cards perform more than one function) and troubleshooting guide are also included herein. A complete parts list and related mechanical and electrical drawings are included in the appendixes.

1-2 EQUIPMENT DESCRIPTION.

Each Data Terminal is a self-contained local-controlled and/or remote-controlled electronic data terminal designed for use in a wide variety of telecommunications systems. Silent electronic printing is achieved using a dot matrix on a monolithic, solid-state printhead which prints characters across the page. The matrix is composed of separate solid-state heating elements, each electronically controlled. A voltage is applied to the proper character element, transferring thermal energy to the heat-sensitive paper, thus creating a visible image.

The Silent 700 KSR/ASR Electronic Data Terminals can be configured to meet a variety of applications. This versatility is accomplished using modular design which permits performance variation by adding the ASR Module Assembly (top unit) and by inserting an appropriate printed circuit (PC) card and keyboard into the basic terminal subassembly. The basic terminal models available are the 732 KSR, 733 KSR, 732 ASR, and 733 ASR.

1-2.1 MODEL 732 KSR. The model 732 KSR (see Figure 1-2.1) is a Baudot-coded keyboard send/receive data

terminal, similar in function to conventional tape punch data terminals. The TI 732 KSR is capable of transmitting, receiving, and printing the Baudot code and character set at switch-selectable speeds of 50, 75, or 100 baud via a standard EIA line interface.

The following options are available with the model 732 KSR:

- a. Answer-back memory
- b. Teletype (TTY) interface.

1-2.2 MODEL 733 KSR. The model 733 KSR (see Figure 1-2.2) is an ASCII-coded, keyboard send/receive data terminal, similar in function to conventional tape punch data terminals. The TI 733 KSR is capable of transmitting, receiving, and printing the ASCII code and character set at switch-selectable speeds of 10, 15, or 30 characters per second (CPS) via a standard EIA line interface.

The following options are available with the model 733 KSR:

- a. Answer-back memory
- b. Auto answer control
- c. TTY line interface series
- d. Automatic device control (line-disconnect function)
- e. Modem line interface
- f. Full (upper and lowercase) ASCII keyboard.
- g. Acoustic coupler.

1-2.3 MODEL 733 ASR. The model 733 ASR (see Figure 1-2.3) is an ASCII-coded automatic send/receive data terminal, similar in function to conventional tape punch data terminals. The TI 733 ASR is capable of transmitting, receiving, printing, playing back (from tape), and recording on tape the ASCII code and character set at switch-selectable speeds of 10, 15, or 30 characters per

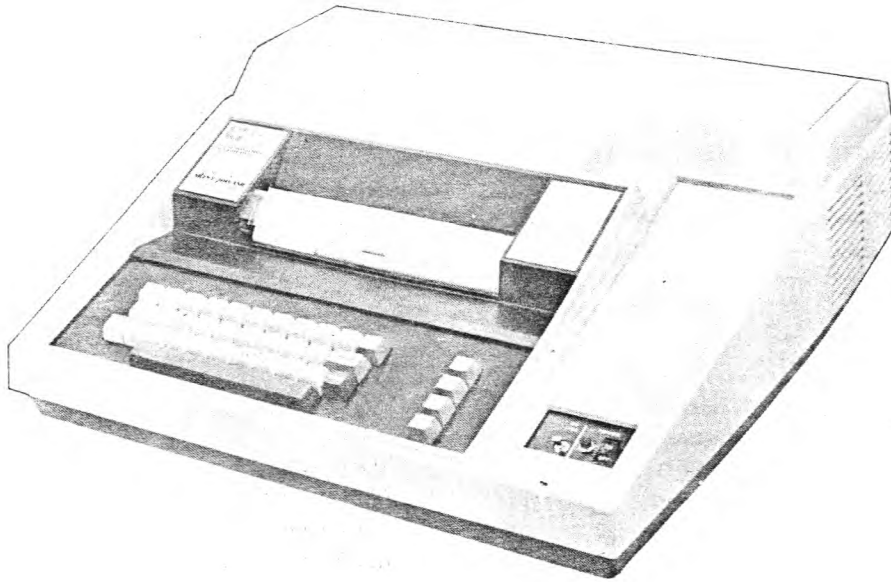


FIGURE 1-2.1. MODEL 732 KSR (BAUDOT CODE)

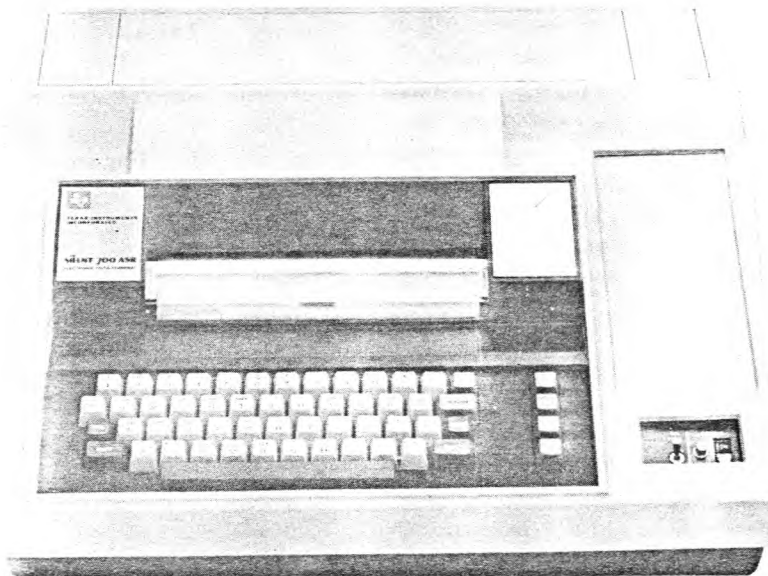


FIGURE 1-2.2. MODEL 733 KSR (ASCII CODE)

second (CPS) via a standard EIA line interface. Functions such as tape edit or high speed tape duplication are also possible in the off-line (local) mode.

The following options are available with the model 733 ASR:

- a. Answer-back ~~memory~~
- b. Auto answer control
- c. TTY line interface series
- d. Modem line interface
- e. Full ASCII keyboard
- f. Automatic search control
- g. Automatic device control
- h. Remote device control
- i. Single - cassette ASR.
- j. 1200 Baud
- k. Footpedal for the tape playback
- l. Acoustic coupler.

1-2.4 MODEL 732 ASR. The Model 732 ASR (see Figure 1-2.4) is a Baudot-coded, automatic send/receive data terminal, similar in function to conventional tape punch data terminals. The 732 ASR is capable of transmitting, receiving, printing, playing back from tape and recording on tape the Baudot code and character set at switch-selectable speeds of 50, 75, or 100 baud via a standard EIA line interface. Functions such as tape edit or high-speed tape duplication are also possible in the off-line (local) mode.

The following options are available with the model 732 ASR:

- a. Answer-back memory
- b. TTY line interface series
- c. Single-cassette ASR.

1-2.5 MODEL 732 RECEIVE ONLY (RO). The Model 732 RO Data Terminal is a Baudot-code, receive-only data terminal. The 732 RO is capable of receiving and printing the Baudot code and character set at switch-selectable data rates of 50, 75, and 100 baud via a standard EIA line interface. The Model 732 is functionally, physically, and operationally equivalent to the Model 732 KSR, except the RO Data Terminal has no keyboard, no ON/OFF LINE switch, and the paper advance switch is located adjacent to the ON/OFF LINE switch.

The following options are available for the 732 RO:

- a. Answer-back memory
- b. TTY line interface series.

1-2.6 MODEL 733 RECEIVE ONLY (RO). The Model 733 RO is an ASCII-coded receive-only data terminal. The TI 733 RO is capable of receiving and printing the ASCII code and character set at switch-selectable data rates of 10, 15, and 30 characters per second (CPS) via a standard EIA line interface. The Model 733 is functionally, physically, and operationally equivalent to the Model 733 KSR, except the RO has no keyboard, no ON/OFF LINE switch, and the paper advance switch is located adjacent to the ON/OFF LINE switch.

The following options are available for the Model 733 RO:

- a. Answer-back memory
- b. Modem line interface (answer-mode only)
- c. Automatic answer control
- d. Automatic device control (line-disconnect function)
- e. TTY line interface series.
- f. Acoustic Coupler.

1-3 OPTIONAL EQUIPMENT.

1-3.1 ANSWER-BACK MEMORY. The Answer-Back Memory provides up to 21 field-programmable, nonvolatile characters. The Answer-Back Memory is activated by the USASCII ENQ character or by depressing the HERE IS key on the keyboard. Printing or recording of the memory contents is a switch-selectable option.

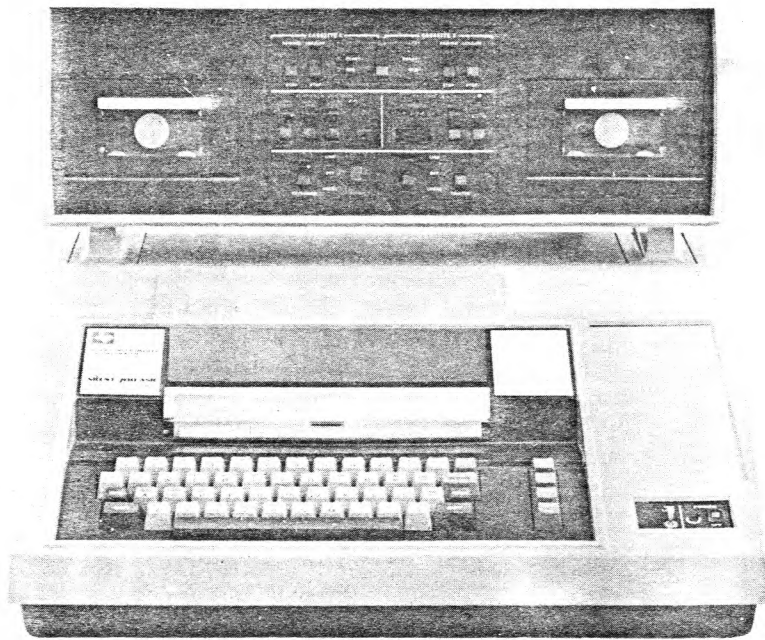


FIGURE 1-2.3. MODEL 733 ASR (ASCII CODE)

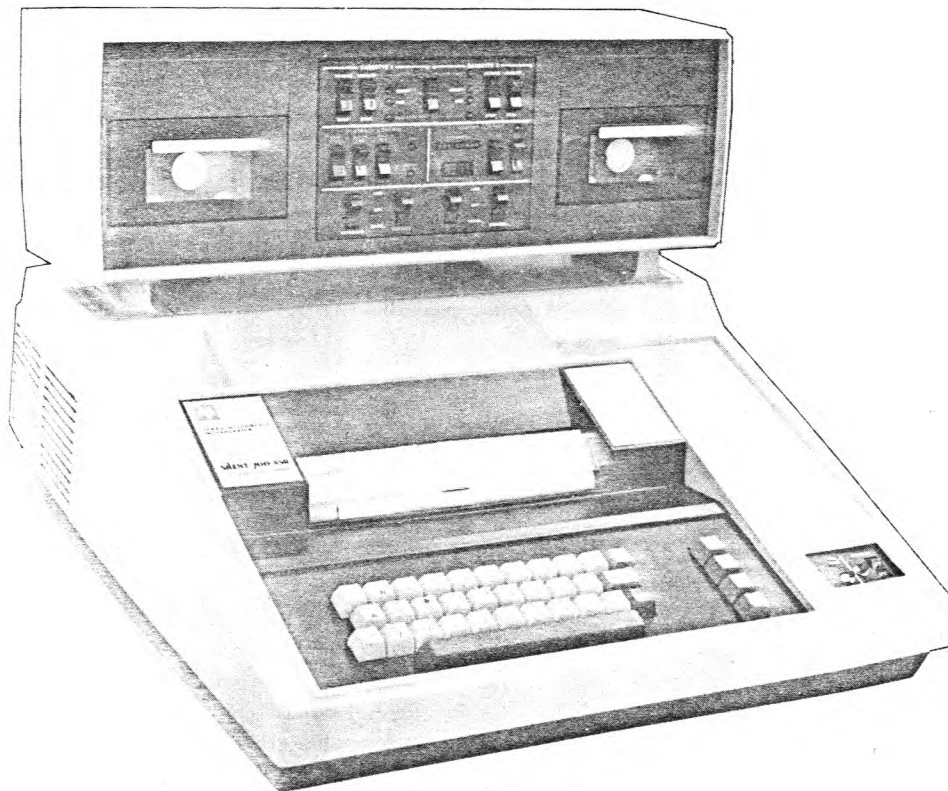


FIGURE 1-2.4. MODEL 732 ASR (BAUDOT CODE)

1-3.2 TTY LINE INTERFACE. The TTY Line Interface replaces the standard EIA interface.

1-3.2.1 Neutral Interface. TTY neutral interface signaling is accomplished by opening and closing the circuit presented to the terminal I/O connector. Nominal operating current is field-settable to either 60 mA or 20 mA.

1-3.2.2 Polar Interface. TTY polar interface signaling is accomplished by alternately opening one circuit and closing the other circuit presented to the terminal I/O connector. A positive current in the external circuit represents a MARK and a negative current represents a SPACE.

1-3.2.3 Computer Line Interface. Designed for computer use, with this interface signaling is accomplished by opening and closing the circuit presented to the I/O connector. Nominal operating current is 13 mA.

1-3.3 MODEM LINE INTERFACE (ORIGINATE OR ANSWER MODE). The Modem Line Interface, which replaces the standard EIA Interface, is a low-speed modem conforming to the requirements of the Bell Data Access Arrangement central data terminal. It operates asynchronously up to a maximum speed of 300 baud in full or half-duplex over a two-wire voice-grade line. Signaling is accomplished by frequency shift keying (FSK).

1-3.4 FULL ASCII KEYBOARD. The Full ASCII Keyboard provides transmission of both uppercase and lower case characters from the keyboard.

1-3.5 AUTOMATIC DEVICE CONTROL. When the Automatic Device Control characters DC1, DC2, DC3 or DC4 are received from the line or generated by the terminal, the record and playback cassette units are switched on or off as shown below:

DC1 (X-ON)	Playback ON
DC2 (TAPE)	Record ON
DC3 (X-OFF)	Playback OFF
DC4 (TAPE)	Record OFF

Activation by these characters in either transmit, receive, or local modes is a selectable option. In the case of the playback cassette reading DC3, one character after DC3 will be played back before the playback cassette is switched off.

1-3.6 SINGLE-CASSETTE ASR. The ASR terminal is optionally available without cassette-2 and associated controls. Cassette-1 retains its controls, indicators, and capabilities. Terminal capabilities requiring simultaneous operation of two cassettes are not available with the single-cassette system.

1-3.7 AUTOMATIC SEARCH CONTROL. The optional Automatic Search Control (ASC) provides the ASR with capability to search a recorded tape cassette at high speed for a predetermined record. The operator or remote device (if used in conjunction with the optional Remote Device Control) enters an activate code through the ASR keyboard. In the case of a remote device, the activate code is transmitted on the line. The ASC answers (local mode only) with a line feed and a carriage return, after which the operator or remote device enters into the ASC memory from one to 16 printable USASCII characters which the ASC uses to identify the searched-for record. The operator then activates the appropriate tape cassette PLAYBACK CONTROL switch to initiate the search, or the remote device issues the appropriate code. The ASC searches the tape cassette at speeds up to 324 characters per second (3.7 blocks per second). Upon locating the desired data blocks, the ASC stops the tape and causes a paper advance (local mode only). The operator or remote device then may initiate a local or remote printout or recording of the desired data.

The Automatic Search Control consists of the ASC printed-circuit card (card slot A7), a motherboard-access PC card (card slot A6), and a top access connector which connects the two PC cards. When used with the optional Automatic Device Control (TI Part No. 971481) or the optional Remote Device Control, the motherboard-access card is not needed.

The ASC receives most operating signals from the motherboard-access PC card or the Automatic Device Control or the Remote Device Control, depending on which one of the three PC cards are installed.

1-3.8 REMOTE DEVICE CONTROL (ASR MODEL ONLY). The Remote Device Control option allows a remote device to change the functional operating modes of the 733 ASR Data Terminal via data received from the communication line. The following functions may be controlled through this option:

1. Playback ON
2. Playback OFF
3. Record ON
4. Record OFF
5. Automatic disconnect from the phone line when used in conjunction with the Auto Answer Control option (EOT)

6. Rewind cassette 1
7. Rewind cassette 2
8. Load/FF cassette 1
9. Load/FF cassette 2
10. Cassette 1 in record mode (cassette 2 in playback mode if dual cassette model)
11. Cassette 1 in playback mode (cassette 2 in record mode if dual cassette model)
12. Block forward
13. Block reverse
14. Printer ON
15. Printer OFF
16. Automatic Device Control ON (items 1 - 4 above) on received data
17. Automatic Device Control OFF (items 1 - 4 above) on received data
18. Request status information
19. Automatic Search Control cancel (when used in conjunction with the ASC option)
20. 1200-baud print local (when used in conjunction with the planned 1200 baud auto answer options).
21. Footpedal option operation of the playback-on function.

In addition, when status information is requested, the status of the cassettes, record, playback, and printer is transmitted by the terminal via a single ASCII character.

These functions provide the following typical applications:

1. Data collection from an unattended terminal
2. Data distribution to an unattended terminal
3. Remote record search when used in conjunction with the Automatic Search Control option

4. Data distribution to any unattended terminal at 1200-baud line speed when used in conjunction with the 1200 baud auto answer option.

1-3.9 1200-BAUD INTERFACE. The 1200-Baud Interface option allows the 733 ASR to transmit and receive data at rates of 10, 15, 30, and 120 characters per second (110, 150, 300, and 1200 baud, respectively). The data set interface section of the 1200-Baud option generates and accepts the necessary signals to operate with Bell System Models 202C and 202D (or equivalent) data sets.

1-3.10 DUAL FORMAT. The Dual Format option enables the Model 733 ASR to transmit and receive either 7 bits of data (standard ASCII configuration) or 8 bits of data (binary configuration).

The Dual Format option consists of four PC cards which provide an additional strappable option to enable the ETX control character to initiate the recording of a block of data (only when operating in the standard ASCII configuration and the TAPE FORMAT switch is in the CONT position).

1-3.11 AUTO ANSWER CONTROL (300 BAUD). The Auto Answer Control option (TI Part No. 960984) provides a 300-baud Model 733 Data Terminal the capability to automatically answer a call through the Bell System's direct distance dialing (DDD) network. Two versions of the Auto Answer Control option are available: one interfaces with a Bell CBS data access arrangement (DAA) or equivalent; the other version interfaces with a Bell 103A data set or equivalent with auto answer control.

TI recommends using the Auto Answer Control option in conjunction with both the Answer-Back Memory and the Remote Device Control options or with the Auto Device Control option.

The Auto Answer Control consists of a 6-foot EIA or modem cable assembly, a PC card, and a display panel.

1-3.12 ASR FOOTPEDAL.

NOTE

The data terminal must be equipped with the optional Remote Device Control (RDC) to enable use of the Footpedal.

Available for the Model 733 ASR Data Terminal is an optional Footpedal (TI Part No. 973866) to permit convenient remote triggering of ASR cassette tape

playback. The Footpedal is particularly useful to control playback of format tapes. The ASR Footpedal option consists of:

1. A footswitch pedal with an integral debounce circuit mounted on a PC card
2. A 7-foot heavy-duty shielded cable
3. A connector to mate the footpedal to the J2 connector at the rear of the 733 ASR Data Terminal.

1-3.13 ACOUSTIC COUPLER. The optional Acoustic Coupler (TI Part No. 969619) is available for the Models 733 ASR, KSR, and Receive-Only Data Terminals. The Acoustic Coupler equips the data terminal to communicate over voice-grade telephone networks at data rates up to 300 baud in full or half duplex mode. The Acoustic Coupler operates over any standard Western Electric 500-series type telephone (or equivalent). The Acoustic Coupler is typically used to gain direct access to a computer timeshare system. In operation, the telephone handset is placed in the Acoustic Coupler muffs and the appropriate connecting number is dialed on the telephone.

The Acoustic Coupler option consists of

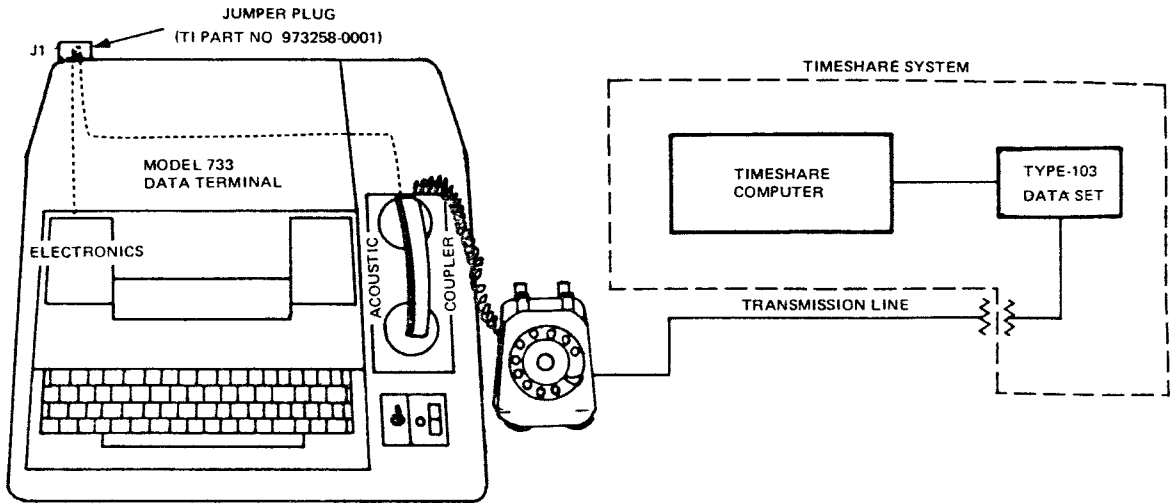
1. A telephone handset receiver panel with muffs and interconnecting wiring

2. The electronic interface, mounted on a single PC card which plugs into the PC card rack.
3. A connector jumper which plugs into the communication interface connector (J1) at the rear of the data terminal. Figure 1-3.1a is a block diagram of a typical Acoustic Coupler application.
4. An optional "Y" connector enables use of the data terminal with both the Acoustic Coupler and a variety of other data sources, as shown in Figure 1-3.1b.

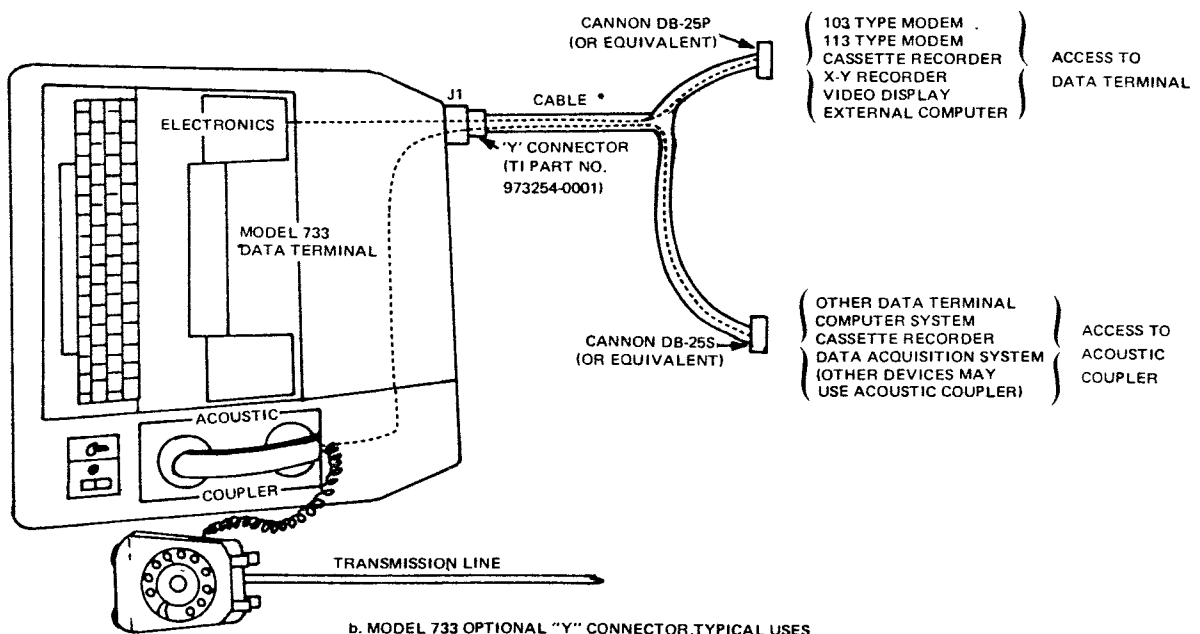
1.3.14 CALCULATOR NUMERIC CLUSTER KEYBOARD. The calculator numeric cluster keyboard provides a calculator numeric cluster in addition to the standard numeric form.

1-4 ACCESSORIES.

1-4.1 STAND. A terminal stand is available which securely supports the terminal. The lower row of key tops are 29 inches from the floor. The stand provides at least 24 inches of leg room from the bottom of the stand to the floor and at least 14 inches of leg room from the front edge of the terminal stand to the back of the stand. The stand weighs approximately 45 pounds.



a STANDARD (THROUGH) JUMPER CONNECTOR FOR ACOUSTIC COUPLER OPERATION



b. MODEL 733 OPTIONAL "Y" CONNECTOR, TYPICAL USES

A 0000154

FIGURE 1-3.1. MODEL 733 ACOUSTIC COUPLER OPTION CONNECTOR BLOCK DIAGRAM

SECTION II

EQUIPMENT INSTALLATION

2-1 GENERAL.

The Silent 700® Electronic Data Terminals are self contained, requiring no auxiliary equipment for standard data terminal operation.

CAUTION

After unpacking, visually inspect the data terminal before applying power. Check for obvious shipping damage. Open the top cover and remove the PC card rack cover. Check for foreign objects. Ensure that all PC cards (see Figure 2-1.1) are tightly plugged into their sockets and that all connectors are plugged into the motherboard. Ascertain that the keyboard cable is connected. Replace the PC card rack cover (be sure the three tabs at the rear are inserted into their mating slots at the rear of the PC card rack) and close the top cover. Check that all keyboard keys operate freely. Do not operate the printer without paper on the platen (see Paragraph 2-5).

2-2 DIMENSIONS.

The terminal should be located in an area where its air inlets and outlets are unobstructed. Dimensions are shown in Figure 2-2.1.

2-3 POWER CONNECTIONS.

The normal power connection is 115 Vac, 50/60 Hz, three wire. To use optional 230 Vac, 50/60 Hz, power, the terminal must be rewired as follows: (1) remove the card rack cover and power assembly cover (Figure 2-1.1); (2) remove the jumpers between TB1-2 and TB1-3 and between TB1-5 and TB1-6; (3) install a jumper between TB1-3 and TB1-5 (see Figure 2-3.1). The power cord plug must be changed; the new cord must meet UL and CSA standards. Change fuse F1 to a 1.5A, 250V Slo Blo.

2-4 EIA LINE INTERFACE.

The EIA line connection located at the rear of the data terminal is an edge connector (see Figure 2-4.1).

A data set cable (Part No. 959372-0001) connects the data terminal to the external data set. A standard RS232C

compatible 25-pin connector is provided at the end of the 6-foot cable. For pin assignments see Table 2-4.1.

CAUTION

When attaching the cable connector screws to the data terminal, do not tighten the screws excessively: the connector ears may break.

2-5 PAPER LOADING.

CAUTION

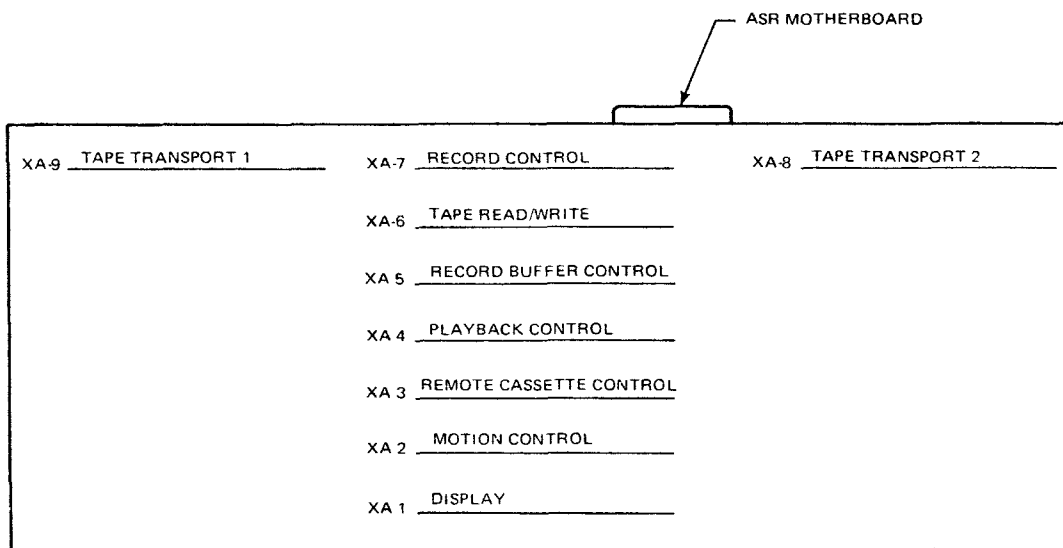
The printer should never be operated without paper on the platen (drive roller); damage to both platen and printhead could result.

The data terminal must be loaded with paper before applying power. Load the paper as follows:

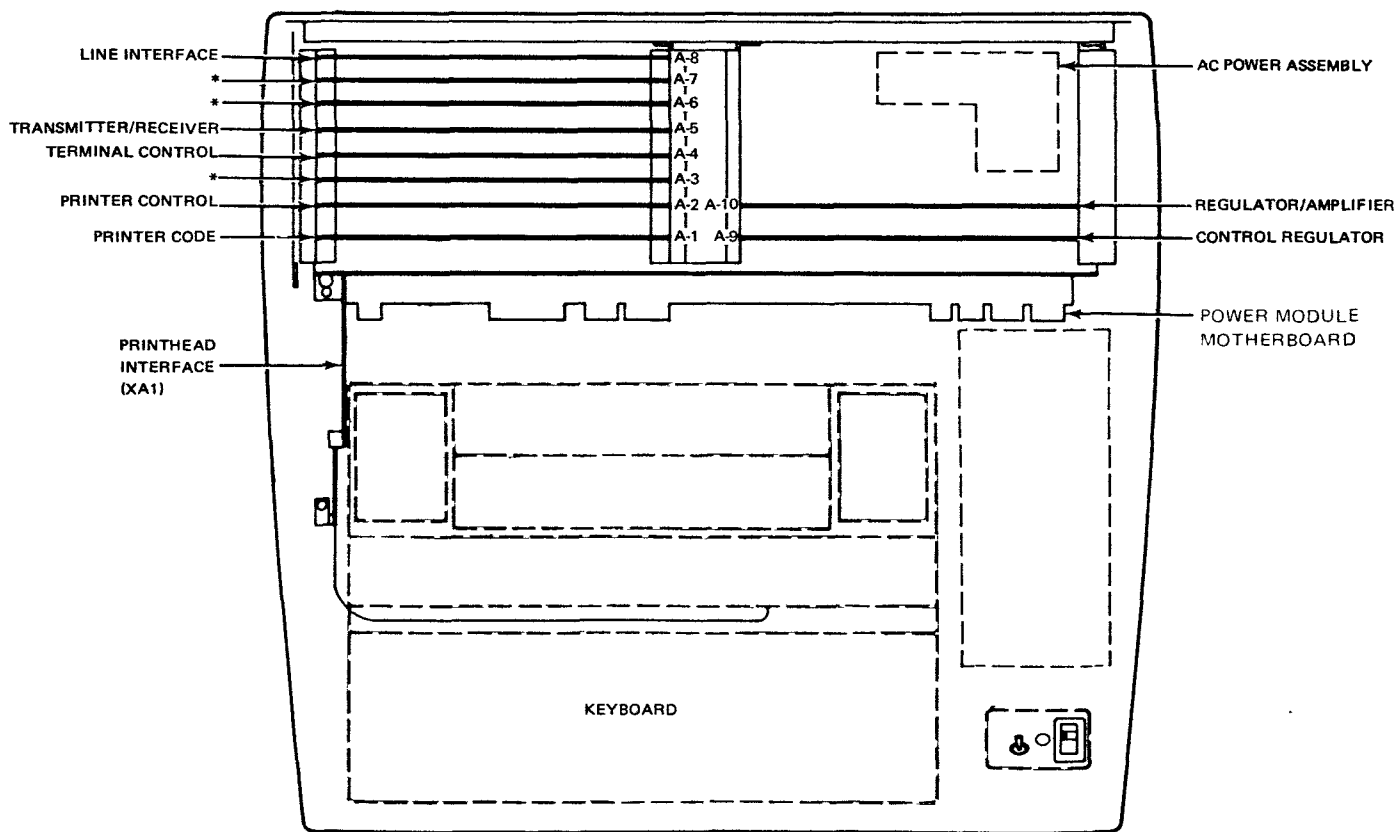
IMPORTANT NOTE

The warranty and/or service contract on the thermal printhead is subject to nullification if the thermal printing paper used in the Silent 700 Data Terminal does not meet TI Specification 213714.

- a. Raise the terminal cover and rotate the window backwards (see Figure 2-5.1).
- b. Place a fresh roll of paper on the supply hubs, ascertaining that the roll can rotate freely.
- c. Thread paper between the paper chute and the drive roller as shown in Figure 2-5.1. Be sure paper is centered in the paper chute.
- d. Lower the window.
- e. Set the POWER switch ON and depress the



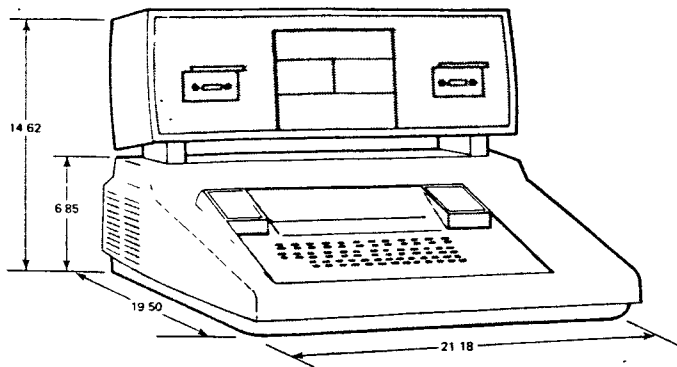
ASR MODULE ASSEMBLY (TOP UNIT) PC CARD LOCATIONS



*RESERVED FOR OPTIONAL DEVICES

KSR (LOWER UNIT) PC CARD LOCATIONS

FIGURE 2-1.1. PC CARD LOCATIONS



(dimensions in inches)

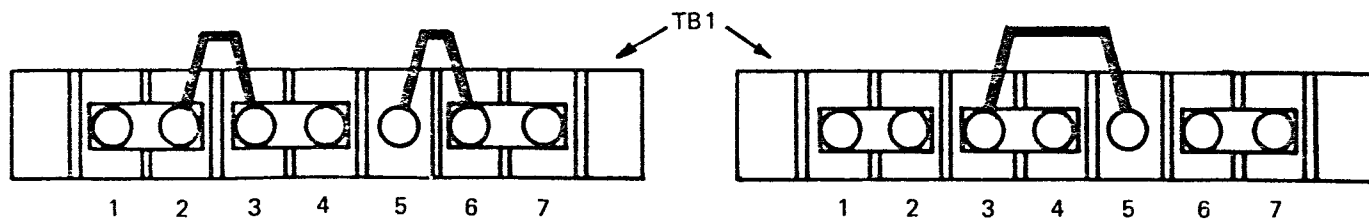
FIGURE 2-2.1. OVERALL DIMENSIONS (ASR/KSR)

PAPER ADV key. Make sure paper is feeding smooth and straight.

- f. Close the data terminal cover, ascertaining that paper is fed through the slot in the cover.

2-6 STRAPPABLE OPTIONS.

2-6.1 END-OF-LINE ALARM. The end-of-line alarm can be prevented from sounding automatically by removing R20 (10 ohms) by hand from connectors J1 and J2 on the Printer Control PC card. If this feature is wanted, hand insert the 10-ohm resistor (R20) between J1 and J2 on the Printer Control card (red tabbed card in slot A2 of the KSR card rack). Removal of R20 will not inhibit the alarm from sounding upon receipt of the ASCII BEL character.:



(a) 115V OPERATION

(b) 230V OPERATION

NOTE: TB1 is located under the Power Assembly Cover (shown in Figure 2-1.1). Fuse F1 (at rear of KSR near power cord exit) must be changed to a Slo-Blo 250V, 1.5A fuse for 230V operation.

FIGURE 2-3.1. 115 Vac AND 230 Vac TERMINAL BOARD JUMPERS

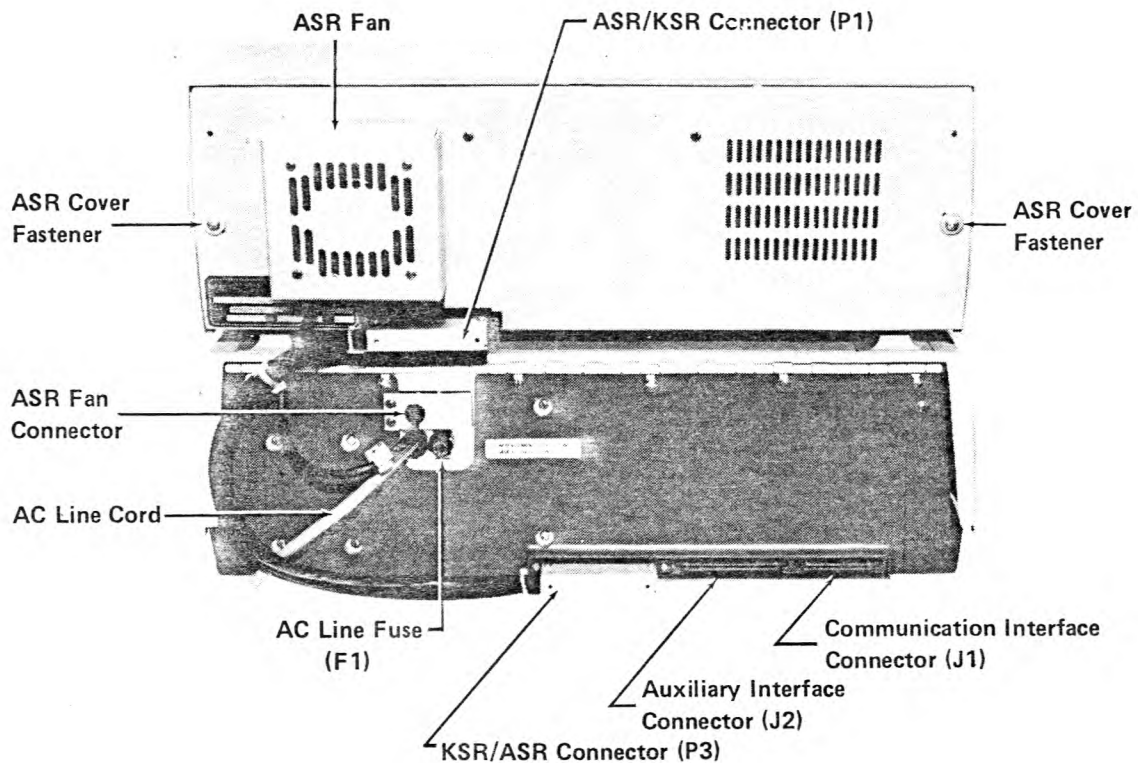


FIGURE 2-4.1. TERMINAL EXTERNAL CONNECTIONS

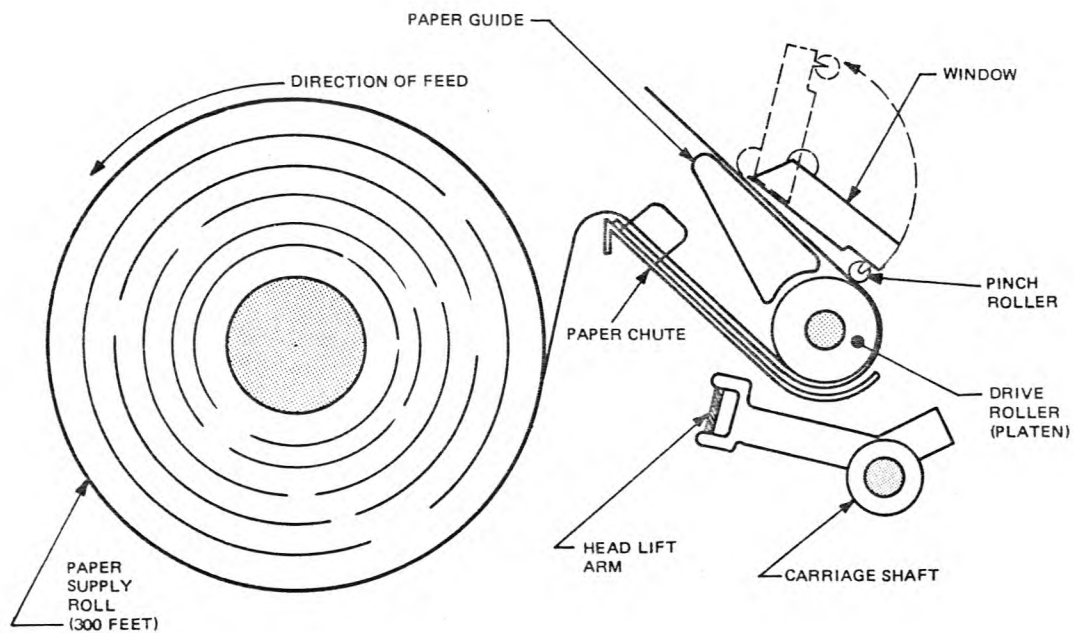


FIGURE 2-5.1. PAPER LOADING

TABLE 2-4.1. EIA INTERFACE CABLE PIN FUNCTIONS⁴
(CABLE 959372-0001)

Connector Pin Numbers		Pin Function
Terminal	Data Set	
6	20 →	Data Terminal Ready ¹
7	7 →	Signal Ground
8	5 ←	Clear to Send ²
9	6 ←	Data Set Ready ³
10	3 ←	Received Data
A	1	Protective Ground
F	4 →	Request to Send ¹
H	2 →	Transmitted Data
K	8 ←	Data Carrier Detect ⁵

NOTES:

- ¹Held to an ON condition by data terminal.
- ²Held to an ON condition by data set during transmission; required by terminal for transmission.
- ³Held to an ON condition when data set is operative; required for terminal operation.
- ⁴All are used only with external modem.
- ⁵Held to an ON condition by modem when carrier is received; required by terminal for data reception.

2-6.2 PLAYBACK STOP ON ERROR. This option is implemented by a strappable resistor or a pencil switch; depending on which version of the Playback Control PC card is installed in slot XA-4 of the ASR upper unit.

2-6.2.1 Standard Playback Control (PC Card 960905)*. Upon detecting a read error when reading from the tape, the Playback Controller will automatically stop if resistor R1 (10 ohms) is connected between J3 and J4 on the Playback Control card (slot 4 in the upper ASR unit). If R1 is connected between J1 and J2 on this same card, the controller will not stop upon detecting a read error; instead, it will transmit the erroneous block to the terminal and continue reading tape (if in continuous playback mode). This resistor is easily pulled out of J3/J4 and inserted in J1/J2, or vice versa, by hand (no tools necessary).

2-6.2.2 Optional Dual-Format Playback Control. The stop-on-error option on the Dual-Format Playback Control (PC Card 969453*) is enabled by setting switch S1-4 to ON. In this position the controller will automatically stop tape playback upon detecting a read error. With switch S1-4 in the OFF position, the erroneous block of data will be transmitted to the line.

The stop-on-error option on the Dual-Format Playback Control (PC Card 981319) is enabled by installing R4 (10 ohms) between J1 and J2.

2-6.3 BAUDOT CHARACTER SET. Code and character set may be selected on the Printer Code PC card (slot 1 in KSR unit) by installing Z23, R46, R47, R48, R49, and R53 according to Table 2-6.1

2-6.4 ETX RECORD INITIATE [733 MODELS WITH DUAL-FORMAT RECORD BUFFER CONTROL (PC CARD 962285) ONLY]. If recording in the CONTinuous tape format, upon receiving the ASCII end-of-text (ETX) control character, the recording of a block of data will be initiated. This permits the ETX control character to perform the function of a carriage return. To enable this strappable option, remove R8 (10 ohms) from between J3 and J4 on the Dual-Format Record Buffer PC card (slot XA-5, ASR upper unit). Reinstall R8 as R13 between J1 and J2.

NOTE

The ETX option cannot be used with binary option. (R9 must not be installed.)

2-7 OPTIONS.

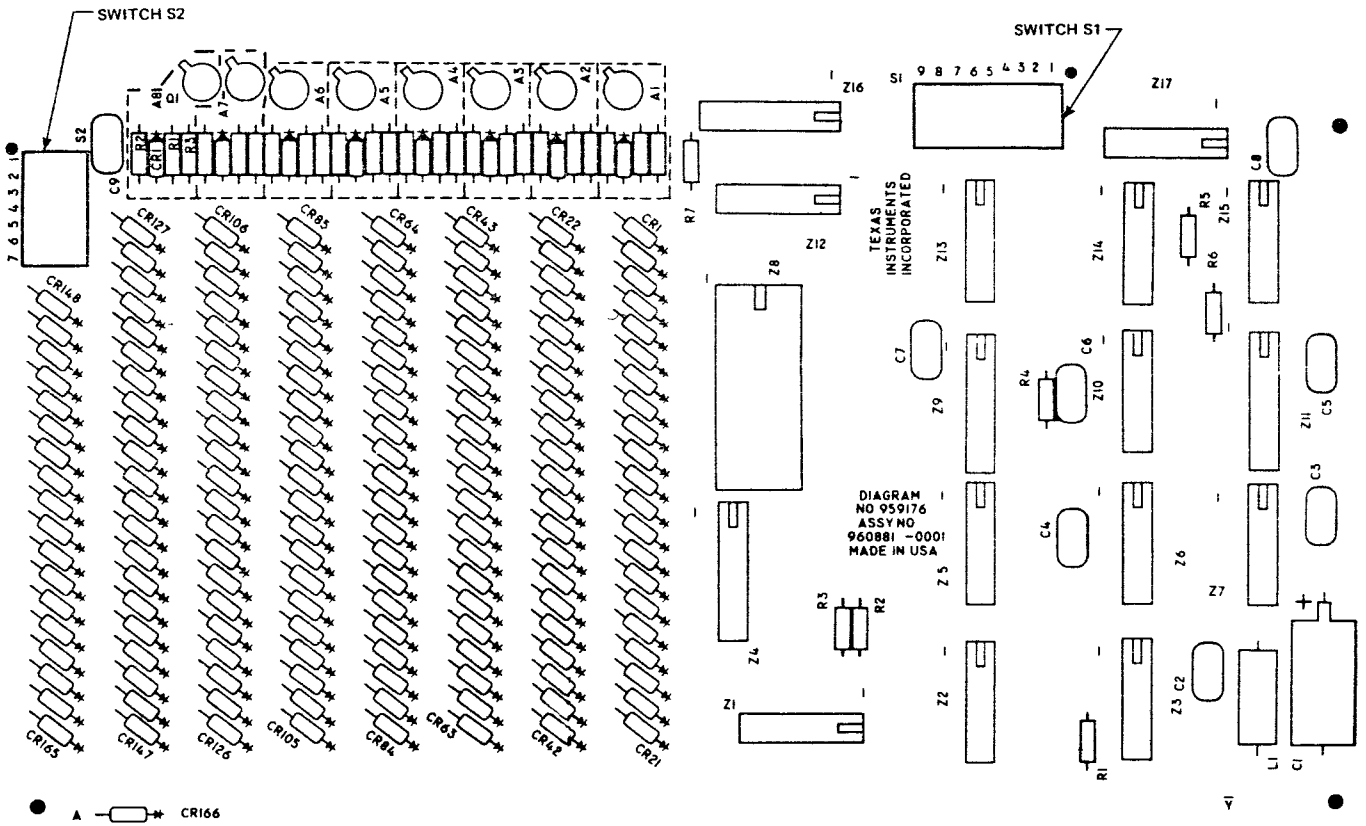
2-7.1 ANSWER-BACK MEMORY. To gain this option, install the Answer-Back Memory PC card (Part No. 960881-0001) in card slot A3. To program the Answer-Back Memory, use the following procedure:

- a. For each character to be transmitted, remove the corresponding diode from rows CR148 through CR165 of the Answer-Back Memory PC card shown in Figure 2-7.1. These diodes are located on the left-hand side of the board.
- b. To encode each character, remove diodes to transmit a ZERO (space), or leave in diodes to transmit a ONE (mark) in each bit position. The first bits for each character are located in the rightmost column of diodes: bit 2 is the

*This PC card is obsolete.

next column left, etc. The first character is encoded in the first row of diodes; hence, CR64 corresponds to bit 4 of character 1.

Several switchable options are incorporated into the Answer-Back Memory PC card. Table 2-7.1 defines each



NOTES:

1. SEE APPENDIX B FOR PARTS LIST AND ASSEMBLY DRAWING.
2. SEE APPENDIX C FOR SCHEMATIC.
3. SEE TABLE 2-7.1 FOR SWITCH OPTIONS

FIGURE 2-7.1. ANSWER-BACK MEMORY PC CARD COMPONENT LOCATIONS.

TABLE 2-6.1 PC CARD CONNECTIONS FOR CODE AND CHARACTER SET

PRINTER CODE CARD ASSY. NO.	CODE AND CHARACTER SET	Z23	R46	R47	R48	R49	R53
959137-0001	ASCII	TI Part No. 959328-0001	10Ω	OPEN	10Ω	OPEN	OPEN
959137-0002	Baudot. U. S. Figures	TI Part No. 959329-0001	OPEN	10Ω	OPEN	10Ω	OPEN
	Baudot. U. K. Figures (Optional)	TI Part No. 959329-0001	OPEN	10Ω	OPEN	OPEN	10Ω

switch on the card and its function. A switch is closed when the 'dot' on the switch rocker arm is in the down position.

2-7.2 AUTO DEVICE CONTROL. The Auto Device Control option accommodates device control characters DC1, DC2, DC3, and DC4. When these characters are received from the line or generated by the terminal, the Record and Playback cassette transports are turned on and off according to the following:

DC1 (X-ON)	Playback ON
DC2 (TAPE)	Record ON
DC3 (X-OFF)	Playback OFF
DC4 (TAPE)	Record OFF

When the playback transport reads DC3 during playback, one character after DC3 will be read and transmitted before the playback transport is turned off. Strappable options allow any of these four code functions to be inhibited during transmit, receive, or local operations.

To use this option, install the Auto Device Controller PC card (TI Part No. 971481-0001) in card slot A6 (Figure 2-1.1) in the KSR unit. Strappable options permit the 733 ASR to respond to DC1, DC2, DC3, and DC4, as shown in Table 2-7.2.

2-7.3 MODEM LINE INTERFACE. To incorporate this option, install the Modem Line Interface PC card (TI Part No. 960887 000X) in Line Interface card slot A8 (Figure 2-1.1). The data terminal may now be connected to the Bell System Data Access Arrangement (DAA) with the phone line cable assembly (TI Part No. 959383-0001). Pin

assignments are listed in Table 2-7.3. After connecting to the Bell System DAA line, adjust the modem level (potentiometer R18) as specified by the Bell System, using a meter which can measure modem output in dBm. Measure directly between the two modem output lines.

2-7.4 CURRENT LOOP LINE INTERFACE (NEUTRAL, POLAR AND COMPUTER). To add this option install the Teletype (TTY) Interface PC card (TI Part No. 959171-000X) in line interface card slot A8. The data terminal may now be connected to the communication line using a cable assembly (TI Part No. 959384-0001). For specific connections see Figures 2-7.1 and 2-7.2. For 60 mA operation, add R34 (150 ohm, 0.5 watt, 5 percent) to the TTY Interface PC card. Pin assignments are listed in Table 2-7.4. The computer interface is connected as a neutral interface.

2-7.5 UPPERCASE/LOWERCASE KEYBOARD. If the uppercase/lowercase keyboard capability is desired, the standard keyboard may be replaced with an Uppercase/Lowercase Keyboard (TI Part No. 959326-0001). To convert, remove the four mounting screws holding the keyboard to the keyboard brackets and disconnect the keyboard cable. When the new keyboard is installed and the cable is plugged in, be sure to remove the protective foam cover taped to the semiconductor chip on the bottom of the keyboard. Full ASCII and limited ASCII keyboard arrangements are shown in Figures 3-5.5 through 3-5.13, in Section III of this manual.

TABLE 2-7.1 ANSWER-BACK MEMORY PC CARD SWITCH OPTIONS

Switch S2 ¹	Function ³
1	Open to remove CR141 (bit 7 character 15) from matrix
2	Open to remove CR21 (bit 1 character 21) from matrix
3	Open to remove CR121 (bit 6 character 16) from matrix
4	Open to remove CR101 (bit 5 character 17) from matrix
5	Open to remove CR81 (bit 4 character 18) from matrix
6	Open to remove CR61 (bit 3 character 19) from matrix
7	Open to remove CR41 (bit 2 character 20) from matrix
Switch S1	Function ³
1	Close for ASCII card; open for Baudot card
2	Close for ASCII card; open for Baudot card
3	Close for ASCII card; open for Baudot card
4	Open for ASCII card; close for Baudot card
5	Open for ASCII card; close for Baudot card
6	Close to disable printing of ABM contents at all times; open to enable printing of ABM contents when on-line in half-duplex
7	Close to disable recording of ABM contents at all times; open to enable recording of ABM contents when on-line in half-duplex
8	Close to put an ABM ON indication on pin 9 (future option); open for NO indication (spare run on AUX1R0F)
9 ²	Close to ignore stop bit (continuous memory cycling) open to stop ABM at stop bit programmed
1 and 4	Open both at same time to ignore triggering ABM from the line only

NOTES

1. Switch S2, all positions are normally closed; open only during unit test
2. Switch S1-9 is normally open; closed only during unit test
3. Switches are closed when the dot on the switch rocker arm is down

TABLE 2-7.2. (A) AUTOMATIC DEVICE CONTROL ENABLING OPTIONS
(For Part No. 971481)

Control Function	Enabling Switch Section		
	To Enable When Transmitting	To Enable When Receiving	To Enable When in Local
DC1 or DC3 (Playback ON/OFF)	S2-1 (DC3 only)	S2-2	S2-3
DC2 or DC4 (Record ON/OFF)		S2-4	S2-5

NOTE

Control characters DC1 through DC4 function in the selected operating modes shown above. Close the appropriate switch section on S2 to enable the corresponding function. When the ADC ON/OFF switch is in the OFF position, all ADC functions are disabled except the automatic disconnect on receipt of the EOT character (if that option is installed).

TABLE 2-7.2. (B) AUTOMATIC DEVICE CONTROL (EARLIER MODEL) ENABLING OPTIONS
(Part No. 960891)

Control Function	To Enable When Transmitting	To Enable When Receiving	To Enable In Local
DC1 Resistor Between (Playback ON)	R1 J1-J2	R2 J3-J4	R3 J5-J6
DC2 Resistor Between (Record ON)	R7 J13-J14	R8 J15-J16	R9 J17-J18
DC3 Resistor Between (Playback OFF)	R4 J7-J8	R5 J9-J10	R6 J11-J12
DC4 Resistor Between (Record OFF)	R10 J19-J20	R11 J21-J22	R12 J23-J24

All Resistors are 10Ω, .25W, 5%

TABLE 2-7.3 PHONE LINE (MODEM) CABLE PIN FUNCTIONS*
(CABLE 959383-0001)

Terminal Pin No.	Wire Color at Spade Lug	Pin Function
C	Red	Communication line
3	Black	Communication line

*Used only with internal modem.

TABLE 2-7.4 CURRENT LOOP (TTY) INTERFACE CABLE PIN FUNCTIONS
(CABLE 959384-0001)

Terminal Pin No.	Wire Color at Spade Lug	Pin Function
4	White	Teletype positive receiver input loop
D	Green	Teletype receiver input loop
5	Black	Teletype transmitter output loop
E	Red	Teletype transmitter output loop

2-7.6 DUAL FORMAT PC CARDS. Four Dual-Format PC cards are necessary:

1. Dual-Format Transmit/Receive (TI Part No. 973905 or 969455*) slot A-5, KSR lower unit
2. Dual-Format Playback Control (TI Part No. 981319 or 969453*) slot XA-4, ASR upper unit
3. Dual-Format Record Buffer Control (TI Part No. 962285) slot XA-5, ASR upper unit
4. Dual-Format Tape Read/Write Control (TI Part No. 969451) slot XA-6, ASR upper unit)

With the Dual-Format PC cards in the terminal and the terminal TAPE FORMAT switch in the CONT position, the terminal has the strappable capability to handle either binary format data or standard format data with or without ETX. These options and their straps are listed in Table 2-7.5.

*This PC card is obsolete.

NOTE

The standard format *without* ETX option renders the terminal functionally equivalent to a terminal equipped with the standard Record Buffer (TI Part No. 960903), Tape Read/Write Control (962281), Playback Control (960905), and the ASCII Transmit/Receive (959135) PC cards.

The data terminal format options listed in Table 2-7.5 are explained in the following paragraphs.

2-7.6.1 CONTInuous Tape Format Position.

- a. Standard Format Without ETX Decode - Each data character transmitted and received consists of 7 bits with parity in the 8th bit. Each

TABLE 2-7.5. DUAL-FORMAT PC CARDS STRAPPABLE OPTION ENABLES

733 ASR/KSR Terminal Format Options	TO ENABLE THIS OPTION. . .			
	Dual Format ASCII Transmit/Receive (Part No. 969455* OR 973905)	Dual Format Tape Read/Write Control (Part No. 969451)	Dual Format Playback Control (Part No. 969453* OR 981319)	Dual Format Record Buffer (Part No. 962285)
† Standard Format Without ETX	Install R17 Between J3 & J4	Install R1 Between J1 & J2	S1-1 OFF S1-2 ON	Install R5 Between J5 & J6 Install R8 Between J3 & J4 Remove R9 Between J5 & J6 Remove R13 Between J1 & J2
Standard Format With ETX	Install R17 Between J3 & J4	Install R1 Between J1 & J2	S1-1 OFF S1-2 ON	Install R5 Between J5 & J6 Install R13 Between J1 & J2 Remove R9 Between J5 & J6 Remove R8 Between J3 & J4
Binary Format	Install R17 Between J1 & J2	Install R1 Between J3 & J4	S1-1 ON S1-2 OFF	Install R5 Between J3 & J4 Install R8 Between J3 & J4 Install R9 Between J5 & J6 Remove R13 Between J1 & J2

*This PC card is obsolete.

†This option is used in the standard data terminal.

recorded block of data consists of 86 characters. Recording of a block out of the buffer is initiated only when the 86th character is entered (CONT tape format). All characters, including carriage return, have a ZERO in the 8th bit.

- b. Standard Format With ETX Decode - Each data character transmitted and received consists of 7 bits with parity in the 8th bit. The recording of a block is initiated either when the 86th character is entered into the buffer, or when the control character ETX is decoded. All characters, except the control character ETX, have a ZERO in the 8th bit.

- c. Binary Format - Each data character transmitted and received consists of 8 bits. Each block consists of 86 characters. Recording of a block out of the buffer is initiated only when the 86th character is entered in the buffer. The entire 8-bit character field is recorded.

2-7.6.2 LINE Tape Format Position. Each data character transmitted and received consists of 7 bits with parity in the 8th bit. Each block of data in the buffer is recorded on tape either when the 86th character is entered, or when the carriage return character is decoded. All characters except the carriage return character have a ZERO in the 8th bit.

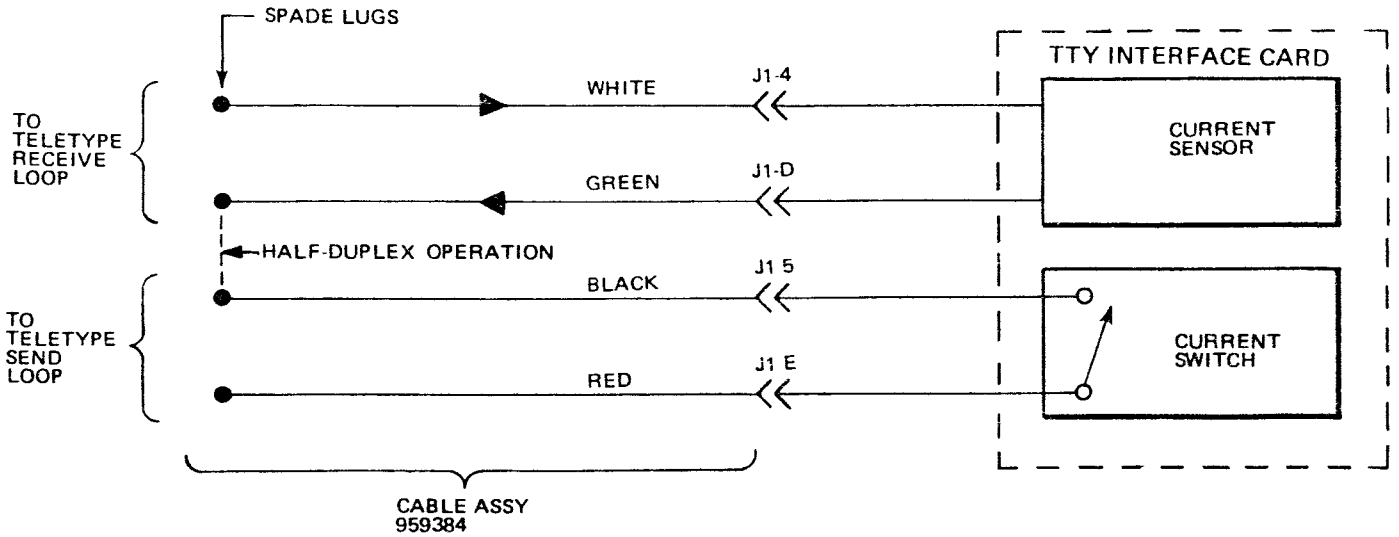


FIGURE 2-7.2. TELETYPEWRITER NEUTRAL INTERFACE WIRING DIAGRAM

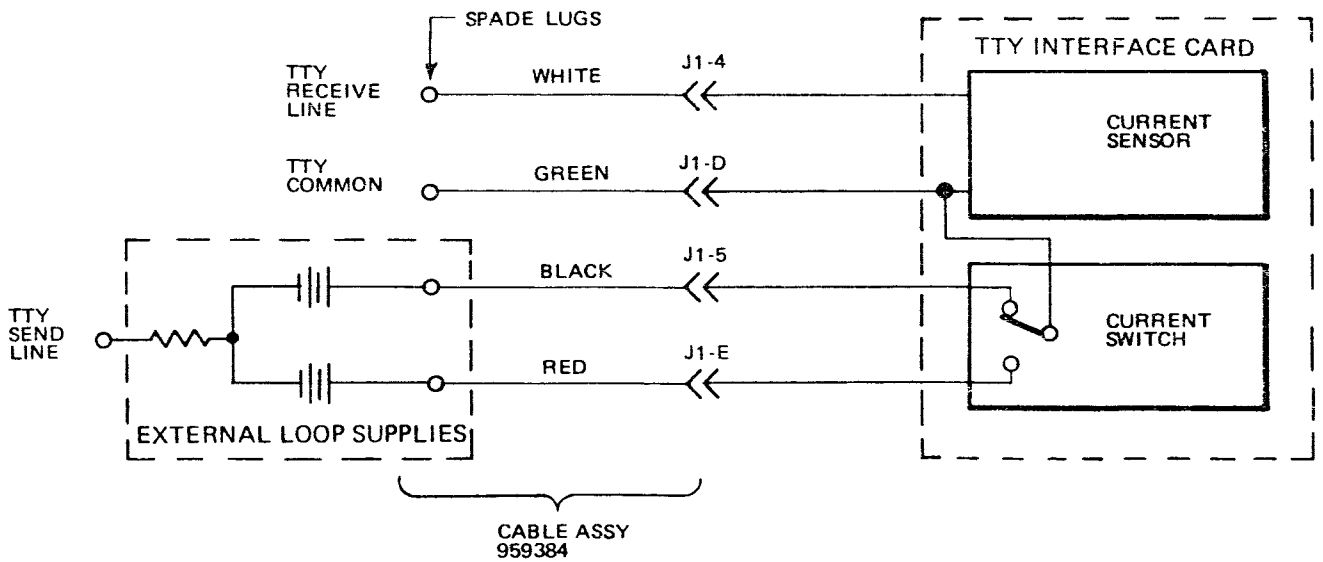


FIGURE 2-7.3. TELETYPEWRITER POLAR INTERFACE WIRING DIAGRAM

2-7.7 AUTOMATIC SEARCH CONTROL (ASC).

Components required for installation of the ASC option depend on which other options are installed in the 733 ASR. When used by itself for local operation, the ASC requires the following items:

- (1) ASC printed-circuit card installed in ASR card slot A7
- (2) Motherboard-access PC card installed in ASR card slot A6
- (3) Top-access connector to connect the two above PC cards.
- (4) 14-ampere power supply, consisting of two PC cards in card slot A9 and A10.

When the ASC is used in conjunction with the Remote Device Control which permits remote operation of the ASC, the motherboard-access PC card is not needed in card slot A6. If the Auto Device Control option is already installed, the motherboard-access PC card is not required in card slot A6. But in all three cases the top access connector (item 3 above) is required between the ASC PC card in slot A7 and one of the other three PC cards in slot A6.

Install the two 14-ampere power supply PC cards into ASR card slots A9 and A10 (right row of PC card rack).

2-7.8 REMOTE DEVICE CONTROL. The Remote Device Control option is contained entirely on one PC card. To install, insert the RDC PC card into PC card slot A6 (Figure 2-1.1) of the KSR lower unit. Take special care when installing the PC card to prevent accidentally changing the pencil switch (S2) positions.



Upon installation, ascertain that the pencil switch (S2) positions on the RDC PC card are set as follows for normal operation:

<u>S2 Position</u>	<u>Normal State</u>
1	ON
2	ON
3	ON
4	ON
5	ON
6	OFF
7	OFF

2-7.9 1200-BAUD INTERFACE. The 1200-Baud Interface option consists of a 1200-Baud Transmit PC card (slot A7 or A8, lower unit), a 1200-Baud Receive PC card (slot A5), a EIA line interface connector cable, and a panel SPEED switch. To install in the 733 ASR, proceed as follows.

- a. Remove the standard 300-Baud Transmit/Receive PC card from lower unit PC card rack slot A5 (green ejector) and replace with the 1200-Baud Receive PC card.
- b. Install the 1200-Baud Transmit PC card in PC card slot A8 (gray dot) if used with an external modem. If the 1200-Baud Modem PC card is installed in slot A8, install the 1200-Baud Transmit PC card in slot A7 (violet dot).
- c. Replace the standard 300-Baud EIA cable from the terminal to the communications interface (see Figure 2-4.1) with the 1200-baud EIA cable.
- d. Gently pry up the black plastic panel which covers the ON LINE/OFF and POWER switch, and
 - (1) Install the SPEED switch in the extra hole in the switch bracket next to the existing ON LINE switch. Mount the lock washer and knurled nut atop the bracket and the locking ring and hex nut on the bottom.
 - (2) Snap the new black POWER switch panel into place.
 - (3) Remove the connector which connects the ON LINE switch to the keyboard. Insert the new SPEED switch wires into position 8 and position H of the connector. Reconnect to the keyboard.

2-7.10 AUTO ANSWER CONTROL. The Auto Answer Control (TI Part No. 960984) is available in two versions. One connects the data terminal to the communication line using a Bell System type CBS data access arrangement (DAA), or equivalent, which requires an internal modem in the 733 Data Terminal. The second Auto Answer Control version is designed for use with a Bell System 103A data set or equivalent (no internal modem is required). A display panel for the 733 Data Terminal is included with both versions.

2-7.10.1 Installation of CBS-type DAA Auto Answer Control. The Auto Answer version for use with CBS-type DAA includes an Auto Answer PC card (TI Part No. 960885), a display panel (960165), a panel mounting bracket (971420), a display panel cable (971556), an internal modem PC card (960887 series), and a 300-baud modem cable (971557). To install this Auto Answer Control version, switch POWER OFF, unplug the power cord, and proceed as follows.

- a. Ascertain that the Auto Answer PC card (960885) has resistor R2 (10 ohms) installed between jumpers J11 and J13. Also check that there is no resistor between J12 and J18.
- b. Lift the terminal cover, remove the PC card rack cover, and insert the Auto Answer PC card (purple color ejector) into PC card slot A7 (purple color dot).
- c. Install the modem PC card (grey color ejector) into PC card slot A8 (grey color dot).
- d. Install the display panel as follows. Refer to Figure 2-7.4 for location of components.

- (1) Remove the two Power Supply PC cards from PC card slots A9 and A10 (brown and red ejectors).
- (2) On the underside of the terminal cover, use diagonal cutters to cut the four pins which hold the blank option panel in place. Cut close to the metal push-on fasteners and pry off the fasteners with a screwdriver. Then cut the four plastic pins again, as short as possible to prevent interference with the new panel.
- (3) Attach the panel mounting bracket to the PC card rack front wall, using two 4-40 x 3/16 screws, two No. 4 splitlock washers, and two 4-40 hex nuts. Insert the screws from inside the PC card rack. See Figure 2-7.5 for installation details.
- (4) Attach the display panel cable (971556) connector P14 to the PC card on the underside of the panel as shown in Figure 2-7.4. The connector number should face the underside of the panel.

- (5) Loosely insert two 6-32 x 5/16 screws into the front lower part of the display panel. Place a drop of Loctite on the threads.
 - (6) Locate the display panel so that the two 6-32 screw heads insert into the keyhole slots in the back of the POWER switch box. Press down on the panel to seat the screws into the narrow part of the keyholes.
 - (7) Insert a screwdriver through the holes in the front of the POWER switch box and tighten both 6-32 screws.
 - (8) Insert and tighten two 4-40 x 1/4 screws and two No. 4 flat washers through the slots at the rear of the display panel and into the panel bracket as shown in Figure 2-7.5.
 - (9) Replace the two Power Supply PC cards removed in step (1) above. Be sure the colored PC card ejectors match the color dots on the PC card rack.
 - (10) Route the display panel cable (971556) behind and below the keyboard and along the left bottom of the data terminal base as shown in Figure 2-7.4. Secure the self-adhesive clamps to the bottom of the data terminal case.
 - (11) Plug connector P1 onto the top of the Auto Answer PC card (card slot A7, purple ejector) installed in step b. above.
- e. Connect the DAA cable leads to the CBS-DAA type data coupler according to Table 2-7.6. Connect the other end of the cable (P1) to the J1 connector at the right rear of the 733 Data Terminal. Secure the P1 connector with the screws provided.
 - f. Replace the PC card rack cover, close the terminal cover, and switch POWER to ON.

2-7.10.2 Installation of 103A-Type Data Sets. The Auto Answer Control version for use with 103A-type data sets includes an Auto Answer Control PC card (TI Part No.

TABLE 2-7.6. 300-BAUD AUTO ANSWER CONTROL PIN ASSIGNMENTS AND SIGNAL NAMES FOR CBS-DAA SERIES (OR EQUIVALENT) DATA COUPLERS*

Cable Lead Colors	DAA Terminal Marking	Signal Name
Black	SG	Signal ground
Brown	DA	Data access
Red	OH	Off hook
Orange	DT	Data tip
Yellow	DR	Data ring
Green	RI	Ring indicator
White	CCT	Coupler cut through

*Used only with built-in internal Answer Modem option.

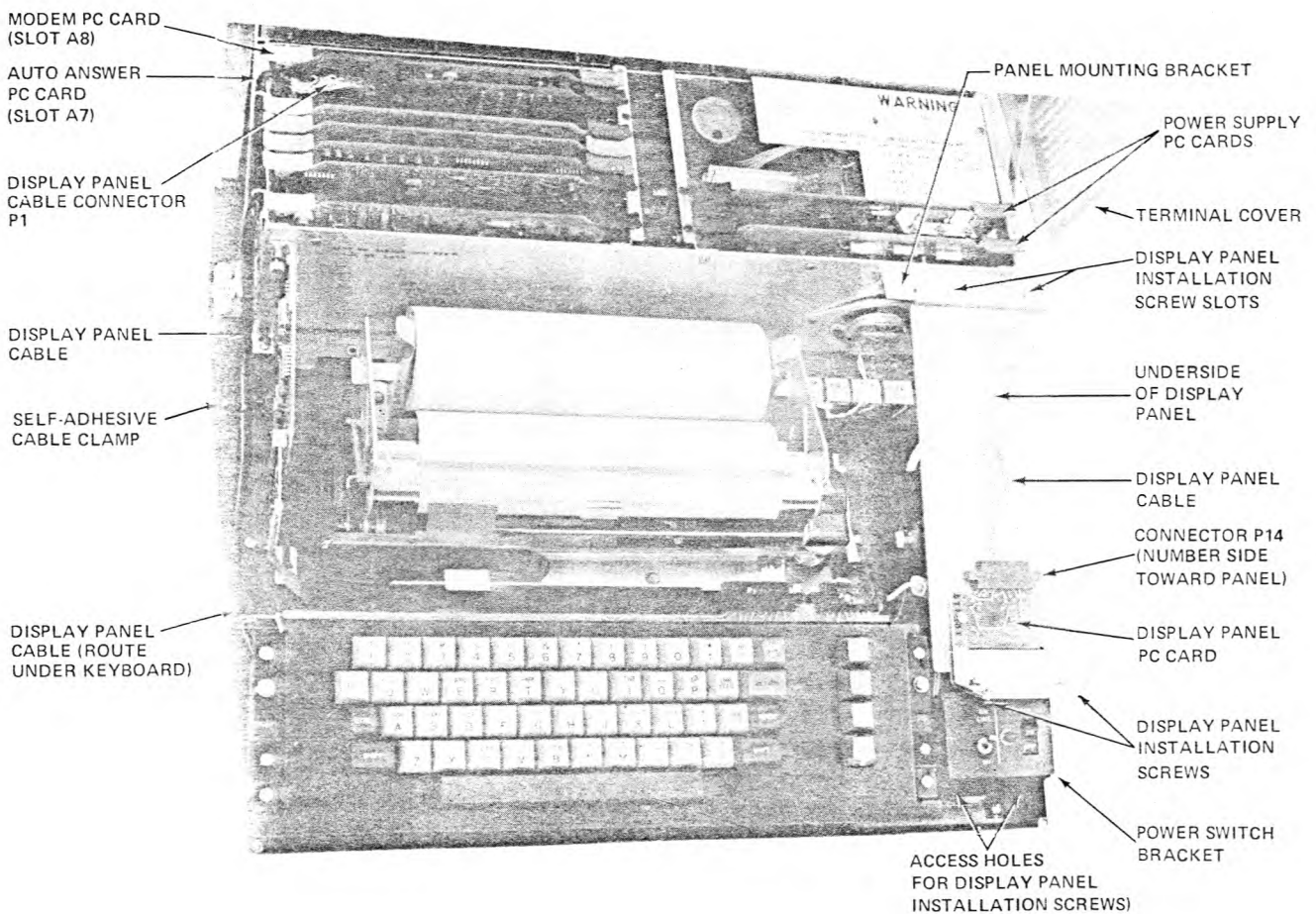


FIGURE 2-7.4. AUTO ANSWER CONTROL OPTION INSTALLATION COMPONENTS

- (1) Place thumbs under the PC card ejectors and lift upward to dislodge the PC card.
- (2) Lift the PC cards up and out of their PC card rack slots.

- e. Attach the panel mounting bracket to the PC card rack front wall, using the hardware shown in Figure 2-7.5.

NOTE

Some Model 733 Data Terminals are delivered with the bracket installed.

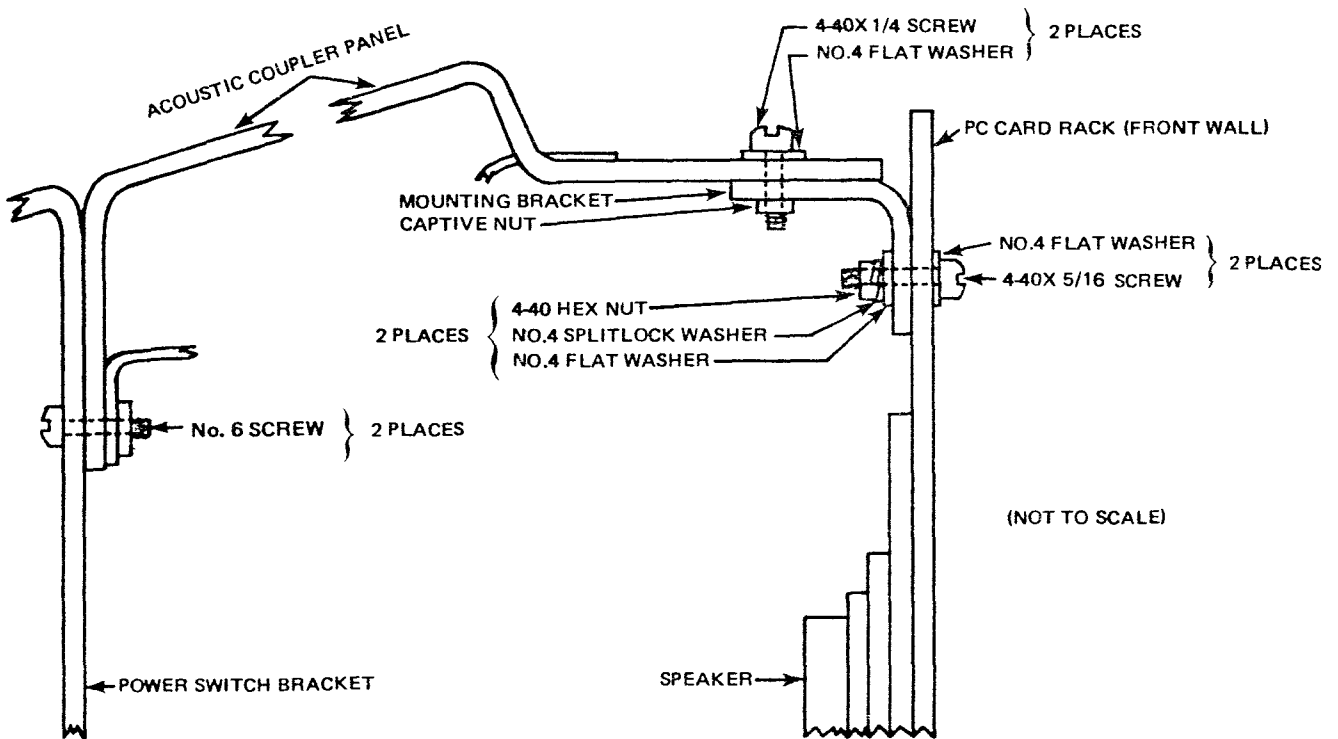


FIGURE 2-7.5. ACOUSTIC COUPLER PANEL INSTALLATION DETAILS

f. Install the cable attached to the Acoustic Coupler panel, routing the cable between the keyboard and the printhead cable bracket and between the left side of the PC card rack and the terminal cover, slide support as shown in Figure 2-7.6.

- (1) Remove the protective paper from the self-adhesive cable clamp and press it on the terminal base between the keyboard and the printhead PC card brace as shown in Figure 2-7.6.
- (2) Press the cable into the cable clamp slots.
- (3) Loosely attach the cable to the PC card rack using a cable tie-down strap as shown in Figure 2-7.6.

g. Add a drop of Loctite to the two 6-32 x 5/16 screws and start them into the captive nuts on the front part of the Acoustic Coupler panel as shown in Figure 2-7.5. Kit 969597 contains two 6-20 x 1/2 self threading screws. The Loctite is not required. Position the panel so that the loose No. 6 screws insert into the two keyhole slots at the rear of the POWER switch box.

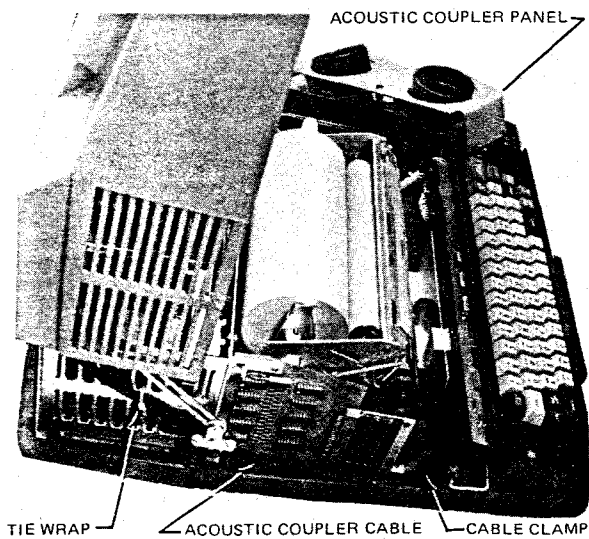


FIGURE 2-7.6. INSTALLING THE ACOUSTIC COUPLER PANEL CABLE

- (1) Press down on the front of the Acoustic Coupler panel so the two loose No. 6 screws seat in the narrow part of the keyhole slots in the POWER switch box.
- (2) Insert two 4-40 x 5/16 screws and two No. 4 flat washers through the two slots in the upper part of the Acoustic Coupler panel and into the mounting bracket captive nut as shown in Figure 2-7.5. Tighten the screws.
- (3) Insert a screwdriver through the front of the POWER switch box as shown in Figure 2-7.7 and tighten the two No. 6 screws at the front part of the Acoustic Coupler panel.

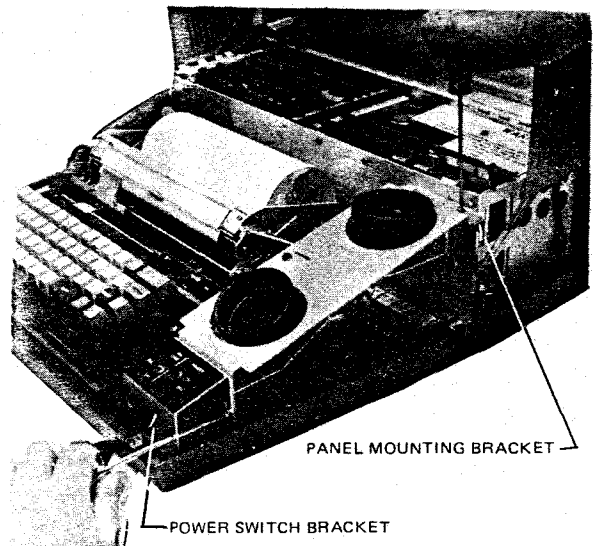


FIGURE 2-7.7. INSTALLING THE ACOUSTIC COUPLER PANEL

- h. Install the Acoustic Coupler PC card (grey ejector) into the left rear PC card slot. Press down firmly on the PC card ejectors.
- (1) Connect the Acoustic Coupler panel cable (installed in step f. above) connector to the left side of the Acoustic Coupler PC card. Route the cable out the rear of the PC card rack.

f. Install the cable attached to the Acoustic Coupler panel, routing the cable between the keyboard and the printhead cable bracket and between the left side of the PC card rack and the terminal cover, slide support as shown in Figure 2-7.6.

- (1) Remove the protective paper from the self-adhesive cable clamp and press it on the terminal base between the keyboard and the printhead PC card brace as shown in Figure 2-7.6.
- (2) Press the cable into the cable clamp slots.
- (3) Loosely attach the cable to the PC card rack using a cable tie-down strap as shown in Figure 2-7.6.

g. Add a drop of Loctite to the two 6-32 x 5/16 screws and start them into the captive nuts on the front part of the Acoustic Coupler panel as shown in Figure 2-7.5. Kit 969597 contains two 6-20 x 1/2 self threading screws. The Loctite is not required. Position the panel so that the loose No. 6 screws insert into the two keyhole slots at the rear of the POWER switch box.

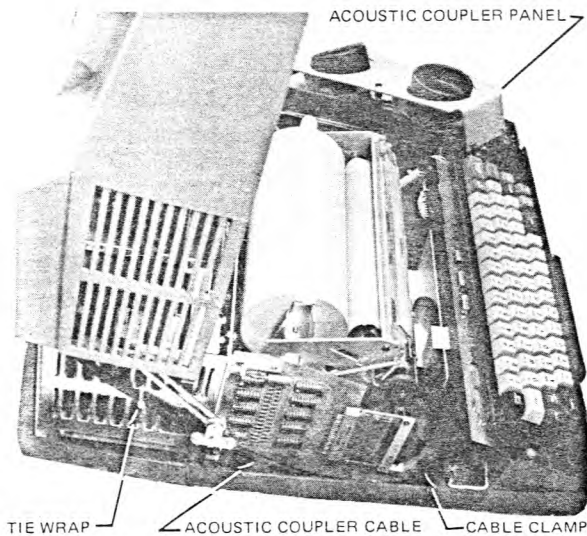


FIGURE 2-7.6. INSTALLING THE ACOUSTIC COUPLER PANEL CABLE

- (1) Press down on the front of the Acoustic Coupler panel so the two loose No. 6 screws seat in the narrow part of the keyhole slots in the POWER switch box.
- (2) Insert two 4-40 x 5/16 screws and two No. 4 flat washers through the two slots in the upper part of the Acoustic Coupler panel and into the mounting bracket captive nut as shown in Figure 2-7.5. Tighten the screws.
- (3) Insert a screwdriver through the front of the POWER switch box as shown in Figure 2-7.7 and tighten the two No. 6 screws at the front part of the Acoustic Coupler panel.

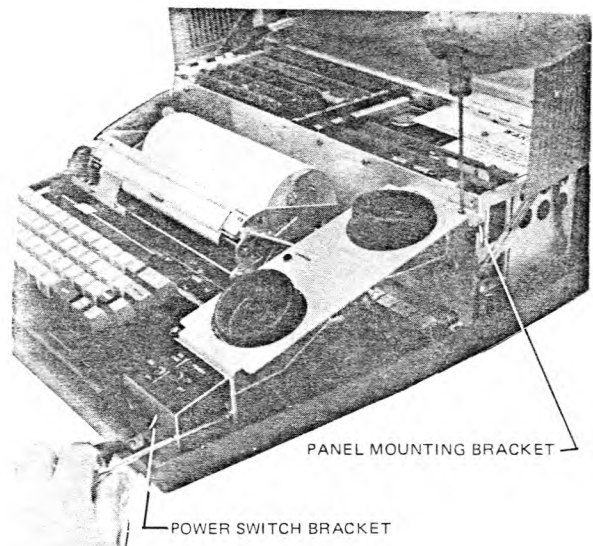


FIGURE 2-7.7. INSTALLING THE ACOUSTIC COUPLER PANEL

h. Install the Acoustic Coupler PC card (grey ejector) into the left rear PC card slot. Press down firmly on the PC card ejectors.

- (1) Connect the Acoustic Coupler panel cable (installed in step f. above) connector to the left side of the Acoustic Coupler PC card. Route the cable out the rear of the PC card rack.

(2) Tighten the loosely attached cable tie-down strap installed in step f. (3) above.

i. Reinstall the two Power Supply PC cards removed in step d. above. Be sure the ejector colors match the color dots on the PC card rack. Press down firmly on the ejectors.

j. Replace the PC card rack cover by inserting the three ears on the rear of the cover into the three slots at the top rear of the PC card rack. Fold down the cover as if hinged and tighten the two cover retaining screws.

k. Install the desired connector into the communication interface connector (J1) at the rear of the data terminal. Two connectors are available:

- A jumper connector (TI Part No. 973258) supplied with the Acoustic Coupler kit equips the terminal to communicate only through the Acoustic Coupler. Connector pin assignments are listed in Table 2-7.7.

- An optional "Y" connector and cable (TI Part No. 973254) permits a variety of interface connections in addition to the Acoustic Coupler. Y-connector pin assignments are listed in Table 2-7.8.

To install either connector into the data terminal, simply plug the connector into the rightmost rear connector slot of the data terminal; insert two 4-40 x 5/16 screws into the connector ears and tighten to secure the connector.

TABLE 2-7.7.

PIN ASSIGNMENTS FOR ACOUSTIC COUPLER JUMPER CONNECTOR (TI PART NO. 973258)

H to 1
10 to 4
8 to B
9 to C
K to 5

TABLE 2-7.8. PIN ASSIGNMENTS FOR ACOUSTIC COUPLER OPTIONAL "Y" CONNECTOR (TI PART NO. 973254)

Y-Connector Pin No.	Signal Source	Function	External Connector Pin No.	
A	Data Terminal	Protective Ground	1	} Cannon DP-25P or Equivalent
H	Data Terminal	Transmitted Data	2	
10	Data Terminal	Received Data	3	
8	Data Terminal	Clear-to-Send	5	
9	Data Terminal	Data-Set Ready	6	
7	Data Terminal	Signal Ground	7	
K	Data Terminal	Carrier Detect	8	
6	Data Terminal	Data-Terminal Ready	20	} Cannon DP-25S or Equivalent
F	Data Terminal	Request-to-Send	4	
1	Acoustic Coupler	Transmitted Data	2	
4	Acoustic Coupler	Received Data	3	
B	Acoustic Coupler	Clear-to-Send	5	
C	Acoustic Coupler	Data-Set Ready	6	
3	Acoustic Coupler	Signal Ground	7	
5	Acoustic Coupler	Carrier Detect	8	
A	Acoustic Coupler	Protective Ground	1	

2-7.13 CALCULATOR NUMERIC CLUSTER KEYBOARD. If the calculator cluster keyboard capability is desired, the standard keyboard may be replaced by the Calculator Cluster Keyboard Kit (TI Part No. 974056-0001). To convert, remove the four mounting screws holding the keyboard to the keyboard brackets and

disconnect the keyboard cable. Install the new keyboard with the keyboard cover supplied in the kit and reconnect the cables to the keyboard. Calculator cluster keyboard layout is shown in Figures 3-5.16 through 3-5.20 in Section III of this manual.

SECTION III

THEORY OF OPERATION

3-1 GENERAL.

Five basic functions are performed within each KSR:

- a. Power supply (Paragraph 3-3)
- b. Printer (Paragraph 3-4)
- c. Keyboard and Interface (Paragraph 3-5)
- d. Line Interface (Paragraph 3-6)
- e. Terminal control (Paragraph 3-7).

Adding the ASR Module Assembly (upper unit), the data terminal has five additional functions necessary for ASR terminal operation:

- a. Record controller
- b. Playback controller
- c. Motion controller
- d. Display functions
- e. Cassette transport.

Each terminal function may be contained on one or more printed circuit (PC) cards in the terminal. Therefore, terminal functions, rather than terminal PC cards, are described in this theory of operation. Frequent references are made to Texas Instruments assembly and electrical drawings contained in the appendixes to this manual.

3-2 SYSTEM ARCHITECTURE.

The data terminal architecture is arranged around a single, serial data bus, a concept illustrated in Figure 3-2.1. The bus is time-shared both by a line loop and local loop within the terminal and by the devices within each loop. The function of controlling which devices may use the serial data bus, and during what times, is done by a terminal control. Because of the high rate at which data is transferred within the terminal on the data bus, and the comparatively slow rate at which the devices on the bus can react once they receive the data, operation of each loop

within the terminal is essentially simultaneous and independent. This simultaneous operation is illustrated in Figure 3-2.2, which shows that the terminal control can send a data character on the bus as rapidly as one every 88 μ sec. Conversely, the table in Figure 3-2.2 states that the fastest line action period is one every 8.33 msec and the fastest local action is one every 180 μ sec.

Since the terminal control can provide enables to the line and local loops much faster than they require, both loops experience negligible delays from terminal control answering their requests to send data on the serial bus.

A better understanding of the terminal control will yield easier comprehension of the system architecture. Figure 3-2.2 shows that the terminal control accepts requests from each transmitting device. The terminal control also monitors the status of each device on the data bus: i.e., whether the device is on-line, local, off, busy, etc. If more than one device has requested to transmit on the serial data bus, the terminal control must decide which device has the highest priority (see priority order in Figure 3-2.3), whether that device is on-line or local, and if the line loop or local loop is busy. For example, if the highest priority device requesting to transmit to the serial data bus is in local and the local loop is not busy, the terminal control will enable the transmitting device (i.e., keyboard) and all receiving devices (i.e., printer), if they too are in local, to the data bus and the data on it during an enable time frame. The local loop will then go busy for some time, and the terminal control may then act upon any request it may have from a line device (if the line loop is not busy). Figure 3-2.4 shows a typical timing sequence when two devices simultaneously request the data bus. Figures 3-2.5 through 3-2.8 show some of the signals and data paths involved when terminal control interfaces with the various devices on the serial data bus.

3-3 POWER SUPPLY.

A functional block diagram of the power supply is shown in Figure 3-3.1. The supply provides voltages of +33V unregulated, +5V regulated, +12V regulated, 5.6V regulated and -12V regulated to the terminal. A power reset is incorporated in the circuit to reset the terminal upon power up or power failure.

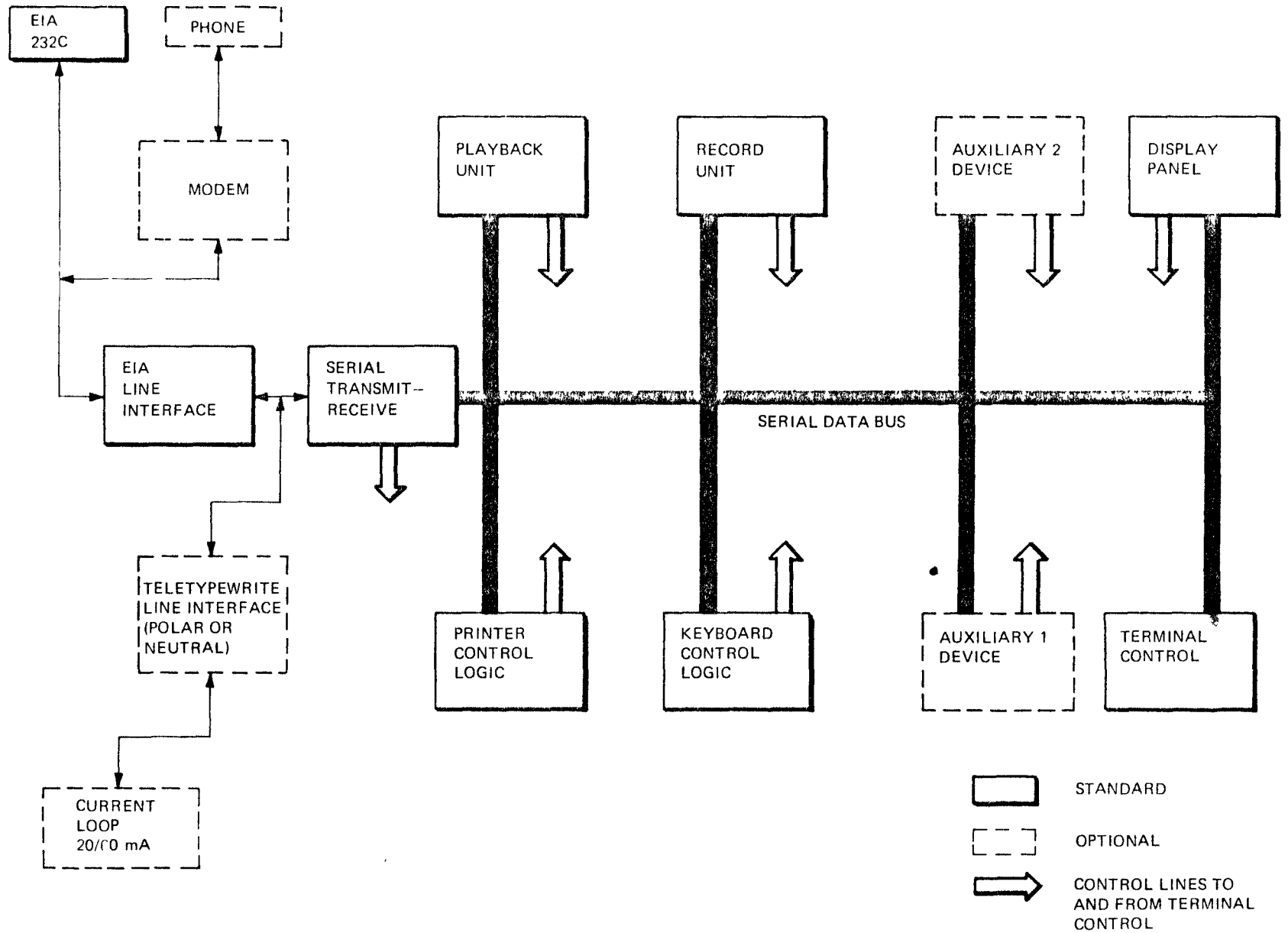
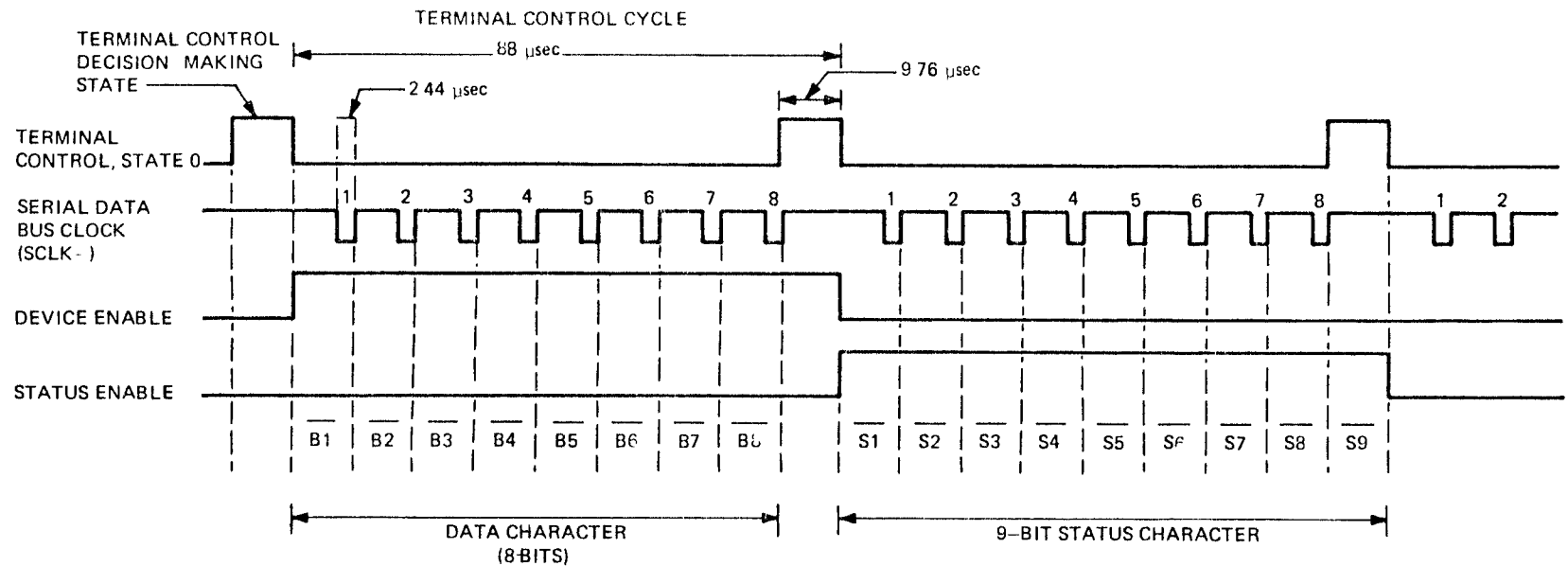


FIGURE 3-2.1. ASR DATA TERMINAL SYSTEM ARCHITECTURE



MAXIMUM REQUIRED TRANSMIT RATES
TO SERIAL DATA BUS

	RATE CPS *	PERIOD msec
1 SERIAL RECEIVER/XMTTER	30	33
2 RECORD PRINT BUFFER	33	30
3 AUX 2 (ANSWER-BACK)	30	33
4 1200 BAUD RECEIVER/XMITTER	120	8.33
5. KEYBOARD (REPEAT TO RECORD)	1140	0.88
6 AUX. 1 (AUX. INPUT TO RECORD)	1140	0.88
7 PLAYBACK (BUFFER TO ASC)	5.5K	0.18

* CPS - CHARACTERS PER SECOND

S1	RCBFFL	RECORD BUFFER FULL
S2	BOEOCA1-	CAS-1 NOT AT THE END OF THE TAPE
S3	BOEOCA2-	CAS-2 NOT AT THE END OF THE TAPE
S4	RERROR-	NO PLAYBACK ERROR
S5	RFEED-	PLAYBACK NOT ON
S6	KBDLOC	KEYBOARD IN LOCAL
S7	PRNLOC	PRINTER IN LOCAL
S8	PRNOFF	PRINTER OFF
S9	PNHRDY-	RECORDER NOT READY

FIGURE 3-2.2. DATA TERMINAL SERIAL DATA BUS TIMING DIAGRAM

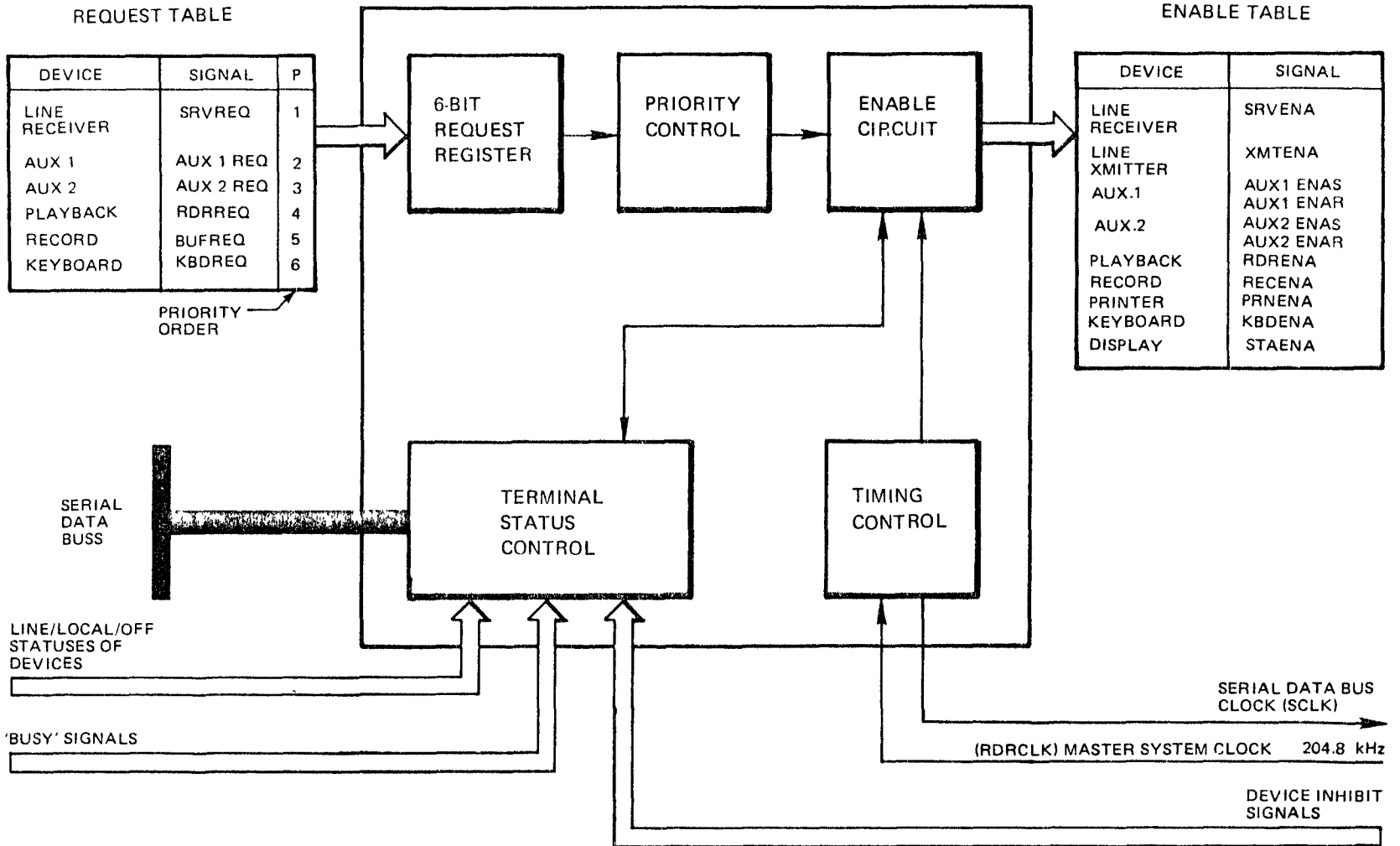


FIGURE 3-2.3. TERMINAL CONTROL BLOCK DIAGRAM

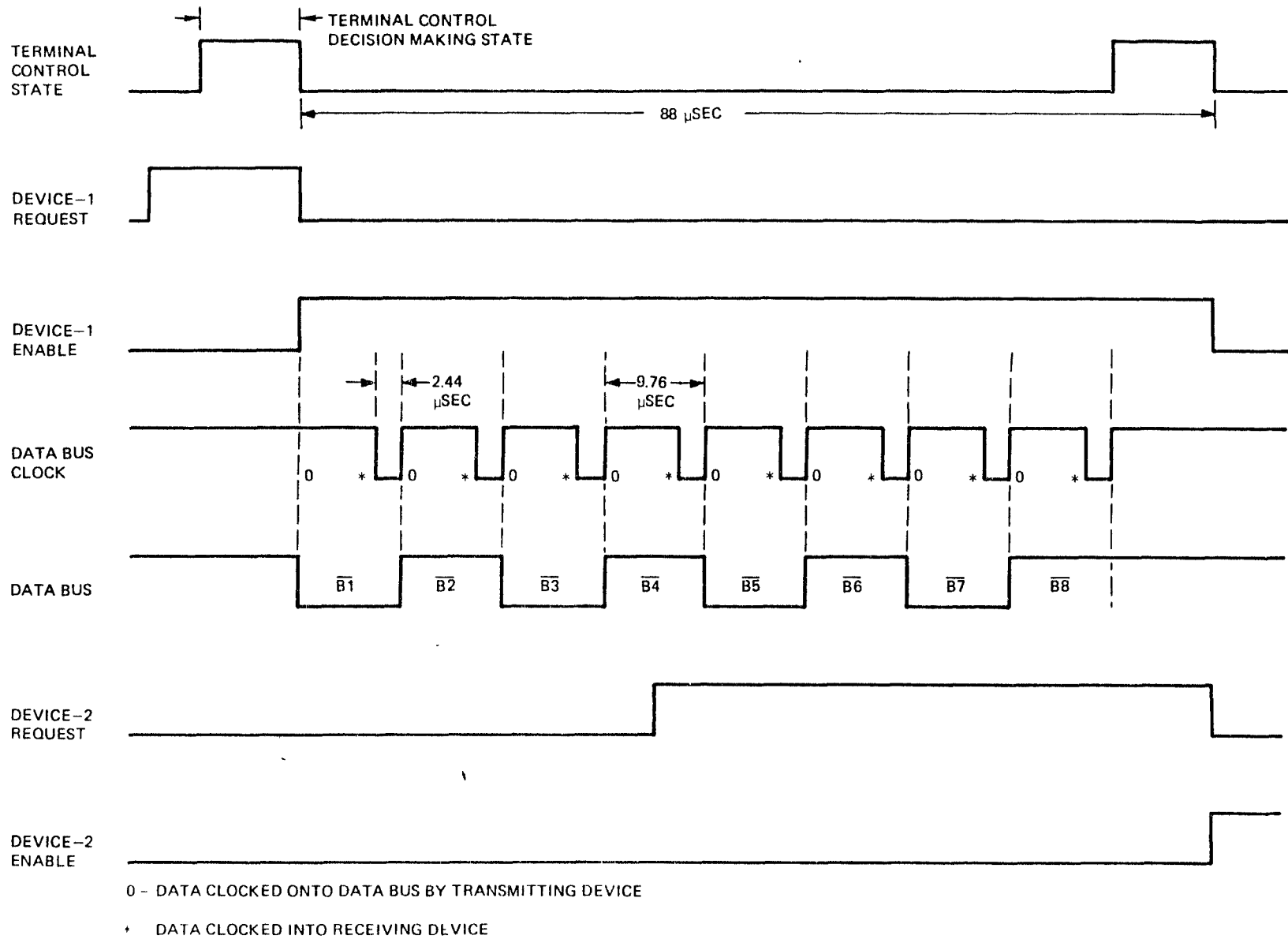


FIGURE 3 2.4. TIMING DIAGRAM, TYPICAL DATA TRANSMISSION VIA DATA BUS

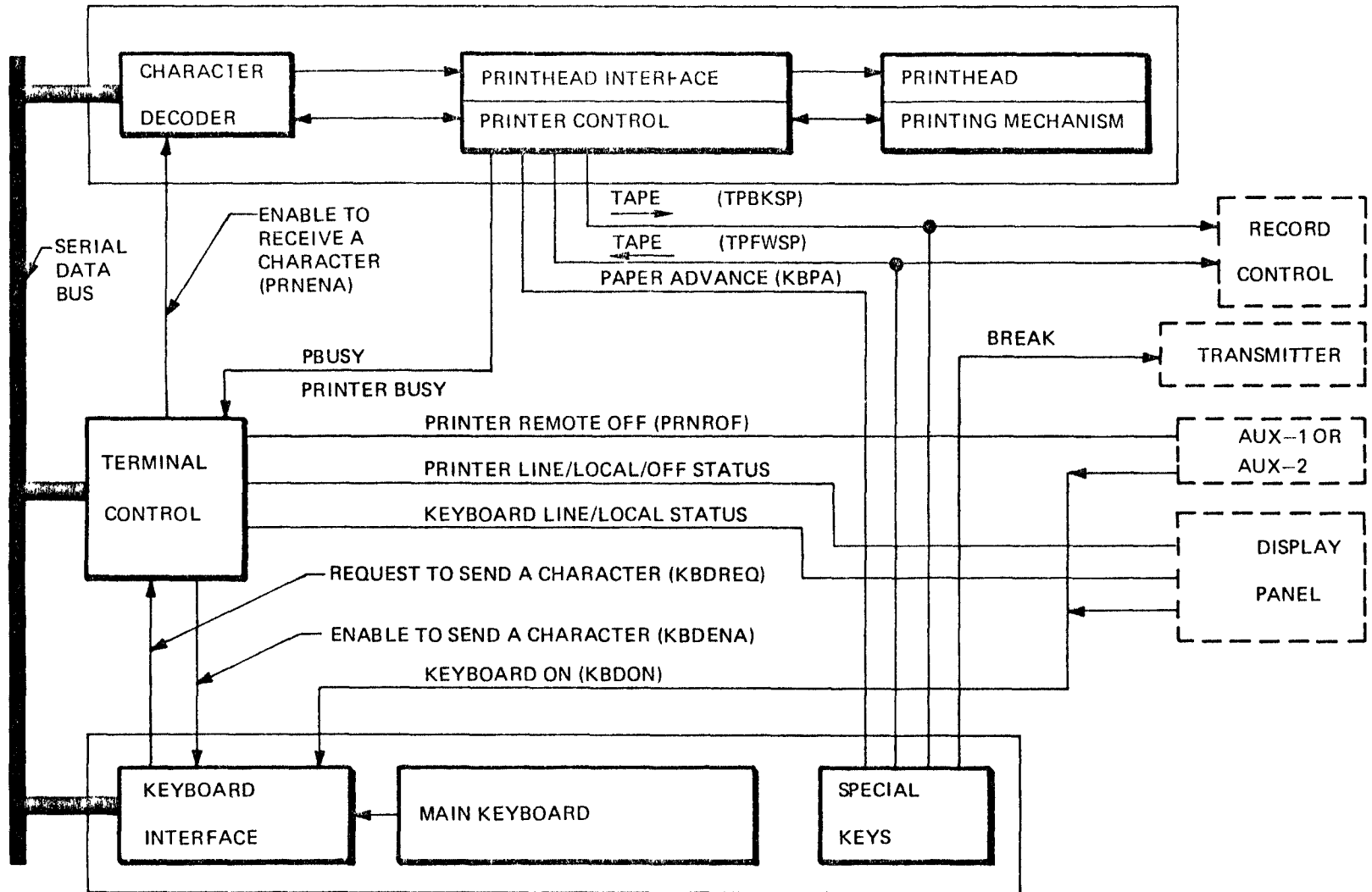


FIGURE 3-2.5. TERMINAL CONTROL PRINTER, AND KEYBOARD BLOCK DIAGRAM

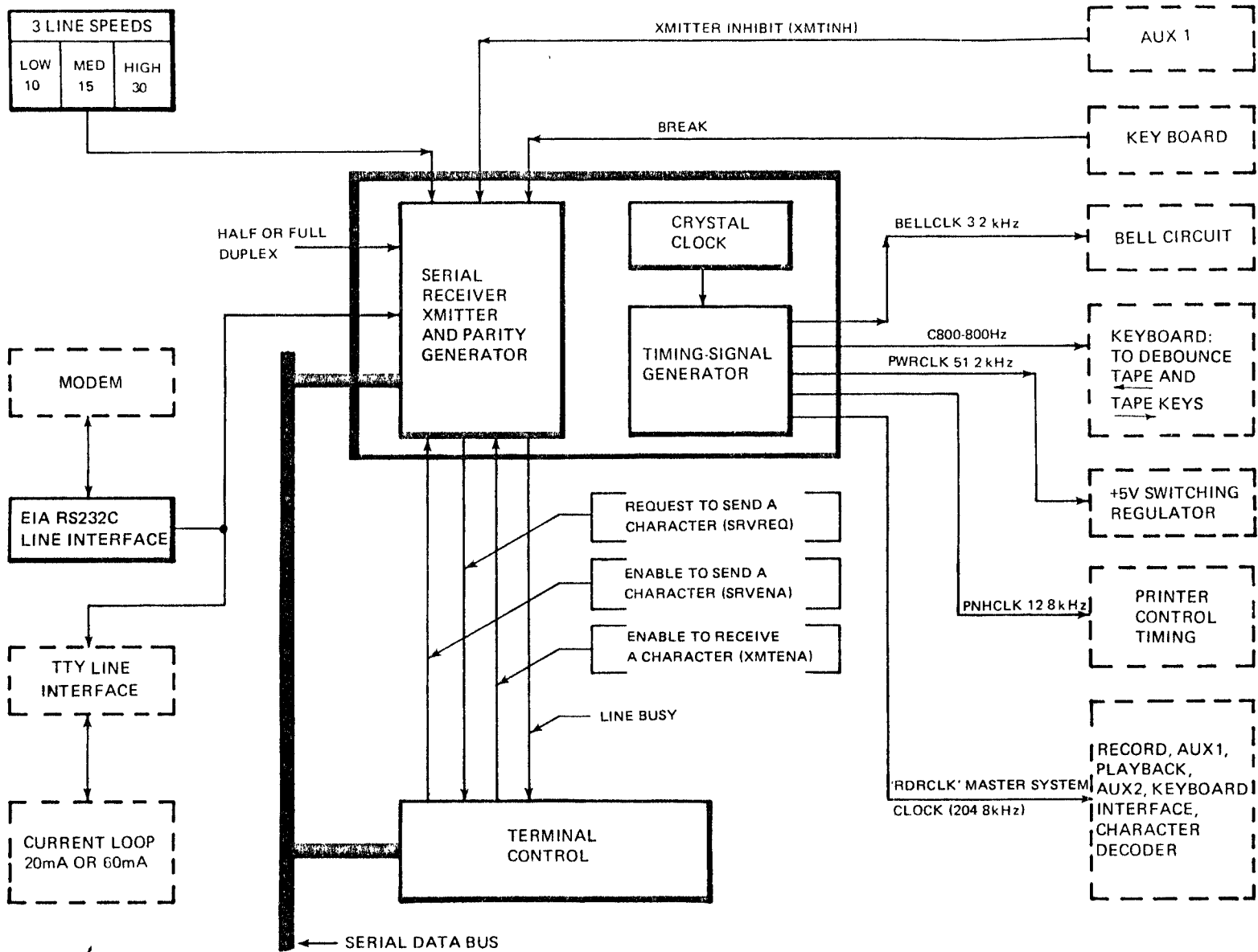
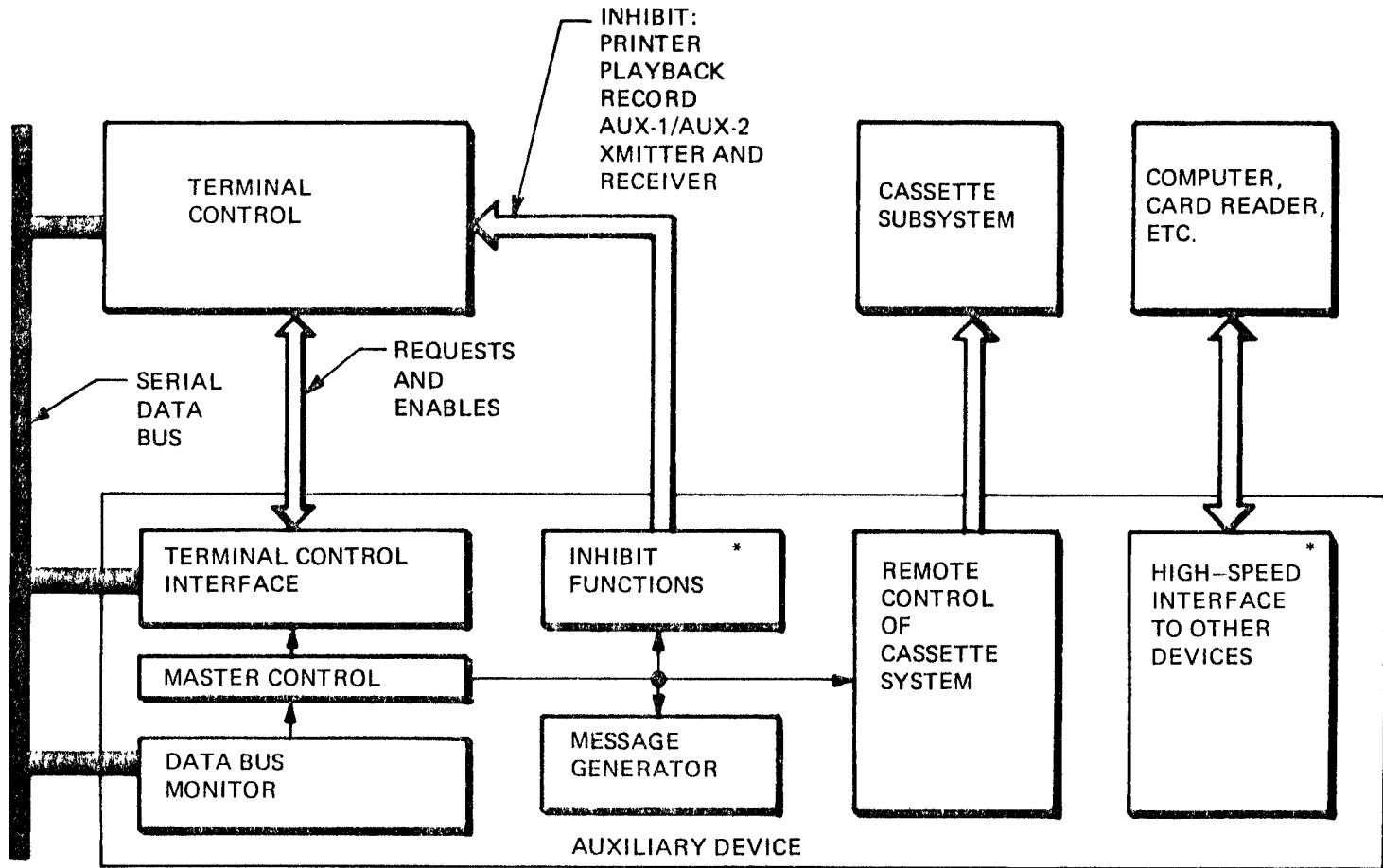


FIGURE 3-2.6. TERMINAL CONTROL, RECEIVER, TRANSMITTER, AND LINE INTERFACE (UP TO 300 baud)



TYPICAL OPTIONS USING AUX DEVICE:

- | | |
|-----------------------------------|--|
| 1. AUTO DEVICE CONTROL | 5. *POLLING OR SELECTIVE CALLING SYSTEM |
| 2. *AUTOMATIC SEARCH CONTROL | 6. *HIGH-SPEED DATA INTERFACE |
| 3. REMOTE CONTROL OF THE TERMINAL | 7. *FOR DECODING, ENCODING, OR CONVERTING 'CODES'. |
| 4. ANSWER-BACK MEMORY | |

*APPLICABLE TO AUX. 1 ONLY

FIGURE 3-2.7. AUXILIARY 1 OR 2 AND TERMINAL CONTROL

SERIAL DATA BUS

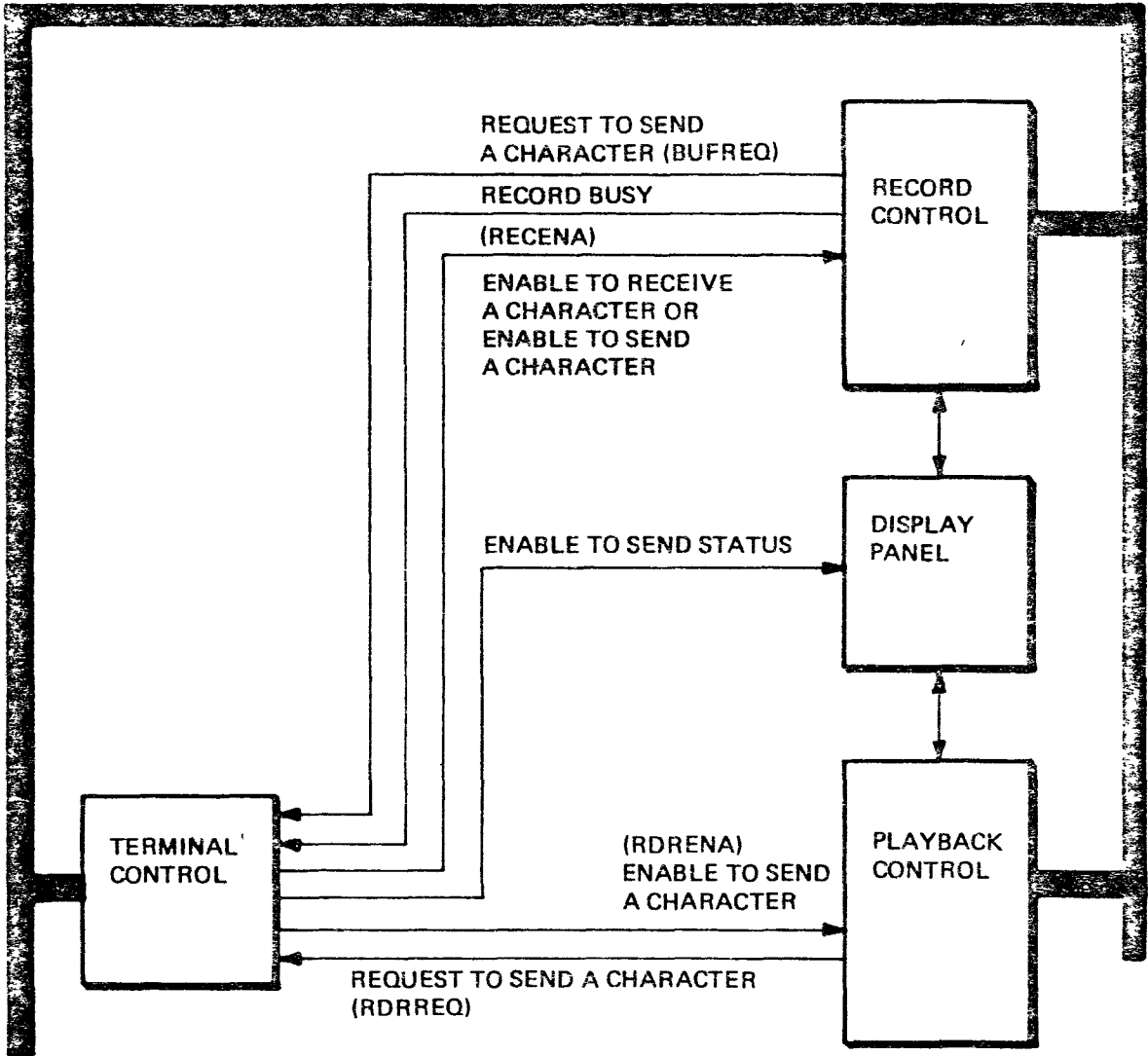


FIGURE 3-2.8. TERMINAL CONTROL, PLAYBACK, RECORD, AND DISPLAY PANEL

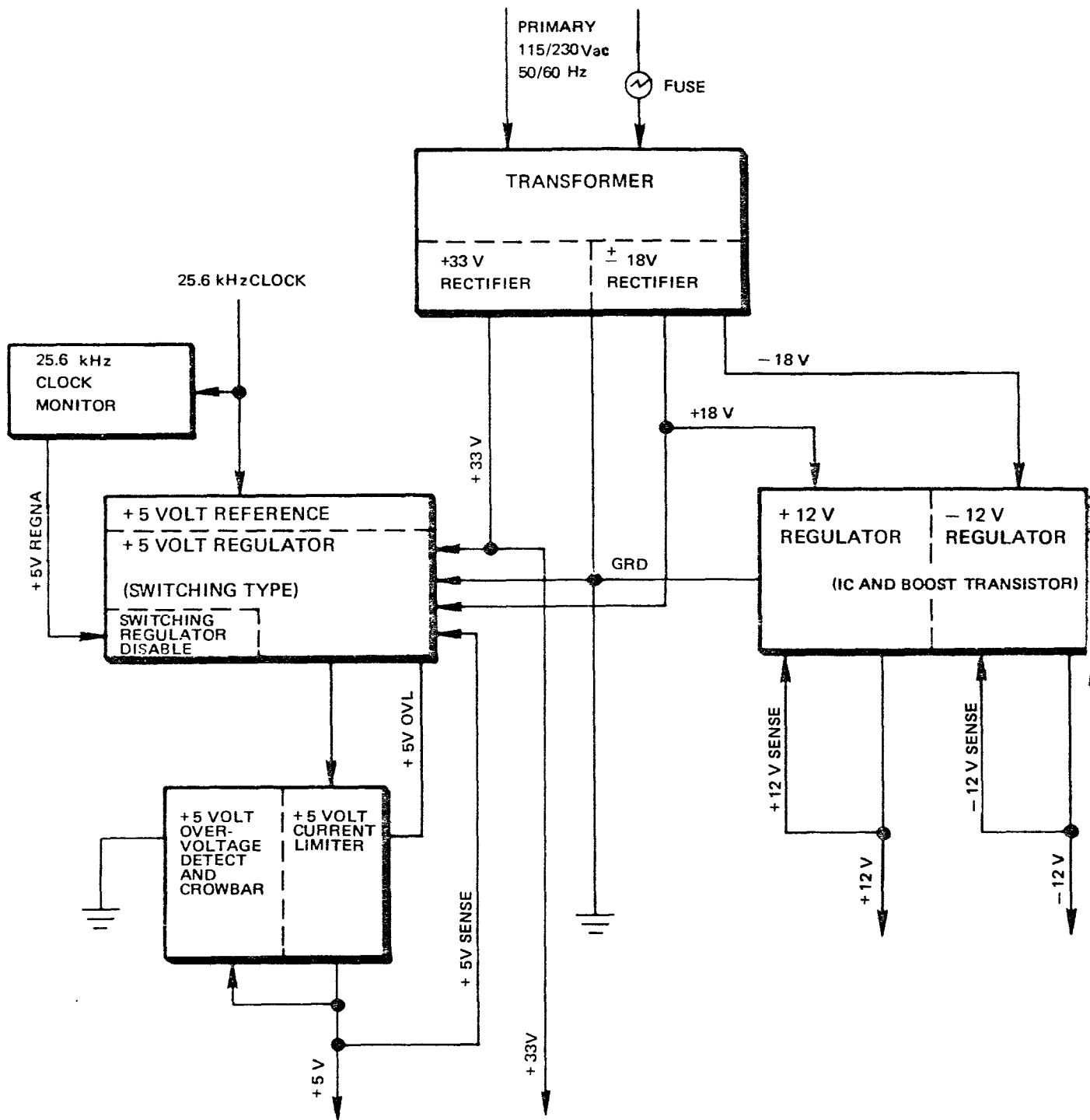


FIGURE 3-3.1. DATA TERMINAL POWER SUPPLY BLOCK DIAGRAM

3-3.1 +33 Volt UNREGULATED SUPPLY. The positive 33 volts for the terminal is obtained directly from the ac power module. The primary line voltage is passed through a stepdown transformer and then rectified. The unfiltered 33 volts goes to the KSR motherboard via a nine-wire cable which plugs into connector J10 on the motherboard. A capacitor and bleedoff resistor on the motherboard filters the 33 volts before it goes to the rest of the terminal. Schematics 959200 and 959188 in Appendix C show the generation of the 33-volt unregulated supply.

3-3.2 +5 VOLT REGULATED SUPPLY. The +5 Volt regulated supply employs a switching-type voltage regulator. The supply consists of four major sections:

- a. +5 Volt reference
- b. The 5 Volt regulator driver
- c. 5 Volt regulator amplifier
- d. Various failsafe circuits.

3-3.2.1 Reference. The +5V reference and auxiliary supplies the reference voltage for the +5V switching regulator, the headlift switching regulator, and the limited +5V needed for logic devices on the Control Regulator PC card. The +5 Volt reference and auxiliary is diagrammed on schematic 971451 or 959182* (Control Regulator PC card in Appendix C). The +5V reference is obtained from the +18V unregulated supply using integrated circuit (IC) voltage regulator AR3. The output voltage of the reference supply ($5.1 \pm 0.02V$) is determined by resistor R27 which is selected at unit test. Transistor Q4 acts as a current booster for the IC voltage regulator (AR3).

3-3.2.2 Regulator Driver. The 5V regulator driver uses a voltage comparator (AR4) to compare the +5V output with the reference voltage supplied by the +5V reference supply. A 25.6-kHz clock supplies the switching frequency which holds the comparator off for approximately two-thirds the clock period and allows the comparator to operate for approximately one-third the clock period (period $\cong 40\mu$ sec). When the comparator is operating, if the +5V output does not match the +5V reference input to the comparator, the regulator will supply a drive voltage to the amplifier switch via Q17. When the +5V output again matches the +5V reference, the regulator will turn off the drive to the amplifier switch. The greater the +5V current load, the longer the regulator drive to the amplifier switch will stay on. Q21 and CR6 help power the regulator driver during power UP to prevent it from latching up while power is coming up. A drawing of the +5V regulator driver is shown on schematic 959182* (control/regulator) in Appendix C.

3-3.2.3 Regulator Amplifier. At the command of the regulator driver, the 5V regulator amplifier switches the 33V supply to charge the 5V capacitor on the motherboard. The 33V supply is switched by Q1, with Q2, Q3, and Q4 supplying the drive current to turn on Q1. Q7 receives the command voltages from the regulator driver and turns on the 33V switch by controlling switch drive current transistors Q2, Q3, and Q4. Greater current loads on the +5V supply cause the 5V capacitor to discharge to a lower value during the off time of the regulator driver comparator. Therefore, during the comparator-on time, the switch must stay on longer to recharge the capacitor back to +5 volts.

Figures 3-3.2 through 3-3.5 show the switch output (input to inductor L1) under various 5V current loads. These figures also show +5V output at loads to illustrate a measure of +5V regulation. The 5 volt regulator amplifier is shown on schematic 971444 or 959181* (regulator amplifier) in Appendix C.

3-3.2.4 Failsafe Circuits. Three basic failsafe circuits are associated with the +5V power supply: current limit, overvoltage, and 25.6-kHz clock and clock detect. The current limit circuit consists of Q5 and Q6 on the Regulator Amplifier PC card and Q16 on the Control Regulator PC card. When R11 on the Regulator Amplifier PC card senses too much current (IR drop), Q6 turns on Q5, Q5 turns on Q16 (Control Regulator PC card), and Q16 turns off the regulator drive to the 33V switch. The current limit should be approximately 12 amps for the +5V supply. The overvoltage circuit consists of diode CR14, CR15, Q14, Q22, and Q23 on the Control Regulator card and SCR1 on the motherboard (schematic 959188).

When the +5V output voltage rises to approximately 5.5 volts, Q18 will turn on sufficiently to trigger the SCR on the motherboard and cause Q22 and Q23 to disable the regulator driver via CR15. When the SCR triggers the +5V output bus is shorted to ground by the SCR. The actual +5V output will then drop zero volts until the terminal power is switched off and then back on. The 25.6 kHz clock detect circuit consists of Z2, Q19, Q15, and Q20 on the Control/Regulator PC card (schematic 959182*). As long as the 25.6-kHz clock is present, a retriggerable oneshot (Z2) is continually triggered. The oneshot output Q keeps Q19 on, and the oneshot output Q keeps Q20 off. As long as Q19 is on, Q15 is off, and the regulator driver is enabled. Since Q20 is kept off, the motor drivers remain enabled and no terminal power reset (PWRRST-) occurs. If at anytime the 25.6-kHz clock is lost, the +5V regulator driver will be disabled, the motor drivers will be disabled, and a terminal

*This PC card is obsolete.

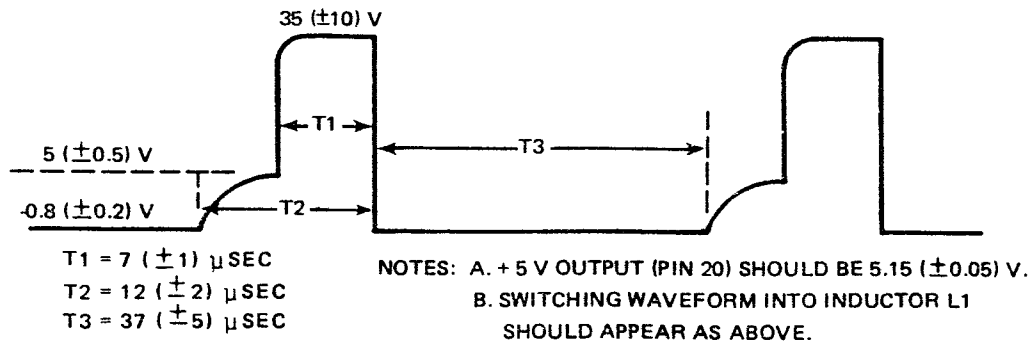


FIGURE 3-3.2. WAVEFORM, + 5 VOLTS AT NO LOAD

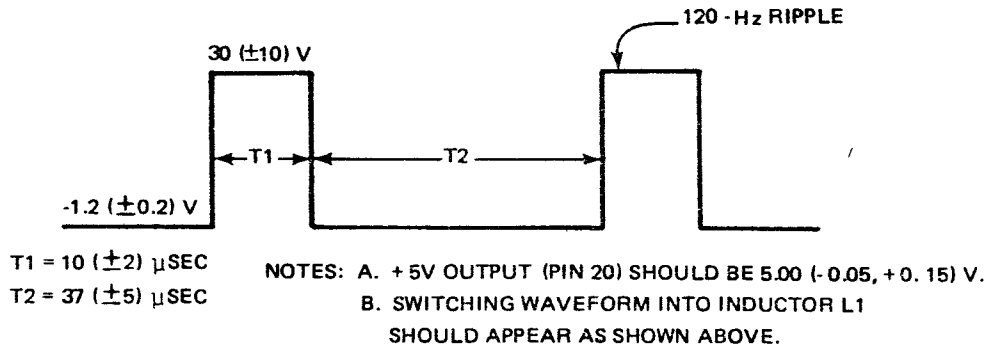


FIGURE 3-3.3. WAVEFORM, + 5 VOLTS AT 5-AMPERES LOAD

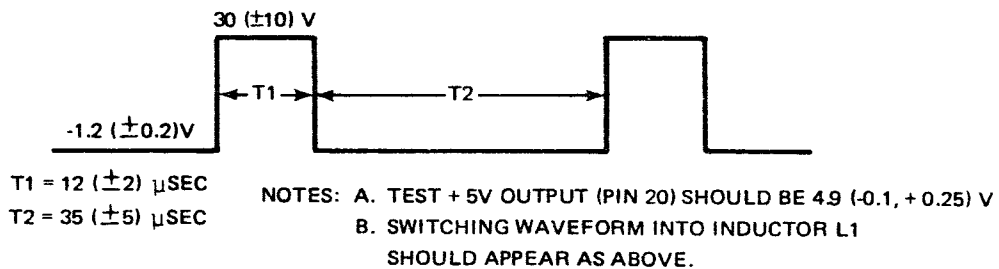


FIGURE 3-3.4. WAVEFORM, + 5 VOLTS AT 10-AMPERES LOAD

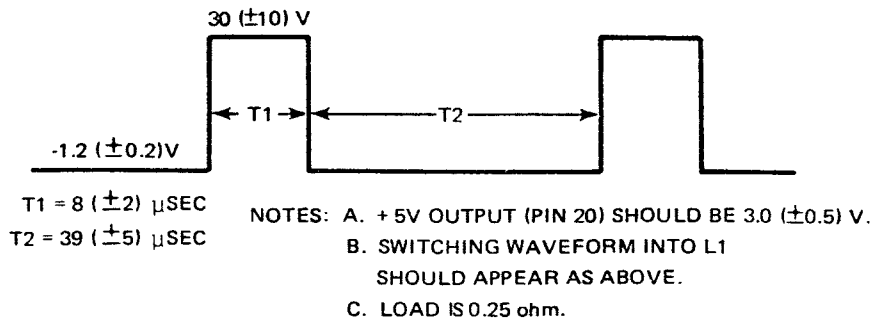


FIGURE 3-3.5. WAVEFORM, +5 VOLTS AT CURRENT LIMIT

APPLYING THE FOLLOWING PULSE TO POS33VUNFIL (PIN 7) . . .

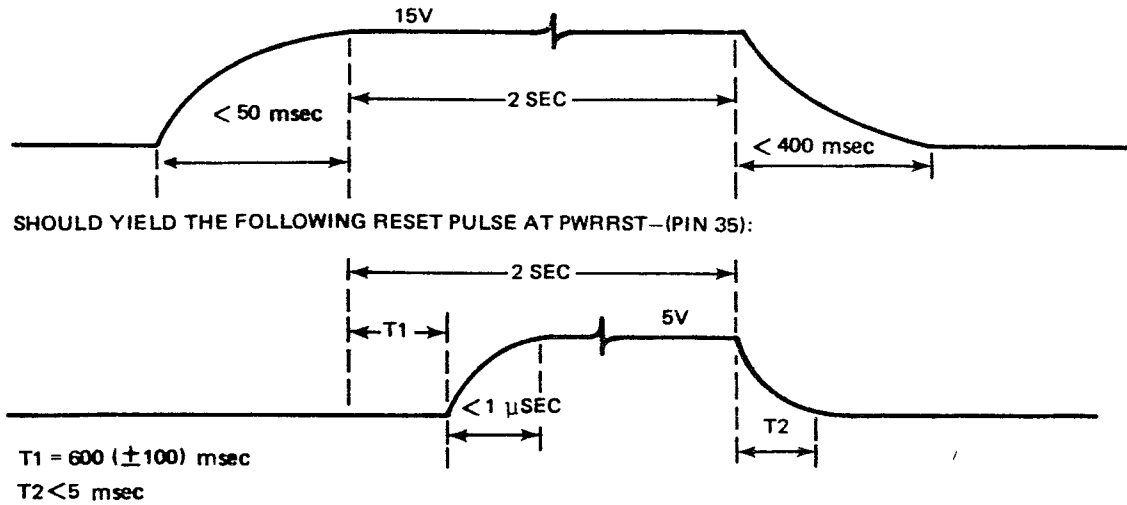


FIGURE 3-3.6. POWER RESET (PWRRST-) SEQUENCE WAVEFORM

power reset will occur. A clock circuit, located on the Control/Regulator PC card, provides the 25.6-kHz clock used by the switching regulators. It consists of a free running multivibrator and a divide-by-two flipflop. If at any time the PWRCLK (51.2-kHz) is lost, the switching regulators will still have a clock, approximately 25.6-kHz after passing through the divide-by-two flipflop (Z1).

3-3.3 +12 VOLT REGULATED SUPPLY. The +12 volt regulated supply is located on the Control/Regulator PC card. It consists of IC voltage-regulator AR1 and two current-booster transistors Q2 and Q1. The IC voltage regulator transforms the +18V unregulated supply to a +12V regulated supply with an approximate 2.5-amp current limit.

3-3.4 -12V REGULATED SUPPLY. The -12 volt regulated supply, located on the Control/Regulator PC card, consists of integrated circuit (IC) voltage regulator AR2 and current booster transistor Q3. The IC voltage regulator transforms the -18V unregulated supply to a -12V regulated supply with an approximate 500 mA current limit.

3-3.5 -5.6V SUPPLY. A -5.6V supply provided is used only

by the voltage comparators of the various switching regulators. The -5.6V supply, located on the Control/Regulator card, consists of zener diode CR9 and filter capacitor C26. Current from the supply is limited to a few milliamperes.

3-3.6 POWER-ON RESET CIRCUIT. A power-on reset circuit on the Control/Regulator PC card holds the terminal in a reset state during power up and resets the terminal when a momentary power failure occurs. Three field effect transistors (Q12, Q13, and Q14) hold the power reset bus (PWRRST-) at ground during a power up until turned off by Q11 and Q24. Q11 is turned on by Q10 which is controlled by a voltage dependent on an RC time constant set by R28 and C17. Momentary power failures are detected by Q8, which then turns off. When Q8 turns off, Q9 goes on and shorts C17 to ground, turning off Q10 and causing the power reset bus to be grounded by the three field effect transistors, Q12, Q13, and Q14. When the power failure ends and power is reapplied to the terminal, Q8 again goes on and Q9 goes off. C17 again charges through R28; approximately 600 msec later, the power reset bus (PWRRST-) again is removed from ground. A typical power reset sequence waveform is shown in Figure 3-3.6.

3-4 PRINTER SYSTEM.

The printer consists of seven major parts:

- a. Paper drive mechanism
- b. Printer drivers
- c. Printer control logic
- d. Character decoding
- e. Printhead
- f. Printhead interface
- g. Printhead compensation circuit.

The printer drivers are located on the Regulator/Amplifier PC card (slot A10), the printer control logic on the Printer Control PC card (slot A2), the character decoding on the Code PC card (slot A1), the printhead interface on the Printer Code PC card (slot A1 on the code card), and the printhead compensation circuit also on Code PC card (slot A1). A block diagram of the printer system is shown in Figure 3 4.1.

3-4.1 PAPER DRIVE MECHANISM. The paper drive mechanism feeds the printer paper and moves the printhead to printout information fed to the terminal. Major components include:

- a. The head stepping motor
- b. Paper advance motor
- c. Head lift solenoid
- d. Margin limit switch.

Adjustments for head lift, head damping, and head return speed are described in Section V.

3-4.2 PRINTER DRIVERS. Three driver groups control the motion of the printer mechanism:

- a. Head step motor drivers
- b. Paper step motor drivers
- c. Head lift solenoid driver.

All three drives are located on the Regulator/Amplifier PC

card (slot A10; see schematic 971444 or 959181*). The head step motor drivers and paper step motor drivers (A1 and A2 on schematic 959181*) are nearly identical circuits (e.g., inputs and outputs are different). Each set of motor phase drivers (three per set) utilizes the same type switching regulator used by the +5V power supply. The Printer Control PC card (slot A2; see schematic 981312 or 959175*) provides the input signals (commands) telling each driver when to institute an action. When the head or paper motor drivers receive a signal telling them a motor phase to step to (e.g., HPHA, HPHB, HPHC, PPHSA, PPHSB, PPHSC) and giving them the command to step (HPC, PACA), comparators A1AR1 or A2AR1 turn on the appropriate motor phase driver transistor (Q1, Q4, Q7) during the comparator-on time allowed; by the switching regulator 25.6 kHz switch clock. During the comparator-on time, the comparator (AR1) compares the input reference voltage from the Printer Control PC card with the voltage across R2 produced by the current flowing through a motor phase. When the current in a motor phase produces sufficient voltage, the comparator (AR1) turns off and stops the drive to the motor phases, and this reduces the motor torque. The object of the input commands (HPC, PACA) is to keep the current through the motor phases constant (via the switching regulator), producing a constant number of ampere turns, and thus a constant force to step (accelerate and decelerate) the motors. When either the head step driver or the paper step driver is not in the process of moving the head or paper, respectively, the drivers keep a "holding current" in one motor phase winding to keep the motor shafts from moving inadvertently. The amount of holding current is also controlled by the switching regulator via comparator AR1 and is determined by the input signals (HPC, PACA) from the Terminal Control PC card. Transistor Q10 (collector) in both A1 and A2 should be switching (between 0V and 5V) at all times except during a power reset.

The head lift solenoid driver is also a switching-type regulator similar to both motor driver regulators. It provides current to the head lift solenoid to lift the printhead during a carriage return or paper advance. The input signal (command) to initiate the head lift (LIFTHEAD) is provided by the printer control PC card. Comparator AR1, during the comparator-on time allowed by the switching clock (25.6 kHz), compares the input reference voltage (LIFTHEAD) with the voltage across R30 produced by the current flowing in the head lift solenoid. When the current in the solenoid produces sufficient voltage, the comparator (AR1) turns off the drive to the solenoid to maintain solenoid current at the proper value. When the head lift signal (LIFTHEAD) is not present, R16

* This PC card is obsolete.

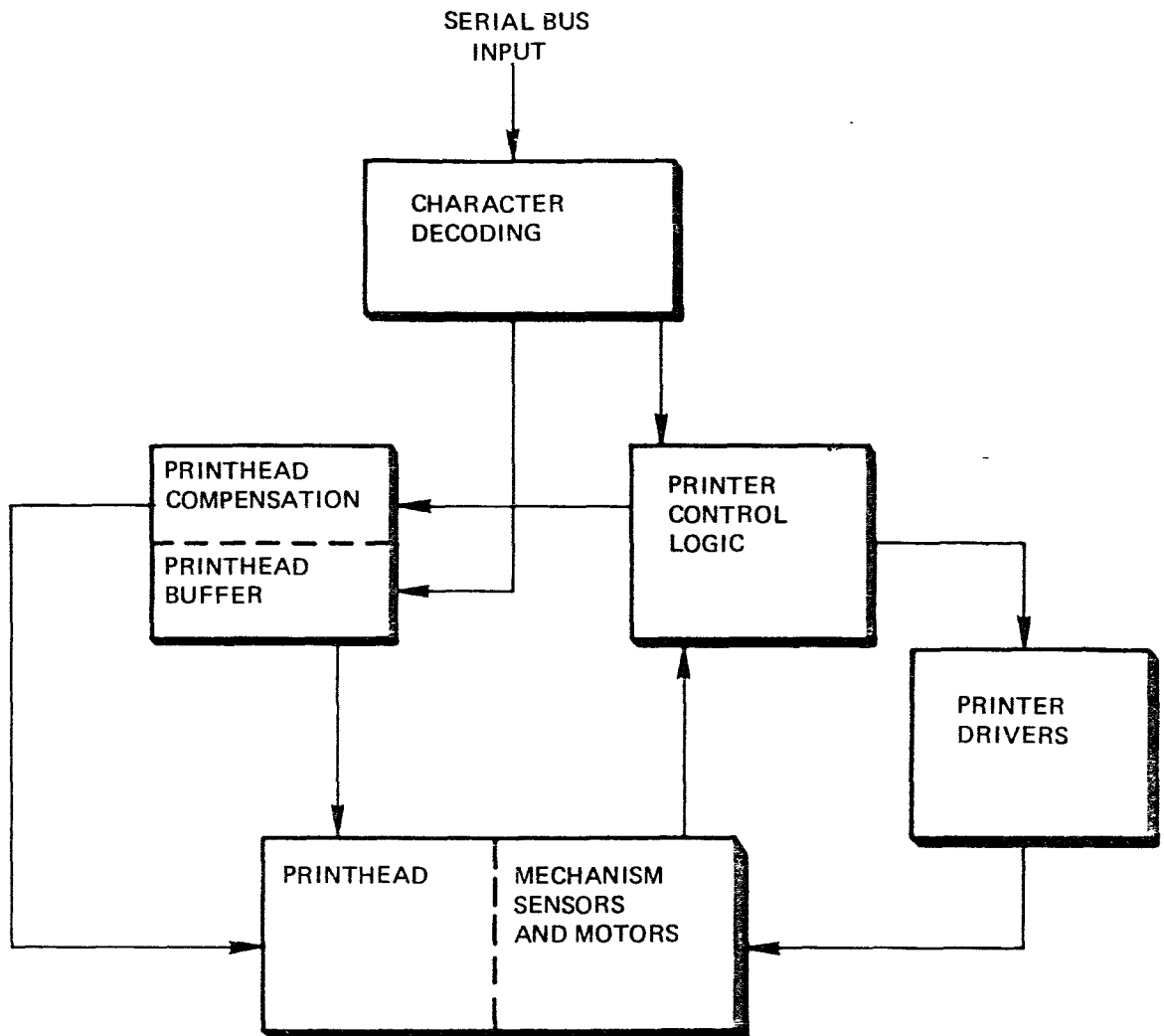


FIGURE 3-4.1. PRINTER SYSTEM BLOCK DIAGRAM

injects sufficient current to the comparator to ensure that it remains in the off state; therefore, no current is provided to the head lift solenoid. The collector of Q13 should switch (between 5V and 33V) only when the LIFTHEAD signal is present.

3-4.3 PRINTER CONTROL LOGIC. The Printer Control PC card (see Figure 2-1.1) contains logic and analog circuitry to control the following printer subsystem functions.

- a. Stepping the printhead to the right (print or space)
- b. Stepping the printhead to the left (backspace)
- c. Slewing the printhead to the left margin (carriage return)
- d. Advancing paper (line feed)
- e. Lifting the printhead during paper advance and carriage return
- f. Sounding the end-of-line warning.

The character decode circuitry of the Printer Code PC card and the keyboard TAPE, TAPE, and PAPER ADV keys provide command inputs to the Printer Control. Basic timing signals are provided by the Transmit/Receive PC card clock dividers. Limit switches and position sensors on the drive mechanism assembly provide status and feedback control signal input.

Printer Control provides output signals to the Regulator Amplifier stepping motor and solenoid drivers and to the printhead compensation and bell circuits of the Code PC card. It also supplies "busy" signal outputs to the Terminal Control.

3-4.3.1 Functional Blocks. The Printer Control consists of the following functional blocks.

- a. Synchronous input register - accepts carriage return, line feed, backspace and print/no-print commands from the printer code character decoder.
- b. Asynchronous input register accepts space (TAPE), backspace (TAPE), and paper advance (simultaneous line feed and carriage return)

commands from the keyboard discrete function (unencoded) keys.

- c. Automatic carriage return generator initiates line feed and carriage return if a print command is received while the printhead is at the right margin.
- d. Character timer - counts down the 12.8-kHz clock to time each character period in 5-msec increments (character period is defined as the time required to perform a space, backspace, or print operation: 30 msec). Line feed is performed in one or two character periods, depending on whether single or double line spacing is selected. Note that the printer control character period is independent of the terminal communication rate.

All command inputs are inhibited while the character timer is counting.

- e. Carriage return timer - counts down the 800-kHz clock to provide a "busy" delay during execution of carriage return. The print command and all asynchronous command inputs are inhibited during the carriage return delay. The delay terminates 190 msec after initiation of carriage return or 10 msec after the printhead reaches the left margin (e.g., after power turn on or an equipment malfunction), whichever is greater.
- f. Synchronizing register - synchronizes input commands to the 12.8-kHz clock and starts the character period and carriage return timers as required. Associated gating inhibits invalid commands (e.g., carriage return or backspace when the printhead is at the left margin).
- g. Column counter and decoder - stores and controls the printhead position. The counter counts up (module 3) to 81 as the head steps to the right and down to 0 as the head moves to the left during backspace or carriage return. The counter is cleared to zero whenever the printhead is at the left margin. Decoder outputs select the head stepping motor phases to be energized, enable the end-of-line alarm, initiate the automatic carriage return from the right margin, and enable operation of the carriage return brake. An input/output list for the

printer control read-only-memory is shown in Table 3-4.1.

- h. Damping controller - provides closed loop control of printhead deceleration when stepping to the right or left to minimize acoustic noise and settling time. When triggered by a position sensor on the stepping motor assembly, a monostable momentarily applies power to the lagging phase of the stepping motor to develop the required retrotorque.
- i. Carriage return controller - receives pulses from a second position sensor (tachometer) on the head stepping motor and synchronizes them to the 12.8kHz clock to drive the column counter during carriage return. The sensor pulses are phased so that the head stepping motor is operated in a slewing (continuous rotation) rather than a controlled (stepping) mode. When the printhead has returned to column 12, the controller switches the column counter clock from the leading to the trailing edge of the tachometer pulse which then begins to decelerate the printhead.

The controller also checks for the absence of tachometer pulses which indicate premature stopping of the printhead. When this occurs the controller enters a "failsafe" mode, reducing power and supplying clocks at 20-msec intervals to return the printhead to the left margin. Failsafe carriage return is initiated automatically when power is switched on.
- j. Carriage return brake controller - provides closed-loop control of printhead deceleration as the head approaches the left margin, maintaining carriage return time and acoustic noise within specified limits independent of friction, temperature, and line voltage variations. The controller operates by integrating tachometer pulses, comparing the resulting voltage to a reference ramp voltage, and applying retrotorque current to the stepping motor when the difference exceeds a preset limit.
- k. Paper feed counter - controls power to the paper advance motor phases. Paper is advanced one line each time the counter cycles through its three-state sequence, sequentially energizing the three stepping motor phases.

3-4.3.2 Printer Control Timing Diagrams. Timing diagrams for various printer control functions are shown in Figures 3-4.2 through 3-4.6.

3-4.4 CHARACTER DECODING, ASCII/BAUDOT. The printer decode block diagram is shown in Figure 3-4.7. When a printer enable is detected, a flipflop is set to allow the system clock (SCLK) to clock data on the data bus into the data buffer. When the data has been clocked in, the SCLK is disabled and the pattern counter is enabled. The pattern counter clocks the pattern from the MOS character generator, and counts the number of patterns sent to the printhead buffer/driver. If the first pattern is a ONE, the character is a control character so the pattern is also clocked to the control decode. Printer control monitors the flipflop which tells if the character is a print character or a control character. When the printer decode tells the printer control to 'GO', printer control either prints the character in the printhead buffer/driver, or does the control function in the control decode register.

For ASCII operation, resistors R46 and R48 are installed; resistors R47, R49, and R53 are left open; and the ASCII character generator is used. For Baudot operation the Baudot character generator is used, resistor R47 is installed, and resistors R46 and R48 are left out. For Baudot U.S. figures, R49 is also installed, and R53 is open. For Baudot U.K. figures, R53 is installed, and R49 is open.

A flow chart for the character decoding is shown in Figure 3-4.8, and a timing diagram is shown in Figure 3-4.9. The ASCII code set is listed in Table 3-4.2, and the Baudot code set is listed in Table 3-4.3.

3-4.5 PRINTHEAD. The printhead consists of a matrix of 35 (5 x 7) separate elements and a diode on a monolithic chip. The chip is mounted on a heatsink and is connected to the Printhead Interface PC card with a flat cable connected to a PC board. Mounted on this board are the balance, slow, and fast resistors used by the printhead compensation circuit. The printhead is controlled by switching both (1) base drive to each element and (2) print voltage to the entire head (PVOLT). The diode voltage on the chip varies with temperature, and the compensation circuit uses this voltage to control print voltage (PVOLT). The balance, slow, and fast resistors are used to match the printhead characteristics to the compensation circuit.

3-4.5.1 Printhead Interface. The Printhead Interface PC card takes serial data (35 bits) from the character generator and converts it to parallel data with five 7-bit shift registers. Each bit is then buffered and sent to the proper element (base lead) on the printhead.

TABLE 3.4.1 PRINTER CONTROL READ ONLY MEMORY INPUT/OUTPUT

WORD	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇	Y ₈
	A	B	C	D	E									
0	L	L	L	L	L	L	H	L	L	H	H	L	L	H
1	H	L	L	L	L	L	L	H	L	H	L	H	L	H
2	L	H	L	L	L	L	L	L	H	H	L	L	H	H
3	H	H	L	L	L	L	L	L	L	H	H	L	L	H
5	H	L	H	L	L	L	L	H	H	H	L	H	L	H
6	L	H	H	L	L	L	L	L	L	L	L	L	H	L
7	H	H	H	L	L	L	L	L	L	H	H	L	L	H
8	L	L	L	H	L	L	H	L	L	H	L	L	H	H
9	H	L	L	H	L	L	L	H	L	H	H	L	L	H
10	L	H	L	H	L	L	L	L	H	H	L	H	L	H
11	H	H	L	H	L	L	L	L	L	H	H	L	L	H
12	L	L	H	H	L	L	H	L	H	H	L	L	H	H
13	H	L	H	H	L	L	L	H	H	H	H	L	L	H
14	L	H	H	H	L	L	L	L	L	L	L	H	L	L
15	H	H	H	H	L	L	L	L	L	H	H	L	L	H
16	L	L	L	L	H	L	L	H	H	L	H	L	L	H
17	H	L	L	L	H	L	L	L	L	H	L	H	L	H
18	L	H	L	L	H	L	H	L	L	H	L	L	H	H
19	H	H	L	L	H	L	L	L	L	H	H	L	L	H
20	L	L	H	L	H	L	L	H	L	H	H	L	L	H
21	H	L	H	L	H	L	L	L	H	H	L	H	L	H
22	L	H	H	L	H	L	H	L	H	H	L	L	H	H
23	H	H	H	L	H	L	L	L	L	H	H	L	L	H
24	L	L	L	H	H	L	L	H	H	L	H	H	L	H
25	H	L	L	H	H	L	L	L	L	H	L	H	H	H
26	L	H	L	H	H	L	H	L	L	H	H	L	H	H
27	H	H	L	H	H	L	L	L	L	H	H	L	L	H
28	L	L	H	H	H	L	L	H	L	H	H	H	L	H
29	H	L	H	H	H	L	L	L	H	H	L	H	H	H
30	L	H	H	H	H	L	H	L	H	H	H	L	H	H
31	H	H	H	H	H	L	L	L	L	H	H	L	L	H
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

L = low, H = high)

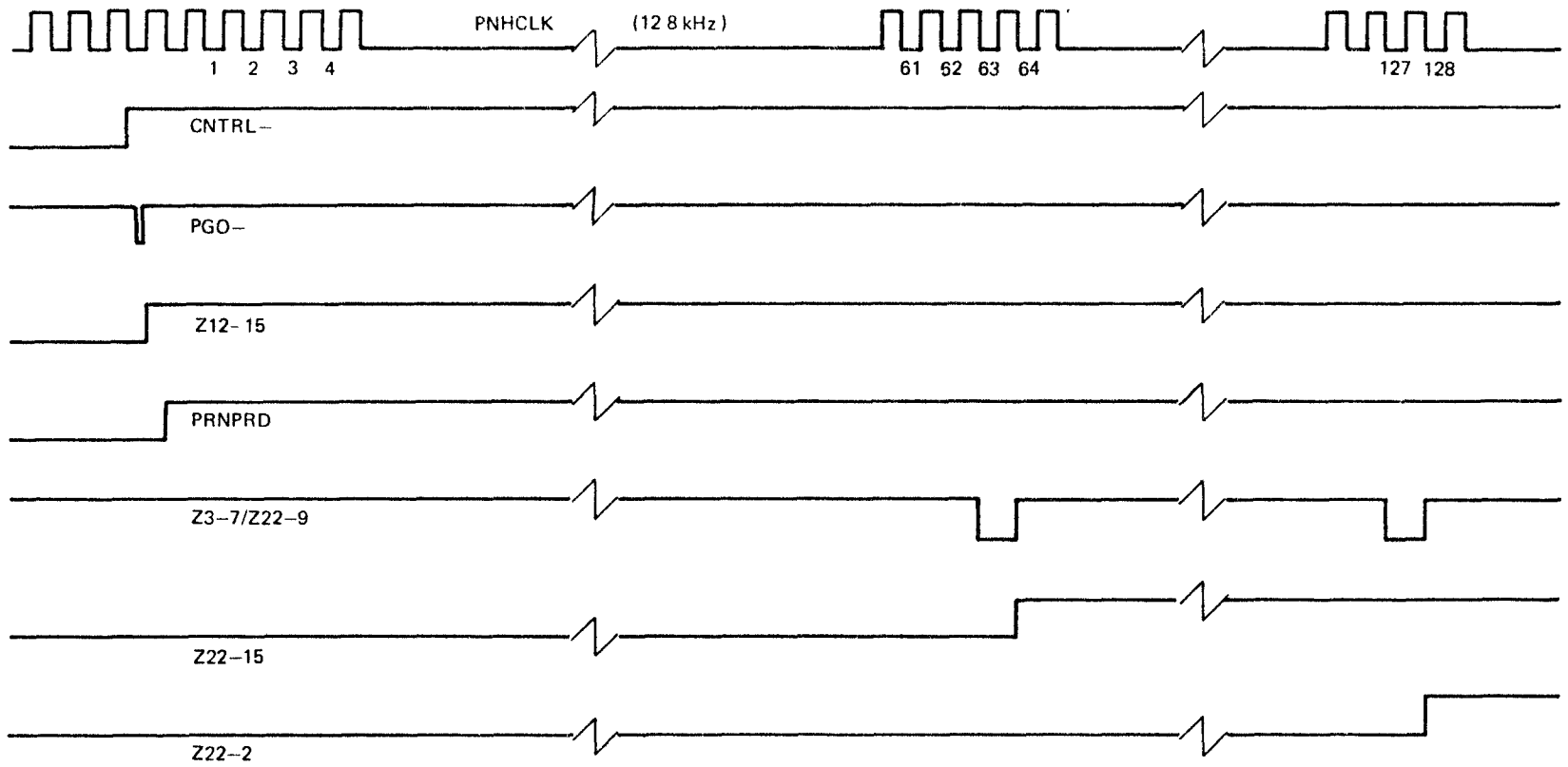


FIGURE 3-4.2. PRINTER CONTROL TIMING SYNCHRONIZATION

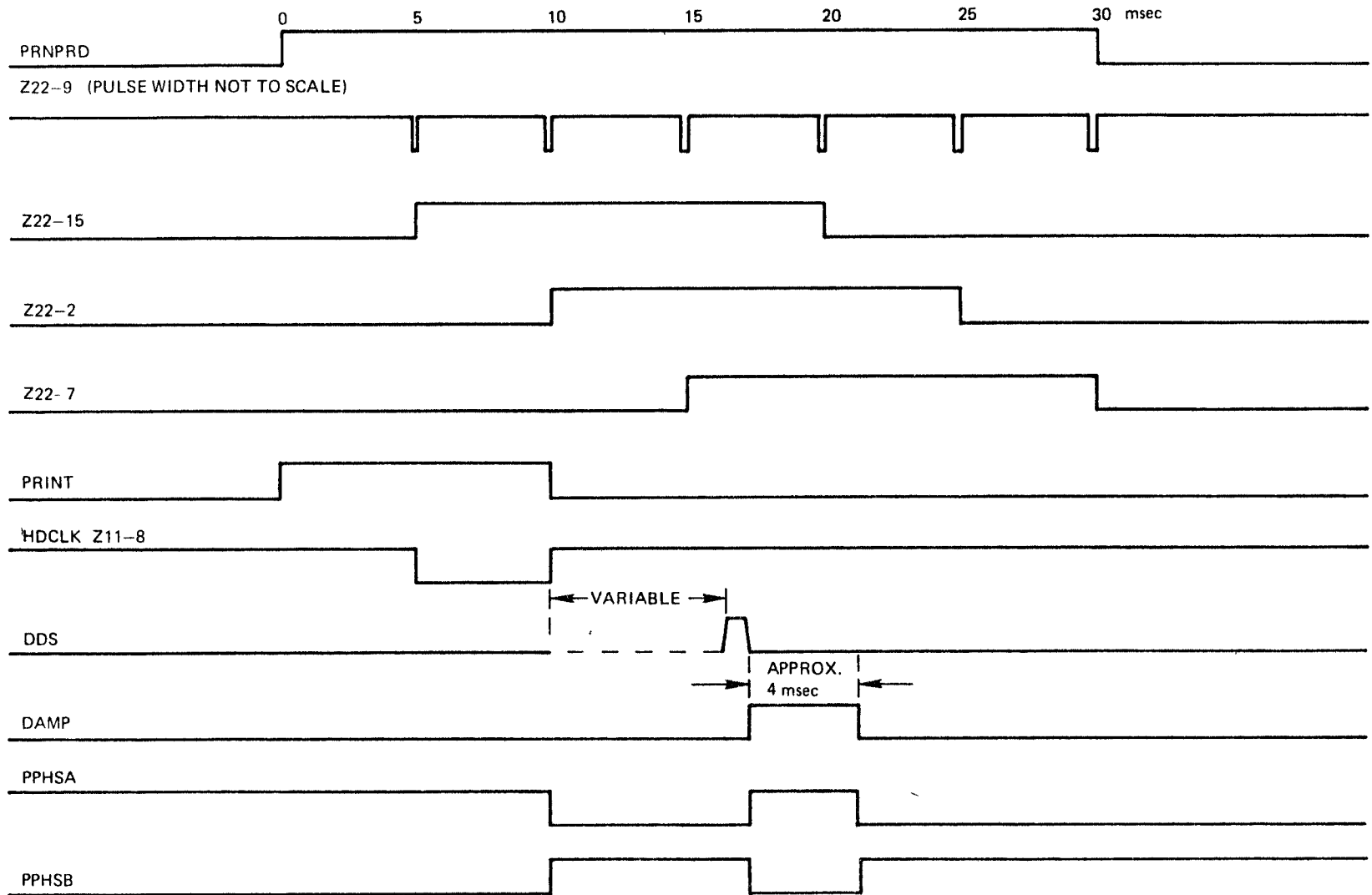


FIGURE 3-4.3. PRINTER CONTROL TIMING, PRINTING IN COLUMNS 1,4, ETC.

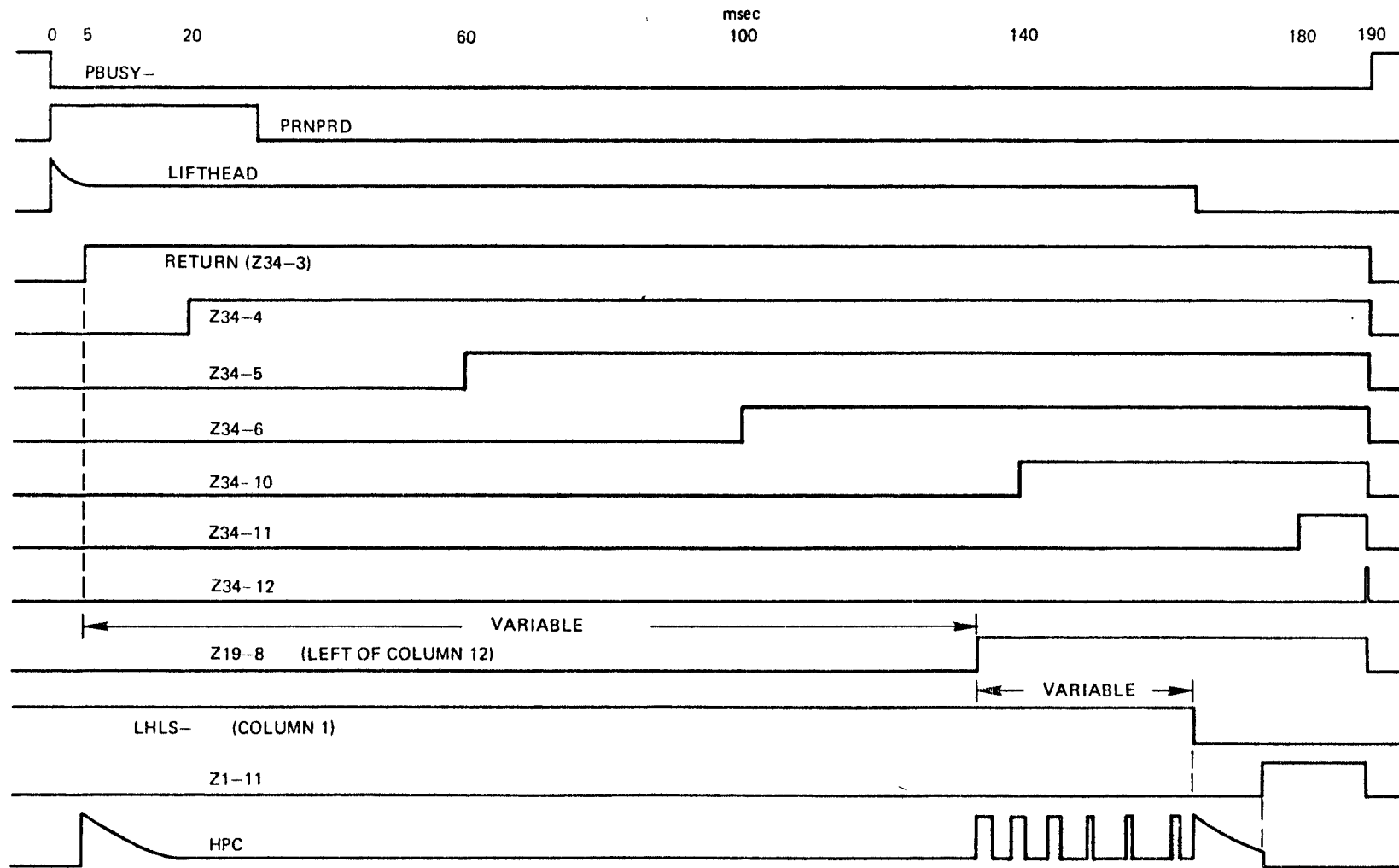


FIGURE3-4.4. PRINTER CONTROL, NORMAL CARRIAGE RETURN TIMING DIAGRAM

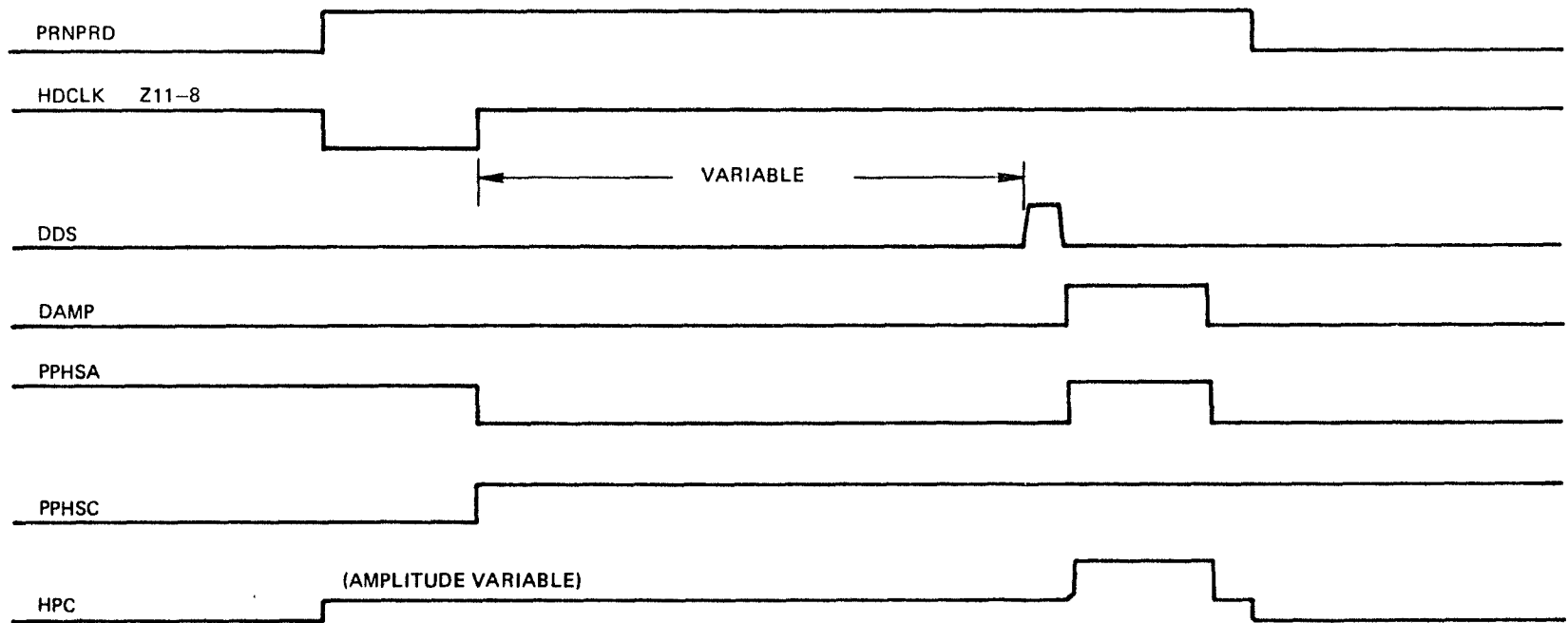


FIGURE 3-4.5. PRINTER CONTROL TIMING, BACKSPACE FROM COLUMNS 4, 8, ETC.

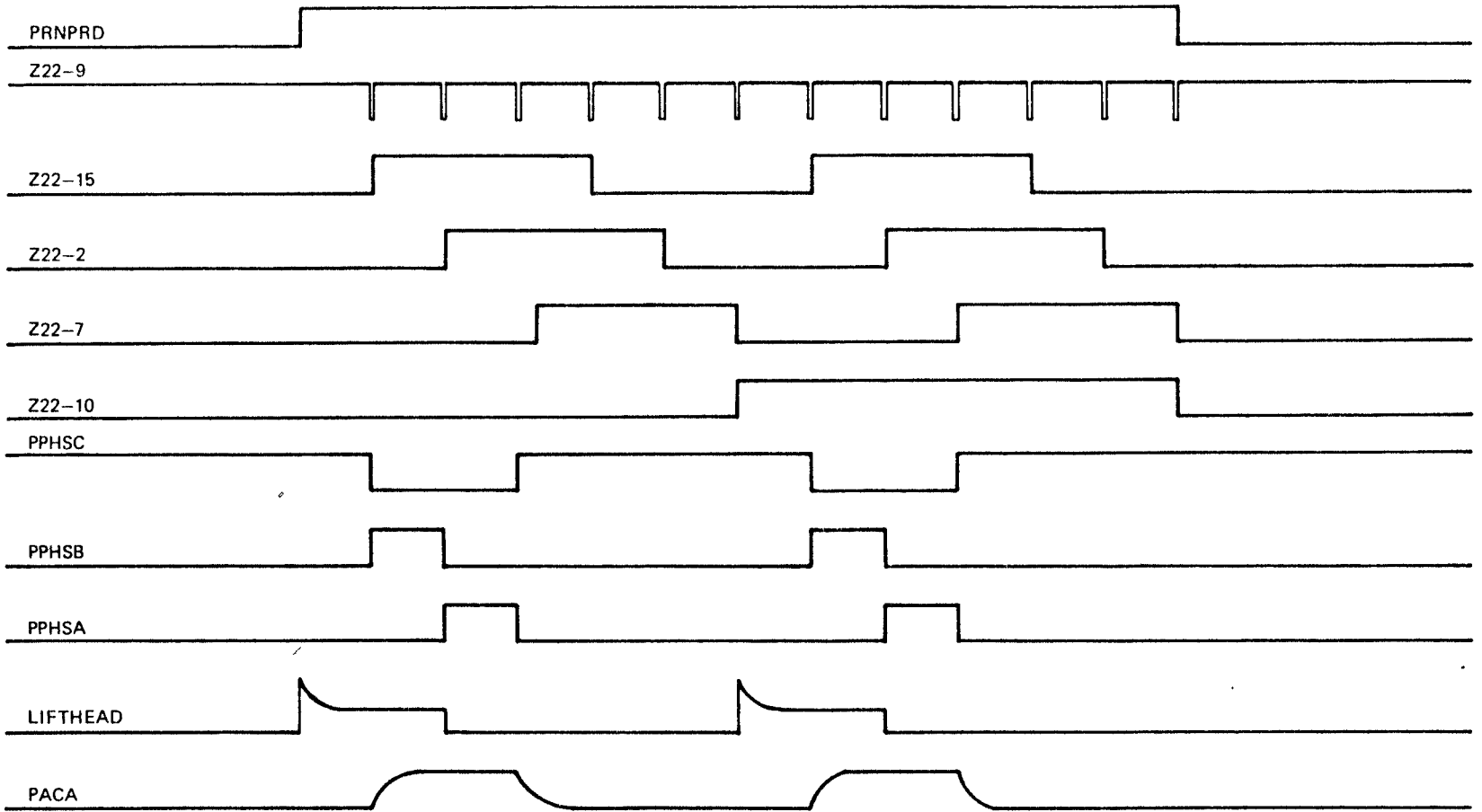


FIGURE 3-4.6. PRINTER CONTROL, LINE FEED TIMING DIAGRAM (DOUBLE LINE SPACING)

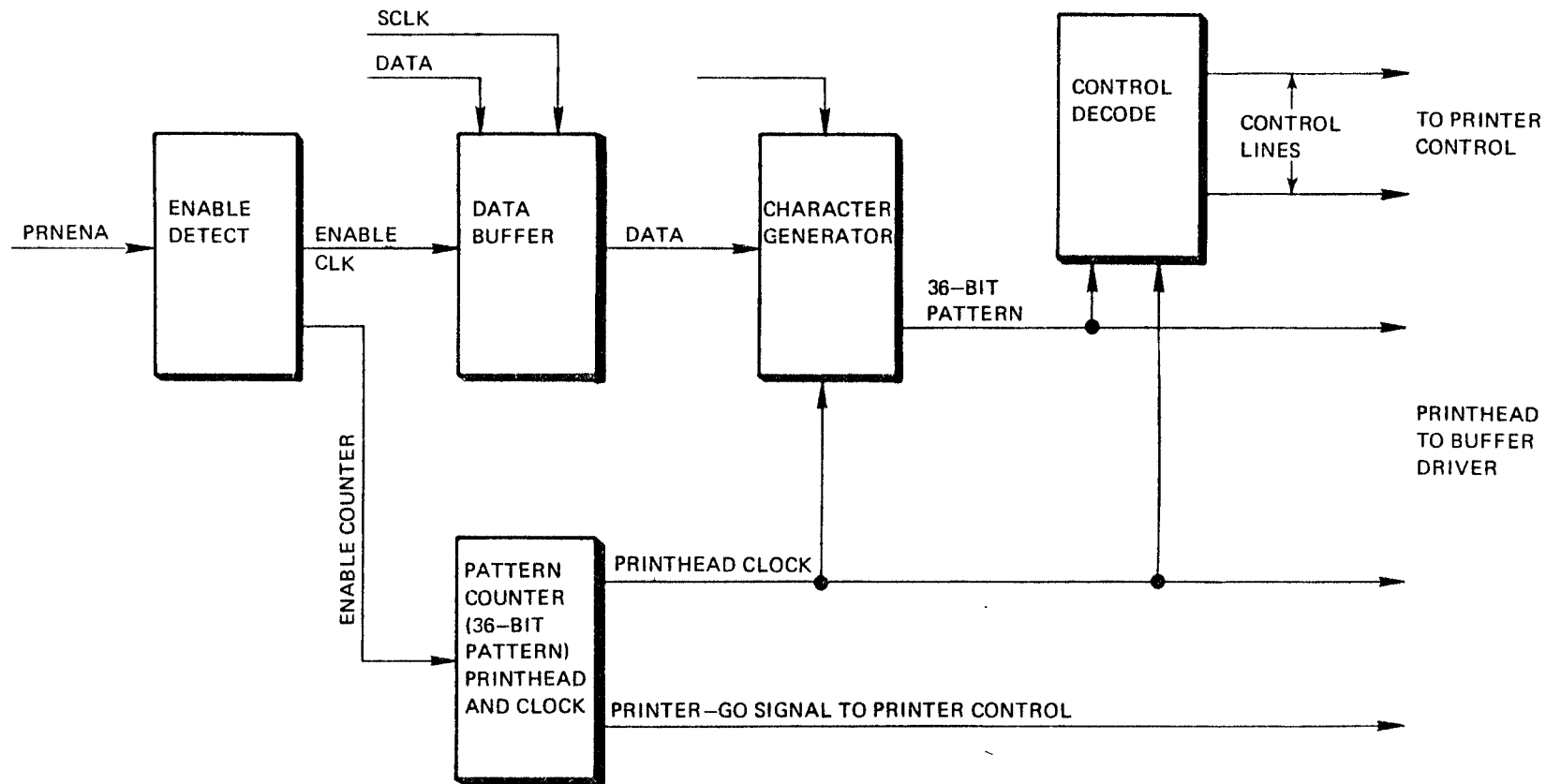


FIGURE 3-4.7. PRINTER DECODE BLOCK DIAGRAM

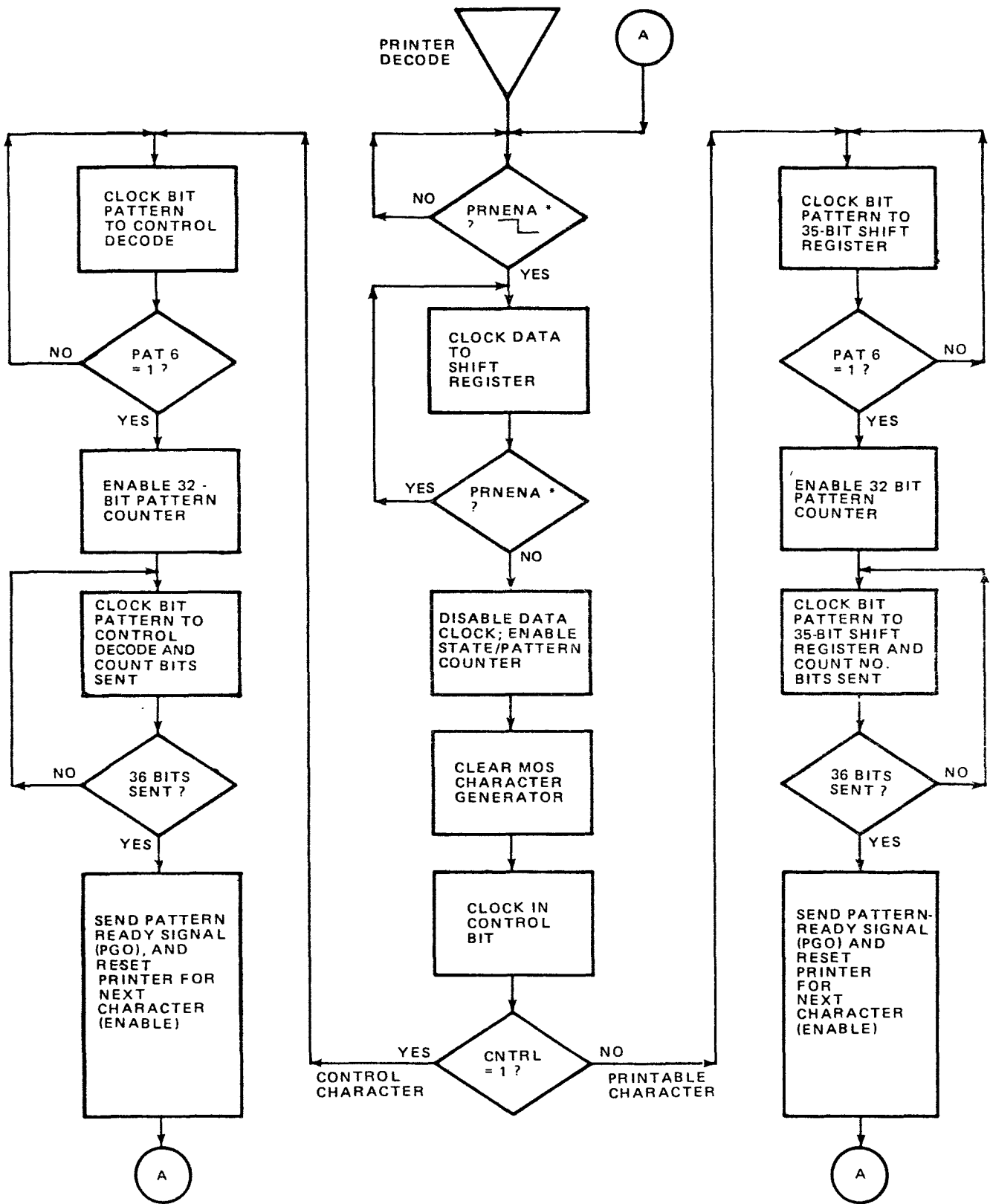


FIGURE 3-4.8. PRINTER CONTROL CHARACTER DECODING FLOW CHART

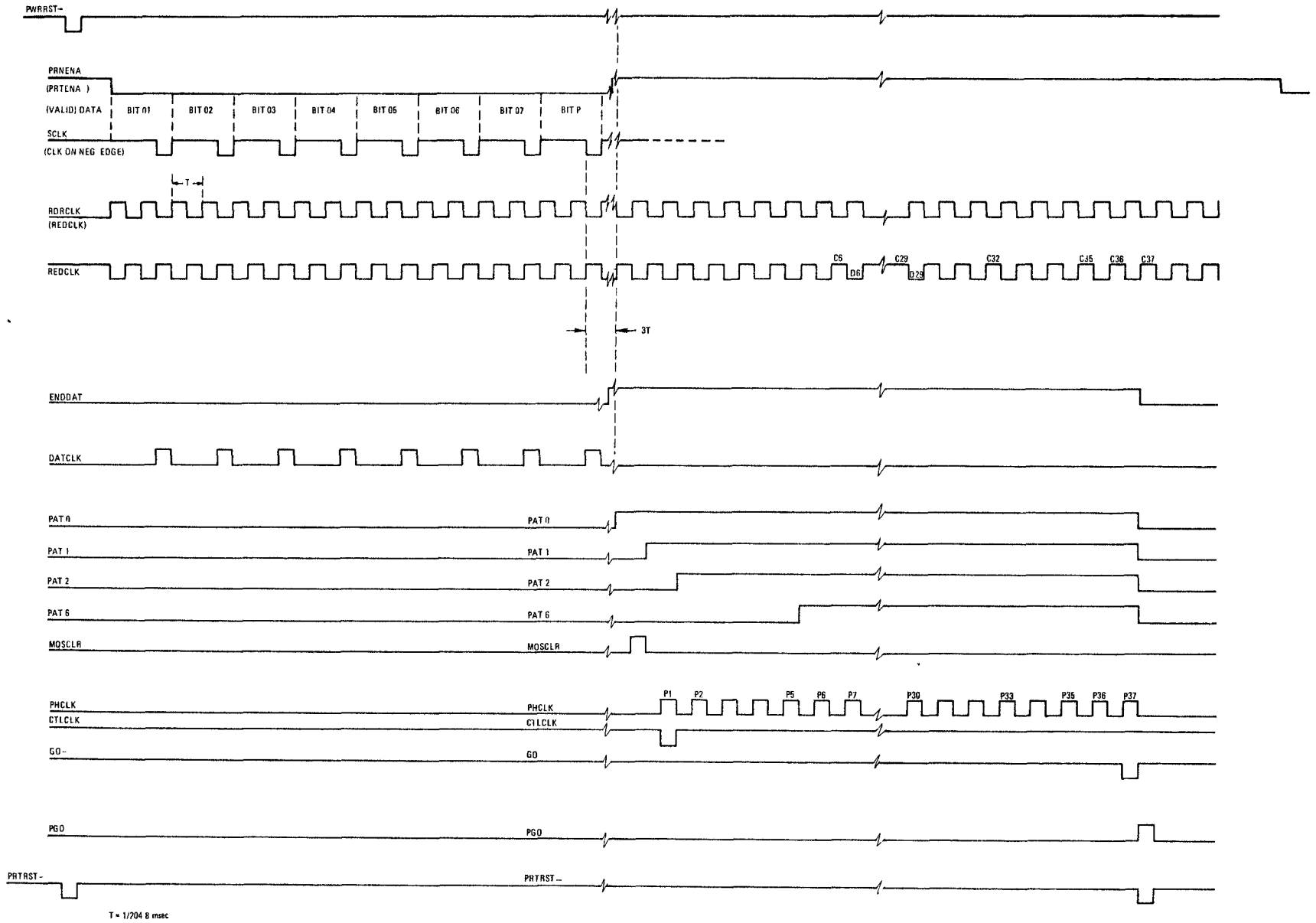
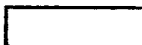





FIGURE 3-4.9. PRINTER CONTROL CHARACTER DECODING TIMING DIAGRAM

TABLE 3-4.2 ASCII CODE SYSTEM AND CHARACTER SET

b ₄ b ₃ b ₂ b ₁	b ₇ → 0	0	0	0	1	1	1	1
	b ₆ → 0	0	1	1	0	0	1	1
	b ₅ → 0	1	0	1	0	1	0	1
0 0 0 0	NUL	DLE	SPACE	0	@	P	`	p
0 0 0 1	SOH	DC1	!	1	A	Q	a	q
0 0 1 0	STX	DC2	"	2	B	R	b	r
0 0 1 1	ETX	DC3	#	3	C	S	c	s
0 1 0 0	EOT	DC4	\$	4	D	T	d	t
0 1 0 1	ENO	NAK	%	5	E	U	e	u
0 1 1 0	ACK	SYN	&	6	F	V	f	v
0 1 1 1	BEL	ETB	'	7	G	W	g	w
1 0 0 0	BS	CAN	(8	H	X	h	x
1 0 0 1	HT	EM)	9	I	Y	i	y
1 0 1 0	LF	SUB	*	:	J	Z	j	z
1 0 1 1	VT	ESC	+	;	K	[k	{
1 1 0 0	FF	FS	,	<	L	\	l	
1 1 0 1	CR	GS	-	=	M]	m	}
1 1 1 0	SO	RS	.	>	N	^	n	~
1 1 1 1	SI	US	/	?	O	_	o	DEL

 PRINTABLE CHARACTER
  AUXILIARY DEVICE CONTROL CHARACTER
 PRINTER CONTROL CHARACTER
  CODES GENERATED BY KEYBOARD, BUT NO ACTION TAKEN

USASCII CONTROL CHARACTERS
(From USA Standards Institute Publication X3.4-1968)

- | | | | |
|------|---------------------------|-----|-----------------------|
| ACK | acknowledge | ETX | end of text |
| BEL | bell | FF | form feed |
| BS | backspace | FS | file separator |
| CAN | cancel | GS | group separator |
| CR | carriage return | HT | horizontal tabulation |
| DC1 | device control 1 | LF | line feed |
| DC2 | device control 2 | NAK | negative acknowledge |
| DC3 | device control 3 | NUL | null |
| DC4 | device control 4 (stop) | RS | record separator |
| *DEL | delete | SI | shift in |
| DLE | data link escape | SO | shift out |
| EM | end of medium | SOH | start of heading |
| ENO | enquiry | STX | start of text |
| EOT | end of transmission | SUB | substitute |
| ESC | escape | SYN | synchronous idle |
| ETB | end of transmission block | US | unit separator |
| | | VT | vertical tabulation |


*not strictly a control character

TABLE 3-4.3 BAUDOT CODE SYSTEM AND CHARACTER SET

NOTE

Essentially two character sets (U. S. and U. K.) are accommodated. Both character sets are printed as described in Paragraph 3-4.4.

Bits					Letters U. S. & U. K.	Figures	
b5	b4	b3	b2	b1		U. S.	U. K.
0	0	0	0	1	E	3	3
0	0	0	1	0	LINE FEED	LINE FEED	LINE FEED
0	0	0	1	1	A	-	-
0	0	1	0	0	SPACE	SPACE	SPACE
0	0	1	0	1	S	!	!
0	0	1	1	0	I	8	8
0	0	1	1	1	U	7	7
0	1	0	0	0	CAR RET	CAR RET	CAR RET
0	1	0	0	1	D	*	*
0	1	0	1	0	R	4	4
0	1	0	1	1	J	BELL	BELL
0	1	1	0	0	N	,	,
0	1	1	0	1	F	\$	%
0	1	1	1	0	C	:	:
0	1	1	1	1	K	((
1	0	0	0	0	T	5	5
1	0	0	0	1	Z	"	+
1	0	0	1	0	L))
1	0	0	1	1	W	2	2
1	0	1	0	0	H	#	£
1	0	1	0	1	Y	6	6
1	0	1	1	0	P	0	0
1	0	1	1	1	Q	1	1
1	1	0	0	0	O	9	9
1	1	0	0	1	B	?	?
1	1	0	1	0	G	&	@
1	1	0	1	1	FIGS	FIGS	FIGS
1	1	1	0	0	M	.	.
1	1	1	0	1	X	/	/
1	1	1	1	0	V	;	-
1	1	1	1	1	LTRS	LTRS	LTRS

 Nonprinting characters

3-4.5.2 Printhead Compensation Circuit. The Printhead Compensation Circuit and printhead driver transistors are located on the Printer Code PC card (see schematic 959178, in Appendix C). These circuits ensure that the proper voltage is applied to the printhead (PVOLT).

Current for the printhead drivers is provided by a constant current source consisting of Q6 and CR6. This source provides current for printhead driver transistors Q7 and Q9. The PVOLT output voltage is controlled by the voltage compensation circuit which adjusts the voltage by sinking a portion of the current available for PVOLT drive. This current consists of two operational amplifier circuits AR2 and AR3. AR3, an OP AMP which sinks current, has two negative inputs: one from the slow printing bias circuit and the other negative input from the gain feedback loop. The slow printing bias is set by choosing the slow resistor on the printhead. This sets PVOLT to the proper level for slow printing (1 char/sec) for this particular printhead. The gain feedback loop consists of resistor R35 and variable resistor R36. R36 acts as a contrast adjustment, capable of changing gain of this stage from 15 to 50. The positive input to AR3 becomes effective when the printer is operating at fast printing speeds.

The operational amplifier AR2 is used as a sensing amplifier for the printhead temperature compensation diode. This amplifier is set for a gain of 30. A resistor divider R14 and R15 hold the negative input to a constant reference voltage. The voltage of the printhead diode is applied to the positive input. This diode is provided with 1 mA current from the 9V reference voltage through R12 and the balance resistor R4 located on the printhead. The balance resistor is chosen at room temperature to ensure that all printheads have the same diode voltage at room temperature. When the printhead is not printing (PRINT is low), Q1 and Q2 turn on FET Q13. This allows capacitor C4 to charge up to the diode voltage (DVOLT). When the print command is given,

Q2 will turn off Q13, and capacitor C4 will be isolated to retain the DVOLT level during the 10 msec printing time.

When printing, the temperature of the diode rises quickly and falls quickly. When printing slow, the diode has time to return to ambient temperature. In this condition the output of AR2 is zero, and the gain of AR3 is controlled exclusively by the slow resistor. When the printer is running fast, the temperature of the printhead rises, causing the diode voltage to drop. This change is amplified by AR2, enabling the fast resistor which controls the gain of AR3. Thus, as the ambient temperature of the head increases, the print voltage is decreased proportionately.

When the print command is low, transistors Q3 and Q4 clamp PVOLT to ground through CR7 and CR8. If the print command stays high too long (longer than 11-12msec) one-shot Z19 will time out, and the buffers on the Printhead Interface PC card will be cleared (PHBFRCLR), removing the base drive from the head. Overvoltage protection for the printhead is provided by CR9, CR10, CR11, and Q8. If PVOLT rises high enough for CR9 and CR10 to conduct, Q8 will generate PHBFRCLR which removes the base drive to the head. At the end of each print pulse, Z22 generates PHBFRCLR to remove base drive from the head. A timing diagram is shown in Figure 3-4.10.

Current regulation to the head is provided by R30 and Q5. This limits the short-circuit current of PVOLT to less than 3.5 amps.

Reference voltages for the compensation circuits are provided by voltage regulator AR1. Resistor R9 is selected to produce the correct reference voltage (approximately 9.0 volts). The bell driver also is located on the Printer Code PC card. When the head reaches column 72 or the BEL character is received, a one-shot is fired. This gates the bell clock (3.2kHz) to transistor A10 and applies a 3200-Hz tone to the speaker.

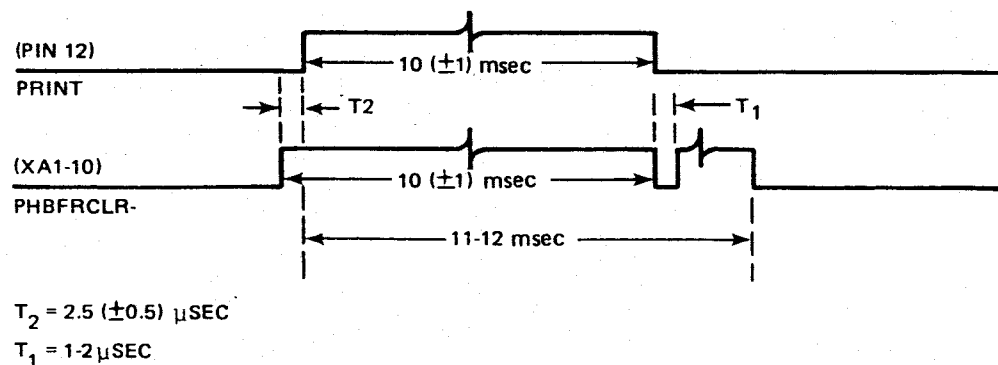


FIGURE 3-4.10. PRINTHEAD BUFFER CLEAR (PHBFRCLR) TIMING DIAGRAM

3-5 KEYBOARDS AND KEYBOARD INTERFACE.

The keyboard used in the data terminals is a fully encoded, alphanumeric keyboard with two-key rollover. The interface for the keyboards is located on the Printer Code PC card (see schematic 959178 for both ASCII and Baudot). A block diagram of the keyboard interface is shown in Figure 3-5.1. A flow chart and a timing diagram are shown in Figures 3-5.2 and 3-5.3.

Upon detection of a keyboard strobe, the parallel keyboard data is loaded into the data buffer, and the strobe flipflop is clocked. The keyboard interface then sends a keyboard request (KBDREQ) to terminal control and waits for a keyboard enable (KBDENA). Keyboard interface uses this enable and eight system clocks (SCLK) to transmit the character serially to the data bus. When this is done, the repeat key (REPEAT) is checked, and a flipflop is set to remember the state of the repeat key. The interface then checks for another strobe; if there is no strobe but the REPEAT key is depressed, another request will be generated and the same character will be retransmitted. This will continue until there is a strobe or until the REPEAT key is released. If the REPEAT key is on and a new keyboard strobe is received, the new character will be loaded into the data buffer, and it will then be transmitted as before. When there is no REPEAT key signal, only one character will be transmitted for each keyboard strobe (depression of a key).

A state counter determines the sequence of operations as shown in Figures 3-5.2 and 3-5.3.

Any time the ASR control panel keyboard LINE/OFF/LOCAL switch is in the OFF position, the keyboard interface will be held in the reset position and will not accept strobes. Since the keyboard outputs only 7

bits and the terminal requires 8 bits on the serial bus, the eighth (parity bit) is hardwired on the motherboard to be the same as bit 1. Therefore, on all data from the keyboard, the eighth bit will be the same as bit 1 when clocked on the internal serial data bus. However, the record control or transmitter may change this arrangement.

3-5.1 STANDARD ASCII. The output of the standard ASCII keyboard is serial by character and parallel by bit. There are seven data bits and a strobe pulse; no parity is generated by the keyboard. The strobe pulse is shown in Figure 3-5.4 relative to a typical data bit. The ASCII codes generated are shown in Table 3-4.2.

All signal outputs are TTL-compatible (data and strobe). The outputs of the special function keys, except TAPE and TAPE, are isolated single-contact closures to ground. The TAPE and TAPE keys are debounced, and the output from these keys is a TTL-compatible pulse. These outputs are normally at a logic ONE. The special function keys are:

- a. HERE IS
- b. PAPER ADV (Advance)
- c. BREAK
- d. REPEAT
- e. TAPE
- f. TAPE

Pin assignments for the standard keyboard connector (inside connector) are listed in Table 3-5.1.

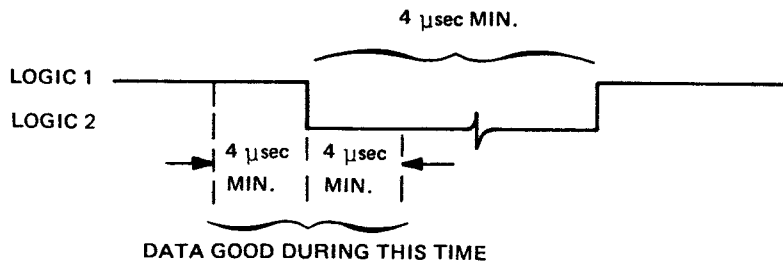


FIGURE 3-5.4. KEYBOARD STROBE PULSE

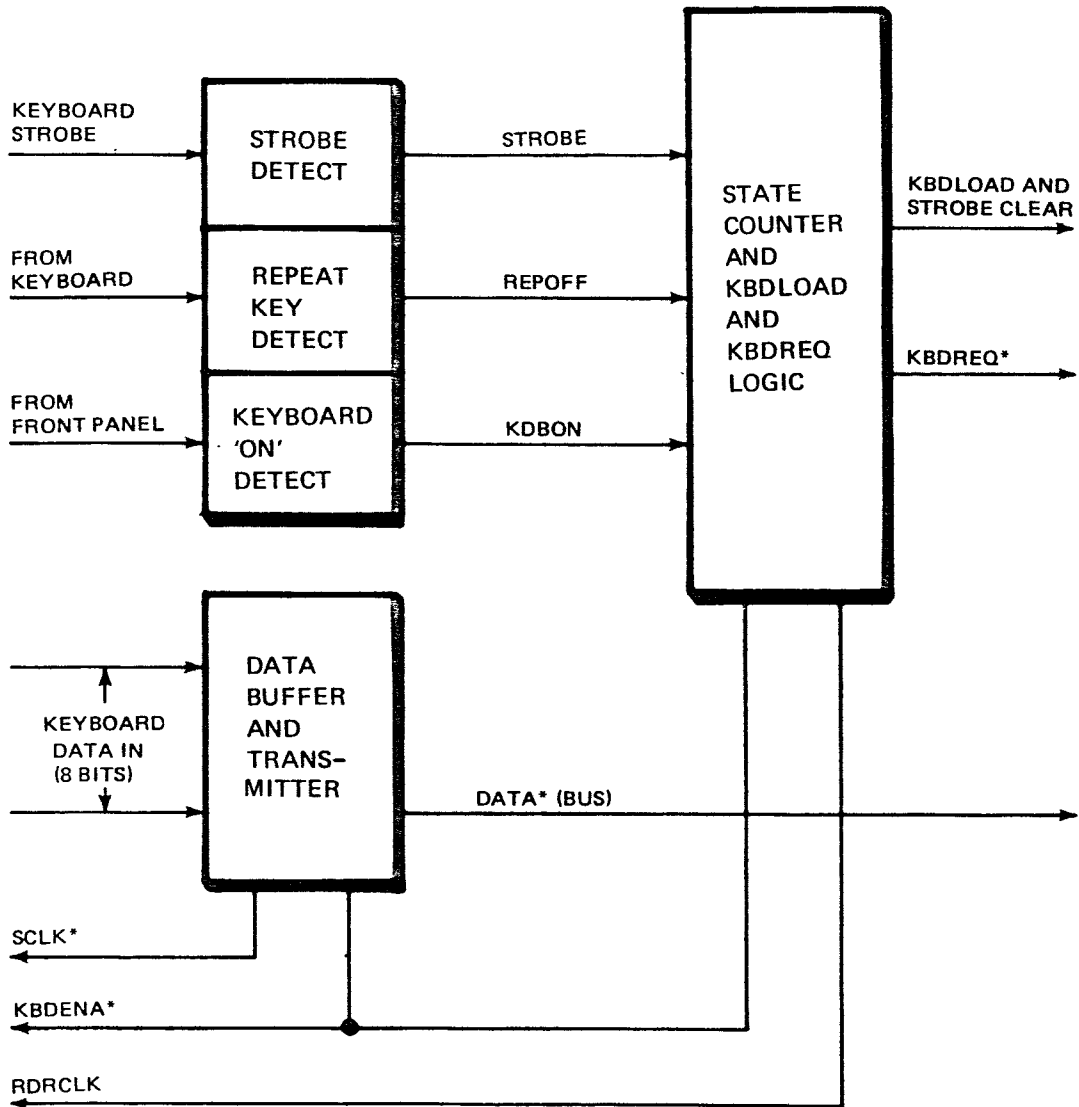


FIGURE 3-5.1. KEYBOARD INTERFACE BLOCK DIAGRAM

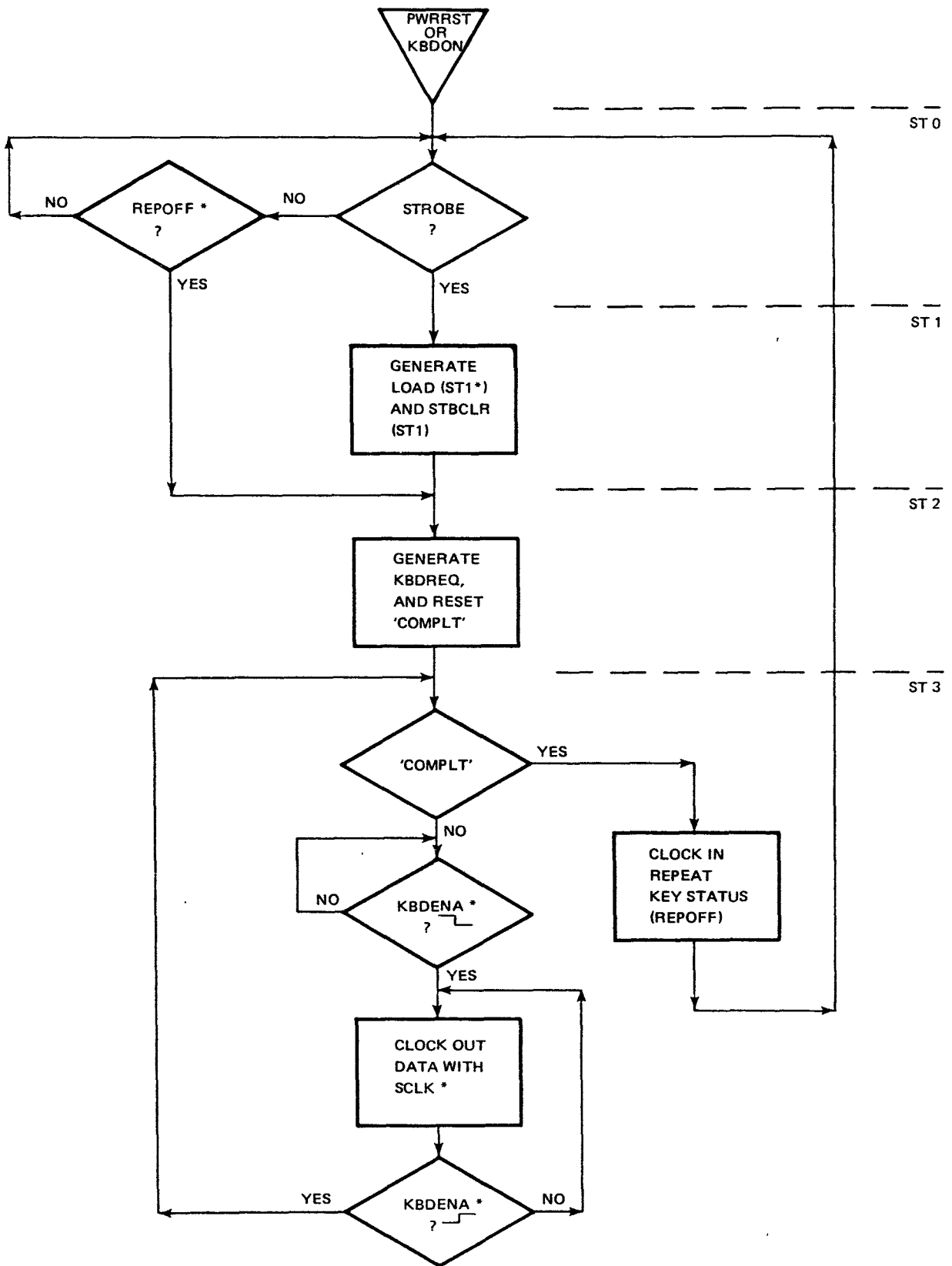


FIGURE 3-5.2. KEYBOARD INTERFACE STATE FLOW DIAGRAM

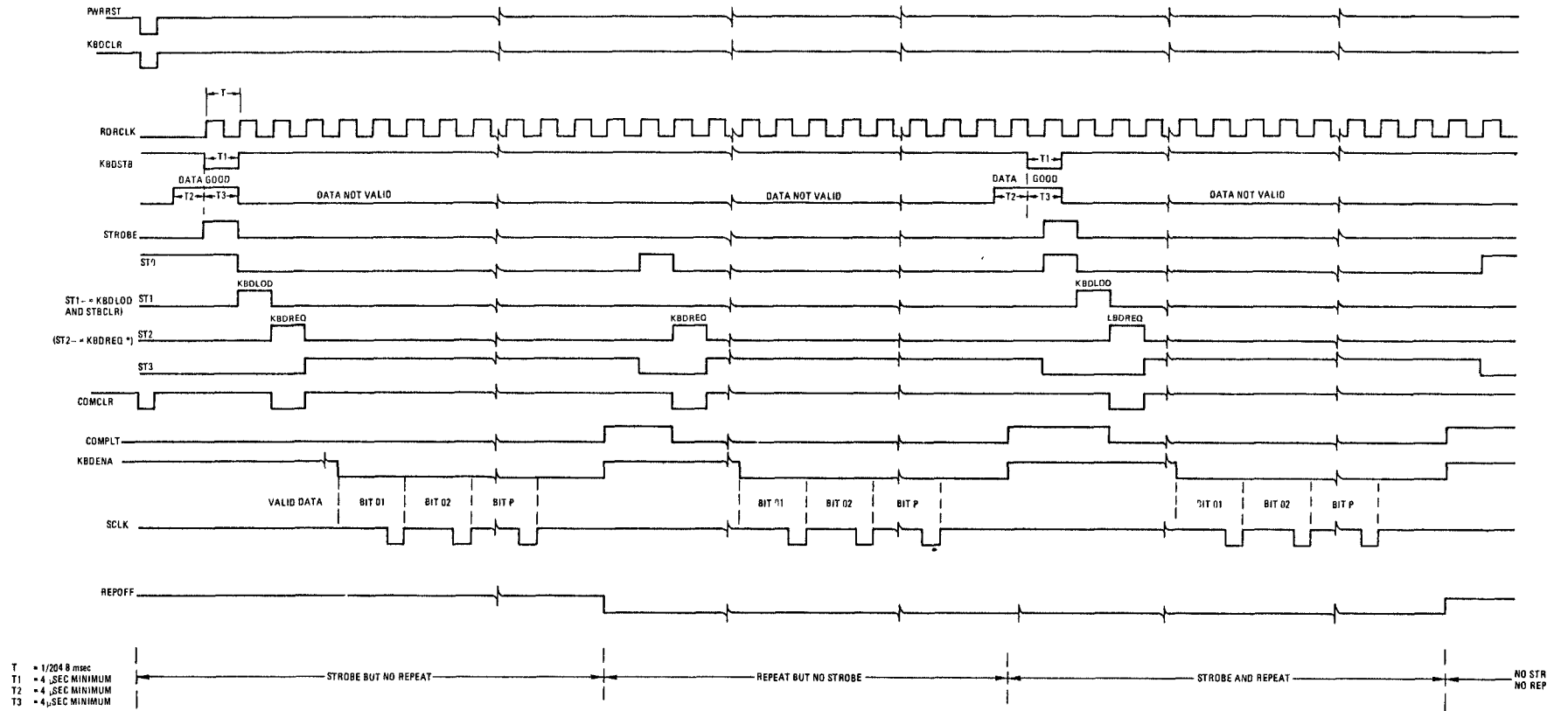


FIGURE 3-5.3. TIMING DIAGRAM KEYBOARD INTERFACE

TABLE 3-5.1. STANDARD KEYBOARD CONNECTOR PIN ASSIGNMENTS

Pin Number	Signal	Pin Number	Signal
1	BIT 6 (Data)	A	BIT 7 (Data)
2	SPEED (Direct Connection to Switch Connector)	B	BIT 5 (Data)
3	BIT 1 (Data)	C	BIT 2 (Data)
4	BIT 3 (Data)	D	
5	REPEAT (Special Function Output)	E	BREAK (Special Function Output)
6	TAPE (Special Function Output)	F	ON LINE (Direct Connection to Switch Connector)
7	TAPE (Special Function Output)	H	STROBE PULSE
8	GROUND	J	HERE IS (Special Function Output)
9	+5V Power	K	PAPER ADVance: (Special Function Output)
10	-12V Power	L	CLOCK (For Debounce Circuit)

Standard ASCII keyboard layout and symbolization are shown in Figure 3-5.5. The character set is shown in Figures 3-5.6 through 3-5.9.

3-5.2 UPPERCASE/LOWERCASE ASCII KEYBOARD. The Uppercase/Lowercase (full) ASCII keyboard is the same as the standard ASCII keyboard (see Section 3-5.1) except the uppercase/lowercase keyboard generates either uppercase or lowercase codes, depending on the position of the UPPERCASE key. Full ASCII keyboard layout and symbolization are shown in Figure 3-5.10. ASCII codes generated are listed in Table 3-4.2. The full ASCII keyboard character set is shown in Figures 3-5.11 through 3-5.13.

3-5.3 BAUDOT KEYBOARD. The Baudot keyboard is the same as the standard ASCII keyboard except the Baudot keyboard generates a 5-bit Baudot code instead of the ASCII code. The additional tab area used for numeric entry on the standard ASCII-type keyboard is used only as a connection for the ON-LINE switch (connects to pin H) on the Baudot-type keyboard (pins 7 and 8 are still grounded).

The Baudot keyboard layout and symbolization are shown in Figure 3-5.14. The Baudot codes generated for the keys shown in Figure 3-5.15 are listed in Table 3-4.3.

3-5.4 CALCULATOR NUMERIC CLUSTER ASCII KEYBOARD. The calculator numeric cluster keyboard is the same as the standard ASCII keyboard (see Section 3-5.1) except the calculator numeric cluster keyboard generates numeric codes when the NUM LOCK key is depressed and the HERE IS key function is not available. Calculator cluster ASCII keyboard layout and symbolization is shown in Figure 3-5.16. ASCII codes generated are listed in Table 3-4.2. The calculator cluster ASCII keyboard character set is shown in Figures 3-5.17 through 3-5.20.

3-6 TRANSMIT/RECEIVE PC CARD (EIA INTERFACE).

3-6.1 ASCII TRANSMIT/RECEIVE PC CARDS (300 BAUD MAXIMUM). Three versions of the ASCII Transmit/Receive PC card are available: the standard version (TI Part No. 959135*) and the optional dual-format version (TI Part No. 969455* or 973905). The dual-format version is equipped with strappable options which permit the Dual-Format Transmit/Receive PC card either to operate like the standard version (standard format) or to operate in binary format. The standard format operation of the PC cards is identical. Differences in binary-format operation are noted in the following description.

*This PC card is obsolete.

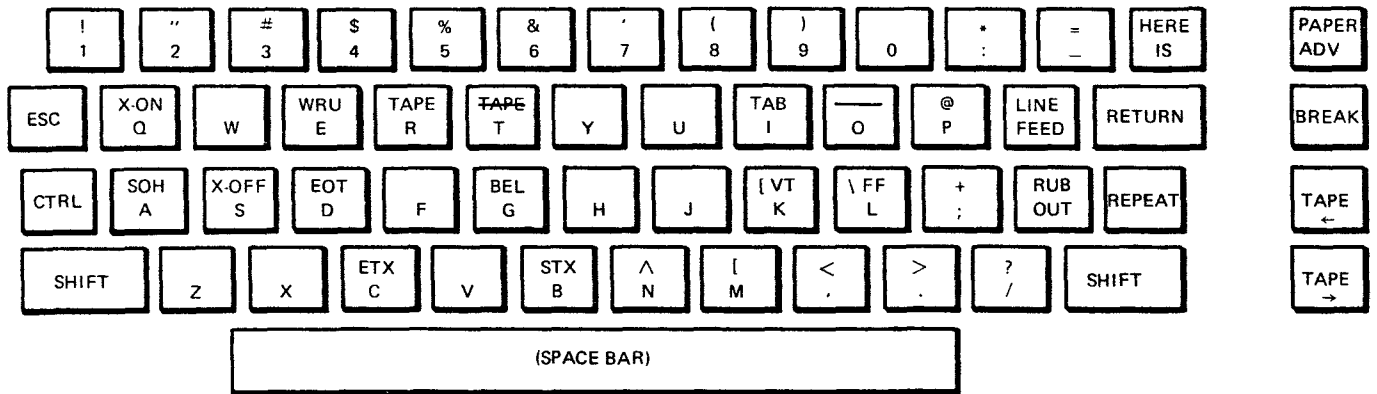
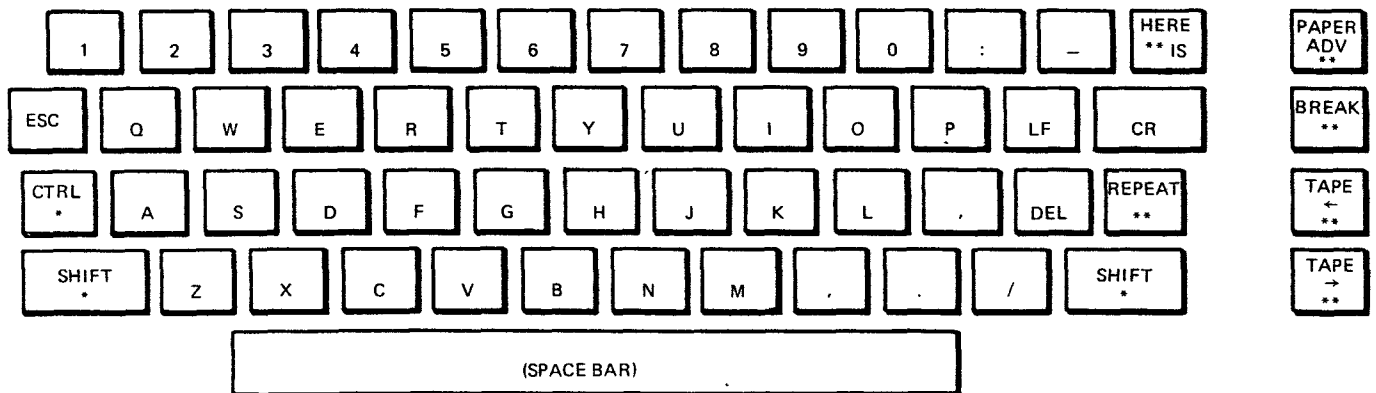
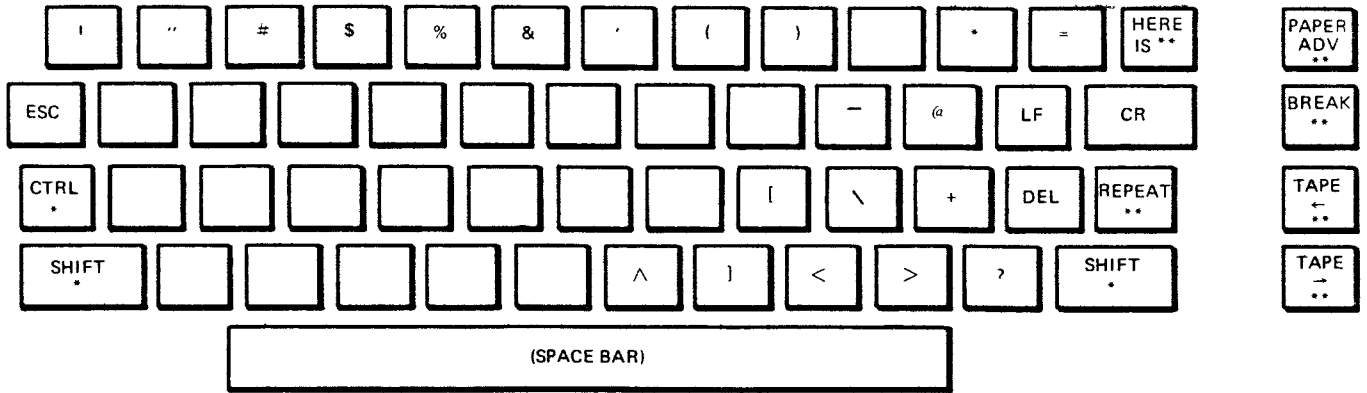


FIGURE 3-5.5. STANDARD ASCII KEYBOARD LAYOUT AND SYMBOLIZATION



- NOTES:
- * The above codes are generated when the labeled key is depressed, but neither the SHIFT nor the CONTROL (CTRL) key is depressed.
 - ** Not a code-generating key.

FIGURE 3-5.6. UNSHIFTED CHARACTERS, STANDARD ASCII KEYBOARD

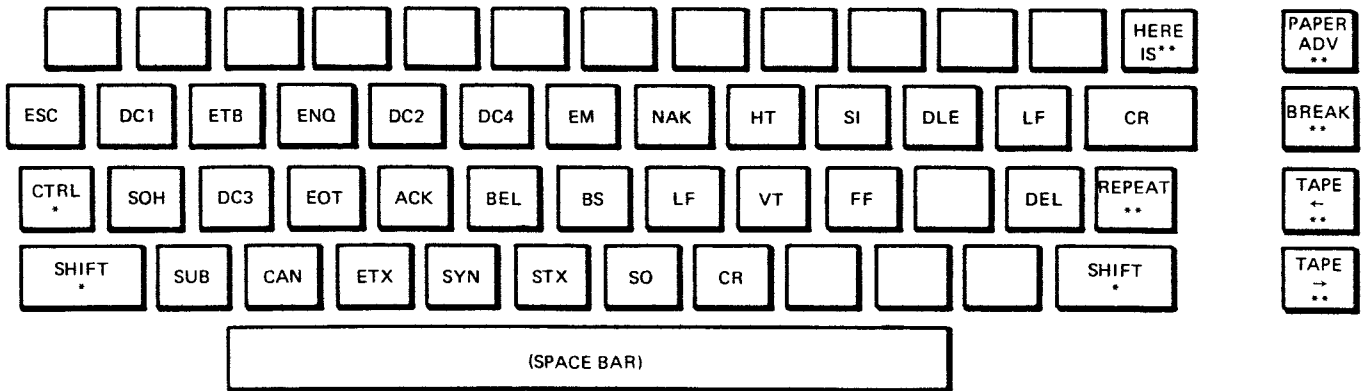


NOTES: * The above codes are generated when the labeled key and the SHIFT key are depressed, but the CONTROL(CTRL) key is not depressed.

** Not a code-generating key.

□ A blank key indicates strobe inhibit

FIGURE 3-5.7. SHIFTED CHARACTERS, STANDARD ASCII KEYBOARD

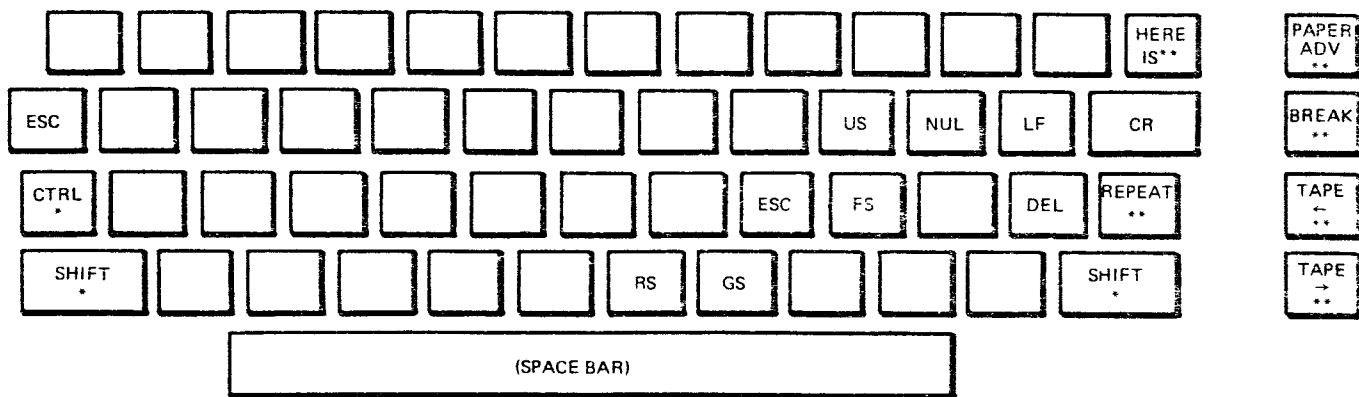


NOTES: * The above codes are generated when the labeled key and the CONTROL (CTRL) key are depressed, but the SHIFT key is not depressed.

** Not a code-generating key

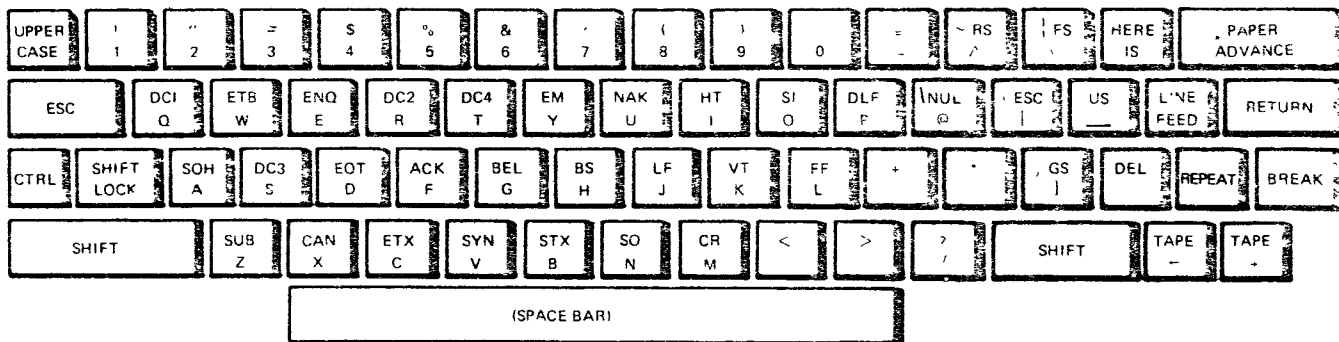
A blank key indicates strobe inhibit.

FIGURE 3-5.8. CONTROL CHARACTERS, STANDARD ASCII KEYBOARD



- NOTES:
- * The above codes are generated when the labeled key, the SHIFT key, and the control (CTRL) key are depressed.
 - ** Not a code-generating key.
- A blank key indicates strobe inhibited.

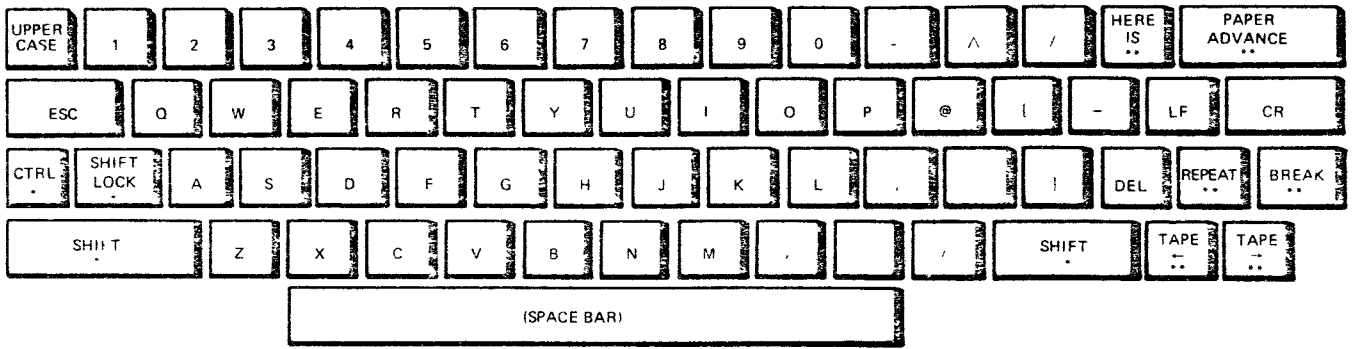
FIGURE 3-5.9. SHIFT AND CONTROL CHARACTERS, STANDARD ASCII KEYBOARD



LEGEND:

- SOH = Control Character
- A = Alphabetic character (SHIFT for uppercase)
- ! = Shifted character
- 1 = Unshifted character
- ~ RS = Shifted character, control character
- ^ = Graphic unshifted

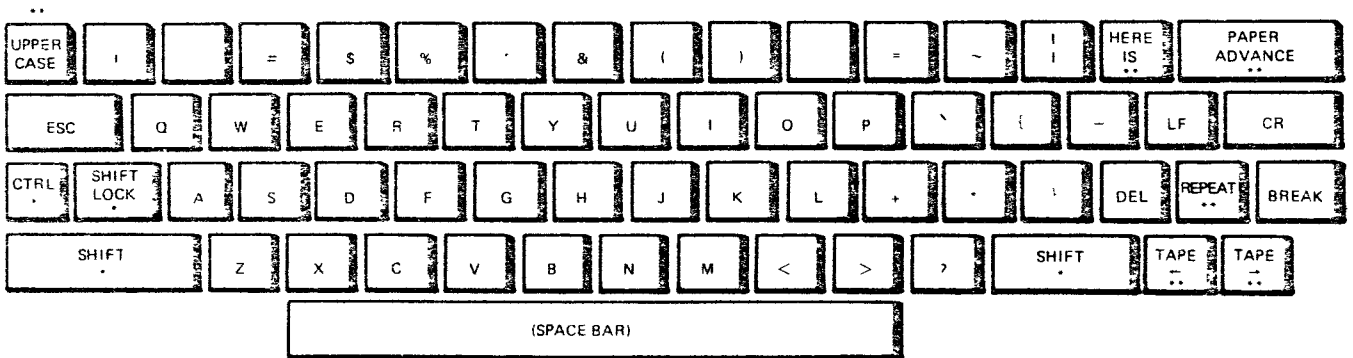
FIGURE 3-5.10. FULL ASCII KEYBOARD SYMBOLIZATION



NOTES:

- *The above codes are generated when the labeled key is depressed but neither the SHIFT nor the CTRL key is depressed.
- **Not a code generating key.
- ***If UPPER CASE is depressed, only upper case alphabet codes are generated, otherwise lower case alphabetic codes are generated.

FIGURE 3-5.11. LOWERCASE CHARACTERS, FULL ASCII KEYBOARD



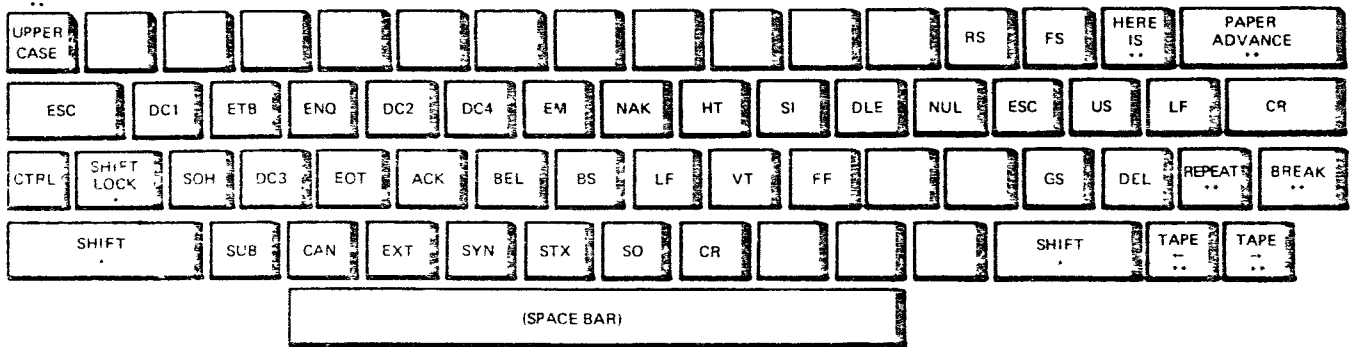
NOTES:

- *The above codes are generated when the labeled key and the SHIFT key are depressed. UPPER CASE has no effect.
- **Not a code generating key.



A blank key indicates strobe inhibit. Depressing SHIFT and CTRL keys together inhibits strobe.

FIGURE 3-5.12. SHIFTED CHARACTERS, FULL ASCII KEYBOARD



NOTES:

* The above codes are generated when the labeled key and the CTRL key are depressed. UPPERCASE and SHIFT keys have no effect.

** Not a code generating key.


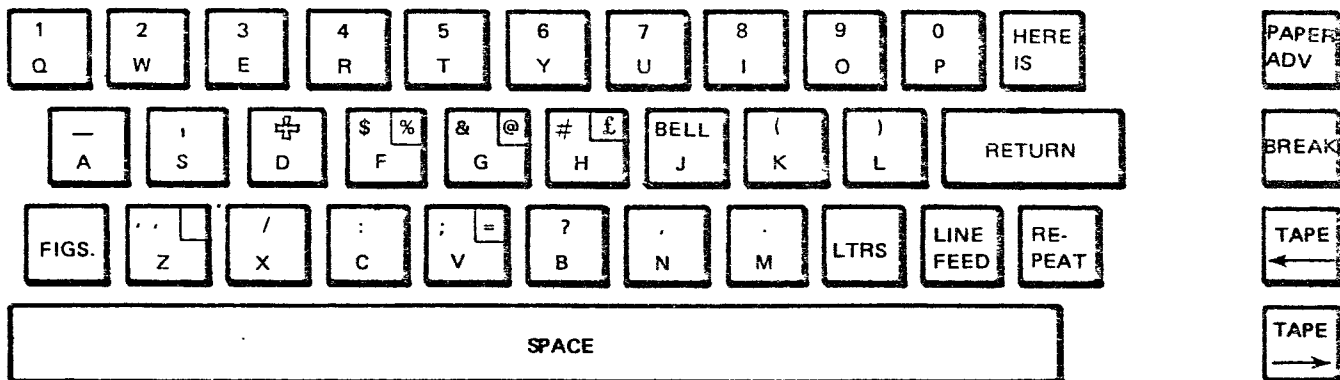
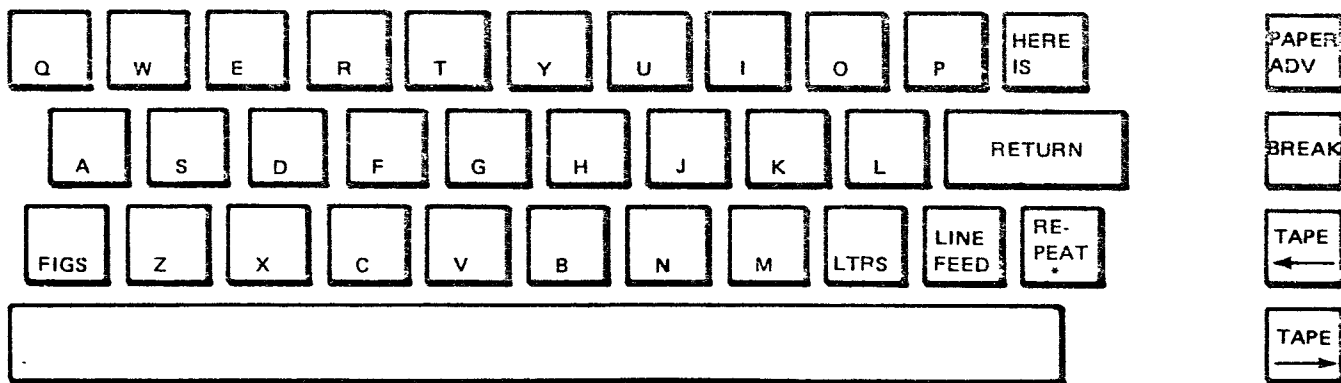
 A blank indicates strobe inhibit. Depressing SHIFT and CTRL keys together inhibits strobe.

FIGURE 3-5.13. CONTROL CHARACTERS, FULL ASCII KEYBOARD



When each key is depressed, the data terminal generates the indicated Baudot characters according to Table 3-3. U. S. figures are shown on upper lefthand surface of the keys, and U. K. figures are shown on upper righthand surface of the keys (where different). Printing of either figure set is a strappable option.

FIGURE 3-5.14. BAUDOT KEYBOARD



The Baudot codes corresponding to the above characters are generated when the LTRS and the labeled key is depressed.

* NOT A CODE-GENERATING KEY

FIGURE 3-5.15. BAUDOT LETTER MODE KEYBOARD CODES

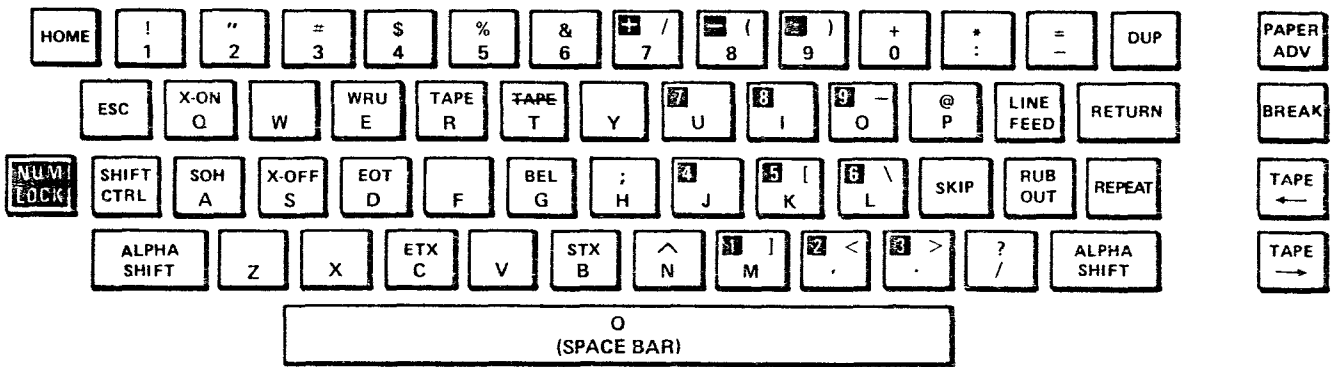
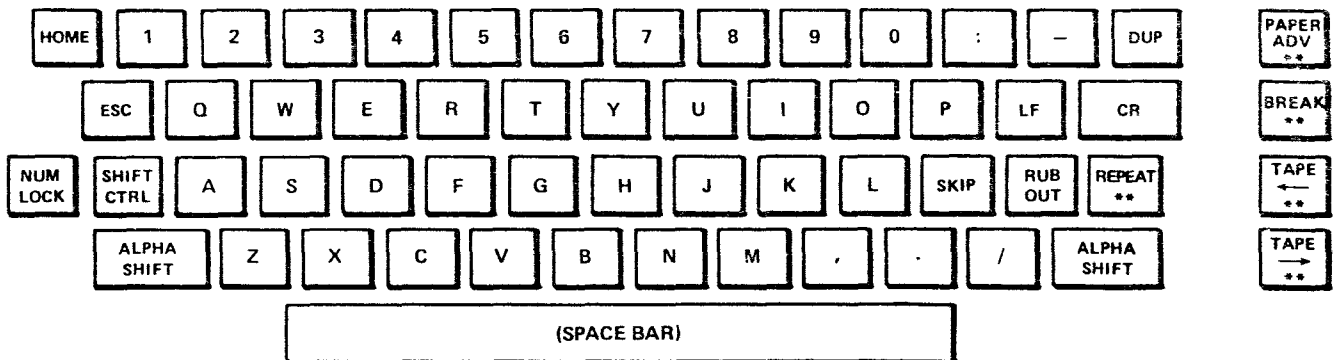


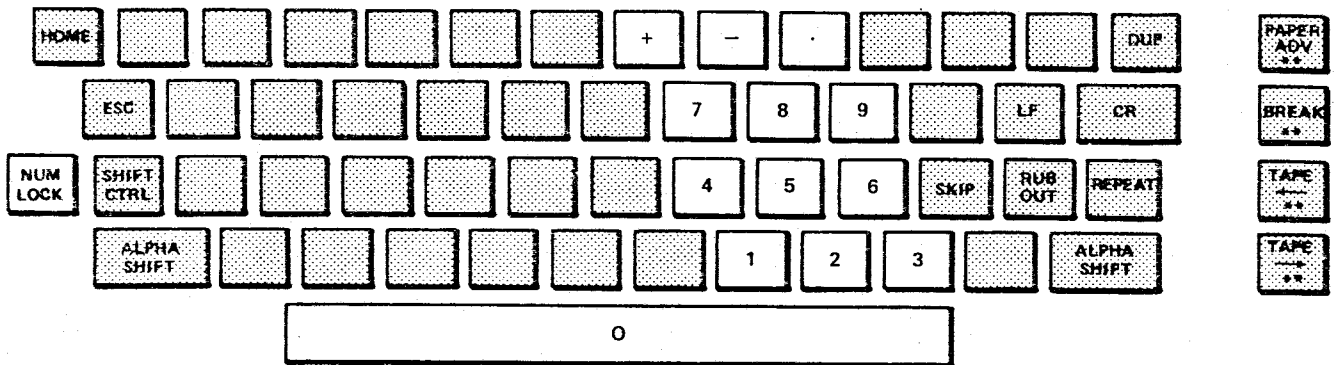
FIGURE 3-5.16. OPTIONAL LIMITED ASCII WITH CALCULATOR CLUSTER KEYBOARD LAYOUT AND SYMBOLIZATION



NOTES THE ABOVE CODES ARE GENERATED WHEN THE LABELED KEY IS DEPRESSED AND NEITHER NUM LOCK, SHIFT/CONTROL, OR ALPHA SHIFT IS DEPRESSED OR WHEN BOTH NUM LOCK AND ALPHA/SHIFT BUT NOT SHIFT/CONTROL IS DEPRESSED

** INDICATES THAT IT IS NOT A CODE GENERATING KEY

FIGURE 3-5.17. UNSHIFTED CHARACTERS, CALCULATOR CLUSTER KEYBOARD



NOTES: THE ABOVE CODES ARE GENERATED WHEN THE LABELED KEY AND THE NUM LOCK IS DEPRESSED WITH SHIFT/CTRL AND ALPHA/SHIFT NOT DEPRESSED.

** INDICATES NOT A CODE GENERATING KEY.

A BLANK KEY INDICATES A NUL CHARACTER IS GENERATED.

FIGURE 3-5.20. CALCULATOR NUMERIC CHARACTERS, CALCULATOR CLUSTER KEYBOARD

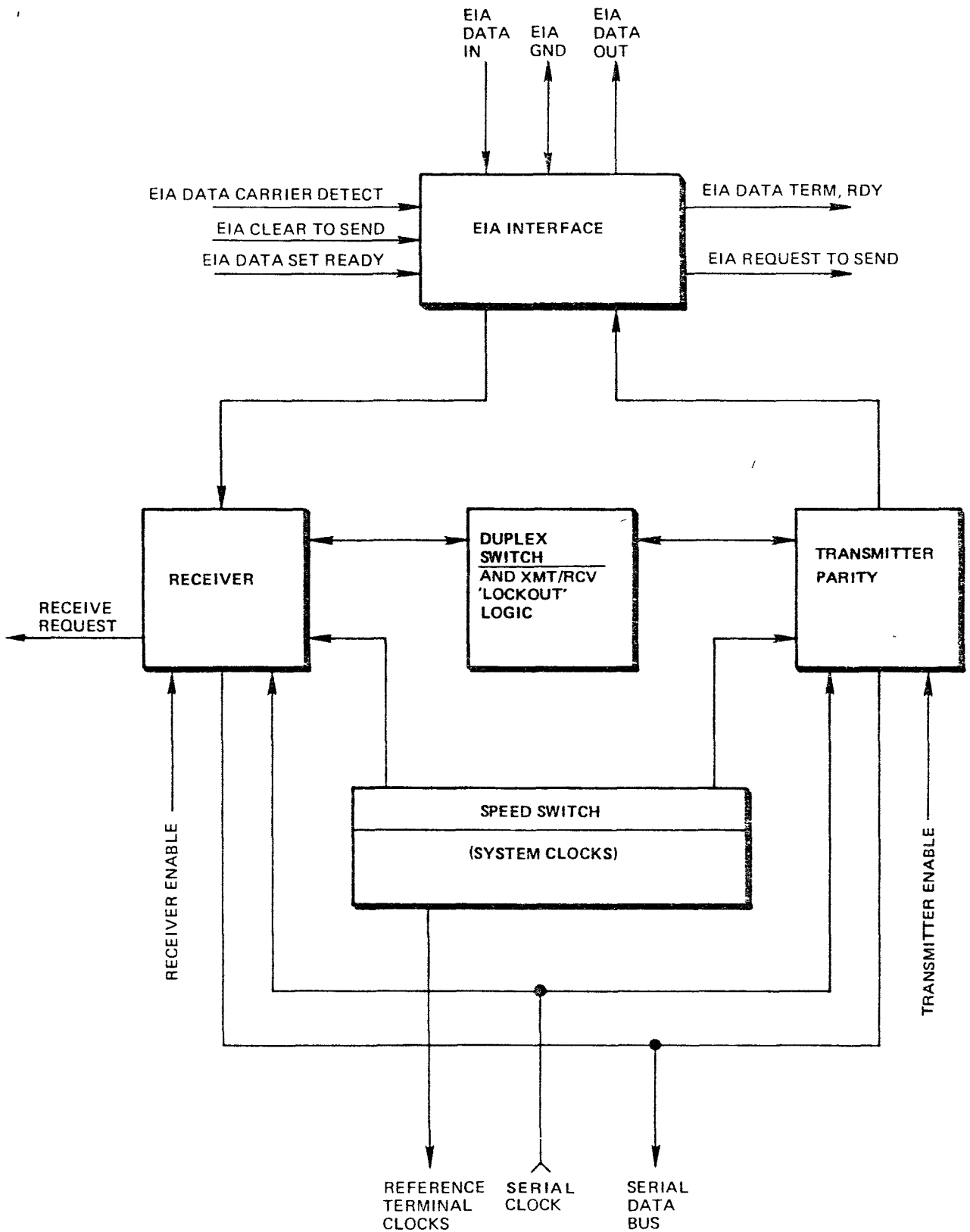


FIGURE 3-6.1. ASCII/BAUDOT TRANSMIT/RECEIVE PC CARD BLOCK DIAGRAM

binary format. The standard format operation of both PC cards is identical. Differences in binary-format operation are noted in the following description.

Both versions of the ASCII Transmit/Receive PC cards, block diagrammed in Figure 3-6.1, are composed of four major sections:

- a. Transmitter
- b. Receiver
- c. System clocks
- d. EIA control signals.

3-6.1.1 Transmitter. Upon receipt of a transmit-enable (XMTENA) and eight system clocks (SCLK) from terminal control, the transmitter stores the character present on the serial data bus in a buffer register. As the data enters the buffer register, parity is generated. The parity is switch-selectable to even, odd, or continuous marking. At the end of the transmit-enable, the transmitter transfers the data (7 bits per character with parity in the 8th bit) in the buffer register to the output buffer.

NOTE

When the Dual-Format Transmit/Receive PC card (TI Part No. 973905 or 969455*) is strapped to binary format (resistor R17 installed between J1 and J2), parity is not generated and 8 data bits (no parity) are transferred from the buffer register to the output buffer. Table 3-6.1 summarizes the resistor-strappable functions of the Dual-Format PC card.

The SPEED switch on the card is adjustable to 10, 15, or 30 characters per second (CPS) and determines the speed at which the transmit clocks (XMTCLK) clock the data from the output buffer. Upon being clocked from the output buffer, a start bit and a stop bit (2 stop bits at 10 CPS) are added to the data. The data also is sent through a level converter which converts the TTL data to EIA data for the transmission line. At the start of a transmit enable, a transmitter busy (XMTBSY) flipflop is set which signals terminal control that the line is busy (LINBUSY) and no other characters can be transmitted during that time. The transmitter continues to clock the output buffer until the total number of bits, including start and stop bits (11 bits at 10 CPS, 10 bits at 15 or 30 CPS), are clocked to the output line. A transmit clock counter counts the transmit clocks and resets the transmitter after the data has been clocked to the line. The output data format is shown in Figure 3-6.2. As long as the transmitter is transmitting continuously (no more than a 0.5-bit time delay between transmit enables), and the DUPLEX switch is set to HALF DUPLEX, the receiver input flipflop is held preset, and the

receiver is "locked out" from receiving any data from the line. Also, if the terminal is on-line (the ON-LINE switch on the Power Switch Panel is ON-LINE) and the BREAK key is depressed, the output line is held to a continuous low level (continuous SPACE) as long as the BREAK key remains depressed. A transmitter timing diagram is shown in Figure 3-6.3, and the transmitter/receiver schematics are contained in Appendix C of this manual.

3-6.1.2 Receive. The receiver section of the Transmit/Receive PC card is an asynchronous device which continuously monitors the transmission line. EIA data on the line is passed through an EIA-to-TTL level converter for use by the receiver. Upon receipt of a start bit (high to low transition from the line), the receiver starts timing for 0.5-bit time. If the line remains low for at least 0.5 bit time, a latch is set which keeps the receiver from resetting until the whole character has been received. If the line does not stay low for at least 0.5-bit time, the receiver resets immediately and continues looking for a true start bit.

When the start bit is recognized, it is clocked into an input buffer, and each succeeding data bit also is clocked into the buffer until the whole character is clocked in. Then the receiver is reset to search for the next start bit. The data is parallel-loaded into a serial data bus buffer for transmission to the serial data bus, and a serial receiver request (SRVREQ) signals terminal control that a character has been received from the line. If the terminal is in half-duplex when the start bit is recognized, a flipflop is set (RCVHDPX) which causes the line busy (LINBUSY) line to go high and inhibit the transmitter from sending any characters.

The transmitter will stay inhibited as long as the receiver continues to receive characters in half duplex, with no longer than a character time between each character received. When terminal control sends a serial receiver enable (SRVENA) and eight system clocks (SCLK) to the receiver, the data in the serial data bus buffer is clocked out to the serial bus. The clock (32CLK) which strobes the input data is derived from the serial receiver clock (SRVCLK), whose frequency is 54 times a bit time (as determined by the SPEED switch). The 32 clock (32 CLK) starts when the clear is removed from the receiver (a start bit is recognized), and the first 32CLK comes at 0.5 bit time and then every bit time thereafter.

If T is the bit time, the 7497 from which the SRVCLK is counted down to the 32CLK will cause the data to be strobed into the input buffer within $\pm T/128$ of the center of each bit time. A block diagram of the receiver is shown in Figure 3-6.1; a timing diagram is shown in Figure 3-6.4; and the Transmitter/Receiver schematics are shown in Appendix C of this manual.

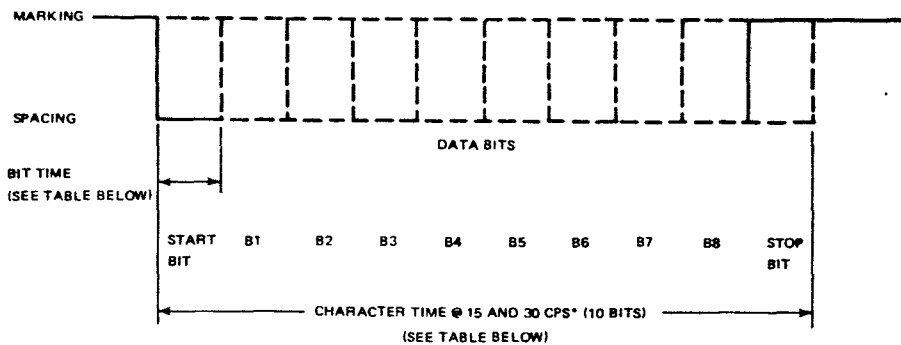
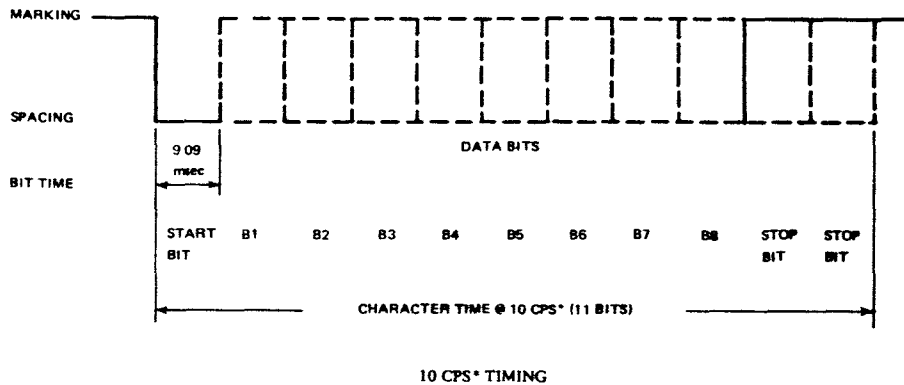
* This PC card is obsolete.

3-6.1.3 System Clocks. The entire clock system is derived from a single crystal (0.005 percent accurate) located on the Transmit/Receive PC card. The 13.5168-mHz crystal frequency is then counted down to provide all system clocks used in the data terminal. A block diagram of the system clock structure is shown in Figure 3-6.5.

3-6.1.4 EIA Control Signals. The transmitter and receiver are governed by a set of EIA control signals. These signals are supplied at the EIA connector by both the EIA sender to the terminal, and the terminal itself. The five EIA control signals and their functions are:

TABLE 3-6.1. DUAL-FORMAT ASCII TRANSMIT/RECEIVE TRANSMITTER DATA FORMAT

Data Format	Install R17 Between	Function
Standard	J3 and J4	Transfers 7 bits of character (parity in the 8th bit) to the output buffer
Binary	J1 and J2	Transfer all 8 bits of character to the output buffer



	15 CPS*	30 CPS*
BIT TIME	6.67 msec	3.33 msec
CHARACTER TIME	66.7 msec	33.3 msec

* CPS = CHARACTERS PER SECOND

FIGURE 3-6.2. ASCII LINE DATA FORMAT

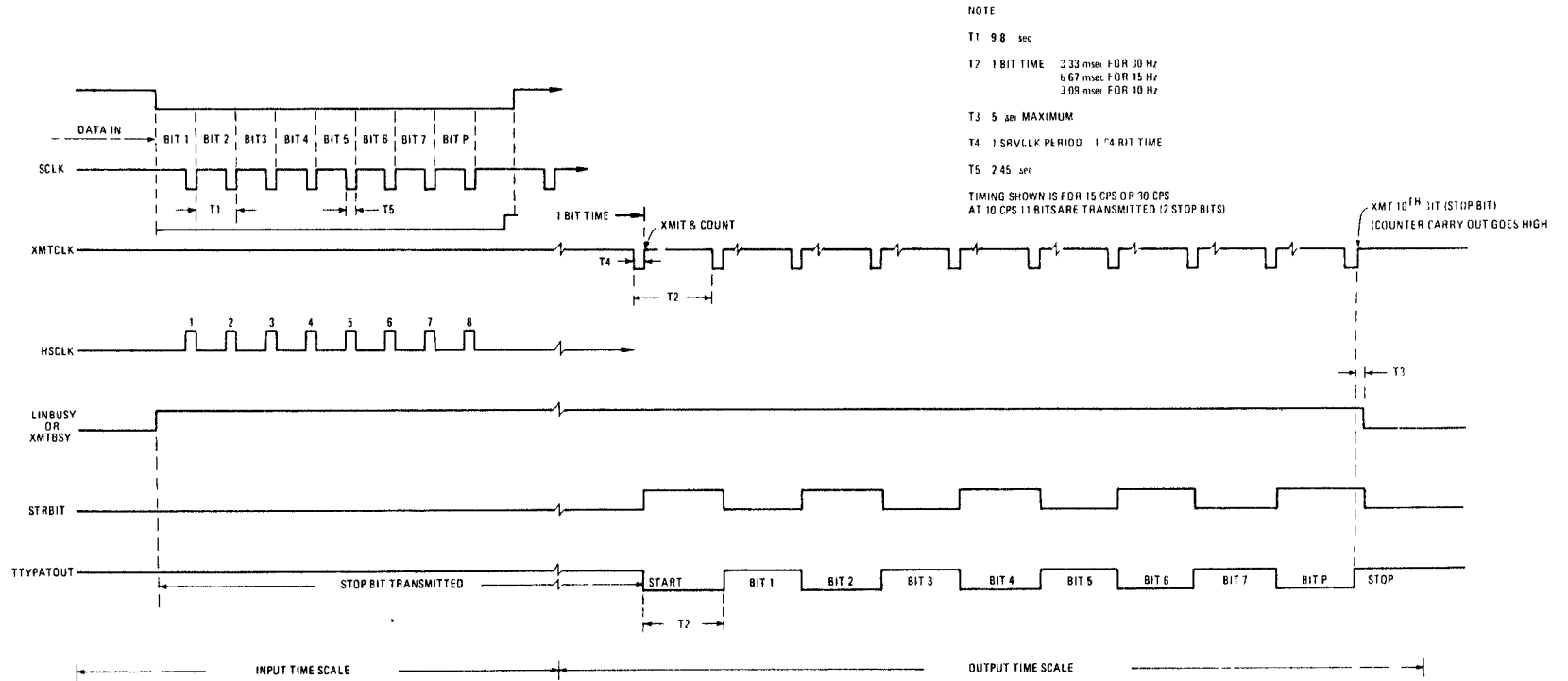


FIGURE 3-6.3. ASCII SERIAL TRANSMITTER TIMING DIAGRAM

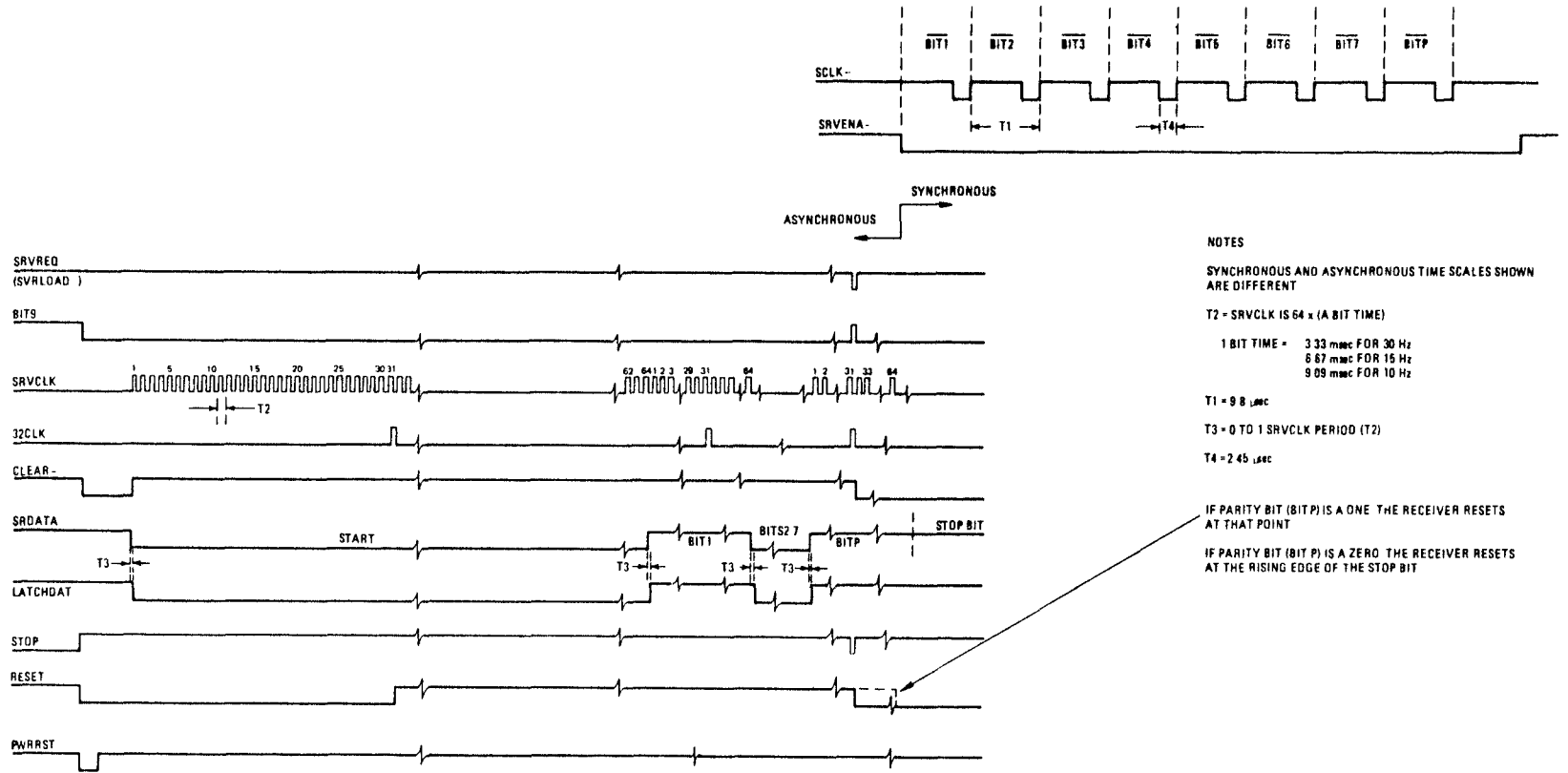


FIGURE 3-6.4. ASCII SERIAL RECEIVER TIMING DIAGRAM

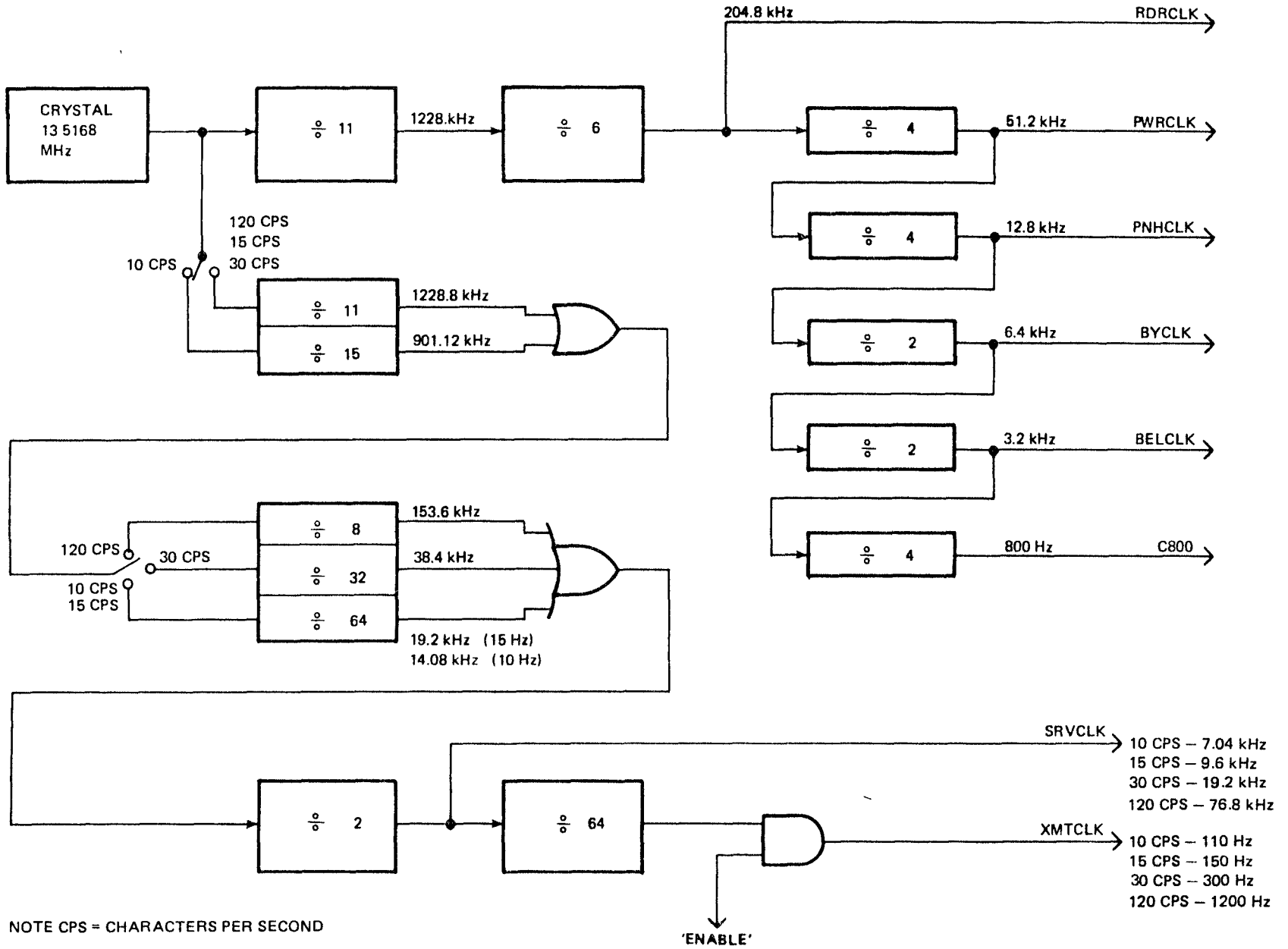


FIGURE 3-6.5. ASCII SYSTEM CLOCKS BLOCK DIAGRAM

EIA data set ready (EIADSR) – Must be a high level (>3.0V) to either transmit or receive

EIA clear to send (EIACTS) – Must be a high level (>3.0V) to transmit

EIA data terminal ready (EIADTR) – Held to a high level (>3.0V) by the terminal

EIA request to send (EIARTS) – Held to a high level (>3.0V) by the terminal.

EIA data carrier detect (EIADCD) – must be a high level (> 3.0V) to receive.

3-6.2 BAUDOT TRANSMIT/RECEIVE PC CARD. The Baudot Transmit/Receive card, block diagrammed in Figure 3-6.1. is composed of four major sections:

- a. Transmitter
- b. Receiver
- c. System clocks
- d. EIA control signals.

3-6.2.1 Transmitter. Upon receipt of a transmit enable (XMTENA) and eight system clocks (SCLK) from terminal control, the transmitter stores the data on the serial data bus in a buffer register and adds a start bit and stop bit to the data. After the character is stored in the output buffer, a timer starts which issues transmit clocks (XMTCLK) which clock the data out of the buffer at the speed (50, 75, or 100 baud) selected on the PC card SPEED switch. The TTL data then is sent through a TTL-to-EIA level converter to the transmission line.

At the start of a transmit enable, a transmitter busy (XMTBSY) flipflop is set which signals terminal control that the line is busy (LINBUSY), and no other character can be transmitted at that time. The transmitter continues to clock the output buffer until the total number of bits, including start and stop bits (7.5 bits at all speeds), are clocked to the output line. A transmit clock counter counts the transmit clocks and resets the transmitter after the data has been clocked to the line. The output data format is shown in Figure 3-6.6.

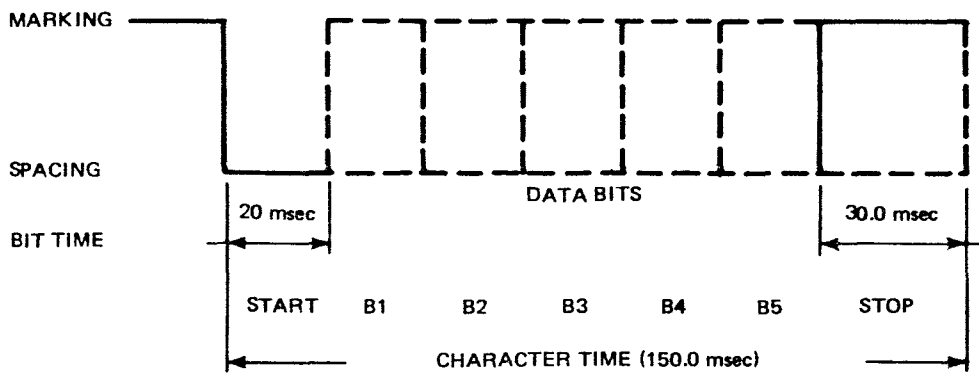
As long as the transmitter is transmitting continuously (no more than 0.5-bit time delay between transmit enables) and the duplex switch is set to half duplex, the receiver input data is held high (logic ONE); and the receiver is "locked out" from receiving any data from the line. If the BREAK

key on the keyboard is depressed, the output line is held to a continuous low level (continuous space) as long as the BREAK key remains depressed. The Baudot transmitter timing diagram is shown in Figure 3-6.7. A transmitter/receiver schematic (Drawing No. 959197) is contained in Appendix C of this manual.

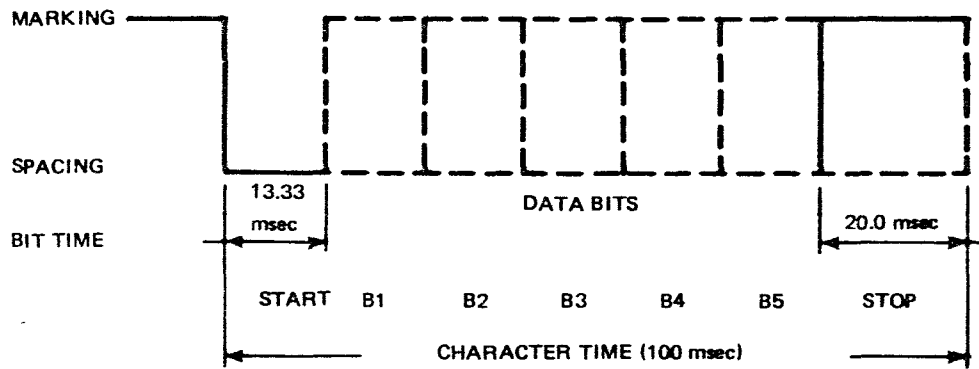
3-6.2.2 Receiver. The receiver is an asynchronous device which continuously monitors the transmission line. EIA data on the line is passed through an EIA-to-TTL level converter for use by the receiver. Upon receipt of a start bit (high to low transition from the line), the receiver starts timing for 0.5-bit time. If the line has remained low for at least a 0.5-bit interval, a latch is set which keeps the receiver from resetting until the whole character has been received. If the line does not remain low for at least 0.5-bit time, the receiver resets immediately and continues looking for a true start bit. When the start bit is recognized, it is clocked into an input buffer, and each succeeding data bit also is clocked into the buffer until the whole character is clocked in. Then the receiver is reset to search for the next start bit, the data in the input buffer is parallel-loaded to a serial data bus buffer, and a serial receiver request (SRVREQ) signals terminal control that a character has been received from the line. If the terminal is in half-duplex when a start bit is recognized, a flipflop is set (HLFDPX) which causes the line busy (LINBUSY) line to go high and inhibit the transmitter from sending any characters.

The transmitter will stay inhibited as long as the receiver continues to receive characters in half-duplex, with no longer than a character time between each character received. When terminal control sends a serial receiver enable and eight system clocks (SCLK) to the receiver, the data in the serial data bus buffer is clocked out to the serial bus. The Baudot code has only 5 bits, and the serial bus must have 8-bit codes, one for each system clock. Therefore, the last 3 bits clocked to the bus from the receiver are always three ONES. The clock (32CLK) which strobes the input data into the input buffer is derived from the serial receiver clock (SRVCLK), whose frequency is 64 times a bit time (as selected on the SPEED switch).

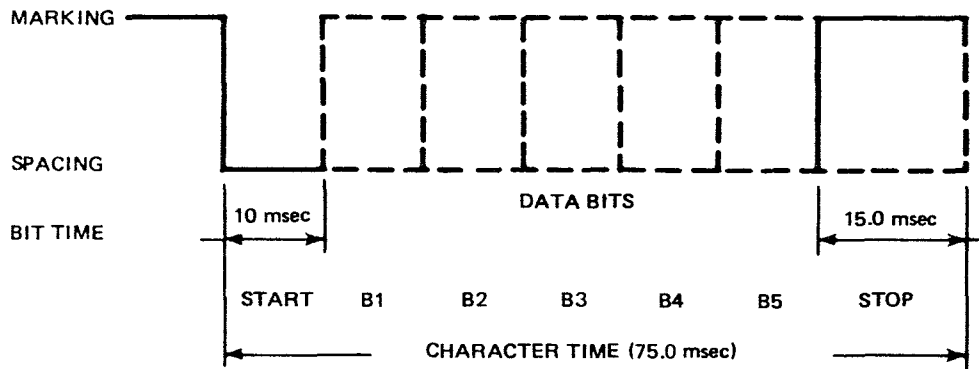
The 32 clock (32CLK) starts when the clear is removed from the receiver (a start bit is recognized). The first 32CLK comes at 0.5 bit time and then every bit time thereafter. If T is the bit time, the 7497 from which the SRVCLK is counted down to the 32CLK, will cause the data to be strobed into the input buffer within $\pm T/128$ of the center of each bit time. A block diagram of the receiver is shown in Figure 3-6.1. A receiver timing diagram is shown in Figure 3-6.8, and a Baudot Transmitter/Receiver schematic (Drawing No. 959197) is contained in Appendix C of this manual.



CHARACTER TIMING: 50 baud



CHARACTER TIMING: 75.0 baud



CHARACTER TIMING: 100 baud

FIGURE 3-6.6. BAUDOT LINE DATA FORMAT

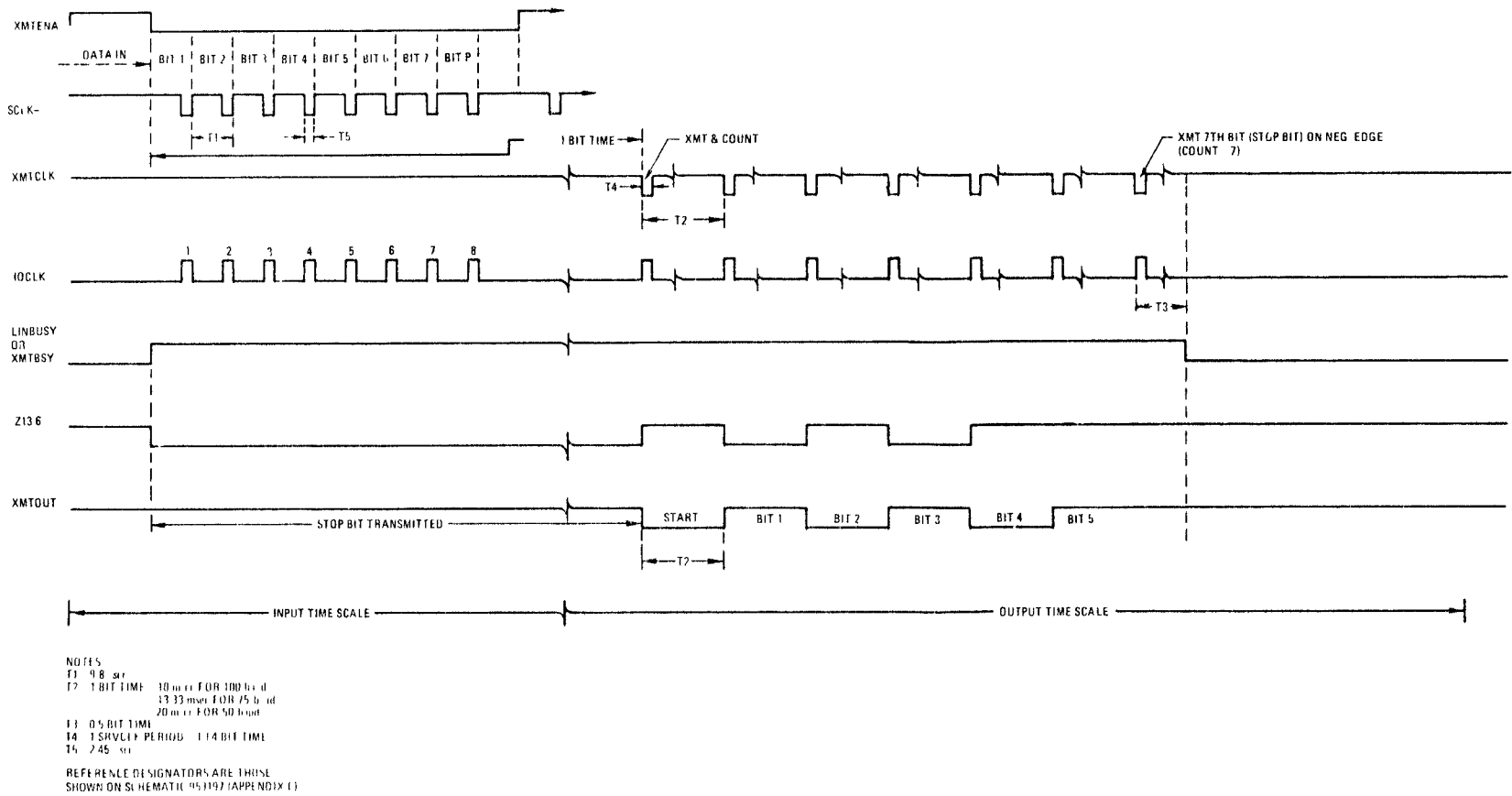


FIGURE 3-6.7. BAUDOT SERIAL TRANSMITTER TIMING DIAGRAM

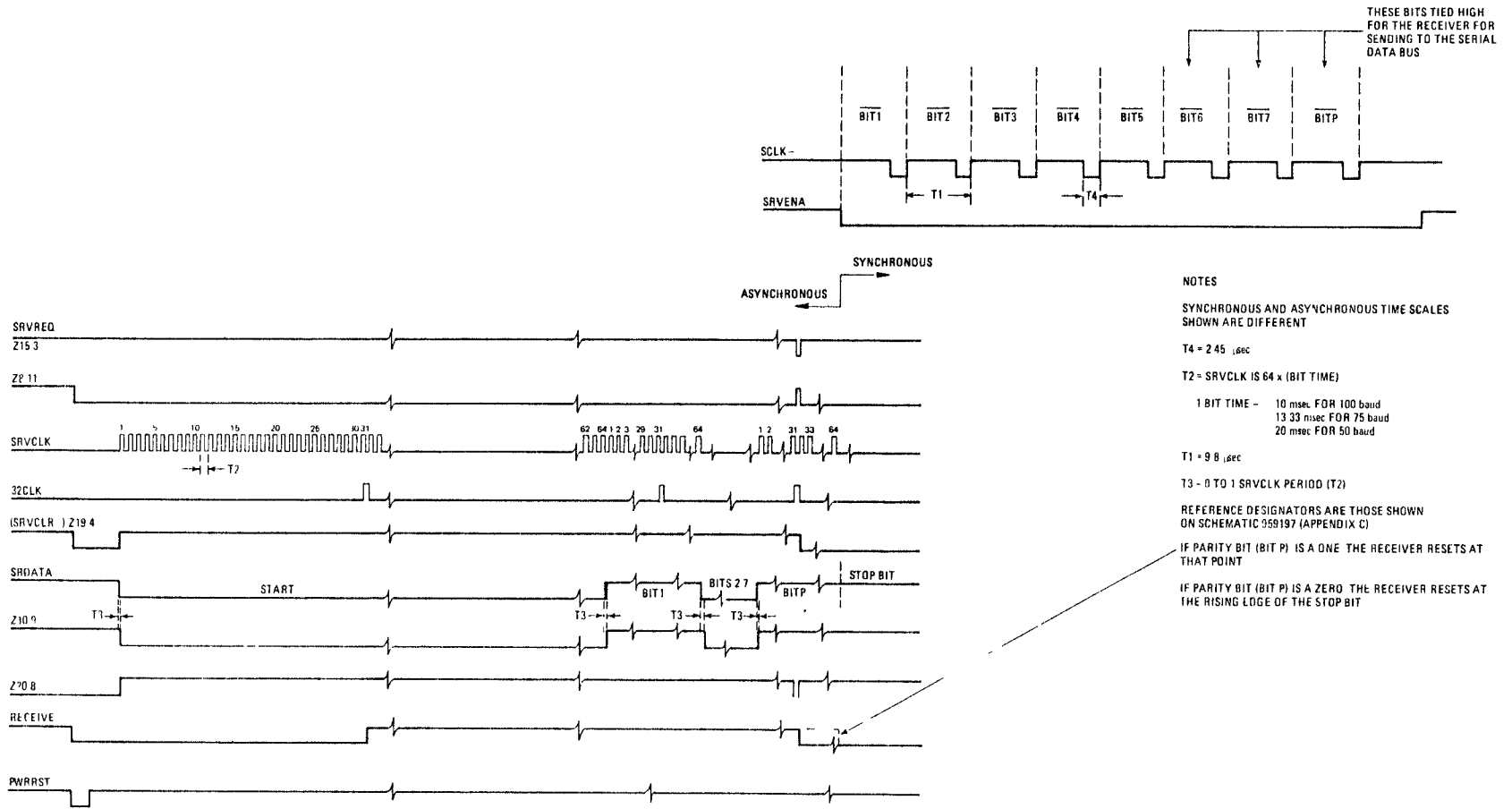


FIGURE 3-6.8. BAUDOT SERIAL RECEIVER TIMING DIAGRAM

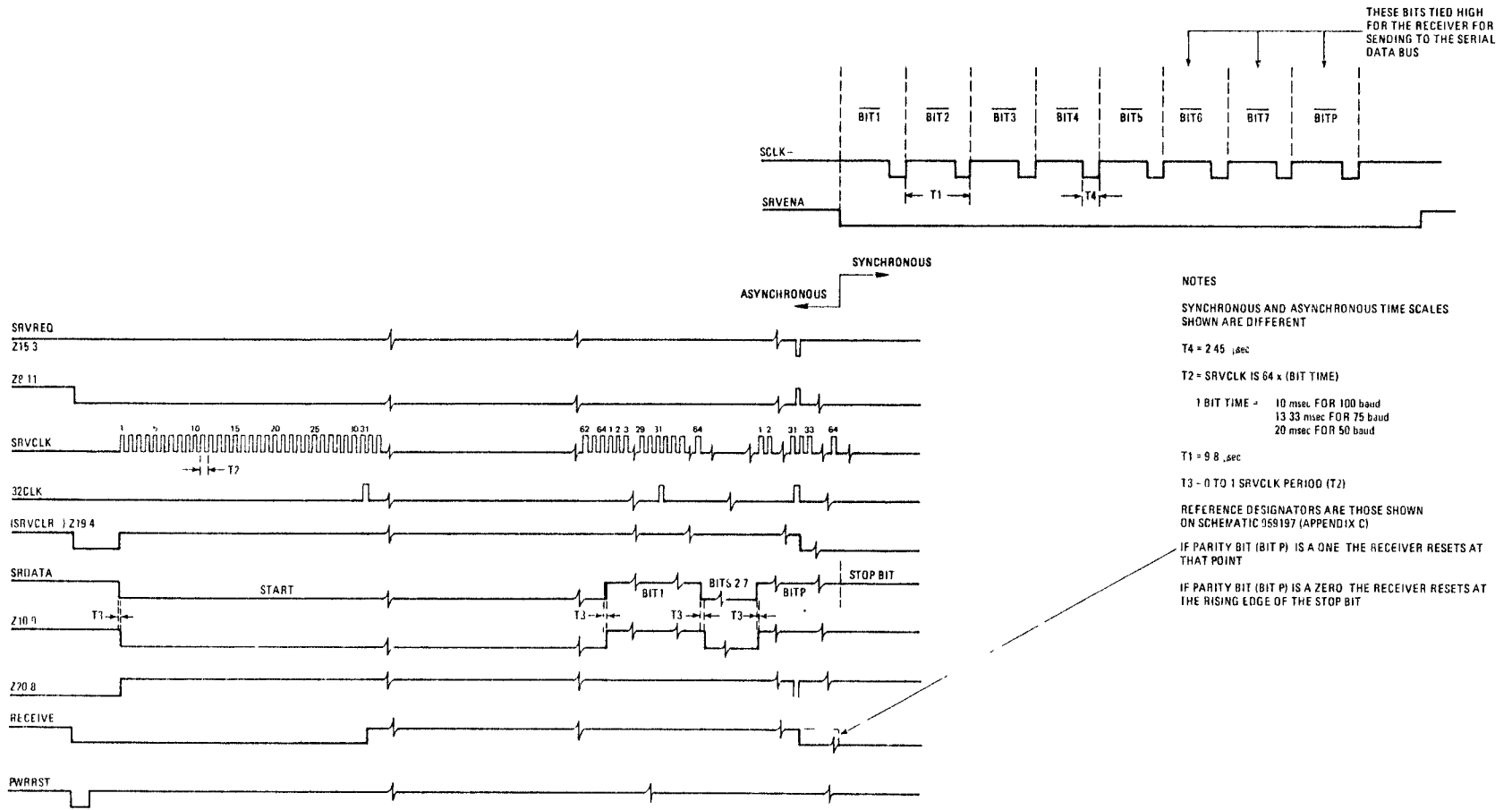
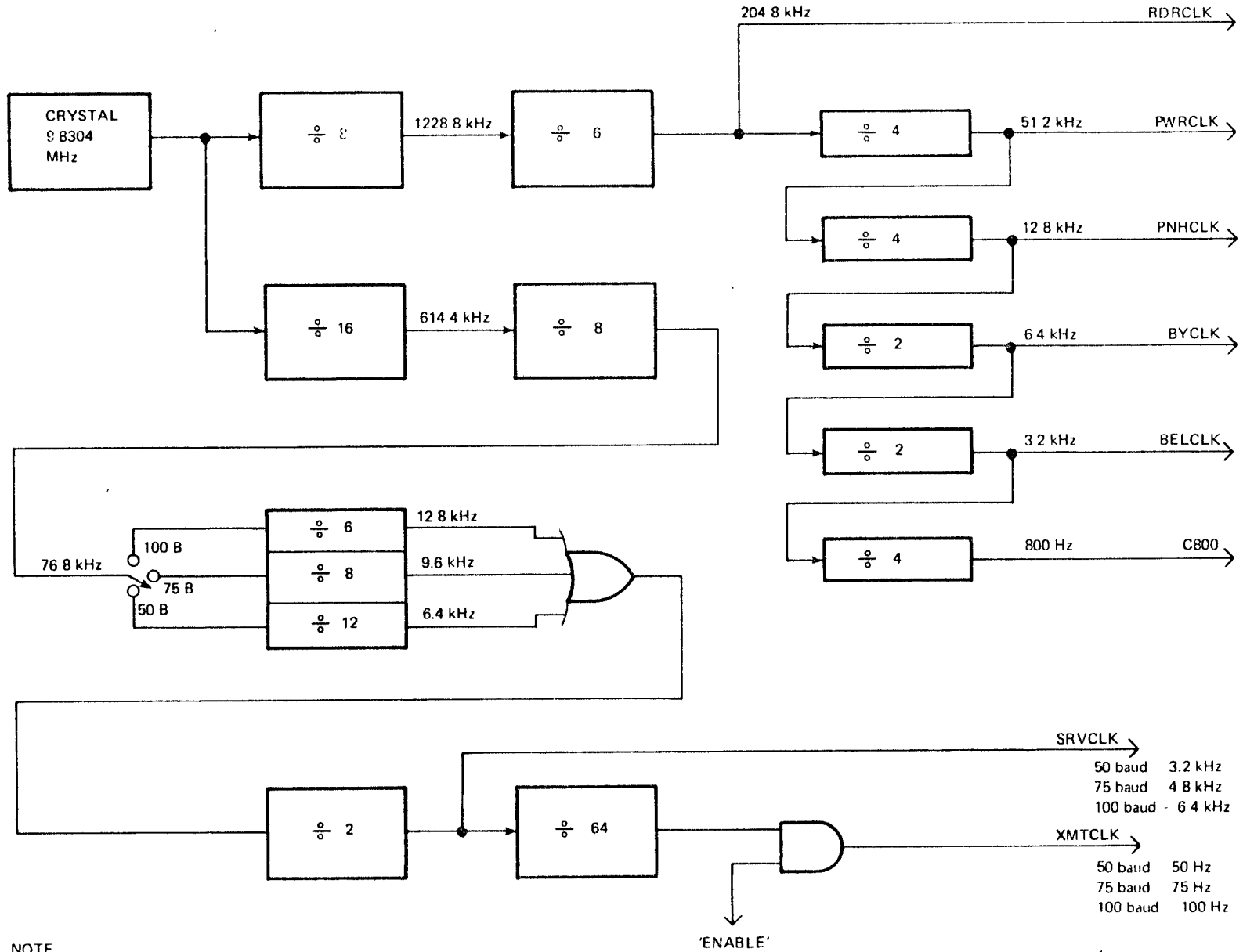


FIGURE 3-6.8. BAUDOT SERIAL RECEIVER TIMING DIAGRAM



NOTE
 SYSTEM CLOCKS ARE LOCATED ON THE TRANSMIT/RECEIVER
 PC CARD SLOT A5

FIGURE 3-6.9. BAUDOT SYSTEM CLOCKS BLOCK DIAGRAM

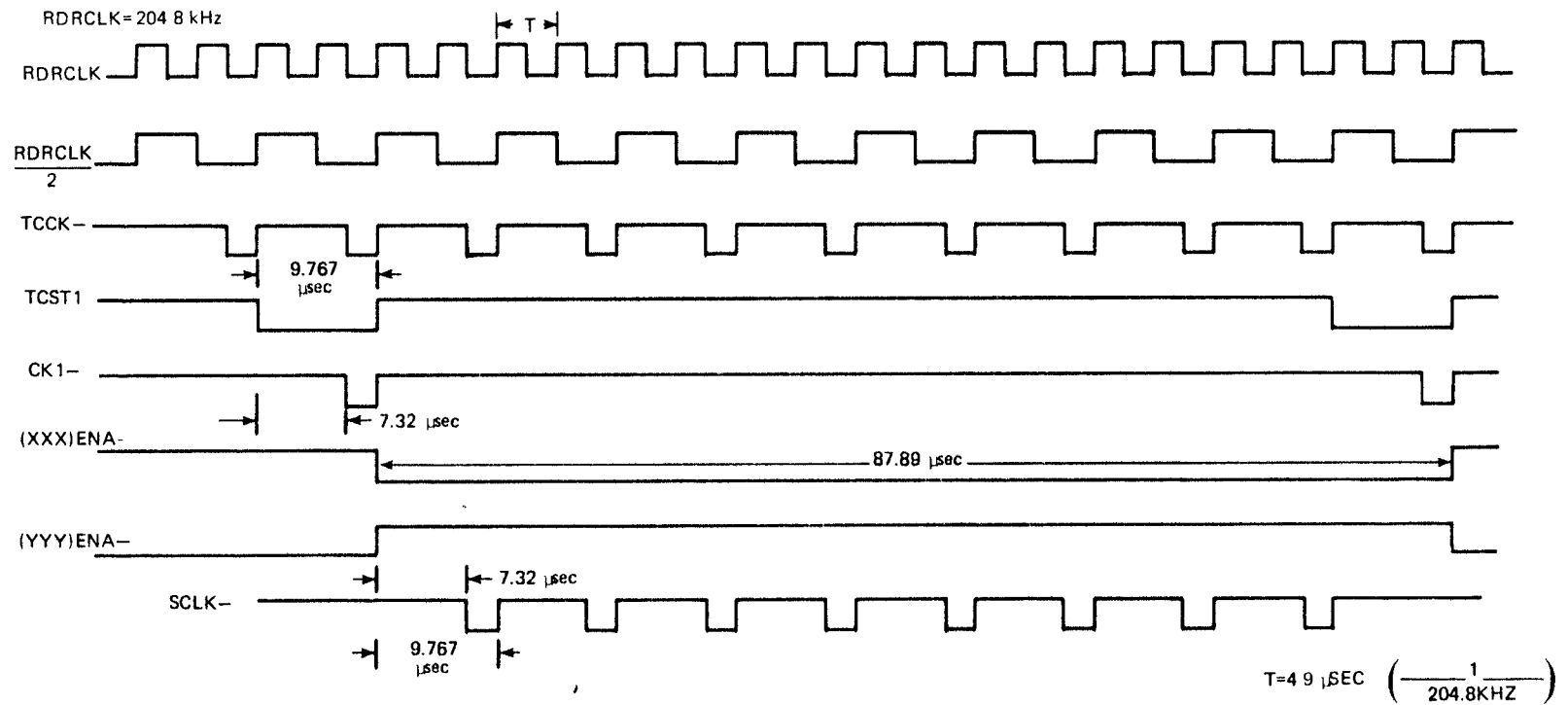


FIGURE 3-7.1. TERMINAL CONTROL SYSTEM TIMING DIAGRAM

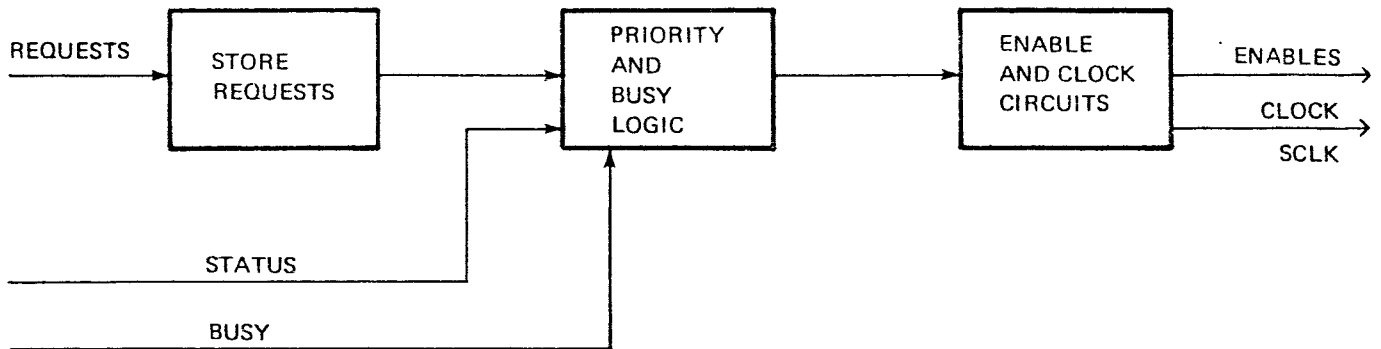


FIGURE 3-7.2. TERMINAL CONTROL BLOCK DIAGRAM

up to receive data on the same bus as the priority device. Terminal control stays in state ONE for $80\mu\text{sec}$, during which eight system clocks are sent to all devices. Ten μsec after state ONE the device enables will go off and the status enable is generated as described above. If the device with priority is in the local mode, terminal control will bring up the local busy line and hold it for 800 to $900\mu\text{sec}$. The busy line also may be held up by AUX1BUSY, or record-buffer-full, or by the printer-busy signal. The local busy line will block devices in the local loop from receiving enables but will not affect the line loop.

The ASR terminal control timing diagram is shown in Figure 3-7.1; a block diagram is shown in Figure 3-7.2.

3-8 CASSETTE SYSTEM.

The cassette system consists of two cassette transports and two motion control circuits. The playback control can be used on either transport but not both simultaneously. The playback control reads data from the tape one block at a time and stores it in a memory. It can then send data from the memory, one block at a time, one character at a time, or continuously.

The record control can be used on either transport but not both simultaneously. The record control accepts data from

the terminal and stores it in a memory. The data can be edited while in the memory (within certain limitations) and then written on tape in line or continuous format. A block diagram of the cassette system is shown in Figure 3-8.1.

3-8.1 RECORD CONTROL. Record control, block diagrammed in Figure 3-8.2, consists of three PC cards: the Record Control PC card, the Record Buffer PC card, and the Tape Read/Write Control PC card.

NOTE

The Record Buffer PC card is available in two versions: the standard format version (TI Part No. 960903) and a dual-format version (TI Part No. 962285). The Tape Read/Write PC card also is available in two versions: standard format (TI Part No. 962281) and dual format (TI Part No. 969451). The terminal is equipped either with all dual-format PC cards or all standard format PC cards. The Record Control PC card (TI Part No. 960909) is the same for either set of PC cards. The difference between the two sets of PC cards is that the dual-format PC cards have strappable options which permit the

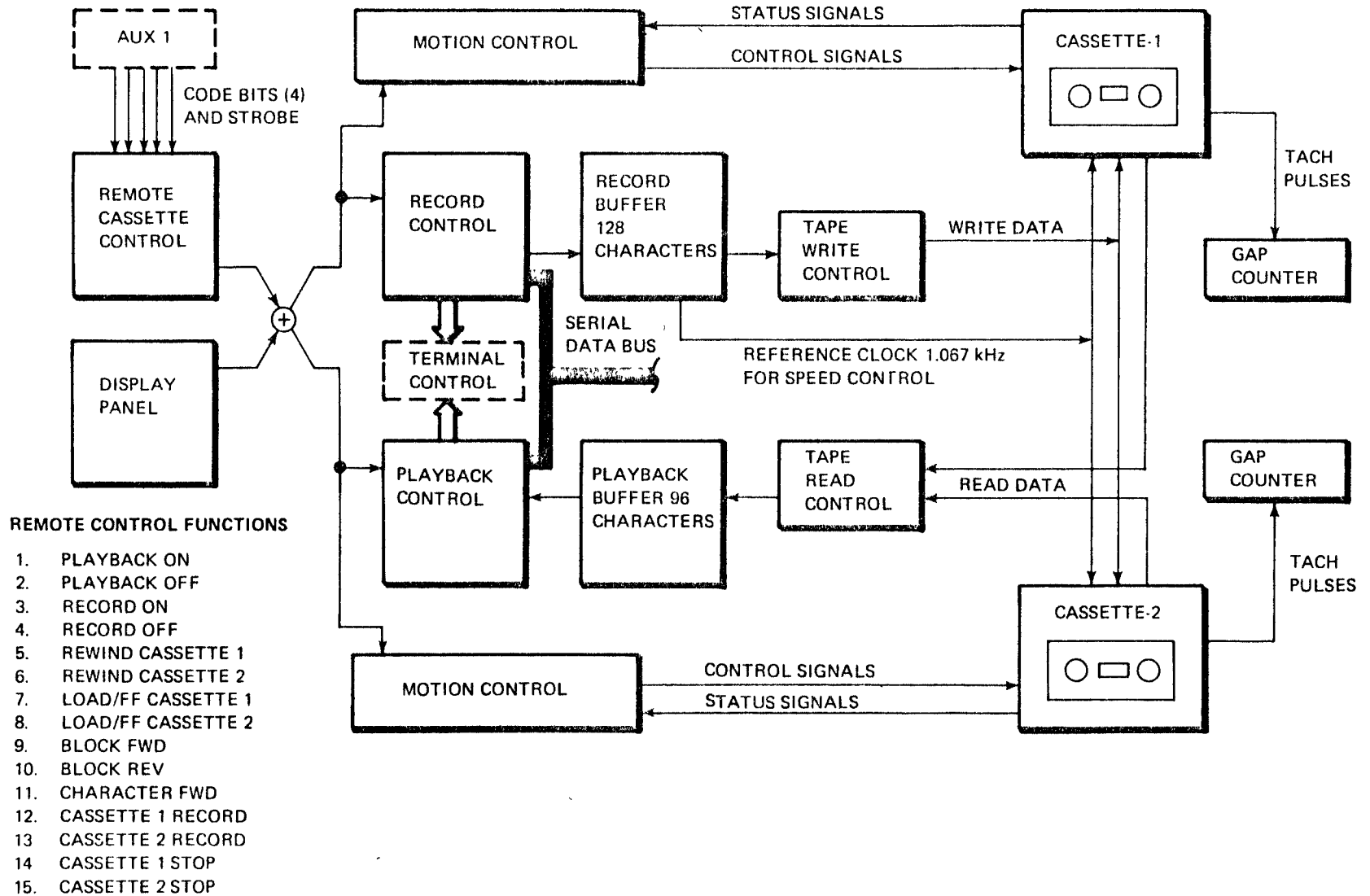


FIGURE 3-8.1. CASSETTE SUBSYSTEM BLOCK DIAGRAM

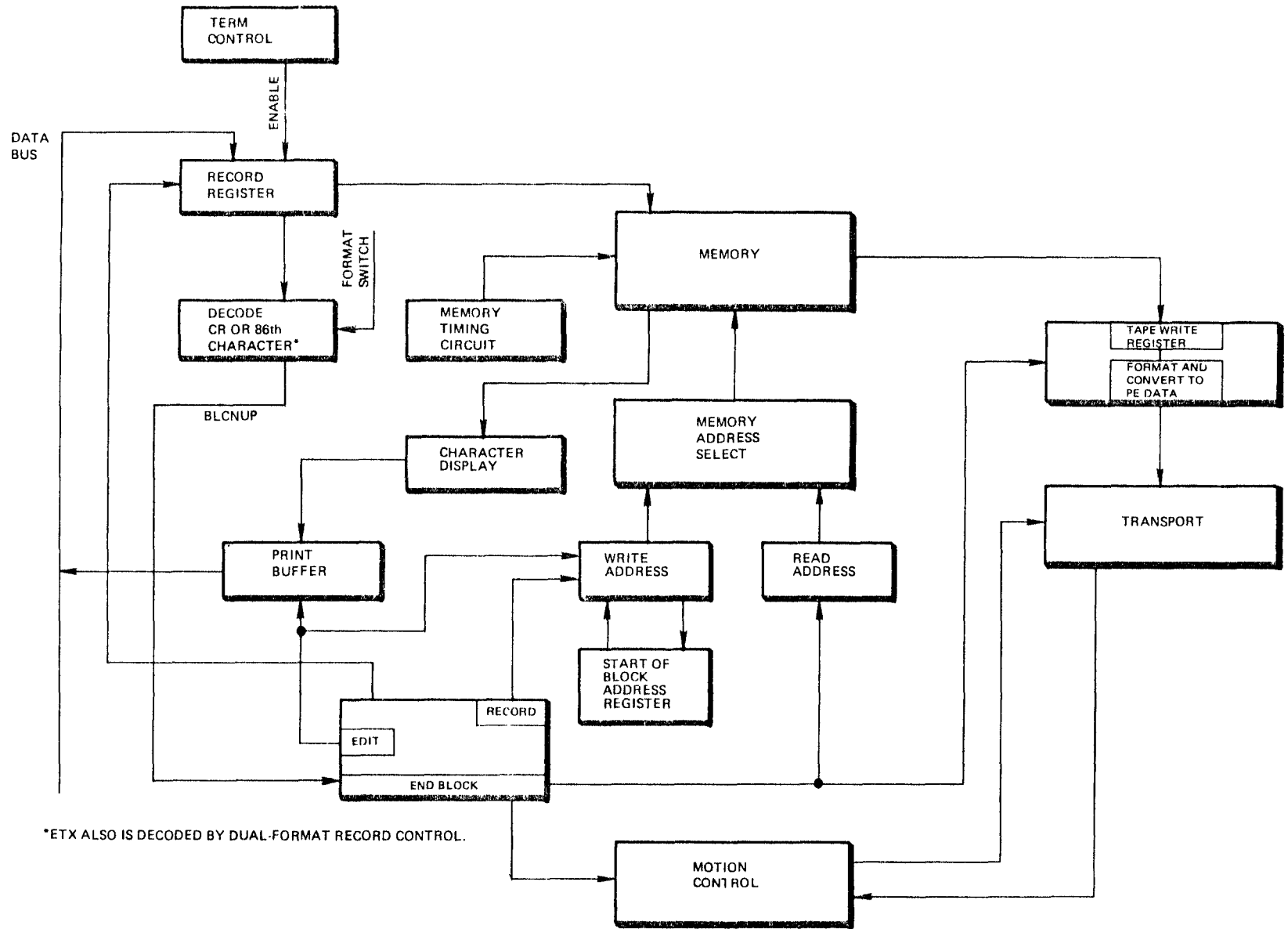
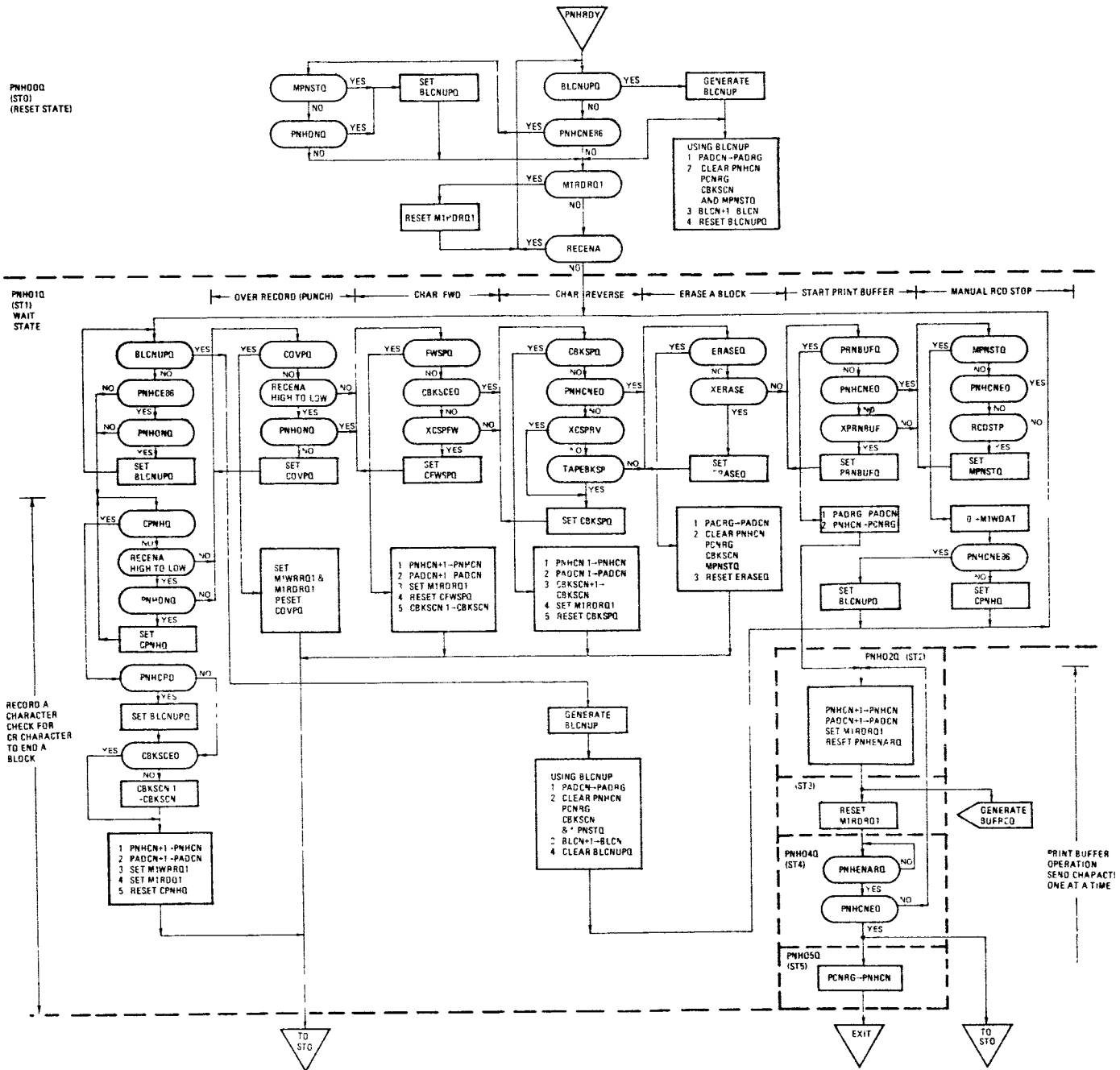


FIGURE 3-8.2. RECORD CONTROL BLOCK DIAGRAM



NOTE 1 WHEN LOW PNHROV RESETS PNH0Q THROUGH PNH0S0 AND PRESETS PNH000
 2 ALL COUNTERS AND FLIP-FLOPS ARE CLEARED BY PNHROV

FIGURE 3-8.3. RECORD CONTROL FLOW DIAGRAM

handling of either standard-formatted or binary-formatted data.

In addition, a strappable option permits the recording of a block of data (in CONTInuous tape format) to be initiated when the ETX control character is received from the communication line (see Sections 2-6.4 and 2-7.6 for implementation of this option).

The basic operation of the standard-format and dual-format PC cards is the same. Any differences in operation of these two versions are noted in the following description.

Record control accepts data and stores it in a 1024-bit memory. The last character entered into the memory is displayed on the character display. While data is in the memory, it can be modified using the tape forward (TAPE) and tape reverse (TAPE) keys on the keyboard. Data in the buffer can be printed without altering the contents of the buffer by activating the PRINT switch, and data in the buffer can be erased by activating the ERASE switch. In line format, record control puts the contents of the buffer on tape when the recorder is manually switched OFF, or when 86 characters are loaded into the buffer, or when the carriage return character is decoded. In CONTInuous tape format, record control transfers the contents of the buffer to tape either when the recorder is manually switched OFF, or when 86 characters are loaded into the buffer.

NOTE

When strapped for standard format operation, the optional dual-format record control also transfers the contents of the buffer on tape when the ETX (end of text) control character is decoded. The ETX decode is a strappable option (see Sections 2-6.4 and 2-7.6 for implementation instructions).

Each of these functions is explained below. A record control flow chart is shown in Figure 3-8.3.

The record control uses recorder enable (RECENA) and eight system clocks (SCLK) to clock data into a serial-to-parallel converter if the recorder is ON (PNHONQ). If the recorder is OFF, the data is clocked in on top of the old data (overpunched). This data is then decoded and loaded into a parallel-to-serial register. If in LINE tape format and a carriage return is decoded, or if in CONTInuous tape format (dual-format record control only) and an ETX is decoded (ETX option installed), bit 8 is forced to a ONE; otherwise, bit 8 is forced to a ZERO.

The first data bit is now clocked into the 1024-bit memory using the memory write enable (M1WRENA). Then the first bit is read from the memory into the character display by MEMORY-1 read clock (M1RD1CK). Then the memory address is changed, and the next data bit is clocked to the memory data line using the other edge of M1RD1CK). Then another write enable is generated, and bit 2 is stored in the memory. In standard format operation, this process is repeated until all 8 bits (7 data bits and 1 bit for carriage return decode, and ETX decode if enabled on Dual-Format PC cards) are stored in the memory and displayed. Figure 3-8.4 shows the memory timing sequence.

NOTE

In binary-format operation the process is repeated until all 8 bits are stored in the memory and displayed.

Each time a character is sent to the memory (CPNHQ), the punch address counter and the punch character counter are incremented by one. If the character backspace counter is not equal to zero (i.e., the buffer has been backed up), it is decremented by one. If a carriage return has been decoded in line format, or if the punch character counter is equal to 86, the block counter is incremented by one.

NOTE

If an ETX control character is decoded by the Dual-Format Record Buffer when in CONTInuous tape format, the block counter is also incremented by one.

This process loads the contents of the punch address counter into the punch address register and clears the punch counter, the punch counter register, and the character backspace counter. The tape write controller now senses that a block is to be written on tape (BLCN≠0) and will start the tape write controller. The tape write controller then starts moving the tape (TPWFW), loads 170 into the block character counter ($256-86=170$), and writes the remainder of the interrecord gaps as the tape comes up to speed (CNTQ).

When the tape is up to speed, the preamble (01010101) is written on tape, after which the first character is read from the memory into the write data register using M1RDRQ2 and M1RD2CK. The first character then is clocked out of this register by M1RD2. Then the block character counter and tape write address counter are incremented by one. This process continues until either the block character counter is equal to 256 (86 characters) or the end-of-block signal (WRTEBD) is sensed. If end-of-block is sensed, the tape write controller will write null characters on the tape until the block character counter is equal to 256. When the

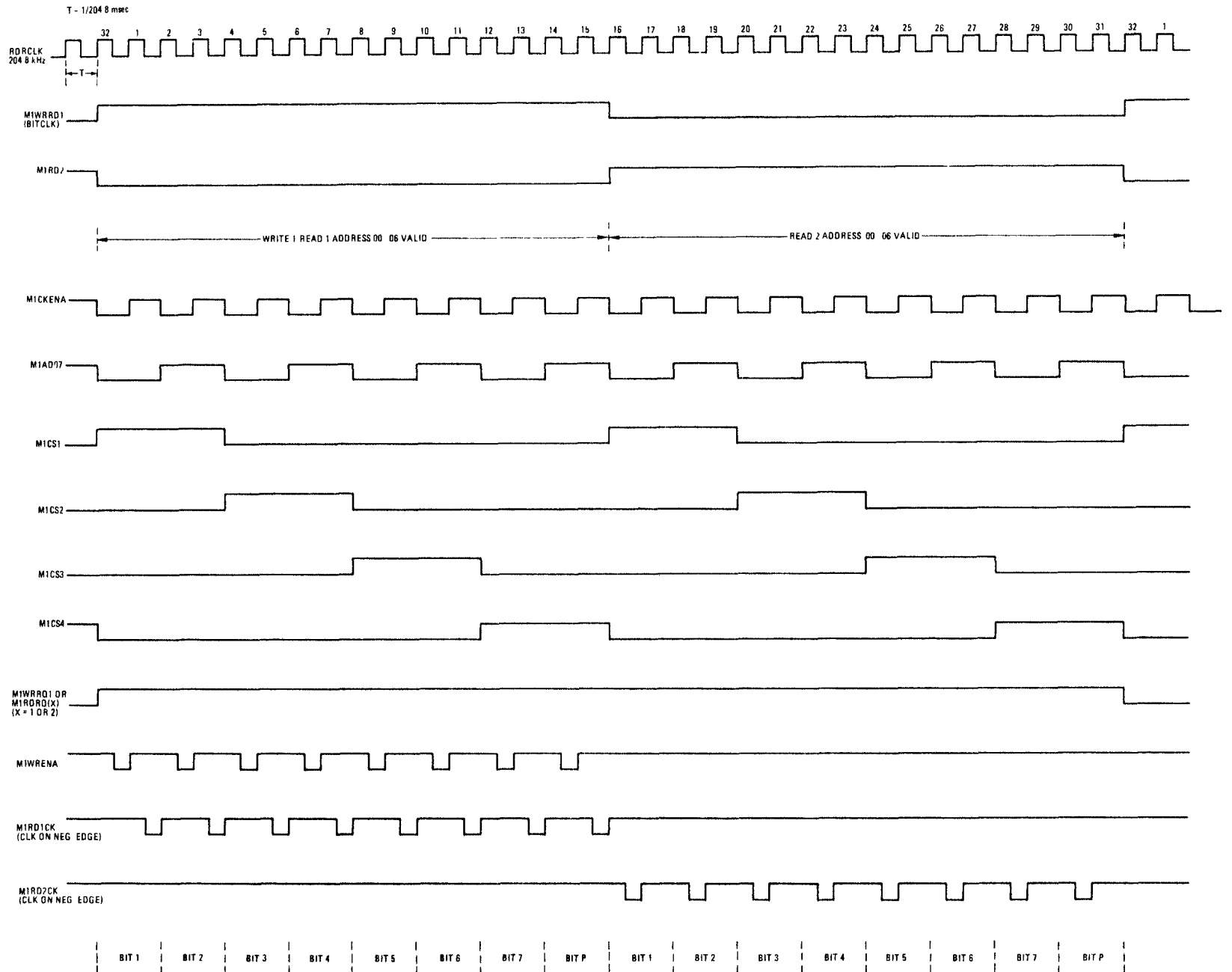
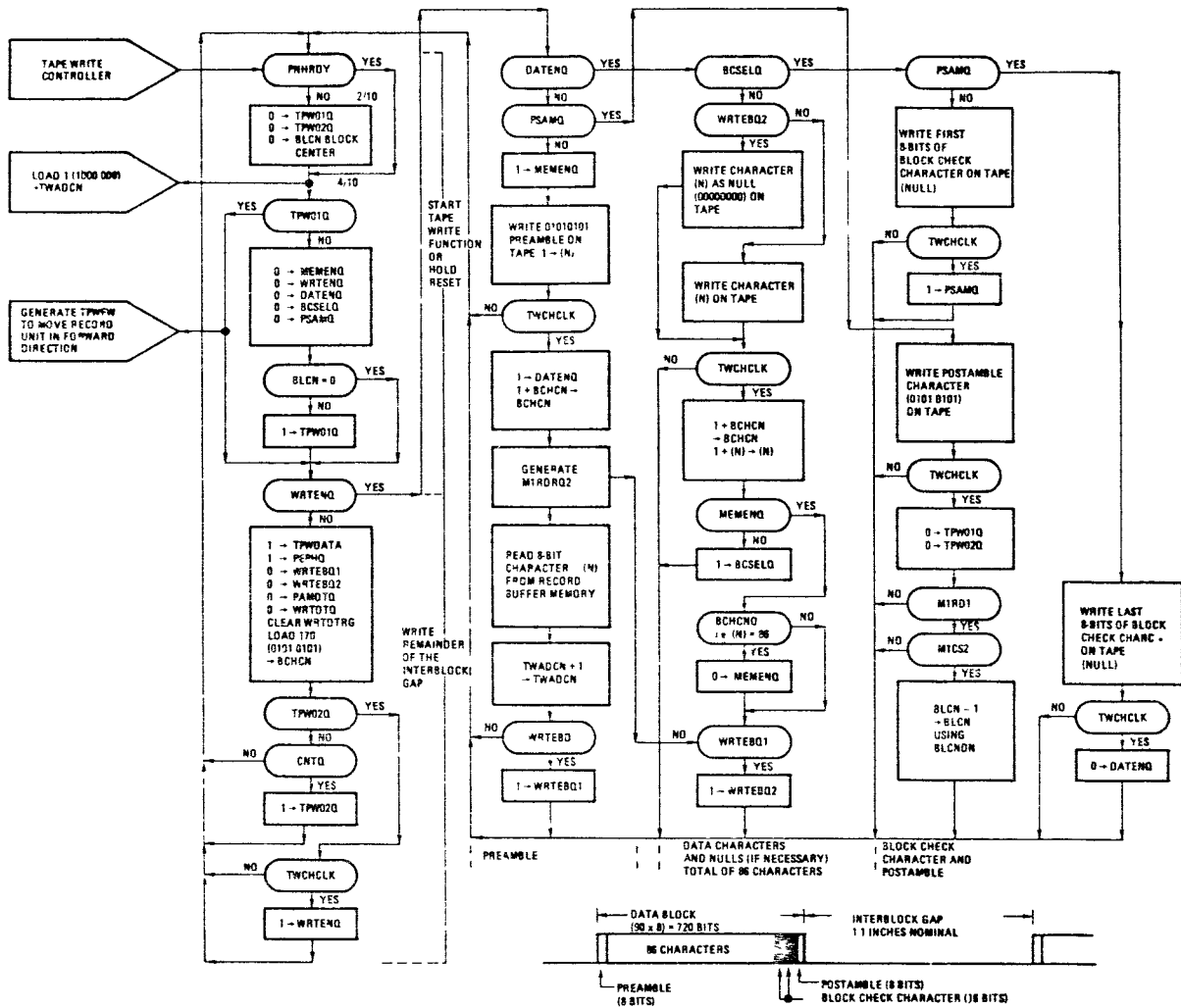


FIGURE 3-8.4. RECORD MEMORY TIMING DIAGRAM



- BCMCR BLOCK CHARACTER COUNTER
8 BITS LONG
- BLCN BLOCK COUNTER
4 BITS LONG (MAX COUNT = 15)
CONTAINS DIFFERENCE BETWEEN
NUMBER BLOCKS RECEIVED
AND NUMBER BLOCKS
WRITTEN ON TAPE
- CNTQ OUTPUT OF GAP COUNTER
- (N) VARIABLE USED IN FLOW CHART ONLY
- TWADCN TAPE WRITE ADDRESS COUNTER
FOR RECORD BUFFER (MEMORY 1)
7 BITS LONG
- WRTDTRG WRITE DATA REGISTER
- WRTEBD END-OF-BLOCK FLAG
(8TH BIT OF WRITE DATA REGISTER)

FIGURE 3-8.5. TAPE WRITE CONTROLLER FLOW DIAGRAM

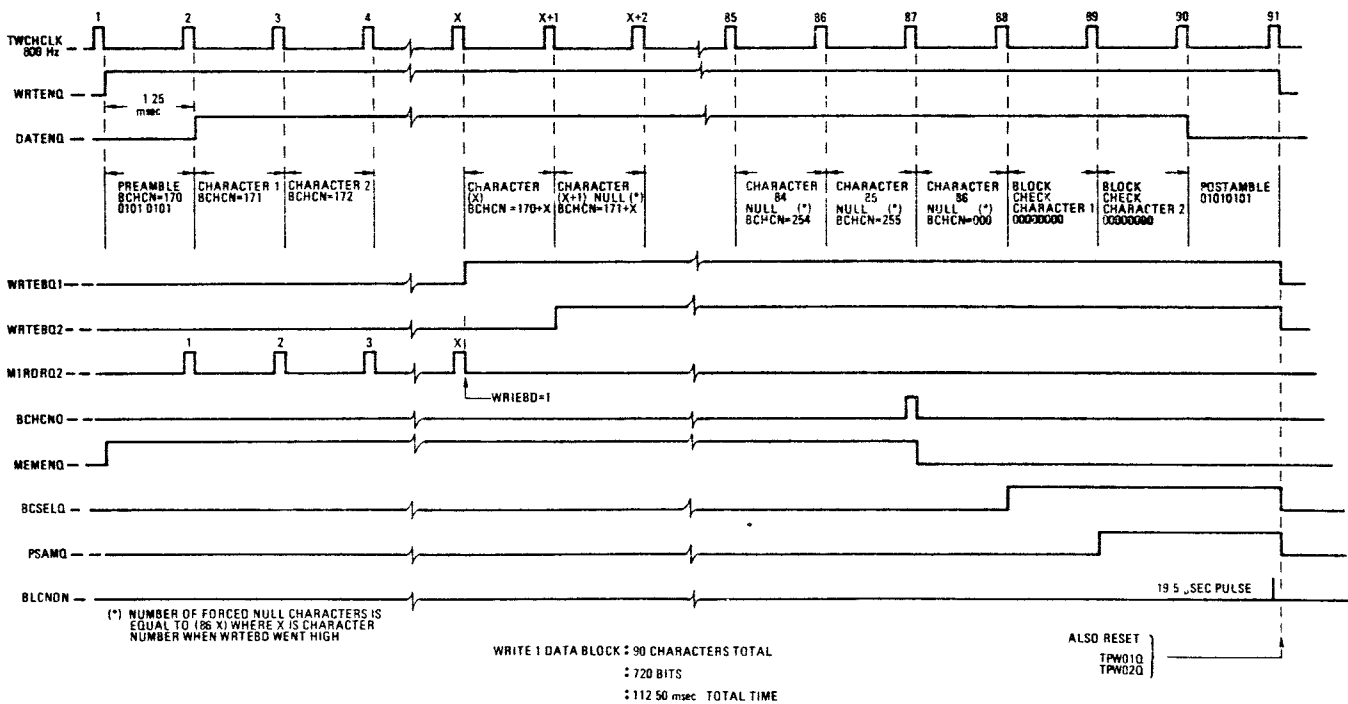
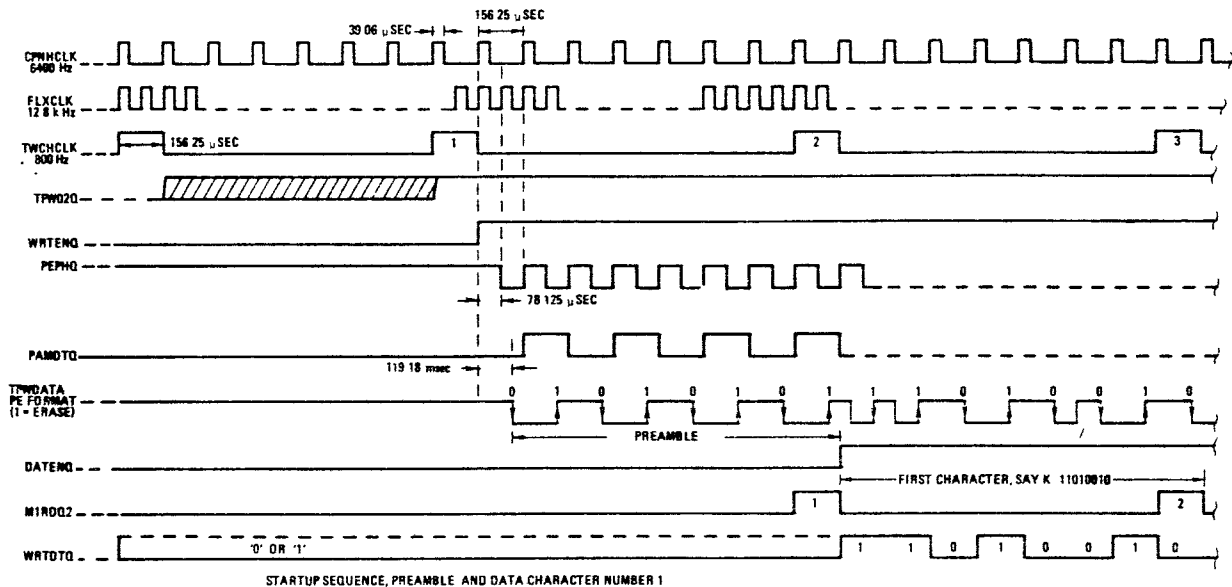


FIGURE 3-8.6. TAPE WRITE CONTROLLER TIMING DIAGRAM

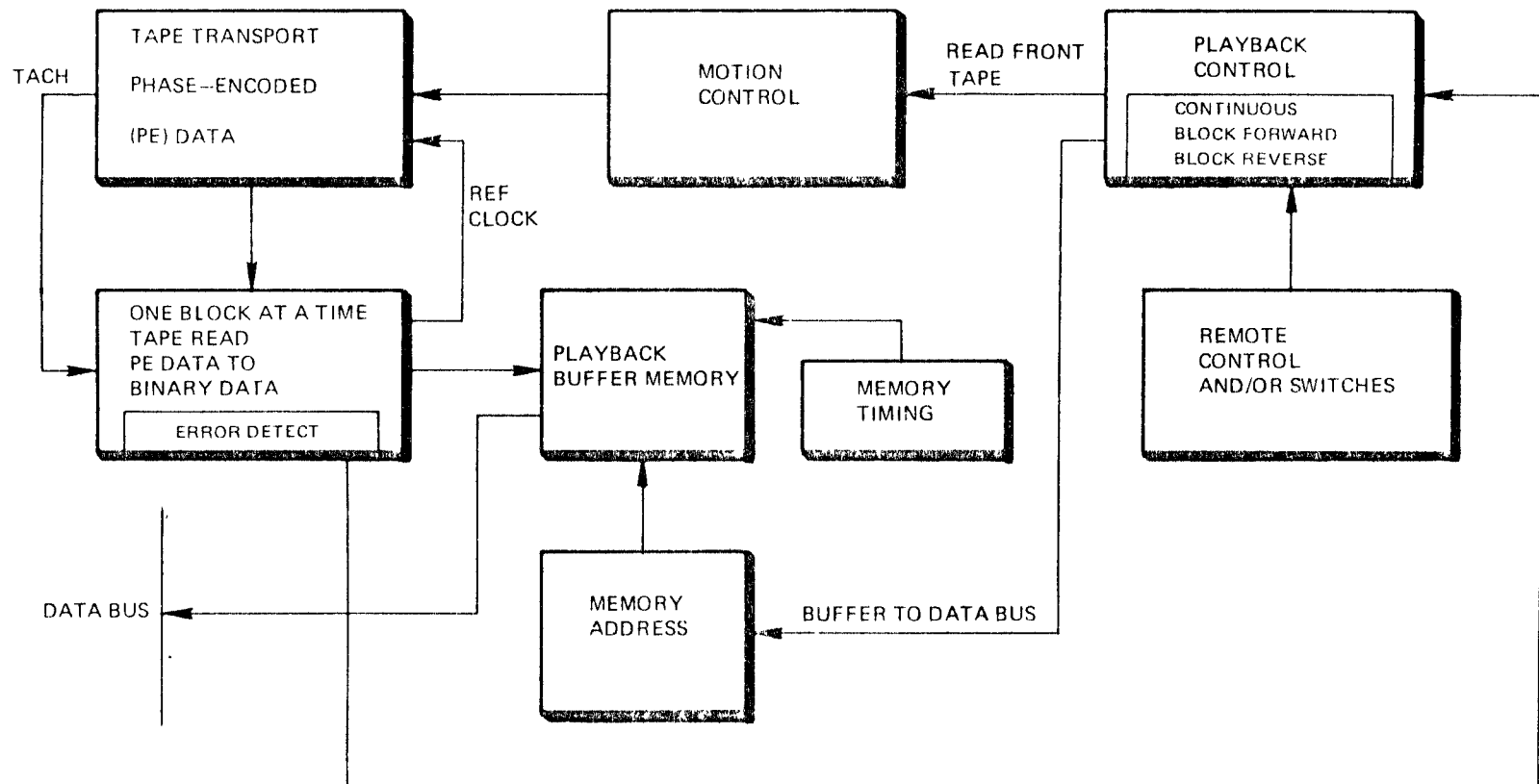


FIGURE 3-8.7. PLAYBACK CONTROL BLOCK DIAGRAM

counter is equal to 256 (86 characters), the tape write controller writes two block check characters and the postamble on tape. The block check characters are nulls (00000000) and the postamble is (01010101). The block counter is now decremented by one, and the tape write controller checks for another block ready to be written after the interrecord gap. A flow chart and timing diagram for the tape write are shown in Figures 3-8.5 and 3-8.6.

As long as data is in the buffer (punch character counter $\neq 0$) and the recorder is in the local mode, the buffer may be edited. Activating the TAPE (backspace) key on the keyboard will decrement the punch character counter and the punch address counter by one, and it will add one to the character backspace counter. It will then read the data from the new memory location into the character display using M1RDRQ1.

If the TAPE (forward space) key is depressed and the backspace counter is not equal to zero, then the backspace counter will be decremented by one, and the punch counter and the punch address counter will be incremented by one. Data from the new memory location is read into the character display using M1RDRQ1.

The contents of the record buffer can be erased by activating the ERASE switch. This will load the contents of the punch address register (last memory location of the previous block) into the punch address counter. It also clears the punch counter, the punch counter register, and the backspace counter.

The contents of the record buffer may be printed out if the RECORD and PRINTER switches are both in the LOCAL mode, and the PRINT switch is activated. This loads the punch address register (last memory location of previous block) into the punch address counter and also loads the punch character counter into the punch counter buffer register. Record control then decrements the punch character counter by one and increments the punch address counter by one. Record control then reads the first character from the buffer memory into the character display register, and issues a buffer request to terminal control (BUFRREQ). When terminal control sends back an enable (RECENA-), the contents of the display register are clocked to the data bus using the system clock (SCLK). If the punch character counter is not equal to zero, record control decrements the punch character counter and increments the punch address counter again and continues as before. When the punch counter does equal zero, the punch counter buffer register is loaded back into the punch character counter, and the record control returns to state ZERO and waits.

*This PC card is obsolete.

3-8.2 PLAYBACK CONTROL. Playback control, block diagrammed in Figure 3-8.7, is composed of four major sections:

- a. Reader controller
- b. Tape read controller
- c. Playback buffer memory
- d. Block backspace controller.

Differences between the standard format playback control (TI Part No. 960905*) and the dual format playback control (TI Part No. 981319 or 969453*) are noted in the following description.

3-8.2.1 Reader Controller. The reader controller controls the operative mode of the playback; i.e., continuous run, one block at a time, one character at a time, or one block reverse. Only one of these modes may be operative at one time, and no mode change is possible while one of the modes is already active (playback ON lamp is illuminated). Figure 3-8.8 shows the entire playback function in flow diagram form.

Upon receiving a mode command such as continuous start (CONT), the reader controller turns off the keyboard if both the reader and keyboard are in the same line mode (either on-line or off-line). In addition, before starting the tape read controller to read data from the tape, the reader controller checks that the playback is ready (cassette in place, door closed, etc.). If not ready, any mode (error or buffer-full) flipflops set are reset. A block backspace (block reverse) command always resets the error and buffer-full flipflops; this allows an error block to be reread as if the block were being read for the first time.

If a bit dropout is detected by the tape read controller while reading the tape, an error flipflop is set. If the stop-on-error option is not enabled on the Playback Control PC card (slot XA-4, ASR upper unit), the error block is sent to the serial data bus. If the stop-on-error option is enabled on the Playback Control PC card, the tape read controller stops on the block in which the error is detected. See paragraph 2-6.2 of this maintenance manual for instructions to enable the stop-on-error option. The error status may be cleared three ways: (1) a block reverse command will clear the error and allow the block to be reread; (2) a block forward command will clear both the error and the buffer-full flipflops and cause the error block to be skipped and reading to continue in the mode used before the error was detected; (3) a continuous start command will cause

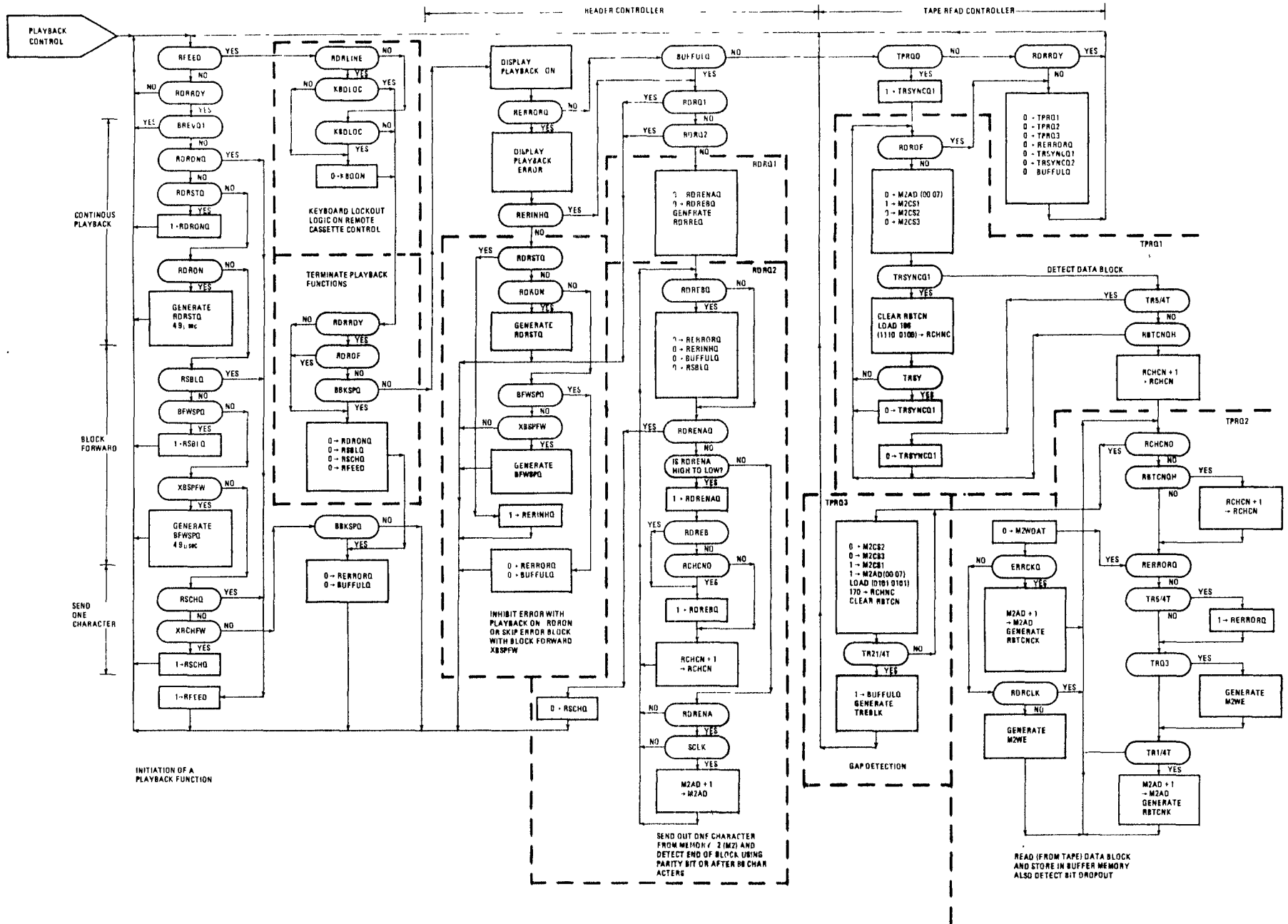


FIGURE 3-8.8. PLAYBACK CONTROL FLOW CHART

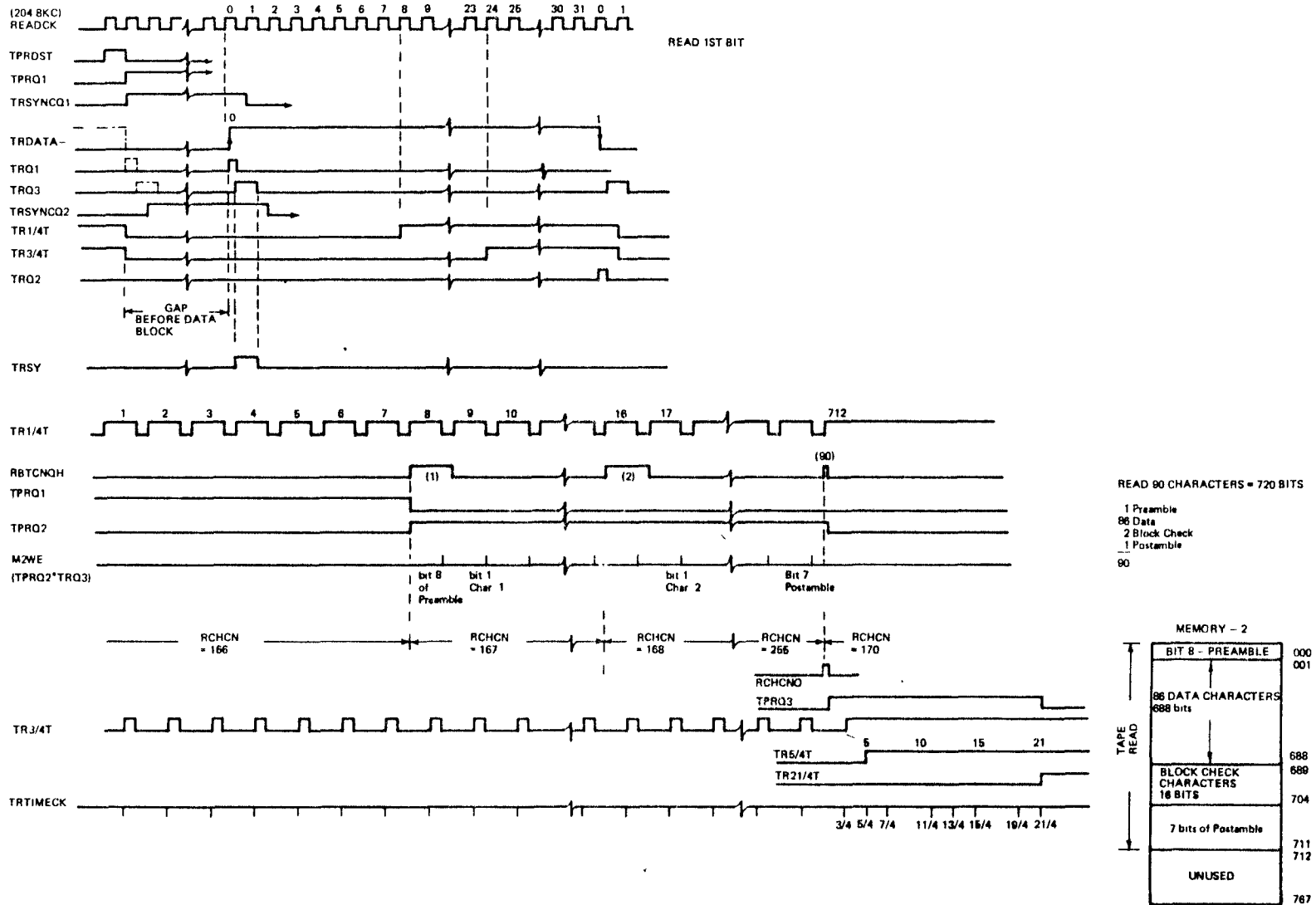


FIGURE 3-8.9. TAPE READ CONTROLLER TIMING DIAGRAM

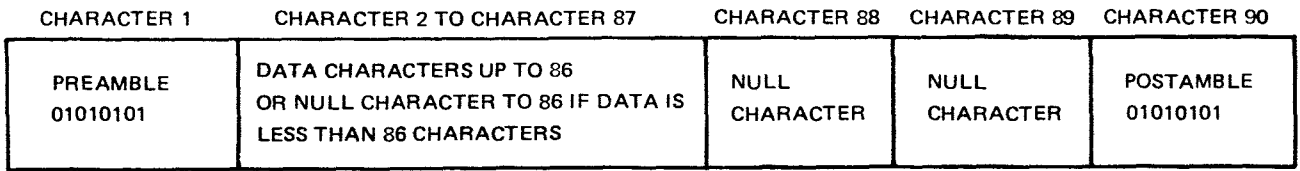


FIGURE 3-8.10. BLOCK OF DATA ON TAPE

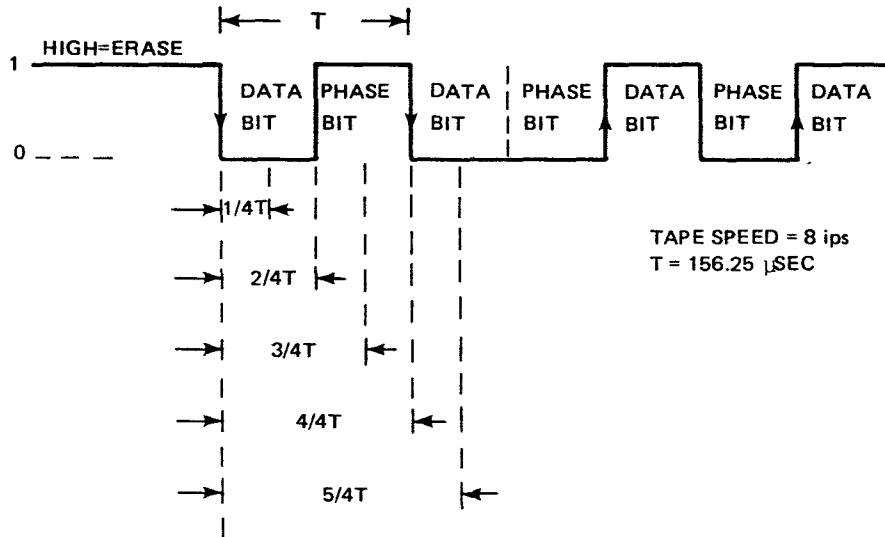


FIGURE 3-8.11. PHASE-ENCODED (PE) DATA TIMING DIAGRAM

the error to be inhibited, and the error block will be transmitted and reading will be continued in the mode used before the error was detected. At the end of the error block, the error flipflop will be cleared.

The reader control causes data to be transmitted to the serial data bus upon command (continuous read, one block at a time, or one character at a time). The tape read controller takes the data off the tape and puts it in the read buffer memory. The reader controller takes the data from the buffer memory and sends it to the serial data bus. The sequence of events for sending one character to the serial data bus from reader memory is as follows:

- a. Send a reader request (RDRREQ) to terminal control.
- b. Wait for a reader enable (RDRENA) and eight system clocks (SCLK) to take the data from the memory.

Data is removed from memory until the reader controller detects a ONE in the 8th bit of a carriage return (or ETX) character or until 86 characters are sent to the serial data bus.

NOTE

In binary format operation, data is removed from memory until 86 characters are sent to the serial data bus.

Depending on the reader controller mode, the controller will either stop at that point or cause the tape read controller to read the next block from tape.

3-8.2.2 Tape Read Controller. The tape read controller does the task of reading a block of data from the magnetic tape and storing in the reader buffer memory (see the flow chart and timing diagram in Figures 3-8.8 and 3-8.9). A block of data is shown in Figure 3-8.10. When the tape read controller detects that the buffer is not full (BUFFULQ=ZERO), it causes the tape transport to start and it searches the tape for the block preamble. Once the controller senses the first flux change of the phase-encoded (PE) data, a timer starts which produces a clock at exactly $1/4T$ (see figure 3-8.11 for PE data timing). If the first bit has remained good for at least $1/4T$ (time), a flipflop is set which inhibits the read circuit from resetting until the whole block is read. After the first preamble bit is sensed as good (true data), the next 7 bits of the preamble then must be detected. After the eighth bit of the preamble is detected, the reader buffer memory is enabled and data is entered into the buffer memory in the following order:

- a. Last bit of preamble

- b. All data bits up to eighty-six 8-bit characters
- c. Zeros to fill the buffer up to 86 characters, if 86 data characters were not written
- d. Two 8-bit null characters (00000000)
- e. Seven bits of the postamble (the eighth bit is not put in memory).

The data on the tape is recorded in a phase-encoded (PE) format. The tape read controller therefore must convert the PE data to digital data for storage in the reader memory. PE data is self-clocking; therefore, no data clock is necessary to read the data from the tape (Figure 3-8.11 shows the PE data timing). On a data transition a timer is started which clocks the data bit into memory at exactly $1/4T$. The tape read circuit is then "locked out" until the phase bit transition passes at $1/2T$. The timer then produces a clock at $3/4T$ which resets the tape read circuit to sense the next data transition. If no new data transition occurs by $5/4T$, a bit dropout is signalled and the error flipflop is set.

At this point the reader buffer memory is filled with zeros instead of data, and the tape read circuit continues reading data until it detects a gap. If no bit dropouts are detected ($5/4T$ clock), the timer is reset at each new data transition and the data is clocked into memory at each $1/4T$. After all data is clocked into memory (through the first 7 bits of the postamble), the tape read controller then seeks the interrecord gap between blocks. When the controller has detected no data for more than five bit times ($21/4T$), the tape read controller signals that the tape is in an interrecord gap and stops the transport. It also sets the buffer-full (BUFFULQ) flipflop to start the reader controller.

3-8.2.3 Playback Buffer Memory. The playback (reader) buffer memory, located on the Playback Control PC card, consists of three 256×1 random access memories and associated address counters and character counters. The memory is capable of holding 768 bits or ninety-six 8-bit characters. The memories are addressed by two 4-bit counters, giving eight address lines to each memory, and three flipflops which provide a chip select line to each memory.

A character counter is provided to the tape read controller to count the number of characters put into the memory. The same character counter is used by the reader controller to count the number of characters taken out of memory. Data is put into memory 1 bit at a time, 8 bits per character. 32 characters per memory. When the tape read is placing characters into memory, the playback buffer memory address is set to ZERO, and the character counter is set to 166. Each time a data bit is written into memory,

the address counter is incremented by one, and each time an eighth bit is received to be written into memory, the character counter is incremented by one until it overflows, after counting 90 characters. The characters are the preamble (only the last bit actually written in memory), 86 data characters, 2 null characters, and the postamble (only the first 7 bits actually written in memory).

When the reader controller is taking characters out of memory, the playback buffer memory address is set to one, and the character counter is set to 170. The memory address is set to one to skip the last bit of the preamble when the reader starts sending data to the serial data bus from the memory. Each time a data bit is taken out of memory and sent to the serial data bus, the memory address is incremented by one. Each time an eighth bit is taken out of memory and put on the data bus, the character counter is incremented by one. The reader controller continues to take data out of memory until a one is seen in the eighth bit of an 8-bit character, or the character counter overflows after counting 86 characters.

NOTE

If the Dual-Format Playback Control PC card (TI Part No. 969453* or 981319) is set for standard format [TERLINE-switch (S1-1) is open and the BINFMT-switch (S1-2) is closed, or R5 is installed between J5 and J6], the reader controller will continue to take data out of memory until a ONE is seen in the 8th bit, or the character counter overflows after counting 86 characters. If the terminal ON-LINE/OFF switch is in ON-LINE position and the Dual-Format Playback Control is set for binary format [TERLINE-switch (S1-1) is closed and the BINFMT-switch (S1-2) is open, or R5 is installed between J3 and J4], the reader controller will continue to take data out of memory until the character counter overflows after counting 86 characters.

Either condition signifies the end of a block, and the tape read controller must then put a new block of data into the memory for the reader controller to send to the serial data bus.

3-8.2.4 Block Backspace Controller. The block backspace controller, located on the Remote Cassette Control PC card, causes the tape to back up one block (see Figure 3-8.12). When a block reverse command is received by the block backspace controller, the tape transport moves the tape in reverse. The tape read circuit reads the tape, and the block backspace controller counts the number of data bits read in the reverse direction. When the backspace controller

counts 16 data bits without a bit dropout (TR 5/4T signals a dropout), it assumes that it is in the middle of a block of data and starts to search for the next interrecord gap. When no data is detected for a period equal to 21/4T ($T=156.25\mu\text{sec}$), the controller assumes that it is in the interrecord gap and should stop the tape. However, the transport's minimum stop time is only 0.2 inches (1 inch = 132.415 tachs) of tape, while the maximum start time is 0.5 inches. Therefore, a delay timer is started when the gap is detected, delaying stopping the transport for approximately 64 tach pulses. These 64 tach pulses, plus the minimum stop distance of the transports, allows enough distance so that when the transport is started again to read the next block, it will be up to speed before it is out of the gap and into the data. The delay timer does not actually count tach pulses to get a 64 tach pulse delay, but instead counts the reference clock (TRFCLKB) used by the transport for the phase lock loop which controls motor speed. When the motor is running at full speed, the phase lock loop ensures that a tach pulse occurs at each reference clock (TRFCLKB) with long-term speed variation of no more than 1 percent. Since the motor is running at full speed during the block reverse, the proper condition exists such that 64 reference clocks (TRFCLKB) should approximately equal 64 tach pulses; therefore, the transport may be stopped after the timer has counted 64 reference clocks into the gap.

3-8.3 MOTION CONTROL. The Motion Control PC card controls rewind, load, and fast forward operations of both cassettes: generates write, forward, reverse, and fast commands; and controls the ready signals for the playback and record. Each of these functions is explained in the following paragraphs. A flow chart of the motion control function is shown in Figure 3-8.13.

3-8.3.1 Rewind: to rewind tape: (1) the cassette door must be closed, (2) the tape must not be on the left end, (3) the cassette tape must not be moving (either forward or reverse), and (4) the cassette transport must not be "BUSY" (reading or recording). When these three conditions are met and the REWIND switch is actuated, the rewind latch will be set (C1RWQ).

This generates reverse and fast commands for the transport until either the STOP switch is actuated (STPCA1), or the left end of the tape is reached (T1LEQ).

3-8.3.2 Load: To load tape: (1) the cassette door must be closed, (2) the write tab must be in place if the transport is in the RECORD mode, (3) the tape must not be at the right end or moving, and (4) the cassette must not be "busy". Then if the LOAD/FF (fast forward) switch is actuated while the tape is on the clear leader (BOE0CA1), the load flipflop is set (LOAD1Q). LOAD1Q generates the

* This PC card is obsolete.

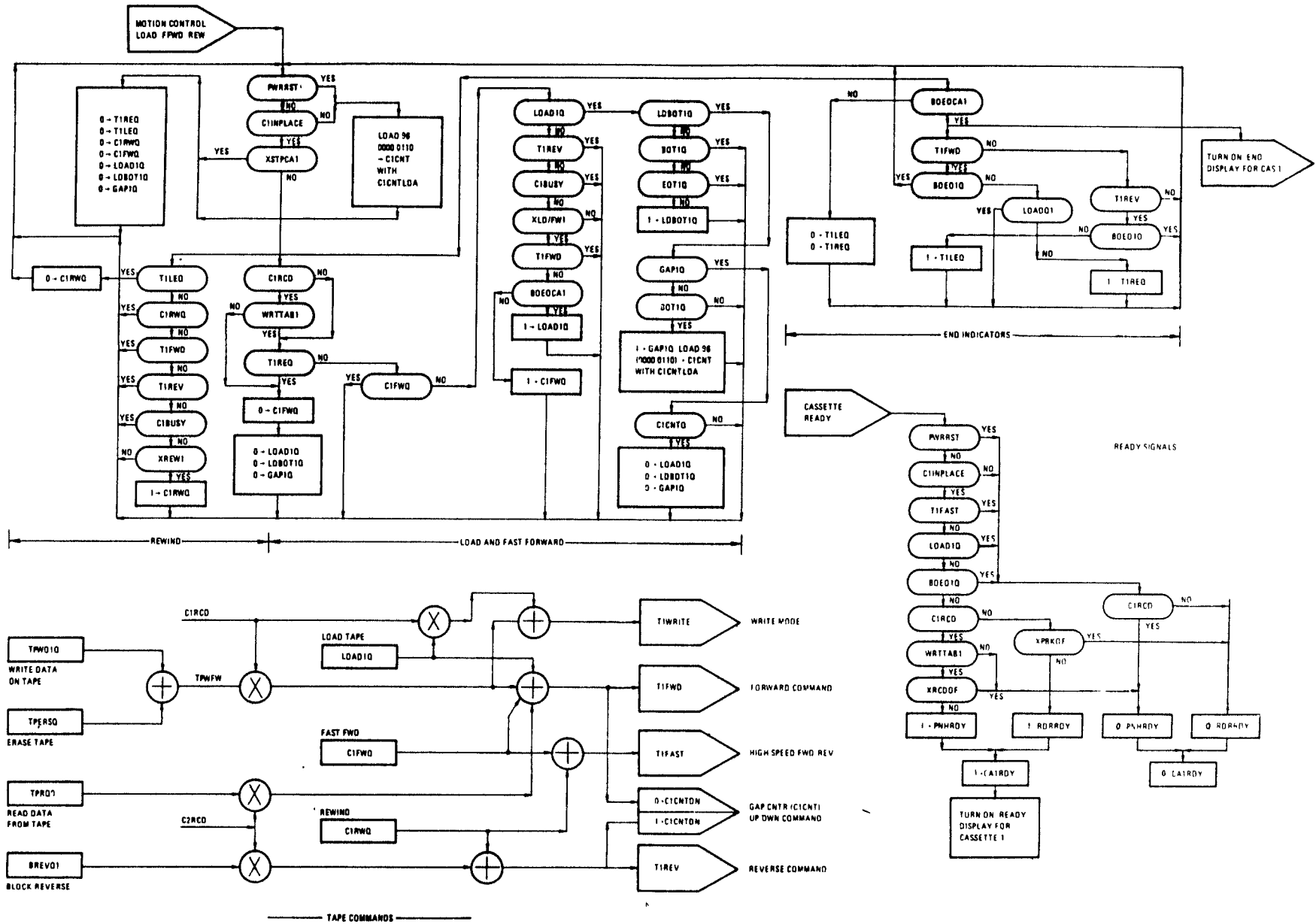


FIGURE 3-8.13. TAPE CASSETTE MOTION CONTROL FLOW DIAGRAM

tape-forward command for the transport, and if the transport is in the record mode, it generates the write command. When the tape reaches the end of clear leader, the BOT flipflop is set (LDB0T1Q). The load controller then waits for BOT to come up (BOT perforation in the tape). When BOT is sensed the gap flipflop is set (GAP1Q), and the gap counter is loaded. The GAP is then written, and the load, BOT and gap flipflops are reset.

3-8.3.3 Fast Forward: To perform fast forward operations the same initial conditions must be met as for load operations, except the tape cannot be on clear leader. When these conditions are met, the forward flipflop is set (C1FWQ). This generates the forward and fast commands for the transport until the right end (TIREQ) is reached or the STOP switch is activated (XSTPCA1).

3-8.3.4 Write. The write command (T1WRITE) is generated when the transport is in the record mode (C1RCD) and

either the load (LOAD1Q), tape write (TPW01Q), or tape erase (TPERSQ) flipflops are set.

3-8.3.5 Forward: The forward command (T1FWD) is generated when the write command (T1WRITE) is generated, or fast forward flipflop is set (C1FWQ), or when the cassette is in playback mode and the read flipflop is set (TPRQ0).

3-8.3.6 Reverse: The reverse command (T1REV) is given when the rewind flipflop is set (C1RWQ) or when the cassette is in the playback mode and the block reverse flipflop is set (BREVQ1).

3-8.3.7 Fast: The fast command is generated when either the fast forward (C1FWQ) or rewind (C1RWQ) flipflops are set.

3-8.3.8 Ready: The ready signal is generated if the cassette

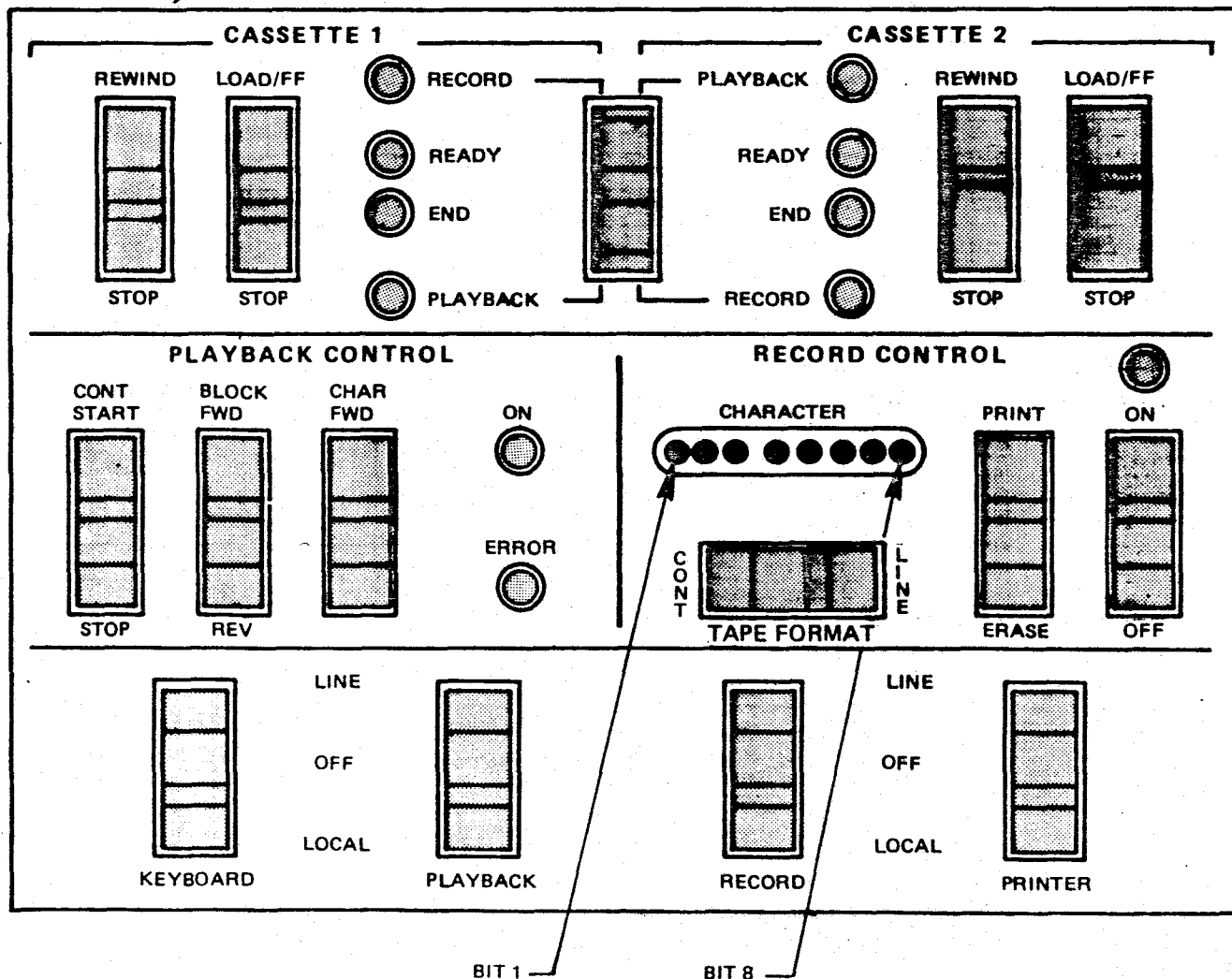


FIGURE 3-8.14. ASR CONTROL AND DISPLAY PANEL

is in place, is not performing fast or load operation, and is not on clear leader. If the above conditions are met and the cassette is in the record mode with a write tab, the READY lamp will illuminate and the recorder ready signal will be generated (PNHRDY) if the record control is not OFF. If the cassette is in the playback mode, the READY lamp will illuminate and the playback ready signal will be generated (RDRRDY) if the playback control is not OFF. If the RECORD or PLAYBACK switches are in the LINE position, the data terminal must also be on-line, or the ready signal will not be generated.

The left end flipflop is set (T1LEQ) when the tape is reversing and the end is sensed. The right end flipflop is set (T1REQ) when the tape is moving forward, not during a load, and the end is sensed.

3-8.4 DISPLAY FUNCTIONS. The Display PC card consists of the switches and indicators necessary to control the tape cassettes. The indicators are light-emitting diodes driven by

open collector TTL gates. The momentary switches on this PC card have debounce circuits consisting of inverter latches. A status register included on this circuit sends information (RFEED, RERROR, BOEOCA1, BOEOCA2, KBDLOC, PRNLOC, PRNOFF) to terminal control in serial form, using status enable (STAENA) and eight clocks (SCLK). The upper display and control panel is shown in Figure 3-8.14.

3-8.5 CASSETTE TRANSPORT. All motion control, read/write, and status-sensing electronics are contained on a single PC card mounted on the rear of the transport (see schematic 960082*, 986357*, or 981337 in Appendix C). A block diagram of the read/write electronics is shown in Figure 3-8.15. Since the head has a single read/write gap, reading and writing cannot occur simultaneously. When writing occurs, the write data appears at the read data outputs.

3-8.5.1 Tape Write Circuit. Writing is inhibited when a write tab is not sensed by the write tab switch. When a write tab

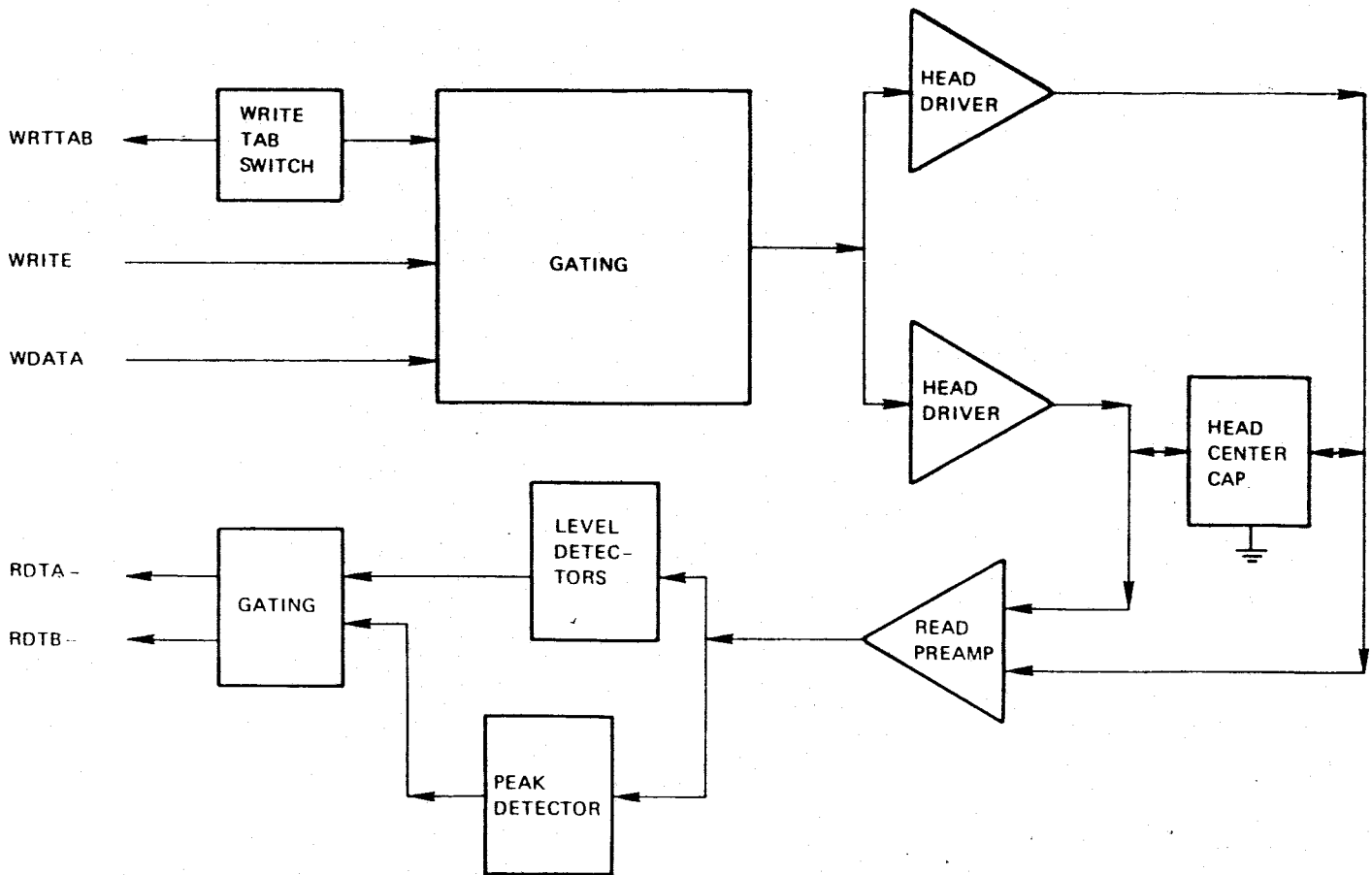


FIGURE 3-8.15. READ/WRITE ELECTRONICS BLOCK DIAGRAM

* This PC card is obsolete.

is present on the cassette and a write command is present on WRITE—, the digital data on WDATA is gated to the head drivers. Each head driver is a current source which forces sufficient current through half of the head coil to saturate the tape.

3-8.5.2 Tape Read Circuit. During a read cycle, the flux reversals on the tape moving past the head cause generation of a voltage across the head coil. This signal is amplified by the read preamp to a level sufficient for use by the peak and level detectors. The level detectors provide noise immunity by allowing only signal peaks above a certain level to reach the output pins. The peak detector detects the point where the head voltage changes direction, which is also the point where the flux of the tape changes direction, and an output data transition occurs. A data transition may occur on RDTA— or RTDB— depending on the direction of the flux change, but the information is contained in the transitions rather than the levels.

3-8.5.3 EOT and BOT Sensors. Optical sensors are used to sense the clear leader at each end of the tape as well as the EOT and BOT perforations in the tape. Light sources (small lamps located in the guide posts directly under the center of the tape guides) are sensed by photo-transistors mounted over holes in the center of the tape guides. The photo-transistor signals are buffered by operational amplifiers and converted to TTL-compatible levels at the card interface.

3-8.5.4 Switches. When actuated, three miniature sensor switches on the tape transport sense that the tape cassette is installed correctly, that the cassette door is closed, and that a write tab is on the cassette. Both the cassette-in-place and door switches must be actuated before the transport will move the tape.

3-8.5.5 Tachometer. The appropriate tachometer signal is available at the card interface for use in keeping up with record locations. The forward tachometer signal is enabled when a forward command (FWD—) is present, and the reverse tachometer signal is enabled when a reverse command (REV—) is present. One tachometer cycle occurs each time 0.0075 inch of tape passes a capstan.

3-8.5.6 Motion Control and Deck Status Electronics. A block diagram of the motion control and deck status electronics is shown in Figure 3-8.16. Tape moved fast in either the forward or reverse direction is controlled by the reel motors. The solenoids are disengaged so the tape does not touch the capstans or the pinch rollers. During read/write operations, the forward or reverse solenoid is engaged, forcing that pinch roller into contact with the tape and capstan. The capstan motor controls the tape motion in this case, while the reel motors supply only enough torque

to keep the tape in tension. The circuits to move tape forward or reverse are identical except that the functions of the forward and reverse components are interchanged.

3-8.5.7 Capstan Control Circuit. The capstan motors are controlled by a phase-locked loop. When a forward command is applied to the transport, the forward solenoid is immediately energized. The forward reel motor torque is increased to provide takeup tension, the forward tachometer signal is gated into the loop, and a 10- to 25-millisecond delay is initiated to allow the pinch roller to engage the tape and capstan. At the end of this delay, the capstan motor driver and the integrator are enabled, completing the servo loop. The initial conditions imposed on the integrator result in an initial motor voltage of approximately 3 volts. As the speed of the tape and capstan motor increases, the frequency of the pulse train from the forward tachometer increases, and the error pulses out of the phase comparator become shorter. When the frequency of the tachometer pulses become higher than the reference frequency, the phase comparator puts out a different pulse train, and the motor voltage is decreased. The steady-state condition is reached when the motor is making small positive and negative excursions from nominal speed. Timing for a typical operation is diagrammed in Figure 3-8.17.

3-8.5.8 Reel Motor Control Circuit (TI Part No. 960331). The reel motors perform three distinct functions, requiring three different amounts of torque. During all operations one reel motor applies a low hold-back torque to the supply tape spool, and both reel motors apply this torque when the transport is idle. During read/write operations additional current is supplied to the reel motor, driving the takeup tape spool so that it applies additional takeup torque. During fast forward and rewind operations 12 volts are applied to the takeup reel motor, resulting in the high torque required to move the tape at an average 60 inches per second (ips). Timing for a typical fast sequence is diagrammed in Figure 3-8.18.

The TI Part No. 986353 transport reel motor control circuit is the same except that the holdback torque is reduced and the takeup torque is decreased during read/write operations.

3-9 OPTIONAL DEVICES.

Several optional functions are available for the 732/733 models as plug-in PC cards, including line interface drives, an answer-back memory, and an auto device controller. The theory of operation of this equipment is explained in this section.

3-9.1 LINE INTERFACE. The standard terminal interface meets requirements of EIA standard RS232C. The terminal

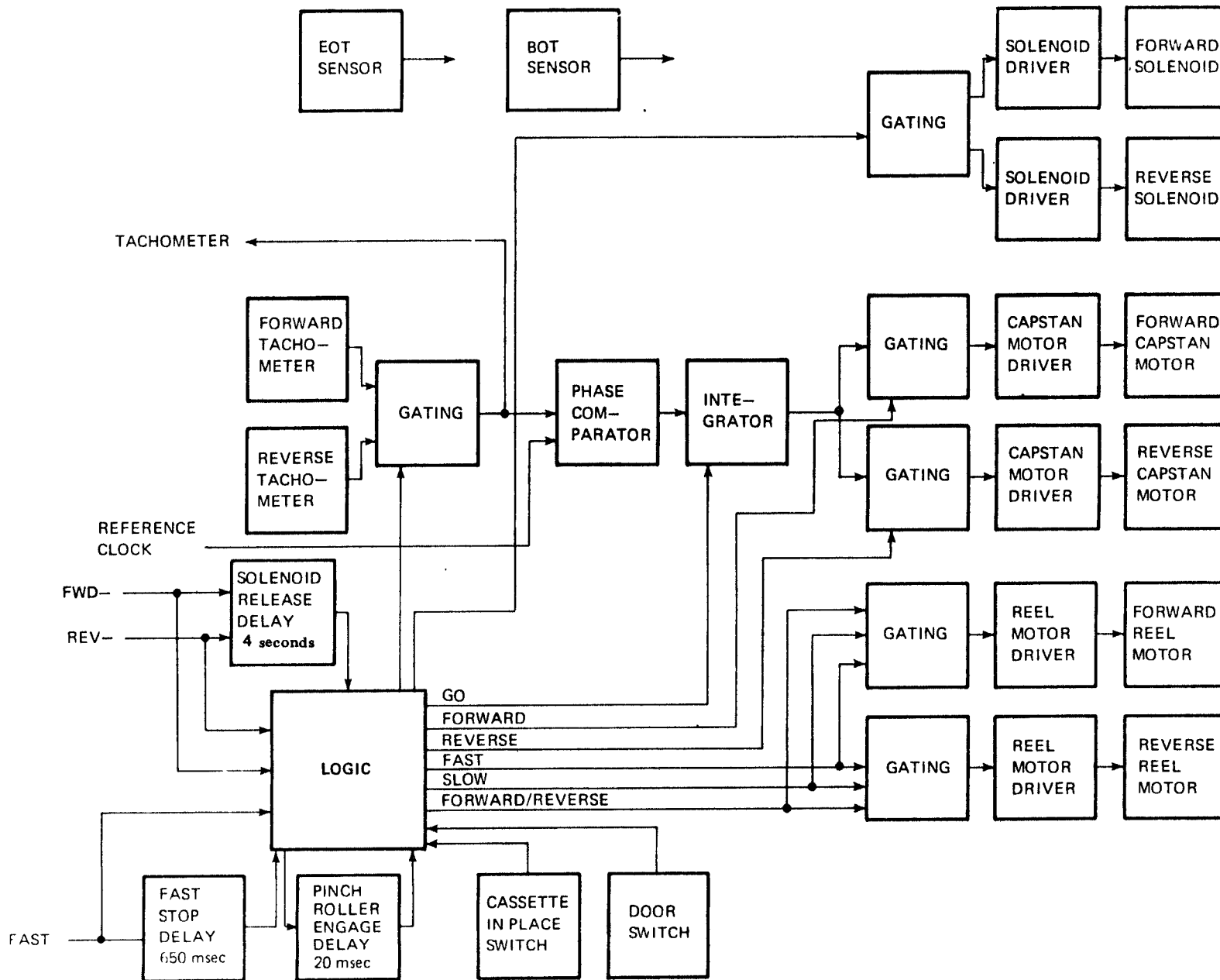


FIGURE 3-8.16. MOTION CONTROL AND DECK STATUS BLOCK DIAGRAM

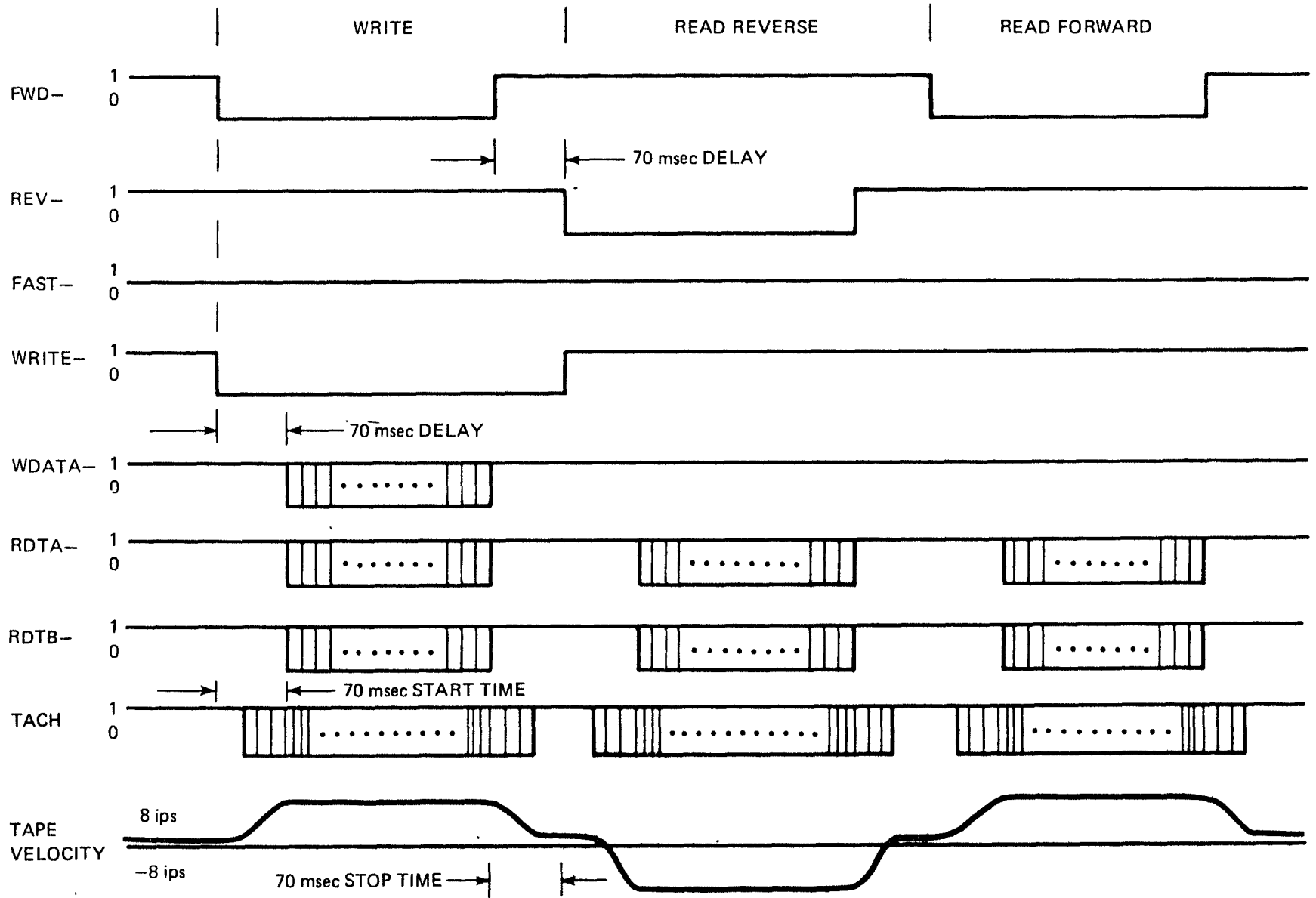


FIGURE 3-8.17. TIMING FOR A TYPICAL WRITE/READ-REVERSE-FORWARD SEQUENCE

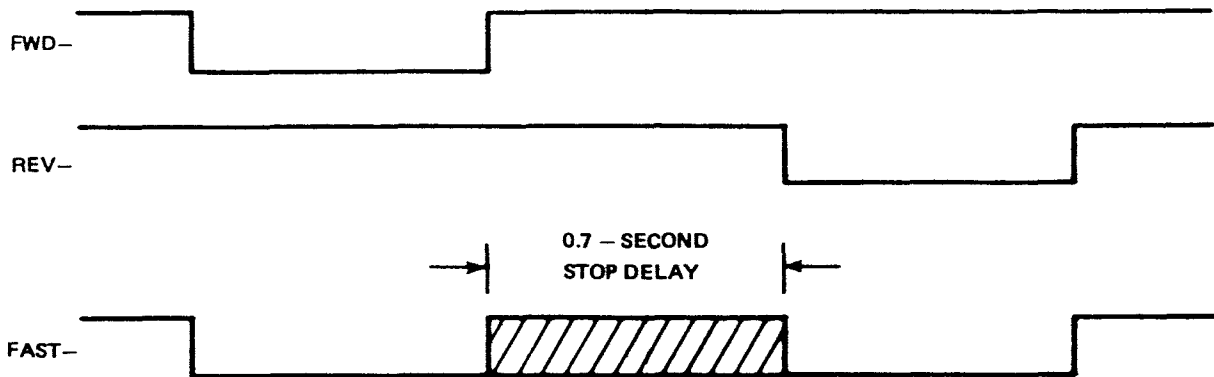


FIGURE 3-8.18. TIMING FOR A TYPICAL FAST-FORWARD/FAST-REVERSE SEQUENCE

can receive without error, signals with mark and space distortion of up to 45 percent. The minimum stop bit time for error free reception at any speed is 0.6 nominal bit time. Four optional line interfaces are available:

- a. TTY current loop - neutral
- b. TTY current loop - polar
- c. Modem - originate mode
- d. Modem - answer mode.

3-9.1.1 Teletype Current Loop – Neutral. The Teletype Current Loop PC card (card slot A8) is divided into two functional sections, receiver and transmitter, described below. A schematic (959192) of this PC card is contained in Appendix C.

- a. Receiver: The teletype (TTY) neutral receiver consists of the necessary circuitry to sense current from an outside source and convert the current levels to appropriate TTL-logic levels. The voltage drop across the receiver inputs (TTYL1 and TTYL2) under working (current

flow) conditions should be less than or equal to 5 volts. The MARK/SPACE nominal threshold decision current at 20mA operation (R34 deleted) should be 10mA ($\pm 26\%$) and at 60mA operation (R 34 installed), should be 30mA ($\pm 20\%$).

The receiver utilizes a differential transistor pair to sense the 10mA or 30mA current level. Upon sensing the decision level the transistor pair switches the current load from one to the other. When the second transistor of the pair starts sinking current through its collector, a voltage sufficient to switch on the optic coupler (Q17) is produced across R31. When the optic coupler transistor turns on, Q11 turns on and switches the appropriate TTL gates to give a TTL-logic level output (logic ONE) corresponding to a mark on the input receiver. Likewise, when the current is below the decision level on the receiver input line, the differential pair switches back to normal, the optic coupler turns off, and the logic level goes back to that (logic ZERO) for a spacing condition on the input receiver line (TTYL1

and TTYL2). Diode CR10 is provided to protect the receiver circuit from line transients.

- b. **Transmitter:** The TTY neutral transmitter consists of the necessary circuitry to sense a TTL-logic level and then, as appropriate, open or close the circuit presented to the transmitter output lines (TTYL3 and TTYL4). When closing the circuit presented to the transmitter output lines (marking), the voltage drop across the lines should be less than 5 volts under nominal current conditions (20mA or 60mA). The circuit utilizes a diode bridge so that the output lines may be connected with either side positive. Under normal circuit conditions the input data (TTYDATOT) is a logic ONE. This input condition causes optical coupler transistors Q13 to be on and Q14 to be off. Since Q14 is off, the amplifier action of Q2, Q4, and Q3 provides sufficient drive to turn on output transistor Q5 which acts as a switch for closing (shorting) the equivalent sending contacts to the outside lines (TTYL3 and TTYL4). Even if power to the terminal is off, the equivalent contacts should remain closed (marking). This is accomplished by diode CR1 and resistors R6 and R7. These three components, using the power provided by the outside line, keep Q1 turned on. Since Q14 is still off when power to the terminal is off, the same conditions apply as when a logic ONE is present at the transmitter input, pin 30 (TTYDATOT), and Q5 remains on, producing a marking condition at the output lines (TTYL3 and TTYL4). To send a spacing condition Q5 must be turned off. This is accomplished by putting a logic ZERO at the transmitter input (pin 30). A logic ZERO input causes Q13 to turn off and Q14 to turn on. With Q14 on, the current provided by Q1 is diverted around the amplifier transistors Q2, Q4, and Q3. and drive to Q5 is insufficient to turn it on. Since Q5 is off the equivalent sending contacts to the outside line (TTYL3 and TTYL4) are open, and a spacing condition exists. CR3 and CR4 are used to protect the transmitter circuit from line transients.

3-9.1.2 Teletype Current Loop – Polar. A schematic (959191) of the TTY polar current loop is contained in Appendix C.

- a. **Receiver:** The TTY polar receiver consists of the necessary circuitry to sense the current

from an outside source and convert the current levels to appropriate TTL-logic levels. The voltage drop across the receiver inputs (TTYL1 and TTYL2) under 20mA or 60mA operation should be less than or equal to 5 volts. The marking-spacing nominal threshold decision current is 0 (± 5) mA.

The receiver circuit utilizes a diode CR10 for protection and an optical coupler to sense the current direction and convert it to TTL-logic levels. When positive current flows from TTYL1 to TTYL2, optical coupler transistor Q17 turns on. When Q17 is on, Q11 is on and a logic ONE is output from the receiver, pin 29 (TTYPATIN). If negative current flows from TTYL1 to TTYL2, optical coupler transistor Q17 turns off, turning off Q11, causing a logic ZERO at the receiver output, pin 29.

- b. **Transmitter:** The TTY polar transmitter consists of the necessary circuitry to sense a TTL-logic level and then, as appropriate, open one set of equivalent contacts and close one set of equivalent contacts to the outside transmitter lines (TTYL3 and TTYL2 or TTYL4 and TTYL2). When closing the circuit presented to the transmitter output lines (marking), the voltage drop across the lines should not exceed 5 volts under nominal current conditions (20mA or 60mA). Operation consists of two identical circuits which complement each other so that equivalent contacts between transmitter output lines TTYL3 and TTYL2 and TTYL4 and TTYL2 are always in opposite states; i.e.. when one set is open, the other set is closed and vice versa. Each transmitter output utilizes a diode bridge arrangement, so that polarity of outside sources is immaterial. When the input data (pin 30) is a logic ONE, optical coupler transistors Q13 and Q16 are on, and optical coupler transistors Q14 and Q15 are off. Since Q13 is on and Q14 is off, current supplied by Q1 is amplified by Q2, Q4, and Q3; therefore, sufficient drive is available to turn on Q5 and close the equivalent contacts between TTYL3 and TTYL2. Conversely, in the other driver circuit Q15 is off and Q16 is on; therefore, no current is supplied to transistor amplifier Q7, Q8, and Q9, keeping Q10 off and the equivalent contacts between TTYL4 and TTYL2 open. If power to the terminal is off, the same situation exists.

Since Q15 is still off, no current is supplied to the transistor amplifier Q7, Q8, and Q9; thus, Q10 is still off and the equivalent contact between TTYL4 and TTYL2 is still open. Conversely, due to diode CR1 and resistors R6 and R7, the outside power supplied by the line maintains Q1 on; and since Q14 is off, the transistor amplifier Q2, Q4, and Q3 apply sufficient drive to turn on Q5 and keep closed the equivalent contacts between TTYL3 and TTYL2. This maintains a "working" condition on the line, even when power to the terminal is off. When the input data to the transmitter (pin 30) changes to a logic ZERO, the optical coupler transistors change (Q14 and Q15 on; Q13 and Q16 off); the transistor amplifier for TTYL3 (Q2, Q4, Q3) turns off; the transistor amplifier for TTYL4 (Q7, Q8, Q9) turns on; and transistor outputs Q5 and Q10 switch the equivalent contacts to the outside line, putting TTYL3 to TTYL2 open and TTYL4 to TTYL2 closed. Diodes CR3, CR4, CR6, and CR7 are used to protect the transmitter circuits from line transients.

3-9.1.3 Teletype Current Loop – Computer. The Teletype Current Loop PC card (slot A8) is divided into two functional sections, receiver and transmitter. A schematic (966657) of this PC card is contained in Appendix C.

- a. Receiver: The TTY computer receiver consists of the necessary circuitry to sense current from an outside source (typically a computer) and convert the current levels to appropriate TTL-logic levels. The voltage drop across the receiver input terminals (TTYL1 and TTYL2) under working (current flow) conditions should be 2.7 volts or less. The MARK/SPACE nominal threshold decision current for 13 mA operation should be 6.5 mA \pm 20 percent.

When current is flowing on the line, a voltage sufficient to switch on the optical coupler (Q17) is produced across R31. When the optical coupler transistor turns on, Q11 turns on and switches the appropriate TTL gates to produce a TTL-logic level output (logic ONE) corresponding to a MARK on the input receiver. Likewise, when the current is below the decision level, the optical coupler turns off and the logic level goes to that (logic ZERO) for a SPACE condition on the receiver line (TTL1 and TTL2). Diode CR10 is provided to protect the receiver circuit from line transients.

- b. Transmitter: The TTY computer transmitter consists of the necessary circuitry to sense a TTL-logic level and then, as appropriate, open or close the circuit presented to the transmitter output lines (TTYL3 and TTYL4). When closing the circuit presented to the transmitter output lines (marking), the voltage drop across the lines should be less than 1.2 volts under nominal current conditions (13 mA).

Under normal circuit conditions the input data (TTYDATOT) is a logic ONE. This input condition causes optical coupler transistors Q13 to be on and Q14 to be off. With Q14 off, sufficient drive is provided by the current flow through Q13 to turn on Q4, which acts as a switch to close (short) the equivalent sending contacts to the outside lines (TTYL3 and TTYL4).

To send a spacing condition Q4 must be turned off. This is accomplished by putting a logic ZERO at the transmitter input (pin 30). A logic ZERO input causes Q13 to turn off and Q14 to turn on. With Q14 on, drive is insufficient to turn Q4 on. Since Q4 is off, the equivalent sending contacts to the outside line (TTYL3 and TTYL4) are open and a spacing condition exists.

3-9.1.4. TL Modem – Originate Mode. The TL Modem is an originate-mode PC card modem, designed to communicate with the comparable answer-mode (TH) modem. The transmitter section of the TL Modem converts a MARK level (EIADATOT low) from the serial transmitter into a MARK (1270 Hz) frequency on the transmission line and converts a SPACE level (EIADATOT high) into a SPACE (1070 Hz) frequency on the transmission line. The TL modem receiver section converts a received MARK (2225 Hz) frequency on the transmission line into a MARK level (EIADATIN low) for the serial receiver and converts a received SPACE (2025 Hz) frequency on the transmission line into a SPACE level (EIADATIN high) for the serial receiver. Modulation and demodulation processes may be carried out for data rates up to 300 baud. A block diagram of the TL modem is shown in Figure 3-9.1.

- a. Reference Regulator Circuit: The reference regulator circuit provides high frequency filtering for the +12Vdc and -12Vdc terminal power supply bus connections to the TL Modem PC card. The circuit's other function is to develop stable, low impedance, reference voltage sources for the other circuits on the PC

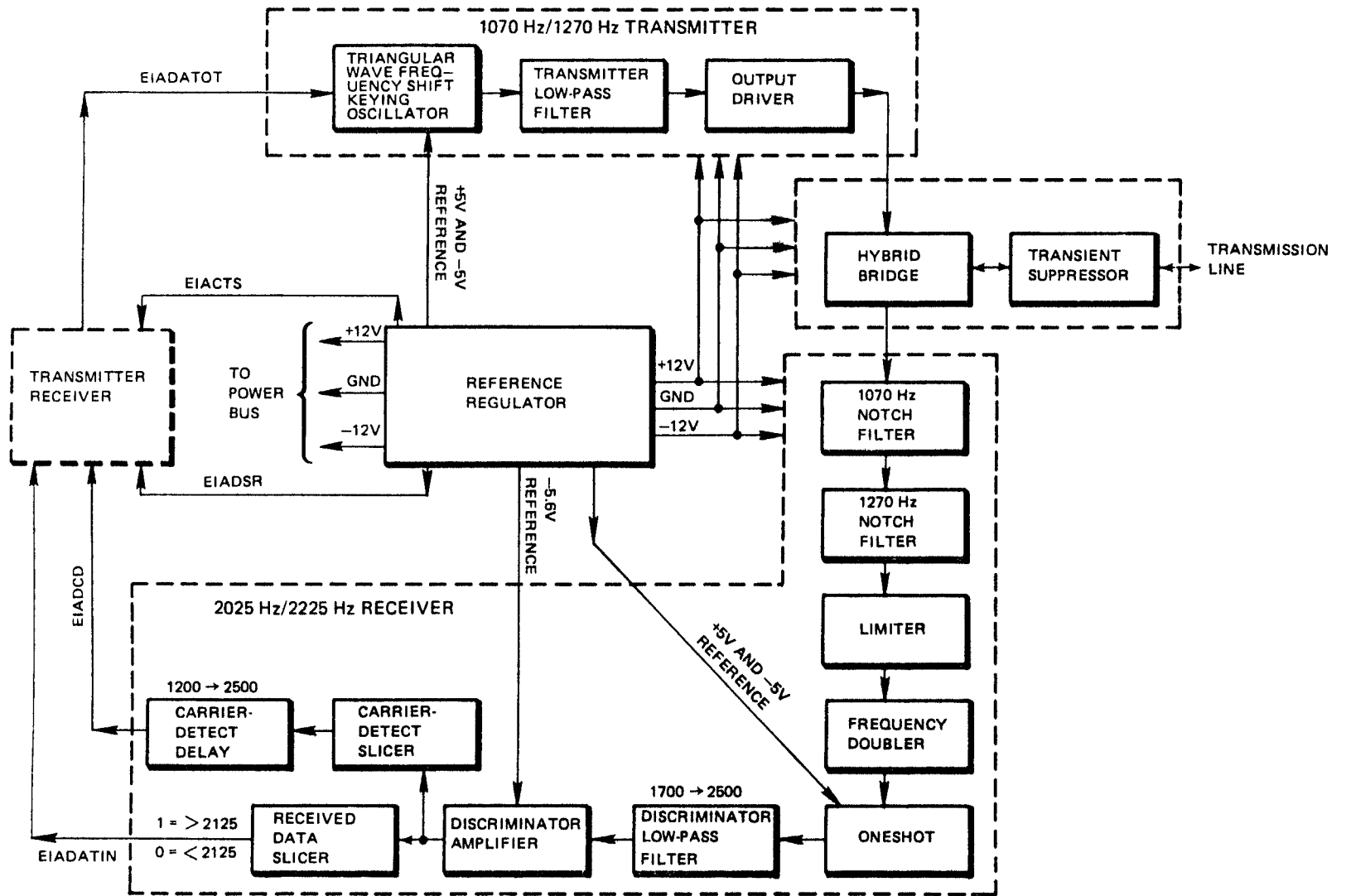


FIGURE 3-9.1. ORIGINATE-MODE (TL) MODEM FUNCTIONAL BLOCK DIAGRAM

card. The circuit includes two complementary emitter followers (Q6, Q7), whose output voltages track the voltage developed across the matched pair of zener diodes CR4/CR5. The anode of CR5 also provides -5.6 volts for use in the receiver discriminator amplifier circuit as a bias reference to track the +5V and -5V reference voltages. Data-set-ready and clear-to-send are held high through R38 and R29 whenever power is applied to the terminal.

- b. **Transmitter Triangular Wave Oscillator:** The transmitter triangular wave oscillator is the source of 1070 Hz (SPACE) and 1270 Hz (MARK) transmitted frequencies. The oscillator frequency is controlled by the EIADATOT signal from the transmit/receive PC card. The output of AR1 is fed back to the noninverting input of AR1 through R3, and the output of AR1 is driven into positive or negative saturation. For purposes of explanation, assume that AR1 is initially driven into negative saturation. CR1 is back-biased and CR2 is forward-biased, clamping the voltage at the cathode of CR2 to -5.6 Vdc. The constant negative voltage at the input to the voltage divider network (consisting of R6 through R9) causes the output of the inverting integrator circuit (AR3, R10, C8) to ramp upward linearly with time. The rate at which the ramp rises is determined by the current flowing into the summing node (inverting input) of AR3. The output voltage of AR3 continues to rise to about +3.73 Vdc, at which time the voltage at the noninverting input of AR1 becomes slightly positive because of the R2/R3 voltage divider between the output of AR3 and the cathode of CR2. The positive voltage at the noninverting input of AR1 causes AR1 to go into positive saturation, back-biasing CR2 and forward-biasing CR1 to clamp the voltage at the anode of CR1 to +5.6 Vdc. The constant positive voltage at the input to the voltage divider (R6 through R9) causes the output of AR3 to ramp downward from +3.73 Vdc toward -3.73 Vdc. When the voltage at the output of AR3 reaches -3.73 Vdc, the noninverting input of AR1 is forced negative, and AR1 rapidly reverses states, going into negative saturation again. This action completes a single cycle of the oscillator.

In order to change the frequency of the oscillator waveform, the magnitude of the input current supplied to the integrator is changed by switching the shunt leg of the attenuator (R8, R9) to ground. When the EIADATOT line is high, Q4 is turned off, and Q5 is held pinched off by -12 Vdc through R31. This action opens the R8/R9 leg of the attenuator, allowing all the current available at the cathode of CR2 to flow to or from the integrator input summing junction (AR3-2). The maximum amount of the current, and hence the maximum slope of the integrator output ramp, is determined by adjusting R7. Since the higher the slope, the shorter the time per oscillator cycle, the higher transmitter (MARK) frequency (1270 Hz) is set by adjusting R7 with the EIADATOT line held high. The lower (SPACE) transmitter frequency (1070 Hz) is produced when Q5 is no longer pinched off by the action of Q4. Since the on-resistance of Q5 is only about 20 ohms, the shunt leg (R8, R9) of the attenuator is essentially switched into the circuit, reducing the current flowing through R10 to or from the integrator summing junction input (AR3-2). The magnitude of the current flowing in the shunt leg of the attenuator is adjusted by means of the pot R9 while the transmitted-data line is held low. It is important to note that the adjustments for MARK and SPACE frequencies are interactive, inasmuch as R7 controls the integrator input current whether the shunt leg of the attenuator is switched in or out of the circuit. Hence, the MARK frequency (1270 Hz) must be set by R7 before setting the SPACE frequency (1070 Hz) with R9.

- c. **Transmitter Low-Pass Filter:** The triangular wave output from the transmitter oscillator circuit is altered to produce a low distortion sine wave at the oscillator fundamental frequency by attenuating all harmonics of the fundamental with the transmitter's low-pass filter (R11-R13, C9-C12, and AR4).
- d. **Transmitter Output Driver:** The transmitter output driver circuit consists of variable attenuator R18 from the output of the transmitter low-pass, followed by noninverting voltage follower AR6. By adjusting the wiper position on R18, the output level transmitted

may be adjusted over the range from +5 dBm to less than -40 dBm.

- e. **Communication Line Transient Suppressor Circuit:** The zener diodes CR7 and CR8 are 6.8-volt units rated at 5 watts. Their function is to limit the difference-mode signal amplitude at the primary (transmission line side) of transformer T1 to an absolute maximum of about 7.5 volts. Chokes L3 and L4, in conjunction with high voltage capacitors C18 and C19 and associated circuit resistances, form low-pass filter sections which limit the coupling of high frequency common mode signals (spikes, etc.) from the primary to the secondary of T1.
- f. **Hybrid Bridge Circuit:** The hybrid bridge circuit performs three important functions. First, it provides the proper driving and terminating impedance to match the modem to the transmission line. Second, it provides isolation between the transmitter and receiver of the modem to prevent a strong transmitted signal from swamping out a small received signal. Third, the bridge components are chosen to limit the bandwidth of the modem receiver.

The bridge's operation is dependent on the balancing of the impedance in its two arms: R14/R39 and R17/R41/T1. For balancing considerations R15 may be neglected, since the very large input impedance of operational amplifier AR5 does not load it. Consider the case when the modem is transmitting into a 600-ohm transmission line termination on which no other signal is impressed. The resistors R14, R39, R17, and R41 are chosen so that the ratio of values of R14 to R39 equals the ratio of values of R17 to the series combination of R41, the line impedance (600 ohms, reflected through 1:1 transformer T1), and the equivalent winding resistance of T1. Since R39 provides negative feedback around AR5, the difference voltage between the inverting and noninverting inputs to AR5 is driven to zero. Since the difference voltage from AR5-2 to AR5-3 is zero, and the bridge resistances are proportional, the voltage across R14 equals the voltage across R39. This means that the voltage across R39 must equal the voltage from AR5-3 to ground; i.e., the output of the bridge (AR5-6) is identically zero. Therefore, the

bridge provides 30 to 35 dB attenuation between the transmitter and receiver.

With the transmitter off AR6-6 will be at ground, and the input impedance to the modem appears as a series combination of R17, R41, and the resistance of the secondary winding of T1 (typically slightly over 600 ohms for the total). This combination is set to 600 ohms so as to match the transmission line impedance. The total input impedance is tapped by AR5-3 via R15 between R41 and R17; thus, about 5/6 of the input signal is present at the noninverting input to AR5. Since R14 is at signal ground with respect to receiving signals from the transmission line, the overall gain is approximately 2.0 from the communication line input to the output of AR5 (input to receiver).

The receiver input bandwidth is limited by the simple RC low-pass filter formed by R15 and C16. This filter has a cutoff (3 dB) frequency of about 4.4 kHz and a rolloff rate of -6 dB per octave.

- g. **1070-Hz Notch Filter Circuit:** AR7 and its associated twin-tee network provides a very narrow, band-elimination filter centered at the transmitter SPACE frequency of 1070 Hz. The function of the filter is to severely attenuate any 1070-Hz output signal from the transmitter which "leaks" through the hybrid bridge circuit to the receiver input.
- h. **1270-Hz Notch Filter Circuit:** AR8 and its attendant twin-tee network provide a very narrow, band-elimination filter centered at the transmitter MARK frequency of 1270 Hz. The function of the filter is to severely attenuate any 1270-Hz output signal from the transmitter which "leaks" through the hybrid bridge to the receiver input.
- i. **Limiter Circuit:** The limiter circuit has two functions. The first function is to produce a square wave output which switches as closely as possible to the zero crossing in the input waveform. The output wave switches between +5.4 and +0.25 Vdc. The high output voltage is set by resistor divider R54/R61 to +12Vdc. The low output voltage is set by the saturation voltage of the output stage of AR9. The second

function of the limiter circuit is to determine the sensitivity of the receiver. The sensitivity of the limiter may be varied by feeding back a small portion of the output waveform to establish the threshold voltage through which the limiter input must pass in order to cause an output transition. The greater the amplitude of this positive feedback voltage, the larger the input signal must be to cause a transition at AR9-7.

C30, R51, R52, and C31 form a rudimentary bandpass filter with nominal (-3 dB) cutoff frequencies of 1040 Hz and 88.4 kHz. This filter further restricts the bandwidth to which the receiver is sensitive. Since C30 couples the limiter circuit to the preceding receiver stage, the input signal applied to the inverting input of the comparator (AR9-3) has no dc component. The band-limited input signal is therefore an ac signal twice the amplitude of the received signal on the transmission line, since the hybrid bridge provides a gain of two. The (positive) feedback signal supplied to the noninverting input AR9-2 must also be an ac signal with no dc component, but the voltage at AR9-7 never goes negative.

A pull-down network composed of R55 and R56 provide the driving potential to pull the feedback signal below ground. Pot R56 provides adjustment to compensate for variation in input offset voltage as well as tolerance variations in R54, R61, and +12 Vdc. Pot R53 provides an additional capability to compensate for input offset voltage in AR9. When a valid input signal is presented to the modem receiver after the carrier detect has been in the off (low) state, FET Q8 is held off and a ± 2 mV signal is presented to the noninverting input of AR9 through the attenuator composed of R57 + R59 and R58. If, for example, the input voltage at AR9-3 is sufficiently negative to cause the output stage of AR9 to cut off, the voltage at AR9-7 rises to +5.4 Vdc, applying about +2 mVdc to AR9-2.

Before the output stage of AR9 can saturate again, the signal at AR9-3 must go higher than the +2 mVdc set at AR9-2. This means that the limiter cannot respond to modem input signals smaller than 1 mV peak (approximately -54 dBm) if Q8 is pinched off. If Q8 is turned on, the positive feedback voltage at AR9-2 is limited to ± 0.6 mVdc swings, thus allowing the

comparator to switch states for modem input signals of 0.3 mV peak (-64 dBm).

The two sensitivity settings of the limiter are controlled by the carrier detect slicer circuit. If no data has been received for some time, carrier detect is low, pinching Q8 off and setting the sensitivity to -54 dBm. When carrier detect is high, Q8 is turned on, increasing the sensitivity to -64 dBm. The higher sensitivity is provided to allow the accurate reproduction of input signal zero crossings by the limiter when the input level is low.

- j. Frequency Doubler Circuit: The squarewave output from the limiter is applied to the frequency doubler where the wave train is differentiated and essentially full-wave-rectified to obtain a train of trigger pulses with a constant amplitude and a repetition rate of twice the incoming signal (and limiter output).

The output of the limiter circuit switches between approximately +0.25 Vdc and +5.4 Vdc; this waveform is applied to R62 and C32. When the limiter output switches to +5.4 Vdc, a short positive-sloped spike is coupled through C32 to the cathode of CR10 where it is blocked from passing to the base of Q10. The high-going limiter output also supplies base drive through R62 to the base of Q9, saturating Q9 and coupling a negative-sloped spike through C33 and CR9 to the base of Q10. When a low-going spike is applied to the base of Q10, it causes a high-going spike at the collector of Q10. Similarly, when the limiter output goes low, a negative-sloped spike is applied to the base of Q10 through C32 and CR10, causing a high-going spike at the collector of Q10. If the output of the limiter is a 50 percent duty-cycle waveform, the train of pulses at the frequency doubler output (Q10 collector) will have exactly twice the frequency of the frequency doubler output waveform. Q10 further acts as a buffer amplifier, providing a low output impedance source of trigger pulses to the oneshot while isolating the differentiating capacitors C32 and C33 from the positive feedback voltage around the amplifier AR10 in the oneshot.

- k. Receiver Oneshot Circuit: The output pulses from the frequency doubler circuit trigger the oneshot to produce a rectangular pulse train. The change in average dc value of this

rectangular pulse train is directly proportional to the change in repetition rate of the trigger pulses and, hence, proportional also to the change in input signal frequency.

In its stable (inactive) state oneshot amplifier AR10-6 is in negative saturation, and the oneshot output (cathode of CR12) is clamped to -5.6 Vdc through CR12. The negative output voltage is fed back to the noninverting input of AR10 through the voltage divider comprised of R69 and R70, holding the noninverting input to -2.8 Vdc. The negative saturation voltage at AR10-6 is also applied to a voltage divider formed by R75 and R74, saturating the collector of Q11 at approximately 0 Vdc. This action holds the ungrounded side of the timing capacitor C34 (inverting input of AR10) very close to ground through R82. Since the noninverting input voltage (-5.4 Vdc) is less than the inverting input voltage (approximately 0 Vdc), the amplifier is latched in negative saturation, holding the oneshot output in its stable state.

When a high-going pulse is applied to the noninverting input of AR10 from the collector of Q10 (low impedance source), the noninverting input of AR10 is made more positive than the inverting input of AR10 (0 Vdc). This condition causes AR10 to switch from negative saturation to positive saturation, and the metastable (active) state of the oneshot is initiated. The oneshot output is bounded to +5.6 Vdc by the clamping action of CR11, and the output voltage is divided by R70 and R69 and applied to the noninverting input of AR10. The positive voltage at AR10-6 causes Q11 to cut off and C34 begins to charge from 0 Vdc toward +5.6 Vdc through the combination of R72, R73, and R76, with the setting of R76 establishing the rate of charge. Since the voltage at the inverting input of AR10 is initially less than the +2.8 Vdc at the noninverting input, the output of AR10 is latched in positive saturation. Finally, when C34 has charged up higher than +2.8 Vdc, the voltage at the inverting input of AR10 exceeds the voltage at the noninverting input of AR10, and the output of AR10 switches to negative saturation. This causes Q11 to saturate, quickly discharging C34 through R71, and the oneshot resumes its stable state.

The adjustment range of R76 allows the oneshot (metastable) period to be set for a (positive) duty cycle of 25 percent when the trigger pulse frequency equals 4250 pulses per second. This frequency is produced when an input signal of 2125 Hz is applied successively to the modem receiver limiter and frequency doubler stages.

- l. Receiver Discriminator Low-Pass Filter Circuit: The rectangular output waveform from the oneshot circuit is fed into the discriminator low-pass filter circuit. Since the cutoff frequency of this filter (150 Hz) is so much lower than the repetition frequency of the oneshot output pulses, the filter acts essentially as an analog integrator. The filter output, then, is a dc voltage equal to the average value of the oneshot pulse train voltage. A change in input frequency thus causes a proportional change in the filter output voltage.
- m. Discrimination Amplifier Circuit: The discriminator amplifier modifies (biases and amplifies) the output signal from the discriminator low-pass filter to make it easier to compare in the received-data slicer and the carrier-detect slicer circuits.

The nominal swing in the discriminator low-pass filter output, which corresponds to a SPACE-frequency-to-MARK-frequency transition at the receiver input, is from -2.93 Vdc to -2.67 Vdc. It is convenient to translate this voltage swing upward so that the decision as to whether the output voltage of the discriminator filter is high or low (corresponding to MARK or SPACE received frequencies, respectively) may be made about ground potential. Such a translation is provided by the discriminator amplifier. When the receiver input frequency is 2125 Hz, the oneshot pulse width is adjusted so that the discriminator amplifier output voltage is zero.

In addition to providing convenient positive translation of the discriminator output voltage, the discriminator amplifier also applies a gain of nearly +25 to the output swing of the discriminator low-pass filter. This additional gain allows the output of the amplifier to swing from -3.25 Vdc for a SPACE (2025 Hz) input

to +3.25 Vdc for a MARK (2225 Hz) input with 0 Vdc corresponding to the mid-band frequency of 2125 Hz.

- n. **Received-Data Slicer Circuit:** The received-data slicer circuit monitors the output voltage of the discriminator amplifier, providing a MARK level to the XMT/RCV logic for any input signal whose frequency is 2125 Hz or higher. It produces a SPACE level to the XMT/RCV logic for any input signal whose frequency is less than 2125 Hz.

When the discriminator amplifier output voltage (AR15-6) is higher than 0 Vdc (corresponding to a MARK input frequency), the inverting input voltage to comparator AR16 is made more positive than noninverting input voltage which is fixed at ground potential. This causes the output of AR16 to saturate, pulling the EIADATIN line to -12 volts through R101. When the discriminator amplifier output voltage is less than 0 Vdc (corresponding to a SPACE input frequency condition), the inverting input voltage to AR16 is made more negative than the noninverting input voltage (0 Vdc). This causes the output stage of AR16 to saturate positive, causing the EIADATIN line to reach +12 volts through R101.

The positive feedback around AR16, provided through R93, decreases the change of comparator output parasitic oscillations as the noninverting input slews through the region near 0 Vdc. It also provides a margin of immunity (approximately 2 mV) to small ripples present at the discriminator amplifier output.

The presence of R91 and C43 provides some additional filtering of the discriminator amplifier output to attenuate any high frequency transients present.

- o. **Carrier Detect Slicer Circuit:** The carrier-detect slicer circuit monitors the output voltage of the discriminator amplifier, providing an in-band signal to the carrier-detect delay circuit for any input signal whose frequency lies between 1950 Hz and 2300 Hz. It produces an out-of-band signal to the carrier-detect delay circuit for any input signal frequency below 1950 Hz or above 2300 Hz.

The biasing of the matched pair of zener diodes CR14/CR15 from the +12 Vdc and -12 Vdc supply buses through R88 and R90 establishes the voltage drops across the zeners at very nearly 5 Vdc. Thus, as the output voltage of AR15-6 is applied to the cathode of CR15 (anode of CR14), the voltage at the cathode of CR14 is set 5 volts above the discriminator amplifier output voltage. Similarly, the voltage at the anode of CR15 is set 5 volts below the discriminator amplifier output voltage.

So long as the voltage at AR15-6 lies in the range -5.6 Vdc to +5.6 Vdc, both diodes CR13 and CR18 remain back-biased and the small positive voltage set by the divider R89/R95 holds AR13 in positive saturation (since with CR13 and CR18 back-biased, AR13-3 is slightly positive and R94 is grounded through R94).

If the voltage at AR15-6 rises about +5.6 Vdc, CR13 remains back-biased but CR18 is forward-biased, increasing the voltage at AR13-2 above that at AR13-3. This condition causes AR13-6 to switch to its negative saturation voltage, indicating carrier-out-of-band.

If the voltage at AR15-6 falls below -5.6 Vdc, CR18 remains back-biased but CR13 is forward-biased, reducing the voltage at AR13-3 below that at AR13-2. This condition causes AR13-6 to switch to its negative saturation voltage, indicating carrier-out-of-band.

- p. **Carrier Detect Delay Circuit:** The carrier-detect delay circuit provides an in-band (EIADCD high) level to the transmit/receive logic in accord with the in-band signal from the carrier-detect slicer circuit. The rising transition in the carrier-detect signal to the transmit/receive logic is delayed until a nominal 150 msec after the carrier-detect slicer in-band indication is given. The carrier-detect delay circuit also provides an out-of-band (EIADCD low) level to the transmit/receive logic, corresponding to the out-of-band signal from the carrier-detect slicer circuit. The falling transition in the EIADCD signal is delayed until a nominal 100 msec after the carrier-detect slicer out-of-band indication is given.

When the carrier detect slicer output (AR13-6) is positively saturated, the base-emitter junction of Q12 is forward-biased, and its collector saturates at about +0.5 Vdc. In this state CR16 is back-biased approximately 11 volts with +0.5 Vdc at its anode. This small positive voltage allows the N-channel FET Q8 to turn on, causing the limiter sensitivity to increase. The forward-biased base-emitter diode drop from Q12 appears across C44 and as a reverse bias across CR17. The base-emitter drop also holds AR14-3 at +0.6 Vdc, causing the output stage of AR14 to saturate positive and hold the carrier detect line (EIADCD) to +12 volts.

If a loss of in-band carrier causes the voltage at AR13-6 to switch to negative saturation, Q12 is immediately turned off and CR16 is forward-biased through R96 to clamp the gate of Q8 to approximately -11 Vdc. These conditions quickly pinch off Q8, switching the limiter sensitivity to its lower level. The carrier-detect "dropout" delay cycle begins as Q12 is cut off and the voltage between R97 and C44 slowly decreases from +0.6 volts as C44 is discharged toward the saturation voltage of AR13 through R97. The output stage of AR14 remains cut off and carrier detect remains at +12 volts until the voltage between R99 and C44 goes slightly negative, approximately 50 msec after AR13 goes into negative saturation. When the voltage at AR14-2 goes negative, the output stage of AR14 is saturated and the carrier-detect line is switched to -12 volts.

After the carrier-detect line has been low for some time, the voltage between C44 and R99 is clamped to -2 volts by the forward-biased multipellet diode CR17 (CR17 serves to limit the differential voltage between AR14-2 and AR14-3, while establishing a 2-volt reference across C44). If the output of the carrier-detect slicer (AR13-6) switches from negative to positive saturation, indicating the presence of in-band data on the transmission line, C44 begins to charge from -2 volts toward the positive saturation output voltage of AR13 through R97. When the voltage between R99 and C44 goes slightly positive (150 msec after switching of AR13), the output stage of AR14 is cut off and the carrier-detect line is pulled up

to +12 volts. C44 continues to charge up to +0.6 volts, at which time Q12 is saturated and the clamping action of the forward base-emitter diode halts the charging process. As Q12 saturates it quickly pulls the gate voltage at Q8 from approximately -11 to +0.5 volts, turning Q12 on and increasing the sensitivity of the receiver limiter.

3-9.1.5 Modem-Answer Mode (TH). The TH Modem is an answer-mode PC card modem, designed to communicate with the comparable originate-mode TL Modem. The transmitter section of the TH Modem converts a MARK level (EIADATOT low) from the serial transmitter into a MARK (2225 Hz) frequency on the transmission line and converts a SPACE level (EIADATOT high) into a SPACE (2025 Hz) frequency on the transmission line. The TH Modem receiver section converts a received MARK (1270 Hz) frequency on the transmission line into a MARK level (EIADATIN low) for the serial receiver and converts a received SPACE (1070 Hz) frequency on the transmission line into a SPACE level (EIADATIN high) for the serial receiver. Modulation and demodulation may be carried out for data rates up to 300 baud. A block diagram of the TH Modem is shown in Figure 3-9.2.

- a. **Reference Regulator Circuit:** The reference regulator circuit provides high frequency filtering for the +12 Vdc and -12 Vdc terminal power supply bus connections to the TH Modem PC card. The circuit's other function is to develop stable, low impedance, reference voltage sources for the other circuits on the PC card. The circuit includes two complementary emitter followers (Q6, Q7) whose output voltages track the voltage developed across the matched pair of zener diodes CR4/CR5. The anode of CR5 also provides -5.6 volts for use in the receiver discriminator amplifier circuit as a bias reference to track the +5V and -5V reference voltages.

Data-set-ready and clear-to-send are held high through R38 and R29 whenever power is applied to the terminal.

- b. **Transmitter triangular Wave Oscillator:** The transmitter triangular wave oscillator is the source of 1070 Hz (SPACE) and 1270 Hz (MARK) transmitted frequencies. The oscillator frequency is controlled by the EIADATOT signal from the transmit/receive. The output of

AR1 is fed back to the noninverting input of AR1 through R3, and the output of AR1 is driven into positive or negative saturation. For purposes of explanation, assume that AR1 is initially driven into negative saturation. CR1 is back-biased and CR2 is forward-biased, clamping the voltage at the cathode of CR2 to -5.6 Vdc. The constant negative voltage at the input to the voltage divider network (consisting of R6 through R9) causes the output of the inverting integrator circuit (AR3, R10, C8) to ramp upward linearly with time. The rate at which the ramp rises is determined by the current flowing into the summing node (inverting input) of AR3. The output voltage of AR3 continues to rise to about +3.73 Vdc, at which time the voltage at the noninverting input of AR1 becomes slightly positive because of the R2/R3 voltage divider between the output of AR3 and the cathode of CR2. The positive voltage at the noninverting input of AR1 causes AR1 to go into positive saturation, back-biasing CR2 and forward-biasing CR1 to clamp the voltage at the anode of CR1 to +5.6 Vdc. The constant positive voltage at the input to the voltage divider (R6 through R9) causes

the output of AR3 to ramp downward from +3.73 Vdc toward -3.73 Vdc. When the voltage at the output of AR3 reaches -3.73 Vdc, the noninverting input of AR1 is forced negative, and AR1 rapidly reverses states, going into negative saturation again. This action completes a single cycle of the oscillator.

In order to change the frequency of the oscillator waveform, the magnitude of the input current supplied to the integrator is changed by switching the shunt leg of the attenuator (R8, R9) to ground. When the EIADATOT line is high, Q4 is turned off, and Q5 is held pinched off by -12 Vdc through R31. This action opens the R8/R9 leg of the attenuator, allowing all the current available at the cathode of CR2 to flow to or from the integrator input summing junction (AR3-2). The maximum amount of the current, and hence the maximum slope of the integrator output ramp, is determined by adjusting R7. Since the higher the slope, the shorter the time per oscillator cycle, the higher transmitter (MARK) frequency (2225 Hz) is set by adjusting R7 with the EIADATOT line held high. The lower (SPACE) transmitter frequency

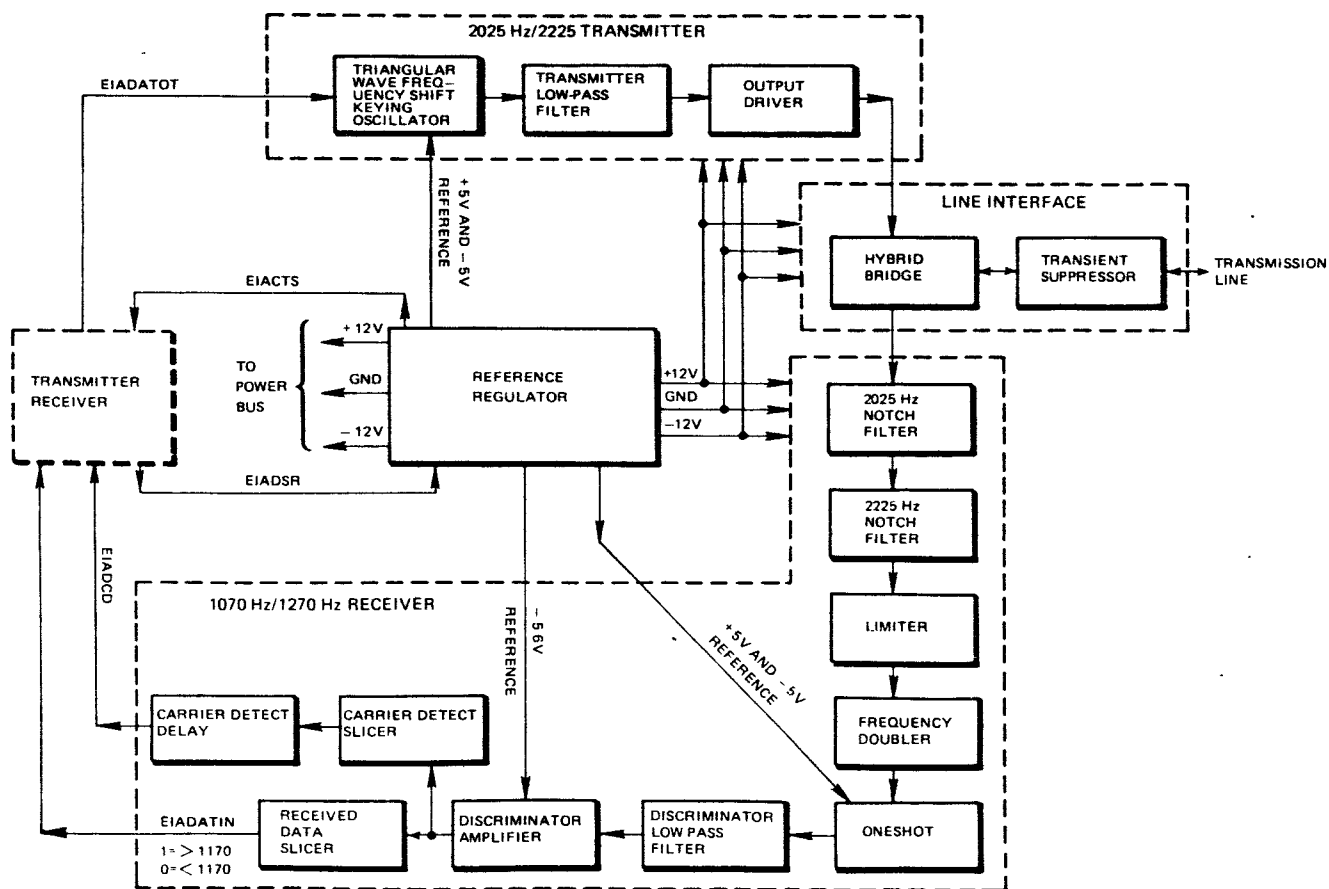


FIGURE 3-9.2. ANSWER MODE (TH) MODEM FUNCTIONAL BLOCK DIAGRAM

(2025 Hz) is produced when Q5 is no longer pinched off by the action of Q4. Since the on resistance of Q5 is only about 20 ohms, the shunt leg (R8, R9) of the attenuator is essentially switched into the circuit, reducing the current flowing through R10 to or from the integrator summing junction input (AR3-2). The magnitude of the current flowing in the shunt leg of the attenuator is adjusted by means of the pot R9 while the transmitted-data line is held low. It is important to note that the adjustments for MARK and SPACE frequencies are interactive. Inasmuch as R7 controls the integrator input current whether the shunt leg of the attenuator is switched in or out of the circuit. Hence the MARK frequency (2225 Hz) must be set by R7 before setting the SPACE frequency (2025 Hz) with R9.

- c. **Transmitter Low-Pass Filter:** The triangle wave output from the transmitter oscillator circuit may be altered to produce a low distortion sine wave at the oscillator fundamental frequency by attenuating all harmonics of the fundamental with the XMITTER low-pass filter (R11-R13, C9-C12, and AR4).
- d. **Transmitter Output Driver:** The transmitter output driver circuit consists of variable attenuator R18 from the output of the transmitter low-pass, followed by noninverting voltage follower AR6. By adjusting the wiper position on R18, the output level transmitted may be adjusted over the range from +5 dBm to less than -40 dBm.
- e. **Communication Line Transient Suppressor Circuit:** The zener diodes CR7 and CR8 are 6.8-volt units rated at 5 watts. Their function is to limit the difference-mode signal amplitude at the primary (transmission line side) of transformer T1 to an absolute maximum of about 7.5 volts. Chokes L3 and L4, in conjunction with high voltage capacitors C18 and C19 and associated circuit resistances, form low-pass filter sections which limit the coupling of high frequency common mode signals (spikes, etc.) from the primary to the secondary of T1.
- f. **Hybrid Bridge Circuit:** The hybrid bridge circuit performs three important functions.

First, it provides the proper driving and terminating impedance to match the modem to the transmission line. Second, it provides isolation between the transmitter and receiver of the modem to prevent a strong transmitted signal from swamping a small received signal. Third, the bridge components are chosen to limit the bandwidth of the modem receiver.

The bridge's operation is dependent on the balancing of the impedance in its two arms: R14/R39 and R17/R41/T1. For balancing considerations R15 may be neglected, since the very large input impedance of operational amplifier AR5 does not load it. Consider the case when the modem is transmitting into a 600-ohm transmission line termination on which no other signal is impressed. The resistors R14, R39, R17, and R41 are chosen so that the ratio of values of R14 to R39 equals the ratio of values of R17 to the series combination of R41, the line impedance (600 ohms, reflected through 1:1 transformer T1), and the equivalent winding resistance of T1. Since R39 provides negative feedback around AR5, the difference voltage between the inverting and noninverting inputs to AR5 is driven to zero. Since the difference voltage from AR5-2 to AR5-3 is zero, and the bridge resistances are proportional, the voltage across R14 equals the voltage across R17. This means that the voltage across R39 must equal the voltage from AR5-3 to ground; i.e., the output of the bridge (AR5-6) is identically zero. Therefore, the bridge provides 30 to 35 dB attenuation between the transmitter and receiver.

With the transmitter off AR6-6 will be at ground, and the input impedance to the modem appears as the series combination of R17, R41, and the resistance of the secondary winding of T1 (typically slightly over 600 ohms for the total). This combination is set to 600 ohms so as to match the transmission line impedance. The total input impedance is tapped by AR5-3 via R15 between R41 and R17; thus, about 5/6 of the input signal is present at the noninverting input to AR5. Since R14 is at signal ground with respect to receiving signals from the transmission line. The overall gain is approximately 2.0 from the communication line input to the output of AR5 (input to receiver).

The receiver input bandwidth is limited by the simple RC low-pass filter formed by R15 and C16. This filter has a cutoff (3 dB) frequency of about 2.473 kHz and a rolloff rate of -6 dB per octave.

- g. 2025 Hz Notch Filter Circuit: AR7 and its associated twin-tee network provide a very narrow band-elimination filter centered at the transmitter SPACE frequency of 2025 Hz. The function of the filter is to severely attenuate any 2025 Hz output signal from the transmitter which "leaks" through the hybrid bridge circuit to the receiver input.
- h. 2225 Hz Notch Filter Circuit: AR8 and its attendant twin-tee network provide a very narrow band-elimination filter centered at the transmitter MARK frequency of 2225 Hz. The function of the filter is to severely attenuate any 2225-Hz output signal from the transmitter which "leaks" through the hybrid bridge to the receiver input.
- i. Limiter Circuit: The limiter circuit has two functions. The first function is to produce a square wave output which switches as closely as possible to the zero crossings in the input waveform. The output wave switches between +5.4 and +0.25 Vdc. The high output voltage is set by the resistor divider R54/R61 to +12Vdc. The low output voltage is set by the saturation voltage of the output stage of AR9.

The second function of the limiter circuit is to determine the sensitivity of the receiver. The sensitivity of the limiter may be varied by feeding back a small portion of the output waveform to establish the threshold voltage through which the limiter input must pass in order to cause an output transition. The greater the amplitude of this positive feedback voltage, the larger the input signal must be to cause a transition at AR9-7.

C30, R51, and C31 form a rudimentary bandpass filter with nominal (-3 dB) cutoff frequencies of 570 Hz and 88.4 kHz. This filter further restricts the bandwidth to which the receiver is sensitive. Since C30 couples the limiter circuit to the preceding receiver stage, the input signal applied to the inverting input

of the comparator (AR9-3) has no dc component. The band-limited input signal is therefore an ac signal twice the amplitude of the received signal on the transmission line since the hybrid bridge provides a gain of two. The (positive) feedback signal supplied to the noninverting input AR9-2 must also be an ac signal with no dc component, but the voltage at AR9-7 never goes negative.

A pull-down network composed of R55 and R56 provide the driving potential to pull the feedback signal below ground. Pot R56 provides adjustment to compensate for variation in input offset voltage as well as tolerance variations in R54, R61, and +12 Vdc. Pot R53 provides an additional capability to compensate for input offset voltage in AR9. When a valid input signal is presented to the modem receiver after the carrier detect has been in the off (low) state, FET Q8 is held off and a ± 2 mV signal is presented to the noninverting input of AR9 through the attenuator composed of R57 + R59 and R58. If, for example, the input voltage at AR9-3 is sufficiently negative to cause the output stage of AR9 to cut off, the voltage at AR9-7 rises to +5.4 Vdc, applying about +2 mVdc to AR9-2.

Before the output stage of AR9 can saturate again, the signal at AR9-3 must go higher than the +2 mVdc set at AR9-2. This means that the limiter cannot respond to modem input signals smaller than 1 mV peak (approximately -54 dBm) if Q8 is pinched off. If Q8 is turned on, the positive feedback voltage at AR9-2 is limited to ± 0.6 mVdc swings, thus allowing the comparator to switch states for modem input signals of 0.3 mV peak (-64 dBm).

The two sensitivity settings of the limiter are controlled by the carrier detect slicer circuit. If no data has been received for some time, carrier detect is low, pinching Q8 off and setting the sensitivity to -54 dBm. When carrier detect is high, Q8 is turned on, increasing the sensitivity to -64 dBm. The higher sensitivity is provided to allow the accurate reproduction of input signal zero crossings by the limiter when the input level is low.

- j. Frequency Doubler Circuit: The squarewave output from the limiter is applied to the

frequency doubler where the wave train is differentiated and essentially full-wave rectified to obtain a train of trigger pulses with a constant amplitude and a repetition rate of twice the incoming signal (and limiter output).

The output of the limiter circuit switches between approximately +0.25 Vdc and +5.4 Vdc; this waveform is applied to R62 and C32. When the limiter output switches to +5.4 Vdc, a short positive-sloped spike is coupled through C32 to the cathode of GR10 where it is blocked from passing to the base of Q10. The high-going limiter output also supplies base drive through R62 to the base of Q9, saturating Q9 and coupling a negative-sloped spike through C33 and CR9 to the base of Q10. When a low-going spike is applied to the base of Q10, it causes a high-going spike at the collector of Q10. Similarly, when the limiter output goes low, a negative-sloped spike is applied to the base of Q10 through C32 and CR10, causing a high-going spike produced at the collector of Q10. If the output of the limiter is a 50 percent duty cycle waveform, the train of pulses at the frequency doubler output (Q10 collector) will have exactly twice the frequency of the frequency doubler output waveform. Q10 further acts as a buffer amplifier, providing a low output impedance source of trigger pulses to the oneshot while isolating the differentiating capacitors C32 and C33 from the positive feedback voltage around the amplifier AR10 in the oneshot.

- k. Receiver Oneshot Circuit: The output pulses from the frequency doubler circuit trigger the oneshot to produce a rectangular pulse train. The change in average dc value of this rectangular pulse train is directly proportional to the change in repetition rate of the trigger pulses and, hence, proportional also to the change in input signal frequency.

In its stable (inactive) state, oneshot amplifier AR10-6 is in negative saturation, and the oneshot output (cathode of CR12) is clamped to -5.6 Vdc through CR12. The negative output voltage is fed back to the noninverting input of AR10 through the voltage divider comprised of R69 and R70, holding the noninverting input to -2.8 Vdc. The negative saturation voltage at

AR10-6 is also applied to a voltage divider formed by R75 and R74, saturating the collector of Q11 at approximately 0 Vdc. This action holds the ungrounded side of the timing capacitor C34 (inverting input of AR10) very close to ground through R82. Since the noninverting input voltage (-5.4 Vdc) is less than the inverting input voltage (approximately 0 Vdc), the amplifier is latched in negative saturation, holding the oneshot output in its stable state.

When a high-going pulse is applied to the noninverting input of AR10 from the collector of Q10 (low impedance source), the noninverting input of AR10 is made more positive than the inverting input of AR10 (0 Vdc). This condition causes AR10 to switch from negative saturation to positive saturation, and the metastable (active) state of the oneshot is initiated. The oneshot output is bounded to +5.6 Vdc by the clamping action of CR11, and the output voltage is divided by R70 and R69 and applied to the noninverting input of AR10. The positive voltage at AR10-6 causes Q11 to cut off and C34 begins to charge from 0 Vdc toward +5.6 Vdc through the combination of R72, R73, and R76, with the setting of R76 establishing the rate of charge. Since the voltage at the inverting input of AR10 is initially less than the +3.8 Vdc at the noninverting input, the output of AR10 is latched in positive saturation. Finally, when C34 has charged up higher than +2.8 Vdc, the voltage at the inverting input of AR10 exceeds the voltage at the noninverting input of AR10, and the output of AR10 switches to negative saturation. This causes Q11 to saturate, quickly discharging C34 through R71, and the one-shot resumes its stable state.

The adjustment range of R76 allows the oneshot (metastable) period to be set for a (positive) duty cycle of 25 percent when the trigger pulse frequency equals 2340 pulses per second. This frequency is produced when an input signal of 1170 Hz is applied successively to the modem receiver limiter and frequency doubler stages.

- l. Receiver Discriminator Low-Pass Filter Circuit: The rectangular output waveform from the

oneshot circuit is fed into the discriminator low-pass filter circuit. Since the cutoff frequency of this filter (150 Hz) is so much lower than the repetition frequency of the oneshot output pulses, the filter acts essentially as an analog integrator. The filter output, then, is a dc voltage equal to the average value of the oneshot pulse train voltage. A change in input frequency thus causes a proportional change in the filter output voltage.

- m. **Discriminator Amplifier Circuit:** The discriminator amplifier modifies (biases and amplifies) the output signal from the discriminator low-pass filter to make it easier to compare in the received-data slicer and the carrier-detect slicer circuits.

The nominal swing in the discriminator low-pass filter output, which corresponds to a SPACE frequency-to-MARK frequency transition at the receiver input, is from -2.93 Vdc to -2.67 Vdc. It is convenient to translate this voltage swing upward so that the decision as to whether the output voltage of the discriminator filter is high or low (corresponding to MARK to SPACE received frequencies, respectively) may be made about ground potential. Such a translation is provided by the discriminator amplifier. When the receiver input frequency is 1170 Hz, the oneshot pulse width is adjusted so that the discriminator amplifier output voltage is zero.

In addition to providing the convenient positive translation of the discriminator output voltage, the discriminator amplifier also applies a gain of nearly +25 to the output swing of the discriminator low-pass filter. This additional gain allows the output of the amplifier to swing from -3.25Vdc for a SPACE (1070 Hz) input to +3.25 Vdc for a MARK (1270 Hz) input with 0 Vdc corresponding to the midband frequency of 1170 Hz.

- n. **Received Data Slicer Circuit:** The received-data slicer circuit monitors the output voltage of the discriminator amplifier, providing a MARK level to the XMT/RCV logic for any input signal whose frequency is 1170 Hz or higher. It produces a SPACE level to the XMT/RCV logic for any input signal whose frequency is less than 1170 Hz.

When the discriminator amplifier output voltage (AR16-6) is higher than 0 Vdc (corresponding to a MARK input frequency) the inverting input voltage to comparator AR16 is made more positive than the noninverting input voltage, which is fixed at ground potential. This causes the output of AR16 to saturate, pulling the EIADATIN line to -12 volts through R101. When the discriminator amplifier output voltage is less than 0 Vdc (corresponding to a SPACE input frequency condition), the inverting input voltage to AR16 is made more negative than the noninverting input voltage (0 Vdc). This causes the output stage of AR16 to saturate positive, causing the EIADATIN line to reach +12 volts through R101.

The positive feedback around AR16, provided through R93, decreases the chance of comparator output parasitic oscillations as the noninverting input slews through the region near 0 Vdc. It also provides a margin of immunity (approximately 2 mV) to small ripples present at the discriminator amplifier output.

The presence of R91 and C43 provides some additional filtering of the discriminator amplifier output to attenuate any high frequency transients present.

- o. **Carrier Detect Slicer Circuit:** The carrier-detect circuit monitors the output voltage of the discriminator amplifier, providing an in-band signal to the carrier-detect delay circuit for any input signal whose frequency lies between 994 Hz and 1339 Hz. It produces an out-of-band signal to the carrier-detect delay circuit for any input signal frequency below 994 Hz or above 1339 Hz.

The biasing of the matched pair of zener diodes, CR14/CR15, from the +12 Vdc and -12 Vdc supply buses through R88 and R90 establishes the voltage drops across the zeners at very nearly 5 Vdc. Thus, as the output voltage of AR15-6 is applied to the cathode of CR15 (anode of CR14), the voltage at the cathode of CR14 is set 5 volts above the discriminator amplifier output voltage. Similarly, the voltage at the anode of CR15 is set 5 volts below the discriminator amplifier output voltage.

So long as the voltage at AR15-6 lies in the range -5.6 Vdc to +5.6 Vdc, both diodes CR13 and CR18 remain back-biased and the small positive voltage set by the divider R89/R95 holds AR13 in positive saturation (since with CR13 and CR18 back-biased AR13-3 is slightly positive and R94 is grounded through R94).

If the voltage at AR15-6 rises about +5.6 Vdc, CR13 remains back-biased, but CR18 is forward-biased, increasing the voltage at AR13-2 above that at AR13-3. This condition causes AR13-6 to switch to its negative saturation voltage, indicating carrier-out-of-band.

If the voltage at AR15-6 falls below -5.6 Vdc, CR18 remains back-biased, but CR13 is forward-biased, reducing the voltage at AR13-3 below that at AR13-2. This condition causes AR13-6 to switch to its negative saturation voltage, indicating carrier-out-of-band.

- p. **Carrier Detect Delay Circuit:** The carrier-detect circuit provides an in-band (EIADCD high) level to transmit/receive logic in accord with the in-band signal from the carrier-detect slicer circuit. The rising transition in the carrier-detect signal to the transmit/receive logic is delayed until a nominal 150 msec after the carrier-detect slicer in-band indication is given. The carrier-detect delay circuit also provides an out-of-band (EIADCD low) level to the transmit/receive logic, corresponding to the out-of-band signal from the carrier-detect slicer circuit. The falling transition in the (EIADCD) signal is delayed until a nominal 100 msec after the carrier-detect slicer out-of-band indication is given.

When the carrier detect slicer output (AR13-6) is positively saturated, the base-emitter junction of Q12 is forward-biased, and its collector saturates at about +0.5 Vdc. In this state CR16 is back-biased by approximately 11 volts with +0.5 Vdc at its anode. This small positive voltage allows the N-channel FET Q8 to turn on, causing the limiter sensitivity to increase. The forward-biased base-emitter diode drop from Q12 appears across C44 and as a reverse bias across CR17. The base-emitter drop also holds AR14-3 at +0.6 Vdc, causing the output

stage of AR14 to saturate positive and hold the carrier detect line (EIADCD) to +12 volts.

If a loss of in-band carrier causes the voltage at AR13-6 to switch to negative saturation, Q12 is immediately turned off and CR16 is forward biased through R96 to clamp the gate of Q8 to approximately -11 Vdc. These conditions quickly pinch off Q8, switching the limiter sensitivity to its lower level. The carrier-detect "dropout" delay cycle begins as Q12 is cut off and the voltage between R97 and C44 slowly decreases from +0.6 Vdc as C44 is discharged toward the saturation voltage of AR13 through R97. The output stage of AR14 remains cut off and carrier detect remains at +12 Vdc until the voltage between R99 and C44 goes slightly negative, approximately 50 msec after AR13 goes into negative saturation. When the voltage at AR14-2 goes negative, the output stage of AR14 is saturated and the carrier detect line is switched to -12 volts.

After the carrier detect line has been low for some time, the voltage between C44 and R99 is clamped to -2 Vdc by the forward-biased multipellet diode CR17 (CR17 serves to limit the differential voltage between AR14-2 and AR14-3, while establishing a 2 volt reference across C44). If the output of the carrier detect slicer (AR13-6) switches from negative to positive saturation, indicating the presence of in-band data on the transmission line, C44 begins to charge from -2 Vdc toward the positive saturation output voltage of AR13 through R97. When the voltage between R99 and C44 goes slightly positive (150 msec after switching of AR13), the output stage of AR14 is cut off and the carrier detect line is pulled up to +12 volts. C44 continues to charge up to +0.6 Vdc, at which time Q12 is saturated and the clamping action of the forward base-emitter diode halts the charging process. As Q12 saturates, it quickly pulls the gate voltage at Q8 from approximately -11 Vdc to +0.5 Vdc, turning Q12 on and increasing the sensitivity of the receiver limiter.

3-9.2 ANSWER-BACK MEMORY. The Answer-Back Memory PC card is an optional accessory for the 733 ASR or KSR. This circuit automatically transmits any programmed sequence of up to twenty-one 7-bit characters

for station identification. The station identification message is stored in a diode matrix as a series of 7-bit ASCII-coded characters. The matrix, shown in Figure 3-9.3, is arranged to facilitate user programming. Each horizontal row in the matrix (starting with CR1) represents one 7-bit character. The first character is the top row, and bit-1 (LSB) is at the top right (CR1). Thus, character-1 is made up of diodes CR1 (bit-1), CR22, CR43, CR64, CR85, CR106, and CR127 (bit-7). The presence of a diode in any bit position indicates a logic ONE in that bit position. For example, if the first character to be programmed is an uppercase B(100010). diodes CR1, CR43, CR64, CR85, and CR106 would be cut out, and diodes CR22 and CR127 would be left in.

For each character (greater than 3) needed for station identification, the corresponding diode in the first column

(CR148 through CR165) must be removed. For example, if a 15-character message is desired, diodes CR148 through CR159 must be removed and CR160 must be left in the circuit.

The Answer-Back Memory (ABM) is triggered by the HERE IS key (terminal on-line and keyboard not OFF), or by receiving the ENQ code (card set for ASCII), or by receiving FIG and D consecutively (card set for Baudot code) from the serial receiver. When one of these signals is decoded, a flipflop is set (ENQRY or HEREISQ). If the terminal is in HALF DUPLEX, the printer (PRNROF-) and/or recorder (RECROF-) will be disabled while the ABM is transmitting if they are on-line, depending on switch S1-6 and S1-7, as shown in Table 3-9.1. This generates an ABM busy (STOQ-) which removes the clear from the character counter and starts the ABM sequence.

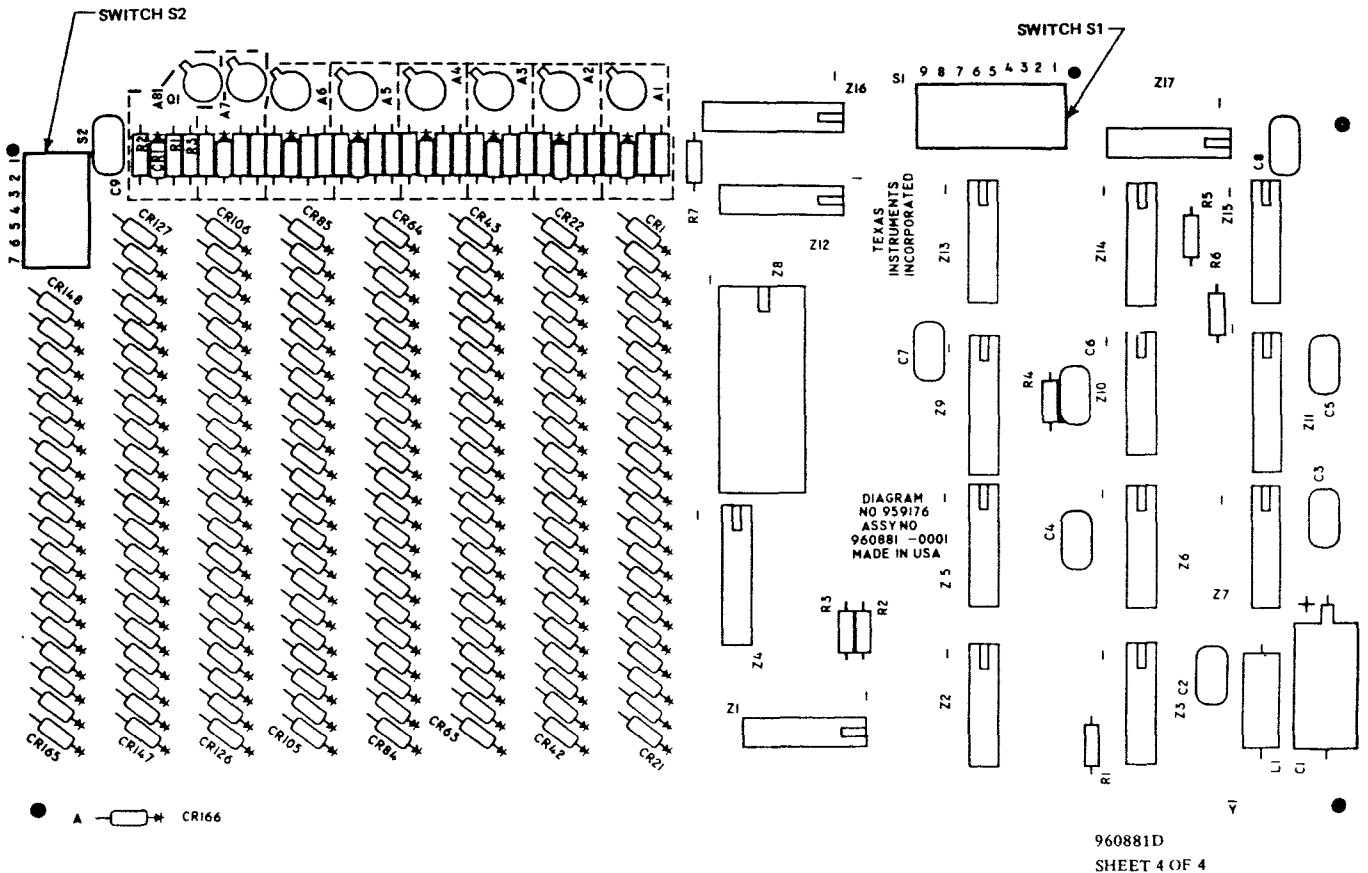


FIGURE 3-9.3. ANSWER-BACK MEMORY DIODE MATRIX

TABLE 3-9.1. ANSWER-BACK MEMORY PC CARD SWITCH OPTIONS

Switch S2	Function
1	Open to remove CR141 (bit 7 character 15) from matrix
2	Open to remove CR21 (bit 1 character 21) from matrix
3	Open to remove CR121 (bit 6 character 16) from matrix
4	Open to remove CR101 (bit 5 character 17) from matrix
5	Open to remove CR81 (bit 4 character 18) from matrix
6	Open to remove CR61 (bit 3 character 19) from matrix
7	Open to remove CR41 (bit 2 character 20) from matrix
Switch S1	Function
1	Close for ASCII card; open for Baudot card
2	Close for ASCII card; open for Baudot card
3	Close for ASCII card; open for Baudot card
4	Open for ASCII card; close for Baudot card
5	Open for ASCII card; close for Baudot card
6	Close to disable printing of ABM contents at all times; open to enable printing of ABM contents when online in half-duplex
7	Same as S1-6 except for recorder
8	Close to put an ABM ON indication on pin 9 (future option); open for NO indication (spare run on AUX1R0F)
9	Close to ignore stop bit (continuous memory cycling) open to stop ABM at stop bit programmed
1 and 4	Open both at same time to ignore triggering ABM from the line only

NOTES

1. Switch S2, all positions are normally closed; open only during unit test
2. Switch S1-9 is normally open; closed only during unit test
3. Switches are closed when the dot on the switch rocker arm is down

The ABM then generates and sends a request signal (AUX2REQ-) to terminal control and loads the first character stored in the diode matrix into a parallel-to-serial converter. The ABM then waits for an enable to send signal from terminal control (AUX2ENAS-). This signal and eight system clocks are used to clock the first character from the parallel-to-serial converter to the data bus. At the end of this enable, the character counter is clocked to character-2 and one clock time later another request is generated and the second character is loaded into the output register. This sequence continues until 21 characters are shifted out, or the character counter reaches a character in which one of the stop bit diodes (CR148 through CR165) have been left in. When one of these diodes is sensed, a stop signal is generated (ABMSTP) which prevents generation of another request. The ABM is now ready for another trigger signal.

A remote trigger signal is also available on pin 24 (FSTIME-) of the ABM card. A 5-μsec pulse on this pin will cause the ABM to trigger as if the HERE IS key had been depressed. This signal will trigger the ABM at all times, except when the terminal is not on line. Another signal on pin 19 (AUX2ROF-) is a remote clear for the ABM: bringing this line low will hold a clear on the ABM. Both these remote lines are used with other terminal options. The Answer-Back Memory timing diagram, flow chart, and state equations are shown in Figures 3-9.4 and 3-9.5, and Table 3-9.2, respectively.

ABM switch options are listed in Table 3-9.1.

3-9.3 AUTOMATIC DEVICE CONTROL PC CARD. The Automatic Device Control (schematic 971498) monitors the data bus at all times except when the ADC's master ON/OFF switch is OFF) and decodes control characters

DC1, DC2, DC3, DC4, and EOT. The ADC can be programmed to respond to or ignore DC1, DC2, DC3, and DC4 characters coming from the serial receiver, transmitter, or local data bus.

The ADC may be programmed to respond to control characters DC1 through DC4 by opening or closing the appropriate switch sections on S2. Table 3-9.3 lists the decodes and appropriate switch section to select to enable or disable them. When the control characters have been decoded, they are loaded into a register and encoded into four control data bits CDBIT1 through CDBIT4. Approximately 20 μsec later control data strobe DCSTRB- is generated. It is a negative-going 4.9 μsec pulse. These four data bits and the strobe are then sent to the ASR remote cassette control where they are decoded and acted upon. The terminal is programmed to respond to the control character EOT by the installation of resistors R1, R2, and R3. R1, R2, and R3 are installed only if the Auto Answer PC card option is installed in the data terminal. Actuating control character EOT will cause the terminal to disconnect from the line only if the resistors are installed.

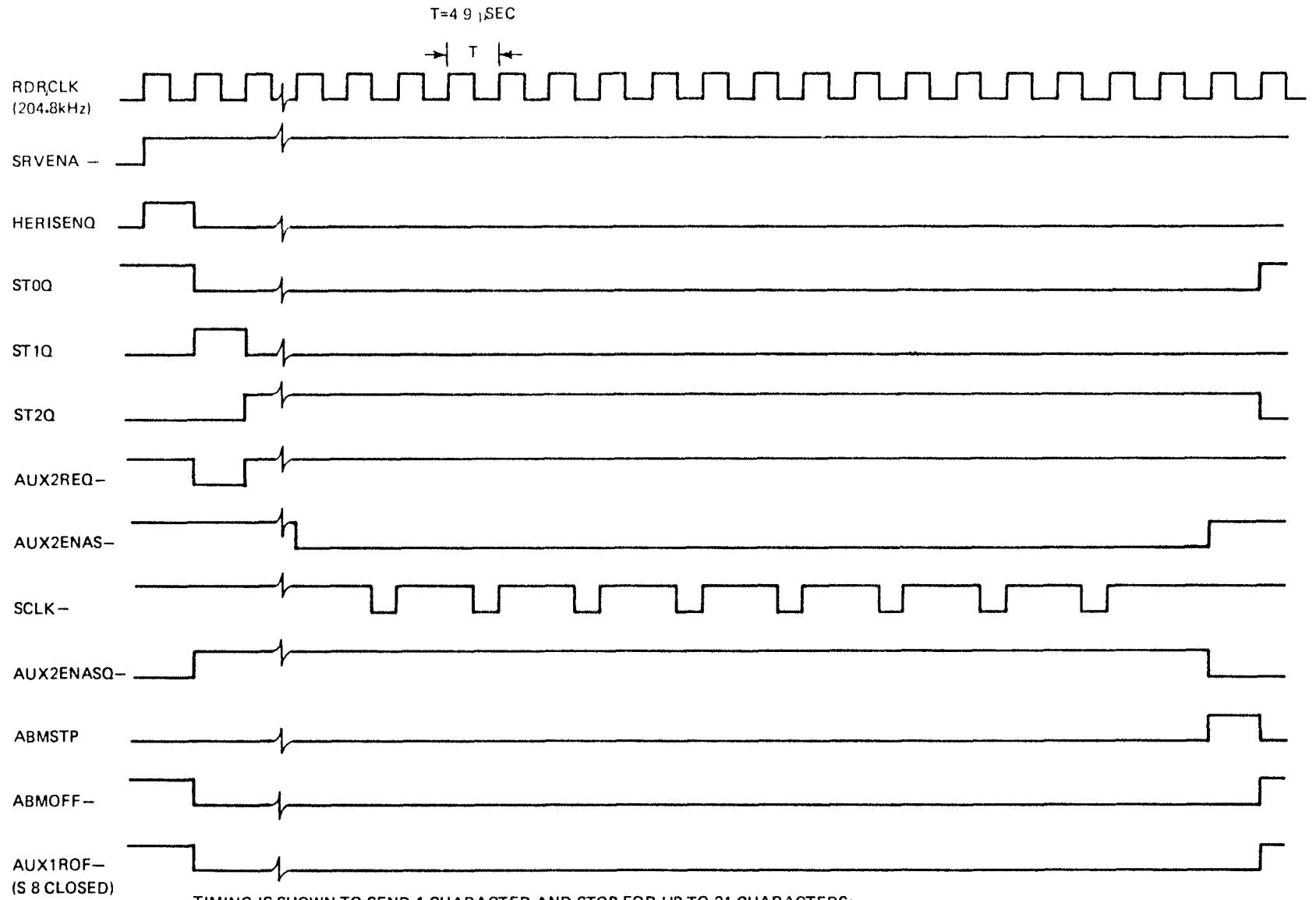
The ADC described above supersedes an earlier version of the ADC (Part No. 960891*). The earlier ADC functions the same as the latest model ADC described above, except that the enabling options are programmed with strappable resistors R1 through R12, and there are no provisions for decoding the control character EOT, nor for operation with the Automatic Search Control (ASC) option, and the earlier ADC has no master ON/OFF switch on the PC card. Table 3-9.4 lists the enabling options for the earlier ADC.

3-9.4 ASCII 1200-BAUD RECEIVER PC CARD. The 1200-baud Receiver PC card (schematic 973931 or 962303*) is

*This PC card is obsolete.

TABLE 3-9.2 ANSWER-BACK MEMORY STATE EQUATIONS

STOD	= (ST1D- x ST2D-)
ST1D	= (STDQ x HERISENQ) + (ST2Q x (ABMSTP- x AUX2ENASQ))
ST2D	= ST1Q + (ST2Q x AUX2ENASQ-)
ABMCLR	= PWRRST + AUX2ROF
HERISENQ	= HERISQ + ENQRY
PRNROF	= PRNLOC- x FULDPX- x STOQ-
AUXIROF	= STOQ-
RECROF	= RECLINE x FULDPX- x STOQ-
ABMTRIGRST	= ABMCLR + TERLIN- + STOQ-
ABMTRIGRST	= Stop ABM after transmission of memory is complete
ABMCER	= Stop and reset ABM after the character now being transmitted



TIMING IS SHOWN TO SEND 1 CHARACTER AND STOP FOR UP TO 21 CHARACTERS;
THE SAME TIMING APPLIES, EXCEPT THAT AT THE END OF EACH AUX2ENAS-,
THE STATE COUNTER RETURNS TO STATE -ONE INSTEAD OF STATE ZERO.

FIGURE 3-9.4. ANSWER-BACK MEMORY TIMING DIAGRAM

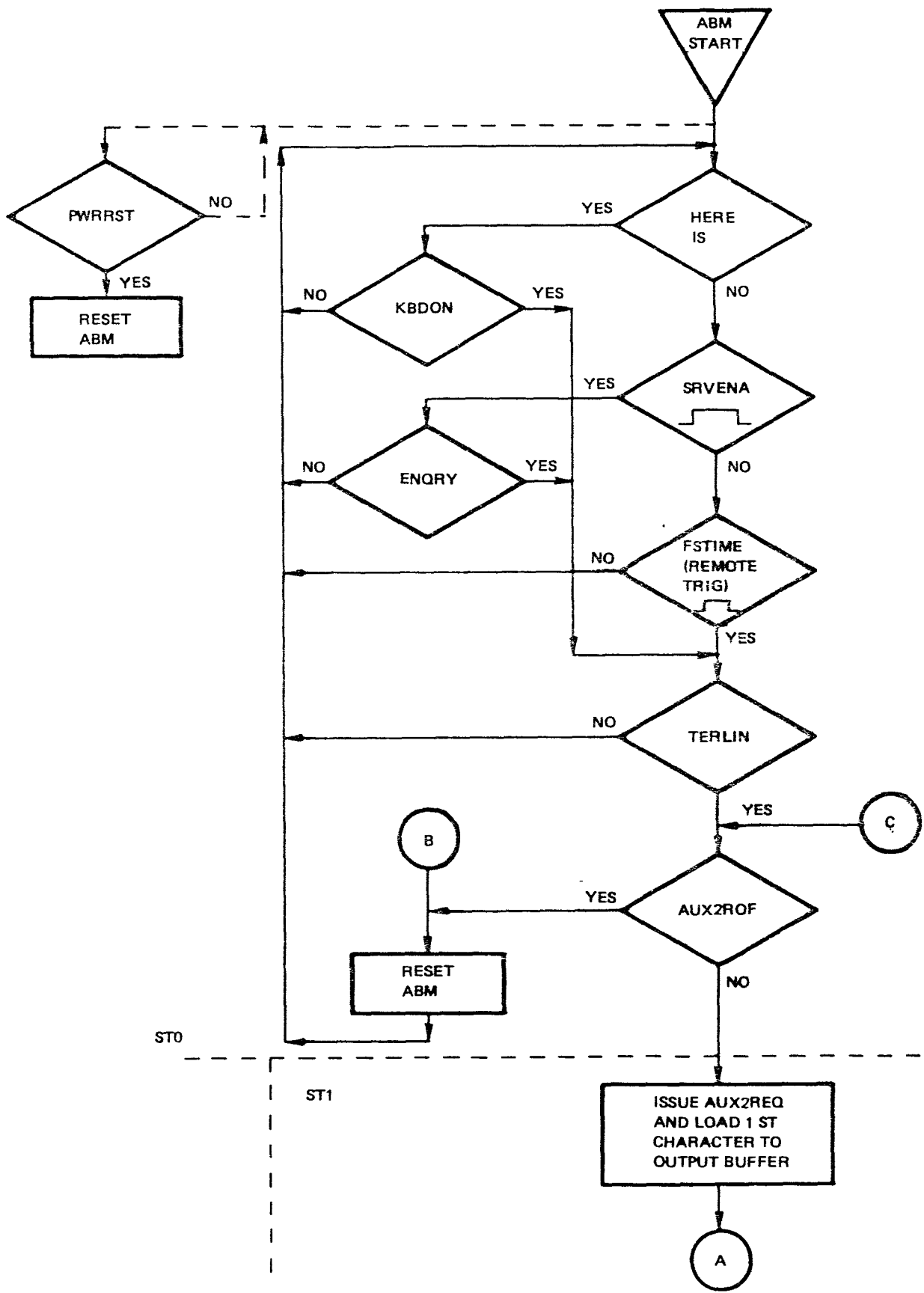


FIGURE 3-9.5. ANSWERBACK MEMORY FLOW CHART (SHEET 1 OF 2)

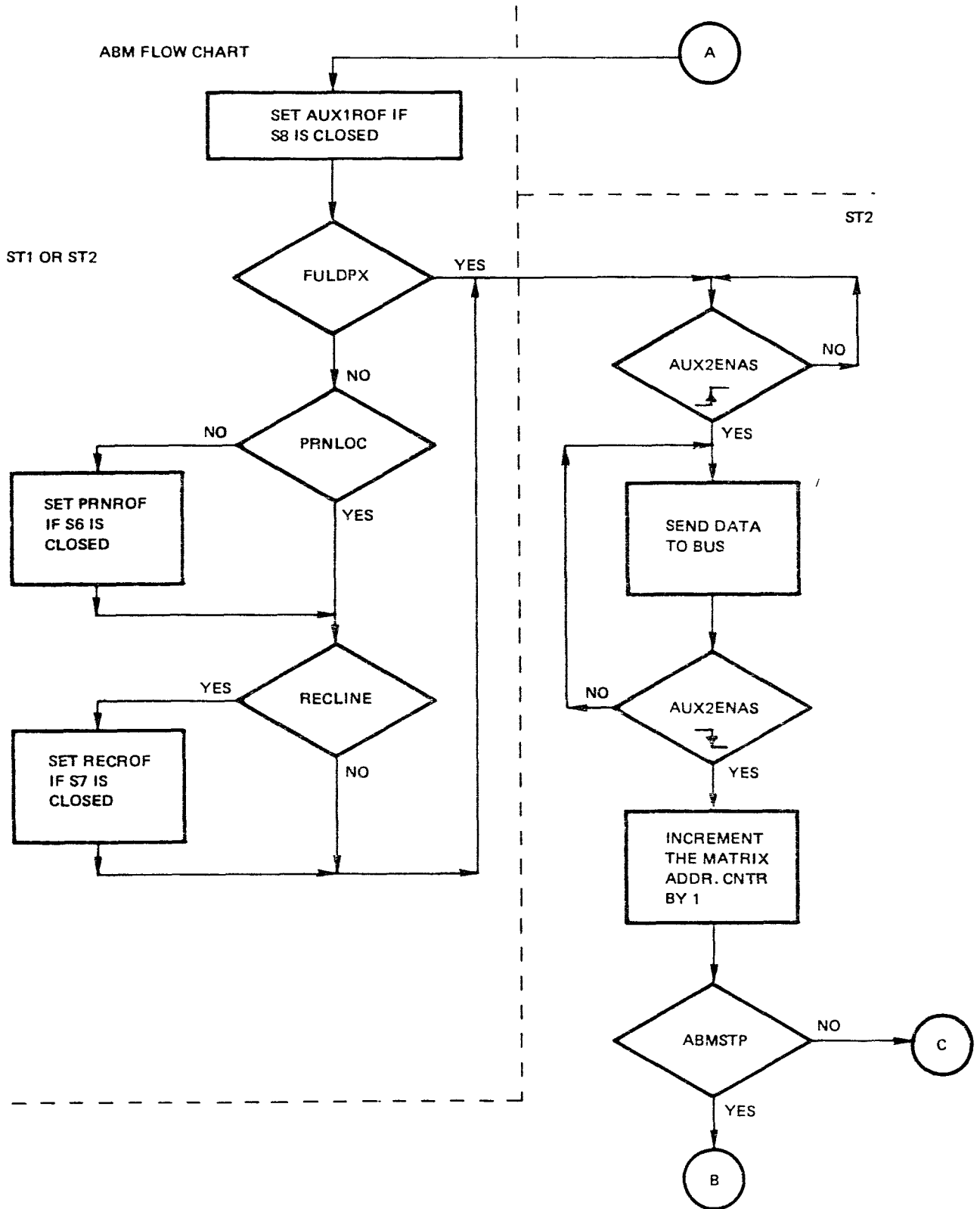


FIGURE 3-9.5. ANSWERBACK MEMORY FLOW CHART (CONTINUED) (SHEET 2 OF 2)

TABLE 3-9.3. AUTO DEVICE CONTROL ENABLING OPTIONS
(for Part No. 971481)

Control Function	Enabling Switch Section		
	To Enable When Transmitting	To Enable When Receiving	To Enable When in Local
DC1 and DC3 (Playback ON/OFF)	S2-1 ON (DC3 only)	S2-2 ON	S2-3 ON
DC2 and DC4 (Record ON/OFF)		S2-4 ON	S2-5 ON

NOTE

Control characters DC1 through DC4 function in the selected operating modes shown above. Close the appropriate switch section on S2 to enable the corresponding function. When the ADC ON/OFF switch is in the OFF position, all ADC functions are disabled except the automatic disconnect on receipt of the EOT character (if the Auto Answer Option is installed).

TABLE 3-9.4. AUTO DEVICE CONTROLLER (EARLIER MODEL) ENABLING OPTIONS
(Part No. 960891)

Control Function	To Enable When Transmitting	To Enable When Receiving	To Enable In Local
DC1 (Playback ON) Resistor Between	R1 J1-J2	R2 J3-J4	R3 J5-J6
DC2 (Record ON) Resistor Between	R7 J13-J14	R8 J15-J16	R9 J17-J18
DC3 (Playback OFF) Resistor Between	R4 J7-J8	R5 J9-J10	R6 J11-J12
DC4 (Record OFF) Resistor Between	R10 J19-J20	R11 J21-J22	R12 J23-J24

NOTE: All resistors are 10 ohm, 0.25 watt, 5 %.

composed of two major sections. The system clock section, which contains the master oscillator, generates the general timing signal used throughout the terminal. The serial receiver section accepts serial data at one of four speeds from an external data set and prepares the data for transmission to other parts of the terminal.

3-9.4.1 System Clocks. The system clock section of the 1200-baud receiver PC card is functionally identical to the clock section of the 300-baud Transmit/Receive PC card (described in Paragraph 3-6.1) with the following exceptions. An additional HIGH SPEED switch is located on the POWER switch panel adjacent to the keyboard to set the terminal to operate at 1200 baud. This switch is independent of the setting of the SPEED switch on the receiver PC card. A block diagram of the system clock structure is given in Figure 3-6.5. When the switch is in the 1200 baud position a SRVCLK of 76.8 kHz is generated.

3-9.4.2 Serial Receiver. Only three differences exist between the 1200-baud receiver section and the 300-baud receiver section (described in Paragraph 3-6.1). First, the 1200-baud receiver accepts TTL data; EIA-to-TTL conversion and enabling is done on the 1200-baud Transmitter PC card. Second, inhibiting of the transmitter while the receiver is receiving a character and the MODE switch is in the HALF DUPLEX position is done on the 1200-baud Transmitter PC card. Third, if the printer is on line and the speed switch is in the 1200 baud position, the printer may be held off (optional strap) with the printer remote off (PRNROF-) signal.

If the optionally strapped PRNROF- signal is not used and visible printing is desired at the 1200-baud speed, filler characters must be added as follows:

- (1) Three deletes following each character
- (2) Twenty-two deletes after each CARRIAGE return.

The deletes compensate for the 30-msec print cycle required by the printer plus the 190-msec carriage return time needed by the printer mechanism.

3-9.5 ASCII 1200-BAUD TRANSMITTER PC CARD. The 1200-baud Transmitter PC card (schematic 962304) is composed of three sections. The data set interface section generates and accepts the necessary signals to operate with a Bell System Model 202C, 202D, or equivalent Data Set. The input section accepts data from the data bus and loads a 64-character first-in-first-out (FIFO) buffer. The transmitter section accepts data from the output of the

FIFO and converts it from parallel to serial for transmission to an external data set.

3-9.5.1 Input. Upon receipt of a transmit enable (XMTENA) and eight system clocks (SCLK) from terminal control, the input section stores the data from the serial data bus (DATA) in the input buffer register on the leading edge of the transmit enable, the line busy flipflop (QLINEBUSY) is set to inhibit terminal control from sending another character. On the trailing edge of XMTENA, the shift-in flipflop (QSIENA) is set. If the first-in-first-out (FIFO) buffer is ready to accept another character, input ready (INPUTRDY) will be high. On the next reader clock (RDRCLK), shift-in (SHIFTIN) is generated to load the character stored in the input buffer register into the FIFO. The eighth data bit loaded into the FIFO may be a MARK (logic ONE), odd or even parity (R6 installed), or the eighth data bit received from the data bus (R11 installed) as determined by the PARITY switch and the two optional resistors (R6 and R11), only one of which is installed at one time. The shift enable flipflop (QSIENA) is cleared as soon as SHIFTIN is generated. The QLINEBUSY flipflop is cleared after approximately 800 μ sec when in the high-speed mode or after a character is transmitted to the line in the low-speed mode. Holding the line busy for at least 800 μ sec assures that the recorder has sufficient time to record a character when the system is in HALF-DUPLEX before terminal control sends the next one.

Once a character is loaded into the FIFO, it is asynchronously propagated to the last empty output location. If more than 64 characters are entered before a character is taken from the output, input ready (IR) output from each of the FIFO's goes low, the 65th character cannot be loaded until a character is taken from the output; in addition LINEBUSY- is held low until the input ready to FIFO goes ready.

3-9.5.2 Data Set Interface. The data set interface generates and accepts the necessary signals for operation with an external data set. For 1200-baud operation a Bell 202C or 202D data set represents the external data set; at speeds of 300, 150, and 110 baud, a Bell 103A or equivalent represents the external data set. The 202C and 202D are both half-duplex data sets: hence the request-to-send signal (EIARTS) must be generated and the terminal must wait for the clear-to-send signal (EIACTS) before transmitting any data to the data set. Cable pin assignments for the 202C or D are listed in Table 3-9.5.

Signals generated by the data set interface and their functions are as follows:

- a. EIA Data Terminal Ready (EIADTR) – This signal is ON (>3.0 volts) as long as the terminal is on-line (TERLINE–, a logic ZERO). The ON condition permits the data set to be connected to the communication channel.
- b. EIA Transmitted Data (EIADATOT) – Serial data to be transmitted by the data set; the MARK, or logic ONE voltage is less than - 3.0 volts and the SPACE voltage is greater than 3.0 volts.
- c. EIA Request-to-Send (EIARTS) – This signal, when at the MARK level (>3.0 volts), indicates that the terminal wishes to transmit information over the EIADATOT line. As long as the terminal is in the full-duplex mode of operation (FULLDPX– a logic ZERO), EIARTS is held to the MARK condition. In the half-duplex mode (FULLDPX–, a logic ONE) EIARTS is held to the MARK condition as soon as the FIFO indicates it has a character to transmit by bringing output ready (OUTPUTRDY) high. After the last character is sent from the FIFO, OUTPUTRDY goes low. After a 20-msec delay, EIARTS will fall to a SPACE level (EIA low).
- a. EIA data set ready (EIADSR) – When in the MARK condition (>3.0 volts) the signal indicates the external data set is ready to operate. This signal, in conjunction with EIA clear-to-send (EIACTS), enables the transmit section to send serial data to the external data set. In conjunction with EIA data carrier detection (EIADCD), this signal also enables sending the serial data from the data set (EIADATIN) to the 1200-baud Receiver PC card.
- b. EIA data carrier detector (EIADCD) – When this signal is in the MARK condition (>3.0 volts), it indicates a valid carrier signal is being received by the external data set.
- c. EIA received data (EIADATIN) – Serial data received from the external data set.
- d. EIA Clear-to-Send (EIACTS) – When in the MARK condition (> 3.0 volts) this signal indicates the external data set is prepared to transmit data.

3-9.5.3 Transmitter Section. The transmit section (see Figure 3-9.6) accepts parallel data from the output buffer of the FIFO and converts it to serial data for transmission

Signals accepted by the data set interface and their functions are as follows:

TABLE 3-9.5. 1200-BAUD, EIA INTERFACE CABLE, PIN FUNCTIONS⁴
(CABLE, TI PART NO. 959372)

Connector Pin Numbers		Pin Function
Terminal	Data Set	
6	20	Data Terminal Ready ¹
7	7	Signal Ground
8	5	Clear to Send ²
9	6	Data Set Ready ³
10	3	Received Data
A	1	Protective Ground
C	4	Request to Send ⁶
H	2	Transmitted Data
K	8	Data Carrier Detect ⁵

NOTES:

- ¹ Held to an ON condition by the data terminal ON LINE switch.
- ² Turned ON in response to "request to send;" typical delay is approximately 220 msec.
- ³ Held to an ON condition when data set is operative; required for terminal operation.
- ⁴ All are used only with external modem.
- ⁵ Held to an ON condition by modem when carrier is received; required by terminal for data reception.
- ⁶ Turned ON when transmission begins; turned OFF 20 msec after transmission ends.

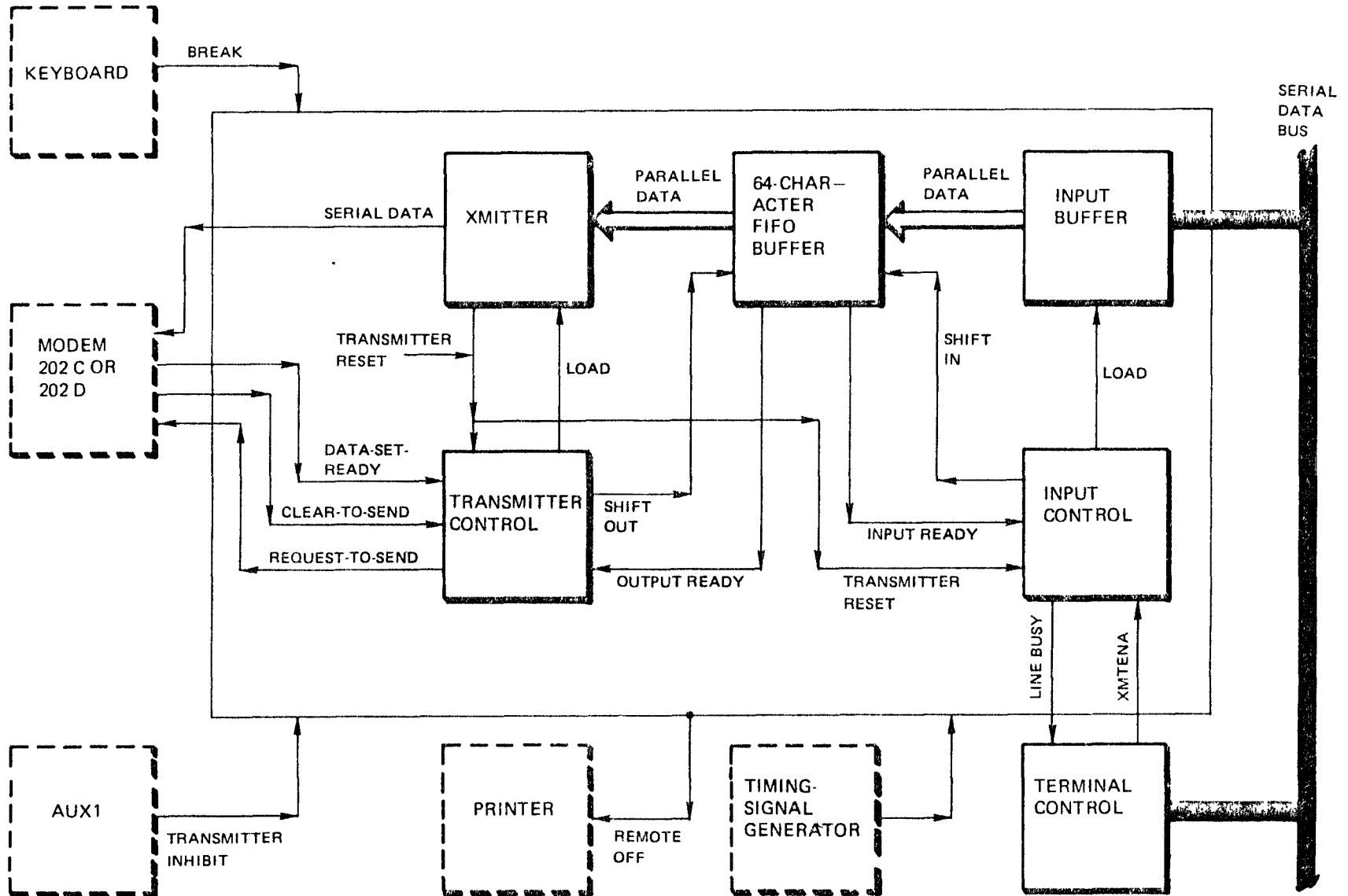


FIGURE 3-9.6. 1200-BAUD TRANSMITTER PC CARD BLOCK DIAGRAM

to an external data set. The transmit section is controlled by the transmit-busy flipflop (XMTBSY). If the FIFO's have data ready for transmission, each FIFO will have the output ready (OR) high; hence QOUTPUTRDY will be high. As soon as XMTENA goes high, the request-to-send flipflop (TTLRTS-) is set to signal the data set that the terminal has data to transmit.

The reader clock (RDRCLK), which occurs after OUTPUTRDY goes high, generates a shift-out pulse (SHIFTOUT) if the data set is prepared to transmit data (ETACTS high) and transmit inhibit (XMTIN4-, generated by the AUX1 device) is not low. The SHIFTOUT pulse sets the XMTBSY flipflop and loads the parallel data into the output buffer when XMTBSY goes low; the pulse then shifts the next character into the output buffer of the FIFO's, and output ready on each FIFO again goes high. The serial receiver clock (SRVCLK) is divided by 64 to generate the transmit clock (XMTCLK) to shift the character out of the output buffer register to the data set. In addition to the eighth data bit, a start bit (logic ZERO)

and stop bit (logic ONE) are added at the beginning and end of the character, respectively. For 10-CPS* operation 2 stop bits are added. The BIT COUNTER counts the number of bits transmitted and sets the transmit reset flipflop (QXMTRST) after the tenth bit has been transmitted (eleventh if the terminal is operating at 10 CPS; i.e., 10 CPS is a logic ONE). Once the transmit flipflop is cleared (XMTBSY logic ZERO), if QOUTPUTRDY goes high (indicating the FIFO's have another character to transmit), another transmit cycle is started. Also, if the terminal is on line (the ON-LINE switch is set) and the BREAK key is depressed, the output line is held to a continuous logic ZERO (SPACE) as long as the BREAK key remains depressed. A timing diagram is shown in Figure 3-9.7.

If the terminal is in the HALF-DUPLEX mode of operation (FULLDPX-, a logic ONE), each time the 1200-baud Receiver PC card receives a character, a reset (RESET) pulse is generated. The RESET pulse goes high after the receiver has received half the start bit and goes back low

*CPS = characters per second

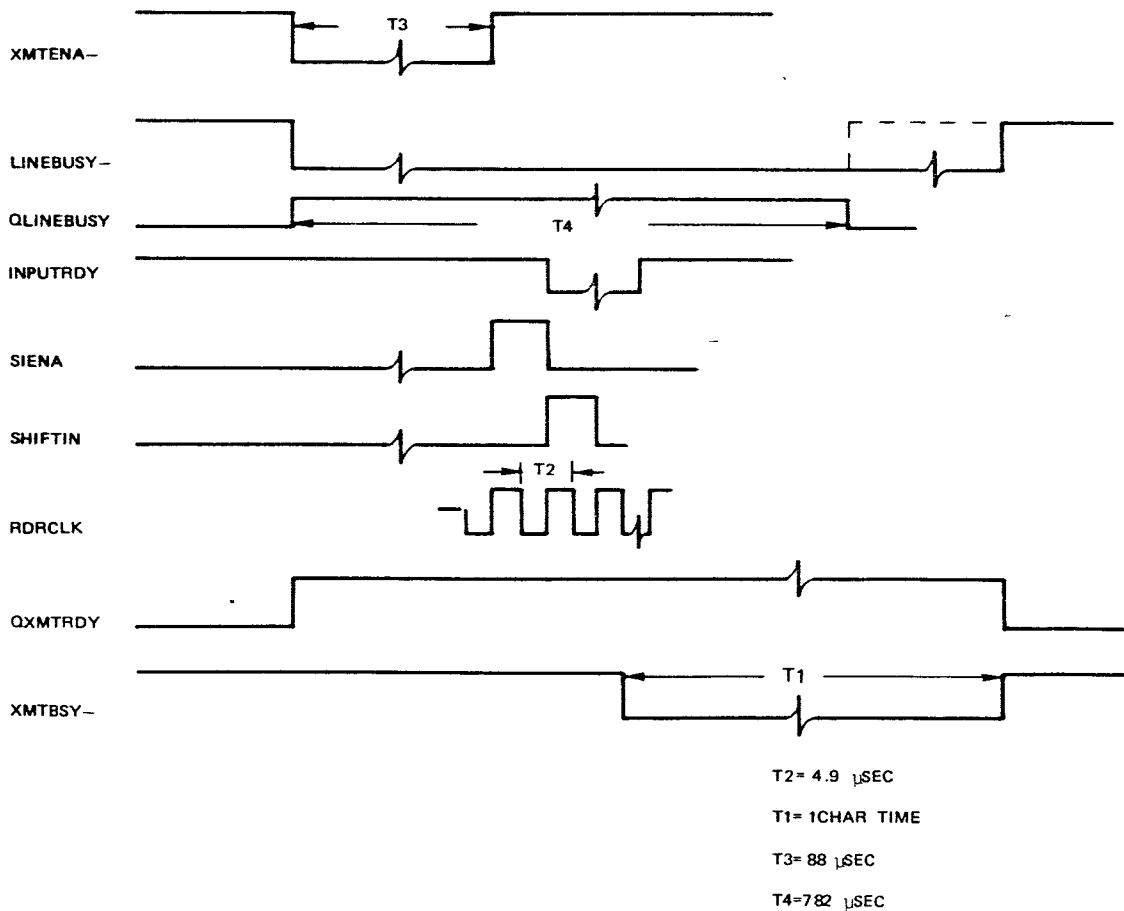


FIGURE 3-9.7. 1200-BAUD TRANSMITTER PC CARD INPUT SECTION TIMING DIAGRAM (FOR 1-CHARACTER INPUT)

after the parity bit is received. When RESET goes high the half-duplex flipflop (RCVHDPX) is set, causing the line to be busy so that no character may be sent to the transmitter. The line is held busy to the transmitter for one character time after the last character is received from the line. This process prevents the transmitter from attempting to transmit a character while the receiver is receiving a character in half-duplex. Conversely, while the transmitter is transmitting a character in half-duplex, the receiver is inhibited by TTLRTS from receiving a character.

3-9.6 AUTO ANSWER CONTROL. The optional Auto Answer Control basically consists of a PC card, a display panel and cabling, and a 6-foot (minimum) EIA or modem cable assembly in kit form. Two versions of the Auto Answer Control Kit are available: one for use with Bell System 103 Data Sets (TI Part No. 960984-0002) and one for use with the Bell System Type-CBS Data Access Arrangement (TI Part No. 960984-0001).

Table 3-9.7 lists interface resistor options for the two versions. Logic diagrams of the Auto Answer Control and its display PC card are shown in drawings 962307 and 962308 in Appendix C of this manual; assembly drawings are contained in Appendix B.

The Auto Answer Control cannot be used with the 733 Data Terminals equipped with the 1200-baud transmit/receive option. Furthermore, TI recommends using the Auto Answer Control in conjunction with the Answer-Back Memory plus the Remote Device Control option or with the Auto Device Controller option, although the Auto Answer will function without them.

The following power is required by either version:

- +5 Vdc @ 380 mA (maximum)
- +12 Vdc @ 10 mA (maximum)
- 12 Vdc @ 8 mA (maximum)

3-9.6.1 Auto Answer Control with Bell 103A Data Set. This version of the Auto Answer Control (TI Part No. 960984-0002) provides the 733 the capability of automatically answering a call on a Bell System DDD network which has a Bell 103A Data Set with auto answer. This version of the Auto Answer Control plugs into PC card slot A8 in the 733 lower enclosure.

In addition to automatically answering a call, the Auto Answer Control includes the following features:

- (1) Automatic triggering of the Answer-Back Memory (ABM) option (with ABM plus ADC

options or RDC option also installed) when the call is answered. The ABM is triggered after an adjustable (with resistor jumpers) delay of 2 msec to 10.2 sec in nine steps from the carrier detect signal (see Table 3-9.6).

- (2) Automatic disconnect from the line and blinding of the printing and record functions if any of the following conditions occur:
 - (a) A carrier from the originating station is not received within 10 seconds after a call is answered.
 - (b) The carrier from the originating station is lost for at least 50 msec during the progress of a call.
 - (c) A disconnect character (usually EOT) is received from the originating station (if a remote device control option is installed).
 - (d) A SPACE of at least 1.28 seconds without a mark is received from the originating station.

Table 3-9.8 lists resistor options necessary to implement either Auto Answer Control version.

a. Indicators

The following indicators (located on the 733 option panel) are provided with the Auto Answer Control:

RING INDICATOR – lamp blinks 2 seconds on and 4 seconds off with the ring indicator of the Bell System 103A. It illuminates steadily after the call is answered (i.e., the DTR line is turned on) until the carrier is received from the originating station.

TERMINAL READY – illuminates when the 733 ON-LINE switch is ON-LINE, indicating that the terminal will answer an incoming call.

LINE READY – illuminates when the terminal has answered the call, received the carrier from the originating station, and is ready to transmit or receive.

b. Typical Operations

Before leaving the data terminal unattended, the operator must switch the appropriate data

TABLE 3-9.6. ANSWER-BACK MEMORY TRIGGER-DELAY CHART, RESISTOR OPTIONS

Delay	Install 10Ω, 0.25 W Resistor ¹	Between
10.24 sec	R15	J10 and J16
5.12 sec	R16	J9 and J14
2.56 sec	R17	J8 and J1
1.28 sec	R18 ²	J7 and J15
640 msec	R19	J6 and J17
320 msec	R20	J5 and J15
160 msec	R21	J4 and J14
80 msec	R22	J3 and J1
0.6-1.9 msec	R23	J2 and J16

NOTES

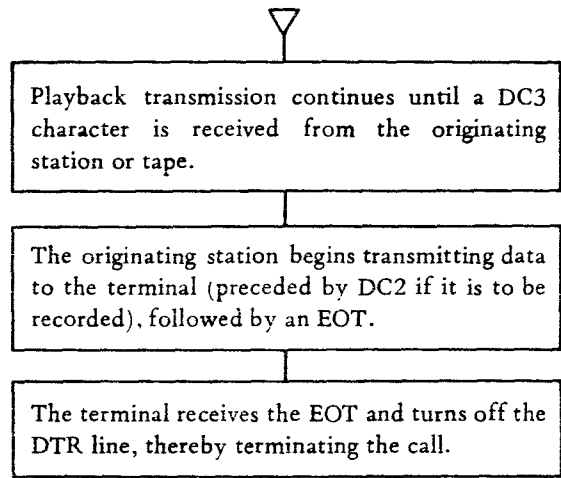
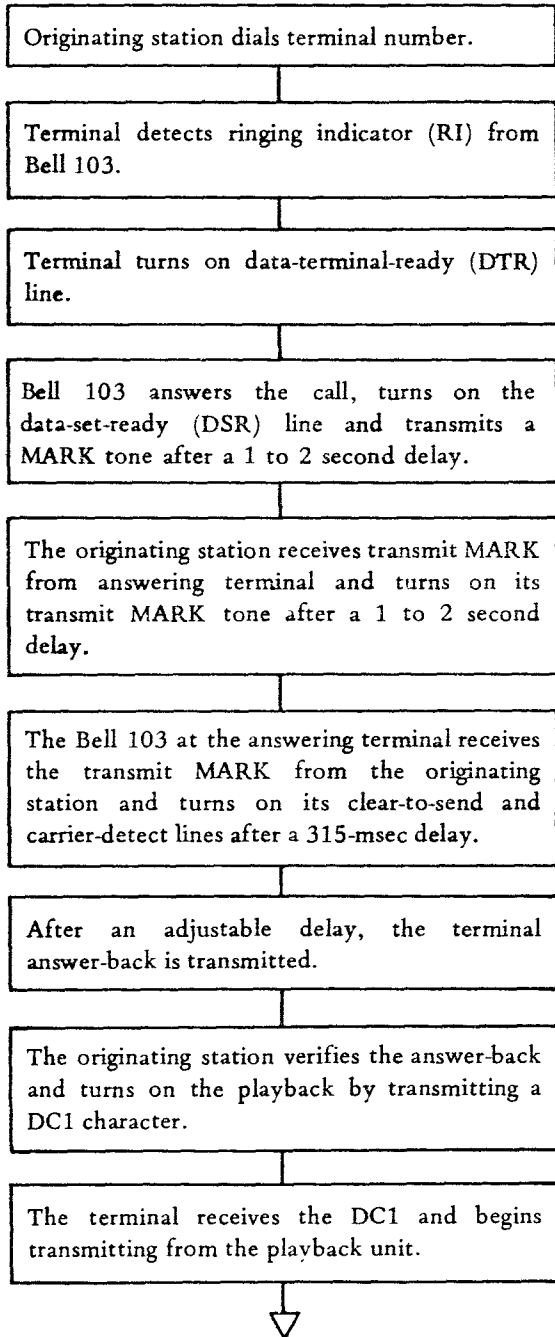
1. Only one of R15 through R23 is used.
2. Resistor normally installed.

TABLE 3-9.7. AUTO ANSWER CONTROL INTERFACE SELECTION CHART, RESISTOR OPTIONS

Install 10Ω, 0.25W Resistor	Between	DAA	For Use With BELL 103
R1	J12 and J18	Open	10Ω
R2*	J13 and J11	10Ω	Open

*Resistor normally installed.

terminal function (RECORD, PLAYBACK and/or PRINTER) to the LINE mode, switch the data terminal to ON-LINE, and switch the Bell 103 Data Set to AUTO. A typical operating sequence (assuming that Answer-Back Memory and Remote Device Control options are installed) is shown in the following flow chart:



A flow diagram of the Auto Answer Control functions is shown in Figure 3-9.8, and state equations are listed in Table 3-9.9.

c. Interface Requirements

The Interface signals conform to EIA Standard RS232C. The interface connector is a 25-pin Cannon DB-25P (or equivalent) at the end of a 6 foot (minimum length) cable. Pin assignments and functions are shown in Table 3-9.10.

3-9.6.2 Auto Answer Control with Bell Type-CBS Data Access Arrangement. This version of the Auto Answer Control (TI Part No. 960984-0001), together with an "answer-mode" modem option, provides the capability of automatically answering a call on a Bell System DDD network which has a Bell type-CBS Data Access Arrangement. This version of the Auto Answer Kit plugs into PC card slot A7 in the 733 lower unit PC card rack.

All other general capabilities are the same as the Auto Answer Control version described in paragraph 3-9.6 above.

a. Indicators

The following indicators (located on the 733 option panel) are provided in the Auto Answer Control:

RING INDICATOR – lamp blinks 2 seconds on and 4 seconds off with the ring indicator of the Bell System DAA. It illuminates steadily after the call is answered [i.e., the off-hook (OH) line is turned on] until the carrier is received from the originating station.

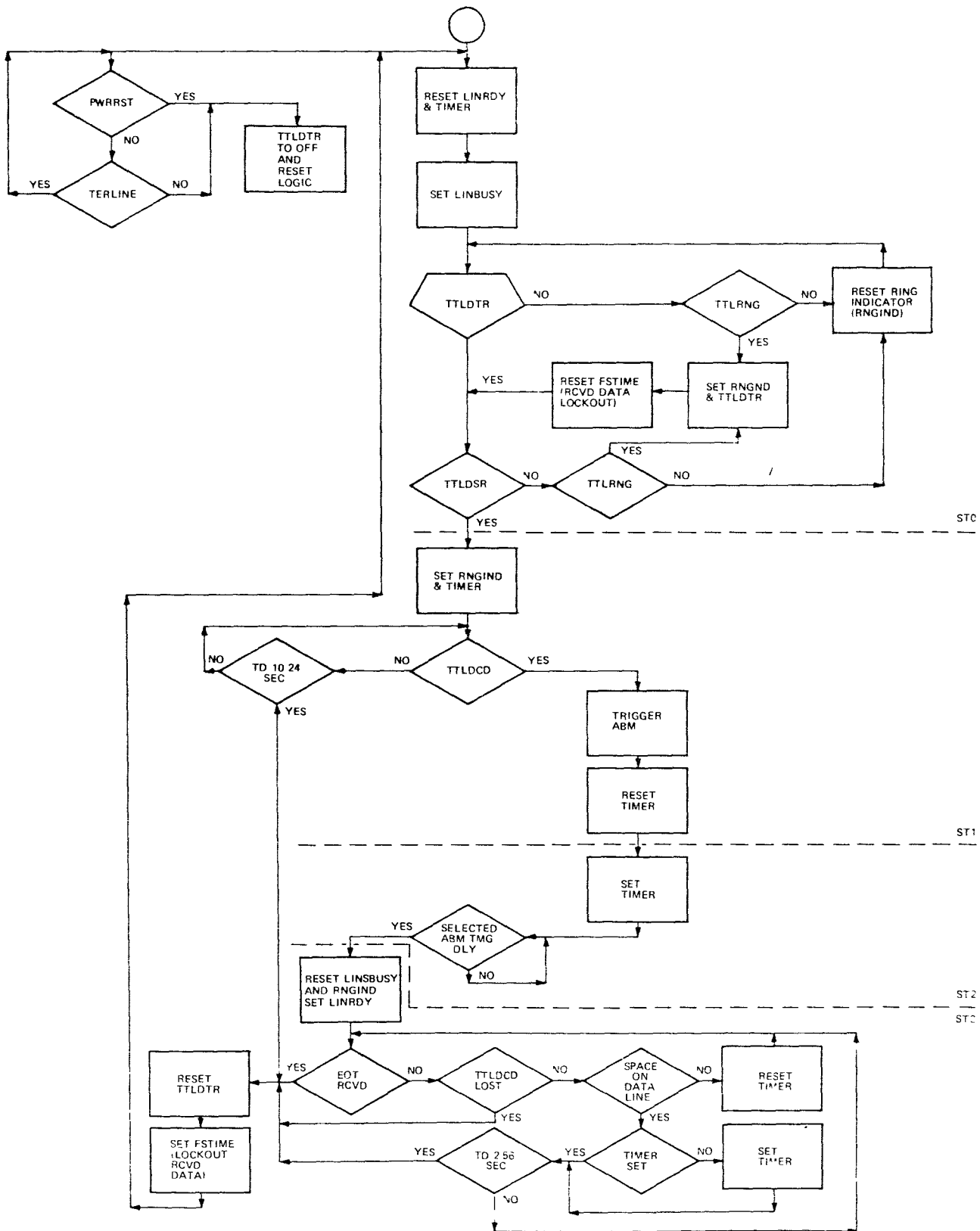


FIGURE 3-9.8. AUTO ANSWER CONTROL, FUNCTIONAL FLOW DIAGRAM

TABLE 3-9.8. AUTOMATIC DISCONNECT AND AUTOMATIC ANSWER-BACK MEMORY TRIGGERING, RESISTOR OPTIONS

To Disable	Delete 10Ω Resistor
Disconnect (hang-up) line upon receipt of EOT character	R5
Long-SPACE Disconnect	R3
Automatic Triggering of Answer-Back Memory	R12

TABLE 3-9.9. STATE EQUATIONS FOR AUTO ANSWER CONTROL

ST0D	= ST1D- * ST2D- * ST3D-
ST1D	= ST0Q * TTLDTR * TTLDSR + ST1Q * (TTLDCD- * TD10.24SEC-)
ST2D	= ST1Q * TTLDCD + ST2Q * TD(xxx)msec-
ST3D	= ST2Q * TD(xxx) MS + ST3Q * RCVEOT- * TTLDCD * TD1.28 Sec-
TIMERRST	= ST0Q + ST1Q * TTLDCD + ST3 * LNDATAQ
TTLDTRD	= TTLRNG + TTLDTR * ((ST1Q + ST3Q) * ST0D-)-
LINBUSY	= ST3Q-
FSTIME	= (ST1Q * TTLDCD) + TTLDTR-
AUX2ROF	= TTLDTR-
TD1.28 SEC	= ST3Q * LNDATAQ- * (1.28-sec delay time)
TD(xxx)MS	= ST2Q * (SELECTED delay time)
TD10.24 SEC	= ST1Q * TTLDCD- * (10.24 sec delay time)
T1MERRST	= ST0Q + ST1Q * TTLDCD + ST3Q * LNDATAQ
STATE 0	= Wait state, no call in progress
STATE 1	= Received ring indication, answer call, and wait for carrier detect (trigger ABM when carrier detect is received)
STATE 2	= Received carrier detect, wait for ABM delay
STATE 3	= ABM delay over, send ABM and set line ready indicator

**TABLE 3-9.10. AUTO ANSWER CONTROL PIN ASSIGNMENTS WITH BELL 103 DATA SET
(CABLE, TI PART NO. 971555-0001)**

Bell 103 Data Set Interface Conn Pin No.	Terminal Conn (J1) Pin No.	Signal Source	Signal Function
1	A	Common	AA – Protective Ground
2	H	Terminal	BA – Transmitted Data
3	10	Data Set	BB – Received Data
5	8	Data Set	CB – Clear-to-Send
6	9	Data Set	CC – Data-Set-Ready
7	7	Common	AB – Signal Ground
8	K	Data Set	CF – Carrier Detect
20	E	Terminal	CD – Data-Terminal-Ready
22	D	Data Set	CE – Ringing Indicator
(All other pins not used)			

**TABLE 3-9.11. AUTO ANSWER CONTROL PIN ASSIGNMENTS WITH BELL TYPE-CBS
DATA ACCESS ARRANGEMENT
(CABLE, TI PART NO. 971557-0001)**

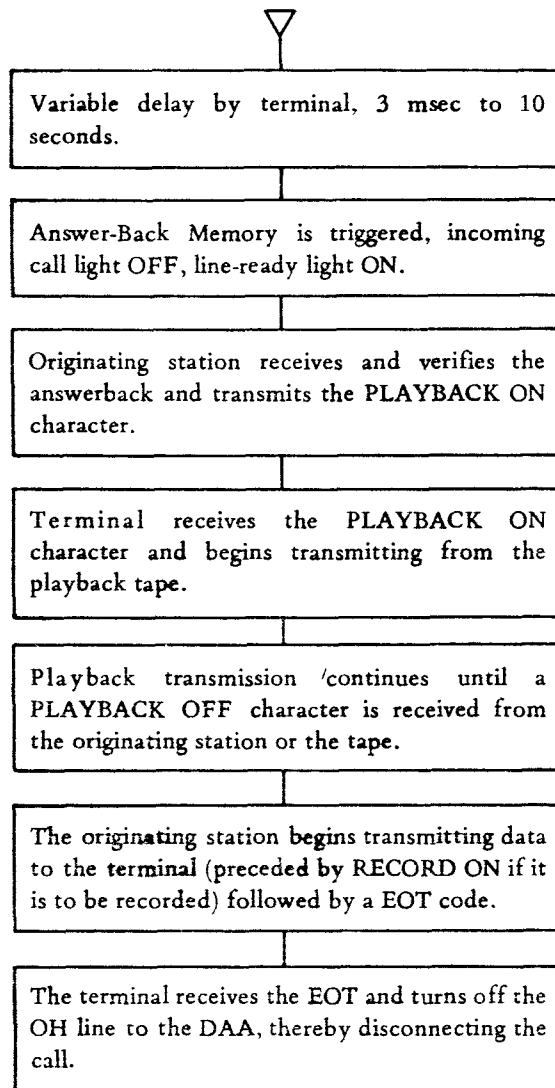
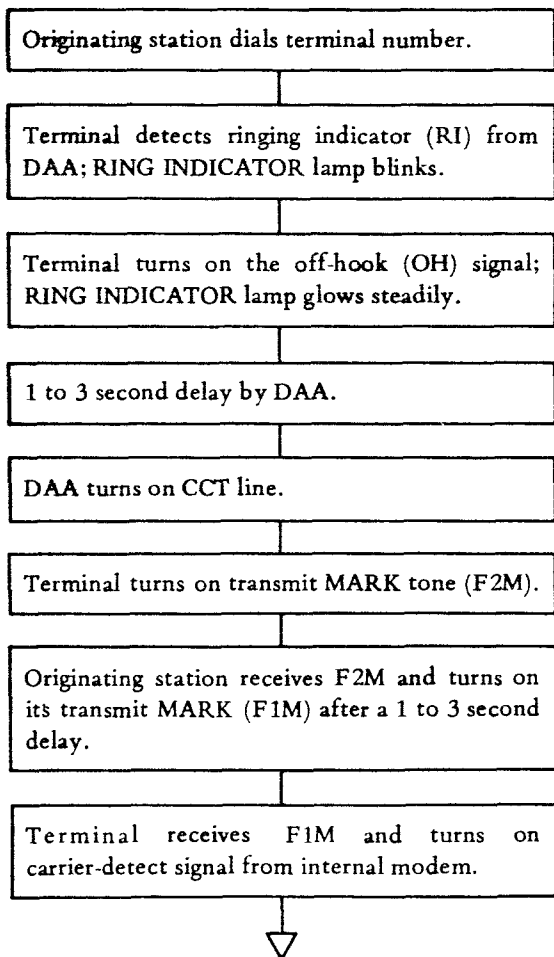
Terminal Conn (J1) Pin No.	DAA Terminal Lugs	Wire Color	Bell Systems Description	Function
C	DT	Orange	Data Tip	Connection to phone line
3	DR	Yellow	Data Ring	Connection to phone line
6	DA	Brown	Data Transmission	Held ON by terminal to request data transmission
E	OH	Red	Off Hook	Held ON by terminal to answer and maintain a call
5	CCT	White	Coupler Cut Through	Held ON by DAA when data path has been established
4	SH	Blue	Switch Hook	Not used by terminal
	SH1		Switch Hook Return	Not used by terminal
7	SG	Black	Signal Ground	Return path for control signals
D	RI	Green	Ring Indicator	Ringing signal present

TERMINAL READY – illuminates when the 733 ON LINE switch is ON-LINE, indicating that the terminal will answer an incoming call.

LINE READY – illuminates when the terminal has answered the call, received the carrier from the originating station and is ready to transmit or receive.

b. Typical Operations

Before leaving the terminal unattended, the operator must switch the appropriate data terminal function (RECORD, PLAYBACK and/or PRINTER) to the LINE mode and the data terminal to ON-LINE. A typical operating sequence (with Answer-Back Memory and Remote Device Control options installed) is shown in the following flow chart.



A flow diagram of the Auto Answer Control functions is shown in Figure 3-9.8, and state equations are listed in Table 3-9.9.

c. Interface Requirements

The control signals to the DAA are compatible with the logic levels and conventions defined in EIA Standard RS232C. The signals-to-phone line (DT and DR) is described under modem options (see Paragraph 3-9.1). The interface connections to the DAA are spade lugs which attach to the screw terminals of the DAA. Pin assignments and functions are listed in Table 3-9.11.

3-9.7 AUTOMATIC SEARCH CONTROL. The Automatic Search Control (ASC) option provides the capability to automatically search at high speed for a desired record contained within a tape cassette. Schematics [971500(M/L) or 971503(M/W)] of the ASC are contained in Appendix C. Signatures are listed in Appendix A.

As shown in Figure 3-9.9, the operator (or remote device if used in conjunction with the Remote Device Control option) enters an activate code on the ASR data bus through the keyboard (or over the remote line). The ASC recognizes the code and if in local mode responds locally by causing a paper advance (KBPA) signal. The printer performs a line feed and a carriage return. The operator (or remote device) can then enter from one to 16 printable USASCII characters into the search field memory of the Automatic Search Control. After the 16th character is entered into memory, the printer is switched off via PRNROFF.

The ASC waits for the cassette to be activated and then writes N-1 characters (one less than entered by keyboard or line) into its cassette data memory. When the cassette data memory is loaded, a character-by-character comparison begins. The ASC then compares up to N-1 characters at which time the ASC waits for one more character from the tape to complete the sequence. If the N-1 field comparison is positive (N-1 matches) and the last character [(N-1)+1] is a match, the ASC stops the cassette and issues a paper advance signal if the data terminal is in local mode. If the fields do not compare, the ASC will shift the cassette data memory data by one character and begin an N-1 compare again.

The read-only memory (ROM) controller is the heart of the Automatic Search Control. The ROM has three basic functions: data path control, data timing and decoding, and logic control.

3-9.7.1 Data Path. The data path begins at the ASR data bus. The ASC converts the serial data to parallel which is applied to the input of the decoders and to the 8-bit parallel buffer register. The output of the buffer register is applied to both the search field memory and the cassette data memory where, at the appropriate time, a write pulse is applied to one of the two memories (16 x 8 bit) to load that character.

The outputs of the memories are continuously fed to two 8-bit magnitude comparators which determine equality. During the character-by-character tape search, the two comparators signify a match.

3-9.7.2 Data Timing and Decoding. Data timing (see Figure 3-9.10) is accomplished by synching the ASC to Terminal Control through two signals: device-enable and terminal control state-ONE. The device-enable determines when a data transfer will take place. The enables are

KB DENA – keyboard data
RDRENA – cassette data playback
RMTENA – line data, generated by the RDC.

Terminal control state-ONE (TCST1) indicates when the data transfer is complete. The data is actually transferred by the serial clock (SCLK). The flipflop CHR DY sets when the correct enable is up, the eight serial clocks have passed, and the falling edge of TCST1 occurs. At this point in the data path, the data is stable, so the outputs of the decoders are inspected for

Printable characters
Activate code (ESC and \$),

If the character is printable, a signal (CHROK) is sent to logic control to signify that the character is ready and printable.

3-9.7.3 Logic Control. The logic control performs two primary functions: state control and function control.

- a. State Control – State Control is implemented in three basic steps: (1) defining the step-by-step sequence in which the controller operates; (2) storing the steps into a permanent read-only memory (ROM) to be recalled later in a predetermined sequence; and (3) implementing the ROM control to assign each step or memory cell to a specific forcing function.

The flow chart (Figure 3-9.11) and block diagram (Figure 3-9.12) illustrate the concept. The diamonds on the flow chart represent forcing functions; the rectangles are control functions; and the connecting lines are jump paths. For example, note that state 11 (state numbers are written in each block) has three jump paths (J0, J1, J2) and two forcing functions (STOP BIT and MATCH). The dominant forcing function is STOP BIT which determines the primary decision regardless of MATCH. If STOP BIT is true, the memory output forces the state counter to address 10; if it is false, MATCH determines whether address OF or OE is forced.

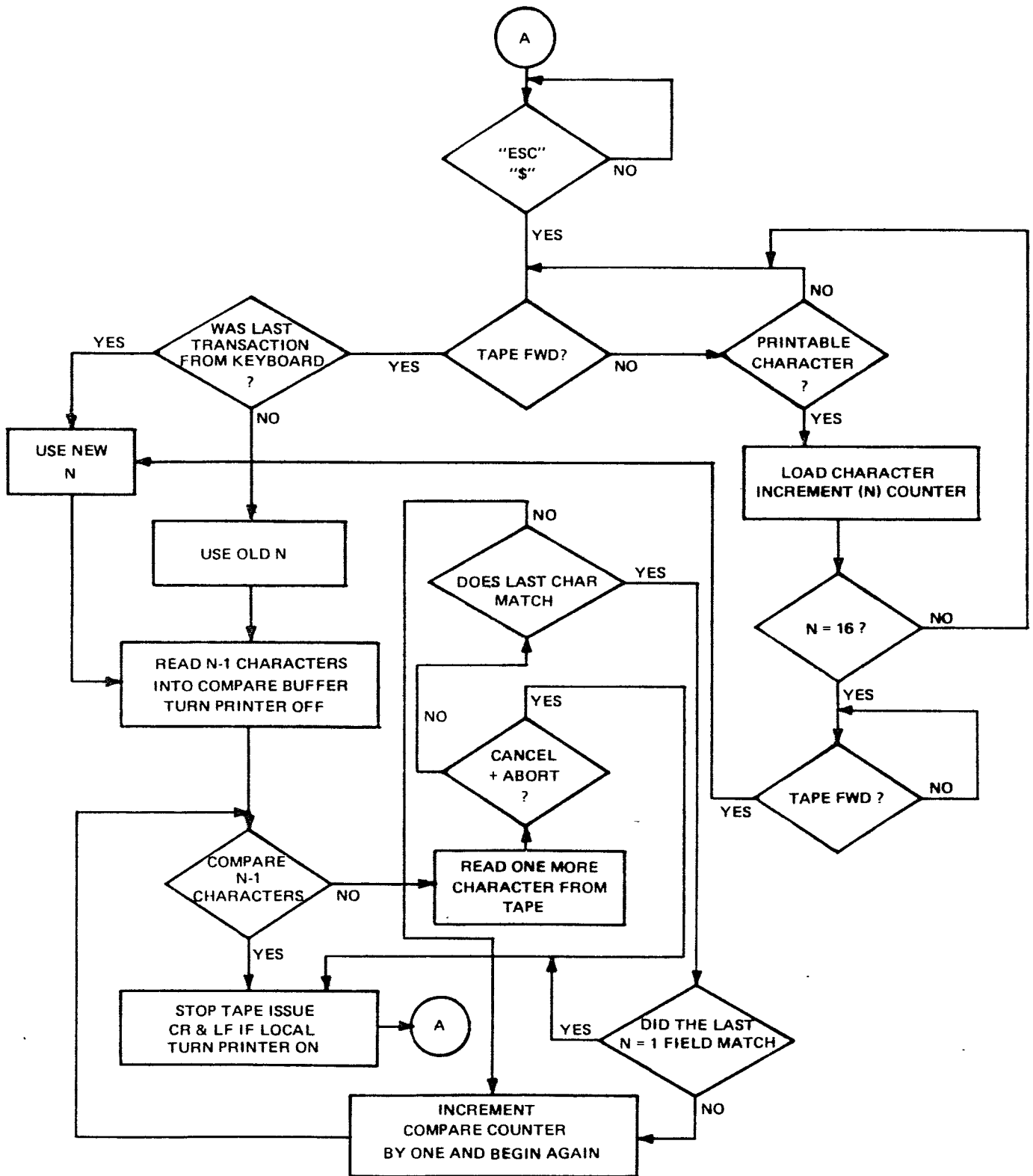


FIGURE 3-9.9. AUTOMATIC SEARCH CONTROL SIMPLIFIED FLOW CHART

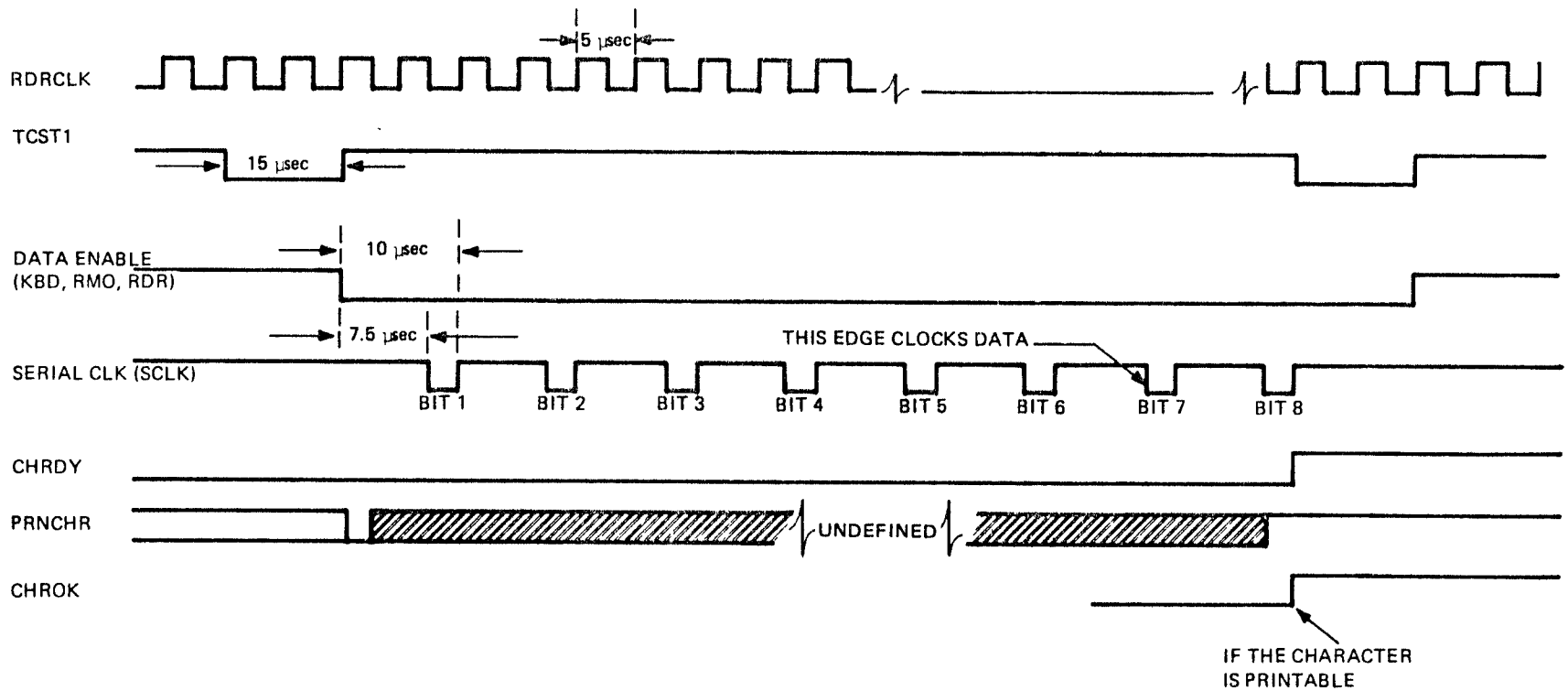


FIGURE 3-9.10. AUTOMATIC SEARCH CONTROL DATA TIMING

Thus, address 11 has three possible next address jump paths: J0 = OE, J1 = OF, and J2 = 10. The method by which they are chosen is determined by the conditions of the forcing functions STOP BIT and MATCH when the clock switches.

The forcing functions are selected by a 2-bit wide, 24-position multiplexer. The multiplexer consists of three sections of two (8 → 1) multiplexers, which are separated into two control bits: A and B. When, for example, address ZERO is applied to the multiplexer, AAM slot-zero is switched to a three-input OR gate (SELA); and BAM multiplexer slot ZERO is switched to a three-input OR gate (SELB).

SELA and SELB are coded into a 2-bit field to select the jump paths. Actually, there are four jump paths: J0, J1, J2, and PA (present address). However, PA is not stored in memory since it is available at the output of the memory address register. A truth table for these four jump paths is shown below.

<u>Bit A</u>	<u>Bit B</u>	<u>PATH</u>
0	0	PA
0	1	J1
1	1	J2
1	0	J0

The A/B bits are applied to the next address (NAM-NEM) selectors which are 4 → 1 multiplexers. The outputs of these selectors are

applied to the inputs of the memory address register (NAA-NAE) the output of which is fed to the five ROM's.

- b. **Function Control.** The function controls operate much the same way as the state control. The control lines needed to make things happen (clock counters, operators, reset flipflops and control data path) are well defined in Figure 3-9.11. The control line functions are stored in the control ROM to be used where appropriate. Each control line is a discrete line from a ROM to the particular device to be clocked or gated, and each line is preprogrammed to switch HIGH or LOW in those states shown in Figure 3-9.11.

The flow chart in Figure 3-9.11 shows that state 11 can step to any of three states: 10 via path J2, OF via J1, and OE via J0. As the controller steps through one of these states, it must perform its assigned task. The following control functions occur each time the controller passes through the noted states.

<u>State</u>	<u>Transfer Function (Control Function)</u>
OE	Increment SF memory address (INCSFMA) Increment Cassette Data RAM address register (INCDRAR)
OF	INCSFMA INCDRAR
	Clear the compare flag (0 → CPRFG)
10	Wait for diamond decisions

3-9.8 REMOTE DEVICE CONTROL. The optional Remote Device Control (RDC) consists of a single printed-circuit card which plugs into KSR card slot A6. A manual ON/OFF switch for the RDC is located atop the PC card, accessible by lifting the terminal cover. Schematics of the RDC [971499(M/L) and 971504(M/W)] are contained in Appendix C.

The RDC permits remote control of most 733 ASR operations via data received over the communication line. The RDC decodes and acts upon on-line data in the form of ASCII character and control codes.

3-9.8.1 Function Codes. All functions are performed by the RDC upon receipt of specific ASCII characters which are established by a programmable read-only memory (PROM) and an option resistor on the RDC PC card. Five functions are performed with single characters from the USASCII control character subset. All other functions are performed using a sequence of two USASCII characters: the first character is derived from the control character subset; the second character is derived from either the control character subset or the third and fourth columns of the USASCII code (see Table 3-4.2), as selected by the option resistor.

NOTE

Once a function is selected in one of the two subsets, all other functions are contained in the same subset.

The standard function code selections are listed below.

a. Single-Character Functions

Playback ON	DC1
Playback OFF	DC3
Record ON	DC2
Record OFF	DC4
Autodisconnect (when used) with Auto Answer Control option – EOT	

First character of double-character sequence – (normally DLE)

b. Two-Character Functions – These functions are performed using the USASCII control character DLE plus the following character

Rewind cassette-1	1
Rewind cassette-2	2
Load cassette-1	3
Load cassette-2	4

Cassette-1 in RECORD mode	5
Cassette-2 in RECORD mode	6
Block forward	7
Block reverse	8
Printer ON	9
Printer OFF	0
Auto Device Control ON	:
Auto Device Control OFF	;
Request status	<
1200-baud print local	>
ASC remote cancel	?

NOTE

The printer is automatically disabled from printing the first character following receipt of the DLE character.

c. Function Description

Playback On – enables the tape playback function

Playback Off – disables the tape playback function

Record On – enables the tape recording function.

Record Off – disables the tape recording function.

Auto Disconnect (EOT) – disconnects the printing and recording functions from on-line (if used in conjunction with Auto Answer Control option).

Rewind Cassette 1 – causes the tape in cassette-1 to slew at high speed toward the beginning of tape until clear leader is sensed.

Rewind Cassette 2 – causes the tape in cassette-2 to slew at high speed toward the beginning of tape until clear leader is sensed.

Load Cassette 1* – causes the tape in cassette-1 to wind forward from clear leader to the beginning of tape.

Load Cassette 2* – causes the tape in cassette-2 to wind forward from clear leader to the beginning of tape.

Cassette-1 in Record Mode – places cassette-1 in RECORD mode; cassette-2 will be in PLAYBACK mode (dual-cassette models).

*If the tape cassette is not on clear leader (i.e., it is on tape), a fast forward will initiate. A fast forward cannot be stopped by a remote command.

Cassette-2 in Record Mode — places cassette-2 in RECORD mode (dual-cassette models); cassette-1 will be in PLAYBACK mode (all models).

Block Forward — causes the next block on tape to be read and played back (or the remainder of a block if playback stopped in the middle of a block).

Block Reverse — causes the tape to reverse one block and stop.

Printer On — enables the printer to receive data from the communications line (if the PRINTER switch is set to LINE) after having been disabled.

Printer Off — disables the printer from receiving line data. If this code sequence is received when the printer is in either the LINE or LOCAL mode, the printer is disabled while in the LINE mode. This function is reset and reverts to the Printer-ON condition when the terminal is switched OFF-LINE or when power is switched OFF and ON.

Auto Device Control ON — enables the functions playback ON/OFF (DC1, DC3) and record ON/OFF (DC2, DC4) after having been disabled by the Auto Device control OFF function.

Auto Device Control OFF — disables the functions playback ON/OFF (DC1, DC3) and record ON/OFF (DC2, DC4), which is particularly useful when recording data from the line containing the playback ON/OFF or record ON/OFF characters (e.g., format tapes). ADC OFF is reset and reverts back to the ON condition when the terminal is switched OFF LINE, or power is switched OFF and ON.

Request Status — enables the terminal to send the status character (see below). It is particularly useful in determining when a rewind, load, or other function has been completed.

3-9.8.2 Status Character. The status character is a USASCII character transmitted by the data terminal when the “request-status” code is received from the line. The specific status and bit locations are

Bit 1 (least significant bit) indicates the playback function is ready when bit 1 is a logic ONE. If bit 1 is a logic ZERO, playback is NOT ready for one of the following reasons:

- (1) Cassette door open or cassette not in place
- (2) Cassette on clear leader
- (3) Playback not in LINE mode
- (4) Other operations being performed; e.g., rewind.

Bit 2 — indicates a playback error has been made if bit 2 is a logic ONE. A logic ZERO indicates a playback error has not been made. If the playback is strapped so as not to stop on an error (see paragraph 2-6.2), bit 2 will indicate a ONE only while a block with an error is being (or waiting to be) transmitted.

NOTE

A playback error may be cleared using the remote control functions PLAYBACK ON, BLOCK REV, or BLOCK FWD.

Bit 3 — indicates cassette 1 is on clear leader at either end of tape if Bit 3 is a logic ONE. A logic ZERO indicates the cassette is not on clear leader.

Bit 4 — same function as bit 3 for cassette 2.

Bit 5 — indicates that the record function is ready to be enabled with the record ON signal when bit 5 is a logic ONE. If bit 5 is a logic ZERO, record is not ready for one of the following reasons:

- (1) Cassette-door-open or cassette-not-in-place
- (2) Cassette on clear leader
- (3) Record not in LINE mode
- (4) Other operation being performed; i.e., rewind or load
- (5) Tape cassette write tab removed.

Bit 6 — indicates that the printer is ready when bit 6 is a logic ONE. If bit 6 is a logic ZERO, the printer is not ready for one of the following reasons:

- (1) Printer not in LINE mode
- (2) Printer is off as a result of "printer off" command, or the Automatic Search Control (ASC) is searching.

Bit 7 – always a logic ONE to force the status character out of the control character subset. This bit may be optionally switched on the PC card to indicate PLAYBACK-ON status (see Table 3-9.12). In this case a logic ZERO indicates playback is on (i.e., playback either reading tape or transmitting data) and a logic ONE indicates playback is not on. Bit 7 is particularly helpful in determining when the ASC is searching tape and when the search is completed. If bit 7 is used, the status character is not excluded from the control character subset.

EXAMPLE

If playback is ready, a playback error has not been made, cassette-1 is not on clear leader, cassette-2 is on clear leader, record is not ready, and printer is ready, the status character would be

b ₁ – ONE	}	= USASCII character "i"
b ₂ – ZERO		
b ₃ – ZERO		
b ₄ – ONE		
b ₅ – ZERO		
b ₆ – ONE		
b ₇ – ONE (strapped to logic ONE)		

3-9.8.3 Function Operating Modes. The remote control functions are performed when the appropriate codes are contained in the transmitted, received, and/or local data as described in the following paragraphs.

- a. **Playback On/Off** – The playback-OFF function is performed on transmitted, received, or local data. It may be disabled in any one or all modes using pencil switch S-2 on the RDC PC card as shown in Table 3-9.12. The playback ON function is performed on only received or local data; it too may be disabled using the pencil switch.
- b. **Record On/Off** – The record ON/OFF function is performed only on received or local data. It may be disabled on received and/or local data via the pencil switch as shown in Table 3-9.12.

- c. **Manual Function Disable Control** – A switch located atop the RDC PC card permits switching off all functions except the auto-disconnect function EOT character when used with the Auto Answer Control option.
- d. **Other Functions** – All other functions are enabled only on received data.

3-9.8.4 Additional RDC Card Options.

- a. **Remote Search (with ASC Option)** – The RDC permits remote initiation of the optional Automatic Search Control (ASC) from the communication line. The initiation sequence to the ASC is enabled if PLAYBACK is set to LINE, the cassette is ready and the RDC is ON. Once search is started, the same conditions are also required for the ASC remote cancel code to be acted on. If these conditions are met and the double-character ASC remote cancel code is received from the line, the RDC will send a search cancel signal to the ASC. Status may be requested from the controlling device any time during the search. The on-line search speed is always 320 characters per second. No on-line tape duplication during search is possible.

During an on-line search, the DC3 (PLAYBACK OFF) control character will be ignored if encountered. No data is transmitted during an on-line search except status (if requested) or the CAN character if a playback error occurs, and the CAN character is enabled.

- b. **Automatic ASCII "CAN" character on Playback Error** – If this switch-selectable option is set on the RDC, the ASCII CAN character will be automatically transmitted to the line whenever a read error is detected during playback. The conditions required for sending an automatic indication of an error are
 - (1) Playback must be on-line and ready.
 - (2) The RDC PC card must be ON.
 - (3) A playback error must be detected by the playback controller.

This switch-selectable option (S-2, position 7) is normally open, which disables automatic transmission of the CAN character on a playback error.

TABLE 3-9.12. RDC PC CARD SWITCH S2 OPTIONS

Switch S2 Position	Function	Data Source	Normal Switch State
1	Record ON/OFF	Local data	ON
2	Record ON/OFF	Received data	
3	Playback ON/OFF	Local data	
4	Playback ON/OFF	Received data	
5	Playback OFF	Transmitted data	OFF
6	Playback-ON Status	N/A	
7	CANcel character on read error	N/A	

TABLE 3-9.13. REMOTE DEVICE CONTROL CODE BITS FOR ASR (UPPER UNIT) FUNCTIONS

Code Bits					Decoded Signal	Function
1	2	3	4	Strobe		
1	1	1	1	1	RDRON	Playback On (DC1)
0	1	1	1	1	RDROF	Playback Off (DC3)
1	0	1	1	1	RCDON	Record On (DC2)
0	0	1	1	1	RCDOF	Record Off (DC4)
1	1	0	1	1	XREW1	Rewind Cassette-1
0	1	0	1	1	XREW2	Rewind Cassette-2
1	0	0	1	1	XLD/FW1	Load or F/FWD Cassette-1
0	0	0	1	1	XLD/FW2	Load or F/FWD Cassette-2
1	1	1	0	1	XBSPFW	Block Forward
0	1	1	0	1	XBSPRV	Block Reverse
1	0	1	0	1	XC1RCD	Cassette-1 Record
0	0	1	0	1	XC2RCD	Cassette-2 Record
1	1	0	0	1	XRCHFW	Send One Character
0	1	0	0	1	XCA1STP	Cassette-1 Stop
1	0	0	0	1	XCA2STP	Cassette-2 Stop
0	0	0	0	1	Unused	

c. Footswitch for Local Playback-ON – This feature on the RDC permits use of a footswitch which closes a contact to ground to initiate the playback-ON function. Conditions required for enabling the footswitch are

- (1) Playback must be local.
- (2) The RDC card must be ON.

d. Rewind from the Right End – This feature on the RDC permits rewinding a tape cassette which is on clear leader at the right end of the tape: i.e., the takeup reel is full and the END lamp is illuminated. The only conditions required for this action are

- (1) The cassette to be rewound is on clear leader.
- (2) A rewind command for that cassette is issued.

NOTE

When a rewind from clear leader command is issued, no other RDC card functions can be used for 1.2 seconds.

e. 1200 Baud Print LOCAL – Not normally installed, this option provides a decoded output for use by the 1200-baud Transmit/Receive PC card with Auto Answer Control to perform the 1200-baud print-local function. The 1200-baud print local command is a standard two-character decode, activated when the command is received from the communication line.

f. Printer On/Off Command with DC2 and DC4 – The standard printer-ON/OFF commands are normally two-character codes. If the RDC incorporates this single-character option, the printer-OFF command may be initiated by the single ASCII DC2 (record-ON) character rather than the double-character sequence of DLE and 0 (zero). Similarly, the printer-ON command may be initiated by the single ASCII DC4 (record-OFF) character rather than the double-character sequence of DLE and 9. With this option the standard double-character printer ON/OFF commands are ignored by the RDC. This option is normally not installed on

the RDC. If used, the rewind from-right-end feature described in paragraph d. above is not possible.

3-9.8.5 Theory of Operation. The optional Remote Device Control (RDC) has two main functions:

- (1) Decoding characters from the serial data bus and causing initiation of the appropriate action for that code or code sequence

- (2) Performing certain additional on-line or local functions, including the footswitch pedal option, automatic sending of the ASCII CAN character upon detecting a playback error, 1200-baud print-local option remote search option (with the Automatic Search Control), and rewind the tape cassette from the right-end option.

- a. Character decoding from the serial data bus – The RDC monitors the serial data bus at all times and decodes those characters selected to perform certain functions. Data from the serial bus is clocked into an input register on each set of eight system clocks (SCLK_n). The last 2 bits of the ASCII character (bit 6 and bit 7) are then decoded to indicate that the character is either in columns 1 and 2 (control characters) of the ASCII code table (see Table 3-4.2) or in columns 3 and 4 (printable characters) of the ASCII code table. Bits 1 through 5 are then decoded by a read-only memory to indicate the character within the two columns selected.

The PROM is programmed to encode the input character (5 bits) into two sets of output lines. One set of three output lines indicates up to seven single-level decodes, and one set of five output lines indicates up to 16 double-level decodes. The output lines are then decoded by a three-line to eight-line single-character decoder and a four-line to 16-line double-character decoder into discrete lines which represent each function performed by the RDC.

If the first character of a double-character sequence (normally DLE) has not been received, only the single-character decoder will be enabled. When the double-character initiator is received from the line with a serial receiver enable (SRVENA-), a flipflop is set (ESCQ)

which enables the double-character decoder for received line data (i.e., that data on the bus during SRVENA-). It will stay enabled until the next character is received from the line. During this period the single-level decoder will still be enabled on transmitted data (during XMTENA-) and during local data transfer (on LOCDAT-). Once the second character of the double-character code is received from the line, the ESCQ flipflop is reset, the double-character decoder is disabled, and the single-character decoder is then re-enabled to line data (on SRVENA-). The ESCQ flipflop (when enabled) also disables the printer when it is on-line via the printer-remote-off (PRNROF-) line, so that the second character of the double-character sequence will not be printed.

All functions decoded which affect the ASR upper unit (record, playback, cassette motion control, or mode select) must be sent to the upper unit via a 4-bit code and a strobe pulse. When any line from either the single- or double-character decoder is low at time Q0 (TIMEQ0), the indication is clocked into a holding register until the next TIMEQ0 (88 μ sec) at which time the present indication (REWIND CASSETTE-1, LOAD CASSETTE-2, etc.) is removed and the next indication, if any is clocked into the holding register (RDC timing is shown in Figure 3-9.12).

While the indication is in the holding register, the code bit encoder is putting the proper code bits (CDBIT1- through CDBIT4-) on the code bit lines going to the ASR upper unit. As shown in Table 3-9.13 the code bits are on the lines, a 5- μ sec strobe (CDSTRB-) is issued at TIMEQ4, and the appropriate action is taken in the ASR upper unit. The strobe is a free-running clock from the timing generator on the PC card. The strobe bits are always issued for a function for 88 μ sec starting from TIMEQ0 at the end of the enable on which the function was decoded until the next TIMEQ0.

The strobe is always issued at TIMEQ4 during each 88 μ sec period of the timer generator (between TIMEQ0 times). The timer generator times are synchronized to terminal control via the terminal control state-ONE (TCST1) signal as shown in Figure 3-9.13. Therefore, all the

times (TIMEQ0, TIMEQ6, etc.) always have the same relationship to the enables issued by terminal control.

The double-character functions can be decoded only from received data (SRVENA-), but the playback ON/OFF and record ON/OFF functions (PC1 through PC4) are optionally selectable using switches (S2) on the RDC PC card. This is done by enabling the single-character decoder output lines for these four functions into the holding register only if the appropriate switch is closed. For example, if the switch for enabling DC1 and DC3 is closed, both these inputs to the holding register are enabled for all local data on the bus. Local data is signified by the local data (DATLOC-) signal from terminal control.

Similarly, transmitted data is signified by the transmit enable (XMTENA-) signal and received data by the serial receiver enable (SRVENA-) signals from terminal control.

- b. Additional RDC card line and local functions – The RDC performs several double-character or single-character decodes which do not affect the ASR upper unit and several optional functions. As a reference to all resistor and pencil switch options, see the RDC schematic (971504 or 971499) in Appendix C.

- (1) Printer ON/OFF. When the printer-OFF code is received from the line, a latch (PRNOFQ) is set at TIMEQ0 which keeps the printer OFF via the PRNROF- line as long as the terminal is on-line. The latch is reset upon receiving the printer-ON code from the line or if the terminal is taken off-line or the RDC PC card is switched OFF. When the RDC card is off via the toggle switch on the PC card, all RDC functions are inhibited except decoding of the ASCII EOT character (used by Auto Answer Control to disconnect a call). The printer-OFF latch may be optionally resistor-strapped to be set/reset upon receiving from the line (SRVENA-) the single-level decoder DC2 and DC4 output lines, respectively. If this option is selected, the double-character decoder lines are not used. See the RDC

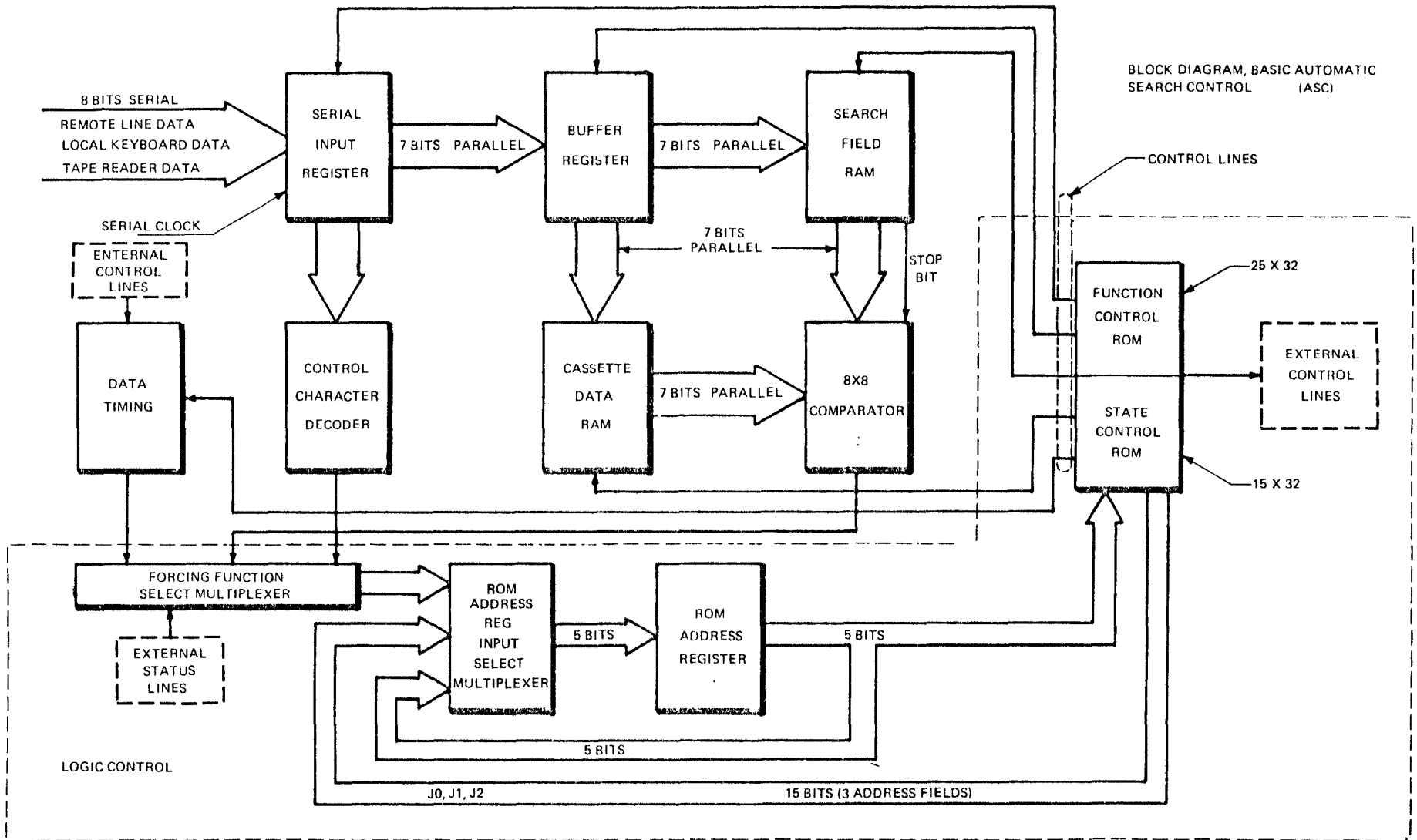


FIGURE 3-9.12. AUTOMATIC SEARCH CONTROL BLOCK DIAGRAM

schematic (971499) for a list of RDC card options and appropriate resistor straps.

- (2) 1200-baud print LOCAL. A double-character decoder output line is provided for the 1200-baud print local option to use. This line is true only between the falling edge of the eighth system clock (SCLK-) for each SRVENA- and the rising edge of the TIMEQ0 signal (see the RDC timing diagram, Figure 3-9.13). The 1200-baud print-local option is described in paragraph 3-9.8.4.e.
- (3) DC1-4 ON/OFF. Upon receipt of the double-character decoder DC1-to-4 OFF code, a latch is set at TIMEQ0 which inhibits the DC1 through DC4 codes from being acted upon when received from the line. This is done by gating out the SRVENA- signal going to the DC1-to-DC4 enabling option logic and switches, so that these functions cannot be strobed into the holding registers on a SRVENA- signal at timeQ0. The latch (DC1-4 OFFQ) is reset upon receipt of the DC1-4 ON code from the line or by switching the terminal off-line or by switching off the RDC OFF toggle switch.
- (4) Status Request. Upon receipt of the status request code from the line, a status flipflop (STATUSQ) clocks in the state of the status (STAT-) output line from the double-character decoder at TIMEQ0. At TIMEQ5 an auxiliary-1 request (AUX1REQ-) is sent to terminal control, and at TIMEQ6 the status flipflop is cleared. When terminal control sends back an auxiliary-1-enable-to-send (AUX1ENAS-), the status is clocked from the status register on the RDC card to the transmitter and sent to the line as a 7-bit ASCII character. All bits of the status character are obtained from information on the KSR motherboard except the printer-off (PRNOFF-) indication which comes from the serial data bus during the status enable (STATUSENA-) time from terminal control.

The PRNOFF- bit is the eighth bit of the terminal status word and is clocked into a flipflop on the RDC PC card for use with the printer-local (PRNLOC-) and printer remote-off (PRNROF-) signals to provide the printer-ready bit of the status character sent to the line.

The seventh bit of the status character sent to the line is switch-selectable to be always a ONE (forces status character not to be a control character) or to indicate the playback-not-on (PBKON-) status. Examples of possible status indications which could be sent by the RDC on request, and the ASCII characters that the status would represent, are shown in Table 3-9.14.

- (5) ASCII CAN character on playback error. The playback error status bit (RERROR) is monitored from an available KSR motherboard signal. When a playback error occurs, the RERROR indication is clocked into a register on the RDC PC card at TIMEQ0 (see RDC timing, Figure 3-9.13) and becomes RERRORQ. The RERRORQ signal going HIGH clocks a cancel/status flipflop (if the playback is on-line and ready and the OPTION switch is closed) which selects which data will be sent to the serial data bus on the next auxiliary-1-enable-to-send (AUX1ENAS-) signal from terminal control.

The data which goes to the data bus on the AUX1ENAS- signal comes from either the status register or the cancel-character register as selected by the flipflop. The playback error will be detected in a status-enable time period, and on the next TIMEQ5 time a request (AUX1REQ-) will be sent to terminal control to transmit the CAN character.

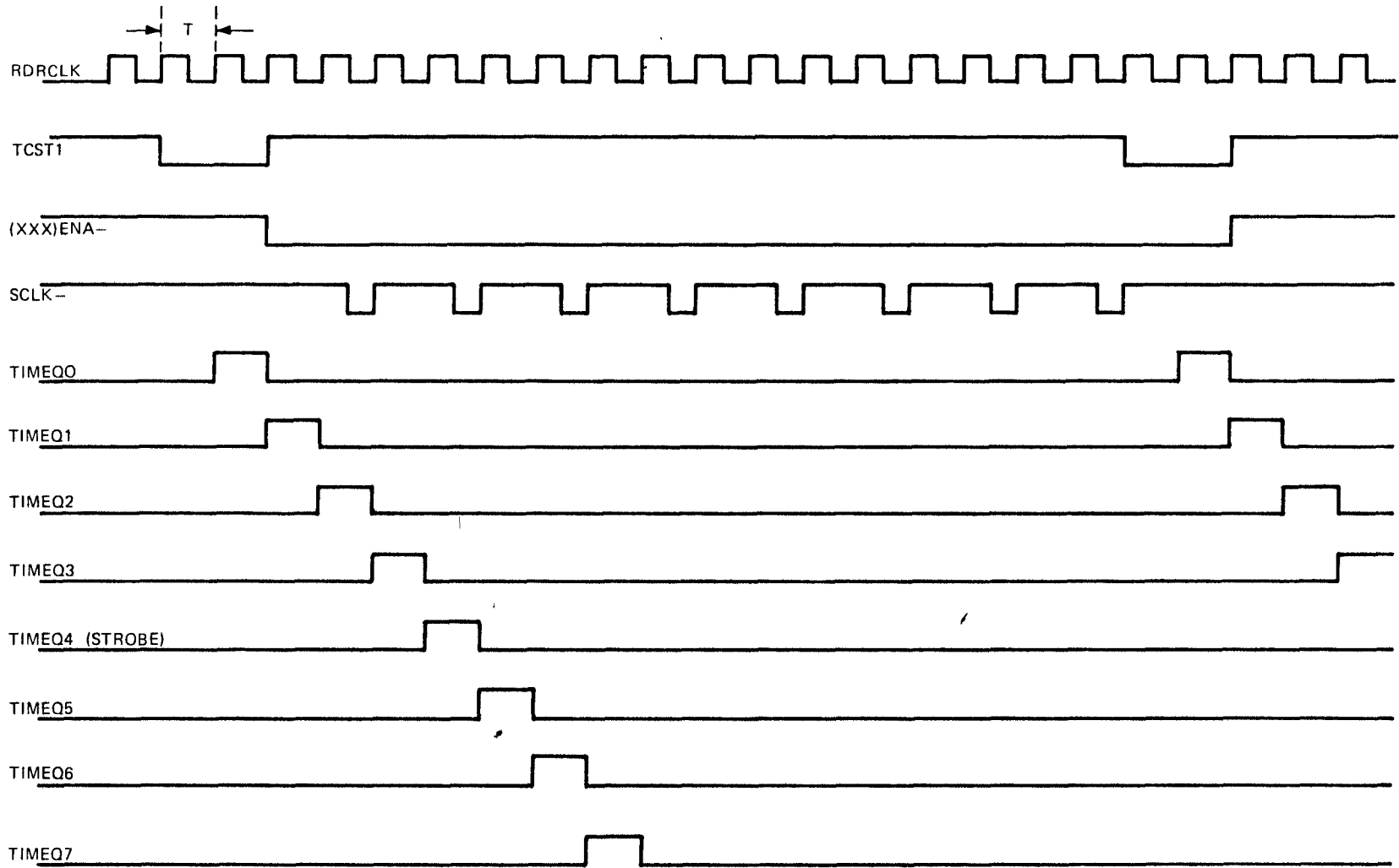
The cancel/status flipflop is reset during the CANRSTENA period at TIMEQ0 as shown in Figure 3-9.13, and data sent after that will come from the status register until another playback error is detected. The CAN character option is inhibited by either opening the pencil switch (S2-7)

TABLE 3-9.14. REMOTE DEVICE CONTROL STATUS CODES AND CHARACTERS

Status Character	Status Code								Status Character	Status Code							
	Parity	High (ONE) or Playback OFF	Printer Ready (ONE)	Recorder Ready (ONE)	Clear Leader Cassette-2	Clear Leader Cassette-1	Playback Error (ONE)	Playback Ready (ONE)		Parity	High (ONE) or Playback OFF	Printer Ready (ONE)	Recorder Ready (ONE)	Clear Leader Cassette-2	Clear Leader Cassette-1	Playback Error (ONE)	Playback Ready (ONE)
	b 8	b 7	b 6	b 5	b 4	b 3	b 2	b 1		b 8	b 7	b 6	b 5	b 4	b 3	b 2	b 1
@	P	1	0	0	0	0	0	0	\	P	1	1	0	0	0	0	0
A	P	1	0	0	0	0	0	1	a	P	1	1	0	0	0	0	1
C	P	1	0	0	0	0	0	1	c	P	1	1	0	0	0	0	1
D	P	1	0	0	0	0	1	0	d	P	1	1	0	0	1	0	0
E	P	1	0	0	0	0	1	0	e	P	1	1	0	0	1	0	1
G	P	1	0	0	0	0	1	1	g	P	1	1	0	0	1	1	1
H	P	1	0	0	0	1	0	0	h	P	1	1	0	1	0	0	0
I	P	1	0	0	0	1	0	0	i	P	1	1	0	1	0	0	1
K	P	1	0	0	1	0	1	1	k	P	1	1	0	1	0	1	1
L	P	1	0	0	1	1	0	0	l	P	1	1	0	1	1	0	0
P	P	1	0	1	0	0	0	0	p	P	1	1	1	0	0	0	0
Q	P	1	0	1	0	0	0	1	q	P	1	1	1	0	0	0	1
S	P	1	0	1	0	0	1	1	s	P	1	1	1	0	0	1	1
T	P	1	0	1	0	1	0	0	t	P	1	1	1	0	1	0	0
X	P	1	0	1	1	0	0	0	x	P	1	1	1	1	0	0	0
SOH	P	0	0	0	0	0	0	1	'	P	0	1	0	0	0	0	1
ETX	P	0	0	0	0	0	1	1	#	P	0	1	0	0	0	1	1
ENQ	P	0	0	0	0	1	0	1	%	P	0	1	0	0	1	0	1
BEL	P	0	0	0	0	1	1	1	/	P	0	1	0	0	1	1	1
HT	P	0	0	0	1	0	0	1)	P	0	1	0	1	0	0	1
VT	P	0	0	0	1	0	1	1	+	P	0	1	0	1	0	1	1
DC1	P	0	0	1	0	0	0	1	1	P	0	1	1	0	0	0	1
DC3	P	0	0	1	0	0	1	1	3	P	0	1	1	0	0	1	1

*Bit 7 is normally held in the logic ONE state. If the playback-OFF indication option is used (S2-6 in ON position), a logic ONE indicates the playback function is OFF and a logic ZERO indicates the playback function is ON. When the playback-OFF option is used, some status characters may be control characters as indicated by the shaded characters in the table.

$T = 1/0.2048 \text{ msec} = 4.9 \text{ msec}$



3-127

FIGURE 3-9.13. REMOTE DEVICE CONTROL TIMING DIAGRAM

for that option or by switching off the RDC PC card toggle switch.

- (6) Footswitch option. A footswitch contact closure to ground is provided as an input to the RDC. The playback-ON (DC1) function can be initiated by footswitch if the PLAYBACK switch is set to LOCAL, and the cassette is loaded and ready. The footswitch provides a contact closure to ground with a switch bounce of 1 msec or less. (The TTL signal input is a low-going pulse, the width of which exceeds 1.25 msec).

The footswitch input is debounced by the C800 clock (1.25 msec period). When the footswitch is depressed, the debounce flipflop clocks the footswitch flipflop if the PLAYBACK is not set to LINE and the RDC card is ON. On the next status enable period at TIMEQ0, the playback-ON (DC1) function is clocked into the holding register and encoded to the 4 cassette data bits. When the DC1 function is issued (DC1Q), the footswitch flipflop is cleared until the next footswitch actuation. The footswitch input (FOOTSWITCH-) to the RDC is resistor-strappable to pin 28 (J2,L), or it may be hard-wire-strapped to any other RDC PC card output pin.

- (7) Local/Remote Search Option (with optional Automatic Search Control). When the optional Automatic Search Control (ASC) is searching tape, the ASCSRCH- line is low. If the PLAYBACK switch is set to LOCAL, the SRCHLOC signal locks out the local data enable (DATLOC-) so that the RDC does not detect the DC1 through DC4 functions while the search is in progress. If the PLAYBACK switch is set to LINE, the SRCHLN signal locks out the transmit enable (XMTENA-) to the RDC so that it will not act on the DC3 function. As long as there is no auxiliary-1 enable to send (AUX1ENS-), such as a status request or CAN character transmission, the transmit inhibit line [XMTINH, Pin 31 (300 baud), Pin 33

(1200 baud)] is kept low so that the transmitter does not detect the transmit enables. Since no transmit enable is detected by the transmitter, it does not hold the line busy (LINBUSY-); therefore, the playback can send data at maximum search speed (320 characters per second). When the PLAYBACK is set to LINE and is ready and the RDC card is ON, the remote enable (RMTENA-) line to the ASC PC card is active. If the ASC initiate code is received from the line via a SRVENA- signal, the code is passed on to the ASC PC card through the RMTENA- line. Also, if PLAYBACK is set to LINE and is ready and the RDC PC card is ON, the double-character ASC cancel code, when received from the line, will cause an 88- μ sec (TIMEQ0 to TIMEQ0) cancel signal to be sent to the ASC PC card via the remote cancel line (RMTCAN-) between the cards.

- (8) Rewind From the Right End Option. The logic in the ASR upper unit tape motion controller is designed so that rewinding a tape from clear leader requires depressing and holding the REWIND switch for that cassette until the tape winds past clear leader and onto magnetic tape. The RDC PC card must simulate holding the REWIND switch depressed by holding the strobe line (CDSTRB-) low and keeping the rewind code on the cassette data lines until the tape has passed clear leader.

When the RDC logic senses that either cassette is on clear leader and a rewind command for that cassette is issued from the line, a oneshot timer is fired which holds the strobe low and disables the timing generator (TIMEQ0 generator) for 1 ± 0.2 seconds. By disabling the timing generator the rewind code just issued will remain in the holding register until the timing generator can again send a TIMEQ0 clock to remove it. The 1 second during which the strobe is held low is sufficient to ensure that the tape has passed clear leader on the right end.

If the tape is already rewound to clear leader on the left end, another rewind

no effect on the tape
the 1-second disable
enever the oneshot
rator is disabled for
e no timing is being
will cause the RDC
hat period of time;
e used for any other
a tape which is not
es not cause the
le to fire; thus the
led.

Model 733 ASR, KSR,
re equipped with an
compatible with a Bell
coupler operates
d of 303 baud in the
lard dial telephone
is an originate-mode
0 Hz for MARK and
ncies of 2225 Hz for

is completed using a
the receive carrier

frequency is present at the receiver for 150 ± 50 msec, the Model 733 Data Terminal is enabled to receive data, and the transmit carrier frequency is enabled.

The Acoustic Coupler contains all circuitry needed to convert logic signals from the terminal to audio signals for transmission over telephone lines. These circuits also convert audio signals to logic signals for transmission to terminal control circuits in the terminal. In addition, the Acoustic Coupler circuits supply carrier detect signals to the terminal control circuits to signify when the received data carrier has been received. The coupler provides the timing required for communication with two data sets at the other end of the line. The Acoustic Coupler is designed to provide reliable operation over the full range of received signals, even under high noise and low signal level conditions. Operation equals or exceeds the performance of the 103-type data sets in half duplex (110 baud) mode.

All circuitry is located on a single PC card which is easily removed for repair or replacement. Adjustment is not required, and all critical factory adjustments are sealed to prevent maladjustment.

SECTION IV

BASIC EQUIPMENT PC CARDS AND FUNCTIONS

4-1 GENERAL.

The following standard-equipment PC cards are installed in the ASR and KSR models as shown in Figures 4-1 and 4-2. Schematics for the PC cards are contained in Appendix C.

4-2 KSR (KEYBOARD) UNIT.

4-2.1 POWER MODULE MOTHERBOARD. The KSR motherboard provides interconnections between all other PC cards in the KSR section. Mounted on the motherboard are the power supply filter capacitors, the 5-volt crowbar SCR, and bleeder resistors for the filter capacitors. The keyboard, printer drive assembly, bell, power module, cassette system and output connectors plug into the power module motherboard.

4-2.2 REGULATOR/AMPLIFIER PC CARD. This PC card contains the motor drivers for the head-stepping and paper advance motors and the head-lift solenoid driver. This PC card also contains the 5-volt switching regulator.

4-2.3 CONTROL REGULATOR PC CARD. This PC card contains the power-on reset circuit and the positive 12-volt and negative 12-volt regulators. It also contains the auxiliary/reference 5-volt supply, the 5-volt regulator oscillator, the 5-volt regulator driver, and the 5-volt crowbar.

4-2.4 PRINTER CODE PC CARD (ASCII AND BAUDOT). This PC card contains the keyboard interface which converts parallel data from the keyboard to serial data for the data bus. It also contains the character generator which converts 8-bit data from the data bus to 35 bits for the printhead. The Printer Code PC card also decodes printer control characters. The printhead compensation and driver circuits are on this PC card along with the contrast adjustment and overvoltage protection for the printhead. The driver circuit for the bell is also on this PC card.

4-2.5 PRINTER CONTROL. The Printer Control PC card has the circuitry to step and damp the head, backspace the head, and lift the head. It includes a column counter and decoders to decode column 80, column 72 (end-of-line bell), and column 12 (carriage return brake). This PC card also contains the carriage return and carriage return brake circuits. Signals for line feed and paper advance are generated on this board. A switch is provided to change

from single-line feed to double-line feed. The timing for the print pulse and the printer-busy signal is also generated on this PC card.

4-2.6 TERMINAL CONTROL. The Terminal Control PC card checks the status of all devices (line/local/off), accepts requests, and sets priorities. It uses the status and priorities to determine which devices receive enable signals. Terminal control generates these enables plus the eight clocks used to clock data to and from the data bus. Terminal control also generates the local-busy signal.

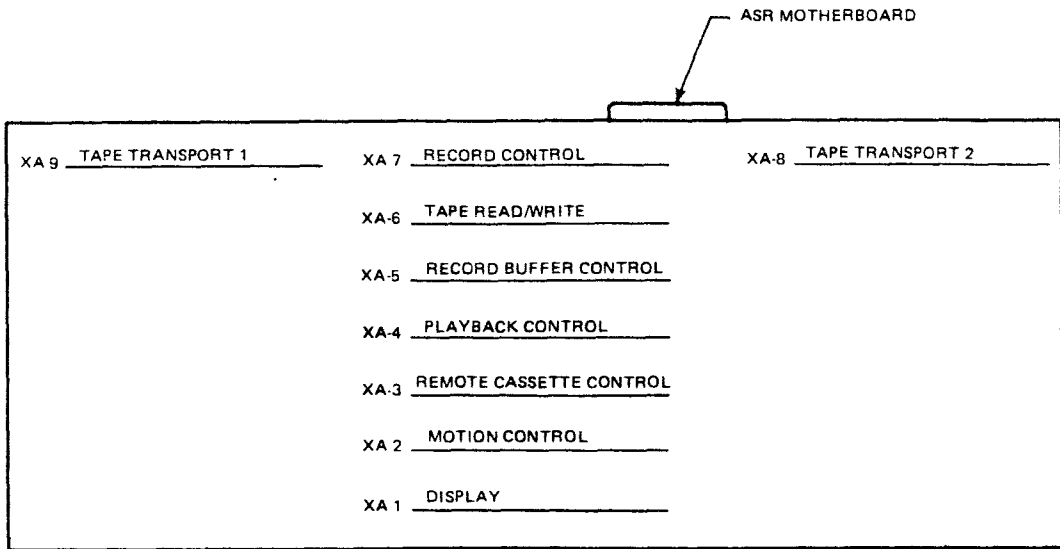
4-2.7 TRANSMIT/RECEIVE (ASCII OR BAUDOT CODE). The Transmitter/Receiver PC card contains the EIA interface circuits and the line receiver and transmitter. The ASCII receiver circuits receive data from the line at 10, 15, and 30 characters per second (CPS) or 50, 75, and 100 Baud for Baudot receivers, and clocks this data to the data bus with an enable and eight clocks from terminal control. The transmitter circuits on this PC card accept data from the data bus using an enable and eight clocks, add parity and START and STOP bits, and then clock this data to the line interface at the appropriate line speed. The SPEED switch (LO, MED, HIGH) is located on this card along with the FULL/HALF DUPLEX switch and the break circuit. The line-busy signal is generated on this card. This PC card also contains the crystal oscillator and countdown circuits which generate all master clocks used in the data terminal in addition to the receiver/transmitter clocks.

4-2.8 PRINthead INTERFACE. The Printhead Interface PC card plugs into the Printer Code PC card and the printhead plugs into this card. It consists of a 35-bit serial-to-parallel converter and 35 buffers. The card accepts serial data from the character generator and converts it to parallel data and buffers for the printhead.

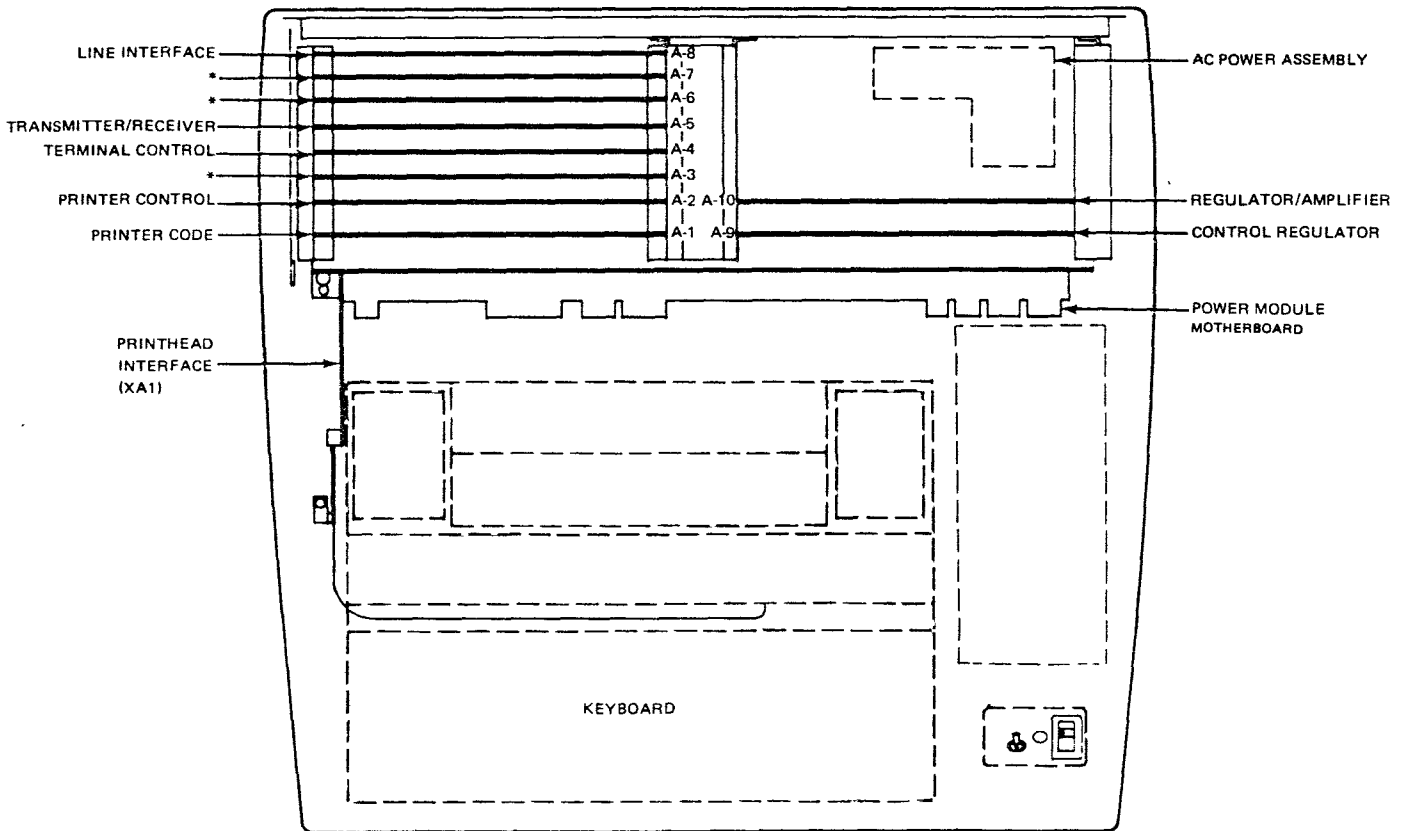
4-3 ASR MODULE (UPPER UNIT).

4-3.1 ASR MODULE MOTHERBOARD. The ASR motherboard connects all PC cards in the ASR unit with each other and with the tape transports. The motherboard is connected to the KSR motherboard through a 36-conductor cable.

4-3.2 DISPLAY PC CARD. The Display PC card contains the switches and indicators to operate the ASR. There are



ASK MODULE ASSEMBLY (UPPER) PC CARD LOCATIONS



*RESERVED FOR OPTIONAL DEVICES

KSR PC CARD LOCATIONS

FIGURE 4-1. PC CARD LOCATIONS

four 3-position switches to place the keyboard, printer, playback, and recorder on LINE, OFF, or LOCAL. Each transport has two switches: one for REWIND and one for LOAD and FF (fast forward). There is also a mode selection switch to place the transports in RECORD or PLAYBACK. The Playback Control has three momentary switches with debounce circuits for continuous START/STOP, BLOCK FORWARD/REVERSE, and CHARACTER FORWARD. The Record Control has one momentary switch for ON/OFF, one momentary switch with debounce circuits for PRINT buffer/ERASE and one two-position switch for CONT/LINE format. The display card also has LED'S and drivers to indicate the following conditions for each cassette: indicators for mode (PLAYBACK/RECORD), READY, and END of tape. The Playback control has indicators for playback ON and playback ERROR. The Record Control has an 8-bit character display and a record-ON indicator.

4-3.3 MOTION CONTROL. The Motion Control PC card accepts inputs from the switches on the Display PC card and from the transport sensors (EOT, BOT, cassette in place, door closed, write tab, etc.) and generates signals to indicate record READY, Playback READY, recorder on-LINE, and playback on-LINE. This card also generates forward, reverse, and fast signals for the transports and the load signal for the gap counter. Circuits which identify and remember which end of the tape is which are also on this PC card.

4-3.4 REMOTE CASSETTE CONTROL. This PC card has the gap counters and mode control for both cassettes. The block reverse function of playback control is located on this PC card. The playback timers (TR3/4T, TR5/4T, and TR21/4T) are located on this PC card along with the tape-erase circuits. This card also contains the decoding for remote control of the cassettes. Four code bits and a strobe are decoded into the following 15 different functions:

1. Playback on
2. Playback off
3. Record on
4. Record off
5. Rewind cassette-1
6. Rewind cassette-2
7. Load/fast forward cassette-1

8. Load/fast forward cassette-2
9. Block forward
10. Block reverse
11. Character forward
12. Cassette-1 record
13. Cassette-2 record
14. Cassette-1 stop
15. Cassette-2 stop

4-3.5 PLAYBACK CONTROL. The Playback Control PC card contains the playback control (continuous, block forward, and character forward) and tape read controller circuits. The playback buffers with their address counters are also on this board in addition to the character counter which is used for playback control and the tape read control and stop-on-read-error circuits.

4-3.6 RECORD BUFFER CONTROL. This PC card contains the 1024-bit record buffer with the punch address counter, tape write address counter, and the address select gates. The punch address register, which is used in the edit function, is on this PC card along with the memory timing circuits and the reference clocks (TRFCLKA and TRFCLKB) for the transports. Also on this card are the serial-to-parallel-to-serial registers which accept data from the line, decode and add the carriage return and end-of-block bit, and convert back to serial for the memory. The character display register also is located on this PC card.

4-3.7 TAPE READ/WRITE. The Tape Read/Write PC card contains the tape read circuit which converts phase-encoded (PE) data from the transport into binary data and the tape write circuit which converts binary data from the write data register into PE data to go to the transport. It also contains the tape write controller which formats the data as follows: preamble, 86 data characters or nulls, two block check characters (nulls), and a postamble. The block character counter and the block counter are also located on this card.

4-3.8 RECORD CONTROL. The Record Control PC card contains the flipflops to synchronize the signals from the record switches (PRINT, ERASE, record ON, and manual STOP) and the state counters for the recorder. The punch character counter and character backspace counter with decoding for count = 0 and count = 86 are included on this card along with the punch counter buffer register.

SECTION V

MAINTENANCE

5-1 PREVENTIVE MAINTENANCE.

Model 732/733 ASR/KSR data terminals are designed and built to provide long term trouble-free operation under rigorous operating conditions. To ensure that the highest performance levels are maintained, the following preventive maintenance procedures should be performed at regular intervals. These consist primarily of keeping the thermal printer mechanism and cassette transports clean and free of foreign objects.

5-1.1 PRINTHEAD CLEANING. To ensure that the thermal printer continues to provide acceptable print quality, the printhead periodically should be cleaned as follows:

- a. Lift the terminal cover and raise the window.
- b. Remove the thermal paper from the platen.
- c. On a sheet of good quality bond paper, wet a 2-inch wide strip with denatured alcohol (available from Texas Instruments in pint containers as Part No. 230007).
- d. Quickly insert the bond paper into the terminal in the same manner as thermal paper.
- e. Type five lines on the alcohol-wetted strip of the bond paper. Use the REPEAT key to accelerate the process.
- f. Advance the bond paper to a dry area and type two more lines.

NOTE

The printer will not print a visible image on the bond paper.

- g. Remove the bond paper and reload the thermal paper.

The printhead should be cleaned each time a new roll of paper is loaded into the printer or more often if the printed images start to fade as a result of residue buildup on the printhead.

5-1.2 PAPER DRIVE ROLLER CLEANING. To maintain uniform line spacing the paper drive roller must be kept clean. Use the following procedure.

- a. Switch off power to the data terminal.
- b. Remove paper from around the drive roller. Leave the window up.
- c. Move the printhead to the far right side of the mechanism.
- d. Wipe the left half of the paper drive roller with a soft rag or paper towel moistened with denatured alcohol. Rotate the drive roller manually to ensure that the entire roller is cleaned.
- e. Slide the printhead to the far left and clean the right half of the drive roller.
- f. Load the paper roll back around the drive roller, lower the window, and switch on power.

This procedure should be repeated every 3 months or whenever line spacing becomes uneven or too close.

5-1.3 PRINTHEAD DRIVE MECHANISM CLEANING. To ensure continued smooth, quiet operation of the printer mechanism, the printhead carriage rod and head lift bar must be kept clean. A dirty carriage can cause increased audible noise and can reduce the lifetime of the printer mechanism. Clean the carriage rod and head lift bar as follows.

- a. Switch off power to the terminal and remove the roll of paper.
- b. Clean the printhead carriage rod and head lift bar with a soft rag to remove paper residue (see Figure 5-1.1).
- c. Carefully apply light grade machine oil (10W) on the carriage rod and light grade multipurpose grease (Shell Darina) on the top

and bottom edges of the head lift bar.

d. Manually run the carriage back and forth several times.

e. Reload the paper and switch on power.

This cleaning procedure should be performed every 3 months or whenever the carriage rod and head lift bar appear dirty.

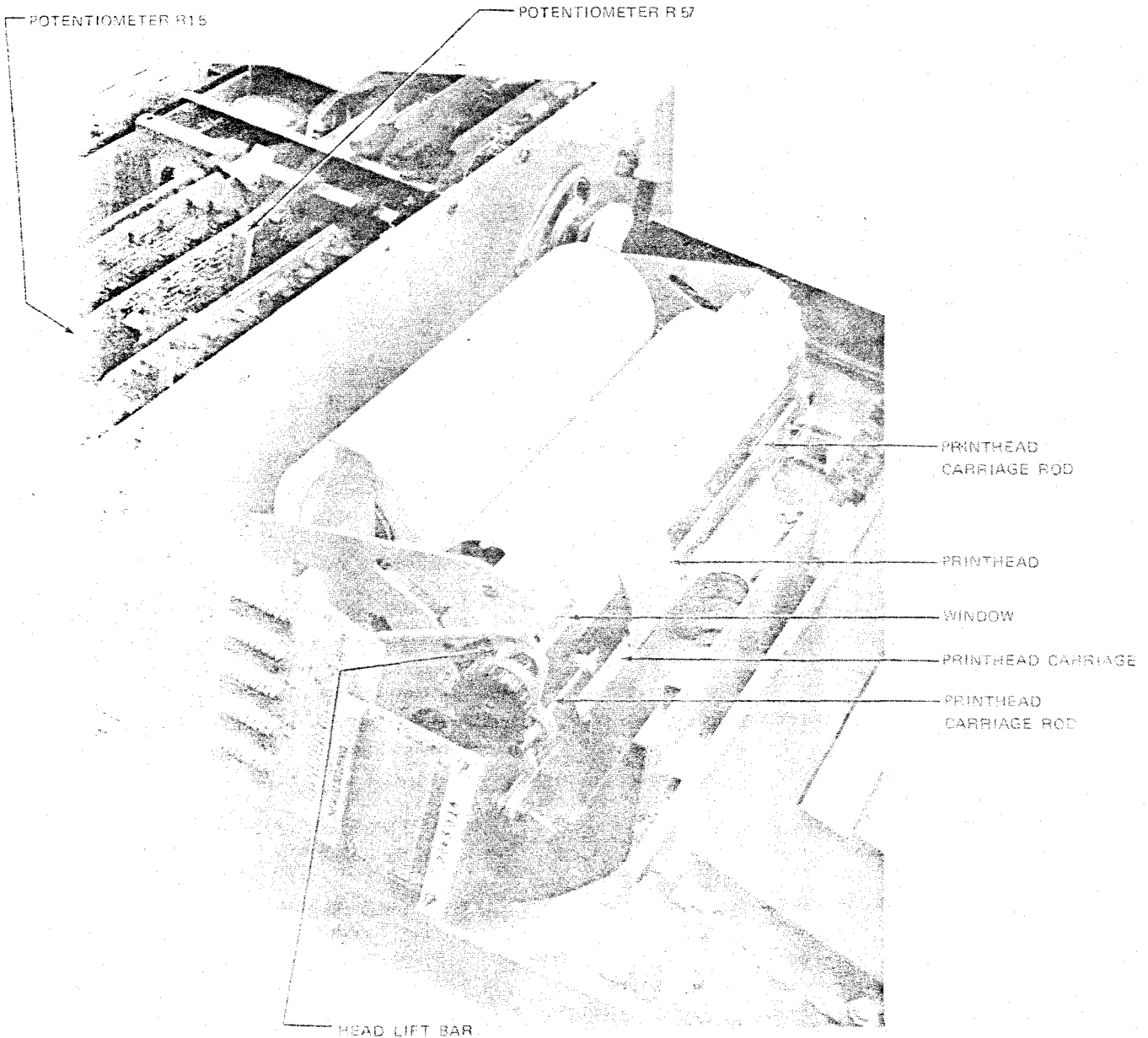


FIGURE 5-1.1. PRINTHEAD DRIVE MECHANISM CLEANING

5-1.4 CASSETTE TRANSPORT CLEANING. Carefully follow the tape manufacturers' recommendations for proper handling and storage of magnetic tape used with the ASR. In addition, clean the tape read/write heads, capstans, pinch rollers, and tape guides at regular intervals. To enhance cassette system data reliability (minimize data error rate), the following cleaning procedures should be completed once each day, or after 8 hours' operation.

- a. Switch OFF data terminal power and remove the tape cassettes from the transports.
- b. Lift the terminal cover to its stops and open the cassette transport doors.
- c. Use clean Q-tip® type cotton swabs saturated with denatured alcohol (available from Texas Instruments in pint containers, Part No. 230007) to clean the pinch rollers, capstans, tape guides, and read/write heads shown in Figure 5-1.2.
 - (1) Swab the pinch rollers across the rolling surface a section at a time; then rotate the roller with the swab and clean another section. Discard the Q-tip when it becomes discolored and resume cleaning with a new Q-tip. Continue swabbing both pinch rollers in both transports until no discoloration appears on the Q-tip.
 - (2) Clean the tape guides by inserting the alcohol-saturated swab into each side of the tape guides. Change the Q-tips until no discoloration appears.
 - (3) Swab the read/write heads using a back-and-forth motion across the heads. Change the Q-tips until no discoloration appears.
 - (4) Lower the terminal cover and swab the capstans (located directly below the pinch rollers). Clean the length of the capstans, changing Q-tips until no discoloration appears.

5-2 TROUBLESHOOTING.

Troubleshooting the data terminal is facilitated by use of Tables 5-1 and 5-2, which will aid in localizing a failure to a particular card or assembly. Table 5-1 lists failures common to all data terminal models, and Table 5-2 lists failures which may occur only in the ASR models. Where more

than one possible cause is listed for a particular problem, the PC card or subassembly is listed in descending order of probable cause. The omission of any PC card or subassembly as a cause for a specific problem does not eliminate that area, but the possibility of a failure is considered remote on the basis of experience.

5-3 ADJUSTMENTS.

The 732/733 ASR/KSR data terminals have only two field adjustments in normal use: the print contrast control and the modem level control (only in units equipped with the optional internal data set). All other adjustments are completed at the factory and should not be changed unless replacement of a component or subassembly makes readjustment necessary.

5-3.1 PRINT CONTRAST. To adjust print image contrast raise the hinged terminal cover and locate Printer Code PC card potentiometer R36. This potentiometer is accessible through a clearance hole in the Power Module card cage cover. To darken the images slowly turn the adjustment screw clockwise while typing characters from the keyboard until the desired contrast is achieved. To lighten the print image turn the adjustment screw counterclockwise.

CAUTION

- 1) DO NOT turn the adjustment screw more than one-quarter turn clockwise without checking contrast by printing a character. Contrast settings which cause scorching or sticking of the paper can result in permanent damage to the printhead.
- 2) If a new printhead is installed, turn the adjustment screw fully counterclockwise before reapplying system power. Then slowly turn the screw clockwise while typing until the desired contrast is obtained.

5-3.2 MODEM LEVEL ADJUSTMENT. Terminals which incorporate the optional internal data set (modem) must have the modem output adjusted when the terminal is installed. The adjustment also should be rechecked periodically.

5-3.2.1 Switched Telephone Network. Connection to the switched telephone network ordinarily is made by means of a data coupler, a Bell Direct Access Arrangement, or similar device provided by the local telephone company. The

telephone company dictates the maximum permissible power level of the combined received and transmitted data signals present at the terminals of the coupling device. This level is usually expressed in dBm (0 dBm = 1 milliwatt dissipated in a 600-ohm load) and is stamped on the face of the coupler.

- a. With power off connect the terminal to the data coupler by means of the data set cable. If the data coupler is not equipped with a power level meter, connect an ac vacuum tube voltmeter to the coupler terminals.
- b. Call another operating terminal within the system and arrange to receive a data or steady

MARK signal. While receiving this signal observe the VTVM; the indication should be several dBm below the allowable limit stamped on the coupler.

- c. Apply power to the terminal and again observe the meter reading. Adjust potentiometer R18 on the Modem PC card (slot A-8) until the meter reading is 1.5 dBm below the allowable maximum.



The adjustment screws of all modem

TABLE 5-1. FAILURE ANALYSIS CHART, ASR AND KSR MODELS

Symptom	Power Assembly	Drive Assembly	Keyboard	Reg/Amp	Control/Regulator	Code Card	Printer Control	Terminal Control	XMT/RCV	Line Interface	Answer-Back Memory	Printhead Interface	Printhead
Terminal Completely Inoperative	1		3	2				4					
Printhead Does Not Return When Power Applied	1	4	3	2		5							
Printhead Returns To Wrong Column		1	2			3							
Paper Advance Inoperative		3	4	2		1							
Will Not Print Although Head Steps					1						2	3	
Printhead Oscillates		2		3		1							
Printhead Steps Erratically		2		3		1							
Printhead Does Not Lift On Paper Advance		1		2		3							
Keyboard Inoperative Except Paper Advance			1		2		3						
Specific Keys Will Not Print			1		2								
Serial Data Not Transmitted							3	2	1				
Serial Data Not Received							3	2	1				
HERE IS Key Inoperative			1							2			
Carriage Return Too Slow		1				2							
Does Not Print All Elements		3			4						2	1	
Printhead Does Not Step		2		1		4	3						

NOTE: Numbers within boxes indicate order of failure probability.

Symptom	Cleaning Areas								Remarks	
	Tape Transport	Display Card	Motion Control	Remote Cassette Control	Playback Control	Tape Read/Write	Record Buffer Control	Record Control		
Tape Will Not Rewind	3		2						1	If In Record Mode Check Write Tabs Be Sure Tape Head, Capstans and Pinch Rollers are Clean
Tape Will Not Load	2		3			4			1	
Cannot Read Tape	2				4	3			1	
No Character Display		2					1			
RECORD ON Lamp Goes Out			1							
Will Not Write Tape	2			5		1	3	4		
Excessive Errors While Reading	1				3		4		2	
Will Not Sense BOT	2		3						1	
Will Not Block Reverse	1			2						
Reads Wrong Data From Good Tape					1		2			
Will Not Write 1st Character of Block							1			
Will Not Write Tape on CR							1			
Will Not Print Buffer							2	1		
Will Not Erase Tape Properly	2			1		3				

NOTE: Numbers within boxes indicate order of failure probability.

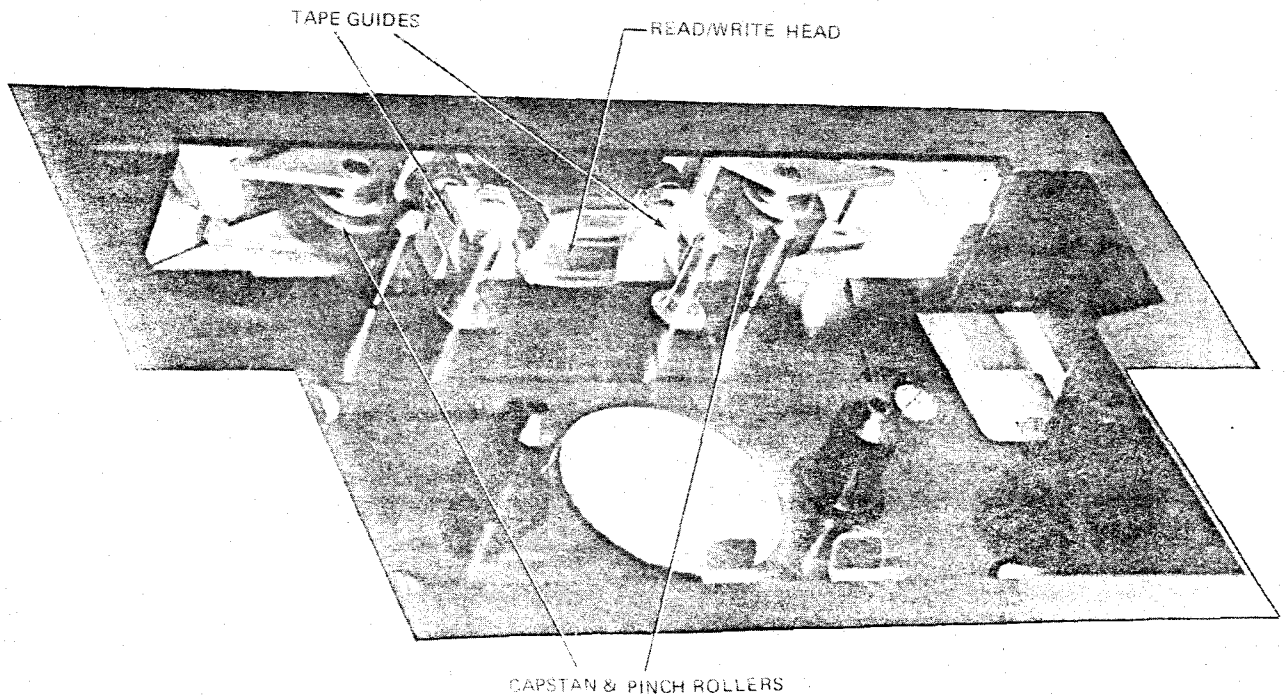


FIGURE 5-1.2. TAPE CASSETTE TRANSPORT CLEANING AREAS

potentiometers, except R18, have been sealed at the factory. Do not readjust any potentiometers except R18.

5-3.2.2 Private Wire Systems. Transmitted data signal levels in private wire communications systems must be established by the systems' engineers. Once this level has been determined, adjust the modem level as described above for the switched telephone network. The level must be adjusted while the terminal is connected to the private wire terminator.

5-3.3 PRINTER SUBSYSTEM ADJUSTMENTS. Under normal operating conditions the closed loop control circuitry of the printer subsystem will compensate for friction changes caused by wear, temperature variations, and component aging. Field adjustments should not be required unless a critical component or subassembly is replaced. If printing performance becomes unsatisfactory, do not attempt adjustments until the cause is fully understood. Be sure that the drive assembly is cleaned and lubricated according to the preventive maintenance instructions. Also, check for excessively worn parts such as a frayed drive cable or loose carriage body before adjusting.

Special test equipment is used at the factory to optimize adjustments so that the printer will perform within specified ranges of temperature, humidity, and power line voltage. The field adjustment procedures listed below should return the printer to operation after replacement of a critical subassembly. The field adjustments may not be optimum, however, and readjustments may be required if operating conditions are changed radically. Field adjustments should always be made under conditions which duplicate as closely as possible the intended operating environment of the terminal.

5-3.3.1 Head Lift Adjustment.

- a. Switch off power and raise the terminal cover.
- b. Cut or tear the printing paper so that a 6-inch strip remains in the printer: remove the paper roll.
- c. Remove the drive belt from the paper advance motor.
- d. Apply power and depress the PAPER ADV key to raise the printhead. With a feeler gauge, carefully measure the clearance between head and platen (roller). If not 0.025 (± 0.010) inch,

adjust the solenoid stroke by turning the knurled knob on the bottom of the solenoid (looking down – CW to increase, CCW to decrease). To prevent the solenoid plunger from rotating, support the black retainer into which the solenoid plunger screws with your other hand or a 3/8 inch open-end wrench.

- e. With the stroke adjusted and power off, measure the printhead force against the platen, using a force gage calibrated from 0 to 32 ounces. (Hunter T-2P-TC or equivalent). The head force should be 12 (± 1) ounces; if not, replace the spring adjacent to the head lift solenoid.

5-3.3.2 Holding Current Adjustment.

- a. Switch off power.
- b. Use a Hunter force gage (T-2P-TC or equivalent) to pull the printhead smoothly across the paper (with head down) from column 1 to column 80. Maximum friction force should not exceed 11 ounces. Minimum and maximum force measurements should not vary more than 3 ounces. If these conditions are not met, check for dirt, improper lubrication, and worn or damaged parts.
- c. Switch on power and step the printhead to column 40. Measure the force required to pull the head to column 41; if not 18 (± 1) ounces, remove the card cage cover and adjust Printer Control PC card (slot A-2) potentiometer R57 (clockwise to increase, counterclockwise to decrease holding force).
- d. Recheck the holding force each time R57 is adjusted 1/4 turn until the force is 18 (± 1) ounces.

5-3.3.3 Forward Stepping Adjustment.

- a. Depress a printable character key, such as L. The printhead should print the character and step to the right one column.
- b. If the head does not step, locate the damping sensor adjustment screw on the rear of the head stepping motor assembly [The damping sensor is on the side of the motor, opposite the

keyboard]. Turn the adjustment screw fully counterclockwise, then 1/2 turn clockwise.

- c. Again depress the L key and observe the printhead. Continue adjusting the screw 1/2 turn clockwise and printing a character until the head consistently steps to the right.
- d. Next, depress the REPEAT and L keys simultaneously and observe the printhead. Adjust the damping sensor screw to the position which results in best defined image (minimum dot smearing) and minimum acoustic noise.

5-3.3.4 Backspace Current Adjustment.

- a. Depress the CTRL (control) and H keys simultaneously. The printhead should step one column to the left. If it does not, turn Printer Control PC card potentiometer R15 fully counterclockwise, then one turn clockwise.
- b. Again depress the CTRL and H keys. Repeat this procedure, adjusting R15 one turn at a time until the printhead steps to the left.
- c. Next, depress the REPEAT, CTRL and H keys simultaneously. The printhead should step smoothly to the left until the REPEAT key is released. If not continue adjusting R15 1/4 turn at a time until smooth repeat backspace performance is observed.
- d. While performing the repeat backspace function, depress the H key, but not the CTRL key. The first letter H printed should not be smeared.
- e. Continue fine adjustment of R15 until optimum performance is achieved.

5-3.3.5 Carriage Return Adjustment.

- a. Connect the Printer Control PC card (slot A-2) to a PC card extender. Connect an oscilloscope to trigger from Z23-1 (981313) or Z11-1 (*959131), the positive-going TTL level shift and observe Z14-6 (981313) or Z30-1 (*959131), the negative-going TTL level shift.
- b. Step the printhead to column 81 (right margin); depress the RETURN (carriage return) key and

observe the oscilloscope. The delay to the fall of Z14-6 (981313) or Z30-1 (*959131), column 12, should be 105 ± 10 milliseconds.

- c. If not within specifications, locate the feedback sensor adjustment screw on the rear of the head stepping motor assembly. The feedback sensor is on the side of the motor nearest the keyboard. Turn the screw counterclockwise to accelerate carriage return; turn clockwise to decelerate.
- d. Repeat step c. until the specified delay to column 12 is achieved.
- e. As a final check, observe the signal at Z2-4 (981313) or Z26-8 (*959131) the positive-going TTL level shift. The delay between carriage return from column 81 and the rise at Z2-4 (981313) or Z26-8 (*959131) should be $140 (\pm 10)$ msec. [Specified times are measured at 25°C and 115 Vac line voltage. Carriage return time will increase as line voltage and/or temperature decrease, and decrease as temperature and voltage increase.]

5-4 SUBASSEMBLY REMOVAL AND REPLACEMENT.

Many modular-design subassemblies are easily removed to facilitate repair or replacement. Figure 5-4.1 shows some of the important modules and their attach and plug-in points. Detailed procedures are described in the following paragraphs.

5-4.1 KEYBOARD. To remove the keyboard from either a KSR or ASR unit, consult Figure 5-4.1 and proceed as follows:

- a. Switch off power to the terminal.
- b. Lift the terminal cover to expose the entire keyboard.
- c. Remove all keyboard connectors along the back right edge of the keyboard.
- d. Remove the four screws which hold the keyboard to its mounting.
- e. Remove screw, nut, and washers at upper left side of keyboard to disconnect ground strap. Note carefully location of washers so they are reinstalled in the same position for proper grounding.

***This PC card is obsolete**

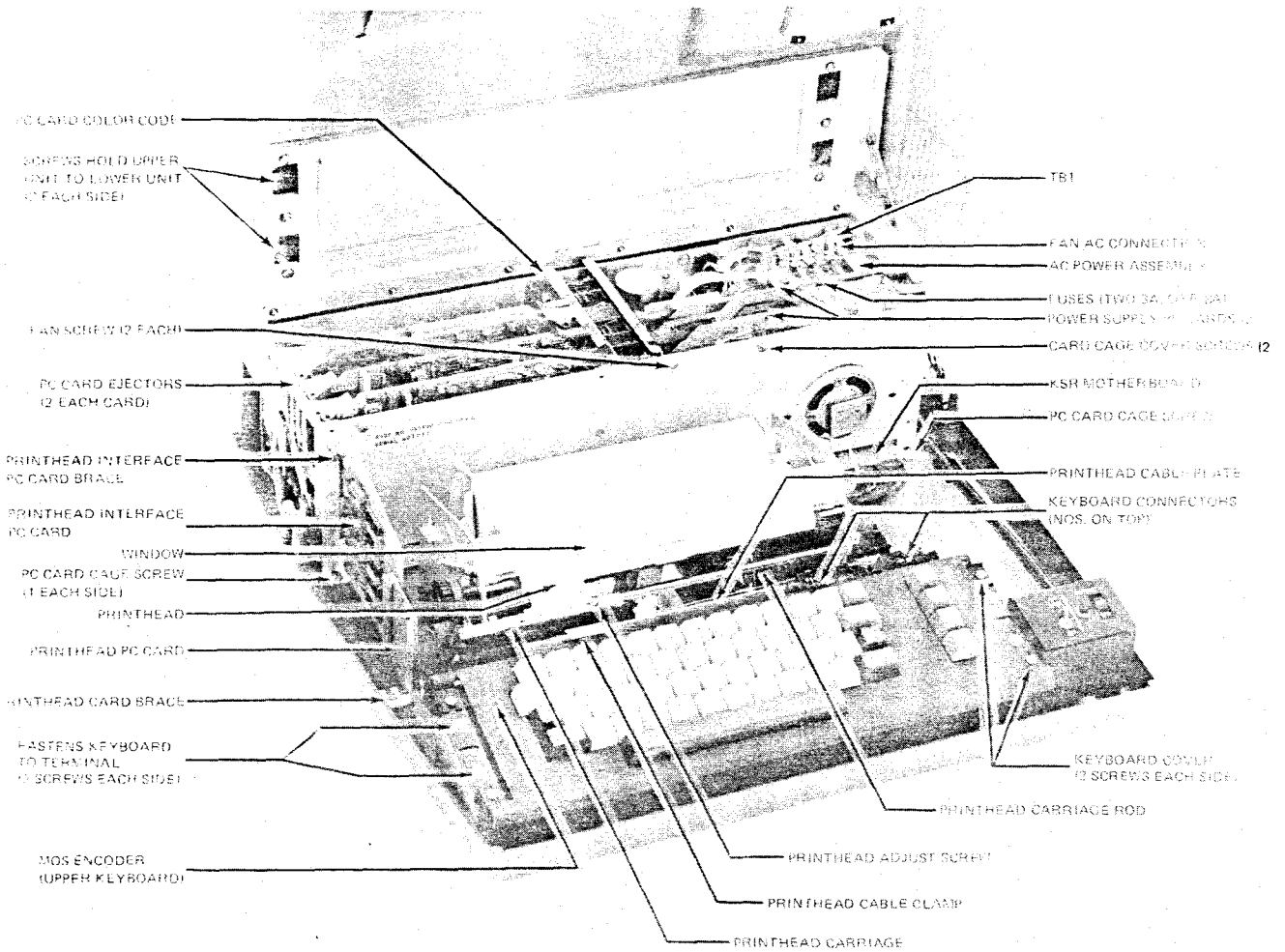


FIGURE 5-4.1. SUBASSEMBLY REMOVAL AND REPLACEMENT INFORMATION

- f. After lifting out the keyboard, place protective foam across the pins of the MOS encoder chip.



Do not touch the MOS encoder pins at anytime; damage to the MOS device may result.

To install the keyboard on either a KSR or ASR unit, proceed as follows (see Figure 5-4.1).

- a. Switch off power to the terminal and remove the old keyboard as described in steps a. through e. above.
- b. After removing the old keyboard from the terminal, remove the keyboard cover by removing the four screws and nuts which fasten the cover to the keyboard.
- c. Reinstall the cover on the new keyboard, ascertaining that all keyboard keys move freely.
- d. Remove the protective foam which may cover the MOS encoder on the new keyboard, and place the foam on the MOS encoder of the old keyboard. Be careful not to touch the MOS encoder pins at anytime on either the old or new keyboards as this may damage the MOS devices.
- e. Mount the new keyboard on its brackets using the four screws from the old keyboard.
- f. Connect the ground strap exactly as previously installed.
- g. Replace all keyboard connectors on the back right edge of the keyboard, being sure the connector is positioned with numbers on top.

5-4.2 PRINTHEAD. To remove the printhead see Figure 5-4.1 and proceed as follows.

- a. Switch off power to the terminal and raise the cover to expose the paper drive mechanism.
- b. Loosen the screw holding the printhead card brace in place and unplug the Printhead PC card from the Printhead Interface PC card.
- c. Lift the window and move the printhead to the

far right margin, noting the curvature of the printhead cable. The cable should lay flat against the printhead for a distance of at least 1/4 inch before curving to the printhead plate.

- d. Remove the clamp which holds the cable to the printhead plate.
- e. Loosen the two screws which hold the printhead to the carriage and remove the entire printhead assembly from the terminal.

Install the printhead as follows (see Figure 5-4.1).

- a. Switch off power to the terminal and remove old printhead as described in steps a. through e. above.
- b. Be sure the carriage is moved to the far right hand margin.
- c. Place the head back on the carriage, being sure slot and hole in printhead are aligned with pins on carriage, and tighten the two screws which fasten it.
- d. Clamp the cable back on the printhead cable plate; the cable should lay flat against the head for at least a distance of 1/4 inch before it starts curving toward the printhead cable plate.
- e. Plug the Printhead PC card into the Printhead Interface PC card and tighten the screw which fastens the printhead card brace to the terminal.
- f. Lower the window and apply power to the terminal.
- g. Type several characters. If full characters do not print, loosen the two printhead mounting screws, turn the printhead adjust slotted pin located on the carriage (CW to raise; CCW to lower). The pin protrudes through the lower left corner of the heat sink. Retighten mounting screws.



The full adjustment range is 1/4 turn of the slot from the horizontal either CW or CCW. Do NOT exceed.

5-4.3 DRIVE ASSEMBLY. To remove the drive assembly, see Figure 5-4.1 and proceed as follows.

- a. Switch off power to the terminal.
- b. Loosen the screw which fastens the Printhead card brace to the terminal and unplug the Printhead PC card from the Printhead Interface PC card.
- c. Remove any paper in the printer.
- d. Unplug all connectors to the drive assembly from the front edge of the KSR motherboard.
- e. Loosen the four screws which hold the drive assembly to the terminal base.
- f. Loosen and remove the grounding strap between the card cage and the mechanism.
- g. Lift out the drive mechanism, being sure the printhead cable or PC card does not catch on any other part of the terminal.

To install the drive assembly, complete the following steps.

- a. Switch off power to the terminal.
- b. Mount the drive assembly on its shock mounts in the terminal base and retighten the four screws which fasten the mechanism to the base plate.
- c. Install all connectors, as marked, along the front edge of the KSR motherboard.
- d. Install the grounding strap between the card cage and the mechanism by retightening the screw.
- e. Mount the printhead on the drive assembly as instructed in paragraph 5-4.2 above.
- f. Reinsert print paper in the terminal and apply power.

5-4.4 PRINTHEAD INTERFACE PC CARD. Remove the Printhead Interface PC card as follows (see Figure 5-4.1).

- a. Switch off power to the terminal.
- b. Loosen the screw holding the printhead card brace to the base plate and unplug the printhead PC card.
- c. Loosen the screw holding the Printhead

Interface PC card brace to the card cage and remove the Printhead Interface PC card.

Install the Printhead Interface PC card as follows (see Figure 5-4.1).

- a. Switch off power to the terminal.
- b. Plug the new Printhead Interface PC (component side out) into the connector on the Printer Code PC card through the opening in the card cage.
- c. Tighten the Printhead Interface PC card brace screw.
- d. Plug in the Printhead PC Card and tighten the screw which fastens the printhead card brace to the base plate.

5-4.5 PLUG-IN PC CARDS (LOWER UNIT). Remove lower unit PC cards as follows (see Figure 5-4.1).

- a. Switch off power to the terminal.
- b. Lift the terminal cover and loosen the card cage cover screws and remove the cover.
- c. Insert thumbs under the card ejectors (to inside of card) and lift.

Install lower unit PC cards as follows.

- a. Switch off power to the terminal.
- b. Locate the appropriate card cage slot for the card to be inserted. The right-hand card ejector (viewing the card from the component side) should match the colored dot on the card cage.
- c. Slide the card into the card cage slot and press it firmly down, applying equal pressure to both card ejectors.
- d. Replace the card cage cover, being sure the three tabs at rear of cover are properly inserted into the slots at rear of card cage, and tighten the screws holding the cover to the card cage.
- e. Close terminal cover and apply power.

5-4.6 SECONDARY FUSES. Remove and replace a secondary fuse (under the terminal cover) as follows (see Figure 5-4.1).

- a. Switch off power to the terminal and REMOVE THE LINE CORD FROM THE AC OUTLET.
- b. Lift the terminal cover and remove the card cage cover.
- c. Remove the two ac power assembly cover screws and the cover.
- d. Remove the appropriate fuse.
- e. Replace the old fuse with a fuse of the SAME SIZE AND RATING.
- f. Replace the ac power assembly cover and the card cage cover.
- g. Close the terminal cover and plug the terminal power cord into the ac outlet.

5-4.7 AC POWER ASSEMBLY. Remove the ac power assembly as follows (see Figure 5-4.2).

- a. Switch off power to the terminal and REMOVE THE TERMINAL LINE CORD FROM THE AC OUTLET.
- b. Remove the KSR fan connections at TB1-2 and TB1-5 and the ASR fan plug at the rear of the terminal. Also remove the two Power Supply PC cards in slots A9 and A10.
- c. Remove the four screws at the back of the terminal which fasten the ac power assembly to the card cage.
- d. Lift the power assembly out of the terminal with one hand and guide the line cord through the rear of the terminal base plate with the other hand.

Install the ac power assembly as follows (see Figure 5-4.2).

- a. Switch off power to the terminal and UNPLUG THE TERMINAL LINE CORD FROM THE AC OUTLET.
- b. Place the ac power assembly in place in the back right corner of the card cage, guiding the ac line cord through the hole in the rear of the base plate.

- c. Fasten the assembly to the card cage with four screws inserted through the four holes in the rear of the base plate.
- d. Reinstall the KSR fan connections at TB1-2 and TB1-5 and plug the ASR fan into the connector at the rear of the terminal.
- e. Replace the power cord in the ac outlet.

5-4.8 LOWER UNIT FAN. Remove the lower unit (KSR) fan as follows (see Figure 5-4.2).

- a. Switch off power to the terminal and REMOVE THE LINE CORD FROM THE AC OUTLET.
- b. Open the terminal cover and remove the card cage cover and the ac power assembly cover.
- c. Remove all PC cards in the lower unit.
- d. Remove the KSR fan connections from TB1-2 and TB1-5.
- e. Loosen and remove the eight screws (four in front and four in back of the card cage) which hold the fan assembly in place.
- f. Remove the fan.

Install the lower unit (KSR) fan as follows (see Figure 5-4.2).

- a. Switch off power to the terminal and UNPLUG THE LINE CORD FROM THE AC OUTLET.
- b. Mount the fan with the ac power line for the fan coming out of the bottom right rear side.
- c. Route the ac line up to the ac power assembly and connect one wire to TB1-2 and the other to TB1-5.
- d. Insert eight screws to fasten the card cage piece back to the card cage, enclosing the fan in the assembly.
- e. Replace the ac power assembly cover.
- f. Plug the PC cards into the terminal, plug the line cord into the ac outlet, and apply power to the terminal.

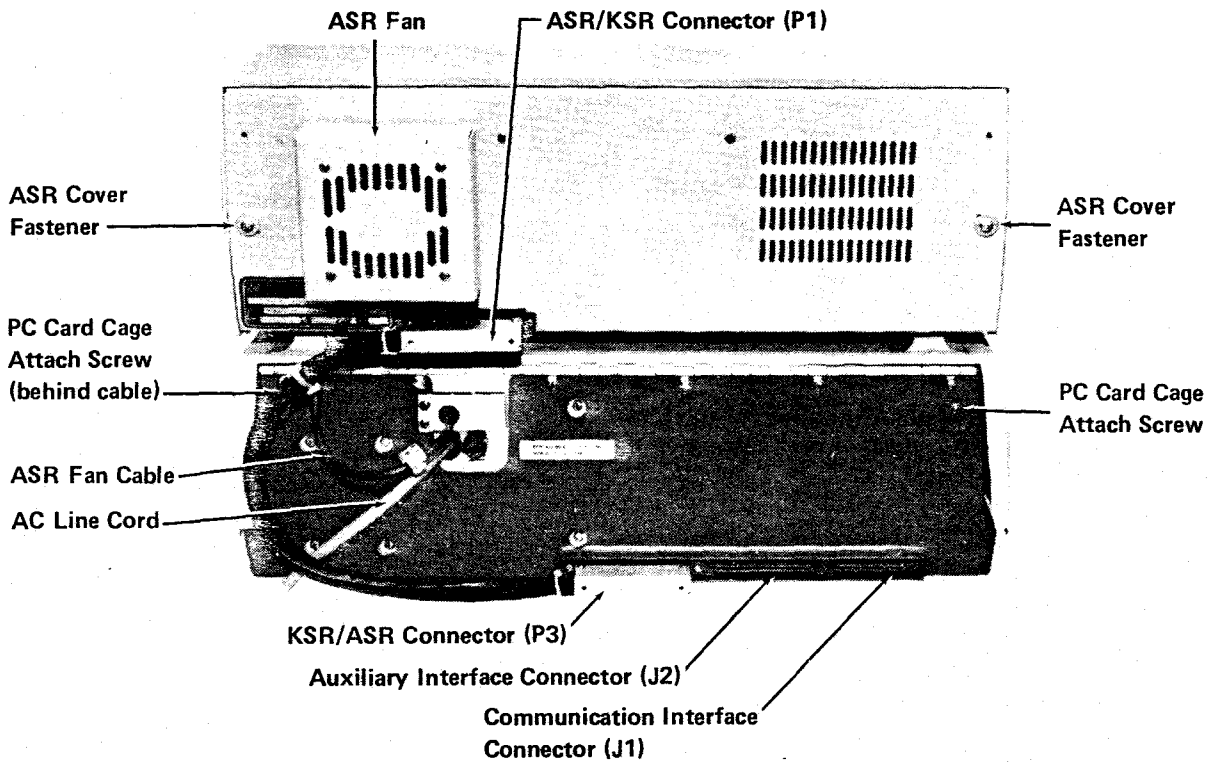


FIGURE 5-4.2. DATA TERMINAL (REAR VIEW)



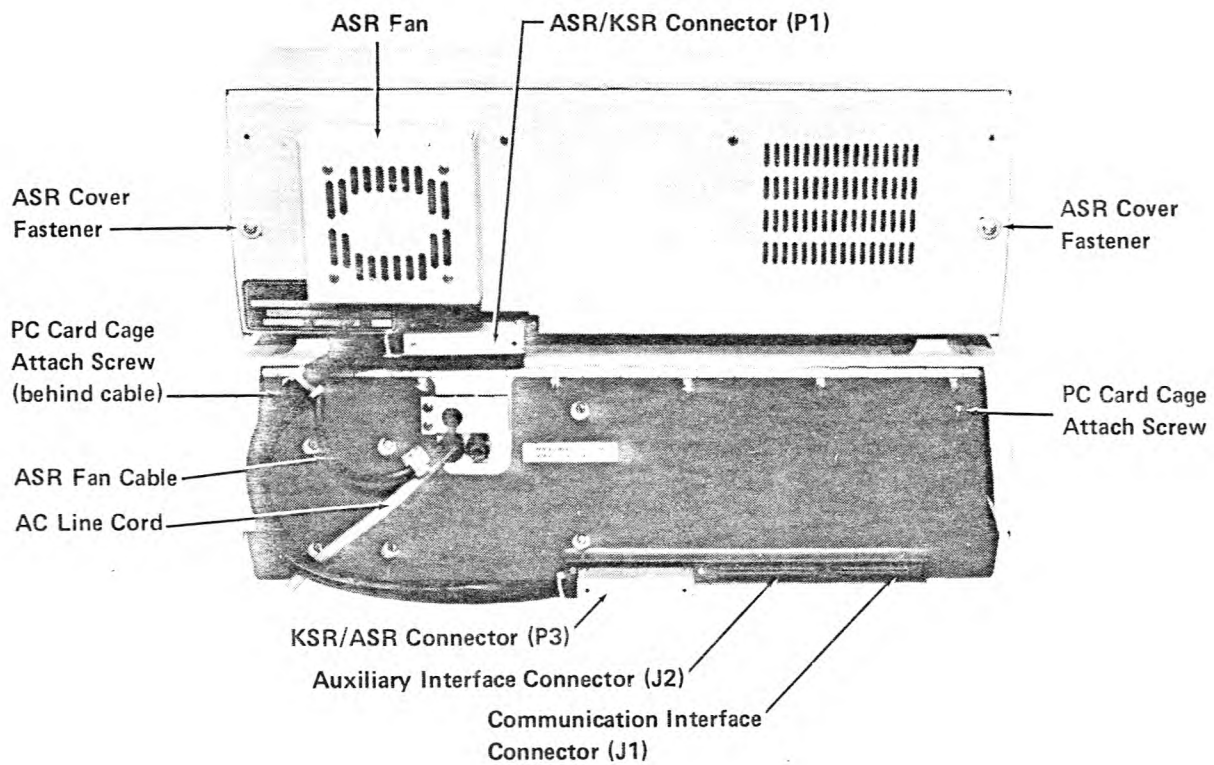


FIGURE 5-4.2. DATA TERMINAL (REAR VIEW)

- g. If the fan blades scrape the card cage, switch off terminal power.
- h. Loosen the eight card cage screws and push the two pieces which hold the fan in place away from each other as far as possible.
- i. Hold the pieces apart as far as possible while retightening the eight screws.
- j. Switch on power. If the fan blades still scrape the card cage, repeat the above procedures (h. and i.) until the fan turns freely.
- k. Replace the card cage cover and close the terminal cover.

5-4.9 POWER MODULE ASSEMBLY. Remove the power module assembly (card cage and attachments) as follows (see Figure 5-4.2).

- a. Switch off power to the terminal and REMOVE THE LINE CORD FROM THE AC OUTLET.
- b. Remove the two screws at the rear of the terminal which fasten the card cage to the base plate.
- c. Lift the terminal cover and remove the card cage cover.
- d. Remove any paper in the machine.
- e. Disconnect all connectors along the front and rear edges of the KSR motherboard and disconnect the ASR fan plug.
- f. Loosen the two screws at the front right and lower left corners of the card cage which fasten the card cage assembly to the base plate.
- g. Remove the grounding strap between the mechanism and the card cage.
- h. Slide the assembly forward as far as possible and lift the front of the card cage forward and upward.
- i. Guide the ac line cord through the hole in the rear of the terminal as the power module is lifted out.

Install the power module assembly as follows (see Figure 5-4.2).

- a. Switch off power to the terminal and REMOVE THE AC LINE CORD FROM THE OUTLET.
- b. Install the power module, being sure to guide the ac line cord through the hole in the rear of the data terminal. Guide the PC edge connectors through the connector hood at the rear of the terminal.
- c. Ascertain that no wires are trapped between the base plate and motherboard and push the assembly back as far as possible to the rear of the terminal. Tighten the two screws at the front lower right and left edges of the card cage.
- d. Install the two screws at the rear of the terminal which hold the card cage to the base plate.
- e. Install all connectors to the front and rear edges of the KSR motherboard and plug in the ASR fan.
- f. Install the PC cards and the card cage cover.
- g. Close the terminal cover and plug in the ac line cord.

5-4.10 ASR MODULE ASSEMBLY (UPPER UNIT). Remove the upper unit assembly as follows (see Figures 5-4.1 and 5-4.2).

- a. Switch off power to the data terminal.
- b. Remove the ASR ac fan connector.
- c. Remove the ASR/KSR interconnecting cable.
- d. Open the terminal cover and loosen the four screws which fasten the ASR unit to the terminal cover.
- e. Close the terminal cover and slide the ASR unit forward and lift off.

Install the ASR upper unit as follows (see Figure 5-4.1).

- a. Switch off power to the terminal.

- b. Insert four screws into the feet of the upper unit several turns.
- c. Place the upper unit onto the pedestals on the terminal cover so that the screws in the base fit into the pedestal slots in the terminal cover (front panel toward front of terminal).
- d. Slide the upper unit back as far as possible to the rear of the terminal.
- e. Open the terminal cover and tighten the four screws securely.
- f. Connect the ASR fan plug and the ASR/KSR interconnecting cable at the rear of the lower unit.

5-4.11 DISPLAY CARD ASSEMBLY. To remove the display card assembly, complete the following steps (see Figure 5-4.3).

- a. Switch off power to the terminal.
- b. Remove the ASR cover and card cage cover.
- c. Remove the two screws which hold the display panel to the card cage.
- d. Place your thumbs under the card ejectors (to inside of card) and lift up.

To install the display card assembly proceed as follows (see Figure 5-4.3).

- a. Switch off power to the terminal.
- b. Place the display card into the proper card slot, matching the card ejector color with the color dot on the card cage.
- c. Apply equal pressure downward to both card ejectors until the card fits snugly into the PC card connector on the motherboard.
- d. Replace the two screws holding the assembly to the card cage; do NOT overtighten these screws.
- e. Replace the ASR card cage cover and the ASR cover.

5-4.12 PLUG-IN PC CARDS (UPPER UNIT). Removal and replacement of all upper unit PC cards is the same as described in paragraph 5-4.5 , except the display PC card (front panel card). It is the only card which is fastened to the card cage with screws.

5-4.13 CASSETTE TRANSPORT. To remove a cassette transport, proceed as follows (see Figure 5-4.3).

- a. Switch off power to the terminal.
- b. Remove the ASR cover.
- c. Open the transport door and remove the tape cassette.
- d. Loosen the three Phillips-head screws which hold the tape transport to the ASR baseplate.
- e. Lift out the transport.

To install a transport proceed as follows (see Figure 5-4.3).

- a. Switch off power to the terminal.
- b. Insert the Transport PC card into the appropriate connector (XA-8 or XA-9).
- c. Use a Phillips-head screwdriver to tighten the three screws which fasten the transport to the ASR baseplate.
- d. Replace the ASR cover.

5-4.14 UPPER UNIT FAN. To remove the upper unit fan complete the following steps (see Figure 5-4.2).

- a. Switch off power to the terminal.
- b. Unplug the ASR fan connector at the rear of the lower unit.
- c. Remove the four screws which fasten the fan to the ASR rear cover.
- d. Remove the ASR fan from its cover.

Install the upper unit fan as follows (see Figure 5-4.2).

- a. Switch off power to the terminal.

- b. Place the fan in the fan cover and orient the ac power cord so that it exits the cover through the bottom.
- c. Insert four screws in the fan assembly, making sure each screw goes through both the cover and the fan.
- d. Insert the four screws in their proper places on the ASR baseplate at the rear of the terminal and tighten.
- e. Plug the ac fan cord into the connector at the rear of the lower unit.

5-4.15 MOTHERBOARD (UPPER UNIT). To remove the upper unit motherboard, complete the following steps (see Figure 5-4.3).

- a. Switch off power to the terminal and UNPLUG THE AC POWER CORD.
- b. Remove the ASR cover, unplug the ASR/KSR interconnecting cable at the rear of the terminal, and remove the card cage cover.
- c. Remove all PC cards and transports as described in previous steps.
- d. Remove the eight screws which fasten the motherboard to the ASR baseplate.

NOTE:

The ASR card cage is also removed by four of the screws.

- e. Remove the ASR motherboard.

To install the upper unit motherboard, complete the following steps (see Figure 5-4.3).

- a. Switch off power to the terminal and remove the old motherboard as described above.
- b. Place the new motherboard on the baseplate standoffs so that the edge connector fits into the slot in the rear of the ASR baseplate.
- c. Position the ASR card cage in the middle of the motherboard so that the card slot for the ASR front panel is toward the front of the terminal.
- d. Loosely insert the eight screws which fasten the motherboard and card cage to the ASR baseplate.
- e. Plug in the ASR/KSR connector at the rear of the ASR unit.
- f. Tighten the eight screws to securely fasten the motherboard and card cage to the ASR baseplate.
- g. Install all PC cards and transports and replace the ASR cover.

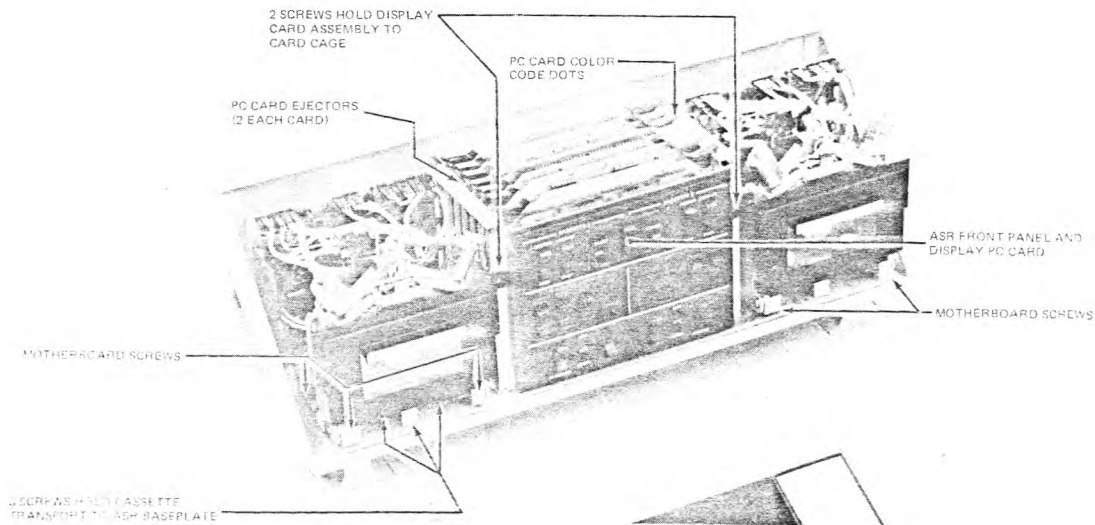


FIGURE 5-4.3. ASR UPPER UNIT REMOVAL AND REPLACEMENT (FRONT VIEW)

APPENDIX A
SIGNATURE LIST

PC Card	Page
Printer Code	A-1
Printer Control	A-2
Answer-Back Memory	A-4
Terminal Control	A-5
Transmit/Receive	A-6
Auto Device Control (option)	A-7
Remote Device Control (option)	A-8
Auto Answer Control (option)	A-12
Automatic Search Control (option)	A-10
TTY Line Interface	A-13
Modem Line Interface	A-13
Control Regulator	A-14
Regulator Amplifier	A-14
Printhead Interface	A-15
Display	A-16
Tape Motion Control	A-16
Remote Cassette Control	A-17
Playback Control	A-19
Record Buffer	A-20
Tape Read/Write	A-21
Record Control	A-22
Cassette Transport	A-23

APPENDIX A

SIGNATURE LIST

The following signal signatures are arranged alphabetically in order of PC card slot number; e.g., the Printer Code card is A1. the Printer Control card is A2. The lower unit (KSR) PC card signatures are listed first, the upper unit (ASR), next. In general, the signatures represent abbreviations of the signal function: CLK = clock, WRT = write, etc.

SLOT A-1. PRINTER CODE.

Signature	Definition	Function
BELCLK	bell clock	3.2 kHz
BELL-	bell	output to speaker
BFIGS	figures	go to figures mode
CLAMP	clamp	clamps print voltage to 0 volt
CNTRL-	control	logic ZERO for control character
CNT72	count 72	signifies column 72
COMCLR	complete clear	clears "complete" flipflop
COMPLT	complete	data transfer complete
CLK	control clock	clocks in control bit
DATA		serial data bus
DBEL	bell	control decode
DBS	backspace	control decode
DCR	carriage return	control decode
DGRND	diode ground	ground return
DHTFIG	figures	control decode
DLF	line feed	control decode
DNULLTR	letters	control decode
DVOLT	diode voltage	temperature compensation
ENDBEL-	end bell	ends column-72 bell
HDRS1	head resistor 1	fast print compensation adjust
HDRS2	head resistor 2	slow print compensation adjust
KBBIT1	keyboard bit 1	same as bit 1; most significant bit
KBBIT2	keyboard bit 2	
KBBIT3	keyboard bit 3	
KBBIT4	keyboard bit 4	
KBBIT5	keyboard bit 5	
KBBIT6	keyboard bit 6	
KBBIT7	keyboard bit 7	
KBBITP	keyboard bit P	same as bit 1; most significant bit
KBDCLR	keyboard clear	
KBDENA-	keyboard enable	data on bus from keyboard
KBDON	keyboard on	also keyboard remote off
KBDREQ-	keyboard request	
KBDSTB-	keyboard strobe	
MOSCLR	MOS clear	character generator clear
OVL-	overvoltage	clears printhead buffer
PAT0	pattern ZERO	removes printhead clear
PAT1	pattern 1	enables character generator clear

SLOT A-1. PRINTER CODE (Concluded)

PAT2	pattern 2	enables control bit clock
PAT6	pattern 6	enables 2nd part of pattern counter
PBIT1	printer bit 1	least significant bit
PBIT2	printer bit 2	
PBIT3	printer bit 3	
PBIT4	printer bit 4	
PBIT5	printer bit 5	
PBIT6	printer bit 6	
PBIT7	printer bit 7	
PBITP	printer bit P	most significant bit
PGO-	printer go	starts printer control
PGORST	printer go reset	reset PGO- flipflop
PHBFRCLR-	printhead buffer clear	
PHCHR	printhead character	35 bits; to printhead buffer card
PHCLK	printhead clock	clocks data to printhead buffer
PRINT	print	print command
PRNENA-	printer enable	data on bus to printer
PRTRST	printer reset	
PVOLT	print voltage	power to printhead
PWRRST-	power reset	
RDRCLK	reader clock	204.8 kHz
REPEAT-		keyboard repeat key
REPOFF	repeat off	REPEAT key not depressed
SCLK-	system clock	clocks data around serial bus
STROBE	strobe	signifies keyboard strobe received
ST1D	state 1D	state 1D flipflop input
ST1Q	state 1Q	state 1Q flipflop output

SLOT A-2 PRINTER CONTROL.

Signature	Definition	Function
BKSPCQ	backspace	indicates printer is backspacing
BRAKECRTN	break carriage return	controls power to head step motor (HPC) during carriage return break time.
BRAKEBSKP	break backspace	controls power to head step motor (HPC) during backspace break time.
CNTRL-	control	input from character decode; low for control characters high for printhead characters.
CNT72	count 72	high when printhead in column 72; enables Code Card bell circuit to sound end-of-line warning.
CRCLK	carriage-return clock	clock for backspacing head during carriage return (derived from feedback sensor).
CYCLRST	cycle reset	resets printer control after a regular print cycle (30 msec).
C800	clock 800	800 Hz square wave.
DBS	decode backspace	input from character decode; high for backspace. low for all other characters.
DCR	decode carriage return	input from character decode; high for carriage return, low for all other characters.
DDS	dynamic damping sensor	input to damping controller, normally 0V; as head steps left or right, a slot in tach wheel passes before sensor, producing a positive-going pulse; clamping monostable triggered on pulse trailing edge.

SLOT A-2 PRINTER CONTROL (CONTINUED)

DLF	decode line feed	input from character decode; high for line feed, low for all other characters.
ENDBEL-	end bell	negative-going pulse approximately 30 msec after PGO- is received when head at column 72; terminates end-of-line warning.
FBS	feedback sensor	input to carriage return controller; alternates from 0 to +2 V as tach wheel passes before sensor.
FSCLK	failsafe clock	clock for backspacing head during failsafe carriage return (derived from a counter, clock occurs every 20 msec).
HDCLK*	head clock	steps carriage forward 1 column
HOME		indicates carriage at left margin
HPC	head power control	analog voltage (always positive), programs current to head-stepping motor; amplitude depends on operation performed.
HPHSA	head phase A	
HPHSB	head phase B	
HPHSC	head phase C	high level on an output enables head stepping motor power driver for corresponding phase.
KBPA-	keyboard paper advance	contact closes to ground when PAPER ADV key depressed; if head not at left margin, carriage return and one line feed (single or double) are executed; if PAPER ADV released within 190 msec, no other action occurs; if PAPER ADV hold down or head at left margin, line feed performed at 30 msec intervals.
LHLS-	left-hand limit switch	approximately 0V when head at left margin (col. 1); approximately +2V at all other times.
LIFTHEAD	lift head	positive-going decaying exponential voltage, programs current to head lift solenoid during carriage return and line feed.
LNFDQ	line feed	indicates printer doing line feed
PBUSY-	printer busy	low level indicates printer control will not accept print commands; high level indicates printer is idle.
PGO-	printer go	negative-going start pulse from character decode; stores DCR, DBS, DLF, and CNTRL- inputs in synchronous input register. 12.8 kHz square wave
PNHCLK	punch clock	
PPHSA	paper phase A	
PPHSB	paper phase B	
PPHSC	paper phase C	high level on an output enables paper drive stepping motor power driver for corresponding phase.
PRINT	print	positive-going 10 msec wide pulse, enables compensation circuit to apply power to printhead.
PRINTPLS	print pulse	print pulse time (= 10 msec)
PRNLOC-	printer local	low when printer in local loop, high when on-line; provided in ASR units only.
PRNPRD-	printer period	low level indicates printer control will not accept command inputs; goes low for 1 character period (30 msec) after receipt of PGO- or an asynchronous input; remains low for 2 character periods when line feed is double space.
PWRRST-	power reset	low level for approximately 400 msec after power on; initializes registers so that paper advances with failsafe carriage return immediately after PWRRST- goes high.
RETURN		indicates printer doing carriage return

SLOT A-2 PRINTER CONTROL (CONCLUDED)

RHLS—	right-hand limit switch	approximately 0V when head at right margin (column 81); approximately +2V at all other times; is a redundant function, providing auto carriage return from right margin if column counter malfunctions.
SELECTA	select A	signal to select motor phase A after carriage returns to left margin
TPBKSPC—	tape backspace	negative-going 1.25 msec pulse when TAPE key depressed; if printhead in local loop, printhead backspaces (if not at left margin)
TPFWD—	tape forward space	negative-going 1.25 msec pulse when TAPE key depressed; if printer in local loop and printhead not at right margin, head spaces forward; space inhibited at right margin but auto carriage return is performed.

SLOT A-3. ANSWER-BACK MEMORY (ABM)

Signature	Definition	Function
ABMCLR—	answer-back clear	clears all ABM logic
ABMTRIGRST—	ABM trigger reset	disables triggering of ABM
ABMSTP	ABM stop	ends and resets ABM
AUX1ROF	auxiliary-1 remote OFF	remote off
AUX2ENAR—	auxiliary-2 enable to receive	data on bus to AUX2
AUX2ENAS—	auxiliary-2 enable to send	data on bus from AUX2
AUX2ENASQ—	auxiliary-2 enable to send Q	signifies AUX2ENAS— has been received (synched with RDRCLK)
AUX2REQ—	auxiliary request	
AUX2ROF	auxiliary-2 remote off	holds a clear on the ABM logic
C800	clock 800	800 Hz
D—	letter 'D'	decoded Baudot 'D' code
DATA—		serial data bus
ENQRY	enquiry	enquiry decode (from the line)
FIGQ—	figures	decoded Baudot figure code
FSTIME—	first time	used as remote ABM trigger line
HEREIS—	here is	from keyboard
HEREISQ	here is Q	HERE IS decode
KBDON	keyboard on	also a remote off function
PRNROF—	printer remote off	
PWRRST—	power reset.	
RDRCLK	reader clock	204.8 kHz
RECROF—	recorder remote off	stop enables to recorder
SCLK—	system clock	clocks data on serial bus
SRVENA—	serial receiver enable	data on bus from serial receiver
STOQ	state ZERO	ABM state controller wait state
ST1Q	state 1	loads memory data to output register and sends out AUX2REQ
ST2Q	state 2	wait for enable (AUX2ENAS—)
TERLINE	terminal on-line	logic low when terminal is on-line

SLOT A-4. TERMINAL CONTROL

Signature	Definition	Function
AUX1BUSY-	auxiliary-1 busy	
AUX1ENAR-	auxiliary-1 enable to receive	data on bus to AUX1
AUX1ENAS-	auxiliary-1 enable to send	data on bus is from AUX-1
AUX1LOC-	auxiliary-1 local	
AUX1REQ-	auxiliary-1 request	
AUX2ENAR-	auxiliary-2 enable to receive	enable the data on bus to AUX-2
AUX2ENAS-	auxiliary-2 enable to send	the data on the bus is from AUX-2
AUX2LOC-	auxiliary-2 local	
AUX2REQ-	auxiliary-2 request	
AX1AX2DR-	auxiliary-1 and -2 to receive D input	
BOEOCA2	BOT, EOT, cassette-2	clear leader on cassette-2
BOEOCA1	BOT, EOT, cassette-1	clear leader on cassette-1
BUFRREQ-	buffer request	for print buffer command
CL1-	clock one	clocks enable D's to enable registers
DATA-		data on serial data bus
DATLOC-	local data	data on bus is for local loop
ENABLE		enables D inputs to enable registers
FSTIME-	first time	'blinds' terminal to incoming data
FULDPX-	full duplex	
KBDENA-	keyboard enable	data on bus is from keyboard
KBDLOC-	keyboard local	keyboard is in local mode
KBDREQ-	keyboard request	keyboard requests to send data
LINBUSY-	line busy	transmitter busy
LOCBUSY	local busy	local loop busy
PAPOUT-	paper out	printing supply roll exhausted
PBUSY-	printer busy	print time (30 msec) or carriage return time (190 msec)
PNHCLK	punch clock	12.8 kHz
PRNENA-	printer enable	data on bus to printer to
PRNLOC-	printer local	printer is in local mode
PRNPRD-	printer period	30 msec per character busy timer from printer
PRNROF-	printer remote off	remotely inhibit the printer from receiving data
PWRRST-	power reset	
RCBFFL-	record buffer full	
RCVRQCL-	receiver request clear	
RDRCLK	reader clock	204.8 kHz master system clock
RDRENA-	reader enable	data on the bus is from playback
RDRLINE-	reader on-line	
RDRREQ-	reader request	reader requests to send data
RDROF-	reader remote off	remotely inhibit the reader from sending data
RECENA-	recorder enable	enable data on bus to/from recorder
RECLINE-	recorder on-line	
RECROF-	recorder remote off	remotely inhibit the record operation
RERROR	reader error	playback read error
RFEED	reader feed	playback busy
SCLK-	system clock	clocks data on serial data bus
SRVENA-	serial receiver enable	data on bus is from receiver
SRVREQ-	serial receiver request	
STAENA-	status enable	data on bus is status

SLOT A-4 TERMINAL CONTROL (CONCLUDED)

STATUSINH-	status inhibit	inhibits a status enable
TCK	terminal control clock	
TCST1	terminal control state 1	ENABLE and SCLK state
TERLINE-	terminal on-line	
XMTENA-	transmit enable	data on bus to transmitter

SLOT A-5. TRANSMIT/RECEIVE (300 & 1200 baud)
(Slot A-8 is 1200 baud transmitter)

Signature	Definition	Function
BELCLK	bell clock	3.2-kHz bell tone
BIT9	bit 9	signifies that a whole character has been received from the line
BIT9Q	bit 9Q	enables a SRVREQ to be sent
BREAK-	break	from keyboard, sends space to LINE
BUSYRST-	busy reset	resets LINBUSY
BYCLK	busy clock	6.4 kHz
CHRTIMECK-	characters time clock	signifies a character has been transmitted
CLEAR	clear	resets receiver
C800	800 Hz clock	800 Hz
DATA-		serial data bus
EIACTS	EIA clear to send	transmitter control
EIADATIN	EIA data in	EIA input data from line
EIADOT	EIA data out	EIA output data to line
EIADCD	EIA data carrier detect	receiver control
EIADSR	EIA data set ready	transmitter/receiver control
EIADTR	EIA data terminal ready	held high by terminal
EIAGRD	EIA ground	
EIARTS	EIA request to send	held high by terminal
EXTCKIN	external clock in	test input
FIFOMR-	first-in first-out memory reset	resets FIFO memory
FULDPX-	full duplex	a terminal status
HSPEED	high speed	1200 baud
INHXTM-	inhibit transmitter	holds output line to a mark
INPUTRDY	input ready	FIFO memory ready to accept a character
INTCKINH	internal clock inhibit	test output
LATCHDAT	latch data	used by receiver reset latch
LINBUSY-	line busy	transmitter busy, 300 baud; FIFO full, 1200 baud
OUTPUTRDY	output ready	signifies a character at the FIFO memory output
PARITY	parity	'parity bit' for transmit data
PBUSY-	printer busy	signifies printer busy for 30 msec per character or 190 msec per carriage return
PNHCLK	punch clock	12.8 kHz
PWRCLK	power clock	51.2 kHz to power supply switching regulators
PWRRST-	power reset	
QSIENA	shift-in enable	
QXMTRDY-	transmitter ready	holds down LINBUSY in half duplex in low-speed operation
RBIT1 -	receiver bit 1	least significant bit
RBIT2-	receiver bit 2	
RBIT3-	receiver bit 3	
RBIT4-	receiver bit 4	

SLOT A-5 TRANSMIT/RECEIVE (CONCLUDED)

RBIT5--	receiver bit 5	
RBIT6--	receiver bit 6	
RBIT7--	receiver bit 7	
RBITP--	receiver bit P	most significant bit
RCVDATA	receiver data	EIA data input converted to TTL data
RCVHDPX	receiver in half duplex	inhibits transmitter
RCVENA	receiver enable	data set is ready and data carrier is present
RDCLK	reader clock	204.8 kHz
REQENA--	request enable	enables bit-9 flipflop
RERROR	reader error	playback read error
RESET	reset	resets receiver, also signifies a character is being received
RFEED	reader feed	playback busy
RSTCHRTIMER	reset character timer	resets character bit counter
RTSDELAYENA	request to send delay enable	enables 20 msec request-to-send delay
SCLK--	system clock	clocks data on bus
SHIFTIN	shift in	enter character into FIFO input buffer
SHIFTOUT	shift out	put next character into FIFO output buffer
SRVCLK	serial receiver clock	$SRVCLK = 64 \cdot XMTCLK$
SRVDAT	serial receiver data	receiver serial data bus data
SRVENA--	serial receiver enable	data on bus from receiver
SRVLOAD--	serial receiver load	loads input data into serial data bus output register
SRVREQ--	serial receiver request	
STRBIT--	start bit	'start bit' for transmit data
TCST1	terminal control state 1	enable and SCLK state
TERLINE--	terminal on-line	
TTYDATIN	TTY data in	
TTYDATOT	TTY data out	
XMTBSY	transmitter busy	transmitter sending data to outside line
XMTENA--	transmit enable	data on bus to transmitter
XMTCLK	transmit clock	clocks data to outside line
XMTHDPX--	transmit in half duplex	'locks out' receiver
XMTINH	transmitter inhibit	'blinds' transmitter to serial data bus
XMTRCVCLK	transmit/receive clock	$XMTRCVCLK = SRVCLK \cdot 2$
XMTRST--	transmitter reset	resets transmit and receive busy indicators
10CPS	10 characters per second	signifies transmit speed of 10 CPS
32CLK	32 clock	clocks received data to input register

SLOT A-6. AUTO DEVICE CONTROL (OPTION)

Signature	Definition	Function
CDBIT1--	code bit 1	least significant code bit to Remote Cassette Control Card
CDBIT2--	code bit 2	
CDBIT3--	code bit 3	
CDBIT4--	code bit 4	
CDSTB--	code bit strobe 1	for remote cassette control
DATA--		serial data bus
DATLOC--	data local	data on bus is for local loop
DC1--		playback on
DC2--		record on
DC3--		playback off

SLOT A-6 AUTO DEVICE CONTROL (CONCLUDED)

DC4-		record off
PWRRST-	power reset	
RCDLINE-	recorder on-line	
RDRCLK	reader clock	204.8 kHz
RDLINE-	reader on-line	
SCLK-	serial clock	clocks data on serial bus
SRVENA-	serial receiver enable	data on bus from receiver
XMTENA-	transmitter enable	data on bus to transmitter

SLOT A-6 REMOTE DEVICE CONTROL (OPTION)

Signature	Definition	Function
ASCCANQ	ASC cancel Q	decode for ASC to cancel search
ASCSRCH-	ASC search	indicates ASC card has tape search in progress
AUX1DAT	auxiliary-1 data	data to serial bus from auxiliary-1
AUX1ENAS-	auxiliary-1 enable to send	data on bus is from auxiliary-1
AUX1REQ-	auxiliary-1 request	request from auxiliary-1 to terminal control to send data on serial bus
AUX1ROF-	auxiliary-1 remote off	optional line for inhibiting RDC
AUX2ROF-	auxiliary-2 remote off	logic ZERO holds ABM in reset state
BLKFWDQ	block forward Q	initiates block forward function
BLKREVQ	block reverse Q	initiates block reverse function
BOEOCA1	BOT and EOT cassette-1	cassette-1 is on clear leader
BOEOCA2	BOT and EOT cassette-2	cassette-2 is on clear leader
CANCLR-	cancel clear	clears CAN flipflop
CANDAT-	cancel data	data from CAN character register
CANENA	cancel enable	enables CAN character register
CANRSTENA	cancel reset enable	enable to reset CAN character flipflop
CAS1RCDQ	cassette-1 record Q	initiates mode switch to cassette-1 record
CAS2RCDQ	cassette-2 record Q	initiates mode switch to cassette-2 record
CCUNIT2	call control unit 2	spare line to jumper ABM-off signal to PC card slots A-7 and A-8
CCUNIT4	call control unit 4	spare line to jumper FSTIME- signal to PC card slots A-7 or A-8
CDBIT1-	code bit 1	1 of 4 parallel cassette control bits
CDSTRB-	code strobe	strobe for 4 parallel control bits
C800	clock 800 Hz	800-Hz system clock
DATA-	data	internal serial data bus
DATLOC-	data local	data on bus is local data
DC1Q	DC1Q	initiates playback-ON function
DC2Q	DC2Q	initiates record-ON function
DC3Q	DC3Q	initiates playback-OFF function
DC4Q	DC4Q	initiates record-OFF function
DC13ENA-	DC1 and DC3 enable	depends on five pencil switch settings
DC14-OFF-	DC1 through DC4 OFF	disables DC1 through DC4 functions on received data
DC14-ON-	DC1 through DC4 ON	resets DC1 through 4 OFF command
DC24-ENA-	DC2 and DC4 enable	depends on five pencil-switch settings
DLE-	data link escape	decodes first character of two-character sequence
EOT-	EOT	decodes 300-baud auto answer disconnect code
ESCQ	escape Q	indicates first character of double-character code sequence is decoded
FOOTSWITCH-	footswitch	input line for local footswitch (initiates local DC1 function)
FSTIME-	first time	"blinds" terminal to received data when at logic ZERO
FTSWD	footswitch-D	causes DC1 function to be initiated at next TIMEQ0 time

SLOT A-6 REMOTE DEVICE CONTROL (OPTION)

Signature	Definition	Function
KBDENA-	keyboard enable	data on bus from keyboard
KBDLOC-	keyboard local	
KBPA-	keyboard paper advance	from PAPER ADVance switch on keyboard
LOAD1Q	load cassette 1 Q	initiates loading of cassette 1
LOAD2Q	load cassette 2 Q	initiates loading of cassette 2
LINBUSY-	line busy	indicates to terminal control the transmitter is busy
MODL2	modem line 2	spare line to PC card slots A-7 or A-8
PBKON-	playback ON	logic ZERO indicates playback is on
PRNROF-	printer remote OFF	when logic ZERO, printer does not receive enables from terminal control
PRNOF-	printer off	printer-off decode
PRNOFF-	printer off	PRINTER LINE/OFF/LOCAL switch is in OFF position
PRNOFQ	printer off Q	causes printer to be inhibited via PRNROF- line
PRNON-	printer ON	printer-on decode
PRNRDY	printer ready	status bit indicates printer is on-line and ready
PWRRST-	power reset	resets RDC card logic during power up or after power failure
PWRRST1-	power reset 1	indicates power reset or RDC off
PWRRST2-	power reset 2	indicates power reset, RDC off, or terminal not on-line
RCVCLK	receive clock	5- μ sec pulse at time Q0 on each SRVENA- signal (signifies stable received data)
RCVEOT-	receive EOT	300-baud auto answer disconnect decode output
RDCBIT1	RDC bit 1	input data bit from data bus (least significant bit)
RDCOFF-	RDC off	manual switch on card is in OFF position (logic ZERO)
RDRCLK	reader clock	master system clock (205.8 kHz)
RDRENA-	reader enable	data on bus is from playback
RDRLINE-	reader on-line	playback is on-line and ready
RDRRDY	reader ready	indicates playback is ready
RDRROF-	reader remote off	inhibits playback from sending data to bus
RECLINE-	record on-line	recorder is on-line and ready
RERROR	reader error	playback-error detected
REW1Q	rewind cassette 1 Q	initiates rewind of cassette 1
REW2Q	rewind cassette 2 Q	initiates rewind of cassette 2
RFEED	reader feed	playback is on (busy)
RMTCAN-	remote cancel	causes remote cancel of ASC search when logic ZERO
RMTENA-	remote enable	enables received line data to ASC for remote search
SCLK-	serial clock	clocks data on serial data bus
SPARE	spare line	spare line to card slots A-7 or A-8
SRCHLN	search line	indicates a remote line search
SRCHLOC	search local	indicates a local search
SRVENA-	send receive enable	data on bus is from send receive
STADAT-	status data	data from status register
STAENA	status enable	enables status register
STAENA-	status enable	data on bus is status
STAT-	status	decode request for status character
STATUSQ	status Q	indicates request for status has been decoded

SLOT A-6 REMOTE DEVICE CONTROL (Concluded)

Signature	Definition	Function
TCST1	terminal control state-ONE	terminal control device enable time
TERLINE-	terminal on-line	from terminal ON-LINE switch, logic ZERO when the terminal is on line
TIMEQ0D	time Q0D	clears CAN flipflop
TIMEQ0	time Q0	indicates input data to RDC is stable
TIMEQ4	time Q4	time at which strobe (CDSTROB-) is sent to ASR unit
TIMEQ5	time Q5	request (AUX1REQ-) is sent to terminal control
TIMEQ6	time Q6	clears status flipflop
TTYDATIN	TTY data in	spare line to A-7 or A-8
TTYDATOT	TTY data out	spare line to A-7 or A-8
XMTENA-	transmit enable	data on bus is for transmitter
XMTINH-	transmitter inhibit	when logic ZERO inhibits data from entering the transmitter
1200BPRNLOC-	1200-baud print local	decode for 1200-baud print-local function

SLOT A-7 AUTOMATIC SEARCH CONTROL (OPTION)

Signature	Definition	Function
ASCLR	ASC clear	clears ASC functions and forces ROM control into its quasi state; this sequence automatically issues a playback-off code and strobe and forces a paper advance if the playback is not on-line.
ASCSRCH	ASC search	ROM control line, indicates ASC is in search mode.
CDMW	cassette data memory-write	pulse on the cassette data RAM, loads the data from the buffer register.
CHRDY	character ready	indicates a serial-to-parallel conversion has taken place.
CHROK	character is OK	indicates that character is ready and printable.
CONCHR	control character decode	inhibits PRNCHR.
CPRFG	compare flag	logic signal to the processor, signifies that the last match was positive; is a flipflop output.
DECSFMA	decrement search-field memory-address register	decrements the search-field RAM address register.
DELETE	decoded "delete" character	inhibits PRNCHR.
DKEYFLG	D input to KEYFLG flipflop	allows KEYFLG flipflop to set on next CHROK pulse.
ENACHRDY	enable character-ready	allows CHRDY to set on falling edge of TCST1.
ENAPLAYOFF	enable playback OFF	ROM control line, sets up the playback-off code (DC3) and sends the code strobe.
INCADR	increment the compare address register	increments the counter which points to the beginning character in the cassette data memory.
INCDRAR	increment cassette-data RAM address register	increments the contents of the cassette data RAM address register.
INCSFMA	increment search-field memory address register	increments the search field memory address register.

SLOT A-7 AUTOMATIC SEARCH CONTROL (Concluded)

Signature	Definition	Function
KENA	keyboard enable	ROM output line, gates KBDENA input to CHRDY logic.
KEYFLG	indicates that the last transaction was a data input to search-field RAM.	forces the ROM controller to search on the new search field.
MATCH		signal to logic processor that one search field and cassette data character compare.
PAA through PAE PADE	present-address bit A, bits A through E present-address bits D and E	ROM address register output bits A through E. output of the logic gate that NANDs present-address bits D and E.
PBKON	playback is on	signal to processor, indicates playback cassette is ON.
PRNCHR RENA	printable character reader enable allow	gated decoder output that passes CHROK. ROM output line, gates RDRENA input to CHRDY logic.
RMTCAN	remote cancel	signal from Remote Device Control PC card, indicates reception of remote cancel code.
RMTENA	remote enable	signal from Remote Device PC card, indicates a data reception from the line.
SBT SELA	stop bit select A	indicates the last character in the search field. bit A of a coded 2-bit field, selects to the ROM address registers: PA, J0, J1, or J2.
SFMAOF	search field-memory-address overflow	carry output of search field memory address register.
SFMAUF	search field-memory-address underflow	borrow output of search field memory address register.
SFMW	search field memory-write	pulse applied to the search field memory to load parallel data from the buffer register.
SINCHFRG	single-character flag	output of a flag flipflop, signifies that search field will be only one character wide.
XCFACDRA	transfers compare field address to the cassette data memory address	transfers the contents of the compare field address counter to the cassette data ROM address register.
XSFASSFA	transfer search field address-counter (actually N) to the search field address-counter store register.	causes a temporary register to store the length of the search field address field (N).
XSSFASF	transfer stored search field-address to search-field register	transfers the contents of the temporary search field storage register to the working search field RAM address register.
ZCADR ZCDRAR	zero compare field address register zero cassette-data RAM address register	clears contents of compare field address register. clears the contents of the cassette data RAM address register.
ZCHRDY ZSFMA	zero character ready zero search-field memory address	clears CHRDY flipflop. clears search field RAM address.

SLOT A-7 OR A-8 AUTO ANSWER CONTROL, 300 BAUD (OPTION)

Signature	Definition	Function
AA103ARST	auto answer 103 reset	resets Auto Answer PC card logic
ABMTRIG-	answer-back memory trigger	remote trigger to ABM PC card
AUX2ROF-	auxiliary-2 remote OFF	When low, a clear is held on the ABM card (if installed); this signal to the ABM must be jumpered through the RDC card to be operational. CCUNIT2 is a spare MB run used to transmit AUX2ROF signal from slot A6 to slots A7 and A8
CCT	coupler cut-through	signals that the input lines to the DAA have been connected to the communication line
C800	clock 800	800-Hz clock
C80MS	clock 80 msec	80-msec clock for timer
DSRDRCLK	data-set reader clock	buffered RDRCLK
EIADATIN	EIA data in	EIA received data from the communication line
EIADCD	EIA data-carrier detect	carrier being detected either by Bell 103 Data Set or by internal modem
EIADSR	EIA data-set ready	signals that data set is ready for operation (from Bell 103 Data Set)
EIAGR	EIA ground	
FSTIME-	first time	when low, all receiving devices in the terminal are blinded to received data; this signal must be jumpered through the RDC card to be operational. CCUNIT4 is a spare run used to transmit FSTIME- signal from slot A6 to slots A7 and A8
LINBUSY-	line busy	signals terminal control that transmitter is busy or receiver is busy (HALF-DUPLEX only)
LINRDY-	line ready	line to option display panel lamp: illuminates when communication line is ready for data transfer
LINDATAQ	line data Q	TTL-level received data from the communication line, synched with RDRCLK
NXTST0	next state 0	call to be disconnected on next RDRCLK
OH/DTR	off hook/data terminal ready	goes high (> 3 V) to answer an incoming call; goes low (< -3 V) to disconnect a call
PWRRST-	power reset	master terminal-reset upon power-on or power failure
RCVEOT	receive EOT	from RDC card; signifies EOT characters received from the line
RDRCLK	reader clock	204.8 kHz
RI	ring indicator	signals incoming call for Bell 103 Data Set or CBS DAA
RNGIND-	ring-indicator lamp	line to option display panel lamp: follows incoming ring indicator (RI) until call is answered; remains on after call is answered until line is ready for communication
ST0Q	state-zero Q	wait state, no call in progress
ST1Q	state-1 Q	call answered and data-set-ready indication received: wait for carrier-detect indication and then trigger ABM
ST2Q	state-2 Q	carrier-detect indication received, wait for ABM-delay time
ST3Q	state-3 Q	ABM delay time completed, bring down the line-busy indication (send ABM data) and wait for a disconnect condition (carrier loss, long space, receive EOT)
TD10.24SEC	time delay 10.24 seconds	10.24-second delay from timer, used for wrong number disconnect
TD1.28SEC	time delay 1.28 seconds	1.28-second delay from timer, used for long space disconnect

SLOT A-7 OR A-8 AUTO ANSWER CONTROL (CONCLUDED)

Signature	Definition	Function
TD80MS TERLINE-	time delay 80 milliseconds terminal on-line	80-msec delay from timer, used for long space disconnect from terminal ON-LINE switch, line is low when terminal is on-line
TERMRDY-	terminal ready	line to option display panel lamp; illuminates when terminal is on-line and thus ready to answer a call
TIMERRST	timer reset	reset delay timer
TTLDCD	TTL data-carrier detect	TTL-level data carrier detect indication; synched with RDRCLK
TTLDSR	TTL data-set ready	TTL-level data set ready indication; synched with RDRCLK
TTLDTR	TTL data terminal ready	TTL-level data terminal ready output; governs connect/disconnect of DAA or 103 systems communication lines
TTLRNG	TTL ring	TTL-level ring indicator; synched with RDRCLK

SLOT A-8. TTY LINE INTERFACE

Signature	Definition	Function
EIACTS	EIA clear to send	tied to + 5 volts
EIADCD	EIA data carrier detect	tied to + 5 volts
EIADSR	EIA data set ready	tied to + 5 volts
TTYDATIN	Teletype interface data in	TTL data from Teletype interface to serial receiver
TTYDATOT	Teletype interface data out	TTL data from serial transmitter to TTY output circuit
TTYL1	Teletype interface line 1	receiver line for neutral or polar
TTYL2	Teletype interface line 2	receiver common for neutral receiver and transmit common for polar
TTYL3	Teletype interface line 3	transmitter line for neutral or polar
TTYL4	Teletype interface line 4	transmitter line for neutral or polar

SLOT A-8. MODEM LINE INTERFACE

Signature	Definition	Function
EIACTS	EIA clear to send	tied to + 12 volts by modem
EIADATIN	EIA data in	EIA (± 12 V) data sent from modem to serial receiver
EIADATOT	EIA data out	EIA (± 12 V) data sent from serial transmitter to modem
EIADCD	EIA data carrier detect	goes high (+12 V) 150 msec after modem senses in-band signal; goes low (-12 V) 100 msec after modem loses in-band signal
EIADSR	EIA data set ready	tied to + 12 volts by modem
MODL1	modem line 1	communication line
MODL2	modem line 2	communication line

SLOT A-9. CONTROL REGULATOR

Signature	Definition	Function
NEG12V	negative 12 volts	-12 volt supply
NEG18V	negative 18 volts	-18 Vdc from ac power assembly
POS18V	positive 18 volts	+18 Vdc from ac power assembly
POS5VCROWBAR	5 volt crowbar	shuts down regulator if + 5 voltage is too high
POS5VOL	5-volt overload	current limit for 5 volts
POS5VREF/AUX	positive 5 volts reference/auxiliary	reference/auxiliary + 5 voltage supply to power + 5 volt regulator
POS5VREGDR	5-volt regulator drive	switches on + 5 volt regulator
POS5VREGNA	5-volt regulator enable	shuts down + 5 volt regulator if clocks are lost
POS5VSENSE	positive 5-volt sense	tied to + 5 volt supply
POS12V	positive 12 volts	+ 12 volt supply
POS33V	positive 33 volts	33 Vdc from ac power assembly
POS33VUNFIL	positive 33 volts unfiltered	33 volts rectified but unfiltered from ac power assembly
PWRCLK	power clock	51.2 kHz reference clock from transmit/receive
PWRRST-	power reset	goes low for approx. 600 msec when power is first applied

SLOT A-10. REGULATOR/AMPLIFIER

Signature	Definition	Function
HDSOLDR	head solenoid drive	drive for head lift solenoid
HDSOLDRET	head solenoid return	return path from head solenoid
HMRET	head motor return	return path for head-stepping current
HPC	head power control	controls current to head-stepping motor
HPHA	head phase A	drive to ϕ A of head-stepping motor
HPHB	head phase B	drive to ϕ B of head-stepping motor
HPHC	head phase C	drive to ϕ C of head-stepping motor
HPHSA	head phase select A	printer control signal, selects phase A of head-stepping motor
HPHSB	head phase select B	printer control signal, selects phase B of head-stepping motor
HPHSC	head phase select C	printer control signal, selects phase C of head-stepping motor
LIFTHEAD	lift head	printer control command to energize head lift solenoid
PACA	paper advance control	controls current to paper stepping motor
PMRET	paper motor return	return path for paper stepping current
POS5V	positive 5 volts	5-volt supply
POS5VOVL	5-volt overload	limits current
POS5VREF/AUX	5-volt reference/auxiliary	auxiliary 5-volt supply from control/regulator
POS5VREGDR	5-volt regulator drive	control regulator signal, switches on regulator
PPHA	paper phase A	drive to ϕ A of paper-stepping motor
PPHB	paper phase b	drive to ϕ B of paper-stepping motor
PPHC	paper phase C	drive to ϕ C of paper-stepping motor
PPHSA	paper phase select A	printer control signal, selects ϕ A of paper-stepping motor
PPHSB	paper phase select B	printer control signal, selects ϕ B of paper-stepping motor
PPHSC	paper phase select C	printer control signal, selects ϕ C of paper-stepping motor
PWRRST	power reset	goes low for approx. 600 msec after power is applied

SLOT XA1. PRINthead INTERFACE.

This PC card is located on the left side of the terminal between the keyboard and the KSR card rack. The Printhead Interface PC card interconnects the Printer Code PC card (slot A-1) and the printhead. Don't confuse this XA1 number with the ASR (upper unit) XA1 Display PC card.

SLOT XA1. PRINthead INTERFACE

Signature	Definition	Function
DGRND	diode ground	return path for diode current
DVOLT	diode voltage	temperature-compensating diode voltage
ELM8	element 8	base drive to printhead element 8
HDRS1	head resistor select-1	slow resistor voltage
HDRS2	head resistor select-2	fast resistor voltage
PHBFRCLR-	printhead buffer clear	removes base drive to all printhead elements
PHCHR	printhead character	data clocked into head buffer
PHCLK	printhead clock	clocks data into head buffer
PVOLT	print voltage	supply voltage to printhead

ASR (UPPER UNIT) PC CARDS

SLOT XA-1. DISPLAY

Signature	Definition	Function
BOEOCA2	beginning and end of cassette-2	indicates when tape is on clear leader
CA2RDY	cassette-2 ready	indicates cassette-2 is ready to send or receive data
CNFMT	continuous format	places recorder in continuous format
C1RCD	cassette-1 record	indicates cassette-1 is in record mode
DATA-	data	serial data bus
DCHBIT8	display character bit 8	signal to LED display for bit 8 of last character in record buffer
KBDLOC-	keyboard local	indicates keyboard is in local mode
KBDON	keyboard on	indicates keyboard is not in off mode
PNHONQ	punch on Q	indicates recorder is not in overpunch mode
PNHRDY	punch ready	indicates recorder on and ready to receive data
PRNLOC-	printer local	indicates printer in local mode
PRNOFF	printer off	indicates printer in off mode
RCBFFL-	record buffer full	indicates when record buffer full and cannot accept more data
RCDON	recorder on	signal from switch which turns on recorder
RCDSTP	recorder stop	signal from switch which turns off recorder
RDROF-	reader off	stops playback operation
RDRON-	reader on	starts continuous playback operation
RERROR	reader error	indicates data dropout on tape
RFEED	reader feed	indicates playback is on
SCLK-	serial clock	clocks out status information to bus
STAENA	status enable	enables status register to send status information to data bus
TERLINE-	terminal on-line	indicates when terminal is on line
XBSPRV	switch block space reverse	signal from switch to initiate block reverse
XERASE	switch erase	signal from switch to clear record buffer or erase tape
XBSPFW	switch block space forward	signal from switch to initiate block forward
XC2RCD	switch cassette-2 record	signal from switch putting cassette-2 in record mode
XLD/FW2	switch load/fast forward 2	command from switch to load or fast forward cassette-2
XPBKLN	switch playback line	switch signal to put playback on line
XPBKOF	switch playback off	switch signal to turn playback off
XPRNBOF	switch print buffer	signal from switch to print out contents of record buffer
XRCDLN	switch recorder line	signal from switch placing recorder on line
XRCDOF	switch recorder off	signal from switch placing recorder in off mode
XRCHFW	switch read character forward	signal from switch to read 1 character
XREW2	switch rewind 2	command from switch to rewind cassette-2
XSTPCA2	switch stop cassette 2	command from switch to stop rewind, load, or fast forward cassette-2

SLOT XA-2 TAPE MOTION CONTROL

Signature	Definition	Function
BOEOCA1	BOT and EOT on cassette-1	clear leader on transport-1
BOT1	beginning-of-tape 1	goes high when BOT sensor does not sense mag tape on transport-1
CA1RDY	cassette-1 ready	indicates cassette-1 loaded and ready
C1BUSY	cassette-1 busy	indicates cassette-1 busy

SLOT XA-2 TAPE MOTION CONTROL (CONCLUDED)

C1CNTLDA	cassette-1 count load	load signal to cassette-1 gap counter
C1CNTDN	cassette-1 countdown	tells gap counter to count up for forward or down for reverse
C1CNTQ	cassette-1 count Q	indicates gap complete
C1FWQ	cassette-1 fast forward Q	set high when LOAD switch depressed while not on clear leader
C1INPLACE	cassette-1 in place	indicates cassette-1 in place and door closed
C1RCD	cassette-1 record	indicates cassette-1 in record mode
C1RWQ	cassette-1 rewind Q	set when REWIND switch is depressed
EOT1	end-of-tape 1	goes high when EOT sensor does not sense mag tape on transport-1
EOT1Q	end of tape 1 Q	synchronized EOT signal
GAP1Q	gap 1 Q	set high after LDBOT1Q set and BOT sensed
LDBOT1Q	load BOT 1 Q	set high after LOAD1Q and mag tape is reached
LOAD1Q	load 1 Q	set high when LOAD switch depressed while not on clear leader
PNHRDY	punch ready	indicates recorder loaded and ready
PWRRST-	power reset	goes low for approx. 600 msec after power is applied
RDLINE	reader line	indicates playback is on line and ready
RDRRDY	reader ready	indicates playback loaded and ready
READCK	read clock	204.8 kHz square wave
RECLINE	recorder line	indicates recorder is on line and ready
TERLINE-	terminal on-line	terminal is on line
TPRQO	tape read Q zero	command to move tape forward in READ mode
TPFWF	tape write forward	command to put tape in write or forward mode
T1FAST	transport-1 fast	command to put transport-1 in fast mode
T1FWD	transport-1 forward	signal puts transport-1 in FORWARD mode
T1LEQ	transport-1 left end Q	set when tape is on left end
T1REQ	transport-1 right end Q	set when tape is on right end
T1REV	transport-1 reverse	signal puts transport-1 in REVERSE mode
T1WRITE	transport-1 write	signal sent to transport-1 enabling write head
WRTTAB1	write tab 1	indicates presence of write enable TAB on transport-1
XLD/FW1	switch load/fast forward 1	switch command to load or fast forward cassette-1
XPBKLN	switch playback line	signal from switch to put playback on line
XPBKOF	switch playback off	signal from switch putting playback in OFF mode
XRCDLN	switch recorder line	signal from switch to put recorder on line
XRCDOF	switch recorder off	signal from switch putting recorder in OFF mode
XREW1	switch rewind 1	switch command to rewind cassette-1
XSTPCA1	switch stop cassette 1	switch command to stop rewind, load, or fast forward cassette-1

SLOT XA-3. REMOTE CASSETTE CONTROL

Signature	Definition	Function
BBKSPQ	block backspace	initiates a block reverse
BFWSPQ	block forward space	initiates a block forward
BLCNDN	block countdown	load gap counter for record transport to write a gap
BREVQ1	block reverse state 1	block reverse in progress
BREVQ2	block reverse state 2	data block detected
BREVQ3	block reverse state 3	gap detected
CDBIT1	code bit 1	1 of 4 parallel control bits
CDSTB	code strobe	strobe for 4 parallel control bits

SLOT XA-3. REMOTE CASSETTE CONTROL (CONCLUDED)

CNTQ	count	signifies gap has been written by record unit
C1BUSY	cassette-1 busy	playback, record, tape erase, or block reverse in progress on transport-1
C2BUSY	cassette-2 busy	playback, record, tape erase, or block reverse in progress on transport-2
C1CNTDN	cassette-1 countdown	signals gap counter-1 to countdown during block reverse
C2CNTDN	cassette-2 countdown	signals gap counter-2 to countdown during block reverse
C1CNTLD	cassette-1 load	load transport-1 gap counters
C2CNTLD	cassette-2 load	load transport-2 gap counters
C1CNTQ	cassette-1 count	terminates loading of transport-1
C2CNTQ	cassette-2 count	terminates loading of transport-2
C1CNTLDA	cassette-1 count load	load signal to transport-1 gap counters
C2CNTLDA	cassette-2 count load	load signal to transport-2 gap counters
C1RCD	cassette-1 record	cassette-1 is in record mode
C1R2BUSY	cassette-1 or -2 busy	
DETLK	detect block	block detected
KBDLOC	keyboard local	keyboard is in local mode
KBDON	keyboard on	
PBKBUSY	playback busy	playback on or block reverse in progress
PNHONQ	punch on	signifies recorder is on
PNHRDY	punch ready	recorder ready to record
RCDBUSY	recorder busy	recorder on or tape erase in progress
RCDOF	record off	remote record off line
RCDON	record on	remote record on line
RCDSTP	record stop	stops tape erase or record controller
RDRLINE	reader line	playback is on line
RDROF	reader off	remote reader is off line
RDRON	reader on	remote reader is on line
RDRSTQ	reader start	initiates continuous read operation
RDRRDY	reader ready	playback is ready
READCK	reader clock	204.8 kHz
RERRORQ	reader error	read error detected
REVDLY	reverse delay	signifies 64 tach pulses counted after gap detected
RFEED	reader feed	playback is reading a block from tape or transmitting data to bus
TPERSQ	tape erase	tape erase operation in progress
TREBLK	tape read block	signifies tape in interblock gap
TRFCLKB	transport reference clock B	1.0667 kHz used to count block reverse delay
TR1/4T	tape read 1/4T	signifies middle of data bit time
TR3/4T	tape read 3/4T	signifies middle of phase bit time
TR5/4T	tape read 5/4T	signifies bit dropout
TR21/4T	tape read 21/4T	signifies gap on tape
T1TACH	transport-1 tach	tach feedback from transport 1
T2TACH	transport-2 tach	tach feedback from transport 2
XBSPFW	switch block space forward	switch command to perform block forward
XBSPRV	switch block space reverse	switch command to perform block reverse
XC1RCD	switch cassette-1 record	switch command to place cassette-1 in record mode
XERASE	switch erase	switch command to erase tape or record buffer
XLD/FW1	switch load/fast forward 1	command to load or fast forward cassette 1
XRCHFV	switch read character forward	switch command to perform character forward
XREW1	switch rewind 1	command to rewind cassette 1
XSTPCA2	switch stop cassette 2	stops rewind, load, or fast forward on cassette 2

SLOT XA-4. PLAYBACK CONTROL

Signature	Definition	Function
BBKSPQ	block backspace	initiates a block reverse
BFWSPQ	block forward space	initiates playback of 1 block
BREVQ1	block reverse state 1	signifies a block reverse is in progress
BUFFULQ	buffer full	a block has been read from tape but not yet fully transmitted
CLRCS-	clear chip select	reset chip select counter
CRDRCLK-	cassette reader clock	buffered RDRCLK
CRDRENA-	cassette reader enable	buffered RDRENA
CSCLK	cassette system serial clock	buffered SCLK
M2ADOO	memory 2 address 0	most significant playback buffer address bit
M2ADUP	memory 2 address up	increments playback buffer address by 1
M2ADUP1	memory 2 address up 1	increments playback buffer address to put data into buffer
M2ADUP2	memory 2 address up 2	increments playback buffer address to take data out of buffer
M2CS1-	memory 2 chip select 1	enable memory chip 1
M2WDAT	memory 2 write data	data from tape read circuit to playback buffer
M2W2-	memory 2 write 2	write enable for playback buffer
RBTCNQH	reader bit count	signifies 8 bits (1 character) have been read from tape
RBTCNCK	reader bit count clock	clock input to tape read bit counter
RHCNLD-	reader character count load	clears tape read bit counter
RHCNO-	reader character count ≠ 0	signifies 90 characters read into playback buffer or 86 read out
RHCNUP-	reader character count up	increments character count by 1
RDRER-	reader end-of-block	end-of-block bit detected
RDRENA-	reader enable	data on bus from playback
RDRENAQ	reader enable Q	reader enable has been detected
RDRERR	reader error	read error and no error inhibit
RDROF-	reader off	stop playback
RDRONQ	reader on Q	signals reader to read continuously
RDRQ0	reader state 0	wait state
RDRQ1	reader state 1	send request to terminal control
RDRQ2	reader state 2	wait for enable state
RDRRDY	reader ready	playback ready
RDRREQ	reader request	
RDRSTQ	reader start	start playback
READCK	reader clock	204.8 kHz
REBCL-	reader end-of-block clear	signifies an end-of-block has been detected from playback
RERROR	reader error	signal to front panel ERROR lamp
RERRORQ	reader error	playback read error detected
RFEED	reader feed	playback reading tape or transmitting buffer contents
RNBCL	reader end-of-block clear Q	clear buffer full and error statuses
RSBLQ	reader send 1 block	signals reader to send 1 block
RSCHQ	reader send 1 character	signals reader to send 1 character
RSCHCK-	reader send a character clock	clocks in send 1 character status
RSCHCLR-	reader send a character clear	clears 'send 1 character' status
SCLK-	serial clock	clocks data on bus
TPRDST-	tape read start	starts tape read controller
TPRQ0	tape reader state 0	wait state
TPRQ1	tape reader state 1	preamble state check

SLOT XA-4. PLAYBACK CONTROL (CONCLUDED)

TPRQ2	tape reader state 2	reading data from tape
TPRQ3	tape reader state 3	looking for gap
TREBLK	tape read block	signifies a block has been read (playback reaches interblock gap)
TRQ3	tape read state 3	signifies tape data bit transition
TRSY	tape read sync	resets read data latch to proper state after TRSYNCQ1 is removed
TRSYNCQ1-	tape read sync 1	syncs tape read circuit to seek first preamble bit
TRSYNCQ2-	tape read sync 2	enables setting read data latch to correct state after TRSYNCQ1 is removed
TR1/4T	tape read 1/4 T	signifies middle of a data bit time
TR5/4T	tape read 5/4 T	signifies missing phase change
TR21/4T	tape read 21/4 T	signifies tape data gap found
XRCHFW	reader character forward	initiates a character forward operation

SLOT XA-5. RECORD BUFFER

Signature	Definition	Function
BLCNUP-	block count up	store beginning address of new block
CBKSPQ-	character backspace	decrement record buffer address by 1 during edit
CNFMT-	continuous format	ignore carriage return decode
CCLK	serial clock	clocks data on bus
DATA-		data on bus
DCHBIT1	display bit 1	bit 1 of character display
DCHCLR-	display character clear	clear character display register
FLCLK	flux clock	12.8 kHz, tape write data clock
MPNSTQ-	manual point stop	causes writing of nulls in memory after a manual stop is detected
M1AD00	memory 1 address 0	most significant bit of record buffer address
M1CK-	memory 1 clock	204.8 kHz
M1CKENA	memory 1 clock enable	
M1CS1	memory 1 chip select 1	selects memory chip 1 of record buffer memory
M1CS2	memory 1 chip select 2	timing to increment block counter
M1RDAT	memory 1 read data	record buffer output for tape write
M1RDRQ1	memory 1 read request 1	request to read from memory record buffer for display
M1RDRQ2	memory 1 read request 2	request to record buffer memory during memory read-only cycle
M1RD1CK	memory 1 read 1 clock	clock data to record buffer memory and then out of memory to display register
M1RD2	memory 1 read 2	read-only part of memory cycle
M1RD2CK-	memory 1 read 2 clock	clocks data from record buffer memory during memory read-only cycle
M1WRENA	memory 1 write enable	write data clocks for record buffer memory
M1WRRD1	memory 1 write/read 1	write/read part of memory cycle
M1WRRQ1	memory 1 write request 1	request to write in record buffer memory
PADCNL-	punch address count load	transfer beginning address of block to record memory address registers
PNHCNUP	punch count up	increment record buffer address by 1 after punching character
PNHCRD	punch carriage return	carriage return decode
PNHENAR	punch enable to receive	data on bus to recorder

SLOT XA-5. RECORD BUFFER (CONCLUDED)

PNHENAW-	punch enable to write	data on bus
PNHONQ	punch on	record is on
PNHRDY	punch ready	record ready
PNHO2Q	punch state 2	increments record buffer address by 1 during print buffer
PWRRST-	power reset	
RCBFFL-	record buffer full	same as TPWBSY-
READCK	read clock	204.8 kHz master system clock
TPWBSY-	tape write busy	recorder has block, but is not yet writing on tape; or recorder is writing block on tape and has second block in buffer
TRFCLKA	transport reference clock A	6400 Hz
TRFCLKB	transport reference clock B	1066.7 Hz

SLOT XA-6. TAPE READ/WRITE

Signature	Definition	Function
BCHCNO-	block character count = 0	86 characters have been written on tape
BCSELQ	block check select	enables block check data to tape
BLCNDN-	block count down	decrement block counter by 1
BLCNEO	block count = 0	no block to write on tape
BLCNG12-	block count > 12	block counter about to overflow (record buffer is full)
BLCNUP-	block count up	increment block counter by 1
CNFFMT-	continuous format	ignore end-of-block flag bit
CNTQ-	count Q	signifies end of a gap on tape
CPNHCLK	cassette punch clock	6.4 kHz
C1RCD	cassette-1 record	cassette 1 in record mode
C2RCD	cassette-2 record	cassette 2 in record mode
DATENQ	data enable Q	enables write data to tape
FLXCLK	flux clock	12.8 kHz tape write data clock
MEMENQ-	memory enable Q	signifies data still in record memory to put on tape
M1CS2	memory 1 chip select 2	block counter is decremented by 1 during this time, if necessary
M1RDAT	memory 1 read data	data from record buffer memory
M1RD2	memory 1 read 2	enables write data register
M1RD2CK	memory 1 read 2 clock	clocks record buffer data to write data register
M1RDRQ2	memory 1 read request 2	request to read data from record buffer memory
M2WDAT	memory 2 write data	tape read binary data for playback buffer memory
PAMTQ	postamble data	data for both preamble and postamble characters
PEPHQ	phase-encoded phase bit	PE data phase bit
PNHRDY	punch ready	record ready
PSAMQ	postamble	enables postamble data to tape
RDRCLK	reader clock	204.8 kHz
RERRORQ-	reader error	causes entry of nulls into playback buffer memory
TPERSQ	tape erase	starts transport forward
TPWBSY-	tape write busy	signifies record buffer is full, stop sending data
TPWDATA	tape write data	PE data to tape
TPWFW	tape write forward	move tape forward
TPW01Q	tape write state 1	start tape forward to write
TPW02Q	tape write state 2	end of gap, start writing data

SLOT XA-6. TAPE READ/WRITE (CONCLUDED)

TRDATA	tape read data	PE data from tape
TRDTA	tape read data A	indicates ZERO to ONE flux transition on tape
TRDTB	tape read data B	indicates ONE to ZERO flux transition on tape
TRQ1	tape read state 1	signifies a tape data bit transition from a ONE to a ZERO
TRQ2	tape read state 2	signifies a tape data bit transition from a ZERO to a ONE
TRQ3	tape read state 3	signifies a tape data bit transition from a ZERO to a ONE
TRSY-	tape read sync	resets read data latch to correct state after TRSYNCQ1 is removed
TRSYNCQ1-	tape read sync 1	syncs tape read circuit to detect first preamble bit
TRSYNCQ2-	tape read sync 2	enables resetting read data latch to correct state after TRSYNCQ1 is removed
TR1/4T	tape read 1/4 T	signifies 1/4 of a tape read data bit time (center of data bit time)
TR3/4T	tape read 3/4 T	signifies 3/4 of a tape read data bit time (center of phase bit time)
TWCHCLK-	tape write character clock	800 Hz, issues requests to read from record buffer memory
T1RDTA-	tape 1 read data A	tape read data from transport 1
T1RDTB-	tape 1 read data B	tape read data from transport 1
T2RDTA-	tape 2 read data A	tape read data from transport 2
T2RDTB-	tape 2 read data B	tape read data from transport 2
WRTDTQ	write data	binary write data to tape
WRTEBD-	write end of block	signifies last character of a block (in line format)
WRTEBQ1-	write end of block 1	end-of-block flag bit detected
WRTEBQ2-	write end of block 2	disable input data

SLOT XA-7. RECORD CONTROL

Signature	Definition	Function
BLCNUP-	block count up	increment record block counter by 1
BUFRREQ-	buffer request	print buffer operation
CBKSCNE0-	character backspace $\neq 0$	
CBKSPQ-	character backspace	decrement record buffer address by 1
CFWSPQ	character forward space	increment record buffer address by 1
COVPQ-	character overpunch	OR input character with record register and put result back into record register
CPNHCLK	cassette punch clock	6.4 kHz
CPNHQ	character punch	record a character
DATA-		serial data bus
DCHBIT1	display character bit 1	output of character display register
DCHCLR-	display character clear	
ERASEQ	erase	erase record buffer contents (reset address)
MPNSTQ-	manual stop	stop punch 'feed'
M1CS2	memory 1 chip select 2	block counter incremented during this time, if necessary
M1RDRQ1	memory 1 read request 1	request to read from record buffer memory
M1WRRQ1	memory 1 write request 1	request to write in record buffer memory
PADCNL-	punch address count load	load beginning address of present block
PNHCE0-	punch count = 0	
PNHCLR	punch clear	reset record controller
PNHCNE86	punch count = 86	

SLOT XA-7. RECORD CONTROL (CONCLUDED)

PNHCNUP	punch count up	increment punch character counter by 1
PNHCRD	punch carriage return decode	signifies a block ended by carriage return (line format)
PNHENAR-	punch enable to read	data on bus from record buffer
PNHENAW-	punch enable to write	data on bus to record buffer
PNHENARQ	punch enable to receive Q	signifies data sent to serial bus (end-of-record enable)
PNHLINE	punch on-line	record on line
PNHONQ	punch on	start punch 'feed'
PNH01Q	punch state 1	wait state
PNH02Q	punch state 2	update counters during print buffer
PNH03Q	punch state 3	send a print buffer request
PNH04Q	punch state 4	wait for a record enable
PNH05Q	punch state 5	terminate print buffer operation and reload record character counter
PNHRDY	punch ready	ready to record
PRNBUFQ-	print buffer Q	print out record buffer memory contents, if any
RCDSTP-	record stop	halts record operation
RECENA-	record enable	data on bus to/from recorder
TPBKSP-	tape backspace	backspace record buffer one character
TPFWSP-	tape forward space	forward space record buffer one character
XERASE-	erase	zero contents of record buffer, or erase tape
XPRNBUF-	print buffer	print the contents of the record buffer

SLOT XA-9. CASSETTE TRANSPORT

Signature	Definition	Function
BOT	beginning of tape	goes high when BOT sensor does not sense magnetic tape
CINPLACE	cassette in place	goes high when cassette in place and door closed
EOT	end of tape	goes high when EOT sensor does not sense magnetic tape
FAST	fast	places transport in fast mode
FWD	forward	command to move tape forward
RDTA	read data A	A component of PE read data (TTL)
RDTB	read data B	B component of PE read data (TTL)
REV	reverse	command to move tape backward
TACH	tach pulse	tach pulses from capstan motor tach generators
TRFCLKA	tape reference clock	reference clock for transports to control tape speed (6400 Hz)
WDATA	write data	TTL PE data to be written on tape
WRITE-	write	ZERO on this pin enables write circuits
WRRTAB	write tab	indicates when write enable tab is present

APPENDIX C

ELECTRICAL SCHEMATICS AND LOGIC DIAGRAMS

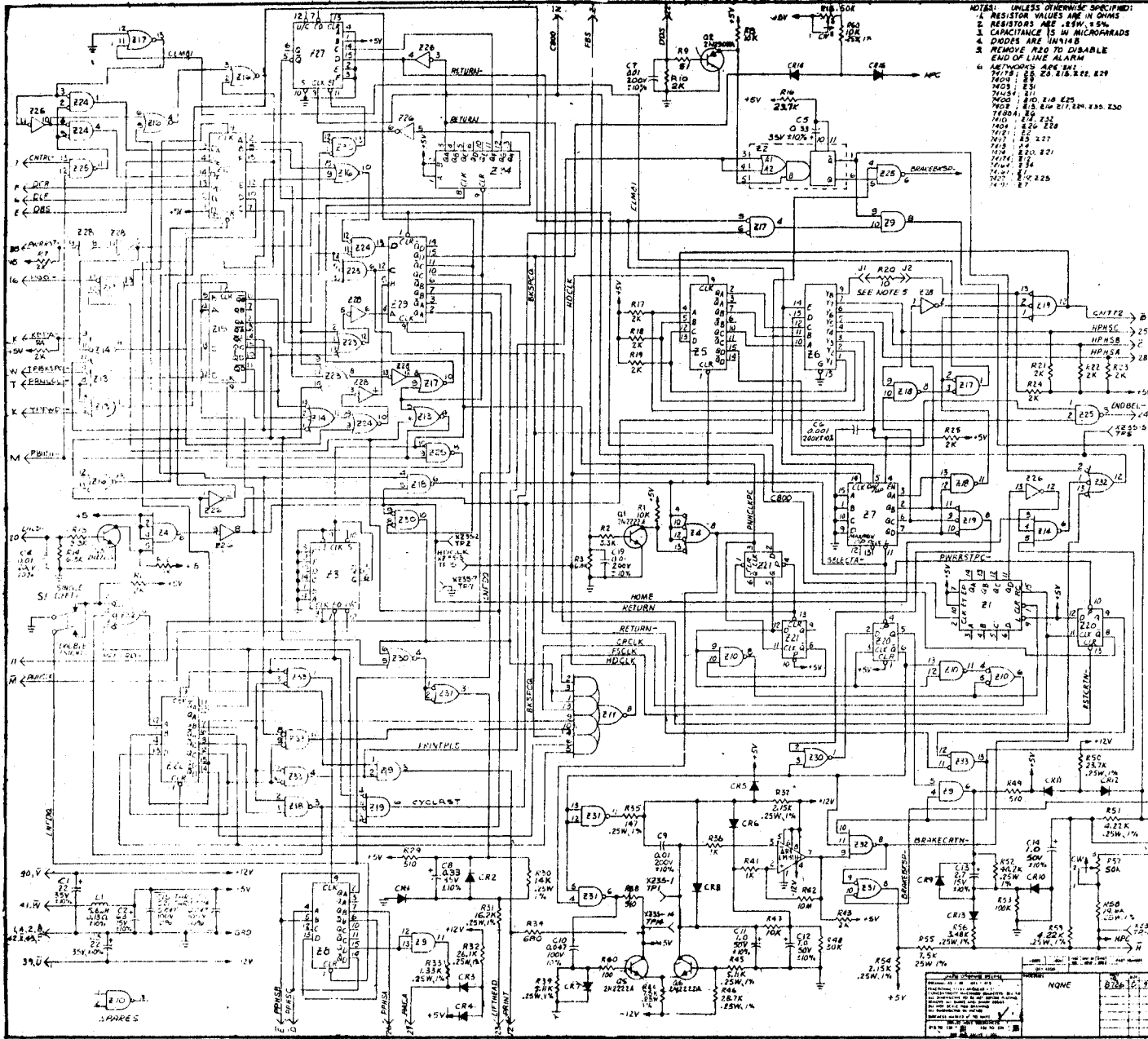
This Appendix contains electrical schematics and PC card logic diagrams to aid data terminal maintenance and troubleshooting. The drawings are arranged in numerical order as follows:

	Title	TI Drawing Number	Page
	*Printer Control	959175P	C-1
	Answer-Back Memory	959176B	C-2
	*ASCII Transmit/Receive	959177K	C-3
P —	Printer Code	959178M(2)	C-4, C-5
P —	Printhead Interface	959180B	C-6
	*Regulator/Amplifier (10A)	959181K	C-7
	*Control/Regulator (10A)	959182N	C-8
	*ASR Terminal Control	959183K	C-9
	Power Module Motherboard	959188G (2)	C-10, C-11
	ASR Module Motherboard	959189A	C-12
	Printhead	959190	C-13
	TTY Interface, Polar	959191D	C-14
	TTY Interface, Neutral	959192D	C-15
	KSR Terminal Control	959193E	C-16
C —	Display	959194F	C-17
	Modem, ATL	959195B (2)	C-18, C-19
	Baudot Transmit/Receive	959197J	C-20
	AC Power Assembly	959200E	C-21
C —	Remote Cassette Control	959201E	C-22
	Record Buffer Control	959202C	C-23
	*Playback Control	959203C	C-24
	*Motion Control	959204G	C-25
	*Tape Cassette Transport	960082T	C-26
C —	Record Control	962295D	C-27
	Tape Read/Write Controller	962296C	C-28
	*Auto Device Control	962297A	C-29
	Drive Mechanism	962299F (2)	C-30, C-31
	Modem, ATL	962300C (2)	C-32, C-33
	Modem, ATH	962301C (2)	C-34, C-35
C —	Dual Format Record Buffer	962302H	C-36
	*1200-Baud Receiver	962303C	C-37
P —	1200-Baud Transmitter	962304D	C-38
	Auto Answer Control	962307C	C-39
	Option Panel Display	962308A	C-40
	Paper Winder	962353	C-41
	TTY Interface, Computer	966657A	C-42
C —	Dual Format Tape Read/Write Control	969480D	C-43
	*Dual Format Playback Control	969481D	C-44
	*Dual Format ASCII Transmit/Receive	969482B	C-45
	Acoustic Coupler	969502C (2)	C-46, C-47
P —	Regulator/Amplifier (14A)	971444E	C-48
P —	Control Regulator (14A)	971451K	C-49
	*Remote Device Control	971495 (2)	C-50, C-51
	Auto Device Control	971498B	C-52

*Obsolete

Title	TI Drawing Number	Page
Remote Device Control (Multilayer)	971499D (2)	C-53, C-54
Auto Search Control (Multilayer)	971500B	C-55
Auto Search Control (Multiwire)	971503A	C-56
P — Remote Device Control (Multiwire)	971504B (2)	C-57, C-58
1200 Dual Format Transmit/Receive	971509E	C-59
ASR Footpedal	973865	C-60
P — 1200-Baud Receiver	973931B	C-61
P — Terminal Control	981309A	C-62
P — Printer Control	981312C	C-63
C — Motion Control	981316B	C-64
C — Dual Format Playback Control	981318A	C-65
Cassette Transport	981337G	C-66
*Cassette Transport (LED)	986357B	C-67

Handwritten note: } Missing



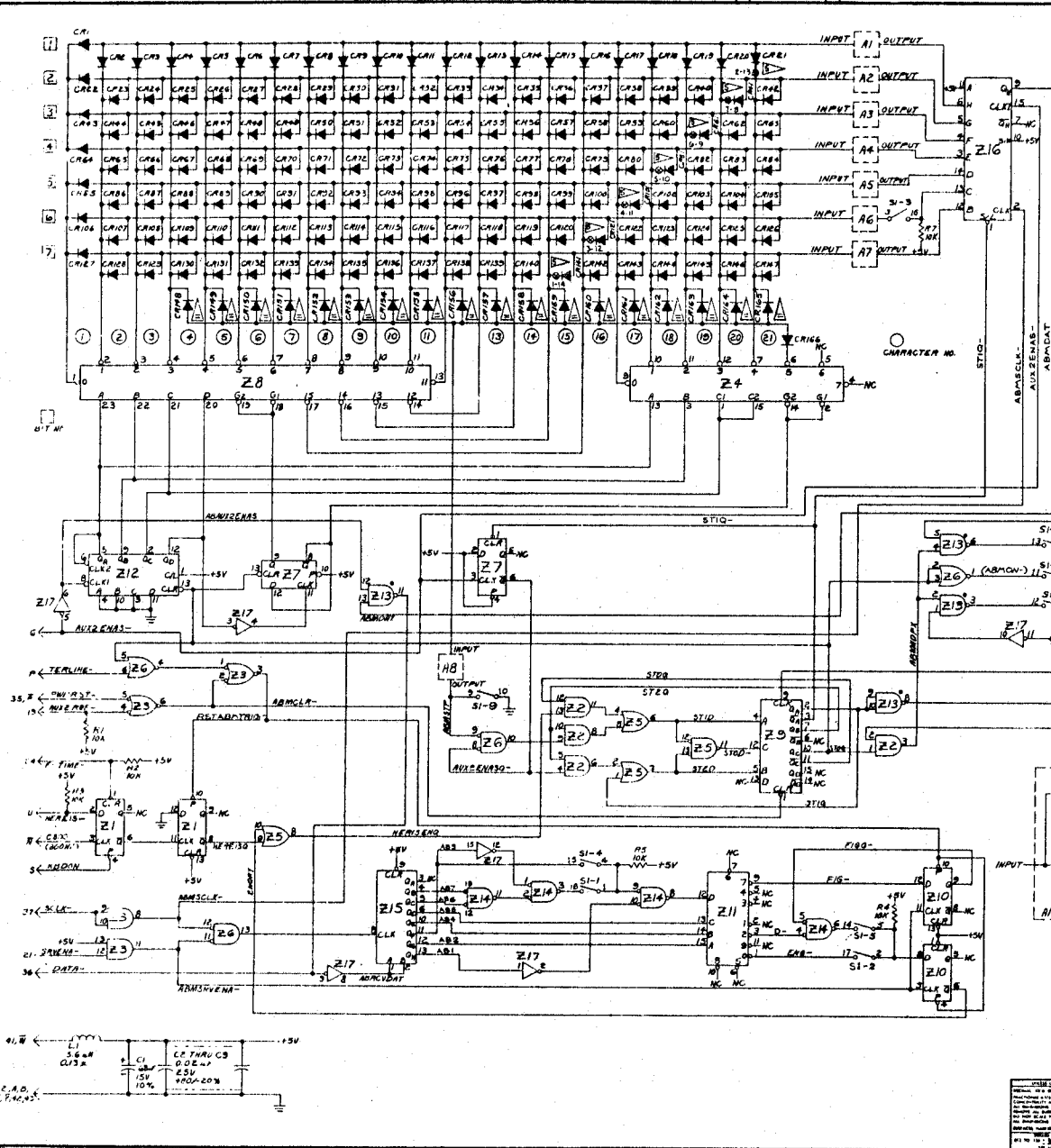
- NOTES: UNLESS OTHERWISE SPECIFIED:
1. RESISTOR VALUES ARE IN OHMS
 2. RESISTORS ARE 5% WATT
 3. CAPACITANCE IS IN MICROFARADS
 4. DIODES ARE 1N4148
 5. REMOVE R20 TO DISABLE END OF LINE ALARM
 6. PART NUMBERS ARE LISTED IN THE PARTS LIST
- 7410: 10
 7401: 11
 7404: 12
 7400: 13
 7402: 14
 7403: 15
 7405: 16
 7406: 17
 7407: 18
 7408: 19
 7409: 20
 7411: 21
 7412: 22
 7413: 23
 7414: 24
 7415: 25
 7416: 26
 7417: 27
 7418: 28
 7419: 29
 7420: 30

1. PRINTED CIRCUIT BOARD
 2. ALL PARTS LISTED IN PARTS LIST
 3. RESISTOR VALUES ARE IN OHMS
 4. CAPACITANCE IS IN MICROFARADS
 5. DIODES ARE 1N4148
 6. REMOVE R20 TO DISABLE END OF LINE ALARM
 7. PART NUMBERS ARE LISTED IN THE PARTS LIST

1. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 2. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 3. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 4. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 5. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 6. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 7. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 8. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 9. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 10. 2N3020 (B) 2N3020 (A) 2N3020 (C)

1. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 2. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 3. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 4. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 5. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 6. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 7. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 8. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 9. 2N3020 (B) 2N3020 (A) 2N3020 (C)
 10. 2N3020 (B) 2N3020 (A) 2N3020 (C)

C1

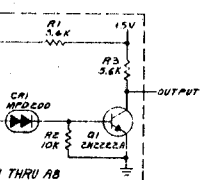


NOTES UNLESS OTHERWISE SPECIFIED
 1. RESISTANCE VALUES ARE IN OHMS
 2. RESISTORS ARE 1/4W, 5%
 3. DIODES ARE 1N34A
 4. NETWORKS ARE AS FOLLOWS:
 A. SW7470A-B-E
 B. SW7470A-B-E
 C. SW7470A-B-E
 D. SW7470A-B-E
 E. SW7470A-B-E
 F. SW7470A-B-E
 G. SW7470A-B-E
 H. SW7470A-B-E
 I. SW7470A-B-E
 J. SW7470A-B-E
 K. SW7470A-B-E
 L. SW7470A-B-E
 M. SW7470A-B-E
 N. SW7470A-B-E
 O. SW7470A-B-E
 P. SW7470A-B-E
 Q. SW7470A-B-E
 R. SW7470A-B-E
 S. SW7470A-B-E
 T. SW7470A-B-E
 U. SW7470A-B-E
 V. SW7470A-B-E
 W. SW7470A-B-E
 X. SW7470A-B-E
 Y. SW7470A-B-E
 Z. SW7470A-B-E

FUNCTION	CHARACTER	OPTIONAL
ASCH ABM	1, 2, 3, 4	1, 2, 3, 4
RECORD ABM	1, 2, 3, 4	1, 2, 3, 4
PRINT ABM	1, 2, 3, 4	1, 2, 3, 4
NOT PRINT ABM	1, 2, 3, 4	1, 2, 3, 4
RECLINE ABM	1, 2, 3, 4	1, 2, 3, 4
NOT RECLINE ABM	1, 2, 3, 4	1, 2, 3, 4
DISABLE ABM	1, 2, 3, 4	1, 2, 3, 4
TRIMMING FROM LINE	1, 2, 3, 4	1, 2, 3, 4

* ONLY TRUE WHEN PRINTER IS ON-LINE AND SYSTEM IS IN HALF-DUPLEX.
 ** ONLY TRUE WHEN RECORDER IS ON-LINE AND SYSTEM IS IN HALF-DUPLEX.

REFERENCE DESIGNATOR	VALUE
Z1	10K
Z2	10K
Z3	10K
Z4	10K
Z5	10K
Z6	10K
Z7	10K
Z8	10K
Z9	10K
Z10	10K
Z11	10K
Z12	10K
Z13	10K
Z14	10K
Z15	10K
Z16	10K
Z17	10K
Z18	10K
Z19	10K
Z20	10K
Z21	10K
Z22	10K
Z23	10K
Z24	10K
Z25	10K
Z26	10K
Z27	10K

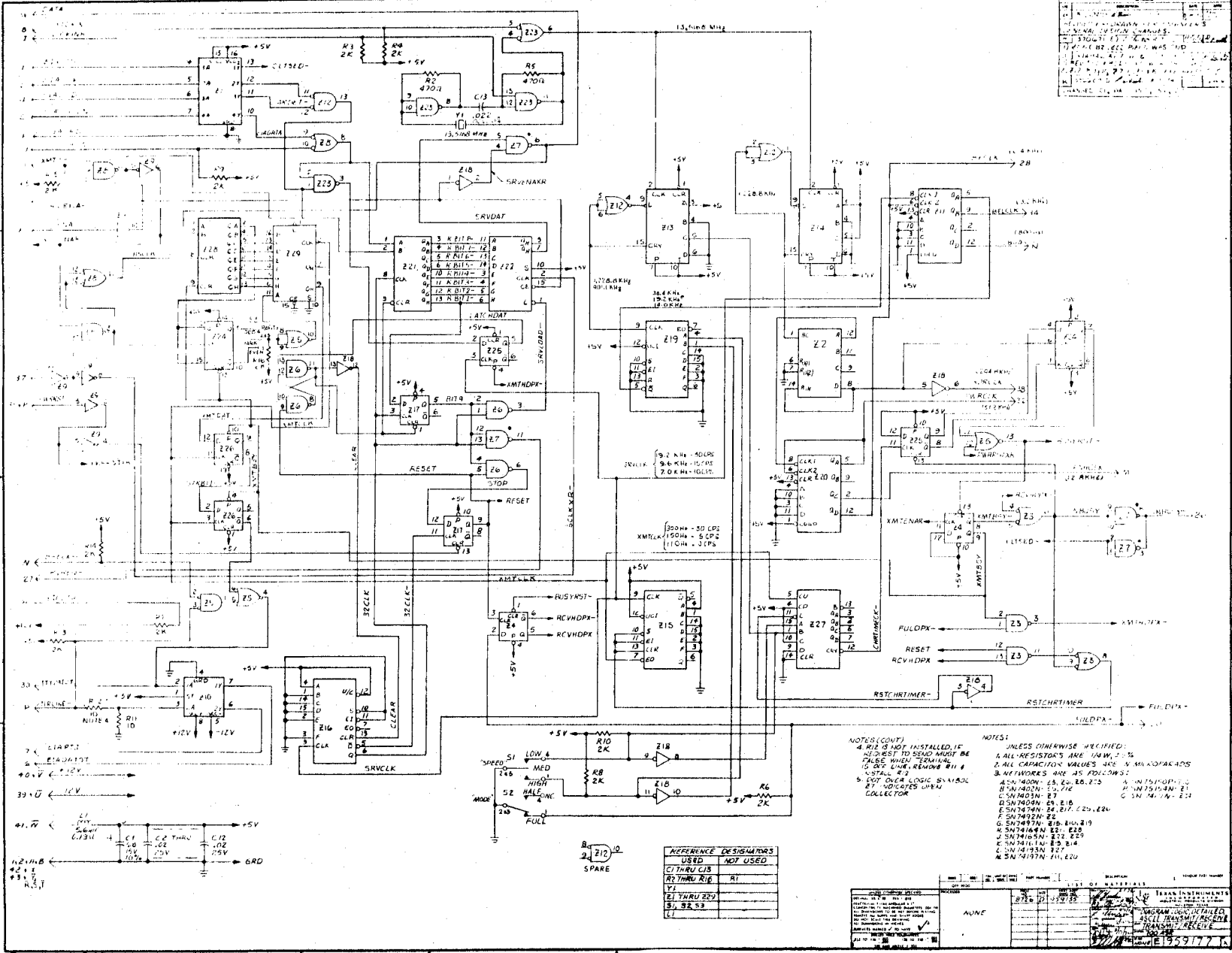


TEST POINT	TEST POINT	TEST POINT	TEST POINT
1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16
17	18	19	20
21	22	23	24
25	26	27	28
29	30	31	32
33	34	35	36
37	38	39	40
41	42	43	44
45	46	47	48
49	50	51	52
53	54	55	56
57	58	59	60
61	62	63	64
65	66	67	68
69	70	71	72
73	74	75	76
77	78	79	80
81	82	83	84
85	86	87	88
89	90	91	92
93	94	95	96
97	98	99	100

C2

1. A.D. 2. 1. 4. 2. 5.

TEXAS INSTRUMENTS
 1965



C3

NOTES (CONT.)

- # R18 IS NOT INSTALLED IF ADDRESS TO SEND MUST BE THREE WHEN TERMINAL IS SET LINE, REMOVE R11 & R12.
- DO NOT CHECK LOGIC SYMBOLS BY VICES WHEN COLLECTOR

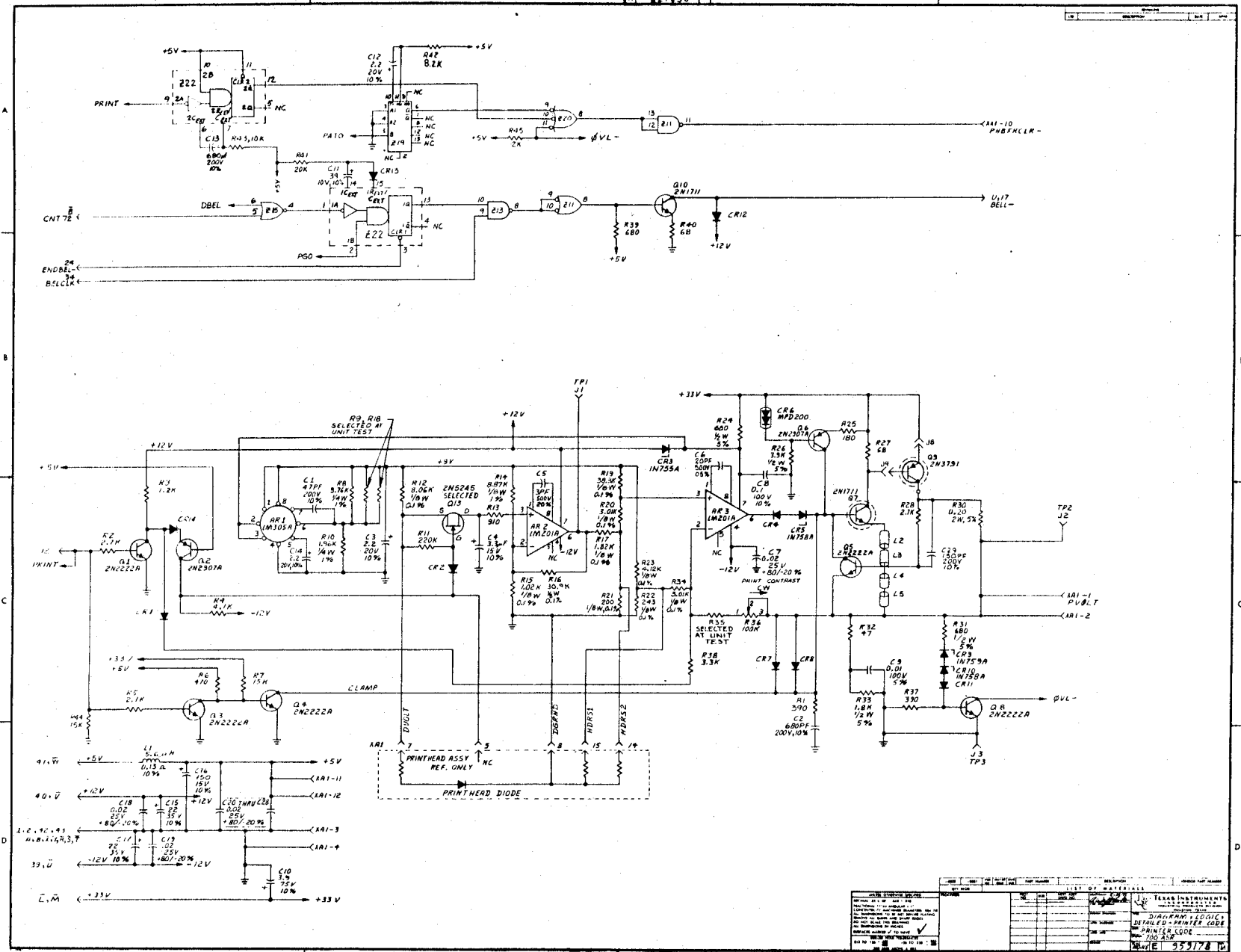
NOTES:

- UNLESS OTHERWISE SPECIFIED:
- ALL RESISTORS ARE 1/4W, 5%.
- ALL CAPACITOR VALUES ARE 5% MKA/PAK405.
- WAVEFORMS ARE AS FOLLOWS:
- 4SN7400N - 25, 20, 20, 25
- 4SN7401N - 25, 20, 20, 25
- 4SN7402N - 25, 20, 20, 25
- 4SN7403N - 25, 20, 20, 25
- 4SN7404N - 25, 20, 20, 25
- 4SN7405N - 25, 20, 20, 25
- 4SN7406N - 25, 20, 20, 25
- 4SN7407N - 25, 20, 20, 25
- 4SN7408N - 25, 20, 20, 25
- 4SN7409N - 25, 20, 20, 25
- 4SN7410N - 25, 20, 20, 25
- 4SN7411N - 25, 20, 20, 25
- 4SN7412N - 25, 20, 20, 25
- 4SN7413N - 25, 20, 20, 25
- 4SN7414N - 25, 20, 20, 25
- 4SN7415N - 25, 20, 20, 25
- 4SN7416N - 25, 20, 20, 25
- 4SN7417N - 25, 20, 20, 25
- 4SN7418N - 25, 20, 20, 25
- 4SN7419N - 25, 20, 20, 25
- 4SN7420N - 25, 20, 20, 25
- 4SN7421N - 25, 20, 20, 25
- 4SN7422N - 25, 20, 20, 25
- 4SN7423N - 25, 20, 20, 25
- 4SN7424N - 25, 20, 20, 25
- 4SN7425N - 25, 20, 20, 25
- 4SN7426N - 25, 20, 20, 25
- 4SN7427N - 25, 20, 20, 25
- 4SN7428N - 25, 20, 20, 25
- 4SN7429N - 25, 20, 20, 25
- 4SN7430N - 25, 20, 20, 25
- 4SN7431N - 25, 20, 20, 25
- 4SN7432N - 25, 20, 20, 25
- 4SN7433N - 25, 20, 20, 25
- 4SN7434N - 25, 20, 20, 25
- 4SN7435N - 25, 20, 20, 25
- 4SN7436N - 25, 20, 20, 25
- 4SN7437N - 25, 20, 20, 25
- 4SN7438N - 25, 20, 20, 25
- 4SN7439N - 25, 20, 20, 25
- 4SN7440N - 25, 20, 20, 25
- 4SN7441N - 25, 20, 20, 25
- 4SN7442N - 25, 20, 20, 25
- 4SN7443N - 25, 20, 20, 25
- 4SN7444N - 25, 20, 20, 25
- 4SN7445N - 25, 20, 20, 25
- 4SN7446N - 25, 20, 20, 25
- 4SN7447N - 25, 20, 20, 25
- 4SN7448N - 25, 20, 20, 25
- 4SN7449N - 25, 20, 20, 25
- 4SN7450N - 25, 20, 20, 25
- 4SN7451N - 25, 20, 20, 25
- 4SN7452N - 25, 20, 20, 25
- 4SN7453N - 25, 20, 20, 25
- 4SN7454N - 25, 20, 20, 25
- 4SN7455N - 25, 20, 20, 25
- 4SN7456N - 25, 20, 20, 25
- 4SN7457N - 25, 20, 20, 25
- 4SN7458N - 25, 20, 20, 25
- 4SN7459N - 25, 20, 20, 25
- 4SN7460N - 25, 20, 20, 25
- 4SN7461N - 25, 20, 20, 25
- 4SN7462N - 25, 20, 20, 25
- 4SN7463N - 25, 20, 20, 25
- 4SN7464N - 25, 20, 20, 25
- 4SN7465N - 25, 20, 20, 25
- 4SN7466N - 25, 20, 20, 25
- 4SN7467N - 25, 20, 20, 25
- 4SN7468N - 25, 20, 20, 25
- 4SN7469N - 25, 20, 20, 25
- 4SN7470N - 25, 20, 20, 25
- 4SN7471N - 25, 20, 20, 25
- 4SN7472N - 25, 20, 20, 25
- 4SN7473N - 25, 20, 20, 25
- 4SN7474N - 25, 20, 20, 25
- 4SN7475N - 25, 20, 20, 25
- 4SN7476N - 25, 20, 20, 25
- 4SN7477N - 25, 20, 20, 25
- 4SN7478N - 25, 20, 20, 25
- 4SN7479N - 25, 20, 20, 25
- 4SN7480N - 25, 20, 20, 25
- 4SN7481N - 25, 20, 20, 25
- 4SN7482N - 25, 20, 20, 25
- 4SN7483N - 25, 20, 20, 25
- 4SN7484N - 25, 20, 20, 25
- 4SN7485N - 25, 20, 20, 25
- 4SN7486N - 25, 20, 20, 25
- 4SN7487N - 25, 20, 20, 25
- 4SN7488N - 25, 20, 20, 25
- 4SN7489N - 25, 20, 20, 25
- 4SN7490N - 25, 20, 20, 25
- 4SN7491N - 25, 20, 20, 25
- 4SN7492N - 25, 20, 20, 25
- 4SN7493N - 25, 20, 20, 25
- 4SN7494N - 25, 20, 20, 25
- 4SN7495N - 25, 20, 20, 25
- 4SN7496N - 25, 20, 20, 25
- 4SN7497N - 25, 20, 20, 25
- 4SN7498N - 25, 20, 20, 25
- 4SN7499N - 25, 20, 20, 25
- 4SN7500N - 25, 20, 20, 25

REFERENCE DESIGNATORS	USED	NOT USED
C1 THRU C18		
R1 THRU R16		R1
V1		
Z1 THRU Z20		
B1, B2, B3		
L1		

DATE	BY	REV	DESCRIPTION
1978	...	1	...
1978	...	2	...
1978	...	3	...
1978	...	4	...
1978	...	5	...
1978	...	6	...
1978	...	7	...
1978	...	8	...
1978	...	9	...
1978	...	10	...
1978	...	11	...
1978	...	12	...
1978	...	13	...
1978	...	14	...
1978	...	15	...
1978	...	16	...
1978	...	17	...
1978	...	18	...
1978	...	19	...
1978	...	20	...
1978	...	21	...
1978	...	22	...
1978	...	23	...
1978	...	24	...
1978	...	25	...
1978	...	26	...
1978	...	27	...
1978	...	28	...
1978	...	29	...
1978	...	30	...
1978	...	31	...
1978	...	32	...
1978	...	33	...
1978	...	34	...
1978	...	35	...
1978	...	36	...
1978	...	37	...
1978	...	38	...
1978	...	39	...
1978	...	40	...
1978	...	41	...
1978	...	42	...
1978	...	43	...
1978	...	44	...
1978	...	45	...
1978	...	46	...
1978	...	47	...
1978	...	48	...
1978	...	49	...
1978	...	50	...
1978	...	51	...
1978	...	52	...
1978	...	53	...
1978	...	54	...
1978	...	55	...
1978	...	56	...
1978	...	57	...
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1978	...	59	...
1978	...	60	...
1978	...	61	...
1978	...	62	...
1978	...	63	...
1978	...	64	...
1978	...	65	...
1978	...	66	...
1978	...	67	...
1978	...	68	...
1978	...	69	...
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1978	...	73	...
1978	...	74	...
1978	...	75	...
1978	...	76	...
1978	...	77	...
1978	...	78	...
1978	...	79	...
1978	...	80	...
1978	...	81	...
1978	...	82	...
1978	...	83	...
1978	...	84	...
1978	...	85	...
1978	...	86	...
1978	...	87	...
1978	...	88	...
1978	...	89	...
1978	...	90	...
1978	...	91	...
1978	...	92	...
1978	...	93	...
1978	...	94	...
1978	...	95	...
1978	...	96	...
1978	...	97	...
1978	...	98	...
1978	...	99	...
1978	...	100	...

C-5



Printer Code

QTY	DESCRIPTION	REF. DESIG.	VALUE	MANUFACTURER
1	RESISTOR	R1	100K	RESISTOR
1	RESISTOR	R2	10K	RESISTOR
1	RESISTOR	R3	1.2K	RESISTOR
1	RESISTOR	R4	10K	RESISTOR
1	RESISTOR	R5	10K	RESISTOR
1	RESISTOR	R6	10K	RESISTOR
1	RESISTOR	R7	15K	RESISTOR
1	RESISTOR	R8	10K	RESISTOR
1	RESISTOR	R9	10K	RESISTOR
1	RESISTOR	R10	10K	RESISTOR
1	RESISTOR	R11	220K	RESISTOR
1	RESISTOR	R12	8.0K	RESISTOR
1	RESISTOR	R13	10K	RESISTOR
1	RESISTOR	R14	10K	RESISTOR
1	RESISTOR	R15	10K	RESISTOR
1	RESISTOR	R16	10K	RESISTOR
1	RESISTOR	R17	1.8K	RESISTOR
1	RESISTOR	R18	10K	RESISTOR
1	RESISTOR	R19	39.3K	RESISTOR
1	RESISTOR	R20	3.0K	RESISTOR
1	RESISTOR	R21	10K	RESISTOR
1	RESISTOR	R22	10K	RESISTOR
1	RESISTOR	R23	10K	RESISTOR
1	RESISTOR	R24	600	RESISTOR
1	RESISTOR	R25	180	RESISTOR
1	RESISTOR	R26	33M	RESISTOR
1	RESISTOR	R27	5K	RESISTOR
1	RESISTOR	R28	21K	RESISTOR
1	RESISTOR	R29	10K	RESISTOR
1	RESISTOR	R30	2W, 5K	RESISTOR
1	RESISTOR	R31	180	RESISTOR
1	RESISTOR	R32	10K	RESISTOR
1	RESISTOR	R33	10K	RESISTOR
1	RESISTOR	R34	10K	RESISTOR
1	RESISTOR	R35	10K	RESISTOR
1	RESISTOR	R36	100K	RESISTOR
1	RESISTOR	R37	10K	RESISTOR
1	RESISTOR	R38	10K	RESISTOR
1	RESISTOR	R39	10K	RESISTOR
1	RESISTOR	R40	10K	RESISTOR
1	CAPACITOR	C1	470P	CAPACITOR
1	CAPACITOR	C2	100V, 10%	CAPACITOR
1	CAPACITOR	C3	100V, 10%	CAPACITOR
1	CAPACITOR	C4	100V, 10%	CAPACITOR
1	CAPACITOR	C5	100V, 10%	CAPACITOR
1	CAPACITOR	C6	200P	CAPACITOR
1	CAPACITOR	C7	0.01	CAPACITOR
1	CAPACITOR	C8	0.02	CAPACITOR
1	CAPACITOR	C9	0.01	CAPACITOR
1	CAPACITOR	C10	100V, 10%	CAPACITOR
1	CAPACITOR	C11	100V, 10%	CAPACITOR
1	CAPACITOR	C12	2.2	CAPACITOR
1	CAPACITOR	C13	5.10K	CAPACITOR
1	CAPACITOR	C14	100V, 10%	CAPACITOR
1	CAPACITOR	C15	100V, 10%	CAPACITOR
1	CAPACITOR	C16	150	CAPACITOR
1	CAPACITOR	C17	100V, 10%	CAPACITOR
1	CAPACITOR	C18	0.02	CAPACITOR
1	CAPACITOR	C19	100V, 10%	CAPACITOR
1	CAPACITOR	C20	100V, 10%	CAPACITOR
1	CAPACITOR	C21	100V, 10%	CAPACITOR
1	CAPACITOR	C22	100V, 10%	CAPACITOR
1	CAPACITOR	C23	100V, 10%	CAPACITOR
1	CAPACITOR	C24	100V, 10%	CAPACITOR
1	CAPACITOR	C25	100V, 10%	CAPACITOR
1	CAPACITOR	C26	100V, 10%	CAPACITOR
1	CAPACITOR	C27	100V, 10%	CAPACITOR
1	CAPACITOR	C28	100V, 10%	CAPACITOR
1	CAPACITOR	C29	100V, 10%	CAPACITOR
1	CAPACITOR	C30	100V, 10%	CAPACITOR
1	CAPACITOR	C31	100V, 10%	CAPACITOR
1	CAPACITOR	C32	100V, 10%	CAPACITOR
1	CAPACITOR	C33	100V, 10%	CAPACITOR
1	CAPACITOR	C34	100V, 10%	CAPACITOR
1	CAPACITOR	C35	100V, 10%	CAPACITOR
1	CAPACITOR	C36	100V, 10%	CAPACITOR
1	CAPACITOR	C37	100V, 10%	CAPACITOR
1	CAPACITOR	C38	100V, 10%	CAPACITOR
1	CAPACITOR	C39	100V, 10%	CAPACITOR
1	CAPACITOR	C40	100V, 10%	CAPACITOR
1	CAPACITOR	C41	100V, 10%	CAPACITOR
1	CAPACITOR	C42	100V, 10%	CAPACITOR
1	CAPACITOR	C43	100V, 10%	CAPACITOR
1	CAPACITOR	C44	100V, 10%	CAPACITOR
1	CAPACITOR	C45	100V, 10%	CAPACITOR
1	CAPACITOR	C46	100V, 10%	CAPACITOR
1	CAPACITOR	C47	100V, 10%	CAPACITOR
1	CAPACITOR	C48	100V, 10%	CAPACITOR
1	CAPACITOR	C49	100V, 10%	CAPACITOR
1	CAPACITOR	C50	100V, 10%	CAPACITOR
1	CAPACITOR	C51	100V, 10%	CAPACITOR
1	CAPACITOR	C52	100V, 10%	CAPACITOR
1	CAPACITOR	C53	100V, 10%	CAPACITOR
1	CAPACITOR	C54	100V, 10%	CAPACITOR
1	CAPACITOR	C55	100V, 10%	CAPACITOR
1	CAPACITOR	C56	100V, 10%	CAPACITOR
1	CAPACITOR	C57	100V, 10%	CAPACITOR
1	CAPACITOR	C58	100V, 10%	CAPACITOR
1	CAPACITOR	C59	100V, 10%	CAPACITOR
1	CAPACITOR	C60	100V, 10%	CAPACITOR
1	CAPACITOR	C61	100V, 10%	CAPACITOR
1	CAPACITOR	C62	100V, 10%	CAPACITOR
1	CAPACITOR	C63	100V, 10%	CAPACITOR
1	CAPACITOR	C64	100V, 10%	CAPACITOR
1	CAPACITOR	C65	100V, 10%	CAPACITOR
1	CAPACITOR	C66	100V, 10%	CAPACITOR
1	CAPACITOR	C67	100V, 10%	CAPACITOR
1	CAPACITOR	C68	100V, 10%	CAPACITOR
1	CAPACITOR	C69	100V, 10%	CAPACITOR
1	CAPACITOR	C70	100V, 10%	CAPACITOR
1	CAPACITOR	C71	100V, 10%	CAPACITOR
1	CAPACITOR	C72	100V, 10%	CAPACITOR
1	CAPACITOR	C73	100V, 10%	CAPACITOR
1	CAPACITOR	C74	100V, 10%	CAPACITOR
1	CAPACITOR	C75	100V, 10%	CAPACITOR
1	CAPACITOR	C76	100V, 10%	CAPACITOR
1	CAPACITOR	C77	100V, 10%	CAPACITOR
1	CAPACITOR	C78	100V, 10%	CAPACITOR
1	CAPACITOR	C79	100V, 10%	CAPACITOR
1	CAPACITOR	C80	100V, 10%	CAPACITOR
1	CAPACITOR	C81	100V, 10%	CAPACITOR
1	CAPACITOR	C82	100V, 10%	CAPACITOR
1	CAPACITOR	C83	100V, 10%	CAPACITOR
1	CAPACITOR	C84	100V, 10%	CAPACITOR
1	CAPACITOR	C85	100V, 10%	CAPACITOR
1	CAPACITOR	C86	100V, 10%	CAPACITOR
1	CAPACITOR	C87	100V, 10%	CAPACITOR
1	CAPACITOR	C88	100V, 10%	CAPACITOR
1	CAPACITOR	C89	100V, 10%	CAPACITOR
1	CAPACITOR	C90	100V, 10%	CAPACITOR
1	CAPACITOR	C91	100V, 10%	CAPACITOR
1	CAPACITOR	C92	100V, 10%	CAPACITOR
1	CAPACITOR	C93	100V, 10%	CAPACITOR
1	CAPACITOR	C94	100V, 10%	CAPACITOR
1	CAPACITOR	C95	100V, 10%	CAPACITOR
1	CAPACITOR	C96	100V, 10%	CAPACITOR
1	CAPACITOR	C97	100V, 10%	CAPACITOR
1	CAPACITOR	C98	100V, 10%	CAPACITOR
1	CAPACITOR	C99	100V, 10%	CAPACITOR
1	CAPACITOR	C100	100V, 10%	CAPACITOR

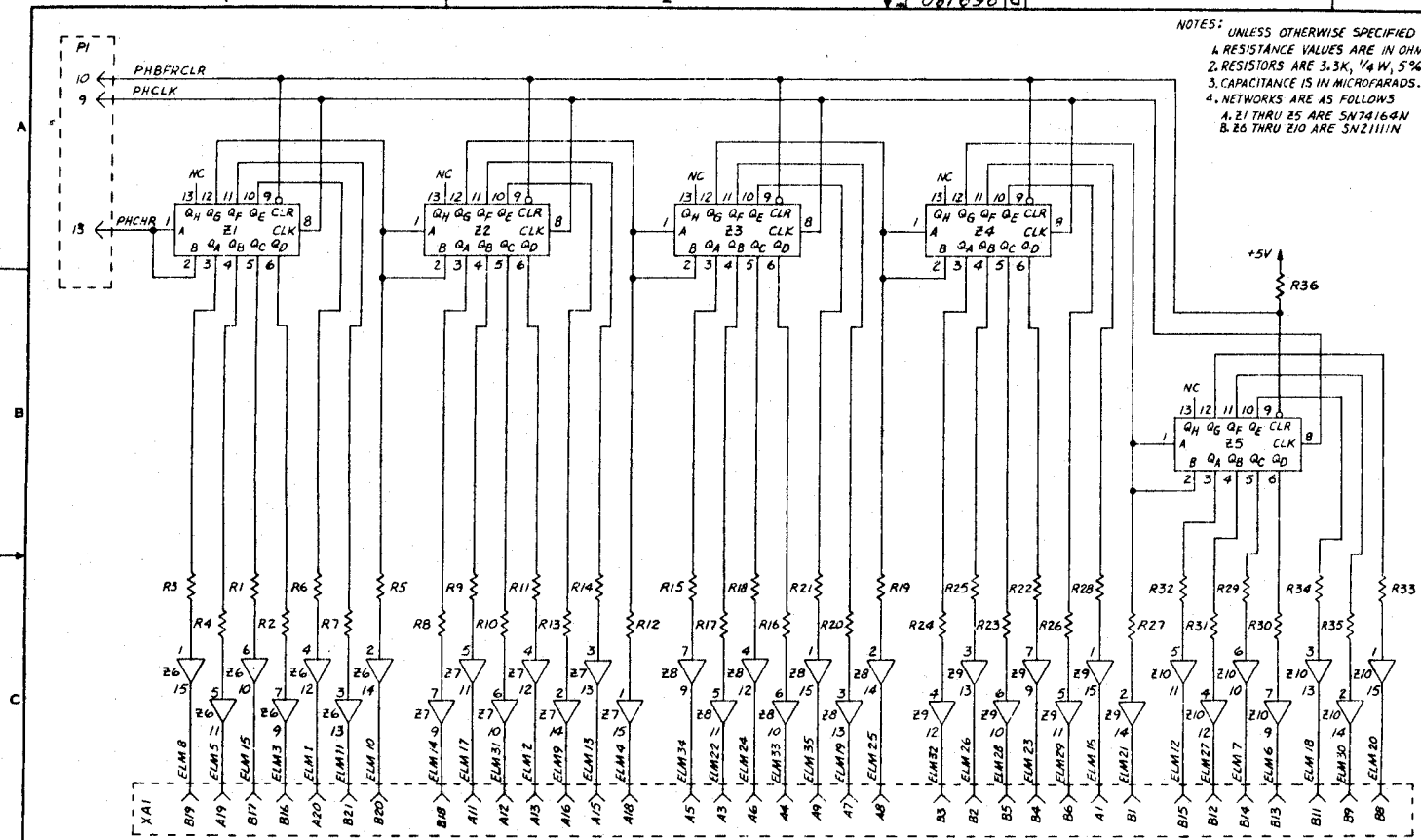
553728 W

Print Read Interface

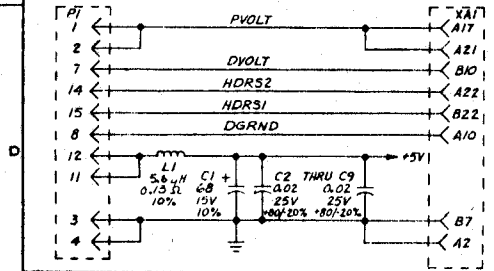
081656

NOTES:
 UNLESS OTHERWISE SPECIFIED
 1. RESISTANCE VALUES ARE IN OHMS
 2. RESISTORS ARE 3.3K, 1/4 W, 5%
 3. CAPACITANCE IS IN MICROFARADS.
 4. NETWORKS ARE AS FOLLOWS
 A. Z1 THRU Z5 ARE SN74164N
 B. Z6 THRU Z10 ARE SN2111IN

REV	DESCRIPTION	DATE	APP'D
A	367327 9-7-71	9-23-71	AK/LS
REMOVED FROM P/D C10 03/05/25V-A/070			
B	370632(1) 1/16/78	1/16/78	LS/LS
C1 WAS SN74164N			
FORMAL RELEASE			



C-6



USED	NOT USED
R1 THRU R36	
C1 THRU C9	
Z1 THRU Z10	
L1	
PI	
XA1	

REV	QTY	UNIT	DESCRIPTION	VENDOR PART NUMBER
0001	1	PCB	PCB	
0002	1	PCB	PCB	
0003	1	PCB	PCB	
0004	1	PCB	PCB	
0005	1	PCB	PCB	
0006	1	PCB	PCB	
0007	1	PCB	PCB	
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0098	1	PCB	PCB	
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0100	1	PCB	PCB	

DIAGRAM LOGIC DETAILED
 PRINTHEAD INTERFACE
 TOO ASR
 NONE D1959180

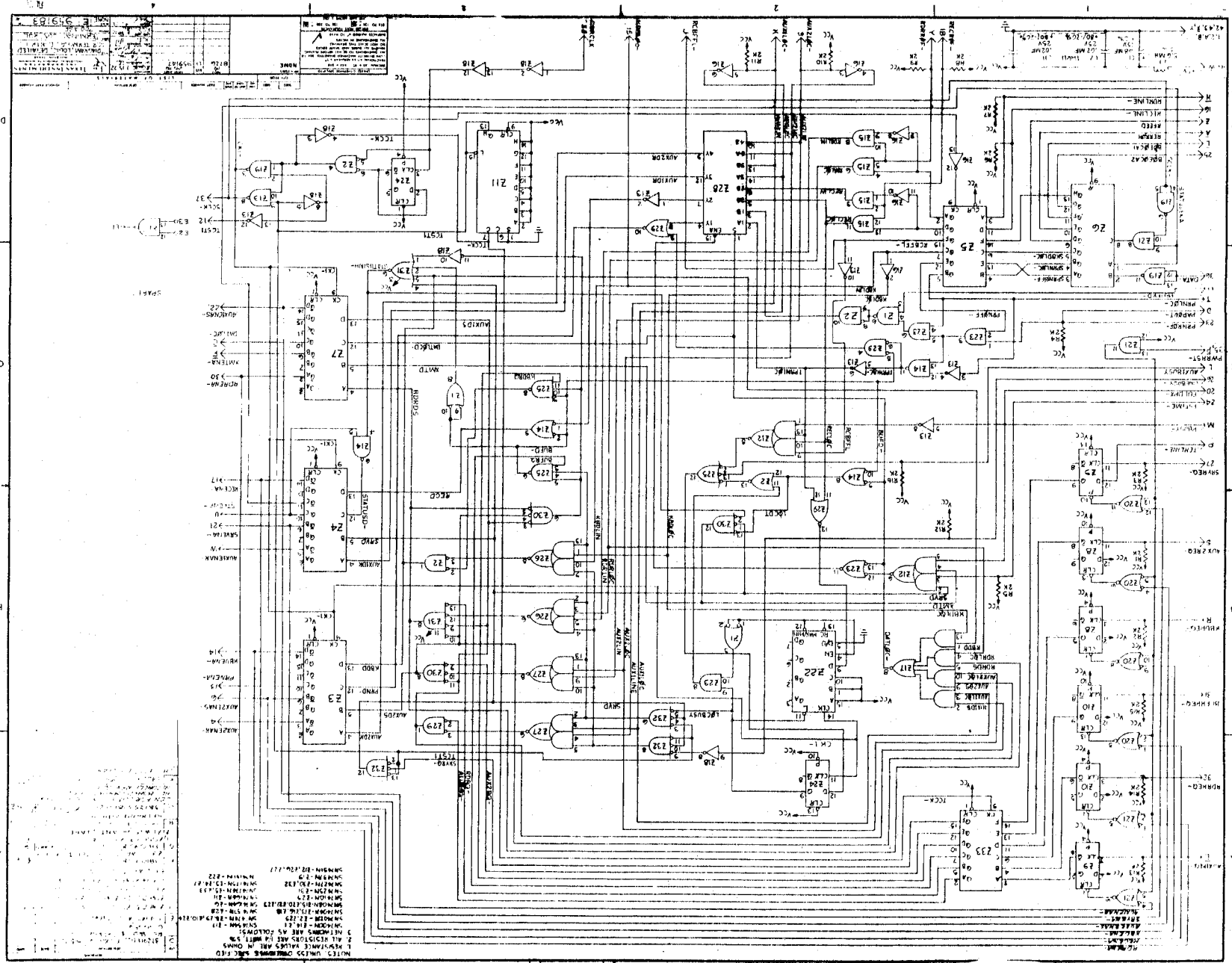
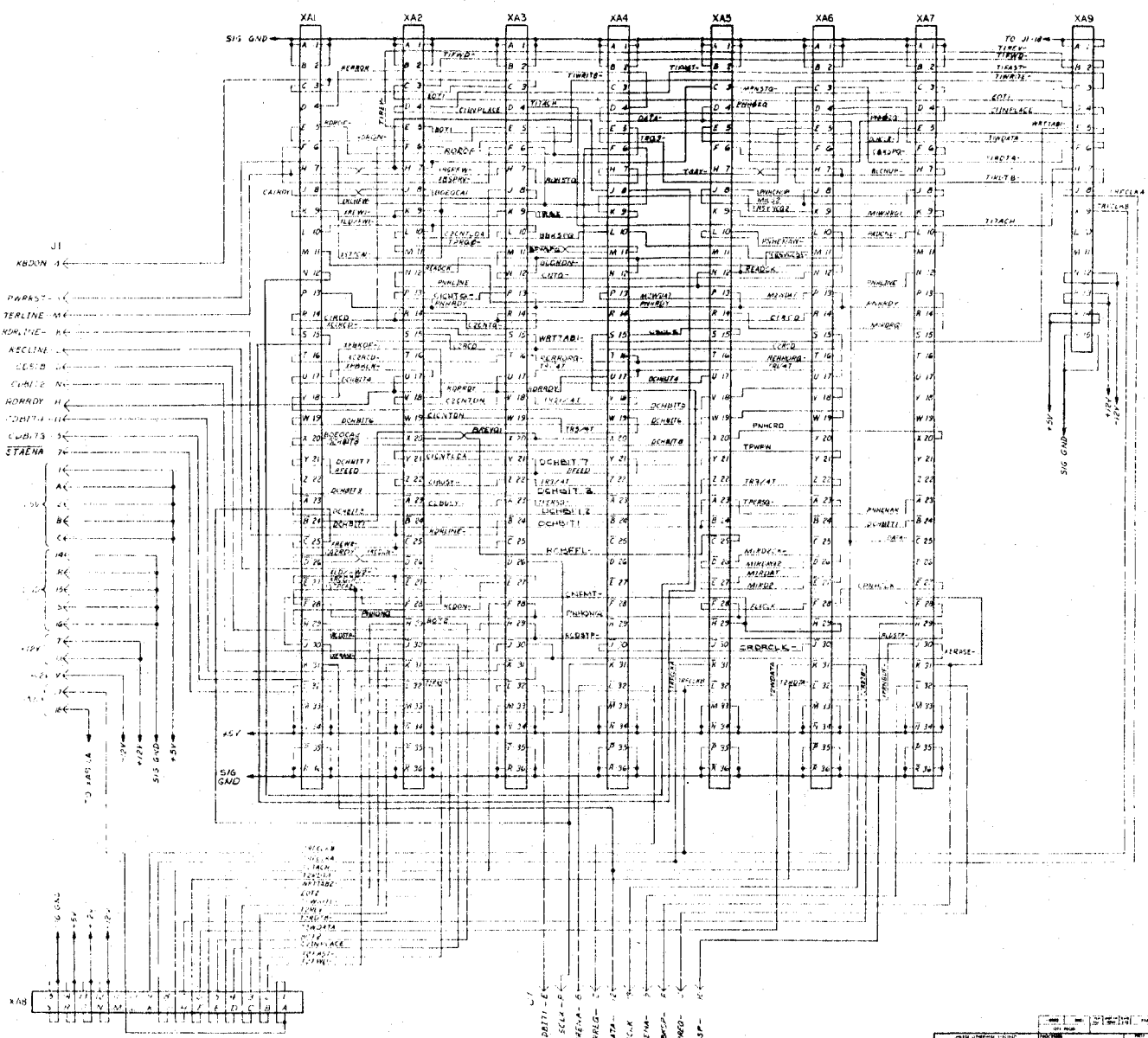


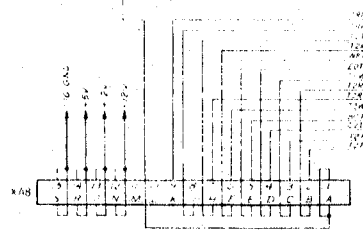
TABLE 1: Component List

IC	Part No.	Quantity	Notes
Z11	7411	1	3-STATE BUFFER
Z12	7412	1	3-STATE BUFFER
Z13	7413	1	3-STATE BUFFER
Z14	7414	1	3-STATE BUFFER
Z15	7415	1	3-STATE BUFFER
Z16	7416	1	3-STATE BUFFER
Z17	7417	1	3-STATE BUFFER
Z18	7418	1	3-STATE BUFFER
Z19	7419	1	3-STATE BUFFER
Z20	7420	1	3-STATE BUFFER
Z21	7421	1	3-STATE BUFFER
Z22	7422	1	3-STATE BUFFER
Z23	7423	1	3-STATE BUFFER
Z24	7424	1	3-STATE BUFFER
Z25	7425	1	3-STATE BUFFER
Z26	7426	1	3-STATE BUFFER
Z27	7427	1	3-STATE BUFFER
Z28	7428	1	3-STATE BUFFER
Z29	7429	1	3-STATE BUFFER
Z30	7430	1	3-STATE BUFFER
Z31	7431	1	3-STATE BUFFER
Z32	7432	1	3-STATE BUFFER
Z33	7433	1	3-STATE BUFFER
Z34	7434	1	3-STATE BUFFER
Z35	7435	1	3-STATE BUFFER
Z36	7436	1	3-STATE BUFFER
Z37	7437	1	3-STATE BUFFER
Z38	7438	1	3-STATE BUFFER
Z39	7439	1	3-STATE BUFFER
Z40	7440	1	3-STATE BUFFER
Z41	7441	1	3-STATE BUFFER
Z42	7442	1	3-STATE BUFFER
Z43	7443	1	3-STATE BUFFER
Z44	7444	1	3-STATE BUFFER
Z45	7445	1	3-STATE BUFFER
Z46	7446	1	3-STATE BUFFER
Z47	7447	1	3-STATE BUFFER
Z48	7448	1	3-STATE BUFFER
Z49	7449	1	3-STATE BUFFER
Z50	7450	1	3-STATE BUFFER
Z51	7451	1	3-STATE BUFFER
Z52	7452	1	3-STATE BUFFER
Z53	7453	1	3-STATE BUFFER
Z54	7454	1	3-STATE BUFFER
Z55	7455	1	3-STATE BUFFER
Z56	7456	1	3-STATE BUFFER
Z57	7457	1	3-STATE BUFFER
Z58	7458	1	3-STATE BUFFER
Z59	7459	1	3-STATE BUFFER
Z60	7460	1	3-STATE BUFFER
Z61	7461	1	3-STATE BUFFER
Z62	7462	1	3-STATE BUFFER
Z63	7463	1	3-STATE BUFFER
Z64	7464	1	3-STATE BUFFER
Z65	7465	1	3-STATE BUFFER
Z66	7466	1	3-STATE BUFFER
Z67	7467	1	3-STATE BUFFER
Z68	7468	1	3-STATE BUFFER
Z69	7469	1	3-STATE BUFFER
Z70	7470	1	3-STATE BUFFER
Z71	7471	1	3-STATE BUFFER
Z72	7472	1	3-STATE BUFFER
Z73	7473	1	3-STATE BUFFER
Z74	7474	1	3-STATE BUFFER
Z75	7475	1	3-STATE BUFFER
Z76	7476	1	3-STATE BUFFER
Z77	7477	1	3-STATE BUFFER
Z78	7478	1	3-STATE BUFFER
Z79	7479	1	3-STATE BUFFER
Z80	7480	1	3-STATE BUFFER
Z81	7481	1	3-STATE BUFFER
Z82	7482	1	3-STATE BUFFER
Z83	7483	1	3-STATE BUFFER
Z84	7484	1	3-STATE BUFFER
Z85	7485	1	3-STATE BUFFER
Z86	7486	1	3-STATE BUFFER
Z87	7487	1	3-STATE BUFFER
Z88	7488	1	3-STATE BUFFER
Z89	7489	1	3-STATE BUFFER
Z90	7490	1	3-STATE BUFFER
Z91	7491	1	3-STATE BUFFER
Z92	7492	1	3-STATE BUFFER
Z93	7493	1	3-STATE BUFFER
Z94	7494	1	3-STATE BUFFER
Z95	7495	1	3-STATE BUFFER
Z96	7496	1	3-STATE BUFFER
Z97	7497	1	3-STATE BUFFER
Z98	7498	1	3-STATE BUFFER
Z99	7499	1	3-STATE BUFFER
Z100	7500	1	3-STATE BUFFER

NOTES: UNLESS OTHERWISE SPECIFIED, ALL COMPONENTS ARE AS SHOWN IN THIS DRAWING. 1. RESISTOR VALUES ARE IN OHMS. 2. ALL DIMENSIONS ARE IN MILLI-METERS. 3. DIMENSIONS ARE AS SHOWN IN THIS DRAWING.



C-12



- REC-10
- REC-11
- REC-12
- REC-13
- REC-14
- REC-15
- REC-16
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- REC-96
- REC-97
- REC-98
- REC-99
- REC-100

62/555

DATE: 1/18/72

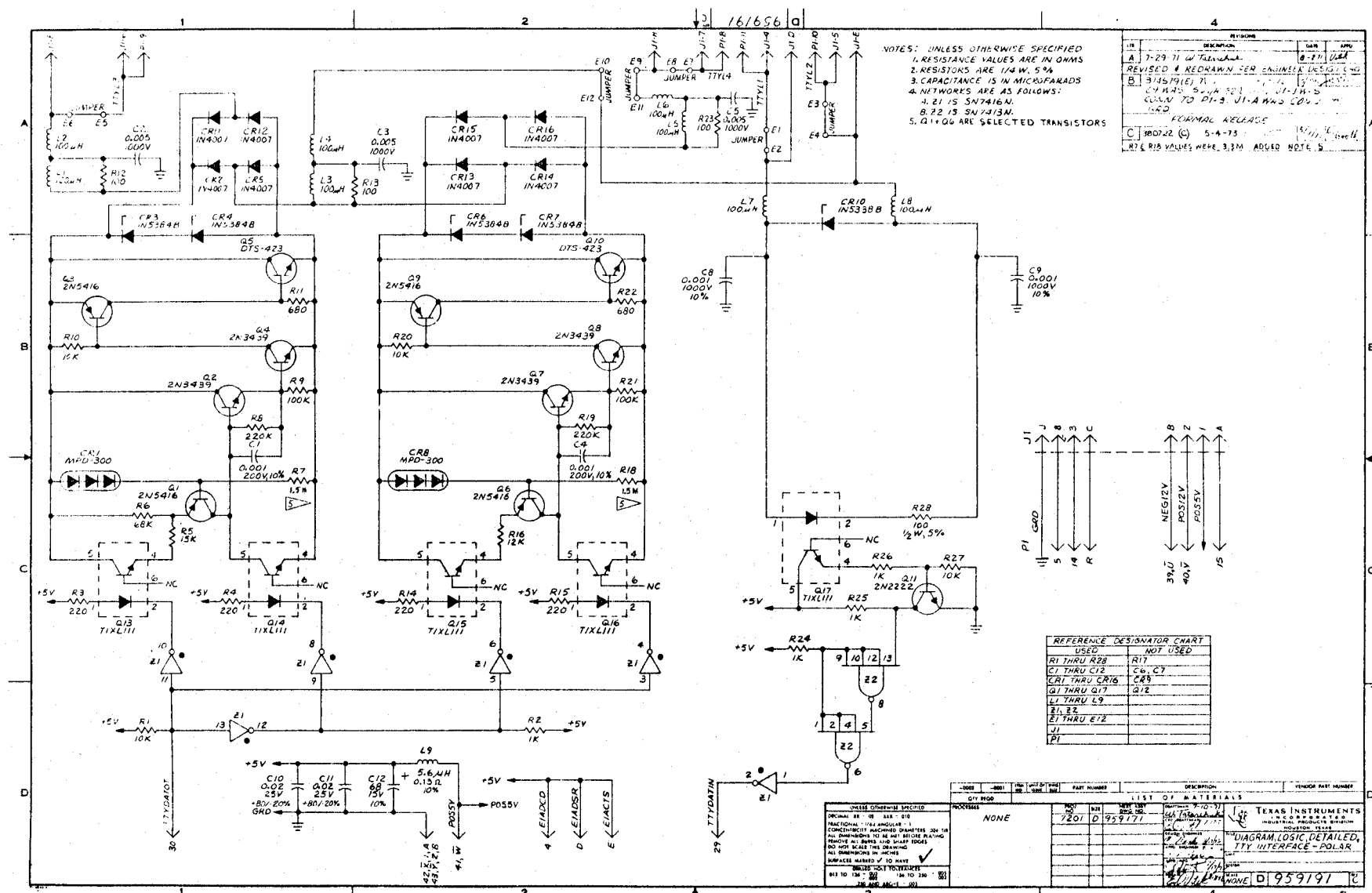
TIME: 9:30 AM

BY: [Signature]

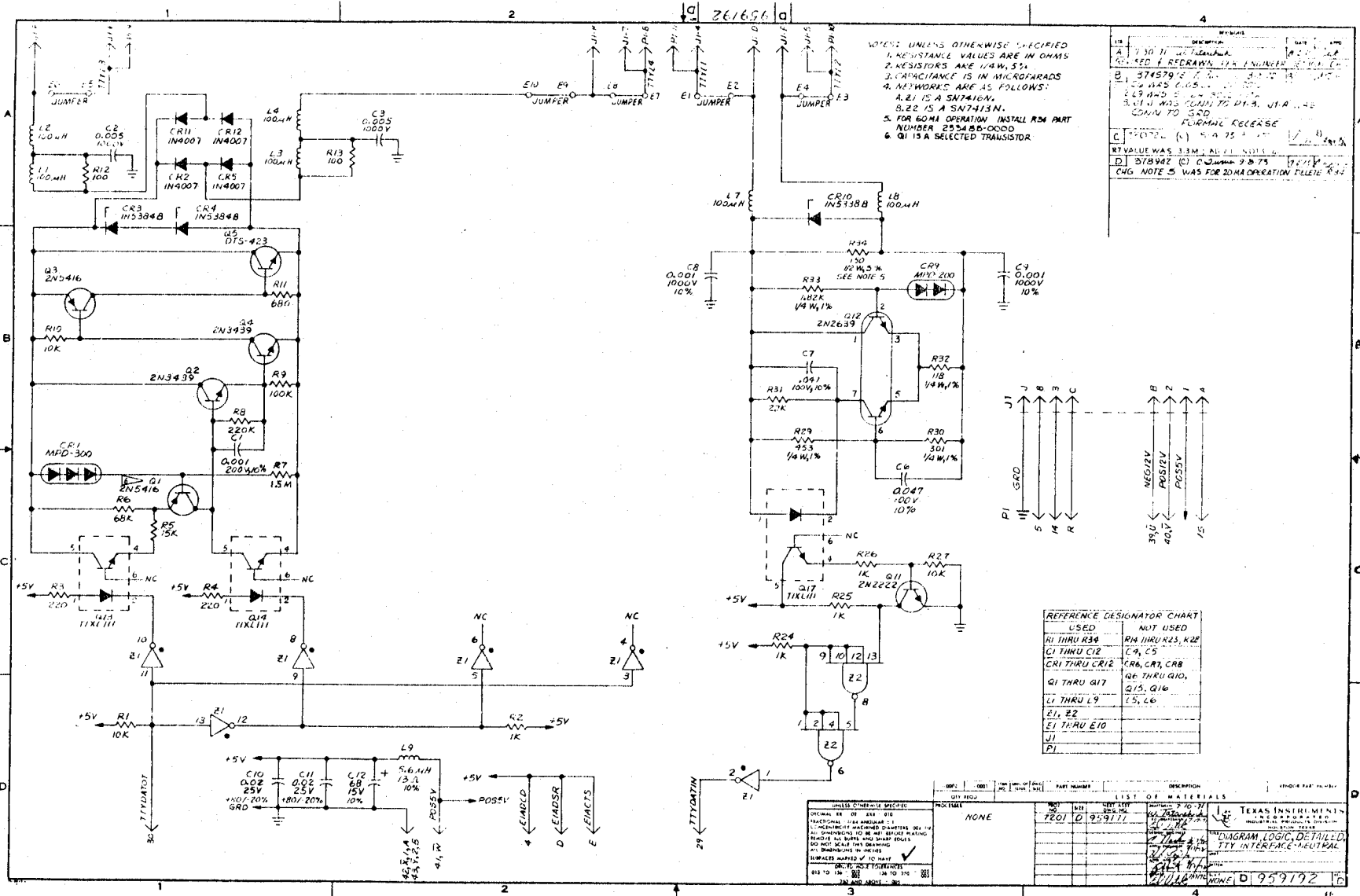
TEST INSTRUMENTS

95918

C14

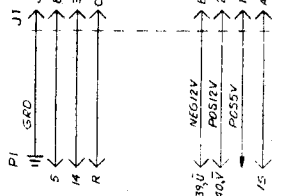


C-15



NOTES: UNLESS OTHERWISE SPECIFIED
 1. RESISTANCE VALUES ARE IN OHMS
 2. RESISTORS ARE 1/4W, 5%
 3. CAPACITANCE IS IN MICROFARADS
 4. NETWORKS ARE AS FOLLOWS:
 A, E1 IS A SN7413N.
 B, E2 IS A SN7413N.
 5. FOR 60M1 OPERATION INSTALL RM PART NUMBER 2534-BD-0000
 6. Q1 IS A SELECTED TRANSISTOR

REVISIONS
 DATE BY
 1 1730 11 11 1964
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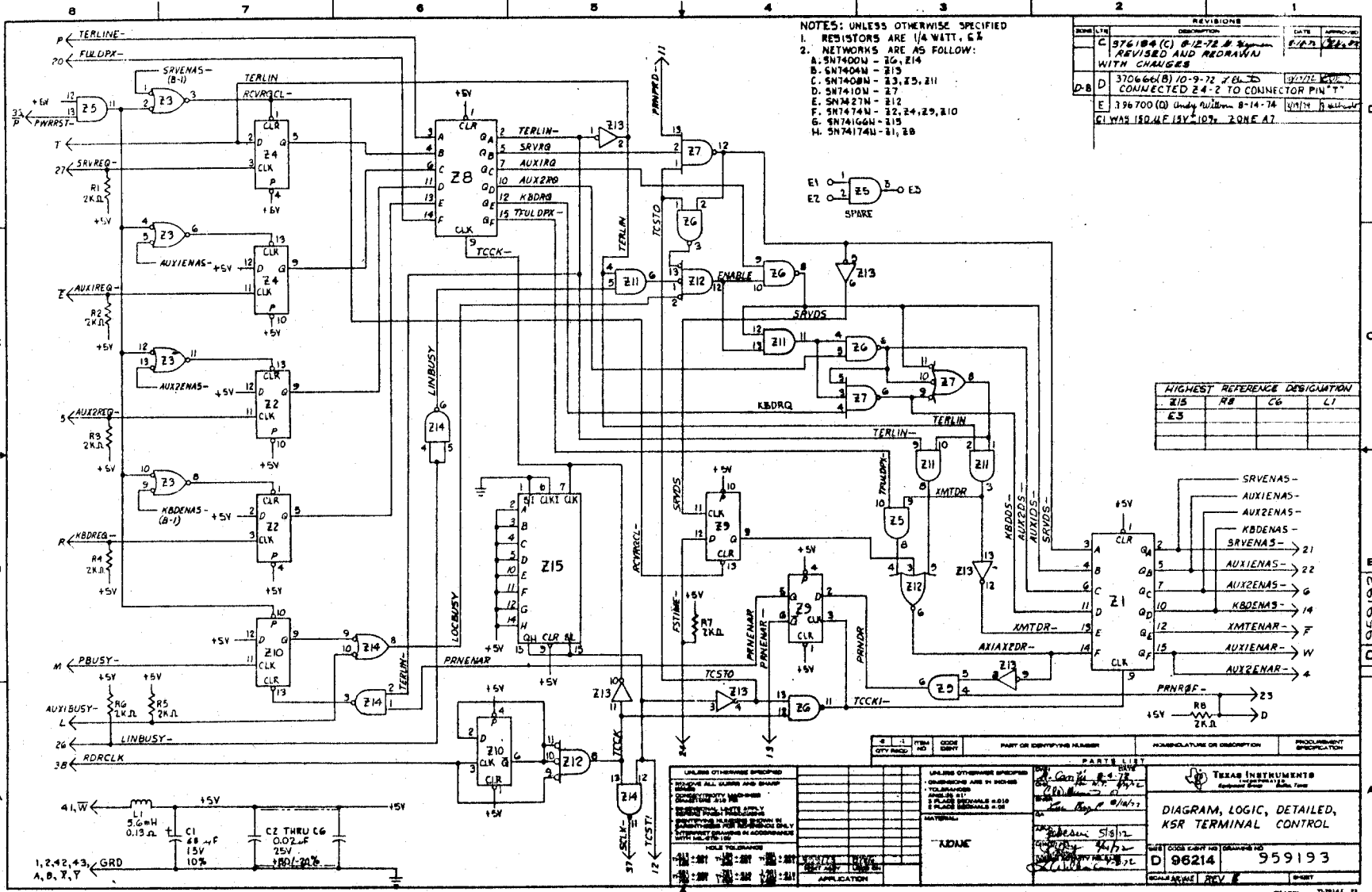


USED	NOT USED
R1 THRU R34	R4 THRU R37
C1 THRU C12	C4, C5
CR1 THRU CR12	CR6, CR7, CR8
Q1 THRU Q17	Q8 THRU Q10, Q15, Q16
L1 THRU L9	L5, L6
E1, E2	
E1 THRU E10	
J1	
P1	

REV	DATE	BY	DESCRIPTION
1	11/11/64		
2	11/11/64		
3	11/11/64		
4	11/11/64		
5	11/11/64		
6	11/11/64		
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50	11/11/64		

TEXAS INSTRUMENTS
 INSTRUMENT PRODUCTS DIVISION
 DALLAS, TEXAS
 DIAGRAM, LOGIC, DETAIL, D.
 TTY INTERFACE - NEUTRAL
 NONE 959192

C-16

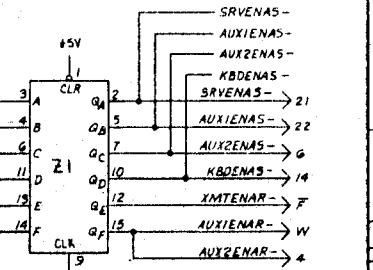


NOTES: UNLESS OTHERWISE SPECIFIED
 1. RESISTORS ARE 1/4 WATT, 5%
 2. NETWORKS ARE AS FOLLOW:
 A. SN7400N - 10, Z14
 B. SN7404N - Z13
 C. SN7408N - Z3, Z5, Z11
 D. SN7410N - Z7
 E. SN7427N - Z12
 F. SN7474N - Z2, Z4, Z9, Z10
 G. SN74166N - Z15
 H. SN74174N - Z1, Z8

REV. NO.	DATE	APPROVED
C	8-12-72	[Signature]
D	10-9-72	[Signature]
E	8-14-74	[Signature]

DESCRIPTION: 976104 (C) 8-12-72 & 10-9-72 REVISED AND REDRAWN WITH CHANGES
 370666 (B) 10-9-72 Z15, Z16 CONNECTED 2-4-2 TO CONNECTOR PIN "T"
 396700 (D) Under Review 8-14-74

HIGHEST REFERENCE DESIGNATION			
Z/S	RB	CG	LT
Z5			

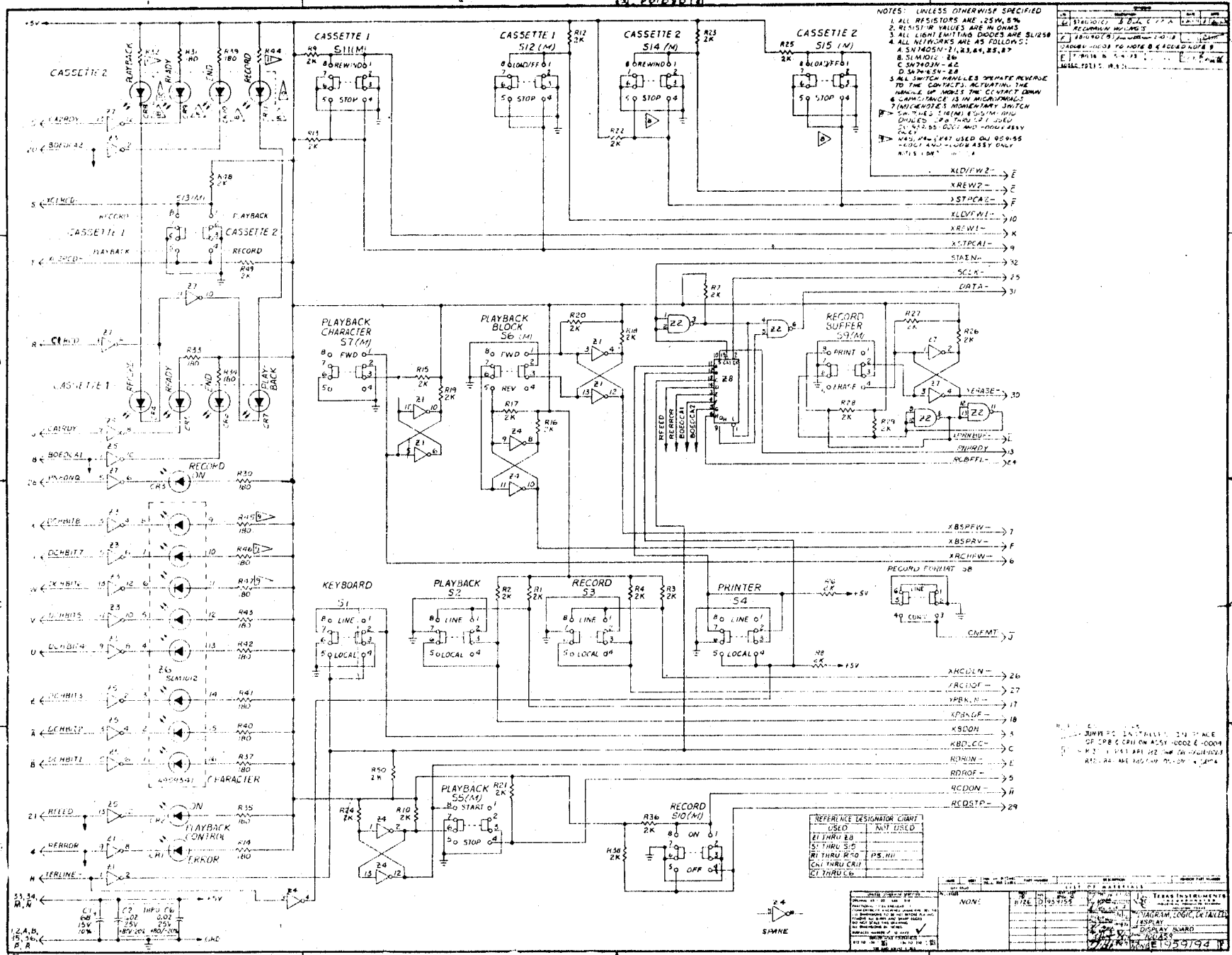


QTY REQ.	ITEM NO.	CODE	PART OR IDENTIFYING NUMBER	MANUFACTURE OR DESCRIPTION	PROCUREMENT SPECIFICATION

PARTS LIST	
QTY	DESCRIPTION
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1	IC 74104
1	IC 74103
1	IC 7410
1	IC 74108
1	IC 74107
1	IC 74106
1	IC 74105
1	IC 74104
1	IC 74103
1	IC 74102
1	IC 74101
1	IC 74100
1	IC 74109
1	IC 74108
1	IC 74107
1	IC 74106
1	IC 74105
1	IC 74104
1	IC 74103
1	IC 74102
1	IC 74101
1	IC 74100
1	IC 74109
1	IC 74108
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1	IC 74103
1	IC 74102
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- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE .25W, 5%.
 2. RESISTOR VALUES ARE IN OHMS.
 3. ALL CAPACITORS UNLESS OTHERWISE SPECIFIED ARE 50VDC.
 4. ALL NETWORKS ARE AS FOLLOWS:
 5. SWITCHES S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, S13, S14, S15, S16, S17, S18, S19, S20, S21, S22, S23, S24, S25, S26, S27, S28, S29, S30, S31, S32, S33, S34, S35, S36, S37, S38, S39, S40, S41, S42, S43, S44, S45, S46, S47, S48, S49, S50, S51, S52, S53, S54, S55, S56, S57, S58, S59, S60, S61, S62, S63, S64, S65, S66, S67, S68, S69, S70, S71, S72, S73, S74, S75, S76, S77, S78, S79, S80, S81, S82, S83, S84, S85, S86, S87, S88, S89, S90, S91, S92, S93, S94, S95, S96, S97, S98, S99, S100, S101, S102, S103, S104, S105, S106, S107, S108, S109, S110, S111, S112, S113, S114, S115, S116, S117, S118, S119, S120, S121, S122, S123, S124, S125, S126, S127, S128, S129, S130, S131, S132, S133, S134, S135, S136, S137, S138, S139, S140, S141, S142, S143, S144, S145, S146, S147, S148, S149, S150, S151, S152, S153, S154, S155, S156, S157, S158, S159, S160, S161, S162, S163, S164, S165, S166, S167, S168, S169, S170, S171, S172, S173, S174, S175, S176, S177, S178, S179, S180, S181, S182, S183, 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NO.	DESCRIPTION	QTY	UNIT
1	RESISTOR	100	PCB
2	CAPACITOR	50	PCB
3	SWITCH	20	PCB
4	DIODE	10	PCB
5	IC	5	PCB
6	RELAY	2	PCB
7	TRANSFORMER	1	PCB
8	CONNECTOR	10	PCB
9	WIRE	100	PCB
10	OTHER	10	PCB



REFERENCE DESIGNATOR CHART

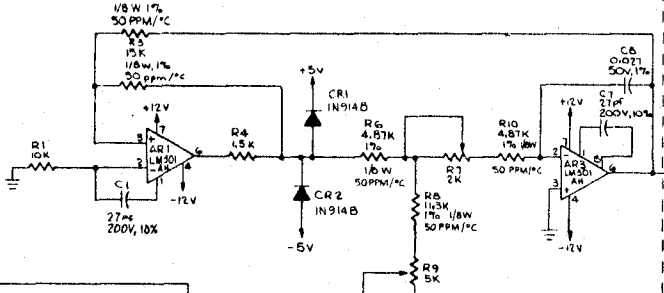
DESIG.	SYM.	UNIT
R1	RES	RESISTOR
C1	CAP	CAPACITOR
S1	SW	SWITCH
D1	DI	DIODE
IC1	IC	IC
REL1	REL	RELAY
TR1	TR	TRANSFORMER
CON1	CON	CONNECTOR
W1	W	WIRE
OT1	OT	OTHER

NO.	DESCRIPTION	QTY	UNIT
1	RESISTOR	100	PCB
2	CAPACITOR	50	PCB
3	SWITCH	20	PCB
4	DIODE	10	PCB
5	IC	5	PCB
6	RELAY	2	PCB
7	TRANSFORMER	1	PCB
8	CONNECTOR	10	PCB
9	WIRE	100	PCB
10	OTHER	10	PCB

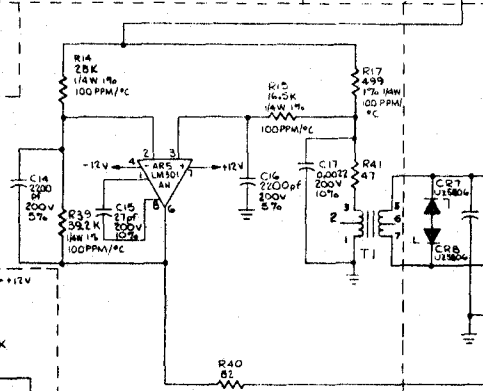
C-17

Diagram

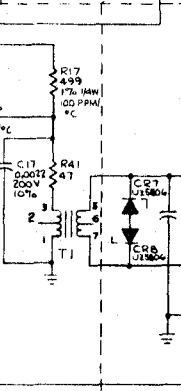
TRIANGULAR WAVE OSCILLATOR



TRANSMITTER LOW PASS FILTER



TRANSMITTER OUTPUT DRIVER



REFERENCE REGULATOR



NOTES:
 UNLESS OTHERWISE SPECIFIED:
 1. RESISTORS ARE 1/4W ± 5%
 2. CAPACITANCE VALUES ARE IN MICROFARADS
 3. RESISTANCE VALUES ARE IN OHMS
 4. CR4/CR5 & CR14/CR15 ARE 1% VOLTAGE MATCHED ZENER DIODE PAIRS (P/N 244547-0001)

REVISIONS

REV	DESCRIPTION	DATE	BY
A	572920(D) T. Collins 7/11/72 ON SH 1, DELETED 'REQUEST TO SEND/CLEAR TO SEND DELAY'. ON CR4 & CR5 'SEE NOTE 4' WAS 'SEE NOTE 2'. C14 & C16 WERE 2200M, 100V, 5%. T1-5, 6, 7 WERE T1-7S, 6. ON 'REV' DESIGN - ADD R19 THRU R28, Q1, Q2, Q3, C2, CR6, AR2 TO NOT USED ON SH 2, ADDED 'DISCRIMINATOR', ADDED PIN 2 TO AR16, REVERSED POLARITY OF CR20. ON CR14 & CR15 - 'SEE NOTE 4' WAS 'SEE NOTE 1'.		
B	98069(D) 2/25/73 P. 2A79 W. 2/21/73 ON SHEET 1 AREA C-3 REVERSED PINS 5 & 7 AND 1 & 3 ON TRANSFORMER		

FORMAL RELEASE

REFERENCE DESIGNATORS	USED	NOT USED
R1 THRU R15	R16, R18 THRU R28	
R17 THRU R18	R19, R20, R21	
Q1 THRU Q3	Q4, Q5, Q6	
C1 THRU C7	C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100	
CR1 THRU CR2	CR3, CR4, CR5	
AR1 THRU AR2	AR3	
T1		
TP1 THRU TP3		

UNLESS OTHERWISE SPECIFIED:

DESIGNER: []

DATE: []

PROCESSED: []

NO. []

REV. []

DATE: []

BY: []

DESCRIPTION: []

VENDOR PART NUMBER: []

TECHNICAL DRAWING

DATE: []

BY: []

DESCRIPTION: []

VENDOR PART NUMBER: []

DIAGRAM, ELECTRONIC SCHEMATIC

MODERN ATL

700 AEE

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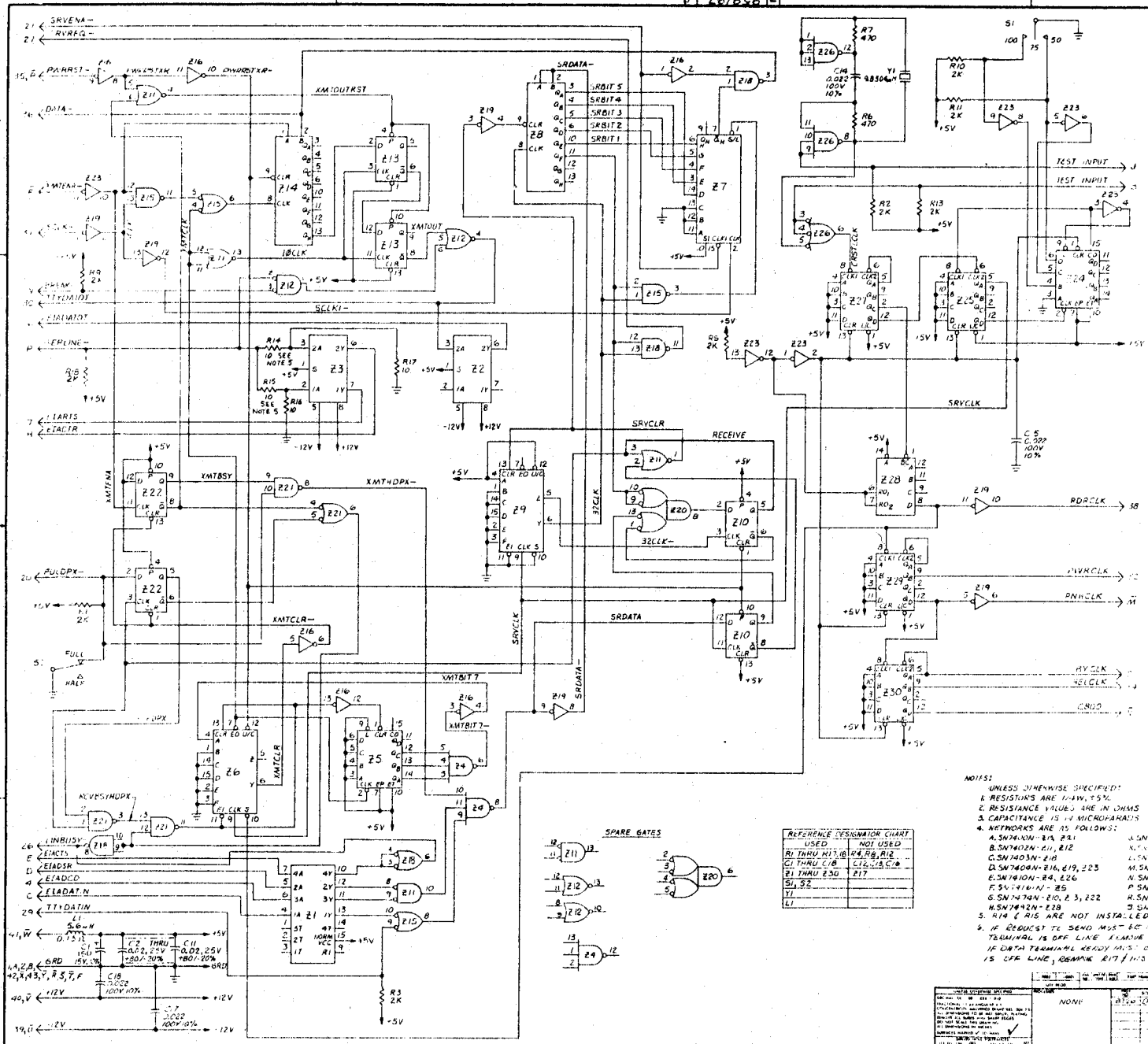
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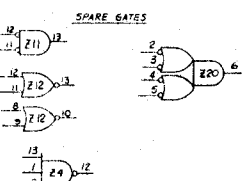
C18

C-20



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- NOTES:
- UNLESS OTHERWISE SPECIFIED: 1. RESISTORS ARE 1/4W, 5%. 2. RESISTANCE VALUES ARE IN OHMS 3. CAPACITANCE IS IN MICROFARADS 4. NETWORKS ARE AS FOLLOWS:
- | | | | | | | | | |
|----------------------|----------------------|----------------------|----------------------------|----------------------|---------------------------------|---------------------------|------------------|------------------|
| A. SN7400N - 2A, 21 | B. SN7402N - 41, 212 | C. SN7403N - 218 | D. SN7400N - 216, 219, 223 | E. SN7410N - 24, 226 | F. SN7410N - 25 | G. SN7410N - 210, 23, 222 | H. SN7412N - 228 | |
| I. SN7410N - 214, 21 | J. SN7412N - 224 | K. SN7414N - 18, 212 | L. SN7414N - 27 | M. SN7414N - 225 | N. SN7414N - 226, 227, 229, 231 | O. SN7414N - 22 | P. SN7414N - 221 | Q. SN7414N - 220 |
- IN REQUEST TO SEND MESSAGES TO THIS TERMINAL IS OFF LINE, PLEASE OR 1-800-333-1111
 - IF DATA TERMINAL READY (M.S. 00) PULSES WHEN TERMINAL IS OFF LINE, REMARK R17 IS INSTALLED. R14.



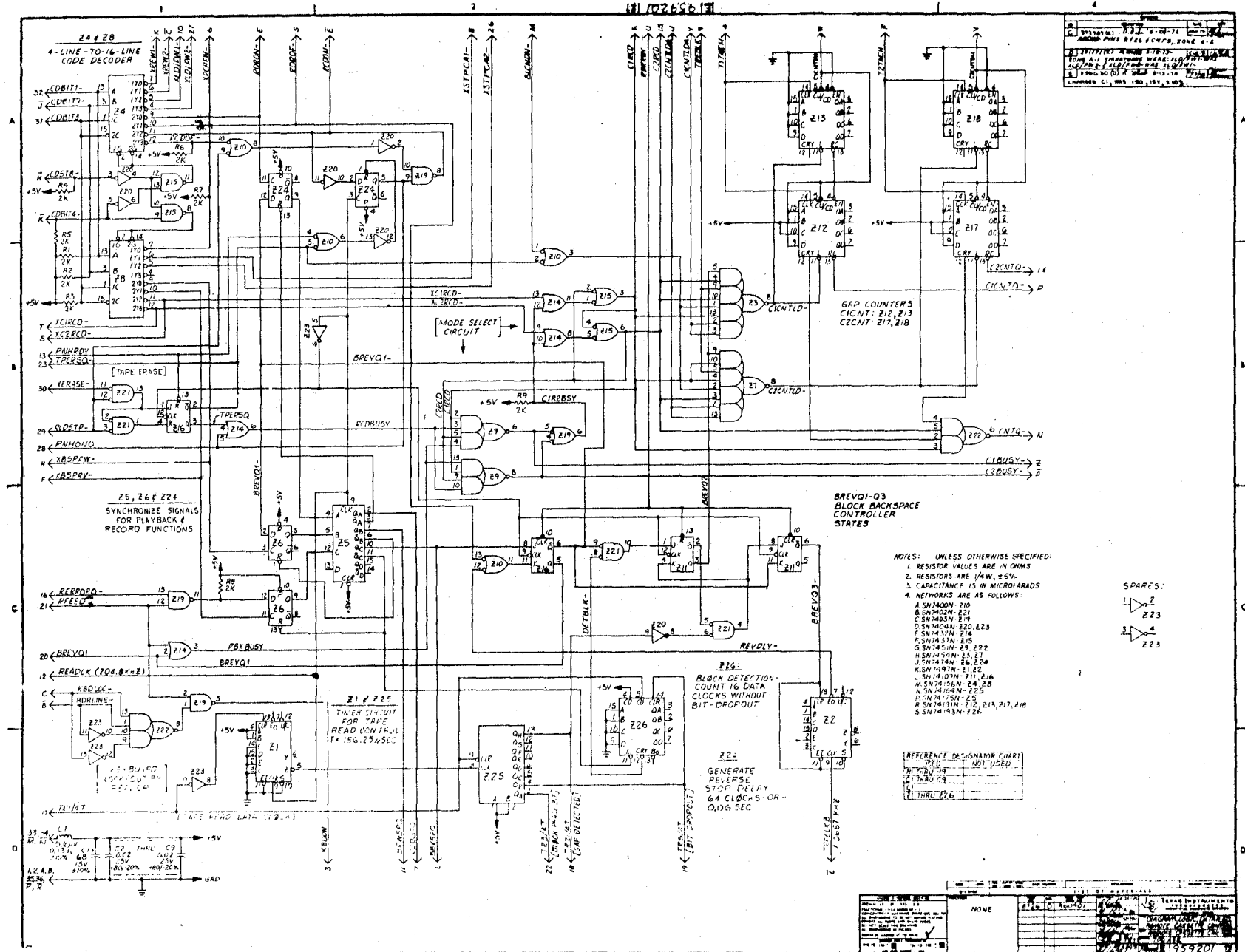
REFERENCE DESIGNATOR CHART

USED	NOT USED
R1 THRU R17	R4, R8, R12
C1 THRU C10	C12, C15, C16
Z1 THRU Z20	Z17
S1, S2	
Y1	

DATE	BY	REVISION	DESCRIPTION
10/12/73
...

939/92

Remote Cassette Control



C-22

SPARE DATA
10 23
2 20

NOTES: UNLESS OTHERWISE SPECIFIED:
1. RESISTANCE VALUES ARE IN OHMS
2. ALL RESISTORS ARE 1/4W, 5%
3. CAPACITANCE IS IN MICROFARADS

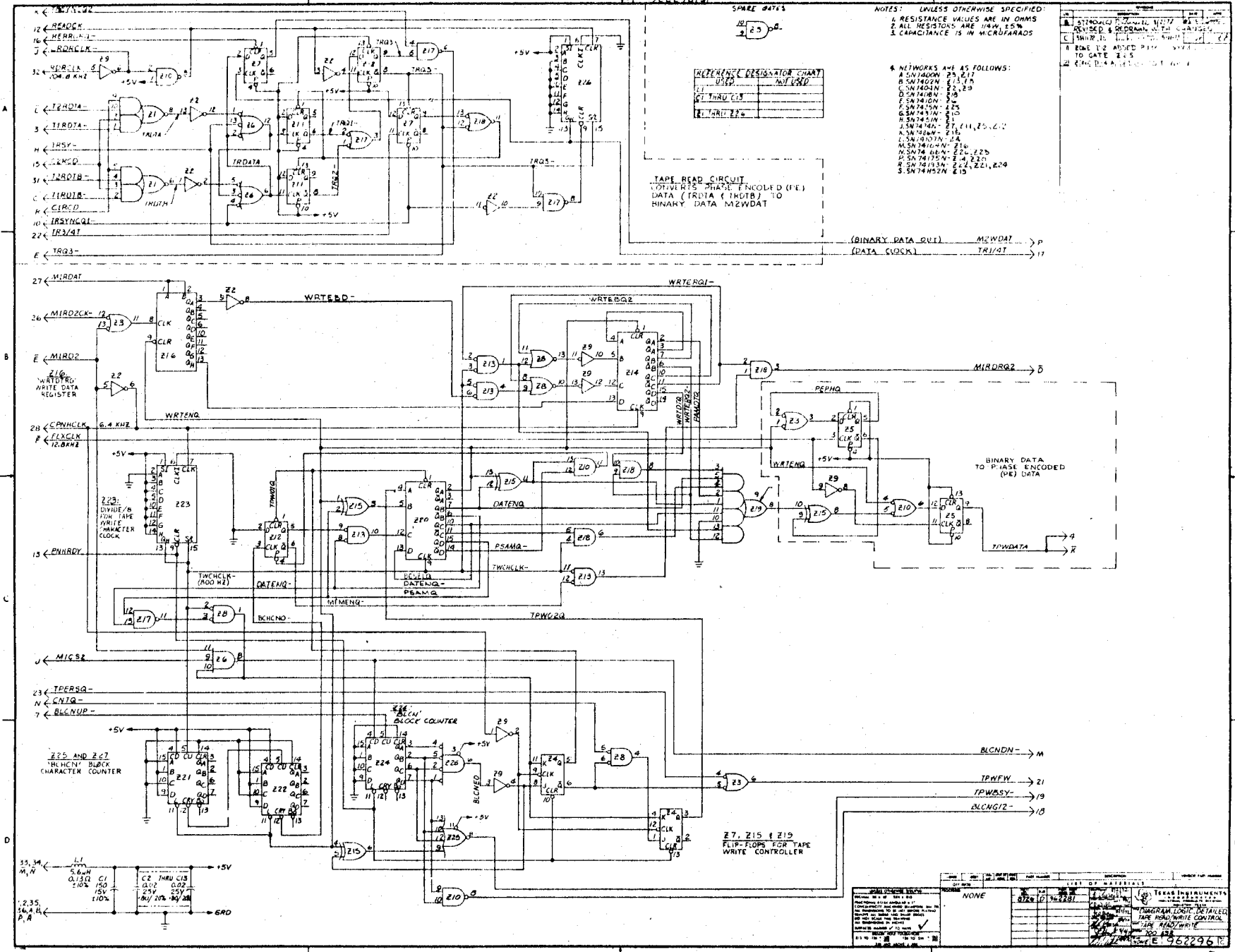
REV	DATE	DESCRIPTION
1		STANDARD DRAWING WITH REVISIONS
2		REVISED PROGRAM WITH CHANGES
3		REVISION TO GATE 205
4		REVISION TO GATE 205
5		REVISION TO GATE 205

INDEPENDENT DESIGNATOR COUNT	
11	101
12	102
13	103
14	104
15	105
16	106
17	107
18	108
19	109
20	110
21	111
22	112
23	113
24	114
25	115
26	116
27	117
28	118
29	119
30	120

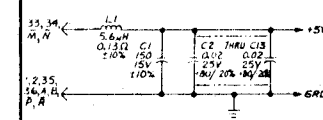
4. NETWORKS ARE AS FOLLOWS:
- A. S17400N 25, 217
 - B. S17402N 2, 17
 - C. S17404N 22, 23
 - D. S17406N 20
 - E. S17410N 20
 - F. S17415N 125
 - G. S17416N 210
 - H. S17417N 21
 - I. S17418N 27, 111, 25, 202
 - J. S17419N 218
 - K. S17420N 24
 - L. S17421N 216
 - M. S17422N 222, 221, 224
 - N. S17423N 213
 - O. S17424N 219

TAPE READ CIRCUIT
CONVERTS PHASE ENCODED (PE)
DATA (TR31A & TR31B) TO
BINARY DATA M2WDAT

(BINARY DATA OUT) M2WDAT
(DATA CLOCK) TR31A/T



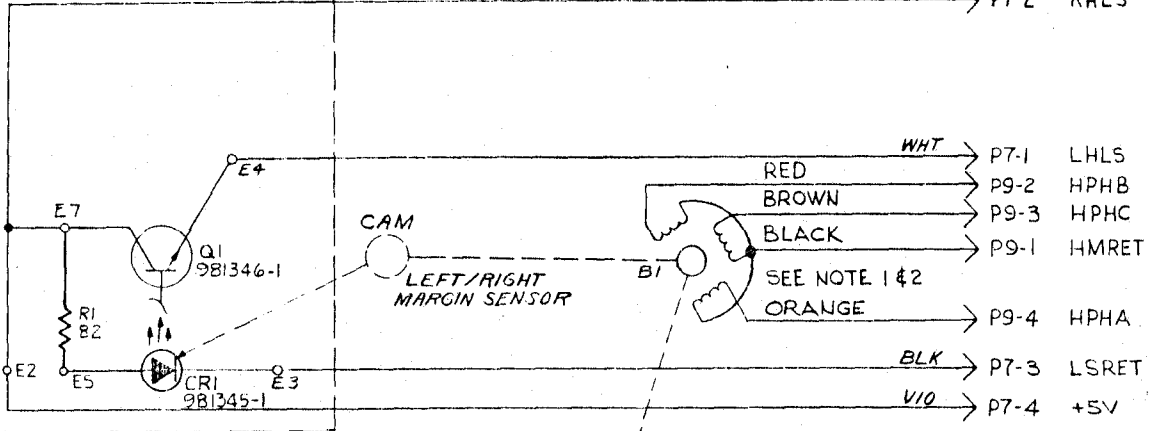
C28



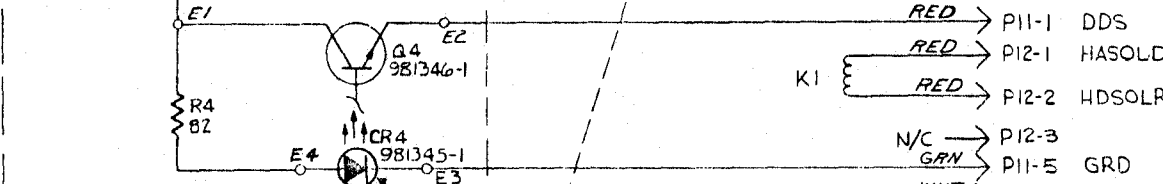
Z7, Z15 & Z19
FLIP-FLOPS FOR TAPE
WRITE CONTROLLER

REV	DATE	DESCRIPTION
1		STANDARD DRAWING WITH REVISIONS
2		REVISED PROGRAM WITH CHANGES
3		REVISION TO GATE 205
4		REVISION TO GATE 205
5		REVISION TO GATE 205

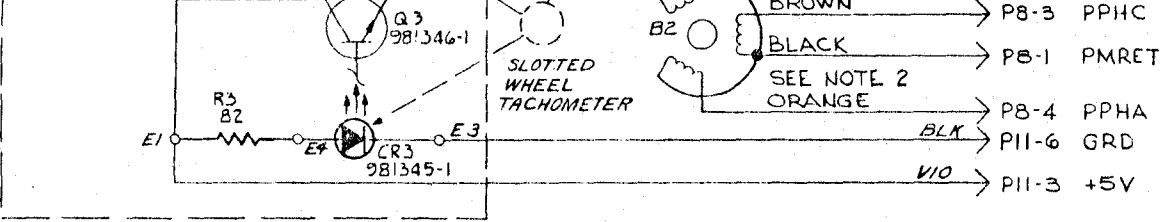
LIMIT SWITCH ASSY
959419-001



SENSOR BLOCK SUBASSY
959427-002



SENSOR BLOCK SUBASSY
959427-001



REVISIONS			
LT#	DESCRIPTION	DATE	APP#
1	380685 (B) 2 PAGES 5-19-73	5/19/73	8/3008
1) Q1 THRU Q4 WERE "CLT-2160"			
2) DELETED R1 THRU R4 (WERE 75Ω, 1/4 W, 1%)			
3) DELETED NOTES 3 & 4.			
4) D51 WAS CR2, D52 WAS CR1, D53 WAS CR3, D54 WAS CR4			
5) ADDED: E7			
B	307410 (D) 11-19-74	11/19/74	1/2008
1) BOMBS ADDED: DELETED Q4, D52, E1, E2 AND E6 FROM LIMIT SWITCH ASSY			
C	403405 (C) 11-19-74	11/19/74	1/2008
1) ADDED NOTES 3 & 4. (2) CHG ASA 7153 WAS CM6833			
3) ADDED E2, RESISTORS BETWEEN E5 & E7, BETWEEN E1 & E4 ZONE C-1, AND BETWEEN E1 & E4 ZONE D-1. 4. DELETE CONNECTION BETWEEN E2 AND E5.			
D	403591 (D) 11-19-75	11/19/75	1/2008
1) VALUES FOR RESISTORS BETWEEN E5 & E7 AND E1 & E4 (2 PLACES) WAS 21Ω.			
E	403498 (B) 1-27-75	1/27/75	1/2008
1. NOTE 4 CHG .25W WAS SW 2 ADDED SHEET 2. 3 ON SH 1 CHG THE FOLLOWING R1 WAS 22Ω, Q1 WAS TIL B1, CR1 WAS D51-CM6833, R4 WAS 22Ω, Q4 WAS TIL B1, CR4 WAS D54-ASA 7153, R3 WAS 22Ω. Q3 WAS TIL B1. CR3 WAS D53-CM6833.			
F	392124 (D) 5-9-75	5/9/75	1/2008
ADDED NOTE 5.			

NOTES:
1 FOR CLOCKWISE ROTATION STEPPING MODE, FOLLOW SEQUENCE ORANGE, RED AND BROWN
2 FOR CCW ROTATION SLEW OR PAPER ADVANCE MODE, FOLLOW SEQUENCE ORANGE, BROWN AND RED
3. RESISTOR VALUES ARE IN OHMS
4. RESISTORS ARE 1/4 W, 1%
5. ON SOME UNITS, Q1 & CR1, Q3 & CR3, AND/OR Q4 & CR4 ARE REPLACED WITH OPTICAL SWITCH, TI P/N 986355-0001

C-30

D

UNLESS OTHERWISE SPECIFIED		PROCESSING		LIST OF MATERIALS		TECHNICAL INFORMATION	
DECIMAL XX ± .00	XXX ± .010	FRAC. XX ± .001	XXX ± .010	QTY REQD	UNIT OF MEAS	PART NUMBER	DESCRIPTION
CONCENTRICITY MACHINED DIAMETERS .004 TIR <td colspan="2">NONE</td> <td>8726</td> <td>E</td> <td>959391</td> <td>DRIVE MECHANISM</td>		NONE		8726	E	959391	DRIVE MECHANISM
ALL DIMENSIONS TO BE MET BEFORE PLATING							700 ASR
REMOVE ALL BURRS AND SHARP EDGES							962299
DO NOT SCALE THIS DRAWING							
ALL DIMENSIONS IN INCHES							
SURFACES MARKED ✓ TO HAVE							
UNFILED HOLE TOLERANCES							
.013 TO .136 ± .003							
.136 TO .250 ± .005							
.250 AND ABOVE ± .008							

TEXAS INSTRUMENTS
IN CORPORATION
INDUSTRIAL PRODUCTS DIVISION
HOUSTON, TEXAS

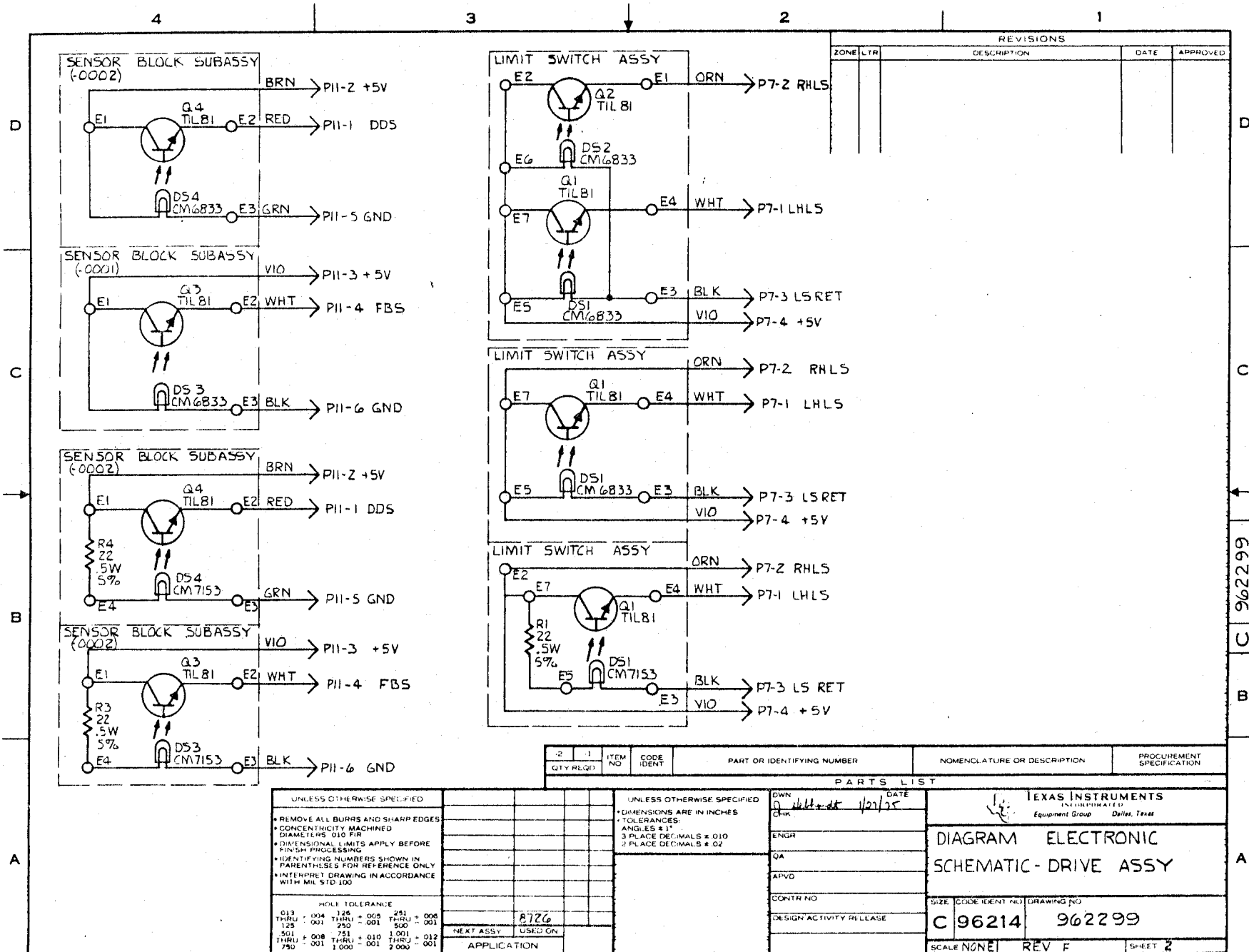
DIAGRAM, ELECTRONIC SCHEMATIC - DRIVE ASSY

UNIT: DRIVE MECHANISM

SCALE: NONE

DATE: 962299

G-31



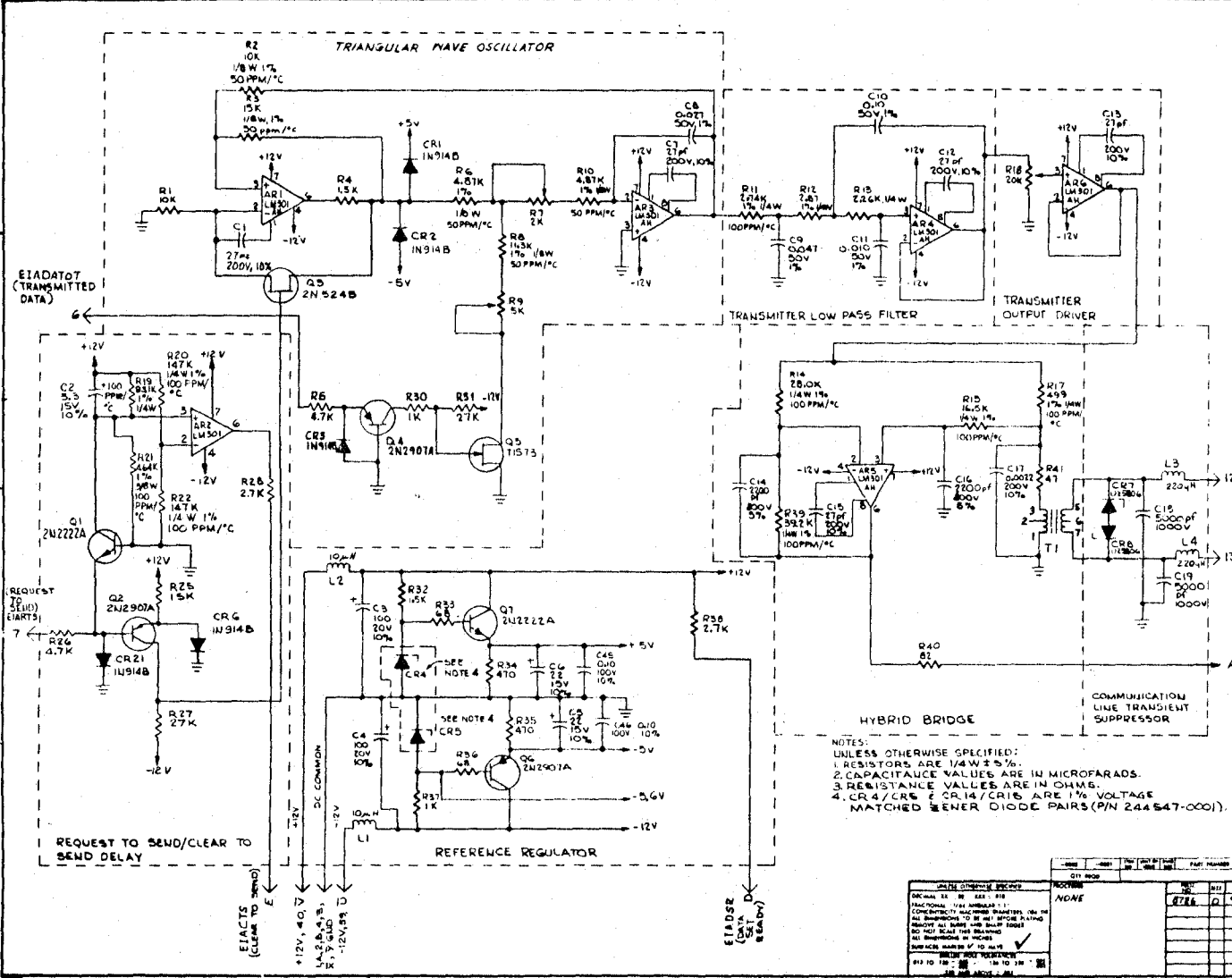
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

2	1	ITEM	CODE	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION
QTY REQD	NO	NO	IDENT			

UNLESS OTHERWISE SPECIFIED • REMOVE ALL BURRS AND SHARP EDGES • CONCENTRICITY MACHINED DIAMETERS .010 FIR • DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING • IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY • INTERPRET DRAWING IN ACCORDANCE WITH MIL STD 100	UNLESS OTHERWISE SPECIFIED • DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° 3 PLACE DECIMALS ± .010 2 PLACE DECIMALS ± .02		DWN DATE 11/27/75	TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas, Texas	
	HOLE TOLERANCE .013 THRU .034 ± .004 .034 THRU .062 ± .005 .062 THRU .125 ± .008 .125 THRU .250 ± .010 .250 THRU .500 ± .015 .500 THRU 1.000 ± .020 1.000 THRU 2.000 ± .030		ENGR QA APVD CONTR NO DESIGN ACTIVITY RELEASE		DIAGRAM ELECTRONIC SCHEMATIC-DRIVE ASSY
	APPLICATION	8726 NEXT ASSY USED ON	SCALE NONE		SIZE CODE IDENT NO DRAWING NO C 96214 962299
	APPLICATION	APPLICATION	REV F		SHEET 2

962299

S



A 572920(D) *Small 10/11*
 ON SH 1 - ADDED R19 TO NOT USED REF DESIGN. DELETED R28. WAS 27K. WAS CONNECTED TO R18. T1-S, L7 WAS T1-T5. C14 & C16 WERE 2200P, 100V, 5%. ON CR4 & CR6 - SEE NOTE 4. WAS 26 NOTE 2.
 ON SH 2 - REVERSED POLARITY OF CR20. ADDED PRU 2 TO AR1. ADDED DISCRIMINATOR. ON CR14 & CR15 - SEE NOTE 4. WAS 26 NOTE 1. CR13 WAS CR18. CR18 WAS CR13.

B 380683 (N) *Small 10/11*
 ON SHEET 1 AREA C3 REVERSED PINS 5, 7 AND 1/3 ON TRANSFORMER

C 382306 (N) *Small 10/11*
 SH2 ZONE A94 B4 ADDED SYMBOL A REF DESIGNATOR CALLOUT TO SHOW C50, C51 & C67. CALLOUT WAS C47 THRU C50 FOR +12V. C62 THRU C76 FOR -12V.

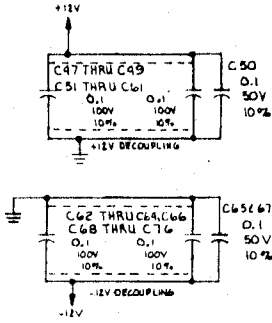
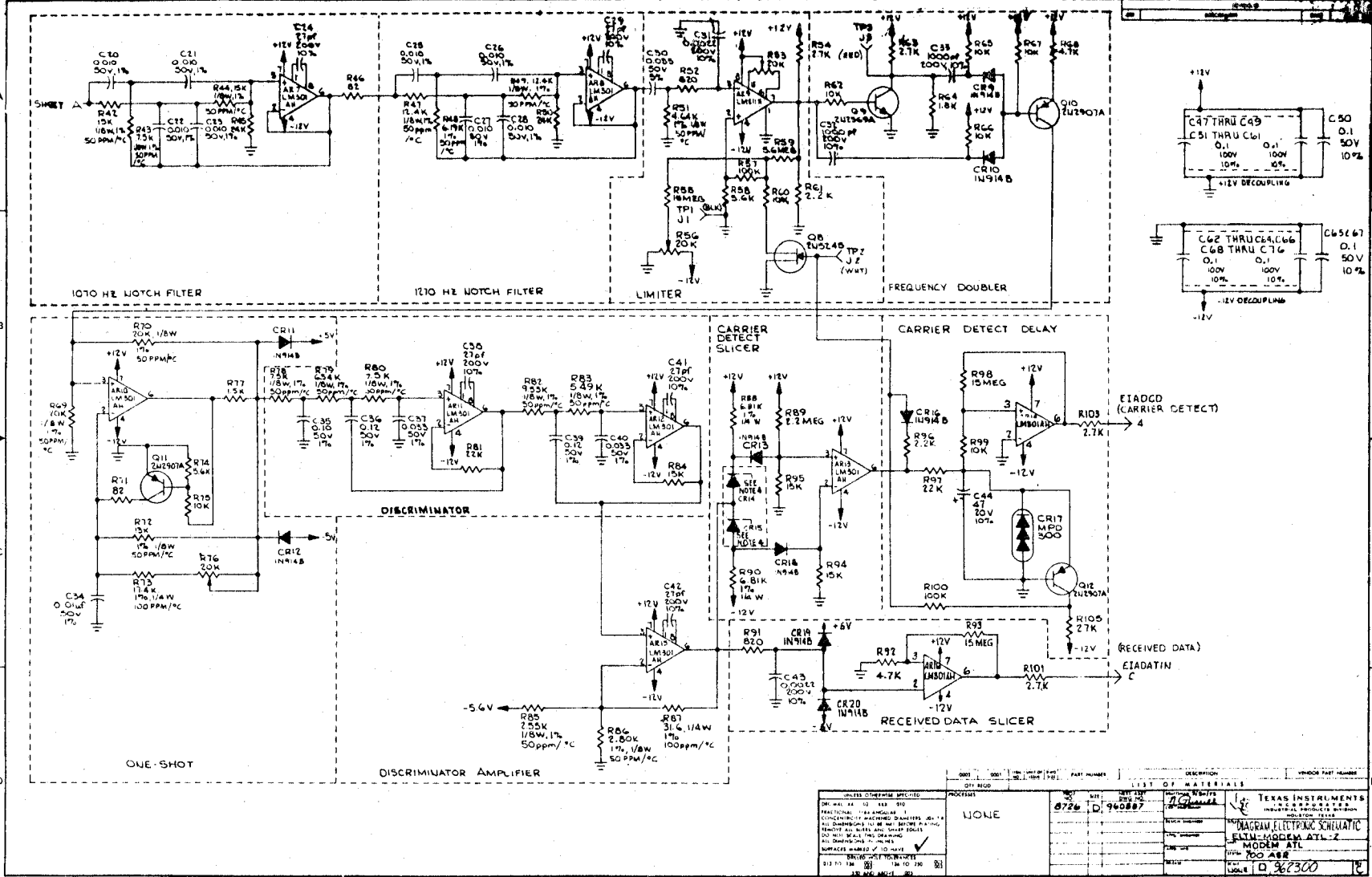
FORMAL RELEASE

REFERENCE DESIGNATORS USED	NOT USED
R1 THRU R15	R16, R23, R24, R25
R17 THRU R18	R102, R104
Q1 THRU Q2	Q77, Q78
C1 THRU C10	
CR1 THRU CR10	
L1 THRU L3	
T1 THRU T2	
J1 THRU J3	

NOTES:
 UNLESS OTHERWISE SPECIFIED:
 1. RESISTORS ARE 1/4W, 5%
 2. CAPACITANCE VALUES ARE IN MICROFARADS.
 3. RESISTANCE VALUES ARE IN OHMS.
 4. CR4 / CR6 & CR14 / CR15 ARE 1% VOLTAGE MATCHED DIODE PAIRS (P/N 244547-000).

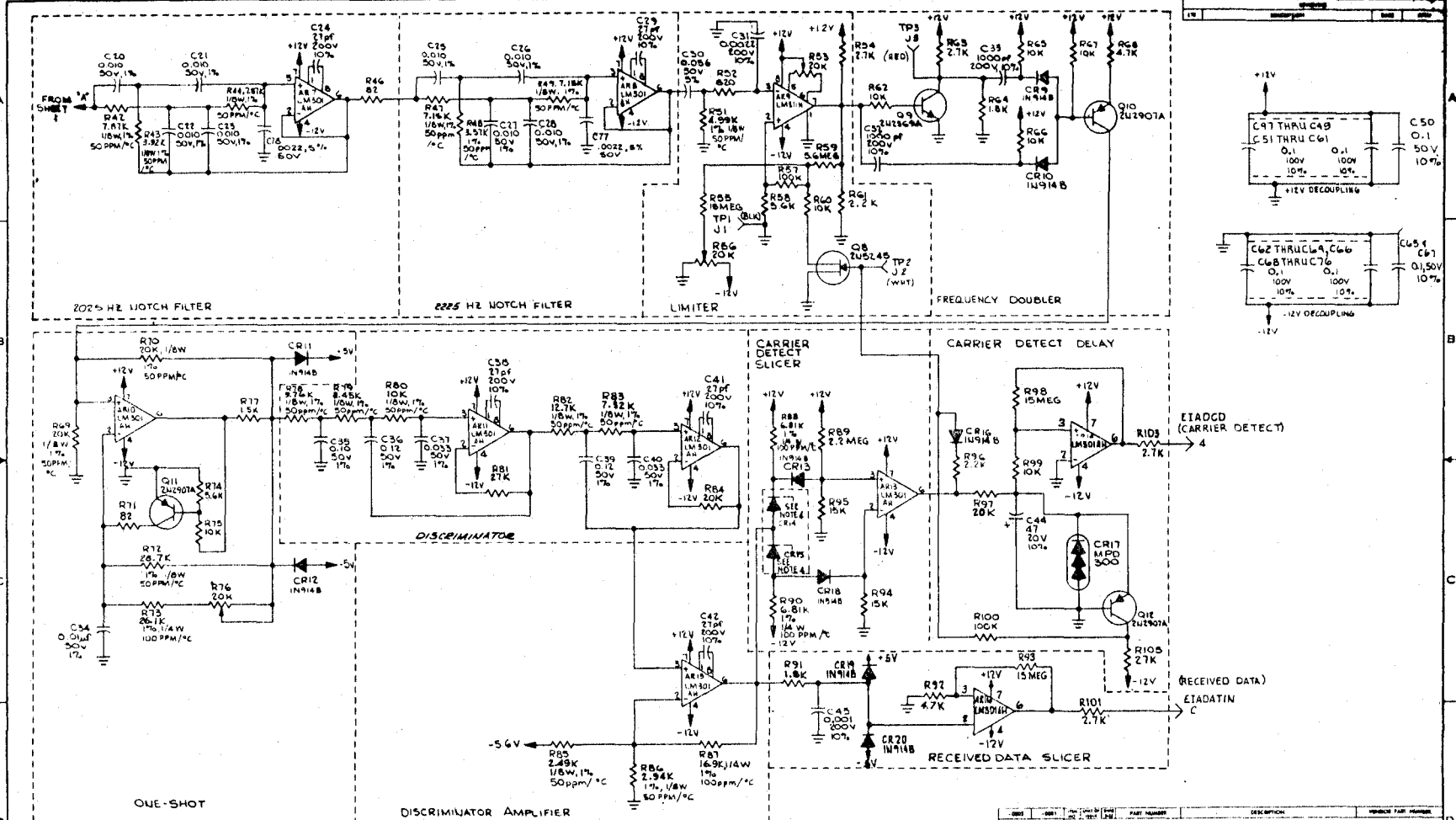
QTY	DESCRIPTION	REVISION	DATE
1	TEXAS INSTRUMENTS		
1	0766 0 76087		
1	DIAGRAM ELECTRONIC SCHEMATIC		
1	FORM 1000 ALL		
1	780 418		
1	362300		

C32



C-33

DESIGN SHEET		PART NUMBER		DESCRIPTION		CHECKED BY	
REV.	DATE	REV.	DATE	REV.	DATE	REV.	DATE
01	11/10/68	01	11/10/68	01	11/10/68	01	11/10/68
TITLE: DIAGRAM ELECTRONIC SCHEMATIC PROJECT: TELEPHONE AT-2 DRAWING NO: MO-200-11 SHEET NO: 2 OF 2		DRAWN BY: W. J. GIBSON CHECKED BY: D. J. GIBSON APPROVED BY: W. J. GIBSON		COMPANY: TEXAS INSTRUMENTS DIVISION: COMMUNICATIONS LOCATION: DAVIDSON, TEXAS		SCALE: 1:1 SHEET: 2 OF 2	



C-35

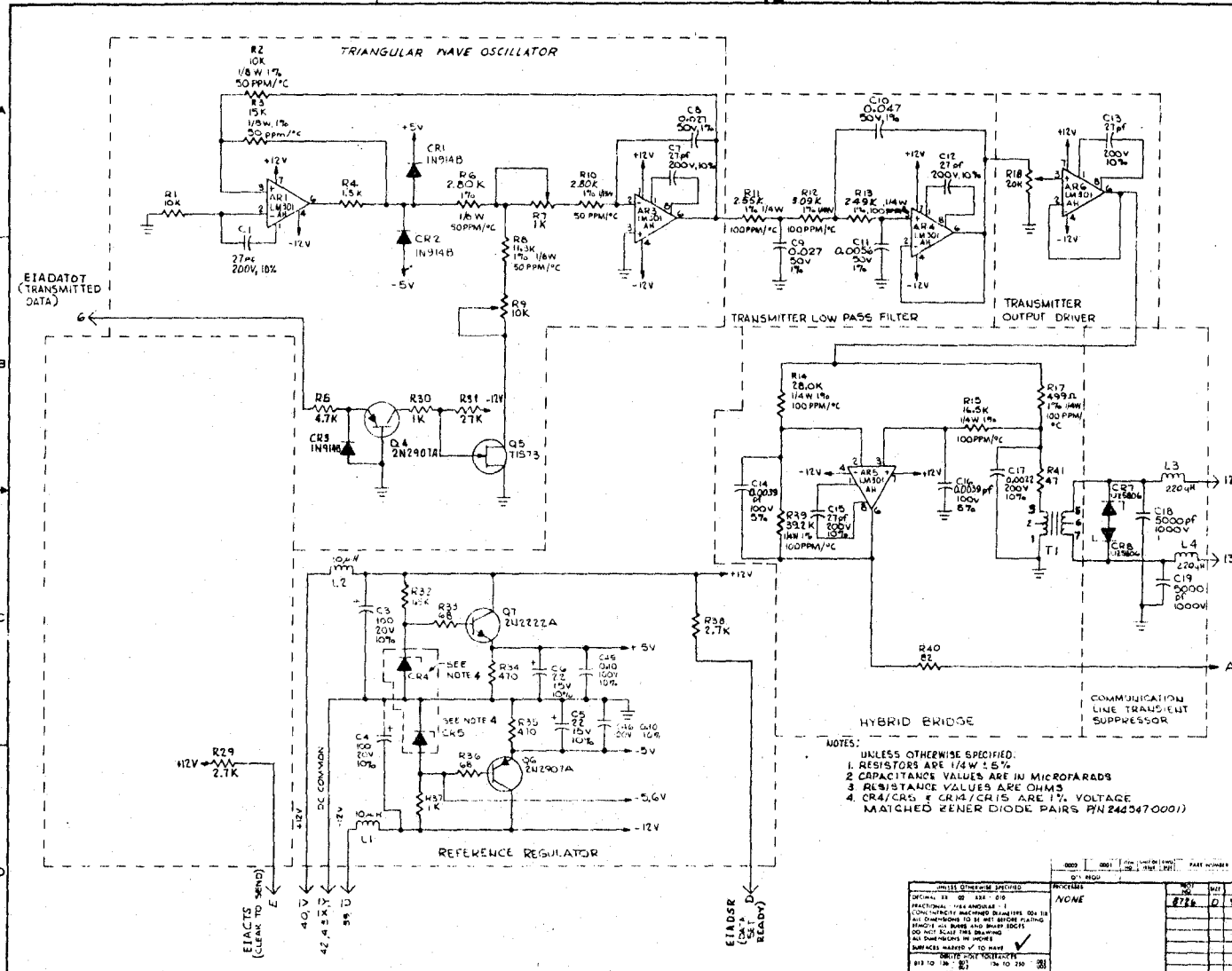
REV	DATE	BY	CHKD	DESCRIPTION	ISSUED BY
0726	9/28/68				

NO.	REV.	DATE	BY	CHKD.	DESCRIPTION
1					

DATE	10/14/68	BY	W. J. B.
TIME	10:30 AM	BY	W. J. B.
DATE	10/14/68	BY	W. J. B.
TIME	10:30 AM	BY	W. J. B.

DATE	10/14/68	BY	W. J. B.
TIME	10:30 AM	BY	W. J. B.

DATE	10/14/68	BY	W. J. B.
TIME	10:30 AM	BY	W. J. B.



17 512920(D) A. G. ...
 ON SH 1 - ON REF DESIGN: ADDED R19 THRU R28, Q1, Q2, Q3, C1, C10, A1 TO NOT USED.
 T1 - 5.0 M7 WAS T1-4.5 G. ON CR4 & CR5 - SEE NOTE 4'S - SEE NOTE 2 - DELETED REQUEST TO SEND CLEAR TO SEND DELAY.
 ON SH 2 - ADDED 'DISCRIMINATOR'. ADDED REF DESIGN: R44. 2225 HZ NOTCH FILTER WAS 1E10 NOTCH FILTER. ADDED PN 2 TO A10.
 REVERSED POLARITY OF CR20 ON CR14 & CR15 - SEE NOTE 4'S - SEE NOTE 1.

FORMAL RELEASE
 B 38063 (A) 75...
 ON SHEET 1, AREA C3 REVERSED PINS 5, 17 AND 18 ON TRANSFORMER
 C 382306 (B) 7...
 SH 2, ZONE A4, Q4, ADDED SYMBOL CR11 DESIGNATOR CR110BT TO SYMBOL C50(C506), CALL OUT WAS C41 THROUGH C4 FOR 12V C60 THROUGH C6 FOR 12V

REFERENCE DESIGNATORS	
USED	NOT USED
R1 THRU R15	R19 THRU R28
R17 THRU R105	R26, R28, R102
C1 THRU C12	C1, C2, C3
C1 THRU C70	C2
C21 THRU C22	CR6, CR21
CR1 THRU CR10	AB2
L1 THRU L4	
T1, THRU T2	
Q1 THRU Q3	

- NOTES:
 1. UNLESS OTHERWISE SPECIFIED.
 2. RESISTOR VALUES ARE 1/4W ± 5%
 3. CAPACITANCE VALUES ARE IN MICROFARADS
 4. RESISTANCE VALUES ARE OHMS
 5. CR4/CR5 & CR14/CR15 ARE 1/2 VOLTAGE MATCHED ZENER DIODE PAIRS (PN2445470001)

UNLESS OTHERWISE SPECIFIED		PART NUMBER		DESCRIPTION		VENDOR PART NO. REF	
QUANTITY	UNIT	REV.	DATE	REV.	DATE	REV.	DATE
NONE		272	0 360887				
SPECIAL INSTRUCTIONS: 1. CONTRACTOR TO MATCH DIMENSIONS ON IN ALL DIMENSIONS TO BE MET BEFORE PLATING. 2. SPECIFIC CALL DIMENSIONS AND SHOWN DIMENSIONS. 3. DO NOT SCALE THE DRAWING. 4. ALL DIMENSIONS IN INCHES. 5. SURFACES MARKED ✓ TO HAVE FINISH TO SPECIFICATION. 6. DIMENSIONS IN INCHES TO 250.				LIST OF MATERIALS 1. TEXAS INSTRUMENTS 2. ... 3. ... 4. ... 5. ... 6. ... 7. ... 8. ... 9. ... 10. ... 11. ... 12. ... 13. ... 14. ... 15. ... 16. ... 17. ... 18. ... 19. ... 20. ... 21. ... 22. ... 23. ... 24. ... 25. ... 26. ... 27. ... 28. ... 29. ... 30. ... 31. ... 32. ... 33. ... 34. ... 35. ... 36. ... 37. ... 38. ... 39. ... 40. ... 41. ... 42. ... 43. ... 44. ... 45. ... 46. ... 47. ... 48. ... 49. ... 50. ... 51. ... 52. ... 53. ... 54. ... 55. ... 56. ... 57. ... 58. ... 59. ... 60. ... 61. ... 62. ... 63. ... 64. ... 65. ... 66. ... 67. ... 68. ... 69. ... 70. ... 71. ... 72. ... 73. ... 74. ... 75. ... 76. ... 77. ... 78. ... 79. ... 80. ... 81. ... 82. ... 83. ... 84. ... 85. ... 86. ... 87. ... 88. ... 89. ... 90. ... 91. ... 92. ... 93. ... 94. ... 95. ... 96. ... 97. ... 98. ... 99. ... 100. ...			

C34

- NOTES: (CONTINUED)
- G. DOT OVER LOGIC SYMBOLS BG AND B13 INDICATES OPEN COLLECTOR NETWORKS.
 - H. REMOVE R8 IF DISCONNECT (HANG UP) OF LINE UPON RECEIPT OF EOT CHARACTER IS NOT DESIRED.
 - I. REMOVE R3 IF LONG SPACE DISCONNECT IS NOT DESIRED.
 - J. REMOVE R9 IF AUTOMATIC TRIGGERING OF ANSWER BACK MEMORY (ABM) IS NOT DESIRED.

- NOTES: UNLESS OTHERWISE SPECIFIED:
- 1. ALL RESISTORS ARE .25 WATT ± 5%
 - 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS
 - 3. ALL RESISTANCE VALUES ARE IN OHMS
 - 4. NETWORKS ARE AS FOLLOWS

- A 7400 - Z10, Z11, Z18
- B 7401N - Z13
- C 7402N - Z16
- D 7403N - Z19
- E 7410N - Z29
- F 7412N - Z24
- G 7474N - Z12
- H 7493N - Z17
- I 74950 - Z1
- J 75154N - Z1
- K 75154N - Z1
- L 74175 - Z1, Z10
- M 74175 - Z1, Z10

THIS CARD IS ASSEMBLED TO OPERATE WITH A DAA SYSTEM AND THE TRIGGERING OF THE ANSWER ONLY MEMORY ABM DELAYED BY 400 MILLISECONDS BY INSTALLED ON BOARD RESISTORS R2 AND R16 RESPECTIVELY FOR OTHER OPTIONS, SEE INTERFACE SECTION CHART AND ABM TRIGGER DELAY CHART.

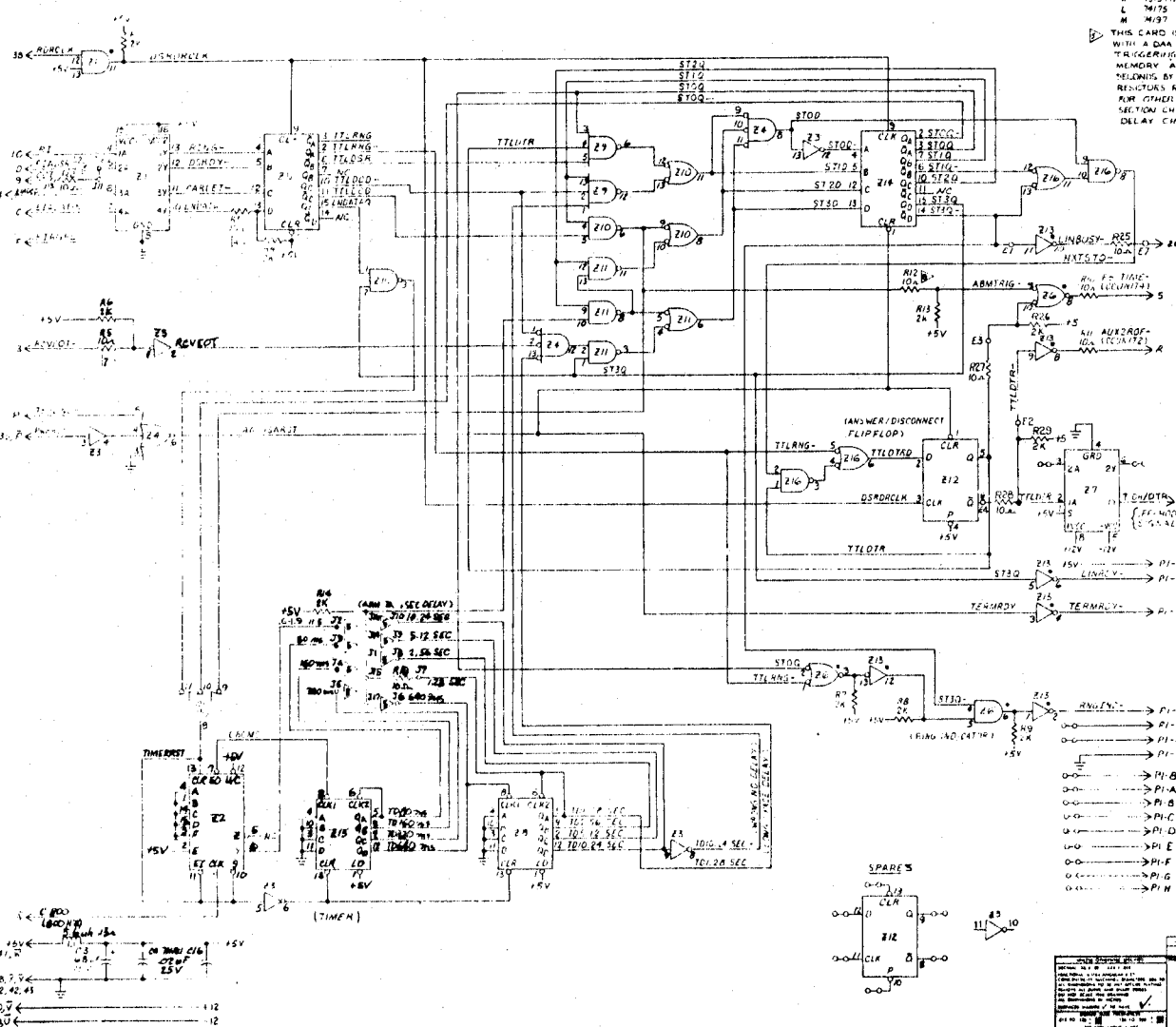
FORMAL RELEASE

CLASSIFICATION: UNCLASSIFIED

DATE: 01/11/2011

BY: 60322 UCBAW/BJS/STP

CONTROL NUMBER: 962100



ABM TRIGGER DELAY CHART

DELAY	RESISTOR	RES. VALUE
10.24 SEC	R12	300 Ω
5.12 SEC	R13	300 Ω
2.56 SEC	R14	300 Ω
1.28 SEC	R15	300 Ω
640 Ω	R16	300 Ω
320 Ω	R17	300 Ω
160 Ω	R18	300 Ω
80 Ω	R19	300 Ω
40 Ω	R20	300 Ω

INTERFACE SELECTION CHART

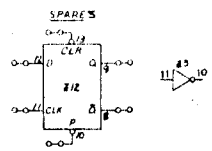
INSTALL RESISTOR	BETWEEN DAA	FOR USE WITH	BELL NO.
R1	J10 C13	OPEN	100A
R2	J10 E11	100A	010N

HIGHEST REFERENCE DESIGNATIONS

Z10	Z11	Z12	Z13	Z14	Z15

REFERENCE DESIGNATIONS NOT USED

Z16	Z17	Z18	Z19	Z20	Z21



TEST INSTRUMENTS

TEST INSTRUMENTS	MODEL NUMBER	DATE
TEST INSTRUMENTS	MODEL NUMBER	DATE

DIAGRAM LOGIC OPTAINED

DATE: 01/11/2011

BY: 60322 UCBAW/BJS/STP

CONTROL NUMBER: 962100

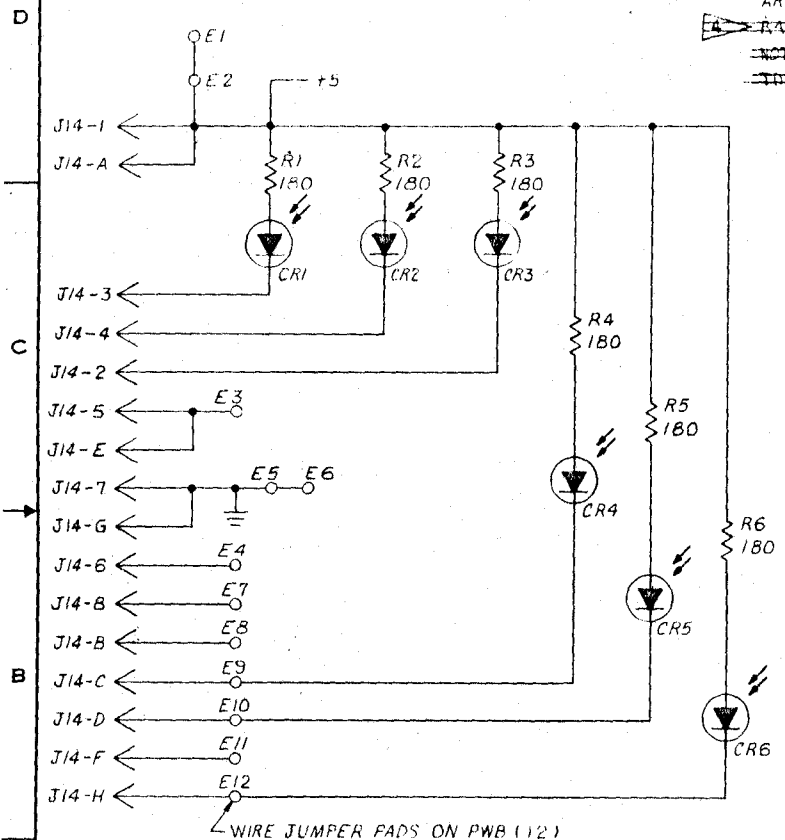
C-39

4 3 2 1

NOTES: UNLESS OTHERWISE SPECIFIED
 1. RESISTANCE VALUES ARE IN OHMS
 2. RESISTORS ARE .25 WATT ± 5 %
 3. ALL LIGHT EMITTING DIODES ARE SL1258

~~4. R4 THRU R6 AND CR4 THRU CR6 NOT USED ON COOL ASSEMBLY TO BE USED FOR FUTURE OPTIONS~~

REVISIONS			
REV	DATE	DESCRIPTION	APPROVED
A	3/5812 (D) 2.4.8.16.0 1/19/73	1) DELETED FLAG NOTE 4 & DOTTED LINE FROM AROUND CR4, 5, 6 AND R4, 5, 6. 2) ADDED 960165-0002 TO PART NUMBER SCHEDULE	



WIRE JUMPER PADS ON PWB (12)

REFERENCE DESIGNATOR CHART	
USED	NOT USED
R1 THRU R6	
CR1 THRU CR6	
E1 THRU E12	

960165-0002	DISPLAY, BLOCK TRANSMISSION	TERMINAL READY	NOT USED	RING INDICATOR	RECEIVE MODE	NOT USED	NOT USED	XMT MODE
960165-0001	DISPLAY AUTO ANSWER	TERMINAL READY	RING INDICATOR	LINE READY	NOT USED	NOT USED	NOT USED	NOT USED
ASSEMBLY NO.	ASSEMBLY DESCRIPTION	CR1	CR2	CR3	CR4	CR5	CR6	

QTY REQD	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION
----------	---------	------------	----------------------------	-----------------------------	---------------------------

UNLESS OTHERWISE SPECIFIED			
• REMOVE ALL BURRS AND SHARP EDGES			
• CONCENTRICITY MACHINED DIAMETERS .010 FIR			
• DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING			
• IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY			
• INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100			
HOLE TOLERANCE			
013 THRU 1.004	178 THRU 1.005	251 THRU 1.006	
125 THRU 1.250	250 THRU 1.500	500 THRU 1.001	
501 THRU 1.008	.751 THRU 1.010	1.001 THRU 1.012	
750 THRU 1.001	1.000 THRU 1.001	2.000 THRU 1.001	
	16016	9726	
	NEXT ASSY	USED ON	
	APPLICATION		

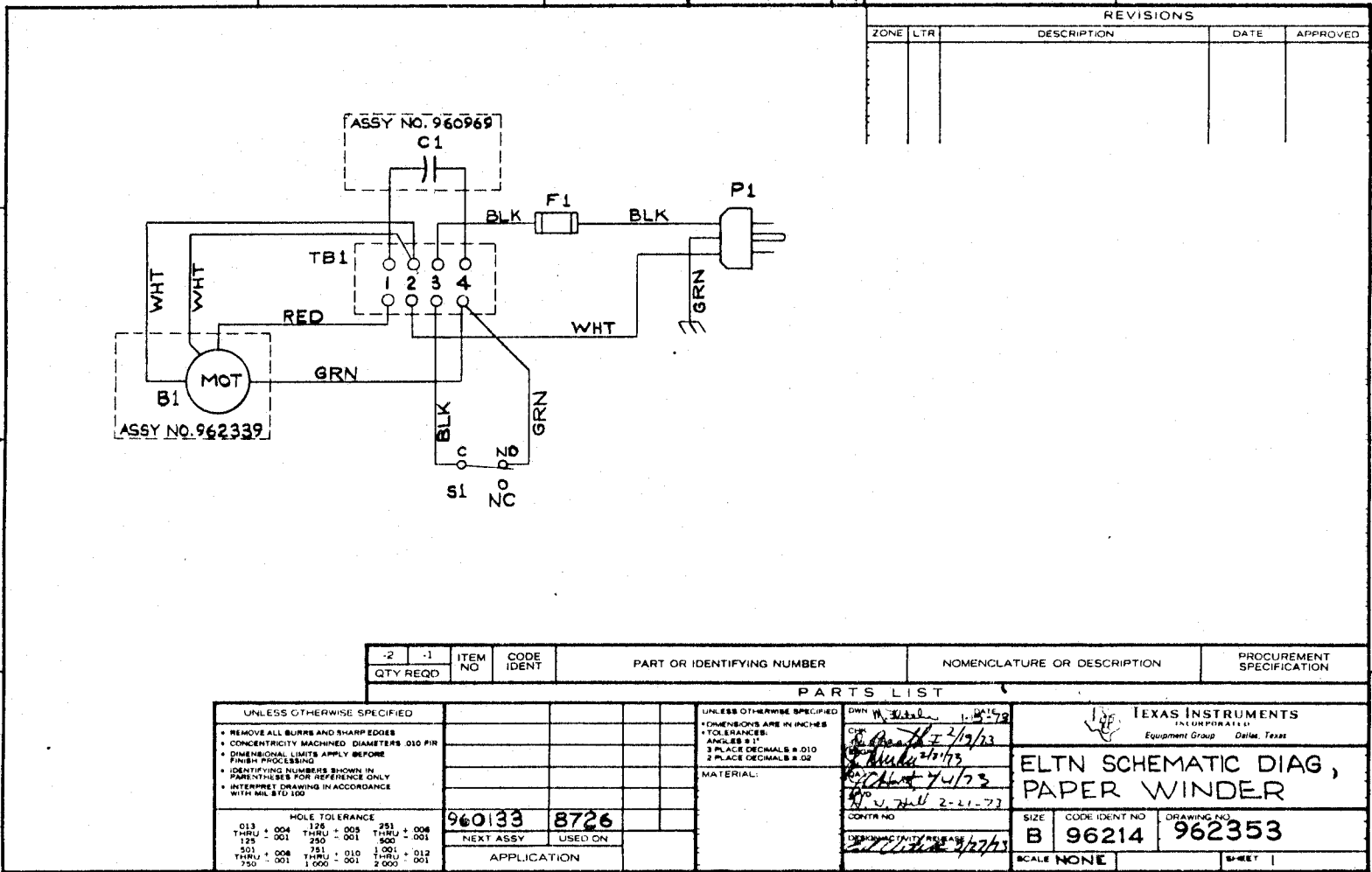
UNLESS OTHERWISE SPECIFIED	
• DIMENSIONS ARE IN INCHES	
• TOLERANCES:	
ANGLES ± 1°	
3 PLACE DECIMALS ± .010	
2 PLACE DECIMALS ± .02	
MATERIAL	
DWN	DATE
CHK	12-19-72
ENGR	3/9/73
QA	3-9-73
APPV	4-1-73
CONTR NO	
DESIGN ACTIVITY RELEASE	
3-22-73	

TEXAS INSTRUMENTS INCORPORATED		
Equipment Group Dallas Texas		
DIAGRAM, LOGIC, DETAILED, OPTION PANEL DISPLAY		
SIZE	CODE IDENT NO	DRAWING NO
C	96214	962308
SCALE NONE	REV A	SHEET 1 OF 1

C40

C 962308

5 4 3 2 1

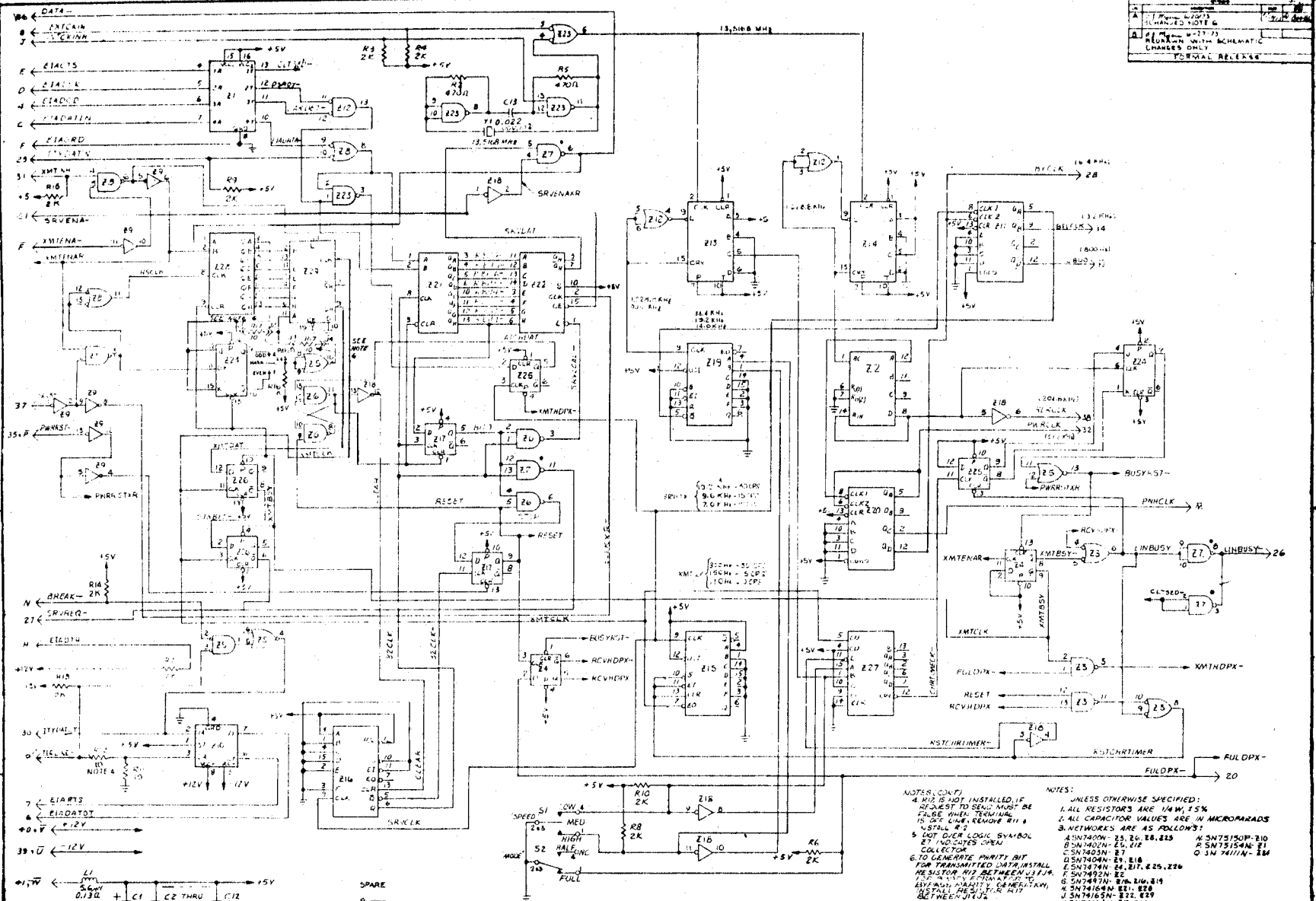


REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

C41

-2	-1	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION
PARTS LIST						
UNLESS OTHERWISE SPECIFIED • REMOVE ALL BURRS AND SHARP EDGES • CONCENTRICITY MACHINED DIAMETERS .010 PIR • DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING • IDENTIFYING NUMBERS SHOWN IN PARENTHESES FOR REFERENCE ONLY • INTERPRET DRAWING IN ACCORDANCE WITH MIL STD 100				UNLESS OTHERWISE SPECIFIED * DIMENSIONS ARE IN INCHES * TOLERANCES: ANGLES ± .1 3 PLACE DECIMALS ± .010 2 PLACE DECIMALS ± .02 MATERIAL:		
HOLE TOLERANCE .013 THRU .125 THRU .251 THRU .500 THRU 1.001 THRU 2.000 .004 .001 .008 .001 .010 .001 .012 .001		960133	8726			
		NEXT ASSY	USED ON			
		APPLICATION				
				DWN M. Eitel 1-21-72 CHK J. Heath 2/19/73 J. Heath 4/1/73 J. Heath 7/1/73 W. V. Hall 2-21-77 CONTR NO DESIGN ACTIVITY RELEASE J. J. Heath 4/27/73	TEXAS INSTRUMENTS INCORPORATED Equipment Group Dallas, Texas	
				ELTN SCHEMATIC DIAG, PAPER WINDER		
		SIZE	CODE IDENT NO	DRAWING NO		
		B	96214	962353		
				SCALE	NONE	
				SHEET		

1	17	204996-1	10/1/73
2	18	204996-2	10/1/73
3	19	204996-3	10/1/73
4	20	204996-4	10/1/73
5	21	204996-5	10/1/73
6	22	204996-6	10/1/73
7	23	204996-7	10/1/73
8	24	204996-8	10/1/73
9	25	204996-9	10/1/73
10	26	204996-10	10/1/73



NOTES (CONT)

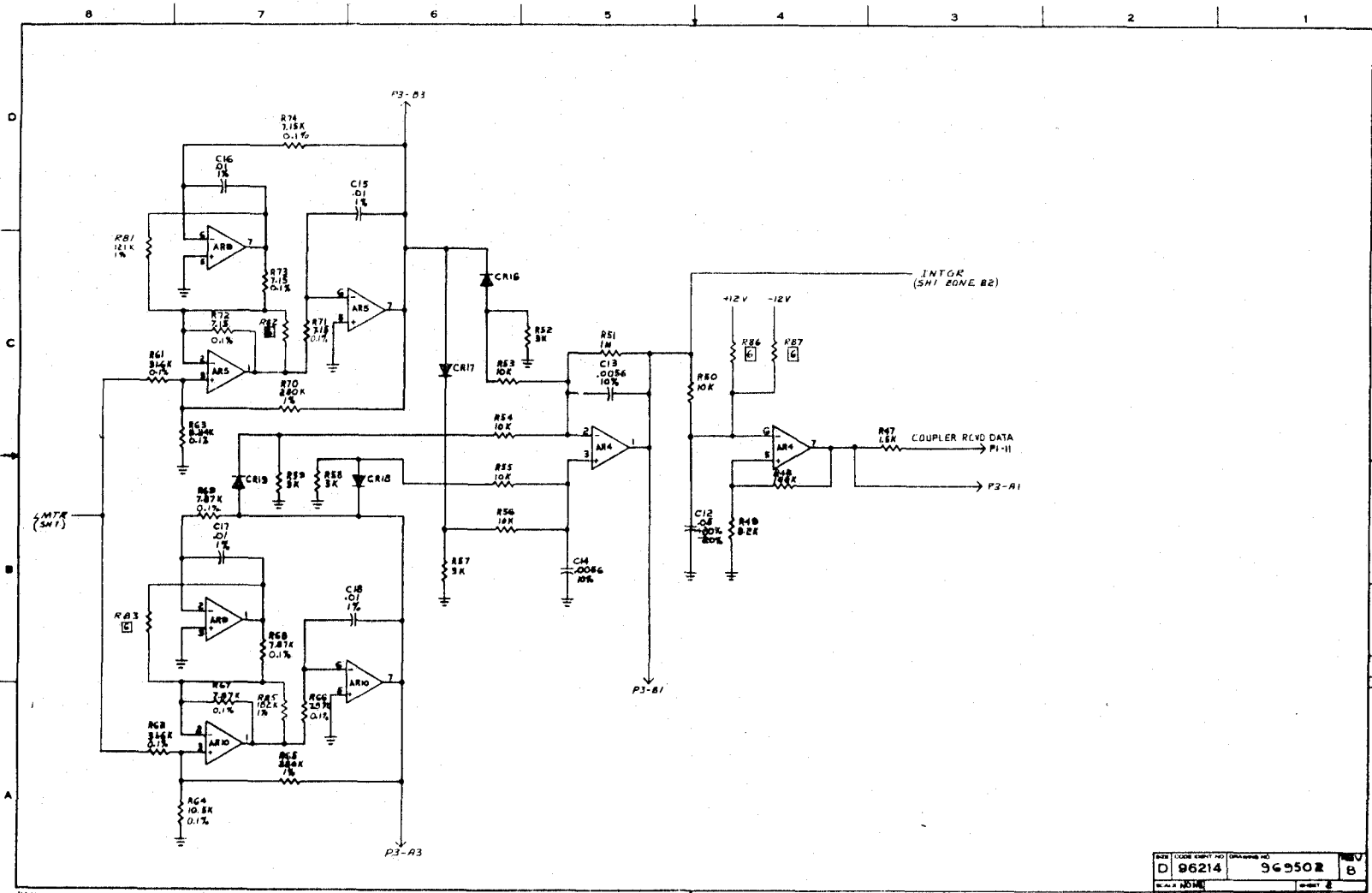
4. WIRE IS NOT INSTALLED IF REQUEST TO SEND MUST BE FALSE WHEN TERMINAL IS SET LOW. REMOVE R11 & INSTALL R2.
5. DOT OVER LOGIC SYMBOL ET INDICATES OPEN COLLECTOR.
6. TO GENERATE PRIORITY BIT FOR TRANSMITTED DATA, INSTALL RESISTOR R12 BETWEEN U17M AND U17N. R12 MUST BE 10K OHMS. R12 MUST BE INSTALLED BETWEEN U17U AND U17V.

NOTES:

1. ALL RESISTORS ARE 1/4W, 1%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. NETWORKS ARE AS FOLLOWS:

1. SN7400N - 25, 26, 28, 225	4. SN7415N - 217, 225, 226
2. SN7401N - 21, 22	5. SN7416N - 218
3. SN7402N - 27	6. SN7417N - 219, 219, 219
4. SN7403N - 28	7. SN7418N - 220
5. SN7404N - 29, 30, 31, 32	8. SN7419N - 221
6. SN7405N - 33, 34	9. SN7420N - 222
7. SN7406N - 35, 36, 37, 38	10. SN7421N - 223
8. SN7407N - 39, 40, 41, 42	11. SN7422N - 224
9. SN7408N - 43, 44, 45, 46	12. SN7423N - 225
10. SN7409N - 47, 48, 49, 50	13. SN7424N - 226
11. SN7410N - 51, 52, 53, 54	14. SN7425N - 227
12. SN7411N - 55, 56, 57, 58	15. SN7426N - 228
13. SN7412N - 59, 60, 61, 62	16. SN7427N - 229
14. SN7413N - 63, 64, 65, 66	17. SN7428N - 230
15. SN7414N - 67, 68, 69, 70	18. SN7429N - 231
16. SN7415N - 71, 72, 73, 74	19. SN7430N - 232
17. SN7416N - 75, 76, 77, 78	20. SN7431N - 233
18. SN7417N - 79, 80, 81, 82	21. SN7432N - 234
19. SN7418N - 83, 84, 85, 86	22. SN7433N - 235
20. SN7419N - 87, 88, 89, 90	23. SN7434N - 236
21. SN7420N - 91, 92, 93, 94	24. SN7435N - 237
22. SN7421N - 95, 96, 97, 98	25. SN7436N - 238
23. SN7422N - 99, 100, 101, 102	26. SN7437N - 239
24. SN7423N - 103, 104, 105, 106	27. SN7438N - 240
25. SN7424N - 107, 108, 109, 110	28. SN7439N - 241
26. SN7425N - 111, 112, 113, 114	29. SN7440N - 242
27. SN7426N - 115, 116, 117, 118	30. SN7441N - 243
28. SN7427N - 119, 120, 121, 122	31. SN7442N - 244
29. SN7428N - 123, 124, 125, 126	32. SN7443N - 245
30. SN7429N - 127, 128, 129, 130	33. SN7444N - 246
31. SN7430N - 131, 132, 133, 134	34. SN7445N - 247
32. SN7431N - 135, 136, 137, 138	35. SN7446N - 248
33. SN7432N - 139, 140, 141, 142	36. SN7447N - 249
34. SN7433N - 143, 144, 145, 146	37. SN7448N - 250
35. SN7434N - 147, 148, 149, 150	38. SN7449N - 251
36. SN7435N - 151, 152, 153, 154	39. SN7450N - 252
37. SN7436N - 155, 156, 157, 158	40. SN7451N - 253
38. SN7437N - 159, 160, 161, 162	41. SN7452N - 254
39. SN7438N - 163, 164, 165, 166	42. SN7453N - 255
40. SN7439N - 167, 168, 169, 170	43. SN7454N - 256
41. SN7440N - 171, 172, 173, 174	44. SN7455N - 257
42. SN7441N - 175, 176, 177, 178	45. SN7456N - 258
43. SN7442N - 179, 180, 181, 182	46. SN7457N - 259
44. SN7443N - 183, 184, 185, 186	47. SN7458N - 260
45. SN7444N - 187, 188, 189, 190	48. SN7459N - 261
46. SN7445N - 191, 192, 193, 194	49. SN7460N - 262
47. SN7446N - 195, 196, 197, 198	50. SN7461N - 263
48. SN7447N - 199, 200, 201, 202	51. SN7462N - 264
49. SN7448N - 203, 204, 205, 206	52. SN7463N - 265
50. SN7449N - 207, 208, 209, 210	53. SN7464N - 266
51. SN7450N - 211, 212, 213, 214	54. SN7465N - 267
52. SN7451N - 215, 216, 217, 218	55. SN7466N - 268
53. SN7452N - 219, 220, 221, 222	56. SN7467N - 269
54. SN7453N - 223, 224, 225, 226	57. SN7468N - 270
55. SN7454N - 227, 228, 229, 230	58. SN7469N - 271
56. SN7455N - 231, 232, 233, 234	59. SN7470N - 272
57. SN7456N - 235, 236, 237, 238	60. SN7471N - 273
58. SN7457N - 239, 240, 241, 242	61. SN7472N - 274
59. SN7458N - 243, 244, 245, 246	62. SN7473N - 275
60. SN7459N - 247, 248, 249, 250	63. SN7474N - 276
61. SN7460N - 251, 252, 253, 254	64. SN7475N - 277
62. SN7461N - 255, 256, 257, 258	65. SN7476N - 278
63. SN7462N - 259, 260, 261, 262	66. SN7477N - 279
64. SN7463N - 263, 264, 265, 266	67. SN7478N - 280
65. SN7464N - 267, 268, 269, 270	68. SN7479N - 281
66. SN7465N - 271, 272, 273, 274	69. SN7480N - 282
67. SN7466N - 275, 276, 277, 278	70. SN7481N - 283
68. SN7467N - 279, 280, 281, 282	71. SN7482N - 284
69. SN7468N - 283, 284, 285, 286	72. SN7483N - 285
70. SN7469N - 287, 288, 289, 290	73. SN7484N - 286
71. SN7470N - 291, 292, 293, 294	74. SN7485N - 287
72. SN7471N - 295, 296, 297, 298	75. SN7486N - 288
73. SN7472N - 299, 300, 301, 302	76. SN7487N - 289
74. SN7473N - 303, 304, 305, 306	77. SN7488N - 290
75. SN7474N - 307, 308, 309, 310	78. SN7489N - 291
76. SN7475N - 311, 312, 313, 314	79. SN7490N - 292
77. SN7476N - 315, 316, 317, 318	80. SN7491N - 293
78. SN7477N - 319, 320, 321, 322	81. SN7492N - 294
79. SN7478N - 323, 324, 325, 326	82. SN7493N - 295
80. SN7479N - 327, 328, 329, 330	83. SN7494N - 296
81. SN7480N - 331, 332, 333, 334	84. SN7495N - 297
82. SN7481N - 335, 336, 337, 338	85. SN7496N - 298
83. SN7482N - 339, 340, 341, 342	86. SN7497N - 299
84. SN7483N - 343, 344, 345, 346	87. SN7498N - 300
85. SN7484N - 347, 348, 349, 350	88. SN7499N - 301
86. SN7485N - 351, 352, 353, 354	89. SN7500N - 302
87. SN7486N - 355, 356, 357, 358	90. SN7501N - 303
88. SN7487N - 359, 360, 361, 362	91. SN7502N - 304
89. SN7488N - 363, 364, 365, 366	92. SN7503N - 305
90. SN7489N - 367, 368, 369, 370	93. SN7504N - 306
91. SN7490N - 371, 372, 373, 374	94. SN7505N - 307
92. SN7491N - 375, 376, 377, 378	95. SN7506N - 308
93. SN7492N - 379, 380, 381, 382	96. SN7507N - 309
94. SN7493N - 383, 384, 385, 386	97. SN7508N - 310
95. SN7494N - 387, 388, 389, 390	98. SN7509N - 311
96. SN7495N - 391, 392, 393, 394	99. SN7510N - 312
97. SN7496N - 395, 396, 397, 398	100. SN7511N - 313
98. SN7497N - 399, 400, 401, 402	101. SN7512N - 314
99. SN7498N - 403, 404, 405, 406	102. SN7513N - 315
100. SN7499N - 407, 408, 409, 410	103. SN7514N - 316
101. SN7500N - 411, 412, 413, 414	104. SN7515N - 317
102. SN7501N - 415, 416, 417, 418	105. SN7516N - 318
103. SN7502N - 419, 420, 421, 422	106. SN7517N - 319
104. SN7503N - 423, 424, 425, 426	107. SN7518N - 320
105. SN7504N - 427, 428, 429, 430	108. SN7519N - 321
106. SN7505N - 431, 432, 433, 434	109. SN7520N - 322
107. SN7506N - 435, 436, 437, 438	110. SN7521N - 323
108. SN7507N - 439, 440, 441, 442	111. SN7522N - 324
109. SN7508N - 443, 444, 445, 446	112. SN7523N - 325
110. SN7509N - 447, 448, 449, 450	113. SN7524N - 326
111. SN7510N - 451, 452, 453, 454	114. SN7525N - 327
112. SN7511N - 455, 456, 457, 458	115. SN7526N - 328
113. SN7512N - 459, 460, 461, 462	116. SN7527N - 329
114. SN7513N - 463, 464, 465, 466	117. SN7528N - 330
115. SN7514N - 467, 468, 469, 470	118. SN7529N - 331
116. SN7515N - 471, 472, 473, 474	119. SN7530N - 332
117. SN7516N - 475, 476, 477, 478	120. SN7531N - 333
118. SN7517N - 479, 480, 481, 482	121. SN7532N - 334
119. SN7518N - 483, 484, 485, 486	122. SN7533N - 335
120. SN7519N - 487, 488, 489, 490	123. SN7534N - 336
121. SN7520N - 491, 492, 493, 494	124. SN7535N - 337
122. SN7521N - 495, 496, 497, 498	125. SN7536N - 338
123. SN7522N - 499, 500, 501, 502	126. SN7537N - 339
124. SN7523N - 503, 504, 505, 506	127. SN7538N - 340
125. SN7524N - 507, 508, 509, 510	128. SN7539N - 341
126. SN7525N - 511, 512, 513, 514	129. SN7540N - 342
127. SN7526N - 515, 516, 517, 518	130. SN7541N - 343
128. SN7527N - 519, 520, 521, 522	131. SN7542N - 344
129. SN7528N - 523, 524, 525, 526	132. SN7543N - 345
130. SN7529N - 527, 528, 529, 530	133. SN7544N - 346
131. SN7530N - 531, 532, 533, 534	134. SN7545N - 347
132. SN7531N - 535, 536, 537, 538	135. SN7546N - 348
133. SN7532N - 539, 540, 541, 542	136. SN7547N - 349
134. SN7533N - 543, 544, 545, 546	137. SN7548N - 350
135. SN7534N - 547, 548, 549, 550	138. SN7549N - 351
136. SN7535N - 551, 552, 553, 554	139. SN7550N - 352
137. SN7536N - 555, 556, 557, 558	140. SN7551N - 353
138. SN7537N - 559, 560, 561, 562	141. SN7552N - 354
139. SN7538N - 563, 564, 565, 566	142. SN7553N - 355
140. SN7539N - 567, 568, 569, 570	143. SN7554N - 356
141. SN7540N - 571, 572, 573, 574	144. SN7555N - 357
142. SN7541N - 575, 576, 577, 578	145. SN7556N - 358
143. SN7542N - 579, 580, 581, 582	146. SN7557N - 359
144. SN7543N - 583, 584, 585, 586	147. SN7558N - 360
145. SN7544N - 587, 588, 589, 590	148. SN7559N - 361
146. SN7545N - 591, 592, 593, 594	149. SN7560N - 362
147. SN7546N - 595, 596, 597, 598	150. SN7561N - 363
148. SN7547N - 599, 600, 601, 602	151. SN7562N - 364
149. SN7548N - 603, 604, 605, 606	152. SN7563N - 365
150. SN7549N - 607, 608, 609, 610	153. SN7564N - 366
151. SN7550N - 611, 612, 613, 614	154. SN7565N - 367
152. SN7551N - 615, 616, 617, 618	155. SN7566N - 368
153. SN7552N - 619, 620, 621, 622	156. SN7567N - 369
154. SN7553N - 623, 624, 625, 626	157. SN7568N - 370
155. SN7554N - 627, 628, 629, 630	158. SN7569N - 371
156. SN7555N - 631, 632, 633, 634	159. SN7570N - 372
157. SN7556N - 635, 636, 637, 638	160. SN7571N - 373
158. SN7557N - 639, 640, 641, 642	161. SN7572N - 374
159. SN7558N - 643, 644, 645, 646	162. SN7573N - 375
160. SN7559N - 647, 648, 649, 650	163. SN7574N - 376
161. SN7560N - 651, 652, 653, 654	164. SN7575N - 377
162. SN7561N - 655, 656, 657, 658	165. SN7576N - 378
163. SN7562N - 659, 660, 661, 662	166. SN7577N - 379
164. SN7563N - 663, 664, 665, 666	167. SN7578N - 380
165. SN7564N - 667, 668, 669, 670	168. SN7579N - 381
166. SN7565N - 671, 672, 673, 674	169. SN7580N - 382
167. SN7566N - 675, 676, 677, 678	170. SN7581N - 383
168. SN7567N - 679, 680, 681, 682	171. SN7582N - 384
169. SN7568N - 683, 684,	

C-47

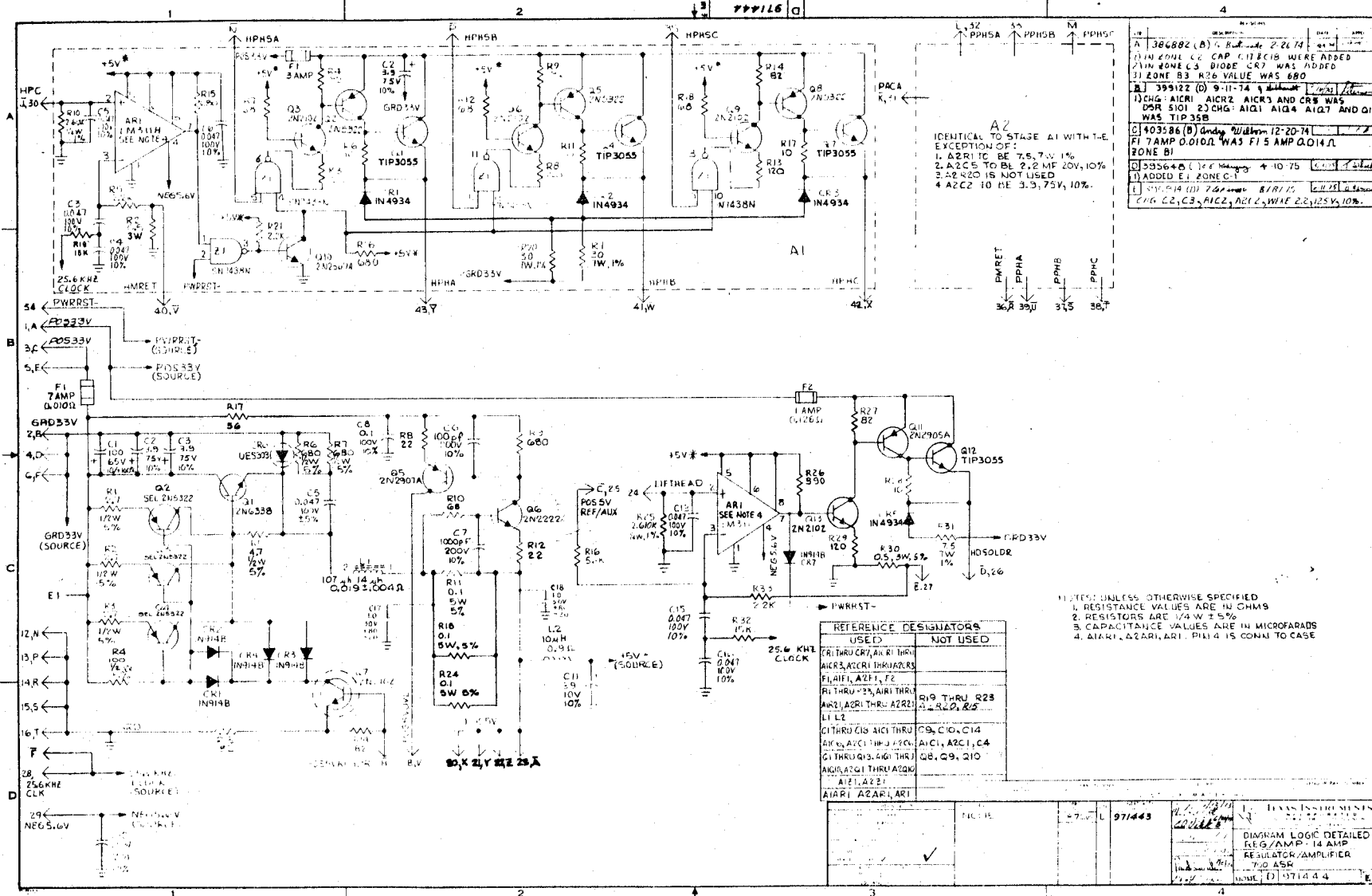


REV	1	LOGIC SYMBOL NO.	96214	DRAWING NO.	969502	REV	B
DATE: 1/15/64				BY: J. H. HARRIS			

FRAMED

Reg/Amp.

C48

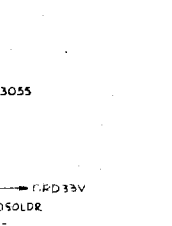
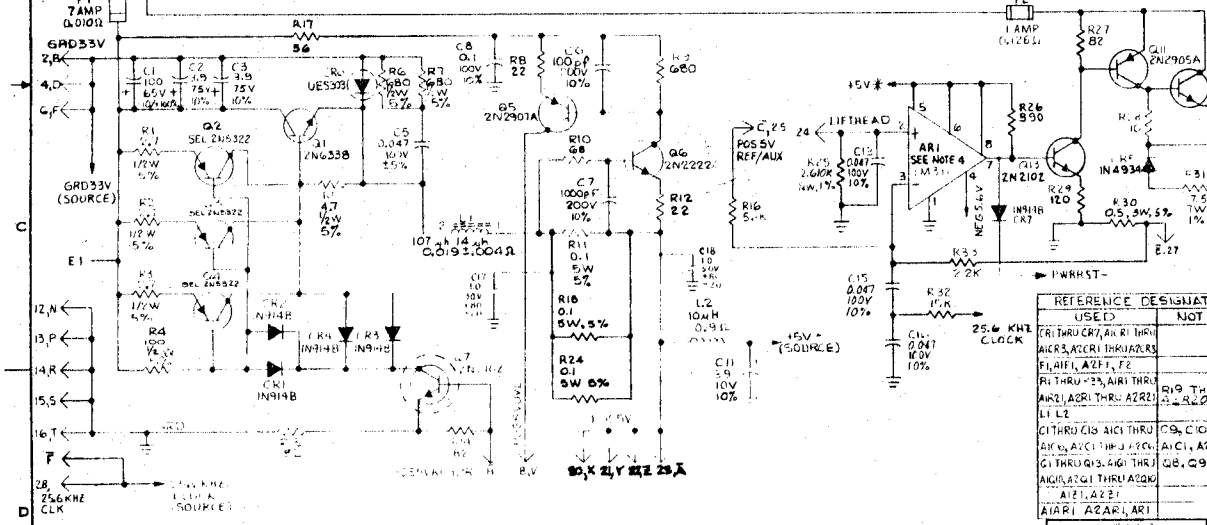
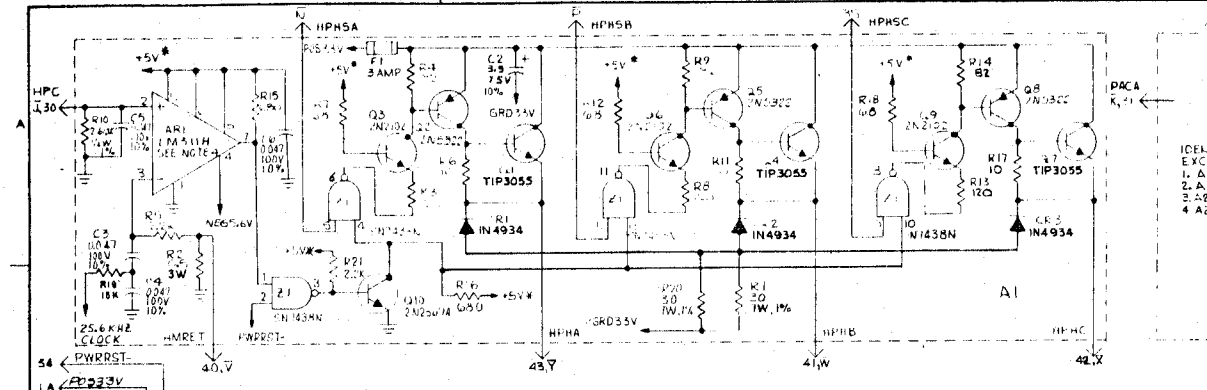


REV	DESCRIPTION	DATE	BY
1	386882 (A) 7. 11. 74 2-26-74		
2	1. IN ZONE C2 CAP C11, C18 WERE ADDED		
3	2. IN ZONE C3 DIODE CR7 WAS ADDED		
4	3. ZONE B3 R26 VALUE WAS 680		
5	399122 (D) 9-11-74		
6	1) CHG: A1C1, A1C2, A1C3 AND CR5 WAS		
7	DSR 5101 2) CHG: A1Q1, A1Q4, A1Q7 AND A1Q2		
8	WAS TIP 35B		
9	C140386 (B) 10/11/74 12-20-74		
10	F1 7 AMP 0.010L WAS F1 5 AMP 0.014L		
11	ZONE B1		
12	D 935645 (C) 1/16/75 4-10-75		
13	1) ADDED F1 ZONE C-1		
14	L 500,014 (M) 7/6/75 8/11/75		
15	CHG C2, C3, A1C2, A1C3, W1E 2.2, 125V, 10%		

A2 IDENTICAL TO STAGE A1 WITH THE EXCEPTION OF:

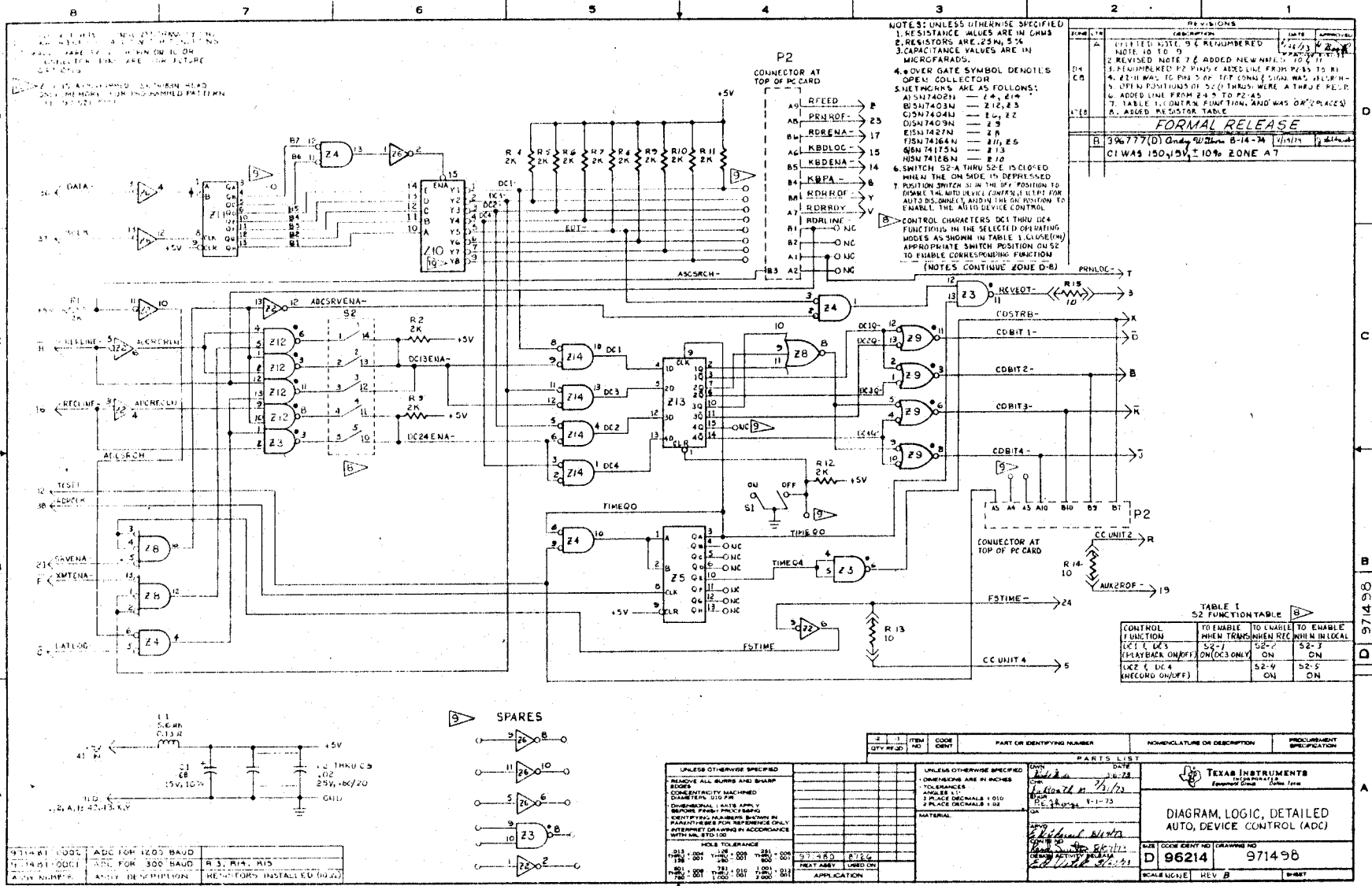
1. A2R1 TO BE 7.5, 7W, 1%
2. A2C2 TO BE 2.2 MF 20V, 10%
3. A2R20 IS NOT USED
4. A2C2 TO BE 3.9, 75V, 10%

PMRET 36.8
PPHA 39.1
PPMB 34.5
PPHC 36.7



USED	NOT USED
A1 THRU A7, A10 THRU A13, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28, A29, A30, A31, A32, A33, A34, A35, A36, A37, A38, A39, A40, A41, A42, A43, A44, A45, A46, A47, A48, A49, A50, A51, A52, A53, A54, A55, A56, A57, A58, A59, A60, A61, A62, A63, A64, A65, A66, A67, A68, A69, A70, A71, A72, A73, A74, A75, A76, A77, A78, A79, A80, A81, A82, A83, A84, A85, A86, A87, A88, A89, A90, A91, A92, A93, A94, A95, A96, A97, A98, A99, A100	A8, A9, A11, A12, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28, A29, A30, A31, A32, A33, A34, A35, A36, A37, A38, A39, A40, A41, A42, A43, A44, A45, A46, A47, A48, A49, A50, A51, A52, A53, A54, A55, A56, A57, A58, A59, A60, A61, A62, A63, A64, A65, A66, A67, A68, A69, A70, A71, A72, A73, A74, A75, A76, A77, A78, A79, A80, A81, A82, A83, A84, A85, A86, A87, A88, A89, A90, A91, A92, A93, A94, A95, A96, A97, A98, A99, A100

REV	DESCRIPTION	DATE	BY
1	386882 (A) 7. 11. 74 2-26-74		
2	1. IN ZONE C2 CAP C11, C18 WERE ADDED		
3	2. IN ZONE C3 DIODE CR7 WAS ADDED		
4	3. ZONE B3 R26 VALUE WAS 680		
5	399122 (D) 9-11-74		
6	1) CHG: A1C1, A1C2, A1C3 AND CR5 WAS		
7	DSR 5101 2) CHG: A1Q1, A1Q4, A1Q7 AND A1Q2		
8	WAS TIP 35B		
9	C140386 (B) 10/11/74 12-20-74		
10	F1 7 AMP 0.010L WAS F1 5 AMP 0.014L		
11	ZONE B1		
12	D 935645 (C) 1/16/75 4-10-75		
13	1) ADDED F1 ZONE C-1		
14	L 500,014 (M) 7/6/75 8/11/75		
15	CHG C2, C3, A1C2, A1C3, W1E 2.2, 125V, 10%		



NOTES: UNLESS OTHERWISE SPECIFIED
 1. RESISTANCE VALUES ARE IN OHMS
 2. RESISTORS ARE .25W, 5%
 3. CAPACITANCE VALUES ARE IN MICROFARADS.
 4. OVER GATE SYMBOL DENOTES OPEN COLLECTOR
 5. SWITCHES ARE AS FOLLOWS:
 A) S174021 --- Z4, Z19
 B) S174034 --- Z12, Z3
 C) S174044 --- Z4, Z2
 D) S174091 --- Z9
 E) S174271 --- Z8
 F) S174284 --- Z1, Z5
 G) S174341 --- Z13
 H) S174381 --- Z10

6. SWITCH S2A THRU S2E IS CLOSED WHEN THE ON SIDE IS DEPRESSED
 7. POSITION SWITCH S2F IS IN THE OFF POSITION TO DISABLE THE AUTO DEVICE CONTROL. IT IS LEFT FOR AUTO DISCONNECT AND IN THE ON POSITION TO ENABLE THE AUTO DEVICE CONTROL
 8. CONTROL CHARACTERS DC1 THRU DC4 FUNCTIONAL IN THE SELECTED OPERATING MODES AS SHOWN IN TABLE 1 (LOCKED) APPROPRIATE SWITCH POSITION ON S2 TO ENABLE CORRESPONDING FUNCTION

(NOTES CONTINUE ZONE D-B)

REV	DATE	APPROVAL
A	1/24/73	W. B. ...
B	1/24/73	W. B. ...
C	1/24/73	W. B. ...
D	1/24/73	W. B. ...

REVISIONS

1. REVISED NOTE 9 & RENUMBERED
 2. REVISED NOTE 7 & ADDED NEW NOTES
 3. RENUMBERED P2 PINS & ADDED LINE FROM P2-5 TO R1
 4. P2-11 WAS TO PIN 5 OF 7410 (P2-11 SIGNAL WAS JERKING)
 5. OPEN POSITIONS OF S2 (C) THRU S2 (F) WERE A TYPICAL ERROR
 6. ADDED LINE FROM Z4-9 TO P2-45
 7. TABLE 1: OUTPUT FUNCTION, AND WAS ON 2 PLACES
 8. ADDED REVISION TABLE

FORMAL RELEASE

B 934777(D) Only 971498 B-14-74 1/14/73
 C1 WAS 150V, 5% ± 10% ZONE A-7

TABLE 1
S2 FUNCTION TABLE

CONTROL FUNCTION	TO ENABLE WHEN TRANSMISSION RECORD ON/OFF	TO DISABLE WHEN TRANSMISSION RECORD ON/OFF	TO ENABLE WHEN RECORD ON/OFF
DC1 & DC3 (PLAYBACK ON/OFF)	ON	OFF	ON
DC2 & DC4 (RECORD ON/OFF)	ON	OFF	ON

QTY	REV	CODE	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	REQUIREMENT SPECIFICATION
1	1	7410	7410	7410	7410
1	1	7412	7412	7412	7412
1	1	7413	7413	7413	7413
1	1	7414	7414	7414	7414
1	1	7415	7415	7415	7415
1	1	7416	7416	7416	7416
1	1	7417	7417	7417	7417
1	1	7418	7418	7418	7418
1	1	7419	7419	7419	7419
1	1	7420	7420	7420	7420
1	1	7421	7421	7421	7421
1	1	7422	7422	7422	7422
1	1	7423	7423	7423	7423
1	1	7424	7424	7424	7424
1	1	7425	7425	7425	7425
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1	1	7427	7427	7427	7427
1	1	7428	7428	7428	7428
1	1	7429	7429	7429	7429
1	1	7430	7430	7430	7430
1	1	7431	7431	7431	7431
1	1	7432	7432	7432	7432
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1	1	7436	7436	7436	7436
1	1	7437	7437	7437	7437
1	1	7438	7438	7438	7438
1	1	7439	7439	7439	7439
1	1	7440	7440	7440	7440
1	1	7441	7441	7441	7441
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1	1	7447	7447	7447	7447
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1	1	7465	7465	7465	7465
1	1	7466	7466	7466	7466
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1	1	7468	7468	7468	7468
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1	1	7495	7495	7495	7495
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1	1	7497	7497	7497	7497
1	1	7498	7498	7498	7498
1	1	7499	7499	7499	7499
1	1	7500	7500	7500	7500

QTY	REV	CODE	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	REQUIREMENT SPECIFICATION
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1	1	7469	7469	7469	7469
1	1	7470	7470	7470	7470
1	1	7471	7471	7471	7471
1	1	7472	7472	7472	7472
1	1	7473	7473	7473	7473
1	1	7474	7474	7474	7474
1	1	7475	7475	7475	

CHARACTER	INPUT ADDRESS	OUTPUT CODE	SIGNAL	FUNCTION
IND	SPACE	0	ALL	SPACE
SON	1	0	CR	LINE FEED
STX	2	0	CR	START OF TEXT
ETX	3	0	CR	END OF TEXT
ENG	4	0	CR	END OF LINE
ACK	5	0	CR	ACKNOWLEDGE
BEL	6	0	CR	BELL
BS	7	0	CR	BACKSPACE
HT	8	0	CR	HORIZONTAL TAB
LF	9	0	CR	LINE FEED
VT	10	0	CR	VERTICAL TAB
FF	11	0	CR	FORM FEED
CR	12	0	CR	CARRIAGE RETURN
SO	13	0	CR	SHIFT OUT
DLE	14	0	CR	DATA LINK ESCAPE
DC1	15	0	CR	DEVICE CONTROL 1
DC2	16	0	CR	DEVICE CONTROL 2
DC3	17	0	CR	DEVICE CONTROL 3
DC4	18	0	CR	DEVICE CONTROL 4
NAK	19	0	CR	NOT ACKNOWLEDGED
SYN	20	0	CR	SYNCHRONOUS IDLE
ETB	21	0	CR	END OF TRANSMISSION BLOCK
CAN	22	0	CR	CANONICAL FLAG
EM	23	0	CR	END OF MESSAGE
SUB	24	0	CR	SUBSTITUTE
ESC	25	0	CR	ESCAPE
FS	26	0	CR	FILE SEPARATOR
GS	27	0	CR	GROUP SEPARATOR
RS	28	0	CR	RECORD SEPARATOR
US	29	0	CR	UNIT SEPARATOR

CHARACTER	INPUT ADDRESS	OUTPUT CODE	SIGNAL	FUNCTION
IND	SPACE	0	ALL	SPACE
SON	1	0	CR	LINE FEED
STX	2	0	CR	START OF TEXT
ETX	3	0	CR	END OF TEXT
ENG	4	0	CR	END OF LINE
ACK	5	0	CR	ACKNOWLEDGE
BEL	6	0	CR	BELL
BS	7	0	CR	BACKSPACE
HT	8	0	CR	HORIZONTAL TAB
LF	9	0	CR	LINE FEED
VT	10	0	CR	VERTICAL TAB
FF	11	0	CR	FORM FEED
CR	12	0	CR	CARRIAGE RETURN
SO	13	0	CR	SHIFT OUT
DLE	14	0	CR	DATA LINK ESCAPE
DC1	15	0	CR	DEVICE CONTROL 1
DC2	16	0	CR	DEVICE CONTROL 2
DC3	17	0	CR	DEVICE CONTROL 3
DC4	18	0	CR	DEVICE CONTROL 4
NAK	19	0	CR	NOT ACKNOWLEDGED
SYN	20	0	CR	SYNCHRONOUS IDLE
ETB	21	0	CR	END OF TRANSMISSION BLOCK
CAN	22	0	CR	CANONICAL FLAG
EM	23	0	CR	END OF MESSAGE
SUB	24	0	CR	SUBSTITUTE
ESC	25	0	CR	ESCAPE
FS	26	0	CR	FILE SEPARATOR
GS	27	0	CR	GROUP SEPARATOR
RS	28	0	CR	RECORD SEPARATOR
US	29	0	CR	UNIT SEPARATOR

CHARACTER	INPUT ADDRESS	OUTPUT CODE	SIGNAL	FUNCTION
IND	SPACE	0	ALL	SPACE
SON	1	0	CR	LINE FEED
STX	2	0	CR	START OF TEXT
ETX	3	0	CR	END OF TEXT
ENG	4	0	CR	END OF LINE
ACK	5	0	CR	ACKNOWLEDGE
BEL	6	0	CR	BELL
BS	7	0	CR	BACKSPACE
HT	8	0	CR	HORIZONTAL TAB
LF	9	0	CR	LINE FEED
VT	10	0	CR	VERTICAL TAB
FF	11	0	CR	FORM FEED
CR	12	0	CR	CARRIAGE RETURN
SO	13	0	CR	SHIFT OUT
DLE	14	0	CR	DATA LINK ESCAPE
DC1	15	0	CR	DEVICE CONTROL 1
DC2	16	0	CR	DEVICE CONTROL 2
DC3	17	0	CR	DEVICE CONTROL 3
DC4	18	0	CR	DEVICE CONTROL 4
NAK	19	0	CR	NOT ACKNOWLEDGED
SYN	20	0	CR	SYNCHRONOUS IDLE
ETB	21	0	CR	END OF TRANSMISSION BLOCK
CAN	22	0	CR	CANONICAL FLAG
EM	23	0	CR	END OF MESSAGE
SUB	24	0	CR	SUBSTITUTE
ESC	25	0	CR	ESCAPE
FS	26	0	CR	FILE SEPARATOR
GS	27	0	CR	GROUP SEPARATOR
RS	28	0	CR	RECORD SEPARATOR
US	29	0	CR	UNIT SEPARATOR

CHARACTER	INPUT ADDRESS	OUTPUT CODE	SIGNAL	FUNCTION
IND	SPACE	0	ALL	SPACE
SON	1	0	CR	LINE FEED
STX	2	0	CR	START OF TEXT
ETX	3	0	CR	END OF TEXT
ENG	4	0	CR	END OF LINE
ACK	5	0	CR	ACKNOWLEDGE
BEL	6	0	CR	BELL
BS	7	0	CR	BACKSPACE
HT	8	0	CR	HORIZONTAL TAB
LF	9	0	CR	LINE FEED
VT	10	0	CR	VERTICAL TAB
FF	11	0	CR	FORM FEED
CR	12	0	CR	CARRIAGE RETURN
SO	13	0	CR	SHIFT OUT
DLE	14	0	CR	DATA LINK ESCAPE
DC1	15	0	CR	DEVICE CONTROL 1
DC2	16	0	CR	DEVICE CONTROL 2
DC3	17	0	CR	DEVICE CONTROL 3
DC4	18	0	CR	DEVICE CONTROL 4
NAK	19	0	CR	NOT ACKNOWLEDGED
SYN	20	0	CR	SYNCHRONOUS IDLE
ETB	21	0	CR	END OF TRANSMISSION BLOCK
CAN	22	0	CR	CANONICAL FLAG
EM	23	0	CR	END OF MESSAGE
SUB	24	0	CR	SUBSTITUTE
ESC	25	0	CR	ESCAPE
FS	26	0	CR	FILE SEPARATOR
GS	27	0	CR	GROUP SEPARATOR
RS	28	0	CR	RECORD SEPARATOR
US	29	0	CR	UNIT SEPARATOR

TABLE 2

1. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

2. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

3. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

4. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

5. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

6. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

7. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

8. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

9. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

10. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

11. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

12. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

13. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

14. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

15. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

16. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

17. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

18. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

19. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

20. SIGNAL PRESENTATION OF DECODED CHARACTER OF SYMBOL

TABLE 3
TERMINAL REMOTE FUNCTIONS

SIGNAL	FUNCTION
IND	SPACE
SON	LINE FEED
STX	START OF TEXT
ETX	END OF TEXT
ENG	END OF LINE
ACK	ACKNOWLEDGE
BEL	BELL
BS	BACKSPACE
HT	HORIZONTAL TAB
LF	LINE FEED
VT	VERTICAL TAB
FF	FORM FEED
CR	CARRIAGE RETURN
SO	SHIFT OUT
DLE	DATA LINK ESCAPE
DC1	DEVICE CONTROL 1
DC2	DEVICE CONTROL 2
DC3	DEVICE CONTROL 3
DC4	DEVICE CONTROL 4
NAK	NOT ACKNOWLEDGED
SYN	SYNCHRONOUS IDLE
ETB	END OF TRANSMISSION BLOCK
CAN	CANONICAL FLAG
EM	END OF MESSAGE
SUB	SUBSTITUTE
ESC	ESC
FS	FILE SEPARATOR
GS	GROUP SEPARATOR
RS	RECORD SEPARATOR
US	UNIT SEPARATOR

TABLE 4 STATUS CHAR

BIT NO.	FUNCTION
0	SPACE
1	LINE FEED
2	START OF TEXT
3	END OF TEXT
4	END OF LINE
5	ACKNOWLEDGE
6	BELL
7	BACKSPACE
8	HORIZONTAL TAB
9	LINE FEED
10	VERTICAL TAB
11	FORM FEED
12	CARRIAGE RETURN
13	SHIFT OUT
14	DATA LINK ESCAPE
15	DEVICE CONTROL 1
16	DEVICE CONTROL 2
17	DEVICE CONTROL 3
18	DEVICE CONTROL 4
19	NOT ACKNOWLEDGED
20	SYNCHRONOUS IDLE
21	END OF TRANSMISSION BLOCK
22	CANONICAL FLAG
23	END OF MESSAGE
24	SUBSTITUTE
25	ESC
26	FILE SEPARATOR
27	GROUP SEPARATOR
28	RECORD SEPARATOR
29	UNIT SEPARATOR

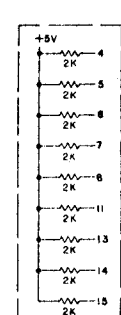


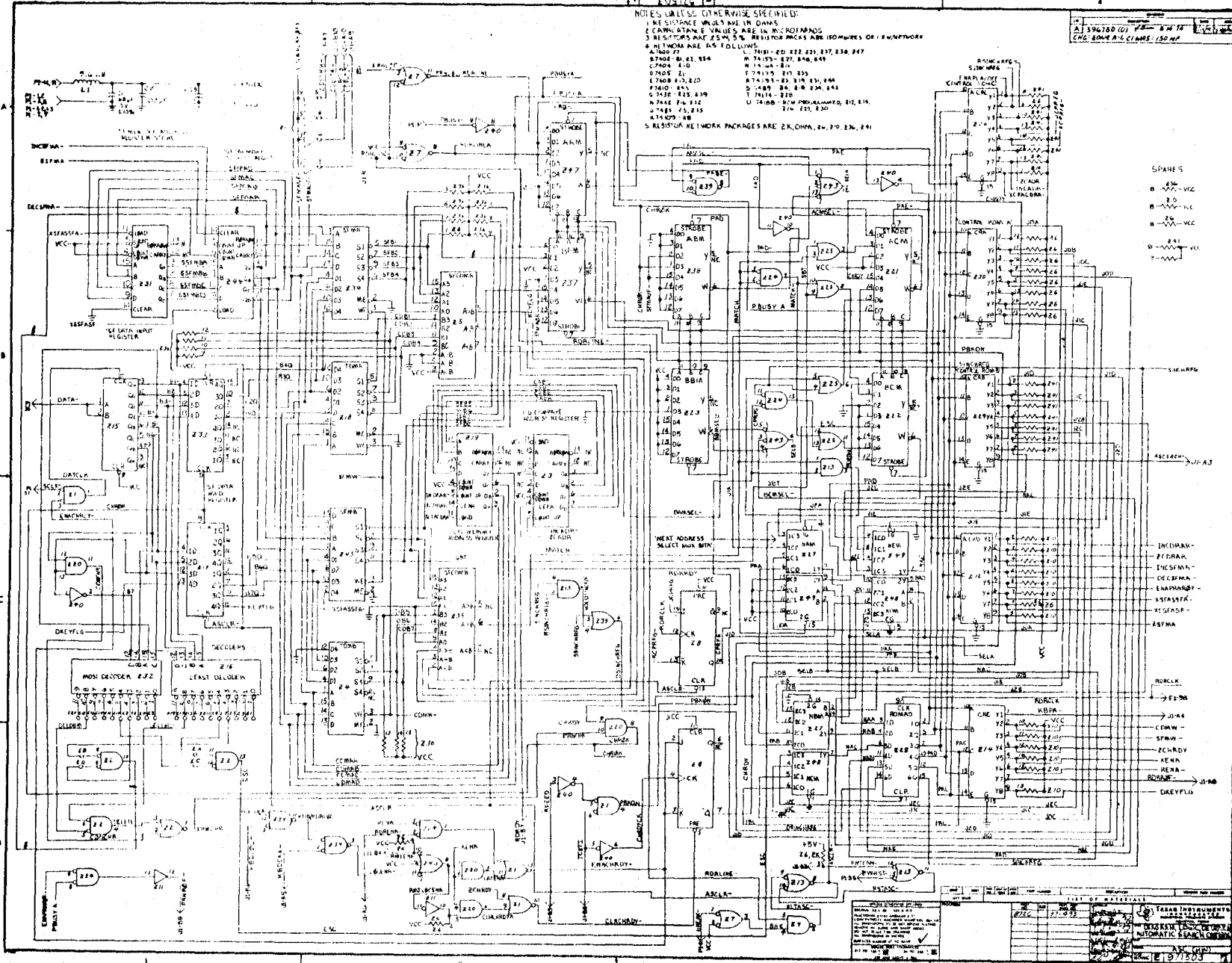
TABLE 5

ASSY NUMBER	ASSY DESCRIPTION	PATTERN	TEST POINTS	TEST POINTS	TEST POINTS	TEST POINTS	TEST POINTS
971483-0007	RDC 100 BAUD CODE 0	PATTERN 4	RT, R1, R4, R6, R10	R1, R10, R15	R1, R10, R15	R1, R10, R15	R1, R10, R15
0006	1200 COMPUTER	1	R1, R10, R15, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R121, R122, R123, R124, R125, R126, R127, R128, R129, R130, R131, R132, R133, R134, R135, R136, R137, R138, R139, R140, R141, R142, R143, R144, R145, R146, R147, R148, R149, R150, R151, R152, R153, R154, R155, R156, R157, R158, R159, R160, R161, R162, R163, R164, R165, R166, R167, R168, R169, R170, R171, R172, R173, R174, R175, R176, R177, R178, R179, R180, R181, R182, R183, R184, R185, R186, R187, R188, R189, R190, R191, R192, R193, R194, R195, R196, R197, R198, R199, R200, R201, R202, R203, R204, R205, R206, R207, R208, R209, R210, R211, R212, R213, R214, R215, R216, R217, R218, R219, R220, R221, R222, R223, R224, R225, R226, R227, R228, R229, R230, R231, R232, R233, R234, R235, R236, R237, R238, R239, R240, R241, R242, R243, R244, R245, R246, R247, R248, R249, R250, R251, R252, R253, R254, R255, R256, R257, R258, R259, R260, R261, R262, R263, R264, R265, R266, R267, R268, R269, R270, R271, R272, R273, R274, R275, R276, R277, R278, R279, R280, R281, R282, R283, R284, R285, R286, R287, R288, R289, R290, R291, R292, R293, R294, R295, R296, R297, R298, R299, R300, R301, R302, R303, R304, R305, R306, R307, R308, R309, R310, R311, R312, R313, R314, R315, R316, R317, R318, R319, R320, R321, R322, R323, R324, R325, R326, R327, R328, R329, R330, R331, R332, R333, R334, R335, R336, R337, R338, R339, R340, R341, R342, R343, R344, R345, R346, R347, R348, R349, R350, R351, R352, R353, R354, R355, R356, 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NOTES UNLESS OTHERWISE SPECIFIED:

- 1. RESISTANCE VALUES ARE IN OHMS
- 2. CAPACITANCE VALUES ARE IN MICROGRAMS
- 3. RESISTORS ARE 5% TOL. 5% RESISTOR PACKS ARE 10% TOLERANCE
- 4. DIMENSIONS ARE AS FOLLOWS:
 A: 1000 ± 0.1
 B: 1700 ± 0.1
 C: 1700 ± 0.1
 D: 1700 ± 0.1
 E: 1700 ± 0.1
 F: 1700 ± 0.1
 G: 1700 ± 0.1
 H: 1700 ± 0.1
 I: 1700 ± 0.1
 J: 1700 ± 0.1
 K: 1700 ± 0.1
 L: 1700 ± 0.1
 M: 1700 ± 0.1
 N: 1700 ± 0.1
 O: 1700 ± 0.1
 P: 1700 ± 0.1
 Q: 1700 ± 0.1
 R: 1700 ± 0.1
 S: 1700 ± 0.1
 T: 1700 ± 0.1
 U: 1700 ± 0.1
 V: 1700 ± 0.1
 W: 1700 ± 0.1
 X: 1700 ± 0.1
 Y: 1700 ± 0.1
 Z: 1700 ± 0.1
- 5. RESISTOR NETWORK PACKAGES ARE 2K, 0HM, 20, 0.10, 2.0, 2.0

1396180 (1) 7-68 4-1/2 X 11
 ENG. BOM. R/L. CLAMS. 150/14



- SPANS
- A - VCC
- B - VCC
- C - VCC
- D - VCC
- E - VCC
- F - VCC
- G - VCC
- H - VCC
- I - VCC
- J - VCC
- K - VCC
- L - VCC
- M - VCC
- N - VCC
- O - VCC
- P - VCC
- Q - VCC
- R - VCC
- S - VCC
- T - VCC
- U - VCC
- V - VCC
- W - VCC
- X - VCC
- Y - VCC
- Z - VCC

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TECHNICAL SPECIFICATIONS

1. GENERAL INFORMATION

2. ELECTRICAL CHARACTERISTICS

3. MECHANICAL DATA

4. ORDERING INFORMATION

5. PACKAGING INFORMATION

6. TEST PROCEDURES

7. TYPICAL APPLICATIONS

8. NOTES

9. LEGEND

10. INDEX

11. REVISIONS

12. APPROVALS

13. DATE

14. DRAWN BY

15. CHECKED BY

16. ENGINEER

17. MANAGER

18. TITLE

19. COMPANY

20. ADDRESS

21. CITY

22. STATE

23. ZIP

24. PHONE

25. FAX

26. E-MAIL

27. WWW

28. COUNTRY

29. LANGUAGE

30. UNITS

31. TOLERANCES

32. DIMENSIONS

33. WEIGHTS

34. VOLUMES

35. SHEETS

36. PARTS

37. MATERIALS

38. FINISHES

39. COATINGS

40. MARKINGS

41. LABELS

42. INSTRUCTIONS

43. SAFETY

44. ENVIRONMENT

45. COMPLIANCE

46. CERTIFICATIONS

47. STANDARDS

48. REFERENCES

49. SOURCES

50. DISTRIBUTORS

51. SUPPLIERS

52. MANUFACTURERS

53. ASSEMBLERS

54. MAINTENANCE

55. REPAIRS

56. UPGRADES

57. MODIFICATIONS

58. REWORKS

59. SCRAPS

60. WASTES

61. RECYCLING

62. DISPOSAL

63. STORAGE

64. HANDLING

65. TRANSPORT

66. PACKAGING

67. LABELING

68. MARKING

69. IDENTIFICATION

70. TRACKING

71. RECORDS

72. DOCUMENTATION

73. ARCHIVING

74. RETRIEVAL

75. ACCESS

76. SECURITY

77. PROTECTION

78. CONFIDENTIALITY

79. PATENTS

80. TRADE SECRETS

81. INTELLECTUAL PROPERTY

82. LEGAL

83. COMPLIANCE

84. ETHICS

85. INTEGRITY

86. HONESTY

87. FAIRNESS

88. RESPECT

89. RESPONSIBILITY

90. ACCOUNTABILITY

91. TRANSPARENCY

92. COMMUNICATION

93. COLLABORATION

94. TEAMWORK

95. LEADERSHIP

96. INNOVATION

97. CREATIVITY

98. PROBLEM SOLVING

99. DECISION MAKING

100. RISK MANAGEMENT

101. CHANGE MANAGEMENT

102. QUALITY MANAGEMENT

103. CONTINUOUS IMPROVEMENT

104. CUSTOMER SATISFACTION

105. EMPLOYEE ENGAGEMENT

106. ORGANIZATIONAL DEVELOPMENT

107. STRATEGIC PLANNING

108. BUSINESS DEVELOPMENT

109. FINANCIAL MANAGEMENT

110. OPERATIONAL EXCELLENCE

111. SUPPLY CHAIN MANAGEMENT

112. LOGISTICS

113. PROJECT MANAGEMENT

114. TIME MANAGEMENT

115. STRESS MANAGEMENT

116. WORK-LIFE BALANCE

117. SAFETY

118. HEALTH

119. ENVIRONMENTAL RESPONSIBILITY

120. SOCIAL RESPONSIBILITY

121. CORPORATE CITIZENSHIP

122. REPUTATION MANAGEMENT

123. BRAND MANAGEMENT

124. MARKETING

125. SALES

126. CUSTOMER SERVICE

127. SUPPORT

128. TRAINING

129. DEVELOPMENT

130. LEARNING

131. GROWTH

132. INNOVATION

133. ADAPTABILITY

134. RESILIENCE

135. AGILITY

136. FLEXIBILITY

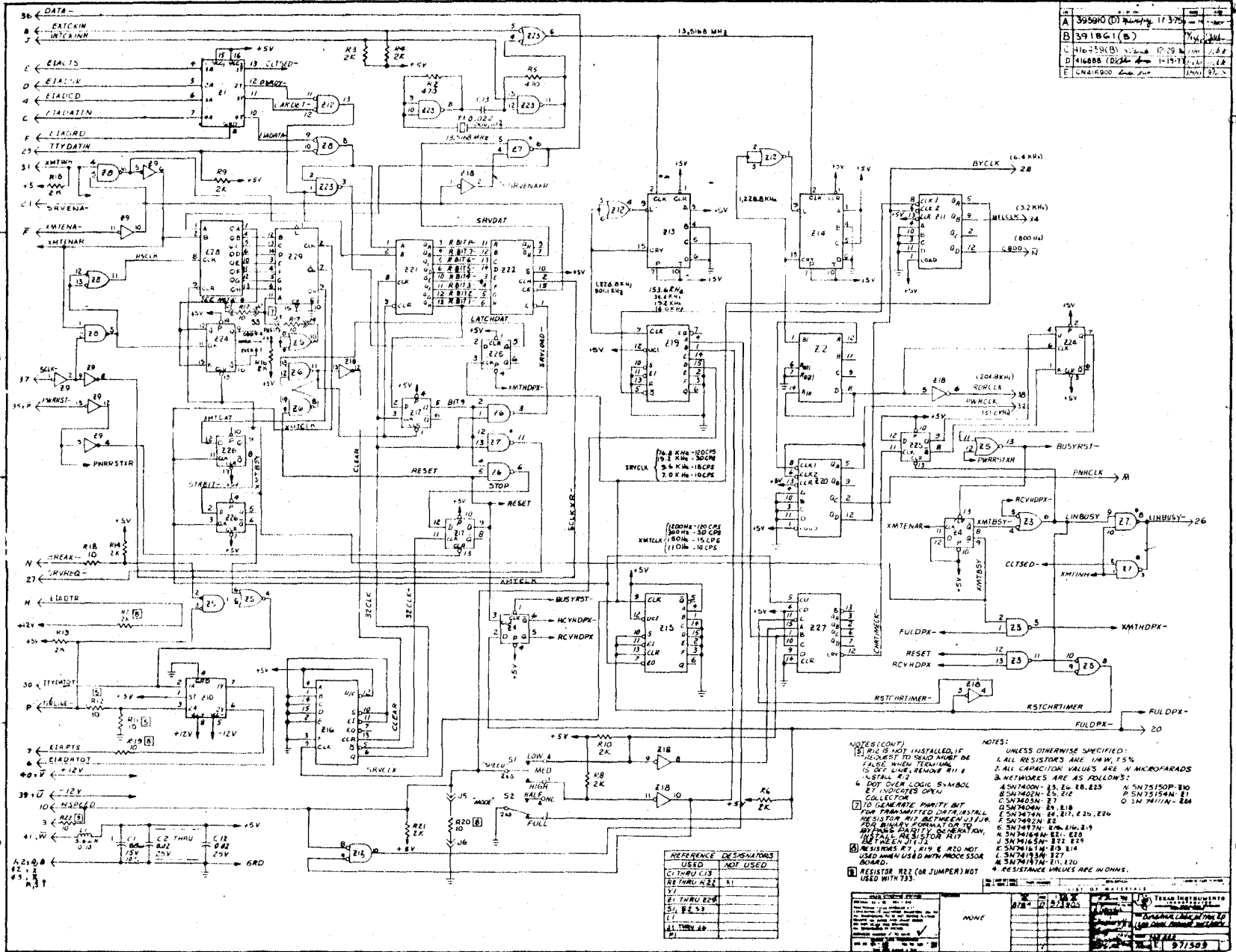
137. SCALABILITY

138. SUSTAINABILITY

139. LONGEVITY

140. SUCCESS

C-59



A	39590 (D)	Quantity	11	375
B	39186 (1)			
C	110-258 (B)		10	29
D	110-688 (D)		10	11
E	110-690 (D)		10	21

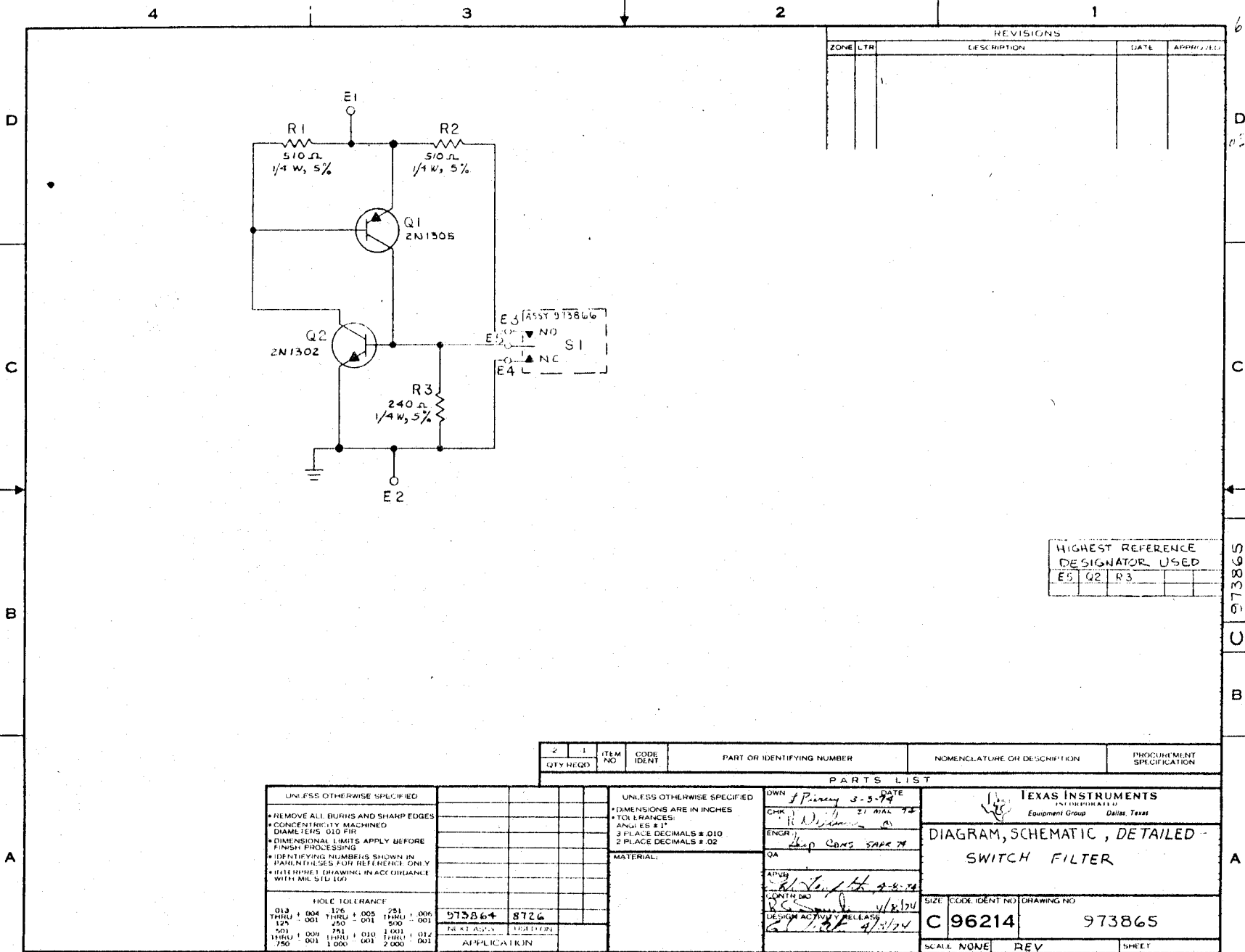
- NOTES (CONT)
1. IC'S NOT INSTALLED, IF NECESSARY TO READ NUMBER VALUE WHEN TESTING.
 2. DOT OVER LOGIC SYMBOL INDICATES OPEN COLLECTOR.
 3. TO GENERATE PARITY BIT FOR TRANSMITTED DATA, INSTALL RESISTOR R17 BETWEEN J11 & J12. PARITY INDICATOR TO ANY LOGIC SYMBOL INDICATES OPEN COLLECTOR.
 4. RESISTORS R17, R18 & R19 NOT USED WHEN USED WITH PROCESSOR BOARD.
 5. RESISTOR R21 (OR JUMPER) NOT USED WITH 733.

- NOTES:
1. ALL RESISTORS ARE 1/4W, 1%. UNLESS OTHERWISE SPECIFIED.
 2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
 3. NETWORKS ARE AS FOLLOWS:
 - A. SN7400N-1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100.

REFERENCE DESIGNATIONS USED	NOT USED
C1 THRU C13	
R1 THRU R22	R1
U1	
U2 THRU U28	
S1, S2, S3	
U1 THRU U8	
U9	

TEST INSTRUMENTS	MAKE	MODEL	TEST POINT
OSCILLOSCOPE			
POWER SUPPLY			
RESISTANCE			
TEST INSTRUMENTS			
MAKE			
MODEL			
TEST POINT			

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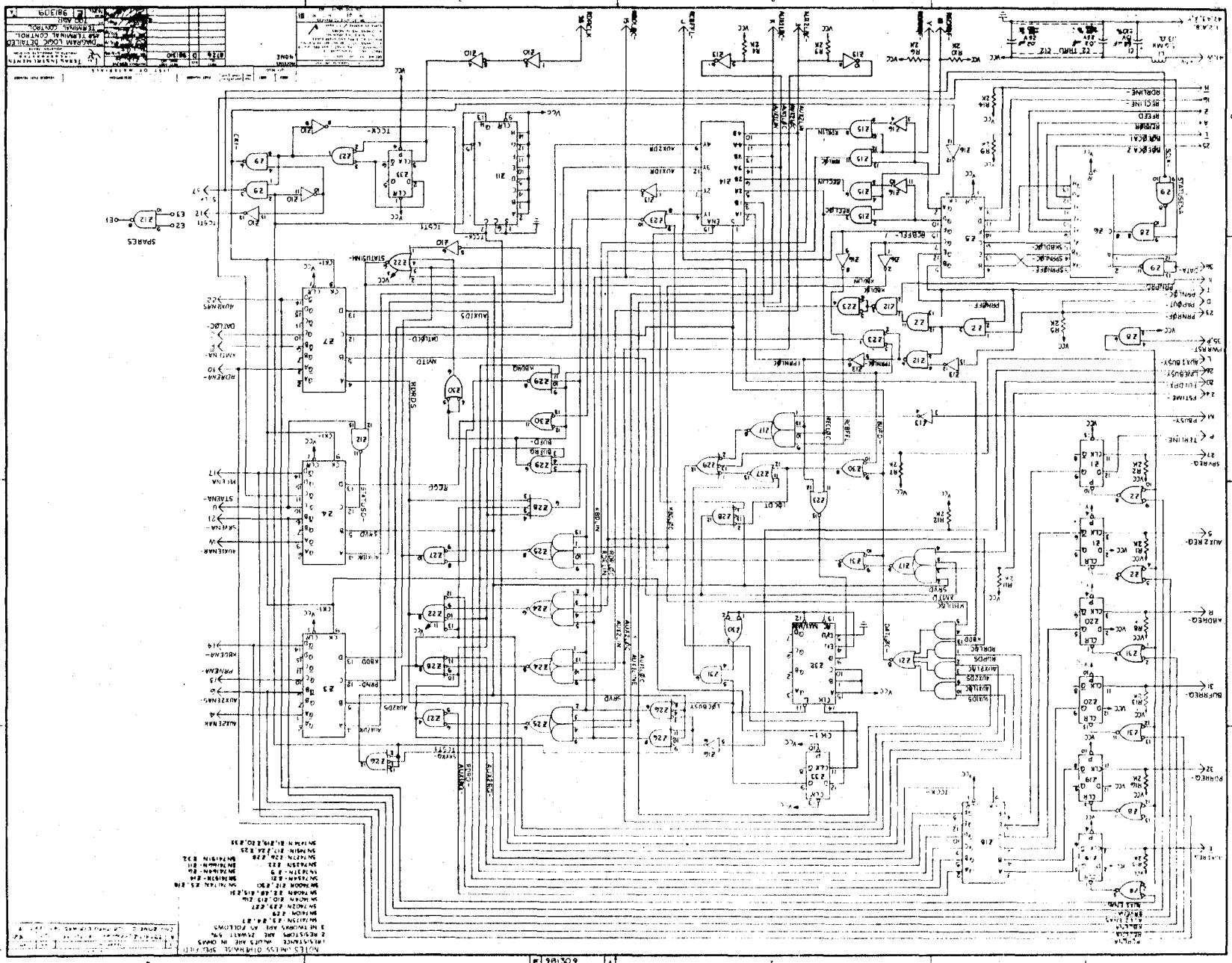
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

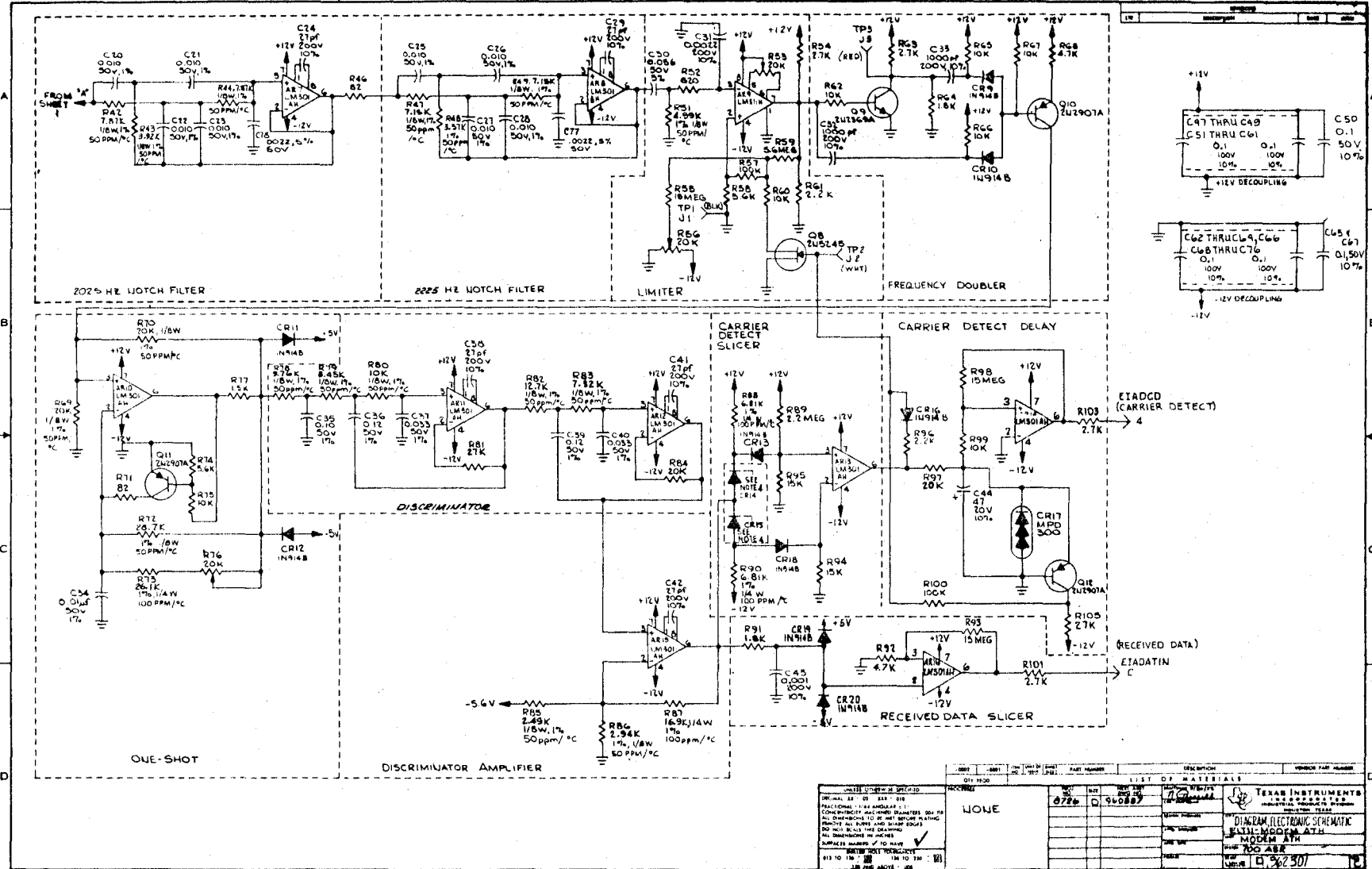
HIGHEST REFERENCE DESIGNATOR USED			
E3	Q2	R3	

2	1	ITEM NO	CODE IDENT	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION
QTY	HEGD					

UNLESS OTHERWISE SPECIFIED				UNLESS OTHERWISE SPECIFIED				PARTS LIST			
<ul style="list-style-type: none"> REMOVE ALL BURRS AND SHARP EDGES CONCENTRICITY MACHINED DIAMETERS .010 FIR DIMENSIONAL LIMITS APPLY BEFORE FINISH PROCESSING IDENTIFYING NUMBERS SHOWN IN PARENTHESSES FOR REFERENCE ONLY DATE THIS DRAWING IN ACCORDANCE WITH MIL STD 100 				<ul style="list-style-type: none"> DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° 3 PLACE DECIMALS ± .010 2 PLACE DECIMALS ± .02 				DWN <i>P. Perry 3-5-79</i> DATE CHK <i>R. Williams</i> 21 MAR 79 ENGR <i>Chip Cons SARK</i> QA APUR <i>W. J. ... 4-8-79</i> LATH DW <i>W. S. ... 4/8/79</i> DESIGN ACTIVITY RELEASE <i>9/3/79</i>		TEXAS INSTRUMENTS <small>INCORPORATED</small> Equipment Group Dallas, Texas	
HOLE TOLERANCE .013 ± .004 .126 ± .005 .251 ± .006 THROUGH ± .001 .250 ± .001 .500 ± .001 .501 ± .009 .751 ± .010 1.001 ± .012 1.251 ± .011 1.501 ± .012 2.001 ± .015 .750 ± .001 1.000 ± .001 2.000 ± .001				MATERIAL 973866-8724 PART AND IDENTIFYING NUMBER APPLICATION				SIZE CODE IDENT NO DRAWING NO C 96214 973865			
SCALE NONE REV SHEET				DATE				DATE			

Terminal Control





C35

QTY	NO.	DESCRIPTION	REVISION	DATE
1	0786	RESISTOR	1	10/1/68
1	0787	RESISTOR	1	10/1/68
1	0788	RESISTOR	1	10/1/68
1	0789	RESISTOR	1	10/1/68
1	0790	RESISTOR	1	10/1/68
1	0791	RESISTOR	1	10/1/68
1	0792	RESISTOR	1	10/1/68
1	0793	RESISTOR	1	10/1/68
1	07			

