As you are now the owner of this document which should have come to you for free, please consider making a donation of £1 or more for the upkeep of the (Radar) website which holds this document. I give my time for free, but it costs me money to bring this document to you. You can donate here https://blunham.com/Misc/Texas

Many thanks.

Please do not upload this copyright pdf document to any other website. Breach of copyright may result in a criminal conviction.

This Acrobat document was generated by me, Colin Hinson, from a document held by me. I requested permission to publish this from Texas Instruments (twice) but received no reply. It is presented here (for free) and this pdf version of the document is my copyright in much the same way as a photograph would be. If you believe the document to be under other copyright, please contact me.

The document should have been downloaded from my website https://blunham.com/, or any mirror site named on that site. If you downloaded it from elsewhere, please let me know (particularly if you were charged for it). You can contact me via my Genuki email page: https://www.genuki.org.uk/big/eng/YKS/various?recipient=colin

You may not copy the file for onward transmission of the data nor attempt to make monetary gain by the use of these files. If you want someone else to have a copy of the file, point them at the website. (https://blunham.com/Misc/Texas). **Please do not point them at the file itself as it may move or the site may be updated.**

It should be noted that most of the pages are identifiable as having been processed by me.

I put a lot of time into producing these files which is why you are met with this page when you open the file.

If you find missing pages, pages in the wrong order, anything else wrong with the file or simply want to make a comment, please drop me a line (see above).

It is my hope that you find the file of use to you.

Colin Hinson
In the village of Blunham, Bedfordshire.

TEXAS INSTRUMENTS

MICROSYSTEMS

Designers Handbook

MICROPROCESSOR SERIES™

2nd EDITION

CONTENTS

Section 1 The Texas Instruments Microsystem Range An Introduction

Section 2 Single-chip microcomputers

Section 3 Microprocessors

Section 4 Microcomputer boards

Section 5 Speech synthesis

Section 6 Development Systems and Software

Section 1 The Texas Instruments Microsystem Range: An Introduction

TEXAS INSTRUMENTS
offers you the complete
MICROSYSTEMS
CAPABILITY SPECTRUM

INTRODUCTION

It is safe to say choosing the required tools for designing microsystems can form a major and very important part of the development cycle.

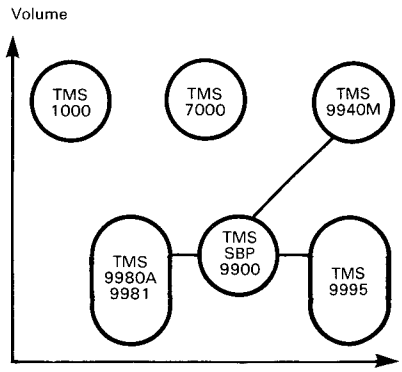
Time spent here can favourably influence the overall development period and to an extent the outcome of the project. Whether it be a one-off or volume-produced system, or whether it is regarded as a complex or relatively simple application task, the process of selecting the basic elements encompasses many non-technical and technical aspects.

This Microsystems Designers Handbook with its product per page approach provides the means for making an optimum first glance technical assessment of the suitability of the micro-related products available from Texas Instruments. If your interest is triggered then more detailed data is available to back up the relevant products you require to investigate.

The overall demands made of a system give a rough and ready, unwritten, designer's guide to the processing power needed by the central processor unit (CPU) to meet a given task. Such a guideline involves the number of bits the CPU needs to handle in parallel or at any one instant in time (i.e. simultaneously).

In initial project discussions you will hear remarks such as "yes, that really needs a 16-bit microprocessor" or "with the addition of these latest features it's too much for a 4-bit machine". For example high volume consumer applications, such as a washing machine say, attract 4-bit and 8-bit single chip microcomputers. Medium volume Point-of-Sale Terminals tend to need 8-bit microprocessors (i.e. multi-chip solution) whilst in medium to low volume areas such as numerical tool control a 16-bit microprocessor is the best choice.

Texas Instruments offer a very diverse and unmatched range of microprocessor components to meet the complexity spectrum of applications which are being tackled today.



The Performance/Volume Relationship of the Texas Instruments Microprocessor Families.

In brief terms there are three main microprocessor component families:

TMS 9900 MICROPROCESSOR FAMILY

1. TMS 9900 Microprocessor Family
A range of 16-bit microprocessors and single-chip microcomputers backed by a comprehensive set of support circuits.

The TMS 9900, introduced back in mid-1976, was the first 16-bit microprocessor to be produced by a major semiconductor manufacturer.

One of the key strengths of the 9900 family is the strict software compatibility (at instruction-set level) that exists between the members. This makes it a comforting choice for the user who may find for example the TMS 9900 is a gross overkill for the application task and can within certain constraints transport the software onto say the lower cost, slower-throughput, TMS 9980A/81. In the family is the SBP 9900A which is a direct functional copy of the TMS 9900 but in the more robust I^2L (Integrated Injection Logic) technology which enables it to meet military specifications.

The 9900 family also boasts the first 16-bit single chip microcomputer, TMS 9940M (masked part). For development only, there is the TMS 9940E (EPROM version).

To date there are numerous applications which have made use of the distinctive 9900 architectural features of context switching (ability to handle interrupts very fast) and the CRU I/O scheme (allows flexible bit manipulation very much akin to real world applications). The solutions adopted have withstood the microprocessor technology advances by competition.

With the TMS 9995 a number of common system functions have been integrated with the central processor function enabling 16-bit dedicated controller applications to be met by minimum package count but still retaining flexibility.

THE FUTURE OF THE 9900 FAMILY

Where is the 9900 family philosophy heading?

TMS 99000!

Well its the 99000 family a well thought out multi-processing network of highly intelligent functions. These functions are themselves based on fast 16-bit microprocessors similar in architecture to the 9900 family.

TMS 7000 MICROCOMPUTER FAMILY

2. TMS 7000 Single Chip Microcomputer Family
This is Texas Instruments newly-launched family of second generation 8-bit chip microcomputers. The instruction set features multiply, flexible I/O manipulation, BCD arithmetic, powerful register-to-register operations (total of 128 general purpose memory-mapped registers) and versatile memory addressing modes.

The 7000 offers the user the unique ability to reconfigure the instruction set by microprogramming the Micro-Code ROM thereby adapting a particular microcomputer for a given application task.

Experience of the family can be gained by using the TMS 7000 Evaluation Module which can also double up as an in-circuit emulator.

As with the next family the single chip microcomputers offered are for volume applications where the on-chip ROM is mask programmed. There are three base members of this new NMOS family TMS 7020 (2K bytes ROM), TMS 7040 (4K bytes ROM) and TMS 7000 itself (ROMless). The family has been designed, right down to the chip layout itself, to comprehend the future enhancements being planned. These include producing the 7000 family in an alternative technology such as CMOS.

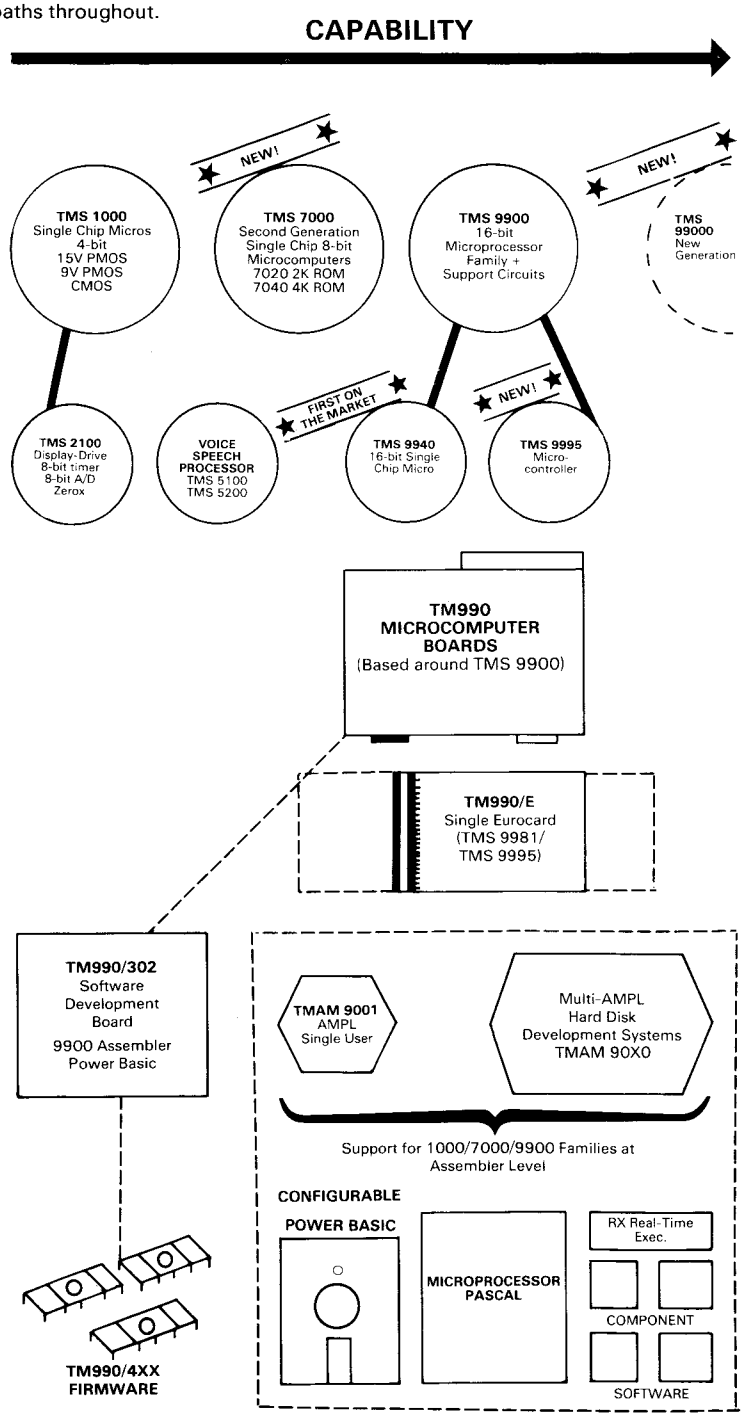
3. TMS 1000 Single Chip Microcomputer Family

Well established family of 4-bit microcontrollers offered with various capacities of ROM, RAM and I/O, and, in various semiconductor technologies such as PMOS, 9V PMOS and CMOS.

Major architectural enhancements have resulted in the TMS 2100 series. These include direct display drive, a/d converter, timer/event counter and zero crossing detector.

It is ill-advised for the designer to adopt the traditional 4/8/16-bit demarcation attitudes towards these Texas Instruments microprocessor families.

This is never better typified than by the TMS 9980A/81 microprocessor and the more recent TMS 9995, microcontroller which have 16-bit capability on-chip, but an 8-bit external data bus. In fact, the TMS 9995 has a faster-throughput than its parent, TMS 9900, microprocessor with its 16-bit data paths throughout.



Another example is the members of the TMS 7000 single chip microcomputer family which can be configured to be 8-bit microprocessors by setting an appropriate level on a particular pin (this is the TMS 7000 part itself).

With the TMS 7000 configured for peripheral expansion use can be made of some of the 9900 family support circuits. This is particularly true of the leadership. TMS 9914 GPIB IEEE-488 Adaptor (talker/listener/controller in one) and the unique TMS 9918A Video Display Processor (plus its derivatives TMS 9928, TMS 9929).

So the message is clear . . . particular attention needs to be paid in deriving the optimum solution from the products available.

Thought should also be given to the fact that the cost of the microprocessor is often a small part of the overall system cost and what was considered to be say a traditional 8-bit application would have best been tackled by 8/16-bitter such as the TMS 9980A/81 with the accompanying ease of use provided by the instruction set.

EASE OF USE?
COMPATIBILITY? √
DEV. TIME? *CORRECT*
S/W INVESTMENT?

Before leaving components mention should be made of Texas Instruments' leadership voice speech processor chips. Recent breakthroughs in synthetic speech, based on a technique called linear predictive coding (LPC), have breached the long standing barriers to high-quality low-cost solid state speech. All that is needed is the speech processor chip, a vocabulary ROM and an optional local intelligent microcomputer controller (otherwise service from host or central processor).

◄SPEECH SYNTHESIS

CAN YOUR DESIGN BENEFIT BY THE ADDITION OF SPEECH?

Two speech synthesis circuits are available:
1. **TMS 5100** – mainly for high volume and optimised for use with single chip microcomputer.
2. **TMS 5200** – low/medium volume; designed as a support circuit that can be easily driven by PIO or PIA part of a microprocessor based system.

Texas Instruments recognise that this existing technology is very much subjective and have made available a number of low-cost subsystems for evaluating speech (Tinytalker), for carrying out field trials and for cost effectiveness in low volume applications (Speech Library and EPSM).

Speech is radically changing the man/machine interface offering intelligent alarms, instructional commands, educational dialogues and such like in a diverse range of applications. Make sure you understand what it can do for you.

CAN SPEECH BE A USEFUL OPTION TO OFFER?

In addition to the 9900 family of components there is the TM990 range of microcomputer modules and firmware which are very attractive for applications where there is either

- insufficient time

or

- low volume requirements

or

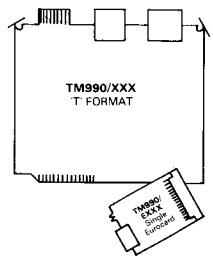
- limited hardware resources

or a combination of these factors.

◄TM990 MICROCOMPUTER MODULE RANGE

TWO RANGES

The TM990 range offers a do-it-yourself building block approach to solving your application. Based around the 16-bit 9900 microprocessor family the TM990 modules offer traditional minicomputer-type power for dedicated controller applications. These modules or supercomponents have been used in the actual end products manufactured (OEM typically 20 to 250 units); factory automation schemes as remote, intelligent, cost effective, stations, prototypes and test equipment to improve production.



There is the well established range of 'T' format size boards, TM990/XXX, which use the TMS 9900.

An alternative range of boards has recently been launched to complement the 'T' format. This is the TM990/EXXX range of single Euroboards (an internationally agreed standard) offering a highly modular/function approach to design. The boards are based on Texas Instruments' E-Bus which is a bus convention enabling multi-processing configurations. The Euroboards are centred around the TMS 9981 and the TMS 9995 processor. Both range of boards support distributed "ring main" style configurations running HDLC (High-Level Data Link Control) communication protocol.
('T' range: TM990/308 E-board range: TM990/E355)

DISTRIBUTED COMPUTING

Texas Instruments is fully committed to expand and fully support both board ranges.

If your application demands high speed precision computation there is the compatible TM990/1481 pair of boards emulating the 9900 architecture by the use of SN74S481 Schottky bit slices. The instruction set has been extended to support double precision (32-bit) and floating point arithmetic.

HIGH SPEED APPLICATION?

When it comes to writing software there is the low-cost development system available *within* the TM990 range which uses audio cassettes and allows programming of EPROM's. The TM990/302 Software Development Board, populated with the appropriate firmware, supports 9900 Assembler and Power BASIC programming.

LOW-COST SOFTWARE DEV. BOARD TM990/302

Another interesting member which is useful for evaluating the 9900 architecture or for training the design team is the standalone educational TM990/189M University Board complete with full tutorial text and user's guide.

MICROPROCESSOR TEACH YOURSELF KIT

Let us now turn our discussion to Development Systems (the "workbench") and Software Support (the "tools") which are an important consideration in any project.

◄DEVELOPMENT SYSTEMS

Important, because these represent a major investment in both money and people. Mistakes cannot be afforded.

Certain factors need to be assessed when looking at Development Systems:
1. Assistance in System Integration (when the application software is being made to run on the target hardware) by provision of in-circuit emulation facilities.

WHAT TO LOOK FOR IN A DEVELOPMENT SYSTEM?

2. Support for other microprocessors and microcomputers.
3. In addition to the expected assembler support the high-level language software support available.
4. The expandability of the system to cope with future requirements.
5. Other uses of the system when not developing target system software e.g. automatic test equipment, logic state analyser, general purpose minicomputer, speech synthesis verification.
6. After Sales Support.

Texas Instruments offers software development support at assembler level plus full in-circuit emulation facilities for the TMS 9900, TM990, TMS 7000 and TMS 1000 product families on the following development systems:

- TMAM 9001 – single user floppy disk.
- TMAM 9010, 9020 and 9040 – upgradable range of multi-user hard disk systems. They differ in size of memory, number of Video Display Terminals (users) and capacity of disk storage.

For 9900 target work and standalone logic state analyser operation there is the unique powerful interactive AMPL control language.

These are indeed universal development systems in a dedicated sort of way!

SOFTWARE ►

As mentioned previously the diverse 9900 microprocessor family has a strict software compatibility at the instruction set level and this goes a long way to:

- Preserving software investment (software is said to form up to 75% of mpu projects today).
- Optimising people resources – only need to train once.

HIGH-LEVEL LANGUAGES FOR TARGET SYSTEMS

This golden principle is further enhanced by the HLL's offered by Texas Instruments for the 9900/TM990 families. These are supplied in the form of easy-to-use self contained development packages. A unique feature is that account is taken of real world target system design constraints such as ROM/RAM partitioning, direct I/O manipulation, optimising interpreter overhead for a given application programme and allowing the designer to drop into assembler-type environment easily to handle say the time critical aspects of an application.

POWER BASIC

The Microprocessor HLL's available from TI are:

- **Power BASIC (Interpretive)**
  Easy to learn and very popular language. Has a number of extensions which enable full manipulation of the hardware resources of a 9900-based system. Can handle interrupts within its high-level environment or transparently in assembler language.
  It's supplied in the form of firmware for direct use on the TM990 range (Development Power BASIC) or on floppy disk for running on the Development Systems and optimising the final run-time interpreter support (Configurable Power BASIC).

MICROPROCESSOR PASCAL

- **Microprocessor PASCAL (MPP – Interpretive and Compilative Versions)**
  Pascal is gaining a great deal of popularity because it is a highly-disciplined structured language forcing the user to logically plan out the solution to his application. This in turn facilitates the future maintainability of the software.

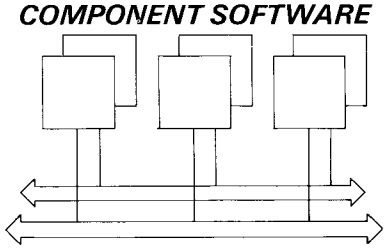
CONCURRENCY

MPP offers the customary features of the Pascal language but has a number of extensions which gives the designer that additional power to implement a solution quickly and reliably. One important extension is concurrency which allows the software to be written as a number of MPP processes (these are simply routines or collection of Pascal statements) each identifying with a particular hardware facility. MPP will run these processes concurrently and carry out the necessary organisation; there is no need to spend time writing an executive and inter-process communication procedures. If you remove a particular hardware facility you also remove the associated software process.

IN-CIRCUIT EMULATION DEBUGGING AT STATEMENT LEVEL

Another highly attractive feature is when you download your MPP programme using the in-circuit emulator onto the target system you can still debug and monitor at Pascal statement level. In other words you are able to debug the end application in the very same terms in which the application software was written. You do not have to resort to instructions and memory locations but stay with processes, statements, stack frames and so on.

COMPONENT SOFTWARE



SOFTWARE FUNCTIONS DIRECTLY RELATED TO HARDWARE FUNCTIONS

Also key to the overall strategy is Texas Instruments' Component Software where standard software components are selected to facilitate and speed up the implementation of microsystems. Complete source listings are supplied so the user can configure his own component with only those features necessary for his application.

Similar to hardware components these software components plug into a bus which in this case is called RX – Real Time Executive. An example of a TI software component is the EIA Communications Package which supports file level communication over multi-port EIA links.

The spectrum of capability available from TI is indeed vast We trust this Microsystems Designers Handbook will serve as a quick, easy-to-use, very informative reference guide and will occupy a permanent ready-to-pick-up place on the design bench.

OUR SUPPORT SERVICES ►

When you select a product then you can request more detailed data from the Customer Response Centre at our Bedford headquarters. Our resources do not stop there, you can discuss your requirements with our authorised distributors who operate TI Microsystem Design Centres. Additionally TI System Specialists are available to work in the field assisting in the design-in and development stages of the project.

TRAINING ►

To speed up that all important getting-started phase TI has a Microprocessor Training School offering extensive in-depth training courses on all aspects of our products.

Happy Designing!

Section 2 Single-chip microcomputers

AN INTRODUCTION TO THE TMS 1000

4-bit MICROCOMPUTER FAMILY

THE LOWEST COST SOLUTION

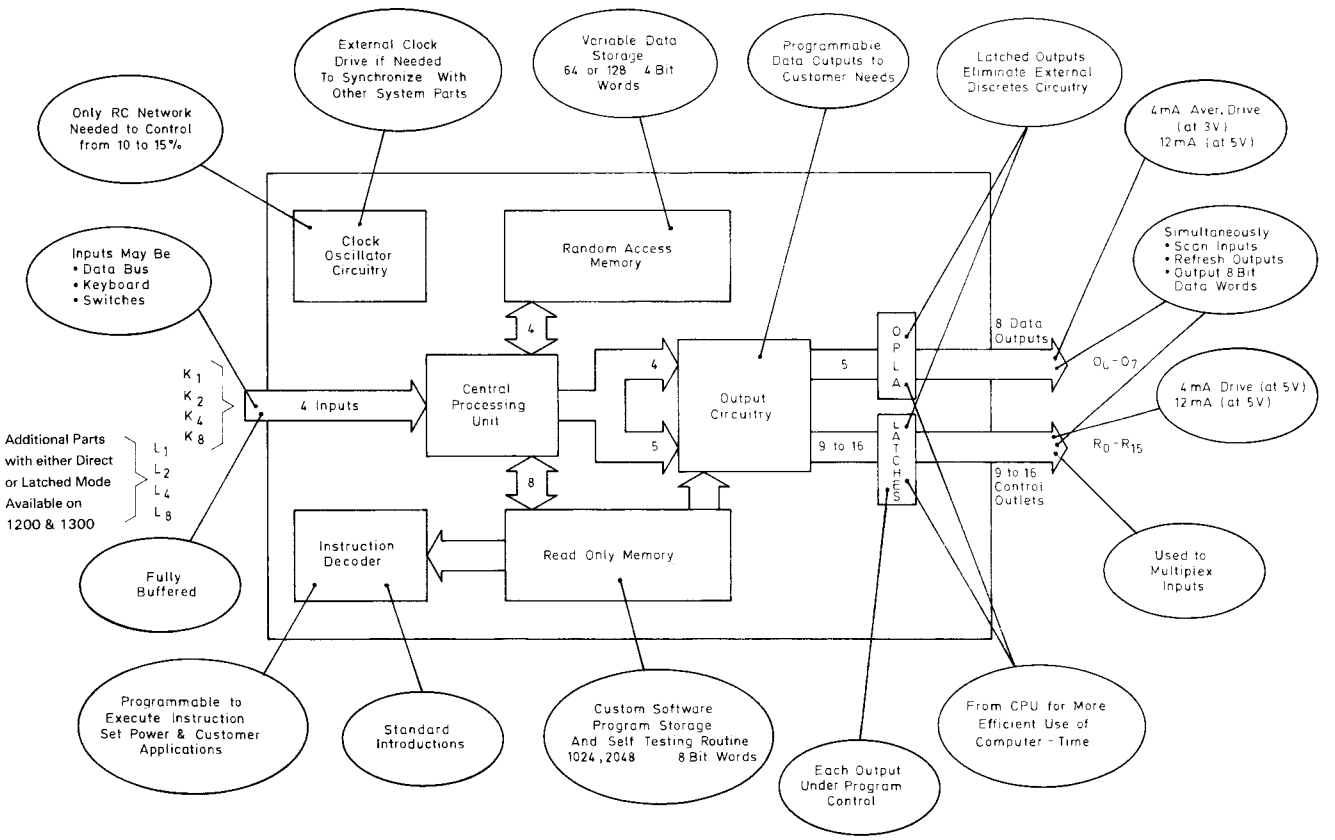
When your high volume (>5000 units) application involves a human-to-computer interface or a machine-to-computer interface, or a similar application with input/output speed restrictions, the TMS 1000 family will normally be the most cost-effective solution. A huge number of variants on the basic 4-bit architecture are available. Options include choice of memory size (0.5, 1, 2 or 4K ROM), variable amounts of I/O, vacuum fluorescent drive options, low power CMOS, A/D converters and many others. And a full complement of development aids are available.

Over 60 million TMS 1000 family units have been shipped worldwide, giving an unparalleled production experience and extremely high reliability.

ANATOMY OF A HIGH-VOLUME MICROCOMPUTER

The TMS 1000 series is a family of 4-bit microcomputers with a ROM, a RAM and an arithmetic logic unit on a single semiconductor chip. A customer's specification determines the software that is reproduced during wafer processing by a single-level mask technique that defines a fixed ROM pattern. The reference chart on the next page shows the various versions that are available so that a microcomputer can be chosen that best fits an application.

Block Diagram of CMOS Microcomputer



Quick Reference Guide

TMS 1000 Family

PART NUMBER		10XX	11XX	12XX	13XX	14XX	16XX	17XX
ROM 512 x 8 bits								P
1024 x 8 bits		P,L,C		P,L,C				
2048 x 8 bits			P,L,C		P,L,C			
4096 x 8 bits						P,L	P,L	
RAM 64 x 4 bits		P,L,C		P,L,C				
128 x bits			P,L,C		P,L,C			
OUTPUTS Port 1:	9 bit addressed							P
	10 bit addressed	C	C					
	11 bit addressed	P,L	P,L			P,L		
	13 bit addressed			P,L				
	16 bit addressed			C	P,L,C		P,L	
Port 2:	8 word addressed	P,L,C	P,L,C	P,L,C	P,L,C	P,L	P,L	P
	10 word addressed			1270P				
INPUTS Port 3:	4 level sensitive	P,L,C	P,L	P,L	P,L	P,L		P
	4 level + 4 edge sensitive			C	C		P,L	
SUBROUTINES	1 level, same page	P,L	P,L	P,L	P,L			P
	3 level any page	C	C	C	C	P,L	P,L	
OSCILLATOR	300 kHz	P,L,C	P,L	P,L,C	P,L			
	600 kHz	P,L,C	P,L,C	P,L,C	P,L,C	P,L	P,L	P
	1000 kHz	C	C	C	C			
SUPPLY	5V	C	C	C	C			
	9V	L	L	L	L	L	L	
	15V	P	P	P	P	P	P	P
I/O LEVELS	SUPPLY (XX00)	P,L,C	P,L,C	P,L,C	P,L,C	P,L	P,L	P
	30/35V (XX70)	P,L,C	P,C	P,L,C	P,C	P,L	P,L	P
PACKAGE	20 Pin							P
	28 Pin	P,L,C	P,L,C			P,L		P
	40 Pin			P,L,C	P,L,C		P,L	P

*P: PMOS L: LOW VOLTAGE PMOS C: CMOS

TMS 2100 Family

PART NUMBER		2100	2170	2300	2370
Package:	28 pin	√	√		
	40 pin			√	√
VF display interfacing			√		√
Analogue Input Lines	1	√	√		
	2			√	√
Independent Output Lines	7	√			
	6		√		
	15			√	
	14				√
Digital Input Lines	8	√	√		
	12			√	√

1K ROM
64 words RAM

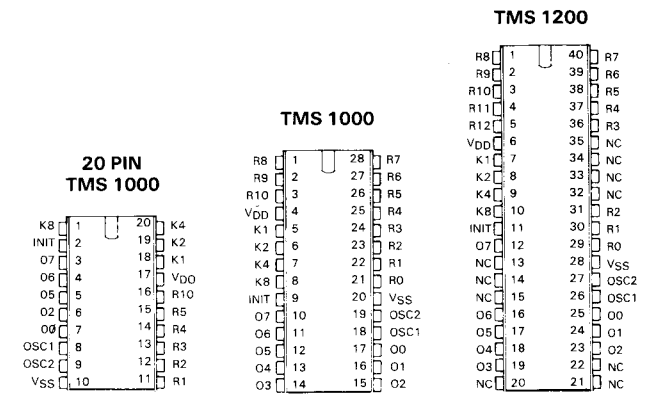
TMS 1000/1200

4-bit PMOS MICROCOMPUTER

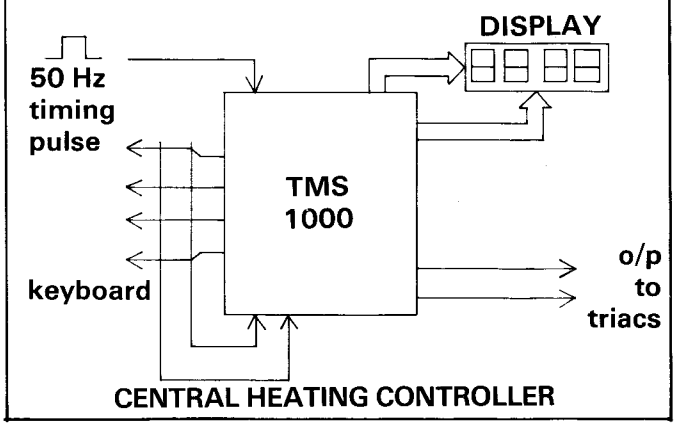
FEATURES:

- 1K of program memory.
- 64 nibbles of data memory.
- 20, 28 & 40 pin versions.
- Low-cost PMOS technology.
- 9V and 15V versions.

PIN ASSIGNMENTS:



TYPICAL APPLICATION:



DESCRIPTION:

TMS 1000 is the basic 1K ROM memory version of the TMS 1000 family suitable for a wide variety of microcontroller applications.

It is available in a 20-pin package for very cost sensitive applications with a reduced number of R & O lines.

It is very suitable for interfacing keyboards and displays for general purpose 'Human-Interface' applications.

HIGH VOLTAGE (Vacuum fluorescent drive) VERSION AVAILABLE ☑

CMOS version available ☑
SE Emulator SE-1 TMS 1099 JLP

CHARACTERISTICS:

Supply voltage	9 or 15V
Supply current	4 or 4.5 mA
Av. R output drive	14 mA
Av. O output drive	24 mA
Temp. range	0–70°C

ORDERING INFORMATION:

MP XXXX-1000 TLP – 20 pin plastic
MP XXXX-1000 NLP – 28 pin plastic
MP XXXX-1200 NLP – 40 pin plastic
MP XXXX-1070 NLP – 28 pin plastic
MP XXXX-1270 NLP – 40 pin plastic

These parts are available in 400 and 600 mil plastic packages and 600 mil ceramic

TMS 1100/1300

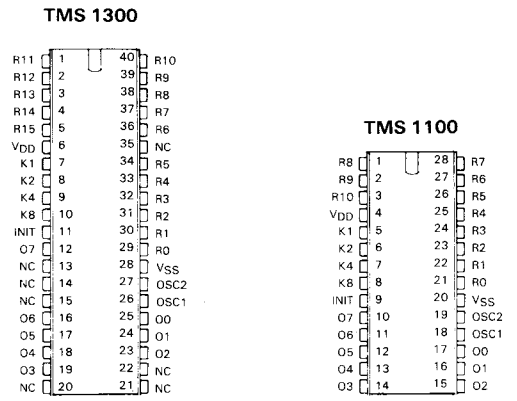
2K ROM
128 words RAM

4-bit PMOS MICROCOMPUTER

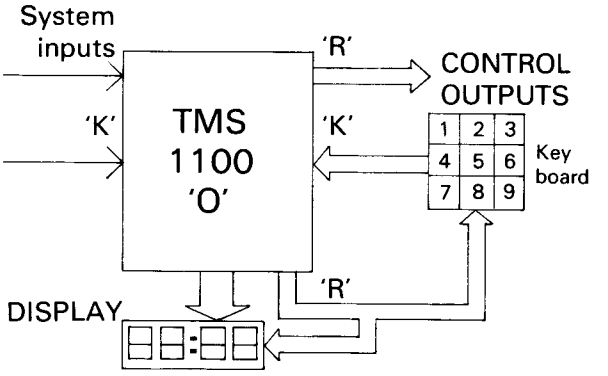
FEATURES:

- **2K words of program ROM.**
- **128 nibbles of data memory.**
- **28 or 40 pin versions.**
- **9V and 15V versions.**
- **Low-cost PMOS technology.**

PIN ASSIGNMENTS:



TYPICAL APPLICATION:



DESCRIPTION:

For applications where the 1K program memory of the TMS 1000 is not sufficient, TMS 1100 may be used. It also offers twice the amount of RAM.
Since it is a pin-for-pin compatible device, upgrading from TMS 1000 to TMS 1100 entails no PCB layout changes.
The TMS 1100 has a slightly modified instruction set to allow it to address twice the amount of ROM.

HIGH VOLTAGE (Vacuum fluorescent drive) VERSION AVAILABLE ☑

CMOS version available
SE Emulator SE-2 TMS 1098 JLP ☑

CHARACTERISTICS:

Supply voltage	9 or 15V
Supply current (typ.)	5 or 7 mA
Av. R output drive	14 mA
Av. O output drive	24 mA
Temp. range	0–70°C

ORDERING INFORMATION:

MP XXXX-1100 NLP
MP XXXX-1300 NLP

MP XXXX-1170 NLP
MP XXXX-1370 NLP
} High voltage output versions

These parts are available in 400 and 600 mil plastic packages and 600 mil ceramic

4K ROM
128 words RAM

TMS 1400/1600/1470/1670

4-bit PMOS MICROCOMPUTER

FEATURES:

- 4K of program memory.
- 128 nibbles of data memory.
- 3 levels of subroutine.
- Mask programmable frequency divider on K8; four selectable options ÷ 1, 2, 10 or 20.
- 28 or 40 pin version.
- 4 latched and 4 unlatched inputs on 40 pin version.

DESCRIPTION:

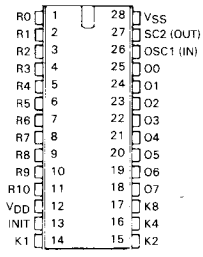
The TMS 1400/1600 offer the largest program memory size of the TMS 1000 family, for programs requiring more complex features or a larger number of features than can be handled by TMS 1100/1300. The on-board frequency divider reduces external hardware and simplifies many closed loop control systems. The devices are available in 9 or 15V PMOS only.

CHARACTERISTICS:

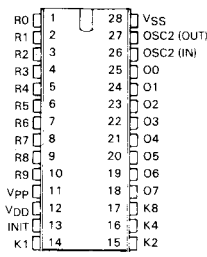
Supply voltage (av.)	0, –9V
Supply current (av.) typ.	7 mA
Max. R output drive (av.)	14 mA
Max. O output drive (av.)	24 mA
Temp. range	0–70°C

PIN ASSIGNMENTS:

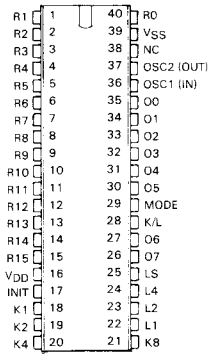
TMS 1400



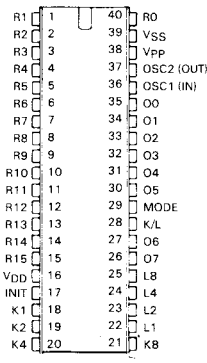
TMS 1470



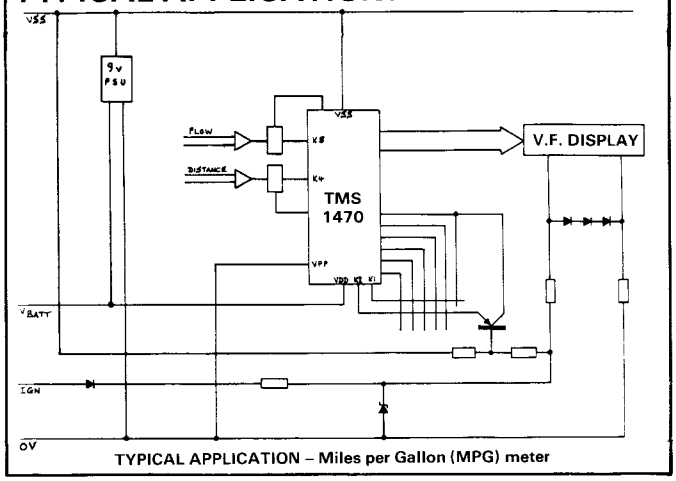
TMS 1600



TMS 1670



TYPICAL APPLICATION:



TYPICAL APPLICATION – Miles per Gallon (MPG) meter

HIGH VOLTAGE (Vacuum fluorescent drive) VERSION AVAILABLE ☑

CMOS version available ☒
SE Emulator SE-5 TMS 1097 JLP

ORDERING INFORMATION:

(600 mil plastic package)

MP XXXX-1400 NLL
MP XXXX-1400 NLP
MP XXXX-1600 NLP
MP XXXX-1600 NLL

MP XXXX-1470 NLL
MP XXXX-1470 NLP
MP XXXX-1670 NLP
MP XXXX-1470 NLL

TMS 1700

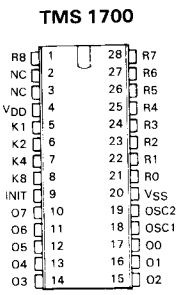
0.5K ROM
32 words RAM

4-bit PMOS MICROCOMPUTER

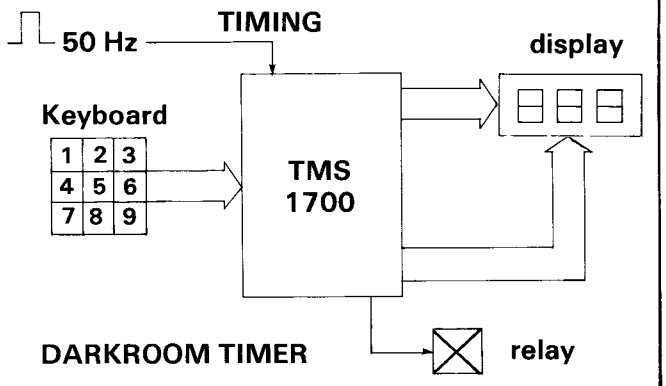
FEATURES:

- **Minimum cost microcomputer.**
- **0.5K program memory.**
- **32 nibbles of data memory.**
- **Available in 20 or 28 pin DIL package.**

PIN ASSIGNMENTS:



TYPICAL APPLICATION:



DESCRIPTION:

Lowest cost member of TMS 1000 family, the TMS 1700 is suitable for simple applications requiring a minimum of program memory. For example it could be programmed as a simple sound generator.

The TMS 1700 is available only in PMOS.

HIGH VOLTAGE (Vacuum fluorescent drive) VERSION AVAILABLE ☑

CMOS version available ☒
SE Emulator SE-1 TMS 1099 JDL

CHARACTERISTICS:

Supply voltage (typ.)	9 or 15V
Supply current (typ.)	4 or 4.5 mA
Max. R output drive	28 mA
Max. O output drive	14 mA
Temp. range	0–70°C

ORDERING INFORMATION:

MP XXXX-1700 NLP

These parts are available in 400 and 600 mil plastic packages and 300 mil 20 pin.

2K ROM
128 words RAM

TMS 2100/2300/2170/2370

4-bit PMOS MICROCOMPUTER

FEATURES:

- On-chip A/D converter with 200μS sample time.
- 1 or 2 analog inputs.
- Event counter/interval timer.
- Zero crossing detector with noise debounce.
- Frequency divider on K8 input.
- Interrupt.
- 3 levels of subroutine.

DESCRIPTION:

The top performance version of the TMS 1000 family, the TMS 2100 is well suited to all types of motor speed control or other applications involving phase control of triacs or similar.

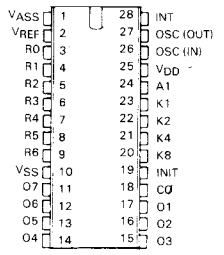
The interrupt and timer facilities allow the 4-bit machine to perform a number of tasks normally associated with an 8-bit processor. TMS 2100 is only available in PMOS.

CHARACTERISTICS:

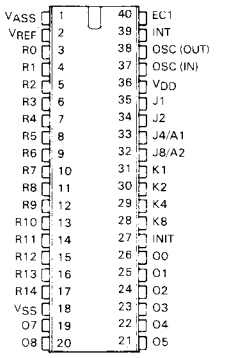
Supply voltage (typ.)	9V
Supply current (typ.)	9 mA
Max. R output drive	28 mA
Max. O output drive	48 mA
Temp. range	0–70°C

PIN ASSIGNMENTS:

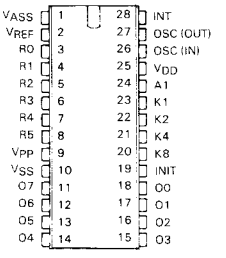
TMS 2100



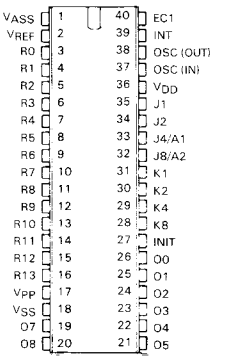
TMS 2300



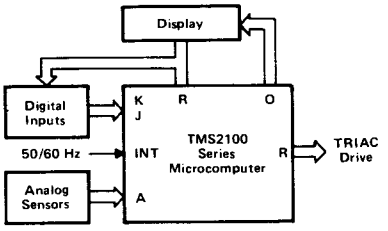
TMS 2170

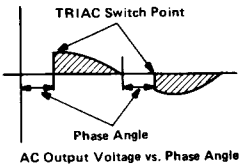


TMS 2370



TYPICAL APPLICATION:





AC Output Voltage vs. Phase Angle

AC POWER CONTROL

HIGH VOLTAGE (Vacuum fluorescent drive) VERSION AVAILABLE ☑

CMOS version available ☒

ORDERING INFORMATION:

MP XXXX-2100 NLP – 28 pin
MP XXXX-2300 NLP – 40 pin
MP XXXX-2170 NLP – 28 pin
MP XXXX-2370 NLP – 40 pin

These parts are available in 400 and 600 mil plastic packages and 600 mil ceramic.

TMS 1000C/1200C/ 1100C/1300C

1K & 2K ROM 64 & 128 words RAM

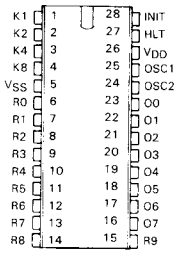
4-bit CMOS MICROCOMPUTERS

FEATURES: (in addition to PMOS)

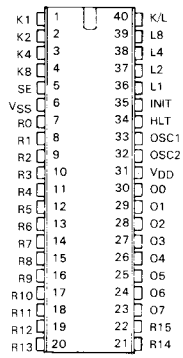
- **Low Power Consumption:**
  Normal operation ..... 3.5 mW
  Standby mode (memory retained) ..5μW
- **3V operating Voltage minimum.**
- **3 levels of subroutine.**
- **28 and 40 pin DIL versions.**
- **40 pin version has latched inputs.**
- **Clock frequency of up to 1MHz for faster operation.**

PIN ASSIGNMENTS:

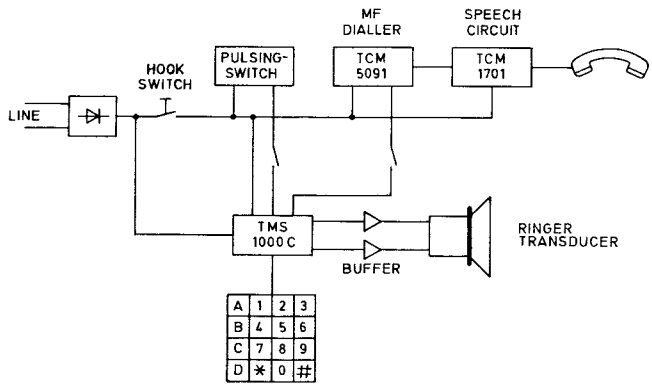
TMS 1000/1100C



TMS 1200/1300C



TYPICAL APPLICATION:



PULSE DIAL TELEPHONE with NUMBER STORAGE FACILITIES

DESCRIPTION

These CMOS microcomputers offer the advantages of low voltage and low power. For example they may be used in battery powered products for long life, or directly powered from a telephone line. The ability to operate in the standby (or HALT) mode enables the contents of the RAM to be saved when the unit is not operating, only using 5μW.

CHARACTERISTICS:

	TMS 1000 C	TMS 1200 C	TMS 1100 C	TMS 1300 C	TMS 1 x 70 C	
Pkg. pin count	28 pins	40 pins	28 pins	40 pins	28 pins	40 pins
Instruction ROM	1024 x 8 bits		2048 x 8 bits		1024 x 8 bits	2048 x 8 bits
Data RAM	64 x 4 bits		128 x 4 bits		64 x 4 bits	128 x 4 bits
"R" individually addressed output latches	10	16	10	16	10	16
Max. rated voltage (O, R and K)	6 V		6 V		-30 V to +7 V	
Data inputs	4	8	4	8	4	8	4	8
Instruction set	43		43		43	
Power supply	3–6 V		3–6 V		3–6 V	
Typ. dissipation	3.5 mV		5 mW		5 mW	
Clock frequency	1 MHz max.		1 MHz max.		1 MHz max.	
Subroutine levels	3		3		3	
Halt (power down)	Yes (5 μW)		Yes (5 μW)		Yes (5 μW)	
Temp. range	0–70°C					

HIGH VOLTAGE (Vacuum fluorescent drive) VERSION AVAILABLE ☑

SE Emulators:
SE-3 TMS 1099 JLC
SE-4 TMS 1098 JLC

ORDERING INFORMATION:

MP XXXX-1000 NLC
MP XXXX-1200 NLC
MP XXXX-1100 NLC
MP XXXX-1300 NLC
MP XXXX-1070 NLC
MP XXXX-1270 NLC
MP XXXX-1170 NLC
MP XXXX-1370 NLC

Note:
SE-3 is used for emulation of TMS 1000C and TMS 1200C; SE-4 is used fo. TMS 1100C and TMS 1300C.

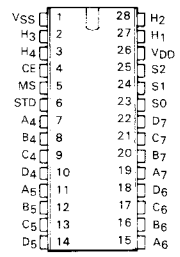
These parts are available in 400 and 600 mil plastic packages and 600 mil ceramic.

FEATURES:

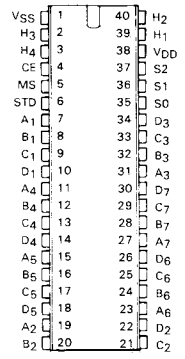
- **Four or seven 4-bit I/O ports with latched output.**
- **Static operation.**
- **Compatible with TMS 1000 family.**
- **Chip enable to allow connection of several expanders in parallel.**
- **PMOS or CMOS technology.**
- **TTL compatible.**
- **Low power consumption.**

PIN ASSIGNMENTS:

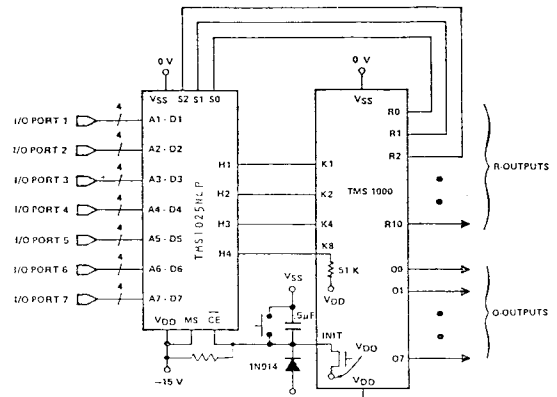
TMS 1024 NLP
TMS 1024 NLL



TMS 1025 NLP
TMS 1025 NLL

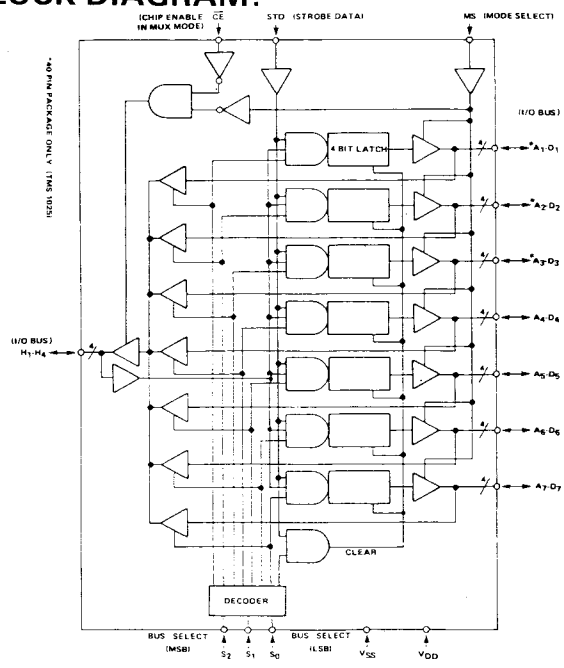


TYPICAL APPLICATION:



INPUT EXPANSION USING THE TMS 1025

BLOCK DIAGRAM:



DESCRIPTION:

TMS 1024/5 are designed to extend the input/output capability of the TMS 1000 family. Depending on package size (28 or 40 pin) they give 4 to 16 line expansion or 4 to 28 I/O lines. The expansion lines may be configured as either input or output; and because of their static operation offer a 28-bit storage capability.

Both 9V and 15V versions are available in PMOS, there is also a 5V CMOS version.

CHARACTERISTICS:

	Low Power TMS 1024 NLL	Standard TMS 1024 NLL	Low Power TMS 1025 NLL	Standard TMS 1025 NLP
Package Pin Count	28 Pin		40 Pin	
Multiplexer Mode	16-line to 4-line		28-line to 4-line	
Chip enable	Yes		Yes	
Latch Mode	Four 4-bit Storage		Seven 4-bit Storage	
Clear Function	Yes		Yes	
Power Supply/ Typical Dissipation	-9V/22.5mW	-15V/60mW	-9V/22.5mW	-15V/60mW
Operating Temp. range	0–70°C			

HIGH VOLTAGE OUTPUT (Vacuum fluorescent drive) VERSION AVAILABLE ☒

CMOS VERSION AVAILABLE ☑

ORDERING INFORMATION: (600 mil plastic package)

TMS 1024 NLP: Standard PMOS
TMS 1024 NLL: Low power PMOS
TMS 1024 NLC: CMOS

TMS 1025 NLP: Standard PMOS
TMS 1025 NLL: Low power PMOS
TMS 1025 NLC: CMOS

The PMOS devices are also available in 400 mil packages: signified by an S in the first letter of the suffix eg TMS 1024 SLL.

SE-1 to SE-5

SYSTEM EMULATOR CHIPS

FEATURES:

- **True emulation of masked microcomputers.**
- **Extra status and control lines that are useful in debugging.**

DESCRIPTION:

These emulators are TMS 1000 family devices which are configured to work with an external program memory (usually in Eprom form) and an external Output Programmable Logic Array (usually a bipolar prom.).

These are the only differences between an SE device and the appropriate masked microcomputer.

High voltage devices are emulated by putting one transistor on each input or output line.

SE-1 = TMS 1000/1200 } same
SE-2 = TMS 1100/1300 } pinout
SE-3 = TMS 1000C/1200C } same
SE-4 = TMS 1100C/1300C } pinout
SE-5 = TMS 1400/1600
SE-6 = TMS 2100/2300

System Emulation devices have the following part numbers:

SE-1 = TMS 1099 JLP
SE-2 = TMS 1098 JLP
SE-3 = TMS 1099 JLC
SE-4 = TMS 1098 JLC
SE-5 = TMS 1097 JLP
SE-6 = TMS 1096 JLP

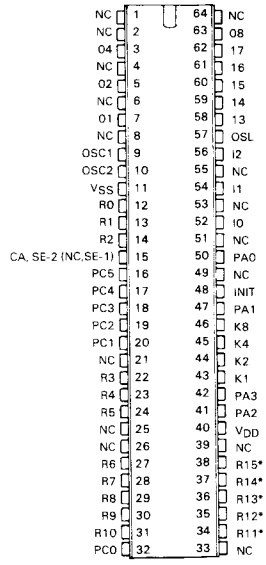
Note: All SE devices are available only in 64 pin ceramic packages.

Any TMS 1000 family microcomputer can be emulated by designing an SE device, Eprom and OPLA Prom into the prototype concerned. However, development is greatly simplified by using a System Emulation Board, which has these, and other components, on board, and then connecting the SEB to the prototype by a 28 or 40 pin connector.

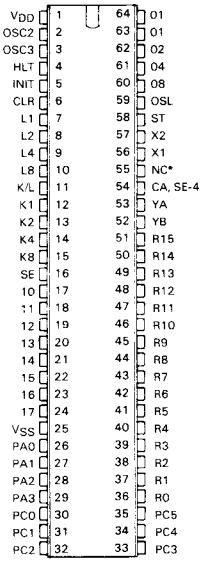
For details on the range of SEB's available, see the Section on Emulator Boards.

PIN ASSIGNMENTS

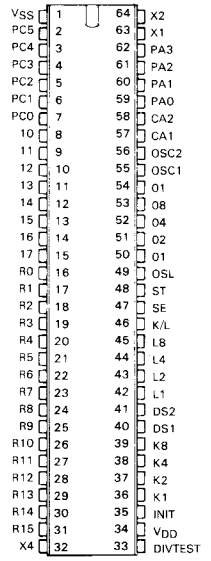
SE-1 and SE-2



SE-3 and SE-4

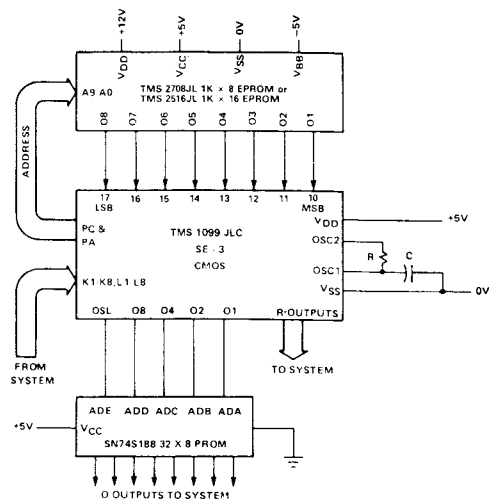


SE-5 TMS 1097 JLP



*The user determines which R outputs are appropriate for a specified device emulation. Note the device descriptions.
NC – NO INTERNAL CONNECTION

BLOCK DIAGRAM:



TMS 1121/1122

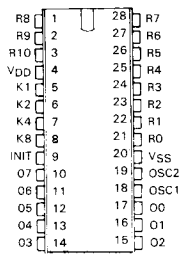
UNIVERSAL TIMER CONTROLLER

FEATURES:

- 4 independent switch outputs.
- 18 daily or weekly times.
- Display of day of week, am/pm, output status, on/off/sleep status.
- 4 digit display.
- 50 Hz or 60 Hz operation.

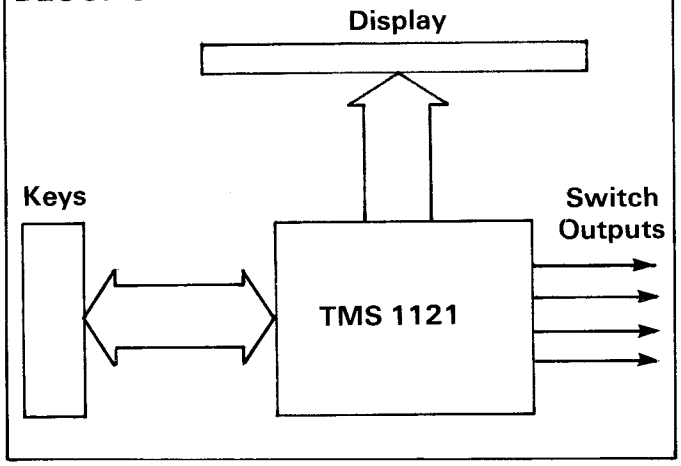
PIN ASSIGNMENTS:

TMS 1121



R7–R10 are the user-defined outputs.

BLOCK DIAGRAM:



Reference Manual: 'TMS 1121/2 Universal Timer Control Manual'.

DESCRIPTION:

Program time-setting and switch selection is entered via the keyboard.

A 4 digit display and 18 individual LED's display system status.

Timing is derived from a 50 or 60 Hz mains input, according to a link-option switch.

TMS 1121 is a 12 hour clock; TMS 1122 is a 24 hour clock.

CHARACTERISTICS:

Supply voltage	9V
Typical supply current	5 mA
Max. R output drive	28 mA
Temp. range	0–70°C

ORDERING INFORMATION:

Part No. **TMS 1121 NLL** **TMS 1122 NLL**

TMS 1601 NLL

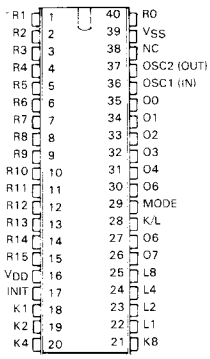
PMOS CONTROLLER/TIMER

FEATURES

- 4 independent switch outputs.
- 28 weekly times.
- 4 daily times.
- 24 hour clock on 4-digit display.
- 7 day sequence, or shorter.

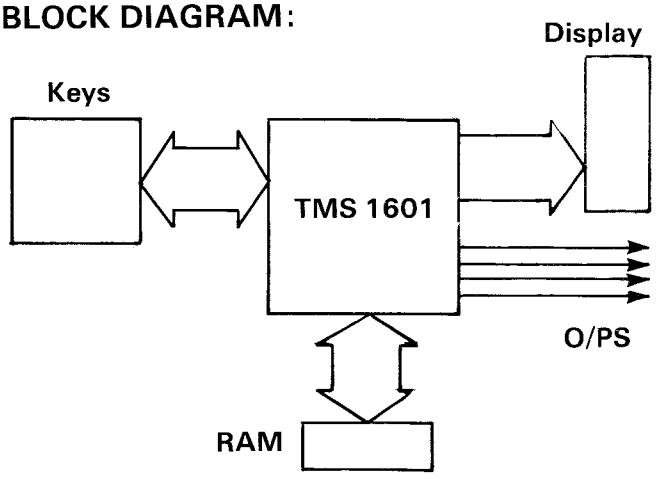
PIN ASSIGNMENTS:

TMS 1601



R12–R15 are the outputs which are controlled by the user.

BLOCK DIAGRAM:



Reference Manual: 'TMS 1601 NL Controller/Timer User Guide'.

DESCRIPTION:

The TMS 1601 is a pre-programmed microcomputer from the TMS 1000 family. It controls 4 outputs according to switch times which are entered via a keyboard and stored in an external RAM memory.

The outputs are controlled by time of day or week and the state of each output, and the system as a whole is displayed using a 4-digit LED display and 19 individual LED's. Timing is derived from a 50 Hz mains input.

CHARACTERISTICS:

Supply voltage	9V
Typical supply current	11 mA
Max. R output drive	28 mA
Temp. range	0–70°C

ORDERING INFORMATION:

Part No. **TMS 1601 NLL**

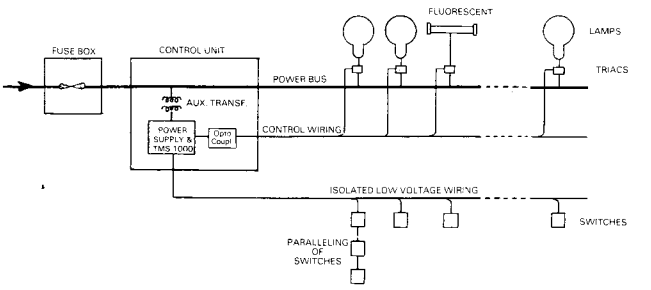
TMS 1019

MICROPROCESSOR BASED LIGHTING SYSTEM

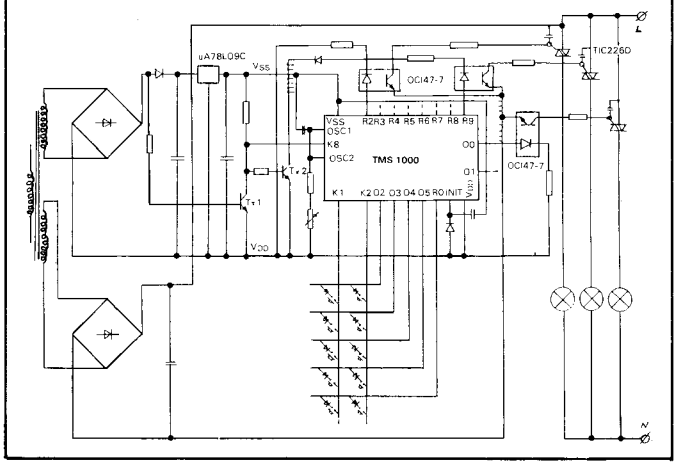
FEATURES:

- **8 lamps on/off, incandescent or fluorescent.**
- **2 dimmer lamps.**
- **1 lamp with timed fading.**
- **1 lamp for intruder alarm or flash light communication.**
- **Addition of further TMS 1000 increases number of controlled lamps to 24.**
- **Low voltage switches (9V, 1 mA isolated) are completely safe and easy to parallel up to same lamp.**
- **Zero-voltage switching prolongs life of incandescent lamps.**

SYSTEM BLOCK DIAGRAM:



TYPICAL APPLICATION:



DESCRIPTION:

The TMS 1019 is a pre-programmed microcomputer which controls up to 12 lamps according to push buttons.

Variations in brightness are achieved by adjusting the triac firing angle – there is one triac for each lamp in the system.

All wiring to and from wall switches is low voltage and isolated (mains is supplied only to the ceiling rose) so, compared with conventional lighting systems, cheaper wire is used without sacrificing the safety advantage.

ORDERING INFORMATION:

Part No. TMS 1019 NLL

A complete kit of parts for this application is available: The order code is NLL 700.

FEATURES:

- **True emulation of masked micro-computers.**
- **Single power supply operation (9V or 15V selected by a link).**
- **Uses 25XX Eproms.**
- **Easy to change the value of pulldown resistors.**
- **Adjustable clock speed.**
- **Emulates High Voltage (1 × 70) devices without any modifications.**
- **Dimensions only 160 × 100mm.**

DESCRIPTION:

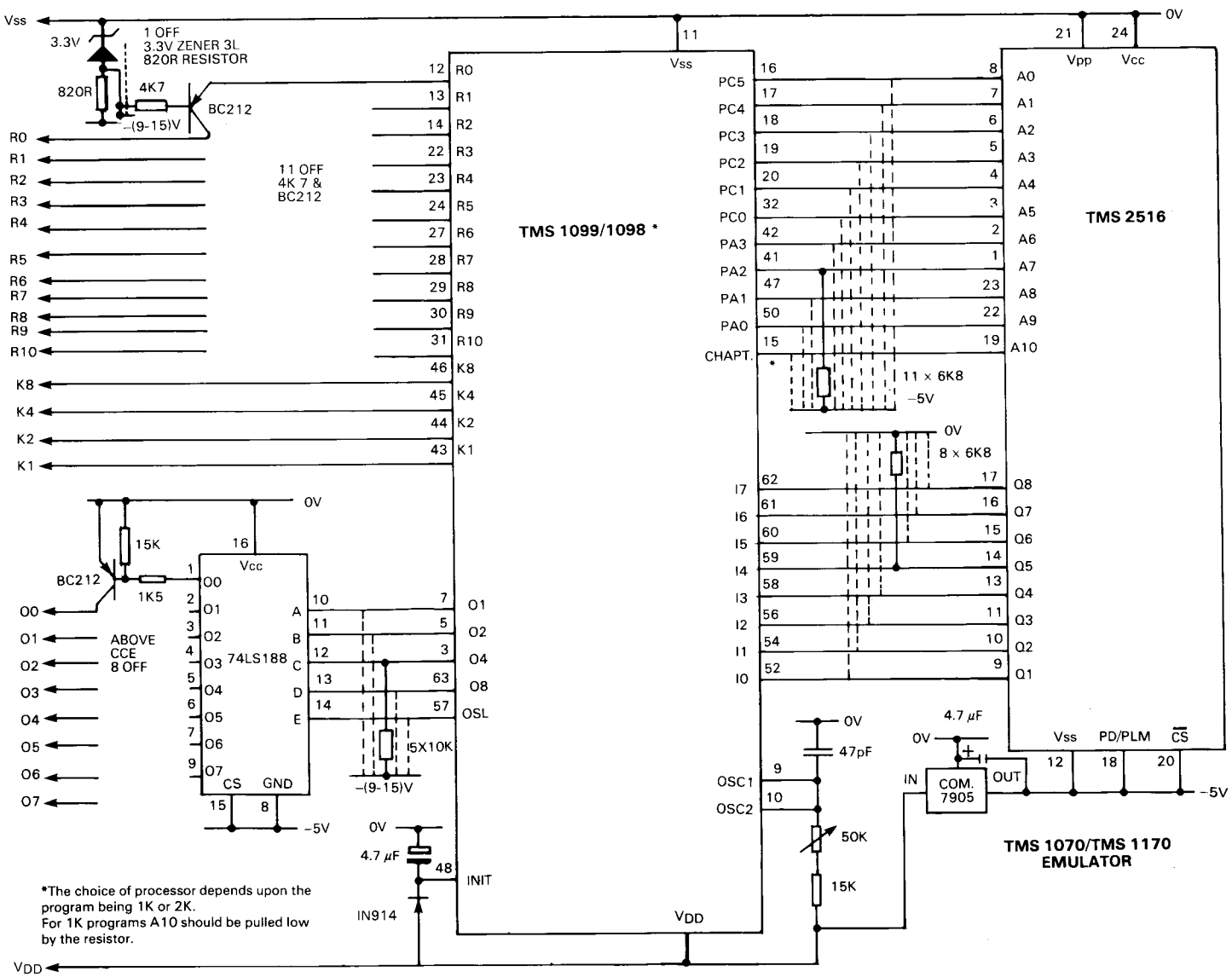
SEB's are populated PCB's which emulate TMS 1000 microcomputers.

SEB 1 = TMS 1000/1070/1200/1270/1100/1170/1300/1370.
SEB 2 = TMS 1400/1470/1600/1670.
SEB 3 = TMS 1000C/1200C/1100C/1300C.

They contain all the components which are fabricated onto the masked microcomputer. The only major difference between SEB's is that the SEB 2 has 2 extra links for setting the ratio for the divider on the K8 input.

All SEB's have a 40 pin double sided edge connector for linking to the prototype board.

CIRCUIT DIAGRAM FOR SEB 1:



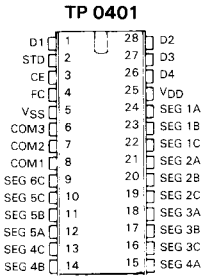
TP 0401

LIQUID CRYSTAL DISPLAY DRIVER

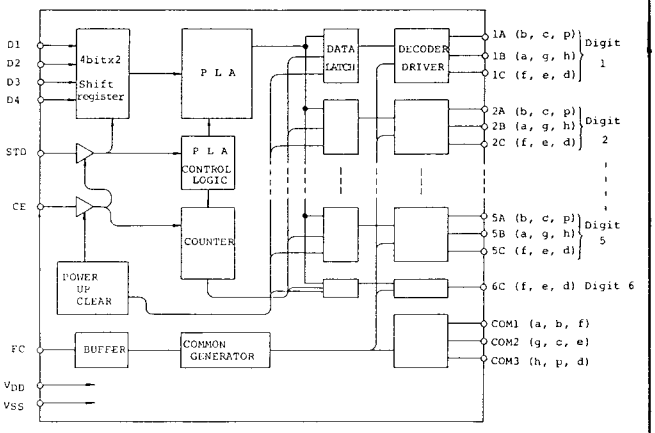
FEATURES:

- **$5\frac{1}{3}$ digit, 9 segment direct drive LCD driver.**
- **Latched outputs.**
- **CMOS technology.**
- **28 pin package.**
- **Compatible with TMS 1000 family.**

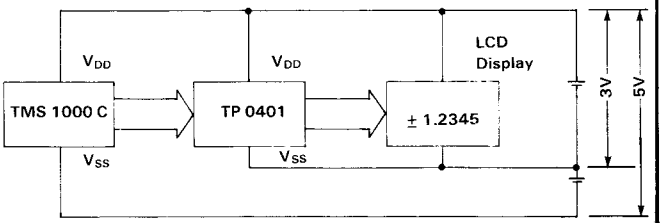
PIN ASSIGNMENT:



BLOCK DIAGRAM:



TYPICAL APPLICATION:



DESCRIPTION:

The TP 0401 can directly drive LIQUID CRYSTAL DISPLAYS, under the control of a microprocessor, eg TMS 1000. It uses a chip enable, strobe data, frame clock and 4 data inputs to achieve this operation.

Since it is fabricated in CMOS it's power and voltage requirements are very low. It is available only in CMOS.

CHARACTERISTICS:

Supply voltage (typ.)	3V
Supply current (typ.)	20 μA
Frame frequency range	100 to 400 Hz
Input current	$\pm$0.1 mA
Temp. range	0–70°C

ORDERING INFORMATION:

Order code: TP 0401

Available in 28 pin 400 or 600 mil package.

1. Display

Can strobe on LED or Vacuum Fluorescent Display of as many digits as the appropriate microcomputer has R lines. Each digit may have 8 segments – usually configured as 7 plus a decimal point.

2. Keyboard

Without any external hardware, the biggest keyboard which can be handled is: 4xn, where n is the number of available R lines.

Note: If the number of digits in the display is greater than or equal to the number of keyboard columns, then R lines can be made to perform both functions (Fig. 1), otherwise it may be necessary to use O lines to scan the keyboard, in the space between turning off one digit and turning on the next.

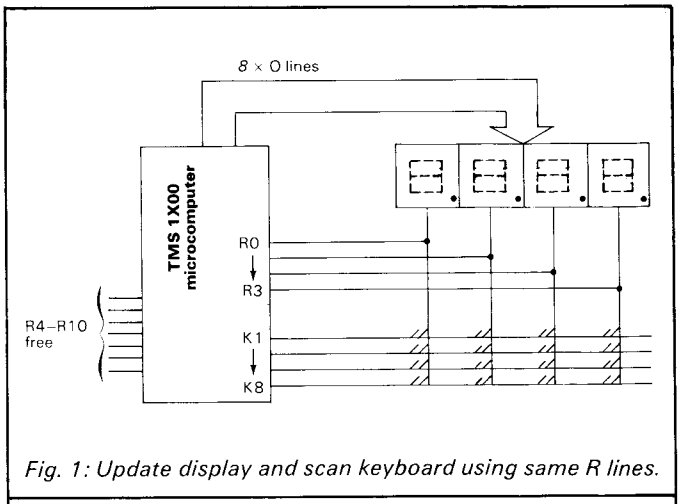


Fig. 1: Update display and scan keyboard using same R lines.

3. Automatic Power Down and/or Halt

If V_{DD} is configured as Fig. 2, then power up is achieved by pushing a button, where upon Rx is set high. In order to power down under program control, Rx is set low.

The "Halt" Mode (CMOS parts only) may be implemented under program control as shown in Fig. 2. When the "restart" button is pressed, program execution continues, and Ry is immediately set low.

4. Controlling External RAM

External RAM is often useful for long-term storage of data, especially if CMOS RAM is used.

This can be achieved using only 4 input lines and 1 input line as shown in Fig. 2.

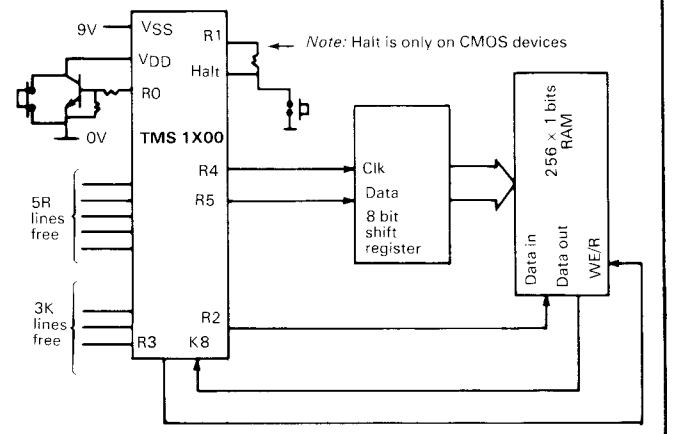


Fig. 2: Automatic Power down/Halt and External RAM.

5. Use of Link-options

One masked microcomputer can be made to perform a variety of different functions by putting more than one program inside it. The desired function can then be selected by external switches, usually diode links on the PCB.

6. A/D Conversion

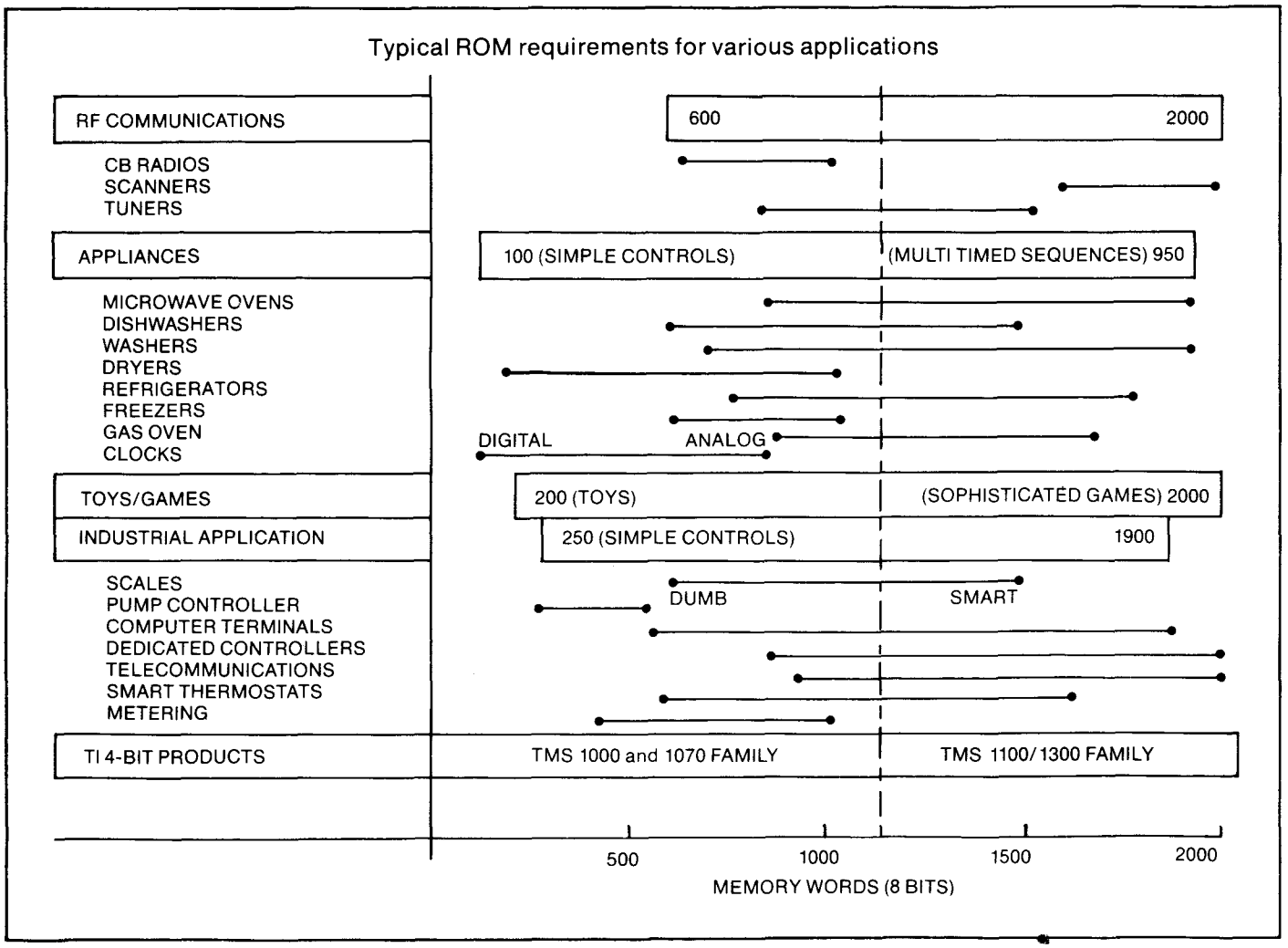
If A/D conversions are required and a TMS 2100 series microcomputer is not suitable, an external A/D conversion chip (either TL505 or TL507) can be used. Controlling either of these requires only 2 ouput lines and 1 input line.

7. Speech Synthesis

Any TMS 1000 microcomputer can control the TMS 5100 speech synthesis chip: I/O requirements are normally 5 output lines and 1 input line.

Applications

The users of the TMS 1000 Family are many and varied. Depending upon the speed required, input/output interface, desired power supplies, a wide range of products can be served. To show some typical examples, the chart below plots application vs. typical read-only-memory (ROM) requirement of those applications to show the wide range and variety of products covered by the TMS 1000 family.



Applications of TMS 1000 series Microcomputers

Electro/Mechanical
- Accounting Machine
- Air Conditioner
- Alarm
- Annunciator
- Appliance Timer
- Beverage Dispensing
- Coin Changer
- Central Clock System
- Cash Register
- Copy Machine
- Door Chimes
- Electronic Balance
- Fax Equipment
- Fuel Metering
- Pin Ball Machine
- Games
- Gas Cooker
- Gas Pumps
- Juke Box
- Photo Processing
- Oven Control
- Microwave Oven Control
- Scales
- Temperature Controller
- Taxi Meter
- Thermometer
- Washing Machine
- Vending Machine

Electronic
- Automatic Telephone Answering
- Automatic Telephone Recording
- Auto Dialer
- Automotive Tester
- CPU Front Panel
- Commercial Building Security
- Decibel Meter
- Digital Voltmeter
- Engine Diagnostic Tester
- Evaluator Control
- ECR Equipment
- Fixed Communication Equipment
- Keyboard Encoder
- Line Control
- M/G Transceiver
- Mobile Telephone
- Measurement Instrument
- PBX Equipment
- PBX Line Compressor
- Pressure Display
- Security System
- Talking Calculator
- Traffic Control
- TV Encoder/Decoder
- TV Programmer
- Numerical Control Display

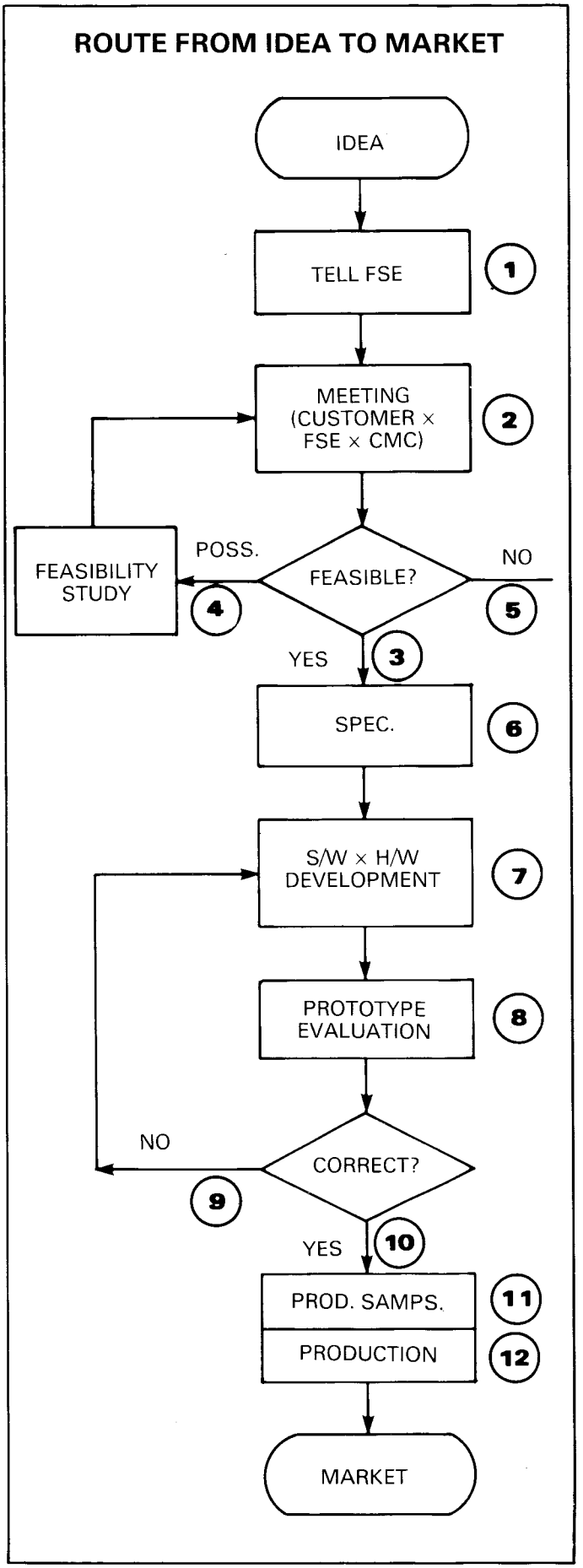
Distributed Computing
- Communication Channel Switch
- Data Collection Equipment
- Hand Held Speedometer
- P.O.S. Terminal
- Printer Terminal

Timescales

(4) Feasibility studies are usually less than 2 weeks long and can be free of charge.

(6, 7, 8) This is the time between agreeing a specification and demonstrating a complete prototype. It ranges from approximately 8 weeks for a standard 1K program to 20 weeks for a complex 4K program.

(11) Once the customer has checked out the program, masked samples can be produced in approximately 12 weeks.



Packages/Reliability

FEATURES:

- **20 pin 0.3" package with 0.1" spacing.**
- **28 pin 0.6" package with 0.1" spacing.**
- **28 pin 0.4" package with 0.07" spacing.**
- **40 pin 0.6" package with 0.1" spacing.**
- **40 pin 0.6" package with 0.07" spacing.**
- **0.05%/1000 failure rate.**

DESCRIPTION:

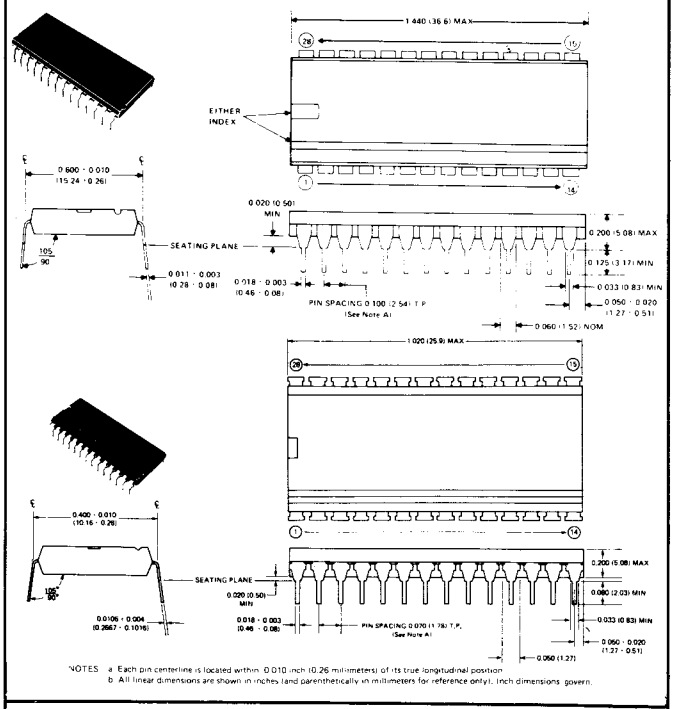
Most of the devices in the TMS 1000 family are available in a wide variety of packages.

Shrunk packages (0.07" pin spacing) are very useful in any application where board area is at a premium.

High Reliability

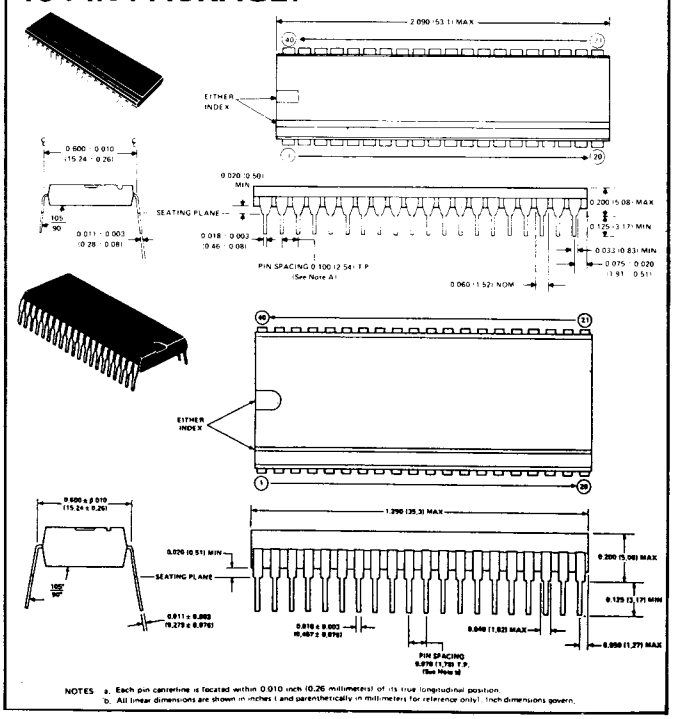
Reliability of TI's PMOS TMS 1000 Series is demonstrated by an attained failure rate of 0.05%/1000 hours now! Six years and millions of devices experience pays off in long system life and minimal service expense. The TMS 1000 reliability, coupled with the reduced package count possible with the TMS 1000 family provides longer life and lower costs for your products.

28 PIN PACKAGE:

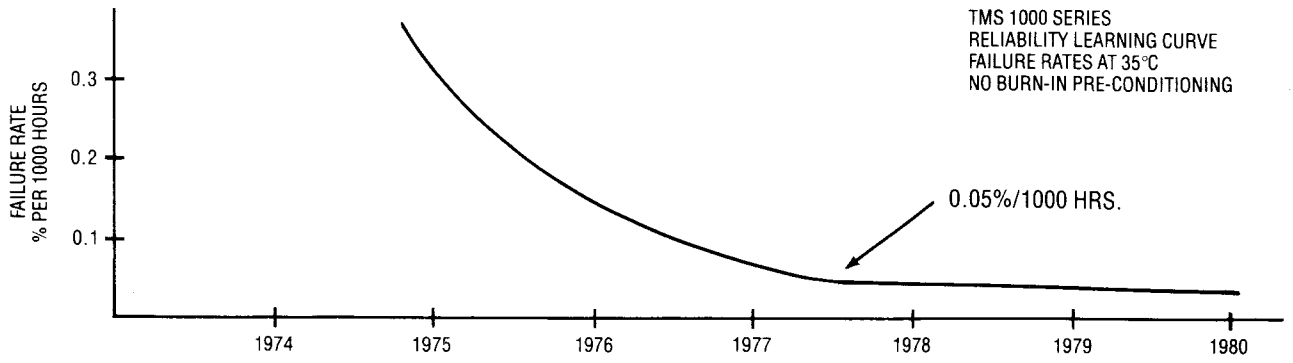


NOTES a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

40 PIN PACKAGE:



NOTES a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.



FAMILY DESCRIPTION:

The TMS 7000 family is a range of 8 bit microcomputers containing on-chip CPU, RAM, ROM and I/O. They are not restricted however to accessing internal memory only but can through expansion modes address up to 64K bytes. Each device even contains the ability to disable it's internal ROM and turn into a powerful 8 bit microprocessor!

The instruction set is also the most powerful on any 8 bit microcomputer of a similar price offering unique features and features only found on more expensive devices.

It may be that in some situations even the standard instruction set is not powerful enough and this is where the TMS 7000 family comes into it's own. The family also goes under the name of the MicroLanguage Processor (MLP), which means that the instruction set is micro-programmable and can be defined by the user to suit his own application.

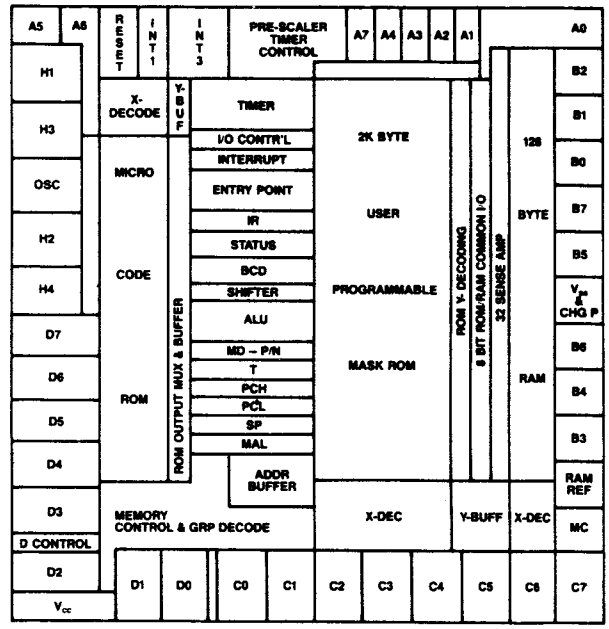
Current devices are produced in NMOS technology but as time progresses a variety of parts will become available. Plans are already being carried out to produce low power NMOS parts and CMOS too. Time will also reveal devices containing other than just the standard features available at present. Such is TI's committment to the 8 bit market.

DEVELOPMENT SUPPORT

No microcomputer is of any use if there are no development tools available to develop programs and emulate the devices. TI has developed a system called MLP Front Panel which will allow on a TI minicomputer the writing, assembling, debugging and emulating of any TMS 7000 program. This system will also allow emulation of custom micro-code.

An evaluation module is also available which allows the development of small programs and the emulation of the final program prior to mask development. Larger programs can be developed on a minicomputer using cross-support software and downloaded to the module for debugging and emulation.

TI will also undertake to write TMS 7000 programs to a customer's specification at it's plant in Bedford. Experienced engineers are available to produce a complete system design including the hardware and software.



The TMS 7020 bar layout using TI's new Strip Chip Architecture Topology (SCAT).

PRODUCTION OF DEVICES

Once a program has been finalised TI will take the source or object file of the program and use it to generate masks from which the first sample devices are produced. This process takes 16 weeks. Assuming the samples are found satisfactory then full production devices can be available 16 weeks later. TI will normally consider production on any device over 5K units in quantity.

PROGRAMMING THE TMS 7000

The TMS 7000 family has taken the advantages of memory to memory and register to register architectures and combined them to achieve a powerful combination of speed and flexibility. The programmer is not restricted to operating on data only in an accumulator nor does he have to consume valuable bytes of program specifying frequently used registers.

This has been achieved by including within the opcodes of certain instructions an implication to one of two registers out of the 128 available. This has the effect to treating them more as accumulators than registers, yet still retaining them within the memory map. It also saves one byte of code since the register is implied. These two registers are known as the A and B registers.

All of the common addressing modes encountered in memory to memory architecture have been included. These are direct, indirect, indexed, program counter relative, and immediate addressing. In addition to these are register A, register B, register file and peripheral file addressing giving a total of nine addressing modes.

Since the RAM, ROM, I/O and external addresses are all within the memory map there is no need to include special instructions to reference these areas. The extended addressing modes specify an unqualified 16 bit address and may access any area within the 64K address range.

Programming is made still easier by the inclusion of the dual operand instructions. One operand being known as the source, the other as the destination. Most microcomputers when using these common instructions (i.e. add, subtract, AND, move etc.) require at least one of the operands to be a CPU register (like A or B) but with the TMS 7000 family any RAM location can be the source and any RAM location can be the destination.

SINGLE OPERAND INSTRUCTIONS:

MNEMONIC	MEANING
CLR	Clear operand
DEC	Decrement operand
DECD	Decrement register pair
INC	Increment operand
INV	Invert operand
POP	Pop from stack
PUSH	Push on stack
RL	Rotate left one place
RLC	Rotate left through carry
RR	Rotate right one place
RRC	Rotate right through carry
XCHB	Exchange with B register

DUAL OPERAND INSTRUCTIONS:

MNEMONIC	MEANING
ADC	Add with Carry
ADD	Add bytes
AND	AND bytes
ANDP	AND Peripheral File
CMP	Compare
DAC	Decimal add with Carry
DSB	Decimal substract w/Borrow
MOV	Move
MOVD	Move register pair
MOVP	Move to/from peripheral file
MPY	Multiply
OR	OR bytes
ORP	OR with peripheral file
SBB	Subtract bytes
SUB	Subtract bytes
XOR	Exclusive OR
XORP	XOR with peripheral file

EXTENDED INSTRUCTIONS:

MNEMONIC	MEANING
BR	Branch
CMPA	Compare to A register
LDA	Load A register
STA	Store A register

THE STANDARD INSTRUCTION SET:

Turning now to look at the standard instruction set we can see from the tables that most of the common features of any microcomputer's instruction set are included. In addition however the TMS 7000 has several interesting features some of which are highlighted here.

The multiply instruction (MPY) is not found on every microcomputer nor is it executed in hardware in only 17.2 μs on many machines either. Those microcomputers of a similar price to the TMS 7000 all perform a software multiplication in 150–200 μs.

A unique feature to the TMS 7000 is the BCD addition and subtraction which perform fully corrected arithmetic on two packed BCD bytes. This makes the TMS 7000 an obvious contender for any financial and scientific application.

MOVD allows a 16 bit value in a register pair to be moved with just one instruction. DECD decrements a register pair which is useful for loop control or indirect addressing situations.

A comprehensive range of jump instructions is included which can perform many logical or boolean tests on the operand. The "bit test and jump if one" instruction for example looks for a one in any bit of the operand which has been indicated by an 8 bit mask included within the instruction. Thus individual bits or groups of bits may be tested according to the mask.

The assembler also allows all the variations of comparisons between one operand and another thus allowing the code to follow the program structure rather than having the instruction set govern the program design.

The stack allows multi-level stacking of interrupts and subroutines as well as providing a simple way of storing temporary data. Subroutines can also be invoked by using the 24 trap instructions which allow the calling of subroutines with just one byte, the subroutine address being found in vectors in the top end of the ROM.

JUMP INSTRUCTIONS:

MNEMONIC	MEANING
BTJO	Bit test and jump if one
BTJOP	Bit test and jump if one PF
BTJZ	Bit test and jump if zero
BTJZP	Bit test and jump if zero PF
DJNZ	Dec. reg. and jump if non zero
JMP	Unconditional jump
JC	Jump if Carry set
JHS	Jump if higher or same
JN	Jump if negative
JLT	Jump if less than
JNC	Jump if no Carry
JL	Jump if lower
JNZ	Jump if not zero
JNE	Jump if not equal
JP	Jump if positive
JGT	Jump if greater than
JPZ	Jump if positive or zero
JGE	Jump if greater or equal
JZ	Jump if zero
JEQ	Jump if equal to

CONTROL INSTRUCTIONS:

MNEMONIC	MEANING
CLRC	Clear Carry bit
DINT	Disable interrupts
EINT	Enable interrupts
IDLE	Idle until interrupt
LDSP	Load Stack Pointer
NOP	No operation
SETC	Set Carry bit
STSP	Store Stack Pointer
SWAP	Swap nibbles
TSTA	Test A register
TSTB	Test B register

SUBROUTINE INSTRUCTIONS:

MNEMONIC	MEANING
CALL	Call subroutine
RETI	Return from interrupt
RETS	Return from subroutine
TRAPO	Trap to subroutine
.	
.	
TRAP23	

EXPANSION MODES

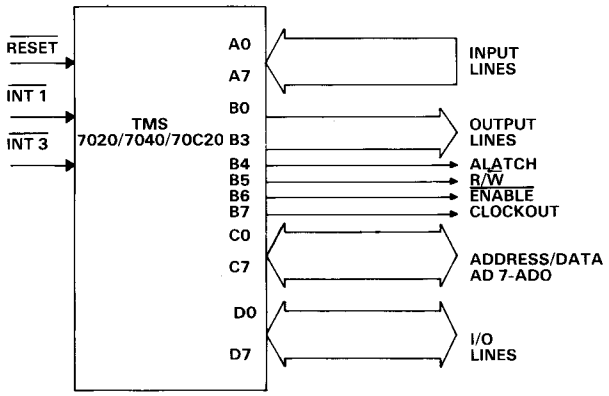
The TMS 7020, 7040 and 70C20 can be used as single-chip microcomputers utilising the A, B, C and D ports as general purpose I/O or they can also, under software control be configured into two different memory expansion modes known as peripheral and full expansion. These modes use the C or the C and D ports as multiplexed data/address buses and half the B port as timing information. This allows the microcomputer to address external memory-mapped devices or external RAM or ROM in the most efficient manner.

The expansion mode is simply selected by writing to two bits in the I/O control register. Therefore, for example a masked device could read external wire links and according to their setting could configure itself in one of the three I/O modes. This clearly gives each masked device tremendous flexibility with the ability to include several applications within the one masked program.

In addition to the three modes mentioned above the devices can also be used as 8-bit microprocessors. Wiring the Mode Control pin to Vcc will disable the on-chip ROM (but still retain the RAM) enabling the device to execute external program in RAM, ROM or EPROM.

Expansion mode	Memory Control Pin	I/O Control Reg. Bits 7 and 6	
Single-Chip	0v	0	0
Peripheral expansion	0v	0	1
Full expansion	0v	1	0
Microprocessor NMOS	Vcc	x	x
Microprocessor CMOS	Vcc	0	0

I/O FOR PERIPHERAL EXPANSION

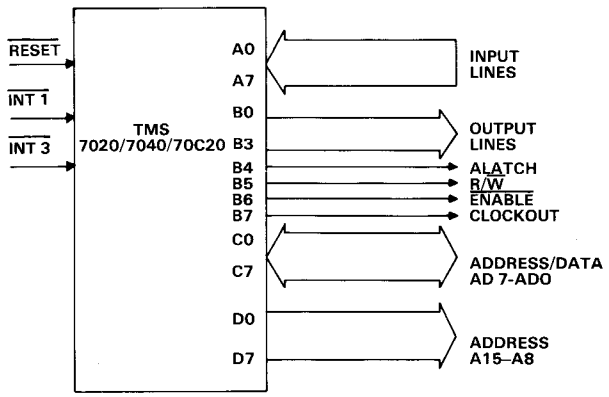


MEMORY MAP FOR PERIPHERAL EXPANSION

>0000 – >007F	REGISTER FILE
>0080 – >00FF	NOT AVAILABLE
>0100 – >0105	ON-CHIP I/O
>0106 – >0107	SEE NOTE
>0108 – >0109	MEMORY EXPANSION
>010A – >010B	ON-CHIP I/O
>010C – >01FF	MEMORY EXPANSION
>0200 – >EFFF	NOT AVAILABLE
>F000 – >F7FF	TMS 7040 ROM ONLY
>F800 – >FFFF	ON-CHIP ROM

Note: Bits 3-0 of >0106 are on-chip, Bits 7–4 of >0106 are off-chip, >0107 reserved.

I/O FOR FULL EXPANSION



MEMORY MAP FOR FULL EXPANSION

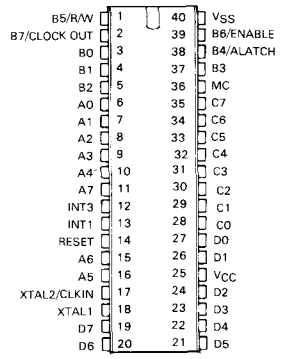
>0000 – >007F	REGISTER FILE
>0080 – >00FF	NOT AVAILABLE
>0100 – >0105	ON-CHIP I/O
>0106 – >0107	SEE NOTE
>0108 – >EFFF	MEMORY EXPANSION
>F000 – >F7FF	TMS 7040 ROM ONLY
>F800 – >FFFF	ON-CHIP ROM

Note: Bits 3–0 of >0106 are on-chip, Bits 7–4 of >0106 are off-chip, >0107 reserved.

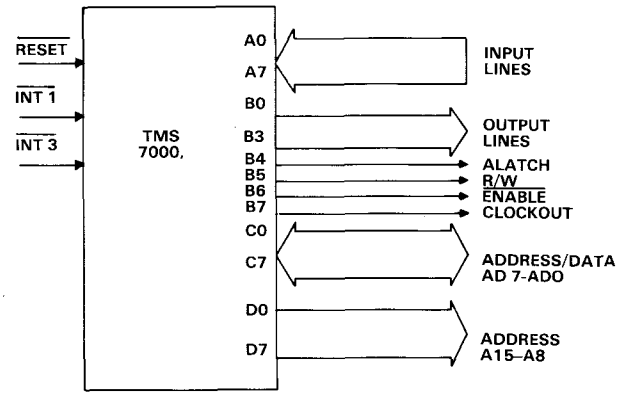
FEATURES:

- **8 bit instruction data word.**
- **65,272 bytes of external addressing.**
- **128 memory mapped registers.**
- **Full feature data/program stack.**
- **Two external maskable interrupts**
- **On-chip 13 bit timer/event counter with interrupt and capture latch.**
- **8 inputs, 4 outputs.**
- **BCD addition and subtraction.**
- **8 × 8 bit multiply in 17.2 μs.**
- **NMOS, +5V operation.**
- **TTL compatible I/O lines.**

PIN-OUT



INPUT-OUTPUT



DESCRIPTION:

The TMS 7000 is the 8 bit NMOS microprocessor of the TMS 7000 family. Compatible with the other family members it executes external program in Eprom/prom or internal RAM and can access the full 64K address range. A versatile instruction set allows anything from bit manipulation to multiplication and BCD arithmetic.

On board timer with capture latch and two external interrupts allow flexible program structure, and up to 126 bytes of stack provides multilevel subroutines and temporary data storage.

MEMORY MAP

>0000 – >007F	REGISTER FILE
>0080 – >00FF	NOT AVAILABLE
>0100 – >0105	ON-CHIP I/O
>0106 – >0107	SEE NOTE
>0108 – >FFFF	MEMORY EXPANSION

Note: Bits 3-0 of >0106 are on-chip, bits 7-4 of >0106 are off-chip, >0107 reserved.

CHARACTERISTICS

Supply voltage	5V
Supply current	80 mA
Oscillator frequency	5 MHz
Operating temperature range	0 to 70°C
40 pin, 600 mil, dil package	

Note: A lower power NMOS TMS 7000 part is in design. Details will be released when more information is available.

ORDERING INFORMATION:

TMS 7000 NL – **Plastic pack**
TMS 7000 JDL – **Ceramic pack**

TMS 7020

8 BIT NMOS MICROCOMPUTER

FEATURES:

- 8 bit instruction data word.
- 2048 bytes of on-chip ROM.
- 128 memory mapped registers.
- External expansion up to 63,220 bytes.
- Can be used in microprocessor mode as a TMS 7000.
- Full feature data/program stack.
- Two external maskable interrupts.
- On-chip 13 bit timer/event counter with interrupt and capture latch.
- 8 inputs, 8 outputs and 16 lines of I/O.
- BCD addition and subtraction.
- 8 × 8 bit multiply in 17.2μs.
- NMOS, +5V operation.
- Microprogrammable instruction set.

DESCRIPTION:

The TMS 7020 is a versatile 8 bit microcomputer containing 2K of on-chip ROM and 128 memory mapped registers. 32 bits of g.p. I/O is available which can be used in expansion modes to address nearly 62K of external addresses.

The standard instruction set allows anything from bit manipulation to multiply and BCD arithmetic, but the device is programmable with a custom instruction set should the application require one.

CHARACTERISTICS:

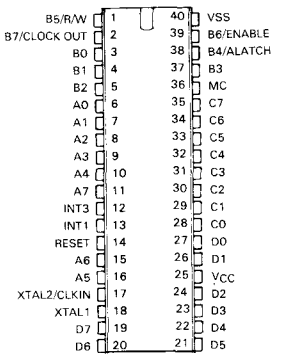
Supply voltage	5V
Supply current	80 mA
Oscillator frequency	5 MHz
Operating temperature	0–70°C
40 pin, 600 mil. dil package	

Note: A lower power NMOS TMS 7020 part is in design. Details will be released when more information is available.

ORDERING INFORMATION:

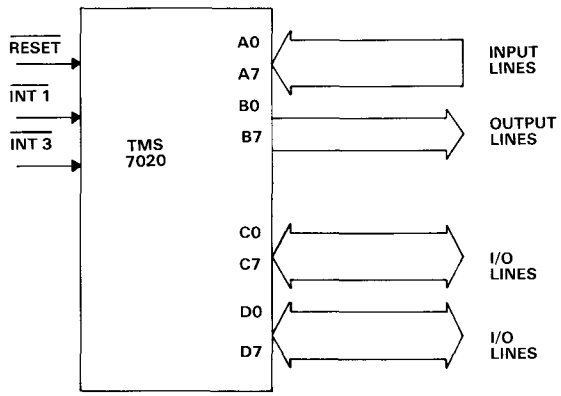
TMS 7020 NL – Plastic pack
TMS 7020 JDL – Ceramic pack

PIN-OUT



I/O – SINGLE CHIP MODE

(See page on expansion modes)



MEMORY MAP – SINGLE CHIP MODE

(See page on expansion modes)

> 0000 – > 007F	REGISTER FILE
> 0080 – > 00FF	NOT AVAILABLE
> 0100 – > 010B	ON-CHIP I/O
> 010C – > F7FF	NOT AVAILABLE
> F800 – > FFFF	ON-CHIP ROM

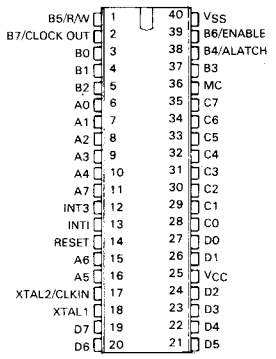
FEATURES:

- 8 bit instruction data word.
- 4096 bytes of on-chip ROM.
- 128 memory mapped registers.
- External expansion up to 61,176 bytes.
- Can be used in microprocessor mode as a TMS 7000.
- Full feature data/program stack.
- Two external maskable interrupts.
- On-chip 13 bit timer/event counter with interrupt and capture latch.
- 8 inputs, 8 outputs and 16 lines of I/O.
- BCD addition and subtraction.
- 8 × 8 bit multiply in 17.2μs.
- NMOS, +5V operation.
- Microprogrammable instruction set.

DESCRIPTION:

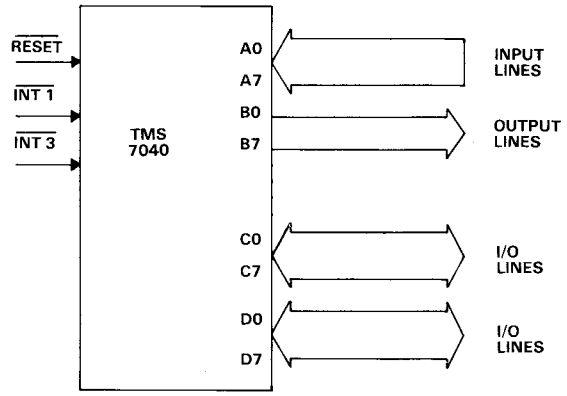
The TMS 7040 is a versatile 8 bit microcomputer containing 4K of on-chip ROM and 128 memory mapped registers. 32 bits of g.p. I/O is available which can be used in expansion modes to address nearly 60K of external addresses.
The standard instruction set allows anything from bit manipulation to multiply and BCD arithmetic, but the device is programmable with a custom instruction set should the application require one.

PIN-OUT



I/O – SINGLE CHIP MODE

(See page on expansion modes)



MEMORY MAP – SINGLE CHIP MODE

(See page on expansion modes)

> 0000 – > 007F	REGISTER FILE
> 0080 – > 00FF	NOT AVAILABLE
> 0100 – > 010B	ON-CHIP I/O
> 010C – > EFFF	NOT AVAILABLE
> F000 – > FFFF	ON-CHIP ROM

CHARACTERISTICS:

Supply voltage	5V
Supply current	80 mA
Oscillator frequency	5 MHz
Operating temperature	0–70°C
40 pin, 600 mil. dil package	

NOTE: A lower power NMOS TMS 7040 part is in design. Details will be released when more information is available.

ORDERING INFORMATION:

TMS 7040 NL – Plastic pack
TMS 7040 JDL – Ceramic pack

TMS 70C00

PRELIMINARY INFORMATION

8 BIT CMOS MICROCOMPUTER

FEATURES:

- **8 bit instruction data word.**
- **65,272 bytes of external addressing.**
- **128 memory mapped registers.**
- **Full feature data/program stack.**
- **Two external maskable interrupts.**
- **On-chip 13 bit timer/event counter with interrupt and capture latch.**
- **Two power-down modes. One with wake-up.**
- **8 inputs, 4 outputs.**
- **BCD addition and subtraction.**
- **8 × 8 bit multiply in 34.4μs.**
- **CMOS, 2.5 to 6 volt operation.**

DESCRIPTION:

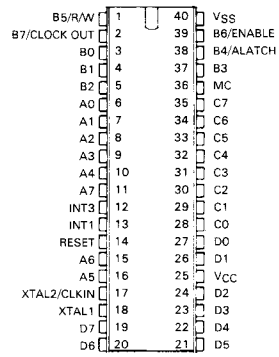
The TMS 70C00 is an 8 bit CMOS microprocessor compatible with the other TMS 7000 family of devices but with the added low power advantage of CMOS technology. In addition to the standard features of the family the TMS 70C00 has two power-down modes in which the RAM and registers are maintained but operation is halted until an interrupt occurs. One of these modes allows the timer to keep on running which can wake up the processor when it decrements past zero.

CHARACTERISTICS:

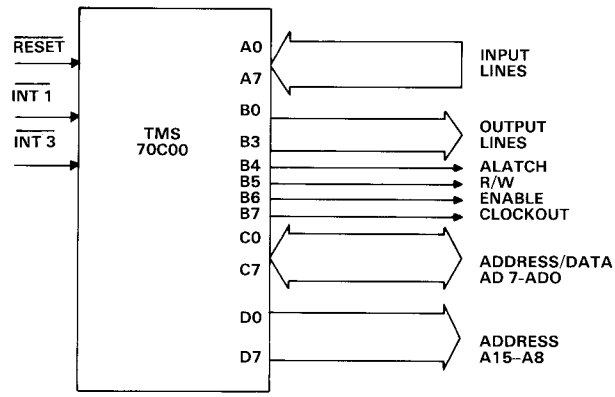
Supply voltage	2.5 to 6V
Supply current:	
Active	5 mA
Wakeup	600 μA
Halted	5 μA
Oscillator frequency @ 5.0V	2.5 MHz
@ 2.5V	0.5 MHz
Operating temp range	–40 to +85°C

Note: This is advanced information subject to change. The part will not become available until 1982.

PIN-OUT



INPUT-OUTPUT



MEMORY MAP

> 0000 – > 007F	REGISTER FILE
> 0080 – > 00FF	NOT AVAILABLE
> 0100 – > 0105	ON-CHIP I/O
> 0106 – > 0107	SEE NOTE
> 0108 – > FFFF	MEMORY EXPANSION

Note: Bits3-0 of >0106 are on-chip, bits 7-4 of >0106 are off-chip, >0107 reserved

ORDERING INFORMATION:

TMS 70C00 JDC – Ceramic 600 mil 40 pin package
TMS 70C00 NL – Plastic 600 mil 40 pin package

PRELIMINARY
INFORMATION

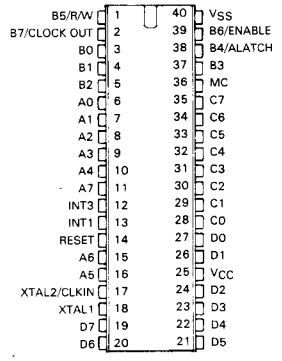
TMS 70C20

8 BIT CMOS MICROCOMPUTER

FEATURES:

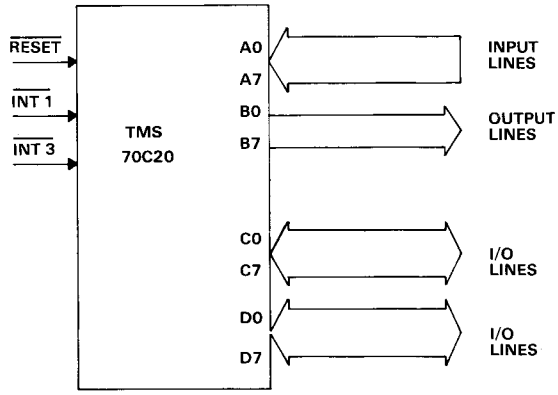
- 8 bit instruction data word.
- 2048 bytes of on-chip ROM.
- 128 memory mapped registers.
- External expansion up to 63,223 bytes.
- Can be used in microprocessor mode as a TMS 70C00.
- Full feature data/program stack.
- Two external maskable interrupts.
- On-chip 13 bit timer/event counter with interrupt and capture latch.
- Two power-down modes. One with wake-up.
- 8 inputs, 8 outputs and 16 lines of I/O.
- BCD addition and subtraction.
- 8 × 8 bit multiply in 34.4μs.
- CMOS, 2.5 to 6V operation.
- Microprogrammable instruction set.

PIN-OUT



I/O – SINGLE CHIP MODE

(See page on expansion modes)



DESCRIPTION:

The TMS 70C20 is an 8 bit CMOS microcomputer containing all the standard features of the TMS 7000 family but with the low power advantages of CMOS technology. The device has two power-down modes one of which allows the timer to wake the processor up when it decrements through zero.

MEMORY MAP – SINGLE CHIP MODE

(See page on expansion modes)

> 0000 – > 007F	REGISTER FILE
> 0080 – > 00FF	NOT AVAILABLE
> 0100 – > 010B	ON-CHIP I/O
> 010C – > F7FF	NOT AVAILABLE
> F800 – > FFFF	ON-CHIP ROM

CHARACTERISTICS:

Supply voltage	2.5 to 6V
Supply current:	
Active	5 mA
Wakeup	600 μA
Halted	5 μA
Oscillator frequency @ 5.0V	2.5 MHz
@ 2.5V	0.5 MHz
Operating temp range	−40 to +85°C

Note: This is advanced information subject to change. The part should be available 2H82.

ORDERING INFORMATION:

TMS 70C20 JDC – Ceramic 600 mil 40 pin package
TMS 70C20 NL – Plastic 600 mil 40 pin package

TMS 7000 Family

EVALUATION MODULE

MODULE FEATURES:

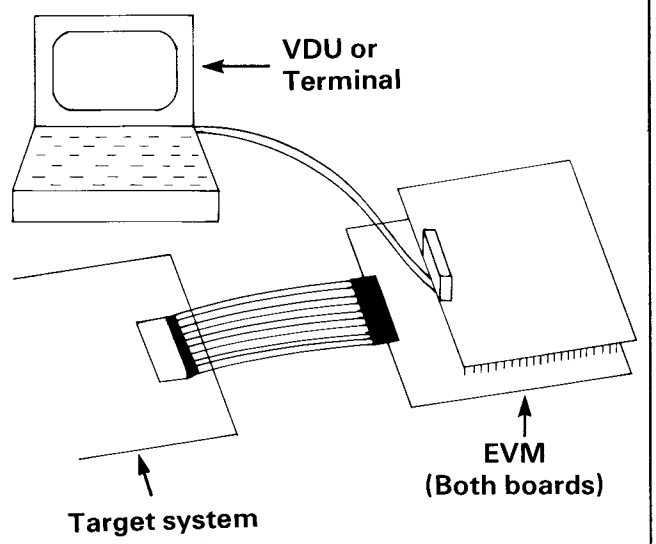
- Single-chip TMS 7020, TMS 7040 and TMS 70C20, TMS 70C40 emulation
- Monitor.
- Line-by-line assembler.
- RS 232 communication through EIA port.
- Program development and debugging capability.
- Execute program from RAM or EPROM.

MONITOR FEATURES:

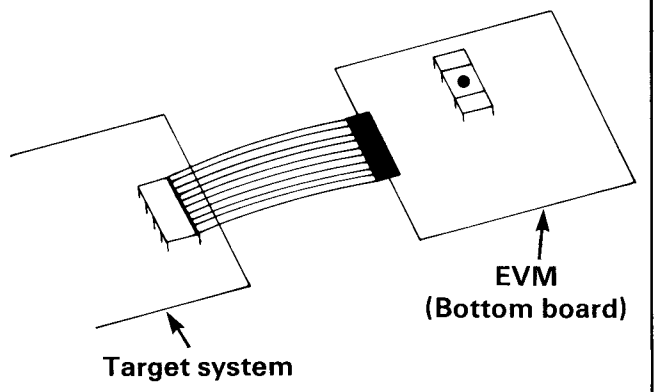
- Load memory from EIA port in MLP object, 9900 object or Tektronix object format.
- Dump memory to EIA port in MLP object or Tektronix object format.
- Initialise user program limit.
- Move memory.
- List memory.
- Display/modify A and B registers.
- Display/modify memory, register file, peripheral file, PC, ST or SP.
- Single step through program.
- Execute at full speed.
- Breakpoint at address.

SYSTEM DIAGRAMS

DEVELOPMENT STAGE



EMULATION STAGE



DESCRIPTION:

The evaluation module (EVM) is a two board system that allows emulation of the TMS 70C20 and TMS 70C40 in single chip modes. The boards plug together in a piggy-back fashion with the bottom board providing the emulation and the top board providing 4K of user RAM for program development and RS 232 communication through an EIA port.

A line-by-line assembler is provided that allows small program development and program modification. Object can be loaded or dumped for ease of larger program development.

ORDERING INFORMATION:

Part No. TMAM 6070

The TMS 9940 is a masked microcomputer intended for high volume (greater than 2000 units) applications. The software for each individual application is used to make a unique version of the device.

The TMS 9940 is in a 40 pin package which includes all of the elements of a computer, that is, memory, I/O and utilities in addition to ALU and control. Useful in a wide variety of dedicated control functions, it contains 2K × 8 ROM (TMS 9940M), or EPROM (TMS 9940E) program memory and a 128 × 8 RAM for data, a 14 bit interval timer, and a multiprocessor system interface. Although the memory organisation on chip is in 8 bit bytes, the instructions are the same instructions of the 9900 family, with four omissions and three additions.

The memory to memory architecture featuring 16 general purpose registers and concept of context switching of the 9900 family are exhibited by the TMS 9940.

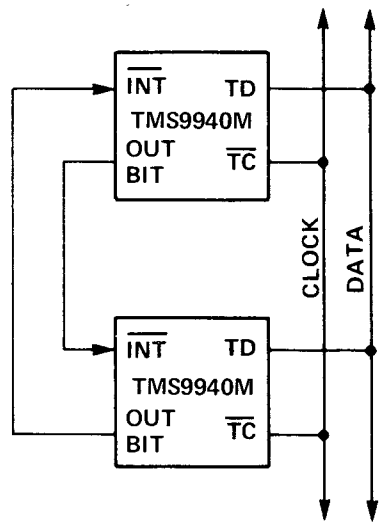
One of the most extraordinary features of the TMS 9940 is the I/O structure in which 32 pins of the 40 pin package are software assignable. That is, they do not perform single, predefined, hard-wired functions, but instead are under the control of the programmer in structuring input/output functions. This is achieved by the implementation of the Communications Register Unit (CRU) concept of the 9900 family. The major emphasis being:

32 bits of input – on chip multiplexer.
32 bits of output – on chip flip flags.
32 bit register defining signal direction (in or out) for the assignable pins.
16 bit flag register – may be written or read.
14 bit "clock" register – for loading the decrementer.
14 bit "read" register – for reading the decrementer.
16 bit shift register for receiving instructions in a multiprocessor application, or used for sending 16 bit information over the Multiprocessor System Interface to other processors.
14 bit decrementer (used as a timer or counter).
256 bit CRU expansion (input and output).

The "I/O Expansion" diagram on the summary sheet shows a system implementation of an I/O interface composing TMS 9901 programmable systems interface, TMS 9902 asynchronous communications controller and a TMS 9903 synchronous communications controller.

The TMS 9940 features a Multiprocessor System Interface (MPSI). The MPSI is a two-wire interface for transferring data in a multiprocessor system.

Since the TMS 9940 can execute instructions out of its RAM, the MPSI allows the capability of efficiently down loading instruction sequences which can then be executed. Thus, multiple processor systems can reconfigure themselves in system applications. The MPSI can also be used to transfer data to be operated on, such as in a master-slave situation with the master distributing tasks to slaves.



Multiple System Interface (MPSI)

The TMS 9940 implements four hardware interrupt levels. The highest priority interrupt level (level 0) is reserved for the RESET function followed by a user defined external interrupt INT1 (level 1), the decrementer (level 2), and the second user defined external interrupt INT2 (level 3). The TMS 9940 external interrupt interface lines signals require no external synchronisation and are TTL level compatible.

The TMS 9940 incorporates a 16-bit flag register internally. Each of the bits is under program control and can be SET, RESET and TESTED. The bits are accessed through dedicated CRU bit addresses.

The design cycle will require prototyping using the EPROM version of the part TMS 9940E. A programming module is available for the FS990 minicomputers. The program, verify and download functions work together with the sophisticated AMPL systems. Program development support is available on these machines (editor, linker, assembler etc). The acceptable vehicles for transmission of object to TI for factory programming of the TMS 9940MCR (ROM part) are: Digital cassette, floppy disc or via time share network (GE, NCSS, Tymeshare).

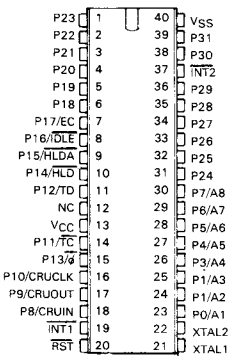
TMS 9940 MCR

16-bit NMOS MICROCOMPUTER

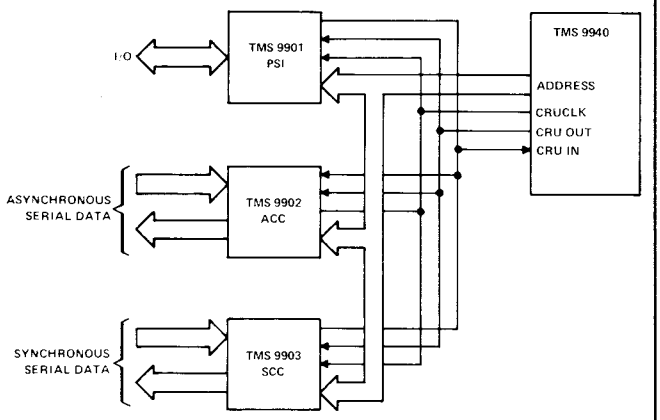
FEATURES:

- 16-bit instruction word.
- Minicomputer instruction set including multiply and divide.
- 2048 bytes of ROM on-chip.
- 128 bytes of RAM on chip.
- 16 general purpose registers.
- 4 prioritized interrupts.
- On-chip timer/event counter.
- 32 bits general purpose I/O Ports.
- 256 bits I/O expansion.
- Multiprocessor system interface.
- 4 MHz oscillator frequency.
- N-channel silicon gate MOS, 5 volt power supply.

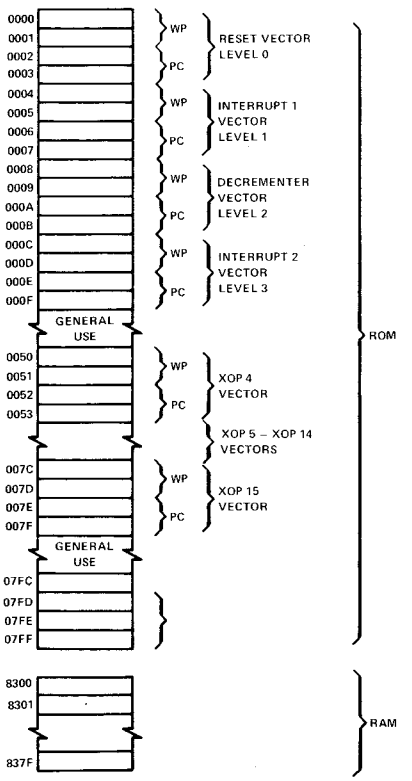
PIN-OUT:



I/O EXPANSION:



MEMORY MAP:



DESCRIPTION:

The TMS 9940 is a single-chip, 16-bit microcomputer containing a CPU, memory (RAM and ROM, and extensive I/O. Except for four instructions that do not apply to the TMS 9940 microcomputer configuration, the TMS 9940 instruction set matches that of the TMS 9900 and includes capabilities offered in **minicomputers**. In addition, the TMS 9940 instruction set includes two instructions that facilitate manipulation of binary coded decimal (BCD) data, and a single-word load-interrupt-mask (LIM) instruction. All members of the TMS 9900 family of peripheral circuits are compatible with the TMS 9940 MCR.

For Prototype Development use the TMS 9940E.

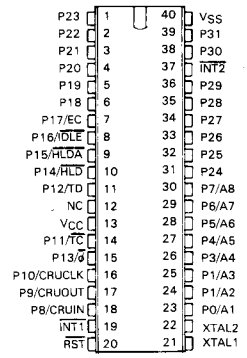
CHARACTERISTICS:

Supply voltage, V_{CC}	−0.3 to 10V
All input voltages	−0.3 to 10V
Output voltage	−2 to 7V
Continuous power dissipation	1.5 W
Operating free-air temp range	0°C to 70°C
Storage temperature range	−55°C to 150°C

FEATURES:

- **16-bit instruction word.**
- **Minicomputer instruction set including multiply and divide.**
- **2048 bytes of EPROM on chip.**
- **128 bytes of RAM on chip.**
- **16 general purpose registers.**
- **4 prioritized interrupts.**
- **On-chip timer/event counter.**
- **32 bits general purpose I/O Ports.**
- **256 bits I/O expansion.**
- **Multiprocessor system interface.**
- **4 MHz oscillator frequency.**
- **N-channel silicon gate MOS, 5 volt power supply.**

PIN-OUT:



DESCRIPTION:

The TMS 9940E is an EPROM memory version of the TMS 9940 MCR specifically designed for prototype development of TMS 9940 MCR based systems. It may be programmed using the AMPL development system in the same way as a normal EPROM and then erased to allow the software to be upgraded.

The TMS 9940E is a single-chip, 16-bit microcomputer containing a CPU, memory (RAM and EPROM), and extensive I/O. With the exception of the multiprocessor system interface (MPSI) and the Branch and Load Workspace Pointer (BLWP) instruction, the TMX 9940E is functionally identical to the TMS 9940MCR mask ROM device. Featuring 2048 bytes of eraseable programmable read-only memory (EPROM) the TMX 9940E supports program code prototyping of the TMS 9940MCR mask ROM device. Programming of the TMX 9940E is accomplished via the 40EP programmer (TI P/N TMAM6057). An AMPL or the user's host system EIA serial communications port is used to download bytes to be programmed to the 40EP system.

CHARACTERISTICS:

Supply voltage, V_{CC}	−0.3 to 10V
All input voltages	−0.3 to 10V
Output voltage	−2 to 7V
Continuous power dissipation	1.5 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

ORDERING INFORMATION:

Order code: TMS 9940E

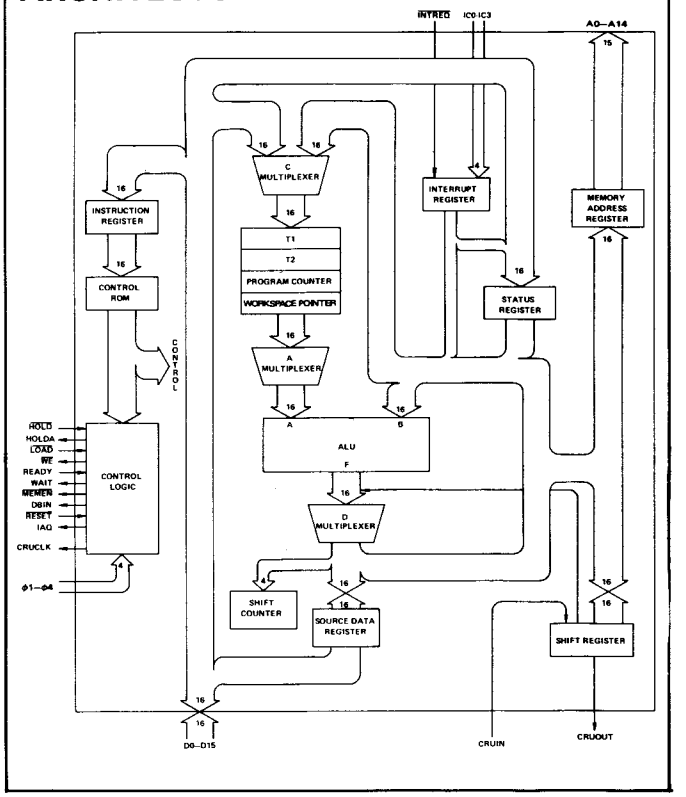
Note: These parts are specifically intended to aid developments of masked programmed TMS 9940 MCR mass production and have only limited availability.

Section 3 Microprocessors

FEATURES:

- 16 Bit Instruction Word.
- Full Minicomputer Instruction Set including Multiply and Divide.
- Up to 65,536 Bytes of Memory.
- Advanced Memory to Memory Architecture.
- Separate Memory, I/O, and Interrupt Bus Structures.
- 16 General Registers.
- 16 Prioritized Interrupts.
- Programmed and DMA I/O Capability.

ARCHITECTURE:



DESCRIPTION:

Operations are carried out with a set of dedicated registers, an ALU, and instruction handling circuits. As clock signals are applied, the Processor will fetch an instruction word from Memory, execute it, fetch another, execute etc. The instruction is saved in the instruction register (IR) on chip. Decode circuitry sets up appropriate control depending upon the IR contents. A memory address register (MAR) holds address information. The ALU and other registers perform their required function during the execute phase of the instruction cycle. There are 3 key registers on chip these are the Workspace Pointer (WP), Program Counter (PC) and Status Register (ST). The WP register holds the address of the first word in the workspace, which is 16 contiguous words of memory treated as general purpose registers for the user. Thereby changing the WP register allows a fast 'context' switch to be made. The PC register holds the address of the next instruction to be executed. The ST register is a set of flags which are set by certain operations, these flags are used as the basis of decision making in the program.

The 9900 supports 3 modes of I/O, DMA which is used for high speed block data transfer when CPU interaction is not desirable or required. Memory Mapped I/O, permits I/O data to be addressed as memory with parallel data transfer through the system data bus. CRU I/O which uses a dedicated serial interface, to transfer between 1 & 16 bits without affecting the memory system.

The TMS 9900 provides 15 maskable interrupt levels as well as Reset and Load (can be used as bootstrap loader) functions. The CPU has a priority ranking system to resolve conflicts between simultaneous interrupts and a level mask to disable lower priority interrupts.

MEMORY-TO-MEMORY

MEMORY-TO-MEMORY ARCHITECTURE

FEATURES:

- **Single Instruction can fetch one or two operands from memory perform an arithmetic or logical operation, and store the result in memory.**
- **Saves on programme code to perform particular operations, no explicit idling of the accumulator.**
- **16 general purpose registers form workspace in memory pointed to by the on chip workspace pointer.**
- **Change of 1 on chip register (WP) allows complete 'environment' switch to new 16 general purpose registers, without needing to store data values.**
- **Rapid 'Context Switch' particularly useful in Subroutine and Interrupt Processing in real time applications.**

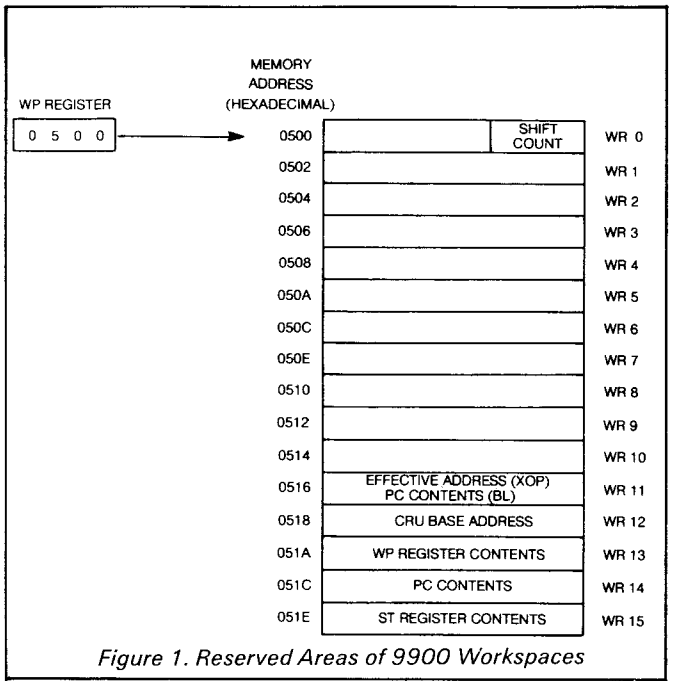


Figure 1. Reserved Areas of 9900 Workspaces

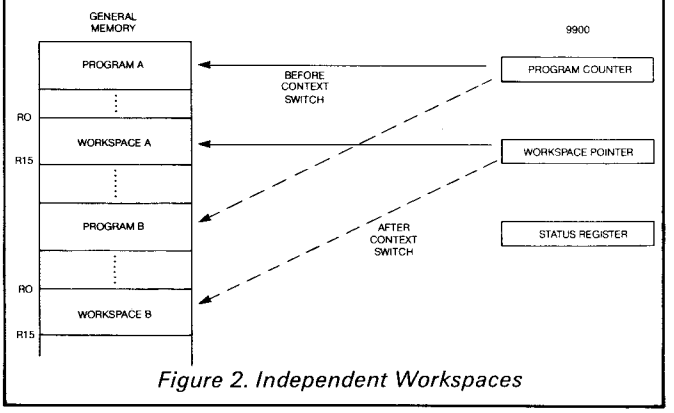


Figure 2. Independent Workspaces

DESCRIPTION:

The 9900 family of processors employ memory to memory architecture in the execution of instructions. Memory to memory architecture is that computer organisation and instruction set which enables direct modification of memory data via a single instruction.

16 general purpose registers used by instructions occupy 16 contiguous words of memory, the first word of which is pointed to by the on chip workspace pointer register. These registers are general purpose registers but perform certain functions in particular circumstances.

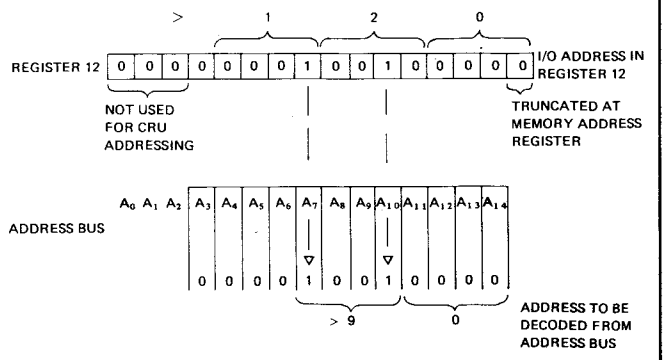
R0 can be an optional shift counter, R1 . . R15 have indexing capability, R11 can hold the return address from a BL instruction, R12 can hold the CRU base address, and R13 . . R15 the WP, PC, and ST register values after a BLWP instruction, XOP or Interrupt context switch.

The contents of the 3 on chip processor registers (PC, WP and ST) completely define the status of the programme at any given time. The contents of the processor and workspace registers define the current 'context' of the system. A change in the registers will lead to a new PC and new WP and hence the system will be switched into a new 'context' i.e. a context switch has taken place. Restoring the original values will restore the original context. This mechanism can be used effectively in Subroutine calls and interrupt servicing. Where the old context registers are stored in R13 . . R15 of the new workspace.

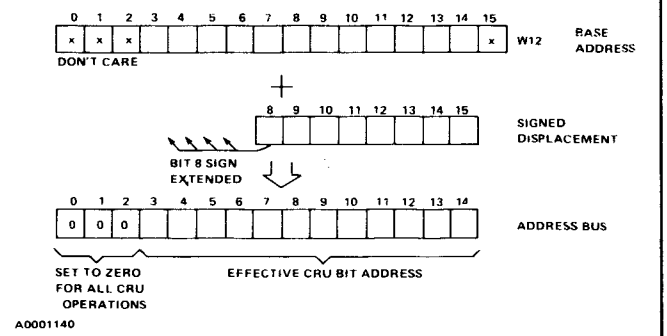
FEATURES:

- **Dedicated I/O bus utilising serial data transfer.**
- **Provides a maximum of 4096 bits read and 4096 bits write space.**
- **Possible to test, set or reset a single bit in the 4096 bit address range using a single instruction, or read and write to any number from 1 to 16 bits.**
- **Provides greater integrity because no cross talk as in parallel data transfer, can be effectively screened at low cost.**
- **'Bit picking' I/O, particularly useful for control applications where I/O typically single bit (sensors, switches, warning lights, relays valves etc. either on or off).**
- **Eliminates masking instructions required to isolate bit in memory map I/O.**
- **Allows use of I/O fields not identical to memory word size, permitting optimal use of I/O interface. Therefore minimizing size and complexity of I/O programs while increasing throughput.**
- **Does not utilise data bus but dedicated 3 wire lines (CRUIN, CRUOUT, CRUCLK). This reduces complexity of PCB layouts for most systems. Standard 16-pin CRU I/O devices less expensive and easier to insert than larger specially designed memory map I/O devices.**
- **Smaller I/O devices possible as result of CRU bus which eliminates need for several pins dedicated to parallel data bus with multiple control lines. System costs are lower because of simplified circuit layouts increased density and lower component costs.**

SOFTWARE AND HARDWARE BASE:



SINGLE BIT DISPLACEMENT:



DESCRIPTION:

5 CRU instructions operate from a base address, which must be stored in workspace register 12 (R12) for the current workspace. The contents of this register is known as the 'Software Base Address'. Infact bits 3 to 14 of this register are used to generate the address and the other bits are ignored. This is the address which appears on the hardware address bus and therefore is known as the 'Hardware Address'. It can be seen therefore that Software Base address = 2 × Hardware Base address.

The 3 single bit CRU instructions use a signed displacement, from the Hardware Base address to reference a particular bit (line). This allows access within a range of −128 to +127 bits from this base address. The 3 instructions are: SBO <displacement> = set bit to one. TB <displacement> = test bit (reads digital input and sets equal status flag, bit 2 in status register to the value of the bit, for further processing). SBZ <displacement> = set bit to zero.

There are 2 multiple bit CRU instructions which use 2 operands, a general 'memory' address (where inputs/outputs to be stored or taken from) and a count (0 to 15) of bits to be transferred. These instructions transfer 1 to 16 bits, count 0 refers to 16 bits, 1 is 1 bit etc. Data is transferred to/from the first bit pointed to by the present base address.

LDCR <mem address, count>, Load Communications Register, transfers the number of bits from memory to the CRU output.

STCR <mem address, count>, Store Communications Register, stores the number of bits from CRU into memory location.

Note:

For transfers concerning 8 bits or less data is stored or taken from the MS Byte of the memory word the LS Bit first. If greater than 8 bits it starts from the LS Byte the LS Bit. This can be overidden by the use of indirect addressing.

Unused bits of the byte/word are set to zero during a STCR instruction. For transfers of 8 bits or less the unused byte is not modified.

TMS 9900/SPEED

9900 INSTRUCTION TIMES (MICRO SECONDS)

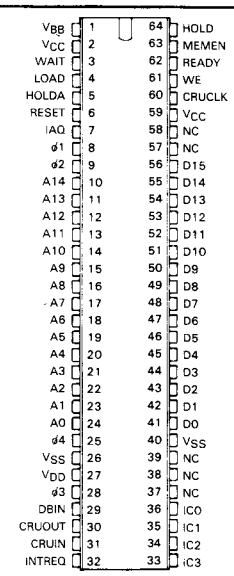
(MNEMONIC) INSTRUCTION	MEANING	9900 (3.3MHz)	9900 (4MHz)	9980 (10MHz)	9995 (12MHz)
A	Add Words	4.2	3.5	8.8	1.3
AB	Add Bytes	4.2	3.5	8.8	1.3
ABS	Absolute Value	3.6	3.0	6.4	1.0
AI	Add Immediate	4.2	3.5	8.8	1.3
ANDI	And Immediate	4.2	3.5	8.8	1.3
B	Branch	2.4	2.0	4.8	1.0
BL	Branch and Link	3.6	3.0	7.2	1.7
BLWP	Branch & Load Workspace Pointer	7.8	6.4	15.2	3.6
C	Compare Words	4.2	3.5	8.0	1.3
CB	Compare Bytes	4.2	3.5	8.0	1.3
CI	Compare Immediate	4.2	3.5	8.0	1.3
CKOF	Clock Off	3.6	3.0	5.6	2.3
CKON	Clock On	3.6	3.0	5.6	2.3
CLR	Clear	3.0	2.5	6.4	1.0
COC	Compare Ones Corresponding	4.2	3.5	8.0	1.3
CZC	Compare Zeroes Corresponding	4.2	3.5	8.0	1.3
DEC	Decrement	3.0	2.5	6.4	1.0
DECT	Decrement by Two	3.0	2.5	6.4	1.0
DIV (ST4 SET)	Divide	4.8	4.0	8.8	3.3
DIV (ST4 RSET)		27.6	22.8	41.6	9.2
DIVS (ST4 SET)	Signed Divide	—	—	—	3.3
DIVS (ST4 RSET)		—	—	—	10.9
IDLE	Idle	3.6	3.0	5.6	2.3
INC	Increment	3.0	2.5	6.4	1.0
INV	Invert	3.0	2.5	6.4	1.0
JMP (PC CHANG)	Unconditional Jump	3.0	2.5	4.8	1.0
JMP (PC NOCHG)		2.4	2.0	4.0	1.0
LDCR	Load Communications Register	6.6	5.5	11.2	3.6
LI	Load Immediate	3.6	3.0	7.2	1.0
LIMI	Load Interrupt Mask Immediate	4.8	4.0	8.8	1.6
LREX	Restart	3.6	3.0	5.6	2.3
LWPI	Load Workspace Pointer Immediate	3.0	2.5	5.6	1.0
MOV	Move Word	4.2	3.5	8.8	1.0
MOVB	Move Byte	4.2	3.5	8.8	1.0
MPY	Multiply	15.6	12.9	24.8	7.6
MPYS	Signed Multiply	—	—	—	8.3
NEG	Negate	3.6	3.0	7.2	1.0
ORI	Or Immediate	4.2	3.5	8.8	1.3
RSET	Reset	3.6	3.0	5.6	2.3
RTWP	Return with Workspace Pointer	4.2	3.5	8.8	2.0
S	Subtract Words	4.2	3.5	8.8	1.3
SB	Subtract Bytes	4.2	3.5	8.8	1.3
SBO	Set Bit to Logic One	3.6	3.0	6.4	2.6
SBZ	Set Bit to Logic Zero	3.6	3.0	6.4	2.6
SETO	Set to One	3.0	2.5	6.4	1.0
SHIFT	Shift Instructions	4.2	3.5	8.0	2.0
SOC	Set One's Corresponding	4.2	3.5	8.8	1.3
SOCB	Set One's Corresponding Byte	4.2	3.5	8.8	1.3
STCR	Store CRU	12.6	10.4	20.0	6.6
STST	Store Status	2.4	2.0	4.8	1.0
STWP	Store Workspace Pointer	2.4	2.0	4.8	1.0
SWPB	Swap Bytes	3.0	2.5	6.4	4.3
SZC	Set to Zeroes Corresponding	4.2	3.5	8.8	1.3
SZCB	Set to Zeroes Corresponding Bytes	4.2	3.5	8.8	1.3
TB	Test Bit	3.6	3.0	6.4	2.6
X	Execute	2.4	2.0	4.8	0.7
XOP	Extended Operation	10.8	8.9	20.8	5.0
XOR	Exclusive OR	4.2	3.5	17.6	1.3

Note: These are the absolute minimum execution times it asumes no wait states, single bit transfer etc.
For more detailed timings for particular situations see:
Further Information.
9900 Family Systems Design and Data Book
TMS 9995 Microprocessor Specification

FEATURES:

- **16-Bit Instruction Word.**
- **Full Minicomputer Instruction Set Capability including Multiply and Divide.**
- **Up to 65,536 Bytes of Memory.**
- **3 MHz Speed (4 MHz option).**
- **Advanced Memory-to-Memory Architecture.**
- **Separate Memory, I/O, and Interrupt-Bus Structures.**
- **16 General Registers.**
- **16 Prioritized Interrupts.**
- **Programmed and DMA I/O Capability.**
- **N-Channel Silicon-Gate Technology.**

TMS 9900 PIN ASSIGNMENTS



900 mil
64 PIN

DESCRIPTION:

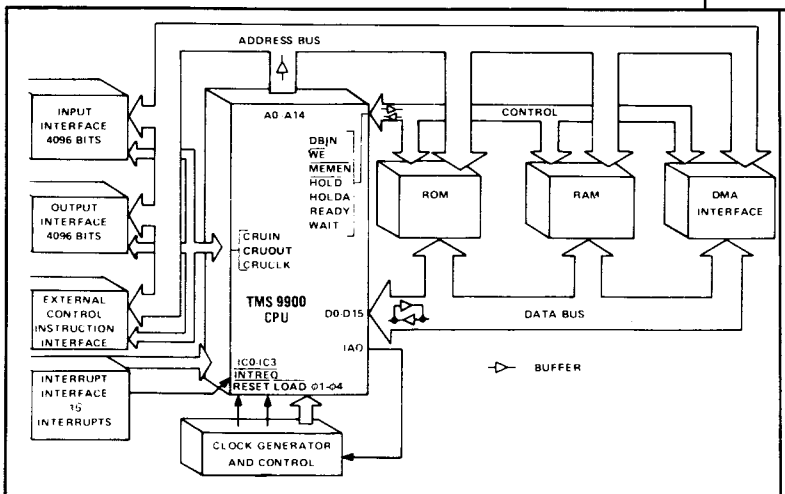
The TMS 9900 microprocessor is a single-chip 16-bit central processing unit (CPU) produced using N-channel silicon-gate MOS technology. The instruction set of the TMS 9900 includes the capabilities offered by full minicomputers. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort. Texas Instruments provides a compatible set of MOS and TTL memory and logic function circuits to be used with a TMS 9900 system. The system is fully supported by software and a complete series of development systems.

The memory word of the TMS 9900 is 16 bits long. Each word is also defined as 2 bytes of 8 bits. The instruction set of the TMS 9900 allows both word and byte operands. Thus, all memory locations are on even address boundaries and byte instructions can address either the even or odd byte The memory space is 65,536 bytes or 32,768 words.

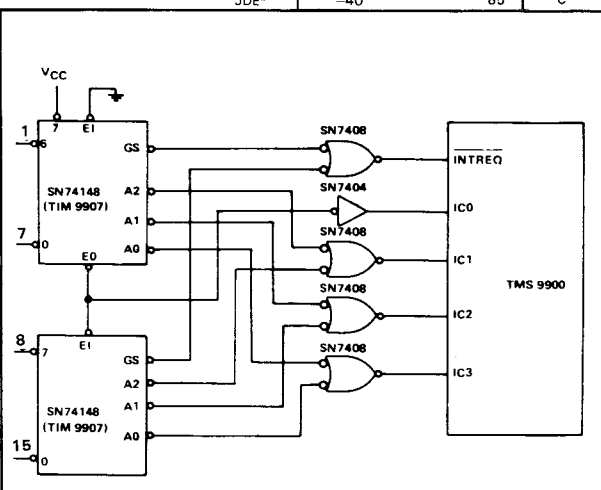
The TMS 9900 utilizes a versatile direct command-driven I/O interface designated at the communications-register unit (CRU). The CRU provides up to 4096 directly addressable input bits and 4096 directly addressable output bits. Both input and output bits can be addressed individually or in fields from 1 to 16 bits. The TMS 9900 employs three dedicated I/O pins (CRUIN, CRUOUT, and CRUCLK) and 12 bits (A3 through A14) of the address bus to interface with the CRU system. The processor instructions that drive the CRU interface can set, reset, or test any bit in the CRU array or move between memory and CRU data fields.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}		−5.25	−5	−4.75	V
Supply voltage, V_{CC}		4.75	5	5.25	V
Supply voltage, V_{DD}		11.4	12	12.6	V
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH} (all inputs except clocks)		2.2	2.4	V_{CC} +1	V
High-level clock input voltage, $V_{IH(\phi)}$		V_{DD}−2		V_{DD}	V
Low-level input voltage, V_{IL} (all inputs except clocks)		−1	0.4	0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$		−0.3	0.3	0.6	V
Operating free-air temperature, T_A	NL/JDL	0		70	°C
	JDE*	−40		85	°C



MAXIMUM TMS 9900 SYSTEM



TMS 9900 INTERRUPT INTERFACE

ORDERING INFORMATION:

TMS 9900 NL – 64-PIN PLASTIC DIL (3 MHz) (0/70°C)
TMS 9900 JDL – 64-PIN CERAMIC DIL (3 MHz) (0/70°C)
TMS 9900 JDE – 64 PIN, −40/+85°C
TMS 9900-40 NL – 64-PIN PLASTIC DIL (4 MHz) (0/70°C)
TMS 9900-40 JDL – 64-PIN CERAMIC DIL (4 MHz) (0/70°C)

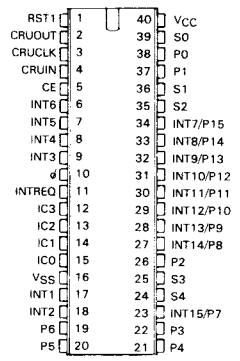
TMS 9901

PROGRAMMABLE SYSTEMS INTERFACE

FEATURES:

- **Lost Cost.**
- **9900-Family Peripheral.**
- **Perfoms Interrupts and I/O Interface functions:**
  - **Six Dedicated Interrupt Lines.**
  - **Seven Dedicated I/O Lines.**
  - **Nine Programmable Lines as I/O or Interrupt.**
  - **Up to 15 Interrupt Lines.**
  - **Up to 22 Input Lines.**
  - **Up to 16 Output Lines.**
- **Easily Cascaded for Expansion.**
- **Interval or Event Timer.**
- **Single 5V Power Supply.**
- **All Inputs and Outputs TTL-Compatible.**
- **Standard 40-Pin Plastic or Ceramic Package.**
- **N-Channel Silicon-Gate MOS Technology.**

PIN ASSIGNMENTS:



600 mil
40 PIN

DESCRIPTION:

The TMS 9901 Programmable Systems Interface (PSI) is a multifunctional component designed to provide low cost interrupt and I/O ports and an interval timer for TMS 9900-family microprocessor systems. The TMS 9901 is fabricated using N-channel silicon-gate MOS technology. The TMS 9901 is TTL-compatible on all inputs and outputs, including the power supply (+5V) and single-phase clock.

The architecture of the TMS 9901 Programmable Systems Interface (PSI) is designed to provide the user maximum flexibility when designating system I/O ports and interrupts. The TMS 9901 can be divided into four subsystems: CRU interface, interrupt interface, input/output interface, and interval timer.

The TMS 9901 PSI Interfaces to the CPU through the Communications Register Unit (CRU) and the interrupt control lines. The TMS 9901 occupies 32 bits of CRU input and output space. The five least significant bits of address bus are connected to the S lines of the PSI to address one of the 32 CRU bits of the TMS 9901. The most significant bits of the address bus are decoded on CRU cycles to select the PSI by taking its chip enable (CE) line active (LOW).

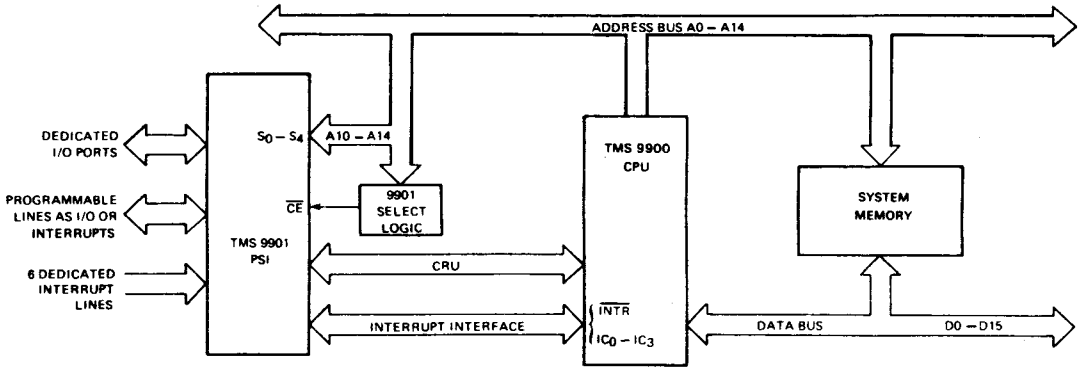
Interrupt inputs to the TMS 9901 PSI are synchronized with ϕ, inverted, and then ANDed with the appropriate mask bit. Once every ϕ clock time, the prioritizer looks at the 15 interrupt input AND gates and generates the interrupt control code. The interrupt control code and the interrupt request line constitute the interrupt interface to the CPU.

The interval timer on the TMS 9901 is accessed by writing a ONE to select bit zero, (control bit) which puts the PSI CRU interface in the clock mode. Once in the clock mode the 14-bit clock contents can be read or written. Writing to the clock register will reinitialize the clock and cause it to start decrementing. When the clock counts to zero, it will cause an interrupt and reload to its initial value.

CHARACTERISTICS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5.0	5.25	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2.0		V_{CC}	V
Low-level input voltage,	V_{SS}–.3		0.8	V
Operating free-air temperature, T_A	0		70	°C

TYPICAL APPLICATION:



TYPICAL TMS 9901 PROGRAMMABLE SYSTEM INTERFACE (PSI) APPLICATION

ORDERING INFORMATION:

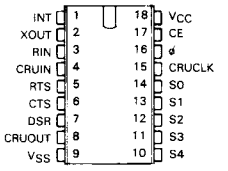
TMS 9901 NL – 40-PIN PLASTIC DIL (3 MHz)
TMS 9901 JDL – 40-PIN CERAMIC DIL (3 MHz)
TMS 9901 JDE – 40-PIN CERAMIC DIL –40/+85°C
TMS 9901-40 NL – 40-PIN PLASTIC DIL (4 MHz)
TMS 9901-40JDL – 40-PIN CERAMIC DIL (4 MHz)

FEATURES:

- **Low Cost, Serial, Asynchronous Interface (for modem or terminal).**
- **Programmable, Five- to Eight-Bit, I/O Character Length.**
- **Programmable 1, 1½, and 2 Stop Bits.**
- **Even, Odd, or No Parity.**
- **Fully Programmable, Data Rate Generation (up to 250K bits per second).**
- **Interval Timer with Resolution from 64 to 16,320 Microseconds.**
- **TTL-Compatibility, Including Power Supply (5V).**
- **Standard 18-Pin Plastic or Ceramic Package.**
- **N-Channel, Silicon-Gate Technology.**
- **Socket compatible with TMS 9903.**
- **CRU peripheral for 9900 family CPU's.**

PIN ASSIGNMENTS:

TMS 9902
18-PIN PACKAGE



300 mil
18 PIN

DESCRIPTION:

The TMS 9902 Asynchronous Communications Controller (ACC) is a peripheral device designed for use with the Texas Instruments 9900 family of microprocessors. The TMS 9902 is fabricated using N-channel, silicon gate, MOS technology. The TMS 9902 is TTL-compatible on all inputs and outputs, including the power supply (+5V) and single-phase clock. The TMS 9902 ACC provides an interface between a microprocessor and a serial, asynchronous, communications channel. The ACC performs the timing and data serialization and deserialization functions, facilitating microprocessor control of the asynchronous channel. The TMS 9902 ACC accepts *EIA Standard RS-232-C* protocol.

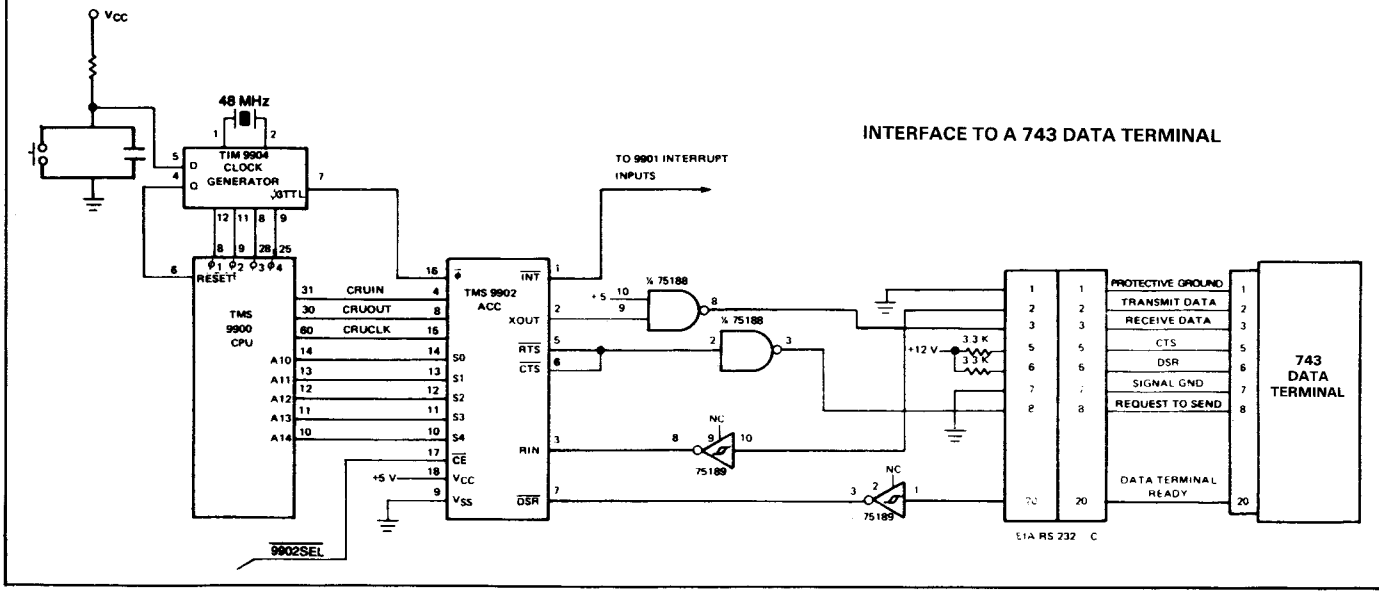
The TMS 9902 interfaces with the CPU through the *communications register unit* (CRU). The CRU interface consists of five address select lines (S0-S4), chip enable (CE), and three CRU lines (CRUIN, CRUOUT, CRUCLK). An additional input to the CPU is the ACC interrupt line (INT). The TMS 9902 occupies 32 bits of CRU space; each of the 32 bits are selected individually by processor address lines A10-A14 which are connected to the ACC select lines S0-S4, respectively. Chip enable (CE) is generated by decoding address lines A0-A9 for CRU cycles. Under certain conditions the TMS 9902 causes interrupts.

The ACC interfaces to the asynchronous communications channel on five lines: request to send (RTS), data set ready (DSR), clear to send (CTS), serial transmit data (XOUT), and serial receive data (RIN). The request to send (RTS) goes active (LOW) whenever the transmitter is activated. However, before data transmission begins, the clear to send (CTS) input must be active. The data set ready (DSR) input does not affect the receiver or transmitter. When DSR or CTS changes level, an interrupt may be generated.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5.0	5.25	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2.0		V_{CC}	V
Low-level input voltage, V_{IL}	V_{SS}–.3		0.8	V
Operating free-air temperature, T_A	0		70	°C

APPLICATION:



ORDERING INFORMATION:

TMS 9902 NL – 18-PIN PLASTIC DIL (3 MHz, 0/70°C)
TMS 9902 JDL – 18-PIN CERAMIC DIL (3 MHz, 0/70°C)
TMS 9902 JDE – 18-PIN CERAMIC DIL (3 MHz, –40/85°C)
TMS 9902-40 JDL – 18-PIN CERAMIC DIL (4 MHz, 0/70°C)
TMS 9902-40 NL – 18-PIN PLASTIC DIL (4 MHz, 0/70°C)

TMS 9903

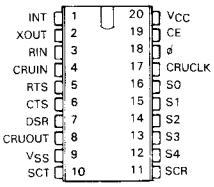
SYNCHRONOUS COMMUNICATIONS CONTROLLER

FEATURES:

- Versatile CRU interface to synchronous and asynchronous serial devices for the TMS 99XX series of microprocessors.
- DC to 250 KBPS data rate, half- or full-duplex.
- Dynamic character length selection.
- Line protocols include BI-SYNC, SDLC, HDLC, and many others.
- Programmable-polynominal CRC generation and detection.
- Interface to unclocked or NRZI data with 32x clocks.
- Two programmable sync registers.
- On-chip interval timer (64 μs to 16.32 ms).
- Automatic zero insert and delete for SDLC and HDLC.
- Single +5V supply, 20-pin DIL, all inputs and outputs TTL compatible.
- N-channel Silicon-Gate technology.
- Replaces 100 SSI and MSI devices.
- Socket compatible with TMS 9902.

PIN ASSIGNMENTS:

TMS 9903 PIN ASSIGNMENTS
20 PIN DUAL-IN-LINE PACKAGE
(TOP VIEW)



300 mil
20 PIN

DESCRIPTION:

The TMS 9903 is a versatile device which provides the system designer with a wide range of capabilities in synchronous and asynchronous communications control. The TMS 9903 operates in a multi-code configuration that allows a broad range in the degree of active participation required in the control of high-speed serial communications. Most synchronous data-link control protocols can be supported through software control of sync and fill characters, timing, CRC generation and detection, etc. Established protocols such as BI-SYNC, SDLC and HDLC are implemented directly in hardware, with others implemented through various combinations of hardware and software.

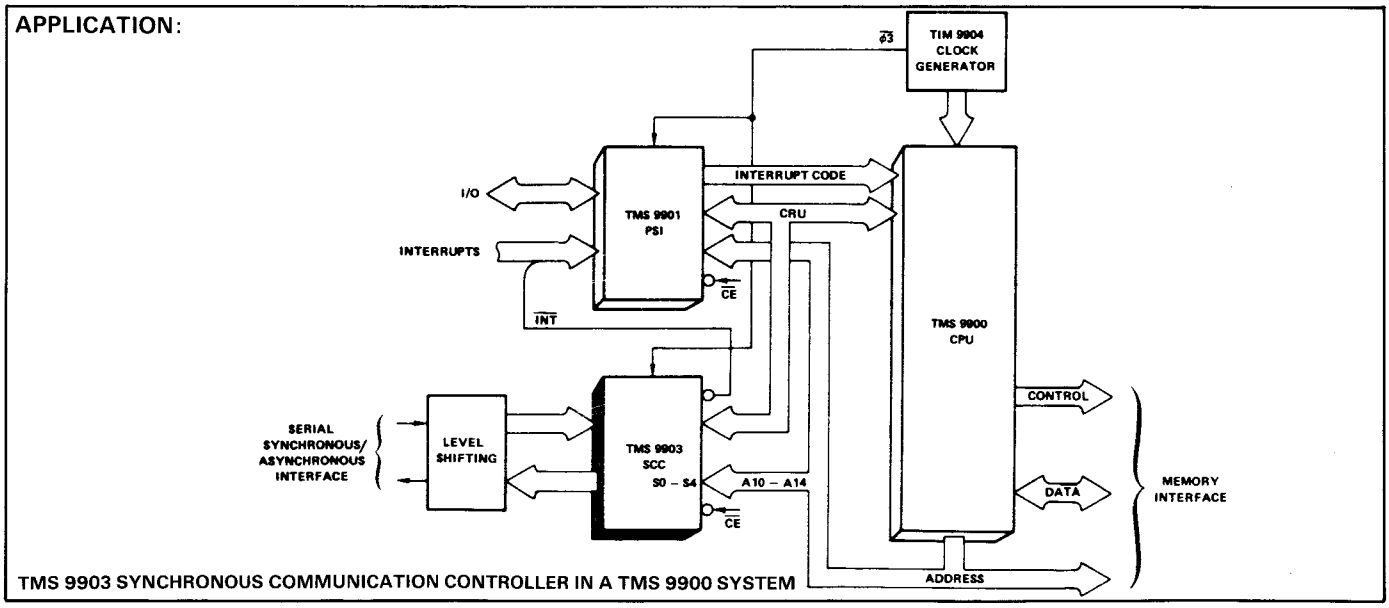
Universal applicability is further assured through the capability for dynamic character length selection from 5- to 9-bit data words plus parity. Definition and operation of all communications control is under software control and as such make upgrading to another protocol simply a matter of changing software with no hardware changes required.

The TMS 9903 interfaces directly with the CPU by means of the communications register unit (CRU) of the TMS 9900 family of microprocessor devices. All device command, status, and data transfers occur under CPU control via the CRU interface. Device reset and initialization is accomplished by software to provide maximum flexibility with minimum pin count. Data transfers occur bit serially the TMS 9903 and the CPU and are controlled via the five address lines (S0–S4), chip enable (CE), and three CRU lines (CRUIN, CRUOUT, CRUCLK).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}		2.2		V
Low-level input voltage, V_{IL}		0.6		V
Operating free-air temperature, T_A	0		70	°C

APPLICATION:



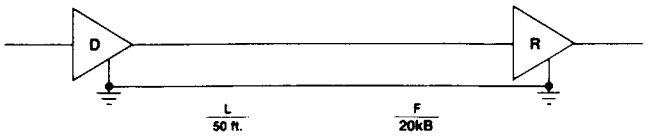
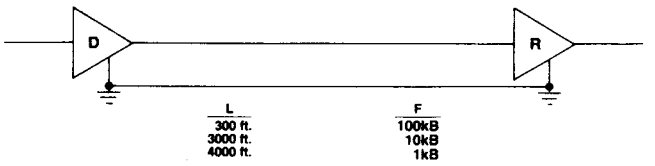
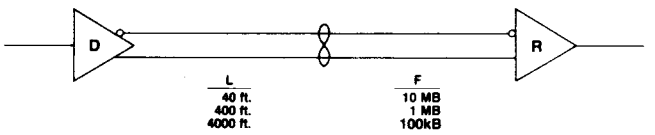
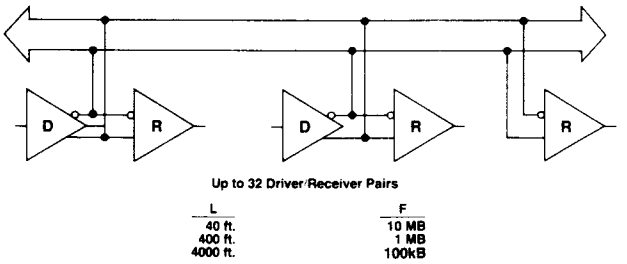
TMS 9903 SYNCHRONOUS COMMUNICATION CONTROLLER IN A TMS 9900 SYSTEM

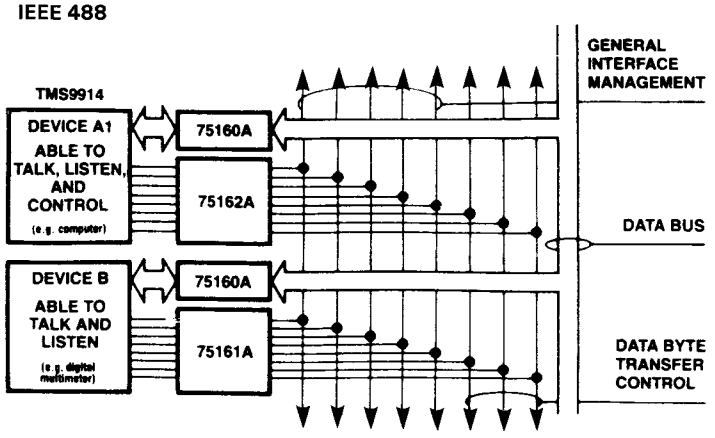
ORDERING INFORMATION:

TMS 9903 NL – 20-PIN PLASTIC DIL (3 MHz, 0/70°C)
TMS 9903 JDL – 20-PIN CERAMIC DIL (3 MHz, 0/70°C)
TMS 9903 JDE – 20-PIN CERAMIC (3 MHz, –40/85°C)
TMS 9903-40 NL – 20-PIN PLASTIC DIL (4 MHz, 0/70°C)
TMS 9903-40 JL – 20-PIN CERAMIC DIL (4 MHz, 0/70°C)

9902, 9903 LINE INTERFACES

LINE CIRCUITS SELECTION GUIDE

STANDARD L = LINE LENGTH, F = MAX. DATA RATE	DRIVERS		RECEIVERS		TRANSCEIVERS
	DUALS	QUADS	DUALS	QUADS	SINGLES
RS232 	SN75150	SN75188 MC1488	SN75152	SN75154 SN75189 SN75189A MC1489 MC1489A	NOT APPLICABLE
RS423 	μA9636A	SN75186 SN75187	μA9637A	AM26LS32A MC3486 SN75173 SN75175	NOT APPLICABLE
RS422 	SN75158 SN75159 μA9638	SN75151 SN75153 AM26LS31 MC3487 SN75172 SN75174	μA9637	AM26LS32A MC3486 SN75173 SN75175	NOT APPLICABLE
PN 1488 (RS 485) 		SN75172 SN75174		SN75153 SN75175	SN75176* SN75177* SN75178*

IEEE 488	QUAD TRANSCEIVERS	OCTAL TRANSCEIVERS
	MC3446	SN75160A SN75161A SN75162A SN75163A

LINE INTERFACES

LINE CIRCUITS SELECTION GUIDE

TABLE 1

PARAMETER		RS232	RS423	RS422	Proposed Std 1306
MODE OF OPERATION		Single Ended	Single Ended	Differential	Differential
NUMBERS OF DRIVERS AND RECEIVERS ALLOWED ON LINE		1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers
MAXIMUM CABLE LENGTH (ft.)		50	4000	4000	4000
MAXIMUM DATA RATE (Bns sec)		20 K	100 K	10 M	10 M
MAXIMUM COMMON MODE VOLTAGE		± 25 V	± 6 V	± 6 V − 0.25 V	± 12 V − 7 V
DRIVER OUTPUT SIGNAL		± 5 V min ± 15 V max	± 3.6 V min ± 6.0 V max	± 2 V min	± 1.5 V min
DRIVER LOAD		3 kΩ-7 kΩ	450Ω min	100Ω	60Ω
DRIVER SLEW RATE	30 V μs	max	*Controlled *Determined by cable length & data rate	N/A	N/A
DRIVE OUTPUT RESISTANCE (High Z state)	Power On	N/A	N/A	N/A	± 100 μA max − 7 V ≤ Vcm ≤ 12 V
	Power Off	300Ω	± 100 μA max at = 6 V	± 100 μA max − 0.25 V ≤ Vcm ≤ 6 V	± 100 μA max − 7 V ≤ cm ≤ 12 V
RECEIVER RESISTANCE		3 kΩ-7 k	>4 kΩ	>4 kΩ	>12 kΩ
RECEIVER SENSITIVITY		± 3 V	± 200 mV	± 200 mV − 7 V ≤ Vcm ≤ 7 V	± 300 mV − 12 V ≤ Vcm ≤ 12 V

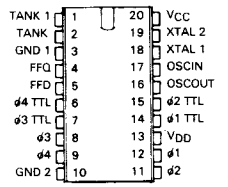
TIM 9904

CLOCK GENERATOR/DRIVER

FEATURES:

- **Single chip oscillator and clock driver for TMS 9900.**
- **Crystal controlled, LC controlled, or TTL input.**
- **3 and 4 MHz operating frequency.**
- **Low Power Schottky.**
- **Shaping and synchronization of reset signal (Schmitt-Trigger input).**
- **20 pin, 300 mil DIL.**
- **Replaces 8 SSI and MSI packages.**
- **Ceramic and plastic packages.**

PIN ASSIGNMENTS:



20 pin, 300 mil

DESCRIPTION:

The TIM 9904 four-phase clock generator/driver is a 20-pin dual-in-line package peripheral device designed for use with the Texas Instruments TMS 9900 microprocessor family and other microprocessors. The TIM 9904 internal oscillator can be controlled by a fundamental or overtone crystal, or capacitor and a tank circuit, or an external oscillator. The TIM 9904 is fabricated using low-power Schottky technology and is available in both plastic and ceramic packages.

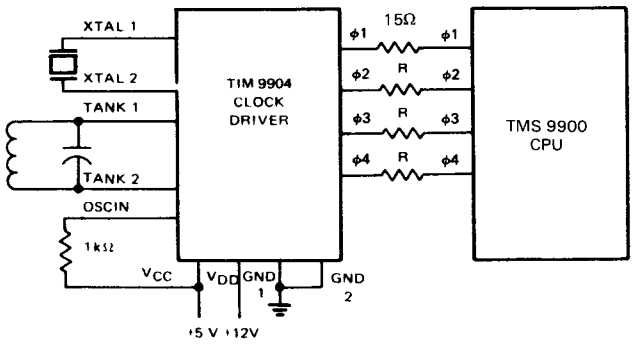
The TIM 9904 may be used in one of the following modes to provide clocking for the TMS 9900 or other microprocessor:

- *Overtone operation* – overtone crystal; tank-circuit bandpass filters the selected harmonic.
- *Fundamental operation* – fundamental crystal; tank circuit not required.
- *Tank-controlled operation* – no crystal; frequency determined as resonant frequency of the tank circuit.
- *Externally-controlled operation* – internal oscillator disabled; TTL input signal determines frequency.
- TIM 9904A uses a divide by 4 oscillator.

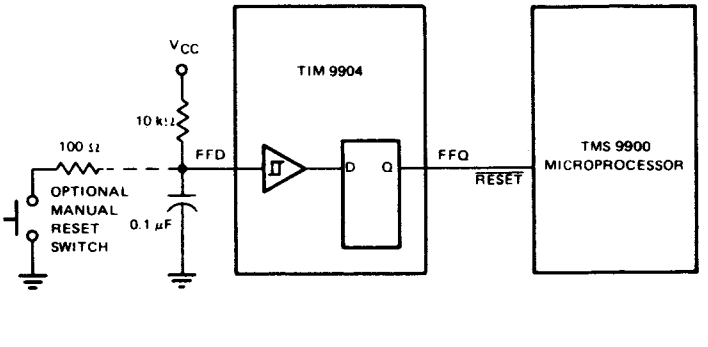
RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltages	V_{CC}	4.75	5	5.25	V
	V_{DD}	11.4	12	12.6	V
High-level output current, I_{OH}	$\phi1, \phi2, \phi3, \phi4$			−100	μA
	All others			−400	μA
Low-level output current, I_{OL}	$\phi1, \phi2, \phi3, \phi4$			4	mA
	All others			8	mA
Internal oscillator frequency, f_{OSC} –9904			48	54	MHz
Internal oscillator frequency, f_{OSC} –9904A			12	16	MHz
External oscillator pulse width, t_w (OSC)		25			ns
Set up time, FFD input (with respect to falling edge of ϕ/3, su		50			ns
Hold time, FFD input (with respect to falling edge of ϕ/3), t_h		−30			ns
Operating free-air temperature, T_A		0		70	°C

APPLICATION:



TIM 9904, CRYSTAL-CONTROLLED OPERATION



POWER-ON RESET

ORDERING INFORMATION:

TIM 9904 NL – 0/70°C 20-PIN PLASTIC 3 MHz
TIM 9904 JDL – 0/70°C 20-PIN CERAMIC 3 MHz
TIM 9904 ANL – 0/70°C 20-PIN PLASTIC 3 MHz
TIM 9904 AJDL – 0/70°C 20-PIN CERAMIC 3 MHz

TIM 9904-40 NL – 0/70°C 20-PIN PLASTIC 4 MHz
TIM 9904-40 JDL – 0/70°C 20-PIN CERAMIC 4 MHz
TIM 9904A-40 NL – 0/70°C 20-PIN PLASTIC 4 MHz
TIM 9904A-40 JDL – 0/70°C 20-PIN CERAMIC 4 MHz

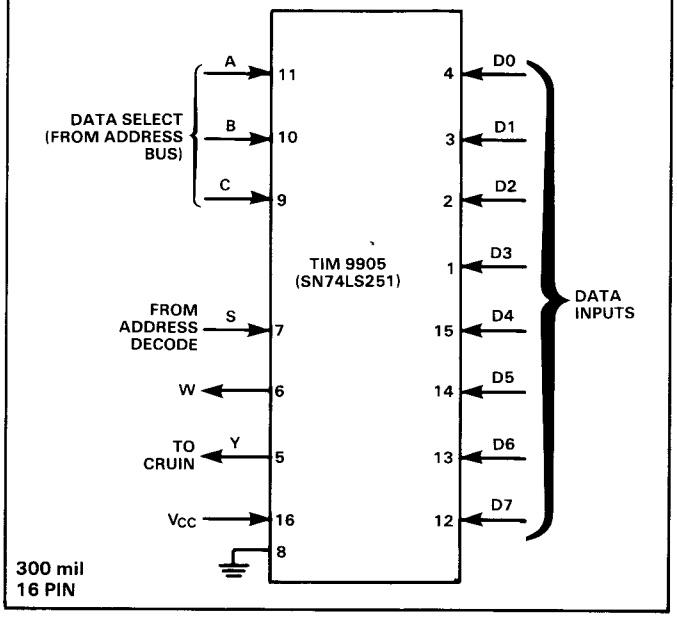
TIM 9905

DATA SELECTOR/MULTIPLEXER

FEATURES:

- Three-State Versions of '151, 'LS151, 'S151.
- Three-State Outputs Interface Directly with System Bus.
- Perform Parallel-to-Serial Conversion.
- Permit Multiplexing from N-lines to One Line.
- Complementary Outputs Provide True and Inverted Data.
- Fully compatible with most TTL circuits.
- Convenient MSI device for providing 8 or more CRU input lines for 9900 systems.
- Low-power Schottky device type SN74LS251
- Space saving 16-pin package.

PIN ASSIGNMENTS:



DESCRIPTION

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources and feature a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activiated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time. The SN54251 and SN74251 have output clamp diodes to attenuate reflections on the bus line.

FUNCTION TABLE

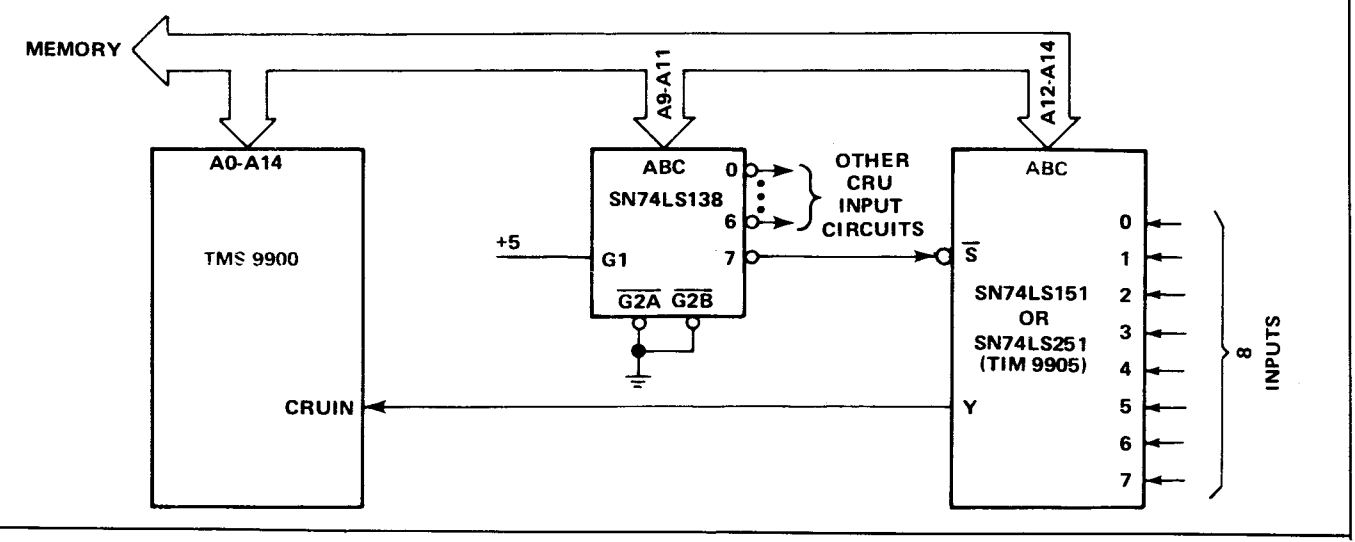
INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
X = Irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D inpı

RECOMMENDED OPERATING CONDITIONS

	SN74LS251			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−2.6	mA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	0		70	°C

APPLICATION:



ORDERING INFORMATION:

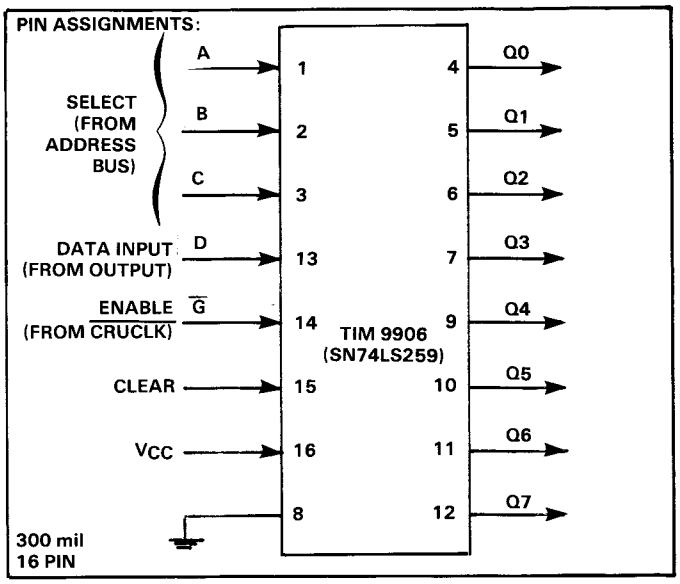
SN74LS251N – 16-PIN PLASTIC DIL – 0/70°C
SN54LS251J – 16-PIN CERAMIC DIL – –55/+125°C

FEATURES:

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion With Storage.
- Asynchronous Parallel Clear.
- Active High Decoder.
- Enable/Disable Input Simplifies Expansion.
- Expandable for N-Bit Applications.
- Four Distinct Functional Modes.
- Typical Propagation Delay Times:

	'LS259
Enable-to-Output	17
Data-to-Output	18
Address-to-Output	20
Clear-to-Output	20

- Fan-Out
  I_{OL} (Sink Current)
  SN74LS259 ..... 8 mA
  I_{OH} (Source Current)
  'LS259 ..... −0.4 mA
- Typical I_{CC}
  LS259 ..... 22 mA



DESCRIPTION:

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the date-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low.

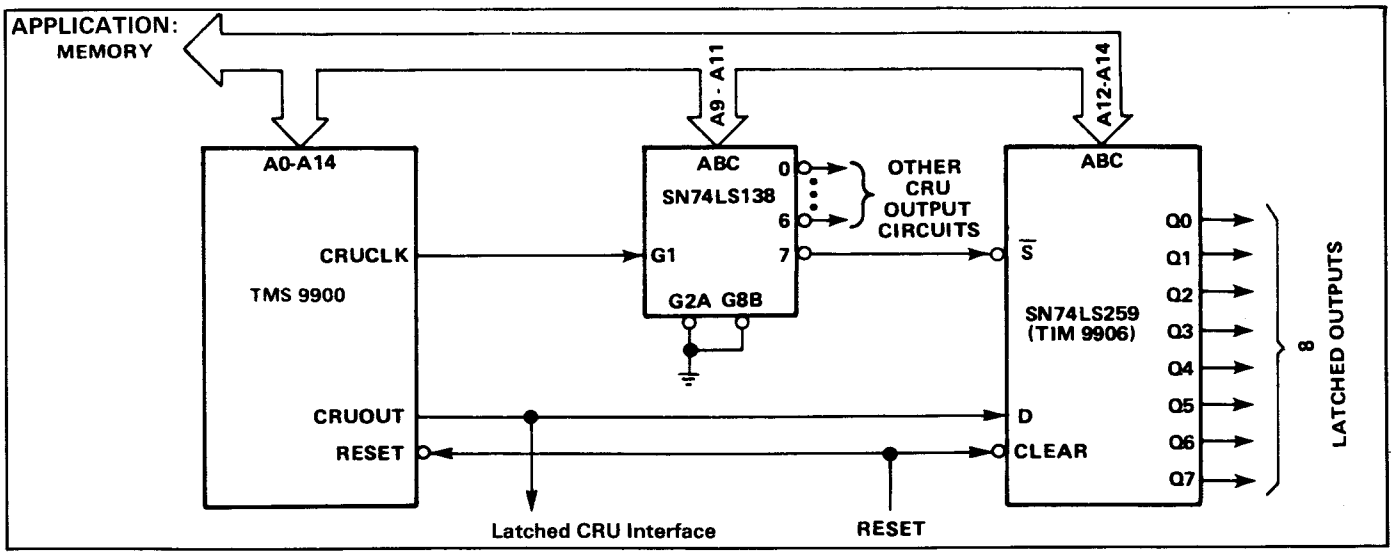
SELECT INPUTS			LATCH
C	B	A	ADDRESSED
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = high level, L = low level
D = the level at the data input
Q_{i0} = the level of Q_i ($i = 0, 1, \ldots 7$, as appropriate) before the indicated steady-state input conditions were established.

RECOMMENDED OPERATING CONDITIONS

		SN74LS259			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}				−400	μA
Low-level output current, I_{OL}				8	mA
Width of clear or enable pulse, t_w		15			ns
Setup time, t_{su}	Data	15 ↑			ns
	Address	15 ↑			
Hold time, t_h	Data	0 ↑			ns
	Address	0 ↑			
Operating free-air temperature, T_A		0		70	°C

↑The arrow indicates that the rising edge of the enable pulse is used for reference



ORDERING INFORMATION:

SN74LS259N – 16-PIN PLASTIC DIL (TIM 9906) – 0/70°C

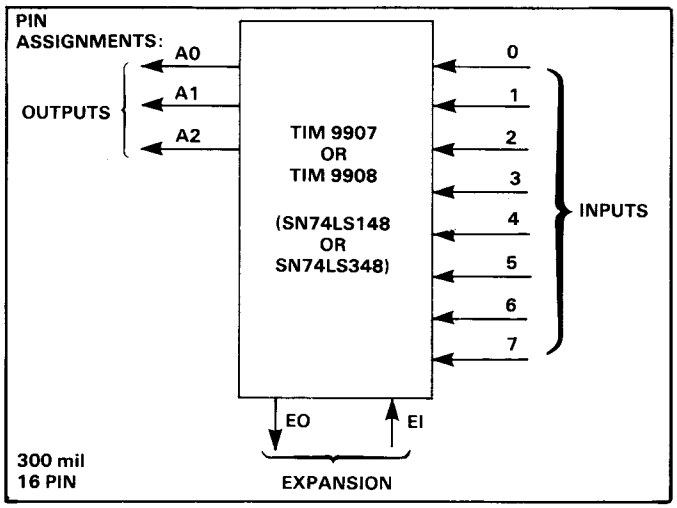
SN54LS259J – 16-PIN CERAMIC DIL – −55/+125°C

TIM 9907/08

8-TO-3 LINE PRIORITY ENCODERS

FEATURES:

- **Provides convenient means of encoding interrupts into 9900 family CPU's.**
- **Expandable with two devices to provide the full 15 levels of priority encoding for 9900 systems.**
- **TIM 9907 (SN74LS148) active outputs.**
- **TIM 9908 (SN74LS348) 3-state outputs.**



DESCRIPTION:

9907

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The '147 and 'LS147 encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. The '148 and 'LS148 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level. All inputs are buffered to represent one normalized Series 54/74 or 54LS/74LS load, respectively.

9908

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The 'LS348 circuits encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion. Outputs A0, A1, and A2 are implemented in three-state logic for easy expansion up to 64 lines without the need for external circuitry.

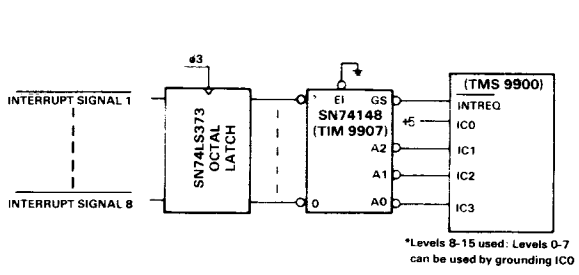
	INPUTS								OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
L	X	X	X	X	X	X	X	X	Z	Z	Z	H	H
L	H	H	H	H	H	H	H	H	Z	Z	Z	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high logic, L = low logic level, X = irrelevant
Z = high-impedance state

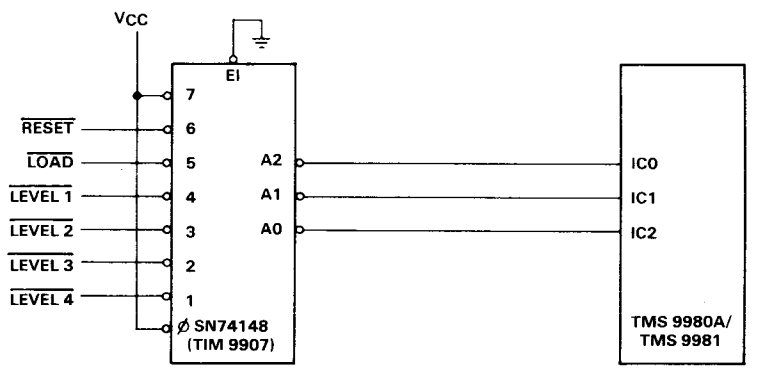
RECOMMENDED OPERATING CONDITIONS

	SN74LS148				SN74LS348			UNIT
	MIN	NOM	MAX		MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25		4.75	5	5.25	V
High-level output current, I_{OH}				A0, A1, A2			−2.6	mA
			−400	EO, GS			−400	μA
Low-level output current, I_{OL}				A0, A1, A2			24	mA
			8	EO, GS			8	mA
Operating free-air temperature, T_A	0		70		0		70	°C

APPLICATION:



Eight Input Interrupt System with Synchronization



TMS 9980A/TMS 9981 INTERRUPT INTERFACE

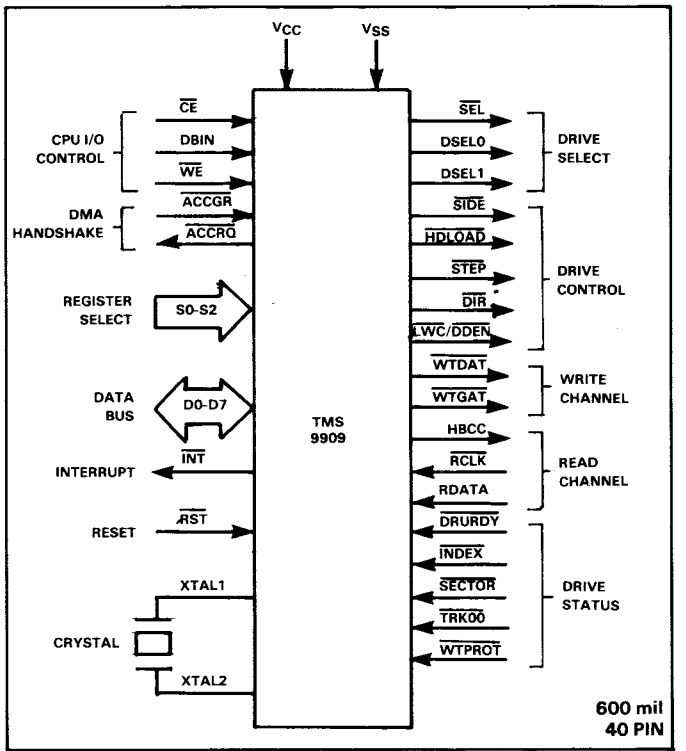
ORDERING INFORMATION:

SN74LS148N – ACTIVE O/P – 0/70°C
SN74LS348N – TRISTATE O/P – 0/70°C

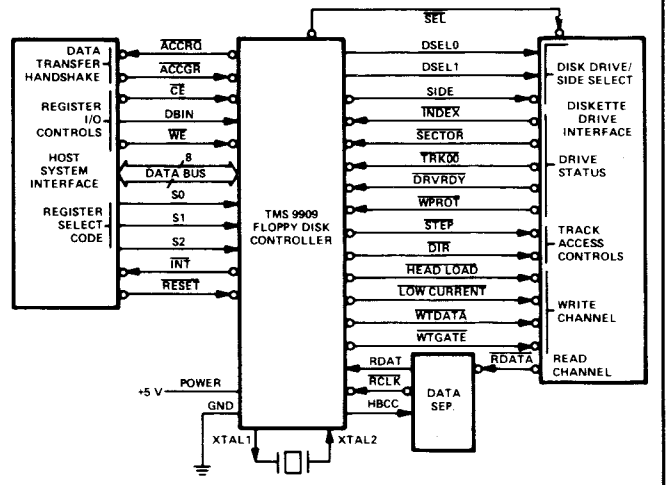
SN54LS148J – CERAMIC DIL – −55/+125°C
SN54LS348J – CERAMIC DIL – −55/+125°C

FEATURES:

- IBM 3740/System 34 compatible.
- Supports 4 single/double sided standard or mini drives.
- Supports Disks with up to 256 cylinders.
- Flexible track formatting.
- Single density FM, double density MFM, M2FM.
- Memory-mapped MPU interface for command/status transfer.
- Programmable on-chip write precompensation.
- Programmable data transfer rates (125, 250, 500 kbits/sec).
- On-chip CRC generation and verification.
- Single/multiple sector read/write for hard/soft sectoring.
- Two different disk types can be mixed on one controller.
- On-chip clock generation – needs only 6 MHz crystal.
- Programmable track step, settle and head load times.
- Single 5V supply, fully TTL compatible.
- Programmable head load and unload.



APPLICATION:



DESCRIPTION:

The TMS 9909 Floppy Disk Controller (FDC) is designed to provide complete subsystem integration of a floppy diskette mass storage capability. The FDC is a general purpose peripheral device for microprocessor systems and is programmable by the CPU for data encoding formats, number and type of diskette drives, etc. This FDC programmability offers control for the interface between most host systems and virtually any floppy disk drive produced.

The FDC performs the following functions:

- Step to any track on the diskette
- Format tracks (initialize)
- Read and write diskette data
- Send status to host system.

The TMS 9909 Floppy Disk Controller is designed to provide high-level processing features for data transfer using single- and double-density formats. Integration of the FDC system is state-of-the-art, producing maximum performance with minimized hardware complexity, low component count and reduced system cost.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5.0	5.25	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2.0			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

ORDERING INFORMATION:

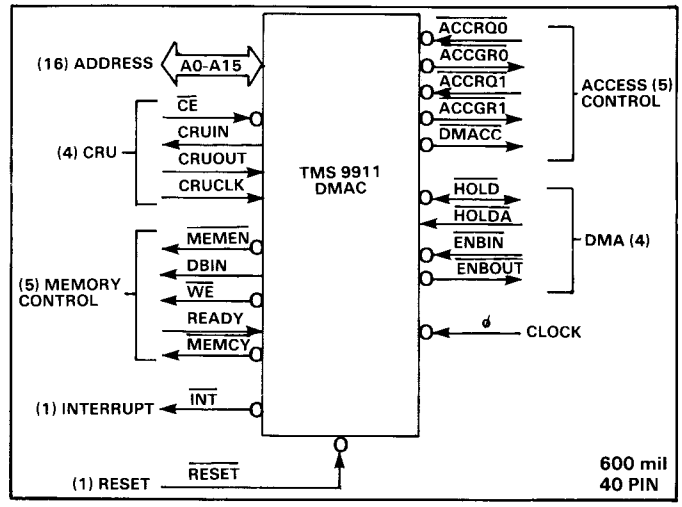
TMS 9909 NL 40-PIN PLASTIC DIL (0°/70°C)
TMS 9909 JDL 40-PIN CERAMIC DIL (0°/70°C)

TMS 9911

DMA CONTROLLER

FEATURES:

- Two independent DMA channels.
- Burst and single transfer capabilty.
- Timing control provided to accommodate slow memories.
- Transfer rate up to 1 million words/second with 3 MHz clock.
- Flexible/efficient 9900 family CRU interface to MPU.
- DMA channel prioritized chaining – allows over 100 channels on-line.
- Programmable word or byte transfers.
- TTL-compatability including power supply and clock (5-volt).
- 40-pin plastic or ceramic package.
- N-channel silicon gate MOS technology.
- Sixteen-bit address bus allows direct access to 64K bytes or 32K words.



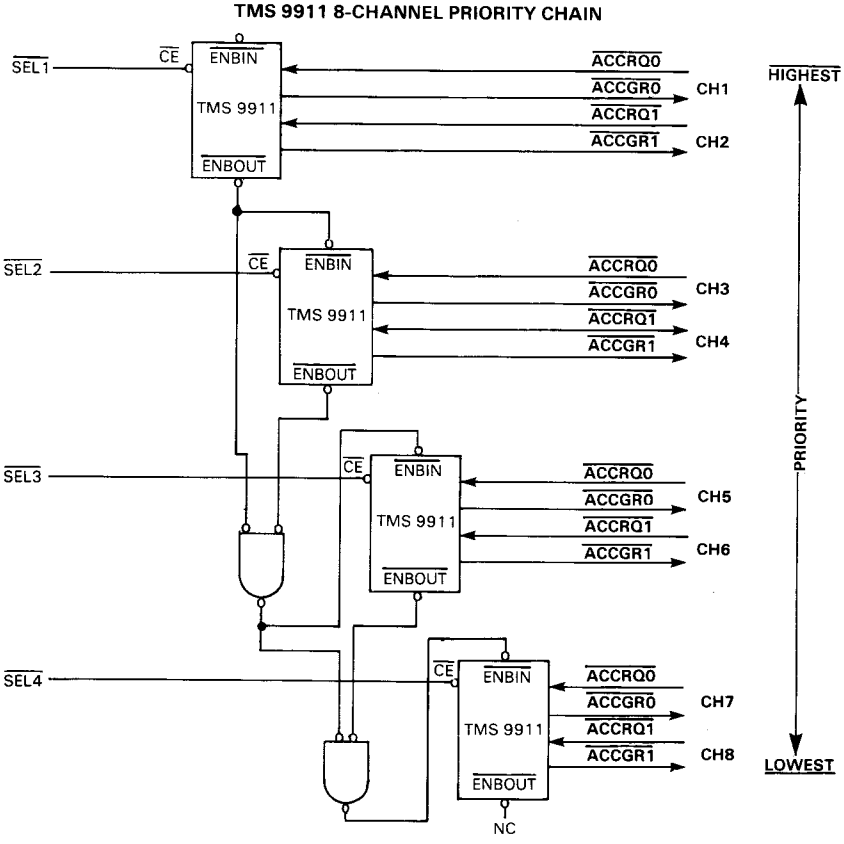
DESCRIPTION:

The TMS 9911 DMAC is an LSI member of the 9900 family of microprocessors and support peripherals. The DMAC is used in 9900 microprocessor systems where devices other than a single CPU require access to memory. The DMAC generates memory control signals and sequential memory addresses for two DMA channels (i.e., two independent DMA devices), allowing these devices to access memory autonomously with respect to the CPU. Multiple DMAC's may be used to extend the number of DMA channels beyond two. The interfaces of the DMAC to the CPU, system memory, and DMA peripheral devices are defined in such a manner as to require a minimum amount of additional electronics.

By using the CRU for set up and status of the TMS 9911, a DMA controller has been configured in a 40-pin package with no data bus at all. The TMS 9911 provides an easy-to-use cost effective method for implementing Direct Memory Access for 9900-family peripherals.

APPLICATION:

TMS 9911 8-CHANNEL PRIORITY CHAIN



CRU OUTPUT BITS

CRU BIT	NAME	DESCRIPTION
0-15	CnA(0-15) OR CnL(0-15)	MEMORY ADDRESS REGISTER OR LAST ADDRESS REGISTER
16	CnASEL	CHANNEL ADDRESS SELECT
17	CHENBn	CHANNEL ENABLE
18	CNTNUn	CONTINUE AFTER LAST ADDRESS
19	MEINRDn	MEMORY READ
20	WRDSLn	WORD SELECT
21	OPCMPn	OPERATION COMPLETE
22	ITENBn	INTERRUPT ENABLE

CRU INPUT BITS

CRU BIT	NAME	DESCRIPTION
0-15	CnA(0-15) OR CnL(0-15)	MEMORY ADDRESS REGISTER OR LAST ADDRESS REGISTER
16	CnASEL	CHANNEL ADDRESS SELECT STATUS
17	CHENBn	CHANNEL ENABLE STATUS
18	CNTNUn	CONTINUE STATUS
19	MEINRDn	MEMORY READ STATUS
20	WRDSLn	WORD SELECT STATUS
21	OPCMPn	OPERATION COMPLETE STATUS
22	IENBn	INTERRUPT ENABLE STATUS
23	CHACTn	CHANNEL n ACTIVE
24	—	NOT USED
25	CHSEL	CHANNEL SELECT STATUS
26	INT0	CHANNEL 0 INTERRUPT
27	INT1	CHANNEL 1 INTERRUPT
28-29	—	NOT USED
30	CHAIN	CHAIN STATUS
31	DMAPRS	DMA PRESENT

ORDERING INFORMATION:

TMS 9911 NL – 40-PIN PLASTIC DIL (3 MHz, 0/70°C)
TMS 9911-40 NL – 40-PIN PLASTIC DIL (4 MHz, 0/70°C)
TMS 9911 JDL – 40-PIN CERAMIC 3 MHz 0/70°C
TMS 9911-40 JDL – 40-PIN CERAMIC 4 MHz 0/70°C

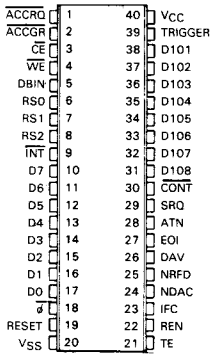
TMS 9914A

GPIB ADAPTER

FEATURES:

- Handles all IEEE 488-1975/78 functions.
- Talker and listener functions (T, TE, L, LE).
- Automatic source and acceptor handshakes (SH, AH).
- Controller with pass control capabilities (C).
- System controller capabilities.
- Device clear and trigger functions (DC, DT).
- Service request functions (SR).
- Parallel and serial poll facilities (PP, SP).
- Remote/local with local lockout (RL).
- Single or dual addressing modes.
- Secondary addressing capabilities.
- Direct I/F to SN75160/1/2 bus transceivers.
- Compatible with most microprocessors.
- DMA facilities (compatible with TMS 9911).
- Memory-mapped microprocessor interface.

PIN ASSIGNMENTS:



600 mil
40 PIN

DESCRIPTION:

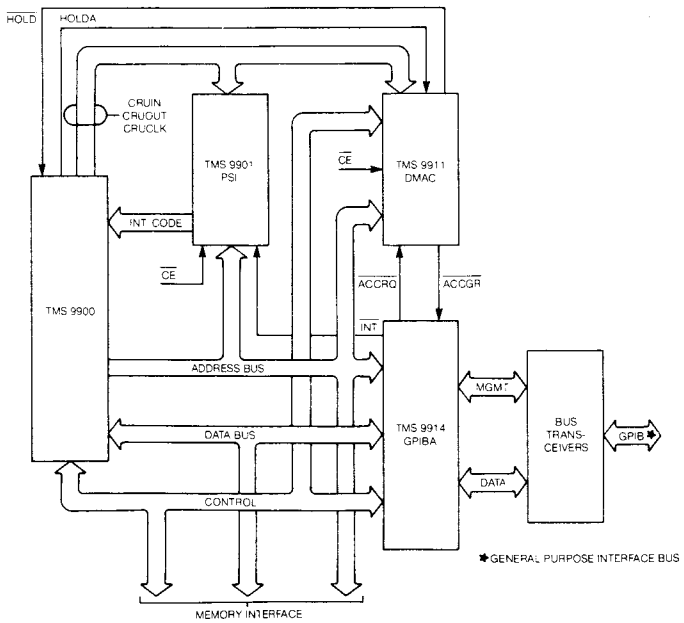
The TMS 9914A is designed to perform the interface function between an IEEE-488-1975/78 General Purpose Interface Bus (GPIB) and a microprocessor. It communicates with the microprocessor via a memory-mapped 8-bit data bus and provides a 16-bit bus to interface with the GPIB via buffer devices. IEEE 488-1975/78 standard protocol is handled automatically in Talker, Listener or Controller operational modes.

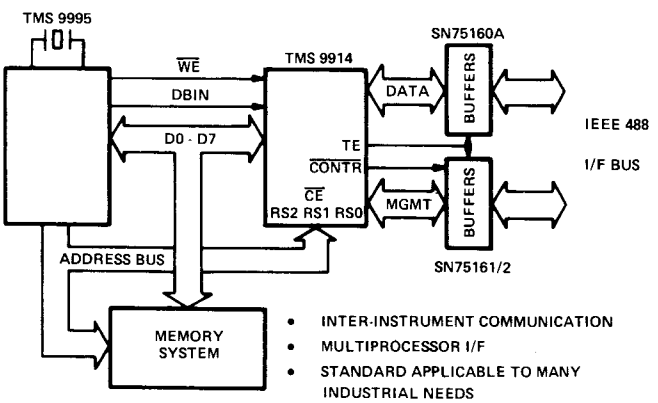
Using this standard, a variety of instruments can be interconnected and remotely or automatically programmed and controlled. The TMS 9914A is fabricated with N-channel silicon-gate technology and is completely TTL compatible on all inputs and outputs including the power supply (+5V). It needs a single phase clock (nominally 5 MHz) which may be independent of the microprocessor system clock and, therefore, it can easily be interfaced with most microprocessors.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5.0	5.25	V
Supply voltage, V_{SS}		0.0		V
High-level input voltage, V_{IH}	2.0		V_{CC} +1	V
Low-level input voltage, V_{IL} (MPU side)	V_{SS}–.3		0.8	V
Low-level input voltage, V_{IL} (GPIB side)	V_{SS}–.3		0.8	V
Operating free-air temperature, T_A	0		70	°C

APPLICATION:





ORDERING INFORMATION:

TMS 9914A NL – 40-PIN PLASTIC DIL (0/70°C)
TMS 9914A JDL – 40-PIN CERAMIC DIL (0/70°C)

TMS 9918A/28A/29A

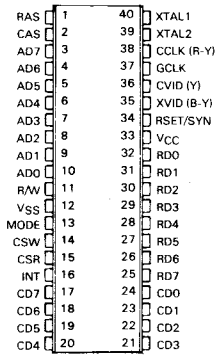
VIDEO DISPLAY PROCESSOR

FEATURES:

- **Single-chip interface to colour TV's (excluding RAM and RF mode).**
- **256 × 192 resolution on TV screen.**
- **16 unique colour (including transparent).**
- **General 8-bit bi-directional interface to MPU.**
- **Automatic and transparent refresh of drams.**
- **External video input capability.**
- **Easy to use for text, graphics, animation.**
- **Unique planar representation allows 3-D simulation.**
- **Standard 40-pin plastic package, 5-volt.**
- **N-channel silicon-gate technology.**
- **9918/18A – NTSC output (composite video)**
- **9928 – colour difference/luminance O/P, 625 lines.**
- **9929 – colour difference O/P – 525 lines.**

PIN-OUT:

9918A PIN-OUT (9928/29)



600 mil
40 PIN

DESCRIPTION:

This specification defines the functional, electrical, and timing requirements for the Video Display Processor (VDP). The VDP is an N-Channel MOS LSI device used in video systems where data display on a raster-scanned home colour television is required. The VDP generates all necessary video, control, and synchronisation signals, and additionally controls the storage, retrieval, and refresh of display data in the dynamic screen refresh memory. The interfaces to the microprocessor, refresh memory, and the TV are defined so as to require a minimum of additional electronics.

The VDP has three video colour display modes: pattern graphics, multicolour, and text. The text mode provides twenty-four 40-character rows in two colours and is intended for computer oriented displays. The multicolour mode provides an unrestricted 64 × 48 dot display in 15 colours. The pattern graphics mode provides a 256 × 192 pixel display and is primarily intended for use in game and educational applications. All 15 colours are also available in the pattern graphics mode.

The video display consists of thirty-five display planes: external video, backdrop, pattern, and sprites 0-31. The planes are vertically stacked with the external video being the bottom or innermost plane. The backdrop plane is the next plane, and the 32 sprite planes are the top planes. A sprite is a special animation pattern used in the pattern graphics and multicolour modes.

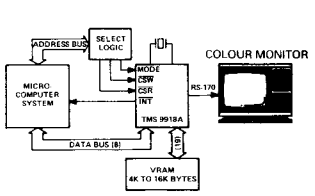
The VDP uses 4K or 16K RAS/CAS memories for storage of the display parameters and for microprocessor temporary data storage.

RECOMMENDED OPERATING CONDITIONS

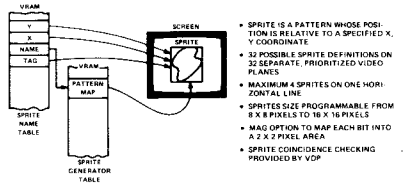
PARAMETER	MIN	NOM	MAX	UNIT
Sync level input voltage, reset V_{IHS}	10.0			V
Supply voltage, V_{CC}	4.75	5.0	5.25	V
Supply voltage, V_{SS}		0.0		V
High-level input voltage, V_{IH} (not reset)	2.2			V
Low-level input voltage, V_{IL} (all pins)			0.8	V
High-level input voltage, V_{IHR} (reset)	.3			V
Operating free-air temperature, T_A	0		55	°C

APPLICATION:

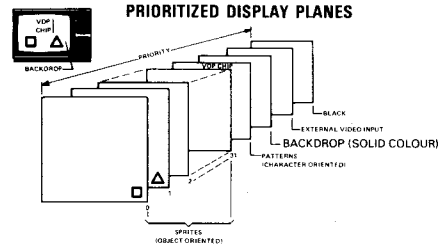
SYSTEM CONFIGURATION



VIDEO DISPLAY PROCESSOR SPRITES



PRIORITIZED DISPLAY PLANES



ORDERING INFORMATION:

TMS 9918ANH – 40-PIN PLASTIC DIL (0/55°C), NTSC COMP. VIDEO
TMS 9928 ANH – 40-PIN PLASTIC DIL (0/55°C), 525 LINES
TMS 9929 ANH – 40-PIN PLASTIC DIL (0/55°C), 625 LINES
TMS 9918 AJDH – 40-PIN CERAMIC DIL (0/55°C), NTSC COMP. VIDEO
TMS 9928 AJDH – 40-PIN CERAMIC DIL (0/55°C), 525 LINES
TMS 9929 AJDH – 40-PIN CERAMIC DIL (0/55°C), 625 LINES

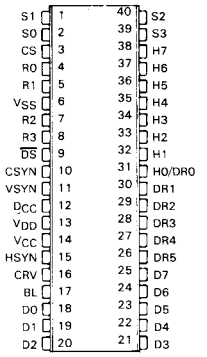
TMS 9927/37

VIDEO TIMER/CONTROLLER

FEATURES:

- Second sourced by SMC as CRT5027/5037.
- TTL Compatibility.
- Standard and Non-standard CRT Monitor Capability.
- Scrolling Capability.
- Interlaced and Non-interlaced Formatting.
- Fully Programmable Display Format.
  - Characters per data row
  - Data rows per frame
  - Raster scans per data row
  - Raster scans per frame
- Fully Programmable Monitor Format
  - Blanking
  - Horizontal sync
  - Vertical sync
  - Composite sync
- Two Programming Methods
  - Processor controlled
  - PROM on data bus
- Generation of Cursor Video
- N-channel Silicon-Gate Technology

PIN-OUT:



600 mil
40 PIN

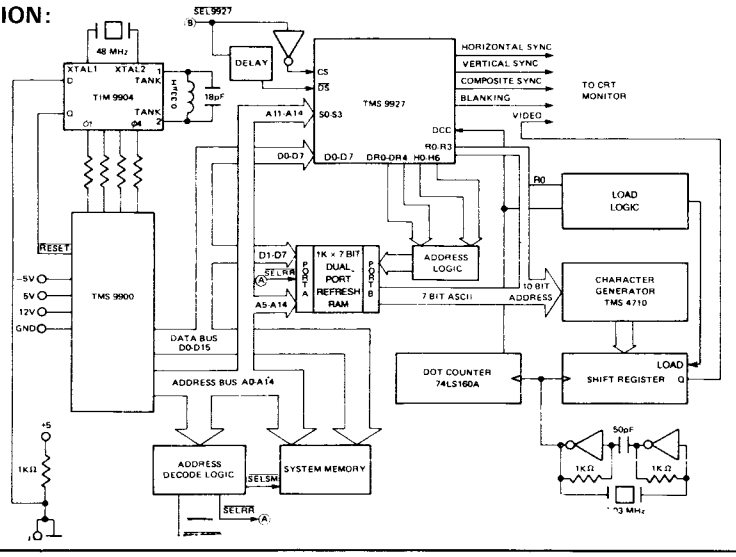
DESCRIPTION:

The TMS 9927 is a single-chip Video Timer/Controller from Texas Instruments produced by Silicon-Gate, NMOS technology. The 40-pin TMS 9927 device generates video display timing signals for standard and non-standard CRT monitors incorporating both interlaced and non-interlaced formats. The TMS 9927 is designed as a memory-mapped I/O device, but can be communicated with over a CRU interface via the TMS 9901. The TMS 9927 provides nine, user-programmable control registers. Seven of the registers control horizontal and vertical formatting, and two control the cursor address. The inherent flexibility of the control registers makes possible a wide variety of cost-effective applications using the versatile TMS 9927.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Ground reference, V_{SS}		0		V
High-level input voltage, V_{IH}	$V_{CC}-1.5$		V_{CC}	V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

APPLICATION:



- 16 rows of 64 characters
- Noninterlaced format
- 5 x 7 display matrix embedded in an 8 x 12 field
- 63.5 μsec per horizontal sweep
- Vertical refresh 60 times per second
- Monitor has 262 scans per frame.

ORDERING INFORMATION:

TMS 9927 NL – 40-PIN PLASTIC DIL PACKAGE (0/70°C)
TMS 9927 JDL – 40-PIN CERAMIC DIL PACKAGE (0/70°C)

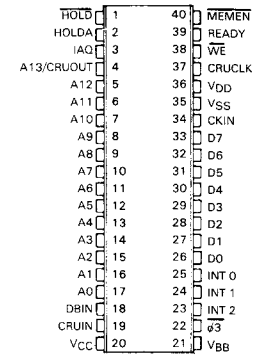
TMS 9980A/81

16-BIT MICROPROCESSOR (8-BIT DATA BUS)

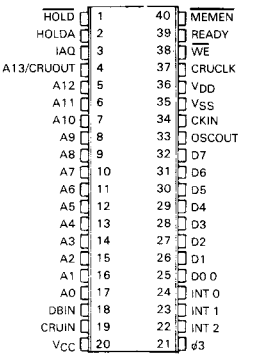
FEATURES:

- 16-Bit Instruction Word.
- Full Minicomputer Instruction Set Capability including Multiply and Divide.
- Up to 16,384 Bytes of Memory.
- 8-Bit Memory Data Bus.
- Advanced Memory-to-Memory Architecture.
- Separate Memory, I/O, and Interrupt-Bus Structures.
- 16 General Registers.
- 4 Prioritized Interrupts.
- Programmed and DMA I/O Capability.
- On-Chip 4-Phase Clock Generator.
- 40-Pin Package.
- N-Channel Silicon-Gate Technology.

TMS 9980A PIN ASSIGNMENTS



TMS 9981 PIN ASSIGNMENTS



600 mil
40 PIN

DESCRIPTION:

The TMS 9980A/TMS 9981 is a software-compatible member of TI's 9900 family of microprocessors. Designed to minimize the system cost for smaller systems, the TMS 9980A/TMS 9981 is a single-chip 16-bit central processing unit (CPU) which has an 8-bit data bus, on-chip clock, and is packaged in a 40-pin package (see Figure 1). The instruction set of the TMS 9980A/TMS 9981 includes the capabilities offered by full minicomputers and is exactly the same as the 9900's. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort. Texas Instruments provides a compatible set of MOS and TTL memory and logic function circuits to be used with a TMS 9980A/TMS 9981 system.

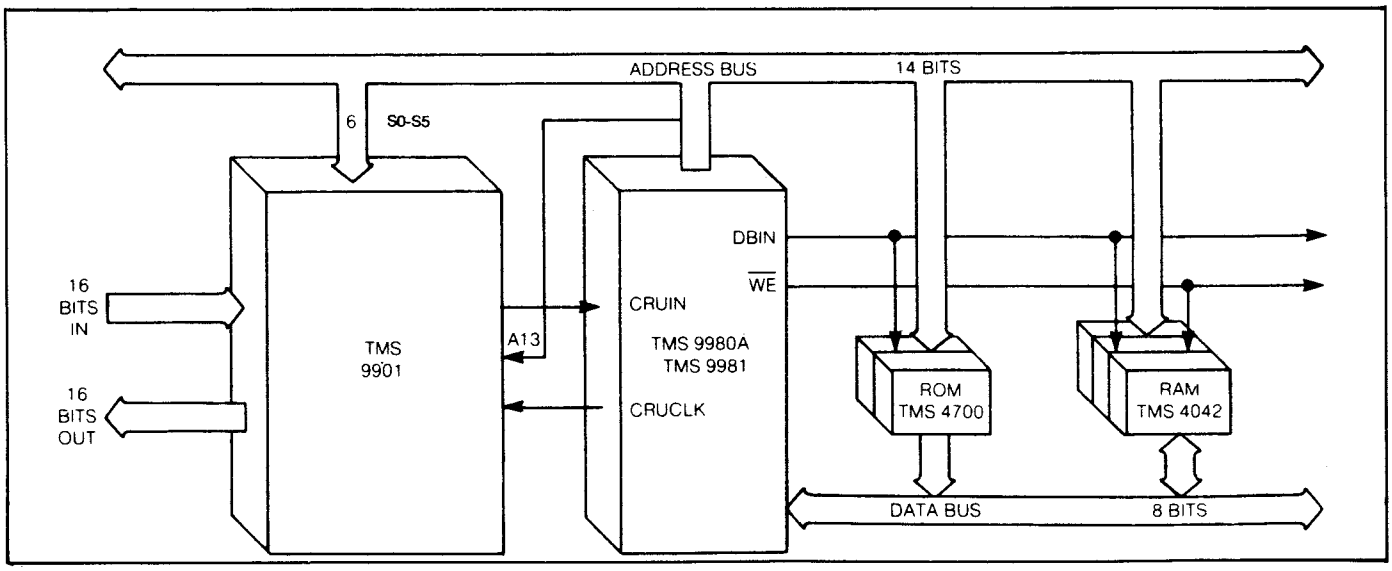
TMS 9980A/TMS 9981 DIFFERENCES

The TMS 9980A and the TMS 9981 although very similar, have several differences which user should be aware.

1. The TMS 9980A requires a V_{BB} supply (pin 21) while the TMS 9981 has an internal charge pump to generate V_{BB} from V_{CC} and V_{DD}.
2. The TMS 9981 has an optional on-chip crystal oscillator in addition to the external clock mode of the TMS 9980A.
3. The pin-outs are not compatible for D0-D7, INT0-INT2, and $\overline{\phi 3}$.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB} (9980A only)	−5.25	−5	−4.75	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2.2	2.4	V_{CC} +1	V
Low-level input voltage, V_{IL}	−1	0.4	0.8	V
Operating free-air temperature, T_A	0	20	70	°C



ORDERING INFORMATION:

TMS 9980A NL – 40-PIN PLASTIC DIL – 10 MHz 0/70°C
TMS 9980A JDL – 40-PIN CERAMIC DIL – 10 MHz 0/70°C
TMS 9981 NL – 40-PIN PLASTIC DIL – 10 MHz 0/70°C
TMS 9981 JDL – 40-PIN CERAMIC DIL – 10 MHz 0/70°C

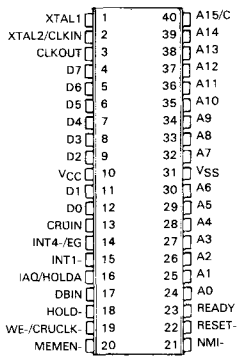
TMS 9995

16-BIT MICROCOMPUTER

FEATURES:

- 64K bytes of memory expansion
- 256 bytes of on-chip RAM.
- 12 MHz crystal oscillator.
- Separate memory, I/O, and Interrupt bus structure.
- Serial I/O via Communications Register Unit (CRU).
- 5 prioritized, vectored interrupts.
- 9900 family instruction set plus signed multiply and divide, load status, load workspace.
- Optional automatic first-wait-state generation.
- Single 5-volt operation, NMOS technology.
- 40-pin package (Plastic and Ceramic).
- 16-bit instruction word, 8-bit data bus.
- On-chip timer/event counter.
- On-chip programmable flags (16).
- Illegal opcode detection.

PIN ASSIGNMENTS:

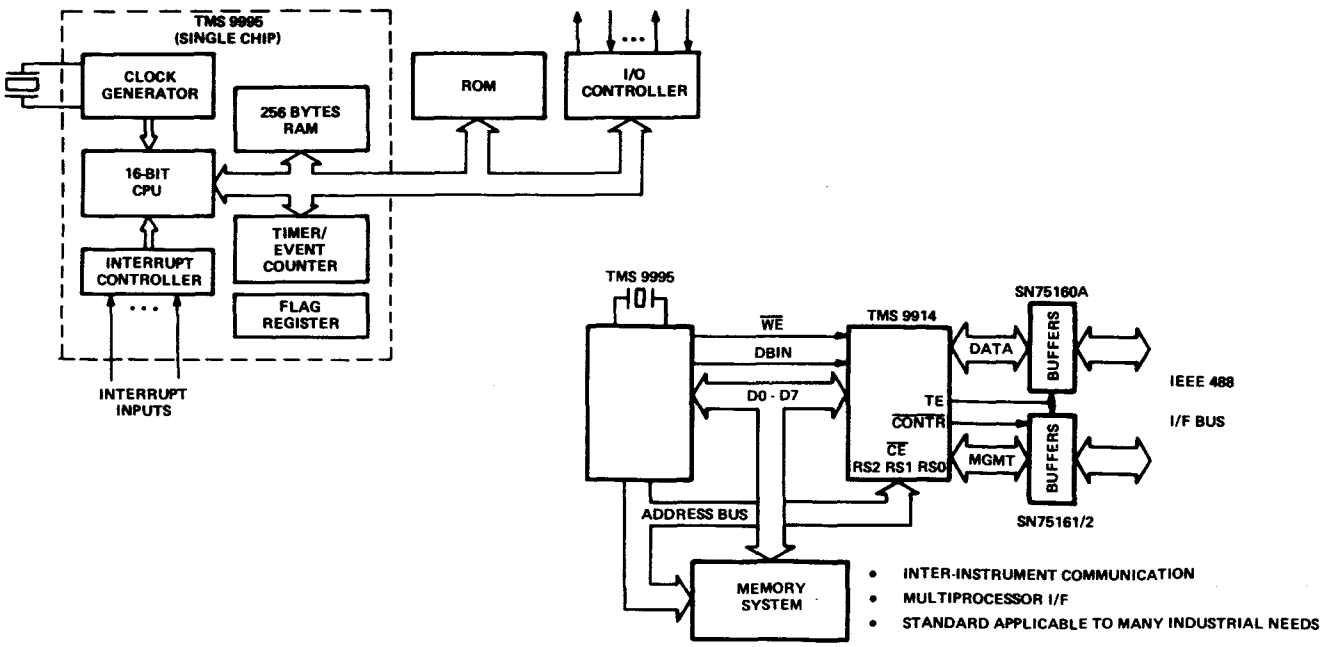


600 mil
40 PIN

DESCRIPTION:

The TMS 9995 microprocessor is a single chip 16-bit central processing unit (CPU) with 256 bytes of on-chip RAM produced using N-channel silicon-gate MOS technology. The instruction set of the TMS 9995 includes capabilities offered in minicomputers, and its unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort.

APPLICATION:



ORDERING INFORMATION:

TMS 9995 NL – 12 MHz PLASTIC 40-PIN DIL (0/70°C)
TMS 9995 JDL – 12 MHz CERAMIC 40-PIN DIL (0/70°C)

TMS 9995

16-BIT MICROCOMPUTER

"FOR MINIMUM CHIP/HIGH PERFORMANCE MICROPROCESSOR SYSTEMS"

FEATURE	BENEFIT
256 BYTES ON-CHIP RAM	• ELIMINATES NEED FOR EXTERNAL RAM IN SMALL SYSTEMS • INCREASED SYSTEM THROUGHPUT
ON-CHIP TIMER/EVENT COUNTER	• REDUCE I/O PACKAGES
SEVEN PRIORITIZED INTERRUPTS	• EASE OF IMPLEMENTATING CONTROLLERS
AUTO WAIT STATE	• SYSTEM IMPLEMENTATION WITH SLOW MEMORIES W/O EXT. LOGIC
16-BIT INSTRUCTION SET	• COMPUTATIONAL PRECISION & EXECUTION SPEED
LOAD STATUS & WP REGISTER INSTRUCTION	• FACILITATES USE OF HLL

TMS 9995 EVALUATION MODULE (TMAM6095)

HARDWARE:

- $8\frac{1}{2}$" × 11" free-standing board format.
- Large prototyping area (4" × 8").
- Two EIA RS-232 serial ports.
- 1K bytes no-wait-state RAM.
- Three user-configurable 28-pin memory sockets to support most "X8" memory devices.
  - 8K to 64K bit EPROMS, ROMS.
  - "X8" RAMS.
  - Bipolar PROMS.

SOFTWARE (IN EPROM):

- Debug monitor.
- Symbolic assembler (supports forward label references).
- Disassembler.
- Communications link package to enable connection of host development system.

FEATURES COMPARISON

	9995	6809	8088
ON-CHIP RAM	256	0	0
ON-CHIP TIMER	YES	NO	NO
ON-CHIP PROGRAMMABLE FLAGS	YES	NO	NO
ON-CHIP INTERRUPT CONTROLLER	YES	NO	NO
ON-CHIP CLOCK	YES	YES	NO
BIT SERIAL I/O	YES	NO	NO
INSTRUCTION PREFETCH	YES	NO	YES
PRIORITIZED INTERRUPTS	7	2	2
NUMBER OF INTERRUPTS	7	3	3
CLOCK FREQUENCY	12 MHz	2 MHz	5 MHz
MINIMUM CHIP COUNT	3	4	8

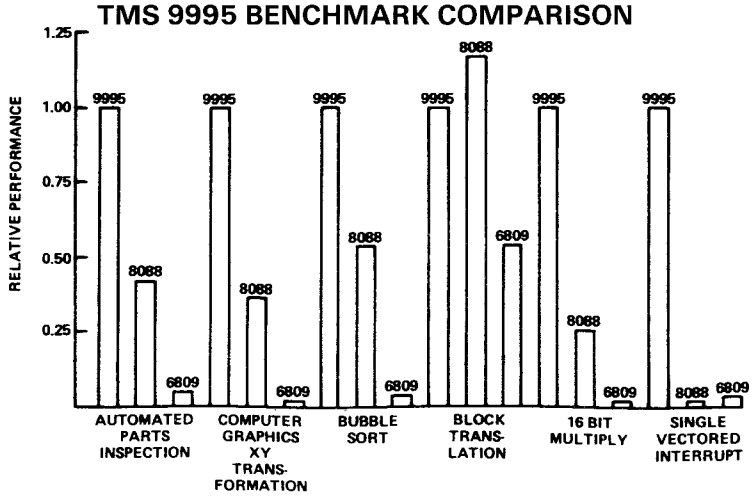
BENCHMARK* COMPARISON

	AUTOMATED PARTS INSPECTION (sec)	COMPUTER GRAPHICS XY TRANSFORM (sec)	BUBBLE SORT (ms)	BLOCK TRANSLATION (ms)	16 BIT MULTIPLY (μs)	SINGLE VECTORED INTERRUPT (μs)
9995 (12 MHz) w/120 ns PROM	0.666	0.863	1.240	1.767	10.00**	8.00
9995 (12 MHz) w/450 ns EPROM	0.950	1.081	1.956	2.696	12.67	10.67
8088 (5 MHz) w/450 ns EPROM	1.596	2.402	2.254	1.522	40.8	77.6
6809 (2 MHz) w/450 ns EPROM	9.67	57.1	2.376	3.01	91.9	27.6
9900 (3 MHz) w/450 ns EPROM	2.053	2.709	3.068	4.593	22.0	12.0

* Intel application note AFN01551A, Intel Corporation, Santa Clara, California 1980.

**7.67 μs if multiplicands don't have to be saved.

TMS 9995 BENCHMARK COMPARISON



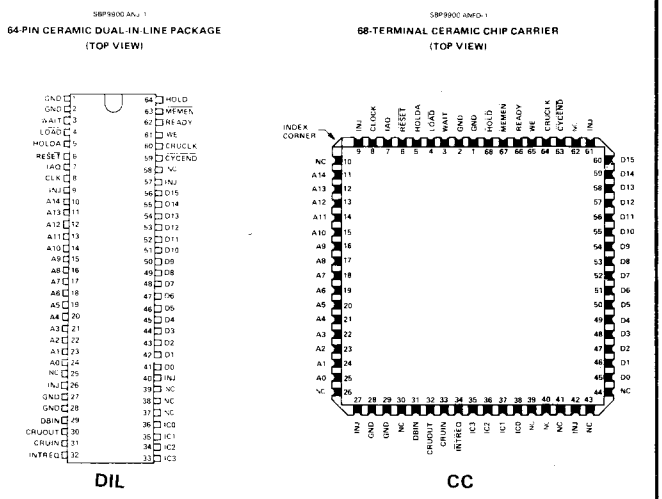
SBP 9900A

16-BIT BIPOLAR MICROPROCESSOR

FEATURES:

- Parallel 16-Bit word length.
- Full minicomputer Instruction Set.
- Directly addresses up to 65,536 Bytes/32,768 words.
- Advanced memory to memory architecture.
- Multiple 16-word Register Files (work space) resident.
- Separate I/O Memory and Interrupt Bus Structures.
- Sixteen prioritized Hardware interrupts.
- Sixteen Software Interrupts (XOPS).
- Programmed and DMA I/O capability.
- Serial I/O via Communications-Register-Unit (CRU).
- Selectable speed/power operations.
- Directly TTL Compatible I/O (including Clock).
- Advanced Integrated Injection Logic (AI²L) technology.
- Functionally identical to TMS 9900 device.
- Radiation-hardened (due to I²L technology).
- Meets full military temperature range (–55/125°C).

PIN ASSIGNMENTS:



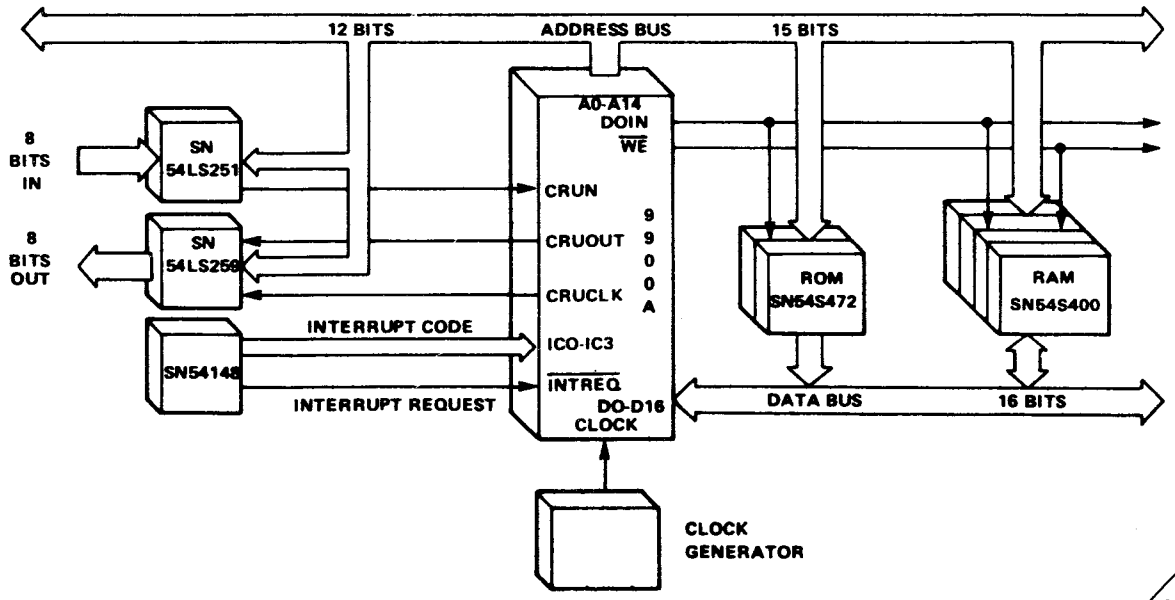
900 mil
64 PIN

DESCRIPTION

The SBP 9900A is a 16-bit microprocessor implemented in a single LSI device using advanced integrated injection logic (I²L) technology. The SBP 9900A is a member of a family of microprocessors and minicomputers, that shares a common architecture and a common instruction set. Also available with the SBP 9900A are the unique power programmability characteristics of I²L that permit very low power operation, i.e., input power and clock frequency may be reduced proportionally and the microprocessor continues to operate. The SBP 9900A operates over the full military temperature range and is tested according to BS 9000 and MIL883B requirements.

Texas Instruments is applying the SBP 9900A in systems applications ranging from simple sensor/actuator controllers to sophisticated multiprocessor computing systems.

APPLICATION:



ORDERING INFORMATION:

SBP 9900A NJ-IBS – –55/125°C, BS 9000 PROCESSING, 3 MHz, DIL
SBP 9900A NJ-I – –55/125°C, 883 B PROCESSING, 3 MHz, DIL
SBP 9900A NFD-I – –55/125°C, 883 B, 3 MHz, CHIP-CARRIER

NOT RECOMMENDED FOR NEW DESIGN
EVALUATE SBP 9989 overleaf

SBP 9989

ADVANCED 16-BIT BIPOLAR MICROPROCESSOR

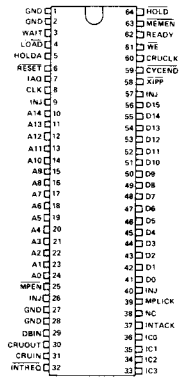
FEATURES:

- **Plug-compatible with SBP 9900A, plus:**
- **Added instructions**
  - **Signed multiply**
  - **Signed divide**
  - **Load workspace pointer**
  - **Load status register**
- **Added functions**
  - **Multiprocessor interlock**
  - **Interrupt acknowledge/pending**
  - **Memory map signal**
  - **External instruction processor I/F**
- **Added status bits 7 through 11.**
- **Improved HOLD/HOLDA interface**
- **Unused/illegal OP code interrupt.**
- **Ready handshake for CRU input.**
- **Arithmetic overflow interrupt**

CONDITION	THROUGHPUT
SBP 9989 USING SAME SOFTWARE AT 3.0 MHz	1.24X
SBP 9989 USING SAME SOFTWARE AT 4.4 MHz	1.82X
SBP 9989 USING MPYS AND DIVS AT 3.0 MHz	1.56X
SBP 9989 USING MPYS AND DIVS AT 4.4 MHz	2.28X

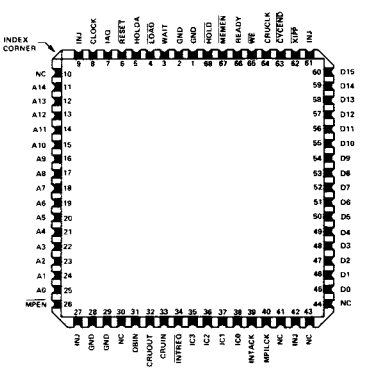
PIN ASSIGNMENTS:

SBP9989NJ
64-PIN CERAMIC DUAL-IN-LINE PACKAGE
(TOP VIEW)



DIL

SBP9989NFD
68-TERMINAL CERAMIC CHIP CARRIER
(TOP VIEW)



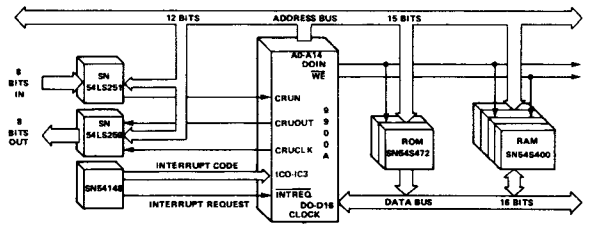
CC

900 mil
64 PIN

DESCRIPTION:

The SBP 9989 is a second generation, bipolar 16-bit microprocessor offering twice the performance of the SBP 9900A. Implemented in Texas Instruments' Advanced I^2L technology, the SBP 9989 features the same environmental ruggedness and inherent reliability of its predecessor. It is feasible to convert existing SBP 9900A designs to the SBP 9989, and it is downward compatible with all of TI's existing micro- and mini-computer products. It employs the advanced memory-to-memory architecture that ensures optimal performance in the structured I/O intensive applications of the '80s. Physical changes required to adapt an SBP 9900A socket to the SBP 9989 are minor and include: (1) Pulling XIPP- (pin 58) to a logic 1.2 mA (from 1.0 mA for SBP 9900A), and (4) Adjusting Injector Power Supply to provide VINJ = 1.25V at IINJ = 400 mA. Additionally, a software audit should be completed to ensure timing differences do not cause a software malfunction.

APPLICATION:



INSTRUCTION TYPE	NUMBER OF TIMES USED IN MIX	NUMBER OF CLOCKS TO EXECUTE INSTRUCTIONS SBP 9900A	SBP 9989	9989 THROUGHPUT INCREASE
MOVE	26	572	416	1.38
JUMP	23	207	207	138
ARITHMETIC	14	280	238	1.18
COMPARE	9	198	162	1.22
PROGRAM TRANSFER	7	147	126	1.17
DATA TRANSFER	6	78	72	1.08
LOGICAL	6	120	96	1.25
SHIFT	5	165	165	1.00
SIGNED MULTIPLY SIGNED DIVIDE	2	658	122	5.39
TOTAL	100 INSTRUCTIONS	2505 CLOCKS	1609 CLOCKS	1.56

ORDERING INFORMATION:

SBP 9989 NJ – 883 B PROCESSING, –55/125°C – 4.4 MHz
SBP 9989 NJ-BS – BS 9000 PROCESSING, –55/125° (TO BE APPROVED)

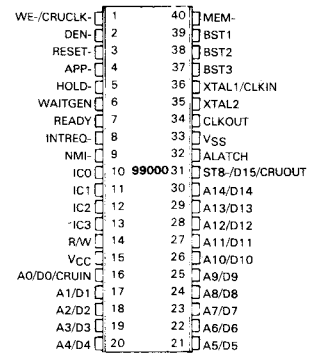
TMS 99000 SERIES

ADVANCED 16-BIT MICROPROCESSOR FAMILY

FEATURES:

- 6 MHz internal operation.
- 24 MHz on-chip clock generation.
- Multiplexed 16-bit data/address bus.
- Directly addresses three 64K byte memory pages.
- Supports 16M byte segmented memory using TIM 99610 mapper.
- Additional instructions (87 total).
  - Signed multiply and divide.
  - Load status register, load workspace pointer.
  - 32-bit addition, subtraction and shifting.
  - Stack operation support – branch and push link.
    – branch indirect.
  - * – Address expansion instructions – load map file.
    – long distance source.
    – long distance destination.
  - Multiprocessor support – test, test and set, test and clear.
- Priviledged instruction trap permits user/supervisor modes.
- Unique on-chip memory (macrostore) for customised instructions.
- Attached processor interface (full access to PC, WP, ST).
- Multiprocessor interlock output signal.
- 16 bus-status codes to identify processor activity.
- Arithmetic overflow interrupt.
- Optional automatic generation of first wait-state for slow memory.
- Instruction prefetch (pipelining) for increased throughput.
- 16 hardware prioritised vectored interrupts.
- Interrupt acknowledge signal.
- Unique CRU I/O for both serial and parallel data transfer.
- DMA interface.
- Single 5-volt, 40-pin package.
- N-channel silicon gate SMOS technology.

PIN ASSIGNMENTS:



600 MIL
40 PIN

PIN ASSIGNMENTS

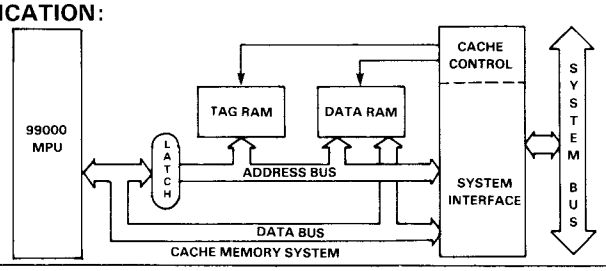
DESCRIPTION:

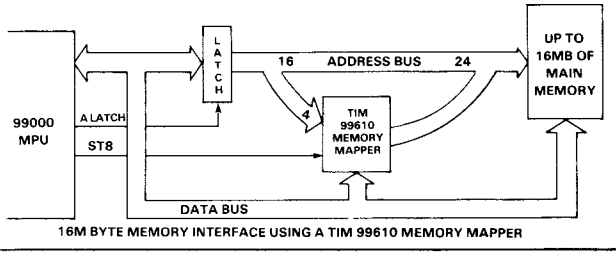
The 99000 series is a family of single-chip 16-bit central processing units (CPU) and peripheral circuits produced using N-channel silicon-gate scaled MOS technology. The instruction set of the 99000 provides capabilities offered by full minicomputers. The unique memory-to-memory architecture features multiple register files, resident in memory, to permit faster response to interrupts and increased programming flexibility. The 99000 series adds several innovative features to a well-proven architecture oriented towards real-time system applications. A unique internal/external memory, the macrostore, allows customisation of the instruction set, both by users and by TI, while taking full advantage of the single 167 nanosecond machine state cycle memory access time.

As well as very fast raw processing speed (see benchmarks) the 99000 has an attached processor interface which facilitates the passing of control to dedicated attached processors/computers. This improves the throughput of the overall system in a way that is completely transparent to the software, allowing an orderly migration in performance from software to firmware (macrostore) to attached processors and finally attached computers, which have local memory and can perform functions in parallel with other computers.

Texas Instruments manufacturers a compatible set of MOS and TTL integrated circuits to provide memory and logic functions for the 99000 system. The system is fully supported by software and complete prototyping systems ranging from low-cost board systems to single-user floppy and multi-user hard-disk AMPLUS systems.

APPLICATION:





TMS 99000 MICROPROCESSOR FAMILY INSTRUCTION SET

MNEMONIC	DESCRIPTION	MNEMONIC	DESCRIPTION
A	Add Word (16-bit)	LWPI	Load Workspace Pointer Immediate
AB	Add Byte (8-bit)	MOV	Move Word
ABS	Absolute Value	MOVB	Move Byte
AI	Add Immediate	MPY	Multiply
AM	Add Multiple (32-bit)	MPYS	Signed Multiply
ANDI	AND Immediate	NEG	Negate
B	Branch	ORI	OR Immediate
BIND	Branch Indirect	RSET	External Reset
BL	Branch and Link	RTWP	Return to Workspace Pointer
BLWP	Branch and Load Workspace Pointer	S	Subtract (16-bit)
BLSK	Branch Immediate and Push Link to Stack	SB	Subtract Byte (8-bit)
C	Compare Word	SBO	Set Bit to One (I/O)
CB	Compare Byte	SBZ	Set Bit to Zero (I/O)
CI	Compare Immediate	SETO	Set Word to Ones
CKOF	External Clock Off	SLA	Shift Left Arithmetic
CKON	External Clock On	SLAM	Shift Left Arithmetic Multiple (32-bit)
CLR	Clear Word	SM	Subtract Multiple (32-bit)
COC	Compare Ones Corresponding	SRA	Shift Right Arithmetic
CZC	Compare Zeroes Corresponding	SRAM	Shift Right Arithmetic Multiple (32-bit)
DEC	Decrement	SRC	Shift Right with Carry
DECT	Decrement by Two	SRL	Shift Right Logical
DIV	Divide	SOC	Set Ones Corresponding Word
DIVS	Signed Divide	SOCB	Set Ones Corresponding Byte
IDLE	Idle Processor	STCR	Store Communications Register Unit (I/O)
INC	Increment	STST	Store Status
INCT	Increment by Two	STWP	Store Workspace Pointer
INV	Invert	SWPB	Swap Bytes
JXX	Jump (1-unconditional, 12-conditional)	SZC	Set Zeroes Corresponding Word
LDD*	Lond Distance Destination (Memory Mapper Control)	SZCB	Set Zeroes Corresponding Byte
LDCR	Load Communications Register Unit (I/O)	TB	Test Bit (I/O)
LDS*	Long Distance Source (Memory Mapper Control)	TCMB	Test and Clear Memory Bit
LI	Load Workspace Register Immediate	TMB	Test Memory Bit
LIMI	Load Interrupt Mask Immediate	TSMB	Test and Set Memory Bit
LMF*	Load Map File (Memory Mapper Control)	X	Execute
LREX	Load External	XOP	Extended Operation (software context switch)
LST	Load Status Register	XOR	Exclusive-OR
LWP	Load Workspace Pointer		

***These instructions implemented on TMS 99110 and TMS 99120 only.**
NOTE: Floating Point (TMS 99110) and Rx instructions (TMS 99120) are not listed.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNITS
Supply voltage, V_{CC}	4.5	5.0	5.5	V
Supply voltage, V_{SS}		0.0		V
High-level input voltage, V_{IH} (all inputs)	2.0		$V_{CC}+1$	V
Low-level input voltage, V_{IL} (all inputs)	−1		0.8	V
High-level output current, I_{OH} (all outputs)			400	μA
Low-level output current, I_{OL}(all ouputs)			2.0*	mA
Operating free-air temperature, T_A	0		70	°C

*Output current of 2.0 mA is sufficient to drive 5 low-power schottky TTL loads (worst case).

ORDERING INFORMATION:

TMS 99105 NL/JDL – 40-PIN PLASTIC/CERAMIC DIL. EXECUTES SAME INSTRUCTION SET AS 9995. NO INTERNAL MACROSTORE (0–70°).

TMS 99110 NL/JDL – 40-PIN PLASTIC/CERAMIC DIL. FULL 99000 INSTRUCTION SET. MACROSTORE PRE-PROGRAMMED WITH FLOATING-POINT INSTRUCTIONS (0–70°C).

INSTRUCTION SET. MACROSTORE PRE-PROGRAMMED WITH KERNEL OF REAL TIME EXECUTIVE (RX) (0–70°C).

NEW ADDITION

TMS 99000 SYSTEM BRIEF

A THIRD GENERATION OF MICROPROCESSOR COMPONENTS, SOFTWARE, AND SUPPORT

The new TMS 99000 microprocessor family has harnessed advanced design concepts into a memory-intensive architecture, which represents true third generation features and performance. The TMS 99000 is a third generation descendent of the TMS 99000 16-bit microprocessor, sharing the same advanced memory-to-memory architecture of the TMS 9900. With TMS 99000 instruction set as a superset of the TMS 9900, full object code compatibility is maintained. Speed of the TMS 99000 microprocessors is from 5 to 12 times faster than the first generation TMS 9900, 2 times faster than the second generation TMS 9995, and up to 3 times faster than other currently available processors.

However with today's computing needs, raw processor performance alone does not determine microprocessor selection. Memory costs, software adaptability, and a clearly defined migration path among cost/performance options all contribute to design decisions. The TMS 99000 family was conceived to facilitate a wide spectrum of cost/performance options – from small systems to large, multiprocessor environments.

Cost/performance flexibility is attained by providing a path for migrating functions from software to higher performance hardware designs. Additionally, a machine-cycle efficient memory interface allows a choice of very fast (<60 ns) memory devices for maximum performance or optionally, slower, less expensive memory devices. Thus, through a selection of software-to-hardware migration and memory options, flexibility in configuration for optimum system cost and performance is attained. This capability enables designers to address the dynamic marketplace problems of the '80s.

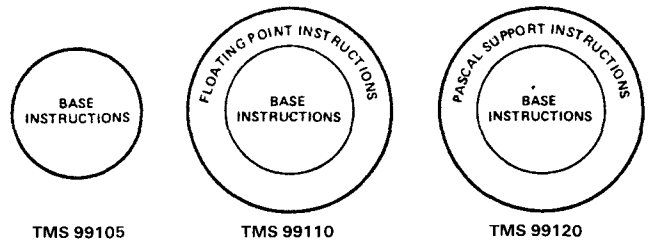


FIGURE 1 – TMS 99000 FAMILY PROCESSORS

Key features of the TMS 99000 family of microprocessors include:

- Unique VLSI memory-to-memory architecture
- Performance
  - 167 ns machine state cycle time
  - Single machine state cycle memory access
- 85 instructions
- 256K byte memory addressability, 16MB with mapping
- Instruction privileging
- 16 hardware prioritized vectored interrupts + NMI
- Serial or parallel I/O transfers
  - I/O data bit, byte, and word addressable
- Attached processor and computer interface
- 16 bus status codes
- DMA interface
- Single 5-volt operation
- 40-pin package
- N-channel silicon gate SMOS technology
- On-chip clock generator

APPLICATION SPECIFIC CPU'S

Flexibility within the TMS 99000 family of CPU's is enhanced through different versions of the same architecture with functions added to the same base instruction set. Through these added functions, a TMS 99000 CPU is tailored to specific tasks. The first members of the TMS 99000 family to be introduced are a base line processor (TMS 99105), a floating point processor (TMS 99110), and a high level language processor, which contains commonly used utilities of the PASCAL language (TMS 99120). Future processors can include support for functions such as linked lists, business applications, and scientific applications. With this approach, the TMS 99000 family of processors can satisfy the requirements of a broad price/performance spectrum while maintaining upward software compatibility.

Peripheral Family

The TMS 99000 family includes members of the powerful 9900 family of peripherals: data communications devices, a floppy disk controller, an IEEE-488 bus interface, video timers and controllers, a powerful color video display processor, and a wide range of interface support circuits.

The 99000 family of peripherals will be expanding to meet the emerging system requirements of the '80s. Devices in definition and development include man-machine interface, speech processing, data communications peripherals such as a high-speed multiprotocol processor, and mass storage support devices such as Winchester disk controller chip sets. Together the TMS 99000 family of peripherals will comprise a powerful family of VLSI support devices, which will in turn be supported with TI's component software. Component software modules will be migrated to the silicon of the peripheral function achieving an unsurpassed level of functionality.

Development Tools

The TMS 99000 family is today supported by an unmatched existing base of software and hardware development systems and software support tools. The powerful Advanced Microprocessor Prototyping Laboratory (AMPL) has seen wide use in development of software and hardware for the TMS 9900, TMS 9940, and the TMS 9995 microprocessors. The AMPL development systems allows the system designer to utilize the efficiences inherent in higher-level languages such a Microprocessor PASCAL, thus increasing programmer productivity. AMPL system options range from low-cost single user systems to cost efficient multi-user hard disk based systems. A photo of the AMPL development labs and options available is shown in Figure 2.

The powerful library of component software was conceived for the TMS 9900 microprocessor. Again due to maintaining full object code compatibility with the TMS 9900, the TMS 99000 can efficiently use this existing software base.

Component software consists of software application modules, which are tied together through a real-time executive "bus" just as peripheral devices are tied together through a common hardware bus. The modularity of component software modules allows the system designer to select only the software functions needed for a specific application without the burden of purchasing a large application program which may contain more functions and consume more memory space than necessary. This modularity also supports eventual migration of the software function to a pure silicon solution, i.e., hardware.

Customer Support

To help system designers take full advantage of the technological capabilities offered by Texas Instruments, a number of Technology Centres have been established. (There is one in Bedford). The Regional Technology Centres (RTCs) provide training in the use of TI products – from microprocessors to speech. Courses and seminars are provided in systems design, software development, and technological overviews. In addition, design services for customer applications may be contracted.

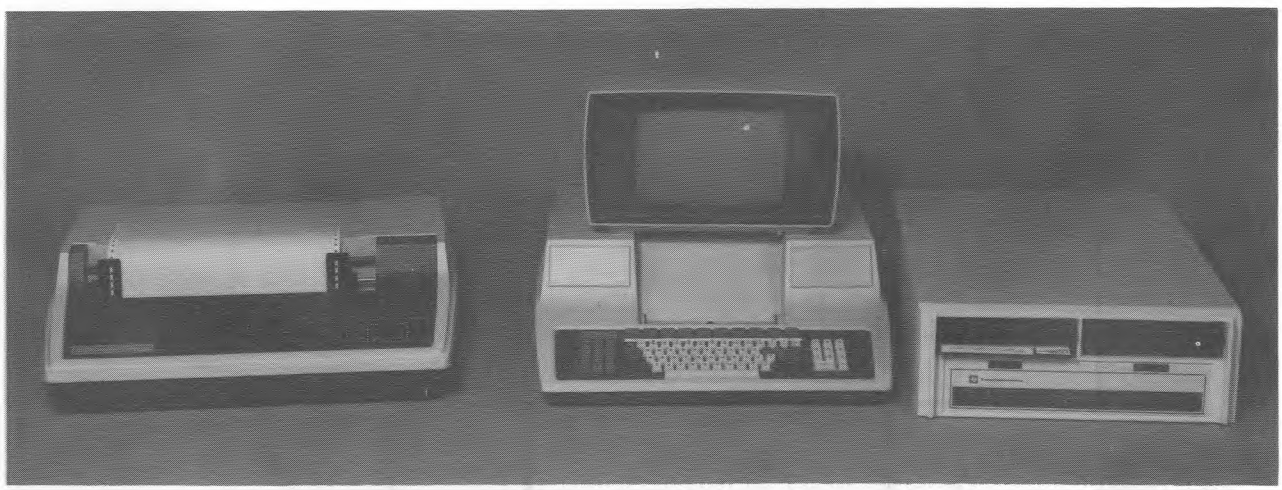


FIGURE 2 – AMPL MICROPROCESSOR PROTOTYPING LABS

THE TMS 99000 MICROPROCESSOR FAMILY – FUNCTIONAL EXTENSIBILITY

As previously discussed, a predefined path for migrating software functions to hardware solutions has been designed into the TMS 99000 family CPU's. This migration path, illustrated in Figure 3, includes: an innovative concept called macrostore, attached processors, and attached computers. Each progressive step in the migration path can result in improving system performance. The impact of these migration steps is represented graphically in Figure 4. Note that a function execution is segmented into four definable steps: invocation, parameter passage, execution, and completion processing.

The migration of the software emulation routine to on-chip macrostore can result in significantly reduced execution time. Execution time is further reduced by performing the function in an attached processor, which essentially executes functions in line with the code execution of the host TMS 99000 CPU. Attached computers remove the effective function execution time completely by allowing concurrent processing with the host TMS 99000. Concurrency is possible due to the private memory capability of the attached computer thus allowing the host TMS 99000 continued access to the memory bus.

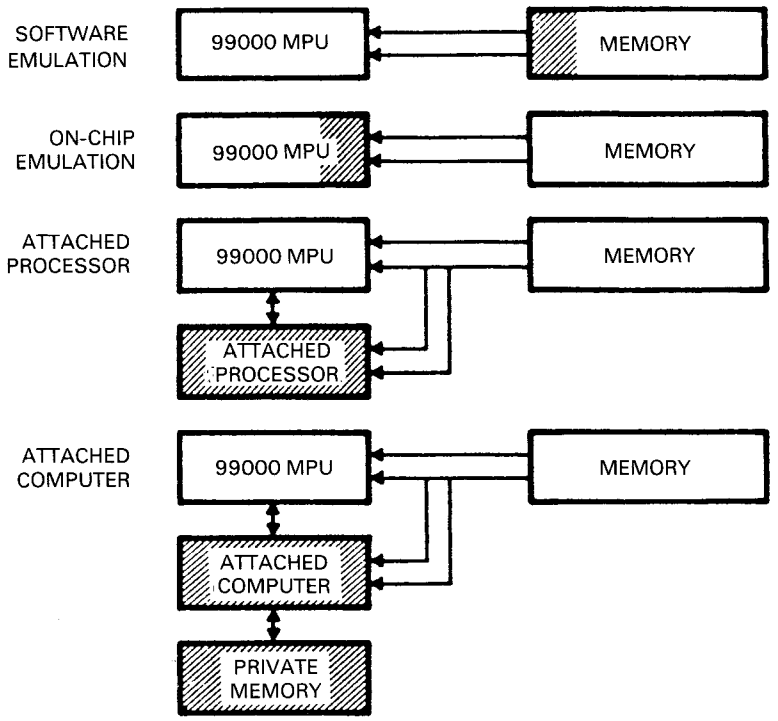


FIGURE 3 – FUNCTION MIGRATION PATHS

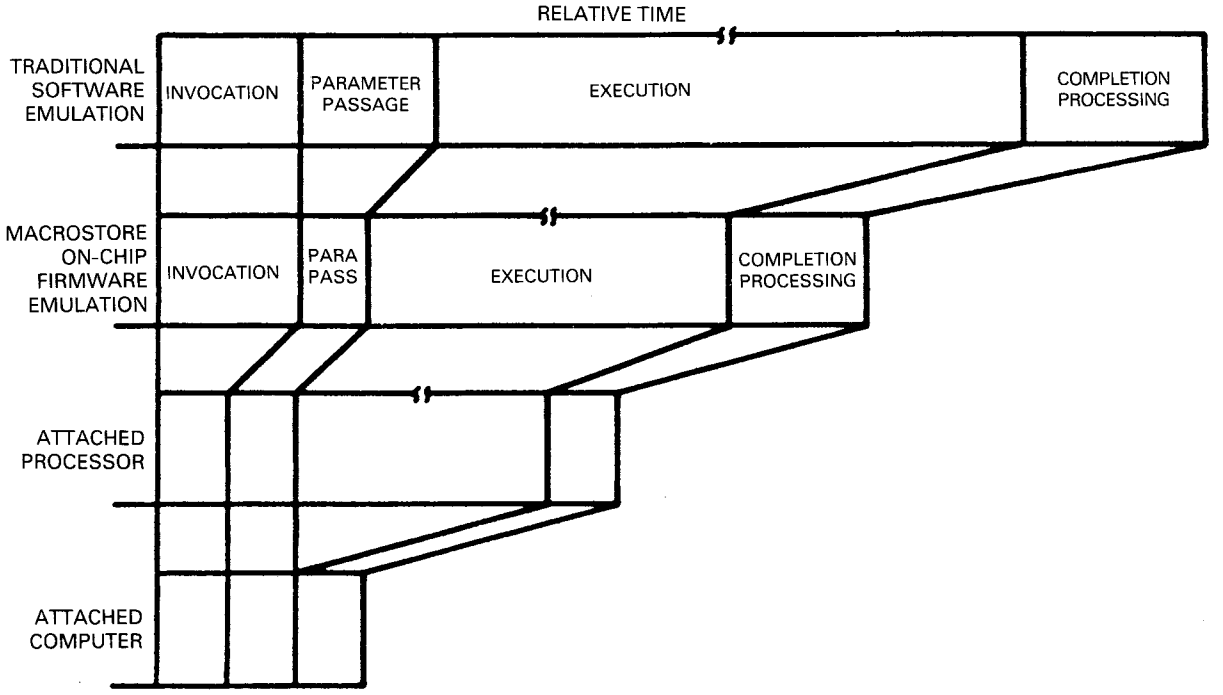


FIGURE 4 – PERFORMANCE IMPACT OF FUNCTION MIGRATION

During normal instruction, fetch, and execute sequences the TMS 99000 family processors perform a decision process shown in Figure 5.

When each instruction is fetched from main memory, several paths of execution may be followed. If the opcode is a standard instruction, i.e., a native instruction of the processor, the instruction is executed through normal on-chip sequences of microcode. If the opcode is not standard, i.e., an illegal or otherwise undefined opcode, the TMS 99000 will test the attached processor/computer interface to determine if an attached processor/computer is waiting to perform the function. If the attached processor or computer is present, the attached processor or computer is invoked; and the TMS 99000 either waits or continues depending on whether an attached processor or an attached computer is present. If no external processors are present, a reference is made to the separate macrostore memory space to determine if an emulation routine resides for that specific opcode. If the emulation routine is found in macrostore, execution control is transferred to this separate memory space to complete execution of the function or instruction – much like a subroutine call. If macrostore emulation is not present, an interrupt is asserted allowing either for emulation of the function or instruction in main memory or handling the non-standard opcode as an opcode violation.

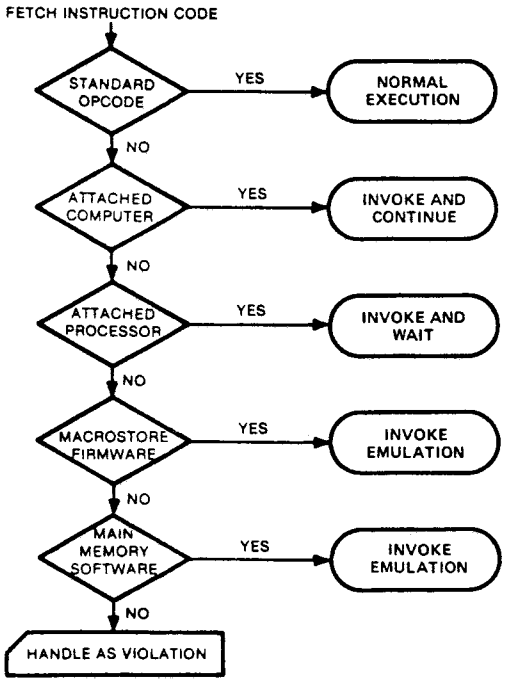
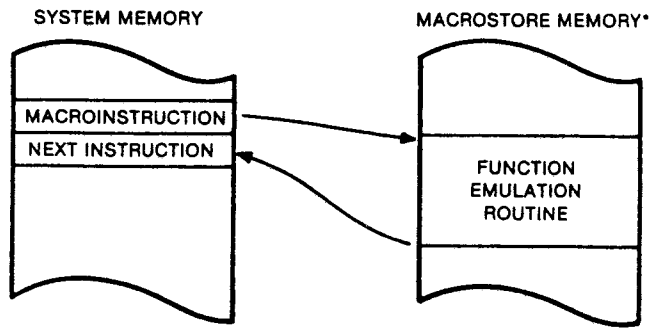


FIGURE 5 – STRUCTURED CONTROL FLOW

The TMS 99000 family of CPU's performs this control flow with no impact to instruction execution performance. All control decisions are performed during the normal instruction decode time.

Macrostore

As previously discussed, macrostore is a logically separate memory address space, which provides for emulation of added functions and instructions. Consisting of 64K bytes, macrostore enables the system designer to tailor system functionally to specific system requirements. New functions and instructions are implemented in normal TMS 99000 machine codes for ease of implementation and efficient use of memory. Figure 6 illustrates how macrostore emulation occurs in the logically distinct address space. During the decision process previously discussed, control is transferred to provide instruction fetch and execute cycles out of the macrostore memory space. The emulation routine, implemented with standard TMS 99000 instructions, is exited in a manner similar to a return from subroutine. Execution is continued out of main memory at the location specified by the program counter.



* A LOGICALLY DISTINCT MEMORY SPACE

FIGURE 6 – EMULATION IN MACROSTORE

Of the 64K byte macrostore logical address spaces, the first 4K bytes are reserved for on-chip integration of macrostore memory. All TMS 99000 processors contain 32 bytes of macrostore RAM on-chip. The TMS 99110 and TMS 99120 processors contain an additional 1K bytes of macrostore ROM. In the TMS 99110, this ROM contains emulation routines for single precision floating point instructions. In the TMS 99120, this ROM contains run-time support for the PASCAL high-level language. The remaining 60K address space allows off-chip expansion as shown in the address map of Figure 7.

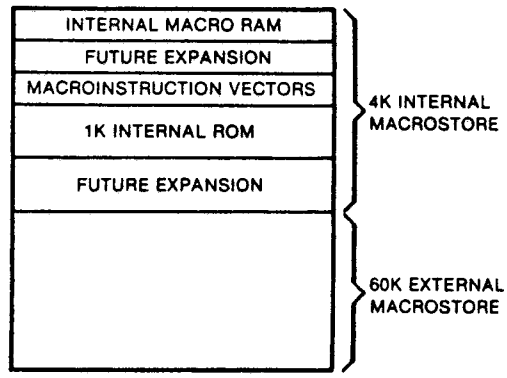


FIGURE 7 – MACROSTORE ADDRESS SPACE

Macrostore functions and instructions are powerful tools for system designers. To the system user, the implementation of instructions or functions in processor microcode or in macrostore emulation is virtually indistinguishable. To the system software designer, macrostore implemented instructions require no special conventions as they may be coded exactly as a subroutine. However, because this "subroutine" resides in a separate logical address space, the funciton is transparent and not subject to modification by the system user. The viewpoints perceived by both the system designer and system user are illustrated in Figure 8.

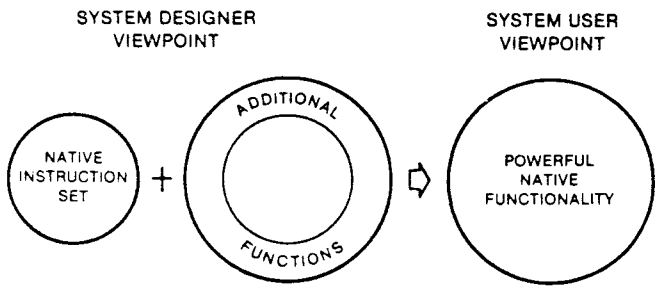


FIGURE 8 – MACROSTORE VIEWPOINTS

Attached Processors and Computers

The next step in functional migration is the migration of the function to a dedicated processor or computer. The distinction between attached computer and attached processor is the manner in which the host TMS 99000 reacts after invocation of a process in the attached element. Attached processors essentially replace in-line execution of code by the host TMS 99000 and, as such, halt the host until function execution is complete. Thus the environment is sequential in nature.

Attached computers, on the other hand, usually have the facilities of a private memory system thus allowing them to release the host TMS 99000 after function invocation. This means concurrent execution of the attached computer with the host TMS 99000. Once the task of the attached computer is complete the attached computer signals the host TMS 99000 completion through an interrupt, DMA or the attached processor interface. Both attached computers and attached processors utilize a common interface with a TMS 99000 family processor as shown in Figure 9.

The ability to configure an attached hardware processor element to operate concurrently or sequentially provides the means to configure the system that best meets the system and function requirements. Some functions are best implemented in a sequential manner such as floating point processors. Some functions, such as communications channel controllers, are more efficiently implemented as concurrent processes.

The invocation stage for attached processors as well as attached computers provides for a full transfer of the TMS 99000 state vector to the attached processor or computer. The exchange of only three internal TMS 99000 registers makes this capability possible. In conventional register-based machines, the overhead of transferring the internal register set of the host processor would have a serious performance impact. The transfer of the entire state vector is critical to maintaining system integrity of both concurrent and sequential processes.

- MEMORY BUS
- ATTACHED PROCESSOR PRESENT (APP)
- BUS STATUS CODES

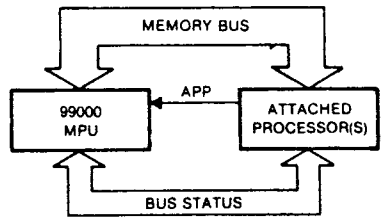


FIGURE 9 – ATTACHED PROCESSOR/COMPUTER INTERFACE

The TMS 99000 microprocessor family provides a structured path for system upgrades and cost reductions. A range of cost and performance options can be considered while maintaining the same level of functionality. As an example of this, consider the implementation of a floating point instruction set. At the first level of implementation, this could be an emulation routine in main memory entered through a system level interrupt when the floating point opcodes are fetched and decoded. The second level is the migration of floating point instruction emulation to macrostore, on or off-chip. This was done on the TMS 99110 floating point microprocessor. A floating point attached processor provides the best performance (with specialized hardware) for floating point instructions. During such a migration scenario no modification to user software need to be made as the floating point opcodes would remain the same. To the system user, the floating point instruction set would appear identical, regardless of the method of implementation.

MEMORY INTERFACE

Another level of cost/performance efficiency, which has been designed into the TMS 99000 microprocessor family, is the ability to configure a memory system consistent with the overall system cost and performance goals. This is a result of an efficient memory interface, which allows the use of fast memory for critical functions or slower, less expensive memory for main memory store. Appreciable performance gains through the use of high-speed memory allow cache memory techniques to become a viable option for configuring high performance systems while reducing the overall memory costs.

The memory cycle time of the TMS 99000 microprocessor can be as fast as 167 nanoseconds with a minimum memory access time of approximately 60 nanoseconds. For slower memories any number of additional memory cycles may be inserted. The result of this memory cycle time is that overall memory bus bandwidth is increased.

Another element contributing to memory interface efficiency is an intelligent instruction prefetch mechanism, which practically eliminates "dead" cycles on the memory bus. Thus internal, or ALU cycles, are performed concurrently with memory bus activity. This prefetch method illustrated in Figure 10, is termed intelligent because the actual program counter location is fetched for branch and jump instructions but not necessarily the next sequential location. The prefetch queue is one instruction deep to eliminate complex queue management, which adversely impacts performance.

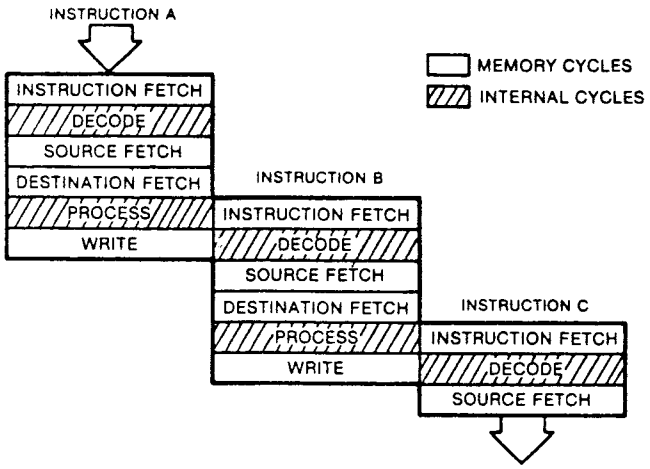


FIGURE 10 – INTELLIGENT INSTRUCTION PREFETCH

TMS 99000 MEMORY SYSTEMS

The ability of the TMS 99000 family of microprocessors to access memory at very fast cycle times provides the system designer wide latitude in configuring the memory subsystem to support cost/performance goals of the entire system. Because memory costs are predominant in most systems, this capability is essential in meeting design goals.

The result of this efficient interface is that TMS 99000 systems support hierarchial memory systems. Figure 11 illustrates the structure of this memory hierarchy. This hierarchy supports a large variation in processor to backing-store mass storage transfer capabilities. In addition, this hierarchy provides growth in memory address reach, supporting memory systems ranging from less than 64K bytes up to 16M bytes of memory.

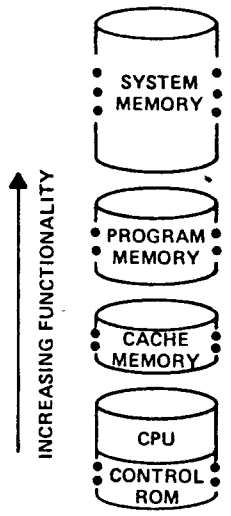


FIGURE 11 – MEMORY HIERARCHY

The TMS 99000 family provides for cost effective growth in physical main memory size through functional segmentation, paging, and use of memory mappers. By use of the status bit output pin, up to 128K bytes of physical memory may be addressed in both the main memory and macrostore memory space for a total of 256K bytes of physical memory. Additional physical memory may be addressed through use of the bus status code outputs to select either a code segment or a data segment, each segment being 64K bytes. These segments may also be paged with the status bit output to provide 128K bytes of physical memory within each segment. Figure 12 illustrates the manner in which large physical addresses may be accessed by the TMS 99000 processor. Note that through the addressing methodologies just discussed, the TMS 99000 family microprocessors can address up to 384K bytes of physical memory.

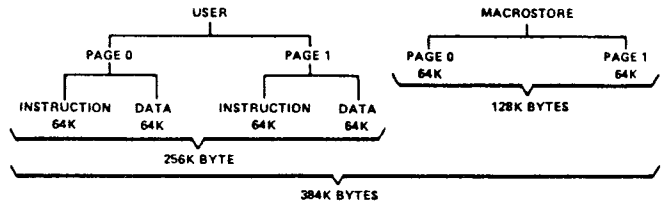


FIGURE 12 –TMS 99000 EXTENDED ADDRESSING

For systems requiring up to 16M bytes of physical memory, a TIM 99610 memory mapper may be used. The TIM 99610 memory mapper provides sixteen, 12-bit mapping registers which expand the TMS 99000 processors four highest order address lines to twelve. This provides a mapping resolution of 4K byte map boundaries for maximum flexibility. Figure 13 illustrates a TMS 99000 microprocessor system utilizing a TIM 99610 memory mapper in a 16M byte memory system.

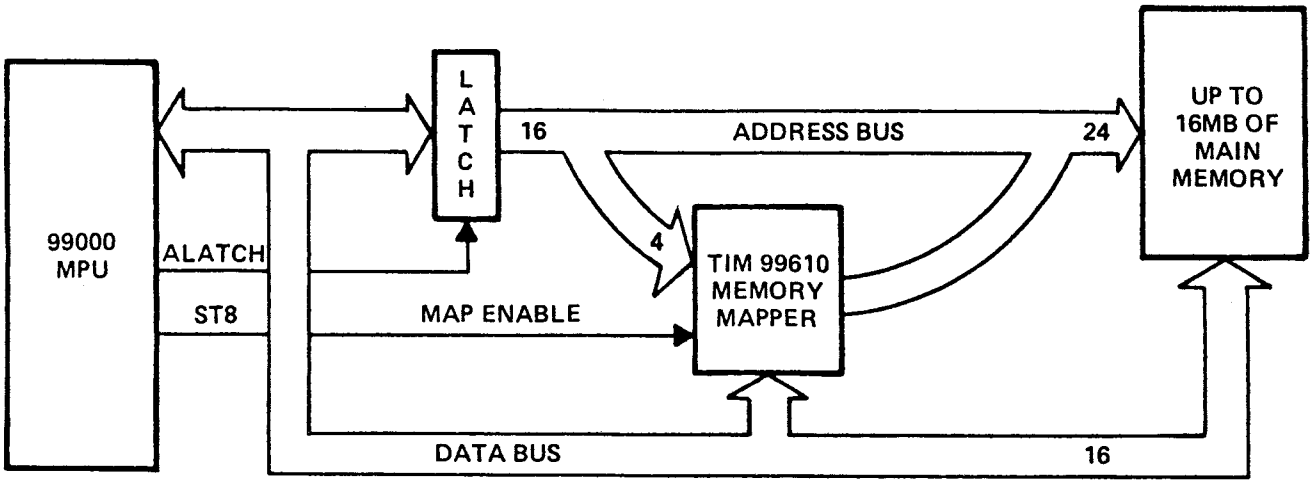


FIGURE 13 – 16M BYTE MEMORY INTERFACE USING A TIM 99610 MEMORY MAPPER

Because time spent in memory transfers is the major factor affecting system performance, it is desirable to achieve the fastest memory cycle time possible. In large memory systems, it is often inconsistent with system cost goals to populate large amounts of high-speed memory. With the TMS 99000 it is not necessary to utilize all high-speed memory to obtain the performance goals. Typically 80 per cent of an application's processing time is spent in 20 per cent of the code. Through use of cache memory and functional partitioning of code segments, a performance advantage is obtained at the established system cost goal. When cacheing or partitioning techniques are utilized, an effective memory cycle time which falls between the cycle time of the high speed and slow speed memory is obtained. Figure 14 illustrates a bar graph of effective memory cycle times for the TMS 99000 with a main memory cycle time of 333 nanoseconds and TMS 99000 effective cycle times utilizing zero wait-state cache with hit ratios of .9 and .6 respectively. For comparison, the zero wait-state memory cycle times are provided for the Motorola 68000 and the Intel 8086-10 microprocessors. (Note: Hit ratio is the percentage of memory cycles which occur in the cache or high-speed memory.) An illustration of a TMS 99000 system with a cache memory system is shown in Figure 15.

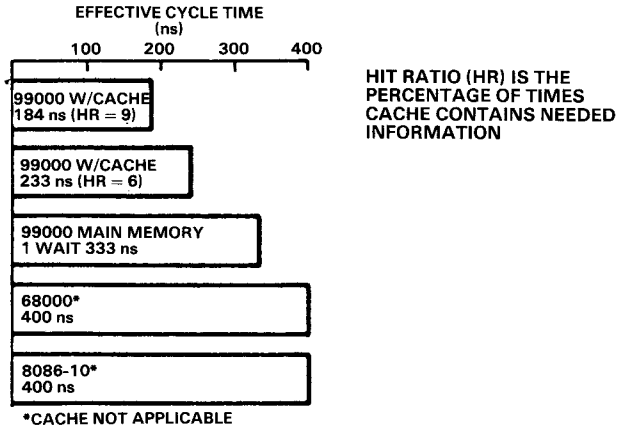


FIGURE 14 – EFFECTIVE MEMORY CYCLE TIME COMPARISONS

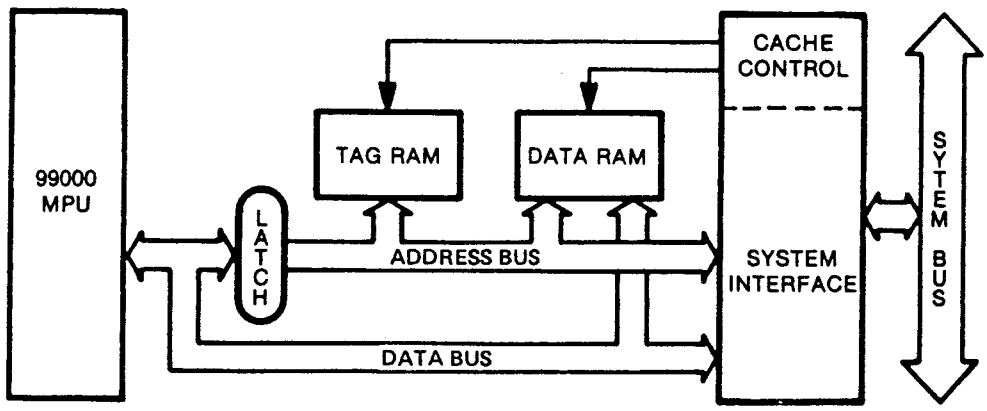


FIGURE 15 – CACHE MEMORY SYSTEM

TMS 99000 PERFORMANCE

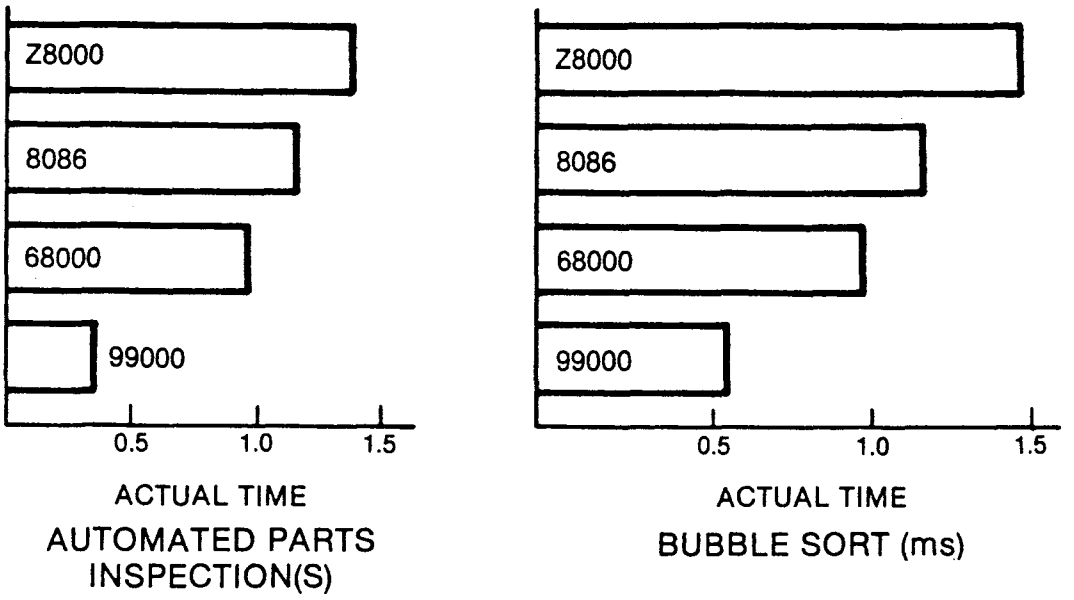
The performance of a microprocessor is a function of the memory cycle time and the memory cycle efficiency. Memory cycle efficiency is a result of accomplishing a given function in the least number of memory accesses. This can be thought of as the information content of each memory access. Because memory cycle times dominate the instruction execution time, the processor that performs a function in the least number of machine states will invariably have the performance advantage. This is especially true when memory cycle times are equal. Thus, as technology improves all microprocessors will lean toward an ultimate in memory cycle times, (in the sub 100 nanosecond range). The processor designed to reduce the number of memory accesses, and thus the number of machine states, will show superior performance. Table 1 contains a comparative listing of common instructions and the number of states required to execute the instruction. The TMS 99000 family of microprocessors is shown as well as state counts and instruction times for the Motorola 68000-8, the Intel 8086-8, and the Zilog Z8000. The results outlined in boxes exhibited the fastest execution time. Note that the TMS 99000 had the highest execution speed for six of the eight instruction statements. A closer examination shows that the TMS 99000 requires fewer machine states for those same instructions.

As a result of reduced state counts and fast machine state time the TMS 99000 exhibits superior performance when compared with competitive processors. The benchmark chosen was found in the Intel Benchmark Report #AFN01551A. The result of including the TMS 99000 in these benchmarks is shown in Figure 16. For all cases the TMS 99000 family processor exhibited superior performance for both zero-and one-wait states. The one-wait state times are given for the TMS 99000 to allow comparison on an equal memory cycle time basis with the MC68000.

TABLE 1 – COMPARATIVE INSTRUCTION EXECUTION

PROCESSOR	99000 STATE TIME = 166		68000-8 STATE TIME = 250		8086-8 STATE TIME = 125		Z-8001 STATE TIME = 250	
	STATES	REAL TIME	STATES	REAL TIME	STATES	REAL TIME	STATES	REAL TIME
MOV (R, R)	3	(500)	2	(500)	2	(250)	3	(750)
MOV (SYM, SYM)	5	(833)	10	(2500)	29	(3625)	20	(5000)
MOV (*R+, *R+)	9	(1500)	6	(1500)	18	(2250)	20	(5000)
ADD (R, R)	4	(667)	2	(500)	3	(375)	4	(1000)
ADD (SYM, R)	5	(833)	6	(1500)	15	(1875)	9	(2250)
JUMP (REL)	3	(500)	5	(1250)	16	(2000)	6	(1500)
MPYS (R, R)	25	(4167)	35	(8750)	128	(16000)	70	(17500)
DIVS (R, R)	34	(5667)	79	(19750)	165	(20625)	95	(23750)

*BENCHMARK FROM INTEL (*AFN015328)



*BENCHMARK FROM INTEL (*AFN015328)

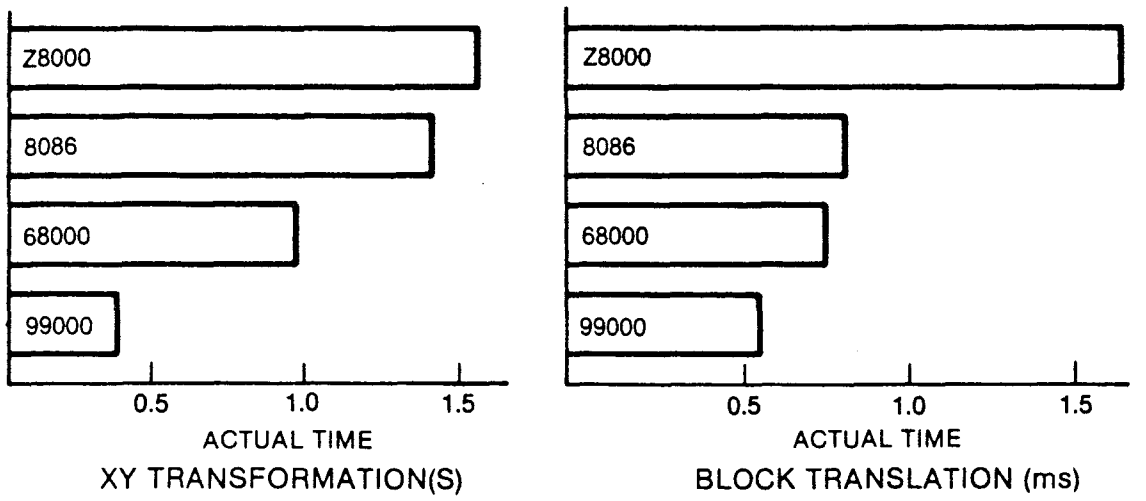


FIGURE 16 – TMS 99000 BENCHMARKS

THE TMS 99000 FAMILY OF ADVANCED 16-BIT MICROPROCESSORS

In addition to sharing an advanced memory-to-memory architecture, each member of the TMS 99000 family of microprocessors shares the same base instruction set as well as memory, I/O, interrupt and DMA interface. Each TMS 99000 is distinguished by instruction set enhancements, which are implemented through customized programming of the on-chip macrostore emulation memory.

Instruction Set

The instruction set is a superset of the proven TMS 9900 microprocessor and consists of 85 instructions as shown in Table 2. Complete object code compatibility has been maintained with the TMS 9900 providing an existing and proven software base for the TMS 99000 family. Enhancements to the base TMS 9900 instructions set are the addition of double precision arithmetic, double precision shifts, signed integer multiply and divide, memory bit test, and stack instructions supporting recursive program environments. Additionally, the TMS 99110 floating point and the TMS 99120 PASCAL kernal processor contain additional instructions, which are a result of macrostore and microcode programmations. These include the external memory mapper control instructions. The memory mapper control instructions are designed to facilitate control of a TIM 9961O memory mapper circuit, allowing memory expansion up to 16M bytes. (See Figure 12).

MNEMONIC	DESCRIPTION	MNEMONIC	DESCRIPTION
A	Add Word (16-bit)	LWPI	Load Workspace Pointer Immediate
AB	Add Byte (8-bit)	MOV	Move Word
ABS	Absolute Value	MOVB	Move Byte
AI	Add Immediate	MPY	Multiply
AM	Add Multiple (32-bit)	MPYS	Signed Multiply
ANDI	AND Immediate	NEG	Negate
B	Branch	ORI	OR Immediate
BIND	Branch Indirect	RSET	External Reset
BL	Branch and Link	RTWP	Return to Workspace Pointer
BLWP	Branch and Load Workspace Pointer	S	Subtract (16-bit)
BLSK	Branch Immediate and Push Link to Stack	SB	Subtract Byte (8-bit)
C	Compare Word	SBO	Set Bit to One (I/O)
CB	Compare Byte	SBZ	Set Bit to Zero (I/O)
CI	Compare Immediate	SETO	Set Word to Ones
CKOF	External Clock Off	SLA	Shift Left Arithmetic
CKON	External Clock On	SLAM	Shift Left Arithmetic Multiple (32-bit)
CLR	Clear Word	SM	Subtract Multiple (32-bit)
COC	Compare Ones Corresponding	SRA	Shift Right Arithmetic
CZC	Compare Zeros Corresponding	SRAM	Shift Right Arithmetic Multiple (32-bit)
DEC	Decrement	SRC	Shift Right with Carry
DECT	Decrement by Two	SRL	Shift Right Logical
DIV	Divide	SOC	Set Ones Corresponding Word
DIVS	Signed Divide	SOCB	Set Ones Corresponding Byte
IDLE	Idle Processor	STCR	Store Communications Register Unit (I/O)
INC	Increment	STST	Store Status
INCT	Increment by Two	STWP	Store Workspace Pointer
INV	Invert	SWPB	Swap Bytes
JXX	Jump (1-unconditional, 12-conditional)	SZC	Set Zeroes Corresponding Word
LDD*	Long Distance Destination (Memory Mapper Control)	SZCB	Set Zeroes Corresponding Byte
LDCR	Load Communications Register Unit (I/O)	TB	Test Bit (I/O)
LDS*	Long Distance Source (Memory Mapper Control)	TCMB	Test and Clear Memory Bit
LI	Load Workspace Register Immediate	TMB	Test Memory Bit
LIMI	Load Interrupt Mask Immediate	TSMB	Test and Set Memory Bit
LMF*	Load Map File (Memory Mapper Control)	X	Execute
LREX	Load External	XOP	Extended Operation (software context switch)
LST	Load Status Register	XOR	Exclusive-OR
LWP	Load Workspace Pointer		

*These instructions implemented on TMS 99110 and TMS 99120 only.
NOTE: Floating Point (TMS 99110) and Rx instructions (TMS 99120) are not listed.

Memory Interface

The TMS 99000 memory interface consists of a multiplexed address and data bus, and a control bus for controlling transfers to and from memory. The bus bandwidth of the memory interface accounts for the superior performance of the TMS 99000.

I/O Interface

Both bit, byte, and word input/output transfers may be performed by the TMS 99000 processor. The interface shares many of the same pins as the memory interface, e.g., the address and data bus. Input/output transfers are similar to memory transfers in that the bit, byte, or word address is output on the address bus. Whether a transfer is a bit, byte, or word is determined by the I/O address specified in the instruction. Figure 17 illustrates the partitioning of I/O addresses between bit serial and byte/word parallel transfers. Note that the first 16K addresses are for bit transfers and the last 16K addresses are for byte/word parallel transfers. Byte/word selection is accomplished at instruction coding. The transfer rate is 1.7M bits, bytes, or words per second providing very fast I/O transfers. Wait-states may be inserted to match transfer rate to the capabilities of the I/O device.

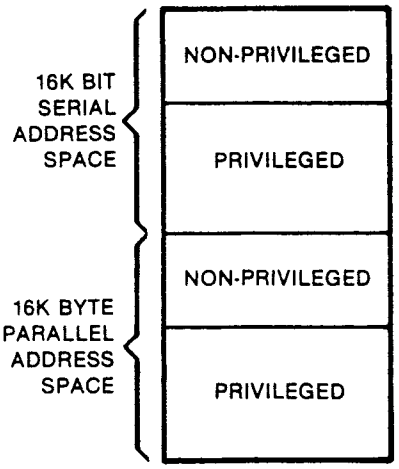


FIGURE 17 – I/O ADDRESS MAP

Interrupt Structure

The TMS 99000 family of microprocessors offer 16 levels of vectored, prioritized interrupts. With advanced memory-to-memory architecture, interrupt context switches are fast and efficient, since a context switch only involves a fetch and store of the workspace pointer, status register, and program counter to redefine the state vector.

Interrupt levels are numbered from level 0 to level 15 with level 0 (RESET) assigned highest priority and level 15 the lowest. Table 3 lists the interrupt levels and their function. Note that level 2 is used for system level interrupts: illegal instruction, privilege violation, and arithmetic fault.

TABLE 3 – INTERRUPT LEVELS

PRIORITY LEVEL	SOURCE AND ASSIGNMENT
LEVEL 0 (HIGHEST PRIORITY)	EXTERNAL : RESET SIGNAL
NMI	NON-MASKABLE INTERRUPT : USER DEFINED
LEVEL 1	EXTERNAL : USER DEFINED
LEVEL 2	INTERNAL : ILLEGAL INSTRUCTION
	INTERNAL : PRIVILEGE VIOLATION
	INTERNAL : ARITHMETIC FAULT
	EXTERNAL : USER DEFINED
LEVEL 3 I LEVEL 15	EXTERNAL : USER DEFINED

The illegal instruction interrupt occurs if an undefined opcode is fetched and decoded and the opcode is not used in an attached processor/computer or macrostore. This interrupt level allows emulation in system memory of instructions which will later be performed by an attached processor/computer or emulated in macrostore. This facilitates transportability of software among system configurations.

The privileged interrupt occurs if execution is attempted of a privileged instruction when the processor is not in the privileged mode. The privileged mode is determined by a bit in the status register. The privileged instructions include input/output instructions and instructions that modify the program environment such as the load status register instruction. Table 4 lists those instructions that are privileged. The privileged interrupt supports user/supervisor environments and implementation of system protection mechanisms.

TABLE 4 – PRIVILEGED INSTRUCTIONS

MNEMONIC	DESCRIPTION
CKON	External Clock On
CKOFF	External Clock Off
IDLE	Processor Idle
LIMI	Load Interrupt Mask Immediate
LREX	Load External
RSET	External Reset
LDCR	Load Communications Register Unit
SBO	Set Bit to One
SBZ	Set Bit to Zero
LMF	Load Map File
LDD	Long Distance Destination
LDS	Long Distance Source

The arithmetic fault interrupt occurs as a result of an arithmetic overflow condition during the execution of arithmetic instructions. This interrupt is enabled/disabled through a bit in the status register. The interrupt context switch occurs immediately following the instruction that caused the overflow without the necessity of using "trap on overflow" type instructions. This provides for a completely automatic interrupt, enhancing execution speed for routines that detect the overflow condition.

SUMMARY

The TMS 99000 microprocessor family provides a true system solution for advanced applications of microprocessors. The TMS 99000 microprocessor family is the only microprocessor family that allows the system designer to design native functionality into his system. It is the only system which supports a path of cost/performance migration with the capability of maintaining system functionality. These options in cost and performance are illustrated in Figure 18. Note that options include both function migration and memory system options to provide the most cost-effective system design. The further integration of functions from memory system software to true silicon solutions has taken the first step with the TMS 99000 microprocessor family. Texas Instruments continues the evolution of functional integration through advanced peripherals and processors to provide leadership in microprocessor products for the '80s.

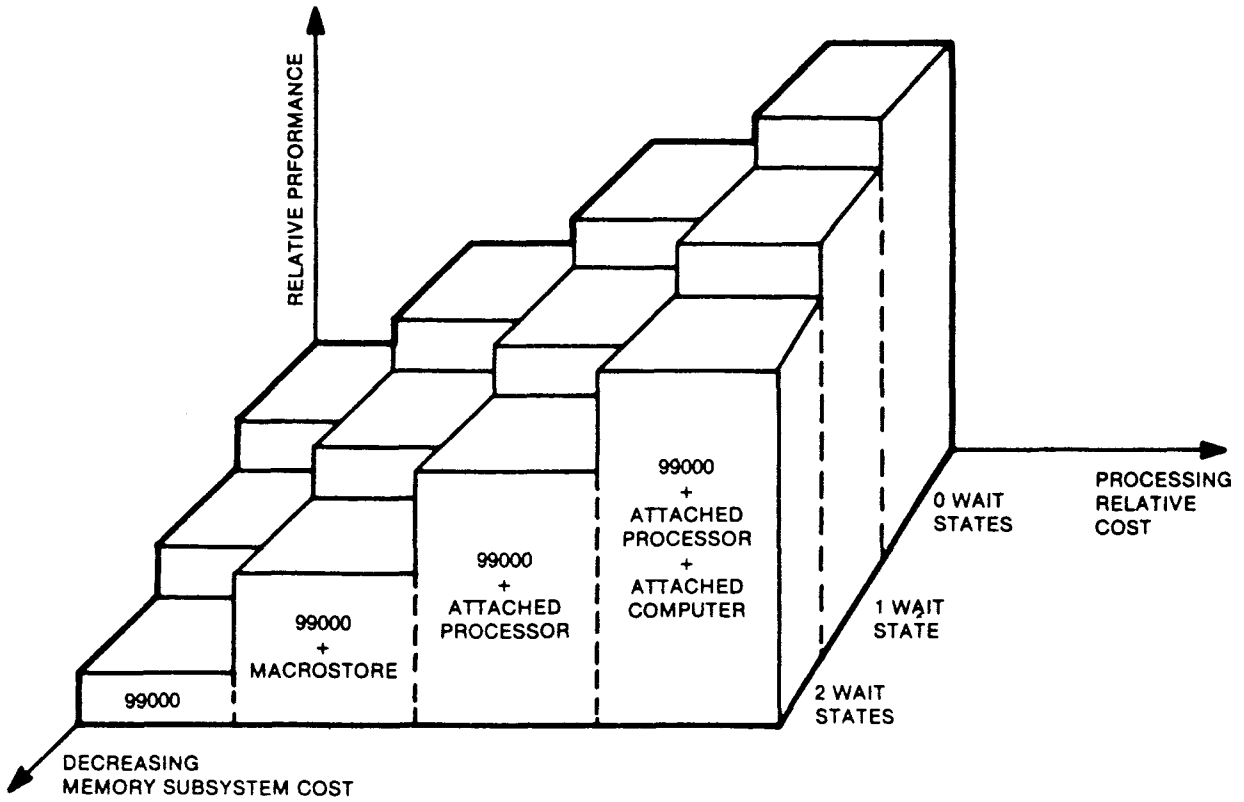


FIGURE 18 – TMS 99000 COST/PERFORMANCE OPTIONS

TMS 99000 BENCHMARK REPORT

PACING COMPETITIVE PROCESSORS

INTRODUCTION

Using the expertise acquired through two generations of building 16-bit processors, Texas Instruments has combined their past successes with the newest and most innovative techniques of today. The result is the TMS 99000, a 16-bit processor family that provides memory cost alternatives, software adaptability, programming ease, cost performance options, and speed.

PROCESSOR DESCRIPTION

This new third-generation microprocessor family builds upon the unique memory-to-memory architecture that was pioneered at Texas Instruments. The TMS 99000 provides an enriched superset of the TMS 9995 instructions. The architecture allows for single cycle memory accesses, (see Figure 1) attached processor and computer interfacing as well as performance upgrades ranging from 5 to 12 times that of the TMS 9900, and twice that of the TMS 9995. Now members of the family can implement software functions in an on-chip memory space known as macrostore, thus providing even further cost/performance options.

TI's product-evolution to a memory-based machine has decreased the use of random logic, trading in its place, dense memory cells. With the technological advances being made in memory speeds, the advantages of memory-to-memory architecture have become increasingly clear. First, since the registers are based in memory, there is a reduction of the overhead involved in transferring data in and out of the typical register. This results in an effective reduction in the number of memory bytes required. There is also a further reduction in the number of instructions required to accomplish a given task. The result is that the execution time of programs is greatly reduced. The following table shows a comparison of arithmetic instructions that are particularly important to industrial control applications (see Table 1).

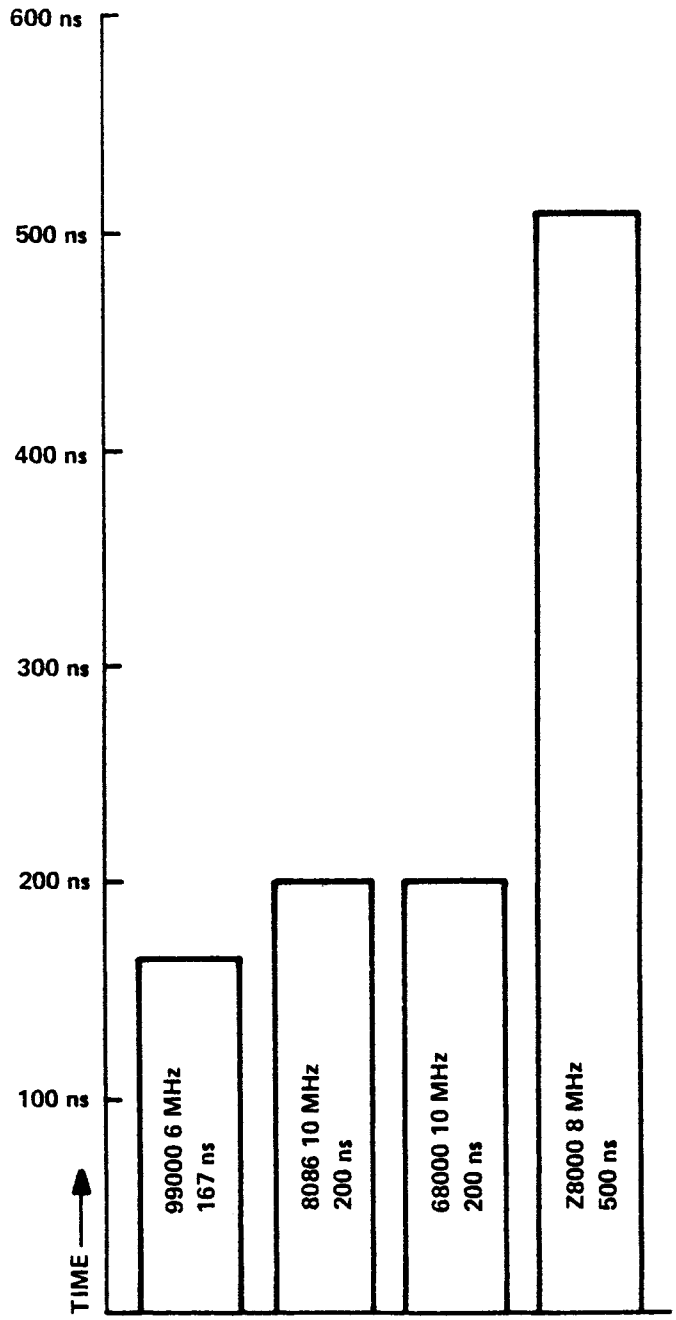
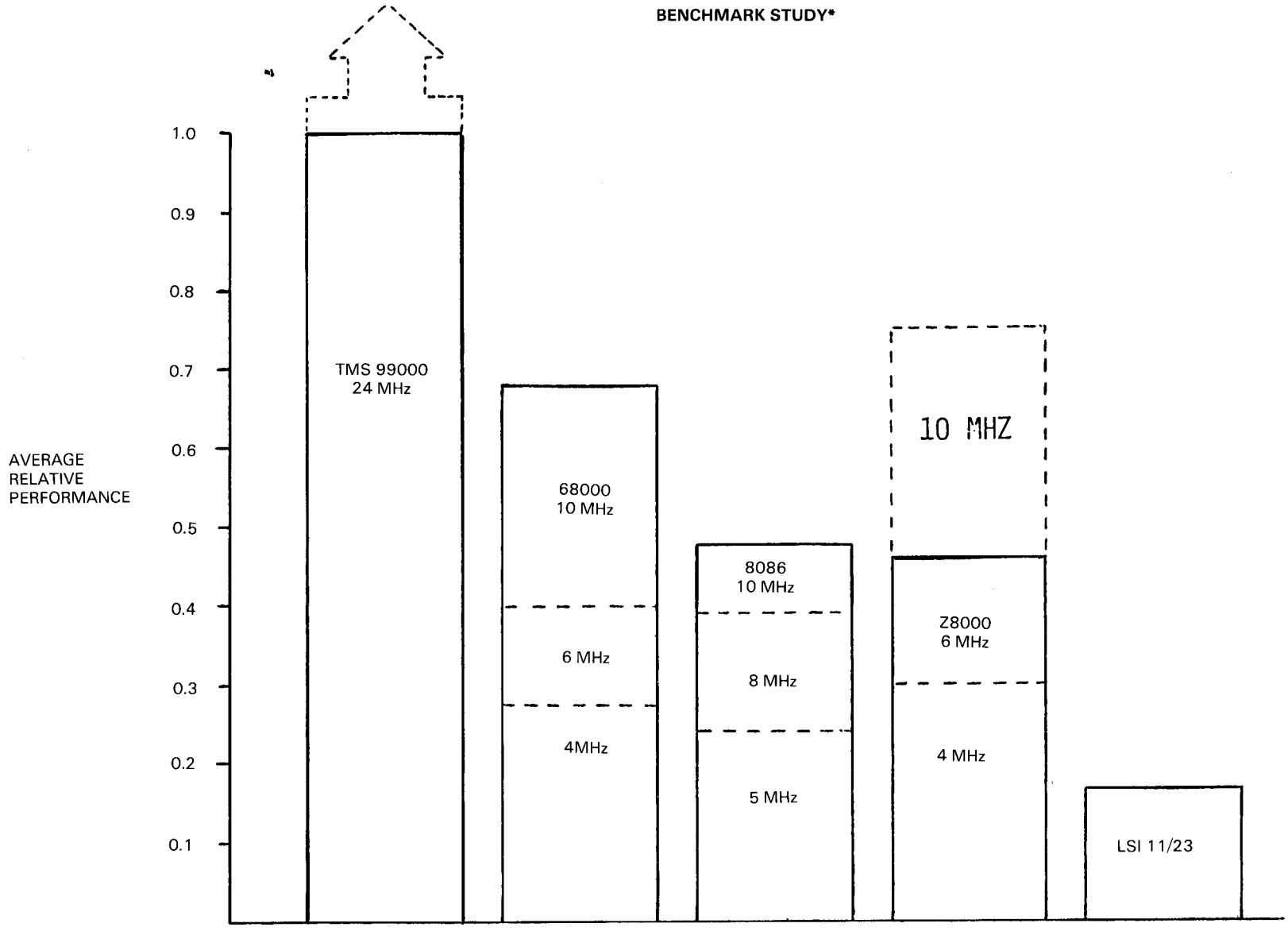


FIGURE 1 – MINIMUM MEMORY CYCLE TIME

BENCHMARK STUDY*



*Normalized average of (1) Intel Benchmark AFN01532A, (2) Digital Filtering application by V. P. Nelson and H. T. Nagel, Jr., and (3) Carnegie-Mellon University Benchmarks.

TABLE 1 – INDUSTRIAL CONTROL CAPABILITIES (μS)

	ADD(SYM,R)	MULS(R,R)	DIVS(R,R)	INTRP/RESP
99000 6 MHz	.83	4.16	5.66	2.16
68000 10 MHz	1.20	7.00	15.80	4.70
8086 10 MHz	2.10	15.40	18.40	6.1
Z8000 8 MHz	1.10	8.75	11.90	N/A

NOTE: Worst case times are given for muls and divs

BENCHMARK DESCRIPTION

This report shows how the 99000 compares with today's advanced 16-bit processors, using independent studies as well as the manufacturer's own yardsticks. The results clearly show the TMS99000 pacing competitive processors (see Figure 2).

At the heart of the 99000 family's performance is unprecedented raw speed. Three sets of benchmarks are used to document this speed.

The first set of programs was generated by a group at Carnegia-Mellon University. In April of 1981 they were featured in an EDN article, "A Tale of Four Microprocessors: Benchmarks Quantify Performance." This particular set of programs is extremely effective in isolating the types of tasks that a user would normally encounter in a typical application environment. Thus it is easy to evaluate a selected processor for a specific application environment.

The second set of programs was taken from Intel's Benchmark AFN01532A. This set attempts to create programs that combine and demonstrate as many of the capabilities of the processor as possible.

Finally a third, independent set of programs was used to show the effectiveness of each processor in a specific application. These programs were created by V.P. Nelson and H.T. Nagle Jr. at Auburn University. This specific application involves digital filtering.

Tables 2 – 7 summarize the results of this study.

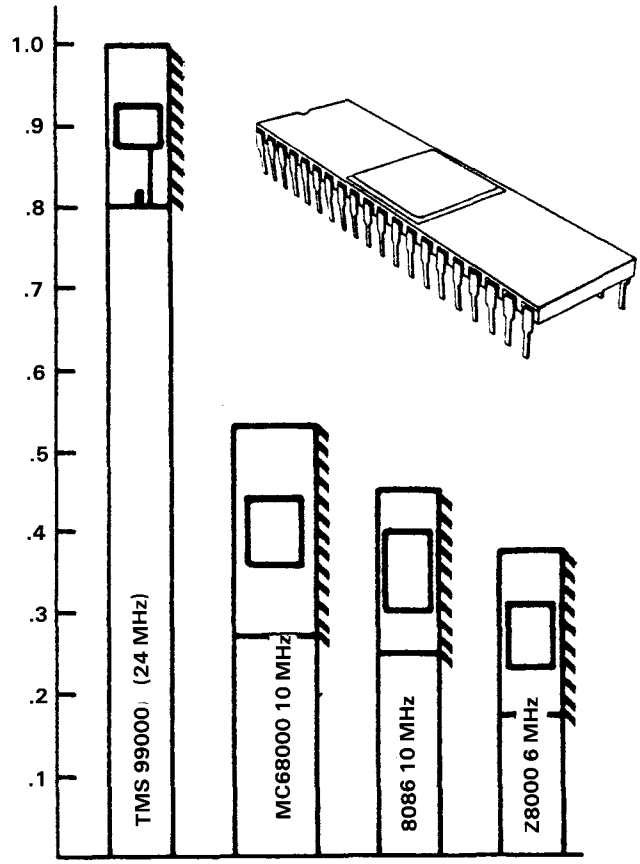


FIGURE 2 – NORMALIZED EXECUTION FOR INTEL BENCHMARK AFN01532A

TABLE 2 – INTELBENCHMARK AFN01532A
Actual Exection Time

BENCHMARK PROGRAM	TMS99000 (24 MHz)	MC68000 (10 MHz)	8086 (10 MHz)	Z8000 (6 MHz)
AUTOMATED PARTS INSPECTION (s)	0.26	0.56	0.67	0.70
BLOCK TRANSLATION (ms)	0.65	0.70	0.74	1.26
BUBBLE SORT (ms)	0.42	0.78	0.91	0.96
COMPUTER GRAPHICS (s)	0.38	0.78	1.12	1.06
RE-ENTRANT PROCEDURE (μs)	7.9	45.20	31.20	46.50

TABLE 3 – INTEL BENCHMARK AFN01532A
Normalized Performance

BENCHMARK PROGRAM	TMS99000 (24 MHz)	MC68000 (10 MHz)	8086 (10 MHz)	Z8000 (6 MHz)
AUTOMATED PARTS INSPECTION (s)	1	.47	.39	.37
BLOCK TRANSLATION	1	.91	.88	.51
BUBBLE SORT	1	.54	.46	.44
COMPUTER GRAPHICS	1	.48	.33	.36
RE-ENTRANT PROCEDURE	1	.17	.25	.17
NORMALIZED AVERAGE	1	.39	.45	.37

TABLE 4 – DIGITAL FILTERING APPLICATION[1]
Actual Execution Time

BENCHMARK PROGRAM (μs)	TMS99000 (24 MHz)	MC68000 (10 MHz)	8086 (10 MHz)	Z8000 (6 MHz)
FILTER (1 LOOP)	12.78	19.80	26.60	20.50
INPUT (NO DELAY)	5.30	8.20	7.40	10.33
OUTPUT (1 DELAY)	41.20	52.40	87.20	84.88
TIME DELAY	12.28	25.60	16.40	20.18
PREPROCESSOR (1 DELAY)	114.04	155.20	291.20	253.63
TOTAL SAMPLE TIME	185.60	261.60	428.80	389.52
TIME LAG FROM INPUT TO OUTPUT	51.29	82.25	133.00	104.23

[1]V.P. Nelson and H.T. Nagel Jr.

TABLE 5 – DIGITAL FILTERING APPLICATION[1]
Normalized Performance

BENCHMARK PROGRAM	TMS99000 (24 MHz)	MC68000 (10 MHz)	8086 (10 MHz)	Z8000 (6 MHz)
FILTER (1 LOOP)	1	.65	.48	.62
INPUT (NO DELAY)	1	.65	.72	.51
OUTPUT (1 DELAY)	1	.79	.47	.49
TIME DELAY	1	.48	.75	.61
PREPROCESSOR (1 DELAY)	1	.73	.39	.45
TOTAL SAMPLE TIME	1	.71	.43	.48
TIME LAG FROM INPUT TO OUTPUT	1	.62	.39	.49

[1]V.P. Nelson and H.T. Nagle Jr.

TABLE 6 – CARNEGIE-MELLON UNIVERSITY
Actual Execution Times (μs)

BENCHMARK PROGRAM	99000 (24 MHz)	68000 (10 MHz)	8086 (10 MHz)	Z8000 (6 MHz)	11/23
I/O INTERRUPT (1)	6.7	33	126	42	141
FIFO INTERRUPT (2)	158.5	390	348	436	1196
STRING SEARCH (3)	302.8	244	193	237	996
BIT MANIPULATION (4)	75.7	70	122	123	799
LINKED LIST (5)	81.5	153	—	237	592
QUICKSORT (6)	46000	33527	115669	115500	—
MATRIX TRANSPOSITION (7)	312.5	368	820	646	1517

TABLE 7 – CARNEGIE-MELLION UNIVERSITY
Normalized Performance

BENCHMARK PROGRAM	99000 (24 MHz)	68000 (10 MHz)	8086 (10 MHz)	Z8000 (6 MHz)	11/23
I/O INTERRUPT (1)	1	.20	.05	.16	.06
FIFO INTERRUPT (2)	1	.41	.46	.36	.13
STRING SEARCH (3)	1	1.24	1.57	1.28	.30
BIT MANIPULATION (4)	1	1.08	.62	.62	.09
LINKED LIST (5)	1	.53	—	.34	.14
QUICKSORT (6)	1	1.37	.40	.40	—
MATRIX TRANSPOSITION (7)	1	.85	.38	.48	.21
NORMALIZED AVERAGE	1	.81	.58	.52	.16

RESULTS

Based on this benchmark study, when all processors were allowed to run at 0 wait states, the TMS99000 proved to average 3.01 times faster than the typical competitor. (See Figure 3.) At the same time, the 99000 required only 83 per cent as much memory space.

OTHER CONSIDERATIONS

Based on these tests the TMS99000 will provide an untouchable level of speed at 0 wait states. By introducing 1 wait state on the TMS99000, the user could significantly reduce the cost of memory, and still remain at a speed that is faster than the competitors, who would still be running at 0 wait states.

The unique design of the 99000 makes it particularly adaptable to a cacheing of memory. By using only a small portion of high-speed memory in cache, with the remainder at 1 wait state, the user could effectively reduce his costs, while running much faster than competitive processors at 0 wait states.

YOUR APPLICATION

The particular timing of your program will vary depending on the concentration of your application in a given type of processing. As mentioned earlier, the Carnegie-Mellon programs are extremely effective in isolating the various types of tasks that you will typically encounter in a normal environment. By comparing your individual task requirements with the table below, (see Table 8) you can determine where your processor will spend its time. Then using the datum provided by this study, you can easily establish your own set of benchmarks, showing which processor is best for your application.

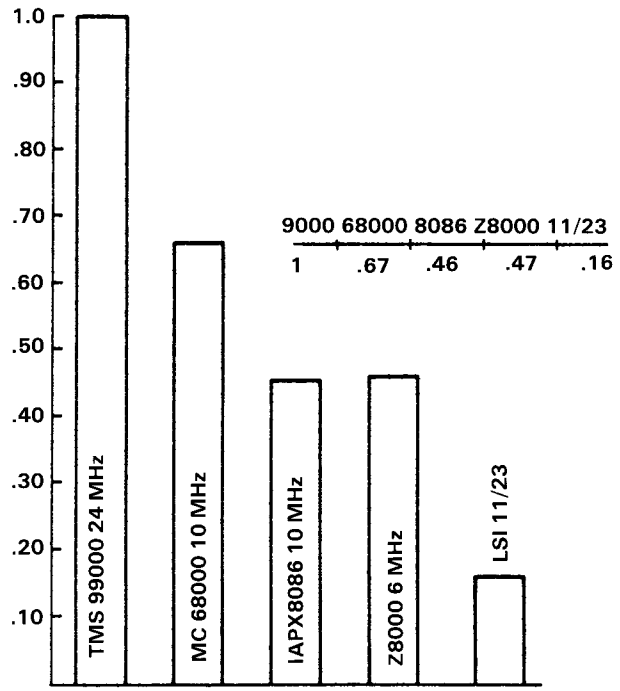


FIGURE 3 – NORMALIZED AVERAGE FOR ALL BENCHMARKS

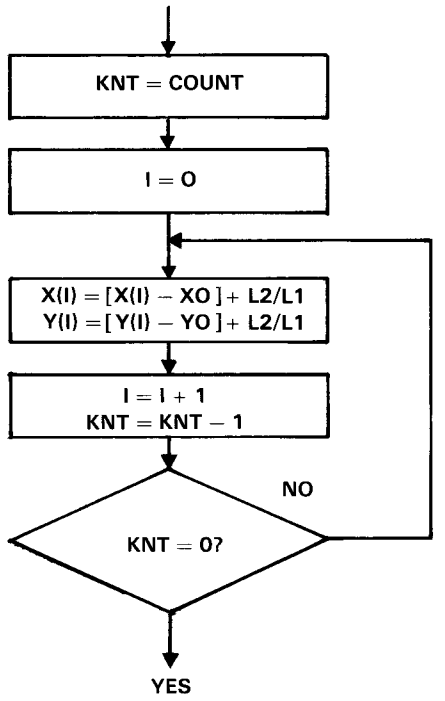
TABLE 8 – CARNEGIE-MELLON BENCHMARKS DESCRIPTION

PROGRAM	PROCESS INVOLVED
1	HANDLING PRIORITIZED INTERRUPTS
¿	QUEUING INTERRUPTS ON A FIFO BASIS
3	WORD PROCESSING – STRING MANIPULATION
4	BIT MANIPULATION
5	DATA BASE MANAGEMENT
6	STACK HANDLING ABILITY
7	ARITHMETIC AND EXTENDED BIT MANIPULATION

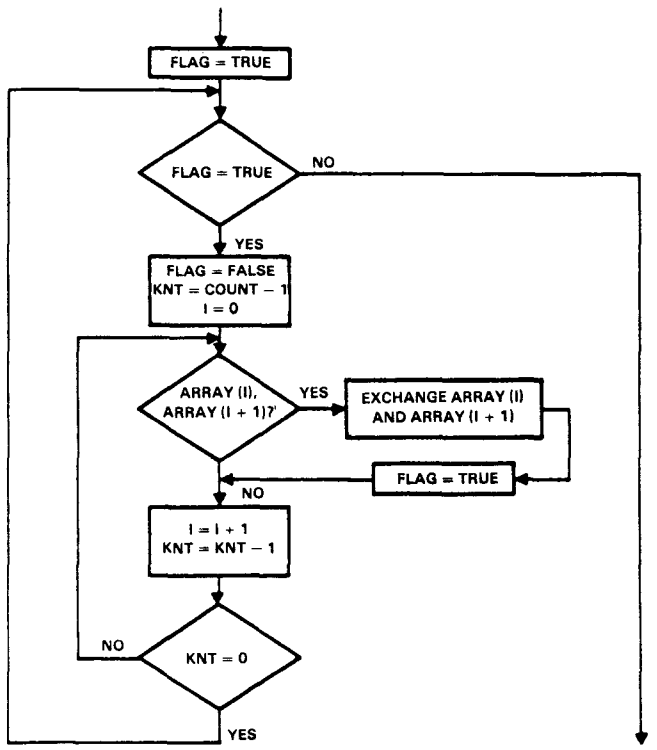
APPENDIX

Listed here are flowcharts selected from Intel Benchmark AFN01532A. A complete listing of flowcharts and actual code for the Carnegie-Mellon Benchmarks appeared in the April 1 issue of EDN, pages 179–265. Further documentation and results can be obtained from your local Texas Instruments sales office.

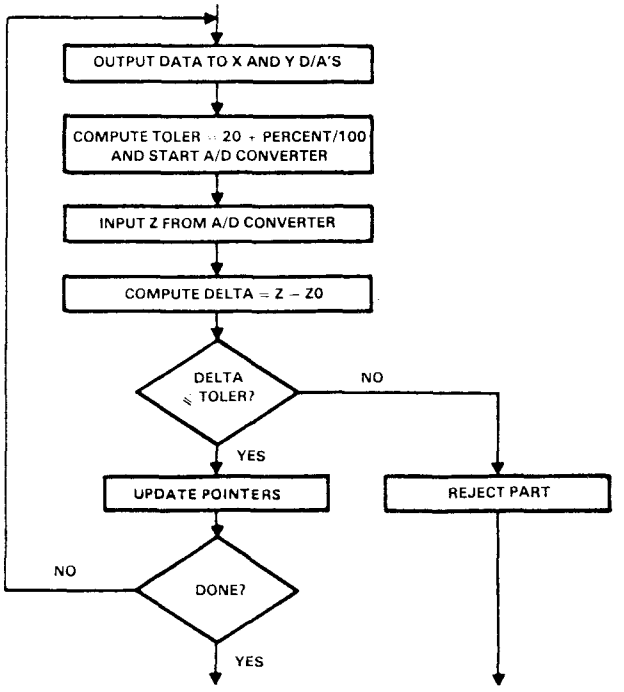
COMPUTER GRAPHICS XY TRANSFORMATION



BUBBLE SORT



AUTOMATED PARTS INSPECTION



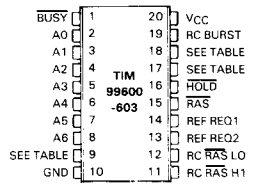
TIM 99600/604/608 SERIES

DYNAMIC RAM REFRESH CONTROLLER CIRCUITS

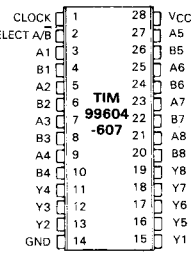
FEATURES:

- Controls 4K/16K/64K dram refresh (600–603).
- Creates static RAM appearance.
- Choice of transparent or cycle steal or burst.
- Refresh violation defection.
- RC programmable for speed and flexibility.
- RAS only refresh.
- 20 pin dip space saver package.
- 16 line to 8 line MUX (604–607).
- 16 D-Type registers.
- Selects data from A bus or B bus.
- 3-state output drives bus lines directly.
- 28 pin dip.
- Provides memory cycle timing (608).
  - Read.
  - Write.
  - Read modify write.
  - RAS only refresh.
  - Page or normal mode.
- Stand alone for microprocessor to memory interface.
- RAS 3-State output share bus with refresh controller.
- Critical times are RC programmable.
- 16 pin dip.

PIN ASSIGNMENTS



300 mil, 20 PIN

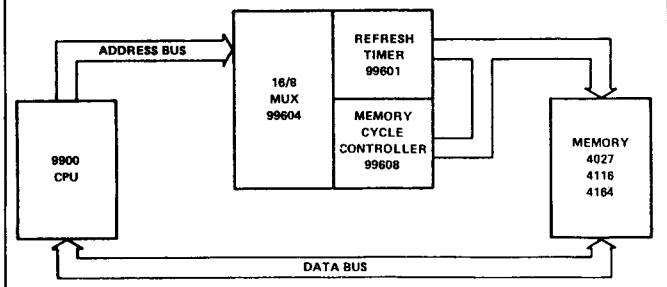


600 mil, 28 PIN

SELECTION TABLE

DEVICE	REFRESH MODES	MEMORY SIZE	PIN ASSIGNMENTS		
			PIN 9	PIN 17	PIN 18
'LS600	Transparent, Burst	4K or 16K	4K/16K	NC	NC
'LS601	Transparent, Burst	64K	A7	NC	NC
'LS602	Cycle Steal, Burst	4K or 16K	4K/16K	READY	RE CYCLE STEAL
'LS603	Cycle Steal, Burst	64K	A7	READY	RC CYCLE STEAL

APPLICATION:



DESCRIPTION:

The 'LS600 thru 'LS603 memory refresh controllers contain one 8-bit synchronous counter, nine 3-state buffer drivers, four RC-controlled multivibrators, and other control circuitry on a monolithic chip. They are intended for use with RAS-only-refresh dynamic RAMs. These controllers have 3-state $\overline{RAS}$ and address outputs that are in the high-impedance state when no refresh is in progress. They become active approximately 30 nanoseconds after the REF REQ pins are taken high and remain active until about 30 nanoseconds after the refresh is complete.

The 'LS608 memory cycle controller is designed to interface between a microprocessor and dynamic RAM memories. It contains six RS latches, five D-type flip-flops, and more than 50 miscellaneous gates on a single chip. The 'LS608 combines maximum flexibility and ease of programming via RC nodes to allow optimum memory cycle performance.

The 'LS608 can operate as a stand-alone interface but is also designed to be part of a three-chip memory controller set. The user must select one of the 'LS600 thru 'LS603 refresh controllers and one of the 'LS604 thru 'LS607 multiplexers to use along with the 'LS608 memory cycle controller for complete dynamic RAM control.

After the user has selected and attached RC networks to pins 1, 12, and 15, the 'LS608 will deliver proper $\overline{RAS}$, $\overline{CAS}$, and READ/$\overline{WRITE}$ output signals to execute one memory cycle as the start input is switched from low to high. The actual cycle executed will depend upon steady-state input conditions of the 'LS608 as indicated in the table below.

The 'LS604 through 'LS607 multiplexed latches are ideal for storing data from two input buses, A and B, and providing the output bus with stored data from either the A or B register.

The clock loads data on the positive-going (low-level to high-level) transition. The clock pin also controls the active and high-impedance states of the outputs. When the clock pin is low, the outputs are in the high-impedance or off state. When the clock pin is high, the outputs are enabled.

The 'LS604 and 'LS605 are optimized for high-speed operation. The 'LS606 and 'LS607 are especially designed to eliminate decoding voltage spikes.

ORDERING INFORMATION:

SN 74LS 600 – REFRESH CONTROLLER, TRANSPARENT, 4K/16K
SN 74LS 601 – REFRESH CONTROLLER, TRANSPARENT, 64K
SN 74LS 602 – REFRESH CONTROLLER, CYCLE STEAL, 4K/16K
SN 74LS 603 – REFRESH CONTROLLER, CYCLE STEAL, 64K

SN 74LS 604 – MULTIPLEXER, TRI-STATE O/P, MAX SPEED
SN 74LS 605 – MULTIPLEXER, OPEN COLLECTOR O/P, GLITCH FREE
SN 74LS 606 – MULTIPLEXER, TRI-STATE O/P, MAX SPEED,
SN 74LS 607 – MULTIPLEXER, OPEN COLLECTOR O/P, GLITCH FREE
SN 74LS 608 – MEMORY CYCLE CONTROLLER

NB –NL SUFFIX FOR PLASTIC DIL. PACK
–JDL SUFFIX FOR CERAMIC DIL. PACK

TIM 99610/1/2/3 SERIES

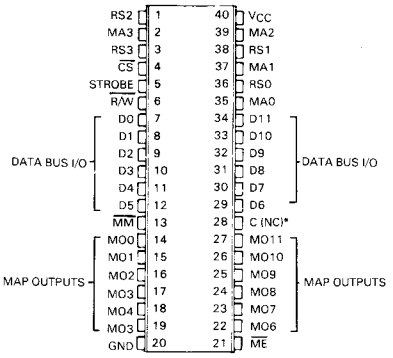
MEMORY-MAPPER CIRCUITS

FEATURES:

- Expands 64K byte memory address to 16 mega bytes.
- Page operation – 4 bits expanded to 12 bits.
- High speed 50 NS operation.
- Compatible with TMS 9900 family and other microprocessors.
- Optional latches for multiplexed bus systems.
- 40 pin package; replaces 6-10 TTL MSI components.
- Choice of 3-state or open-collector map outputs.
- Mapper bypass made supports supervisor/user separation.
- General purpose solution to memory size, management, maintenance and protection problems with microprocessors (9900).

PIN ASSIGNMENTS:

SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



Note: Pin 28 has no internal connection on 'LS612 and 'LS613

40 PIN, 600 mil

DESCRIPTION:

These memory-mapper integrated circuits contain a 4-line to 16-line decoder, a 16-word by 12-bit RAM, 16 channels of 2-line to 1-line multiplexers, and other miscellaneous circuitry on a monolithic chip. The 'LS610 and 'LS611 also contain 12 latches with an enable control.

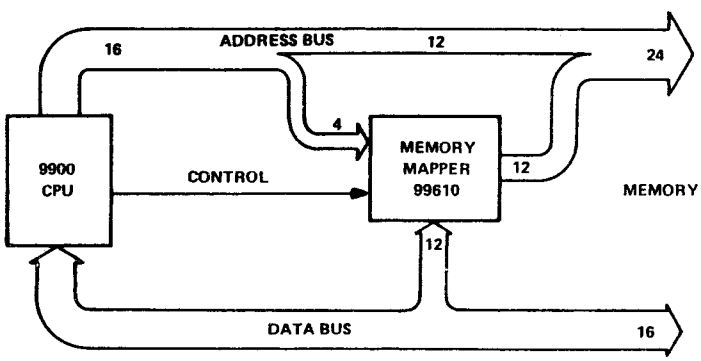
The memory mappers are designed to expand a microprocessor's memory address capability by eight bits. The four most-significant bits of the memory address bus can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus through the map output buffers along with the unused memory address bits from the CPU. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressable memory space is increased only by periodically reloading the map registers from the data bus.

This configuration lends itself to memory utilization of 16 pages of $2^{(n-4)}$ registers each without reloading (n = number of address bits available from CPU).

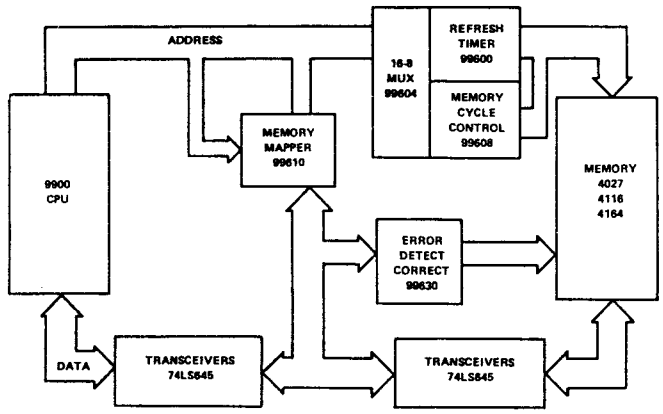
These devices have four modes of operation (read, write, map, and pass). Data may be read from or loaded into the map register selected by the register select inputs (RS0 thru RS3) under control of R/$\overline{W}$ whenever chip select ($\overline{CS}$) is low. The data I/O takes place on the data bus D0 thru D7. The map operation will output the contents of the map register selected by the map address inputs (MA0 thru MA3) when $\overline{CS}$ is high and $\overline{MM}$ (map mode control) is low. The 'LS612 and 'LS613 output stages are transparent in this mode, while the 'LS610 and 'LS611 outputs may be transparent or latched. When $\overline{CS}$ and $\overline{MM}$ are both high (pass mode), the address bits on MA0 thru MA3 appear as the most significant bits at the map outputs (assuming appropriate latch enable) with low levels in the other bit positions.

APPLICATION:

SYSTEM FUNCTION



LARGE MEMORY SYSTEM SUPPORT



ORDERING INFORMATION:

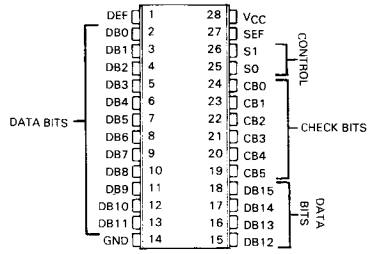
SN74LS610 – Latched outputs, Tri-state map o/p (TIM 99610)
SN74LS611 – Latched outputs, Open-collector map o/p (TIM 99611)
SN74LS612 – Unlatched outputs, Tri-state map o/p (TIM 99612)
SN74LS613 – Unlatched outputs, Open-collector map o/p (TIM 99613)
NB –NL SUFFIX FOR PLASTIC DIL. PACK
–JDL SUFFIX FOR CERAMIC DIL. PACK

FEATURES:

- **Detects and corrects single bit errors in a 16 bit word. This would account for 97% of all errors.**
- **Detects and flags dual bit errors in a 16 bit word.**
- **Fast processing times**
  - **Generates checkword in 35 ns.**
  - **Flags errors in 40 ns.**
- **Choice of tristate or open collector outputs (630/631).**
- **Compact 28 pin package.**
- **Can be used in an 8 bit environment if required.**
- **Replaces up to 24 discrete packages saving at least 12 square inches of PCB area.**
- **Power dissipation 600 mW typical.**

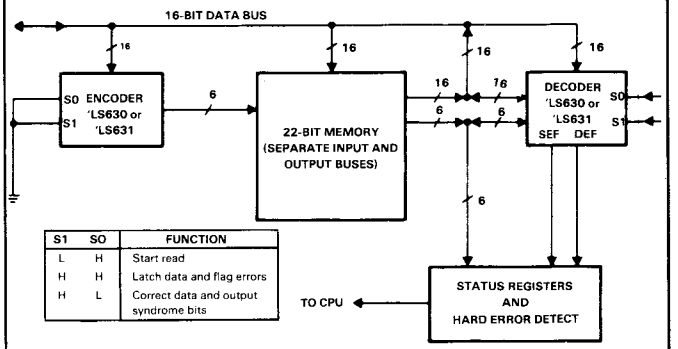
PIN ASSIGNMENTS:

SN74LS630
28 PIN PACKAGE

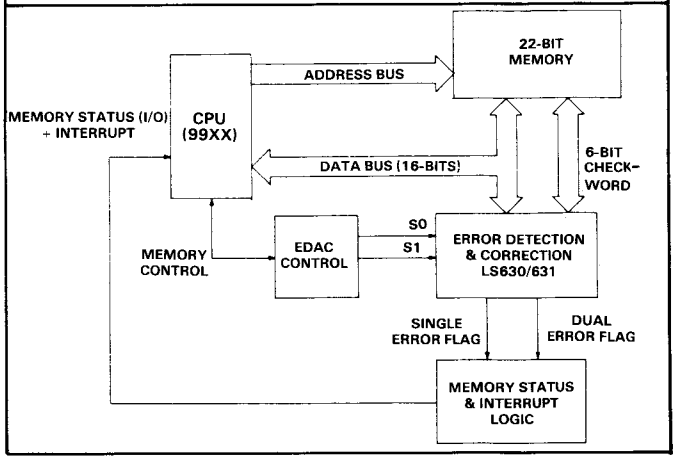


600 mil, 28 PIN

APPLICATION:



ERROR DETECTION AND CORRECTION USING TWO EDAC UNITS



DESCRIPTION:

The 'LS630 and 'LS631 devices are 16-bit parallel error detection and correction circuits (EDACs) in 28-pin, 600-mil packages. They use a modified Hamming code to generate a 6-bit checkword from a 16-bit data word. This checkword is stored along with the data word during the memory write cycle. During the memory read cycle, the 22-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 16-bit data word are flagged and corrected.

Single-bit errors in the 6-bit checkword are flagged, and the CPU sends the EDAC through the correction cycle even though the 16-bit word is not in error. The correction cycle will simply pass along the original 16-bit word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These dual errors may occur in any two bits of the 22-bit word from memory (two errors in the 16-bit data word, two errors in the 6-bit checkword, or one error in each word.

RECOMMENDED OPERATING CONDITIONS

		SN74LS630 SN74LS631			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	CB or DB, 'LS630 only			−1	mA
	DEF or SEF			−0.4	
High-level output voltage, V_{OH}	CB or DB, 'LS631 only			5.5	V
Low-level output current, I_{OL}	CB or DB			24	mA
	DEF or SEF			8	
Setup time, t_{su}	CB or DB to S1↑	10			ns
Hold time, t_h	CB or DB after S1↑	15			ns
Operating free-air temperature, T_A		0		70	°C

CONTROL FUNCTION TABLE

Memory Cycle	Control S1	Control S0	EDAC Function	Data I/O	Checkword I/O	Error Flags SEF	Error Flags DEF
WRITE	L	L	Generate Checkword	Input Data	Output Checkword	L	L
READ	L	H	Read Data & Checkword	Input Data	Input Checkword	L	L
READ	H	H	Latch & Flag Errors	Latch Data	Latch Checkword	Enabled	
READ	H	L	Correct Data Word & Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	

ORDERING INFORMATION:

SN74LS630NL – 28 PIN PLAS. DIL. (TRISTATE O/P's) 0/70°C
SN74LS630JL – 28 PIN CER. DIL. (TRISTATE O/P's) 0/70°C
SN74LS631NL – 28 PIN PLAS. DIL. (O/C O/P's) 0/70°C
SN74LS631JL – 28 PIN CER. DIL. (O/C O/P's) 0/70°C

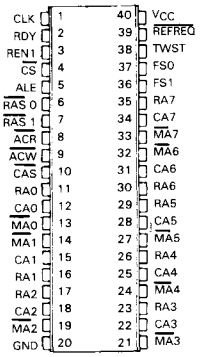
TMS 4500 NH

DYNAMIC RAM CONTROLLER

- Controls Operation of 8K/16K/32K/64K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 256K Bytes of Memory Without External Drivers
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
- Strap-Selected Wait State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)

PIN ASSIGNMENTS:

TMS 4500
40-PIN PLASTIC
DUAL IN-LINE PACKAGE
(TOP VIEW)



600 mil
40 PIN

DESCRIPTION

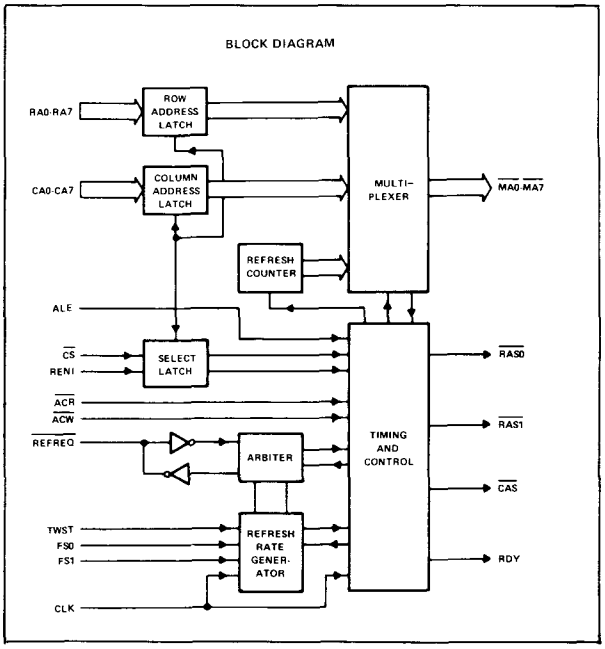
The TMS 4500 is a monolithic DRAM system controller designed to provide address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

The controller contains a 16-bit multiplexer that generates the address lines for the memory device from the 16 system address bits and provides the strobe signals required by the memory to decode the address. An 8-bit refresh counter generates the 256-row addresses required for refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention.

The TMS 4500 also contains refresh/access arbitration circuitry to resolve conflicts between memory access requests and memory refresh cycles. The TMS 4500 is offered in a 40-pin, dual-in-line plastic package nd is guaranteed for operation from 0°C to 55°C.

BLOCK DIAGRAM



PIN DESCRIPTIONS

RA0 – RA7	Input	Row Address – These address inputs are used to generate the row address for the multiplexer.
CA0 – CA7	Input	Column Address – These address inputs are used to generate the column address for the multiplexer.
$\overline{MA0}$ – $\overline{MA7}$	Output	Memory Address – These outputs are designed to drive the addresses of the dynamic RAM array.
ALE	Input	Address Latch Enable – This input is used to latch the 16 address inputs, $\overline{CS}$ and REN1. This also initiates an access cycle if chip select is valid. The rising edge (low level to high level) of ALE, $\overline{ACR}$ or $\overline{ACW}$, whichever occurs first, terminates the cycle by returning $\overline{RAS}$ and $\overline{CAS}$ to the high level.
CS	Input	Chip Select – A low on this input enables an access cycle. The trailing edge of ALE latches the chip select input.
REN1	Input	RAS Enable 1 – This input is used to select one of two banks of RAM via the $\overline{RAS}$ 0 and $\overline{RAS}$ 1 outputs when chip select is present.
$\overline{ACR}$, $\overline{ACW}$	Input	Access Control, Read; Access Control, Write – A low on either of these inputs causes the column address to appear on $\overline{MA0}$ – $\overline{MA7}$ and the column address strobe. The rising edge of $\overline{ACR}$ or $\overline{ACW}$ or $\overline{ALE}$ terminates the cycle by ending $\overline{RAS}$ and $\overline{CAS}$ strobes.
CLK	Input	System Clock – This input provides the master timing to generate refresh cycle timings and refresh rate. Refresh rate is determined by the TWST, FS1 FS0 inputs.
$\overline{REFREQ}$	Input/Output	Refresh Request – (This input should be driven by an open-collector output.) On input, a low-going edge initiates a refresh cycle and will cause the internal refresh timer to be reset on the next falling edge of the CLK. As an output, a low-going edge signals an internal refresh request and that the refresh timer will be reset on the next low-going edge of CLK. $\overline{REFREQ}$ will remain low until the refresh cycle is in progress and the current refresh address is present on $\overline{MA0}$–$\overline{MA7}$.
$\overline{RAS0}$, $\overline{RAS1}$	Output	Row Address Strobe – These outputs are used to latch the row address into the bank of DRAMs selected by REN1. On refresh both signals are driven.
$\overline{CAS}$	Output	Column Address Strobe – This output is used to latch the column address into the DRAM array.
RDY	Output	Ready – This output synchronizes memories that are too slow to guarantee microprocessor access time requirements. This output is also used to inhibit access cycles during refresh when in cycle-steal mode.
TWST	Input	Timing/Wait Strap – A high on this input indicates a wait state should be added to each memory cycle. In addition it is used in conjunction with FS0 and FS1 to determine refresh rate and timing.
FS0, FS1	Inputs	Frequency Select 0; Frequency Select 1 – These are strap inputs to select Mode and Frequency of operation as shown in Table 1.

ORDERING INFORMATION:

TMS 4500 NH – 40 PIN PLASTIC (0/55°)
TMS 4500 JDH – 40 PIN CERAMIC (0/55°C)

FUNCTION	DESCRIPTION	AVAILABLE TECHNOLOGIES
0 OCTAL LINE DRIVERS/BUFFERS		
SN54/74LS240	3 STATE, INVERTING O/P DRIVES	LS, S, ALS*
SN54/74LS241	3 STATE O/P DRIVER	LS, S, ALS*
SN54/74LS244	3 STATE O/P DRIVER	LS, S, ALS*
SN54/74LS540	3 STATE INVERTING O/P DRIVER BUFFER	LS, ALS*
SN54/74LS541	3 STATE O/P DRIVER/BUFFER	LS, ALS*
SN54/74ALS1240	ULTRA LOW POWER 240	ALS*
SN54/74ALS1241	ULTRA LOW POWER 241	ALS*
SN54/74ALS1244	ULTRA LOW POWER 244	ALS*
0 BIDIRECTIONAL OCTAL BUS TRANSCEIVERS		
SN54/74LS245	3 STATE O/P	LS
SN54/74LS620	3 STATE INVERTING O/P	LS, ALS*
SN54/74LS621	O-C O/P	LS, ALS*
SN54/74LS622	O-C INVERTING O/P	LS, ALS*
SN54/74LS623	3 STATE O/P	LS, ALS*
SN54/74LS638		LS, ALS*
SN54/74LS639		LS, ALS*
SN54/74LS640	3-STATE INVERTING O/P	LS, ALS*
SN54/74LS641	O-C O/P	LS, ALS*
SN54/74LS642	O-C INVERTING O/P	LS, ALS*
SN54/74LS643	3-STATE TRUE AND INVERTING O/P	LS, ALS*
SN54/74LS644	O-C TRUE AND INVERTING O/P	LS, ALS*
SN54/74LS645	3-STATE TRUE O/P	LS, ALS*
SN54/74LS646	3-STATE O/P TRANSCEIVERS/REGISTER	LS, ALS*
SN54/74LS647	O-C O/P TRANSCEIVER/REGISTER	LS, ALS*
SN54/74LS648	3-STATE INVERTING O/P TRANSCEIVER/REGISTER	LS, ALS*
SN54/74LS649	O-C INVERTING O/P TRANSCEIVER/REGISTER	LS, ALS*
SN54/74ALS1638	ULTRA LOW POWER 638	ALS*
SN54/74ALS1639	ULTRA LOW POWER 639	ALS*
SN54/74ALS1640	ULTRA LOW POWER 640	ALS*
SN54/74ALS1641	ULTRA LOW POWER 641	ALS*
SN54/74ALS1642	ULTRA LOW POWER 642	ALS*
SN54/74ALS1643	ULTRA LOW POWER 643	ALS*
SN54/74ALS1644	ULTRA LOW POWER 644	ALS*
SN54/74ALS1645	ULTRA LOW POWER 645	ALS*
0 TRIDIRECTIONAL QUAD BUS TRANSCEIVERS		
SN54/74LS440	O-C O/P	LS
SN54/74LS441	O-C INVERTING O/P	LS
SN54/74LS442	3-STATE O/P	LS
SN54/74LS443	3-STATE INVERTING O/P	LS
SN54/74LS444	3-STATE TRUE/INVERTING O/P	LS
SN54/74LS448	O-C TRUE/INVERTING O/P	LS

O-C = OPEN COLLECTOR O/P = OUTPUT * = 1982 AVAILABILITY

MEMORIES

ORGANISATION	DEVICE CODE	SPEED (NS) ACCESS/CYCLE	MAX OPERATING POWER	MAX STAND BY POWER	PACKAGE
16K x 1 DRAM	TMS 4116-15	150/375	462 mw	20 mw	16 pin
	TMS 4116-20	200/375	462 mw	20 mw	16 pin
	TMS 4116-25	250/410	462 mw	20 mw	16 pin
32K x 1 DRAM	TMS 4532-15	150/280	200 mw	27.5 mw	16 pin
	TMS 4532-20	200/350	200 mw	27.5 mw	16 pin
	TMS 4532-25	250/410	200 mw	27.5 mw	16 pin
64K x 1 DRAM	TMS 4164-15	150/280	200 mw	27.5 mw	16 pin
	TMS 4164-20	200/350	200 mw	27.5 mw	16 pin
	TMS 4164-25	250/410	200 mw	27.5 mw	16 pin
4K x 1* SRAM	TMS 4044-15	150 ns	440 mw	—	18 pin
	TMS 4044-20	200 ns	440 mw	—	18 pin
	TMS 4044-25	250 ns	440 mw	—	18 pin
	TMS 4044-45	450 ns	440 mw	—	18 pin
4K x 1 SRAM	TMS 2147-3	35 ns	715 mw	165 mw	18 pin
	TMS 2147-4	45 ns	715 mw	165 mw	18 pin
	TMS 2147-5	55 ns	715 mw	165 mw	18 pin
	TMS 2147-7	70 ns	715 mw	165 mw	18 pin
1K x 4* SRAM	TMS 2114-15	150 ns	550 mw	—	18 pin
	TMS 2114-20	200 ns	550 mw	—	18 pin
	TMS 2114-25	250 ns	550 mw	—	18 pin
	TMS 2114-45	450 ns	550 mw	—	18 pin
1K x 4 SRAM	TMS 2149-3	35 ns	715 mw	—	18 pin
	TMS 2149-4	45 ns	715 mw	—	18 pin
	TMS 2149-5	55 ns	715 mw	—	18 pin
	TMS 2149-7	70 ns	715 mw	—	18 pin
2K x 8 SRAM	TMS 4016-15	150 ns	475 mw	—	24 pin
	TMS 4016-20	200 ns	475 mw	—	24 pin
	TMS 4016-25	250 ns	475 mw	—	24 pin
	TMS 4016-45	450 ns	475 mw	—	24 pin
1K x 8 EPROM	TMS 2708 JL	450 ns	—	—	24 pin
	TMS 2708-35 JL	350 ns	—	—	24 pin
	TMS 27L08 JL	450 ns	580 mw	—	24 pin
	TMS 2508-25 JL	250 ns	447 mw	132 mw	24 pin
	TMS 2508-30 JL	300 ns	447 mw	132 mw	24 pin
	TMS 2758 JL	450 ns	525 mw	132 mw	24 pin
2K x 8 EPROM	TMS 2716 JL	450 ns	720 mw	—	24 pin
	TMS 2516-35 JL	350 ns	525 mw	132 mw	24 pin
	TMS 2516 JL	450 ns	525 mw	132 mw	24 pin
4K x 8 EPROM	TMS 2532 JL	450 ns	840 mw	132 mw	24 pin
	TMS 25L32 JL	450 ns	500 mw	132 mw	24 pin
	TMS 2532-35 JL	350 ns	840 mw	132 mw	24 pin
	TMS 2532-30 JL	300 ns	840 mw	132 mw	24 pin
8K x 8 EPROM	TMS 2564 JL	450 ns	880 mw	132 mw	28 pin
16 x 4 BIPOLAR RAM	SN74LS189/289	80 ns	315 mw	—	16 pin
	SN74S189/289	35 ns	518 mw	—	16 pin
32 x 8 PROM	TBP18SO30/SAO30	40 ns	578 mw	—	16 pin
256 x 4 PROM	TBP24S10/SA10	55 ns	525 mw	—	16 pin
256 x 8 PROM	TBP28L22/LA22	70 ns	525 mw	—	20 pin
512 x 8 PROM	TBP28S42/SA42	60 ns	709 mw	—	20 pin
1K x 4 PROM	TBP 24541/SA41	60 ns	735 mw	—	18 pin
1K x 8 PROM	TBP28S86/SA86	70 ns	919 mw	—	24 pin
2K x 8 PROM	TBP28S166	75 ns	525 (typ)	—	24 pin

*LOW-POWER VERSIONS (40L44, 2114L) AVAILABLE.

Section 4 Microcomputer boards

FEATURES:

- **Provides a standard electrical and mechanical connection.**
- **20 line address/data/interrupt bus.**
- **16 lines control bus.**
- **3 lines CRU bus (CRUOUT is multiplexed with A/D15).**
- **3 lines analog signal bus.**
- **7 lines reserved.**

DESCRIPTION:

Power Bus:- 4 lines for +5V, 1 line +12V, 1 line −12V, +BATT, +5VSTBY, +15V, −15V and 6 GND lines. These lines provide regulated voltages to the modules, +15V and −15V are for use by the analog interfaces, and there are 2 lines for backup, +5VSTBY which is used when the power fails and when it is operational, and a +BATT line which is for other than 5V and is only used in a powerfail mode.

Address/Data/Interrupt Bus:- Consists of 20 three state lines. These lines are triple multiplexed to function as address/data/interrupt buses at different points in time, A/D 15 is also used as a CRUOUT line. The particular type of data on the bus at a particular time is indicated by the control bus. This bus can only be driven by the present bus master. The address bus allows addressing up to 1MByte of memory using 16 basic address lines and 4 extended address lines, it also allows 12 bit CRU addressing. The data bus consists of 16 bi-directional lines. The interrupt bus consists of 7 lines which hold an interrupt code (consists of priority and who is to service) when an interrupt has occurred (signaled by INTEN line going to logic 0).

Control Bus:- This consists of 16 lines which control all transactions on the bus, it can be broken down into several subsets:-

Memory Control:- Consists of $\overline{\text{MEMEN}}$, $\overline{\text{WE}}$, $\overline{\text{AREADY}}$, $\overline{\text{READY}}$, $\overline{\text{DEN}}$, ALATCH, MEMWIDTH, these indicate that a memory access is in progress, data to memory is on the bus memory is ready next clock cycle, memory is ready this clock cycle, memory read is taking place, memory address on the bus, and an indication of the width of data transfer (word or byte), respectively.

CRU Bus:- Used for serial data transfer, 3 lines provide separate information paths, CRUIN serial input line, CRUOUT serial output line, CRUCLK clock signal gating data.

3 bus arbitration signals $\overline{\text{BUSY}}$, GRANTIN, GRANTOUT. Which indicate requesting device has taken bus, no device with higher priority is requesting the bus, and that a lower priority device may request control of the bus, respectively. GRANTIN and GRANTOUT form a daisy chain priority scheme for transfering bus control. Sync signal, $\overline{\text{BUSCLK}}$ provides synchronisation and must not exceed 10 MHz.

5 Miscellaneous Signals:- $\overline{\text{IORST}}$, $\overline{\text{PRES}}$, $\overline{\text{NMI}}$, $\overline{\text{PWFRFAIL}}$, $\overline{\text{INTEN}}$, which indicate to the system that a system reset is in progress to the I/O devices, power supply has stabilised and processor can begin execution, non maskable interrupt is taking place, a signal from the power supply indicating the loss of primary power, a valid interrupt code is on the bus, respectively.

Analog Signal Bus:- Consists of 3 lines ANAHI, ANALO, ANACOM which can carry analog signal of up to +/− 10V.ANACOM is the ground return path.

Reserved Lines:- Bussed to all slots on the backplane intended for future use.

E-BUS PIN DEFINITION

	ROW A		ROW C	
PIN	SIGNAL	GROUP	SIGNAL	GROUP
1	GND	POWER BUS	GND	POWER BUS
2	$\overline{\text{PRES}}$	CONTROL BUS	$\overline{\text{BUSCLK}}$	CONTROL BUS
3	+12V	POWER BUS	−12V	POWER BUS
4	$\overline{\text{IORST}}$	CONTROL BUS	$\overline{\text{NMI}}$	CONTROL BUS
5	+5V	POWER BUS	+5V	POWER BUS
6	+BATT			
7		RESERVED		RESERVED
8				
9				
10	$\overline{\text{INTEN}}$	CONTROL BUS	ALATCH	CONTROL BUS
11	XA0		XA1	
12	XA2		XA3	
13	A0/D0/INT0		A1/D1/INT1	
14	A2/D2/INT2	ADDRESS/DATA/	A3/D3/INT3	ADDRESS/DATA/
15	A4/D4/INT4	INTERRUPT BUS	A5/D5/INT5	INTERRUPT BUS
16	A6/D6/INT6		A7/D7	
17	A8/D8		A9/D9	
18	A10/D10		A11/D11	
19	A12/D12		A13/D13	
20	A14/D14		A15/D15/CRUOUT	
21	$\overline{\text{AREADY}}$		$\overline{\text{MEMEN}}$	
22	$\overline{\text{DEN}}$		$\overline{\text{READY}}$	
23	$\overline{\text{GRANTIN}}$	CONTROL BUS	$\overline{\text{GRANTOUT}}$	CONTROL BUS
24	$\overline{\text{PWRFAIL}}$		$\overline{\text{BUSY}}$	
25	GND	POWER BUS	GND	POWER BUS
26	+15V		ANAHI	ANALOG BUS
27	ANACOM	ANALOG BUS	ANALO	
28	−15V	POWER BUS	CRUIN	CRU BUS
29	$\overline{\text{WE}}$	CONTROL BUS	+5VSTBY	POWER BUS
30	+5V	POWER BUS	+5V	
31	MEMWIDTH	CONTROL BUS	$\overline{\text{CRUCLK}}$	CRU BUS
32	GND	POWER BUS	GND	POWER BUS

FURTHER INFORMATION:

E-BUS SPECIFICATION
E-BUS DESIGN MANUAL

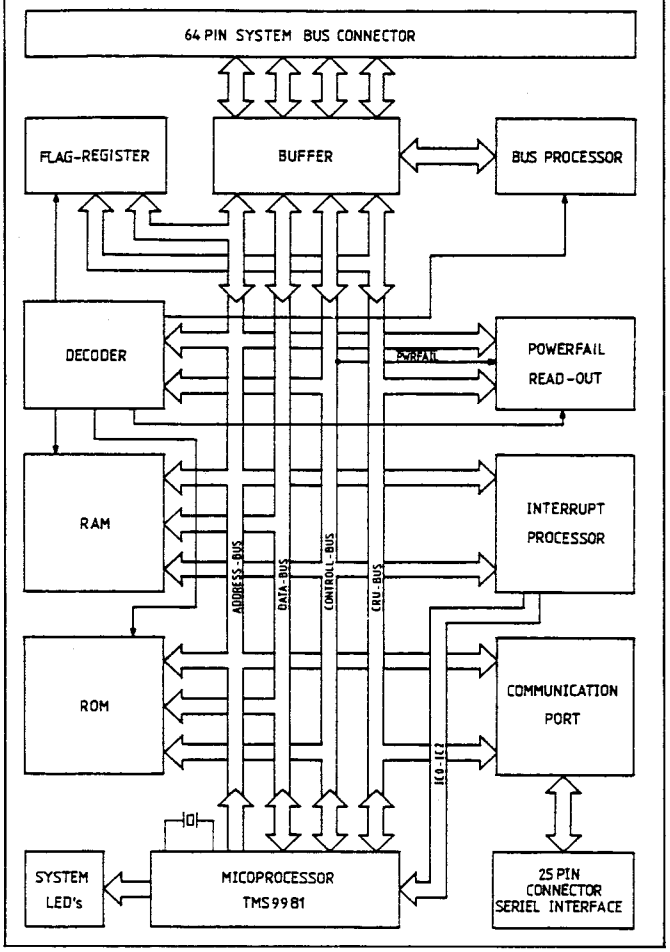
TM990/E150

E-BUS MICROCOMPUTER

FEATURES:

- **16 Bit 9981 Microprocessor.**
- **Up to 8K bytes EPROM.**
- **1K byte on-board RAM.**
- **1K bit Flag register.**
- **6 Interrupt Levels.**
- **Serial port EIA/RS232C compatible may be synchronous or asynchronous.**
- **E-BUS COMPATIBLE, DIN 41612 Connector.**
- **0–70°C operating temperature range for HARSH INDUSTRIAL ENVIRONMENTS.**
- **Factory burnt-in for RELIABILITY.**
- **COMPACT 100 mm × 160 mm single eurocard.**

BLOCK DIAGRAM:



DESCRIPTION:

The TM990/E150 is a Microcomputer (MC) module designed to be the MASTER in a single master E-BUS system.

RAM-Memory
The on board RAM consist of 2X TMS 4045 NL-45 4K static RAM's. It does not require any wait states. The 1K Byte RAM area is located from > 3COO to > 3FFF or > O to > 3FF.

EPROM/ROM Memory
One 28 Pin EPROM/ROM can be used to use TMS 2508, 2516, 2532 and TMS 2564 EPROM's or TMS 4732/4764 ROM. This gives up to 8K Byte on board EPROM. A jumper on the memory decoder selects TMS 2532 or 2564. In the jumper position "TMS 2532" a TMS 2516 or TMS 2508 can be inserted when the loss of 2K or 3K Byte address space can be accepted. If not, a new memory decoder PROM must be generated.

OFF Board RAM/EPROM
The internal RAM/EPROM space can be externally extend to the full 16K Byte address space of the TMS 9981. OFF board ALATCH cycles are generated to accomplish the BUS Spec A0, A1, XA0–XA3 is held low and MEMWIDTH is held high on any external memory cycle.

EIA PORT
The programmable asynchronous/synchronous communication port of the TM990/150 is implemented by the TMS 9902/9903. In addition to the standard RS-232-C interface the μT- and 20 mA TTY-interface is jumper selected. The TM990/150 EIA-Port is identical to P2 of the TM990/100M/101M.

Timer
The TM990/150 has one programmable timer with up to 19.5 ms time interval provided by the TMS 9902 UART.

Interrupt Logic
The TM990/150 supports four external interrupts inputed on the coded INT4 thru INT6 bus lines. INTO–INT3 interrupt lines of the bus are not used.

External and internal $\overline{\text{PRES}}$ and $\overline{\text{NMI}}$ interrupt is also provided. The TMS 9902 interrupt output is connected to the interrupt level 4 of the TMS 9981. The $\overline{\text{PWRFAIL}}$ interrupt of the backplane is set to the level 1 interrupt of the TMS 9981 and can be read out thru the CRU interface.

Flag Register
A 1K bit flag register (TMS 4044 NL-45) is available on the CRU address >800 – FFE and >0 – >3F (WR12), see Appendix B. This can be used in conjunction with the CRU set, reset and test bit instruction for easy control of a large number of flags.

BUS Logic
The E-BUS logic is implemented for single master systems with a DMA mode to allow external (DMA) controller to access the bus. GRANTOUT is directly connected to the GRANTIN with a 2.2KOhm resistor to +5V. All driver and receiver loads to meet the BUS-SPEC.

ORDERING INFORMATION:

TM990/E150-1	MICROCOMPUTER, EPROM SOCKET POPULATED, with TIBUG in TMS 2516. 1K byte RAM, 1K bit FLAGS.
TM990/150-2	OEM VERSION, NO EPROM, NO DOCUMENTATION.

TM990/E151

E-BUS SYSTEM, STANDALONE MICROCOMPUTER

FEATURES:

- **16-bit microprocessor TMS 9981 with on-chip oscillator.**
- **1K to 8K byte EPROM's using TMS 2508/16/32/64 or compatible ROM's.**
- **2K byte fully static RAM using TMS 2114.**
- **1K bit FLAG-register (optional).**
- **6 interrupt levels (4 maskable and 2 nonmaskable, RESET and NMI).**
- **Compatible with the CRU-I/O part of TI's advanced E-BUS system.**
- **Compatible with standard DIN 41612 connectors, racks and cabinets.**
- **On board 8 channel A/D-converter with 8 bit resolution (option).**
- **E-BUS compatible, DIN 41612 connectors.**
- **0–70°C operating temperature range for HARSH INDUSTRIAL ENVIRONMENTS.**
- **Factory burnt in for RELIABILITY.**
- **COMPACT 100 mm × 160 mm single eurocard.**

DESCRIPTION:

The TM990/E151 is a single eurocard STANDALONE microcomputer module designed for high volume OEM applications. It has an interface to the E-BUS system for I/O expansion only through the use of TI's CRU Command Driven I/O architecture.

MICROPROCESSOR UNIT (TMS 9981 MPU)
The TMS 9981/TMS 9981 NL microprocessor is used as the Micro-Processor Unit at 10 MHz clock rate. This gives a 2.5 MHz system clock frequency.

CONTROL LOGIC
The control-logic generates a reset signal during power on sequence and also if PRES- (power reset) is active. Also it generates an IORSET-signal for all I/O-circuits.

An on board reset switch is not provided. This function might be implemented externally by pulling the PRES- line low.

ON BOARD MEMORY
The on board memory area provides for enough ROM and RAM to cover the applications foreseen for the board.

RAM MEMORY
The on board RAM-area consists of 4 × TMS 4045 4K static RAM's which do not require any wait states. The 2K byte RAM area is located from >3800 to >3FFF (see also Appendix A).

ROM MEMORY
One 28 pin socket can be used for ROM's or EPROM's with a single +5V supply voltage. These are EPROM's of the series TMS 25XX (TMS 2508/16/32/64) and ROM's of the TMS 47XX series. These give up to 8K byte program area to the user. The ROM memory area is located in the lower memory area from >0 to >1FFF.

FLAG REGISTER
A 1K bit FLAG register (TMS 4044) is available at the CRU address >800 to >FFE (WR 12, see also Appendix B). This can be used in conjunction with all CRU instruction to easily control of a large number of flags.

INTERRUPT LOGIC
The TM990/TM990/E151 supports four maskable static interrupts and two nonmaskable. These are:

- RESET (non maskable)
- NMI (non maskable)
- POWER FAIL (level 1)
- ADC (level 2)
- CLOCK (level 3)
- INTEN (level 4)

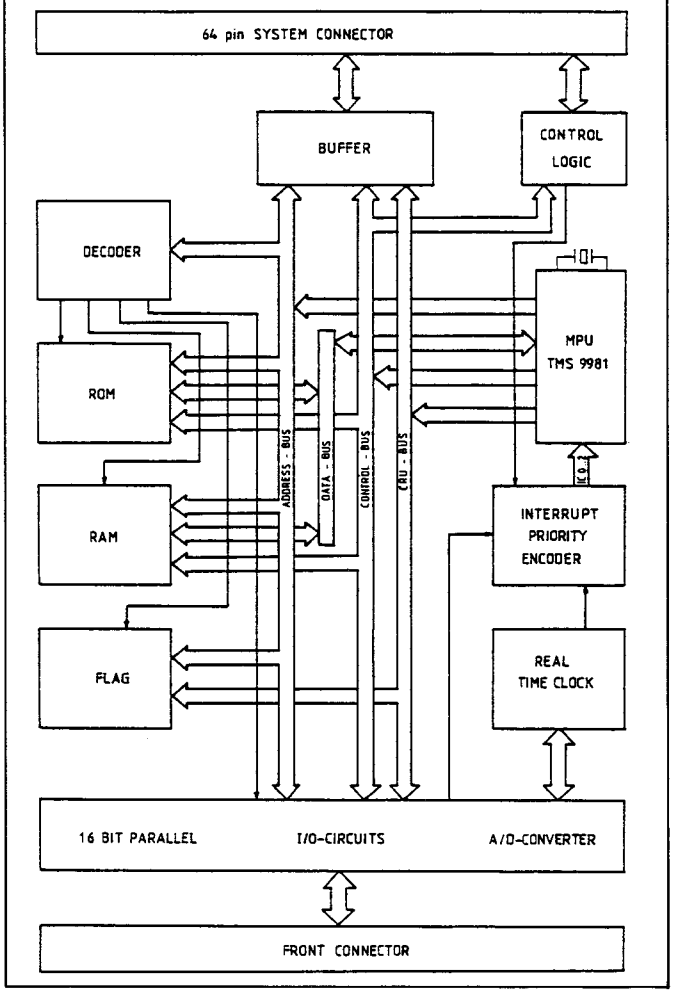
All interrupts are changed into a code, by the interrupt priority encoder (ICO..2) for the TMS 9981.

BUS BUFFER
The bus interface is a reduced E-BUS interface, it allows only CRU-Expansion. Therefore the following signals are necessary:

- Address Lines A0 to A14
- CRUCLK-
- CRUOUT
- BUSCLK
- IORSET
- BUSY (always LOW)
- MEMEN-

The bus drivers can be disabled (jumper selectable). Therefore, it is possible to plug this microcomputer board into a TM990/E-Microcomputer system as a stand alone computer.

BLOCK DIAGRAM:



TTL I/O CIRCUITS
The I/O area consists of 16 TTL inputs (2 ×SN74LS251) and 16 TTL outputs (2 × SN74LS259). The ports can be easily controlled via CRU.

Three output ports and one input port are needed for the TI-BUS interface, if an IIL-Clock is used. An additional input port is needed for the POWERFAIL-Identification, if a POWERFAIL/Routine is used (jumper selectable).

A/D-CONVERTER
The used ADC 0808 is a new TI device in CMOS technology.

- 8 Bit Resolution
- Total Unadjusted Error ×/— 1/2 LSB
- 100 µs Conversion Time
- Latched 3-state Outputs
- Single 5-Volt Supply

After each conversion the device generates an interrupt (level 2) to indicate the end of conversion.

ORDERING INFORMATION:

TM990/E151-2 1K Byte RAM, socket for further 1K byte. No a/d, clock or flag register.

TM990/E151-3 TM990/E151-1 with no RTC clock chip.

TM990/E155

E-BUS MICROCOMPUTER

FEATURES:

- 12 MHz, 16 Bit 9995 microprocessor.
- 64K byte physical address space.
- 1M byte logical address space using CRU BANK SWITCHING.
- Up to 16K byte EPROM.
- Up to 4K byte static RAM.
- 6 interrupt levels.
- On board TIMER/EVENT COUNTER.
- On board 16 Bit FLAG REGISTER.
- E-BUS compatible, DIN 41612 Connector.
- 0–70°C operating temperature range, for harsh industrial environments.
- Factory burnt in for RELIABILITY.
- COMPACT 100 mm × 160 mm single eurocard.
- Single 5V supply.

DESCRIPTION:

The TM990/E155 is a microcomputer (MC) module deisgned to be a MASTER in a single master E-BUS system. It uses TI's 9995 microprocessor, which features on-chip RAM, TIMER & FLAG REGISTER, and using a 12 MHz crystal clock benchmarks at between 1.5 and 3.0 times the throughput of a 3 MHz TMS 9900. A 16 Bit by 16 Bit multiply instruction takes just 7.67 µS to execute. The TM990/E155, uses TI's unique Command Driven I/O architecture (CRU) to access the four most significant address lines of the E-BUS backplane (XA0–XA3) to effectively expand the address capability of the 9995 from 64K bytes to 1M byte, through a "bank switching" mapping technique.

CONTROL LOGIC
The control logic generates a reset signal during the power-on sequence. A PRES- signal, fed from the system bus to this circuitry, forces a CPU reset as well as generating the IORST-signal. All CRU-modules attached to this signal on the system bus will thereby be set to a proper condition during power up.
The TM990/E155 control logic also contains single-step logic which allows the execution of a single instruction under software control.
The LREX instruction generates the LREX-Pulse (external instruction) which activates the Single-Step Logic, ending in an NMI interrupt on completion of the single instruction execution.
The NMI-Interrupt from the E-Bus goes directly to the MPU and therefore the NMI can also be used as a normal Interrupt.

On Board Memory
On the TM990/E155 there are three ways to change The Memory Map. A jumper is installed for selecting the ROM (32K/64K) size. The other two signals are changeable via CRU (see section 3.5). These are RAM HIGH/LOW and Memory Map 0/1. Since in memory map 1 the on-board memory can be disabled, the names of the signals RAM L/H and ROM 32/64 only make sense in the Memory Map 0. In Memory Map 1 the user can employ these signals to select one of the four other different Memory maps.

Memory Map Applications
This feature, plus the separate on-board areas allows the use of different standard Software Systems in one Hardware configuration. A small program in the on-chip RAM area can control this switching by CRU. E.g. use EUROBUG 4 for program debugging, and in the same system, have the possibility to switch to POWER BASIC which is installed at the Memory address >0000 on a Memory expansion board. If the user switches off the on board Memory and goes with a BLWP to address >0000 he is automatically in POWER BASIC. For this he has two possibilities, to switch off the whole on-board Memory, if he has a RAM expansion on address >F000 to >FFFF, or only on-board ROM. If bank switching is used, 17 different programs can be chosen in this way.

RAM Memory
The on-board RAM area consists of two TMS 4016 devices. Each of those devices is organised as 2K × 8-Bits. RAM's used must have an access time without wait states of less than 130 ns, and with one wait, less than 460 ns. The two chips are wired to provide 4K-bytes of RAM.

ROM Memory
Two 28 pin sockets may be used for several different ROM/EPROM devices with a single +5V supply voltage. These are EPROM's of the TMS 25XX series. It is also possible to use pin-compatible ROM's (e.g. TMS 4732).
The EPROM's or ROM's used must have an access time without wait states of less than 95 ns, and with one wait state, less than 428 ns.
The standard memory map is set up for TMS 2532 and TMS 2564 EPROM's (jumper selectable).

On-board CRU

ADDR. WR 12	CRU ADDR.	CRU READ	CRU WRITE
–0000–	–0000–		
–013E–	–009F–		
–0140–	–00A0–	PWRF–IDENTIFICATION	ERROR LED
–0142–	–00A1–	INT4–IDENTIFICATION	NOT USED
–0144–	–00A2–	RAM HIGH/LOW	RAM HIGH/LOW
–0146–	–00A3–	MEMORY MAP0/1	MEMORY MAP 0/1
–0148–	–00A4–	XA3	XA3
–014A–	–00A5–	XA2	XA2
–014C–	–00A6–	XA1	XA1
–014E–	–00A7–	XA0	XA0
–0150–	–00A8–	SAME BLOCK REPEATED	
–015E–	–00AE–		
–FFFE	–7FFF–		

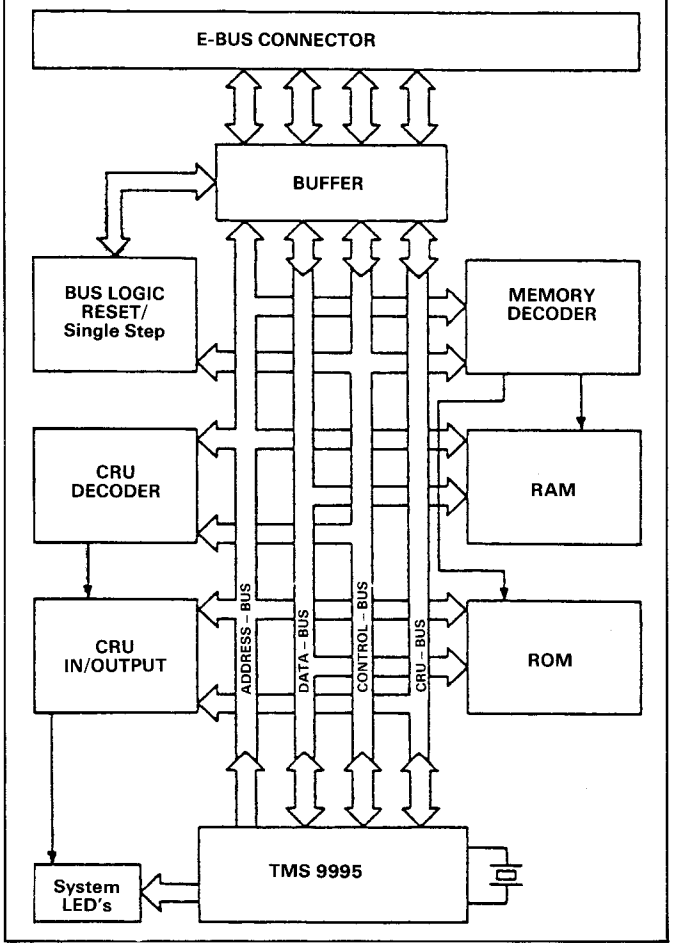
On-Board CRU Map

There are 8 CRU in- and output bits used on the CPU board. For these bits, the addresses are not fully decoded, therefore they all have two different addresses (e.g. bit 0: >140 and >150 in WR12).
After a RESET, all output bits are LOW.

ORDERING INFORMATION:

TM990/E155-1 EPROM sockets unpopulated.
TM990/E155-2 RAM & EPROM sockets unpopulated.

BLOCK DIAGRAM:



POWER-FAIL Identification
At this CRU address the status of the POWER FAIL-interrupt line from the back-panel can be read. This feature is useful after executing a power fail routine. After all vital data has been saved, the routine can test the POWER FAIL line and decide whether to go into the IDLE state (interrupt still active), or to resume normal operation (interrupt no longer present, was probably caused by a short power glitch).

INT4-Identification
The TM990/E155 uses the INTEN- line as a static common interrupt line, connected to the INT4 input of the TMS 9995 CPU. Therefore the INT4-identification, at >142 in WR12, can be used to test the INTEN-line. A signal on INT4 means that some interrupt was received from the bus, and polling must be used to determine which one. At the end of an INT4 activated routine, after the source of the interrupt has been cleared, if the INT4-identification line is still low (active), another interrupt has occurred in the meantime and is pending, and the processor may avoid some delay in processing the new interrupt by immediately resuming the polling process.

ERROR LED
The output bit (>140) is connected to the error LED, and can be switched on and off. Please note, that the LED is initially ON after reset. It is off when the CRU bit is one.

Extended Address Lines (XA0–XA3)
The TM990/E155 has a directly addressable memory area of 64K byte. Via CRU it is possible to control the Extended Address lines (XA0–XA3). This allows bank switching and gives access to a memory area of up to 1M Byte (16 banks with up to 64K bytes each).

Interrupts
Four of the 6 Interrupts of the TMS 9995 are at the user's disposal. Four Interrupts are maskable, PRES- and NMI- are non-maskable. Table 1 shows the interrupt assignment.

Table 1: Interrupt Data

Use	Interrupt level	Function	
PRES-	0	RESET	Highest priority
NMI-	—	Non-Maskable-Interrupt (LOAD, single step)	
INT1	1	POWERFAIL	
INT2	2	Arithmetic overflow, MID	
INT3	3	Internal Decrementer	
INT4	4	INTEN-*	Lowest priority

*This Interrupt line is used as static common interrupt line.

SYSTEM LED's
There are three LED's on the front edge of the board.
The upper one is the red IDLE LED. This LED is controlled by the IDLE pulse, and it is ON if the processor is in the IDLE state.
The second one is the green RUN LED. It is controlled by the IAQ pulse of the processor. If the processor is executing instructions, this LED will be ON.
The last one, is a red ERROR LED. It is controlled via CRU (see section 3.5.1), and is initially ON after reset. It should then normally be extinguished by the user software after a successful self-test.

TM990/E250

E-BUS MEMORY AND I/O EXPANSION MODULE

FEATURES:

- **Up to 4K bytes of static RAM.**
- **BATTERY BACKUP Option for RAM.**
- **Up to 8K bytes of EPROM.**
- **16 TTL compatible inputs.**
- **16 TTL compatible outputs.**
- **E-BUS COMPATIBLE, DIN 41612 Connector.**
- **DIN 41612 Standard I/O Connector.**
- **0–70°C Operating Temperature range for HARSH INDUSTRIAL ENVIRONMENTS.**
- **Factory Burnt in for RELIABILITY.**
- **COMPACT 100 mm × 160 mm Single eurocard.**
- **Single 5V supply rail.**

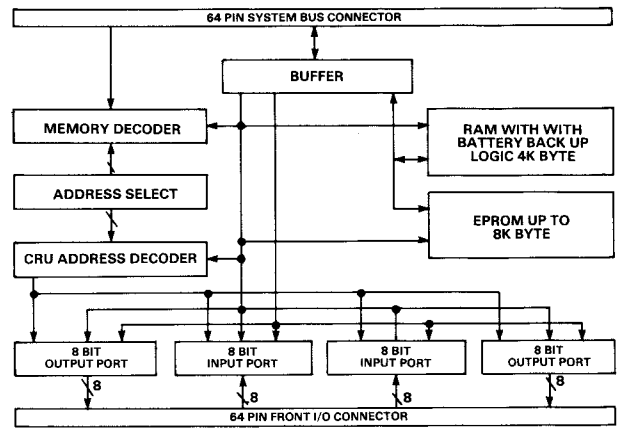
DESCRIPTION:

The TM990/E250 is a combination memory and I/O expansion (MIE) module designed to work with TI's popular range of E-BUS eurocard standard MICROCOMPUTERS. Both the RAM and EPROM memory blocks can be mapped into E-BUS SYSTEM memory, using Dual-In-Line (DIL) switches on board. Designed for REALTIME Systems, the memory control circuits make use of the standard E-BUS signal PRES- to limit access to the RAM during power-up, power-down and 'brown-out' sequences. Additionally a facility for using the E-BUS Standby option, to provide for non-volatile data or program storage in the absence of primary power. The I/O is accomplished using TI's unique Command Driven I/O architecture, the Communications Register Unit ('CRU') allowing direct access to single or multiple bits of either input or output using single instructions. The TM990/E250 provides DIL switches for the selection of the CRU base address.
The I/O is configured as four ports of 8-bits each, the two output ports using SN74LS259 latches; the inputs using SN74LS251 circuits. Both these IC's utilise Robust Schottky Bipolar technology for excellent drive capability. A self-test facility could be provided by the user by looping back an output port to an input port off board. Both the E-BUS and I/O connectors conform to DIN 41612 standards for reliability and a wide range of compatible racking equipment is available for the standard 100 mm × 160 mm Single Eurocard.

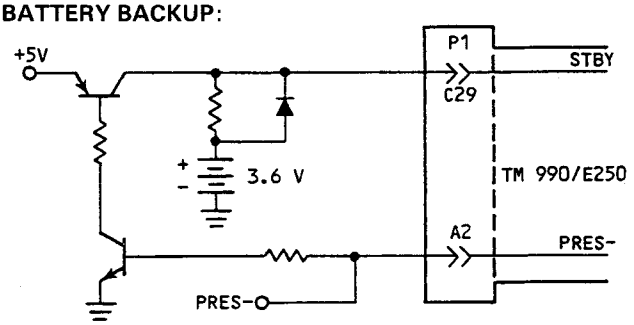
ORDERING INFORMATION:

TM990/E250-1	FULLY POPULATED 4K bytes RAM & I/O, NO EPROM.
TM990/E250-2	2Kbytes RAM, NO I/O OR CONNECTOR.

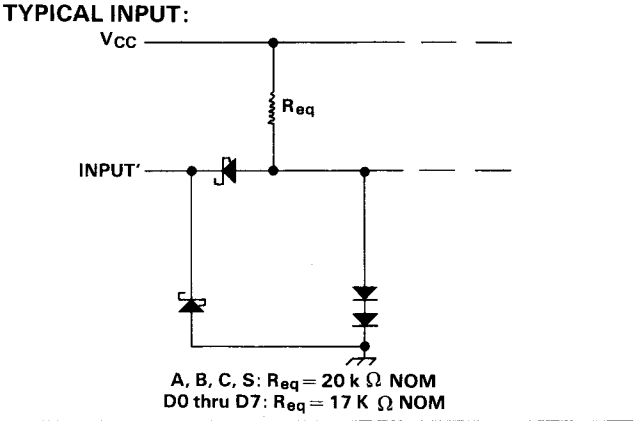
BLOCK DIAGRAM:



BATTERY BACKUP:

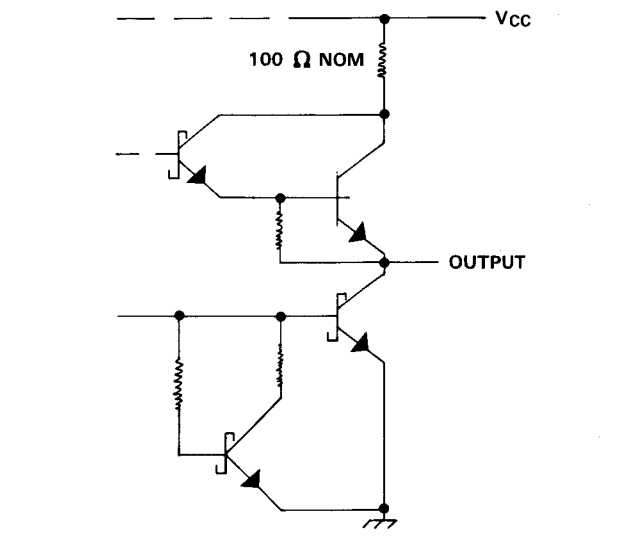


TYPICAL INPUT:



A, B, C, S: R_{eq} = 20 k Ω NOM
D0 thru D7: R_{eq} = 17 K Ω NOM

TYPICAL OUTPUT:



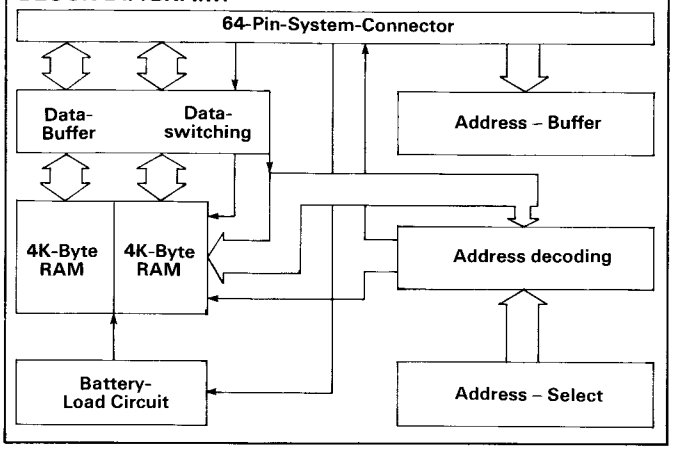
TM990/E251

E-BUS RAM MEMORY EXPANSION MODULE

FEATURES:

- **Up to 8K bytes of Static RAM.**
- **Compatible with NMOS or CMOS RAMS.**
- **BATTERY BACKUP option, on or off board.**
- **MINIMUM 350 HOURS data retention with CMOS RAMS and on board 70 mAH Battery.**
- **8 or 16 bit Data width.**
- **Selectable number of Wait States.**
- **Mappable anywhere in E-BUS 1Mbyte SYSTEM RAM.**
- **E-BUS COMPATIBLE, DIN 41612 Connector.**
- **0–70°C temperature range, for HARSH INDUSTRIAL ENVIRONMENTS.**
- **100 mm × 160 mm COMPACT single eurocard format.**
- **Factory Burnt in for RELIABILITY.**

BLOCK DIAGRAM:



DESCRIPTION:

The TM990/251 is a RAM memory expansion memory (RME) module designed to work with TI's popular range of E-BUS eurocard standard MICROCOMPUTERS. The E-BUS system 20 bit address range is fully decoded on board by means of Dual-In-Line (DIL) switches, giving a start address alterable in 2Kbyte steps. Standalone system operation is facilitated by the use of the E-BUS PRES- signal to protect on board data during power-up, power-down and 'brown-out' sequences. Two different mechanisms to provide non-volatile data storage are provided; the first uses the +5 VSTBY supply rails provided by the E-BUS backplane (the user must ensure his power supply will provide this standby supply during primary supply failure). Alternatively the user may use plug compatible CMOS RAMS, in which case the optional on board battery will provide backup. The selection between +5 VSTBY and on board battery is made via jumpers. The E-BUS connector conforms to DIN 41612 standards for reliability, and a wide range of compatible racking equipment is available for this standard 100 mm × 160 mm single eurocard.

WAIT STATE TABLE:

max. access time from address	max. access time from Chip select	required wait states TM990/E150, 2,5 MHz BUSCLK
440 ns	255 ns	0
840 ns	655 ns	1
1240 ns	1055 ns	2
		TM990/E155 3 MHz BUSCLK-
—	—	0
415 ns	310 ns	1
750 ns	640 ns	2

Required wait states

POWER CONSUMPTION:

Battery: 3,6V NiCd Battery 70 mAH

Power Supply:

	+5V type	+5V max	+5V typ	STBY* max
without RAM	700 mA	1100 mA		
with RAM	960 mA	1400 mA	260 mA	360 mA

*TM990/E251-1

ORDERING INFORMATION

TM990/E251-1 FULLY POPULATED 8Kbyte NMOS RME MODULE, NO BATTERY OR LOAD CIRCUIT.

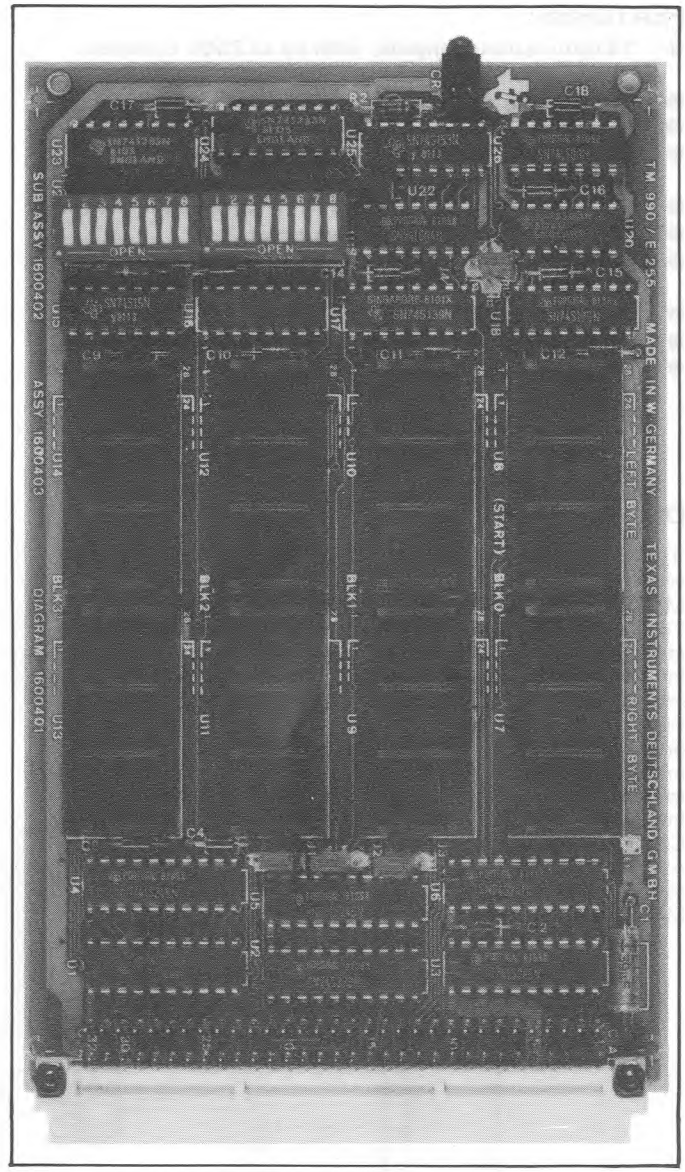
TM990/E251-2 BATTERY AND LOAD CIRCUIT INCLUDED, SOCKETS ONLY FOR UP TO 4 RAM DEVICES.

TM990/E255

EBUS EPROM MEMORY EXPANSION MODULE

FEATURES:

- Up to 64K bytes of EPROM.
- 8 or 16 bit data.
- E-BUS COMPATABLE, DIN 41612 Connector.
- 0–70°C FOR HARSH INDUSTRIAL ENVIRONMENTS.
- 100 mm × 160 mm COMPACT single eurocard.
- Factory burn in for RELIABILITY.
- 20 bit address bus decoding.



Power Supply (typ): ..... + 5V @ 750 mA
— w/o EPROM.

ORDERING INFORMATION:

TM990/E255 SHIPPED WITHOUT EPROM. SOCKETS FOR TMS2516, 2532, 2564 SUPPLIED.

TO BE ANNOUNCED
STOP PRESS

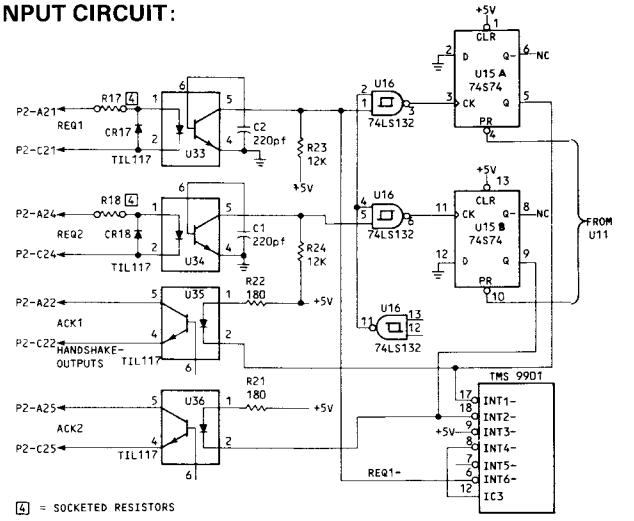
TM990/E350

E-BUS INPUT EXPANSION MODULE

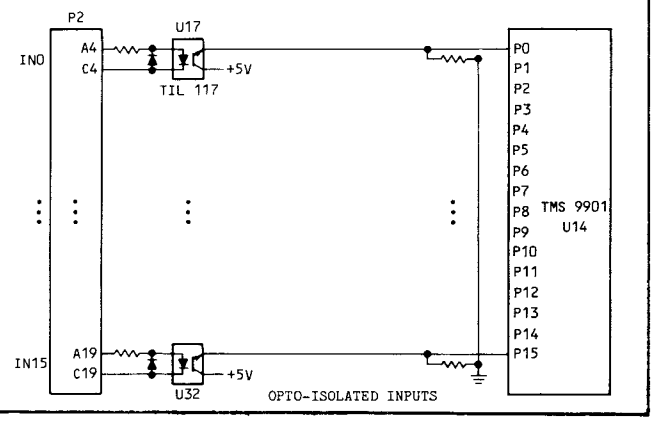
FEATURES:

- **16 opto-isolated inputs, with up to 250V common mode rejection.**
- **2 opto-isolated "handshake" channels.**
- **2 positive EDGE TRIGGERED INTERRUPTS.**
- **PROGRAMMABLE TIMER with up to 420 mS time intervals.**
- **E-BUS COMPATIBLE, DIN 41612 Connector.**
- **DIN 41612 standard I/O Connector.**
- **0–70°C operating temperature range for HARSH INDUSTRIAL ENVIRONMENTS.**
- **Factory burnt in for RELIABILITY.**
- **COMPACT 100 mm × 160 mm single eurocard.**
- **Single 5V supply.**

INPUT CIRCUIT:



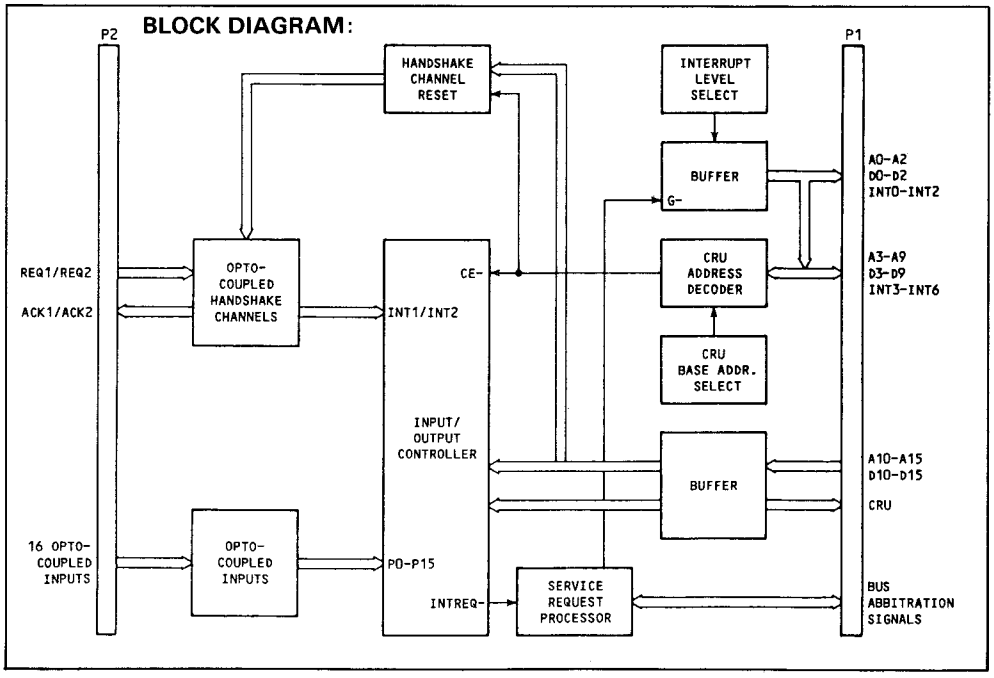
HANDSHAKE CIRCUIT:



DESCRIPTION:

The TM990/350 is an Input Expansion (IE) module designed to work with TI's popular range of E-BUS eurocard standard MICROCOMPUTERS. The 16 input lines are isolated inputs using TIL117 opto-couplers. Either TTL compatible inputs are available as standard or the user may select the version without series resistors factory fitted for almost any required input voltage. The I/O is implemented using TI's unique Command Driven I/O architecture, the Communications Register Unit (CRU), allowing direct access to single or multiple bit inputs without resorting to time-consuming software masking routines or using the E-BUS memory space. The CRU is used to interface with an on board TMS 9901 Programmable System Interface IC, and allows the inputs to be mapped any where in 4Kbit CRU address space through the use of Dual-In-Line (DIP) switches. Additionally the E-BUS SYSTEM interrupt scheme is implemented allowing the interrupts generated to be routed to any one of 8 E-BUS Multi-microcomputers.

BLOCK DIAGRAM:



ORDERING INFORMATION:

TM990/E350-1 FULLY POPULATED, TTL INPUT LEVELS.

TM990/E350-2 NON-TTL INPUT OPTION, NO SERIES LIMITING INPUT RESISTORS SUPPLIED.

TM990/E351

E-BUS OUTPUT EXPANSION MODULE

FEATURES:

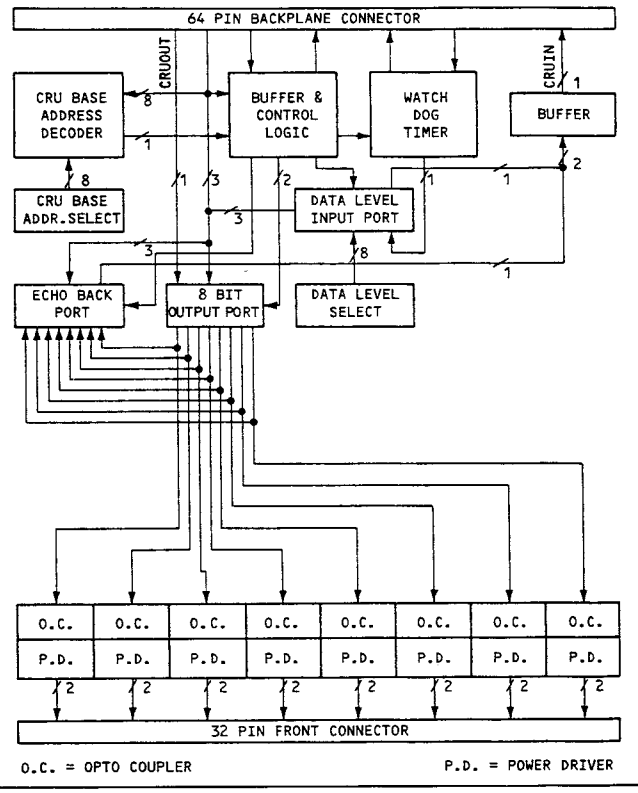
- **8 opto-isolated power outputs.**
- **1.2 Amp drive capability each.**
- **On board dual WATCHDOG TIMER.**
- **Echoback logic for SELTESTING.**
- **8-bit constant input DIP switch.**
- **E-BUS COMPATIBLE, DIN 41612 connector.**
- **DIN 41612 I/O connector (P2).**
- **0–70°C operating temperature range for HARSH INDUSTRIAL ENVIRONMENTS.**
- **Factory BURNT IN, for REALIABILITY.**
- **COMPACT 100 mm × 160 mm single eurocard.**
- **Single 5V supply rail.**

DESCRIPTION:

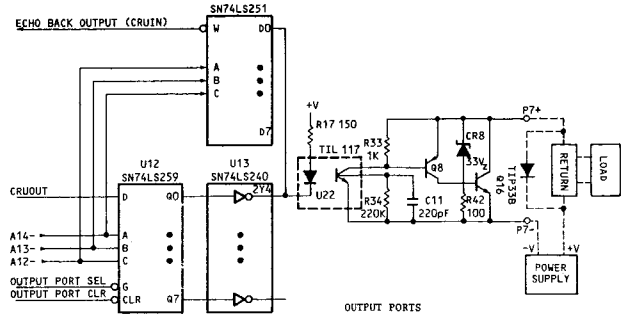
The TM990/E351 is an Output Expansion (OE) module designed to work with TI's popular range of E-BUS standard MICROPROCESSORS. The eight output lines are all opto-isolated, giving 500V isolation between two channels or ground, feature a 1.2 Amp DC sink capability using rugged TIP33 power transistors. Withstanding voltages of up to 30, these outputs are ideal for direct drive of relays, lamps, or motors in 5 to 24V systems. The outputs are implemented using TI's unique command driven I/O architecture, the Communications Register Unit (CRU), allowing direct access, in a single instruction, to single or multiple bits of output, without resorting to time consuming software masking routines.

The on board WATCHDOG TIMER provides the user with a powerful tool to identify corrupt program sequences and thus protect the system interfaces and attached peripherals from malfunction. The TM990/E351 has two timeouts, the first is started after reset, giving a 20 mS period after which a PWRFAIL- or LOAD- interrupt (jumper selectable) is generated so the system is given the chance to re-initialise. Whether the outputs are reset at this stage is jumper selectable. The second timeout, of 10 mS, starts after the first, and if not reset will cause a system HOLD by asserting GRANTOUT (jumper selectable). Once in HOLD the system can only be restarted with a SYSTEM-RESET.

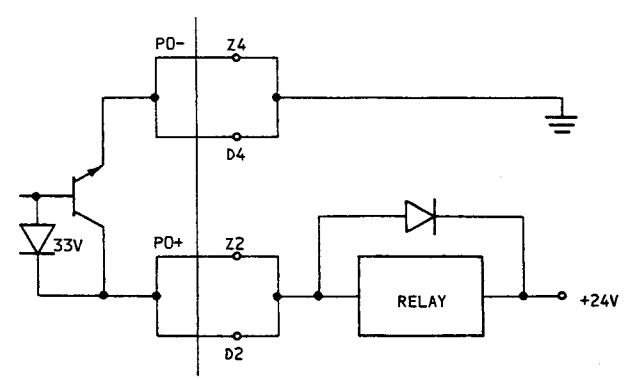
BLOCK DIAGRAM:



OUTPUT DRIVER CIRCUIT:



DRIVING A 24V RELAY:



ORDERING INFORMATION:

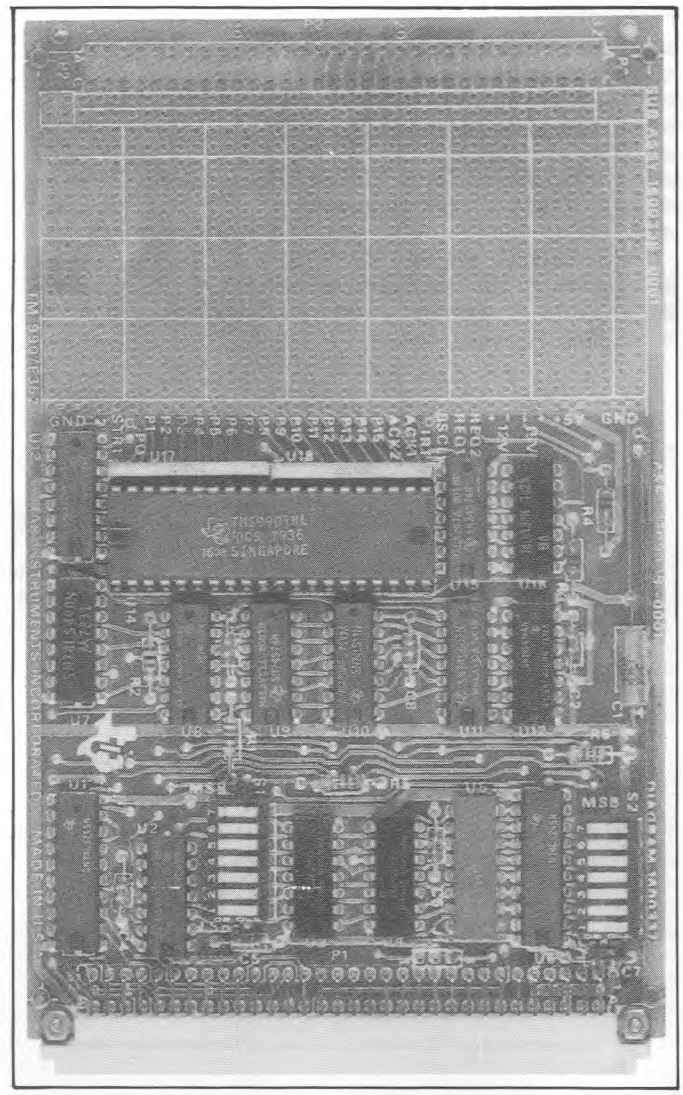
TM990/E351-1	Fully populated with DIP constant switch and timer and manuals.
TM990/E351-2	OEM version, no manuals, DIP switch or timer.

TM990/E352

E BUS UNIVERSAL I/O MODULE

FEATURES:

- 16 TTL Compatible I/O lines.
- 2 'HANDSHAKE' lines.
- 37 × 19 hole PHOTOTYPING AREA.
- PROGRAMMABLE TIMER with up to 420 mS interval.
- EBUS COMPATIBLE, DIN 41612 Connector.
- 0–70°C Operating temperature and 0–95%. Humidity (non-condensing) FOR HARSH INDUSTRIAL ENVIRONMENTS.
- Factory burnt in for RELIABILITY.
- COMPACT 100 mm × 160 mm single eurocard.
- Single 5V supply.



Power Supply (typ): ..... 5V @ 600 mA

ORDERING INFORMATION

TM990/E352 UNIVERSAL INPUT/OUTPUT MODULE

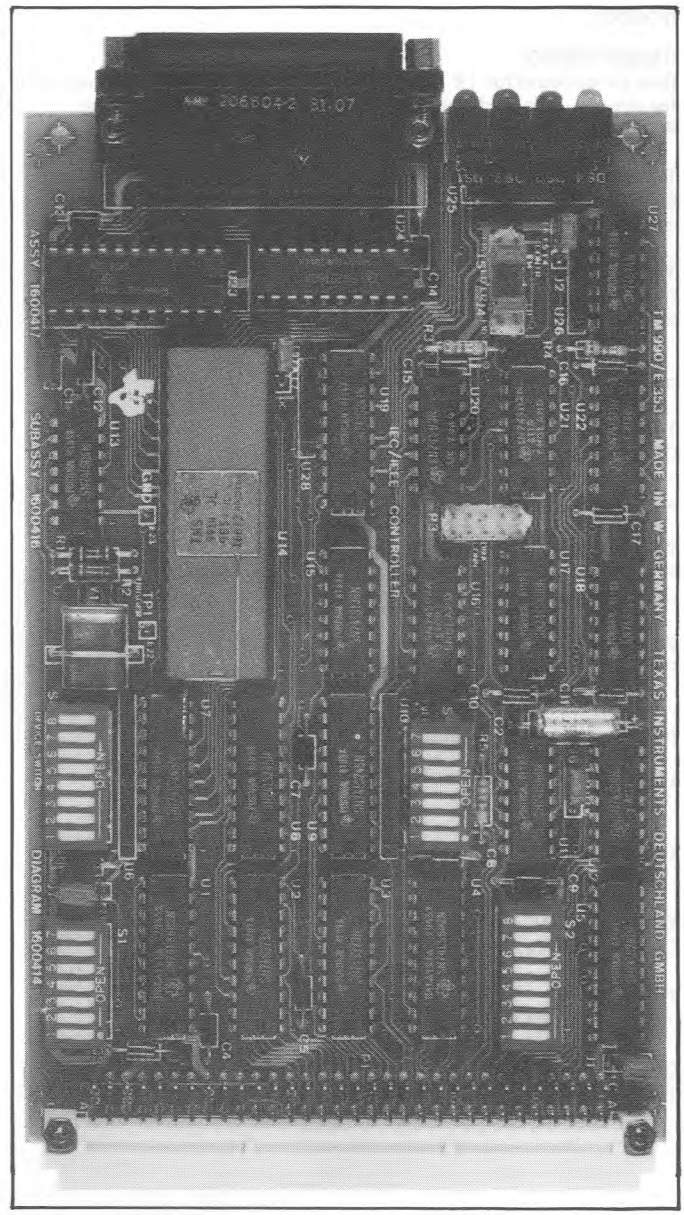
TO BE ANNOUNCED
STOP PRESS

TM990/E353

IEEE 488 ('GPIB') BUS INTERFACE

FEATURES:

- Conforms to 1975/78 IEEE 488 SPECIFICATION.
- LISTENER, TALKER AND CONTROLLER FUNCTIONS.
- Automatic Send/Receive handshake.
- Interface for DMA operation.
- Status LED's for REN, SRG, DAV, CONTROL.
- IEC 6622 connector to IEEE BUS.
- Up to 250 KBS OPERATION.
- Memory MAPPED.
- EBUS Computable, DIN 41612 connector.
- 0–70°C operating temperature range, FOR HARSH INDUSTRIAL ENVIRONMENTS.
- Factory burnt in for RELIABILITY.
- Compact 100 mm × 160 mm single eurocard.
- Single 5V supply rail.



Power Supply: (typ) .....5V @ 750 mA

ORDERING INFORMATION:

TM990/E353 GPIB BUS INTERFACE MODULE.

TO BE ANNOUNCED
STOP PRESS

E-BUS ACCESSORIES

Boards

TM990/E5000
Rear panel board for 19" housing with 12 plug positions; connections for power supply and several control lines, with watchdog timer. Plug type: DIN 41612.

TM990/E5011
Extender Board. Makes it possible to operate boards outside the chassis for testing and checking purposes.

TM990/E5013
Prototype board for wire-wrap circuits. Prefabricated board in European format with E-BUS-connection for user-specific circuitry.

Power Packs

TM990/518
OEM power pack (open chassis) +5V/6.0A, +12V/0.9A, −12V/0.9A, −45V/0.1A. Overvoltage protection at +5V, current limiter for +5V and +12V.

TM990/518A
Power Pack (cased) +5V/4.0A, +12V/0.6A, −12V/0.4A, +45V/0.1A, otherwise like TM990/518.

TM990/519
Power Pack (cased), +5V/2A, +12V/0.35A, −12V/0.2A.

Accessories: Cable

TM990/502
I/O connector cable.

TM990/503
I/O connector cable for 743 KSR/745 terminals.

TM990/504
Connector cable.

TM990/505
I/O connector cable for 733 ASR.

OTHER:
TM990/E50004 – 4 slot (3V) chassis.

FEATURES:

- **Provides a standard electrical and mechanical connection.**
- **Flexibility provides a wide range of configurations.**
- **Easy to interface from custom boards.**
- **CRU interfacing.**
- **DMA capability.**
- **20 bit address bus allows up to 1M Byte addressing capability.**
- **28 lines for power and ground.**
- **20 lines for address bus.**
- **16 lines for the data bus.**
- **18 lines for bus control.**
- **15 lines for prioritised interrupts.**
- **3 lines for CRU interfacing.**

DESCRIPTION:

Power Bus:- 4 lines for +5V, 2 lines for +12V, 2 lines −12V, 2 lines for battery voltage, 2 lines for auxillary voltage and 16 lines for ground.

Address Bus:- 16 lines of basic address space, 4 lines of extended addressing giving 1MByte memory address range. Can address CRU locations, and is controlled by the bus master, the bus isn't terminated on the back plane.

Data Bus:- 16 lines for data, used to transfer data between processors, memory and peripherals. It is controlled by the current bus master and is not terminated on the back plane.

CRU Bus:- Used for serial data transfer, 3 lines provide separate information paths, CRUIN serial input line, CRUOUT serial output line, CRUCLK clock signal gating data.

Interrupt Bus:- Fifteen lines allows each level of prioritized interrupts.

Control Bus:- 15 separate lines to control data transfers and system synch 4 memory control signals MEMEN, MEMCYC, DBIN and READY which indicate bus contains a valid memory address, memory cycle in progress, data bus inputting data and memory will be ready to complete its memory access, respectively.

2 timing and sync signals, BUSCLK and REFCLK, both generated by the master processor to cause sync of memory and bus cycles and timing reference to I/O devices respectively.

5 bus arbitration signals HOLD, HOLDA, BUSY, GRANTIN, GRANTOUT. Which indicate a device is requesting the bus for data transfer, bus master has relinquished control of the bus to the requesting device, requesting device has taken bus, no device with higher priority is requesting the bus, and that a lower priority device may request control of the bus, respectively. GRANTIN and GRANTOUT form a daisy chain priority scheme for transfering bus control.

4 miscellaneous signals:- IORST, PRES, RESTART, IAQ, which indicate to the system that a system reset is in progress to the I/O devices, power supply has stabilised and processor can begin execution, a load function should be performed and an instruction fetch is being performed by the processor respectively.

TM990 SYSTEM BUS PIN DEFINITION

PIN	SIGNAL	GROUP	PIN	SIGNAL	GROUP
1	GND	Power/Ground	2	GND	Power/Ground
3	+5V		4	+5V	
5	$\overline{INT8}$		6	$\overline{INT7}$	
7	$\overline{INT10}$		8	$\overline{INT9}$	
9	$\overline{INT12}$		10	$\overline{INT11}$	
11	$\overline{INT14}$	Interrupt	12	$\overline{INT13}$	Interrupt
13	$\overline{INT2}$		14	$\overline{INT15}$	
15	$\overline{INT3}$		16	$\overline{INT1}$	
17	$\overline{INT5}$		18	$\overline{INT4}$	
19	IAQ	Control Bus	20	$\overline{INT6}$	
21	GND		22	$\overline{BUSCLK}$	
23	GND		24	$\overline{REFCLK}$	
25	GND	Power/Ground	26	RESERVED	
27	GND		28	RESERVED	
29	CRUIN		30	CRUOUT	CRU Bus
31	GND		32	BUSY	Control Bus
33	D0		34	D1	
35	D2		36	D3	
37	D4		38	D5	
39	D6	Data Bus	40	D7	Data Bus
41	D8		42	D9	
43	D10		44	D11	
45	D12		46	D13	
47	D14		48	D15	
49	VAUX		50	VAUX	Power/Ground
51	VBATT	Power/Ground	52	VBATT	
53	XA0		54	XA1	
55	XA2		56	XA3	
57	A0		58	A1	
59	A2		60	A3	
61	A4		62	A5	
63	A6	Address Bus	64	A7	Address Bus
65	A8		66	A9	
67	A10		68	A11	
69	A12		70	A13	
71	A14		72	A15	
73	−12V		74	−12V	Power/Ground
75	+12V		76	+12V	
77	GND	Power/Ground	78	$\overline{WE}$	
79	GND		80	$\overline{MEMEN}$	
81	GND		82	$\overline{DBIN}$	
83	GND		84	$\overline{MEMCYC}$	
85	GND		86	$\overline{HOLDA}$	
87	$\overline{CRUCLK}$	CRU Bus	88	$\overline{IORST}$	Control Bus
89	GND		90	READY	
91	GND	Power/Ground	92	$\overline{HOLD}$	
93	RESTART	Control Bus	94	$\overline{PRES}$	
95	$\overline{GRANTOUT}$		96	$\overline{GRANTIN}$	
97	+5V	Power/Ground	98	+5V	Power/Ground
99	GND		100	GND	

TM990/204

T-BUS CMOS RAM MODULE

TM990/204 NONVOLATILE RAM MODULE

FEATURES:

- Bus compatible with TM990/10X or TM990/1481.
- Choice of 4, 8 or 16KB on-board CMOS RAM.
- On-board battery with charger.
- Data retention.

	Mem Size	Retention Min	Retention Typical
TM990/204-1	4KB	408 hrs	37 days
TM990/204-2	8KB	240 hrs	34 days
TM990/204-3	16KB	120 hrs	30 days

- Memory assignable at 4KB boundaries in 1MB space.
- Memory write protection and execute protection by switch accessible at the front panel.
- Execute or memory protect interrupt level selection.
- LEDS at the front edge indicating:
  - Execute protect violation.
  - Write protect violation.
  - User defined indication.

TM990/602

SYSTEM HARDWARE KIT

TM990/602 SYSTEM HARDWARE KIT

FEATURES:

- User configurable consumable development system.
- Can run UCSD-P system.
- Pre-configured and tested for operation with:
  - SA800/801, SA400, CDC9494B and QUME DT/8 drives
  - EIA Terminal – ADM-3 or equivalent.
- Includes the following components:

– TM990/101MA-3	μC MODULE
– TM990/203-23	64KB DRAM
– TM990/303A	Floppy disk drive controller
– TM990/522	System enclosure
– TM990/527	Cable to connect two standard disk drives
– TM990/538	EIA extension cable

TO BE ANNOUNCED
STOP PRESS

TM990/601

SYSTEM HARDWARE KIT

TM990/601 SYSTEM HARDWARE KIT

FEATURES:

- User configurable consumable development system.
- Can run either UCSD-P system or SDD development system software.
- Pre-configured and tested for operation with:
  - SA800/801, CDC9404B and QUME DT/8 drives.
  - EIA terminal – ADM-3 or equivalent.
- Includes the following components.
  - TM990/101MA μC module 2 asynchronous ports
  - TM990/203-23 64KB dram
  - TM990/303A Floppy disk drive controller
  - TM990/510 4 Slot card cage
  - TM990/527 Cable to connect two standard disk

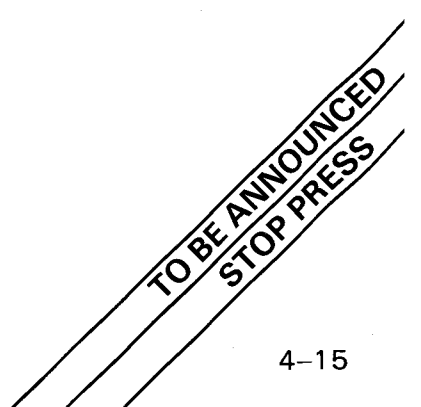
TMSW 600P

UCSD PASCAL DEVELOPMENT SOFTWARE

TMSW 600P UCSD-P DEVELOPMENT SOFTWARE

FEATURES:

- Provides complete S/W development environment.
  - UCSD Pascal Compiler
  - TMS9900 Assembler
  - Editor
    Screen/Line oriented
  - File handler
- Wide spread use gives access to large library of UCSD Pascal Programs.
- Increases programmer productivity via ease of use.
- Offers portability of software.
- Simplifies program design.
- Lowers maintenance cost.
- Extends utility of the language via pre-programmed units.
- Links Pascal Programs with assembler.
- Provides multi-programming.



TM990/CXXX

CONFORMALLY COATED BOARDS

FEATURES:

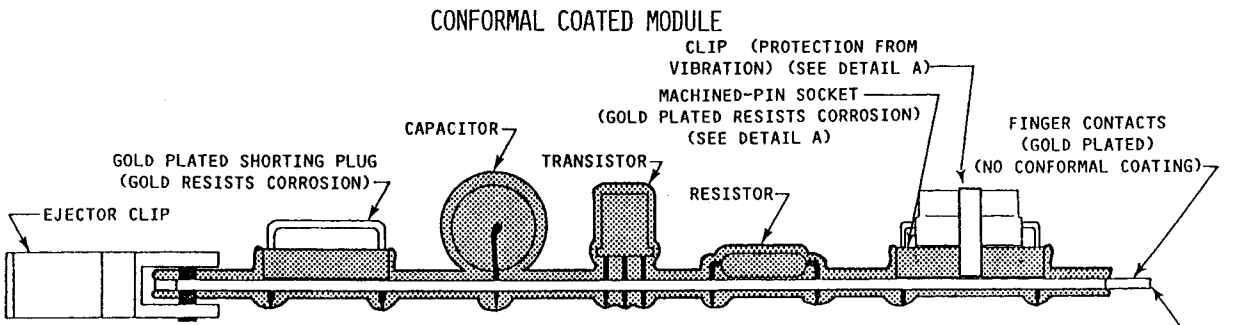
- **Conformal coating – providing:**
  - **– Excellent corrosion resistance**
  - **– Fungal and particulate resistance**
- **Tougher temperature specs 0–70°C ambient operation.**
- **High quality control standards.**
- **Use of gold plated machined-pin sockets.**
- **ICS soldered directly to the board.**

RANGE:

TM990/C101MA	CPU with 8KB EPROM, Sockets, 4KB RAM
TM990/C201	Memory module, up to 32KB EPROM, 16KB CMOS RAM
TM990/C307	Quad Serial I/O module
TM990/C308	Industrial HDLC module
TM990/C311	48 bits I/O module

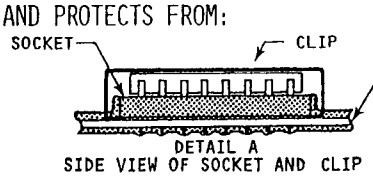
INDUSTRIAL GRADE MODULES REQUIREMENTS

ENVIRONMENTS	TYPICAL INDUSTRIES/EXAMPLES
● Dusty	Saw mills Grain processing Cement factories Petrochemical (sand)
● Corrosive	Petrochemical Oil drilling (sea)
● Humid	Off shore drilling Tropical environment Open environment
● Electrically noisy environment	Mills Machine shops Heavy electrical
● High temperature	Steel mills Uncontrolled environment
● Shocks and vibration	Trucks/Locomotive Ap. Machine tool control Avionics



SHADED AREA IS CONFORMAL COATING WHICH INSULATES AND PROTECTS FROM:

- CORROSION
- MOISTURE
- DUST
- FUNGAL GROWTH



TO BE ANNOUNCED
STOP PRESS

TM990/100MA

T-BUS MICROCOMPUTER

FEATURES:

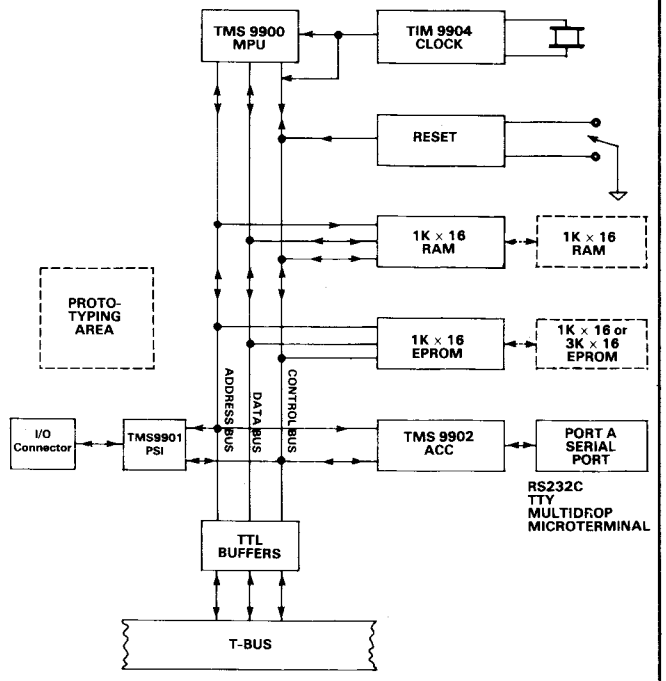
- **3 MHz TMS 9900 16 Bit CPU.**
- **Up to 4K bytes of 2114 Static RAM.**
- **Up to 8K bytes of 2716 EPROM or ROM.**
- **EIA/TTY/Multidrop synchronous port.**
- **16 TTL programmable I/O and Interrupts.**
- **2 programmable timers.**
- **Prototyping area for custom applications.**
- **Fully compatible with "T-BUS".**
- **0–70°C temperature range for harsh industrial environments.**
- **Factory burnt-in for reliability.**

DESCRIPTION:

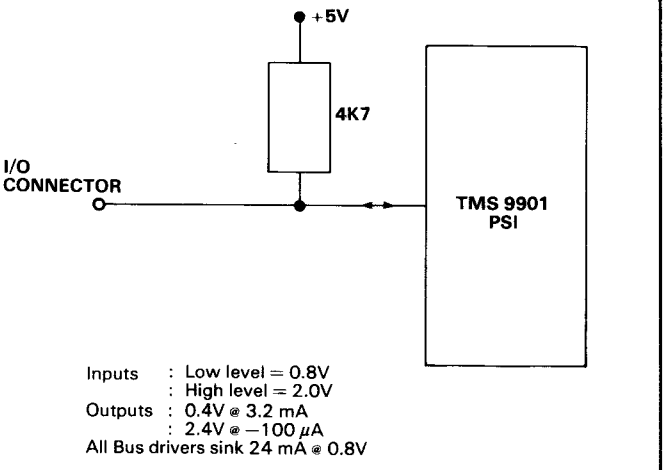
This complete Microcomputer board contains sockets for up to 4 EPROMS (either TMS 2708 or TMS 2716) and up to 8 RAMS (TMS 4014 or 2114). Memory map options are provided to allow the RAM area to be mapped in either to the high or to the low end of memory. DMA facilities are provided for off-board memory. 16 TTL input/output lines are provided by the TMS 9901 and any of these inputs can be configured to cause an INTERRUPT. Interrupts can be generated by signals from the T-BUS and all are individually maskable.

A variety of SERIAL input/output methods are supported, including EIA, 20 mA neutral current loop TTY and Private Wire Differential line driver/receiver. If required, the TMS 9902 can be replaced by the plug compatible TMS 9903 to provide synchronous serial communication. Each TMS 9901 or TMS 9902 also has an on-chip Timer which is available for use, and may be configured as an EVENT COUNTER in the case of the TMS 9901. Full CRU expansion facilities are implemented to allow a maximum of 4096 inputs and outputs. A large prototyping area is provided on the board to allow customisation of the board for specific projects. The area is large enough to accommodate one 40-pin DIP (0.6 inch centres) plus four 16-pin DIP's (0.3 inch centres), and many signal lines are made available at the edge of the prototyping area.

BLOCK DIAGRAM:

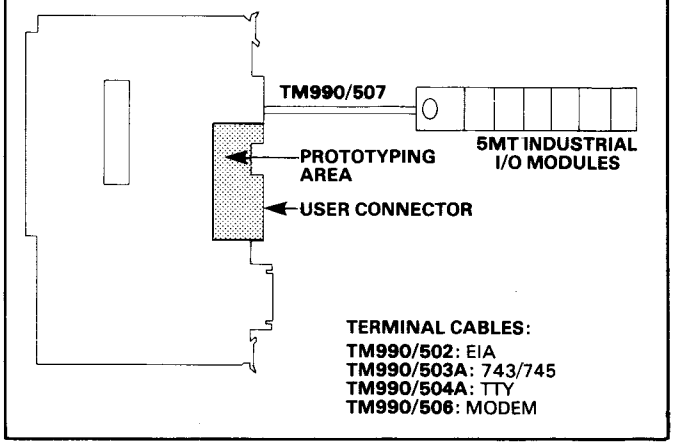


INPUT/OUTPUT SCHEMATIC:



Inputs : Low level = 0.8V
: High level = 2.0V
Outputs : 0.4V @ 3.2 mA
: 2.4V @ −100 μA
All Bus drivers sink 24 mA @ 0.8V

CONNECTORS:



TERMINAL CABLES:
TM990/502: EIA
TM990/503A: 743/745
TM990/504A: TTY
TM990/506: MODEM

TYPICAL POWER REQUIREMENTS:

	TM990/100MA-1	TM990/100MA-2
× 5V ± 3%	1.2 A	1.4 A
×12V ± 3%	0.2 A	0.1 A
−12V ± 3%	0.1 A	0.1 A

ORDERING INFORMATION:

Part number	EPROM	RAM
TM990/100MA-1	2 x 2708 with TIBUG monitor	4 x 2114 (2Kbytes)
TM990/100MA-2	2 x 2716 Blank	8 x 2114 (4Kbytes)

TM990/101MA

T-BUS MICROCOMPUTER

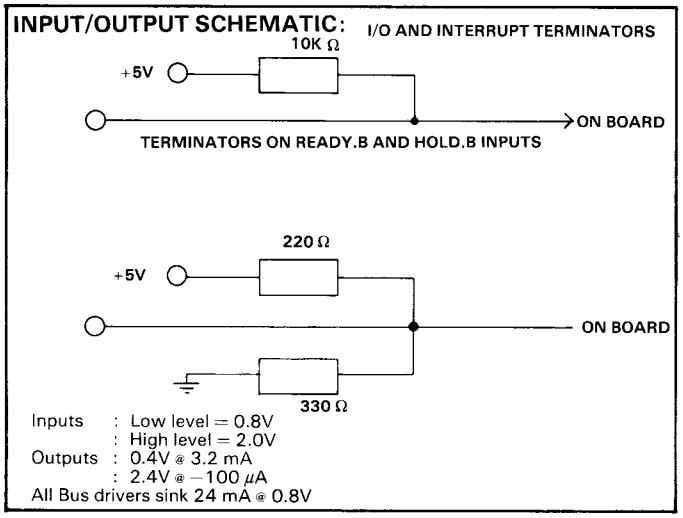
FEATURES:

- 3 MHz TMS 9900 16 Bit CPU.
- 4K bytes of 2114 Static RAM.
- 8K bytes of 2716 EPROM or ROM.
- 2 EIA/TTY asynchronous ports.
- 16 TTL programmable I/O and Interrupts.
- 3 programmable timers.
- Fully compatible with "T-BUS".
- 0–70°C temperature range.
- Factory burnt-in.

DESCRIPTION:

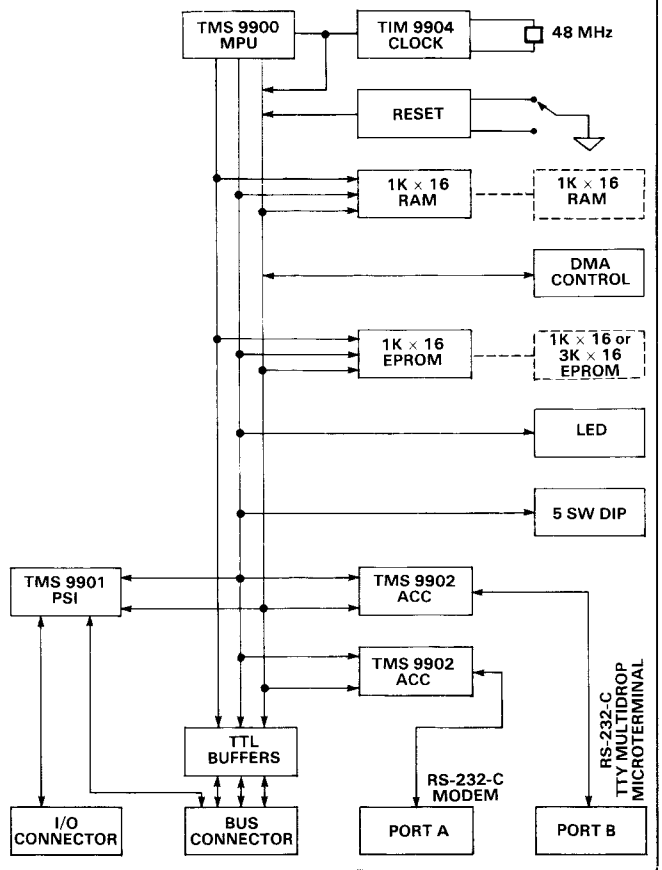
This complete Microcomputer board contains sockets for up to 4 EPROMS (either TMS 2708 or TMS 2716) and up to 8 RAMS (TMS 4014 or 2114). Memory Map options are provided to allow the RAM area to be mapped in either to the high or to the low end of the memory. Full DMA facilities are provided, both to on-board and off-board memory. 16 TTL input/output lines are provided by the TMS 9901 and any of these inputs can be configured to cause an INTERRUPT. Interrupts can be generated by signals from the T-BUS and all interrupts are individually maskable. Interrupt level 6 is also provided with EDGE DETECTION logic to allow for either positive or negative edge triggering. A variety of SERIAL input/output methods are supported by the two ports, including EIA, 20 mA neutral current loop TTY (port A only), Differential line driver/receiver (port A only) and Series 102 and 103 Modems (port B only). If required the TMS 9902 can be replaced by the plug compatible TMS 9903 to provide synchronous serial communication. Each TMS 9901 or TMS 9902 also has an on-chip TIMER which is available for use, and may be configured as an EVENT COUNTER in the case of the TMS 9901. Full CRU expansion facilities are implemented to allow a maximum of 4096 inputs and outputs.

INPUT/OUTPUT SCHEMATIC:

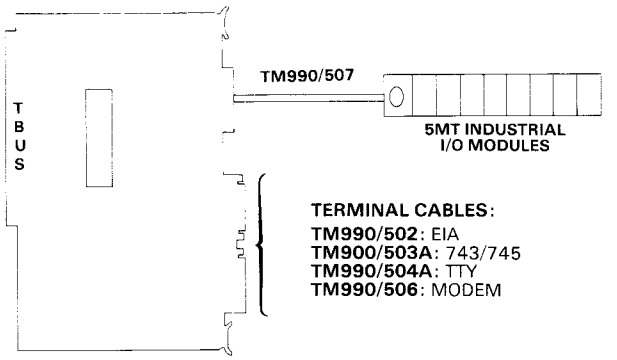


Inputs : Low level = 0.8V
: High level = 2.0V
Outputs : 0.4V @ 3.2 mA
: 2.4V @ −100 μA
All Bus drivers sink 24 mA @ 0.8V

BLOCK DIAGRAM:



CONNECTORS:



TYPICAL POWER REQUIREMENTS:

	101MA-1	101MA-2	101MA-3
Vcc × 5V ± 3%	1.8 A	1.8 A	1.8 A
Vdd × 12V ± 3%	0.3 A	0.3 A	0.4 A
Vaa −12V ± 3%	0.2 A	0.2 A	0.2 A

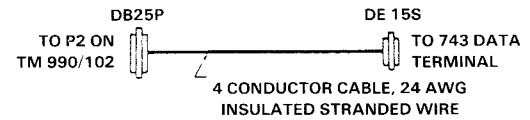
ORDERING INFORMATION:

Part number	EPROM	RAM	Port A option
TM990/101MA-1	2 × 2708 with TIBUG monitor	4 × 2114 (2Kbytes)	TTY/EIA
TM990/101MA-2	2 × 2716 Blank	4 × 2114 (2Kbytes)	EIA/MD
TM990/101MA-3	4 × 2716 Blank	8 × 2114 (4Kbytes)	TTY/EIA
TM990/101MA-10	4 × 2716 with POWER BASIC	4 × 2114 (2Kbytes)	TTY/EIA

FEATURES:

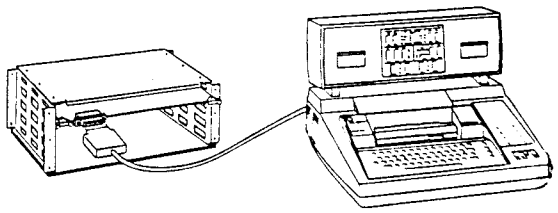
- 3 MHz 9900 CPU.
- Up to 128K bytes on board RAM.
- Up to 16K bytes on board EPROM.
- Optional TM 990/404 mapping monitor.
- Off board memory expansion to 1 mbyte.
- 2 interval timers.
- EIA RS232-C serial port, programmable from 110 to 19200 BAVD.
- On board 99610 memory mapper.
- On board TMS 4500 refresh controller.

CONNECTOR P2 CONNECTED TO MODEL 733 ASR

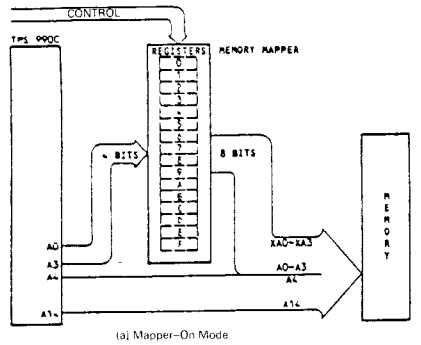


CONNECTIONS		
PIN ON DE 15S	PIN ON DB25P	SIGNAL
13	2	XMIT
12	3	RECV
11	8	DCD
1	7	GND

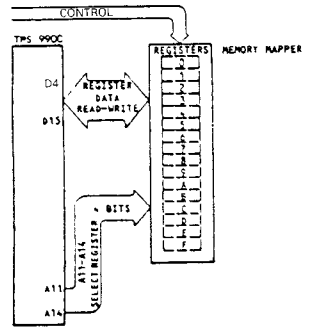
743 KSR TERMINAL CABLE



BLOCK DIAGRAM USING THE MEMORY MAPPER

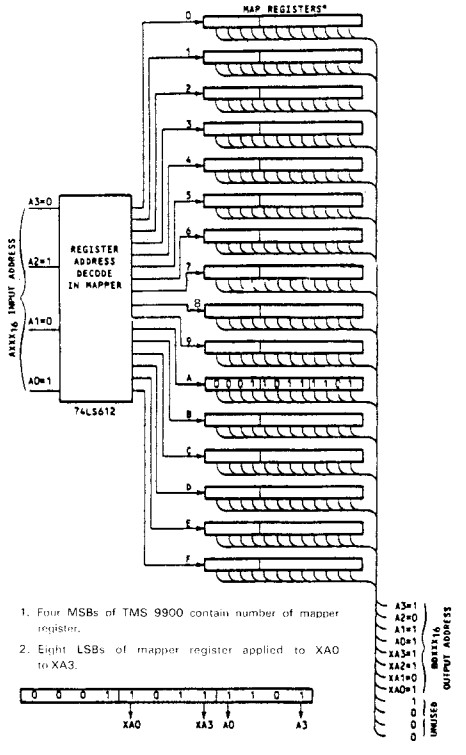


(a) Mapper-On Mode



(b) Register-Access Mode

MAPPER REGISTER SELECTION



*EACH REGISTER ADDRESSES 4K BYTES

ENVIRONMENTAL SPECIFICATIONS: (TENTATIVE)

OPERATING TEMPERATURE RANGE: 0–70°C
HUMIDITY: 5 to 95%, non-condensing.
STORAGE TEMPERATURE RANGE: −40° – +85°C.
SHOCK: 2 inch vertical drop.
VIBRATION: 1g @ 5 to 80 Mz.
0.3g @ 80 to 500 Mz.

POWER CONSUMPTION:

	+5V		+12V		−12V	
	Typ	Max	Typ	Max	Typ	Max
TM 990/102-1	1.7	2.0	0.3	0.5	0.25	0.40
TM 990/102-2	1.9	2.0	0.3	0.5	0.25	0.40
TM 990/102-3	1.9	2.0	0.3	0.5	0.25	0.40

ORDERING INFORMATION:

TM990/102-1
TM990/102-2
TM990/102-3

TO BE ANNOUNCED

TM990/180M

T-BUS MICROCOMPUTER

FEATURES:

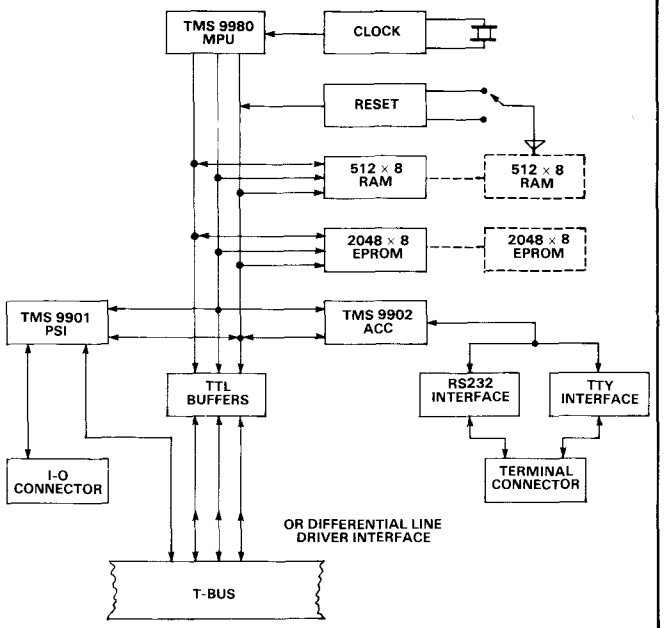
- **TMS 9980 16 bit CPU.**
- **Up to 1K bytes of static RAM.**
- **ZUp to 4K bytes of EPROM.**
- **EIA/TTY asynchronous ports.**
- **16 TTL programmable I/O and Interrupts.**
- **2 programmable timers.**
- **Prototyping area for custom applications.**
- **0–70°C temperature range.**
- **Factory burnt-in**

DESCRIPTION:

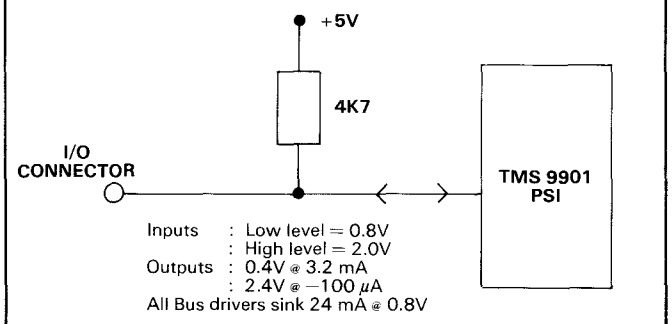
The TM990/180M microcomputer module is a software compatible member of the TM990 family. The TMS 9980 is used as a CPU to provide a 16 bit processor at 2.5 MHz operation. All six levels of prioritised interrupts are available for use and the board contains sockets for up to 4 EPROMS (TMS 2708) and up to 8 RAMS (TMS 4042). DMA control lines are available for use off-board. 16 TTL input/output lines are provided by the TMS 9901 and any of these inputs can be configured to cause an INTERRUPT. Interrupts can be generated by signals from the T-BUS and all interrupts are individually maskable. The serial port can be configured either for an EIA type interface or for 20 mA neutral current loop TTY. The TMS 9902 can be replaced by the plug compatible TMS 9903 to provide synchronous serial communication.

Each TMS 9901 or TMS 9902 also has an on-chip TIMER which is available for use, and may be configured as an EVENT COUNTER in the case of the TMS 9901. Full CRU expansion is available up to a maximum of 2048 inputs and outputs, but this board is not compatible with memory expansion modules or memory mapped peripheral boards. A large prototyping area is provided on the board to allow customisation of the board for specific projects. The area is large enough to accommodate one 40-pin DIP (0.6 inch centres) plus four 16-pin (0.3 inch centres) and many signal lines are made available at the edge of the prototyping area.

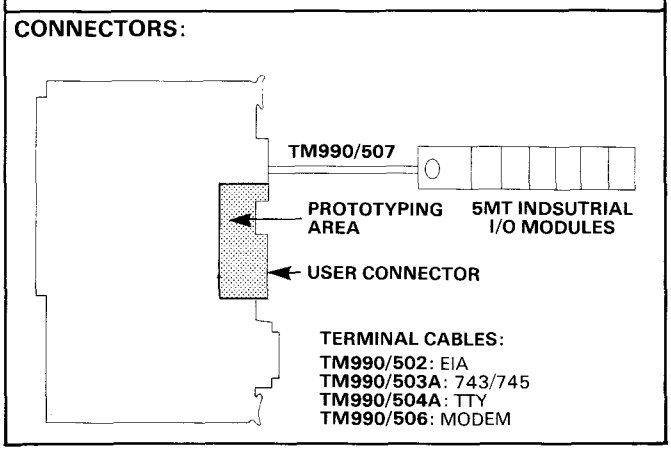
BLOCK DIAGRAM:



TYPICAL INPUT/OUTPUT SCHEMATIC:



CONNECTORS:



ORDERING INFORMATION:

Part number	EPROM	RAM
TM990/180M-1	2 x 2708 with TIBUG monitor	512 bytes

NOT RECOMMENDED FOR NEW DESIGNS

TM990/189M

UNIVERSITY BOARD

FEATURES:

- **TMS 9980 16 bit CPU.**
- **Up to 2K bytes of static RAM.**
- **Up to 6K bytes of EPROM.**
- **Optional EIA/TTY asynchronous ports.**
- **16 TTL programmable I/O and Interrupts.**
- **Microprocessor tutorial textbook supplied.**
- **Audio cassette interface.**
- **45 Key ALPHANUMERIC keyboard.**
- **Ten digit, psuedo ALPHANUMERIC display.**
- **Visual and acoustic indicators on-board.**

DESCRIPTION:

The TM990/189 is a self-contained, single-board microcomputer system. It is intended for use as a learning aid in the instruction of microcomputer fundamentals, machine and assembly language programming, and microcomputer interfacing. It also demonstrates TMS 9900 family applications and advantages and software compatible with the TMS 9900/990 family. A TMS 9980 is used as the CPU to provide 16 bits of processing power to an 8-bit data bus. An instruction set with the capabilities of full minicomputers and identical to that of the TMS 9900 is featured. The TM990/189 is designed for 2 MHz operation, utilizing the full six levels of prioritized interrupts and the advanced memory-to-memory architecture of the TMS 9980. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility.

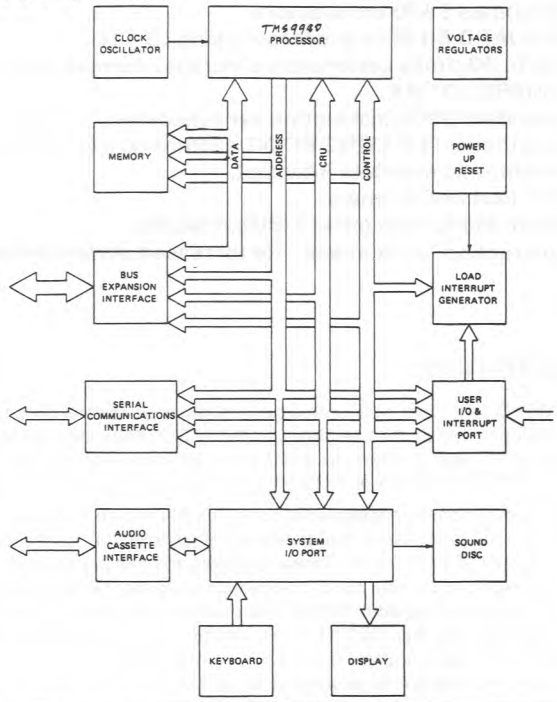
The on-board memory includes both an EPROM/ROM section and a static RAM section. Two sockets are available for TMS 2708, TMS 2716, TMS 2532 EPROM or TMS 4732 ROM operation. By performing a simple board modification, the on-board EPROM may be expanded to 6144 bytes via 1 TMS 2532 and 1 TMS 2716. The static RAM area is populated with 1K bytes of socketed static RAM and contains sockets for an additional 1K bytes of RAM.

The UNIBUG monitor is supplied preprogrammed in TMS 4732 ROM. Fifteen commands and seven subroutines are provided by UNIBUG. Memory inspect/change and CRU inspect/change allow the user to effectively look at memory and CRU addresses. Load and dump commands allow the user to recall and store programs from audio cassette, or paper tape/digital cassette via user supplied data terminal. An execute command is provided to execute an entire program or execute to a breakpoint address where the program is halted. There is a status register inspect/change command along with individual program counter, workspace register and workspace pointer inspect/change commands. The New Line Request command causes a carriage return, line feed and new line request if a terminal is used. When the keyboard is used, a "?" prompt is displayed. Seven utility subroutines allow the user to read and write ASCII or hexadecimal characters to and from a terminal. UNIBUG displays "ERR" on the board when an invalid command is entered or when an invalid termination character is detected.

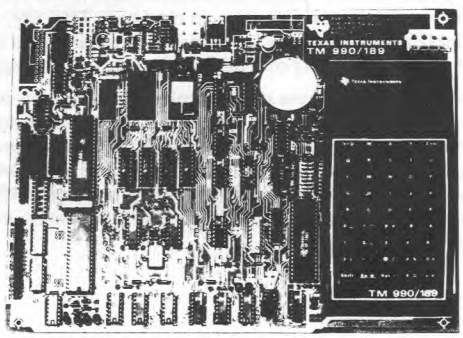
The most powerful feature of the UNIBUG monitor is the symbolic assembler. By interpreting assembly language source statements into object code, the TM990/189 symbolic assembler processes all 69 instructions of the TMS 9980. In addition, the pseudo instruction NOP assemblies as "JMP $+2". Six assembler directives are also featured: AORG, BSS, DATA, END, EQU, TEXT. Comments as well as two character labels can be used with this assembler.

The board has been designed to allow easy expansion of RAM/EPROM or I/O using off-board devices, and the connection of an EIA or TTY, 100 or 300 baud terminal.

BLOCK DIAGRAM:



CONNECTORS:



● Stand-alone educational module for teaching microcomputer fundamentals, machine and assembly language programming, and microcomputer interfacing ● Alpha-numeric keyboard and display ● Complete tutorial text included.

Tutorial Text Chapter Contents

Chapter 1. Overview of Computers, Microprocessors, and Microcomputer
A. Basic Computer Architecture
B. Example of Computer Operation
C. Architectural Enhancements of Microprocessors
D. TMS 9980 Microprocessor Description.

Chapter 2. Arithmetic, Logic, and the Arithmetic Logic Unit
A. Number Systems
B. Arithmetic Logic Unit
C. On-Board Terminal (Terminal on University Board)
D.On-Board Monitor Commands
E. Exercises

Chapter 3. Introduction to Computer Addressing and Program Development
A. Computer Addressing: Explanation of What It Means
B. Instruction Set of Texas Instruments TMS 9980 Microprocessor
C. Programming Example, Exercises, and Lab Experiments.

Chapter 4. Assembly Language
A. Overview of Assembler Functions
B. University Board Symbolic Assembler
C. Directives, Labels
D. Program Example and Lab Experiments

Chapter 5. Memory Systems
A. Description of Memory Systems – Data Buffers, Manipulation, Memory Map
B.Memory Characteristics, Systems
C. Programming an EPROM for the Univeristy Board
D. Program Example and Lab Experiments

Chapter 6. Input/Output Concepts
A. Overview of I/O Operation
B. Program Example and Lab Experiments

Chapter 7. Input/Output Design
A. I/O Interfacing Considerations
B. I/O Peripheral Components
C. Program Example and Lab Experiments

Chapter 8. Modular Programming
A. Definitions and Advantages of Modular Programming
B. Subroutines
C. Program Example and Lab Experiments

Chapter 9. Software Engineering
A. Hardware/Software Tradeoffs
B. Structuring the Software
C. Linking Program Modules
D. Interrupt Servicing
E. Real-Time Considerations
F. Program Example and Lab Experiments

Chapter 10. Product Development
A. Product Overview and Definition
B. System Design and Development
C. Software Development
D. Debugging, Testing, and Development Tools
E. Program Example

ORDERING INFORMATION:

Part number	
TM990/189M	Includes TMS 9980 CPU, UNIBUG monitor in ROM 1K RAM and tutorial textbook
TM990/189K-1	Optional expansion kit including EIA expansion, off-board memory, control and data bus buffers, and on-board cassette relay
TM990/189K-2	Optional expansion kit to fully expand RAM to 2K bytes
TM990/469	University BASIC EPROM kit – Integer version of TI's POWER BASIC complete with colour graphics commands for use with TMS 9918 VDP (not supplied)

TM990/1481

T-BUS BIT-SLICE PROCESSOR BOARD

FEATURES:

- **Emulates 9900 architecture.**
- **2 BOARD Bit Slice processor using LS TTL.**
- **Up to 40 times performance increase compared with TM990/101MA.**
- **Standard 9900 instruction set supported.**
- **Additional FLOATING POINT arithmetic instructions.**
- **Arithmetic overflow interrupt.**
- **EIA Port and 2 timers.**
- **Compatible with other T-BUS modules.**
- **Instruction "look ahead" for increased performance.**

DESCRIPTION:

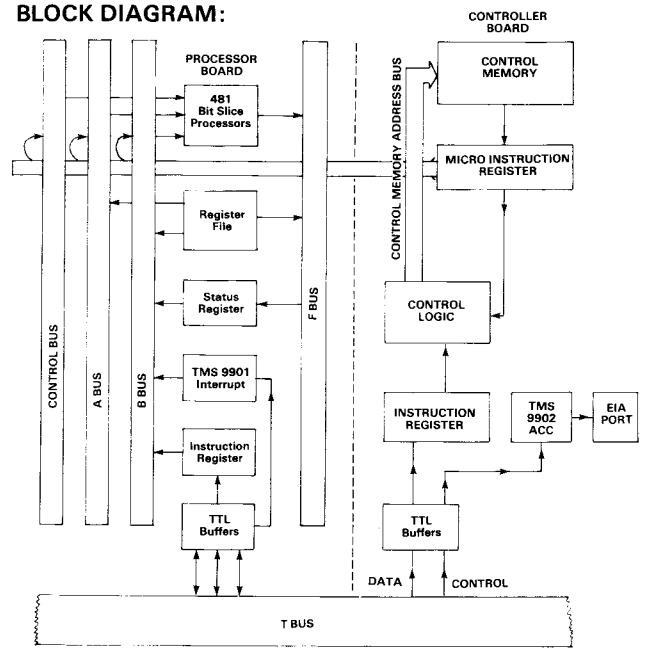
The TM990/1481 is a high-speed general purpose central processing unit, implemented on two modules, utilizing Schottky and low power Schottky TTL logic. It offers up to 40 times performance improvement over the TM900/100MA or TM990/101MA single-board computers.

The processor board is designed around TI's SN74S481 bit-slice processor. The processor's major operating registers are contained within the SN74S481 chips. These registers are: the program counter (PC), the memory counter (MC), the working register (WR), and the extended working register (XWR). This module also contains the status register, register file (R0–R15), and the instruction register. The principal instruction register is on the controller module. The instruction register on the processor is used to store the variable part of the instruction such as addressing parameters.

The interrupt and transfer vector generation logic is included on this module. Interrupts are controlled by an on-board TMS 9901 programmable systems interface device. It can selectively mask out or test any of the 15 interrupts and generate a four-bit interrupt vector.

The controller board contains the control memory, which stores the microinstructions emulating the TMS 9900 and generating new instructions and enhances the integer and floating-point arithmetic. It also contains the instruction register, clock control logic, an RS232 serial communication controller (CRU hardware address 40), and ready handshaking logic to enable the TM990/1481 to operate with TM990 family memory boards.

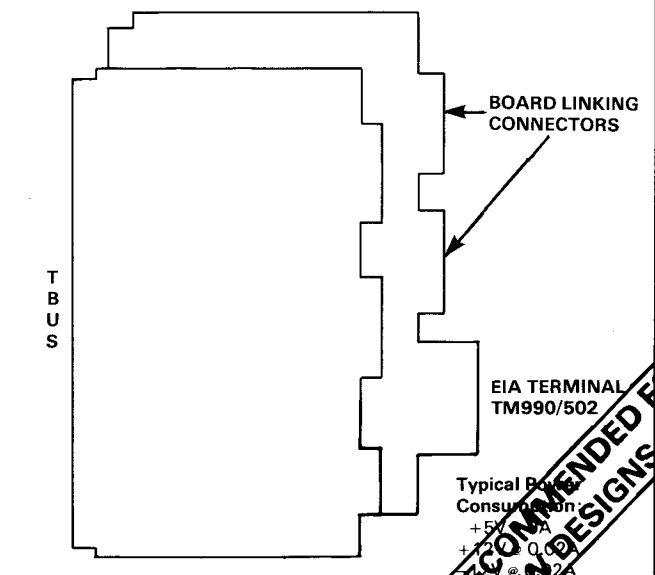
BLOCK DIAGRAM:



INSTRUCTIONS ADDITIONAL TO STANDARD 9900 INSTRUCTION SET

ASSEMBLY LANGUAGE MNEMONIC	INSTRUCTION	ASSEMBLY LANGUAGE MNEMONIC	INSTRUCTION
AD	Add Double Precision Real	LD	Load Double Precision
AR	Add Real	LR	Load Real
CDE	Convert Double Precision Real to Extended Integer	LST	Load Status Register
CDI	Convert Double Precision Real to Integer	LWP	Load Workspace Pointer Register
CED	Convert Extended Integer to Double Precision Real	MD	Multiply Double Precision Real
CER	Convert Extended Integer to Real	MPYS	Multiply Signed
CID	Convert Integer to Double Precision Real	MR	Multiply Real
CIR	Convert Integer to Real	NEGD	Negate Double Precision Real
CRE	Convert Real to Extended Integer	NEGR	Negate Real
CRI	Convert Real to Integer	SD	Subtract Double Precision Real
DD	Divide Double Precision Real	SR	Subtract Real
DIVS	Divide Signed	STD	Store Double Precision Real
DR	Divide Real	STR	Store Real

CONNECTORS:



ORDERING INFORMATION:

Part number	
TM990/1481	2 board set including link cables, 5 MHz Bus Clock
TM990/201-44	EPROM/RAM expansion module
TM990/203A-13	Dynamic RAM expansion module
TM900/403	TIBUG Interactive Debug Monitor
TM990/433	Floating point demonstration software

NOT RECOMMENDED FOR NEW DESIGNS

TM990/201

T-BUS MEMORY EXPANSION MODULE

FEATURES:

- **Up to 32K bytes of TMS 2716 EPROM.**
- **Up to 16K bytes of TMS 2114 Static RAM.**
- **1 microsecond cycle time (3 MHz).**
- **Bus compatible with T-BUS TM990/10X CPU boards.**
- **TM990/201-44 compatible with TM990/1481.**
- **16 memory maps for both EPROM and RAM.**
- **Selectable Wait State generator.**
- **0–70°C temperature range.**
- **Factory burnt-in.**

DESCRIPTION:

The TM990/201 memory expansion board is a member of Texas Instruments line of OEM computer products which takes advantage of Texas Instruments broad based semiconductor technology to provide economical, computer based solutions for OEM applications. The memory expansion board is contained on a $7\frac{1}{2} \times 11$ inch printed circuit board which is fully compatible with the TM990 board format.

The TM990/201 features up to 16K bytes of static RAM and up to 32K bytes of EPROM. The static RAM array is composed of Texas Instruments TMS 4014/2114 1K × 4 static memory devices. The EPROM array comprises Texas Instruments TMS 2716, 2K × 8 EPROM devices. The static RAM array is arranged into four banks of memory, each 2K × 16. The EPROM array is likewise arranged into eight banks, each 2K × 16. Both memory arrays are socketed for convenient memory expansion. (The TM990/201-42 and TM990/201-43 are fully socketed).

The TM990/201 memory controller logic provides the timing and memory mapping functions necessary to interface the TM990/201 to 16-bit TM990/10X series microcomputers. The memory map is switch selectable for both the RAM and EPROM arrays. Sixteen convenient memory map configurations are possible for each array, and the maps are configured on 4K byte address boundaries. The map logic also is designed to accommodate customized memory maps.

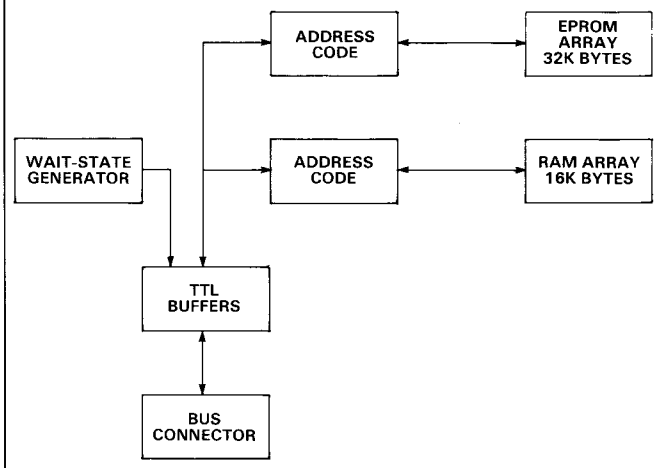
The TM990/201-4X family of memory expansion boards is populated with TMS 4014/2114-45 static RAM's and TMS 2176 EPROM's. Both devices offer 450 nsec access time; consequently, each memory cycle to the TM990/201 is extended one clock cycle by the insertion of a wait state. If faster static RAM's are utilized in the RAM array, the WAIT state in RAM memory cycles can be conveniently removed using only a jumper.

ORDERING INFORMATION:

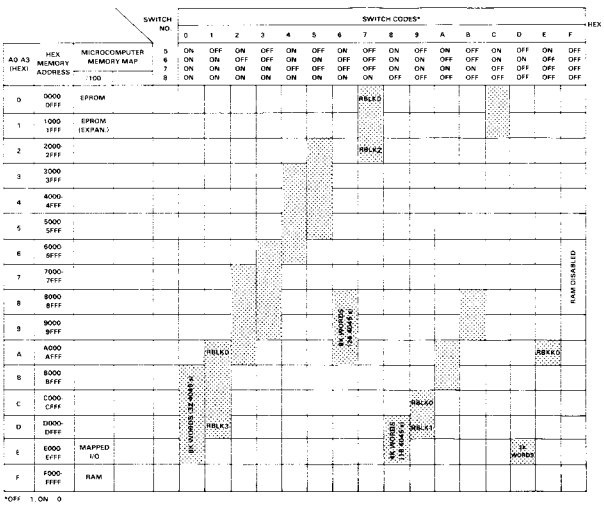
Part number	EPROM	RAM	Typical Power Requirements +5V	+12V	−12V
TM990/201-41	8K (16K)	4K (8K)	1.0 A	160 mA	50 mA
TM990/201-42	16K (32K)	8K (16K)	1.4 A	225 mA	125 mA
TM990/201-43	32K (32K)	16K (32K)	2.2 A	475 mA	225 mA
TM990/201-44	0 (32K)	16K @ 5 MHz	2.2 A	475 mA	225 mA

Numbers in brackets refer to area socketed. All memory sizes are in bytes.

BLOCK DIAGRAM:

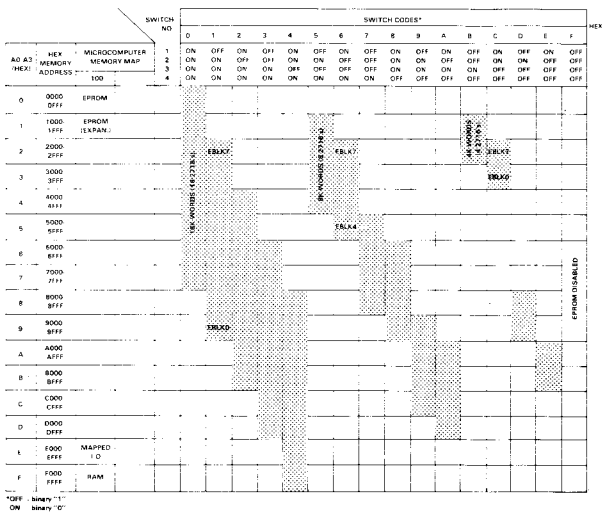


RAM DECODE CONFIGURATIONS:



N.B. THE TM990/201-44 HAS DIFFERENT MEMORY CODE CONFIGURATIONS

EPROM DECODE CONFIGURATIONS:



N.B. THE TM990/201-44 HAS DIFFERENT MEMORY CODE CONFIGURATIONS

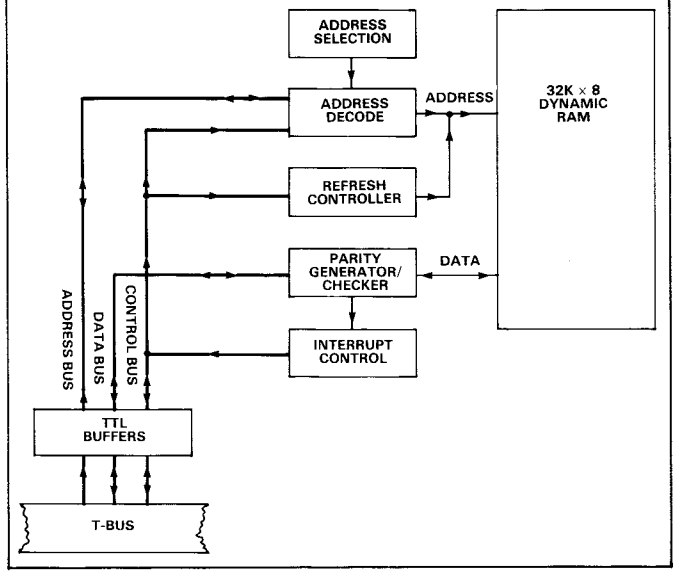
TM990/203

T-BUS MEMORY EXPANSION MODULE

FEATURES:

- **Up to 64K bytes of TMS 4116 DYNAMIC RAM.**
- **Cycle steal or Transparent refresh.**
- **Runs with no wait states at 3 MHz.**
- **5 MHz Clock capability option for use with TM990/1481 Bit Slice Processor.**
- **Parity error detection.**
- **Full DMA capability.**
- **16 memory maps for both EPROM and RAM.**
- **Selectable Wait State generator.**
- **0–70°C temperature range, for harsh Industrial Environments.**
- **Factory burnt-in for reliability.**

BLOCK DIAGRAM:



DESCRIPTION:

Address decoding circuitry on the TM990/203 module decodes both 16- and 20-bit addresses. Upper and lower boundaries are DIP switch selectable on 4K byte boundaries. Boundary selection is independent of the amount of memory actually populated on the module. This means the user can disable any 4K bytes of memory for other use such as a 4K EPROM loader. All of the TM990/203 memory may be disabled without removing it from the card cage by selecting a starting address that is greater than the ending address.

The TM990/203 memory module will interrupt the processor in the event of a parity error if operation with parity is used. An interrupt handler (software routine) must be generated by the user to reset the parity interrupt and flag the memory location which is in error. The exact location in error may be found by the interrupt routine if a read operation is performed, with all additional interrupts masked, on the entire RAM memory while the software monitors the interrupt line to check for errors.

Three jumper selectable parity options are available: no parity interrupts, parity interrupts resetable by the CPU's TMS 9901, or parity interrupts resetable by a discrete CRU location (with user supplied PROM). Jumpers are also provided to configure the TM990/203 parity interrupt to level 1 or level 2.

Parity interrupts may be reset by the TM990 bus signal INT15.B-/P7 which is usually generated by setting bit P7 in the CPU TMS 9901 I/O port. A low on this line will clear and disable the parity interrupt. A high on this line will enable the parity interrupt.

Parity interrupts can also be reset by doing a CRUOUT operation. The particular location is programmed into an SN74S287N PROM supplied by the user. This allows the user to free INT15.B- for other purposes. It also allows the user to configure his reset in the CRU address map.

Two jumper selectable refresh modes are available. Transparent refresh automatically refreshes the dynamic memories when they are not being accessed. In transparent mode the processor indicates to the memory that the following few cycles are available to do a refresh cycle. This indication is the rising edge of MEMEN-. When this is sensed by the TM990/203 the next 2 consecutive clock cycles following this edge are used for refresh.

The TM990/203 is designed such that transparent mode defaults to cycle steal mode; this occurs every time there is a minimum refresh violation. That is, the number of refresh cycles performed during any fixed time is less than the minimum required to insure data integrity. For example, if the processor is placed in a hold state in order that another processor may take the line, MEMEN-, as well as the data and address lines of the processor, is placed in the three-state, high impedance condition. If the bus is not captured and MEMEN- stays in this state, the TM990/203 cycle steal circuitry will time out and issue a refresh request. This is all done on board the TM990/203 and is transparent to the user unless he tries to access the TM990/203 during this time. In that case a not ready condition will be asserted until the end of the refresh cycle.

POWER REQUIREMENTS (CYCLE STEAL MODE)

	Currents (cycle steal)					
	16K (bytes)		32K		64K	
Voltage	TYP	MAX	TYP	MAX	TYP	MAX
Vcc +5V ± 3%	1.9 A	3.0 A	1.85 A	2.7 A	1.9 A	3.0 A
Vdd +12V ± 3%	77 mA	1.2 A	65 mA	0.6 A	90 mA	1.2 A
Vaa −12V ± 3%	10 mA	20 mA	10 mA	15 mA	10 mA	20 mA

POWER REQUIREMENTS (TRANSPARENT MODE)

	Currents (transparent mode)					
	16K (bytes)		32K		64K	
Voltage	TYP	MAX	TYP	MAX	TYP	MAX
Vcc +5V ± 3%	1.9 A	3.0 A	1.85 A	2.7 A	1.9 A	3.0 A
Vdd +12V ± 3%	150 mA	1.2 A	110 mA	0.6 A	190 mA	1.2 A
Vaa −12V ± 3%	10 mA	20 mA	10 mA	15 mA	10 mA	20 mA

ORDERING INFORMATION:

Part number	Description
TM990/203-21A	16K bytes of TMS 4108-25 RAM with Parity
TM990/203-22	32K bytes of TMS 4116-25 RAM with Parity
TM990/203-23	64K bytes of TMS 4116-25 RAM with Parity
TM990/203A-13	64K bytes of TMS 4116-15 RAM with Parity

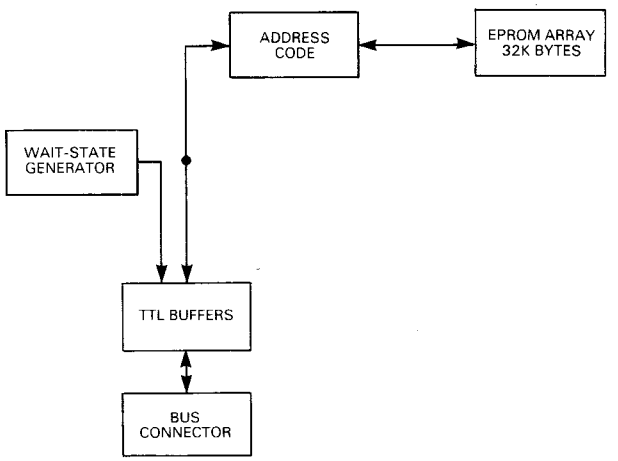
TM990/206

T-BUS MEMORY EXPANSION MODULE

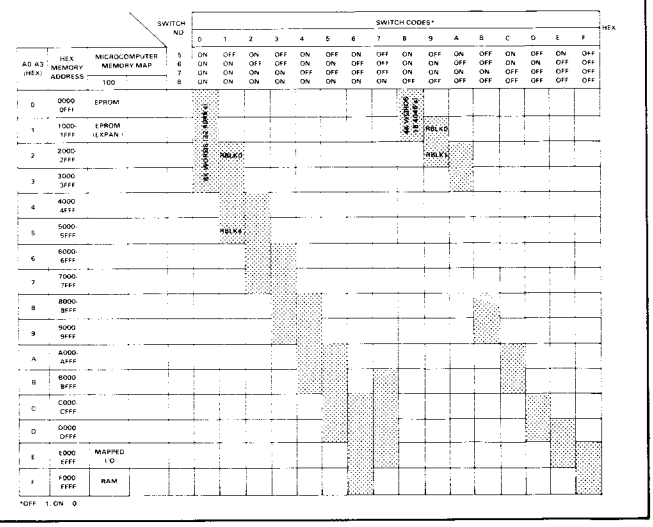
FEATURES:

- **Up to 16K bytes of TMS 2114 Static RAM.**
- **1 microsecond cycle time (3 MHz).**
- **Bus compatible with T-BUS TM990/10X CPU boards.**
- **16 memory maps for both EPROM and RAM.**
- **Selectable wait state generator.**
- **0–70°C temperature range.**
- **Factory burnt-in.**

BLOCK DIAGRAM:



RAM DECODE CONFIGURATIONS:



DESCRIPTION:

The TM990/206 expansion memory board is a member of Texas Instruments' line of OEM computer products which take advantage of Texas Instruments' broad based semiconductor technology to provide economical, microcomputer based solutions for OEM applications. The memory expansion board is contained on a $7\frac{1}{2} \times 11$ inch printed circuit board which is fully compatible with the TM990 board format. The TM990/206 features up to 16K bytes static RAM. The RAM array is composed of Texas Instruments TMS 4014/2114-45 1K × 4 static memory devices. The array is configured into four banks of memory, each bank consisting of 4K bytes. The RAM array is fully socketed for convenient memory expansion.

The memory controller logic provides the timing and memory mapping functions necessary to interface the TM990/206 to 16-bit TM990/10X series microcomputers. Sixteen convenient, switch selectable, memory map configurations are possible. All maps are configured on 8K byte address boundaries.

The TM990/206-4X family of memory expansion boards is populated with TMS 4014/2114-45 static RAM's, featuring an access time of 450 nsec. For operation with a TM990/100M microcomputer, each memory cycle to the TM990/206 is extended one clock cycle by the insertions of a WAIT state. If faster static RAM's are utilized, the WAIT state can be conveniently removed with a jumper.

ORDERING INFORMATION:

Part number	RAM	Typical power requirements		
		+5V	+12V	−12V
TM990/206-41	4K (8K)	1.3A	0	0
TM990/206-42	8K (16K)	2.2A	0	0

Numbers in brackets refer to area socketed.
All memory sizes are in bytes.

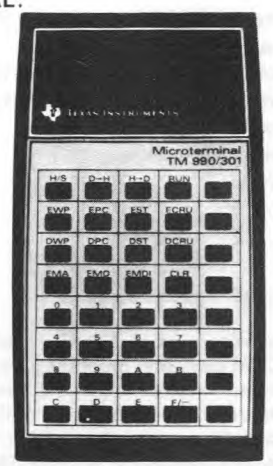
TM990/301

MICROTERMINAL

FEATURES:

- **Hexadecimal push button keyboard.**
- **4 digit hexadecimal display of address and data.**
- **Register, memory, or CRU display and entry keys.**
- **Execution, single instruction and conversion keys.**
- **Operates under TIBUG monitor.**
- **Integral cable connects directly to serial EIA port on CPU module.**

MICROTERMINAL:



DESCRIPTION:

The TM990/301 is a microterminal designed to interface with the TM990 series of microcomputer modules. The microterminal's communications link to the TM990 CPU module is via the EIA type cable and the serial terminal interface. The TM990/301 performs the front panel functions of the microcomputer system, giving the programmer the ability to display and change register and memory information. This low cost terminal offers the capability to enter short programs in hexadecimal or alter a section of a longer sequence.

The TM990/301 operates under control of the TM990/401 TIBUG monitor. The data rate utilized is 110 baud. Once the CPU board is initialized, depressing the clear (CLR) key transfers TIBUG monitor control to the microterminal. The TIBUG software will enter a wait routine unless performing a function defined by the microterminal. Depressing the run (RUN) key will cause the CPU module to begin program execution and it will ignore other key depressions.

COMMAND SUMMARY:

KEY	FUNCTION
CLR	Clear—blank all displays—initialize software.
RUN	Run—TM990 CPU begins program execution "RUN" is displayed in data digits.
HALT/SIE	Halt/Single Instruction Execution—If in run mode, halts CPU execution—address of next instruction displayed in address digits. If CPU is halted, one single instruction will be executed. Address display indicates address of next instruction data display indicates contents of that location.
0–F	Hexadecimal digits (0–15)—data entry. F/- also indicates negative.
EPC	Enter Program Counter—Enter 4 digits, key depression alters active program counter, data display indicates entered value.
DPC	Display Program Counter—Active PC register indicated in data display.
EST	Enter Status Register—Enter 4 digits—key depression alters active status register, data display indicates entered value.
DST	Display Status Register—Active status register indicated in data display.
EWP	Enter Workspace Pointer—Enter 4 digits—key depression alters active workspace pointer—data display indicates entered value.
DWP	Display Workspace Pointer—Active WP indicated in data displayed.
EMA	Enter Memory Address—Enter 4 digits—key depression will shift display of digit from data display to address display. Contents of the new memory address will then be indicated in the data display.

KEY	FUNCTION
EMD	Enter Memory Data—After EMA function has been executed, enter 4 digits—the data display indicates the new data—key depression alters the data at the displayed memory address.
EMDI	Enter Memory Data/Increment—Functions the same as EMD—after key depression of EMDI and data update the address display will automatically increment by 2 and the new address' contents will be indicated by the data display. To increment the address register without altering data contents, depress EMDI key without entering new digit information.
DCRU	Display CRU Data—Enter 4 digits—the first digit specifies the CRU bit count; the remaining 3 digits specify the CRU address. Key depression shifts the entered digits to the address display and indicates the contents of that address in the data display. All 16 bits will be displayed.
ECRU	Enter CRU Data—After DCRU function has been executed, enter 4 digits—the new data is now indicated by the data display—key depression alters the data at the specified CRU address—only the number of bits specified will be altered.
H→D	Hexadecimal to Decimal Conversion—Enter 4 digits—key depression will indicate the decimal equivalent in rightmost display digits.
D→H	Decimal to Hexadecimal Conversion—Enter 6 digits—the first digit designates the sign (F/ = negative, 0 = positive) the remaining 5 are decimal data—key depression displays hexadecimal equivalent in 4 right digits.

ORDERING INFORMATION:

Part number	Description
TM990/301	Microterminal compatible with all TM990 series microcomputer modules.

POWER REQUIREMENTS (Typical)

+5V ± 3% @ 150 mA +12V ± 3% @ 50 ma −12V ± 3% @ 20 mA	Supplied from CPU module through cable

TM990/302

SOFTWARE DEVELOPMENT BOARD

FEATURES:

- **Complete low-cost Development system.**
- **Dual or single AUDIO cassette interface.**
- **EPROM programming for TMS 25xx and TMS 27xx devices.**
- **4K bytes of RAM on-board.**
- **On-board EPROM supporting:**
  Text Editor
  Symbolic Assembler
  Relocating Loader
  EPROM Programming
  I/O Schedular and Handler
  Debugger
- **Uplink to AMPL Development system.**
- **EIA Communication with other Computers.**

DESCRIPTION:

Using the TM990/302 Software Development Module it is possible to construct a very low cost development system. It consists of a CPU module, power supply, audio cassette, software development board and EPROM programmer personality card. The end algorithm is generally related to industrial control with less than 500 lines of code and 10 to 20 target systems in production.

The heart of this low-cost software development system is the TM990/302 Software Development Board; typical power requirement is +12V @ 132 mA, −12V @ 55 mA, +5V @ 830 mA and 35 to 55V @ 80 mA. This module is used for developing assembly language software to be used on 990/9900 family microprocessor based system. The TM990/302 provides dual audio cassette interfaces, both static RAM and ROM memory, and hardware circuitry to aid in the programming or read-only memory devices. Used in conjunction with either the TM990/100MA or TM990/101MA CPU modules, the TM990/302 provides a complete standalone software development system offering support for program generation, editing, assembly, debugging, and EPROM programming.

To create or update the source program, the text editor provides manipulation of individual lines of code. The designer may delete, insert, print and resequence text from his keyboard. The text editor handles programs of any length by segmenting the source code into "buffer" blocks. It controls buffer loading and storage into cassette-tape memory. The buffer is enlarged by plugging in memory-expansion cards, which also expand the amount of target system memory available for execution.

The next step in program development is a two pass assembly of TMS 9900, SBP 9900, TMS 9940, TMS 9980 instructions sets into absolute standard 9900 object code. This two pass assembler allows four-character symbolic addressing. The assembly listing output, including error messages, is routed to a user chosen device.

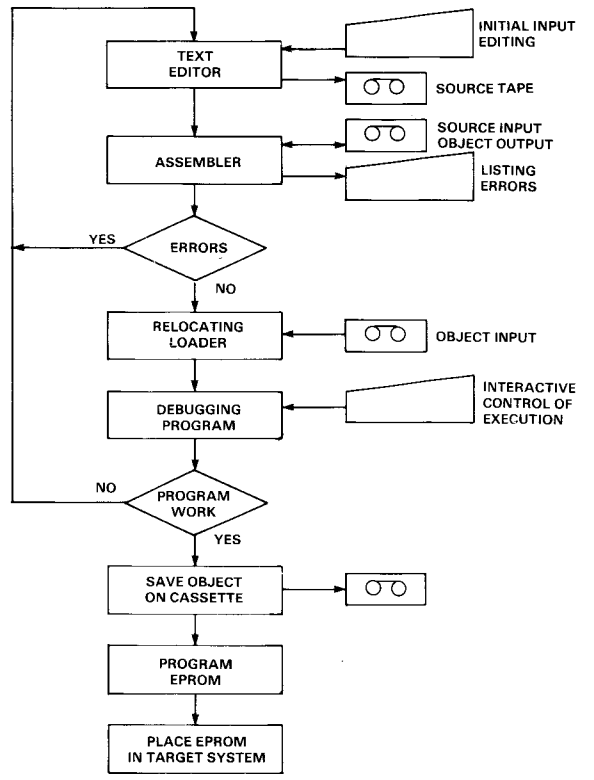
Seven debug commands aid program development after the loader program puts the assembled object into memory. Multi-step trace, software breakpoints and data inspection/changes are featured.

After debug, the EPROM programmer can be invoked to program EPROM's, read back EPROM's into memory, or compare EPROM contents to memory. Byte and word serial formats are available. The EPROM programmer is able to program the following EPROM's: TMS 2708, TMS 2716, TMS 2516, TMS 2532 and TMS 2508.

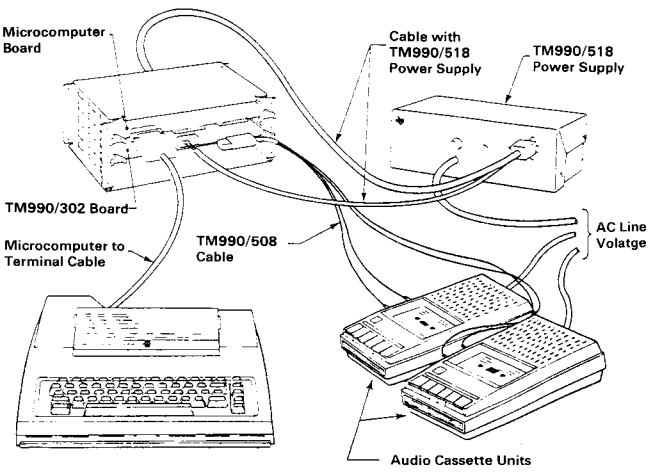
ORDERING INFORMATION:

Part number	
TM990/302	Software Development Module including Audio Cassette interface cable.
TM990/508	Replacement Audio cassette cable.
TM990/514	Personality Module for programming TMS 27XX EPROMS.
TM990/515	Personality Module for programming TMS 25XX EPROMS.
TM990/451D	Optional Development Power Basic EPROM set.
TM990/452D	Optional Development Power Basic enhancement package POWER BASIC.

SOFTWARE DEVELOPMENT EXECUTION:



CONNECTORS:



SOFTWARE COMMAND SUMMARY:

TEXT EDITOR COMMANDS:

D	Delete lines n thru m
I	Insert at line n with optional line-number auto-increment by m
K	Keep (store) buffer and print new top line in the buffer
P	Print lines n thru m
Q	Flush the input file until end of input file and return to executive
R	Resequence output line numbers, giving the initial line number and the increment

DEBUG COMMANDS:

SB	Set software breakpoint and execute
IM	Inspect/change memory
IC	Inspect/change CRU
IR	Inspect/change registers
RU	Run program and trace conditional jumps
ST	Single step for 1 or more instructions
DM	Dump memory to specified cassette in object format

TM990/303A

T-BUS FLOPPY DISC CONTROLLER

FEATURES:

The TM990/303 floppy disk controller has the following features:

- **Formats supported:**
  - **IBM single density format**
  - **IBM double density format**
  - **TI Digital Systems Group (DSG) double density format (TILINE floppy controller)**
- **Disk sizes: Standard or mini.**
- **Disk sides: Single only.**
- **Number of disk drives (daisy chained): Four maximum for standard size, and three maximum for mini size.**
- **Recording methods:**
  - **Single density frequency modulation (FM)**
  - **Double density modified frequency modulation (MFM)**
- **Data format:**
  - **IBM 3740 compatible**
  - **TI FS 990 compatible**
- **System interface:**
  - **CRU (controller initialization)**
  - **DMA transfer (data and commands)**
- **Three LED's indicate controller status.**
- **Bootstrap load feature can be used to initialize system from diskette.**
- **Controller firmware (see below) provided on two TMS 2716's (2K words); controller firmware EPROM space expandable to 4K words by using two TMS 2532's.**

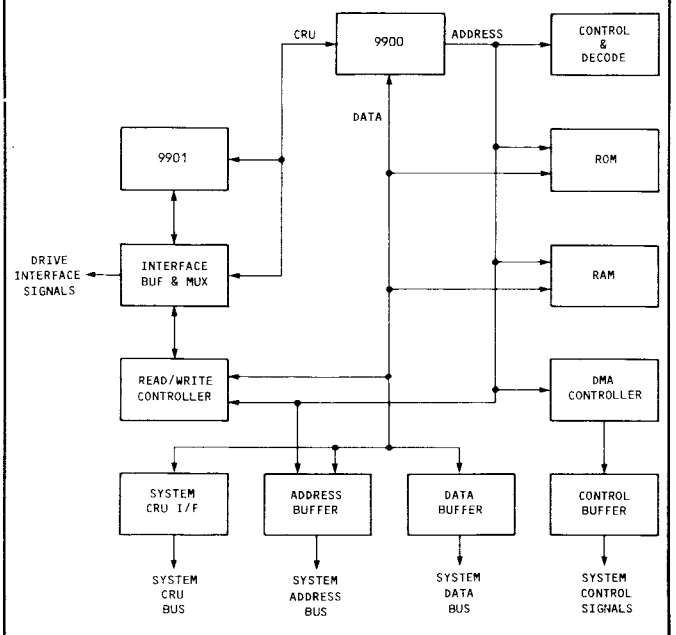
DESCRIPTION:

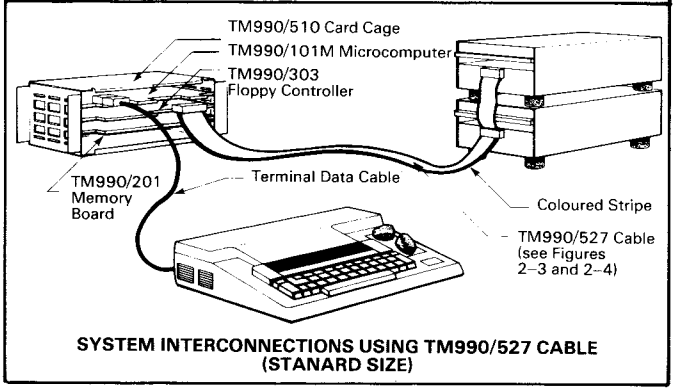
The TM990/303 is a TM990 compatible intelligent floppy disk controller with a DMA interface to the host bus. It supports a wide range of drives and disk formats and is fully compatible with the file manager software component.

Software on the controller includes the following features:

- Seventeen commands including controller self test, read and write to/from diskette and host memory, read to and write from controller and host RAM, bootstrap load from diskette software, format diskette, execute program in controller memory, read status of specified drive.
- Command completion interrupt to host (interrupt level jumper selectable); completion status reported to host.
- Controller call through interrupt via CRU.

BLOCK DIAGRAM:





SYSTEM INTERCONNECTIONS USING TM990/527 CABLE (STANARD SIZE)

ORDERING INFORMATION:

Part number	Description
TM990/303A	Floppy Disc Controller
TM990/527	Data Cable
TM990/425	Demonstration Software

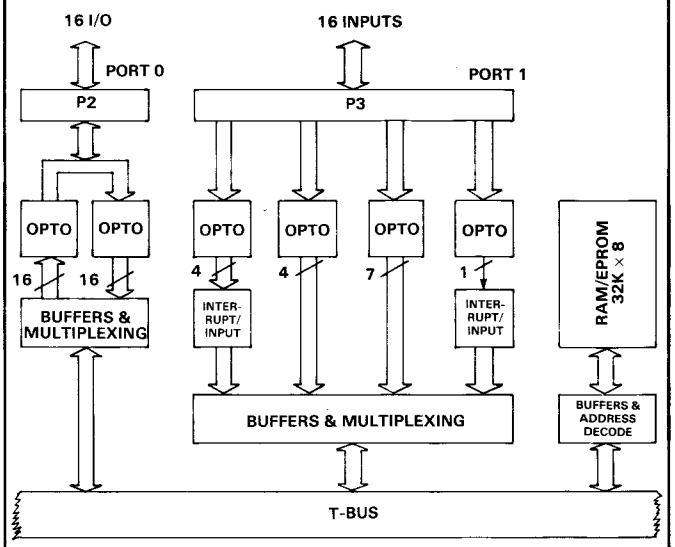
TM990/305

COMBINATION MEMORY AND INPUT/OUTPUT EXPANSION MODULE

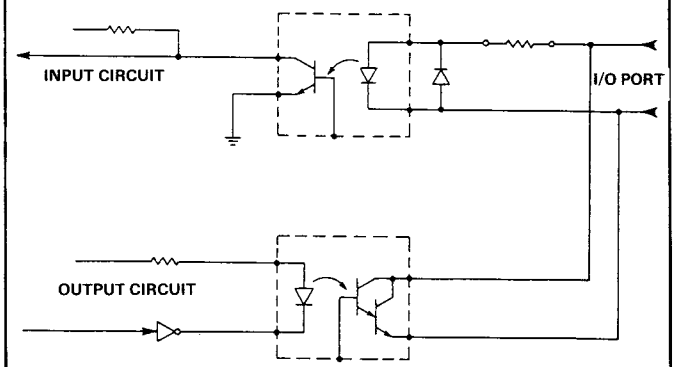
FEATURES:

- **5MT interface via TM990/509 cable (includes 8V supply to power 5MT module).**
- **Memory capacity of up to 32K bytes.**
- **16 optically isolated parallel input lines.**
- **16 optically isolated parallel input/output lines.**
- **500 volts input to output isolation.**
- **2 +ve and 2 –ve edge triggered and latched interrupts.**
- **16 or 20-bit address handling.**

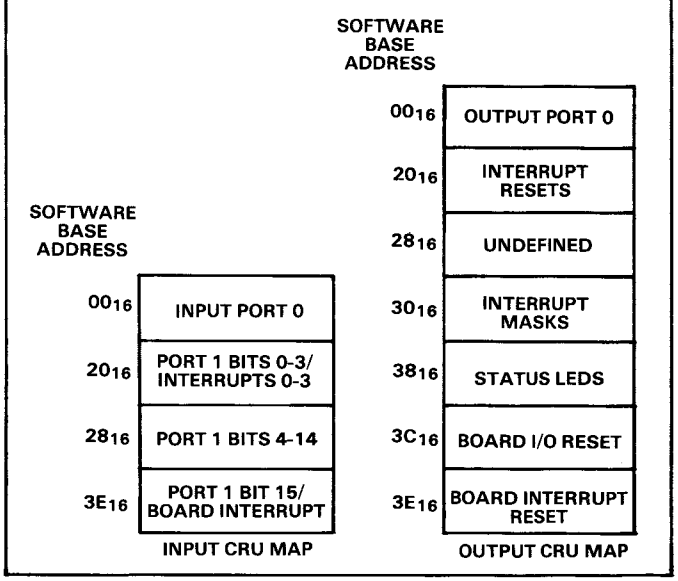
BLOCK DIAGRAM:



INPUT/OUTPUT SCHEMATIC:



CRU ADDRESS MAP:



DESCRIPTION:

The TM990/305 is a combination memory and input/output expansion module. This module can comprehend a 16-bit address, as used in a TM990/10X system, or a 20-bit address, as used in a system utilizing a memory-mapping CPU. The TM990/305 has a memory capacity of 32K bytes. Memory configuration is significantly enhanced by allowing the use of either static RAM* or EPROM** in each of the memory sockets. This module has 16 parallel input channels (Port 1) and 16 parallel input/output channels (Port 0) that can be configured individually as either inputs or outputs. All I/O channels are optically isolated and interface through the Communications Register Unit (CRU).

Input/output flexibility is designed into the TM990/305 to allow the user to configure the I/O channels to meet his requirements. Input channels may be configured for input voltages up to 30V, while output channels may be configured for TTL compatibility or as current drivers. Output channel polarity can be selected by the user as either inverting or non-inverting.

5MT industrial I/O interface capability is provided on the TM990/305 module. An on-board voltage regulator supplies the required +8V V_{CC} while the required pullup resistors for the I/O channels can be installed in sockets provided on the module. A TM990/509 cable is then required to connect the TM990/305 to a 5MT I/O system.

*(TMS 4016) **(TMS 2516 or TMS 2532)

POWER REQUIREMENTS (Typical)

+5V ± 3% @ 0.7 A (no memory) to 1.5 A.
+12V ± 3% @ 600 mA if 5MT interface cable (TM990/509) is used.

ORDERING INFORMATION:

Part number	Description
TM990/305U	305 card with unpopulated memory sockets.
TM990/305E	305 card with 8K bytes EPROM.
TM990/509	5MT module interface cable.

Note: TM990/305 Module is shipped with 16 input opto-couplers and 4 output opto-couplers in PORT 0. No opto-couplers are shipped in PORT 1.

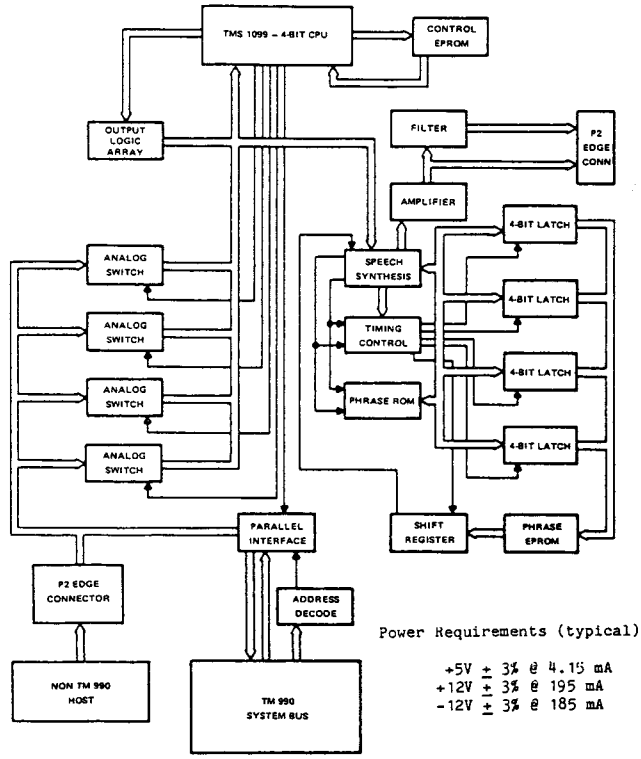
TM990/306

SPEECH MODULE

FEATURES:

- **Self-contained 180 word vocabulary.**
- **On-board 1 watt audio amplifier.**
- **Inputs/outputs are TTL compatible.**
- **Preamplifier outputs available.**
- **Interval timer available.**
- **CRU or interrupt driven operation.**
- **Stand-alone operation possible.**

BLOCK DIAGRAM:



DESCRIPTION:

The TM990/306 is a bus-compatible member of the TM990 product family capable of generating speech from a self-contained data set. The module contains a fixed vocabulary from which the user may construct phrases or sentences. The module has been especially designed to operate in noisy industrial environments such as found on assembly lines, stockrooms, etc.

In addition to the numbers from 0 to 12 and alphabet from A to Z, there are 140 words in the base vocabulary. The user is encouraged to be ingenious in his use of the speech set. For instance, it is suggested that certain letters sound like words: "R" = are, "N" = in, "B" = be, "C" = see. from these letters, words can be constructed such as "N" + crease = increase; and "D" + crease = decrease. The vocabulary also contains the following pauses: 80 ms, 160 ms, 240 ms and 320 ms.

Polled-status Operation
In this mode of operation the CPU issues the address of a word to be spoken, sets the talk command and waits for the word to be spoken. When the talk flag goes inactive CPU decides whether to say another word. All communication is through the CRU bus to the on-board TMS 9901.

Interrupt-Driven Operation
Since generating speech is a very slow operation compared to computer cycles, computer time could be tied up in a polled-status mode where the CPU would spend all its time checking to see if the speech has stopped. The system may be free to do other things while it is talking if the interrupt mode is selected. A jump-selectable interrupt is issued when the speech processor stops talking. When the host CPU sees the interrupt, it decides whether to say another word or delay or stop speaking entirely.

The TM990/306 may be obtained without speech data EPROM's for those users who wish to customize their own speech set. TI Regional Technology Centres (RTC) can provide customized vocabulary sets on EPROM's in a format compatible with the TM990/306.

TM990/306 ON-BOARD VOCABULARY:

A
ABORT
ADJUST
ALERT
ALL
AMPS
AND
AUTOMATIC

B
BACK
BUTTON

C
CALIBRATE
CALL
CANCEL
CARPENTER
CHECK
CLOCK
CLOSE
CONTROL
CRANE
CREASE
CYCLE

D
DANGER
DAYS
DEGREES
DEVICE
DIRECTION
DISPLAY
DOOR
DOWN

E
ELECTRICIAN
ELEVEN
ENTER
EQUAL
EXIT
EIGHT
EAST

F
FAIL
FARAD
FAST
FEET
FOUR
FIVE

G
GAGE
GATE
GET
GO
GREEN

H
HENRY
HERTZ
HIGH
HOLD
HOURS
HUNDRED

I
INCH
INITIALIZE
INSPECTOR
INTRUDER
IS

J
JOG

K

L
LEFT
LIGHT
LINE
LOW

M
MACHINE
MAKER
MANUAL
MEASURE
MEGA
METER
MICRO
MILL
MILLI
MINUS
MINUTES
MOTOR
MOVE

N
NUMBER
NINE
NORTH

O
OF
OFF
OHMS
ON
ONE
OPEN
OPERATOR
OUT
OVER

P
PASS
PASSED
PERCENT
PICO
PLUS
POINT
POSITION
POUND
POWER
PRESS
PRESSURE
PRIORITY
PROBE
PROCESSING
PULL
PUSH
PUT

Q

R
RANGE
READY
RED
REPAIR
REPEAT
REPLACE
RIGHT

S
SAFE
SECONDS
SET
SEVEN
SHUT
SIX
SLOW
SMOKE
SOUTH
SPEED
START
STOP
SWITCH

T
TEMPERATURE
TEN
TEST
THE
THOUSAND
THREE
TIME
TIMER
TOOL
TURN
TWELVE
TWO

U
UNDER
UNIT
UP

V
VALVE
VOLTS

W
WAIT
WARD
WATTS
WELDER
WEST

X/Y/Z
YELLOW
ZERO

ORDERING INFORMATION:

Part number	Description
TM990/306	Speech Module with 180 word vocabulary.
TM990/306-2	Speech Module (no vocabulary).
TM990/426	TM990/306 Demonstration software EPROM kit.

TM990/307

T-BUS SERIAL INPUT/OUTPUT EXPANDER CARD

FEATURES:

- **Four RS 232C EIA ports using DB-25P connectors (Port D provides RS 232C or RS 422 interfaces).**
- **Bell automatic calling unit interface.**
- **Individual channels are CRU address selectable.**
- **CRU addressable DIP switches and status LED's provided.**
- **Software compatible with TM990/101MA Port B RS 232 interface.**
- **Loopback allows self testing.**
- **Software programmable baud rates.**

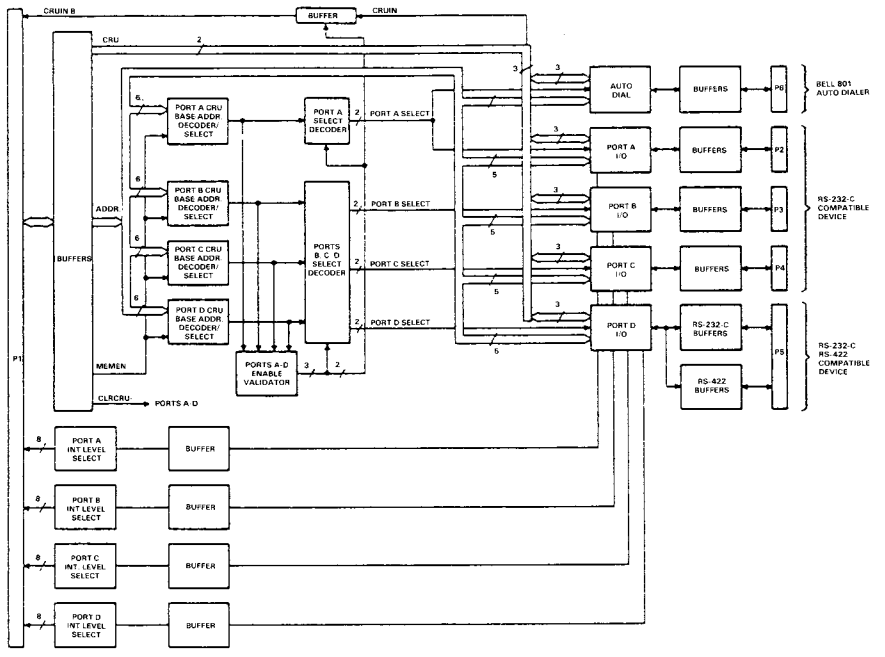
DESCRIPTION:

The TM990/307 communication expander module, is a bus-compatible member of the TM990 product family. This module can communicate with up to four asynchronous or synchronous devices through RS 232 interfaces (an optional TMS 9903 is required for synchronous devices). The devices can be either modems or terminals. A parallel interface is included for interfacing to an auto-dialer – such as Bell 801 Automatic Calling Unit.

The TM990/307 Communication Expander Module is implemented using the TM990 printed circuit format. The TM990/307 uses four TMS 9902 asynchronous communication controller devices for transmitting and receiving serial data. Each TMS 9902 also contains an interval timer – giving the user four programmable timers. By replacing the TMS 9902's with TMS 9903's communication to synchronous modems is possible.

Each EIA data port occupies 64 bits in the CRU map. Ports B, C and D use identical CRU maps. The first thirty two bits are used to address the TMS 9902 communication controller. The next 32 bits are used for modem control, CRU addressable switches, status monitoring and LED. In addition, Port A has the Auto Dialer feature.

BLOCK DIAGRAM:



INPUT/OUTPUT SPECIFICATION:

Data Ports:
TMS 9902 asynchronous controller.
Programmable data rate, stop bits, parity.
Break characters generation.
Framing, parity, and overrun errors detected.
75 to 38400 baud, software programmable.
EIA RS 232 signal compatible.
Switch selectable CRU address, each port independent.
Two CRU addressable switches per port.
One CRU addressable LED per port.

Auto Dialer:
(Port A only) Header connector with pinouts compatible with a Bell 801 auto dialer or equivalent. Pinouts are arranged such that an interface cable can be constructed using: 25/26-pin ribbon cable; a 26-pin header connector and a 25-pin DB-25 EIA connector.

RS 422 Port:
(D only) Can be jumper configured as an RS 422 Port.)

INTERVAL TIMER SPECIFICATION:
Four timers with a resolution of 64 microseconds and a maximum interval of 16.32 milliseconds.

ORDERING INFORMATION:

TM990/307 Serial I/O expander board
TM990/502 (RS 232 EIA terminal)
TM990/503 (743/745)
TM990/505 (733 ASR)
TM990/506 RS 232 modem cable

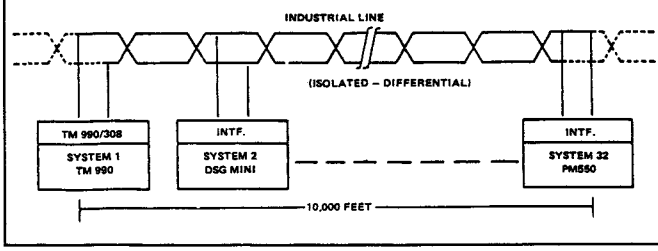
TM990/308

T-BUS INDUSTRIAL COMMUNICATIONS MODULE

FEATURES:

- **Point-to-point or multi-point operation – jumper selectable.**
- **Two-wire interface utilizing isolated differential line driver/line receiver stage – 1500 VRMS isolation provided.**
- **Communication to 10,000 feet at 9600 bits/second.**
- **Separate EIA RS 232C interface for modem operation – Bell 208 modem compatible using TM990/502 cable.**
- **Self-test capability.**
- **Jumper-selectable baud rates: 1200, 2400, 4800 or 9600 b/s.**
- **Compatible with TI's DSG Minicomputers and PM550 Controllers.**
- **Down-load command implementation.**
- **Hardware cyclic redundancy checking (CRC) and generation provided by on-board TMS 9903.**
- **Switch-selectable station ID.**
- **928 bytes for data buffering.**
- **Jumper-selectable interrupt levels – 1 through 15.**
- **Switch-selectable CRU base address.**

SYSTEM OPERATING IN MULTIDROP MODE:



DESCRIPTION:

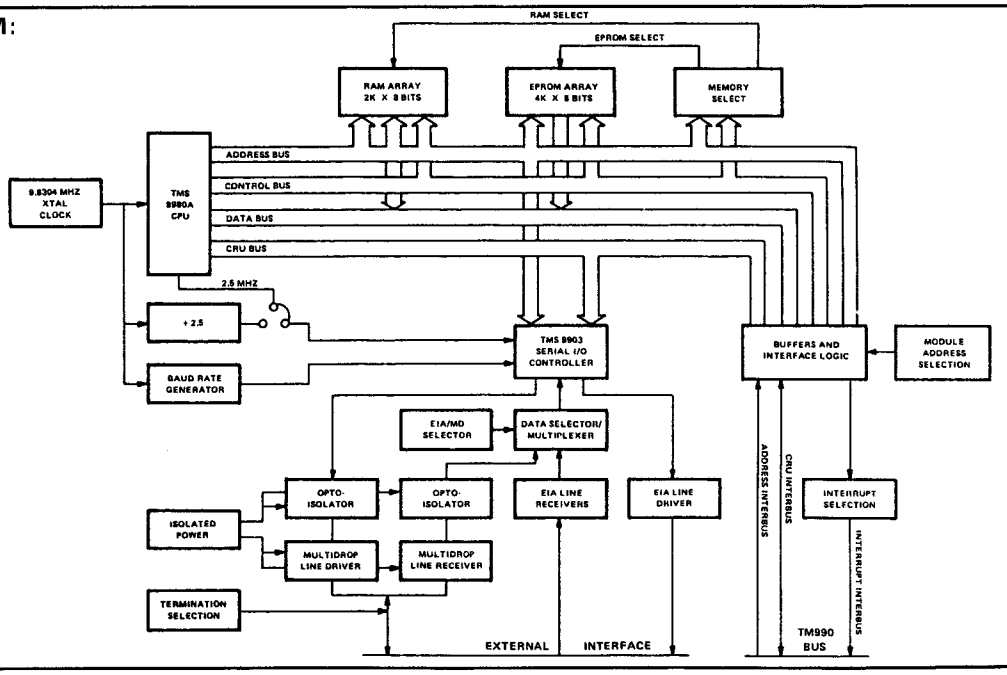
The TM990/308 Industrial Communication Module (ICM) is a bus-compatible member of the TM990 product family. This module provides necessary interface logic for implementing a serial, synchronous communication link between two or more TM990 systems. The ICM extends the communication range of the CPU module by providing industrial-line or RS 232C EIA interfaces that can be used with twisted-pair line and telephone line respectively to provide a long-range communication link. This interface allows serial transmission using CRU interface for byte and status transmission between the host microcomputer and ICM.

The TM990/308 ICM uses a TMS 9903 to perform the serial synchronous transmit and receive functions and a TMS 9980A to control the TMS 9903 and to provide the interface between the ICM and the TM990 bus. The TMS 9980A performs address decoding, download command decoding, and data buffering functions.

The TM990/308 has 3 modes of communication:

- Serial transmission over the communication link from one ICM to another.
- Communication through interrupts between microcomputer and ICM module.
- Handshaking using the Communication Register Unit (CRU) for byte and status bit transmission between (to and from) the host microcomputer and ICM.

BLOCK DIAGRAM:



ORDERING INFORMATION:

TM990/308 Industrial Communications Module.

FEATURES:

- **Allows connection of up to 192 input & 192 outputs using TI 6MT I/O modules.**

GENERAL:

The 6MT Series I/O system is a modularly packaged system designed for use in severe industrial environments. It is similar to the 5MT I/O system, but requires less power. The system consists of mounting bases, logic interface modules, and I/O modules (4 I/O points per module).

The 6MT system requires two power supplies, an 8.5 Vdc supply for general logic and a switched 7.5 Vdc supply for enabling the output point I/O modules. Approximately 1 A total per mounting base is required. The actual current required from either supply is dependent on point configuration.

The logical structure of the 6MT system resembles two shift registers which use a common clock, one for the input points, and one for the output points. The points are identified by X-numbers for inputs and Y-numbers for outputs. The lowest number is the one which is "closest" to the TM 990/309 6MT. For example, X0 would be the first input point seen by the TM 990/309 6MT during a scan, and Y0 would be the last output point sent by the TM 990/309 6MT during a scan.

Figure A illustrates this logical structure. Figure B shows the numbering scheme and physical location of the field terminations for each point.

MOUNTING BASE:

The mounting base provides the interconnection between the I/O modules and the field wiring terminals. Each mounting base will support ten 6MT I/O modules, i.e., 32 I/O points. The center two positions are reserved for the logic interface modules. The remaining eight positions are used to mount the I/O modules which provide the isolated interface to the field wiring terminals.

The mounting base takes the 8.5 Vdc and provides the 5 Vdc required by the modules which plug into it. It also contains the line drivers and receivers by which it communicates with other bases and/or the TM 990/309 6MT.

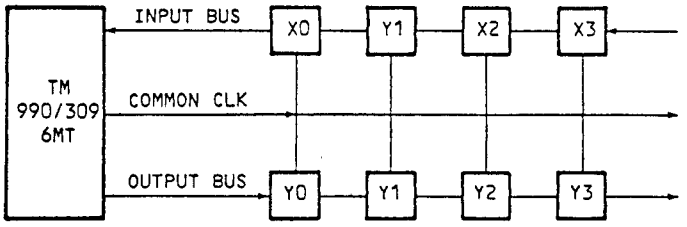


FIGURE A. 6MT I/O SYSTEM LOGICAL STRUCTURE

INPUT MODULE SPECIFICATIONS

Part Number →	6MT11-E05L	6MT11-A05L	6MT11-B05L	6MT13-D05L
Input Voltage	17–28 Vac at 47–63 Hz	85–132 Vac at 47–63 Hz	170–260 Vac at 47–63 Hz	4–28 Vdc
Input Current	30 mA max at 28 Vac, 60 Hz	30 mA max at 132 Vac, 60 Hz	30 mA max at 260 Vac, 60 Hz	10 mA max at 28 Vdc
Input Resistance*	13K ohm min at 24 Vac, 60 Hz	13K ohm min at 120 Vac, 60 Hz	26K ohm min at 220 Vac, 60 Hz	40K ohm min at 28 Vdc
Turn on time	8 ms typical 14 ms max at 24 Vac, 60 Hz	8 ms typical 14 ms max at 120 Vac, 60 Hz	8 ms typical 14 ms max at 220 Vac, 60 Hz	2.5 ms typical 5.0 ms max
Turn off time	10 ms typical 16 ms max at 24 Vac, 60 Hz	10 ms typical 16 ms max at 120 Vac, 60 Hz	10 ms typical 16 ms max at 220 Vac, 60 Hz	2.8 ms typical 5.0 ms max

*which will not cause turn on and will allow turn off.

ORDERING INFORMATION:

TM990/309–6MT Interface module.

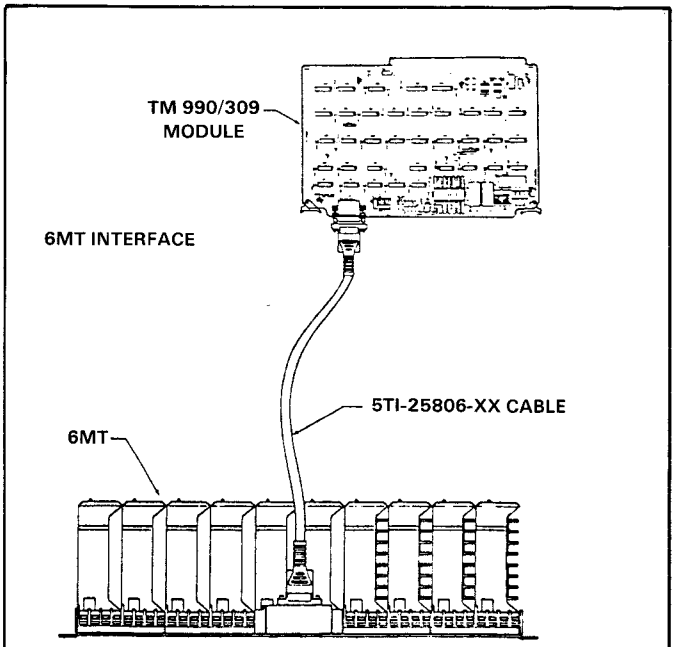
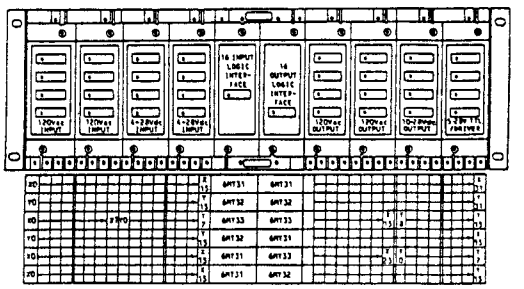


FIGURE B-1. TM 990/309 TO 6MT INTERCONNECTION

A TYPICAL I/O COMBINATION, FIG. B.



OUTPUT MODULE SPECIFICATIONS

Part Number →	6MT12-40EL	6MT12-40AL	6MT12-40BL	6MT-14-40CL	6MT14-40DL
Output voltage	17–28 v-ac at 47–63 Hz	85–132 v-ac at 47–63 Hz	170–260 v-ac at 47–63 Hz	10–28 v-dc	5–28 v-dc
Output current	.05–2A at 40°C *	.05–2A at 40°C *	.05–2A at 40°C *	1A at 60°C	16 mA, 5≤ +dc≤ 10 100 mA, 10< +dc≤ 28
Inrush current	12A at 24 v-ac, 60 Hz 1 cycle	12A at 120 v-ac, 60 Hz 1 cycle	12A at 220 v-ac, 60 Hz 1 cycle	3A at 5 sec max	
On state voltage drop	1.2 v-ac typical 2.0 v-ac max at I_{load} – 2A	1.2 v-ac typical 2.0 v-ac max at I_{load} – 2A	1.2 v-ac typical 2.0 v-ac max at I_{load} – 2A	1.4 v-dc at I_{Ldc} – 1A	0.4 v-dc at I_{Ldc} – 16 mA 0.8 v-dc at I_{Ldc} – 100 mA
Off state leakage current	6 mA max at 28 v-ac	6 mA max at 132 v-ac	6 mA max at 260 v-ac	1 mA at 28 v-dc	250 μa at 5 v-dc 1 ma at 28 v-dc
Turn on time	8.3 ms max at 60 Hz	8.3 ms max at 60 Hz	8.3 ms max at 60 Hz	0.1–0.5 ms at 10–28 v-dc	0.5 ms max
Turn off time	8.3 ms max at 60 Hz	8.3 ms max at 60 Hz	8.3 ms max at 60 Hz	0.3–0.4 ms at 10–28 v-dc	2.0 ms max

*Higher output ratings available – consult detailed specification.

6MT ORDERING

For pricing and delivery of 6MT I/O modules and the 5TI-25806-XX cable.

Address Enquries to:

In the UK:
Marketing Manager (Ref 309)
EICD – MS45
Texas Instruments
Manton Lane.

Outside the UK:
The Marketing Manager, EICD of your local TI office.

TO BE ANNOUNCED

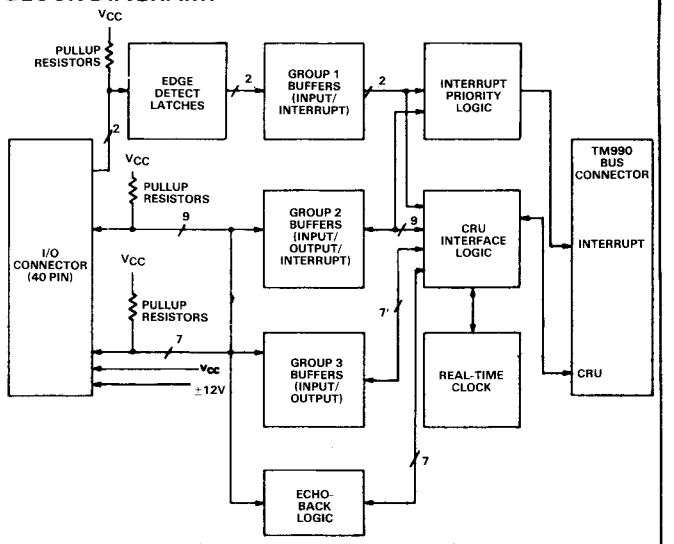
TM990/310

T-BUS PARALLEL INPUT/OUTPUT EXPANDER CARD

FEATURES:

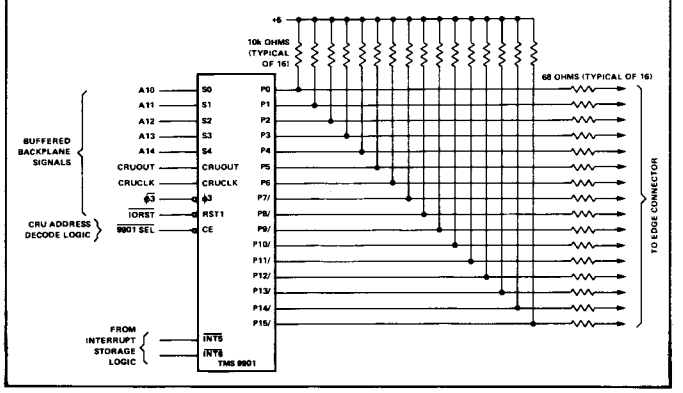
- **48 bits individually programmable as inputs or outputs; 27 of these bits may be programmed as logic-zero-sensitive interrupts, rather than inputs or outputs.**
- **Three negative edge-triggered interrupts and three positive edge-triggered interrupts; each of the six interrupts are edge-detected, stored, and have unique software resets. The edge inputs are pulse shaped by Schmitt trigger circuits.**
- **Backplane interrupt priority is determined by wires installed on two 16-pin platforms.**
- **Board CRU base address is changed by altering the contents of S1, a four-switch DIP.**
- **All 48 input/output signals may be echoed back into the CRU via STCR instructions.**
- **Compatible with TM990 CRU bus.**
- **CRU addressing provided for up to 14 cards per system.**
- **In multiple card I/O systems, CRU addressing can be switch selected such that all CRU addresses are consecutive.**
- **Contains three programmable interval timers.**
- **Plugs into TM990/510 chassis.**
- **Inputs and outputs are TTL compatible.**
- **May be used with wire-wrap, solder, or ribbon cable edge connectors.**
- **+5V, +12V, and −12V are available at the edge connectors.**

BLOCK DIAGRAM:



TM990/310 EXPANSION MODULE, 16 I/O LINES, LOGIC GROUP BLOCK DIAGRAM (ONE OF THREE GROUPS)

INPUT/OUTPUT SCHEMATIC:



DESCRIPTION:

The TM990/310 is a fully assembled, fully tested, input/output expansion module compatible with all TM990 family microcomputer modules. The TM990/310 offers a maximum I/O expansion capability of 48 I/O points, programmable as either inputs or outputs.

The TM990/310 input/output expansion module is implemented using the TM990 printed circuit format. The TM990/310 uses three TMS 9901 LSI programmable systems interface chips to control I/O. The extreme versatility and low cost of the TM990/310 module makes it usable in a wide variety of I/O applications. Inputs and outputs may be mixed in any proportion, and any number of interrupts may be utilized, up to a maximum of 33. The interrupt priority encoding scheme also permits use of the module as an interrupt expander for the TM990/100M microcomputer family.

The TM990/310 expansion module contains three I/O logic groups, each of which interfaces to separate connectors with 16 I/O lines. (Signal and ground are routed for each I/O line, and each line is equipped with pullup resistors). Each I/O group may be programmed as 16 inputs, 16 outputs, nine interrupts, or any combination thereof. Each of the output lines is equipped with an echo back feature which enables the user to read back each bit as it is written to a given output point. In addition, each connector contains a "rising edge" detect interrupt input and a "falling edge" detect interrupt input, along with +5 volts, +12 volts, and −12 volts power supply connections.

ORDERING INFORMATION:

TM990/310 Input/Output Expander Module.

T-BUS PARALLEL INPUT/OUTPUT EXPANDER CARD

FEATURES:

- **Software compatible with I/O and reset features of the TM990/310 I/O module.**
- **Blocks programmed as outputs can be read (echoed) with a CRU input instruction.**
- **Output drivers can be exchanged to provide non-inverting or inverting outputs.**
- **User option of series, pull-up or pull-down resistors on outputs.**
- **+12V, −12V, +8V and +5V are available (at the user's option) at each port's edge connector.**
- **Programmed Inputs:**
  High-level input voltage: 2.0V minimum.
  Low-level input voltage: 0.8V maximum.
  Allowed voltage range: 0.0V to 7.0V.
  Input current (with no pull-up resistors): 20 μA at 2.7.
- **Programmed Outputs:**
  High-level output voltage: 2.4V minimum @ 15 mA maximum.
  Low-level output voltage: 0.50V maximum @ 24 mA.
  Maximum user current sink: 24 mA.

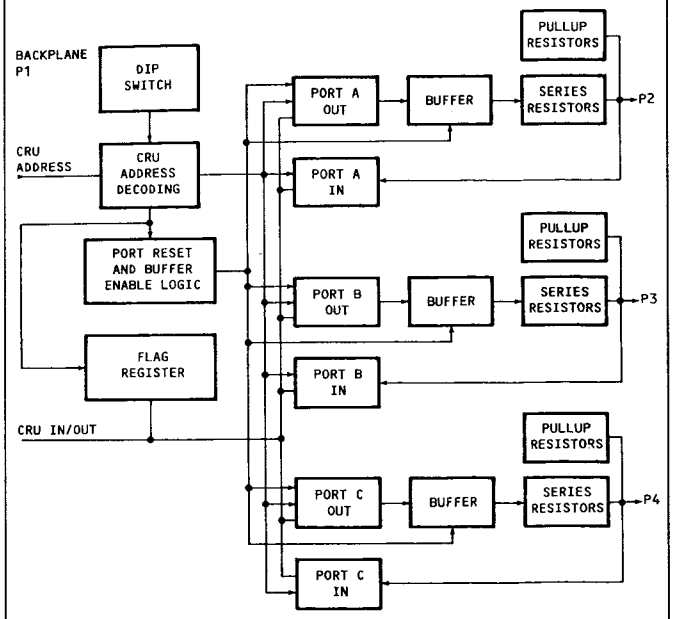
DESCRIPTION:

The TM990/311 is an input/output module designed for use with a TM990 CPU module. The module has 48 I/O bits. These bits are organized into 8 bit blocks. Each block is programmable as input or output. Two blocks (of 8 bits each) make up a port. Each port has its own unique switch-selectable CRU base address. There are three ports, each port occupying one of the three edge connectors.

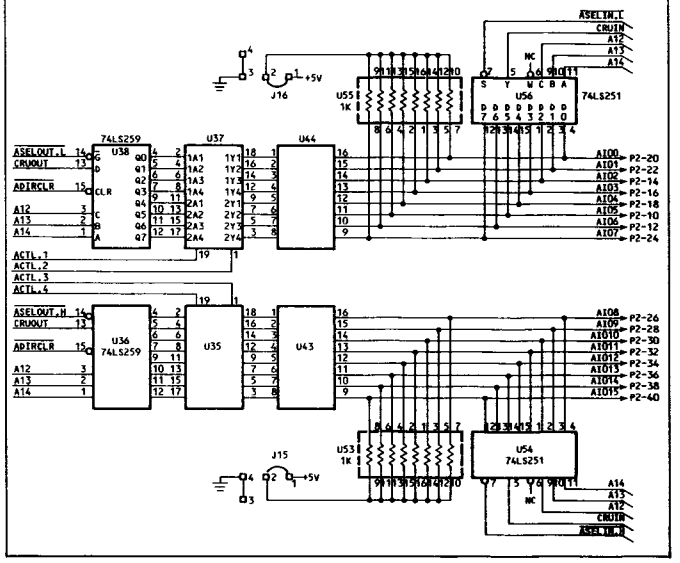
ORDERING INFORMATION:

TM990/311 Parallel Input/Output expansion.

BLOCK DIAGRAM:



INPUT/OUTPUT LATCHES AND BUFFERS:



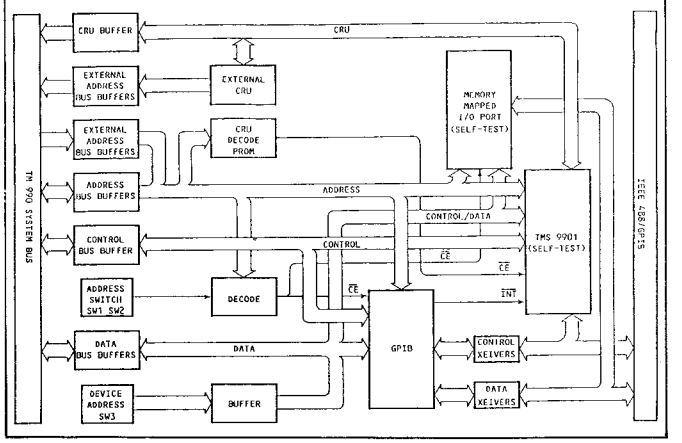
TM990/314

GENERAL PURPOSE INTERFACE BUS (GPIB) INTERFACE MODULE

FEATURES:

- **Memory-mapped I/O port to the TM990 System.**
- **Can act as System Controller, Listener, Talker or Controller.**
- **Self-diagnostic mode to verify proper board operation.**
- **Up to 15 instruments can communicate on common bus.**
- **IEEE Standard 488-1978 compatible.**

BLOCK DIAGRAM:



DESCRIPTION:

The TM990/314 is an adaptor module which enables a user to interface a TM990 CPU to the General Purpose Interface Bus (GPIB defined by IEEE Standard 488-1978. The GPIB is designed to allow up to 15 instruments within a localized area to communicate with each other over a common bus. Each device has a unique address (usually set from external switches), to which it responds. Information is transmitted in byte serial/bit parallel format and may consist of either device data or interface control information.

Messages may be sent by one device at a time (the Talker) and received by any number of other devices (Listerners). Instructions such as select range, select function, or measurement data for processing or printout may be sent in this way. One of the devices on the bus, designated the Controller in charge, may send interface control messages. Devices can be assigned to the bus as Listerners or Talkers by sending their unique talk or listen addresses, and may be switched between remote and local control.

The bus consists of a 24-wire cable: 8 lines carry data, 8 lines are signal and system grounds, and 8 lines are control lines.

The TM990/314 can function as Listener, Talker, and Controller; and handles all IEEE 488-1978 functions. An interrupt is generated when the GPIB changes state (affecting the board), or the CPU may poll the status registers of the TMS 9914 periodically and take action if needed. Interrupt levels 5 through 12 are jumper selectable.

This module represents a memory-mapped I/O port to the TM990 CPU. It occupies 64 bytes of a 4K I/O page of the memory map. The 14 most significant address bits of a 20-bit address field are decoded to generate a module select signal.

The TM990/314 possesses two eight-bit I/O ports which are used as inputs and outputs to the GPIB port in order to test and verify proper board operation. A TMS 9901 is used to read and drive the eight GPIB control lines (ATN, SRQ, EOI, DAV, NRFD, NDAC, REN and IFC).

POWER REQUIREMENTS (Typical)

+5V ± 3% @ 1.0 A.

ORDERING INFORMATION:

Part number	Description
TM990/314-1	IEEE-488 Interface Module with memory mapped interface.
TM990/536	IEEE-488 Interface Cable (stackable).
TM990/429	TM990/314 Demonstration Software EPROM kit.

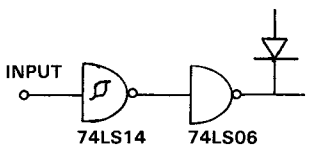
TM990/317

T-BUS COUNTER TIMER MODULE

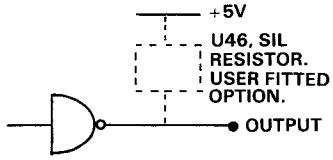
FEATURES:

- 4 TTL software gateable (on/off) counter inputs with programmable debounce filters (0 to 0.2 second time constant).
- 5 independent 16 bit counters with 5 MHz counting rate.
- Up/down and BCD/binary counting capability.
- 16 bit timers with 8 steps of software programmable resolution ranging from 200 nanoseconds to 200 milliseconds.
- Counters may be concatenated to form an effective counter width of up to 80 bits.
- Counters configurable as event counters with softwear programmable leading or trailing edge triggering.
- Counters may be configured to perform time of day clock or watchdog timer functions.
- Alarm comparators on 2 counters.
- 5 outputs connected to counters.
- Complex duty cycle outputs.
- Interrupt and LOAD/RESET capability.

TYPICAL INPUT:

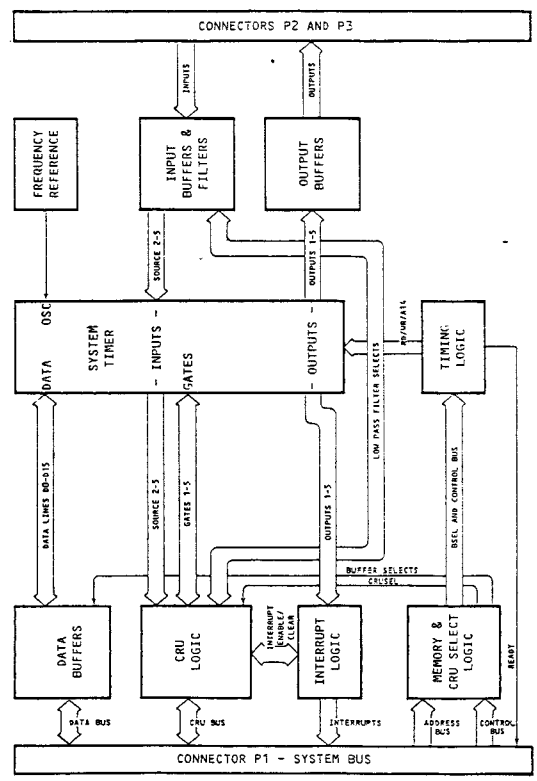


TYPICAL OUTPUT:



7404 FACTORY FITTED
7405, 6, 7, 16 or 18 USER FITTED OPTIONS

BLOCK DIAGRAM:



APPLICATION POSSIBILITIES

Application	Input Device
Shaft position detector	Shaft encoder
Motor speed detector (Tach)	Shaft encoder
Winding counter	Shaft encoder
Process time detector	Shaft encoder
Over speed detector	Shaft encoder
Under speed detector	Shaft encoder
Material length measurement	Shaft encoder with wheel
Skiver Knife controller	Shaft encoder with wheel
Roll radius computer	Two shaft encoders
Ratio detector	Two shaft encoders
Draw measurement	Two shaft encoders with wheels
Fluid velocity detector	Flow encoder
Fluid quantity detector	Flow encoder
Totalizing counter	Any
Event counter	Any
Preset counter	Any
Rate multiplier	Any
Stepper motor timing generator	Any
Motor controller	Any
Brake controller	Any
Clutch controller	Any
Process monitor	Any
Duty cycle detector	Buffered source signal
Frequency meter	Buffered source signal
Clock reference	Internal or external source
Triggered pulse generator	Internal or external source
Baud rate detector	Source signal
Frequency divider	Source signal
80 bit wide counter	Source signal
Reliability monitor	Source signal

GENERAL SPECIFICATIONS:

Power Requirements at +5V ± 3%:
Typical: 0.90 A
Maximum: 1.66 A
Input Frequency: 5 MHz maximum (TTL)
Output Frequency: 1 MHz maximum (TTL)
Operating Temperature: 0°C to 70°C
Storage Temperature: –40°C to 80°C
Humidity: 0 – 95% non-condensing

ORDERING INFORMATION:

TM 990/317 Counter timer module

TO BE ANNOUNCED

TM990/4XX

EPROM SOFTWARE (TM990/400 Series)

TIBUG MONITOR TM990/401-3
TM990/401 is a comprehensive, interactive debug monitor included in the basic price of most TM990 CPU modules. TIBUG includes 13 user commands plus six user accessible utilities and operates with 110, 300, 1200 and 2400 baud terminals.

TIBUG is supplied in two 2708 EPROM's. TIBUG provides a monitor from which other 990/400 Series software modules may be activated. These modules are described below:-

LINE-BY-LINE ASSEMBLER TM990/402
TM990/402 is a line-by-line assembler (no labels) supplied pre-programmed into a ROM kit for immediate system use. By allowing you to enter instructions in mnemonic form and performing simple addres resolution calculations up to a displacement range of +245/—256 bytes, the assembler is an extremely powerful tool for assembly language input of short programs or easy patching of long programs.

DEMONSTRATION SOFTWARE
Demonstration software is available for a number of TM990 microcomputer modules. This software works in conjunction with TIBUG to verify the operation of the TM990 module, and to provide a useful example of how to program the board in a realistic application.

Demonstration software is available for the following boards:-

Board	*Software Part Number*
TM990/303A	**TM990/425**
TM990/306	**TM990/426**
TM990/307	**TM990/427**
TM990/308	**TM990/428**
TM990/314	**TM990/429**
TM990/1481	**TM990/433**

POWER BASIC
TI's POWER BASIC is available in three versions: Evaluation POWER BASIC, Development POWER BASIC and Configurable POWER BASIC.

Evaluation POWER BASIC
Evaluation POWER BASIC (TM990/450) occupies 8K bytes of memory contained in four ROM's. In conjunction with either of the 100 series CPU modules, Evaluation POWER BASIC allows the user to enter and execute various applications programs directly from a terminal or other input device. In addition, the user can store his programs directly on digital cassette via the EIA connector on the module. Evaluation POWER BASIC provides the user with the lowest cost capability for design, development and debugging of POWER BASIC programs.

Development POWER BASIC
Development POWER BASIC (TM990/451) occupies 12K bytes of memory contained in six ROM's Development POWER BASIC provides several advantages over Evaluation POWER BASIC. For example, one can call assembly language programs as subroutines directly from a POWER BASIC program. This feature is particularly useful for subroutines where high speed execution time is critical.

A typical Development POWER BASIC system would include the six ROM's (TM990/451), a 100 series CPU module (i.e. TM990/101M), and a memory expansion board (i.e. TM990/201). In addition to EPROM programming, the POWER BASIC Enhancement Package (TM990/452) provides features not available in Evaluation or Development POWER BASIC, such as print formatting for decimal numbers, and an enhanced set or error messages.

If the user development cycle requires audio cassette storage and EPROM programming, an add-on package to the TM990/451 is available. The POWER BASIC Enhancement Package (TM990/452) works directly with the TM990/451 to provide the user with complete POWER BASIC board level capability – from evaluation to EPROM programming. A typical EPROM programming system would include the TM990/10M module, the TM990/302 software development board, Development POWER BASIC (TM990/451 and the Development POWER BASIC Enhancement Package (TM990/452).

Configurable POWER BASIC
Configurable POWER BASIC (TMSW510F) is our third version of POWER BASIC. Configurable POWER BASIC is a set of floppy diskettes for the FS990 minicomputer. As our most sophisticated POWER BASIC package, Configurable POWER BASIC provides the user with all the statement and library routines available in the ROM resident version of Development POWER BASIC as well as the means to reduce application programs to their minimal memory requirements.

The user can write a program in POWER BASIC, eliminate unnecessary library and statement routines through the Configurator, and then "burn" the application program and minimum runtime POWER BASIC interpreter into EPROM's.

E-Pack
The E-Pack contains a powerful 2K Byte monitor (EUROBUG 2), a line by line-assembler and a disassembler in a 4K EPROM module for the E-Series of Texas Instruments. The E-Pack has been developed for the micro computerboard TM990/E150, the small European format (100 mm × 160 mm) offering the user the possibility to input small programs in assembly language.

In addition to the 13 monitor instructions of EUROBUG 2, instructions are available to the user for manipulating a 990 object buffer in the RAM.

SOFTWARE (TM990/4000 Series)

Eurobug 2
EUROBUG 2 is an interactive DEBUG monitor for the E-series of Texas Instruments' TM990 family, and requires 2K byte of EPROM. It presents to the user an interactive service interface, allowing programs to be loaded from cassette or punch tape, tested, and finally, stored again in absolute object code. During the test phase, EUROBUG 2 permits inspection or change of: locations in memory, work-space registers, and input/output registers (CRU). User programs can be run in single or multi step modes, or with up to two breakpoints. There are a total of 13 monitor commands available.

ORDERING INFORMATION:

TM990/401-3	TIBUG for TM990/10X.
TM990/402-1	TIBUG for TM990/10X.
TM990/402-2	TIBUG for TM990/180M.
TM990/403	TIBUG monitor for TM990/1481.
TM990/425	Demonstration S/W for TM990/303A.
TM990/426	Demonstration S/W for TM990/306.
TM990/427	Demonstration S/W for TM990/307.
TM990/428	Demonstration S/W for TM990/308.
TM990/429	Demonstration S/W for TM990/314.
TM990/433	Demonstration S/W for TM990/1481.
TM990/450	Evaluation Power Basic.
TM990/451D	Development Power Basic.
TM990/452	Enhancement Power Basic.
TM990/4003	EUROBUG II.
TM990/4004	EPACK

CARD CAGES

PARAMETER	TM990/510A	TM990/520A	TM990/530
Number of Card Slots	4	8	16
Card Slot Spacing	1.00"	0.75"	1.00"
Approximate Dimensions:			
Height	12.55"	12.55"	12.00"
Width	5.01"	8.25"	17.25"
Depth*	7.43"	7.43"	12.00"
Mounting Provisions:			
Panel Mount	Y	Y	Y
19" Rack Mount	N	N	Y

*Does not include terminal strip.

Because the TM990 chassis have termination networks, they do consume a small amount of power. The +5 volt dc requirement is 0.24 A (typical). This should be added to the system power requirements.

TM990/531 Power supply mounting bracket for use with TM990/530.
TM990/532 Fan mounting bracket for use with TM990/530.

SYSTEMS ENCLOSURE

The TM990/522 System Enclosure is a self-contained enclosure with card cage, power supply, fan, and front panel. The 4-slot card cage can accommodate any of the TM990 family of microcomputers, memory, I/O, or peripheral interface modules, up to the 75 watt power supply maximum.

ORDERING INFORMATION:

TM990/522

CONNECTORS

A variety of connector kits are available for system development. The TM990 bus required 100 lines, the EIA connector requires 25 lines and 40 lines are required for I/O or interrupt. The bus connector is a 100-pin printed circuit tab on 0.125 inch centres. The 40-pin, printed circuit tab connectors for I/O or interrupt are on 0.10 inch centres. Additionally, the CPU modules come mounted with a 25-pin EIA connector, and the universal prototyping boards have space for mounting the same. The TM990/501 is a three piece connector kit. It includes one each of the 100, 40, and 25-pin connectors. Following is a list of the connector kits that are available:

TM990/501 25 Pin EIA, 40 Pin, and 100 Pin Connectors
TM990/523 100 Pin Connector Kit
TM990/524 40 Pin Connector Kit
TM990/525 25 Pin EIA Connector Kit
TM990/528 50 Pin Connector Kit

POWER SUPPLIES

Texas Instruments provides two power supplies to be used with the TM990 Series Modules. The TM990/519 is a low current version that was especially designed to be used with the TM990/189 University Board. The TM990/518 provides a higher current output and is especially suited for use with the TM 990/302 software development module. The TM990/518A is an enclosed version of the TM990/518 but with a lower power rating.

DC POWER SUPPLY SPECIFICATIONS

Power Supply	+5V	−12V	+12V	+45V
TM990/518	6.0 A	0.9 A	0.9 A	0.1 A
TM990/518A	4.0 A	0.4 A	0.6 A	0.1 A
TM990/519	2.0 A	0.18 A	0.25 A	

CABLES

Part Number	Description
TM990/502	Cable to connect TM990 CPU module to a RS-232-C terminal. Also used with TM990/308 to interface to Bell 208 modem.
TM990/503A	Cable to connect TM990 Series CPU module to a Texas instruments 743 or 745 terminal.
TM990/504A	Cable to connect a TM990/10X series CPU module to a Model 33 ASR teletype modified for 20 mA current loop operation.
TM990/505	Cable to connect a TM990 CPU module with a Texas Instruments Model 733 ASR data terminal.
TM990/506	Cable to connect port P3 of the TM990/101MA CPU module to a RS-232-C modem such as a 103 type data set.
TM990/507	Cable to connect TM990/100MA, TM990/101MA, or TM990/310 I/O Module to TM990/5MT industrial I/O interface.

Part Number	Description
TM990/508	Audio cassette interface cable to be used with the TM990/302 software development module.
TM990/509	Cable to connect TM990/305 I/O Module to TM990/5MT industrial I/O interfaces.
TM990/527	Cable to connect TM990/303A Floppy Disk Controller to one or two standard size (8") drives.
TM990/535	Cable to connect TM990/303A Floppy Disk Controller to three Shuggart Model 400 Disk Drives.
TM990/536	IEEE-488 Interface Cable for use with the TM990/314 IEEE-488 Interface Module.
TM990/538	25-pin Extension Cable for use with the TM990/522 System Enclosure.

AUXILIARY MODULES

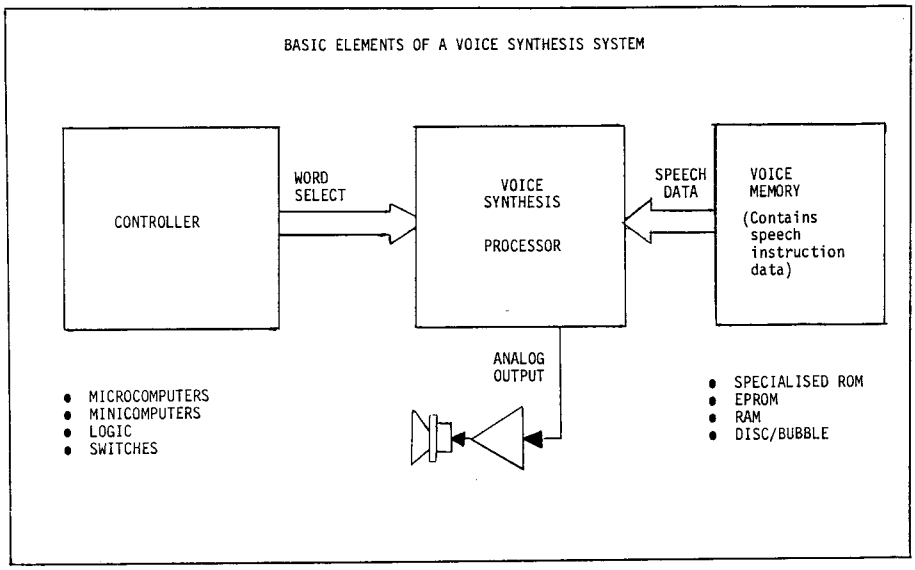
Part number	Description
TM990/511	Extender board for operating TM990 modules outside card cage; includes card guide.
TM990/512	Universal prototyping board for T-FORMAT cards without wire wrap pins.
TM990/513	Universal prototyping board for T-FORMAT cards with wire wrap pins.

Section 5 Speech synthesis

SOLID STATE SPEECH

An introduction to voice synthesis technology

Since the mid-seventies, Texas Instruments has been actively involved in developing voice synthesis technology – solid state voices for machines. In 1978 the first result of these developments was the introduction of the world's first toy with a solid state voice, SPEAK 'N' SPELL™. Since then TI has continued to develop new innovative speech products and systems, and today TI offers the broadest range of products and services on the market; from voice synthesiser chips, to specialised voice memories, to speech boards, plus word library facilities, custom speech processing and even speech development laboratories, which allow anyone to develop his own electronic speech in the same way that today he can write a microprocessor program.



A VOICE SYNTHESIS SYSTEM USES SPEECH INSTRUCTION DATA STORED IN MEMORY TOGETHER WITH A VOICE SYNTHESIS PROCESSOR TO RECREATE THE HUMAN VOICE.

How is it done?

Linear predictive coding (LPC) reduces the amount of data required to store a second of speech by a factor of about 100 over normal digitisation methods, so 1 second of speech takes typically only 1K bits to store. It does this by extracting pitch, energy and vocal tract filter information from human speech recordings to produce 'speech instruction data'. This data can then be used with a voice synthesiser i.c. to recreate the human voice.

Basic Elements of a Speech System

The heart of the system is the Voice Synthesis Processor (VSP) which imitates the action of the human vocal system. Speech instruction data is stored in the memory which controls an oscillator, white noise source, and 10-pole lattice filter on the VSP. A controller provides the start address of speech data in memory and makes the VSP 'speak' at the appropriate command.

1. GETTING STARTED

The cheapest and most simple introduction to speech synthesis is the TINYTALKER, a self-contained unit which speaks 1-of-8 phrases at the touch of a button. It uses the TMS 5100 VSP voice synthesis processor.

To produce a more sophisticated evaluation tool, the TMS 5100 can be used with some extra TTL packages and additional speech data in EPROMS to build a general purpose speech peripheral for a microprocessor based system.

2. THE DESIGN STAGE

Speech instruction data in the form of individual words is readily available from a selection of over 1000 words in the TI speech library run by TI's distributors. Custom speech data can easily be produced by TI when the words or phrases required for a particular application are not available in the library.

3. PRODUCTION

High Volume

The most cost-effective solution for a high volume (>3000 units) application is a 3 chip one comprising a customised TMS 1000 microcomputer, a TMS 5100 VSP, and TMS 6100 or TMS 6125 voice memory programmed with a specific word set.

An 'Add-On'

Where there is already a microprocessor in a system, the TMS 5200 VSP is normally the best solution because it has an on-board 8-bit data bus buffer. It is interrupt driven and connects directly to the data bus. Speech data is stored in the main program memory and fed to the TMS 5200 by the Host Processor, or from a masked TMS 6100 or TMS 6125.

Low Volume

Where a standalone low volume system is required for experimenting or production, a standard TMS 1000 microcontroller is available. This type of system uses TMS 5100 and speech instruction data in EPROMS and can be configured with a 'vector map' in the EPROM to be driven by a keyboard or digital inputs. This map can be generated on the TI library computer.

WORDS (1)

'CUSTOM' SPEECH DATA

FEATURES:

- **Any word, phrase or language produced to specification.**
- **Speech data editing gives extremely high quality reproduction.**
- **Low data rate (900 to 1600 BPS).**
- **Male or female voice.**
- **Speaker may be anyone with suitable voice pattern.**

DESCRIPTION:

'Custom' words and phrases for any application can be generated by Texas Instruments according to the requirements of the system. Expert TI speakers are used to record customer-specified vocabularies, or the customers own chosen speaker may be trained and used, providing his or her voice lies within the vocal capability of the voice processor.

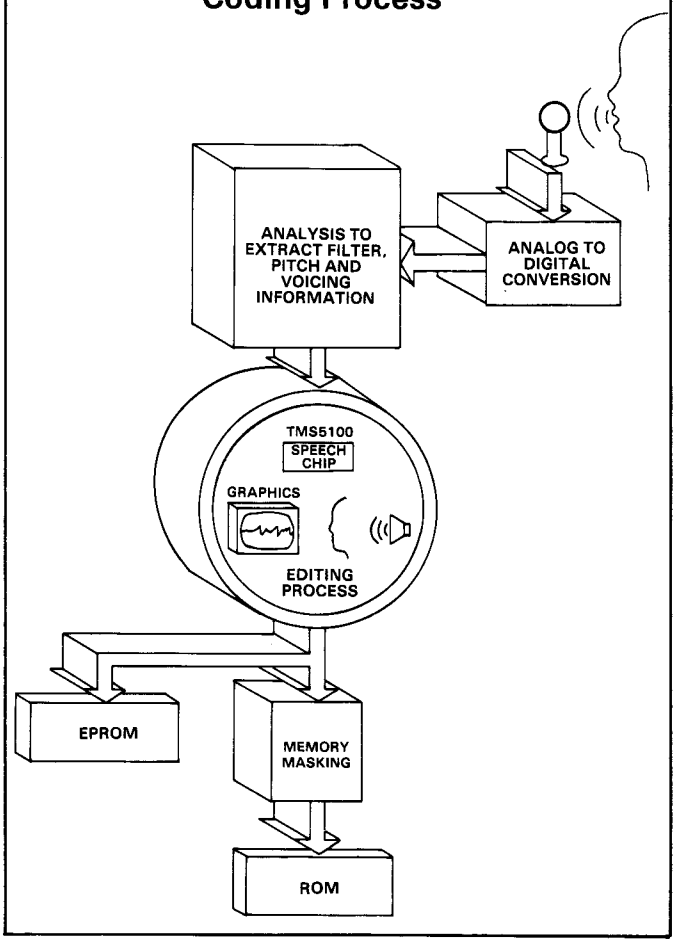
Once the required speech set has been determined, it may be recorded on a high-quality tape recorder in a professional recording studio.

The recorded speech is digitized and fed into a computer. Once in the computer, the digitized speech can be analysed to extract filter, pitch and voicing information and edited to further increase the speech quality.

The speech data thus obtained may then be evaluated by the customer in his target system and if necessary re-edited to meet the customers final specification. It is usually advisable for the customer to be present at this final stage.

The whole speech analysis procedure may be carried out separately by the customer using TI's speech development system. This is based on the AMPL computer and further details are given in a separate section.

TI's Speech Analysis and Coding Process



ORDERING INFORMATION:

When ready to order a Solid State Speech vocabulary, a final word/phrase list should be prepared, with separate sections for words and phrases. Any desired accents must be clearly specified for each word/phrase. If specific words will be used in a unique context, such as the object of a common subject and verb, the complete context should be given for the word. For example:

"CLOSE THE . . . DOOR"
". . . WINDOW"
". . . BLINDS"

would be specified as follows:

Phrase Section:
1. Close the . . . (door, window, etc.)

Word Section:
1. Door (Close the door)
2. Window (Close the window)
3. Blinds (Close the blinds)

There is a trade-off inherent in the customization of vocabularies. Single words offer memory savings and flexibility, while phrases yield more natural inflection.
Texas Instruments has a team of experienced engineers in Bedford who are able to give advice on developing custom speech data. For further information please contact TI directly.

FEATURES:

- **A library of common words already digitised.**
- **Nearly 1,000 words available.**
- **Low cost.**
- **Available through distributors.**
- **Words supplied in EPROM's.**
- **Facility to program EPROM's in Tinytalker or Superspeaker format.**
- **Suitable even for 'one-off' applications.**

DESCRIPTION:

The "off-the-shelf" speech library is a service offered by Texas Instruments franchised distributors.

It is suitable for experimenting with voice synthesis or developing prototype or production systems.

A wide selection of words is available in the form of speech instruction data suitable for use with the TI voice synthesis chips.

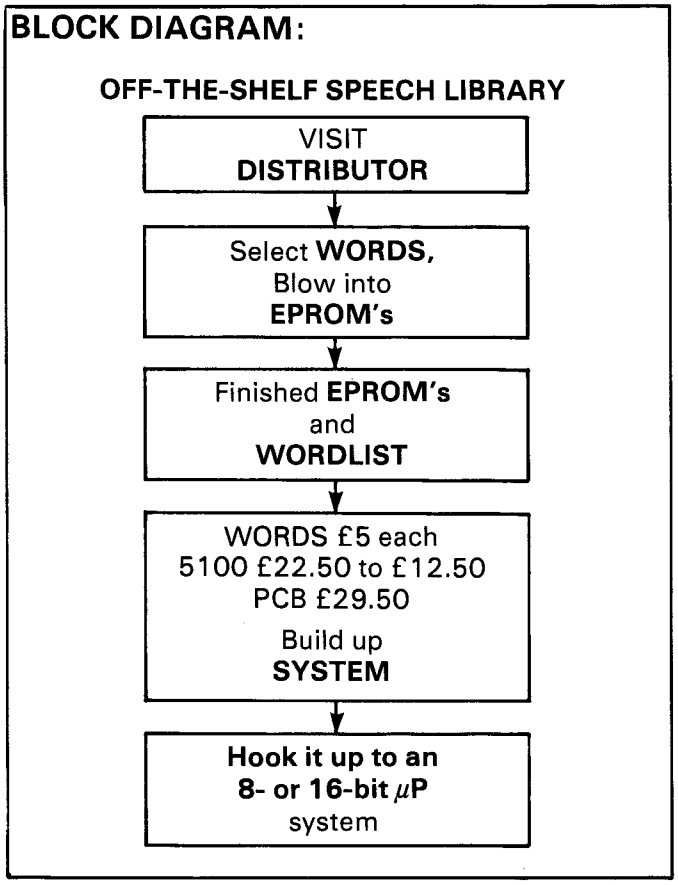
The potential user can select only those words he requires for his application, and these are supplied in EPROM form, together with all the necessary documentation.

The speech instruction data is stored on an AMPL system, and a potential user may visit the distributor and listen to and select words from the master library. Alternatively he may select them by post.

Words may be concatenated together to form sentences as part of the service, or they may be supplied to use with the Superspeaker or TINYTALKER modules.

Details of how to build a simple speech peripheral for a microcomputer are given in the TI application note No. B214 "A general purpose Speech Synthesis Peripheral".

BLOCK DIAGRAM:



ORDERING INFORMATION:

Speech instruction data from the TI "off-the-shelf" word library may be obtained from TI's franchised distributors and they should be contacted directly for full details of using the service.

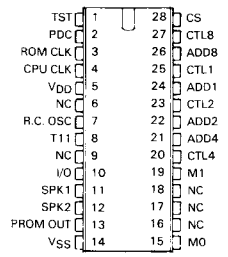
TMS 5100

VOICE SYNTHESIS PROCESSOR

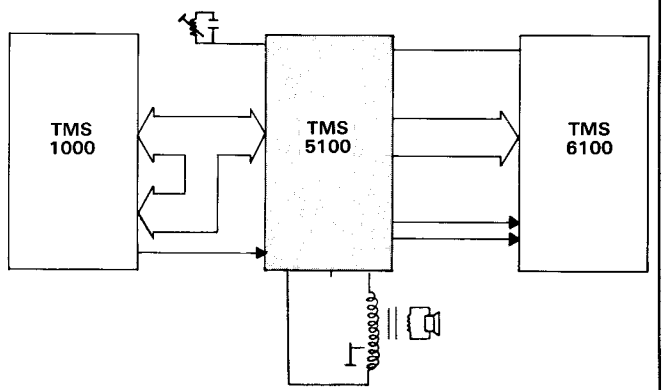
FEATURES:

- **High quality voice synthesis from a microcomputer system.**
- **Low-data-rate LPC encoding.**
- **Low-cost PMOS technology.**
- **Single 9 volts power supply.**
- **On-chip D/A converter and push-pull power amplifier.**

PIN ASSIGNMENTS:



TYPICAL APPLICATION:



THE 3-CHIP SYSTEM

DESCRIPTION:

The TMS 5100 is a single-chip voice synthesis processor (VSP).

Speech is synthesised by processing externally provided speech data and converting the result to an audible output using an on-chip 8-bit d/a converter and push-pull power amplifier.

The TMS 5100 was designed to be used with one or more TMS 6100 voice synthesis memories (VSM) and therefore outputs all control signals necessary for direct interface to these devices.

The TMS 5100–TMS 6100 operation simply requires a start-address and a 'SPEAK' command in order to say a complete word or phrase from the TMS 6100.

CHARACTERISTICS:

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage	−8.3	−9	−9.7	V
Supply current		−20	−45	mA
Oscillator frequency (RC)	608	640	674	kHz
Operating temperature range	0	25	70	°C

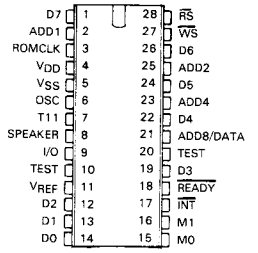
ORDERING INFORMATION:

TMS 5100 NL **600 mil package**
TMS 5100 SL **400 mil package**

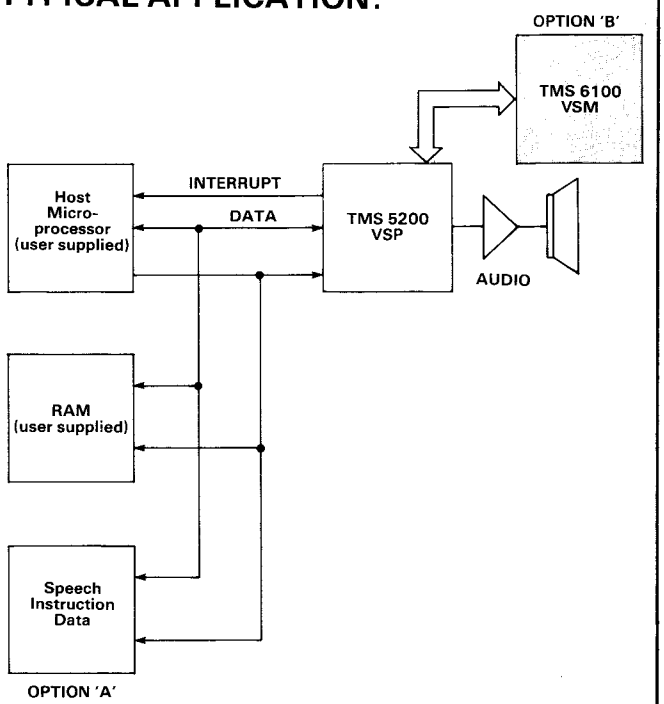
FEATURES:

- **High quality voice synthesis from a microcomputer system.**
- **Low-data-rate LPC encoding.**
- **Low-cost PMOS technology.**
- **+5V and −5V power supplies only.**
- **8-bit data bus compatibility.**
- **TTL compatible.**
- **Male/female voice capability.**
- **Polled, or interrupt-driven.**

PIN ASSIGNMENTS:



TYPICAL APPLICATION:



DESCRIPTION:

The TMS 5200 is a single-chip voice synthesis processor (VSP).

Speech is synthesised by processing externally provided encoded speech data and converting the output to a synthetic speech waveform using an on-chip 8-bit d/a converter.

The TMS 5200 is an ideal add-on to an existing microprocessor system. It supports an 8-bit data bus, through which commands are sent from the host processor. The encoded speech data is stored in memory (EPROM, RAM, ROM, etc.) and is fed to the TMS 5200 via the data bus.

Speech data for the TMS 5200 contains six pitch bits (as opposed to five for the TMS 5100), this improves the speech quality and also allows synthesis of female voices due to its extra frequency range.

CHARACTERISTICS:

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage V_{SS}	4.5	5	5.5	V
Supply voltage V_{DD}	−4.5	−5	−5.5	V
Supply current I_{DD}		10	35	mA
Oscillator frequency (RC)	576	640	704	kHz
Operating temperature range	0	25	70	°C

ORDERING INFORMATION:

TMS 5200 NL **600 mil package**
TMS 5200 SL **400 mil package**

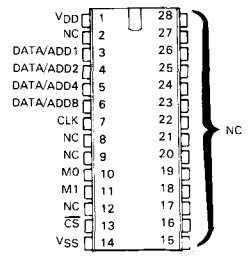
TMS 6100

VOICE SYNTHESIS MEMORY

FEATURES:

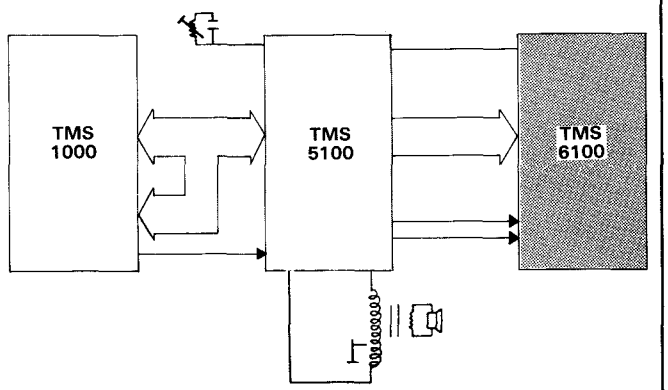
- **128K bit ROM organised as 16K by 8.**
- **Low-cost PMOS technology.**
- **Single 9 volts power supply.**
- **Can contain up to 2 minutes of speech.**

PIN ASSIGNMENTS:



NC = no internal connection

TYPICAL APPLICATION:



THE 3-CHIP SYSTEM

DESCRIPTION:

The TMS 6100 is a PMOS 128K bit Voice Synthesis Memory (VSM), internally organised as 16K by 8.

Externally it appears as either a one-bit (serial) or four-bit (parallel) output.

Data can be read out either one bit or one nibble at a time. After eight bits or two nibbles have been read, the address is internally incremented. This output option (one bit or four bits) is chosen at the time of manufacture.

Up to 4 TMS 6100's may be used in parallel in one system giving a total unrepeated speech time of approximately 8 minutes.

Consult TI for information about the availability of TMS 6100's with standard vocabularies.

CHARACTERISTICS:

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage	−8.3	−9	−9.7	V
Supply current			−10	mA
Operating temperature range	0	25	70	°C

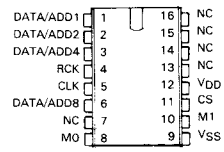
ORDERING INFORMATION:

TMS 6100 NL **600 mil package**
TMS 6100 SL **400 mil package** **(custom parts will be assigned a VM 6XXXX number)**

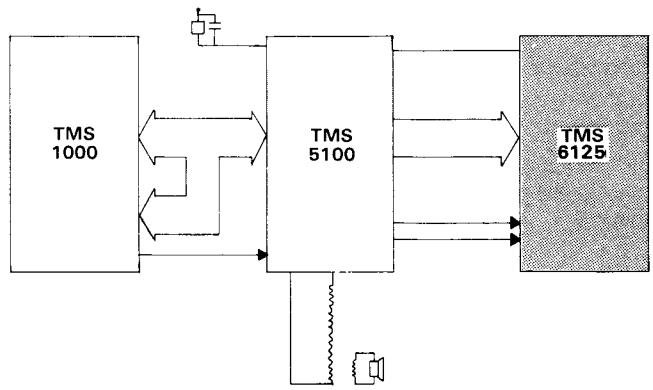
FEATURES:

- **32K bit ROM organised as 4K by 8.**
- **Low-cost PMOS technology.**
- **Single 9 volts power supply.**
- **Can store a 50 word vocabulary.**
- **Smaller, cost-effective alternative to the TMS 6100 where large amounts of speech data are not required.**

PIN ASSIGNMENTS:



TYPICAL APPLICATION:



THE 3-CHIP SYSTEM

DESCRIPTION:

The TMS 6125 is a PMOS 32K bit Voice Synthesis Memory (VSM), internally organised as 4K by 8.

Externally it appears as either a one-bit (serial) or four-bit (parallel) output.

Data can be read out either one bit or one nibble at a time. After eight bits or two nibbles have been read, the address is internally incremented. This output option (one bit or four bits) is chosen at the time of manufacture.

Up to 4 TMS 6125's may be used in parallel in one system giving a total unrepeated speech time of approximately 2 minutes.

CHARACTERISTICS:

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage	−8.3	−9	−9.7	V
Operating temperature range	0	25	70	°C

ORDERING INFORMATION:

The following standard TMS 6125 VROMS are available with pre-programmed American voice speech sets for small volume application:

VM 71001
VM 71002
VM 71003

For high volume applications (those requiring more than 5,000 units) custom ROM's may be produced using standard speech library words or custom encoded speech. The speech instruction data supplied to Texas Instruments is used to generate photomasks and produce custom ROM's. This takes between 14 to 16 weeks.

TMS 5220A

PRELIMINARY INFORMATION

VOICE SYNTHESIS PROCESSOR

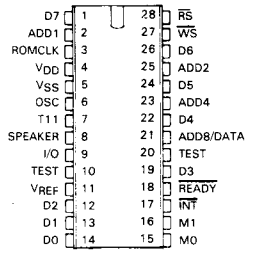
FEATURES:

- **High quality LPC-10 voice synthesis.**
- **Allophone capability.**
- **8-bit data bus interface.**
- **PMOS technology.**
- **28 pin DIL package.**

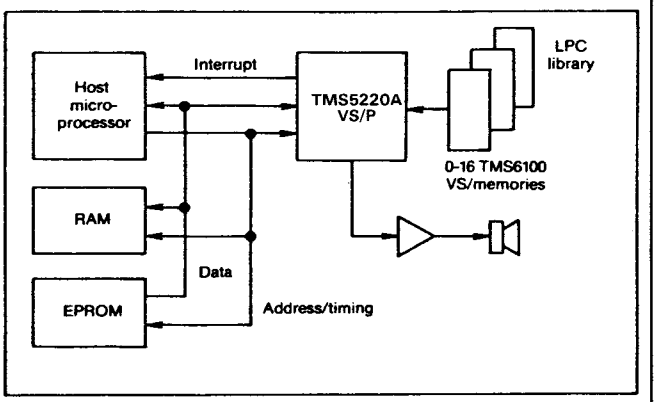
DESCRIPTION:

The TMS 5220A can operate in a high-quality LPC system, in a medium quality allophonic system, or in a combination system, with a minimum of external controller suspension. Because of recent improvements in speech synthesis, ASCII-Keyboard entered or stored test material can be converted to relatively high-quality speech at modest-cost, by stringing together speech sound components called allophones. The TMS 5220A can operate in a combined allophonic – LPC mode to produce male, female or children's voices.

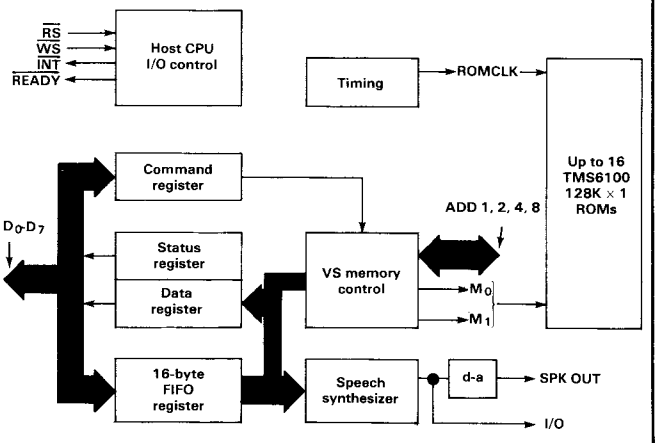
PIN ASSIGNMENTS:



TYPICAL APPLICATION:



BLOCK DIAGRAM:



CHARACTERISTICS:

Supply voltage V_{SS} (av)	+5V
Supply voltage V_{DD} (av)	−5V
Supply current I_{DD}	10 mA
Oscillator frequency	640 kHz
Temperature range	0–70°C

This part will be available early in 1982.

ORDERING INFORMATION:

TMS 5220A NL **600 mil package**
TMS 5220A SL **400 mil package**

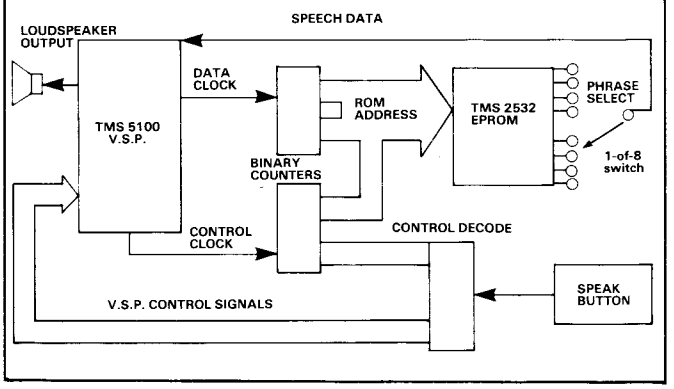
TINYTALKER

SPEECH EVALUATION BOARD

FEATURES:

- **Ready built and tested low-cost evaluation board.**
- **Up to 32 seconds of speech.**
- **8 selectable words/phrases.**
- **Speech easily customised to application.**
- **Single 9 volts power supply.**
- **Activated by switches or TTL voltage levels.**
- **Low chip-count – voice synthesis processor + EPROM + 3 standard TTL packages.**

BLOCK DIAGRAM:



DESCRIPTION:

Tinytalker is a simple low-cost speech unit, able to speak words and phrases without having to use a microprocessor. It is supplied with eight phrases stored in a TMS 2532 EPROM but any suitable data from TI's speech data library may be used.

Each phrase can be over four seconds long due to the high data compression achieved by TI's LPC coding technique. The module's phrase selection can be simply increased with further EPROM's, either TMS 2532's, or TMS 2516's for shorter phrases.

If control of the module by a microprocessor is required, the addition of a TTL part buffers the module for interface to any parallel output port. This is the ideal solution for low/medium volume products needing a number of 'canned' phrases; warning systems and video games are typical examples.

An evaluation EPROM is available with the TINYTALKER, other phrases can be constructed from individual words in the extensive Speech library supported by TI's franchised distributors. For production systems the required phrases can be custom synthesised to a particular customers requirements.

Tinytalker has a power amplifier and loudspeaker mounted on the circuit board, so to get the system up and running, all that is required is a single 9 volts power supply.

ORDERING INFORMATION:

Order Code: TINY-TALKER-ø1

SUPERSPEAKER

PROGRAMMABLE VOICE COMPUTER

FEATURES:

- **Intelligent, reconfigurable add-on speech module.**
- **Operation by keyboard, microprocessor or digital inputs (external events).**
- **Configured through vector map.**
- **Standard or custom speech data sets available.**
- **Speaks up to 128 words or phrases.**
- **Several modes of actuation – including leading or trailing edge triggered inputs and programmable switch debounce time.**
- **Programmable 'audio attributes' – alarm option, repeat facility, combined repeat/alarm and word concatenation.**
- **'Wake-up' speech option.**
- **Up to 32 queued speech commands.**

DESCRIPTION:

Superspeaker is a self-contained add-on speech unit based around the TMS 1100 microcomputer and TMS 5100 Voice Synthesis Processor (VSP). It is capable of speaking 128 words or phrases depending upon particular event conditions.

Superspeaker may be controlled by the on-board keypad, digital inputs from external circuitry or by the in-circuit 8-bit microprocessor interface.

The system speech data is contained in EPROM and can contain the standard data set or may be configured with custom words and phrases from TI's speech data library using the ORATOR Custom Speech Development System.

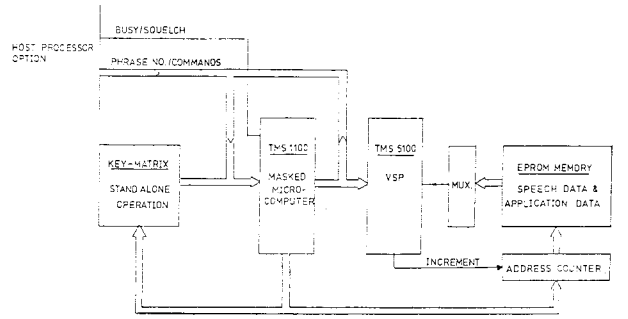
The Superspeaker options may be selected by the user by use of an EPROM vector map to suit his particular system requirements. These options allow incoming signals to be recognised on their leading or trailing edges, variable timing on switch debouncing, variable timing on alarm signal and repeat functions and programmable word concatenation.

The advantage of Superspeaker is its extreme flexibility and as such may be incorporated into many different types of system.

ORDERING INFORMATION:

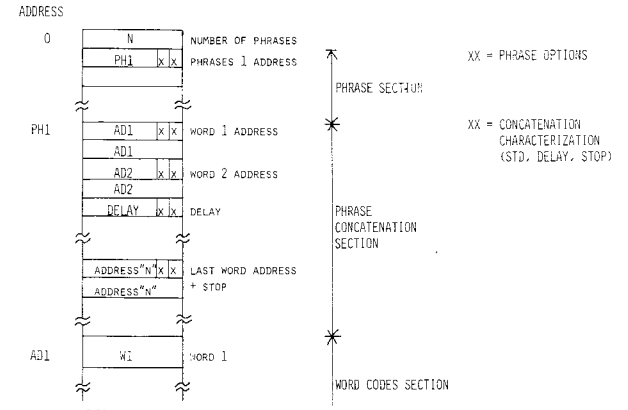
Part No. SUPER-SPEAK-ø1

BLOCK DIAGRAM:



EPROM BASED SPEECH MODULE PROGRAMMABLE VOICE COMPUTER

VECTOR MAP:



MEMORY ORGANISATION "VECTOR MAP"

PHROM EMULATOR

VOICE SYNTHESIS MEMORY EMULATOR BOARD

FEATURES:

- **Single-board emulation of TMS 6100 voice synthesis memory.**
- **Allows full in-circuit emulation of VSM with speech and system data resident in EPROM.**
- **TMS 6100 chip enable switch selectable.**
- **Speech data easily updated before final masking decision is made.**
- **Single 5 volts power supply.**

DESCRIPTION:

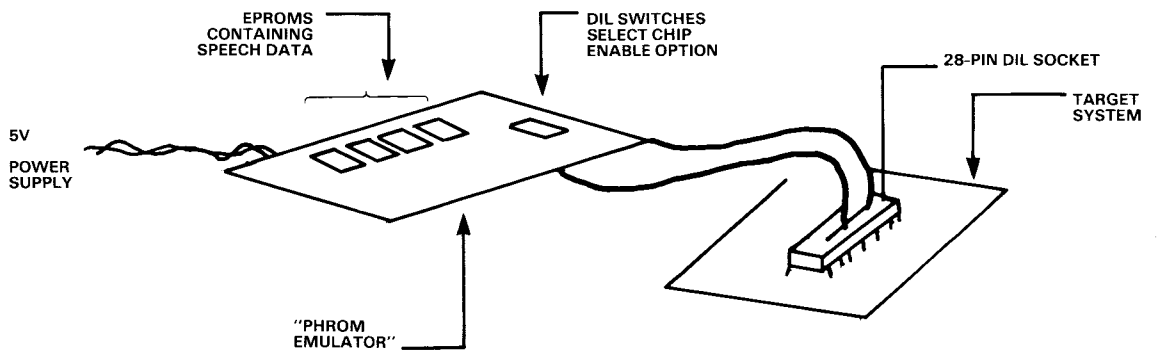
The Voice Synthesis Memory (VSM) emulator is a single-board TTL + EPROM emulation of the TMS 6100 VSM.

The speech data is contained in four TMS 2532 32K bit EPROMS to give the total data capacity of 128K bits of the TMS 6100.

The mask programmable chip enable option of the TMS 6100 is selectable by dual-in-line switches on the circuit board. This allows up to sixteen emulators to be used in the same system, as with the actual TMS 6100 part.

The emulator requires only a single 5 volts power supply. All other interfacing signals are transmitted to and from the board via a ribbon cable, which connects directly to the 28 pin TMS 6100 socket on the target system.

TYPICAL APPLICATION:



ORDERING INFORMATION:

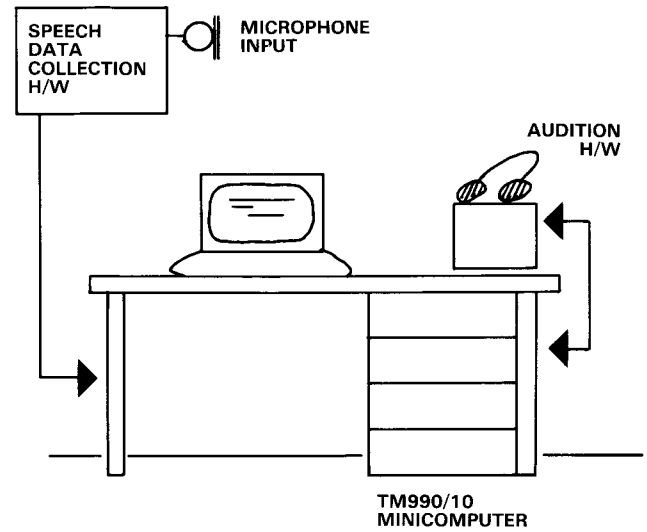
PHROM-EMU-1

SPEECH DEVELOPMENT LABORATORY

FEATURES:

- **A complete speech data development system.**
- **Designed around AMPL minicomputer.**
- **Direct voice or recorded input.**
- **Audio output via loudspeaker or headphones.**
- **Supports all TI Speech Synthesis chips.**
- **Full LPC-10 editing facilities.**
- **Allophone and Phoneme capability.**
- **Normal and slow speed audition feature.**
- **Full analysis capability.**

BLOCK DIAGRAM:



DESCRIPTION:

The speech development laboratory allows speech instruction data to be developed totally independently from TI. This obviously allows greater flexibility and control over the process. The user is able to experiment with the speech data using the editing facilities to obtain exactly the quality of speech he requires.

Further details of the AMPL system may be found in the section on development systems.

ORDERING INFORMATION:

For more details and availability on this system, please contact TI directly.

THE MAN MACHINE INTERFACE

SPEECH CAN BE USED WHERE THERE IS:

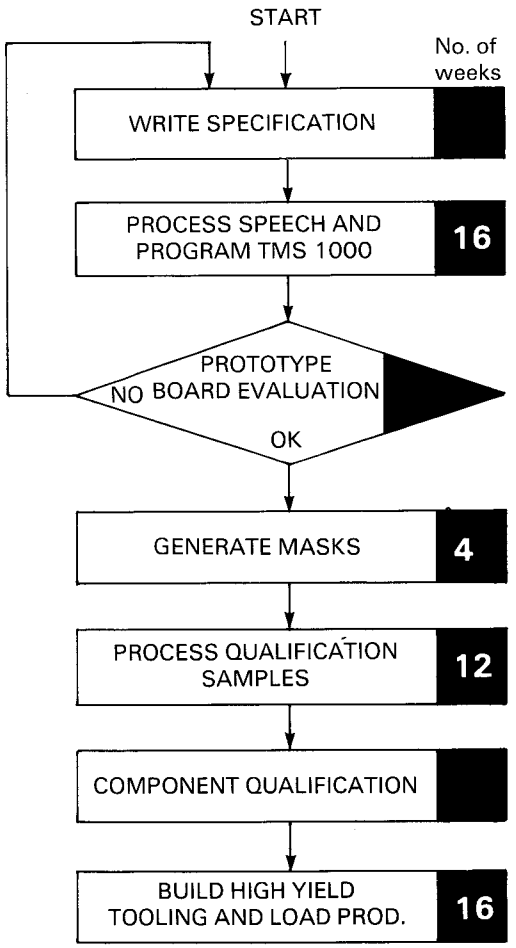
- A NEED TO REINFORCE A VISUAL DISPLAY.
- A NEED TO SUPPLY MORE COMPLEX INFORMATION.
- POOR LIGHTING.
- HAND EYE COORDINATION REQUIRED.
- VOICE NORMALLY USED AS TRANSMISSION MEDIUM.
- WARNING APPLICATION.
- A NOVEL PRODUCT.
- INSTRUCTION REQUIRED – STEP-BY-STEP.
- DISABLED OPERATORS.

APPLICATIONS OF VOICE SYNTHESIS

INDUSTRIAL:	INSTRUCTIONS FOR COMPLEX MACHINERY; ALARMS/WARNING SYSTEMS; PRODUCTION LINE/ PROCESS CONTROL; METERS; DARKROOM AIDS; . . .
TELECOMMS:	ANSWERING MACHINES; SECURITY ALARMS; INFORMATION SYSTEMS; PABX's.
AUTOMOTIVE:	DASHBOARD; MPG METERS; SERVICE AIDS; INFORMATION SYSTEMS.
CONSUMER:	WASHING MACHINES; COOKERS; TOYS; . . .
COMPUTERS:	TRANSACTION TERMINALS; BANKING TERMINALS; WORD PROCESSORS.

16

DEVELOPMENT CYCLE FOR THE '3-CHIP' SYSTEM



No. of weeks	RESPONSIBILITY	OUTPUT
	CUSTOMER	COMPLETE WRITTEN FUNCTIONAL SPECIFICATION OF SYSTEM PERFORMANCE
16	TI	SPEECH AND TMS 1000 EPROM's
	CUSTOMER	SPEC. RELEASED FOR MASK GENERATION
4	TI	
12	TI	10 QUAL KITS
	CUSTOMER	FORMAL RELEASE TO PRODUCTION
16	TI	FIRST PRODUCTION OUTPUT
48	TOTAL	

Section 6 Development Systems and Software

AMPL

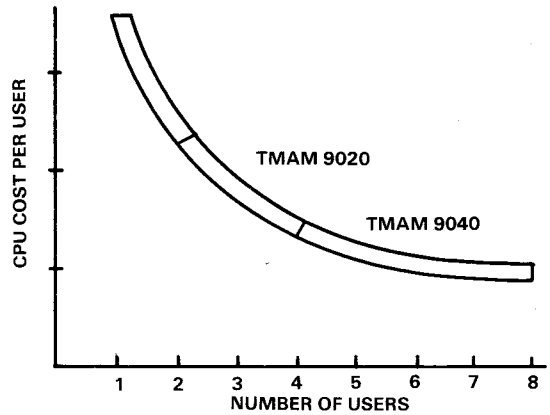
ADVANCED MICROPROCESSOR PROTOTYPING LABORATORY

The AMPL range meets all the requirements for development of systems using TI microprocessors and microcomputers. An AMPL development system is based on a TI minicomputer running AMPLUS software. To this an AMPL station may be added to integrate target software and hardware, providing full-speed in-circuit emulation.

All of TI's Component Software packages and high-level languages like Microprocessor Pascal are fully supported.

AMPL SUPPORTS THESE PROCESSORS:
***TMS 9995**
TMS 9900
TMS 9940
TMS 9980A
TMS 9981
SBP 9900/SBP 9989
***TMS 1000 SERIES**
***TMS 7000 SERIES**
***TMS 5100 SERIES SPEECH PROCESSORS**

**NEW AMPL PRODUCTS*



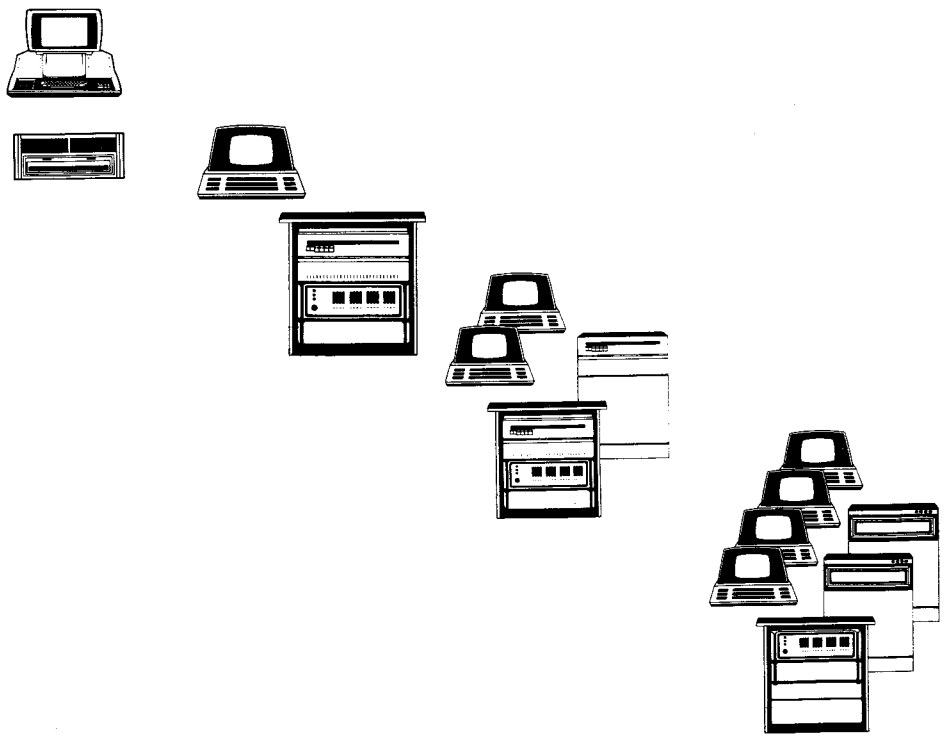
System cost per user

For a single user, the AMPL software development system consists of a table top console and dual floppy disc drive. For more than one user, MULTI-AMPL systems use hard disc storage and pooled resources to cut costs.

The table shows the range of development systems available. Details on each system may be found on the following pages. Systems may be upgraded from TMAM 9010 through TMAM 9020 up to full TMAM 9040 systems.

AMPL SYSTEMS

DESCRIPTION	TMAM 9001	TMAM 9010	TMAM 9020	TMAM 9040
Main memory (Bytes)	64K	256K	256K	320K
Mass storage	DSDD floppy	Hard disc	Hard disc	Hard disc
Total disc storage (formatted bytes)	2.2M	9.0M	18.0M	85.2M
No. of disc drives	1 (dual)	1 (dual)	2 (dual)	2
Fixed storage		1 × 4.5M	2 × 4.5M	
Removable storage	2 × 1.1M	1 × 4.5M	2 × 4.5M	2 × 42.6M
Number of terminals included	1	1	2	4
Number of users with extra termninals	–	2	4	8+



All systems support AMPL hardware stations, printers and PROM programming.

MULTI-AMPL systems support extra terminals and many other peripherals.

Included in the price of a MULTI-AMPL system is a site survey, installation and system generation of the AMPLUS software.

90 day warranty

To enable you to get the best out of your AMPL system training courses are run at Bedford. See courses page.

For ordering information refer to the individual system pages.

TMAM 9001

SINGLE-USER DEVELOPMENT SYSTEM

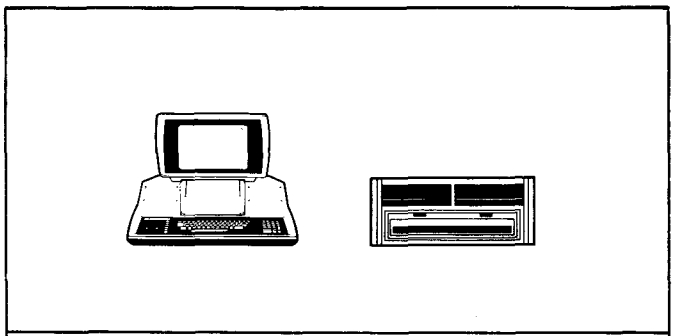
FEATURES:

TMAM 9001 consists of:

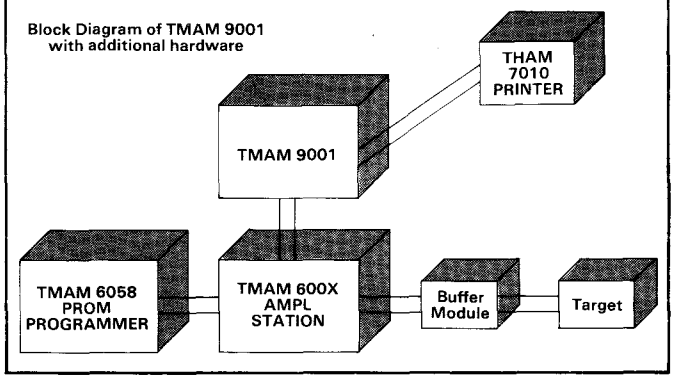
- **Desk top computer console with integral keyboard and video display terminal.**
- **Dual FD1000 double density, double sided diskette drives, giving 2.2M bytes of formatted on-line storage.**
- **Interactive AMPLUS software on a single diskette. Just load and go.**
- **Interface for AMPL station and printer.**

TMAM 9001 is a single-user development system. The software is configured to support an AMPL station, printer and PROM programmer. The prom programmer plugs into an AMPL station.

TMAM 600X series AMPL stations add hardware emulation and logic state trace facilities to the TMAM 9001. Under control of the AMPL utility, target hardware and software can be tested then integrated.



Block Diagram of TMAM 9001 with additional hardware



OPTIONS:

- **TMAM 7010 150 character/s printer**
- **TMAM 600X AMPL stations**
- **TMAM 6058 prom programming kit**

DESCRIPTION:

AMPLUS SOFTWARE
The AMPLUS software supplied with the TMAM 9001 provides the following:

MENU BASED OPERATING SYSTEM
When the TMAM 9001 is turned on, AMPLUS loads automatically and displays a menu of commands. All utilities have their own menus so available commands are always displayed on the screen. Most commands prompt for inputs and many display default values. This means that it is not necessary to remember complex syntax.

SCREEN-BASED TEXT EDITOR
In any system the most used utility is the text editor. Much thought has gone into an editor that is easy and fast to use. Data is entered simply by typing it in. Changes are made by moving the cursor on the screen and typing the new data. Commands are used for moving blocks and finding/replacing strings etc.

FILE MANAGEMENT
Files are organised into directories for ease of handling. File commands include Show File, Copy File, File Protection, Map Directory or Disc and many more.

ASSEMBLER
The assembler supports all TMS 9900 family microprocessors. Output is relocatable object code which may be linked with other modules to produce a complete program. Common, Program and Data segmentation is supported. This is used to separate ROM and RAM parts of the target program. A sorted symbol list may be produced. All error messages are in English text.

LINK EDITOR
When modules are assembled separately the Link Editor is used to produce a load module. External definitions and references are resolved. Component software packages and other pre-written modules may be connected to the user program when linking. A control file is used to specify the link parameters to save typing each time. Facilities supported by the link editor include overlay structures and task-procedure segmentation for re-entrant programming.

AMPL TARGET DEBUG UTILITY
The AMPL utility itself is provided as part of the AMPLUS software. This is described separately on the AMPL STATION page.

PROM PROGRAMMER
This utility controls the optional PROM programming hardware. Devices supported include all the 27XX and 25XX EPROMS, and all TI fusbile link PROMS. The data in memory may be manipulated before blowing. Commands available include re-ordering bits, masking bits and complementing data.

TEXT FORMATTER
The formatter is used for preparing documents. Commands in the source text are processed to produce a formatted output. Features include page heading, page numbering, left and right margin adjustment and line spacing control.

TX/TX5 CONVERSION
This utility manipulates files on the single sided single density diskettes used on FS990 systems. Files can be transferred to/from the TX5 format used by AMPLUS.

ORDERING INFORMATION:

TMAM 9001-01	Single user software development system, 220V/50Hz.
TMAM 9001-02	Single user software development system, 240V/50Hz.
***TMAM 4005-03**	AMPLUS software kit for FS990/4 systems.
TMAM 4014-21	AMPLUS software kit for TMAM 9001 systems.

Note: TMAM 9001 includes TMAM 4014-21.

*To be announced.

TMAM 9010

MULTI-USER HARD DISC AMPL SYSTEM

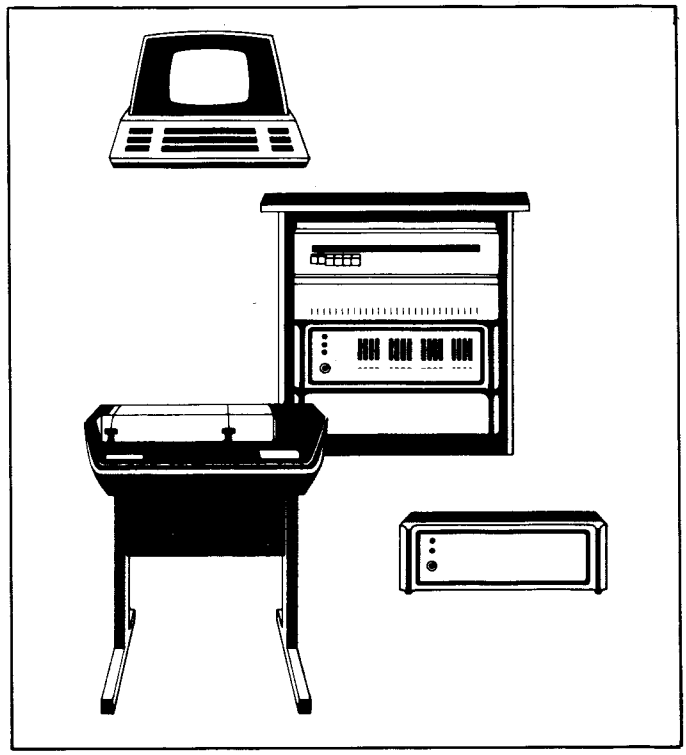
FEATURES: TMAM 9010 CONSISTS OF:

- **990/10 CPU with 256K bytes of error correcting memory.**
- **Dual DS10 disc drive providing 4.5M byte fixed and 4.5M byte removable mass storage.**
- **One 911 visual display terminal (VDT) and controller for a second.**
- **MULTI-AMPLUS software sysgened to customers requirements.**
- **Interface for AMPL station and printer.**

Optional add-ons:

- **TMAM 7001 printer, 150 characters per second.**
- **TMAM 600X AMPL station for emulation and trace.**
- **TMAM 6058 PROM programming kit.**
- **TMAM 7003 second 911 VDT.**

The use of hard disc storage increases both throughput and storage space. The fixed disc is used to hold system software. User development files are normally kept on the removable disc cartridges.



TMAM 9010 is a 1-2 user development system. The software is configured to support an AMPL station, printer, PROM programmer and 2 terminals. The computer and dual 4.5M byte disc drive are mounted in a 30 inch rack unit.

MULTI-AMPLUS SOFTWARE
The MULTI-AMPLUS software supplied with the TMAM 9010, 9020 and 9040 is based on the DX10 operating system and is an extension of the AMPLUS software provided with the TMAM 9001. The features of AMPLUS are provided plus the following:

MENU DRIVEN USER INTERFACE
The many commands available directly on MULTI-AMPLUS are presented in a tree-structured menu format. This makes finding the wanted command very fast. These are implemented using a 'system command interpreter' or 'SCI' language. Using SCI, commands may be modified, their names changed or new commands created.

MULTI TASKING
A user may set non-interactive programs, such as assembly or linking, running 'in the background'. Meanwhile, he may continue editing or target debugging, in 'foreground'. When the background program completes a message is sent to the terminal. Printing also takes place in parallel with all other activities.

FILE MANAGEMENT
Files are organised in a hierarchical directory structure. This makes it easy to keep track of files on the large hard discs. File and directory manipulation commands are available directly without first loading a file management utility.

ASSEMBLER
The assembler is an extention of that provided with AMPLUS. Additional features include conditional assembly and macros. This assembler implements planned instructions for future TI microprocessors.

TX/DX10 CONVERSION
When diskette drives are fitted to a TMAM 9010 TX format files may be manipulated and transferred. Files generated on a TMAM 9001 using AMPLUS may be used directly without conversion, with the appropriate floppy disc drive unit.

Also available is the full range of Component Software and high-level languages such as Microprocessor Pascal.

ORDERING INFORMATION:

TMAM 9010-01 1-2 user software development system, 220V/50Hz.
TMAM 9010-02 1-2 user software development system, 240V/50Hz.

TMAM 4001-10 AMPLDX, AMPL target debug utility for hard disc systems.
TMAM 4004-10 MULTI-AMPLUS software kit for TMAM 9010 and TMAM 9020.

Note: TMAM 9010 includes TMAM 4004 and TMAM 4004 includes TMAM 4001.

TMAM 9020

MULTI-USER HARD DISC AMPL SYSTEM

FEATURES; TMAM 9020 CONSISTS OF:

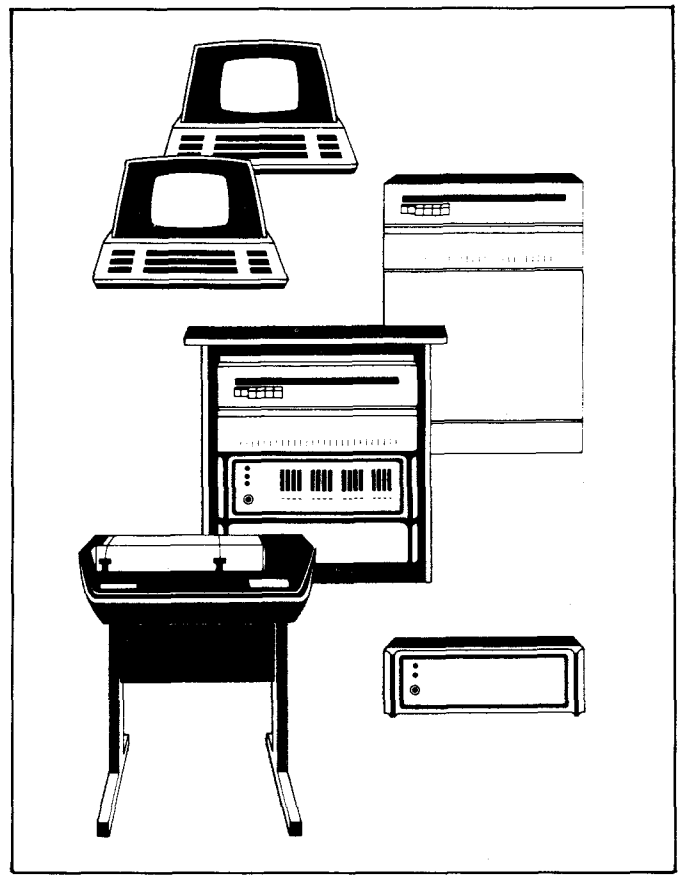
- **990/10 CPU with 256K bytes of error correcting memory.**
- **2 Dual DS10 disc drives providing a total of 9M byte fixed and 9M byte removable mass storage.**
- **Two 911 visual display terminals (VDT's).**
- **MULTI-AMPLUS software sysgened to customers requirements.**
- **Interface for up to 2 AMPL stations and printer.**

Optional add-ons:

- **TMAM 7001 printer, 150 characters per second; or**
- **TMAM 7002 printer, 600 lines per minute.**
- **TMAM 600X AMPL station for emulation and trace.**
- **TMAM 6058 PROM programming kit.**
- **TMAM 7004/5 additional 911 VDT's.**

The addition of a second DS10 disc drive, as compared to the TMAM 9010, produces a number of advantages. There is more storage space, backup of discs is easier and simultaneous access to more than one high-level language is possible.

The extra disc space allows the '9020 to support up to 4 users and two AMPL stations.



TMAM 9020 is a 2-4 user development system. The software is configured to support up to 2 AMPL stations, printer, PROM programmer and up to 4 terminals. The computer and one dual 4.5M byte disc drive are mounted in a 30 inch rack unit; the second dual disc drive is mounted on a pedestal

As with all hard disc systems, price includes site survey, installation and system generation to customers requirements.

MULTI-AMPLUS SOFTWARE

The MULTI-AMPLUS software supplied with the TMAM 9020 is fully described on the TMAM 9010 page. High-level language products, such as Microprocessor Pascal and Fortran are supplied on cartridge discs. As the 9020 has 2 such drives, more than one such package may be accessed at once by different users.

UPGRADE FROM TMAM 9010

A TMAM 9010 may be upgraded to a TMAM 9020 with the upgrade package including:

- Dual 4.5M byte secondary disc drive mounted on a pedestal.
- Additional 911 VDT.
- Reconfigured software for the expanded system.

ORDERING INFORMATION:

TMAM 9020-01	2-4 user software development system, 220V/50Hz.
TMAM 9020-02	2-4 user software development system, 240V/50Hz.
TMAM 9020-U10-01	Upgrade from TMAM 9010 to TMAM 9020, 220V/50Hz.
TMAM 9020-U10-02	Upgrade from TMAM 9010 to TMAM 9020, 240V/50Hz.
TMAM 4001-10	AMPLDX, AMPL target debug utility for hard disc systems.
TMAM 4004-10	MULTI-AMPLUS software kit for TMAM 9010 and TMAM 9020.

Note: TMAM 9020 includes TMAM 4004 and TMAM 4004 includes TMAM 4001.

TMAM 9040

MULTI-USER HARD DISC AMPL SYSTEM

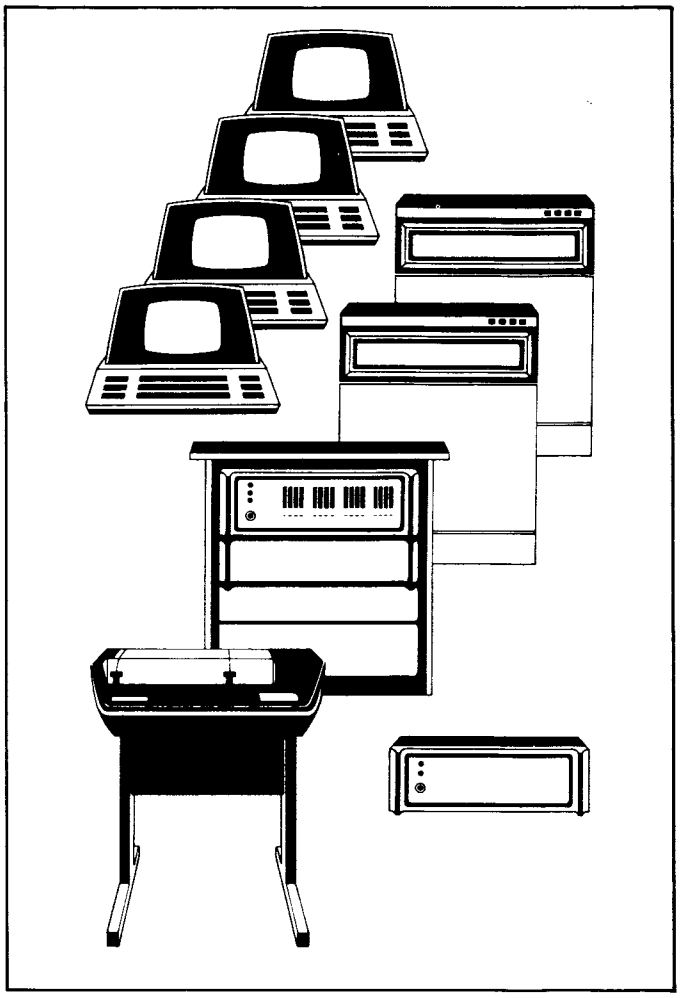
FEATURES; TMAM 9020 CONSISTS OF:

- **990/10 CPU with 320K bytes of error correcting memory.**
- **2 DS50 drives providing a total of 50M byte mass storage on removable cartridges.**
- **Four 911 visual display terminals (VDT's).**
- **MULTI-AMPLUS software sysgened to customers requirements.**
- **Interface for 4 AMPL stations and printer.**

Optional add-ons:

- **TMAM 7002 printer, 600 lines per minute; or**
- **TMAM 7001 printer, 150 characters per second.**
- **TMAM 600X AMPL station for emulation and trace.**
- **TMAM 6058 PROM programming kit.**
- **TMAM 7004/5 additional 911 VDT.**

The use of DS50 disc drives gives a five fold increase in storage space as compared to the TMAM 9020. In addition, the DS50 has a transfer rate about two and a half times that of a DS10. This serves to increase system throughput. The two identical drives provide a fast disc to disc backup method.



TMAM 9040 is a 4-8 user development system. The software is configured to support up to 4 AMPL stations, printer, PROM programmer and 8 terminals. The computer is mounted in a 30 inch rack unit. The two DS50 disc drives are mounted on pedestals.

As with all hard disc systems, price includes site survey, installation and system generation to customers requirements.

MULTI-AMPLUS SOFTWARE

The MULTI-AMPLUS software supplied with the TMAM 9040 is fully described on the TMAM 9010 page. High-level language products, such as Microprocessor Pascal and Fortran, can be supplied as add on packages with the system. Alternatively, they can be added later on separate DS50 packs. The increased storage space allows these packages to be held together on the system disc with the system software. The second 50M byte pack may be dedicated to user files.

UPGRADE FROM TMAM 9010 or TMAM 9020

A TMAM 9010 or TMAM 9020 may be upgraded to TMAM 9040 with the upgrade packages consisting of:

Two 50M byte DS50 disc drives mounted on pedestals.
Additional 911 VDT's and controllers (3 from 9010, 2 from 9020).
Reconfigured software for the expanded system.

It should be noted that the resulting system consists of TMAM 9040 plus DS10 disc drives (1 from a 9010, 2 from a 9020). These may be included in the new configuration for extra storage space.

ORDERING INFORMATION:

TMAM 9040-01	4-8 user software development system, 220V/50Hz.
TMAM 9040-02	4-8 user software development system, 240V/50Hz.
TMAM 9040-U10-01	Upgrade from TMAM 9010 to TMAM 9040, 220V/50Hz.
TMAM 9040-U10-02	Upgrade from TMAM 9010 to TMAM 9040, 240V/50Hz.
TMAM 9040-U20-01	Upgrade from TMAM 9020 to TMAM 9040, 220V/50Hz.
TMAM 9040-U20-02	Upgrade from TMAM 9020 to TMAM 9040, 240V/50Hz.
TMAM 4001-06	AMPLDX, AMPL target debug utility for hard disc systems.
TMAM 4004-06	MULTI-AMPLUS software kit for TMAM 9040.

Note: TMAM 9040 includes TMAM 4004 and TMAM 4004 includes TMAM 4001.

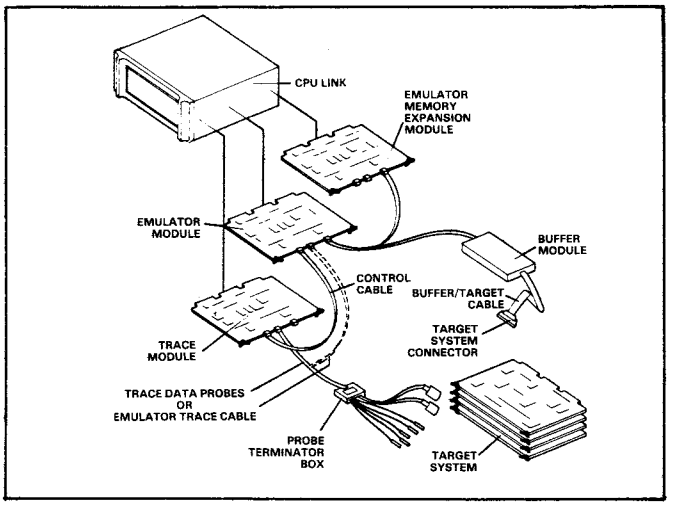
TMAM 6001, 2, 3, 4

TMS 9900 SERIES AMPL STATIONS

FEATURES; AN AMPL STATION CONSISTS OF:

- **Six slot chassis with CRU expansion board and cable to interface to the TMAM 9000 series development system.**
- **Emulator control board for the specified processors.**
- **Emulator expansion memory where appropriate:**
- **Buffer module and target connectors for the specified processors.**
- **Trace kit including trace module, probes and accessories.**

TYPES:	CPU'S SUPPORTED:
TMAM 6001	TMS 9900, TMS 9900-40
TMAM 6002	TMS 9980, TMS 9981
TMAM 6003	SBP 9900
TMAM 6004	TMS 9940



THAM 6000 series AMPL stations add target debugging facilities to a THAM 9000 series development system. The ports of an AMPL station are installed in a table top chassis. This may be up to 20 feet away from the host system.

EMULATOR

The emulator is implemented as a control board and buffer module. The TMS 9900-40, TMS 9980A/81 and SBP 9900A use the came controller and only the buffer module need be changed to switch processors.
The TMS 9940 requires a different controller and buffer module.

Facilities provided by the emulator include:

- **Full speed in circuit emulation.**
- **Address trace and breakpoint.**
- **Access to target memory and CRU.**

EMULATOR MEMORY

Target memory may be tapped into the emulator for simulation of ROM.
Where appropriate, an expansion memory module is included with the AMPL station. This gives the full memory map for the processor and allows software debug to take place with no target hardware.

Emulator memory is provided as follows:
(Bytes)

Processor	Controller board	Expansion board	Total map
TMS 9900/-40 5BR 9900	8K	56K	64K
TMS 9980A TMS 9981	8K	8K	16K
TMS 9940	2128 bytes	—	—

LOGIC STATE TRACE MODULE

The 10 MHz trace module may act with the various emulators to trace the data bus or in "stand-alone" mode as a logic state analyser. Using AMPL commands, display may be in binary, hex, octal, decimal, ASCII, instruction or 20 channel oscilloscope format.
4 of the trace lines are equipped with 10.5 glitch latches.

AMPL target delay utility and the AMPL language.

The AMPL software is supplied with all TMAM 9000 series development systems. It is used to control the emulator and trace modules.
Memory and data references may be symbolic. These symbols may be defined or displayed in any one of the AMPL formats: Binary, Octal, Hexadecimal, Decimal, ASCII or instruction. The last provides a line by line assembler and disassembler.
AMPL may be used in several ways to control the target debug:

(1) AMPL commands may be used directly. This provides a powerful method for accurate control of emulator and trace.
(2) These commands may be grouped into procedures. The addition of Pascal-type control constructs forms the powerful AMPL language. Complex test routines may be written in this way and stored on disc.
(3) Libraries of pre-written procedures are supplied with the software. These provide a user-friendly interface for those not familiar with AMPL language constructions. Each library included a HELP command. The procedures, written in standard AMPL language, may be cusomised to suit a particular application.

A fast, memory based, screen editor is available from within the utility. This is a subset of the AMPLUS editor. It is designed for easy production of AMPL procedures.

ORDERING INFORMATION:

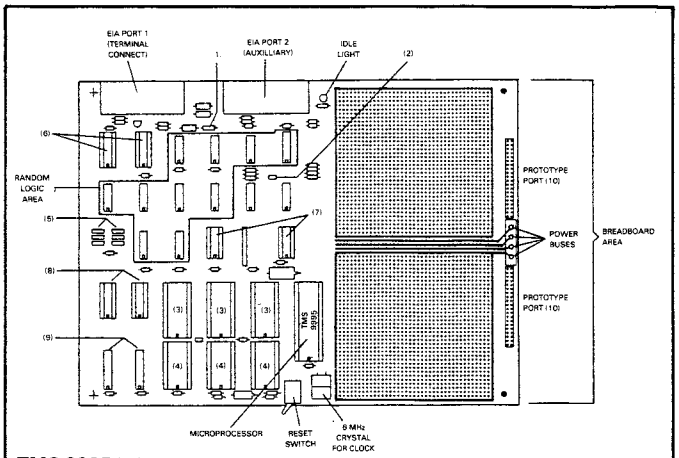
TMAM 6001-01	TMS 9900/-40 station, 220V/50Hz.
TMAM 6001-02	TMS 990/-40 station, 240V50Hz.
TMAM 6002-01	TMS 9980A/81 station, 220V/50Hz.
TMAM 6002-02	TMS 9980A/81 station, 240V/50Hz.
TMAM 6003-01	SBP 9900A station, 220V/50Hz.
TMAM 6003-02	SBP 9900A station, 240V/50Hz.
TMAM 6004-01	TMS 9940 station, 220V/50Hz.
TMAM 6004-02	TMS 9940 station, 240V/50Hz.
TMAM 6011-01	Station chassis, 220V/50Hz.
TMAM 6011-02	Station chassis, 240V/50Hz.
TMAM 6005	TMS 9940 emulator.
TMAM 6006	TMS 9940 buffer.
TMAM 6007	TMS 9900/80/81 SBP emulator.
TMAM 6008	SBP 9900 buffer.
TMAM 6009	TMS 9900/-40 buffer.
TMAM 6010	TMS 9980A/81 buffer.
TMAM 6012	Trace kit (includes *).
TMAM 6013*	Trace module.
TMAM 6014*	Trace probes.
TMAM 6015*	Trace accessories.
TMAM 6016	8K byte emulator memory expansion module.
TMAM 6017	56K byte emulator memory expansion module.

Development support for the TMS 9995 will become available in three phases:

1. TMS 9995 Evaluation Module (EVM)

FEATURES:

- **Single board microcomputer system with TMS 9995 processor.**
- **Low cost evaluation for TMS 9995 systems.**
- **6K software supplied include editor, assembler of debug monitor.**
- **2 RS232 ports for local terminal and cost link.**
- **3 user configurable 28 pin sockets for PROM, EPROM or RAM.**
- **Large prototyping area.**



TMS 9995 EVALUATION MODULE

1. Terminal selector
2. Wait state selector
3, 4, 5. Memory sockets/jumpers
6. UARTS for EIA ports
7. Memory decode PROMS
8, 9. 1K on board RAM
10. Prototype I/O ports

The TMS 9995 EVM may be used alone or, with an RS232 link, with a TMAM 9000 series development system. Either a telytype or RS232 terminal may be used to control the EVM. Target systems may be built up using the RAM/ROM sockets, prototyping area and prototype ports.

2. TMS 995 EVM Emulator

FEATURES:

- **In circuit emulator for TMS 9995 using EVM board as host.**
- **Stand alone or RS232 link to TMAM 9000 series system.**
- **Real time operation.**
- **No restrictions on target system.**
- **8K bytes of on board memory (capable to target requirement).**
- **Hardware breakpoint with complete qualification.**
- **Address and data trace.**

The combination of EVM and EVM emulator provides a complete in-circuit emulations facility for the TMS 9995. Code may be produced using the EVM or down loaded from a TMAM 9000 series system.

3. TMS 9995 AMPL STATION

FEATURES:

- **AMPL station chassis.**
- **Emulator control and buffer unit for full speed no wait state operation.**
- **Logic state trace module with probes.**
- **56K bytes emulator expansion memory giving full memory map without target present.**
- **Full control by AMPL utility.**
- **Internal memory cycle data trace.**

The TMS 9995 AMPL station is similar to the TMAM 6001 series stations for the other processors in the TMS 9900 range. It is connected to a TMAM 9000 series development system and controlled by the AMPL utility and the AMPL language.

ORDERING INFORMATION:

TMAM 6093 TMS 9995 EVM Emulator
TMAM 6095 TMS 9995 Evaluation module

TMAM 700X

DEVELOPMENT SYSTEM EXPANSION PARTS

Model 810 printer TMAM 7001 and 9
The model 810 is a 150 CPS dot matrix printer. It includes paper tray, full upper and lower case ASCII character set and vertical forms control. Printing may be at 10 or 16.5 CPI and 6 or 8 LPI. TMAM 7001 is just the printer and may be used to provide a printer for TMAM 9001. TMAM 7009 is required for a MULTI-AMPLUS system and consists of:

- Model 810 printer and paper tray.
- Printer stand.
- Controller board and cable.
- Installation and operation manual.

LP600 line printer kit TMAM 7002
The LP600 provides a 600 lines per minute line matrix printer for large development systems. The full upper lower case ASCII character set with descenders is supported. In addition, special characters may be printed by providing extra PROMS. The kit includes:

- LP600 line printer with stand and basket.
- Controller board and cable.
- Installation and operation manual.

Expansion 911 VDT's TMAM 7003 to 5
To add more users to a MULTI-AMPLUS system extra 911 VDT's are used. Each controller supports 2 VDT's, so the choice of an expansion unit depends on the availability of spare controller ports. The 911 has a 96 ASCII character set plus graphics characters. The separate keyboard unit has cursor control keys, numeric pad and 10 function keys.

Card reader Kit TMAM 7006
The model 804 card reader uses standard 80 column cards. It has a highly accurate fiber optic read station. The kit includes cable, controller and manual.

Magnetic tape drive kits TMAM 7007 and 8
The model 979A tape drive uses 1600 BPI phase encoded data. The TMAM 7007 is a master kit with all the parts needed to add a tape drive to a system. The 7008 is a secondary kit to add an extra drive.

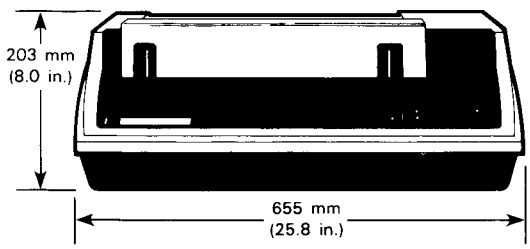
Note: The 979A drive must be rack mounted.

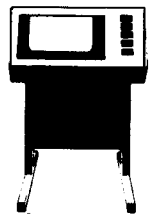
PROM programming kit TMAM 6058
This kit provides PROM and EPROM facilities for any TMAM 9000 series system. The PROM software is provided with all AMPLUS systems. The adaptors plug into the table top unit. The kit includes:

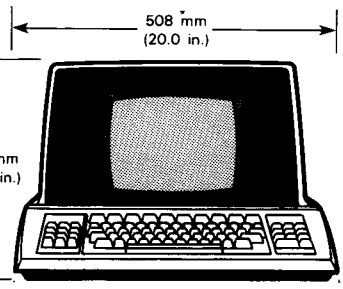
- Controller board and cable.
- Tabletop power supply unit.
- PROM 2 adaptor for DLM PROM's.
- EPROM 1 adaptor for 27XX EPROM's.
- EPROM 2 adaptor for 25XX EPROM's.

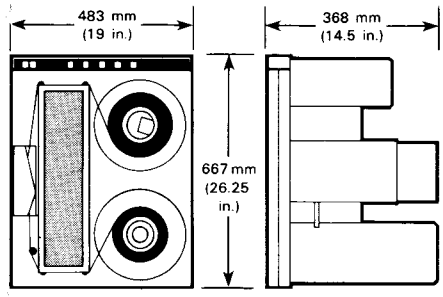
The components of this kit are also available separately, see ordering information.
Note: The PROM programming unit may only be fitted to a TMAM 9001 when it is equipped with an AMPL station chassis.

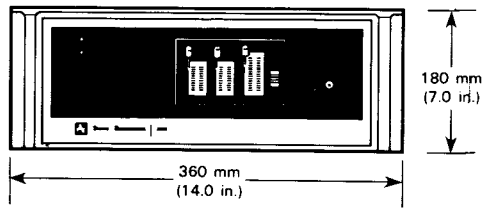
THE TMAM 9000 SERIES SYSTEMS MAY BE EXPANDED BY ADDING THE EXTRA PERIPHERALS ON THIS PAGE











ORDERING INFORMATION:

TMAM 7001	Model 810 printer.
TMAM 7002	LP600 line printer kit.
TMAM 7003	911 VDT expansion display and keyboard (requires controller port).
TMAM 7004	911 VDT expansion display, keyboard and dual controller.
TMAM 7005	2 911 VDT's, 2 keyboards and dual controller.
TMAM 7006	Model 804 card reader kit.
TMAM 7007	979A 1600 BPI Magnetic tape drive master kit.
TMAM 7008	979A 1600 BPI Magnetic tape drive secondary kit.
TMAM 7009	Model 810 printer, stand and controller.
TMAM 6022*	PROM programmer controller and table top unit.
TMAM 6023	PROM 1 adaptor panel (SLM PROM's).
TMAM 6024*	EPROM 1 adaptor panel (27XX EPROM's).
TMAM 6055*	PROM 2 adaptor panel (most DLM PROM's).
TMAM 6056*	EPROM 2 adaptor panel (25XX EPROM's).
TMAM 6057	TMS 9940E programming kit.
TMAM 6058	Full PROM kit, includes items marked*

MICROPROCESSOR PASCAL

Microprocessor Pascal allows systems using TMS 9900 series processors to be developed using a high-level language. Compared to assembly language programming code is easier to write, document, read and modify. It is therefore much less error prone. Direct CRU commands allow bit and byte manipulation. Concurrency extentions are suitable to real time multitasking programs.

Language is only part of a complete computer aided development tool. At least as important is the *support environment,* which gives a software engineer the tools and facilities he needs to take an application from design to implementation.

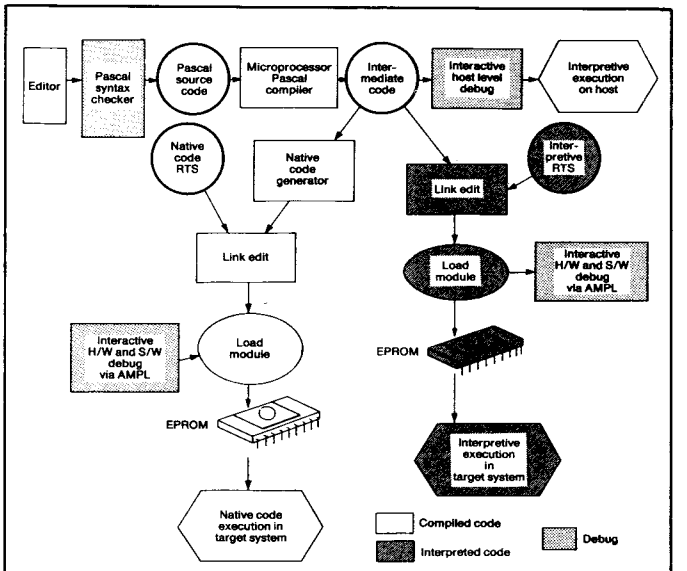
The software development tools forming the Microprocessor Pascal System link closely together to minimise development bottlenecks. The tools provided are:

- **Source Editor** — The MPP editor is screen based, and based on the standard AMPLUS editors. Additions include a syntax checker, avoiding the need for many compilations, and automatic indenting.
- **Compiler** — Compiles conventional Pascal programs as well as TI's Pascal concurrent extensions into interpretive code, which can then be executed directly or converted in 9900 native machine code.
- **Host Debugger** — More than 15 options for tracing variables and modifying data.
- **Configurator** — Enables the target system to retain only the parts of the run-time support necessary for program execution.
- **Native-Code Support** — Converts Pascal interpretive code into 9900 native machine code for direct execution.
- **Run-Time Support** — Both interpretive and native-code execution provide a speed/memory tradeoff.
- **Target Debugger** — A library of AMPL procedures provide a target look-alike to the host debugger. The high-level language structure may still be used even at the target stage. In addition all the standard AMPL commands are available.

Time critical routines may be written in assembly language and linked with the Microprocessor Pascal system regardless of whether the Pascal is executing interpretively or in native code.

Component software packages (detailed on subsequent pages) supplied by TI are generally written using Microprocessor Pascal and the source of these is supplied. Their use in a system together with the high-level language can drastically reduce development times.

Pascal also minimises the "life cycle" cost of product development. Independent studies have shown that initial development represents only 25-30 per cent of the total investment in a piece of software: the rest is spent on maintenance and upgrades for new products. It's in these areas of maintenance and upgradeability that Pascal really scores.



THE MICROPROCESSOR PASCAL SYSTEM

Design language	Specification	Design	Implementation	Integration	Documentation	Audit	Total	3-year follow-on	Life-cycle total
Assembly	10%	25%	10%	25%	20%	10%	100%	300%	400%
Basic	10%	13%	2%	13%	14%	9%	61%	120%	182%
Pascal	10%	8%	4%	5%	10%	5%	42%	42%	84%

1. The choice of language deeply affects software development and life-cycle costs. Compared with assembly, Pascal can save 79% over the full life of a program.

ORDERING INFORMATION:

TMS W753P-03 Microprocessor Pascal on Single Sided single density diskette (for FS990).
TMS W755P-21 Microprocessor Pascal on Double Sided double density diskette (for TMAM 9001).
TMS W754P-06 Microprocessor Pascal on DS50 cartridge (for TMAM 9040).
TMS W754P-10 Microprocessor Pascal on DS10 cartridge (for TMAM 9010 & 20).

COMPONENT SOFTWARE

EIA, HDLC, RX AND MATHS PACK

RX FEATURES:

- **Pre-emptive priority scheduling**
- **Interrupt processing and control**
- **Memory management**
- **Interprocess communication**
- **Realtime clock servicing**
- **Semaphore creation and management**
- **Dynamic process creation/reclamation**
- **Debug support**

RX

The Realtime Executive (RX) provides the framework within which software components operate.

RX is included in the Microprocessor Pascal Executive (MPX), and is therefore not required by the Pascal user. It is supplied as a separate component for use with assembly language programs.

RX provides:

- a standard framework for writing concurrent realtime applications
- minimum overhead (configurable 3K-6K bytes)
- use of all component software products (file manager, HDLC, maths pack, data types etc). Assembly Language Programmers may require Maths Pack or Data Pack in addition to RX, if they wish to use certain high-level components (e.g. HDLC). Check with your TI supplier.

Assembly language programs that are to use TI Component Software must conform to the RX standards. These are described in the Realtime Executive user's manual.

MATHS PACK

This product provides the assembly language RX user with a full range of arithmetic and trigonometric functions. The package supports:

- Full floating point operations
  - add
  - subtract
  - negate
  - multiply
  - divide
  - load
  - store
  - real/integer conversion
  - real/longint conversion
- Square root
- Sine
- Cosine
- Arctan
- Natural log
- Exponential
- Round real number
- Compare real number

Like all TI Component Software products, the Maths Pack is configurable for minimum size.

EIA COMMUNICATIONS PACKAGE

- Full and half-duplex operation
- Device independent interface
- Flexible line termination conditions
- Echo capability available for each port
- User defined error conditions
- Protocol independent messages possible
- Compatible with TM990/307 Communication Expander Module

The EIA Communications Package supports file level communication with another processor system, or an input or output device, through EIA communications links. The package supports multiple port configurations, and dynamic logical connection of one or more files to each port at run time. File transfers can be initiated and left to run concurrently with other activities in the system.

The EIA Communications package is supplied with source and object libraries, and full documentation. Like all TI Component Software products, it is configurable for minimum size.

HDLC COMMUNICATIONS PACKAGE

Features of the package include:

- Up to 32 stations in each local network
- Larger networks through the use of shared nodes
- Automatic counts of 'soft' and 'hard' errors
- Running average of data block sizes
- Compatible with TM990/308 Industrial Communication Module

The HDLC Communications Package will support communication with different processor systems (including mainframe computers and programmable controllers) via the HDLC protocol. It is fully compatible with TI's Device Independent File I/O strategy. Programs can interface with each HDLC port through dynamically connected, device independent files, or at a lower, device-dependent level. This package permits communication over long distances, and the construction of computer networks.

HDLC is an important element in distributed computer systems, whether on the factory floor or in the office. Often, a network of distributed microcomputers can serve an application need better and cheaper than a large central computer system. Distributed systems tend to be more flexible, and more responsive to users' requirements.

The standard HDLC protocol allows one computer to talk to another, whether a microcomputer, minicomputer, mainframe or even a programmable controller such as TI's PM550.

ORDERING INFORMATION

Maths Pack to be announced

TMSW 330R-03 Real time Executive on Single Sided single density

TMSW 330R-21 Real time Executive on Double Sided double density diskette.

TMSW 330R-06 Real time Executive on DS50 cartridge (for TMAM 9040).

TMSW 330R-10 Real time Executive on DS10 cartridge (for TMAM 9010 & 9020).

TO BE ANNOUNCED

ORDERING INFORMATION:

EIA communications to be announced.

TMSW 344H-03 HDLC on Single Sided single density diskette (for FS990).

TMSW 344H-21 HDLC on Double Sided double density diskette (for TMAM 9001).

TMSW 344H-06 HDLC on DS50 cartridge (for TMAM 9040).

TMSW 344H-10 HDLC on DS10 cartridge (for TMAM 9010 and 9020).

TO BE ANNOUNCED

COMPONENT SOFTWARE

FILE MANAGER, DEVICE INDEPENDENT I/O AND DATA PACK

LICENSING AND UPDATES

TI Component Software products are supplied under a one year renewable license. Texas Instruments will continue to develop and enhance TI Component Software products after release (providing additional features, optimising size and performance, and so on).

The license fee covers production of any number of derivative application programs during the period of the license. It also includes automatic update with all new releases during this period. Texas Instruments does not make a royalty charge for each product made or sold by a user of TI Component Software.

The first software components to be made available by TI perform such functions as file management and data communications. Later products will be provided in more specific application areas – process control, for example.

The framework of TI Component Software is available to software vendors for development and sale of their own component software products.

TI Component Software products will be supplied as libraries of modules on magnetic media. The package will include source code, object code and full documentation.

THE FILE MANAGER

Texas Instruments' File Manager allows a microprocessor application to store and manipulate data on a bulk storage medium, such as floppy disc.

The File Manager can be configured to provide several levels of capability:

- high-level device independent interface via application language verbs
- high-level device independent interface by procedure calls.
- logical interface to storage device with or without file structure.
- direct physical interface via device handlers

At each level, configuration will select features used by the application. Features supported by the file manager include:

- Volume initialization and installation
- Dynamic file creation and deletion
- Random and sequential access methods
- Fixed or dynamically extendable files
- Fixed and variable record formats
- File cataloguing by volume name (VOLNAME.FILENAME)
- Directory structure (VOL.DIR.FILE)
- File protection
- Controller self-test
- Copy, concatenate utilities
- Backup/compression utility
- Support of single and dual density formats

The File Manager currently supports file storage on diskette using the TM990/303 floppy disc controller. Future releases will support bubble memory and other media. (The initial license fee includes a 1-year renewable update service for all new releases).

The File Manager software component provides a flexible 'kit of parts' for configuring a custom file manager to suit any application. It supports Texas Instruments' Device Independent File I/O strategy, which is a feature of the RX environment.

NEW PRODUCTS:

DEVICE INDEPENDENT FILE I/O PACK

This product provides the assembly language RX user with:

- Device independent file level I/O
- Interprocess communication via files
- An example I/O subsystem for a simple keyboard
- Conversion of primitive data types to character strings

The file level I/O routines supply the device independent interface between the user application and various I/O subsystems (file manager, interprocess files, record oriented devices, etc) which may be in the system. Procedures for device independent connection, opening, reading, writing, closing etc are provided. This device independent interface can be used to connect to components such as TI's File Manager or HDLC or EIA Communications Packages, or to I/O subsystems defined by the user. Use of this package means that programs can be written independent of the device they will be interfacing with, file connections to different subsystems can be established dynamically at run time. (In TI's I/O strategy, programs can also interface directly with subsystems in a device-dependent way if required).

Two subsystems are supplied with the File I/O Pack itself. The Interprocess Communication subsystem permits concurrent processes to write to one another as if they were writing to files. The files are implemented as dynamic message areas in user RAM. The keyboard device subsystem can be used as supplied, or employed as a tempate for custom subsystem designs. The character string conversion routines permit easy interface when data is input from a keyboard or printed at an output device.

The File I/O Pack is supplied with source and object libraries, and full documentation. Like all TI Component Software products, it is configurable, so that only those functions used are included in an application.

DATA PACK

The Data Pack provides the assembly language RX user with a range of operations on simple and complex data types, of the kind normally associated with high-level languages. It features:

- Signed integer arithmetic
- Signed longinteger arithmetic
- Full range of set operations
- String compare
- Packed array manipulation

As other operations are defined, they will be included in future releases of Data Pack. (The original purchase price includes a one year update service). All operations are separately configurable.

PRODUCTS UNDER DEVELOPMENT

IEEE-488 Data Communications and Control
Industrial Control Package
Video Graphics Output Package

ORDERING INFORMATION:

TMSW 340F-03	File manager on Single Sided single density diskette (for FS990).
TMSW 340F-21	File manager on Double Sided double density diskette (for TMAM 9001).
TMSW 340F-06	File manager on DS50 cartridge (for TMAM 9040).
TMSW 340F-10	File manager on DS10 cartridge (for TMAM 9010 and TMAM 9020).

TO BE ANNOUNCED

MAINTAINANCE

TM990/AMPL REPAIR PROCEDURES – UK MAINLAND

TM990 Boards

All TM990 boards are covered by a special guarantee procedure. This is attached to the product and marked "UK guarantee". Within the envelope you will find a pre-addressed guarantee registration card which should be completed immediately upon receipt of the product and mailed to the address shown.

In the event of malfunction of any TM990 product the following procedure should be adopted:–

(A) If the product is within the 90 day warranty period "and" the warranty has been registered using the pre-addressed warranty card. . . "Then" . . . return the product pre-paid securicor "A" as follows. . .

(i) the authorised TI distributor from whom it was purchased.

OR

(ii) If purchased from TI direct. . .

RMR Dept.
Texas Instruments Ltd
Manton Lane
Bedford.

Turnround time is 48 hrs. after receipt of goods.

(B) If the product is within the 90 day warranty period "and" the warranty has not been pre-registered. . . "Then" . . . a copy of the suppliers dated invoice for the product concerned is required with the goods.

Turnround time is 48 hrs. after receipt of goods.

(C) If the Product is outside the warranty period or does not fulfil the above conditions then a signed pruchase order as below "must" be provided before any repair will be commenced.

Normal Service	£50 + components	Turnround = 5 w.d.
Expedited service	£75 + components	Turnround = 2 w.d.

w.d. = Working days.

NOTE:

1. **Warranty returns must be complete and with manual sets.**
2. **Under no circumstances can TI accept liability for custom software returned with the product. Any non-standard software/firmware will be automatically erased upon receipt.**
3. **Customising modifications will be removed and the product performance verified in an unmodified state. TI reserves the right to replace a faulty product and therefore cannot guarantee the return of a particular board.**

AMPL REPAIR

All development systems are covered automatically with a 90 day warranty from the date of purchase. Subsequently all development system customers are recommended to engage in a renewable service agreement for service of their development system. The cover provided by the warranty and by the renewable service agreement are identical, except that various levels of response time are available on call-out under the service agreement.

A request for service may be made by calling the local TI office and asking for. . .

"Digital Systems Division Field Service".

If your system is not under warranty and you do not have a service agreement with TI then field service is available as above however payment will be assessed on a job-by-job basis.

Service is normally on a board replacement level so as to minimise a customer's downtime.

Outside the UK: Contact your local TI office.

The Microprocessor Training Centre provides a series of modular courses for engineers, managers and technicians, which can be taken individually or combined together to give a flexible and yet comprehensive training in microprocessor technology.

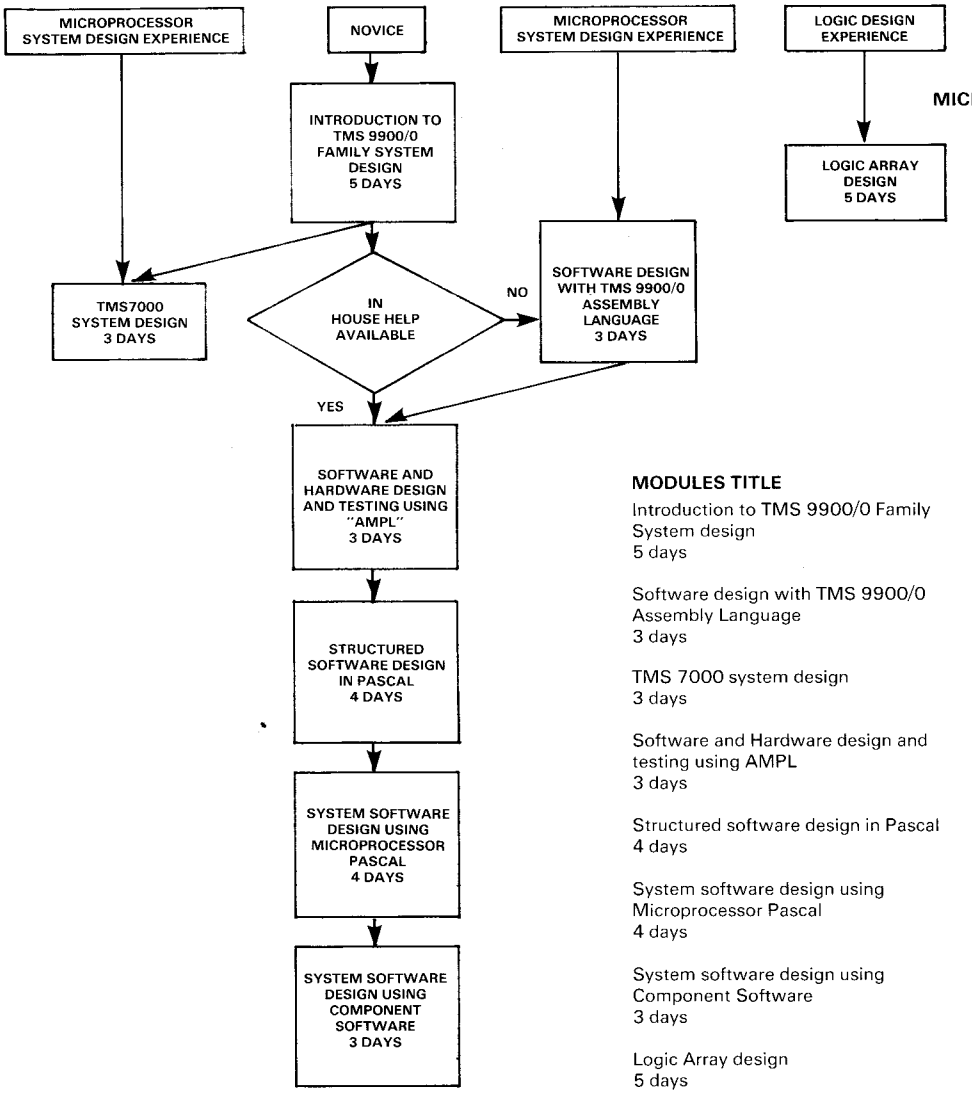
Each module of training is self-contained and specified in a manner which enables direct measurement of the results of training to be made. This modular structure provides precisely the training required by customers but at the same time ensures that existing modules can be easily adapted to technological changes and new modules created to satisfy newly identified needs.

Devolved Courses

The Microprocessor Training Centre will provide training on customers' premises. The customer would be responsible for refreshments and a suitably equipped classroom, while the centre provides hardware, software, instructor and training literature. The cost of one of these "devolved" courses would be eight times the course cost less 30%, which represents a substantial saving in training costs and accommodation expenses.

For more details on the courses offered at the Microprocessor Training Centre please contact the Customer Response Centre for a folder and booking form.

MICROPROCESSOR TRAINING CENTRE



MODULES TITLE

Introduction to TMS 9900/0 Family System design
5 days

Software design with TMS 9900/0 Assembly Language
3 days

TMS 7000 system design
3 days

Software and Hardware design and testing using AMPL
3 days

Structured software design in Pascal
4 days

System software design using Microprocessor Pascal
4 days

System software design using Component Software
3 days

Logic Array design
5 days

YOUR GUIDE TO TEXAS INSTRUMENTS MICRO-ELECTRONIC SYSTEMS DESIGN TRAINING FOR 1982

SUMMARY OF CONTENTS

"Hands-on" experience using the TM 990/189M microcomputer module to explore machine code, assembly language and high level language programs. With further work on interfacing, process control and the features of the TMS 9900/0 family.

An in depth study of TMS 9900/0 Assembly Language programming and software development.

Software development, interfacing and in-circuit emulation for the TMS 7000 range of 8-bit Microprocessors.

Use of software development utilities, in-circuit emulation and the logic state analyser with AMPL control language to de-bug application software and hardware.

Creation, debugging and execution of Pascal programs.

Implementing stand alone multiprogrammed systems using TI's Microprocessor Pascal system.

Configuring of the Real time Executive (Rx) and the accessing of I/O subsystems at the various levels of possible user interaction.

Introduction to circuit design using the range of Logic Arrays available from Texas Instruments. This includes in some detail the design methods and rules required when designing networks with Logic Arrays.

AMPL

AMPL 1000

The AMPL 1000 system provides development tools for the TMS 1000 series processors. For further information about the family itself, refer to the microcomputer section.

An AMPL 1000 development system consists of the following:

- TMAM 9000 series or FS990 development system.
- AMPL station chassis for use with TMAM 9000 series.
- Emulator control board.
- Buffer module.
- AMPL 1000 software.

Any of the TMAM 9000 series add-on peripherals, including PROM programming, may be used with this system. The AMPL 1000 software runs as an add-on to AMPLUS or MULTI-AMPLUS.

AMPL 1000 SOFTWARE

The emulator and buffer modules for the TMS 1000 series of mask programmable 4 bit processors are controlled by this software. Code is typed into a screen based, syntax checking, editor. This is a derivative of the standard AMPLUS screen editor.

The first pass of assembly is carried out as the code is entered. Assembly is completed quickly to enter emulation mode. In this mode, the complete machine state is displayed on the screen, as shown. The exact display will depend on which of the series of processors is in use.

The code may be executed at slow speed, when the source executing is displayed and the machine state updated. Breakpoints are set by moving the cursor to the source statement and pressing a key. When halted, the machine state is altered by the cursor around the display and entering new values.

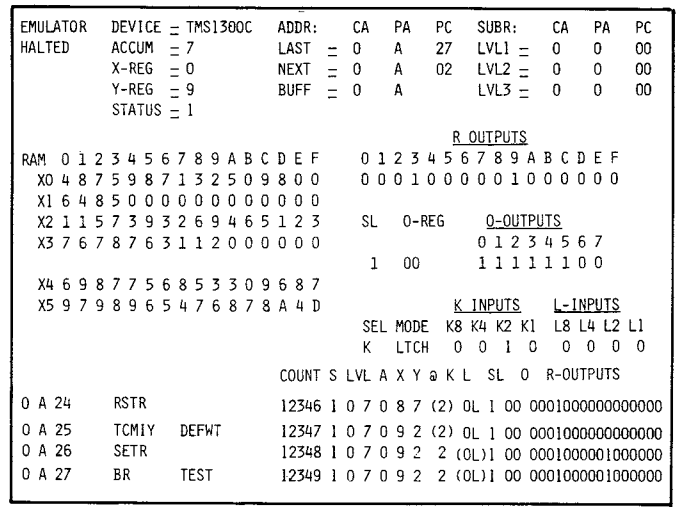
When initial debugging is complete, the program may be executed at full speed, Using AMPLUS software, the logic state analyser can be used for hardware debugging.

Other facilities offered by AMPL 1000 include:

- Debugging uses source code throughout, including patches.
- Software definition of output programmable logic array for debugging.
- Passing breakpoints without halting causes a pulse on a buffer module output for timing reference.
- Emulator board contains PROM (for OPLA) and EPROM programming facilities.

All AMPL 1000 kits contain:

- Emulator control board.
- Buffer module.
- Emulator chips for all processors supported by the kit.
- AMPL 1000 software.
- Manuals.



ORDERING INFORMATION:

TMAM 6075-03 AMPL 1000 kit for FS990 supporting 1K and 2K ROM PMOS processors: TMS 1000/1100/1200/1300/1070/1170/1270/1370.

TMAM 6073-03 AMPL 1000 kit for FS990 supporting 4K ROM PMOS processors: TMS 1400/1600/1470/1670.

TMAM 6071-03 AMPL 1000 kit for FS990 supporting CMOS processors:TMS 1000C/1100C/1200C.

To be announced: AMPL 1000 for TMAM 9000 series systems.
Kits for TMS 2100 series.

Development support for the TMS 7000 will become available in 3 phases:

1. Evaluation module.
2. AMPL 7000 with TMS 7000 'front panel' software.
3. Full AMPL 7000 system with hardware and software.

The AMPL 7000 hardware consists of the following parts:

- Emulator control board.
- TMS 7000 buffer module.
- Logic state analyser module.

The trace module is the same as that used for the TMS 9900 family development systems. For use with TMAM 9000 series systems, the boards are housed in a 6 slot chassis to make a complete AMPL station.

The front panel software provides standard debug facilities including memory display/modify, execution of target program and breakpoints.

AMPL 7000 software provides all the target debug power associated with AMPL systems.

EVALUATION MODULE MODULE FEATURES:

- Single-chip TMS 7020 and TMS 7040 emulation.
- Monitor.
- Line-by-line assembler.
- RS232 communication through EIA port
- Program development and debugging capability.
- Execute program from RAM or EPROM.

MONITOR FEATURES:

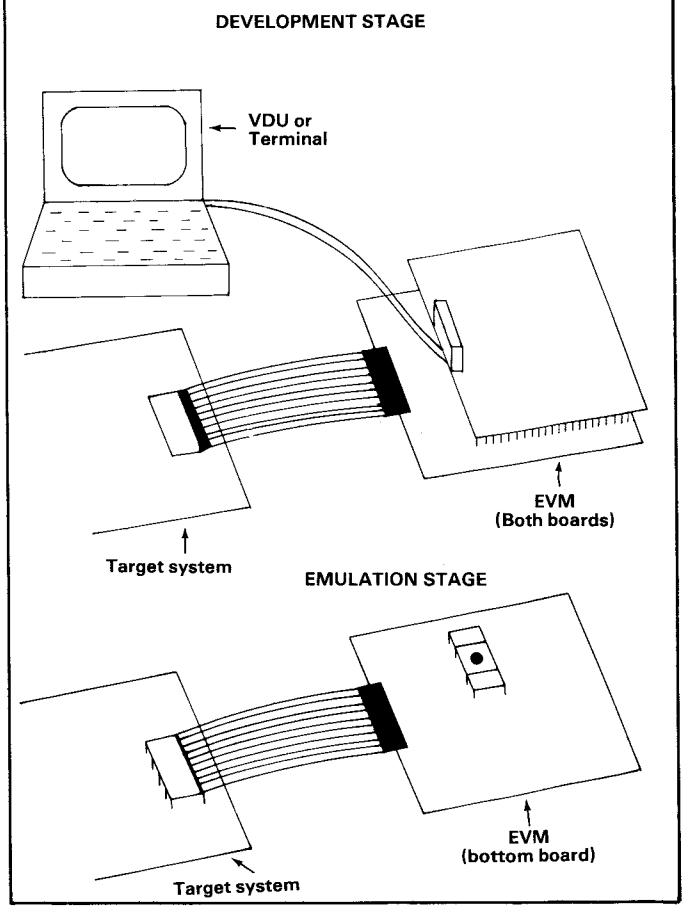
- Load memory from EIA port in MLP object, 9900 object or Tektronix object format.
- Dump memory to EIA port in MLP object or Tektronix object format.
- Initialise user program limit.
- Move memory.
- List memory.
- Display/modify A and B registers.
- Display/modify memory, register file, peripheral file, PC, ST or SP.
- Single step through program.
- Execute at full speed.
- Breakpoint at address.

DESCRIPTION:

The evaluation module (EVM) is a two board system that allows emulation of the TMS 7020 and TMS 7040 in single chip modes. The boards plug together in a piggy-back fashion with the bottom board providing the emulation and the top board providing 4K of user RAM for program development and RS232 communication through an EIA port.

A line-by-line assembler is provided that allows small program development and program modification. Object can be loaded or dumped for ease of larger program development.

SYSTEM DIAGRAMS:



ORDERING INFORMATION:

	TMS 7000 evaluation module.
TMAM 4013-03	'Front panel' software for AMPL 7000 on FS990.
To be announced:	AMPL 7000 software.
TMAM 6012	Logic state trace kit, contains*
TMAM 6013*	Trace module.
TMAM 6014*	Trace probes.
TMAM 6015*	Trace accessory kit.
TMAM 6099	TMS 7000 emulator and buffer module.
To be announced:	TMS 7000 AMPL station.