RA 3790 Series

HF Receivers

Maintenance Manual

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RACAL

The Electronics Group

Ref. A5258

Printed in England

Issue 1
Mar 94 - 100

WARNINGS

ANY SPECIAL SAFETY WARNINGS OR INSTRUCTIONS WHICH APPEAR IN THIS MANUAL MUST BE STRICTLY OBSERVED.

HIGH VOLTAGE

LETHAL VOLTAGES EXIST IN THE EQUIPMENT. GREAT CARE MUST BE TAKEN WHEN CARRYING OUT ADJUSTMENTS OR WHEN FAULT FINDING.

ENSURE THAT A RELIABLE SAFETY EARTH IS CONNECTED TO THE EQUIPMENT BEFORE POWER IS APPLIED.

ALL POWER SOURCES MUST BE ISOLATED AND ALL HIGH VOLTAGE POINTS DISCHARGED TO EARTH BEFORE ANY FAULT RECTIFICATION WORK IS UNDERTAKEN.

HIGH CURRENT

HIGH CURRENTS EXIST IN THE EQUIPMENT. CARE MUST BE TAKEN WHEN CARRYING OUT ADJUSTMENTS OR WHEN FAULT FINDING.

STATIC SENSITIVE DEVICES

THE EQUIPMENT CONTAINS COMPONENTS WHICH ARE SUSCEPTIBLE TO DAMAGE BY STATIC ELECTRICAL CHARGES. APPROPRIATE PRECAUTIONS SHOULD BE OBSERVED WHEN HANDLING SUCH COMPONENTS OR SUB-ASSEMBLIES CONTAINING THEM, OR WHEN MAKING DIAGNOSTIC TESTS.

CAUTION

'POZIDRIV' SCREWDRIVERS

METRIC THREAD CROSS-HEAD SCREWS FITTED TO RACAL EQUIPMENT ARE OF THE 'POZIDRIV' TYPE. PHILLIPS TYPE AND 'POZIDRIV' TYPE SCREWDRIVERS ARE NOT INTERCHANGEABLE, AND THE USE OF THE WRONG SCREWDRIVER WILL CAUSE DAMAGE. POZIDRIV IS A REGISTERED TRADE MARK OF G. K.N. SCREWS AND FASTENERS LIMITED. THE 'POZIDRIV' SCREWDRIVERS ARE MANUFACTURED BY STANLEY TOOLS LIMITED.

LETHAL VOLTAGE WARNING

VOLTAGES WITHIN THIS EQUIPMENT ARE SUFFICIENTLY HIGH TO ENDANGER LIFE.

COVERS MUST NOT BE REMOVED EXCEPT BY PERSONS QUALIFIED AND AUTHORISED TO DO SO AND THESE PERSONS SHOULD ALWAYS TAKE EXTREME CARE ONCE THE COVERS HAVE BEEN REMOVED.

RESUSCITATION

TREATMENT OF THE NON-BREATHING CASUALTY

1 SHOUT FOR HELP. TURN OFF WATER, GAS OR SWITCH OFF ELECTRICITY IF POSSIBLE

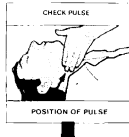
Do this immediately. If not possible don't waste time searching for a tap or switch.

2 REMOVE FROM DANGER: WATER, GAS, ELECTRICITY, FUMES, ETC.

Safeguard yourself when removing casualty from hazard. If casualty still in contact with electricity, and the supply cannot be isolated, stand on dry non-conducting material (rubber mat, wood, linoleum).
Use rubber gloves, dry clothing, length of dry rope or wood to pull or push casualty away from the hazard.

3 REMOVE OBVIOUS OBSTRUCTION TO BREATHING

If casualty is not breathing start ventilation at once



PULSE PRESENT

PULSE ABSENT

CONTINUE INFLATIONS UNTIL RECOVERY OF NORMAL BREATHING

ONE FIRST AIDER
15 Compressions at 80 per minute followed by 2 inflations

TWO FIRST AIDERS
One conducts chest compressions without pause at 80 per minute. The other administers mouth to mouth ventilation after each 5th compression.

Check heart beat after first minute and then after every three minutes. Continue external chest compression and mouth-to-mouth ventilation until a normal pulse is felt and colour improves.

CONTINUE INFLATIONS UNTIL RECOVERY OF NORMAL BREATHING

Keep casualty at rest. Remove on a stretcher. Watch closely, particularly for difficulty in breathing. Lightly cover with blankets or other materials.

SEND FOR DOCTOR AND AMBULANCE

DOCTOR	AMBULANCE	HOSPITAL	Nearest First Aid Post
TELEPHONE	TELEPHONE	TELEPHONE	

RA3790 SERIES HF RECEIVER

MAINTENANCE MANUAL

CONTENTS

PREFACE

SCOPE OF MANUAL

This manual is for use with all receivers in the RA3790 Series. The manual contains receiver maintenance information and is separated into chapters as follows:

1. Chapters 1 to 5 contain general descriptive and maintenance information.

2. Chapters 6 to 10 are self-contained board chapters for the boards provided with a basic receiver, and include functional descriptions, block and circuit diagrams, layout illustrations, components lists, fault location and alignment information as appropriate to each board.

3. Chapters 11 covers the chassis assembly and includes the receiver interconnection diagram.

4. Chapter 12 gives assembly parts list information for the overall receiver. Detailed components list information is included in each board chapter.

5. Appendices will be added, as necessary, to cover additional special-purpose boards and variants of the basic receiver family.

ASSOCIATED DOCUMENTS

RA3790 Series HF Receiver Operators Manual (Ref. A5256)

RA3790 Series HF Receiver Interface Manual (Ref. A5257)

CHAPTER 1

GENERAL DESCRIPTION

CONTENTS

Illustrations

Fig.

CHAPTER 1

GENERAL DESCRIPTION

INTRODUCTION

1. The RA3790 series of communications receivers is a family of fully synthesised programmable receivers covering the frequency range 10 kHz to 30 MHz in 1 Hz steps. Reception facilities for CW, MCW, AM, USB/LSB, FM and FSK signals are provided as standard with ISB available as an option.

2. A conventional tuning knob with selectable tuning rates enables continuous tuning over the frequency range without any need for band changing. Alternatively, instant frequency selection is available using numeric push-buttons. A 100-channel, non-volatile memory is provided for storing 100 frequencies and their associated operating settings for instant recall. Facilities for automatic scanning of these preset channels and sweeping of a pre-defined frequency range are also provided.

3. All receivers can be controlled remotely and contain comprehensive built-in test equipment (BITE) facilities, which may be accessed either locally or remotely to enable fault location and subsequent repair to be carried out rapidly.

4. The RA3790 Series is modular in design and numerous different configurations are available, as follows:

   (1) RA3791 HF receiver with front panel controls plus local and remote control facilities.

   (2) RA3792 dual HF receiver which is effectively two RA3791 receivers in one chassis sharing a common front panel, which may be switched to control one receiver at a time, or both receivers in diversity operation.

   (3) RA3793 HF receiver which is a remote control version of the RA3791 and intended for operation as a slave receiver.

   (4) RA3794 dual HF receiver which is a remote control version of the RA3792 and intended for operation as two independent slave receivers.

   (5) MA3790 receiver control unit with a receiver front panel for use as a controller for receivers in the RA3790 Series.

5. The receiver consists of the following assemblies:

   (1) Analogue Board: This contains all RF signal path and local oscillator circuits.

   (2) Digital Board: This contains the analogue-to-digital converter (ADC), the digital signal processor (DSP), the receiver processor and the audio circuitry.

   (3) Front Panel: This contains the receiver controls and displays.

   (4) Power Supply: A universal input switched-mode power supply unit.

6. Details of the above assemblies are contained in the appropriate handbook chapter. All external connections except headphones are made at the rear panel, while the front panel provides all the local controls. Front and rear panel views for the various versions are shown in Figs. 1.1 to 1.4.

RA3791 BLOCK DIAGRAM DESCRIPTION

7. The following brief technical description of the basic RA3791 receiver should be read in conjunction with the block diagram given in Fig. 1.5. A more detailed description of each board is given in the appropriate board chapter.

RF Input

8. The incoming RF signal is routed via a protection and muting circuit through a 30 MHz low pass filter (LPF) either side of a selectable wideband RF AMP, 10 dB attenuator or bypass route via relays controlled from the processor section of the digital board.

9. The protection circuit contains a relay which automatically open-circuits the RF path for signals at the antenna greater than approximately +18 dBm, or when a mute signal is applied to the receiver via a rear panel connection or via the remote control interface.

10. The low pass filters protect the receiver from image frequency signals and also attenuate first local oscillator re-radiation from the antenna connection.

First Mixer and IF Amplifier

11. After amplification in the drive amp, the 40.032 MHz to 70.032 MHz output of the first LO synthesiser is mixed with the received signal in the first mixer stage. The resulting difference frequency of 40.032 MHz is fed as the first IF to the gain-controlled first IF amplifier, via a crystal filter centred on 40.032 MHz. This acts as a 'roofing' filter to establish the maximum bandwidth of 12 kHz for the receiver.

First Local Oscillator

12. The first local oscillator signal is produced by a single-loop synthesiser and is phase locked to a 10 MHz reference signal derived from the Reference Module. In the synthesiser a voltage controlled oscillator (VCO) generates the basic first LO frequency of between 40.032 MHz to 70.032 MHz. The frequency is controlled by a phase locked loop in which the VCO frequency is divided by the programmable divider and compared with a 1 MHz reference frequency in the phase comparator. The output of the phase comparator is filtered by the loop filter and fed back to the VCO to lock the loop.

13. The division ratio of the signal fed back to the phase comparator is determined by the programmable divider. This is controlled by a synthesiser control (LSI) device which is loaded with frequency setting data from the receiver processor on the digital board, and processes this information in such a way as to obtain a frequency resolution down to 1 Hz.

Second Mixer and IF Amplifier

14. The second mixer mixes the first IF of 40.032 MHz with a 40 MHz local oscillator signal. The resulting second IF output of 32 kHz is amplified in a fixed gain 32 kHz second IF amplifier prior to being routed to the digital board.

Second Local Oscillator

15. The second LO output is produced in the reference module by a 40 MHz voltage controlled crystal oscillator (VCXO), phase locked to a 1 MHz reference signal which may be derived from either an internal or external frequency standard.

16. The user may select the frequency standard source by means of a switch on the rear panel, setting it to either INT or EXT. With INT selected and an internal 10 MHz Frequency Standard Module fitted, the frequency standard output is divided to produce a 1 MHz reference to lock the synthesiser. In this mode a reference output is made available at the rear panel for connection to external equipment. By setting additional switches No. 2 and No. 3 (switch No. 4 not used), an external reference output frequency of either 1 MHz, 5 MHz or 10 MHz is derived from a frequency divider.

17. With EXT selected, an external frequency standard of either 1 MHz, 5 MHz or 10 MHz may be used by setting the switches accordingly.

Clock Frequency Generation

18. A 5 MHz reference signal generated on the analogue board is used to phase lock the 11.2 MHz and 12.288 MHz clock signals used by the ADC stage, the Coder/Decoder (CODEC) stages and the IF output ASIC (Application Specific Integrated Circuit).

Analogue to Digital Converter

19. The balanced 32 kHz second IF signal, from the analogue board, is amplified before being fed into the ADC. This Sigma Delta ADC device, which provides third order noise shaping, has a 100 dB dynamic range. It combines the analogue signal to produce a serial data output at a rate of 16 bits at 96 Ksamples per second. This data is fed to the Digital Signal Processors (DSPs) for further signal processing.

20. The second IF signal is also presented to a second ADC; this converter has the nominal signal level some 18 dB below its maximum level and is used, with a programmed logic array (PAL), to detect the peak of the signal for analogue board AGC processing.

Digital Signal Processors

21. The digital signal processors perform filtering, AGC, demodulation, metering, BITE and special functions.

Audio Interface

22. The DSP audio output is sent to the CODECs which provide digital to analogue conversion (DAC) and image filtering. The analogue output is then fed to the front panel loudspeaker, external loudspeaker, tri-state audio bus or a 600 ohm balanced line output. The line level is adjusted via multiplying DACs using the menu system.

23. A digital audio interface is also available.

IF Interface

24. The analogue IF output can be set to 1.4 MHz or to a frequency in the range 10 kHz to 455 kHz, in 5 kHz steps, to suit user requirements.

25. The baseband digital IF is first passed to an ASIC which provides mix and interpolation filtering before digital to analogue conversion. A digital IF interface is also available.

Receiver Processor

26. The receiver processor uses a 68000 microprocessor to control all the receiver local control functions, as well as the receiver remote control functions.

27. Remote control is provided either via the Master/Auxiliary port or Tributary port. The two ports are controlled via a single Dual Asynchronous Receiver/ Transmitter (DUART). Each port is RS423 compatible. The receiver may be used as a controller with a built-in, multi-addressing capability of up to 99 receiver channels or as a slave.

28. Control of the receiver boards and external interface are via two Programmable Interface Timer (P/IT) devices.

29. A DAC and comparator is used to provide BITE measurements.

30. An IEEE-488 remote control interface option is also available.

Front Panel Circuits

31. The Front Panel Assembly provides the controls and displays necessary to operate the receiver. These are interfaced with the digital board which processes front panel commands as well as those received via the remote control ports.

32. Single function pushbuttons control the most commonly used operations and four soft keys control the receiver's many special facilities by means of a menu system.

33. Three liquid crystal displays (LCDs) indicate the current selections and operating settings of the receiver. Backlighting is provided, the intensity being controlled by the digital board.

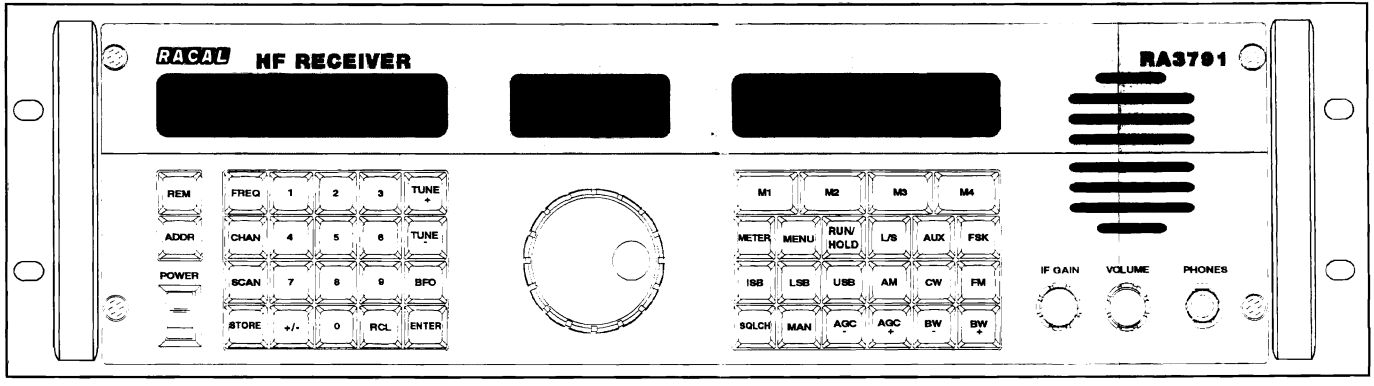
34. Frequency setting information from the shaft encoder is sampled by the digital board, which also decodes any pushbutton selections made at the keyboard.

Power Supplies

35. A switch mode power supply module provides +5 V, +15 V and -15 V outputs which are distributed throughout the equipment.

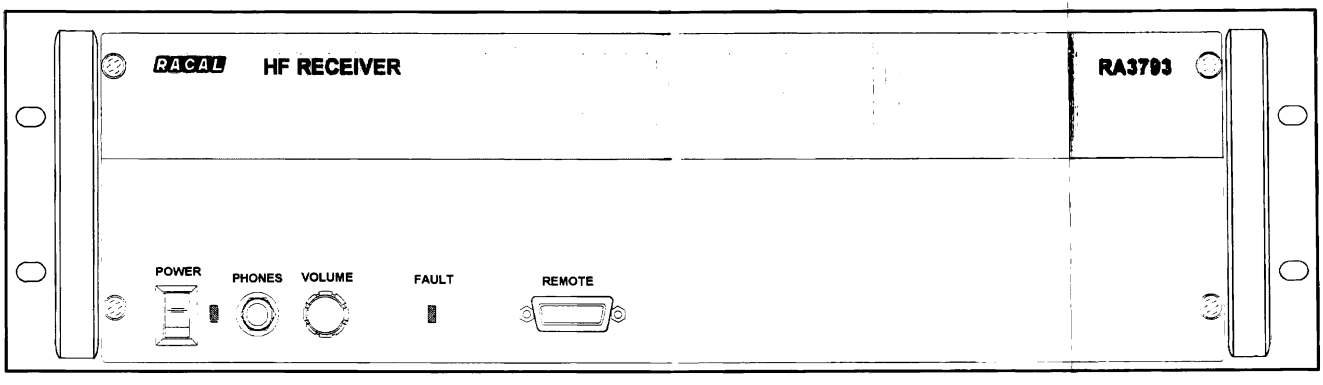
BITE

36. A comprehensive BITE facility monitors automatically receiver operation to identify faults to module level. These BITE facilities may be controlled locally through a menu system or remotely via the remote interface. Details of all these facilities are contained in Chapter 3.



RA3791/RA3792: Front Panel View

Fig. 1.1



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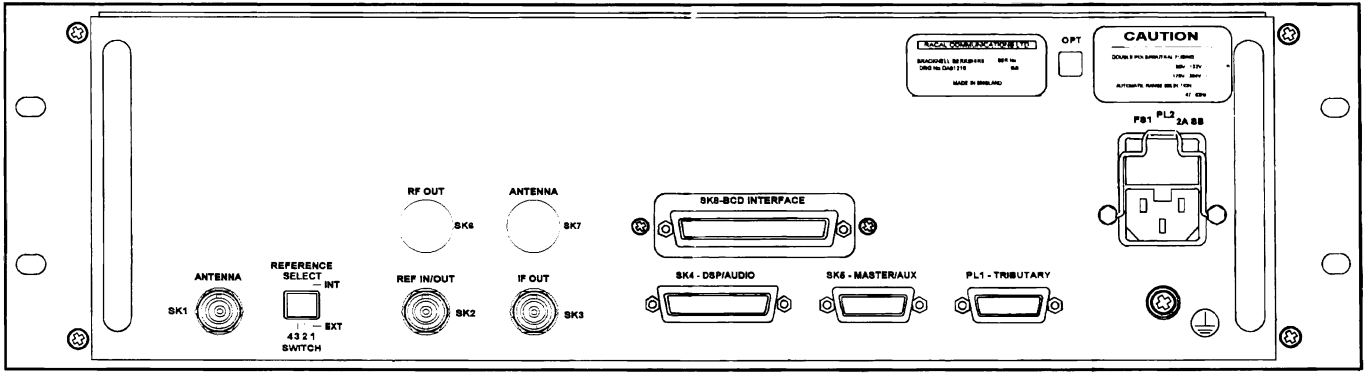
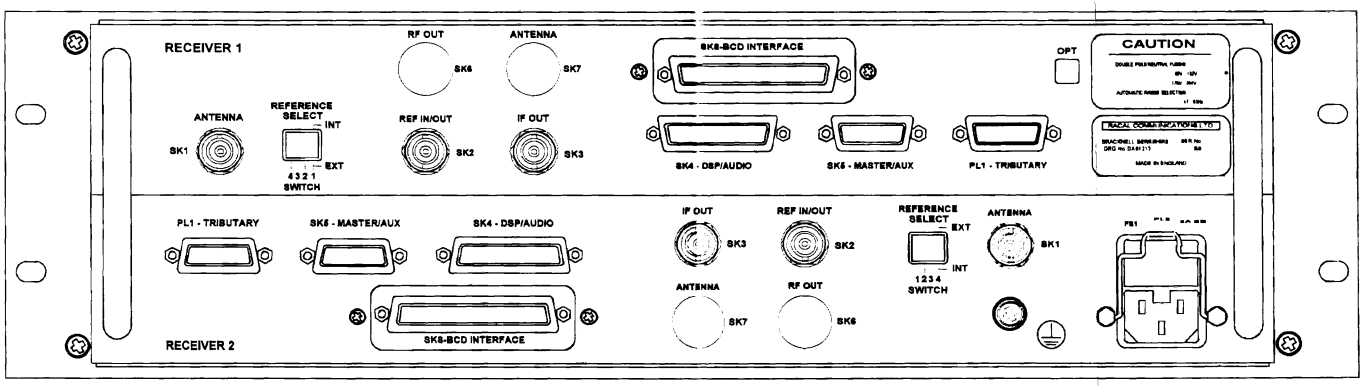
RA3793/RA3794: Front Panel View Fig. 1.2

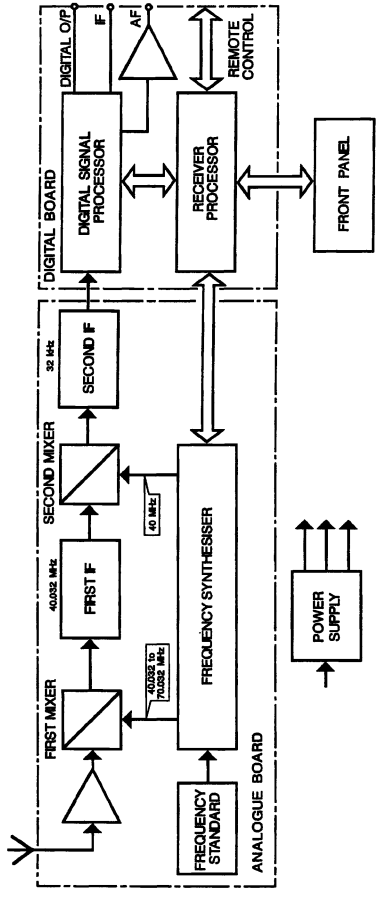


RA3791/RA3793: Rear Panel Layout View

Fig. 1.3



RA3792/RA3794: Rear Panel View Fig. 1.4



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RA3791: Simplified Block Diagram

Fig 1.5

CHAPTER 2

RECEIVER SERVICING

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CHAPTER 2

RECEIVER SERVICING

INTRODUCTION

1. This chapter introduces fault diagnosis techniques and provides information to assist in the subsequent repair of the equipment.

FAULT LOCATION TECHNIQUES

2. The presence of a fault condition may be indicated by the illumination of the FAULT indicator or by a failure occurring when the unit confidence test is run. A fault condition may also be detected during normal equipment operation.

3. The user may wish to identify and replace a faulty board in order to return the equipment to service as quickly as possible. Alternatively, the user may wish to identify and replace the faulty component. This manual contains information to assist with fault diagnosis to both board and component level.

4. The built-in test equipment (BITE) identifies many faults to board level using the continuous monitoring or unit confidence test facilities. Instructions on the use of these BITE facilities are given in Chapter 3. The preliminary functional checks and overall receiver performance tests detailed in Chapter 4 of this manual can also be used to indicate the presence of a fault condition and to assist in fault diagnosis. The faulty board can easily be replaced with no re-alignment being necessary.

5. In addition to identifying a faulty board, the BITE routines also provide more information to assist in isolating the fault to an area within the suspect board. A fault finding BITE facility (select test) is provided to allow individual BITE tests to be selected manually and run repeatedly as an aid to fault finding to component level.

6. Signature analysis facilities are also included as a means of locating faulty components in the digital circuitry throughout the receiver.

7. Full details explaining the use of the fault finding BITE facility, including signature analysis, are also provided in Chapter 3. The actual BITE tests are detailed in the appropriate board chapter, which also includes a fault directory listing faults against possible causes with suggested actions; in some cases these refer to a separate check procedure. The fault directory may be used when a fault is detected by the BITE or by other means. Where applicable, signature analysis tables are included at the end of the board chapter.

8. Refer to the appropriate board chapter for a functional description of the board under test. A circuit diagram is supplied with each board chapter.

9. To assist with fault location in the signal path through the Analogue Board, a signal level diagram is provided. This may be used to determine the correct signal level at each stage for any input level. It also indicates the correct nominal gain of each stage.

10. Fault location to component level can be carried out with the boards plugged in using the receiver as a test bed. Internal access to the suspect board is gained using an extender cable provided with the BITE Kit (Table 2.1). Only standard proprietary workshop test equipment is required. A list of recommended test equipment and tools required for servicing is given later in this chapter.

11. The receiver employs components which are surface mounted to the printed circuit board (PCB). The recommended methods of replacement for these surface mounted devices (SMDs) are detailed in the board repair instructions given later in this chapter.

SAFETY PRECAUTIONS

12. Observe all safety regulations. Do not remove or replace boards or make repairs with power applied to the receiver.

WARNING:

Voltages within this equipment are sufficiently high to endanger life. Use caution when servicing power supplies or their load components.

TEST EQUIPMENT AND TOOLS

13. Table 2.1 lists the test equipment recommended for conducting performance checks, fault location and maintenance procedures. Alternative items of test equipment of similar specification may be used. No special tools other than normal hand tools are required for the replacement of any board in the RA3790 series receivers. However, the replacement of surface mount components is simplified by the use of more specialised supplementary tools, as listed in Table 2.1.

Table 2.1 Test Equipment and Tools

Item	Description	Example
1	Signal Generator (Quantity 2) Frequency range to suit Receiver Modulation: CW, AM, FM Output Impedance: 50 Ohms	Racal-Dana Instruments 9087
2	RF Millivoltmeter Input Impedance: 1 Megohm with 50 Ohm Adaptor	Racal-Dana Instruments 9302 or 9303
3	Digital Frequency Meter Frequency Range:	Racal-Dana Instruments
4	Oscilloscope, Dual Trace Sensitivity: 5 mV/div Bandwidth:	Tektronix
5	Digital Multimeter	Racal-Dana Instruments 4008
6	Audio Power Meter Input Impedance: 15 Ohms and 600 Ohms	Marconi TF893B
7	AC Voltmeter	Racal-Dana Instruments 9300B or 5002
8	Spectrum Analyser with Tracking Generator Frequency Range:	Marconi 2382 with 2389 Display
9	Signal Combiner	Racal CA612
10	Signature Analyser	Hewlett Packard 5006A
11	BITE Kit (see Chap.7, RA3790 Series Operators Manual for details)	Racal supplied to order
12	Desolder Station	Weller DS801 or Adcola 555 with SM desoldering attachments
13	SMD Desoldering/Reflow tips for soldering irons	Adcola
14	Tweezers, non-magnetic, fine point	
15	Solder Pump or Braid Wick	

DISMANTLING THE RECEIVER

14. The modular design of the equipment keeps to a minimum the amount of dismantling necessary to gain access for maintenance purposes. The boards can be quickly removed and replaced without the use of a soldering iron. Following repair, ensure that all dismantled assemblies are correctly re-assembled and that all covers are replaced.

Fuse Replacement

15. The receiver is fitted with a single supply fuse, a 2 ampere power fuse located in the voltage selector unit on the chassis assembly. A spare 2 ampere mains fuse is also provided in the voltage selector unit.

16. To replace the mains fuse proceed as follows:

    (1) Remove the mains lead.

    (2) Open the cover of the mains filter unit.

    (3) Withdraw the fuse holder and replace the 2 ampere slow-blow fuse. (Racal Part No. 922457). A spare fuse is normally contained in the adjacent spare fuse holder.

    (4) Insert the fuse holder with the arrow pointing in the direction shown on the inside of the cover.

    (5) Close the mains filter unit cover.

    (6) Refit the mains lead.

Board Removal

17. **Analogue Board**

    (1) Disconnect the mains lead.

    (2) Remove the top cover.

    (3) Remove any option boards fitted above the analogue board (see relevant board chapter).

    (4) Remove the 50-way ribbon cable from the digital board.

    (5) Remove the fixings from the three BNC connectors on the rear panel, and remove any connections to SK4 or SK5

(6) Remove fixings securing the board and remove the analogue board from the chassis.

18. **Digital Board**

(1) Disconnect the mains lead.

(2) Remove the top cover and remove any option boards above the digital board.

(3) Disconnect all ribbon cables from the board.

(4) Remove the cannon connector fixings on the rear panel.

(5) Disconnect the power supply cable, remove fixings securing the board and remove the digital board from the chassis.

19. **Front Panel**

(1) Disconnect the mains lead.

(2) Remove the top cover.

(3) Disconnect the mains connector and the 40-way ribbon cable.

(4) Remove the single fixing screw from the bottom of the receiver, remove the four front panel fixing screws and remove the front panel.

20. **Power Supply**

(1) Disconnect the mains lead.

(2) Remove the top cover.

(3) Remove the input and output cables from the power supply

(4) Remove the four fixing screws holding the power supply, and remove the power supply.

21. On a dual receiver use the following procedure:

(1) Disconnect the mains lead.

(2) Remove the six securing screws on the side panel and remove the side panel.

(3) Remove the four pillars holding the power supply, disconnect the input and output cables and then remove the power supply.

22. **Frequency Standard**

(1) Disconnect the mains lead.

(2) Remove the top cover.

(3) Disconnect SK1 from frequency standard.

(4) Remove the four fixing screws, and remove the frequency standard.

BOARD REPAIR

General

23. Board repairs consist mainly of component replacement. It is assumed at this stage that with the aid of the circuit diagram and component layouts the faulty component has been identified.

24. Generally, normal established workshop practices are applicable. However, because the boards use SMDs it is recommended that tools designed for the removal of SMDs are employed. Removed components should be discarded.

SMD Identification and Handling

25. The higher density of SMDs prevents these components being labelled on the PCB. All components are however identified on the appropriate board layout drawings using the component circuit reference numbers.

26. All components are allocated a Racal part number, as specified in the components lists, and this number is clearly marked on packages containing spares supplied by Racal.

27. Because of the small size and lack of marking on some components, it is important that when individual components are removed from the packaging and issued for repair, they are kept in containers marked with the correct part numbers until they are actually fitted to the board. Static sensitive device handling precautions for SMDs are identical to those for conventional leaded components.

SMD Removal

28. Although the repair of boards is possible using conventional tools and techniques, there is a wide range of specially designed tools available which makes the task easier and reduces the chances of damaging the printed circuit board.

29. The simplest tools are SMD desoldering/reflow tips designed to fit conventional soldering irons and desoldering tools. Some incorporate a vacuum pump to melt the solder and a 'sucker' to lift the component off the printed circuit board. Examples of these are listed in Table 2.1.

30. Also available are more sophisticated Rework Stations which include a positioning system, hot air gun for melting the solder, vacuum pump to remove molten solder and built-in microscope for inspection and alignment.

31. It is recommended that the repair workshop is equipped with some SMD repair facility of the type described above. Information on the removal of SM components using these tools will be found in the manufacturer's instructions.

SMD Replacement

32. Surface mounted components may be replaced using a conventional miniature soldering iron and low melting point solder or using a Rework Station with a hot air gun. Before fitting the new component, any excess solder should be removed from the printed circuit board to allow the component to lie flat on the board. To avoid thermal shock to the new component, particularly capacitors, heat should be applied directly to the pads, not the component.

33. Clean the area worked upon, then inspect it to ensure the following:

    (1) No damage to or displacement of adjacent components.

    (2) No damage to tracks or pads.

    (3) No solder bridges, solder spikes or solder splashes.

    (4) No flux residues on the board.

34. The board is now ready for electrical testing.

LOGIC LEVELS

35. TTL (transistor-transistor logic), C-MOS (complementary metal oxide silicon) and ECL (Emitter Coupled Logic) devices are used in this equipment. All types of device are DC voltage level operated, and for this reason, where an oscilloscope is used for monitoring these levels, it should be set for DC coupling.

TTL Voltage Levels

36. Positive logic is utilised, and the voltage levels are defined as follows:

(1) Less than 0.8 V at an input is a logic '0'.
(2) More than 2.4 V at an input is a logic '1'.

Any voltage between 0.8 V and 2.4 V is a potential fault condition, as the input state is then undefined.

C-MOS Voltage Levels

37. The supply and earth (0 V) pins of the C-MOS device are denoted by VDD and VSS respectively. VDD is +5 V for some devices, +12 V for others. C-MOS voltage levels are defined as follows:

(1) More than 70% of the supply voltage (VDD) at an input is a logic '1'.

(2) Less than 30% of the supply voltage at an input is logic '0'.

When related to +5 V and +12 V supplies, the following levels arise:

	VDD at +5 V	**VDD at +12 V**
LOGIC '1'	More than +3.5 V	More than 8.4 V
LOGIC '0'	Less than +1.5 V	Less than +3.6 V

(3) In general, the output of a C-MOS device is VDD for logic '1' and 0 V for logic '0'.

ECL Voltage Levels

38. For the ECL devices used in this equipment, VCC is at +5 volts and VEE is at 0 V; this gives rise to the following input and output logic levels:

Vout High	- 4.24 V to 4.39 V
Vout Low	- 3.35 V to 3.55 V
Vin High	- 4.07 V to 4.19 V
Vin Low	- 3.05 V to 3.72 V

CHAPTER 3

USE OF BUILT IN TEST EQUIPMENT

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CHAPTER 3

USE OF BUILT IN TEST EQUIPMENT

INTRODUCTION

1. The power-up and continuous monitoring BITE tests are executed automatically without operator intervention. Access to the more in-depth BITE facilities is obtained either via the front panel menu system or the remote control port, or by using the switches on the digital board. A summary of the BITE tests is given at the end of this chapter.

INTERPRETATION OF THE FAULT LEGEND

2. During the power-up BITE routine an automatic validity test of data stored when power was switched off is performed. If uncorrupted, this data is used to set up the receiver operational settings. If an error is found, the FAULT indicator is illuminated.

3. The continuous monitoring BITE routines check for correct operation of the receiver during the whole time it is switched on. A detected failure causes the FAULT indicator to be illuminated.

4. In the above cases, more information on the nature of the fault can be obtained using the SHOW FAULT facility accessed via the menu system, as described in Chapter 6, Operator Servicing, of the RA3790 Series Operators Manual.

UNIT CONFIDENCE TEST

5. This BITE facility performs a more comprehensive test of receiver operation and includes a performance check of the signal path using a 5 MHz source as a test signal. In this mode the reception of normal signals is interrupted.

6. Upon detection of a fault condition, the test is halted and the name of the suspect receiver section at fault is displayed. Further information can then be obtained as to the nature of the fault using the BITE operating instructions in the Operators Manual, as before.

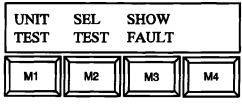
7. It is good practice to make a note of all failed tests so that a more accurate diagnosis can be made.

SELECT TEST

8. This BITE facility is intended as an aid to tracing a fault to component level. It includes all the tests performed by the unit confidence test but allows individual tests to be selected and run repeatedly. It also includes other tests which are not included in the unit confidence test.

9. To access the select test BITE facility, proceed as follows:

(1) Press the MENU pushbutton repeatedly until the following BITE test (level 3) options are displayed:



(2) Press the M2 pushbutton to select the required test option.

(3) Check that a board or section name is displayed on the top line with INC (increment), DEC (decrement), SLCT (select) and EXIT displayed on the bottom line. The digital board receiver processor tests are presented first.

(4) If another board or section is required to be tested, select by pressing the M1 or M2 pushbutton repeatedly until the desired board or section name is displayed.

(5) To select the BITE tests for the displayed module or section, press the M3 pushbutton. The first test for the chosen section is then displayed.

(6) If the displayed test is required to be carried out, press M3 again to select SLCT. The selected test is then performed repeatedly with the result indicated alongside the test title.

(7) To exit the test press M4.

(8) If another test is required, select by pressing M1 or M2 until the desired test is displayed and then select by pressing M3.

(9) To exit to the board or section level display press M4.

(10) To exit to the level 3 options, select EXIT by pressing M4.

(11) Press the RCL pushbutton to exit the menu system and return the receiver to normal operation.

INTERPRETATION OF DIGITAL BOARD INDICATORS

10. Some faults may prevent the menu system from displaying information on the front panel. Similarly, a fault in the remote interface of a receiver intended for remote operation would prevent the receiver controller from examining the fault condition.

11. For reasons such as these, status LED indicators are provided on the digital board. These are described below:

12. LEDs D1 and D14 indicate the status of the control processor, such that they flash green during normal operation, or red if a BITE failure is detected. Any other state indicates that the control processor is not running.

13. LEDs D15 and D16 illuminate to indicate that the two sample clock phase locked loops are in lock. If D15 is off and D16 is on, this indicates that only the second phase locked loop is in lock, and that either the 5 MHz reference input is absent or that the first phase locked loop cannot lock to it. If both LEDs are off, it suggests that the DSPs are not running and so have not programmed the phase locked loop dividers.

SUMMARY OF BITE TESTS

14. Table 3.1 lists the BITE tests provided and indicates if they are performed during the automatic BITE tests, or presented for selection during the manual select BITE tests. A more detailed description of each test is given in the appropriate board chapter.

15. Only the BITE tests applicable to the receiver options fitted are available. On the MA3790 Controller, only the control processor, master/auxiliary, tributary, Rx bus and front panel tests are available (tests 001 to 152).

Table 3.1: BITE Tests

Test No.	Test Name	Power up	Continuous Monitoring	Unit Confidence	Select Test
001	Control Processor EPROM Checksum	YES	NO	NO	NO
002	Control Processor RAM Even Bytes	YES	NO	YES	YES
003	Control Processor RAM Odd Bytes	YES	NO	YES	YES
004	EEROM Test	NO	YES	NO	NO
005	+5 V Digital Rail	NO	YES	YES	YES
006	+15 V Rail	NO	YES	YES	YES
007	-15 V Rail	NO	YES	YES	YES
008	-5 V Rail	NO	YES	YES	YES
009	Digital Board I/O	NO	NO	NO	YES
010	Parallel I/O	NO	NO	NO	YES
051	Master/Auxiliary Port Internal	NO	NO	NO	YES
052	Master/Auxiliary Port External	NO	NO	NO	YES
053	Tributary Port Internal	NO	NO	NO	YES
054	Tributary Port External	NO	NO	NO	YES
055	Diversity Master Link	NO	YES	NO	NO
101	RX Data Bus	YES	NO	YES	YES
102	RX Address Bus	YES	NO	YES	YES
103	RX Bus Control	YES	NO	YES	YES
104	RX BITE Bus	YES	NO	YES	YES
151	Front Panel Display	NO	NO	NO	YES
152	Front Panel Keyboard	NO	NO	NO	YES
201	+5 V Analogue Rail	NO	YES	YES	YES
202	Reference Input Level	NO	YES	YES	YES
203	Reference Lock 1	NO	YES	YES	YES
204	Reference Lock 2	NO	YES	YES	YES
205	Board Interface	NO	YES	YES	YES
206	DSP EPROM Checksum	NO	NO	YES	YES
207	DSP RAM Test High	NO	NO	YES	YES
208	DSP RAM Test Mid	NO	NO	YES	YES
209	DSP RAM Test Low	NO	NO	YES	YES
210	DSP Reset	NO	NO	YES	YES
211	DPRX ASIC Test	NO	NO	YES	YES
212	Sample Rate Clock Test	NO	NO	YES	YES

Table 3.1: BITE Tests (cont.)

Test No	Test Name	Power up	Continuous Monitoring	Unit Confidence	Select Test
213	Peak Detector Level Test	NO	NO	YES	YES
214	Input level/Peak Detector Test	NO	NO	YES	YES
215	IF SNR Test	NO	NO	YES	YES
216	ADC Sampling Clock Lock Test	NO	NO	YES	YES
217	AGC Voltage Test	NO	NO	YES	YES
218	DSP1 IRQA Test	NO	NO	YES	YES
219	Data Bus Parallel I/O Test	NO	NO	YES	YES
220	CODEC 1 Control Test	NO	NO	YES	YES
221	CODEC/Mult.DAC1 Level Test	NO	NO	YES	YES
222	CODEC/Mult.DAC1 SINAD Test	NO	NO	YES	YES
223	Internal Audio Level Test	NO	NO	YES	YES
224	Int. Audio Output SINAD Test	NO	NO	YES	YES
225	Multiplying DAC2 Level Test	NO	NO	YES	YES
226	Multiplying DAC2 SINAD Test	NO	NO	YES	YES
227	IF Valid Line Loopback Test	NO	NO	NO	YES
228	External AGC Loopback Test	NO	NO	NO	YES
229	Audio Line 1 Level Test	NO	NO	NO	YES
230	Audio Line 1 IMD Test	NO	NO	NO	YES
231	Audio Line 2 Level Test	NO	NO	NO	YES
232	Audio Line 2 IMD Test	NO	NO	NO	YES
233	IF Output Level Detector Test	NO	NO	YES	YES
234	IF Output IMD Test	NO	NO	NO	YES

Table 3.1: BITE Tests (cont.)

Test No	Test Name	Power up	Continuous Monitoring	Unit Confidence	Select Test
251	Frequency Standard Level	NO	YES	YES	YES
252	40 MHz Lock Detector	NO	YES	YES	YES
253	Second LO Drive Level	NO	YES	YES	YES
254	VCO Lock Detector	NO	YES	YES	YES
255	First LO Drive Level	NO	YES	YES	YES
256	First LO Sweep	NO	YES	YES	YES
257	First Mixer Sweep	NO	NO	YES	YES
258	Analogue Board Gain	NO	NO	YES	YES
259	RF Amplifier Gain	NO	NO	YES	YES
260	RF Attenuator	NO	NO	YES	YES
261	First IF AGC	NO	NO	YES	YES
262	Receiver Gain	NO	NO	YES	YES
301	CODEC2 Control	NO	NO	YES	YES
302	CODEC2 SINAD	NO	NO	YES	YES
351	FSK Loopback	NO	NO	NO	YES
401	SSI Data Line	NO	NO	NO	YES
402	SSI Sync line	NO	NO	NO	YES

CHAPTER 4

RECEIVER PERFORMANCE TESTING

CONTENTS

Tables

CHAPTER 4

RECEIVER PERFORMANCE TESTING

INTRODUCTION

1. This chapter contains detailed test procedures to check the performance of the complete receiver.The tests can be carried out as part of a routine maintenance schedule or as an aid to fault location. Refer to the appropriate board chapter for fault location information and alignment procedures.

2. It is assumed that the receiver is fitted with an internal frequency standard. If this is not the case, then a suitable external frequency standard must be connected to the rear panel REF IN/OUT connector, SK2.

PRELIMINARY FUNCTIONAL TEST (No test equipment required)

3. Carry out the following procedure to check that the receiver is functioning and that no major faults exist. The tests are written for receivers with full front panel controls but can be adapted for slave receivers by using a controller to operate the receiver via its remote interface.

4. **Procedure**

   (1) Inspect the equipment for signs of physical damage.

   (2) Check all controls for correct mechanical action, i.e. freedom from binding, scraping or general interference of parts.

   (3) Set the REF INT/EXT switch (S1) on the rear panel to INT unless an internal frequency standard is not fitted. Set the other selector switches (S2, S3) for a 10 MHz reference frequency output.

   (4) Connect the receiver to the local source of supply.

   (5) Connect a pair of headphones to the front panel PHONES socket.

   (6) Set the receiver POWER switch to ON.

   (7) Ensure that the front panel displays are activated after a delay of approximately two seconds.

(8) Ensure that the FAULT legend is not visible on the left-hand display. If a fault condition is indicated, use the SHOW FAULT option accessed via the menu system to reveal the nature of the failure (refer to the RA3790 Series Operators Manual for instructions on usage).

(9) Using the menu system, run the unit confidence test as detailed in the Operators Manual.

(10) In the event of a failure occurring during either of the above tests, refer to the receiver servicing chapter in this manual for fault location information.

(11) Select each control function in turn by pressing the appropriate buttons (refer to the RA3790 Series Operators Manual for operating procedures) and observe that the front panel displays indicate that the correct function has been selected and that the tuned and BFO frequencies are correctly displayed.

(12) Set the receiver to 0 MHz. Press the TUNE pushbutton repeatedly until SLOW is indicated on the centre display. Slowly rotate the tuning control clockwise and ensure that the receiver tunes up in 1 Hz steps. Repeat in the anti-clockwise direction. Ensure each tune rate is displayed on the centre display by pressing the TUNE + button repeatedly.

Note: The tune rates are made available for selection by the tune rate list menu facility

(13) Select widest bandwidth, AM detector, Manual IF gain and enter a frequency above 500 kHz. Ensure that the noise output from the receiver varies with the setting of the IF GAIN and VOLUME controls, becoming louder as the controls are advanced.

(14) Select SHORT AGC. Select each bandwidth in turn and ensure that the receiver noise level falls as the bandwidth is reduced.

(15) Select FM and CW and ensure that the character of the noise output changes for each demodulator.

(16) Select CW, MEDIUM AGC, enter tuned frequency 0 MHz, select BFO tune and tune the BFO through the range -8 kHz to +8 kHz using the main tuning knob. Ensure that a beat note corresponding to the BFO offset is audible. Ensure that the front panel loudspeaker output can be switched off and on using the L/S button.

(17) Tune the BFO to +1.00 kHz, and observe that RF and AF levels are indicated as appropriate on the LCD meter scales.

(18) Select SHORT AGC and set the IF GAIN control fully clockwise. Press SQLCH and ensure that the tone disappears (after a delay) when the IF GAIN control is set fully anti-clockwise.

(19) Connect an antenna to the rear panel antenna socket and tune to a known transmission. Refer to the Operators Manual and observe that all controls function normally.

(20) Check the channel memory by storing operational settings and recalling them as instructed in the Operators Manual.

(21) Switch the receiver off and on again to see if it returns to the previous operational settings.

PERFORMANCE TEST PROCEDURE

5. Details of test equipment called up in the following test procedure can be found in Table 2.1 of Chapter 2.

Audio Output Power

6. Connect the signal generator output to the receiver antenna input. Connect the audio power meter to the receiver external loudspeaker output (on the rear panel). Set the power meter load to 8 ohms.

7. Set the receiver as follows:

Mode:	USB
AGC:	Short
Internal Loudspeaker:	Off
Volume control:	Fully clockwise
Frequency:	1.02 MHz

8. Set the signal generator output to -53 dBm, CW, and its frequency to 1.021 MHz.

9. Ensure that the audio output power is not less than 1 W.

10. Transfer the power meter to the PHONES output on the front panel. Set the power meter load to 600 ohms. With the volume control fully clockwise ensure that the power output is not less than 1 mW.

11. Connect the AC voltmeter with 600 ohm load to the receiver line output (on the rear panel). Ensure that the line level is 0 dBm ± 3 dB. If necessary, adjust the line level output (see Operators Manual).

Sensitivity

12. Connect the signal generator output to the receiver antenna input. Connect the AC voltmeter with 600 ohm load to the receiver line output.

13. Set the receiver as follows:

Mode:	USB, 2.7 kHz bandwidth
AGC:	Manual
IF Gain:	Maximum
RF Amplifier:	On

14. Set the signal generator output to -113 dBm, CW.

15. Set the receiver frequency to 0.52 MHz and the signal generator frequency to 0.5215 MHz. Note the reading on the AC voltmeter. Switch off the signal generator output and ensure that the reading on the AC voltmeter drops by not less than 16 dB. This is the S+N/N ratio.

16. Repeat para 15 with the receiver frequency set to 10.52 MHz and the signal generator frequency set to 10.5215 MHz.

17. Repeat para 15 with the receiver frequency set to 20.52 MHz and signal generator frequency set to 20.5215 MHz.

18. Repeat para 15 with the receiver frequency set to 29.52 MHz and the signal generator frequency set to 29.5215 MHz.

19. On the receiver, switch off the RF amplifier. Repeat para 15 to para 18 ensuring that the S+N/N ratio is not less than 10 dB.

20. Set the receiver as follows:

Mode:	AM
Bandwidth:	6 kHz
AGC:	Short
RF Amplifier:	On

21. Set the signal generator output to -103 dBm, 70% AM modulated at 1 kHz.

22. Set the receiver frequency and signal generator frequency to 0.52 MHz. Note the reading on the AC voltmeter. Switch off the signal generator modulation and ensure that the reading drops to not less than 16 dB.

23. Repeat para 22 to measure the AM sensitivity at 29.52 MHz.

Selectivity

24. Connect the signal generator to the receiver antenna input. Connect the RF millivoltmeter (50 ohm input impedance) to the IF output socket (on the rear panel).

25. Set the receiver as follows:

Frequency:	5.5 MHz
Mode:	USB
AGC:	Manual
IF Gain:	Maximum

26. Set the signal generator to 5.501 MHz, CW and its level to -53 dBm.

27. Adjust the IF Gain control for a reading of -10 dBm on the RF millivoltmeter.

28. Select the appropriate mode and bandwidth and carry out the following procedure to check the passband selectivity. The specifications for the standard filters are listed in Table 4.1.

29. Tune the signal generator frequency across the passband of the selected filter and record the maximum output level indicated on the RF millivoltmeter. This peak response is the reference level.

30. Measure the offset frequencies at which the response of the filter is 6 dB down on the reference level noted in para 51. Table 4.1 lists the correct limits for the standard filters.

Table 4.1 Passband Selectivity Characteristics

Filter Number	Filter Type	Offset Frequencies at -6 dB	
		Not Exceeding (kHz)	Not Less Than (kHz)
USB	2.7	+0.3	+0.3
LSB	2.7	-3.0	-3.0
Sym	0.3	-0.15	+0.15
Sym	1.0	-0.5	+0.5
Sym	2.7	-1.35	+1.35
Sym	6.0	-3.0	+3.0
Sym	12.0	-6.0	+6.0

AGC and Manual Gain Control

31. Connect the signal generator output to the receiver antenna input. Connect the AC voltmeter with 600 ohm load to the line output.

32. Set the receiver as follows:

Mode:	USB
AGC:	Short
RF Amplifier:	On
Frequency:	1.02 MHz
Meter:	RF

33. Set the signal generator output to 1.021 MHz, CW, -107 dBm (0 dB µV pd).

34. Note the indication on the AC voltmeter as a reference. Increase the output level of the signal generator in 10 dB steps up to a maximum of +13 dBm. At each step monitor the RF meter on the front panel and ensure that it reads within ±20 dB of the signal generator level. Also observe the AC voltmeter and ensure that the reading remains within ±2 dB of the reference level.

35. Repeat para 34 for AGC medium, omitting the front panel meter tests.

36. Repeat para 34 for AGC long, omitting the front panel meter tests.

37. Set the AGC to manual and the IF Gain control fully clockwise.

38. Set the signal generator to the following output levels in turn and ensure that at each output level the IF Gain control can be used to restore the indication on the AC voltmeter to within ±2 dB of the reference noted at para 34.

- 107 dBm
- 87 dBm
- 67 dBm
- 47 dBm
- 27 dBm
- 7 dBm
+13 dBm

Out of Band IMPs

39. Connect the outputs of the two signal generators to the signal combiner inputs. Connect the AC voltmeter with 600 ohm load to the receiver line output.

40. Set the receiver as follows:

Mode:	CW
Bandwidth:	300 Hz
AGC:	Manual
BFO:	1 kHz
RF Amplifier:	On

41. Set the equipment to the following frequencies:

Receiver:	2.123 MHz
Signal generator 1:	2.148 MHz
Signal generator 2:	2.173 MHz

42. Connect the RF millivoltmeter (50 ohm input impedance) to the output of the combiner.

43. Switch off the output of signal generator 2 and set the output level of signal generator 1 for an indication of -13 dBm on the RF millivoltmeter.

44. Switch off the output of signal generator 1, switch on the output of signal generator 2 and set its output level for an indication of -13 dBm on the RF millivoltmeter.

45. Switch on the output of signal generator 1.

46. Disconnect the combiner output from the RF millivoltmeter and connect it to the receiver antenna input.

47. Adjust the IF Gain control for an indication of 0 dBm on the AC voltmeter. If 0 dBm cannot be achieved then set the IF Gain control fully clockwise. Note the AC voltmeter indication for use as the reference level.

48. Switch off the output of signal generator 2. Set signal generator 1 to the receiver frequency and reduce its output level until the indication on the AC voltmeter is restored to the reference level. Ensure that the reduction in signal generator level is not less than 70 dB.

49. Repeat para 42 to para 48 for the following frequencies:

Receiver:	29.123 MHz
Signal generator 1:	29.148 MHz
Signal generator 2:	29.173 MHz

Cross Modulation

50. Connect the outputs of the two signal generators to the signal combiner inputs. Connect the AC voltmeter with 600 ohm load to the receiver line output.

51. Set the receiver as follows:

Mode:	AM
Bandwidth:	2.7 kHz
AGC:	Short
RF Amplifier:	On

52. Set the equipment to the following frequencies:

Receiver:	5.02 MHz
Signal generator 1:	5.02 MHz (wanted signal)
Signal generator 2:	5.04 MHz (unwanted signal)

53. Connect the RF millivoltmeter (50 ohm input impedance) to the output of the combiner.

54. Switch off the output of signal generator 2 and set the output level of signal generator 1 for an indication of -13 dBm on the RF millivoltmeter.

55. Switch off the output of signal generator 1, switch on the output of signal generator 2 and set its output level for an indication of -13 dBm on the RF millivoltmeter.

56. Switch on the output of signal generator 1.

57. Disconnect the combiner output from the RF millivoltmeter and connect it to the receiver antenna input.

58. Set each signal generator for 30% amplitude modulation at 400 Hz and reduce the output level by 40 dB (to produce a signal at -53 dBm).

59. Note the AC voltmeter indication for use as the reference level.

60. Switch off the modulation of signal generator 1.

61. Increase the output level of signal generator 2 until the AC voltmeter indicates 20 dB below the reference level. Ensure that the increase in signal generator level is not less than 54 dB.

Blocking

62. Connect the outputs of the two signal generators to the signal combiner inputs. Connect the AC voltmeter with 600 ohm load to the receiver line output on the rear panel.

63. Set the receiver as follows:

Mode:	CW
Bandwidth:	2.7 kHz
AGC:	Short
BFO:	1 kHz
RF Amplifier:	On

64. Set the equipment to the following frequencies:

Receiver:	5.02 MHz
Signal generator 1:	5.02 MHz (wanted signal)
Signal generator 2:	5.04 MHz (unwanted signal)

65. Connect the RF millivoltmeter (50 ohm input impedance) to the output of the combiner.

66. Switch off the output of signal generator 2 and set the output level of signal generator 1 for an indication of -13 dBm on the RF millivoltmeter.

67. Switch off the output of signal generator 1, switch on the output of signal generator 2 and set its output level for an indication of -13 dBm on the RF millivoltmeter.

68. Switch on the output of signal generator 1.

69. Disconnect the combiner output from the RF millivoltmeter and connect it to the receiver antenna input. Decrease the output level of both signal generators by 40 dB (to produce a signal at -53 dBm).

70. Note the AC voltmeter indication for use as the reference level.

71. Increase the output level of signal generator 2 until the indication on the AC voltmeter drops by 3 dB.

72. Disconnect the combiner output from the antenna and connect it to the RF millivoltmeter.

73. Switch off the output of signal generator 1 to measure the output level of signal generator 2. Check that it is not less than +7 dBm.

In-Band IMPs

74. Connect the outputs of the two signal generators to the signal combiner inputs. Connect the spectrum analyser input to the MAIN IF OUT socket (SK3) on the rear panel.

75. Set the receiver as follows:

Mode:	CW
Bandwidth:	2.7 kHz
AGC:	LONG
BFO:	1 kHz
RF Amplifier:	On

76. Set the equipment to the following frequencies:

Receiver:	5020.00 kHz
Signal generator 1:	5019.70 kHz
Signal generator 2:	5020.30 kHz

77. Connect the RF millivoltmeter (50 ohm input impedance) to the output of the combiner.

78. Switch off the output of signal generator 2 and set the output level of signal generator 1 for an indication of -13 dBm on the RF millivoltmeter.

79. Switch off the output of signal generator 1, switch on the output of signal generator 2 and set its output level for an indication of -13 dBm on the RF millivoltmeter.

80. Switch on the output of signal generator 1.

81. Disconnect the combiner output from the RF millivoltmeter and connect it to the receiver antenna input.

82. Adjust the spectrum analyser to display the two wanted signals plus the third-order intermodulation products.

83. Check that the third-order intermodulation products are more than 50 dB down relative to the wanted signals.

84. Switch off and disconnect all test equipment.

CHAPTER 5

SIGNATURE ANALYSIS TECHNIQUES

CONTENTS

CHAPTER 5

SIGNATURE ANALYSIS TECHNIQUES

INTRODUCTION

1. Signature analysis is used to aid fault location to component level for digital circuitry on a board. When the board digital circuitry is operating correctly, the non-sequential program instructions cause continuously changing data patterns to be present within the logic circuitry. Because these data patterns are continuously changing, data analysis or data checking using conventional test equipment (oscilloscopes, logic probes, etc.) becomes almost impossible.

2. The signature analysis technique requires the Receiver Processor to continuously execute a short test program and so produce repetitive data patterns at selected data nodes throughout the logic circuitry. If the signature analyzer START, STOP, CLOCK and GROUND leads are connected to appropriate test points, and the signature analyzer probe is connected, in turn, to a number of circuit nodes on a known serviceable unit, then a series of unique 4-digit alpha-numeric 'signatures' will be obtained (a signature is in fact a serial CRC (Cyclic Redundancy Check) signal of the data seen at a given point). If these signatures are recorded, they may be used at a later date as a reference when the same tests are made during the test or fault location procedures. If an incorrect signature is found at a particular node, the operator traces back, with reference to the circuit diagrams, through gates, memory devices, etc. until an element with a correct signature at the input and a faulty signature at the output is isolated.

SIGNATURE ANALYZER HP5006A

3. The specified signature analyzer instrument, the Hewlett Packard HP5006A, is capable of measuring 'normal' signatures and 'qualified' signatures. For normal operation, the signal edge (i.e. rising or falling) for the Clock, Start and Stop inputs is selected using the POLARITY keys. The start signal is applied to the START/ST/SP (green) Timing Pod lead, the stop signal is applied to the STOP/QUAL (red) Timing Pod lead, the clock signal is applied to the CLOCK (yellow) Timing Pod lead, and the measurement is made using the Data Probe. The displayed signature is then entered into the HP5006A memory by pressing the Data Probe switch.

4. During signature analysis measurements, the front-panel GATE LED indicator will flash if the start, stop and clock inputs are valid. The Data Probe tip LED indicator acts as a logic-state indicator, illuminating 'brightly' for a logic high state, 'dimly' for a high-impedance state, and 'off' for a logic low state. The Data Probe tip LED will 'flash' to indicate activity at the node, although the flash duration frequency is modified by internal circuitry and does not reflect the data frequency at the node. The UNSTABLE LED indicator will flash if a difference is detected between two or more successive signatures.

5. The Qualified signature analysis mode (selected by pressing the QUAL function key) is similar to the normal mode, except that the STOP/QUAL Timing Pod input is sensed as a 'data qualifier'. The qualifier input is effectively an enable signal which is used to window the signature measurement within a specific stream of data. In the QUAL mode of operation, the red Timing Pod lead is the QUAL input, the green Timing Pod lead is both the START and STOP input, and the measurement is made using the Data Probe (as for the normal mode of operation).

6. Where a qualifier input is specified in a signature analysis procedure, ensure that the QUAL function is selected, and transfer the STOP/QUAL Timing Pod input lead to the specified node on the card under test. For further information on the use of the HP5006A, refer to the Operating and Service Manual, ref. 05006-90010, supplied with the Signature Analyzer.

SIGNATURE ANALYSIS ROUTINES

7. A common signature analysis routine is used for all boards. The board under test is mounted via the appropriate BITE extender lead (part of BITE kit). The DIL switches on the Digital Board are then used to select the required signature analysis routine. Details of the DIL switch settings are given in the relevant board chapter.

USE OF SIGNATURE TABLES

8. Each relevant board chapter is provided with tables listing unique 4-digit alphanumeric signatures obtained from a known serviceable unit for various nodes throughout the logic circuitry. These signatures then provide the reference for comparison with signatures obtained when the same test is repeated as part of the fault location procedure.

9. To enter the signature analysis mode and set up the signature analyser, proceed as follows:

   (1) Ensure that the receiver is switched off.

   (2) Set the Digital Board switches to the appropriate positions, as given at the beginning of each signature analysis table.

(3) Connect the signature analyser gating inputs to the test nodes given at the beginning of each signature analysis table and set the polarity as indicated.

(4) If necessary, consult the signature analyser operating manual for further detailed instructions on usage.

(5) Switch on the receiver. Examine the test nodes using the logic probe and check the signatures given in the table against the faulty board, working from left to right and top to bottom.

(6) Matching signatures imply correct functioning, incorrect signatures imply the existence of a fault condition. If an incorrect signature is found, consult the relevant circuit diagram and establish the driving logic to determine the faulty component.

(7) The first signature given in each table is for the relevant power supply rail. In addition to checking the IC supplies, a valid signature also verifies that the test equipment is correctly set up.

CHAPTER 6

ANALOGUE BOARD

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CONTENTS (cont.)

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Illustrations

Text:

Illustrations (cont.)

At end of Chapter:

CHAPTER 6

ANALOGUE BOARD

INTRODUCTION

1. The analogue board contains both the signal path and the synthesiser section of the receiver. The signal path accepts RF signals in the range 10 kHz to 30 MHz at the antenna input; these RF signals are mixed with the first local oscillator frequency and produce the first intermediate frequency signal at 40.032 MHz. After filtering and amplification, this signal is mixed with the 40 MHz second local oscillator frequency to produce two single-ended 50 ohm output signals at the second intermediate frequency of 32 kHz.

2. The synthesiser section of the analogue board provides the first local oscillator signal in the range 40.032 MHz to 70.032 MHz for injection into the first mixer. The synthesiser is based on a phase locked loop (PLL) locked to a 1 MHz signal also produced in the reference part of the synthesiser.

3. The reference section provides a 5 MHz signal for the digital board, a 5 MHz signal BITE signal, the 40 MHz second local oscillator signal and the 1 MHz reference signal which is used to lock the synthesisers. The reference section can operate with a choice of a 10 MHz internal standard or an external standard selected for inputs of either 1, 5 or 10 MHz. If the internal reference is selected, then a reference output is also provided at 1, 5 or 10 MHz.

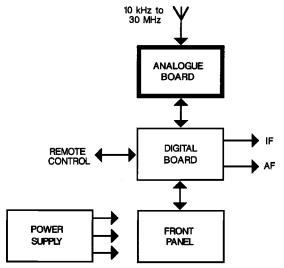


Fig. 6.1 RA3791 Receiver Block Diagram

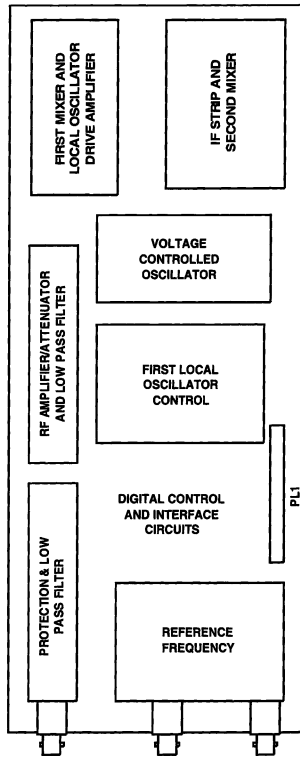


Fig. 6.2 Analogue Board Sub-Module Diagram

BOARD DESCRIPTION

4. The following descriptions should be read in conjunction with the analogue board block diagrams and circuit diagrams included in this chapter. The component references given on a block diagram allow it to be related to the circuit diagram. Sheet numbers refer to the analogue board circuit diagram sheet number. Component layout drawings are also included at the end of the chapter.

Input Protection (Sheet 2)

5. Input protection circuits (Fig. 6.3) are provided to protect the receiver from lightning strikes and from continuous overloads of up to 50 V emf. The circuits include a lightning arrestor, a fuse and protection diodes.

6. The lightning arrestor (SG1) strikes at about 90 volts, thereby limiting the voltage applied to the next stages. The 1 Amp fuse (F1) provides protection for the receiver in the event of failure of the other protection circuits or of an overload greatly exceeding the specification. Protection diodes D31, 32, 34 & 35 are connected in a limiter circuit to limit the signal voltage applied to further receiver input stages.

Muting Circuit (Sheet 6)

7. The muting circuit contains an overload detector (TR8, Sheet 2), an antenna relay (RL1, Sheets 2 and 7) and a mute control circuit (IC11, TR17 - 22, Sheet 6). RF muting is distinguished from antenna relay muting in that it is electronic, muting the first mixer drive level and the first and second IF amplifiers. Muting of the board occurs as a result of:

   (1) An RF input signal exceeding approximately +18 dBm.

   (2) A BITE signal generated by the processor.

   (3) A rear panel hardware mute signal.

   (4) A mute signal generated by the processor in response to a remote command.

8. When the RF input signal exceeds approximately +18 dBm, the overload detector, through the mute control circuit, applies both antenna relay (RL1) and RF mute, thus providing a high degree of muting.

9. During BITE operation, the processor mutes the antenna relay and, during BITE tests, switches on the 5 MHz BITE signal to provide a test signal for injection, via the antenna relay, on to the RF path. In this mode, the RF muting is disabled to allow the test signal to pass through the RF circuits.

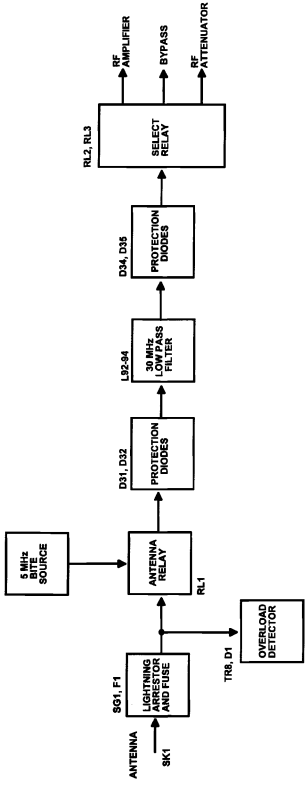


Fig. 6.3 Input Protection

10. The mute control circuit may also be activated to mute the receiver by an external hardware input via the rear panel. Another external mute facility is also available via the bus interface circuits. This responds to the appropriate muting command sent to the Processor when the receiver is under remote control.

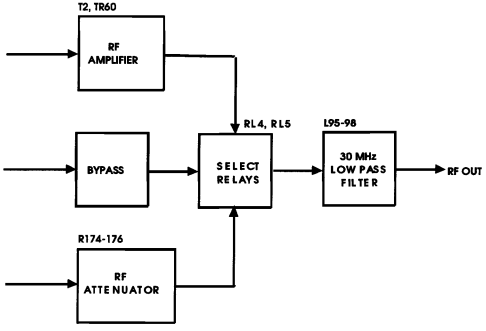


Fig. 6.4 RF Filter, Amplifier and Attenuator

30 MHz Filter and RF Amplifier/Attenuator (Sheets 2 & 3)

11. The 30 MHz low pass filter stages prevent signals at the first image and first IF frequencies from reaching the mixer. They also filter the first LO mixer breakthrough signal thus allowing only a low level of re-radiation from the antenna socket. The low pass filter is implemented in two stages, one preceding and one following the RF amplifier/10 dB attenuator.

12. The RF amplifier (TR60), with a gain of about 9 dB, or the 10 dB attenuator (R174-176), may be switched in or out to provide optimum sensitivity or intermodulation performance as required. Selection of the amplifier, the attenuator or neither is achieved using the front panel menu system or by sending the appropriate remote command. Relay circuits either side of the RF amplifier/attenuator perform the switching.

First Mixer and Drive Amplifiers (Fig. 6.5 & Sheet 4)

13. The first LO input from the VCO is passed through a 40 MHz high pass filter to reject any noise or spurious signals below 30 MHz. It is then applied to the first LO amplifiers to provide a high level drive signal to the first mixer. A first LO level detector is provided to monitor the first LO drive level to the first mixer for the receiver BITE system.

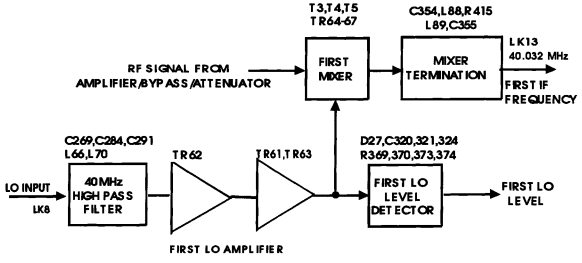


Fig. 6.5 First Mixer and LO Drive

14. The first mixer is of the switching type, consisting of a ring of four FETs; these are switched at the first LO frequency, mixing the incoming RF signal from the antenna to produce the first IF of 40.032 MHz.

40.032 MHz Crystal Filter (Sheet 4)

15. The first mixer output is fed via a mixer termination circuit to a 40.032 MHz crystal filter FL1. This functions as a 'roofing' filter with a centre frequency of 40.032 MHz and a bandwidth of 12 kHz to protect the succeeding receiver circuits from out of band signals and second image frequencies. It also defines the widest available IF bandwidth.

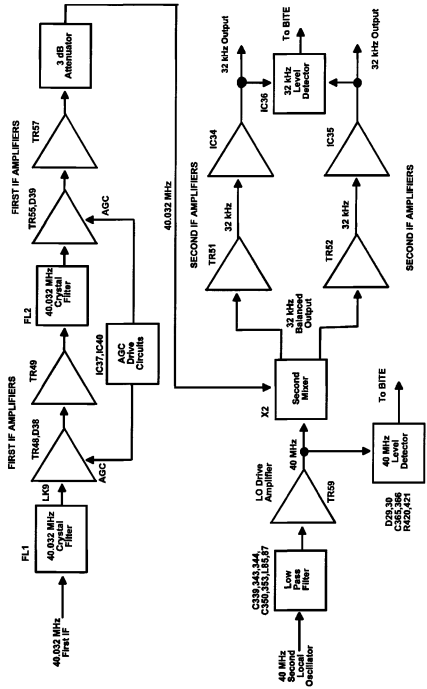


Fig. 6.6 IF Strip & Second Mixer

IF Strip and Second Mixer (Fig. 6.6 and Sheet 5)

AGC Drive Circuit

16. The function of the AGC drive circuit (IC37, IC40) is to convert the first IF AGC voltage, which is provided by the Digital Board, to a current to drive the two PIN diodes (D38 and D39) and to control the gate voltage applied to TR48. The linear change in the first IF AGC voltage is converted to a logarithmic change in PIN diode current in order to obtain the required first IF AGC voltage versus gain reduction characteristic.

17. R395, R396 and IC40(a) provide a temperature compensated reference voltage. IC37(a) and associated components act as a virtual earth amplifier and the linear voltage to log current conversion is performed by IC40(b) and IC40(d) which drive the PIN diodes D38 and D39 respectively. The purpose of transistor IC40(a) is to linearise the AGC characteristic at high input signal levels when the PIN diode currents are largest.

IF Amplifiers (Sheet 5)

18. The two pairs of two IF amplifiers are separated by a second 40.032 MHz crystal filter FL2. The first pair of amplifiers has a tuned FET (TR48) stage with AGC and a non-tuned FET (TR49) amplifier stage. The first stage gain is maximised by varying L100 during the test set up.

19. The second pair of amplifiers are non-tunable FET (TR55 and TR57) amplifiers. The IF strip also has a -3 dB attenuator pad to improve the matching into the second mixer.

20. The gains of the first and third amplifier stages are controlled by adjusting the current through PIN diodes D38 and D39, which are connected to the drains of the FETs in the amplifier stages. This control is achieved since, at 40.032 MHz, the PIN diodes behave as variable resistors as the current is varied accordingly. Hence, as the current is varied by the AGC, the resistance shunting the tuned circuit is also varied, thus changing the stage gain.

21. As the signal at the antenna increases above a defined threshold, the gate voltage for the first FET stage (TR48) is increased in proportion by IC 37(a) in the AGC drive circuit. This optimises the amplifier noise figure for small signals and the signal handling performance for large signals.

Second Mixer and Drive Circuit (Sheet 5)

22. The second mixer (X2) converts the first intermediate frequency signal at 40.032 MHz to the second intermediate frequency of 32 kHz.

23. The second mixer consists of a diode ring switching mixer with a balanced output. It is driven by a 40 MHz local oscillator provided by the reference part of the synthesiser. This 40 MHz reference signal is filtered and then amplified (TR59) to provide a sufficiently large signal to switch the mixer diodes. A

second local oscillator level detector (D29, D30) is provided so that the mixer local oscillator drive level may be monitored by the receiver BITE system on the digital board.

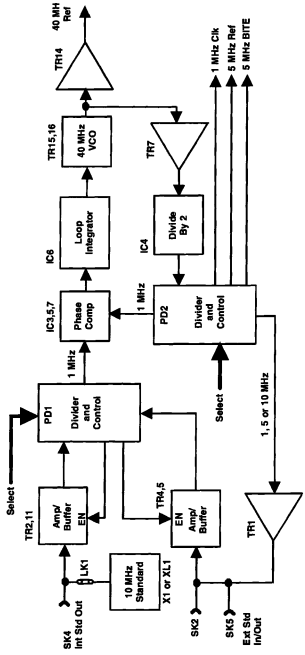


Fig. 6.7 Reference Frequency Generation

Reference Frequency Generation (Fig. 6.7, Sheets 8 & 9)

40 MHz Reference

24. The 40 MHz reference oscillator consists of a crystal (XL2) voltage controlled oscillator (VCO), TR15, TR16. Its nominal frequency of 40 MHz is controlled by the DC voltage applied to a varactor diode (D6) connected in series with the crystal. An increase in varactor voltage causes a decrease in varactor capacitance and hence an increase in oscillator frequency, and vice-versa.

25. The VCO output signal is amplified, shaped and buffered (TR7) in order to provide the feedback stages with squared pulses of sufficient drive level. After further amplification (TR14), the 40 MHz reference signal is used as the second local oscillator signal (para. 23).

1 MHz Reference Output (Sheet 8)

26. A 1 MHz Clock signal, generated by dividing the 40 MHz reference signal, is used as a reference signal for the first LO synthesiser and for the 40 MHz VCO.

Dividers (Sheet 8)

27. A divider chain (PD1, IC4) with a combined division ratio of 40 takes the 40 MHz square wave from the VCO and produces a 1 MHz feedback signal for the phase comparator (IC3, 5, 7). The 1 MHz Clock, 5 MHz Reference, 5 MHz BITE and 10 MHz External Standard outputs are also derived using these divider stages.

5 MHz Output (Sheet 8)

28. A 5 MHz output buffer (IC2(b)) feeds the 5 MHz square wave output from the dividers to a low pass filter (L5, L9, C37, C40, C41, C43, C44). This filter converts the square wave into a 5 MHz sine wave which is used as a reference on the digital board.

Int/Ext Standard Selection (Sheets 8 & 9)

29. The frequency standard is selected by setting the four DIL switches at the rear of the receiver. If 'INT' is selected, the internal 10 MHz frequency standard is chosen. For this case, the output signal selected by switches 2 and 3 is sent to SK2. The frequency selection is made according to Table 6.1 given below.

30. If 'EXT' is selected, the frequency of the external standard must correspond to that given in Table 6.1 as indicated by the switch settings.

Table 6.1 Frequency Standard Selection

SWITCH 1 BROWN	SWITCH 2 RED	SWITCH 3 ORANGE	SWITCH 4 YELLOW	EXTERNAL FREQUENCY STANDARD INPUT	INTERNAL FREQUENCY STANDARD OUTPUT
ON	OFF	OFF	X	-	1 MHz
ON	OFF	ON	X	-	5 MHz
ON	ON	ON	X	-	10 MHz
OFF	OFF	OFF	X	1 MHz	-
OFF	OFF	ON	X	5 MHz	-
OFF	ON	ON	X	10 MHz	-

31. In order to buffer and amplify both the internal and external frequency standard inputs to the reference PLL, two similar input amplifiers are used, each consisting of two high gain transistor stages. Only one amplifier is allowed to operate at a time. This is achieved using the INT/EXT switch (SW1, Sheet 9) and the internal/external standard select circuit (IC25, Sheet 9), which causes the first stage of the unused amplifier to be switched off.

External Reference Output (Sheet 8)

32. When the internal standard is selected, a reference signal is made available at the REF OUT socket (SK2) for external use and is derived from the 40 MHz VCO output divider (PD2) using a reference output frequency select circuit. This circuit is controlled by switch SW1 (Sheet 9) to select the required output frequency, which is fed via output amplifier TR1 to obtain the necessary isolation, impedance and drive level for the external output.

Reference Phase Comparator (Sheet 8)

33. The reference phase comparator produces negative-going output pulses of a length proportional to the phase difference between the 1 MHz reference and feedback signals. If the VCO frequency is too high, IC7(a) is clocked before IC5(a), placing a logic low on IC3(d) pin 12. This has no effect until IC5(a) is clocked and puts a logic low on IC3(d) pin 13, causing both latches to be cleared. Hence the output consists of very short duration negative pulses. In the case of a low VCO frequency, IC5(a) is clocked before IC7(a) and its output remains low until IC5(a) is clocked, thus clearing both latches as before. However, this time a longer duration negative-going output pulse is produced.

34. The nature and timing relationship of these input and output pulses is shown in Fig.6.8. Waveforms are given for the in-lock condition and the out-of-lock condition, when the VCO frequency can be either too high or too low.

Loop Integrator (Sheet 8)

35. The output pulses from the phase comparator are fed to the loop integrator (IC6) which produces a DC voltage at its output. This voltage controls the frequency of the 40 MHz VCO in order to lock the loop.

36. IC7(b) and IC8 form a fast lock detector. If the loop goes out-of-lock, IC7(b) output closes IC8 to reduce the integrator time constant, allowing the loop to lock quickly. A peak detector (D5, C82) provides a DC voltage to the BITE to indicate an out-of-lock condition.

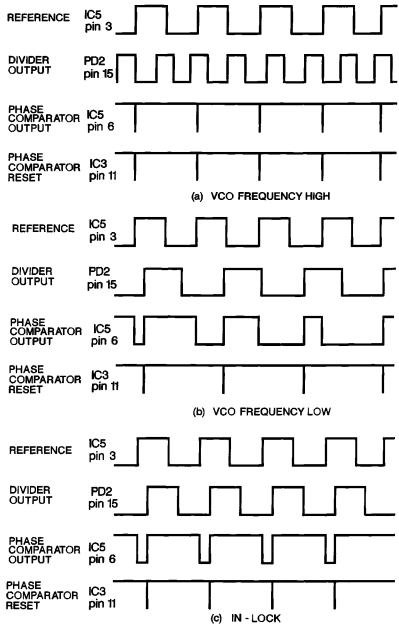


Fig. 6.8 Timing Diagram: Reference Phase Comparator

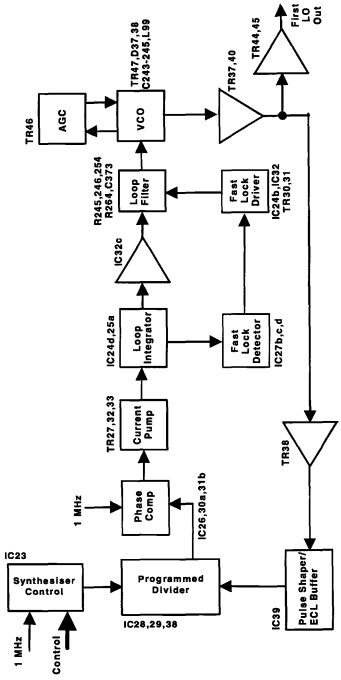


Fig. 6.9 First LO Synthesiser

First Local Oscillator Synthesiser

Basic Synthesiser Operation

37. The basic frequency synthesiser is shown in Fig. 6.10. The output of the VCO is divided by 'N' and compared in a phase comparator with a reference signal. The phase comparator output is filtered and used to control the VCO frequency. Phase lock is achieved when the divided VCO frequency and reference frequency signals are equal in frequency and phase.

38. Use is made of an LSI device containing the synthesiser control circuitry. This controls the division ratio of the divide by 'N' stage in a way that allows fractional division ratios to be obtained. Consequently, tuning resolution down to 1 Hz steps is achieved using a single phase-locked loop. The synthesiser control device is programmed with frequency setting data sent by the Processor via the board data bus.

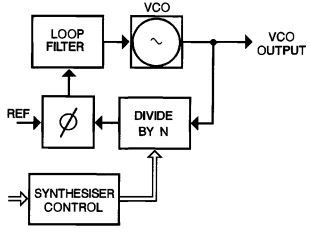


Fig. 6.10 Basic Frequency Synthesiser

Voltage Controlled Oscillator (Sheet 12)

39. The first LO output frequency is derived from a VCO comprising a switched range oscillator (TR47). A VCO range switching circuit allows the VCO to be operated in eight switched ranges using three fixed capacitors as shown in Table 6.2. The capacitors are switched into circuit in a binary sequence by means of transistor switches (TR41, TR42, TR43) controlled by the digital board.

Table 6.2 VCO Range Switching

Range	Receiver Freq. (MHz)	Components Switched In	
7	0.000000 to 1.800000	C243, C244, C245	R68, R74, R75
6	1.800001 to 3.600000	C243, C244	R68, R74
5	3.600001 to 3.800000	C243, C245	R68, R75
4	6.800001 to 9.400000	C243	R68
3	9.400001 to 12.700000	C244, C245	R74, R75
2	12.700001 to 16.300000	C244	R74
1	16.300001 to 23.700000	C245	R75
0	23.700001 to 30.000000	NONE	NONE

40. A DC control voltage is applied to varactor diodes (D36, D37) connected to the VCO tuned circuit. An increase in the varactor voltage causes a decrease in varactor capacitance and hence an increase in oscillator frequency, and vice versa.

AGC Circuit (Sheet 12)

41. An AGC circuit (TR46, D19, D20) maintains the VCO output level constant over the frequency range by setting the VCO bias current in response to variations in the VCO output level. The circuit detects an increase in VCO output level to provide a corresponding decrease in bias current to reduce the gain, and vice-versa.

First LO Output (Sheet 12)

42. The output of the VCO is buffered to an output amplifier (TR44, TR45) which provides the required drive level at the correct impedance for the first LO output. In addition, the VCO signal is fed back to the phase-locked loop via an isolation buffer. The resulting signal is then passed through an ECL pulse shaper and buffer to provide a suitable signal for the programmable divider.

Programmable Dividers (Sheet 10)

43. In the programmable divider, the oscillator frequency is first divided by a dual modulus pre-scaler, IC38. The pre-scaler divides by either 5 or 6 depending on the logic level at the output of IC33(b).

44. Counters IC28 and IC29 are loaded with a preset number by the synthesiser control device (IC23) and then start counting down. The pre-scaler, IC38, is set to divide-by-6 using gate IC33(b). The output of this gate is at logic low whilst counting is in progress because at least one of the counter Q outputs will be at logic high.

45. When the IC28 count sequence reaches number 1, the output of gate IC33(b) goes high, setting the prescaler to divide-by-5 and inhibiting IC28 from counting down any further. Counter IC29 continues counting down until it reaches zero at which point a carry out pulse reloads the counters and the sequence is repeated.

46. Before application to the phase comparator for comparison with the 1 MHz reference signal on the other input, the carry out pulse is synchronised to the counter clock signal by the divider re-clocking latch (IC30(b)).

Synthesiser Control (Sheet 10)

47. The synthesiser control device, IC23, allows the VCO output frequency to be incrementally adjusted in steps which are much less in size than the 1 MHz reference frequency. Computation circuitry within this device processes frequency setting data loaded in from the Processor data bus to control the division ratio of the programmable divider. The actual division ratio is constantly varied between integer values for brief periods of time to give the required non-integer division ratio necessary for fractional division of the feedback signal, thus achieving the required synthesiser resolution.

Phase Comparator and Loop Integrator (Sheet 10)

48. The phase comparator (IC31(b), IC30(a), IC26) produces output pulses of length proportional to the phase difference between the reference and divided feedback inputs. When the Q outputs of both D-type latches of the phase comparator are high, the reset output (TP10) of the flip-flop formed by IC26 goes low. This clears both latches to determine the width of the phase comparator output pulses and causes the Q outputs of both D-type latches to go high again. These outputs cause the reset output of IC26 to go high, ready for the next cycle.

49. The timing relationship between the phase comparator inputs and outputs is shown in Fig. 6.11. Waveforms are given for the in-lock condition and the out-of-lock condition, when the VCO frequency can be either too high or too low.

50. The output pulses are applied to a current pump consisting of switching transistors (TR27, 32 & 33); this produces a mean current output which varies linearly with the phase difference between the two input signals. The circuit action is as follows.

51. Considering first the in-lock condition and referring to the circuit diagram it can be seen that 150 ns pulses are produced at the base of TR27. For each pulse, TR27 switches on and a current I flows out of the integrator (IC25) i.e. I is negative. During the remainder of the cycle the current I into the integrator is such that the average current over the whole 1 µs period is zero, and the loop integrator output voltage remains constant. Under these conditions the short pulses from IC30 are insufficient to switch TR33 on and TR32 is thus switched off.

52. For VCO output frequencies too high, the wider pulses now produced at the base of TR33 switch it and TR32 on. Current is pumped into the integrator and the average current over the whole cycle is positive. The output from the integrator ramps down reducing the VCO varactor voltage, and hence the VCO frequency, until phase lock occurs.

53. For VCO frequencies too low, pulses longer than 150 nanoseconds are now produced at the base of TR27, switching it on for a longer time than in the in-lock condition. This causes more current to flow out of the integrator and the average current over the whole cycle is now negative. The output of the integrator ramps up, increasing the VCO varactor voltage and hence the VCO frequency until phase lock occurs.

54. To compensate for variations in loop gain over the VCO frequency range caused by the change in division ratio, a pulse width to voltage converter circuit is included. In this circuit, Schottky diodes D15 and D16 detect the programmable divider output pulses for integration by IC32(d) into a voltage which increases with an increase in division ratio. This voltage is then used in the current pump to vary the phase comparator gain in proportion to the VCO frequency.

Loop Amplifier and Loop Filter (Sheet 10)

55. The loop integrator output voltage is applied to a loop amplifier and linearisation circuit (IC32(b)). The amplifier gain is adjusted in two ways to compensate for the variation in VCO tuning sensitivity with frequency. Firstly, three resistors are switched into circuit depending on the chosen VCO range, as shown in Table 6.2. Secondly, the amplifier gain is altered when its output voltage exceeds 0.5 V, causing D18 to become forward biased. Both these linearisation methods keep the loop gain constant over each switched VCO range and also over the entire VCO frequency coverage.

56. After amplification and linearisation, the voltage is then filtered in the loop filter and applied as the control voltage to the VCO varactor diodes.

Fast Lock Detector (Sheet 10)

57. The phase locked loop is brought into lock more quickly following a frequency change by the action of a fast lock detector. This consists of a limit comparator (IC27) which senses an out-of-lock varactor voltage resulting from an abrupt change in frequency in either direction. The fast lock detector activates analogue switch IC24. Three of the now closed sections of this switch are used to modify the loop integrator and loop filter by widening the loop bandwidth, and also bring the fast lock driver into operation to force a rapid return to the phase locked condition.

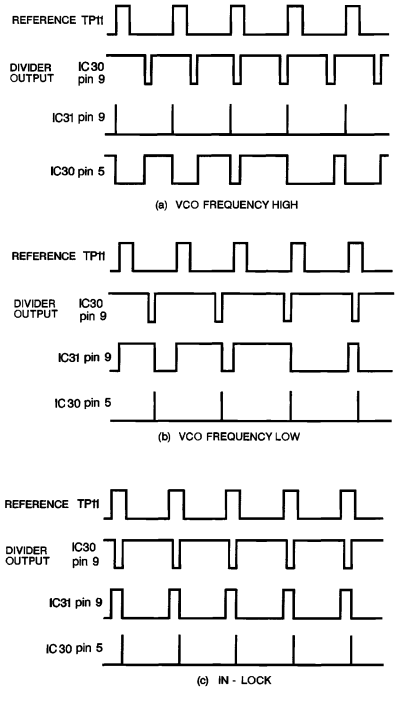


Fig. 6.11 Timing Diagram: LO Synthesiser Phase Comparator

BUS INTERFACE (Sheet 1)

58. A unique hard-wired code is received via the address bus to the analogue board from the processor part of the digital board. This code is used by the address decoder (IC10) to detect addresses on the bus and then produce read or write pulses according to the state of the R/W input. These pulses allow the processor to read the analogue board identification number or write data to the data latches (IC13,19,20) and bus driver (IC18), using the data bus. Pulses on the strobe input ensure correct timing of write pulses. The data latch outputs are used to control the various functions throughout the board.

BITE Measurement System (Sheet 1)

59. The BITE measurement system, comprising a BITE multiplexer (IC14) operating in conjunction with a BITE voltage comparator (IC17(a)), allows the processor part of the digital board to measure various voltages and operating levels on the analogue board. The voltage to be measured is selected by the BITE multiplexer and compared in the BITE comparator with a voltage generated by a digital to analogue converter (DAC) in the processor part of the digital board. The processor measures the level of the selected voltage by applying voltages representing upper and lower limits to the comparator and then monitoring the resulting output.

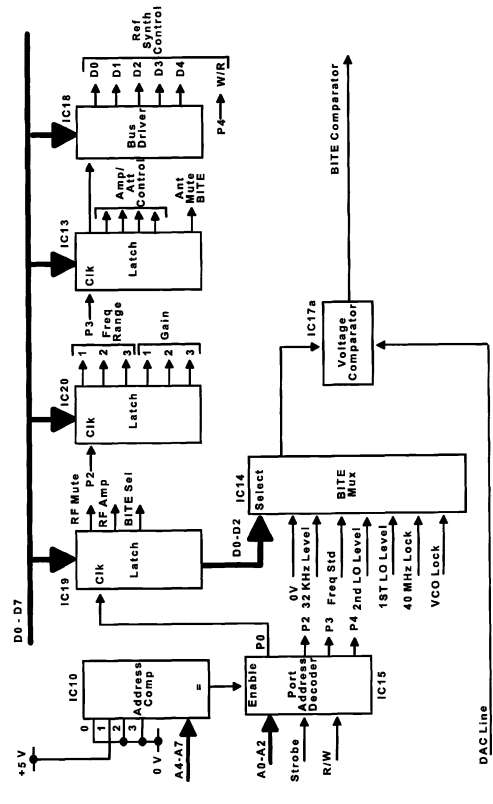


Fig. 6.12 Bus Interface

FAULT LOCATION

General

60. Fault location techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the Analogue Board is given in the following sections.

BITE Tests

61. The following BITE tests for the analogue board are arranged in the order in which they are performed or presented for selection.

Test number:	**251**
Title:	Frequency Standard Level
Performed:	Continuous, unit confidence test, select test.
Description:	BITE multiplexer input 2 is selected and the frequency standard level is measured.
Limits:	Within the range 0.7 to 1.5 volts at TP3.
Fault directory:	Fault no. 7
Test number:	**252**
Title:	40 MHz lock detector
Performed:	Continuous, unit confidence test, select test.
Description:	BITE multiplexer input 5 is selected and the DAC line is set to 0.2 volts (i.e. minimum). The output of the BITE comparator is checked to ensure it is high.
Limits:	Less than 0.5 volts at TP3.
Fault directory:	Fault no. 8
Test number:	**253**
Title:	Second local oscillator drive level
Performed:	Continuous, unit confidence test, select test.
Description:	BITE multiplexer input 3 is selected and the second LO drive level is measured.

Limits:	Within the range 0.3 to 1.5 volts at TP3.
Fault directory:	Fault no. 5
Test number:	**254**
Title:	VCO lock detector
Performed:	Continuous, unit confidence test, select test.
Description:	BITE multiplexer input 6 is selected and the DAC line is set to 0.5 volts (i.e. minimum). The output of the BITE comparator is checked to ensure it is high.
Limits:	Less than 0.5 volts at TP3.
Fault directory:	Fault no. 9
Test number:	**255**
Title:	First local oscillator drive level
Performed:	Continuous, unit confidence test, select test.
Description:	BITE multiplexer input 4 is selected and the first LO drive level is measured.
Limits:	Within the range 0.8 to 2.55 volts at TP3.
Fault directory:	Fault no. 4
Test number:	**256**
Title:	First LO sweep
Performed:	Unit confidence test, select test.
Description:	BITE multiplexer input 6 is selected. Checks the first LO is locked at the edges of each LO range. Also checks the VCO is out of lock when trying to lock to 0 MHz with 5 MHz settings.

Limits:	Less than 0.5 volts at TP3 for VCO settings at each end of the frequency ranges.
Fault directory:	Fault no. 10
Test number:	**257**
Title:	First Mixer sweep
Performed:	Unit confidence test, select test.
Description:	BITE multiplexer input 4 is selected. The drive level is measured at RF frequencies of 0, 5, 10, 15, 20, 25 and 30 MHz.
Limits:	Within the range 0.8 to 2.55 volts at TP3.
Fault directory:	Fault no. 4
Test number:	**258**
Title:	Analogue board gain
Performed:	Unit confidence test, select test.
Description:	BITE multiplexer input 1 is selected and the 5 MHz BITE signal energised with the RF amplifier on and AGC set to maximum gain. Measure the 32 kHz level output.
Limits:	Within the range 0.6 to 2.55 volts at TP3.
Fault directory:	Fault no. 6
Test number:	**259**
Title:	RF amplifier gain
Performed:	Unit confidence test, select test.
Description:	BITE multiplexer input 1 is selected and the 5 MHz BITE signal energised with the RF amplifier on and AGC set to maximum gain. Measure the 32 kHz level output (level 1). Note the level and then select RF amplifier off and re-measure the 32 kHz level output (level 2).
Limits:	Level 2 < level 1 divided by two
Fault directory:	Fault no. 6

Test number:	**260**
Title:	RF attenuator
Performed:	Unit confidence test, select test.
Description:	BITE multiplexer input 1 is selected and the 5 MHz BITE signal energised with the RF amp off and AGC set to maximum gain. Measure the 32 kHz level output (level 1). Note the level, select attenuator on and remeasure the 32 kHz level output (level 2).
Limits:	Level 2 < level 1 divided by two
Fault directory:	Fault no. 6
Test number:	**261**
Title:	First IF AGC
Performed:	Unit confidence test, select test.
Description:	With the RF Amplifier OFF, MANUAL gain, and the receiver tuned to 5 MHz, 3k Hz bandwidth, CW , the 5 MHz BITE signal is switched on.
Limits:	For each 10 dB step in the first IF AGC up to 60 dB of gain reduction, the RF metering is checked to be within ± 6dB of the expected level.
Fault directory:	Fault no. 6
Test number:	**262**
Title:	Receiver gain
Performed:	Unit confidence test, select test.
Description:	With the RF Amplifier ON, SHORT AGC and the receiver tuned to 5 MHz, 3k Hz bandwidth, CW , the 5 MHz BITE signal is switched on. The DSP then performs a SINAD measurement.
Limits:	> 35 dB SINAD
Fault directory:	Fault no. 6

FAULT DIRECTORY

62. Use the following fault directory to identify the fault condition and take the necessary corrective action. Note that all inputs are assumed to be correct.

Table 6.3 Fault Directory

Fault No.	Fault Symptom	Possible Causes	Suggested Action
1	Fails to run BITE tests for analogue board	Address decoding/board ident. not responding	Check address decoding/board ident. logic operation using signature analysis routine if necessary.
2	BITE indicates failure but manual check shows no fault.	(a) BITE hardware fault. (b) Faulty BITE detector.	Select all BITE tests for the board to check multiplexer action for all inputs. Use signature analysis routine to check multiplexer addressing
3	Unable to control one or more functions.	Board interface faulty.	Check status of appropriate select line using oscilloscope.
4	First mixer drive level low.	Faulty first LO drive circuit.	Follow first mixer LO drive check procedure.
5	Second mixer drive level low.	Faulty second LO drive circuit.	Follow second mixer LO drive check procedure.
6	Low sensitivity/gain	Low gain in signal path.	Follow AGC drive check procedure.
7	Internal/external reference level fault.	(a) Internal/external reference not present at input. (b) Input amplifier failure.	(a) Check switch settings or supply. (b) Check signal levels.
8	40 MHz incorrect	40 MHz oscillator out of lock.	Check 40 MHz loop.
9	Synthesiser frequency incorrect.	No 1 MHz reference to PLL or PLL out of lock.	Follow synthesiser loop check procedure.
10	Synthesiser frequency incorrect for part of a range.	VCO linearisation or range switching fault.	Check operation of dividers, pulse width to voltage converter and VCO linearisation.
11	Synthesizer frequency incorrect on one or some ranges.	Range or VCO switching fault.	Check action of VCO or loop amplifier range switching components.
12	VCO level low or varies with frequency.	VCO or output stage fault.	Check signal levels around these circuits.
13	Synthesiser responds slowly to sudden tuning changes.	Fast lock circuit not functioning.	Check circuit levels.
14	5 MHz level low.	5 MHz output circuit fault.	Check divider, 5 MHz output buffer and low pass filter operation.
15	Reference output low or absent.	(a) Board not set for operation from internal reference. (b) Reference output select circuit or amplifier fault.	(a) Check switch settings. (b) Check circuit operation, and signal levels.
16	Out-of band IMPs, cross-modulation.	(a) Low LO drive to first mixer. (b) first mixer faulty.	(a) See fault 4 (b) Check components, especially FETs. (c) Follow relevant part of the signal path check procedure.
17	Internal spurious responses.	Incorrectly fitting covers and lids.	Refit correctly.
18	In-band IMPs	Distortion in any stage of signal path.	See fault nos. 4,5 and 6.2
19	No response to external mute (from rear panel or remote control).	Faulty mute circuit.	Follow mute circuit check procedure. Use signature analysis routine to check mute circuit output signals.
20	Poor selectivity.	Alignment requires adjustment.	Follow alignment procedure.

FIRST MIXER LO DRIVE CHECK PROCEDURE

63. Tune the receiver to 30 MHz. Measure the LO drive level by connecting LK11 position B to the oscilloscope input, set for 50 ohms input impedance. With LK12 set to positions B and D in turn, ensure that the waveform is greater than 0.55 V pk-pk at 70.032 MHz.

SIGNAL PATH CHECK PROCEDURE

Overall Board Gain Test

64. Set the AGC to manual and set the IF gain control fully clockwise. Switch the RF amp in and inject a test signal of -73 dBm at the antenna input (SK1). Measure the IF output level at LK10 using the RF millivoltmeter high impedance probe. If the gain does not conform to the signal level chart (see Fig. 6.13), then perform the next test.

32 kHz IF Amplifier Test

65. Set the AGC to manual and set the IF gain control fully clockwise. Switch the RF amp in and inject a test signal of -73 dBm at the antenna input (SK1). Measure the IF output at LK10 using the RF millivoltmeter high impedance probe. Check that the result agrees with the signal level chart. If the result is correct, adjust R316 and R317 in accordance with the alignment procedure before checking voltages around the suspect 32 kHz IF amplifier. If the test fails then proceed with the following tests in sequence until the fault is found.

Protection Circuit, LPF and RF Amplifier Test

66. Inject a test signal of 0 dBm at the antenna input (SK1). The gain from the antenna input may be checked against the signal level chart first at LK3, then at LK7. For each test remove the link and connect the RF millivoltmeter set for 50 ohms input impedance. Repeat the test at LK7 with the RF amplifier switched into circuit and check that the gain has increased by 9 dB as shown in the signal level chart.

First Mixer and Roofing Filter Test

67. Before checking these circuits ensure that the first LO drive level is sufficient. Inject a test signal of 0 dBm at the antenna input (SK1). Measure the gain from the antenna input to LK9, by removing the appropriate link and connecting the RF millivoltmeter set for 50 ohms input impedance. The gain should correspond to that shown in the signal level charts. If this figure is low then check the insertion loss of the roofing filter (FL1) by injecting a test signal of 0 dBm at LK13 and measuring the output at LK9. Check the measurement figure against the signal level chart.

40.032 MHz IF Amplifier Test

68. Because the IF amplifier gain is automatically controlled, the AGC drive circuit should be verified first (see para. 70). If this is satisfactory, proceed with checking the IF amplifier as follows.

69. Set the AGC to manual and set the IF gain control fully clockwise (i.e. maximum gain). Switch the RF amp in. Inject a test signal of -53 dBm at the antenna input (SK1). Measure the gain from the antenna input to LK14, using the RF millivoltmeter set to 50 ohms input impedance. Check that the gains are as shown on the signal level chart.

Second Mixer Test

70. Prior to checking the second mixer, ensure that the second LO drive level is sufficient (Test 253). Switch the RF amplifier in and inject a test signal of -53 dBm at the antenna input (SK1). Measure the gain from antenna input to LK4 and LK5 respectively using the RF millivoltmeter high impedance probe. Check that the gain is as shown on the signal level chart.

AGC Drive Circuit Check Procedure

71. Set the AGC to manual. As the IF gain control is turned anti-clockwise the first IF AGC voltage is reduced and the current through PIN diodes D38 and D39 is increased. This reduces the gain of IF amplifiers TR48 and TR55. The table below indicates the gain reduction against voltages which may be measured as the first IF AGC voltage, at TP17, is varied using the IF gain control.

Table 4: AGC Voltage/Gain Reduction Figures

AGC Voltage (TP17)	Gain Reduction
10 V	0 dB
9 V	3.5 dB
8 V	16 dB
7 V	13 dB
6 V	22 dB
5 V	33 dB
4 V	47 dB
3 V	65 dB

Muting Circuit Check Procedure

72. Set the AGC to manual and set the IF gain control fully clockwise. Connect PL1/28 to 0 V to activate the 'hardware' mute (the MUTE legend should appear on the centre display). Check that the mute circuit inhibits the AGC drive circuit by ensuring TP17 is at 0 V.

40 MHZ LOOP CHECK PROCEDURE

1 MHz Reference

73. Check the SW1 switch settings (Sheet 9) and the position of LK2. Ensure that if internal standard is selected, the corresponding output signal is present at SK2. If external standard is selected, ensure that a signal at the correct frequency and level (greater than 70 mV rms) is applied to SK2.

74. Check the reference input to the phase comparator at IC5 pin 3 and ensure that the frequency is 1 MHz. When the loop is locked the VCO frequency is 40 times the frequency at IC5 pin 3. The loop will not lock if the frequency at IC5 pin 3 differs from 1 MHz by more than 85 Hz.

40 MHz VCO

75. Ensure that the VCO oscillates and that the drive to the divide by two stage is adequate. Check the frequency of oscillation by connecting a frequency counter to C71. The VCO tuning may be checked by removing LK2 and connecting a variable DC power supply between the R88 side of LK2 and ground to provide a tuning voltage. As the tuning voltage is adjusted in the range 2 V to 8 V it should be possible to tune the VCO over the range at least 40 MHz ±1500 Hz.

Dividers

76. Check that the dividers in the loop are working correctly and that the frequency at PD2 pin 15 is the VCO frequency divided by 40.

Phase Comparator and Loop Integrator

77. The operation of the phase comparator can be checked initially by manually tuning the VCO as described above. When the frequency at PD2 pin 15 is greater than the frequency at IC5 pin 3, the phase comparator outputs should be similar to Fig. 6.8(a) (short pulses at IC5 pin 5, longer pulses at IC7 pin 5) and the loop integrator output should be driven high (greater than 12 V). When the frequency at PD2 pin 15 is less than the frequency at IC5 pin 3, the above situation should be reversed, with the phase comparator output similar to Fig.6.8(b).

Overall Loop

78. Remove the DC power supply and replace LK2. The loop should lock with the phase comparator waveforms being similar to Fig. 6.8(c). The loop integrator should produce a steady DC output at IC6 pin 6 to set the VCO frequency to 40 MHz (40 times the frequency at IC5 pin 3). If there is any instability (an AC waveform at IC6 pin 6), check the components in the loop integrator and the fast lock circuit. In the latter circuit IC18 should be switched off (0 V at IC18 pin 11).

LO SYNTHESISER LOOP CHECK PROCEDURE

1 MHz Reference

79. Check the reference input to the phase comparator at TP11 and ensure that the frequency is 1 MHz.

LO VCO

80. Ensure that the LO VCO oscillates and that the drive level to the programmable divider at IC39 pin 3 is adequate (i.e. ECL levels). The tuning of the VCO may be checked by connecting a variable DC power supply between the R245 side LK6 (remove link first) and 0 V. Connect a frequency counter to LK8 and tune the receiver frequency to each frequency range in Table 6.1. As the tuning voltage is varied over the range -11 V to +11 V it should be possible to tune the VCO over the frequencies shown in Table 6.1.

Programmable Divider

81. An indication that the programmable divider is functioning in basic terms may be obtained by checking that a waveform is present at the output of the divider re-clocking stage (IC38 pin 7). If absent, check that the clock input is present at IC38 pin 15 and is divided by the prescaler, producing a lower frequency at IC38 pin 7. The division ratio of the prescaler is continuously being changed by the output of gate IC33(b). If this output is always high or low, check that the presettable binary counters are being loaded with preset data from IC23 by a negative-going pulse at the carry out (IC29 pin 15).

82. The preset data can be checked by setting the receiver to 2.968 MHz (giving an LO frequency of 43 MHz) and monitoring the following logic levels:

IC28 pin:	3	high	IC29 pin:	3	low
	4	high		4	low
	5	high		5	high
	6	low		6	low

If these levels are incorrect, carry out the synthesiser control checks contained in the overall loop check procedure.

LO Phase Comparator and Loop Integrator

83. An initial check of the LO phase comparator operation may be carried out by tuning the VCO with a DC voltage applied to LK6, as before. Set the receiver to 2.968 MHz (to set the LO frequency nominally to 43 MHz) and the DC voltage to approximately 1 V. Adjust to give a VCO frequency of greater or less than 43 MHz as described below.

84. When the frequency at IC30 pin 9 is greater than at TP11 (i.e. VCO frequency high) the phase comparator outputs should be similar to Fig.6.11(a) (short pulses at IC31 pin 9, longer pulses at IC30 pin 5) and the loop integrator output at IC25 pin 6 should be driven low (less than -9 V). When the frequency at IC30 pin 9 is less than that at TP11 (i.e. VCO frequency low) the phase comparator outputs should be similar to Fig.6.11(b) and the loop integrator output at LK6 should be driven high (greater than +9 V).

Overall Loop

85. With the DC power supply removed and the link replaced the loop should lock with the phase comparator waveforms similar to Fig.6.11(c). The loop integrator should produce a steady DC output voltage at LK6. If there is any instability (an AC waveform at LK6) check the components around the integrator, and the fast lock circuit.

86. If the output frequency does not respond to changes in the setting of the main tuning knob, check IC23 divide outputs. The signal levels on these outputs should be changing as the receiver is tuned across its entire frequency range.

87. To determine if the fault is in IC23, the input data to the device should be checked next. This can be carried out by checking that the write strobe on pin 24 and the levels on data lines D0 to D4 toggle as the synthesiser frequency is tuned. Also check high levels are present on pins 15 and 37 (low levels on pins 42 and 50).

BOARD ALIGNMENT

88. The board is aligned at the factory during production test. All adjustable components should be left undisturbed unless a known misalignment has been established following, for example, component replacement.

89. Do not attempt the following procedures unless the test equipment called-for is available, and where applicable, has been suitably calibrated.

Test Equipment

90. The following items of test equipment, as detailed in Chapter 2, are required for aligning the Analogue Board:

(1) BITE Kit
(2) Spectrum Analyser and Tracking Generator
(3) Signal Generator
(4) RF Millivoltmeter
(5) AC Voltmeter
(6) Digital Multimeter
(7) Frequency Counter

Preliminary

91. Remove the Analogue Board from the receiver and place it on the bench next to the receiver. Remove the screening lids from the board to gain access to the preset components. Reconnect the board to the receiver using the extender assembly provided with the BITE Kit. Adjust the preset components according to the following alignment procedure.

Three-Section Low Pass Filter

92. Connect the tracking generator output, set to -10 dBm, to the antenna input (SK1). Remove the shorting link from LK3. Connect the spectrum analyser input to LK3 (position D). Adjust coils L92, L93, and L94 for stopband notches (minimum amplitude) at the centre frequencies given below:

L92: 77.8 MHz
L93: 40.032 MHz
L94: 48.41 MHz

93. Repeat as necessary. Check that the insertion loss is less than 2 dB up to 30 MHz. Check that the stopband up to 100 MHz is better than 38 dB. Refit shorting link to LK3 position C.

Four-Section Low Pass Filter

94. Remove the shorting links from LK3 and LK7. Connect the tracking generator output, set to -10 dBm, to LK3 (position B). Connect the spectrum analyser input to LK7 (position D). Ensure that the RF amplifier is switched out of circuit. Adjust coils L96, L97 and L98 for stopband notches at the centre frequencies given below:

    L96: 46.53 MHz
    L97 41.39 MHz
    L98: 57.88 MHz

95. Repeat procedure as necessary and then adjust coil L95 for minimum insertion loss up to 30 MHz with the spectrum analyser set to display the filter passband from 20 MHz to 30 MHz. Check that the insertion loss up to 30 MHz is less than 2 dB and that the stopband up to 100 MHz is better than 60 dB. Refit shorting links to LK3 position C and LK7 position C.

Overall 30 MHz Low Pass Filter

96. Remove the shorting link from LK7 and ensure that the RF amplifier is switched out of circuit. Connect the tracking generator output, set to -10 dBm, to the antenna input (SK1). Connect the spectrum analyser input to LK7 (position D) to display the overall filter passband from 20 MHz to 30 MHz. Adjust L95 to achieve minimum insertion loss up to 30 MHz. Check that the insertion loss up to 30 MHz is less than 2 dB. Refit shorting link to LK7 position C.

First IF Amplifier Adjustment

97. Remove the shorting links LK9 and LK14. Connect the signal generator output, set to -77 dBm at a frequency of 40.032 MHz, CW, to LK9 (position B). Connect the spectrum analyser input to LK14 (position D). Set the AGC to manual and set the IF gain control fully clockwise. Adjust coil L100 to give a maximum signal output at 40.032 MHz. Repeat alignment with the spectrum analyser set for greater sensitivity.

98. Note the signal level on the spectrum analyser. Set the IF gain control fully anti-clockwise. Increase the signal generator output level from -77 dBm to achieve the same output level as noted earlier. The AGC range is given by the required increase in the signal generator output level, which should be greater than 65 dB. Refit the shorting links LK9 and LK14 to position C.

Analogue Board Gain Adjustment

99. Set the IF gain control fully clockwise and switch the RF amplifier into circuit using the menu system. Ensure that the receiver is tuned to 15.02 MHz. Connect the signal generator output, set to -53 dBm at a frequency of 15.02 MHz, CW, to SK1 the antenna input. Connect the AC voltmeter to LK4 (position D), the 32 kHz output, terminated into a 50 ohm load, and set to read dBm.

100. Measure the output signal and adjust R316 to give an output reading of -6 dBm.

101. Connect the AC voltmeter to LK5 (position D), the 32 kHz output, terminated into a 50 ohm load, and set to read dBm.

102. Measure the output signal and adjust R317 to give an output reading of -6 dBm.

VCO Frequency Adjustment

103. Place LK6 in position B. Tune the receiver to 24.0 MHz. Connect the frequency counter to LK8 (position D). Adjust L99 for an output frequency of between 67.21 MHz and 67.25 MHz. Replace LK6 in (position C).

SIGNATURE ANALYSIS

104. A signature analysis routine, to assist in the location of a fault, is detailed below. This routine checks that the control signals are interfaced and decoded correctly by the analogue board.

IMPORTANT: Only the analogue board should be connected to the digital board during this test. Isolate the front panel by disconnecting PL2 on the digital board.

105. Digital board SW1 DIL switch settings: 1, 2, 4, 7 OFF
3, 5-6, 8 ON

106. Signature analyser connection and settings:

Start:	PL2-9 on digital board, negative trigger.
Stop:	PL2-9 on digital board, negative trigger.
Clock:	PL2-11 on digital board, positive trigger.
Earth:	TP5 on digital board

Note: Signatures xxxxF signify a flashing probe indicator with the same signature as either the 0 volt or 5 volt supplies.

Table 6.5 Signature Analysis

Signal	Signature	Test Node
+5V	A2C3	IC10-16
0V	0000	IC10-8
D0	1292	PL1-13 IC9-3 IC18-2 IC13-3 IC20-3 IC19-3
D1	5H2P	PL1-14 IC18-4 IC13-4 IC20-4 IC19-4
D2	7H4U	PL1-15 IC18-6 IC13-6 IC20-6 IC19-6
D3	5241	PL1-16 IC18-10 IC13-11 IC20-11 IC19-11
D4	7AU8	PL1-17 IC18-12 IC13-13 IC20-13 IC19-13
D5	H19A	PL1-18 IC18-14 IC13-14 IC20-14 IC19-14
A0	0U7P	PL1-3 IC15-1
A1	366H	PL1-4 IC15-2
A2	UFP6	PL1-5 IC15-3
A4	A2C3	PL1-7 IC10-10
A5	0001	PL1-8 IC10-12
A6	0000	PL1-9 IC10-13
A7	0001	PL1-10 IC10-15
STROBE	0000F	PL1-11 IC15-4
R/W	0000F	PL1-12 IC9-1 IC15-5
IC10-6	A2C2	IC10-6 IC9-2 IC15-6
PORT0	FA8A	IC15-15 IC19-9
PORT2	9CA0	IC15-13 IC20-9
PORT3	AHFF	IC15-12 IC13-9
PORT4	5P54	IC15-11 IC23-24
IC19-2	050U	IC19-2 IC14-11
IC19-5	8788	IC19-5 IC14-10
IC19-7	46FC	IC19-7 IC14-9
IC20-2	3663	IC20-2
IC20-5	55AC	IC20-5
IC20-7	644U	IC20-7
IC20-10	9CA0	IC20-10

Table 6.5 Signature Analysis (cont.)

Signal	Signature	Test Node
IC20-12	5241	IC20-12
IC20-15	U6U8	IC20-15
IC13-2	052A	IC13-2 IC18-15
IC18-3	17C8	IC18-3 IC23-17
IC18-5	5804	IC18-5 IC23-18
IC18-7	7865	IC18-7 IC23-19
IC18-9	576C	IC18-9 IC23-20
IC18-11	7UH2	IC18-11 IC23-22

COMPONENTS LIST

ANALOGUE BOARD ASSEMBLY
PART No. 91221-02
DRAWING No. DA91221 ISSUE 2C

REF	DESCRIPTION	PART No.
CAPACITORS		
C1	CHIP 1 N 5% 50 V CER C	999154/102P
C2	CHIP 33 P 5% 50 V CER C	999154/330P
C3	CHIP 33 P 5% 50 V CER C	999154/330P
C4	CHIP 10 N 5% 50 V CER X	999151/103P
C5	CHIP 10 N 5% 50 V CER X	999151/103P
C6	CHIP 10 N 5% 50 V CER X	999151/103P
C7	CHIP 10 N 5% 50 V CER X	999151/103P
C8	CHIP 10 N 5% 50 V CER X	999151/103P
C9	CHIP 1 U 20% 35 V TAN	945049
C10	CHIP 10 N 5% 50 V CER X	999151/103P
C11	CHIP 10 N 5% 50 V CER X	999151/103P
C12	CHIP 10 N 5% 50 V CER X	999151/103P
C13	CHIP 10 N 5% 50 V CER X	999151/103P
C14	CHIP 10 N 5% 50 V CER X	999151/103P
C15	CHIP 1 U 20% 35 V TAN	945049
C16	CHIP 1 N 5% 50 V CER C	999154/102P
C17	CHIP 1 U 20% 35 V TAN	945049
C18	CHIP 1 N 5% 50 V CER C	999154/102P
C19	CHIP 100 N 10% 50 V CER X	948163
C20	CHIP 10 N 5% 50 V CER X	999151/103P
C21	CHIP 10 N 5% 50 V CER X	999151/103P
C22	CHIP 10 N 5% 50 V CER X	999151/103P
C23	CHIP 10 N 5% 50 V CER X	999151/103P
C24	CHIP 1 N 5% 50 V CER C	999154/102P
C25	CHIP 10 N 5% 50 V CER X	999151/103P
C26	CHIP 10 N 5% 50 V CER X	999151/103P
C27	CHIP 100 N 10% 50 V CER X	948163
C28	CHIP 56 P 5% 50 V CER C	999154/560P
C29	CHIP 1 U 20% 35 V TAN	945049
C30	CHIP 220 N 5% 50 V CER X	999150/224P

REF	DESCRIPTION						PART No.
C31	CHIP 10	N	5%	50	V	CER X	999151/103P
C32	CHIP 220	N	5%	50	V	CER X	999150/224P
C33	CHIP 10	N	5%	50	V	CER X	999151/103P
C34	CHIP 10	N	5%	50	V	CER X	999151/103P
C35	CHIP 220	N	5%	50	V	CER X	999150/224P
C36	CHIP 10	U	20%	25	V	TAN	Y00643
C37	CHIP 1	N	5%	50	V	CER C	999154/102P
C38	CHIP 10	N	5%	50	V	CER X	999151/103P
C39	CHIP 10	N	5%	50	V	CER X	999151/103P
C40	CHIP 68	P	5%	50	V	CER C	999154/680P
C41	CHIP 1	N	5%	50	V	CER C	999154/102P
C42	CHIP 10	N	5%	50	V	CER X	999151/103P
C43	CHIP 1	N	5%	50	V	CER C	999154/102P
C44	CHIP 150	P	5%	50	V	CER C	999154/151P
C45	CHIP 10	N	5%	50	V	CER X	999151/103P
C46	CHIP 1	N	5%	50	V	CER C	999154/102P
C47	CHIP 39	P	5%	50	V	CER C	999154/390P
C48	CHIP 22	P	5%	50	V	CER C	999154/220P
C49	CHIP 10	N	5%	50	V	CER X	999151/103P
C50	CHIP 10	N	5%	50	V	CER X	999151/103P
C51	CHIP 10	N	5%	50	V	CER X	999151/103P
C52	CHIP 10	N	5%	50	V	CER X	999151/103P
C53	CHIP 220	N	5%	50	V	CER X	999150/224P
C54	CHIP 10	N	5%	50	V	CER X	999151/103P
C55	CHIP 1	N	5%	50	V	CER C	999154/102P
C56	CHIP 220	N	5%	50	V	CER X	999150/224P
C57	CHIP 10	N	5%	50	V	CER X	999151/103P
C58	CHIP 1	N	5%	50	V	CER C	999154/102P
C59	CHIP 100	N	10%	50	V	CER X	948163
C60	CHIP 15	P	5%	50	V	CER C	999154/150P
C61	CHIP 1	N	5%	50	V	CER C	999154/102P
C62	CHIP 10	N	5%	50	V	CER X	999151/103P
C63	CHIP 47	N	5%	50	V	CER X	999151/473P
C64	CHIP 10	N	5%	50	V	CER X	999151/103P
C65	CHIP 10	N	5%	50	V	CER X	999151/103P

REF	DESCRIPTION								PART No.
C66	CHIP	120	P	5%	50	V	CER	C	999154/121P
C67	CHIP	10	N	5%	50	V	CER	X	999151/103P
C68	CHIP	10	N	5%	50	V	CER	X	999151/103P
C69	CHIP	1	U	20%	35	V	TAN		945049
C70	CHIP	10	N	5%	50	V	CER	X	999151/103P
C71	CHIP	1	N	5%	50	V	CER	C	999154/102P
C72	CHIP	1	N	5%	50	V	CER	C	999154/102P
C73	CHIP	100	N	10%	50	V	CER	X	948163
C74	CHIP	1	N	5%	50	V	CER	C	999154/102P
C75	CHIP	10	N	5%	50	V	CER	X	999151/103P
C76	CHIP	10	U	20%	25	V	TAN		Y00643
C77	CHIP	100	N	10%	50	V	CER	X	948163
C78	CHIP	82	P	5%	50	V	CER	C	999154/820P
C79	CHIP	10	N	5%	50	V	CER	X	999151/103P
C80	CHIP	1	N	5%	50	V	CER	C	999154/102P
C81	CHIP	10	N	5%	50	V	CER	X	999151/103P
C82	CHIP	1	U	20%	35	V	TAN		945049
C83	CHIP	10	N	5%	50	V	CER	X	999151/103P
C84	CHIP	10	N	5%	50	V	CER	X	999151/103P
C85	CHIP	10	N	5%	50	V	CER	X	999151/103P
C86	CHIP	33	P	5%	50	V	CER	C	999154/330P
C87	CHIP	100	P	5%	50	V	CER	C	999154/101P
C88	CHIP	10	N	5%	50	V	CER	X	999151/103P
C89	CHIP	10	N	5%	50	V	CER	X	999151/103P
C90	CHIP	10	N	5%	50	V	CER	X	999151/103P
C91	CHIP	10	P	5%	50	V	CER	C	999154/100P
C92	CHIP	1	N	5%	50	V	CER	C	999154/102P
C93	CHIP	10	N	5%	50	V	CER	X	999151/103P
C94	CHIP	100	P	5%	50	V	CER	C	999154/101P
C95	CHIP	1	N	5%	50	V	CER	C	999154/102P
C96	CHIP	1	N	5%	50	V	CER	C	999154/102P
C97	CHIP	1	N	5%	50	V	CER	C	999154/102P
C98	CHIP	33	P	5%	50	V	CER	C	999154/330P
C99	CHIP	56	P	5%	50	V	CER	C	999154/560P
C100	CHIP	10	N	5%	50	V	CER	X	999151/103P

REF	DESCRIPTION							PART No.
C101	CHIP 1	N	5%	50	V	CER	C	999154/102P
C102	CHIP 10	N	5%	50	V	CER	X	999151/103P
C103	CHIP 10	N	5%	50	V	CER	X	999151/103P
C104	CHIP 100	N	10%	50	V	CER	X	948163
C105	CHIP 10	N	5%	50	V	CER	X	999151/103P
C106	CHIP 10	N	5%	50	V	CER	X	999151/103P
C107	CHIP 10	N	5%	50	V	CER	X	999151/103P
C108	CHIP 10	N	5%	50	V	CER	X	999151/103P
C109	CHIP 1	U	20%	35	V	TAN		945049
C110	CHIP 100	N	10%	50	V	CER	X	948163
C111	CHIP 10	N	5%	50	V	CER	X	999151/103P
C112	CHIP 10	U	20%	25	V	TAN		Y00643
C113	CHIP 100	N	10%	50	V	CER	X	948163
C114	CHIP 100	N	10%	50	V	CER	X	948163
C115	CHIP 10	N	5%	50	V	CER	X	999151/103P
C116	CHIP 10	N	5%	50	V	CER	X	999151/103P
C117	CHIP 10	N	5%	50	V	CER	X	999151/103P
C118	CHIP 1	N	5%	50	V	CER	C	999154/102P
C119	CHIP 1	N	5%	50	V	CER	C	999154/102P
C120	CHIP 10	N	5%	50	V	CER	X	999151/103P
C121	CHIP 1	N	5%	50	V	CER	C	999154/102P
C122	CHIP 10	N	5%	50	V	CER	X	999151/103P
C123	CHIP 10	U	20%	25	V	TAN		Y00643
C124	CHIP 10	N	5%	50	V	CER	X	999151/103P
C125	CHIP 1	N	5%	50	V	CER	C	999154/102P
C126	CHIP 1	N	5%	50	V	CER	C	999154/102P
C127	CHIP 1	N	5%	50	V	CER	C	999154/102P
C128	CHIP 1	N	5%	50	V	CER	C	999154/102P
C129	CHIP 1	N	5%	50	V	CER	C	999154/102P
C130	CHIP 1	N	5%	50	V	CER	C	999154/102P
C131	CHIP 1	U	20%	35	V	TAN		945049
C132	CHIP 1	N	5%	50	V	CER	C	999154/102P
C133	CHIP 1	N	5%	50	V	CER	C	999154/102P
C134	CHIP 1	N	5%	50	V	CER	C	999154/102P
C135	CHIP 1	N	5%	50	V	CER	C	999154/102P

REF	DESCRIPTION							PART No.
C136	CHIP 10	U	20%	25	V	TAN		Y00643
C137	CHIP 10	N	5%	50	V	CER	X	999151/103P
C138	CHIP 1	N	5%	50	V	CER	C	999154/102P
C139	CHIP 10	N	5%	50	V	CER	X	999151/103P
C140	CHIP 10	N	5%	50	V	CER	X	999151/103P
C141	CHIP 10	P	5%	50	V	CER	C	999154/100P
C142	CHIP 10	N	5%	50	V	CER	X	999151/103P
C143	CHIP 10	N	5%	50	V	CER	X	999151/103P
C144	CHIP 100	P	5%	50	V	CER	C	999154/101P
C145	CHIP 1	N	5%	50	V	CER	C	999154/102P
C146	CHIP 47	U	10%	10	V	TAN		999043/476P
C147	CHIP 10	N	5%	50	V	CER	X	999151/103P
C148	CHIP 10	N	5%	50	V	CER	X	999151/103P
C149	CHIP 10	N	5%	50	V	CER	X	999151/103P
C150	CHIP 10	N	5%	50	V	CER	X	999151/103P
C151	CHIP 10	N	5%	50	V	CER	X	999151/103P
C152	CHIP 100	N	10%	50	V	CER	X	948163
C153	CHIP 47	N	5%	50	V	CER	X	999151/473P
C154	CHIP 1.5	N	5%	50	V	CER	X	999151/152P
C155	CHIP 10	N	5%	50	V	CER	X	999151/103P
C156	CHIP 1	N	5%	50	V	CER	C	999154/102P
C157	CHIP 10	N	5%	50	V	CER	X	999151/103P
C158	CHIP 10	N	5%	50	V	CER	X	999151/103P
C159	CHIP 10	U	20%	25	V	TAN		Y00643
C160	CHIP 10	N	5%	50	V	CER	X	999151/103P
C161	CHIP 10	N	5%	50	V	CER	X	999151/103P
C162	CHIP 1	U	20%	35	V	TAN		945049
C163	CHIP 10	N	5%	50	V	CER	X	999151/103P
C164	CHIP 82	P	5%	50	V	CER	C	999154/820P
C165	CHIP 1	U	20%	35	V	TAN		945049
C166	CHIP 1	N	5%	50	V	CER	C	999154/102P
C167	CHIP 10	N	5%	50	V	CER	X	999151/103P
C168	CHIP 10	N	5%	50	V	CER	X	999151/103P
C169	CHIP 6.8	P	5%	50	V	CER	C	999154/689P
C170	CHIP 1	U	20%	35	V	TAN		945049

REF	DESCRIPTION								PART No.
C171	CHIP	150	P	5%	50	V	CER	C	999154/151P
C172	CHIP	1	N	5%	50	V	CER	C	999154/102P
C173	CHIP	10	N	5%	50	V	CER	X	999151/103P
C174	CHIP	1	N	5%	50	V	CER	C	999154/102P
C175	CHIP	10	N	5%	50	V	CER	X	999151/103P
C176	CHIP	10	N	5%	50	V	CER	X	999151/103P
C177	CHIP	1	U	20%	35	V	TAN		945049
C178	CHIP	10	N	5%	50	V	CER	X	999151/103P
C179	CHIP	10	N	5%	50	V	CER	X	999151/103P
C180	CHIP	10	U	20%	25	V	TAN		Y00643
C181	CHIP	120	P	5%	50	V	CER	C	999154/121P
C182	CHIP	39	P	5%	50	V	CER	C	999154/390P
C183	CHIP	1	N	5%	50	V	CER	C	999154/102P
C184	CHIP	1	N	5%	50	V	CER	C	999154/102P
C185	CHIP	1	U	20%	35	V	TAN		945049
C186	CHIP	10	N	5%	50	V	CER	X	999151/103P
C187	CHIP	1	U	20%	35	V	TAN		945049
C188	CHIP	1	N	5%	50	V	CER	C	999154/102P
C189	CHIP	1	N	5%	50	V	CER	C	999154/102P
C190	CHIP	1	N	5%	50	V	CER	C	999154/102P
C191	CHIP	1	N	5%	50	V	CER	C	999154/102P
C192	CHIP	10	N	5%	50	V	CER	X	999151/103P
C193	CHIP	10	N	5%	50	V	CER	X	999151/103P
C194	CHIP	56	P	5%	50	V	CER	C	999154/560P
C195	CHIP	1	N	5%	50	V	CER	C	999154/102P
C196	CHIP	120	P	5%	50	V	CER	C	999154/121P
C197	CHIP	1	U	20%	35	V	TAN		945049
C198	CHIP	10	N	5%	50	V	CER	X	999151/103P
C199	CHIP	10	U	20%	25	V	TAN		Y00643
C200	CHIP	10	N	5%	50	V	CER	X	999151/103P
C201	CHIP	1	N	5%	50	V	CER	C	999154/102P
C202	CHIP	1	N	5%	50	V	CER	C	999154/102P
C203	CHIP	10	N	5%	50	V	CER	X	999151/103P
C204	CHIP	10	N	5%	50	V	CER	X	999151/103P
C205	CHIP	10	N	5%	50	V	CER	X	999151/103P

REF	DESCRIPTION							PART No.
C206	CHIP 10	N	5%	50	V	CER	X	999151/103P
C207	CHIP 10	N	5%	50	V	CER	X	999151/103P
C208	CHIP 10	N	5%	50	V	CER	X	999151/103P
C209	CHIP 1	U	20%	35	V	TAN		945049
C210	CHIP 10	N	5%	50	V	CER	X	999151/103P
C211	CHIP 100	N	10%	50	V	CER	X	948163
C212	CHIP 1	N	5%	50	V	CER	C	999154/102P
C213	CHIP 1	N	5%	50	V	CER	C	999154/102P
C214	CHIP 1	N	5%	50	V	CER	C	999154/102P
C215	CHIP 10	N	5%	50	V	CER	X	999151/103P
C216	CHIP 10	N	5%	50	V	CER	X	999151/103P
C217	CHIP 1	N	5%	50	V	CER	C	999154/102P
C218	CHIP 27	P	5%	50	V	CER	C	999154/270P
C219	CHIP 10	N	5%	50	V	CER	X	999151/103P
C220	CHIP 1	U	20%	35	V	TAN		945049
C221	CHIP 10	N	5%	50	V	CER	X	999151/103P
C222	CHIP 10	N	5%	50	V	CER	X	999151/103P
C223	CHIP 1	N	5%	50	V	CER	C	999154/102P
C224	CHIP 1	N	5%	50	V	CER	C	999154/102P
C225	CHIP 10	N	5%	50	V	CER	X	999151/103P
C226	CHIP 1	N	5%	50	V	CER	C	999154/102P
C227	CHIP 68	P	5%	50	V	CER	C	999154/680P
C228	CHIP 10	N	5%	50	V	CER	X	999151/103P
C229	CHIP 1	N	5%	50	V	CER	C	999154/102P
C230	CHIP 1	U	20%	35	V	TAN		945049
C231	CHIP 10	N	5%	50	V	CER	X	999151/103P
C232	CHIP 1	N	5%	50	V	CER	C	999154/102P
C233	CHIP 10	U	20%	25	V	TAN		Y00643
C234	CHIP 100	P	5%	50	V	CER	C	999154/101P
C235	CHIP 10	N	5%	50	V	CER	X	999151/103P
C236	CHIP 10	N	5%	50	V	CER	X	999151/103P
C237	CHIP 100	N	10%	50	V	CER	X	948163
C238	CHIP 10	N	5%	50	V	CER	X	999151/103P
C239	CHIP 1	N	5%	50	V	CER	C	999154/102P
C240	CHIP 100	N	10%	50	V	CER	X	948163

REF	DESCRIPTION							PART No.
C241	CHIP 10	U	20%	25	V	TAN		Y00643
C242	CHIP 10	P	5%	50	V	CER	C	999154/100P
C243	CHIP 47	P	2%	500	V	MIC		945135
C244	CHIP 27	P	2%	500	V	MIC		945134
C245	CHIP 12	P	2%	500	V	MIC		945133
C246	CHIP 1	N	5%	50	V	CER	C	999154/102P
C247	CHIP 1	N	5%	50	V	CER	C	999154/102P
C248	CHIP 1	N	5%	50	V	CER	C	999154/102P
C249	CHIP 68	N	10%	50	V	CER	X	28758-035-00
C250	CHIP 1	N	5%	50	V	CER	C	999154/102P
C251	CHIP 100	P	5%	50	V	CER	C	999154/101P
C252	CHIP 1	N	5%	50	V	CER	C	999154/102P
C253	CHIP 10	N	5%	50	V	CER	X	999151/103P
C254	CHIP 10	N	5%	50	V	CER	X	999151/103P
C255	CHIP 1	N	5%	50	V	CER	C	999154/102P
C256	CHIP 1	N	5%	50	V	CER	C	999154/102P
C257	CHIP 1	N	5%	50	V	CER	C	999154/102P
C258	CHIP 1	N	5%	50	V	CER	C	999154/102P
C259	CHIP 1	U	20%	35	V	TAN		945049
C260	CHIP 1	N	5%	50	V	CER	C	999154/102P
C261	CHIP 10	N	5%	50	V	CER	X	999151/103P
C262	CHIP 1	N	5%	50	V	CER	C	999154/102P
C263	CHIP 1	N	5%	50	V	CER	C	999154/102P
C264	CHIP 1	U	20%	35	V	TAN		945049
C265	CHIP 10	N	5%	50	V	CER	X	999151/103P
C266	CHIP 1	N	5%	50	V	CER	C	999154/102P
C267	CHIP 1	N	5%	50	V	CER	C	999154/102P
C268	CHIP 1	U	20%	35	V	TAN		945049
C269	CHIP 68	P	5%	50	V	CER	C	999154/680P
C270	CHIP 68	P	5%	50	V	CER	C	999154/680P
C271	CHIP 1	N	5%	50	V	CER	C	999154/102P
C272	CHIP 10	N	5%	50	V	CER	X	999151/103P
C273	CHIP 1	U	20%	35	V	TAN		945049
C274	CHIP 1	U	20%	35	V	TAN		945049
C275	CHIP 1	U	20%	35	V	TAN		945049

REF	DESCRIPTION							PART No.
C276	CHIP 10	N	5%	50	V	CER	X	999151/103P
C277	CHIP 1	U	20%	35	V	TAN		945049
C278	CHIP 2.2	N	5%	50	V	CER	X	999151/222P
C279	CHIP 10	N	5%	50	V	CER	X	999151/103P
C280	CHIP 1	N	5%	50	V	CER	C	999154/102P
C281	CHIP 2.2	N	5%	50	V	CER	X	999151/222P
C282	CHIP 1	N	5%	50	V	CER	C	999154/102P
C283	CHIP 2.2	N	5%	50	V	CER	X	999151/222P
C284	CHIP 39	P	5%	50	V	CER	C	999154/390P
C285	CHIP 10	N	5%	50	V	CER	X	999151/103P
C286	CHIP 10	N	5%	50	V	CER	X	999151/103P
C287	CHIP 2.2	N	5%	50	V	CER	X	999151/222P
C288	CHIP 27	P	5%	50	V	CER	C	999154/270P
C289	CHIP 27	P	5%	50	V	CER	C	999154/270P
C290	CHIP 2.2	P	5%	50	V	CER	C	999154/229P
C291	CHIP 68	P	5%	50	V	CER	C	999154/680P
C292	CHIP 56	P	5%	50	V	CER	C	999154/560P
C293	CHIP 10	N	5%	50	V	CER	X	999151/103P
C294	CHIP 1	N	5%	50	V	CER	C	999154/102P
C295	CHIP 1	N	5%	50	V	CER	C	999154/102P
C296	CHIP 220	P	5%	50	V	CER	C	999154/221P
C297	CHIP 2.2	N	5%	50	V	CER	X	999151/222P
C298	CHIP 56	P	5%	50	V	CER	C	999154/560P
C299	CHIP 10	N	5%	50	V	CER	X	999151/103P
C300	CHIP 1	U	20%	35	V	TAN		945049
C301	CHIP 10	N	5%	50	V	CER	X	999151/103P
C302	CHIP 1	U	20%	35	V	TAN		945049
C303	CHIP 1	U	20%	35	V	TAN		945049
C304	CHIP 2.2	N	5%	50	V	CER	X	999151/222P
C305	CHIP 220	P	5%	50	V	CER	C	999154/221P
C306	CHIP 1	U	20%	35	V	TAN		945049
C307	CHIP 1	U	20%	35	V	TAN		945049
C308	CHIP 10	N	5%	50	V	CER	X	999151/103P
C309	CHIP 1	N	5%	50	V	CER	C	999154/102P
C310	CHIP 1	N	5%	50	V	CER	C	999154/102P

REF	DESCRIPTION							PART No.
C311	CHIP 1	U	20%	35	V	TAN		945049
C312	CHIP 1	U	20%	35	V	TAN		945049
C313	CHIP 10	N	5%	50	V	CER	X	999151/103P
C314	CHIP 10	N	5%	50	V	CER	X	999151/103P
C315	CHIP 1	N	5%	50	V	CER	C	999154/102P
C316	CHIP 10	N	5%	50	V	CER	X	999151/103P
C317	CHIP 10	N	5%	50	V	CER	X	999151/103P
C318	CHIP 10	N	5%	50	V	CER	X	999151/103P
C319	CHIP 10	N	5%	50	V	CER	X	999151/103P
C320	CHIP 10	N	5%	50	V	CER	X	999151/103P
C321	CHIP 10	N	5%	50	V	CER	X	999151/103P
C322	CHIP 1	N	5%	50	V	CER	C	999154/102P
C323	CHIP 10	N	5%	50	V	CER	X	999151/103P
C324	CHIP 100	P	5%	50	V	CER	C	999154/101P
C325	CHIP 1	U	20%	35	V	TAN		945049
C326	CHIP 22	P	5%	50	V	CER	C	999154/220P
C327	CHIP 1	U	20%	35	V	TAN		945049
C328	CHIP 1	U	20%	35	V	TAN		945049
C329	CHIP 1	U	20%	35	V	TAN		945049
C330	CHIP 2.2	N	5%	50	V	CER	X	999151/222P
C331	CHIP 1	U	20%	35	V	TAN		945049
C332	CHIP 2.2	N	5%	50	V	CER	X	999151/222P
C333	CHIP 1	N	5%	50	V	CER	C	999154/102P
C334	CHIP 10	N	5%	50	V	CER	X	999151/103P
C335	CHIP 10	N	5%	50	V	CER	X	999151/103P
C336	CHIP 10	N	5%	50	V	CER	X	999151/103P
C337	CHIP 1	N	5%	50	V	CER	C	999154/102P
C338	CHIP 68	P	5%	50	V	CER	C	999154/680P
C339	CHIP 120	P	5%	50	V	CER	C	999154/121P
C340	CHIP 56	P	5%	50	V	CER	C	999154/560P
C341	CHIP 220	P	5%	50	V	CER	C	999154/221P
C342	CHIP 10	N	5%	50	V	CER	X	999151/103P
C343	CHIP 6.8	P	5%	50	V	CER	C	999154/689P
C344	CHIP 150	P	5%	50	V	CER	C	999154/151P
C345	CHIP 1	N	5%	50	V	CER	C	999154/102P

REF	DESCRIPTION								PART No.
C346	CHIP	10	N	5%	50	V	CER	X	999151/103P
C347	CHIP	1	N	5%	50	V	CER	C	999154/102P
C348	CHIP	10	N	5%	50	V	CER	X	999151/103P
C349	CHIP	10	N	5%	50	V	CER	X	999151/103P
C350	CHIP	2.2	P	5%	50	V	CER	C	999154/229P
C351	CHIP	56	P	5%	50	V	CER	C	999154/560P
C352	CHIP	10	N	5%	50	V	CER	X	999151/103P
C353	CHIP	100	P	5%	50	V	CER	C	999154/101P
C354	CHIP	10	P	5%	50	V	CER	C	999154/100P
C355	CHIP	39	P	5%	50	V	CER	C	999154/390P
C356	CHIP	1	N	5%	50	V	CER	C	999154/102P
C357	CHIP	10	N	5%	50	V	CER	X	999151/103P
C358	CHIP	220	P	5%	50	V	CER	C	999154/221P
C359	CHIP	10	N	5%	50	V	CER	X	999151/103P
C360	CHIP	10	N	5%	50	V	CER	X	999151/103P
C361	CHIP	10	N	5%	50	V	CER	X	999151/103P
C362	CHIP	1	U	20%	35	V	TAN		945049
C363	CHIP	1	U	20%	35	V	TAN		945049
C364	CHIP	10	N	5%	50	V	CER	X	999151/103P
C365	CHIP	10	N	5%	50	V	CER	X	999151/103P
C366	CHIP	1	N	5%	50	V	CER	C	999154/102P
C367	CAP	1	U	10%	100	V	PYC	P---	931133
C368	CAP	1	U	10%	50	V	CER	P-M-	945010
C369	CAP	220	U	T%	25	V	ALU	TAC-	921536/EQ
C370	CAP	220	U	T%	25	V	ALU	TAC-	921536/EQ
C371	CAP	220	U	T%	25	V	ALU	TAC-	921536/EQ
C372	CAP	1	U	10%	50	V	CER	P-M-	945010
C373	CAP	2.2	U	10%	100	V	PYC	P---	931134
C374	CAP	220	U	T%	25	V	ALU	TAC-	921536/EQ
C375	CAP	220	U	T%	25	V	ALU	TAC-	921536/EQ
C376	CHIP	10	U	20%	25	V	TAN		Y00643
C377	CHIP	1	N	5%	50	V	CER	C	999154/102P
C378	CHIP	1	N	5%	50	V	CER	C	999154/102P
C379	CHIP	2.2	N	5%	50	V	CER	X	999151/222P
C380	CHIP	100	P	5%	50	V	CER	C	999154/101P
C381	CHIP	2.2	N	5%	50	V	CER	X	999151/222P

REF	DESCRIPTION				PART No.
DIODES					
D1	SWITCHG	BAS16	75V		999206/MC
D2	SWITCHG	BAS16	75V		999206/MC
D3	PIN (A2)	BAT18	35V		999227/MC
D4	PIN (A2)	BAT18	35V		999227/MC
D5	SCHOTTKY	BAT17			943953
D6	CHIP (J7B)	ZC836B			946482
D7	SWITCHG	BAS16	75V		999206/MC
D8	SWITCHG	BAS16	75V		999206/MC
D9	SWITCHG	BAS16	75V		999206/MC
D10	SWITCHG	BAS16	75V		999206/MC
D11	SWITCHG	BAS16	75V		999206/MC
D12	SWITCHG	BAS16	75V		999206/MC
D13	SWITCHG	BAS16	75V		999206/MC
D14	SWITCHG	BAS16	75V		999206/MC
D15	SCHOTTKY	BAT17			943953
D16	SCHOTTKY	BAT17			943953
D17	SCHOTTKY	BAT17			943953
D18	SWITCHG	BAS16	75V		999206/MC
D19	SCHOTTKY	BAT17			943953
D20	SCHOTTKY	BAT17			943953
D21	PIN (A2)	BAT18	35V		999227/MC
D22	PIN (A2)	BAT18	35V		999227/MC
D23	PIN (A2)	BAT18	35V		999227/MC
D24	SWITCHG	BAS16	75V		999206/MC
D25	SWITCHG	BAS16	75V		999206/MC
D26	SWITCHG	BAS16	75V		999206/MC
D27	SWITCHG	BAS16	75V		999206/MC
D28	SWITCHG	BAS16	75V		999206/MC
D29	SCHOTTKY	BAT17			943953
D30	SCHOTTKY	BAT17			943953
D31	RECTIFIER	1N4002	100V		911460/EQ
D32	RECTIFIER	1N4002	100V		911460/EQ
D33	REF	1N6273A			945181
D34	SWITCHING	1N4149/BAW62		75V	914898/EQ
D35	SWITCHING	1N4149/BAW62		75V	914898/EQ

REF	DESCRIPTION			PART No.
D36	TUNING	ZC714	30V	920267/EQ
D37	TUNING	ZC714	30V	920267/EQ
D38	PIN	1N5767	250M	928377/SD
D39	PIN	1N5767	250M	928377/SD
FILTERS				
FL1	BANDPASS 40.032MHZ			90683-01
FL2	BANDPASS 40.032MHZ			90683-01
FUSES				
FS1	FUSELINK 1	AMP		Y00734
INTEGRATED CIRCUITS				
IC1	74HC00	CMS Q 2IP NAN GATE		999296/SD
IC2	74HC00	CMS Q 2IP NAN GATE		999296/SD
IC3	74HC00	CMS Q 2IP NAN GATE		999296/SD
IC4	74AC74	CMS D DTP FLP FLOP		945544
IC5	74HC74T	CMS D DTP FLP FLOP		999353/SD
IC6	3140 MS	OP AMP		946094
IC7	74HC74T	CMS D DTP FLP FLOP		999353/SD
IC8	74HC4053	CMS S 2CH ANA MUX		999322/SD
IC9	74HC03	CMS Q 2IP NAN GATE		945501
IC10	74HC85	CMS S 4B MAG COMP		943978/SD
IC11	339	LIN Q IND VOL COMP		945023/SD
IC12	02	S VOL REF PLUS		999644/SD
IC13	74HC174	HEX FLP FLOP		999693/SD
IC14	74HC4051	CMS S 8CH ANA MUX		999323/SD
IC15	74HC138	CMS 3/8 LNE DCDR		943980/SD
IC16	324	LIN Q L/P OPL AMP		945026
IC17	339	LIN Q IND VOL COMP		945023/SD
IC18	74HC365	H 3S BUF NINV		999691/SD
IC19	74HC174	HEX FLP FLOP		999693/SD
IC20	74HC174	HEX FLP FLOP		999693/SD

REF	DESCRIPTION				PART No.
IC21	211	CMS Q ANA SW SPST			945024
IC22	3140 MS	OP AMP			946094
IC23	RMI375	SURFACE MT (QPG 64-PIN)			946763
IC24	211	CMS Q ANA SW SPST			945024
IC25	3140 MS	OP AMP			946094
IC26	74HC00	CMS Q 2IP NAN GATE			999296/SD
IC27	339	LIN Q IND VOL COMP			945023/SD
IC28	74LS169	TTL S BIN U/D CNTR			945014
IC29	74LS169	TTL S BIN U/D CNTR			945014
IC30	74HC74T	CMS D DTP FLP FLOP			999353/SD
IC31	74HC74T	CMS D DTP FLP FLOP			999353/SD
IC32	324	LIN Q L/P OPL AMP			945026
IC33	74LS27	TTL T 3IP NOR GATE			945013
IC34	5534	OP AMP LOW NOISE			999704/001
IC35	5534	OP AMP LOW NOISE			999704/001
IC36	5534	OP AMP LOW NOISE			999704/001
IC37	324	LIN Q L/P OPL AMP			945026
IC38	12009	ECL D 5-6 PRES			945016/SD
IC39	10115	ECL Q LIN RCVR			935262/SD
IC40	3046	LIN TRN ARAY			945025
INDUCTORS					
L1	CHOKE	22	UH	10%	945033
L2	CHOKE	22	UH	10%	945033
L3	CHOKE	22	UH	10%	945033
L4	CHOKE	22	UH	10%	945033
L5	CHOKE	1.2	UH	5%	999103/122L
L6	CHOKE	22	UH	10%	945033
L7	CHOKE	22	UH	10%	945033
L8	CHOKE	22	UH	10%	945033
L9	CHOKE	1.2	UH	5%	999103/122L
L10	CHOKE	22	UH	10%	945033
L11	CHOKE	100	UH	10%	945037
L12	CHOKE	22	UH	10%	945033
L13	CHOKE	22	UH	10%	945033
L14	CHOKE	22	UH	10%	945033
L15	CHOKE	22	UH	10%	945033

REF	DESCRIPTION					PART No.
L16	CHOKE	1.2	UH	5%		999103/122L
L17	CHOKE	22	UH	10%		945033
L18	CHOKE	22	UH	10%		945033
L19	CHOKE	22	UH	10%		945033
L20	CHOKE	22	UH	10%		945033
L21	CHOKE	22	UH	10%		945033
L22	CHOKE	22	UH	10%		945033
L23	CHOKE	22	UH	10%		945033
L24	CHOKE	22	UH	10%		945033
L25	CHOKE	22	UH	10%		945033
L26	CHOKE	100	UH	10%		945037
L27	CHOKE	22	UH	10%		945033
L28	CHOKE	22	UH	10%		945033
L29	CHOKE	22	UH	10%		945033
L30	CHOKE	22	UH	10%		945033
L31	CHOKE	22	UH	10%		945033
L32	CHOKE	22	UH	10%		945033
L33	CHOKE	22	UH	10%		945033
L34	CHOKE	22	UH	10%		945033
L35	CHOKE	22	UH	10%		945033
L36	CHOKE	22	UH	10%		945033
L37	CHOKE	22	UH	10%		945033
L38	CHOKE	22	UH	10%		945033
L39	CHOKE	22	UH	10%		945033
L40	CHOKE	22	UH	10%		945033
L41	CHOKE	22	UH	10%		945033
L42	CHOKE	22	UH	10%		945033
L43	CHOKE	22	UH	10%		945033
L44	CHOKE	22	UH	10%		945033
L45	CHOKE	22	UH	10%		945033
L46	CHOKE	22	UH	10%		945033
L47	CHOKE	22	UH	10%		945033
L48	CHOKE	330	UH	10%		945038
L49	CHOKE	22	UH	10%		945033
L50	CHOKE	4.7	UH	5%	SMD	999103/472L

REF	DESCRIPTION					PART No.
L51	CHOKE	100	UH	10%		945037
L52	CHOKE	4.7	UH	5%	SMD	999103/472L
L53	CHOKE	4.7	UH	5%	SMD	999103/472L
L54	CHOKE	4.7	UH	5%	SMD	999103/472L
L55	CHOKE	22	UH	10%		945033
L56	CHOKE	22	UH	10%		945033
L57	CHOKE	100	UH	10%		945037
L58	CHOKE	10	UH	5%		999103/103L
L59	CHOKE	22	UH	10%		945033
L60	CHOKE	22	UH	10%		945033
L61	CHOKE	22	UH	10%		945033
L62	CHOKE	22	UH	10%		945033
L63	CHOKE	22	UH	10%		945033
L64	CHOKE	22	UH	10%		945033
L65	CHOKE	470	NH	10%		999105/471L
L66	CHOKE	150	NH	5%		999104/151L
L67	CHOKE	22	UH	10%		945033
L68	CHOKE	22	UH	10%		945033
L69	CHOKE	4.7	UH	5%	SMD	999103/472L
L70	CHOKE	150	NH	5%		999104/151L
L71	CHOKE	22	UH	10%		945033
L72	CHOKE	4.7	UH	5%	SMD	999103/472L
L73	CHOKE	1.2	UH	5%		999103/122L
L74	CHOKE	330	NH	10%		999105/331L
L75	CHOKE	330	UH	10%		945038
L76	CHOKE	330	UH	10%		945038
L77	CHOKE	22	UH	10%		945033
L78	CHOKE	10	UH	5%		999103/103L
L79	CHOKE	10	UH	5%		999103/103L
L80	CHOKE	22	UH	10%		945033
L81	CHOKE	22	UH	10%		945033
L82	CHOKE	22	UH	10%		945033
L83	CHOKE	470	NH	10%		999105/471L
L84	CHOKE	330	NH	10%		999105/331L
L85	CHOKE	150	NH	5%		999104/151L

REF	DESCRIPTION				PART No.
L86	CHOKE	22	UH	10%	945033
L87	CHOKE	150	NH	5%	999104/151L
L88	CHOKE	150	NH	5%	999104/151L
L89	CHOKE	100	NH	10%	999105/101L
L90	CHOKE	330	NH	10%	999105/331L
L91	CHOKE	1.2	UH	5%	999103/122L
L92	CHOKE,VAR	0.28-0.4		UH	945058
L93	CHOKE,VAR	0.16-0.23		UH	945056
L94	CHOKE,VAR	0.16-0.23		UH	945056
L95	CHOKE,VAR	0.28-0.4		UH	945058
L96	CHOKE,VAR	0.28-0.4		UH	945058
L97	CHOKE,VAR	0.24-0.36		UH	945057
L98	CHOKE,VAR	0.24-0.36		UH	945057
L99	COIL ASSY				87457-01
L100	CHOKE,VAR	0.28-0.4		UH	945058
L101	CHOKE	6.8	UH	5%	999103/682L

LINKS

LK1	4-WAY P FX STR	945062
LK2	4-WAY P FX STR	945062
LK3	4-WAY P FX STR	945062
LK4	4-WAY P FX STR	945062
LK5	4-WAY P FX STR	945062
LK6	4-WAY P FX STR	945062
LK7	4-WAY P FX STR	945062
LK8	4-WAY P FX STR	945062
LK9	4-WAY P FX STR	945062
LK10	4-WAY P FX STR	945062
LK11	4-WAY P FX STR	945062
LK12	4-WAY P FX STR	945062
LK13	4-WAY P FX STR	945062
LK14	4-WAY P FX STR	945062

REF	DESCRIPTION	PART No.
PINS		
P1	PSH LD .02 R S	937625/EQ
P2	PSH LD .02 R S	937625/EQ
P3	PSH LD .02 R S	937625/EQ
P4	PSH LD .02 R S	937625/EQ
P5	PSH LD .02 R S	937625/EQ
P6	PSH LD .02 R S	937625/EQ
P7	PSH LD .02 R S	937625/EQ
P8	PSH LD .02 R S	937625/EQ
P9	PSH LD .02 R S	937625/EQ
P10	PSH LD .02 R S	937625/EQ
PROGRAMMED DEVICES		
PD1	PAL	91125/001-01
PD2	PAL	91125/002-01
PLUGS		
PL1	50-WAY P FX STR	943388
RESISTORS		
R1	CHIP 10 2% 0.063 W MF	999160/100R
R2	CHIP 1 K 2% 0.063 W MF	999160/102R
R3	CHIP 1 K 2% 0.063 W MF	999160/102R
R4	CHIP 1 K 2% 0.063 W MF	999160/102R
R5	CHIP 10 K 2% 0.063 W MF	999160/103R
R6	CHIP 100 2% 0.063 W MF	999160/101R
R7	CHIP 100 2% 0.063 W MF	999160/101R
R8	CHIP 10 K 2% 0.063 W MF	999160/103R
R9	CHIP 1 K 2% 0.063 W MF	999160/102R
R10	CHIP 220 K 2% 0.063 W MF	999160/224R
R11	CHIP 6.8 K 2% 0.063 W MF	999160/682R
R12	CHIP 1 K 2% 0.063 W MF	999160/102R
R13	CHIP 10 K 2% 0.063 W MF	999160/103R
R14	CHIP 22 2% 0.063 W MF	999160/220R
R15	CHIP 820 2% 0.063 W MF	999160/821R

REF	DESCRIPTION					PART No.
R16	CHIP 1	K	2%	0.063 W	MF	999160/102R
R17	CHIP 6.8	K	2%	0.063 W	MF	999160/682R
R18	CHIP 10	K	2%	0.063 W	MF	999160/103R
R19	CHIP 22		2%	0.063 W	MF	999160/220R
R20	CHIP 1	K	2%	0.063 W	MF	999160/102R
R21	CHIP 6.8	K	2%	0.063 W	MF	999160/682R
R22	CHIP 1	K	2%	0.063 W	MF	999160/102R
R23	CHIP 330		2%	0.125 W	MF	999161/331R
R24	CHIP 1	K	2%	0.063 W	MF	999160/102R
R25	CHIP 10	K	2%	0.063 W	MF	999160/103R
R26	CHIP 270		2%	0.063 W	MF	999160/271R
R27	CHIP 10	K	2%	0.063 W	MF	999160/103R
R28	CHIP 820		2%	0.063 W	MF	999160/821R
R29	VAR 50	K	20%	PCB MF	SMD	Y00869
R30	CHIP 470		2%	0.063 W	MF	999160/471R
R31	CHIP 10	K	2%	0.063 W	MF	999160/103R
R32	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R33	CHIP 1	K	2%	0.063 W	MF	999160/102R
R34	CHIP 10		2%	0.063 W	MF	999160/100R
R35	CHIP 1	K	2%	0.063 W	MF	999160/102R
R36	CHIP 220		2%	0.063 W	MF	999160/221R
R37	CHIP 10		2%	0.063 W	MF	999160/100R
R38	CHIP 270		2%	0.063 W	MF	999160/271R
R39	CHIP 470		2%	0.063 W	MF	999160/471R
R40	CHIP 1	K	2%	0.063 W	MF	999160/102R
R41	CHIP 1	K	2%	0.063 W	MF	999160/102R
R42	CHIP 10	K	2%	0.063 W	MF	999160/103R
R43	CHIP 10		2%	0.063 W	MF	999160/100R
R44	CHIP 10	K	2%	0.063 W	MF	999160/103R
R45	CHIP 22		2%	0.063 W	MF	999160/220R
R46	CHIP 1	K	2%	0.063 W	MF	999160/102R
R47	CHIP 1	K	2%	0.063 W	MF	999160/102R
R48	CHIP 10	K	2%	0.063 W	MF	999160/103R
R49	CHIP 22		2%	0.063 W	MF	999160/220R
R50	CHIP 10		2%	0.063 W	MF	999160/100R

REF	DESCRIPTION					PART No.
R51	CHIP 10	K	2%	0.063 W	MF	999160/103R
R52	CHIP 1	K	2%	0.063 W	MF	999160/102R
R53	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R54	CHIP 10		2%	0.063 W	MF	999160/100R
R55	CHIP 10	K	2%	0.063 W	MF	999160/103R
R56	CHIP 220	K	2%	0.063 W	MF	999160/224R
R57	CHIP 22		2%	0.063 W	MF	999160/220R
R58	CHIP 22		2%	0.063 W	MF	999160/220R
R59	CHIP 10		2%	0.063 W	MF	999160/100R
R60	CHIP 220	K	2%	0.063 W	MF	999160/224R
R61	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R62	CHIP 100	K	2%	0.063 W	MF	999160/104R
R63	CHIP 10	K	2%	0.063 W	MF	999160/103R
R64	CHIP 22		2%	0.063 W	MF	999160/220R
R65	CHIP 22		2%	0.063 W	MF	999160/220R
R66	CHIP 22		2%	0.063 W	MF	999160/220R
R67	CHIP 220	K	2%	0.063 W	MF	999160/224R
R68	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R69	CHIP 10	K	2%	0.063 W	MF	999160/103R
R70	CHIP 1.5	K	2%	0.063 W	MF	999160/152R
R71	CHIP 22		2%	0.063 W	MF	999160/220R
R72	CHIP 390		2%	0.062 W	MF	999160/391R
R73	CHIP 1	K	2%	0.063 W	MF	999160/102R
R74	CHIP 1	K	2%	0.063 W	MF	999160/102R
R75	CHIP 10		2%	0.063 W	MF	999160/100R
R76	CHIP 10	K	2%	0.063 W	MF	999160/103R
R77	CHIP 10		2%	0.063 W	MF	999160/100R
R78	CHIP 10		2%	0.063 W	MF	999160/100R
R79	CHIP 10		2%	0.063 W	MF	999160/100R
R80	CHIP 10		2%	0.063 W	MF	999160/100R
R81	CHIP 1	K	2%	0.063 W	MF	999160/102R
R82	CHIP 10		2%	0.063 W	MF	999160/100R
R83	CHIP 390		2%	0.062 W	MF	999160/391R
R84	CHIP 1	K	2%	0.063 W	MF	999160/102R
R85	CHIP 10	K	2%	0.063 W	MF	999160/103R

REF	DESCRIPTION					PART No.
R86	CHIP 1	K	2%	0.063 W	MF	999160/102R
R87	CHIP 100	K	2%	0.063 W	MF	999160/104R
R88	CHIP 10	K	2%	0.063 W	MF	999160/103R
R89	CHIP 47	K	2%	0.063 W	MF	999160/473R
R90	CHIP 3.3	K	2%	0.063 W	MF	999160/332R
R91	CHIP 100		2%	0.063 W	MF	999160/101R
R92	CHIP 6.8	K	2%	0.063 W	MF	999160/682R
R93	CHIP 3.3	K	2%	0.063 W	MF	999160/332R
R94	CHIP 3.9	K	2%	0.063 W	MF	999160/392R
R95	CHIP 22	K	2%	0.063 W	MF	999160/223R
R96	CHIP 10	K	2%	0.063 W	MF	999160/103R
R97	CHIP 10	K	2%	0.063 W	MF	999160/103R
R98	CHIP 820		2%	0.063 W	MF	999160/821R
R99	CHIP 6.8	K	2%	0.063 W	MF	999160/682R
R100	CHIP 100		2%	0.063 W	MF	999160/101R
R101	CHIP 1	K	2%	0.063 W	MF	999160/102R
R102	CHIP 10	K	2%	0.063 W	MF	999160/103R
R103	CHIP 10	K	2%	0.063 W	MF	999160/103R
R104	CHIP 10	K	2%	0.063 W	MF	999160/103R
R105	CHIP 1	K	2%	0.063 W	MF	999160/102R
R106	CHIP 10	K	2%	0.063 W	MF	999160/103R
R107	CHIP 10	K	2%	0.063 W	MF	999160/103R
R108	CHIP 10	K	2%	0.063 W	MF	999160/103R
R109	CHIP 10	K	2%	0.063 W	MF	999160/103R
R110	CHIP 10		2%	0.063 W	MF	999160/100R
R111	CHIP 10		2%	0.063 W	MF	999160/100R
R112	CHIP 10	K	2%	0.063 W	MF	999160/103R
R113	CHIP 33	K	2%	0.063 W	MF	999160/333R
R114	CHIP 47	K	2%	0.063 W	MF	999160/473R
R115	CHIP 1.5	K	2%	0.063 W	MF	999160/152R
R116	CHIP 100	K	2%	0.063 W	MF	999160/104R
R117	CHIP 10	K	2%	0.063 W	MF	999160/103R
R118	CHIP 33	K	2%	0.063 W	MF	999160/333R
R119	CHIP 47	K	2%	0.063 W	MF	999160/473R
R120	CHIP 47	K	2%	0.063 W	MF	999160/473R

REF	DESCRIPTION					PART No.
R121	CHIP 10	K	2%	0.063 W	MF	999160/103R
R122	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R123	CHIP 220	K	2%	0.063 W	MF	999160/224R
R124	CHIP 100	K	2%	0.063 W	MF	999160/104R
R125	CHIP 10		2%	0.063 W	MF	999160/100R
R126	CHIP 33	K	2%	0.063 W	MF	999160/333R
R127	CHIP 10	K	2%	0.063 W	MF	999160/103R
R128	CHIP 47	K	2%	0.063 W	MF	999160/473R
R129	CHIP 47	K	2%	0.063 W	MF	999160/473R
R130	CHIP 47	K	2%	0.063 W	MF	999160/473R
R131	CHIP 47	K	2%	0.063 W	MF	999160/473R
R132	CHIP 47	K	2%	0.063 W	MF	999160/473R
R133	CHIP 47	K	2%	0.063 W	MF	999160/473R
R134	CHIP 47	K	2%	0.063 W	MF	999160/473R
R135	CHIP 47	K	2%	0.063 W	MF	999160/473R
R136	CHIP 47	K	2%	0.063 W	MF	999160/473R
R137	CHIP 47	K	2%	0.063 W	MF	999160/473R
R138	CHIP 47	K	2%	0.063 W	MF	999160/473R
R139	CHIP 47	K	2%	0.063 W	MF	999160/473R
R140	CHIP 47	K	2%	0.063 W	MF	999160/473R
R141	CHIP 10	K	2%	0.063 W	MF	999160/103R
R142	CHIP 330		2%	0.125 W	MF	999161/331R
R143	CHIP 330		2%	0.125 W	MF	999161/331R
R144	CHIP 330		2%	0.125 W	MF	999161/331R
R145	CHIP 47	K	2%	0.063 W	MF	999160/473R
R146	CHIP 330		2%	0.125 W	MF	999161/331R
R147	CHIP 330		2%	0.125 W	MF	999161/331R
R148	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R149	CHIP 330		2%	0.125 W	MF	999161/331R
R150	CHIP 10		2%	0.063 W	MF	999160/100R
R151	CHIP 10	K	2%	0.063 W	MF	999160/103R
R152	CHIP 330		2%	0.125 W	MF	999161/331R
R153	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R154	CHIP 10		2%	0.063 W	MF	999160/100R
R155	CHIP 330		2%	0.125 W	MF	999161/331R

REF	DESCRIPTION					PART No.
R156	CHIP 100	K	2%	0.063 W	MF	999160/104R
R157	CHIP 270		2%	0.063 W	MF	999160/271R
R158	CHIP 47	K	2%	0.063 W	MF	999160/473R
R159	CHIP 100	K	2%	0.063 W	MF	999160/104R
R160	CHIP 10	K	2%	0.063 W	MF	999160/103R
R161	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R162	CHIP 47	K	2%	0.063 W	MF	999160/473R
R163	CHIP 47	K	2%	0.063 W	MF	999160/473R
R164	CHIP 47	K	2%	0.063 W	MF	999160/473R
R165	CHIP 47	K	2%	0.063 W	MF	999160/473R
R166	CHIP 47	K	2%	0.063 W	MF	999160/473R
R167	CHIP 47	K	2%	0.063 W	MF	999160/473R
R168	CHIP 47	K	2%	0.063 W	MF	999160/473R
R169	CHIP 47	K	2%	0.063 W	MF	999160/473R
R170	CHIP 220		2%	0.063 W	MF	999160/221R
R171	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R172	CHIP 10	K	2%	0.063 W	MF	999160/103R
R173	CHIP 47	K	2%	0.063 W	MF	999160/473R
R174	CHIP 27		2%	0.063 W	MF	999160/270R
R175	CHIP 27		2%	0.063 W	MF	999160/270R
R176	CHIP 27		2%	0.063 W	MF	999160/270R
R177	CHIP 390		2%	0.062 W	MF	999160/391R
R178	CHIP 390		2%	0.062 W	MF	999160/391R
R179	CHIP 100		2%	0.063 W	MF	999160/101R
R180	CHIP 3.3	K	2%	0.063 W	MF	999160/332R
R181	CHIP 10	K	2%	0.063 W	MF	999160/103R
R182	CHIP 3.3	K	2%	0.063 W	MF	999160/332R
R183	CHIP 100		2%	0.063 W	MF	999160/101R
R184	CHIP 12	K	2%	0.063 W	MF	999160/123R
R185	CHIP 47	K	2%	0.063 W	MF	999160/473R
R186	CHIP 22	K	2%	0.063 W	MF	999160/223R
R187	CHIP 1	K	2%	0.063 W	MF	999160/102R
R188	CHIP 1	K	2%	0.063 W	MF	999160/102R
R189	CHIP 1	K	2%	0.063 W	MF	999160/102R
R190	CHIP 1	K	2%	0.063 W	MF	999160/102R

REF	DESCRIPTION					PART No.
R191	CHIP 1	K	2%	0.063 W	MF	999160/102R
R192	CHIP 1	K	2%	0.063 W	MF	999160/102R
R193	CHIP 1	K	2%	0.063 W	MF	999160/102R
R194	CHIP 470		2%	0.063 W	MF	999160/471R
R195	CHIP 10	K	2%	0.063 W	MF	999160/103R
R196	CHIP 47	K	2%	0.063 W	MF	999160/473R
R197	CHIP 12	K	2%	0.063 W	MF	999160/123R
R198	CHIP 8.2	K	2%	0.063 W	MF	999160/822R
R199	CHIP 1	K	2%	0.063 W	MF	999160/102R
R200	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R201	CHIP 100		2%	0.063 W	MF	999160/101R
R202	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R203	CHIP 10	K	2%	0.063 W	MF	999160/103R
R204	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R205	CHIP 220	K	2%	0.063 W	MF	999160/224R
R206	CHIP 10		2%	0.063 W	MF	999160/100R
R207	CHIP 1.5	K	2%	0.063 W	MF	999160/152R
R208	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R209	CHIP 470		2%	0.063 W	MF	999160/471R
R210	CHIP 470		2%	0.063 W	MF	999160/471R
R211	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R212	CHIP 22		2%	0.063 W	MF	999160/220R
R213	CHIP 10	K	2%	0.063 W	MF	999160/103R
R214	CHIP 10		2%	0.063 W	MF	999160/100R
R215	CHIP 470		2%	0.063 W	MF	999160/471R
R216	CHIP 470		2%	0.063 W	MF	999160/471R
R217	CHIP 10	K	2%	0.063 W	MF	999160/103R
R218	CHIP 10		2%	0.063 W	MF	999160/100R
R219	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R220	CHIP 10	K	2%	0.063 W	MF	999160/103R
R221	CHIP 220		2%	0.063 W	MF	999160/221R
R222	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R223	CHIP 39	K	2%	0.063 W	MF	999160/393R
R224	CHIP 18	K	2%	0.063 W	MF	999160/183R
R225	CHIP 10		2%	0.063 W	MF	999160/100R

REF	DESCRIPTION					PART No.
R226	CHIP 10	K	2%	0.063 W	MF	999160/103R
R227	CHIP 10	K	2%	0.063 W	MF	999160/103R
R228	CHIP 390		2%	0.062 W	MF	999160/391R
R229	CHIP 100		2%	0.063 W	MF	999160/101R
R230	CHIP 10	K	2%	0.063 W	MF	999160/103R
R231	CHIP 820		2%	0.063 W	MF	999160/821R
R232	CHIP 18	K	2%	0.063 W	MF	999160/183R
R233	CHIP 10		2%	0.063 W	MF	999160/100R
R234	CHIP 10		2%	0.063 W	MF	999160/100R
R235	CHIP 10	K	2%	0.063 W	MF	999160/103R
R236	CHIP 47	K	2%	0.063 W	MF	999160/473R
R237	CHIP 47	K	2%	0.063 W	MF	999160/473R
R238	CHIP 100		2%	0.063 W	MF	999160/101R
R239	CHIP 1	K	2%	0.063 W	MF	999160/102R
R240	CHIP 10		2%	0.063 W	MF	999160/100R
R241	CHIP 10	K	2%	0.063 W	MF	999160/103R
R242	CHIP 10		2%	0.063 W	MF	999160/100R
R243	CHIP 22	K	2%	0.063 W	MF	999160/223R
R244	CHIP 47	K	2%	0.063 W	MF	999160/473R
R245	CHIP 220	K	2%	0.063 W	MF	999160/224R
R246	CHIP 10		2%	0.063 W	MF	999160/100R
R247	CHIP 220	K	2%	0.063 W	MF	999160/224R
R248	CHIP 6.8	K	2%	0.063 W	MF	999160/682R
R249	CHIP 1	K	2%	0.063 W	MF	999160/102R
R250	CHIP 220	K	2%	0.063 W	MF	999160/224R
R251	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R252	CHIP 15	K	2%	0.063 W	MF	999160/153R
R253	CHIP 10		2%	0.063 W	MF	999160/100R
R254	CHIP 820		2%	0.063 W	MF	999160/821R
R255	CHIP 820		2%	0.063 W	MF	999160/821R
R256	CHIP 10		2%	0.063 W	MF	999160/100R
R257	CHIP 1	K	2%	0.063 W	MF	999160/102R
R258	CHIP 10	K	2%	0.063 W	MF	999160/103R
R259	CHIP 10	K	2%	0.063 W	MF	999160/103R
R260	CHIP 1	K	2%	0.063 W	MF	999160/102R

REF	DESCRIPTION					PART No.
R261	CHIP 10		2%	0.063 W	MF	999160/100R
R262	CHIP 1	K	2%	0.063 W	MF	999160/102R
R263	CHIP 15	K	2%	0.063 W	MF	999160/153R
R264	CHIP 22		2%	0.063 W	MF	999160/220R
R265	CHIP 33	K	2%	0.063 W	MF	999160/333R
R266	CHIP 33	K	2%	0.063 W	MF	999160/333R
R267	CHIP 270		2%	0.063 W	MF	999160/271R
R268	CHIP 22		2%	0.063 W	MF	999160/220R
R269	CHIP 220		2%	0.063 W	MF	999160/221R
R270	CHIP 100		2%	0.063 W	MF	999160/101R
R271	CHIP 560		2%	0.063 W	MF	999160/561R
R272	CHIP 1	K	2%	0.063 W	MF	999160/102R
R273	CHIP 10	K	2%	0.063 W	MF	999160/103R
R274	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R275	CHIP 220		2%	0.063 W	MF	999160/221R
R276	CHIP 390		2%	0.062 W	MF	999160/391R
R277	CHIP 22	K	2%	0.063 W	MF	999160/223R
R278	CHIP 22	K	2%	0.063 W	MF	999160/223R
R279	CHIP 10	K	2%	0.063 W	MF	999160/103R
R280	CHIP 22	K	2%	0.063 W	MF	999160/223R
R281	CHIP 10		2%	0.063 W	MF	999160/100R
R282	CHIP 10	K	2%	0.063 W	MF	999160/103R
R283	CHIP 22		2%	0.063 W	MF	999160/220R
R284	CHIP 1	K	2%	0.063 W	MF	999160/102R
R285	CHIP 270		2%	0.063 W	MF	999160/271R
R286	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R287	CHIP 10	K	2%	0.063 W	MF	999160/103R
R288	CHIP 220		2%	0.063 W	MF	999160/221R
R289	CHIP 1.5	K	2%	0.063 W	MF	999160/152R
R290	CHIP 220		2%	0.063 W	MF	999160/221R
R291	CHIP 47	K	2%	0.063 W	MF	999160/473R
R292	CHIP 47	K	2%	0.063 W	MF	999160/473R
R293	CHIP 1	K	2%	0.063 W	MF	999160/102R
R294	CHIP 47	K	2%	0.063 W	MF	999160/473R
R295	CHIP 22		2%	0.063 W	MF	999160/220R

REF	DESCRIPTION					PART No.
R296	CHIP 1	K	2%	0.063 W	MF	999160/102R
R297	CHIP 390		2%	0.062 W	MF	999160/391R
R298	CHIP 10	K	2%	0.063 W	MF	999160/103R
R299	CHIP 10	K	2%	0.063 W	MF	999160/103R
R300	CHIP 1	K	2%	0.063 W	MF	999160/102R
R301	CHIP 1	K	2%	0.063 W	MF	999160/102R
R302	CHIP 820		2%	0.063 W	MF	999160/821R
R303	CHIP 330		2%	0.125 W	MF	999161/331R
R304	CHIP 22		2%	0.063 W	MF	999160/220R
R305	CHIP 10		2%	0.063 W	MF	999160/100R
R306	CHIP 22		2%	0.063 W	MF	999160/220R
R307	CHIP 100		2%	0.063 W	MF	999160/101R
R308	CHIP 22		2%	0.063 W	MF	999160/220R
R309	CHIP 100		2%	0.063 W	MF	999160/101R
R310	CHIP 100		2%	0.063 W	MF	999160/101R
R311	CHIP 10	K	2%	0.063 W	MF	999160/103R
R312	CHIP 10	K	2%	0.063 W	MF	999160/103R
R313	CHIP 470		2%	0.063 W	MF	999160/471R
R314	CHIP 220		2%	0.063 W	MF	999160/221R
R315	CHIP 390		2%	0.062 W	MF	999160/391R
R316	VAR 100		20%	PCB CC	VER	Y00590
R317	VAR 100		20%	PCB CC	VER	Y00590
R318	CHIP 82		2%	0.063 W	MF	999160/820R
R319	CHIP 2.7	K	2%	0.063 W	MF	999160/272R
R320	CHIP 390		2%	0.062 W	MF	999160/391R
R321	CHIP 390		2%	0.062 W	MF	999160/391R
R322	CHIP 10		2%	0.063 W	MF	999160/100R
R323	CHIP 10		2%	0.063 W	MF	999160/100R
R324	CHIP 1	K	2%	0.063 W	MF	999160/102R
R325	CHIP 82		2%	0.063 W	MF	999160/820R
R326	CHIP 10		2%	0.063 W	MF	999160/100R
R327	CHIP 82		2%	0.063 W	MF	999160/820R
R328	CHIP 2.7	K	2%	0.063 W	MF	999160/272R
R329	CHIP 27		2%	0.063 W	MF	999160/270R
R330	CHIP 390		2%	0.062 W	MF	999160/391R

REF	DESCRIPTION					PART No.
R331	CHIP 100	K	2%	0.063 W	MF	999160/104R
R332	CHIP 10		2%	0.063 W	MF	999160/100R
R333	CHIP 1	K	2%	0.063 W	MF	999160/102R
R334	CHIP 10		2%	0.063 W	MF	999160/100R
R335	CHIP 330		2%	0.125 W	MF	999161/331R
R336	CHIP 10		2%	0.063 W	MF	999160/100R
R337	CHIP 51		2%	0.063 W	MF	999160/510R
R338	CHIP 330		2%	0.125 W	MF	999161/331R
R339	CHIP 2.7	K	2%	0.063 W	MF	999160/272R
R340	CHIP 10		2%	0.063 W	MF	999160/100R
R341	CHIP 2.7	K	2%	0.063 W	MF	999160/272R
R342	CHIP 82		2%	0.063 W	MF	999160/820R
R343	CHIP 470		2%	0.063 W	MF	999160/471R
R344	CHIP 470		2%	0.063 W	MF	999160/471R
R345	CHIP 470		2%	0.063 W	MF	999160/471R
R346	CHIP 470		2%	0.063 W	MF	999160/471R
R347	CHIP 10	K	2%	0.063 W	MF	999160/103R
R348	CHIP 10		2%	0.063 W	MF	999160/100R
R349	CHIP 10		2%	0.063 W	MF	999160/100R
R350	CHIP 150		2%	0.063 W	MF	999160/151R
R351	CHIP 10		2%	0.063 W	MF	999160/100R
R352	CHIP 10		2%	0.063 W	MF	999160/100R
R353	CHIP 47	K	2%	0.063 W	MF	999160/473R
R354	CHIP 10		2%	0.063 W	MF	999160/100R
R355	CHIP 47	K	2%	0.063 W	MF	999160/473R
R356	CHIP 22	K	2%	0.063 W	MF	999160/223R
R357	CHIP 22	K	2%	0.063 W	MF	999160/223R
R358	CHIP 82		2%	0.063 W	MF	999160/820R
R359	CHIP 10		2%	0.063 W	MF	999160/100R
R360	CHIP 100		2%	0.063 W	MF	999160/101R
R361	CHIP 47	K	2%	0.063 W	MF	999160/473R
R362	CHIP 47	K	2%	0.063 W	MF	999160/473R
R363	CHIP 27		2%	0.063 W	MF	999160/270R
R364	CHIP 10		2%	0.063 W	MF	999160/100R
R365	CHIP 22		2%	0.063 W	MF	999160/220R

REF	DESCRIPTION					PART No.
R366	CHIP 1	K	2%	0.063 W	MF	999160/102R
R367	CHIP 22		2%	0.063 W	MF	999160/220R
R368	CHIP 1	K	2%	0.063 W	MF	999160/102R
R369	CHIP 18	K	2%	0.063 W	MF	999160/183R
R370	CHIP 820		2%	0.063 W	MF	999160/821R
R371	CHIP 10	K	2%	0.063 W	MF	999160/103R
R372	CHIP 10		2%	0.063 W	MF	999160/100R
R373	CHIP 18	K	2%	0.063 W	MF	999160/183R
R374	CHIP 680		2%	0.063 W	MF	999160/681R
R375	CHIP 330		2%	0.125 W	MF	999161/331R
R376	CHIP 330		2%	0.125 W	MF	999161/331R
R377	CHIP 1	K	2%	0.063 W	MF	999160/102R
R378	CHIP 1	K	2%	0.063 W	MF	999160/102R
R379	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R380	CHIP 560		2%	0.063 W	MF	999160/561R
R381	CHIP 330		2%	0.125 W	MF	999161/331R
R382	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R383	CHIP 10		2%	0.063 W	MF	999160/100R
R384	CHIP 10		2%	0.063 W	MF	999160/100R
R385	CHIP 270		2%	0.063 W	MF	999160/271R
R386	CHIP 270		2%	0.063 W	MF	999160/271R
R387	CHIP 3.3	K	2%	0.063 W	MF	999160/332R
R388	CHIP 220	K	2%	0.063 W	MF	999160/224R
R389	CHIP 51		2%	0.063 W	MF	999160/510R
R390	CHIP 51		2%	0.063 W	MF	999160/510R
R391	CHIP 51		2%	0.063 W	MF	999160/510R
R392	CHIP 1	K	2%	0.063 W	MF	999160/102R
R393	CHIP 10		2%	0.063 W	MF	999160/100R
R394	CHIP 150		2%	0.063 W	MF	999160/151R
R395	CHIP 100	K	2%	0.063 W	MF	999160/104R
R396	CHIP 120		2%	0.063 W	MF	999160/121R
R397	CHIP 10	K	2%	0.063 W	MF	999160/103R
R398	CHIP 100	K	2%	0.063 W	MF	999160/104R
R399	CHIP 33	K	2%	0.063 W	MF	999160/333R
R400	CHIP 100		2%	0.063 W	MF	999160/101R

REF	DESCRIPTION					PART No.
R401	CHIP 2.7	K	2%	0.063 W	MF	999160/272R
R402	CHIP 1	K	2%	0.063 W	MF	999160/102R
R403	CHIP 1	K	2%	0.063 W	MF	999160/102R
R404	CHIP 33	K	2%	0.063 W	MF	999160/333R
R405	CHIP 100	K	2%	0.063 W	MF	999160/104R
R406	CHIP 22	K	2%	0.063 W	MF	999160/223R
R407	CHIP 10		2%	0.063 W	MF	999160/100R
R408	CHIP 100	K	2%	0.063 W	MF	999160/104R
R409	CHIP 10		2%	0.063 W	MF	999160/100R
R410	CHIP 150		2%	0.063 W	MF	999160/151R
R411	CHIP 1	K	2%	0.063 W	MF	999160/102R
R412	CHIP 390		2%	0.062 W	MF	999160/391R
R413	CHIP 51		2%	0.063 W	MF	999160/510R
R414	CHIP 10		2%	0.063 W	MF	999160/100R
R415	CHIP 51		2%	0.063 W	MF	999160/510R
R416	CHIP 10		2%	0.063 W	MF	999160/100R
R417	CHIP 1	K	2%	0.063 W	MF	999160/102R
R418	CHIP 1	K	2%	0.063 W	MF	999160/102R
R419	CHIP 100		2%	0.063 W	MF	999160/101R
R420	CHIP 22	K	2%	0.063 W	MF	999160/223R
R421	CHIP 1	K	2%	0.063 W	MF	999160/102R
R422	CHIP 270		2%	0.063 W	MF	999160/271R
R423	CHIP 15	R	2%	0.063 W	MF	999160/150R
R424	CHIP 390		2%	0.062 W	MF	999160/391R

RELAYS

RL1	12 V 1028 R 1A DPDT REED	A00743
RL2	12 V 1028 R 1A DPDT REED	A00743
RL3	12 V 1028 R 1A DPDT REED	A00743
RL4	12 V 1028 R 1A DPDT REED	A00743
RL5	12 V 1028 R 1A DPDT REED	A00743

SWITCH

S1	SLIDE DIL MX 4 PCB	945028

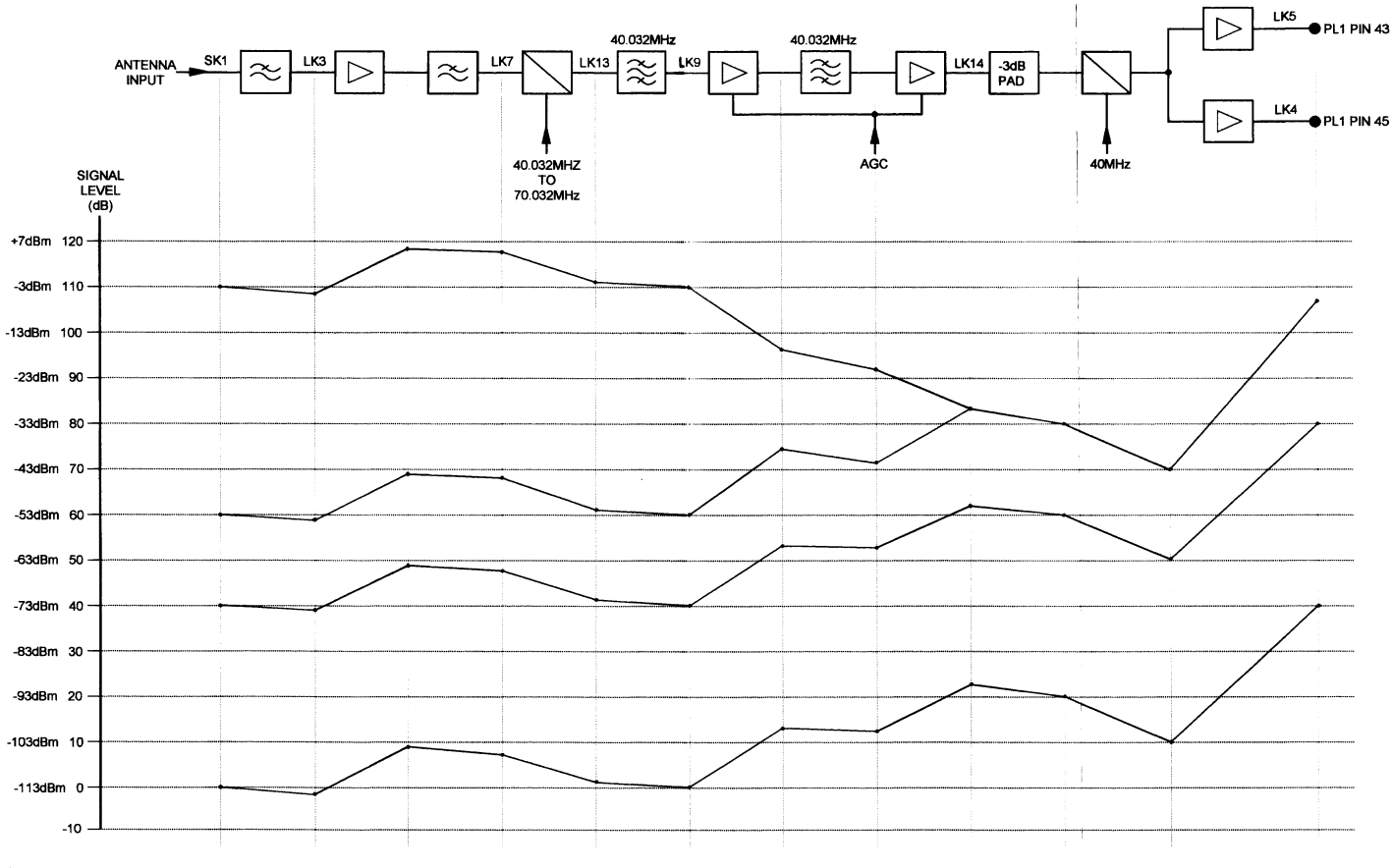
SUPPRESSOR

SA1	SPARK GAP 90V DC	938761

REF	DESCRIPTION		PART No.
SOCKETS			
SK1	50 OHM BNC S FX BAY R/ANG		A00827
SK2	50 OHM BNC S FX BAY R/ANG		A00827
SK3	50 OHM BNC S FX BAY R/ANG		A00827
SK4	50 OHM S FX PSH R/ANG		A00126
SK5	50 OHM S FX PSH R/ANG		A00126
TRANSFORMERS			
T1	ISOLATION 1:1 RF		Y00757
T2			91232-01
T3	ASSY		87456-03
T4	ASSY		87455-02
T5			87454-02
TRANSISTORS			
TR1	N	MMBT2369	943946
TR2	N	MMBT2369	943946
TR3	N	MMBT2369	943946
TR4	N	MMBT2369	943946
TR5	N	MMBT2369	943946
TR6	N	MMBT2369	943946
TR7	N	MMBT2369	943946
TR8	F	MMBFU310	943945
TR9	N	MMBT2369	943946
TR10	N	PZT3904	948281
TR11	N	MMBT2369	943946
TR12	GP (BJ) P	BCX71J 150M	999204/MC
TR13	N	MMBT2369	943946
TR14	F	MMBFU310	943945
TR15	N	MMBT2369	943946
TR16	N	MMBT2369	943946
TR17	N	MMBT2369	943946
TR18	N	MMBT2369	943946
TR19	N	MMBT2369	943946
TR20	N	MMBT2369	943946

REF	DESCRIPTION		PART No.
TR21	N	MMBT2369	943946
TR22	N	MMBT2369	943946
TR23	N	MMBT2369	943946
TR24	N	PZT3904	948281
TR25	N	MMBT2369	943946
TR26	N	MMBT2369	943946
TR27	N	MMBT2369	943946
TR28	GP (BJ) P	BCX71J 150M	999204/MC
TR29	N	MMBT2369	943946
TR30	N	MMBT2369	943946
TR31	GP (BJ) P	BCX71J 150M	999204/MC
TR32	GP (BJ) P	BCX71J 150M	999204/MC
TR33	N	MMBT2369	943946
TR34	N	MMBT2369	943946
TR35	N	MMBT2369	943946
TR36	N	MMBT2369	943946
TR37		BFG16A	946709
TR38	F	MMBFU310	943945
TR39	GP (BJ) P	BCX71J 150M	999204/MC
TR40		BFG16A	946709
TR41	GP (BJ) P	BCX71J 150M	999204/MC
TR42	GP (BJ) P	BCX71J 150M	999204/MC
TR43	GP (BJ) P	BCX71J 150M	999204/MC
TR44	CHIP N	BFG35	999702/001
TR45	N	MMBT2369	943946
TR46	N	MMBT2369	943946
TR47	F	MMBFU310	943945
TR48	F	MMBFU310	943945
TR49	F	MMBFU310	943945
TR50			
TR51	F	MMBFU310	943945
TR52	F	MMBFU310	943945
TR53	GP (BJ) P	BCX71J 150M	999204/MC
TR54			
TR55	F	MMBFU310	943945

REF	DESCRIPTION	PART No.
TR56		
TR57	F MMBFU310	943945
TR58		
TR59	N BFQ19	943944
TR60	N 2N5109	945131
TR61	P 2N5160	938418
TR62	AMPLIFIER N 2N3866	947277
TR63	AMPLIFIER N 2N3866	947277
TR64	4 OFF MATCHED	88003/VAR-03
TR65	4 OFF MATCHED	88003/VAR-03
TR66	4 OFF MATCHED	88003/VAR-03
TR67	4 OFF MATCHED	88003/VAR-03
MIXER		
X2	RF	91459-01
CRYSTAL		
XL2	QUARTZ 40 MHZ	87964-01



Notes: 1. PL2 Terminating Impedance not less then 1kOhm
2. RF Amplifier is shown switched ON
3. Levels are with AGC ON

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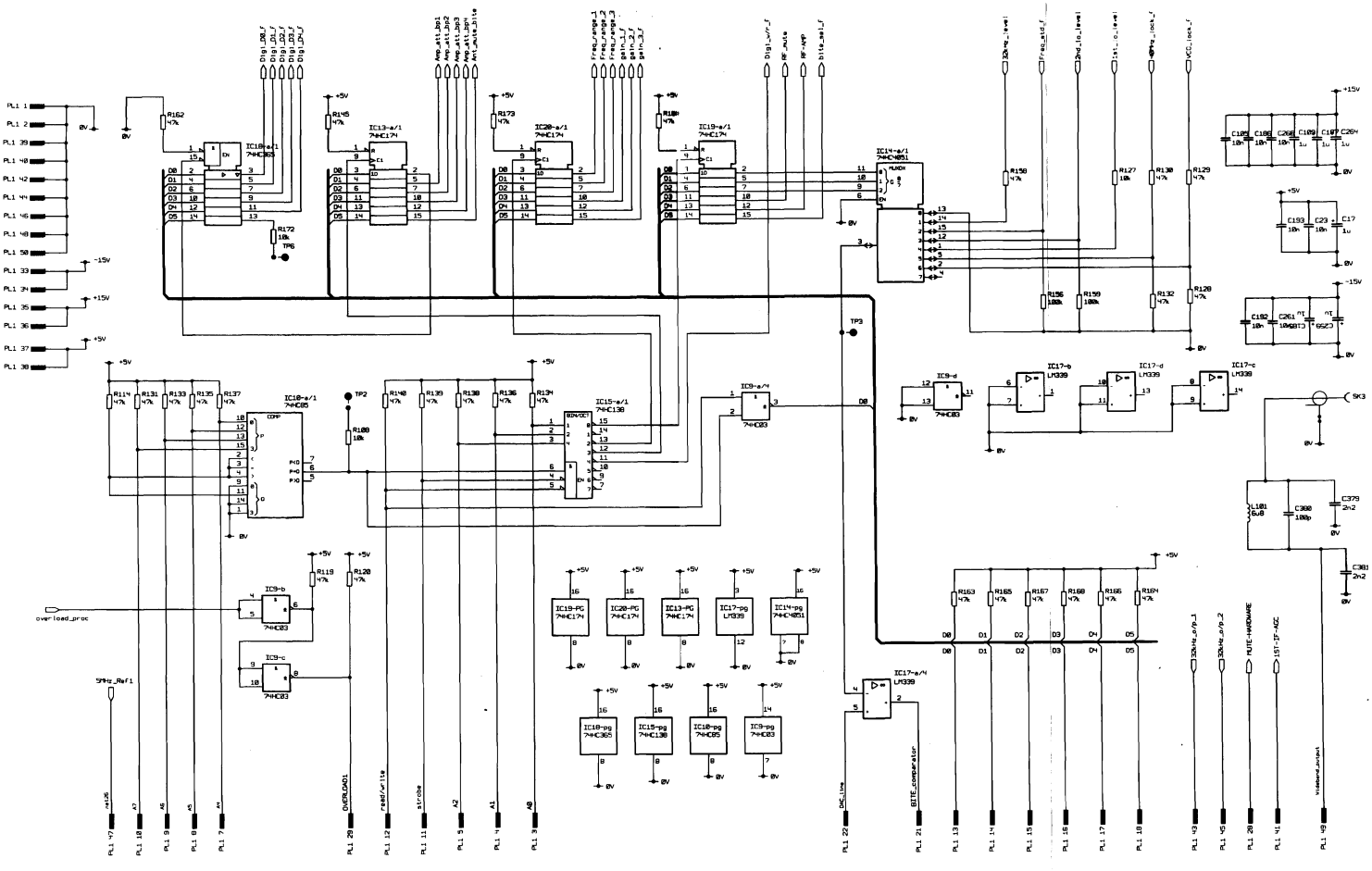
A5258

Signal Level Chart Fig. 6.13



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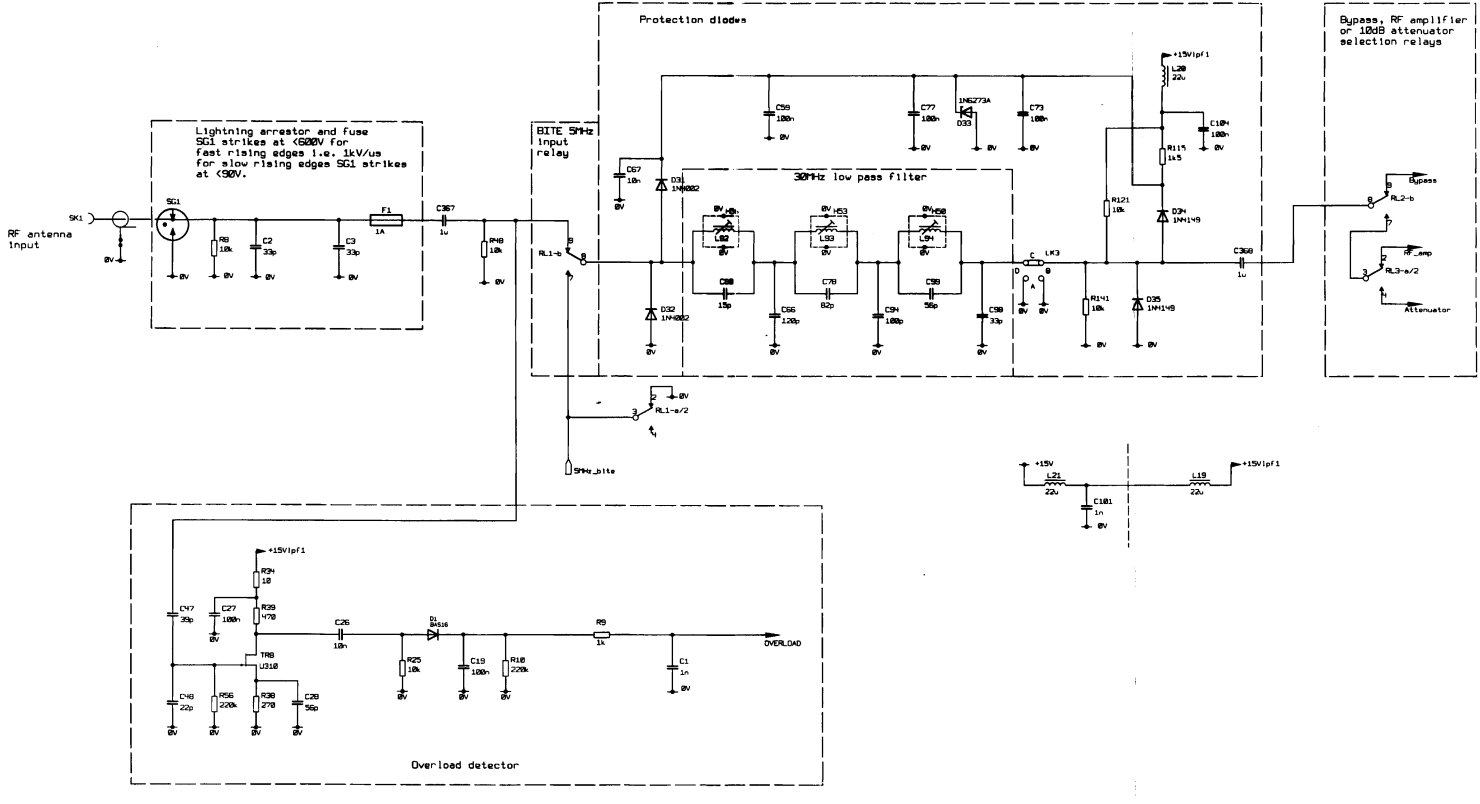
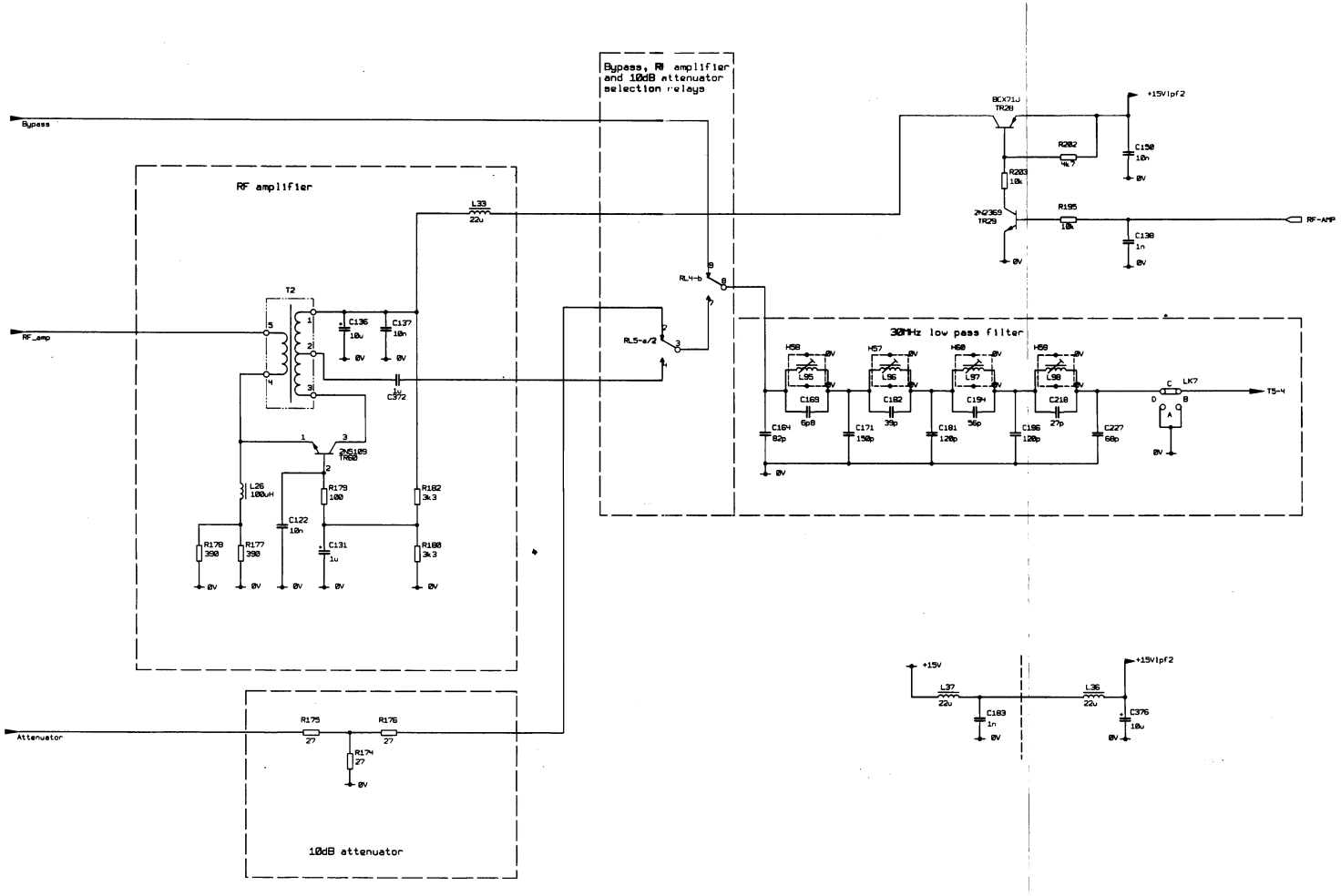
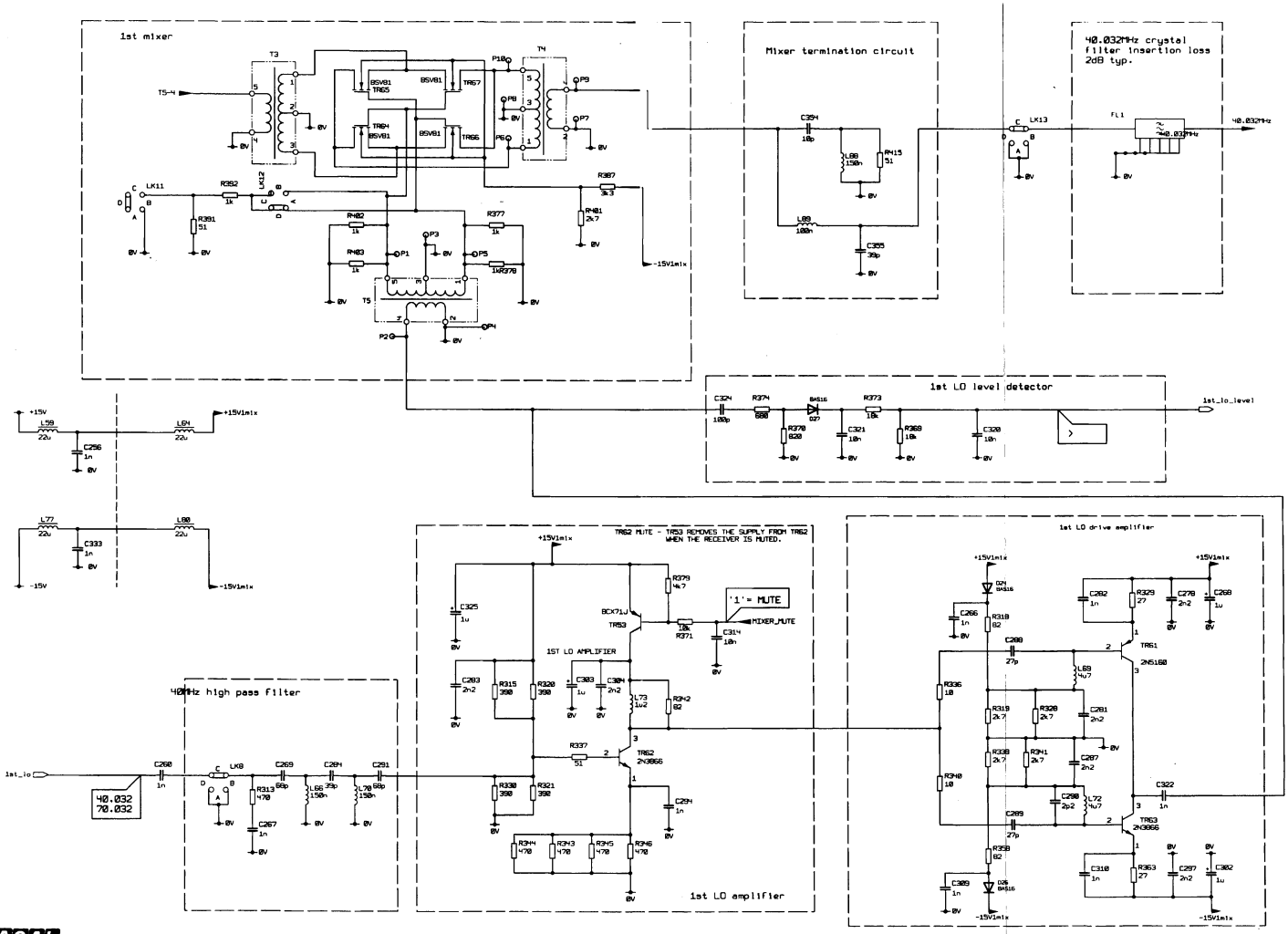
A5258/91220/1/3

Circuit: Analogue Board (Sheet 1) Fig. 6.14


Protection diodes
Bypass, RF amplifier or 10dB attenuator selection relays
Lightning arrestor and fuse
SG1 strikes at <600V for fast rising edges i.e. 1kV/us for slow rising edges SG1 strikes at <90V.
BITE 5MHz input relay
30MHz low pass filter
RF antenna input
SK1
SG1
F1
1A
C367
1u
R48
10k
RL1-b
RL1-a/2
5MHz_bite
D3
1N4002
D32
1N4002
C59
100n
C77
100n
1N5273A
D33
C73
100n
+15Vlpf1
L20
22u
C104
100n
R115
1k5
D2
1N4148
R121
10k
R141
10k
D35
1N4148
C360
1u
LK3
Bypass
RL2-b
RL3-a/2
RF_amp
Attenuator
L92
L93
L94
C88
15p
C66
120p
C78
82p
C94
100p
C98
56p
C99
33p
R9
10k
C2
33p
C3
33p
+15V
L21
22u
C101
1n
L19
22u
+15Vlpf1
Overload detector
R34
10
C47
39p
C27
100n
R39
470
C26
10n
D1
BA316
R9
1k
OVERLOAD
TR8
U310
C48
22p
R56
220k
R38
270
C28
56p
R25
10k
C19
100n
R10
220k
C1
1n


Bypass, RF amplifier and 10dB attenuator selection relays
Bypass
RF amplifier
RF_amp
Attenuator
10dB attenuator
30MHz low pass filter
RF-AMP
T5-4
+15V
+15V1pf2
BCX71J TR28
2N2369 TR29
2N5109 TR60
RL4-b
RL5-a/2
L33 22u
T2
C136 10u
C137 10n
C372 1u
L25 100uH
R178 390
R177 390
R179 100
C122 10n
C131 1u
R182 3k3
R180 3k3
R175 27
R176 27
R174 27
L95
L96
L97
L98
C163 6p8
C164 82p
C182 33p
C171 150p
C194 56p
C181 120p
C218 27p
C196 120p
C227 68p
R202 4k7
R203 10k
R195 10k
C150 10n
C138 1n
L37 22u
L36 22u
C183 1n
C376 10u
0V



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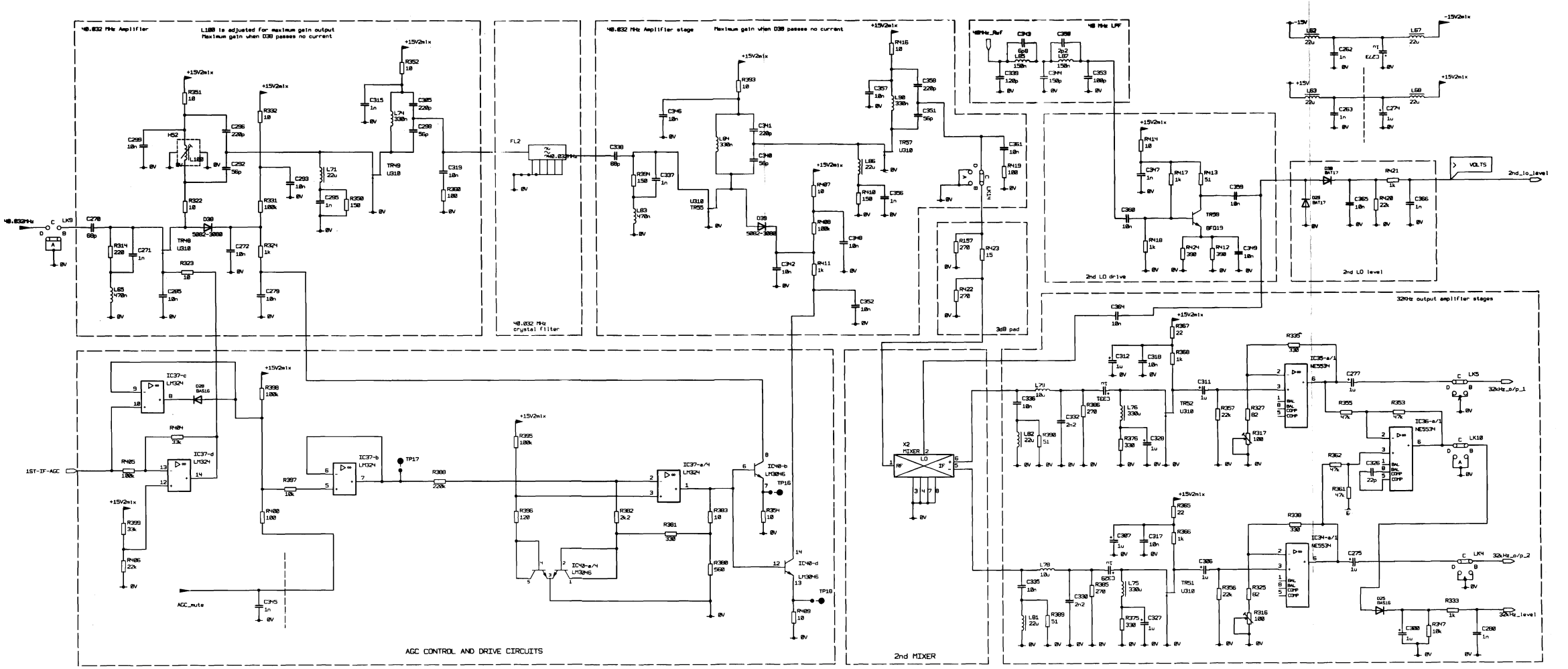
A5258/91220/4/3

Circuit: Analogue Board (Sheet 4) Fig. 6.17



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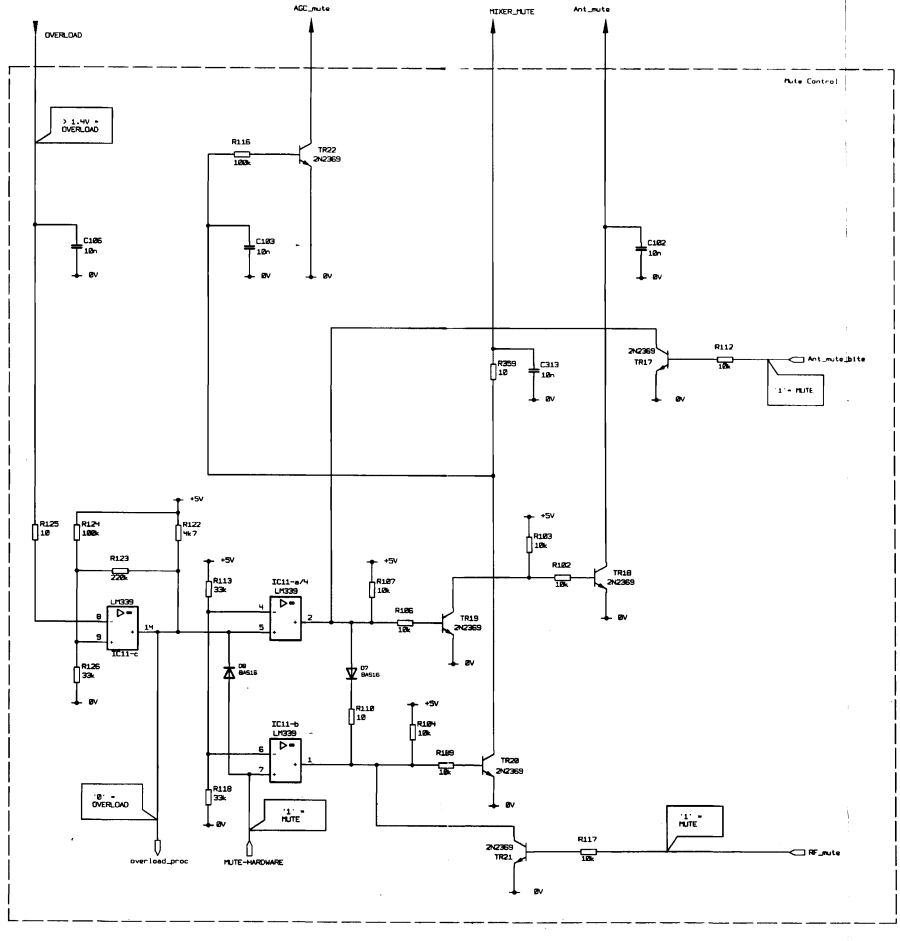
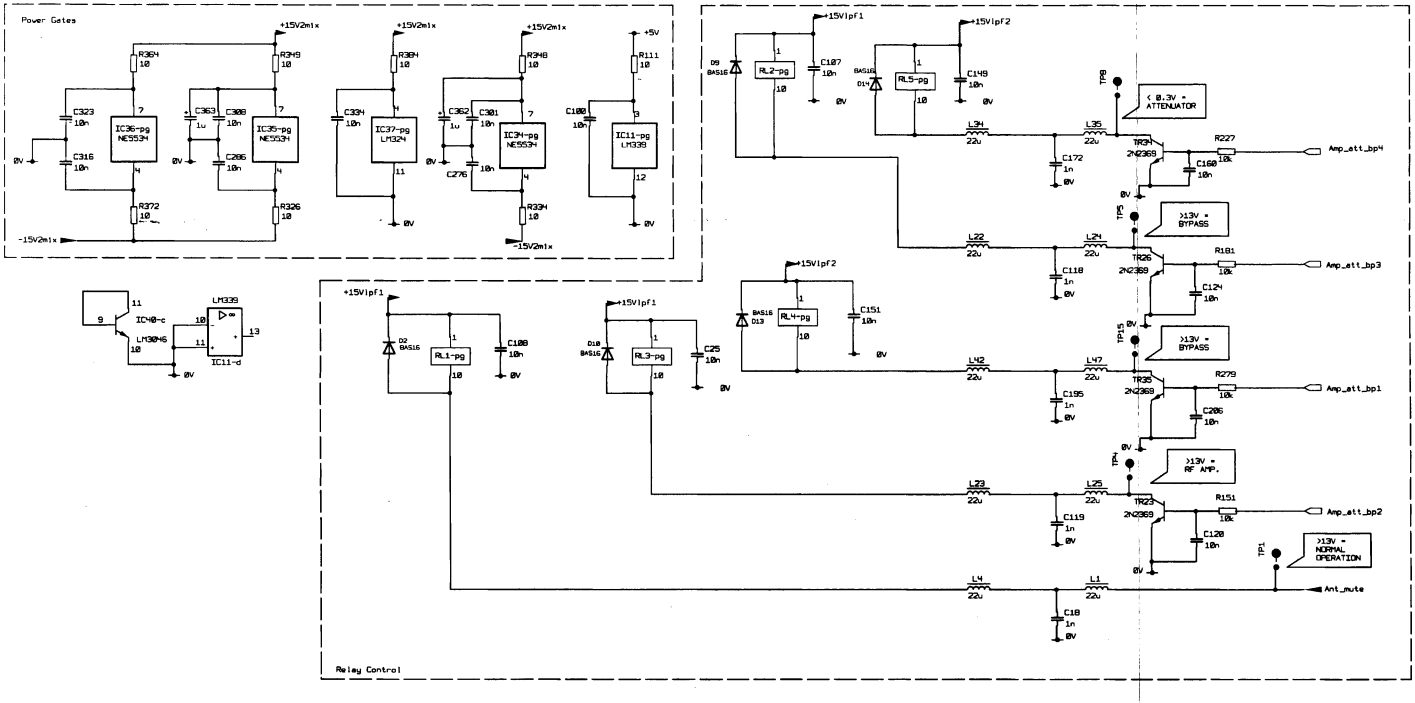
A5258/91220/5/3

Circuit: Analogue Board (Sheet 5) Fig. 6.18

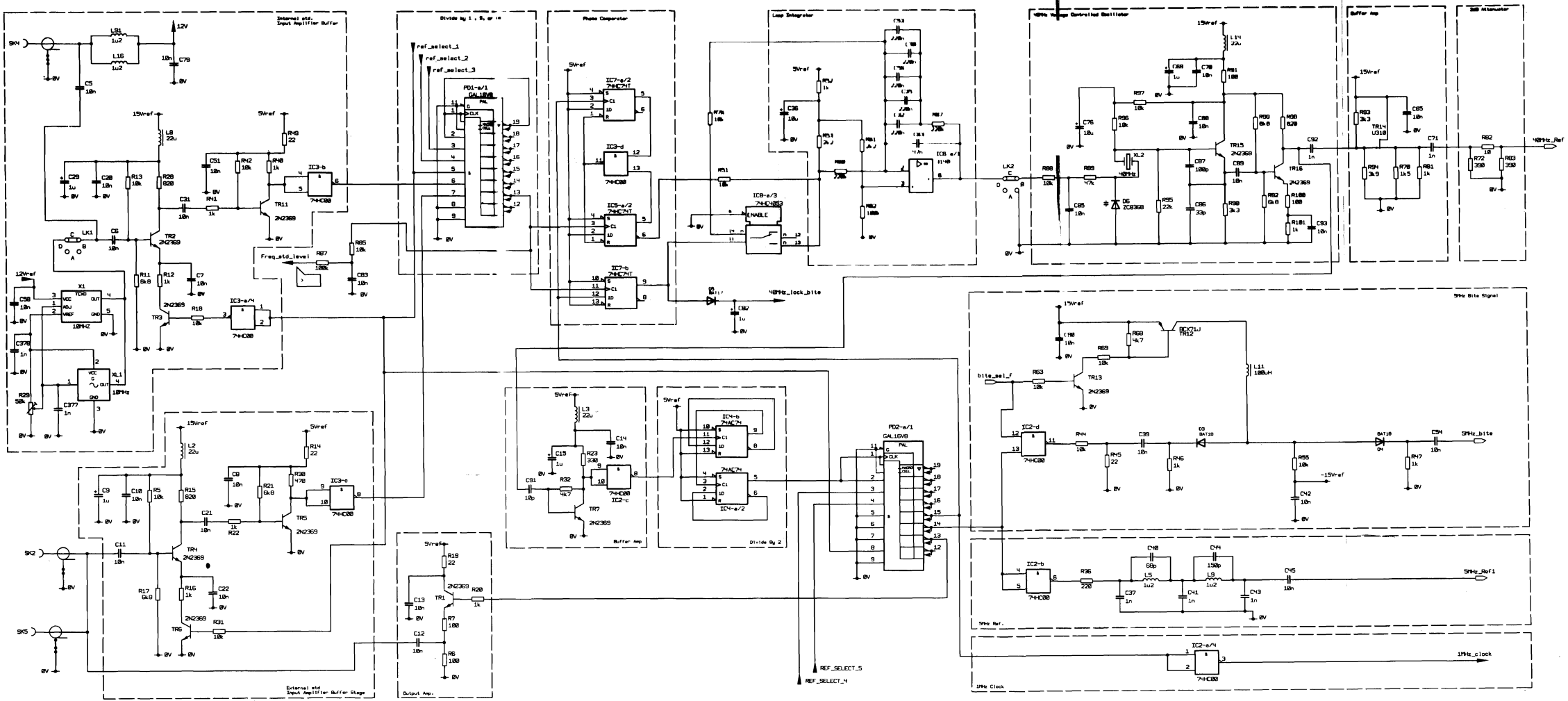

AGC_mute
MIXER_MUTE
Ant_mute
OVERLOAD
Mute Control
> 1.4V = OVERLOAD
R116
100k
TR22
2N2369
C105
10n
C103
10n
C102
10n
0V
R359
10
C313
10n
2N2369
TR17
R112
10k
Ant_mute_bite
'1' = MUTE
+5V
R125
10
R124
100k
R122
4k7
R123
220k
LM339
IC11-c
14
9
8
R126
33k
R113
33k
IC11-a/4
LM339
4
5
2
R107
10k
R105
10k
TR19
2N2369
R103
10k
R102
10k
TR18
2N2369
D6
BAS16
D7
BAS16
R118
10
IC11-b
LM339
6
7
1
R104
10k
R109
10k
TR20
2N2369
R118
33k
'0' = OVERLOAD
'1' = MUTE
overload_proc
MUTE-HARDWARE
2N2369
TR21
R117
10k
'1' = MUTE
RF_mute



	TP4	TP15	TP5	TP8
RF AMP	> 13V	< 0.3V	< 0.3V	> 13V
ATTEN	< 0.3V	< 0.3V	< 0.3V	< 0.3V
BYPASS	X	> 13V	> 13V	X

X = DON'T CARE
> 13V = RELAY DE-ENERGISED
< 0.3V = RELAY ENERGISED

Circuit: Analogue Board (Sheet 7) Fig. 6.20



RACAL
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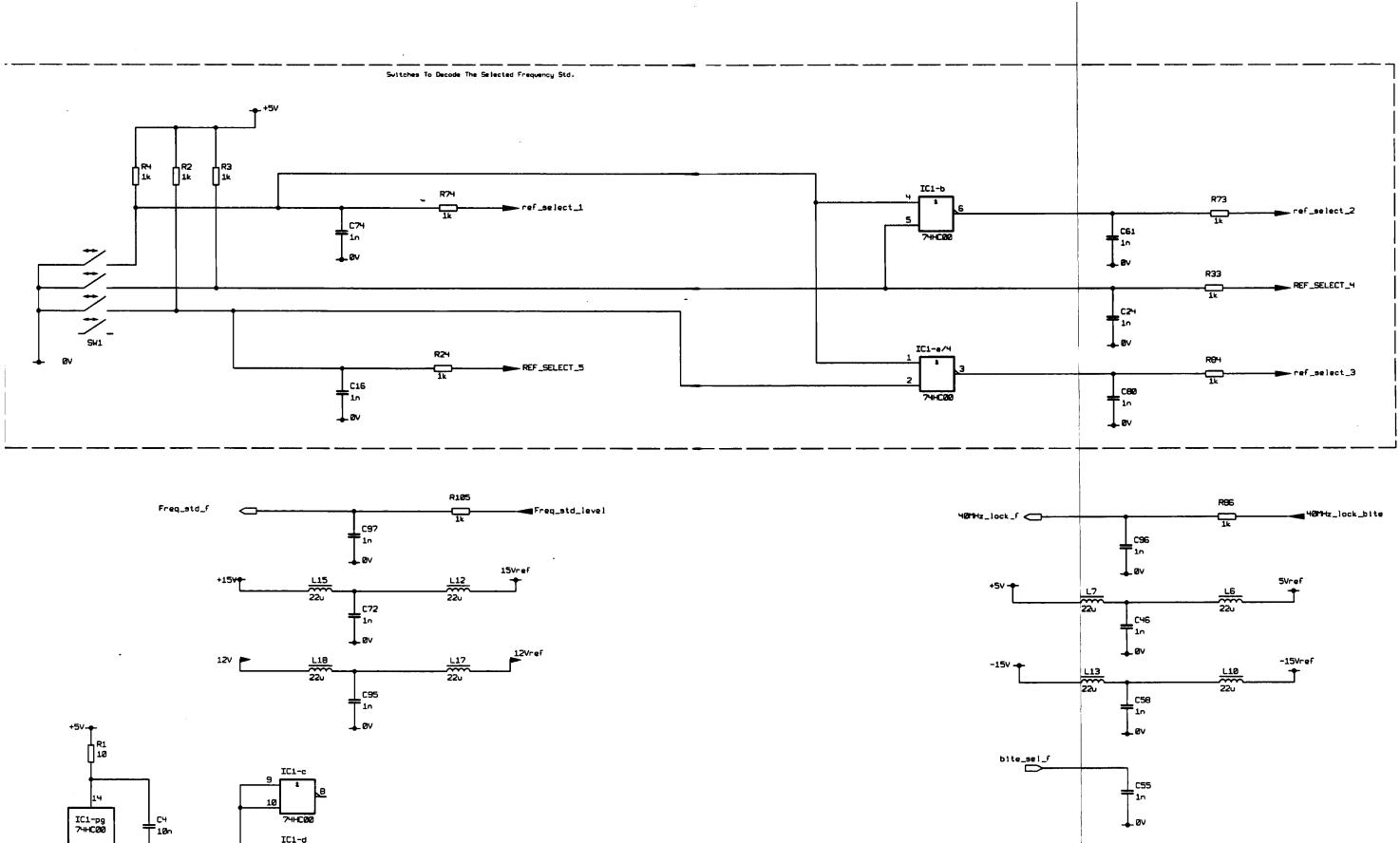
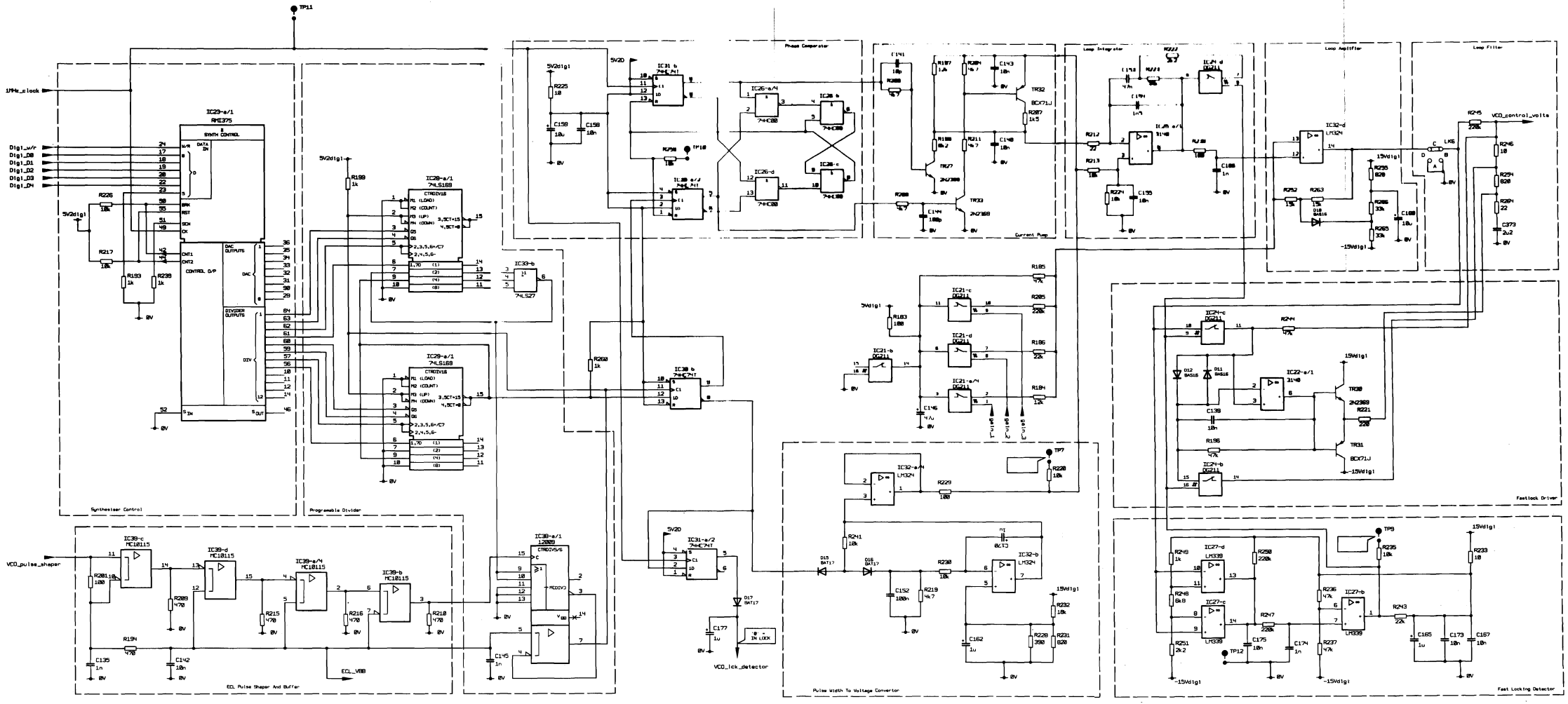
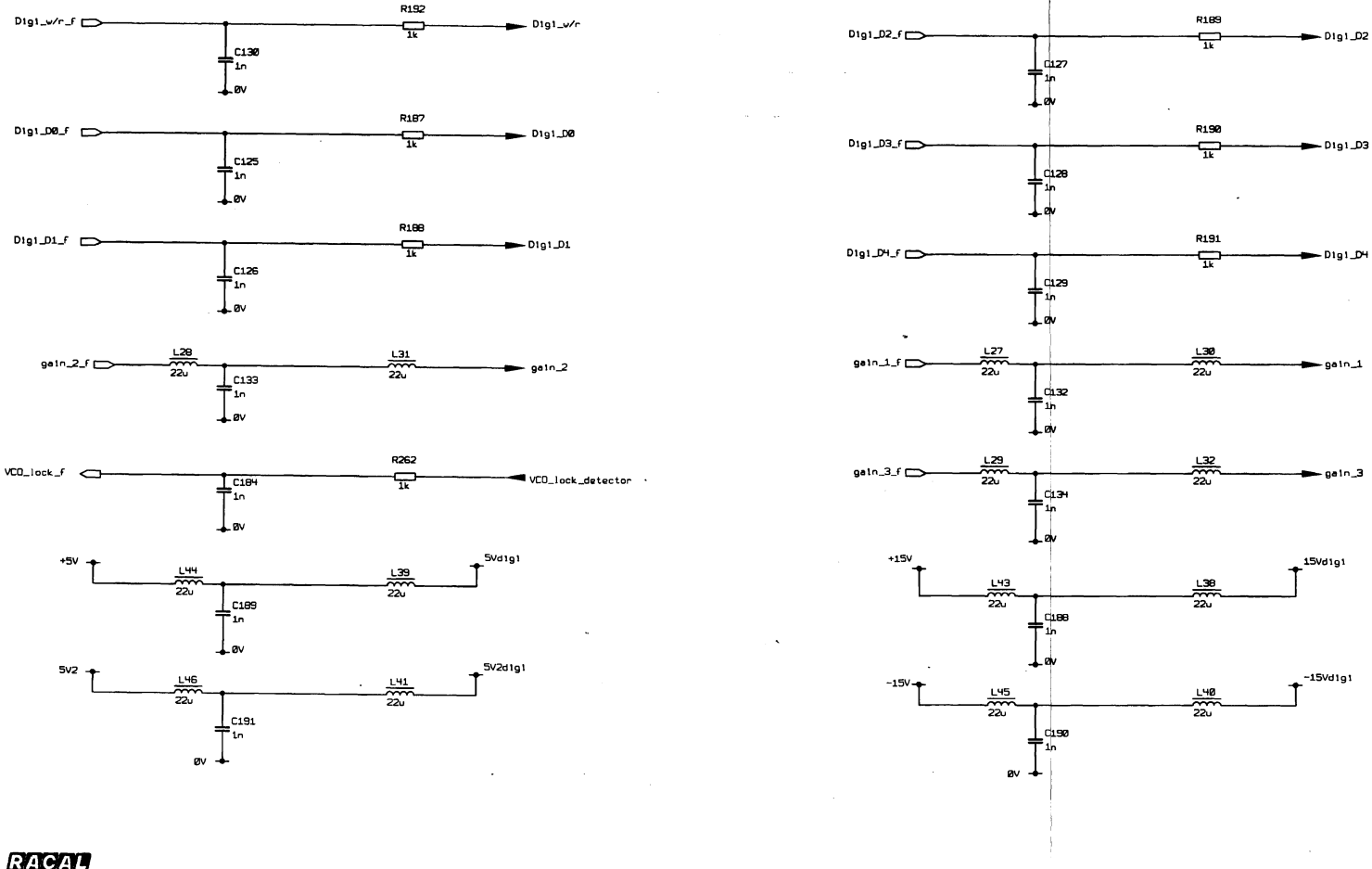
Circuit: Analogue Board (Sheet 8) Fig. 6.21

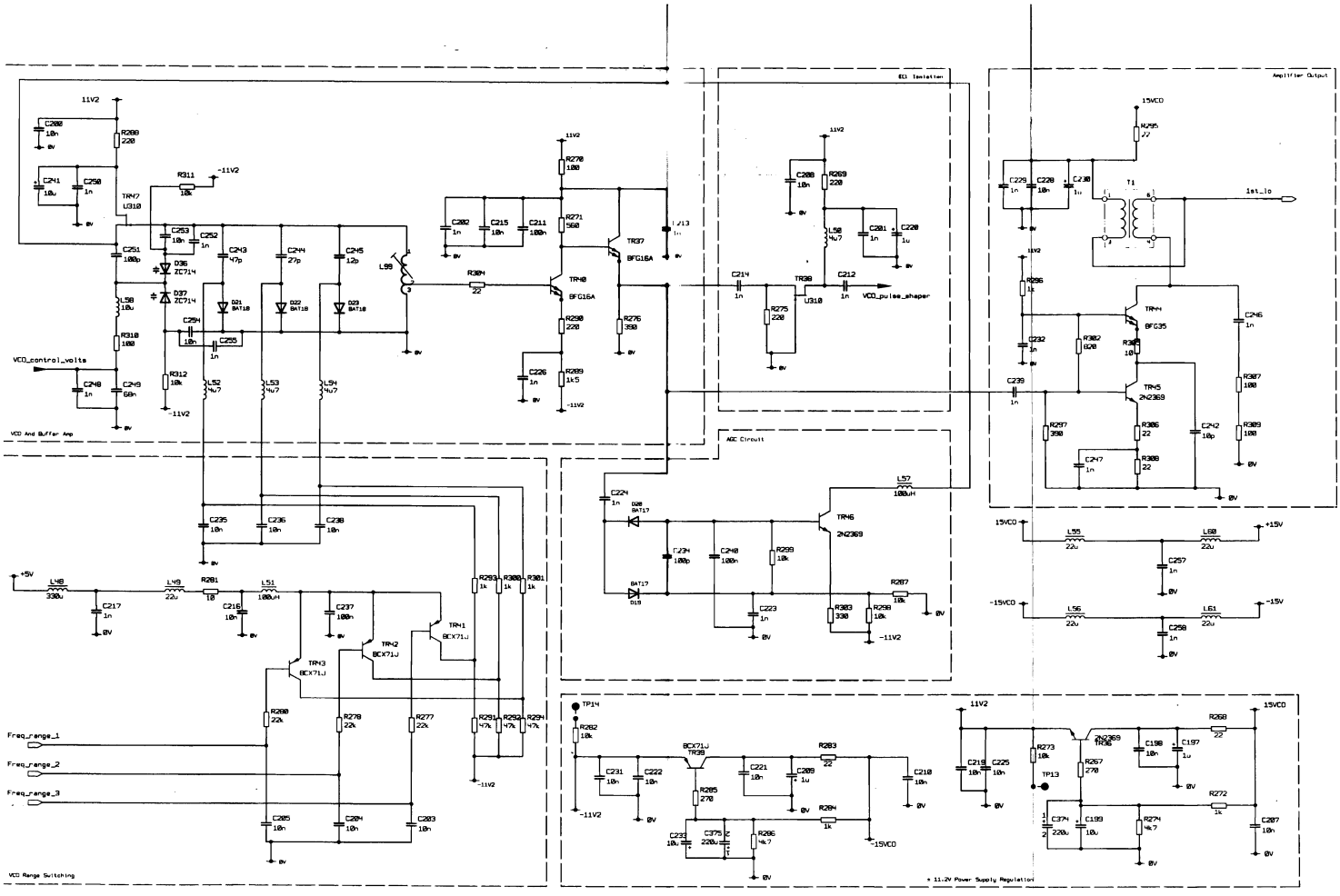

Switches To Decode The Selected Frequency Std.
+5V
R4 1k
R2 1k
R3 1k
SW1
0V
R74 1k
ref_select_1
C74 1n
0V
R24 1k
REF_SELECT_5
C16 1n
0V
IC1-b
74HC00
R73 1k
ref_select_2
C61 1n
R33 1k
REF_SELECT_4
C24 1n
IC1-a/4
74HC00
R84 1k
ref_select_3
C80 1n
Freq_std_f
R105 1k
Freq_std_level
C87 1n
+15V
L15 22u
L12 22u
15Vref
C72 1n
12V
L18 22u
L17 22u
12Vref
C95 1n
+5V
R1 10
IC1-pg 74HC00
C4 10n
IC1-c
74HC00
IC1-d
74HC00
400Hz_lock_f
R86 1k
400Hz_lock_bite
C96 1n
+5V
L7 22u
L6 22u
5Vref
C46 1n
-15V
L13 22u
L10 22u
-15Vref
C58 1n
bite_sel_f
C55 1n

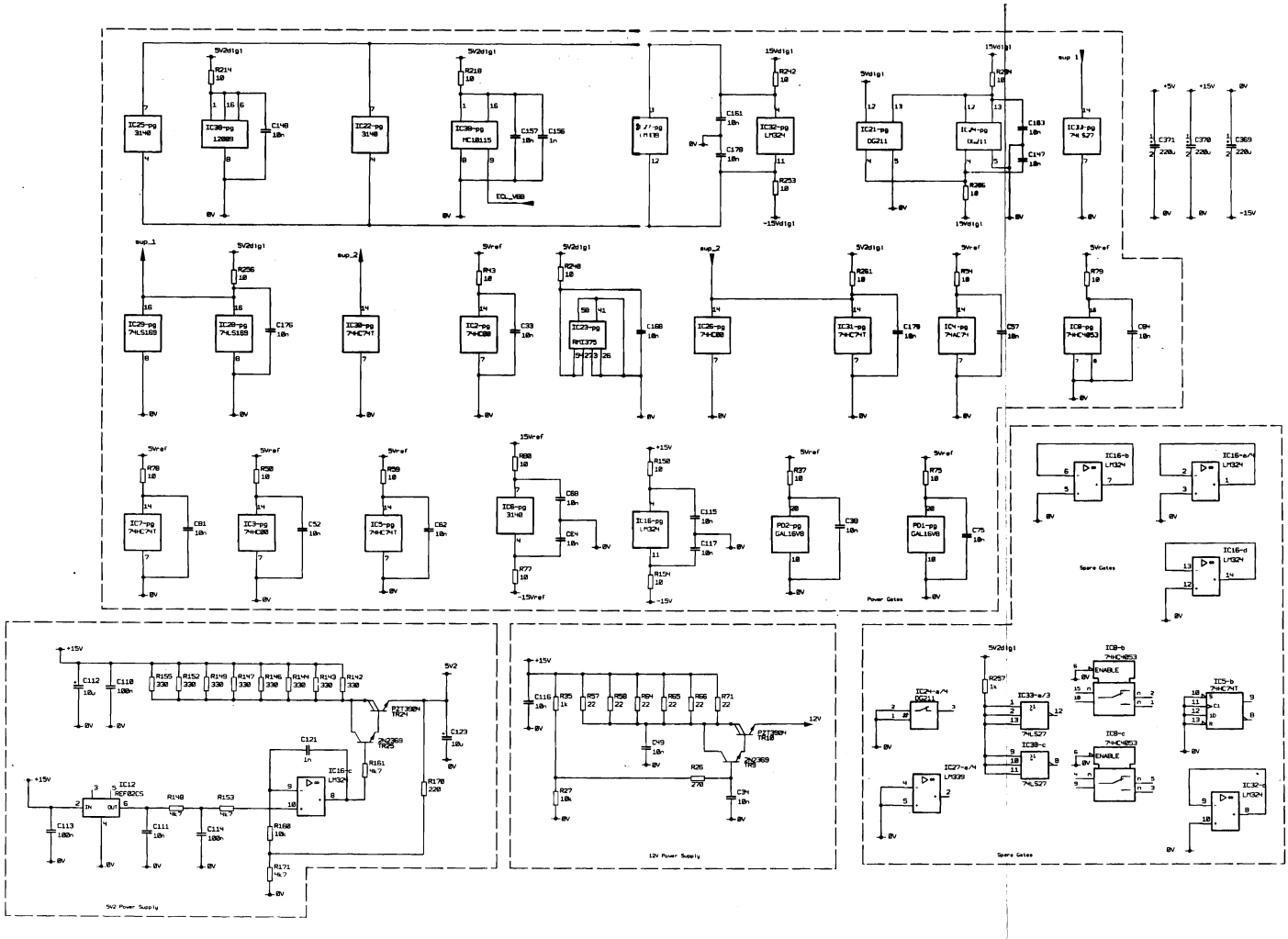


Circuit: Analogue Board (Sheet 10) Fig. 6.23

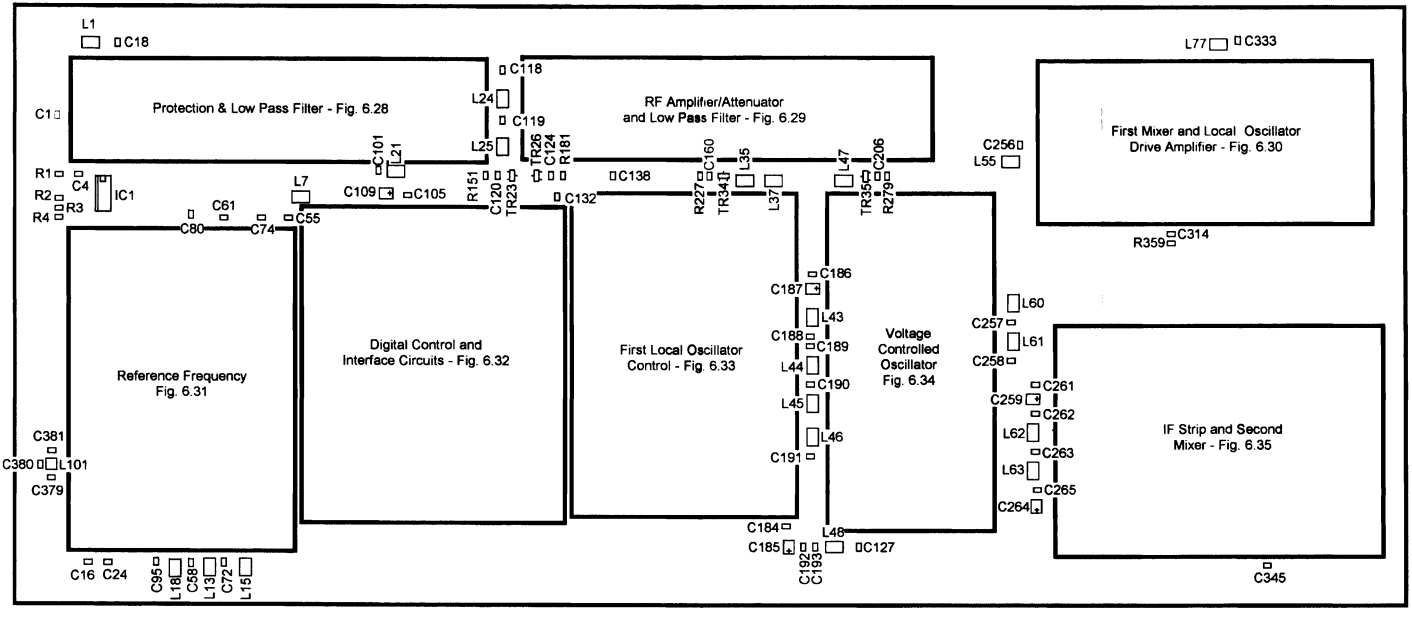


Circuit: Analogue Board (Sheet 11) Fig. 6.24


VCO And Buffer Amp
VCO Range Switching
AGC Circuit
ECL Isolation
Amplifier Output
+ 11.2V Power Supply Regulator
VCO_control_volts
VCO_pulse_shaper
Freq_range_1
Freq_range_2
Freq_range_3
1st_lo
11V2
-11V2
15VCO
-15VCO
+15V
-15V
+5V
0V



Circuit: Analogue Board (Sheet 13) Fig. 6.26



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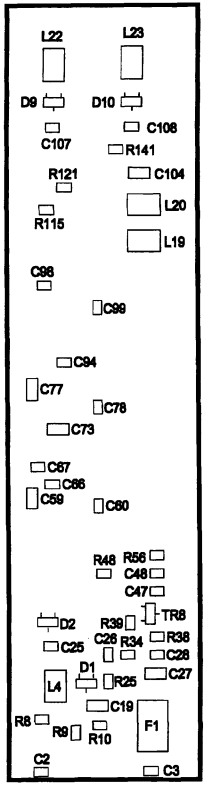
Layout: Analogue Board (Side 1)

Fig. 6.27



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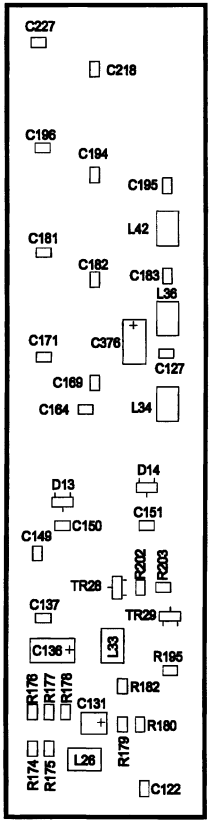
Layout: Protection & Low Pass Filter

Fig. 6.28



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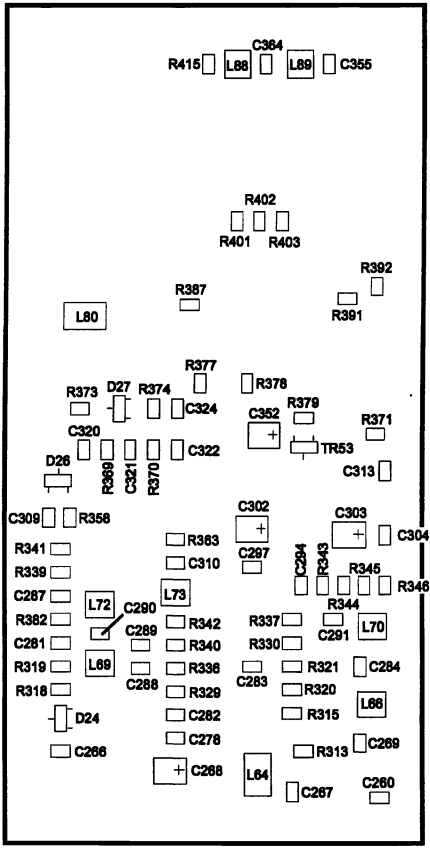
A5258

Layout: RF Amplifier/Attenuator and Low Pass Filter

Fig. 6.29



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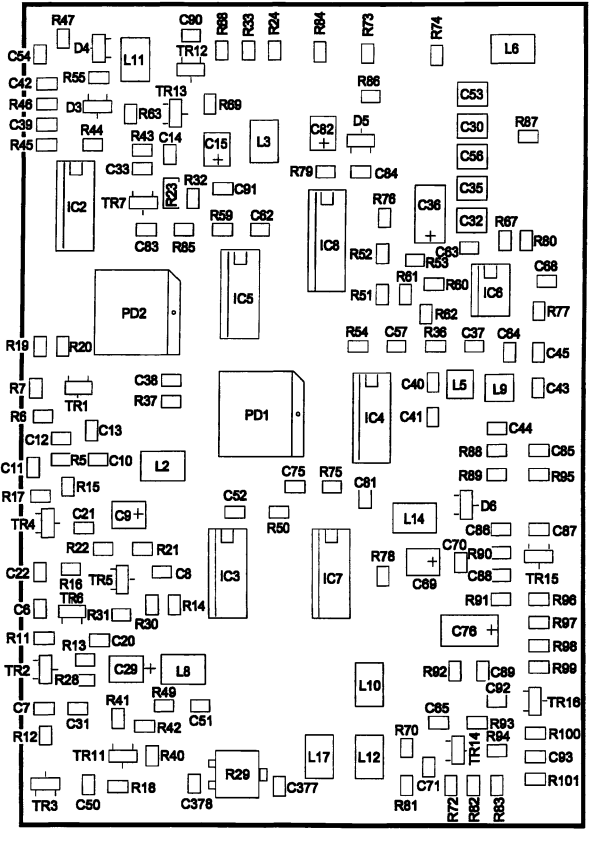
Layout: First Mixer & Local Oscillator Drive Amplifier

Fig. 6.30



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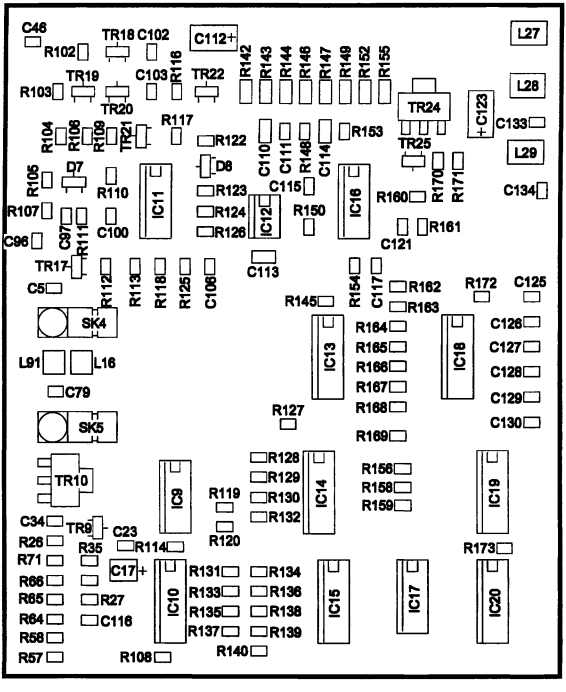
Layout: Reference Frequency

Fig. 6.3



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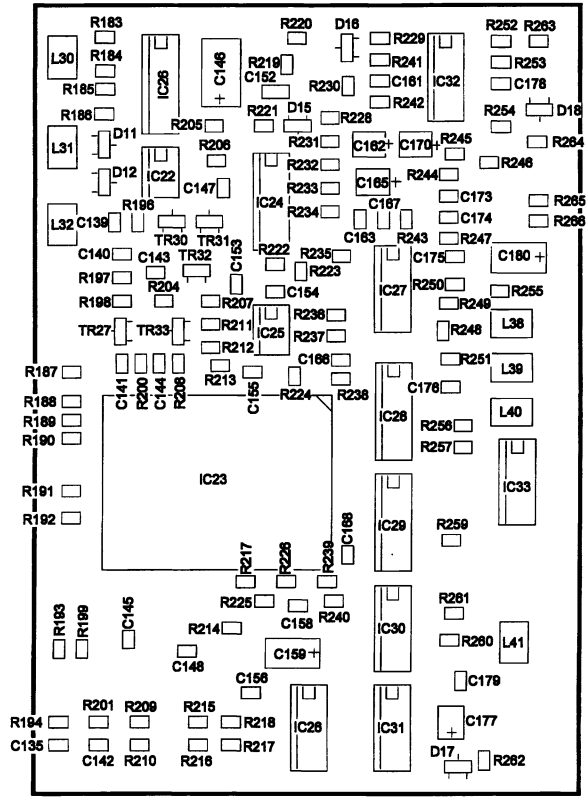
Layout: Digital Control and Interface Circuits

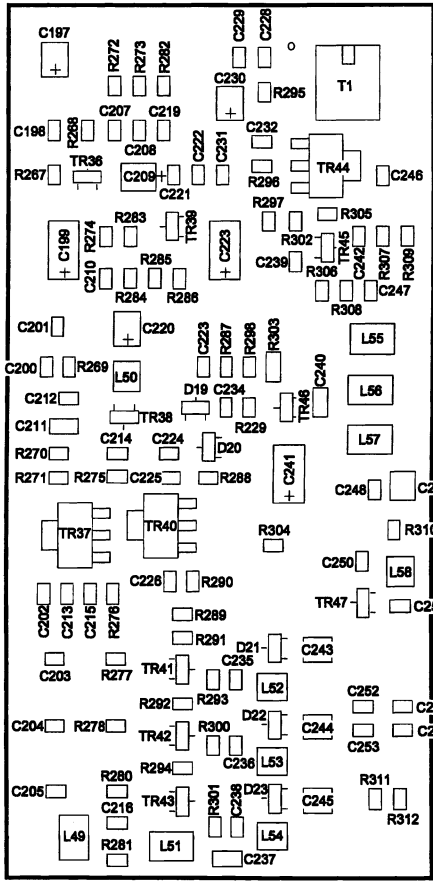
Fig. 6.32



RACAL
A5258

Layout: First Local Oscillator Control

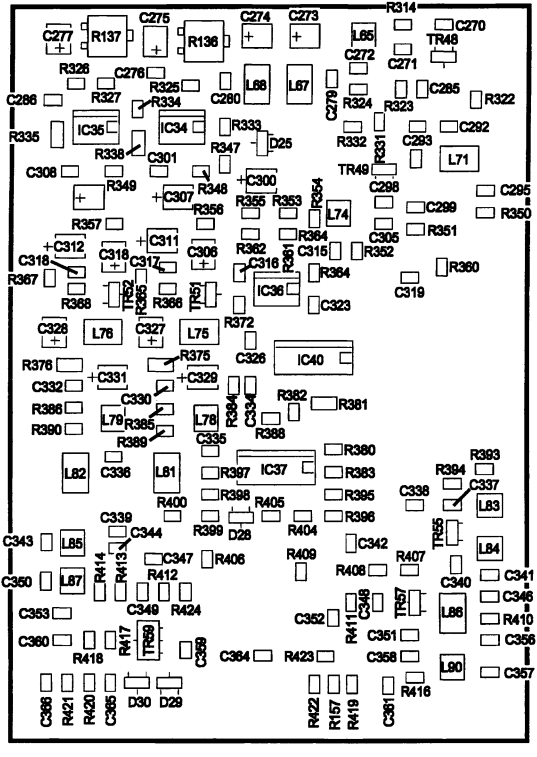
Fig. 6.33



RACAL
A5258

Layout: Voltage Controlled Oscillator

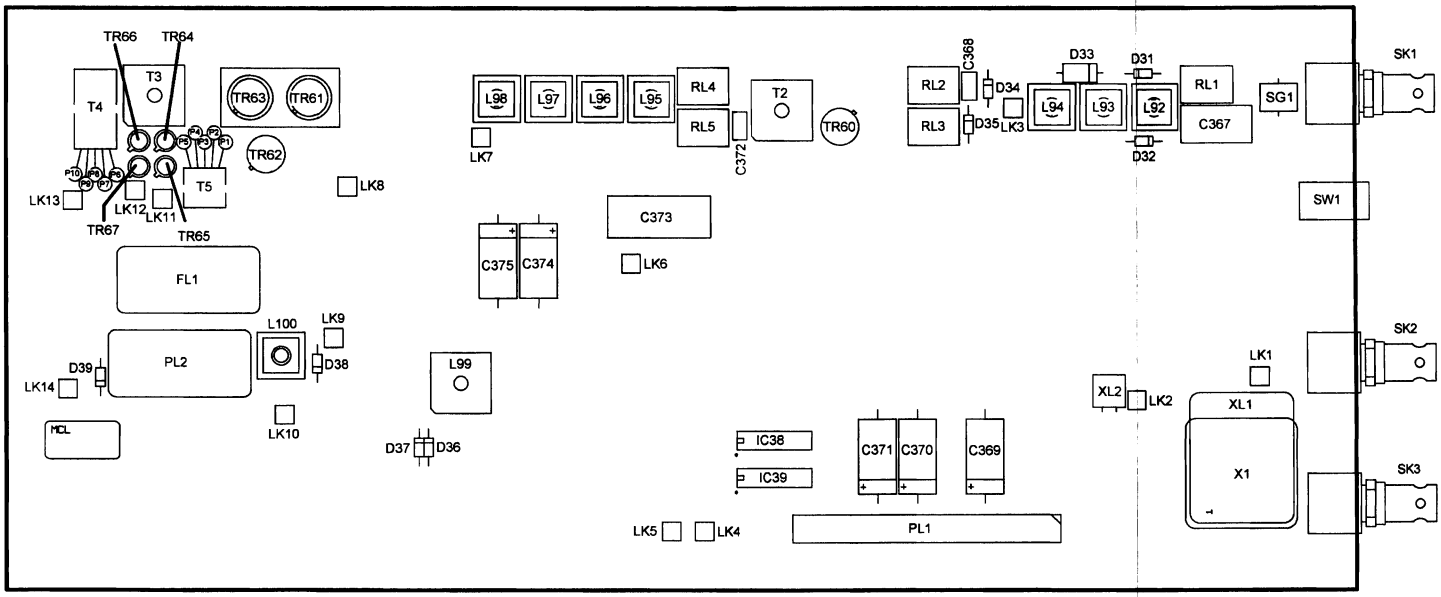
Fig. 6.34



RACAL
A5258

Layout: IF Strip & Second Mixer

Fig. 6.35



RACAL
A5258

Layout: Analogue Board (Side 2)

Fig. 6.36

CHAPTER 7

DIGITAL BOARD

CONTENTS

Tables

Illustrations

Text:

At end of Chapter:

Fig.

CHAPTER 7

DIGITAL BOARD

INTRODUCTION

1. The digital board contains the receiver control processing and the IF/AF function of the receiver. It performs the following functions:

   (1) It accepts the IF signals from the analogue board.

   (2) It provides IF filtering using digital filters.

   (3) It provides the signal demodulation for CW + BFO, AM, FM, FSK, SSB and, optionally, ISB (SSB demodulation only).

   (4) It provides the front and back-end gain control - automatic, manual and automatic with threshold.

   (5) It provides a digital IF/AF and spectrum output.

   (6) It provides signal detection, based on RF level and signal-to-noise ratio (SNR).

   (7) It provides an analogue audio output to the front-panel.

   (8) It provides two analogue audio 600-ohm balanced-line outputs.

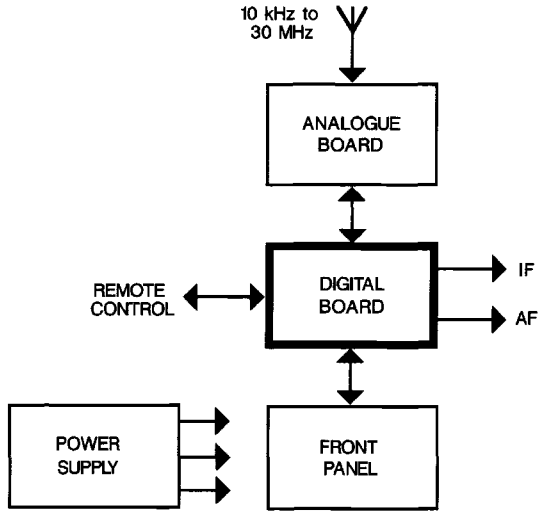


Fig. 7.1 RA3791 Receiver Block Diagram

(9) It provides an analogue IF output signal, either wideband or filtered, for application to the analogue board, at 1.4 MHz or in the range 10 kHz to 455 kHz.

(10) It provides the processing for the front-panel display and user control.

(11) It provides two serial remote control ports to allow the receiver to be controlled remotely, and for it to control other RA3790 series receivers.

BOARD DESCRIPTION

2. The following description should be read in conjunction with the block diagrams and circuit diagrams included in this chapter. Where a sheet number is given against a particular heading or circuit reference, this refers to the circuit diagram sheet number. Board printed circuit component layout drawings are also included at the end of the chapter.

3. The board description is divided into two sections, the DSP section and the Control Processor section.

DSP Section

Digital Signal Processing (Sheets 1 and 2)

4. The board can accommodate four digital signal processor devices (type DSP56002), but either one or both of DSP3 (IC82) and DSP4 (IC91) may be not fitted, dependant on the particular options fitted. The four DSP devices share a common 24-bit data bus, which allows common access to the 28K x 24-bit RAM (IC84, 87 and 89), the 52K x 8-bit EPROM (PD7), the peak detection PAL (PD2 - Sheet 3), the DPRX ASIC (IC86 - Sheet 3) and the parallel input/output (IC60 and 76 - Sheet 6).

5. DSP2, DSP3 and DSP4 have their host ports connected to the DSP data bus, which enables them to have code from EPROM loaded into them by DSP1 at RESET, and allows communication between them (in addition to data transfers via the RAM). The address decoding to select the devices on the bus is carried out by the address decoding PAL devices (PD4 and PD5).

6. To allow the four DSP devices to share the data bus, a bus arbitration PAL device (PD3) is used to control the DSP bus request lines. The inputs to the bus arbitrator from each DSP are:

(1) The bus grant line (BGn)

(2) Two software controlled lines, PC2 for requesting the bus (RBn), and PC4 for requesting data transfer (DTn).

7. Outside the data transfer time, the arbitrator gives the bus to the highest priority DSP that requests it (the order being DSP1, DSP2, DSP3, DSP4), or if none of them request the bus, it is given to DSP1.

8. At data transfer time, the arbitrator waits until all four DSPs are ready for data transfer and then gives the bus to each of them in turn to carry out their data transfer, the order being DSP2, DSP3, DSP4, DSP1. The DSP3 and DSP4 select lines are also input to the bus arbitrator so it can account for them not being present. The HACK pin of each DSP is configured as a general purpose input to monitor its bus request line.

9. The IRQB interrupt for all four DSPs is generated by the DPRX ASIC (IC86) by dividing its 11.2 MHz clock to 16 kHz, locked to the 5 MHz reference. This is used to initiate data transfers between the DSPs, and as the sample rate clock for the signal processing. The IRQA interrupt to DSP2 and DSP3 is also generated by the ASIC. Programmed at 80 kHz, it is used as the sample rate for the analogue IF output.

10. The four DSPs run from the same 10 MHz clock, generated by a crystal oscillator (XL3). Each DSP multiplies this to a 40 MHz processing clock using an internal phase locked loop (PLL). The 40 MHz clock generated by DSP1 is routed to the bus arbitrator and to the slow address decoder (PD4) for clocking the outputs. The IRQA and IRQB lines are gated with the reset line (with a 1 µs delay added) so that DSP2, 3 and 4, which have NMI pulled high, are all in mode 9, bootstrap from host mode, at reset. DSP1 has its NMI line controlled by the control processor so at reset it can be low for bootstrap from EPROM (normal operation) or high for bootstrap from host (code downloaded from the Control Processor for signature analysis).

11. The Control Processor communicates with the DSP section using the host port of DSP1. This sits on the Control Processor data, address and control buses. The HREQ line from the host is an interrupt line into the Control Processor to request communication.

12. The Key PAL (PD6), when fitted, is used to determine which software options are made accessible. The Key PAL is seeded, clocked and then read on power-up to determine the option.

13. The four plugs, PL7, 8, 9 and 10, connected to the DSP devices, are provided for emulation purposes during development via an on-chip emulator (ONCE) interface. These plugs are not normally fitted.

DSP Serial Ports (Sheets 1 and 2)

14. Each DSP has two bi-directional serial ports, SSI and SCI. The SSI ports are synchronous (ie the transmit and receive data share a clock and frame sync) and the SCI ports are asynchronous (ie no clock is used). The ports are configured as follows:

(1) DSP1: SSI is connected to codec 1 (IC22) for audio input and output. The 1.536 MHz clock and 16 kHz frame sync are generated by the codec. The SC0 line is used as a general purpose output to reset the codec.

SCI is connected to an RS-423 interface (IC9 and 16) for FSK. The external interface is also set as an input for BITE.

(2) DSP2: SSI is connected to the sigma-delta ADC (IC59 - Sheet 3) to receive the IF input and to the AGC DAC (IC55 - Sheet 3) for front-end control voltage output. The SC0 line is used to generate an IRQA interrupt in DSP1 and DSP4.

SCI is connected to an RS-423 interface (IC9 and 14) for external gain control, input and output.

(3) DSP3: SSI is connected to an RS-422 interface (IC3) for the digital IF/AF data. The clock is 1.536 MHz, generated by codec 1 (IC22), the frame sync is 64 kHz generated by DSP3 and the data is 24-bit words. The SC0 line is used as a general purpose output to enable/disable the output line drivers. SCI is not connected.

(4) DSP4: SSI is connected to codec 2 (IC23) for audio input and output. The 1.536 MHz clock and 16 kHz frame sync are generated by the codec. The SC0 line is used as a general purpose output to reset the codec.

SCI is connected to an RS-423 interface for FSK2 output, but this is not used. The external interface can also be set as an input (but not if FSK1 is an output).

IF Section (Sheet 3)

15. The balanced 32 kHz IF input from the analogue board is amplified (IC56 and 57), so that the nominal peak level (under AGC) is -3 dB_{fs}, and is then converted (and filtered) to a 16-bit digital signal by the sigma-delta ADC (IC59) at a 6.144 MHz sampling rate. This is read by DSP2 (IC70) via its SSI port at 96 Ksamples/second. Each sample is a 16-bit word with the serial data clocked at 1.536 MHz.

16. In a parallel path the IF is attenuated (IC63), so that the nominal peak level is -18 dB_{fs}, and converted to an 8-bit digital signal by an ADC (IC69) at a sample rate of 3.072 MHz. The peak value of this signal is calculated by the peak detection PAL (PD2) which is read, and automatically reset, by the DSPs using the DSP data bus at a 16 kHz rate.

17. The front-end AGC voltage is calculated by the software and converted to an analogue signal (in the range 0 to 10 V) by the AGC DAC (IC55) and amplifier (IC54), with a 16 kHz low pass filter to remove any images. The value is written to the DAC by DSP2 via its SSI running synchronously with sigma-delta ADC (ie 96 Ksamples/second, 16-bit words).

18. The analogue 1.4 MHz IF output is either wideband, or filtered by digital filters. The complex IF output produced by the DSP software is written to the DPRX ASIC (IC86) as two 16-bit signals (in-phase (I) and quadrature (Q)) via the DSP data bus at 80 Ksamples/second (the IRQA rate). The DPRX ASIC (Digital Processing Receiver Application Specific IC) is a quadrature-baseband processor designed for use in a digital transceiver. In this application, the transmit mode only is used to produce a real 1.4 MHz IF 8-bit digital output signal which is converted to an analogue signal by the DAC (IC90) at an 11.2 MHz sampling rate. This signal is filtered, amplified and buffered (for a 50 ohm load).

Audio Section (Sheet 4)

19. The audio output is written to the codecs (IC22 and IC23) via the SSI of DSP1 and DSP4 at 16 Ksamples/second, as 14-bit data at a nominal -6 dB_{fs}. Similarly, the audio input is read from the codecs via the SSI of DSP1 and DSP4, with the transmit and receive data synchronous (ie sharing a clock and frame sync). For each SSI the clock and frame sync are generated by the codec which divides its 6.144 MHz input clock to give a 1.536 MHz clock and 16 kHz frame sync. The data is 14-bits of audio plus 2 control bits. The codecs provide digital to analogue conversion, with sinx/x correction and a 6.5 kHz image filter, for the audio output and analogue to digital conversion, with anti-aliasing and DC rejection filters for the audio input.

20. The audio switching routes the signals to where they are required. The line input/output has a range of -30 dBm to +10 dBm and this level is set by the multiplying DACs (IC24) which have the audio signal as their voltage reference input. The audio switching and multiplying DACs are controlled by the control processor. The audio to the front-panel, for the loud speaker, is via a buffer (IC12) whose input is either from the codec output or from an external audio input. This audio is also routed back to the codec auxiliary input (for BITE) and via a FET switch (TR11) to the monitor audio output. The output of the multiplying DACs is routed to the codec input for BITE.

21. Transformers T1 and T2 provide 600 ohm balanced line outputs. With links LK1 and LK2 in position A, the lines are outputs. By moving either link to position B, the respective line becomes an input and is used for BITE loopback tests.

Frequency Reference (Sheet 5)

22. The frequency reference section consists of two phase-locked loops (PLL) from which are derived all the clocks except the DSPs clock. The first loop takes the

amplified, external 5 MHz reference and produces 11.2 MHz locked to it, for the DPRX ASIC and the IF output DAC clocks. The PLL synthesiser (IC74) divides the 5 MHz and the 11.2 MHz to produce 200 kHz signals (available at pins 13 and 3) which are the inputs to the phase detector.

23. The second loop takes the 11.2 MHz from the first loop and produces 12.288 MHz locked to it, for the sigma-delta clock. The 12.288 is divided by two (IC71) to give 6.144 MHz which is used for the codec clock. The PLL synthesiser (IC75) divides the 5 MHz and the 11.2 MHz to produce 64 kHz signals (available at pins 13 and 3) which are the inputs to the phase detector.

24. Each PLL synthesiser produces a lock indication which is used to turn on the associated lock indicator LED, D15 and D16 via TR16 and TR17 respectively, and for BITE.

Variable Frequency IF Output (Sheet 6)

25. The analogue IF output can either be 1.4 MHz or variable in the range 10 kHz to 455 kHz, with the frequency set via the front-panel menu and the position of links LK4 and LK5.

26. To provide a 1.4 MHz IF output links LK4 and LK5 are set to position A, and the 1.4 MHz (from the DPRX ASIC/DAC) is routed straight to the analogue board.

27. For the variable IF output, links LK4 and LK5 are set to position B. The 1.4 MHz is then routed to the mixer (IC58) and mixed with the variable frequency oscillator output. This output is amplified (IC66) and then filtered by a 500 kHz low-pass filter to remove the unwanted mixer products.

28. The variable frequency oscillator is a phase locked loop that produces a signal in the range 1.41 MHz to 1.855 MHz. It is locked to the external 5 MHz reference using the PLL synthesiser (IC79) which divides the 5 MHz and the oscillator to produce 5 kHz signals which are the inputs to the phase detector. The divide ratios are programmed by the Control Processor, via a latch (IC78) to give the required oscillator frequency. The IF out of the DSPs is inverted for the variable IF output to compensate for the inversion in the mixer, so that the sidebands are on the correct side of the carrier.

DSP Parallel I/O (Sheet 6)

29. The DSP data bus has a 6-bit latch (IC76) for parallel output and a 6-bit buffer (IC60) for parallel input. The parallel outputs and parallel inputs are listed below:

(1) Parallel Outputs:

(a) Four lines are used to write to the frequency reference PLL synthesisers to set up the divide ratios.
(b) One line is used to drive the external IF valid line via a transistor (TR3), and also as an internal loopback for BITE.
(c) One line is used as a mute control to the analogue board, via an inverter (IC73) and an open-collector gate (IC42).

(2) Parallel Inputs:

(a) Three lines are connected to switches, two of which select whether DSP3 and DSP4 are fitted, the other is for future use.
(b) One line is for internal BITE loopback, from the parallel output latch.
(c) One line is to detect a mute of the analogue board.
(d) One line is an input from the analogue board (PTT_F) which is not used.

Control Processor Interface (Sheet 6)

30. The Control Processor interface, in addition to the host port of DSP1, consists of three 6-bit latches (IC78, 81 and 85) on the Control Processor data bus, for audio switching, DSP reset, variable IF output PLL control and FSK1 port direction. Another two control lines (and eight data lines) are used to program the multiplying DACs for the audio line level setting.

31. The reset line (from the reset controller) is gated with a line from the Control Processor data bus latch which allows the Control Processor to reset the DSPs without affecting the rest of the receiver or power supplies. The control processor can similarly control the NMI/MODC line of DSP1 and hence the type of bootstrap it carries out.

DSP Hardware BITE (Sheet 6)

32. The DSP hardware BITE signals available to the BITE multiplexer (IC65 on Sheet 8) are the audio power supplies, the 5 MHz reference input, the AGC control voltage, the two PLL lock detectors, and the analogue IF output level, which is measured by the level detector.

Power Supplies (Sheet 7)

33. Voltage regulators (IC49, IC28 and IC48) are provided for the +5 V_{if} and +5 V_{audio} (from the +15 V input) and -5 V_{if} (from the -15 V input) supplies. The -5 V_a supply is taken from the -5 V, with a series inductor (L1) to provide filtering. The +5 V_{ref} is generated from the +15 V input by voltage reference (IC41), which is used in the AGC control circuits to ensure the voltage is accurate.

Control Processor Section

Control Processor (Sheet 9)

34. This consists of a 68000 processor which is driven from an 8 MHz clock (XL2). The processor fetches data either from the input or memory devices, processes the information according to the program code stored in the EPROM, and then sends the results of these computations to an output or memory device.

35. The data bus is a 16-bit bi-directional bus, which is split into two bytes (D0 to D7 and D8 to D15). Each half of the data bus is buffered by a bi-directional data buffer (IC44 and IC45). These buffers may be disabled by SW1-8 for signature analysis. Data transfers are handled by signals on the control bus.

36. Five interrupt lines are used which are encoded by a priority encoder (IC38) as follows :-

    1 - Serial Ports (IC21) (Highest Priority)
    2 - Expansion Port
    3 - DSP Processor (IC64)
    4 - Programmable Timer (IC29)
    5 - Programmable Timer (IC11) (Lowest Priority)

Address Decoding (Sheet 9)

37. According to the state of address lines AA18 to AA22 the address decoder (IC27, IC33, IC35, IC37 and IC43) asserts the appropriate select line to allow the various on-board devices to communicate with the processor via the data bus. This ensures that only the relevant data is routed to and from these devices. During interrupts the address decoding is disabled (via IC37) by the 3-bit function code (FC0-3).

38. Address lines AA1 to AA17 form the address bus. This is used by the processor to address the memory and interface devices to allow data transfers via the data bus.

39. During data transfer, acknowledgment to the control processor that data transfer is completed is produced by the DTACK (data transfer acknowledge) counter (IC32 and IC36) to terminate the bus cycle. This ensures that the processor allows sufficient time to access devices on the bus.

Memory Devices (Sheet 9)

40. As well as providing storage for the main program, the EPROM (PD1) contains the BITE program which is initiated at power-up, returning to the normal program on completion of testing. Included within the main program are the continuous BITE tests which are performed automatically without operator intervention. Signature analysis routines are also held in this memory.

41. Non-volatile storage of operational settings is provided by the EEPROM (IC30), which requires no back-up supply. Data can be written into this memory when bit 7 of port B on the parallel interface timer (IC11 sheet 8) is driven active low. The current operational settings are updated if a change has occurred since they were last copied to the EEPROM, but only if they remain at these settings for more than one minute.

42. Two 32 K by 8 static RAM devices (IC15 and IC20) form the RAM store. In addition to storing the front panel settings, it also serves as working memory for the program. A capacitor-backed supply is provided (C12, Sheet 11) to provide short term data retention when the supply is switched off.

43. If for example, the power is momentarily interrupted, the front panel settings stored in the RAM are recalled when the power is restored. The data is checked and if it is uncorrupted, is used as the receivers operational settings. If the data in the RAM is corrupted, for example because the supply has been switched off for some time, the data is taken form the EEPROM. The reset generator (IC26 sheet 8) is used to disable the RAM on power-up, thus avoiding data corruption. In the event of the EEPROM also being corrupted then the default settings in the EPROM will be used.

Interface Devices (Sheet 8)

44. The processor is interfaced to other devices in the in the equipment through the use of parallel interface timer 1 (IC29). This bidirectional parallel interface provides a module bus for internal communication. It consists of an 8-bit address bus, an 8-bit data bus, read/write and strobe lines and lines for BITE and monitoring purposes. The strobe and read/write lines are looped back to enable them to be tested in BITE. This device also contains a timer to generate timing pulses for periodic events such as servicing the front panel shaft encoder, reading the keyboard or updating the displays.

45. A second bi-directional parallel interface is provided by parallel interface timer 2 (IC11). This mainly provides the interface to the rear panel for connection to external equipment. It is also used to read the status of the seven DIL test switches (SW1). As before, a timer is included in this device. This acts as a 'watchdog' timer, which applies a reset to the board (via IC42) unless it is regularly updated by the program.

46. The antenna lines on the rear panel and the LED indicators on the board are controlled via a 6-bit latch (IC10).

47. Interfacing with remotely-controlled equipment is performed by two serial I/O ports conforming to standard RS423-A and V10. Each port has two data lines (RX and TX) and two handshake lines (CTS and RTS) to synchronize data

transfers. Both ports are provided by a dual UART (IC21). A 3.6864 MHz clock is used to provide the baud rate timing. The dual UART converts the information on the data bus from the processor into a serial data stream and vice-versa.

48. The outputs of the UART are routed to the rear panel connections via differential line drivers and receivers (IC4, IC5 and IC6), which translate the logic levels to/from the UART to the RS423-A line levels. The TX data outputs may be disabled via the outputs on IC21.

BITE measurement System (Sheet 8)

49. The BITE measurement system allows the processor to measure supply voltages and check analogue levels within the equipment.

50. It comprises of an analogue multiplexer (IC65) and a 8-bite digital-to-analogue convertor (IC53). The DAC has a range of 0 to 2.55 V in 10 mV steps. The voltage to be measured is selected via the multiplexer, which is controlled by a latch (IC61). This selected voltage is then compared by the BITE comparator (IC62) with the test voltage set on the DAC.

51. To allow BITE measurements on other boards within the equipment, the DAC line is taken to a BITE comparator on each of the other boards. All comparator outputs are connected to an open-collector BITE line whose status can be read by the processor.

Link Configuration Switches (Sheet 10)

52. The settings for the serial links are defined by the switches SW2, SW3 and SW4. The switches can be read by the processor via the board data bus. Each switch bank can be enabled onto the data bus via the associated bus transceivers (IC50, IC51 and IC52) depending upon the address set on the board address bus. These switches are only read at power-up.

Test Facilities

53. The digital board switch bank SW1 provides access to various test facilities. The switches are set in accordance with the positions shown below for the desired operating mode.

Function Selected	SW1-1	SW1-5	SW1-6	SW1-7	SW1-8
Normal Operation	OFF	ON	ON	ON	ON
Receiver Default Set-up	OFF	OFF	ON	ON	ON
Signature Analysis	ON*	ON*	ON*	OFF	ON
Processor Free-run	ON	ON	ON	ON	OFF
Enable Config. Menus	ON	ON	ON	ON	ON

54. Switches SW1-2 to SW1-4 normally have no significance. However, if signature analysis has been entered (SW1-7 to OFF), switches SW1-1 to SW1-6 are used to select the required signature analysis routine.

55. Switch 8 on SW1 is normally set to ON; when set to OFF, the processor operates in a free-run mode, where the processor is isolated from the rest of the circuit and a test data word is used to instruct the processor to execute a one-word instruction. This instruction is continually stepped through the entire address range to create a repetitive data pattern, which enables signature analysis to be performed on the processor and associated circuitry.

Board Connections (*see the Interface Handbook for external connections*).

Front-Panel Connector PL2

56. This is a 40-way DIL plug. It is used with 'user' front panels only. A dual receiver will use this connector on receiver 1 digital board only. The connections are listed in Table 1.

Blank Front Panel Audio/Dual Receiver Digital Board Connector PL3

57. This is a 26-way DIL plug which is used in a dual receiver and for a blank front-panel receiver. The connections are listed in Table 2.

Analogue Board Connector PL4

58. The connections for this 50-way DIL plug are listed in table 3.

External Interface Board Connector PL5

59. This is a 40-way DIL plug which is only used when an external interface board is present. The connections are listed in Table 4.

Table 1: PL2 Connections

Pin	Signal	Description
1	0V	0 Volts
2	0V	0 Volts
3	BA0	Board Address Bus Bit 0
4	BA1	Board Address Bus Bit 1
5	BA2	Board Address Bus Bit 2
6	BA3	Board Address Bus Bit 3
7	BA4	Board Address Bus Bit 4
8	BA5	Board Address Bus Bit 5
9	BA6	Board Address Bus Bit 6
10	BA7	Board Address Bus Bit 7
11	BSTB	Board Strobe
12	BR/W	Board Read/Write
13	BD0	Board Data Bus Bit 0
14	BD1	Board Data Bus Bit 1
15	BD2	Board Data Bus Bit 2
16	BD3	Board Data Bus Bit 3
17	BD4	Board Data Bus Bit 4
18	BD5	Board Data Bus Bit 5
19	BD6	Board Data Bus Bit 6
20	BD7	Board Data Bus Bit 7
21	BITE	BITE Comparator input
22	DAC	Bite DAC output line
23	(R)	Reset
24	Spare1	General Purpose Control, not currently used
25	Spare2	General Purpose Control, not currently used
26	Spare3	General Purpose Control, not currently used
27	PTT_F	Press To Talk (PTT)
28	AUDOP	Front panel audio output
29	MIC	Microphone input
30	0VA	Audio ground
31	LSP	Loudspeaker
32	LSGND	Loudspeaker ground
33	-15V	-15 Volts
34	-15V	-15 Volts
35	+15V	+15 Volts
36	+15V	+15 Volts
37	+5V	+5 Volts
38	+5V	+5 Volts
39	0V	0 Volts
40	0V	0 Volts

Table 2: PL3 Connections

Pin	Signal	Description
1	+15 V	+15 Volts headphone supply
2	AUDOP	Headphone audio
3	FAULT LED	Fault Led
4	LSP	Loudspeaker
5	LSGND	Loudspeaker ground
6	TRAN1	FSK/Diversity AGC input common
7	FSK2	FSK input
8	AGCIP	Diversity AGC input
9	0VA	Monitor Audio ground
10	TRAN2	External Audio input
11	FAULT I/O	Fault line
12	TXDATA	Transmit data output
13	TX COMMON	Transmit data common
14	RXCOM	Receive data common
15	RXDATA	Receive data input
16	FAULT I/O	Fault line
17	MON_AUD	Monitor audio output
18	0VA	Monitor audio ground
19	AGCOP	Diversity AGC output
20	FSK1	FSK output
21	0V	FSK/Diversity AGC common
22		Not used
23		Not used
24		Not used
25		Not used
26		Not used

Table 3: PL4 Connections

Pin	Signal	Description
1	0V	0 Volts
2	0V	0 Volts
3	BA0	Board Address Bus Bit 0
4	BA1	Board Address Bus Bit 1
5	BA2	Board Address Bus Bit 2
6	BA3	Board Address Bus Bit 3
7	BA4	Board Address Bus Bit 4
8	BA5	Board Address Bus Bit 5
9	BA6	Board Address Bus Bit 6
10	BA7	Board Address Bus Bit 7

Table 3: PL4 Connections (continued)

Pin	Signal	Description
11	BSTB	Board Strobe
12	BR/W	Board Read/Write
13	BD0	Board Data Bus Bit 0
14	BD1	Board Data Bus Bit 1
15	BD2	Board Data Bus Bit 2
16	BD3	Board Data Bus Bit 3
17	BD4	Board Data Bus Bit 4
18	BD5	Board Data Bus Bit 5
19	BD6	Board Data Bus Bit 6
20	BD7	Board Data Bus Bit 7
21	BITE	BITE Comparator input
22	DAC	Bite DAC output line
23	(R)	Reset
24	Spare1	General Purpose Control, not currently used
25	Spare2	General Purpose Control, not currently used
26	Spare3	General Purpose Control, not currently used
27	PTT_F	Press To Talk (PTT)
28	Mute	Mute output
29	Overload	Receiver overload (input)
30		Not connected
31		Not connected
32		Not connected
33	-15V	-15 Volts (filtered)
34	-15V	-15 Volts (filtered)
35	+15V	+15 Volts (filtered)
36	+15V	+15 Volts (filtered)
37	+5V	+5 Volts (filtered)
38	+5V	+5 Volts (filtered)
39	0V	0 Volts (filtered)
40	0V	0 Volts (filtered)
41	AGC	Analogue board gain control voltage (output)
42	0V	0 volts
43	IFIP+	Balanced IF input signal (+ side)
44	0V	0 volts
45	IFIP-	Balanced IF input signal (- side)
46	0V	0 volts
47	5M_REF	5 MHz reference input
48	0V	0 volts
49	IFOP	Analogue IF output
50	0V	0 volts

Table 4: PL5 Connections

Pin	Signal	Description
1	0V	0 Volts
2	0V	0 Volts
3	AA1	Control Processor Address Bus Line 1
4	AA2	Control Processor Address Bus Line 2
5	AA3	Control Processor Address Bus Line 3
6	AA4	Control Processor Address Bus Line 4
7	AA5	Control Processor Address Bus Line 5
8		8 MHz Clock
9	CLK1	8 MHz Clock
10	AS1	Address Strobe
11	R/(W)	Read/Write Bar
12	(R)/W	Read Bar/Write
13	D0	Control Processor Data Bus Bit 0
14	D1	Control Processor Data Bus Bit 1
15	D2	Control Processor Data Bus Bit 2
16	D3	Control Processor Data Bus Bit 3
17	D4	Control Processor Data Bus Bit 4
18	D5	Control Processor Data Bus Bit 5
19	D6	Control Processor Data Bus Bit 6
20	D7	Control Processor Data Bus Bit 7
21	LDS1	Lower data Strobe
22	E1	Control Processor device enable
23	VMA1	Control Processor device valid memory address
24	(R)	Reset
25	CS1	Chip Select 1 for Control Processor Devices
26	CS2	Chip Select 2
27	CS3	Chip select 3
28	I3	Interrupt Line (I3)
29		Not connected
30		Not connected
31		Not connected
32		Not connected
33	-15V	-15 Volts
34	-15V	-15 Volts
35	+15V	+15 Volts
36	+15V	+15 Volts
37	+5V	+5 Volts
38	+5V	+5 Volts
39	0V	0 Volts
40	0V	0 Volts

Digital Board Power Supply Connections

60.

P1	0 volts
P2	0 volts
P3	+ 5 Volts
P4	+ 5 Volts
P5	+ 15 volts
P6	- 15 volts

FAULT LOCATION

61. Fault location techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the digital board is given in the following paragraphs.

BITE Tests

Test No 001 Control Processor EPROM Checksum

62. This test performs a 16 bit checksum on the EPROM (PD1) for the control processor. This test is run at power-up only.

Test No 002 Control Processor RAM Even Bytes

63. This test performs the following test on the first 16K Bytes of the control processor RAM (IC15 and IC20), even addressed Bytes: All 0's, all 1's, walking 0's, walking 1's and (except at power-up) a test of the independence of the address lines. This test is available at all levels except continuous.

Test No 003 Control Processor RAM Odd Bytes

64. As detailed for test 002, but for the first 16K Bytes, odd addressed Bytes, of control processor RAM.

Test No 004 EEROM Test

65. This test checks the data residing in the EEROM (IC30) against the corresponding checksums. This test is run as a continuous test only.

Test No 005 +5 V Digital Rail

66. The +5 V rail on the digital board is checked to be within the limits 1.74 volts to 1.39 volts. This test is available at all levels except power up.

Test No 006 +15 V Rail

67. The +15 V rail on the digital board is checked to be within the limits 1.53 volts to 1.18 volts. This test is available at all levels except power up.

Test No 007 -15V Rail

68. The -15 V rail on the digital board is checked to be within the limits 1.80 volts to 0.88 volts. This test is available at all levels except power up.

Test No 008 -5 V Rail

69. The -5 V rail on the digital board is checked to be within the limits 2.26 to 1.44 volts. This test is available at all levels except power up.

Test No 009 Digital Board I/O

70. This test simply produces a ramp on the DAC (IC53) output, toggles the antenna, COR, fault and parallel I/O line outputs. The test will always pass - it is intended for fault finding with the use of additional test gear. This test is available as a select test only.

Test No 010 Parallel I/O

71. This test checks the parallel I/O signal lines to the 15-way connectors (PL1 and SK5) on the Digital Board. It requires the use of the external parallel loopback connector to interconnect the following:

Input	Output
Frequency Strobe (PL1-12)	Antenna 0 (SK5-12)
Scan Inhibit (PL1-13)	Antenna 1 (SK5-13)
External Mute (PL1-14)	Antenna 2 (SK5-14)
Dump (PL1-15)	Antenna 3 (SK5-15)
Fault (SK5-11)	COR (SK4-18)

72. All combinations of bits are tested to ensure all lines can be driven and read correctly and there is no cross-talk. This test is available as a select test only.

RX Configuration Serial Receiver.

73. These tests are only available on a receiver which is configured as an ASCII controlled equipment.

(1) **Test No 051 Master/Auxiliary Port Internal**

Performs an internal loopback test on the master port. A test pattern consisting of all characters that may be transmitted is output. The pattern should be read back as transmitted. The link is tested at all possible baud rates. This test is available as a select test only.

(2) **Test No 052 Master/Auxiliary Port External**

This test is similar to the test detailed in test 051 but the internal loopback mode is not used. Rather, an external loopback connector is required on SK5 as follows:

Data output (pin 2) to data input (pin 3)
CTR/RTS (pin 4) to CTS (pin 5).
Receive common (pin 6) to Transmit common (pin 7).

Note: All connections refer to master port pins.

(3) **Test No 053 Tributary Port Internal**

As test 051 but for the tributary port.

(4) **Test No 054 Tributary port External**

As detailed in test 052 but for the tributary port. (All connections refer to tributary port pins on PL1).

(5) **Test No 055 Diversity Master Link**

Checks the link to a diversity slave if applicable is operational. This test is run as a continuous test only.

74. **RX Bus**

(1) **Test No 101 RX Data Bus**

Checks that PI/T 1 (IC29) (the parallel interface to the receiver boards) can drive the data bus. A walking '1' pattern is placed on the data bus and read back into the PI/T such that instantaneous levels are obtained. Short circuits on the data bus are detected by this method. This test is used during power up, select, or unit test.

(2) **Test No 102 RX Address Bus**

As detailed in test 101, but checks out the Receiver address bus.

(3) **Test No 103 RX Bus Control**

Checks the signals used to control the flow of data on the RX bus. The RX bus strobe line is checked by reading it at the RX bus R/W line and vice versa. This test is used during power up, select, or unit test.

(4) **Test No 104 RX BITE Bus**

This test checks that no board asserts the BITE line when all the multiplexer have been deselected. The DAC voltage is set to 100 mV, so that even a low voltage at a board multiplexer would be detected. This test is used during power up, select, or unit test.

75. **Test No 201 +5V Analogue Rail**

The +5 volt analogue rail on the digital board is checked to be within the limits 2.26 to 1.44 volts. This test is run at all levels except power up.

76. **Test No 202 Reference Input Level**

Checks that the 5 MHz reference input level is within the limits 0.5 to 1.9 volts. This test is run at all levels except power up.

Test No 203 Reference Lock 1

77. Checks that the reference loop 1 is in lock at the operating frequency. The in-lock voltage is within the limits 1.0 to 2.55 volts. This test is run at all levels except power up.

Test No 204 Reference Lock 2

78. As for detailed in test 203 but tests reference loop 2.

Test No 205 Board Interface

79. Checks that the receiver processor can communicate with the DSP processor. If the test fails the DSP is reset and updated it with its correct operating conditions, thereby allowing the receiver to continue to operate normally. This test is run at all levels except power up.

Test No 206 DSP EPROM Checksum

80. Checks that the checksum for the DSP eprom (PD7) is correct. This test is available as a select or unit test.

81. **Test No 207 DSP RAM Test High**

Checks that the high DSP RAM (IC89) is working. This test is available as a select or unit test.

82. **Test No 208 DSP RAM Test Mid**

Checks that the mid DSP RAM (IC87) is working. This test is available as a select or unit test.

83. **Test No 209 DSP RAM Test Low**

Checks that the low DSP RAM (IC84) is working. This test is available as a select or unit test.

84. **Test No 210 DSP Reset**

Checks that the Control Processor can reset the DSP. The DSP is reset by writing a logic to 1 followed by a logic 0 to bit 0 on port 1 on the digital board. This test is available as a select or unit test.

85. **Test No 211 DPRX ASIC Test**

Checks that the DPRX ASIC (IC86) can be controlled, that its clock and IRQA interrupt divider and output are working. It measures the 80 kHz IRQA rate, which can be examined at IC88 pin 3. This test is available as a select or unit test.

86. **Test No 212 Sample Rate Clock Test**

Checks that the ASIC interrupt B divider and output are working. It measures the 16 kHz IRQB rate, which can be examined on IC77, pin 3. This test is available as a select or unit test.

87. **Test No 213 Peak Detector Level Test**

This test checks the attenuated 32 kHz IF level measured by the peak detector (IC69 and PD2) is correct. This test is available as a select or unit test.

88. **Test No 214 Input level/Peak Detector Test**

This test checks the difference in IF level between the peak detector and sigma-delta ADC (IC59) paths. This test is available as a select or unit test.

89. **Test No 215 IF SNR Test**

Checks that the SNR for the receiver is within specification. This test is available as a select or unit test.

90. **Test No 216 ADC Sampling Clock Lock Test**

Checks that the 12.288 MHz ADC clock is locked to the receiver LO (via the 5 MHz reference). The test is available as a select or unit test.

91. **Test No 217 AGC Voltage Test**

This test checks that the front-end AGC control voltage (at IC54 pin 6) can be set to its minimum and maximum levels. The receiver is set to manual AGC with the front-end muted. The receiver gain is set to maximum and the front-end AGC control voltage checked to be within the limits 2.18 to 2.47 volts. The receiver gain is then set to minimum and the front-end AGC control voltage checked to be within the limits 0 to 0.2 volts. This test is available as a select or unit test.

92. **Test No 218 DSP1 IRQA Test**

This test checks that DSP2 (on PC3/2) is able to write to DSP1s IRQA input. This test is available as a select or unit test.

93. **Test No 219 Data Bus Parallel I/O Test**

Checks the DSP parallel data latch (IC76) and buffer (IC60) by toggling the internal loopback line between them. This test is available as a select or unit test.

94. **Test No 220 CODEC 1 Control Test**

Checks CODEC 1 (IC22) clock, dividers and digital interface, by measuring the 16 kHz frame sync which can be examined at IC67 pin 2. This test is available as a select or unit test.

95. **Test No 221 CODEC/Multiplying DAC 1 Level Test**

Checks the gain through CODEC 1 (IC22) and DAC 1 (IC24) by routing the DAC output (at IC18 pin 7) to the CODEC 1 auxiliary input, via IC19-a, IC2-c and IC19-b. This test is available as a select or unit test.

96. **Test No 222 CODEC/Multiplying DAC 1 SINAD Test**

Checks linearity and noise through CODEC 1 and DAC1 audio path (with the same routing as test 221). This test is available as a select or unit test.

97. **Test No 223 Internal Audio Level Test**

Checks the internal audio level, by routing the audio output (IC12 pin 6) to CODEC 1 input, via IC2-a, IC8-a, IC8-c, IC24, IC25, IC17-a, IC8-b and IC17-b. This test is available as a select test only.

98. **Test No 224 Internal Audio Output SINAD Test**

Checks internal audio SINAD (with the same routing as test 223). This test is available as a select or unit test.

99. **Test No 225 Multiplying DAC 2 Level Test**

Checks the level through CODEC 1 (IC22) and DAC 2 (IC24) audio path, by routing the DAC 2 output (at IC25 pin 7) to the CODEC 1 input via IC17-a, IC8-b and IC17-b. This test is available as a select or unit test only.

100. **Test No 226 Multiplying DAC 2 SINAD Test**

Checks linearity and noise through CODEC 1 and DAC 2 audio path (with the same routing as test 225). This test is available in select or unit test.

101. **Test No 227 IF Valid Line Loopback Test**

This test checks the IF valid line output and requires a loopback connector between PL1 pins 11 and 14. This test is available as a select test only.

102. **Test No 228 External AGC Loopback Test**

This test checks the AGC line driver (IC14) and receiver (IC9) and the SCI of DSP2. It requires an external loopback connector between SK4 pins 7 and 19 and link LK7 to be in position B. This test is available as select test only.

103. **Test No 229 Audio Line 1 Level Test**

This test checks the gain of the audio path through CODEC 1 (IC22), DAC 1 (IC24) and line driver. This test requires link LK1 in position A, link LK2 in position B and an external loopback connector as below on SK4 :-

Pins 1 and 16
Pins 2 and 3
Pins 14 and 15

The audio line output is routed back to the CODEC 1 input via the loopback connector and DAC 2. This test is available as select test only.

104. **Test No 230 Audio Line 1 IMD Test**

Checks the line 1 IMD, requires links LK1 and LK2 set and an external loopback connector as detailed in test 229. This test is available as select test only.

105. **Test No 231 Audio Line 2 Level Test**

Checks the gain of the line 2 audio path through CODEC 1 (IC22), DAC 2 (IC24) and line driver. This test requires link LK1 in position B, link LK2 in position A and an external loopback connector as below on SK4 :-

Pins 1 and 16
Pins 2 and 3
Pins 14 and 15

The audio line output is routed back to the CODEC 1 input via the loopback connector and DAC 1. This test is available as select test only.

106. **Test No 232 Audio Line 2 IMD Test**

Checks the line 2 IMD, requires links LK1 and LK2 set and an external loopback connector as detailed in test 231. This test is available as select test only.

107. **Test No 233 IF Output Level Detector Test**

This test checks the IF output level detector. The IF output level detector is selected and the level checked to be within the limits 1.0 to 2.0 volts. This test is available as a select test or a unit test.

108. **Test No 234 IF Output IMD Test**

This checks the 1.4 MHz IF output by feeding it via an external loopback connector to the antenna input. Links LK4 and LK5 must be set to position A. The receiver is automatically tuned to 1.4 MHz, a two-tone 1.4 MHz output is generated and fed back to the DSPs via the RF input path. This test is available as select test only.

ISB Option Tests

109. These tests are only available if the ISB option is fitted.

Test No 301 CODEC 2 Control Test

This tests that the CODEC 2 clock, dividers and digital interface are operating. This test is available in select or unit test.

Test No 302 CODEC 2 SINAD Test

This test checks CODEC 2 audio path. This test is available in select or unit BITE.

FSK Tests

110. **Test No 351 FSK Loopback Test**

This test checks the FSK1 line driver. This test is available in select test only. An external loopback connector should be fitted between SK4 pins 8 and 20.

Note: MA3790 Exclusion: Test 351 is NOT available on the MA3790.

Digital IF Option Tests

111. These tests are only available if the Digital IF option is fitted.

Test No 401 SSI Data Line Test

This test checks the digital IF/AF SSI. This test is available in select or unit BITE. An external loopback connector should be fitted to SK4 as below:-

Pins 11 and 12
Pins 23 and 24

Test No 402 SSI Sync Line Loopback Test

112. This test checks the digital IF/AF SSI strobe driver. This test is available as a select test only. An external loopback connector as detailed below should be fitted to SK:-

Pins 10 and 11
Pins 22 and 23

SIGNATURE ANALYSIS ROUTINES

113. **IMPORTANT:** For all of the following routines the front panel and analogue boards (if fitted) should be disconnected from the digital board.

Control Processor Signature Analysis Tests

Routine Free Run

114. This routine checks the fundamental operation of the 68000 processor address bus and address decoding.

Digital board SW1 DIL switch settings:

8	OFF
1-7	ON

Signature analyser connections and settings:

Start:	TP22 negative trigger
Stop:	TP22 negative trigger
Clock:	TP2 positive trigger
Earth:	TP5

Table 5: Routine Free Run

Signal	Signature	Test Node
+5V	C565	IC34/14
0V	0000	IC34/56
CLK	C565	XL2/3 IC36/2 IC32/3
AS	6544	PL5/10 TP3 IC32/5 IC33/4 IC34/6 IC35/1
UDS	6544	IC35/10 IC39/9 IC34/7
LDS	6544	PL5/21 IC35/4 IC39/1 IC39/13 IC34/8
R/(W)	C565	PL5/11 IC44/1 IC32/1 IC39/5 IC39/10 IC39/12 IC34/9 IC29/47 IC11/47 IC21/9 IC45/1 IC64/12
(R)/W	0000	PL5/12 IC32/2 IC20/22 PD1/20 IC30/25 IC15/22
RESET	C565	PL2/23 PL5/24 PL4/23 IC78/1 IC85/1 IC42/8 IC77/5 IC76/1 IC36/1 IC34/19 IC34/20 IC29/43 IC21/38 IC81/1
IPL0	C565	IC34/25 IC38/6
IPL1	C565	IC34/26 IC38/7
IPL2	C565	IC34/27 IC38/9
IC38/11	C565	IC38/11 IC11/39
IC38/12	C565	IC38/12 IC29/37 IC29/29
IC38/13	C565	IC38/13 IC64/13
IC38/1	C565	IC38/1 PL5/28
IC38/2	C565	IC38/2 IC21/24
FC0	0000	IC34/30 IC37/1
FC1	C565	IC34/29 IC37/2
FC2	C565	IC34/28 IC37/13
IC37/12	C565	IC27/13 IC33/6 IC37/12
VPA	644C	IC35/3 IC36/7 IC34/23
IC35/2	644C	IC35/2 IC27/11
VMA	3AP2	PL5/23 IC34/21
AA1	UCA1	PL3/3 IC20/10 PD1/21 IC34/32 IC29/32 IC11/32 IC21/2 IC30/11 IC64/7 IC15/10
AA2	H7H7	PL5/4 IC20/9 PD1/22 IC34/33 IC29/31 IC11/31 IC21/4 IC30/10 IC64/6 IC15/9
AA3	4006	PL5/5 IC20/8 PD1/23 IC34/34 IC29/30 IC 11/30 IC21/6 IC30/9 IC64/4 IC15/8
AA4	5870	PL5/6 IC20/7 PD1/24 IC34/35 IC29/29 IC11/29 IC21/7 IC30/8 IC15/7
AA5	8464	PL5/7 IC20/6 PD1/25 IC34/36 IC29/28 IC11/28 IC30/7 IC15/6
AA6	CF69	IC20/5 PD1/26 IC34/37 IC30/6 IC15/5
AA7	32P8	IC20/4 PCD1/27 IC34/38 IC30/5 IC15/4

Table 5: Routine Free Run (cont.)

Signal	Signature	Test Node
AA8	C4A3	IC20/3 PD1/28 IC34/39 IC30/4 IC15/3
AA9	0PH3	IC20/25 PD1/29 IC34/40 IC30/329 IC15/25
AA10	1A0H	IC20/24 PD1/31 IC34/41 IC30/28 IC15/24
AA11	8P92	IC20/21 PD1/32 IC34/42 IC30/24 IC15/21
AA12	UP27	IC20/23 PD1/33 IC34/43 IC30/27 IC15/23
AA13	8938	IC20/2 PD1/34 IC34/44 IC30/3 IC15/2
AA14	F5CF	IC20/26 PD1/35 IC34/45 IC15/26
AA15	H5UF	IC20/1 PD1/36 IC34/46 IC15/1
AA16	5745	PD1/37 IC34/47
AA17	UCA1	PD1/38 IC34/48
AA18	H7H7	IC43/2 IC43/14 IC34/49
AA19	4006	IC34/50 IC43/3 IC43/13
AA20	5870	IC34/51 IC33/1
AA21	6401	IC34/53 IC33/2
AA22	U364	IC34/54 IC33/3
AA23	7U6P	IC36/3 IC34/55
DTACK	5CCH	IC32/8 IC34/10
IC32/6	H021	IC32/6 IC36/9
RAM WE(L)	C565	IC39/11 IC15/27
RAM WE(H)	C565	IC39/8 IC20/27
PD1 CE	P7A8	PD1/2 IC33/15
EEPROM CE	970F	IC33/13 IC30/23
RAM CE	21H4	IC33/12 IC36/13 IC42/11 IC42/12 IC42/13 IC15/20 IC20/20
PIT1 CE	6525	IC43/12 IC29/45
PIT2 CE	6525	IC43/4 IC11/45
LATCH CE	138P	IC43/10 IC10/9
UART CE	7829	IC43/11 IC21/39
DAC CE	FP75	IC53/4 IC43/7
DSP CE	FP75	IC43/9 IC64/10
IC33/11	7592	IC33/11 IC35/5 IC35/9
IC35/6	7592	IC35/6 IC43/1
IC35/8	7592	IC35/8 IC43/15
IC33/7	080A	IC33/7 PL5/27
IC33/9	1H8U	IC33/9 PL5/26
IC33/10	644C	PL5/25 IC27/12 IC33/10

ROUTINE 0

115. This checks the RAM and the data read into the 68000 processor via the data buffer.

Digital board SW1 DIL switch settings: 7 OFF
1-6, 8 ON

Signature analyser connection and settings:

Start: TP4 negative trigger
Stop: TP4 negative trigger
Clock: TP3 positive trigger
Earth: TP5

Note: The gating period is approximately 5 seconds for this test, therefore allow sufficient time for signatures to settle before taking result.

Table 6: Routine 0

Signal	Signature	Test Node
RAM +5V	2P72	IC15/28 IC20/28
RAM 0V	0000	IC15/14 IC20/14
CE	A041	IC33/12 IC36/13 IC42/11 IC42/12 IC42/13 IC15/20 IC20/20
OE	783A	IC32/2 IC20/22 IC15/22
WE(L)	7AH9	IC39/11 IC15/27
WE(H)	5648	IC39/8 IC20/27
D0	485P	IC15/11 IC45/2 IC45/18 IC34/5
D1	5UH3	IC15/12 IC45/3 IC45/17 IC34/4
D2	8312	IC15/13 IC45/4 IC45/16 IC34/3
D3	7580	IC15/15 IC45/5 IC45/15 IC34/2
D4	FF30	IC15/16 IC45/6 IC45/14 IC34/1
D5	9UP1	IC15/17 IC45/7 IC45/13 IC34/68
D6	UP9F	IC15/18 IC45/8 IC45.12 IC34/67
D7	25CU	IC15/19 IC45/9 IC45/11 IC34/66
D8	5H7P	IC20/11 IC44/2 IC44/18 IC34/65
D9	F016	IC20/12 IC44/3 IC44/17 IC34/64
D10	8656	IC20/13 IC44/4 IC44/16 IC34/63
D11	2910	IC20/15 IC44/5 IC44/15 IC34/62
D12	538H	IC20/16 IC44/6 IC44/14 IC32/61
D13	U620	IC20/17 IC44/7 IC44/13 IC32/60
D14	4H30	IC20/18 IC44/8 IC44/12 IC32/59
D15	9606	IC20/19 IC44/9 IC44/11 IC32/58

ROUTINE 1

116. This routine checks the LED display and antenna lines latch.

Digital board SW1 DIL switch settings: 1,7 OFF
2-6, 8 ON

Signature analyser connection and settings:

Start: TP4 negative trigger
Stop: TP4 negative trigger
Clock: TP3 positive trigger
Earth: TP5

Table 7: Routine 1

Signal	Signature	Test Node
+5V	5UAH	IC10/1 IC10/16
0V	0000	IC10/8
UDS	U07C	IC34/7 IC35/10
IC35/8	5333	IC35/8 IC43/15
LATCH CS	5333	IC10/9 IC43/10
ANT 0	2128	IC10/2
ANT 1	U267	IC10/5
ANT 2	1FUH	IC10/7
ANT 3	PC89	IC10/10
LED 1	9F32	IC10/12
LED 2	HU8U	IC10/15

ROUTINE 2

117. This routine checks the EEPROM.

WARNING: The contents of the EEPROM will be corrupted when this test is run.

Digital board SW1 DIL switch settings: 2, 7 OFF
1,3-6,8 ON

Signature analyser connection and settings:

Start: TP4 negative trigger
Stop: TP4 negative trigger
Clock: TP3 positive trigger
Earth: TP5

Table 8: Routine 2

Signal	Signature	Test Node
+5V	481P	IC30/32
0V	0000	IC30/16
CE	2P2F	IC33/13 IC30/23
D0	09CP	IC30/13
D1	8PP4	IC30/14
D2	8A11	IC30/15
D3	159F	IC30/18
D4	U49U	IC30/19
D5	1354	IC30/20
D6	3UHU	IC30/21
D7	85FH	IC30/22

ROUTINE 3

118. This routine checks parallel interface provided by PIT1.

Digital board SW1 DIL switch settings: 1-2, 7 OFF
3-6, 8 ON

Signature analyser connection and settings:

Start: TP4 negative trigger
Stop: TP4 negative trigger
Clock: TP3 positive trigger
Earth: TP5

Table 9: Routine 3

Signal	Signature	Test Node
+5V	5826	IC29/13
0V	0000	IC29/42
CE	3349	IC29/45 IC43/12
RESET	5826	IC29/43
R/W	6176	IC29/47
PIRQ	5826	IC29/39
D8	FF8U	IC29/48
D9	910P	IC29/49
D10	9890	IC29/50
D11	H808	IC29/51

Table 9: Routine 3 (cont.)

Signal	Signature	Test Node
D12	P5AH	IC29/52
D13	7P82	IC29/1
D14	C8A2	IC29/2
D15	1A0C	IC29/3
A1	PP26	IC29/32
A2	9749	IC29/31
A3	2218	IC29/30
A4	FPU2	IC29/29
A5	39PH	IC29/28
PC0	7C80	IC29/34 IC32/11
PC1	2530	IC29/35 IC32/13
BRW	7H16	PL2/12 PL4/12 IC32/12
BSTB	23A6	PL2/11 PL4/11 IC32/10
BD0	26A3	PL2/13 PL4/13 IC29/18
BD1	U5PF	PL2/14 PL4/14 IC29/19
BD2	1C76	PL2/15 PL4/15 IC29/22
BD3	PF02	PL2/16 PL4/16 IC29/23
BD4	9CC9	PL2/17 PL4/17 IC29/24
BD5	H804	PL2/18 PL4/18 IC29/25
BD6	A219	PL2/19 PL4/19 IC29/26
BD7	9HC9	PL2/20 PL4/20 IC29/27
BA0	72F4	PL2/3 PL4/3 IC29/4
BA1	2UH5	PL2/4 PL4/4 IC29/5
BA2	2H3H	PL2/5 PL4/5 IC29/6
BA3	4H2A	PL2/6 PL4/6 IC29/7
BA4	C538	PL2/7 PL4/7 IC29/9
BA5	9A72	PL2/8 PL4/8 IC29/10
BA6	4090	PL2/9 PL4/9 IC29/11
BA7	0AUA	PL2/10 PL4/10 IC29/12

ROUTINE 4

119. This routine checks data lines to the DAC.

Digital board SW1 DIL switch settings:

3, 7	OFF
1-2, 4-6, 8	ON

Signature analyser connection and settings:

Start:	TP4 negative trigger
Stop:	TP4 negative trigger
Clock:	TP3 positive trigger
Earth:	TP5

Table 10: Routine 4

Signal	Signature	Test Node
+5V	7FC2	IC53/10
0V	0000	IC53/9
CE	702F	IC53/4
D0	H497	IC53/2
D1	U41U	IC53/1
D2	41F5	IC53/16
D3	7P7P	IC53/15
D4	14AA	IC53/14
D5	9AC1	IC53/13
D6	CAHP	IC53/12
D7	H8C1	IC53/11

ROUTINE 5

120. This routine checks PIT2 watchdog timer/reset and PIT1 event timer.

Digital board SW1 DIL switch settings:

1, 3, 7	OFF
2, 4-6, 8	ON

Signature analyser connection and settings:

Start:	TP23 negative trigger
Stop:	TP23 negative trigger
Clock:	TP3 positive trigger
Earth:	TP5

Table 11: Routine 5

Signal	Signature	Test Node
+5V	6204	IC11/13
0V	0000	IC11/42
D0	855C	IC11/48
D1	5P25	IC11/49
D2	8C36	IC11/50
D3	205C	IC11/51
D4	U930	IC11/52
D5	0PA6	IC11/1
D6	A004	IC11/2
D7	P24A	IC11/3
A1	F4P3	IC11/32
A2	00CU	IC11/31
A3	H9U0	IC11/30
A4	438C	IC11/29
A5	04H5	IC11/28
I0	6204	IC11/39 IC38/11
I1	5486	IC38/12
I2	6204	IC38/13
I3	6204	IC38/1
I4	6204	IC38/2
IC38/9	6204	IC34/27 IC38/9
IC38/7	5486	IC34/26 IC38/7
IC38/6	6204	IC34/25 IC38/6
TOUT	3102	IC11/37 IC42/10
RESET	1881	IC42/8 IC34/19 IC34/20

ROUTINE 6

121. This routine checks data lines to the dual UART.

Digital board SW1 DIL switch settings:

2-3, 7	OFF
1, 4-6, 8	ON

Signature analyser connection and settings:

Start:	TP4 negative trigger
Stop:	TP4 negative trigger
Clock:	TP3 positive trigger
Earth:	TP5

Table 12: Routine 6

Signal	Signature	Test Node
+5V	6FP6	IC21/44
0V	0000	IC21/22
CE	F2AP	IC21/39 IC43/11
R/W	0A19	IC21/9
D8	PP4H	IC21/28
D9	7FA3	IC21/18
D10	7FA3	IC21/27
D11	1PAC	IC21/19
D12	AC55	IC21/26
D13	8FFH	IC21/20
D14	447A	IC21/25
D15	0010	IC21/21
OP0	C66A	IC21/32
OP1	C563	IC21/14
OP2	FHAH	IC21/31
OP3	C5C3	IC21/15

ROUTINE 7

122. This routine checks the ports on the digital board connected to the receiver control bus.

Set the switches on the digital board as follows:

SW1:	1, 2, 3, 7	OFF
	4-6, 8	ON
SW2:	2, 4	OFF
	1, 3	ON

Leave switches 5-8 in the present positions; these are used by the DSP's.

SW3:	1, 3, 5, 7	OFF
	2, 4, 6, 8	ON
SW4:	2, 4, 6, 8	OFF
	1, 3, 5, 7	ON

Signature analyser connection and settings:

Start:	PL4-9 negative trigger
Stop:	PL4-9 negative trigger
Clock:	PL4-11 positive trigger
Earth:	TP5

Note: Signatures xxxxF signify a flashing probe indicator.

Table 13: Routine 7

Signal	Signature	Test Node
+5V	PCP5	IC46/16
0V	0000	IC46/8
BD0	HU6U	IC78/3 IC85/3 IC61/3 IC51/18 IC29/18 IC81/3 IC52/18 IC29/4 IC50/18
BD1	AF3P	IC78/4 IC85/4 IC61/4 IC51/16 IC29/19 IC81/4 IC52/16 IC24/10 IC50/16
BD2	1596	IC78/6 IC8/6 IC61/6 IC51/14 IC29/22 IC81/6 IC52/14 IC24/1 IC50/14
BD3	4942	IC78/11 IC85/11 IC61/11 IC51/12 IC29/23 IC81/11 IC52/12 IC24/12 IC50/12
BD4	6728	IC78/13 IC85/13 IC61/3 IC51/9 IC29/24 IC81/13 IC52/9 IC24/13
BD5	U01H	IC78/14 IC85/14 IC61/14 IC51/7 IC29/25 IC81/14 IC52/7 IC24/14
BD6	3C87	IC51/5 IC29/26 IC52/5 IC24/25
BD7	PCP5	IC51/13 IC29/27 IC52/3 IC24/16
BSTB	0000F	IC32/10 IC47/5
BRW	0000F	IC32/12 IC39/9 IC37/10 IC37/11 IC47/4
BA0	HA04	IC40/1 IC29/4 IC47/1 IC24/17
BA1	HU56	IC40/2 IC29/5 IC47/2
BA2	4P19	IC40/3 IC29/6 IC47/3
BA3	0001	IC29/7
BA4	PCP4	IC46/9 IC29/9
BA5	0001	IC46/11 IC29/10
BA6	0001	IC46/14 IC29/11
BA7	0001	IC46/1 IC29/12
IC46/6	PCP4	IC46/6 IC40/6 IC47/6
IC37/8	PCP5F	IC37/8 IC40/4
BITE MUX SEL	4363	IC47/15 IC61/9
BS1	4C6C	IC47/14 IC85/9
BS2	0196	IC47/13 IC81/9
BS3	AF62	IC47/12 IC77/13

Table 13: Routine 7 (cont.)

Signal	Signature	Test Node
BS4	16C5	IC47/11 IC77/12
BS5	2A0P	IC47/10 IC77/10
BS6	65A1	IC47/9 IC77/9
BS7	1702	IC47/7 IC78/9
SW2 SEL	PCP5F	IC40/14
SW3 SEL	PCP5F	IC40/13
SW4 SEL	PCP5F	IC40/12

ROUTINE 8

123. This routine checks the host interface to the DSPs.

Digital board SW1 DIL switch settings:

4, 7	OFF
1-3, 5-6, 8	ON

Signature analyser connection and settings:

Start:	TP4 negative trigger
Stop:	TP4 negative trigger
Clock:	TP3 positive trigger
Earth:	TP5

Table 14: Routine 8

Signal	Signature	Test Node
+5V	A02F	IC64/20
0V	0000	IC64/5
CE	3769	IC64/10 IC43/9
R/W	A07F	IC64/12
D8	03C1	IC64/24
D9	2623	IC64/23
D10	F500	IC64/21
D11	69U4	IC64/19
D12	4F3U	IC64/18
D13	P14U	IC64/17
D14	C96F	IC64/15
D15	HC11	IC64/14
AA1	6HC2	IC64/7
AA2	6CF7	IC64/6
AA3	70A0	IC64/4

DSP Signature Analysis Tests

124. Loading the Signature Analysis program

(1) If DSP4 is fitted, then set DSP4 switch to ON, else set to OFF.

(2) If DSP3 is fitted, then set DSP3 switch to ON, else set to OFF.

(3) Set switch SW2-6 to OFF.

(4) Execute Routine 9 (para. 126)

(5) Reset the RA3790 Receiver.

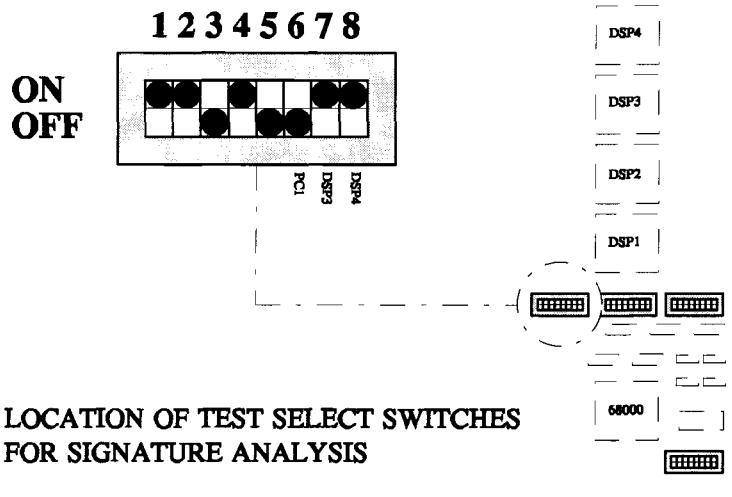
ROUTINE 9

125. Digital board SW1 DIL switch settings:

1, 4 & 7	OFF
2, 3, 5, 6 & 8	ON

Signature analyser connection and settings:

Start:	TP8
Stop:	TP8
Clock:	see text
Earth:	TP5



LOCATION OF TEST SELECT SWITCHES FOR SIGNATURE ANALYSIS

Test Phase 1

126. Ensure that PC1 is set to OFF. Perform the following signature analysis tests.

127. **Test 1a**

(1) Attach the CLOCK probe to test point TP17 (Positive trigger)
(2) Set the signature analyser to START on a rising edge and STOP on a falling edge.
(3) Test the data bus:

D0 40C5	D1 511A	D2 H081	D3 AFA4
D4 P614	D5 PA89	D6 8P80	D7 02F5
D8 40C5	D9 511A	D10 H081	D11 AFA4
D12 P614	D13 PA89	D14 8P80	D15 02F5
D16 40C5	D17 511A	D18 H081	D19 AFA4
D20 P614	D21 PA89	D22 8P80	D23 02F5

(4) Test the address bus:

A0 H9FH	A1 1F59	A2 AUC3	A3 UH5P
A4 216P	A5 72H2	A6 76H6	A7 0UA7
A8 C388	A9 753F	A10 6717	A11 CPA4
A12 07C0	A13 0PUF	A14 0PUF	A15 0PUF

(5) Test the address decode PAL - PD5:

PIN 18 0PUF	PIN 13 451P	PIN 12 84F1

(6) Test the parallel output latch - IC76:

PIN 2 H081	PIN 5 AFA4	PIN 7 P614
PIN 10 PA89	PIN 12 8P80	PIN 15 02F5

128. **Test 1b**

(1) Attach the CLOCK probe to test point TP12
(2) Set the signature analyser to START on a rising edge and STOP on a falling edge.
(3) Test the external RAM:

D0 1567	D1 02U2	D2 69AH	D3 C7PH
D4 H2P9	D5 400C	D6 343P	D7 9H27

129. **Test 1c**

(1) Attach the CLOCK probe to test point TP12
(2) Set the signature analyser to START on a falling edge and STOP on a rising edge.
(3) Test the EPROM - PD7:

PIN 11 1804	PIN 12 2U9U	PIN 13 25C3	PIN 15 9CA5
PIN 16 19PC	PIN 17 1A75	PIN 18 1CA1	PIN 19 7UU4

Note: The signatures for this test depend upon the issue of the DSP software. The above signatures are for software issue P90553 Iss. 1.0. For other software issues the signatures can be compared with those of a working board fitted with the same software issue.

130. **Test Phase 2**

(1) Ensure that switch PC1 is set to OFF.
(2) Ensure that DSP3 switch is set to OFF.
(3) Ensure that DSP4 switch is set to OFF.
(4) Set switch PC1 to ON.
(5) Perform the following signature analysis tests.

131. **Test 2a**

(1) Attach the CLOCK probe to test point TP17
(2) Set the signature analyser to START on a rising edge and STOP on a falling edge.
(3) Test DSP2 - IC70. Ensure that DSP4 switch is set to OFF.
(4) Set switch PC1 to ON.
(5) Perform the following signature analysis tests.

D0 H785	D1 F010	D2 AC4U	D3 750U
D4 100C	D5 82P9	D6 U6HF	D7 5UF5

(6) Test the bus arbitrator PAL - PD3

PIN 3 FF2U	PIN 4 F2P2	PIN 5 F2P2	PIN 6 CP5P

(7) Test Port C output for DSP2 on IC14

PIN 2 CP5P

132. **Test 2b**

(1) Attach the CLOCK probe to test point TP12
(2) Set the signature analyser to START on a rising edge and STOP on a falling edge.
(3) Test the host port for DSP2

D9 PP7P	D10 PP7P	D11 PP7U

133. **Test 2c**

(1) Attach the CLOCK probe to test point TP17
(2) Set the signature analyser to START on a falling edge and STOP on a rising edge.
(3) Test data transfer for DSP1 and DSP2

D0 PC9H	D1 H8PC

(4) Test the bus arbitrator PAL - PD3

PIN 17 H8PA	PIN 18 C0A0

134. **Test phase 3** (only run if DSP3 is fitted)

(1) Ensure that switch PC1 is set to OFF.
(2) Ensure that DSP3 switch is set to ON.
(3) Ensure that DSP4 switch is set to OFF.
(4) Set switch PC1 to ON.
(5) Perform the following signature analysis tests.

135. **Test 3a**

(1) Attach the CLOCK probe to test point TP17
(2) Set the signature analyser to START on a rising edge and STOP on a falling edge.
(3) Test DSP3 - IC82

D0 H785	D1 F010	D2 AC4U	D3 750U
D4 100C	D5 82P9	D6 U6HF	D7 5UF5

(4) Test the bus arbitrator PAL - PD3

PIN 3 F9C6	PIN 4 F2P2	PIN 7 F2P2	PIN 9 CP5P

(5) Test Port C output for DSP3 on IC3

PIN 9 CP5P

136. **Test 3b**

(1) Attach the CLOCK probe to test point TP12
(2) Set the signature analyser to START on a rising edge and STOP on a falling edge.
(3) Test the host port for DSP3

D9 PP7P	D10 PP7P	D11 PP7U

137. **Test 3c**

(1) Attach the CLOCK probe to test point TP17
(2) Set the signature analyser to START on a falling edge and STOP on a rising edge.
(3) Test data transfer for DSP1 DSP2 and DSP3

D0 F561	D1 4F6H

(4) Test the bus arbitrator PAL - PD3

PIN 17 4F6P	PIN 18 84A9	PIN 27 5F2F

138. **Test phase 4** (only run if DSP4 is fitted)

(1) Ensure that switch PC1 is set to OFF.
(2) Ensure that DSP3 switch is set to OFF.
(3) Ensure that DSP4 switch is set to ON.
(4) Set switch PC1 to ON.
(5) Perform the following signature analysis tests.

139. **Test 4a**

(1) Attach the CLOCK probe to test point TP17
(2) Set the signature analyser to START on a rising edge and STOP on a falling edge.
(3) Test DSP4 - IC91

D0 H785	D1 F010	D2 AC4U	D3 750U
D4 100C	D5 82P9	D6 U6HF	D7 5UF5

(4) Test the bus arbitrator PAL - PD3

PIN 3 6P06	PIN 4 F2P2	PIN 10 F2P2	PIN 11 CP5P

(5) Test Port C output for DSP4 on IC16

PIN 2 CP5P

140. **Test 4b**

(1) Attach the CLOCK probe to test point TP12
(2) Set the signature analyser to START on a rising edge and STOP on a falling edge.
(3) Test the host port for DSP4

D9 PP7P	D10 PP7P	D11 PP7U

141. **Test 4c**

(1) Attach the CLOCK probe to test point TP17
(2) Set the signature analyser to START on a falling edge and STOP on a rising edge.
(3) Test data transfer for DSP1 DSP2 and DSP4

D0 9A5U	D1 CP67

(4) Test the bus arbitrator PAL - PD3

PIN 16 A0A2	PIN 17 UUA1	PIN 18 7275

142. **Test phase 5** (only run if DSP3 and DSP4 are fitted)

(1) Ensure that switch PC1 is set to OFF.
(2) Ensure that DSP3 switch is set to ON.
(3) Ensure that DSP4 switch is set to ON.
(4) Set switch PC1 to ON.
(5) Perform the following signature analysis tests.

143. **Test 5a**

(1) Attach the CLOCK probe to test point TP17
(2) Set the signature analyser to START on a falling edge and STOP on a rising edge.
(3) Test data transfer for DSP1 DSP2 DSP3 and DSP4

D0 H50F	D1 HFP8

(4) Test the bus arbitrator PAL - PD3

PIN 16 3H8C	PIN 17 A7U8	PIN 18 UA3H	PIN 27 14FA

MODULE ALIGNMENT

144. The module will maintain factory alignment for a considerable period of time, and the adjustable components should be left undisturbed unless a known misalignment has been established (for example component replacement).

145. The only adjustable components on the board are the variable inductors (L20, L21 and L23) in the 1.4 MHz bandpass filter on the analogue IF output.

146. To adjust these use the following procedure:

(1) Tune the receiver to 1.4 MHz, manual gain and select 1.4 MHz wideband IF output (via the front-panel menu system).

(2) Set links LK4 and LK5 to position A.

(3) Using a spectrum analyser with a tracking generator, set the centre frequency to 1.4 MHz and the span to be 20 kHz. The filters can be adjusted for a flat passband with minimum attenuation.

COMPONENTS LIST

DIGITAL BOARD ASSEMBLY
PART No. 91217-02
DRAWING No. DA91217 ISSUE 2A

REF	DESCRIPTION							PART No.
CAPACITORS								
C1	CHIP	1	U	20%	35	V	TAN	999182/105P
C2	CHIP	1	U	20%	35	V	TAN	999182/105P
C3	CHIP	1	U	20%	35	V	TAN	999182/105P
C4	CHIP	10	U	20%	25	V	TAN	Y00643
C5	CHIP	1	U	20%	35	V	TAN	999182/105P
C6	CHIP	3.3	U	20%	16	V	TAN	945050
C7	CHIP	4.7	P	5%	50	V	CER C	999154/479P
C8	CHIP	4.7	P	5%	50	V	CER C	999154/479P
C9	CHIP	10	U	20%	25	V	TAN	Y00643
C10	CHIP	10	N	10%	100	V	CER X	999155/103P
C11	CHIP	10	N	10%	100	V	CER X	999155/103P
C12		0.047	U	-20/80%		5V5	ALU RADIAL	945002
C13	CHIP	10	U	20%	25	V	TAN	Y00643
C14	CHIP	10	U	20%	25	V	TAN	Y00643
C15	CHIP	1	U	20%	35	V	TAN	999182/105P
C16	CAP	220	U	T%	25	V	ALU TAC-	921536/EQ
C17	CAP	220	U	T%	25	V	ALU TAC-	921536/EQ
C18	CHIP	10	U	20%	25	V	TAN	Y00643
C19	CAP	220	U	T%	25	V	ALU TAC-	921536/EQ
C20	CHIP	10	U	20%	25	V	TAN	Y00643
C21	CHIP	47	U	10%	10	V	TAN	999043/476P
C22	CHIP	3.3	U	20%	16	V	TAN	945050
C23	CHIP	3.3	U	20%	16	V	TAN	945050
C24	CHIP	3.3	U	20%	16	V	TAN	945050
C25	CHIP	100	N	10%	50	V	CER X	948163
C26	CHIP	1	U	20%	35	V	TAN	999182/105P
C27	CHIP	1	U	20%	35	V	TAN	999182/105P
C28	CHIP	1	U	20%	35	V	TAN	999182/105P
C29	CHIP	100	N	10%	50	V	CER X	948163
C30	CHIP	3.3	U	20%	16	V	TAN	945050

REF	DESCRIPTION						PART No.
C31	CHIP 100	N	10%	50	V	CER X	948163
C32	CHIP 10	N	10%	100	V	CER X	999155/103P
C33	CHIP 100	N	10%	50	V	CER X	948163
C34	CHIP 10	U	20%	25	V	TAN	Y00643
C35	CHIP 3.3	U	20%	16	V	TAN	945050
C36	CHIP 3.3	U	20%	16	V	TAN	945050
C37	CHIP 100	N	10%	50	V	CER X	948163
C38	CHIP 10	U	20%	25	V	TAN	Y00643
C39	CHIP 3.3	U	20%	16	V	TAN	945050
C40	CHIP 100	N	10%	50	V	CER X	948163
C41	CHIP 10	N	10%	100	V	CER X	999155/103P
C42	CHIP 1	U	20%	35	V	TAN	999182/105P
C43	CHIP 3.3	U	20%	16	V	TAN	945050
C44	CHIP 1	U	20%	35	V	TAN	999182/105P
C45	CHIP 3.3	U	20%	16	V	TAN	945050
C46	CHIP 47	U	10%	10	V	TAN	999043/476P
C47	CHIP 3.3	U	20%	16	V	TAN	945050
C48	CHIP 47	U	10%	10	V	TAN	999043/476P
C49	CHIP 1	U	20%	35	V	TAN	999182/105P
C50	CHIP 47	U	10%	10	V	TAN	999043/476P
C51	CHIP 47	U	10%	10	V	TAN	999043/476P
C52	CHIP 1	U	20%	35	V	TAN	999182/105P
C53	CHIP 10	N	10%	100	V	CER X	999155/103P
C54	CHIP 10	N	10%	100	V	CER X	999155/103P
C55	CHIP 3.3	U	20%	16	V	TAN	945050
C56	CHIP 3.3	U	20%	16	V	TAN	945050
C57	CHIP 10	N	10%	100	V	CER X	999155/103P
C58	CHIP 10	N	10%	100	V	CER X	999155/103P
C59	CHIP 10	N	10%	100	V	CER X	999155/103P
C60	CHIP 10	N	10%	100	V	CER X	999155/103P
C61	CHIP 10	N	10%	100	V	CER X	999155/103P
C62	CHIP 10	N	10%	100	V	CER X	999155/103P
C63	CHIP 220	P	5%	50	V	CER C	999154/221P
C64	CHIP 220	P	5%	50	V	CER C	999154/221P
C65	CHIP 470	P	5%	50	V	CER C	999154/471P

REF	DESCRIPTION								PART No.
C66	CHIP	470	P	5%	50	V	CER	C	999154/471P
C67	CHIP	1	U	20%	35	V	TAN		999182/105P
C68	CHIP	100	N	10%	50	V	CER	X	948163
C69	CHIP	100	N	10%	50	V	CER	X	948163
C70	CHIP	10	N	10%	100	V	CER	X	999155/103P
C71	CHIP	10	N	10%	100	V	CER	X	999155/103P
C72	CHIP	100	N	10%	50	V	CER	X	948163
C73	CHIP	47	U	10%	10	V	TAN		999043/476P
C74	CHIP	1	U	20%	35	V	TAN		999182/105P
C75	CHIP	1	N	10%	100	V	CER	X	999155/102P
C76	CHIP	100	P	5%	50	V	CER	C	999154/101P
C77	CHIP	100	P	5%	50	V	CER	C	999154/101P
C78	CHIP	100	P	5%	50	V	CER	C	999154/101P
C79	CHIP	1	N	10%	100	V	CER	X	999155/102P
C80	CHIP	10	N	10%	100	V	CER	X	999155/103P
C81	CHIP	100	P	5%	50	V	CER	C	999154/101P
C82	CHIP	100	P	5%	50	V	CER	C	999154/101P
C83	CHIP	100	P	5%	50	V	CER	C	999154/101P
C84	CHIP	10	N	10%	100	V	CER	X	999155/103P
C85	CHIP	100	P	5%	50	V	CER	C	999154/101P
C86	CHIP	100	P	5%	50	V	CER	C	999154/101P
C87	CHIP	10	N	10%	100	V	CER	X	999155/103P
C88	CHIP	100	P	5%	50	V	CER	C	999154/101P
C89	CHIP	100	P	5%	50	V	CER	C	999154/101P
C90	CHIP	1	N	10%	100	V	CER	X	999155/102P
C91	CHIP	10	N	10%	100	V	CER	X	999155/103P
C92	CHIP	1	N	10%	100	V	CER	X	999155/102P
C93	CHIP	10	N	10%	100	V	CER	X	999155/103P
C94	CHIP	10	N	10%	100	V	CER	X	999155/103P
C95	CHIP	10	N	10%	100	V	CER	X	999155/103P
C96	CHIP	1	N	10%	100	V	CER	X	999155/102P
C97	CHIP	10	N	10%	100	V	CER	X	999155/103P
C98	CHIP	100	P	5%	50	V	CER	C	999154/101P
C99	CHIP	10	N	10%	100	V	CER	X	999155/103P
C100	CHIP	100	N	10%	50	V	CER	X	948163

REF	DESCRIPTION								PART No.
C101	CHIP	10	N	10%	100	V	CER	X	999155/103P
C102	CHIP	10	N	10%	100	V	CER	X	999155/103P
C103	CHIP	100	P	5%	50	V	CER	C	999154/101P
C104	CHIP	100	P	5%	50	V	CER	C	999154/101P
C105	CHIP	10	N	10%	100	V	CER	X	999155/103P
C106	CHIP	10	N	10%	100	V	CER	X	999155/103P
C107	CHIP	10	N	10%	100	V	CER	X	999155/103P
C108	CHIP	10	N	10%	100	V	CER	X	999155/103P
C109	CHIP	100	N	10%	50	V	CER	X	948163
C110	CHIP	100	N	10%	50	V	CER	X	948163
C111	CHIP	100	N	10%	50	V	CER	X	948163
C112	CHIP	100	N	10%	50	V	CER	X	948163
C113	CHIP	100	N	10%	50	V	CER	X	948163
C114	CHIP	100	N	10%	50	V	CER	X	948163
C115	CHIP	100	N	10%	50	V	CER	X	948163
C116	CHIP	100	N	10%	50	V	CER	X	948163
C117	CHIP	100	N	10%	50	V	CER	X	948163
C118	CHIP	10	N	10%	100	V	CER	X	999155/103P
C119	CHIP	10	N	10%	100	V	CER	X	999155/103P
C120	CHIP	100	N	10%	50	V	CER	X	948163
C121	CHIP	10	N	10%	100	V	CER	X	999155/103P
C122	CHIP	10	N	10%	100	V	CER	X	999155/103P
C123	CHIP	10	N	10%	100	V	CER	X	999155/103P
C124	CHIP	10	N	10%	100	V	CER	X	999155/103P
C125	CHIP	10	N	10%	100	V	CER	X	999155/103P
C126	CHIP	100	N	10%	50	V	CER	X	948163
C127	CHIP	100	N	10%	50	V	CER	X	948163
C128	CHIP	10	N	10%	100	V	CER	X	999155/103P
C129	CHIP	100	N	10%	50	V	CER	X	948163
C130	CHIP	100	N	10%	50	V	CER	X	948163
C131	CHIP	100	N	10%	50	V	CER	X	948163
C132	CHIP	100	N	10%	50	V	CER	X	948163
C133	CHIP	100	N	10%	50	V	CER	X	948163
C134	CHIP	10	N	10%	100	V	CER	X	999155/103P
C135	CHIP	10	N	10%	100	V	CER	X	999155/103P

REF	DESCRIPTION							PART No.
C136	CHIP 10	N	10%	100	V	CER	X	999155/103P
C137	CHIP 10	N	10%	100	V	CER	X	999155/103P
C138	CHIP 10	N	10%	100	V	CER	X	999155/103P
C139	CHIP 10	N	10%	100	V	CER	X	999155/103P
C140	CHIP 100	N	10%	50	V	CER	X	948163
C141	CHIP 10	N	10%	100	V	CER	X	999155/103P
C142	CHIP 2.2	N	10%	100	V	CER	X	999155/222P
C143	CHIP 100	N	10%	50	V	CER	X	948163
C144	CHIP 10	N	10%	100	V	CER	X	999155/103P
C145	CHIP 10	N	10%	100	V	CER	X	999155/103P
C146	CHIP 10	N	10%	100	V	CER	X	999155/103P
C147	CHIP 2.2	N	10%	100	V	CER	X	999155/222P
C148	CHIP 10	N	10%	100	V	CER	X	999155/103P
C149	CHIP 10	N	10%	100	V	CER	X	999155/103P
C150	CHIP 10	N	10%	100	V	CER	X	999155/103P
C151	CHIP 100	N	10%	50	V	CER	X	948163
C152	CHIP 2.2	N	10%	100	V	CER	X	999155/222P
C153	CHIP 470	P	5%	50	V	CER	C	999154/471P
C154	CHIP 470	P	5%	50	V	CER	C	999154/471P
C155	CHIP 10	N	10%	100	V	CER	X	999155/103P
C156	CHIP 10	N	10%	100	V	CER	X	999155/103P
C157	CHIP 100	N	10%	50	V	CER	X	948163
C158	CHIP 100	N	10%	50	V	CER	X	948163
C159	CHIP 10	N	10%	100	V	CER	X	999155/103P
C160	CHIP 10	N	10%	100	V	CER	X	999155/103P
C161	CHIP 100	N	10%	50	V	CER	X	948163
C162	CHIP 10	N	10%	100	V	CER	X	999155/103P
C163	CHIP 10	N	10%	100	V	CER	X	999155/103P
C164	CHIP 100	N	10%	50	V	CER	X	948163
C165	CHIP 2.2	N	10%	100	V	CER	X	999155/222P
C166	CHIP 100	N	10%	50	V	CER	X	948163
C167	CHIP 100	N	10%	50	V	CER	X	948163
C168	CHIP 100	N	10%	50	V	CER	X	948163
C169	CHIP 10	N	10%	100	V	CER	X	999155/103P
C170	CHIP 100	N	10%	50	V	CER	X	948163

REF	DESCRIPTION								PART No.
C171	CHIP	100	N	10%	50	V	CER	X	948163
C172	CHIP	10	N	10%	100	V	CER	X	999155/103P
C173	CHIP	100	N	10%	50	V	CER	X	948163
C174	CHIP	100	N	10%	50	V	CER	X	948163
C175	CHIP	10	N	10%	100	V	CER	X	999155/103P
C176	CHIP	100	N	10%	50	V	CER	X	948163
C177									
C178	CHIP	10	N	10%	100	V	CER	X	999155/103P
C179	CHIP	100	N	10%	50	V	CER	X	948163
C180	CHIP	15	P	5%	50	V	CER	C	999154/150P
C181	CHIP	100	N	10%	50	V	CER	X	948163
C182	CHIP	100	N	10%	50	V	CER	X	948163
C183	CHIP	1	N	10%	100	V	CER	X	999155/102P
C184	CHIP	2.2	N	10%	100	V	CER	X	999155/222P
C185	CHIP	10	N	10%	100	V	CER	X	999155/103P
C186	CHIP	100	N	10%	50	V	CER	X	948163
C187	CHIP	10	N	10%	100	V	CER	X	999155/103P
C188	CHIP	10	N	10%	100	V	CER	X	999155/103P
C189	CHIP	100	N	10%	50	V	CER	X	948163
C190	CHIP	10	N	10%	100	V	CER	X	999155/103P
C191	CHIP	100	N	10%	50	V	CER	X	948163
C192	CHIP	100	N	10%	50	V	CER	X	948163
C193	CHIP	1	N	10%	100	V	CER	X	999155/102P
C194	CHIP	100	N	10%	50	V	CER	X	948163
C195	CHIP	10	N	10%	100	V	CER	X	999155/103P
C196	CHIP	10	N	10%	100	V	CER	X	999155/103P
C197	CHIP	10	N	10%	100	V	CER	X	999155/103P
C198	CHIP	100	N	10%	50	V	CER	X	948163
C199	CHIP	100	N	10%	50	V	CER	X	948163
C200	CHIP	10	N	10%	100	V	CER	X	999155/103P
C201	CHIP	100	N	10%	50	V	CER	X	948163
C202	CHIP	100	N	10%	50	V	CER	X	948163
C203	CHIP	100	N	10%	50	V	CER	X	948163
C204	CHIP	100	N	10%	50	V	CER	X	948163
C205	CHIP	10	N	10%	100	V	CER	X	999155/103P

REF	DESCRIPTION							PART No.
C206	CHIP 10	N	10%	100	V	CER	X	999155/103P
C207	CHIP 10	N	10%	100	V	CER	X	999155/103P
C208	CHIP 10	N	10%	100	V	CER	X	999155/103P
C209	CHIP 10	N	10%	100	V	CER	X	999155/103P
C210	CHIP 100	N	10%	50	V	CER	X	948163
C211	CHIP 100	N	10%	50	V	CER	X	948163
C212	CHIP 100	N	10%	50	V	CER	X	948163
C213	CHIP 10	N	10%	100	V	CER	X	999155/103P
C214	CHIP 10	N	10%	100	V	CER	X	999155/103P
C215	CHIP 2.2	N	10%	100	V	CER	X	999155/222P
C216	CHIP 100	N	10%	50	V	CER	X	948163
C217	CHIP 1	N	10%	100	V	CER	X	999155/102P
C218	CHIP 100	N	10%	50	V	CER	X	948163
C219	CHIP 100	N	10%	50	V	CER	X	948163
C220	CHIP 100	N	10%	50	V	CER	X	948163
C221	CHIP 10	N	10%	100	V	CER	X	999155/103P
C222	CHIP 100	N	10%	50	V	CER	X	948163
C223	CHIP 2.2	N	10%	100	V	CER	X	999155/222P
C224	CHIP 10	N	10%	100	V	CER	X	999155/103P
C225	CHIP 100	N	10%	50	V	CER	X	948163
C226	CHIP 470	P	5%	50	V	CER	C	999154/471P
C227	CHIP 100	N	10%	50	V	CER	X	948163
C228	CHIP 100	N	10%	50	V	CER	X	948163
C229	CHIP 100	N	10%	50	V	CER	X	948163
C230	CHIP 10	N	10%	100	V	CER	X	999155/103P
C231	CHIP 1	N	10%	100	V	CER	X	999155/102P
C232	CHIP 470	P	5%	50	V	CER	C	999154/471P
C233	CHIP 220	P	5%	50	V	CER	C	999154/221P
C234	CHIP 100	N	10%	50	V	CER	X	948163
C235	CHIP 100	N	10%	50	V	CER	X	948163
C236	CHIP 10	N	10%	100	V	CER	X	999155/103P
C237	CHIP 100	N	10%	50	V	CER	X	948163
C238	CHIP 100	N	10%	50	V	CER	X	948163
C239	CHIP 470	P	5%	50	V	CER	C	999154/471P
C240	CHIP 100	N	10%	50	V	CER	X	948163

REF	DESCRIPTION								PART No.
C241	CHIP	10	N	10%	100	V	CER	X	999155/103P
C242	CHIP	10	N	10%	100	V	CER	X	999155/103P
C243	CHIP	100	N	10%	50	V	CER	X	948163
C244	CHIP	10	N	10%	100	V	CER	X	999155/103P
C245	CHIP	100	N	10%	50	V	CER	X	948163
C246	CHIP	100	N	10%	50	V	CER	X	948163
C247	CHIP	470	P	5%	50	V	CER	C	999154/471P
C248									
C249	CHIP	68	P	5%	50	V	CER	C	999154/680P
C250	CHIP	100	N	10%	50	V	CER	X	948163
C251	CHIP	2.2	N	10%	100	V	CER	X	999155/222P
C252	CHIP	1	N	10%	100	V	CER	X	999155/102P
C253	CHIP	100	N	10%	50	V	CER	X	948163
C254	CHIP	100	N	10%	50	V	CER	X	948163
C255	CHIP	100	N	10%	50	V	CER	X	948163
C256	CHIP	100	N	10%	50	V	CER	X	948163
C257	CHIP	100	N	10%	50	V	CER	X	948163
C258	CHIP	10	N	10%	100	V	CER	X	999155/103P
C259	CHIP	68	P	5%	50	V	CER	C	999154/680P
C260	CHIP	470	P	5%	50	V	CER	C	999154/471P
C261	CHIP	470	P	5%	50	V	CER	C	999154/471P
C262	CHIP	10	N	10%	100	V	CER	X	999155/103P
C263	CHIP	10	N	10%	100	V	CER	X	999155/103P
C264	CHIP	470	P	5%	50	V	CER	C	999154/471P
C265	CHIP	10	N	10%	100	V	CER	X	999155/103P
C266	CHIP	220	P	5%	50	V	CER	C	999154/221P
C267	CHIP	10	N	10%	100	V	CER	X	999155/103P

DIODES

D1	CHIP	SCM23VMWS		LED	RD/GN	Y00829
D2	SWITCHG	BAS16	75V			999206/MC
D3	SWITCHG	BAS16	75V			999206/MC
D4	SWITCHG	BAS16	75V			999206/MC
D5	SWITCHG	BAS16	75V			999206/MC

REF	DESCRIPTION				PART No.
D6	SWITCHG	BAS16	75V		999206/MC
D7	SWITCHG	BAS16	75V		999206/MC
D8	SWITCHG	BAS16	75V		999206/MC
D9	SWITCHG	BAS16	75V		999206/MC
D10	CHIP	BAR43A D	SCHOTTKY		999683/SD
D11	SWITCHG	BAS16	75V		999206/MC
D12	CHIP	BAR43A D	SCHOTTKY		999683/SD
D13	SWITCHG	BAS16	75V		999206/MC
D14	CHIP	SCM23VMWS	LED	RD/GN	Y00829
D15	CHIP	LGS260-DO	LED	GREEN	Y00723
D16	CHIP	LGS260-DO	LED	GREEN	Y00723
D17	SWITCHG	BAS16	75V		999206/MC
D18	SWITCHG	BAS16	75V		999206/MC
D19	VARICAP	(J7A) ZC836A			943956
D20	SWITCHG	BAS16	75V		999206/MC
D21	SWITCHG	BAS16	75V		999206/MC
D22	VARICAP	(J7A) ZC836A			943956
D23	VARICAP	(J7A) ZC836A			943956

INTEGRATED CIRCUITS

IC1	081	LIN OPL AMP	945085
IC2	74HC4053	CMS S 2CH ANA MUX	999322/SD
IC3	3487	INT Q LIN DRV	A00258
IC4	26LS30	INT D DIF LNE RCVR	938684
IC5	26LS30	INT D DIF LNE RCVR	938684
IC6	26LS32	INT Q DIF LNE RCVR	938683
IC7	081	LIN OPL AMP	945085
IC8	74HC4053	CMS S 2CH ANA MUX	999322/SD
IC9	26LS32	INT Q DIF LNE RCVR	938683
IC10	74HC174	HEX FLP FLOP	999693/SD
IC11	68230	CMS PAR INT TIMR	Y00674
IC12	081	LIN OPL AMP	945085
IC13	74HC4053	CMS S 2CH ANA MUX	999322/SD
IC14	26LS30	INT D DIF LNE RCVR	938684
IC15	62256	CMS 32K X 8 ST RAM	945471/SD

REF	DESCRIPTION		PART No.
IC16	26LS30	INT D DIF LNE RCVR	938684
IC17	072	JFT-IP OP AMP	999680/SD
IC18	072	JFT-IP OP AMP	999680/SD
IC19	072	JFT-IP OP AMP	999680/SD
IC20	62256	CMS 32K X 8 ST RAM	945471/SD
IC21	68681	CMS D ASYN RXTX	Y00675
IC22	DC32044	CMS-AUD SIG PROC	999681/SD
IC23			
IC24	8408	Q D/A 8B CONV	999696/SD
IC25	072	JFT-IP OP AMP	999680/SD
IC26	700	CMS P/S MONITOR	948257
IC27	74HC08	CMS Q 2IP AND GATE	999335/SD
IC28	78M05	LIN S 5V VOL REG	994901/EQ
IC29	68230	CMS PAR INT TIMR	Y00674
IC30	28C64	CMS S 8K X 8 EEPROM	Y00772
IC31	7905	LIN S 5V NEG REG	945150
IC32	74HC04	CMS H INVERTER	999312/SD
IC33	74HC138	CMS 3/8 LNE DCDR	943980/SD
IC34	68HC000	CMS 8B MICRO	Y00673
IC35	74HC32	CMS Q 2IP OR GATE	999308/SD
IC36	74HC161	CMS 4 BIT BIN CNTR	A00240
IC37	74HC10	CMS T 3IP NAN GATE	999307/SD
IC38	74HC147	CMS S ENCODER	Y00708
IC39	74HC32	CMS Q 2IP OR GATE	999308/SD
IC40	74HC138	CMS 3/8 LNE DCDR	943980/SD
IC41	02	S VOL REF PLUS	999644/SD
IC42	74LC09	TTL Q 2IP AND GATE	945155
IC43	74HC139	CMS D 2-4 LNE DCDR	999331/SD
IC44	74HCT245	CMS O BUS TRA RCVR	943988/SD
IC45	74HCT245	CMS O BUS TRA RCVR	943988/SD
IC46	74HC85	CMS S 4B MAG COMP	943978/SD
IC47	74HC138	CMS 3/8 LNE DCDR	943980/SD
IC48	79L05	LIN VOL REG	947223
IC49	78M05	LIN S 5V VOL REG	994901/EQ
IC50	74HC244	CMS O BUF 3ST DRIV	999650/SD

REF	DESCRIPTION		PART No.
IC51	74HC244	CMS O BUF 3ST DRIV	999650/SD
IC52	74HC244	CMS O BUF 3ST DRIV	999650/SD
IC53	428	LIN 8B D/A CONV	945158
IC54	081	LIN OPL AMP	945085
IC55	1856	INT D/A CON	Y01262
IC56	5534	OP AMP LOW NOISE	999704/001
IC57	5534	OP AMP LOW NOISE	999704/001
IC58	1496	LIN BAL MOD DMOD	945027
IC59	56	INT 16B A-D CONV	948143
IC60	74HC365	H 3S BUF NINV	999691/SD
IC61	74HC174	HEX FLP FLOP	999693/SD
IC62	324	LIN Q L/P OPL AMP	945026
IC63	081	LIN OPL AMP	945085
IC64	56002	DSP 24B	Y01126
IC65	74HC4067	CMS ANA MUX 16CH	947643
IC66	5534	OP AMP LOW NOISE	999704/001
IC67	74HC04	CMS H INVERTER	999312/SD
IC68	74HC14	CMS H INV SCHM	999334/SD
IC69		CONVERTER AD VIDEO	999682/SD
IC70	56002	DSP 24B Y01126	
IC71	74HC74T	CMS D DTP FLP FLOP	999353/SD
IC72	081	LIN OPL AMP	945085
IC73	74HC04	CMS H INVERTER	999312/SD
IC74	145157	PPL	999692/SD
IC75	145157	PPL	999692/SD
IC76	74HC174	HEX FLP FLOP	999693/SD
IC77	74HC08	CMS Q 2IP AND GATE	999335/SD
IC78	74HC174	HEX FLP FLOP	999693/SD
IC79	145157	PPL	999692/SD
IC80	081	LIN OPL AMP	945085
IC81	74HC174	HEX FLP FLOP	999693/SD
IC82			
IC83	081	LIN OPL AMP	945085
IC84	6206	CMS 32K X 8 SRAM	A00204
IC85	74HC174	HEX FLP FLOP	999693/SD

REF	DESCRIPTION					PART No.
IC86						
IC87	6206	CMS 32K X 8 SRAM				A00204
IC88	74HC32	CMS Q 2IP OR GATE				999308/SD
IC89	6206	CMS 32K X 8 SRAM				A00204
IC90	1171	INT D/A CONV				999689/SD
INDUCTORS						
L1	CHOKE	1	UH	10%		999105/102L
L2	CHOKE	10	UH	10%	RF	A00887
L3	CHOKE	10	UH	10%	RF	A00887
L4	CHOKE	10	UH	10%	RF	A00887
L5	CHOKE	15	UH	10%		945764
L6	CHOKE	15	UH	10%		945764
L7	CHOKE	15	UH	10%		945764
L8	CHOKE	15	UH	10%		945764
L9	CHOKE	15	UH	10%		945764
L10	CHOKE	15	UH	10%		945764
L11	CHOKE	10	UH	5%		999103/103L
L12	CHOKE	1	UH	10%		999105/102L
L13	CHOKE	10	UH	5%		999103/103L
L14	CHOKE	150	UH	10%		945098
L15	CHOKE	10	UH	5%		999103/103L
L16	CHOKE	10	UH	5%		999103/103L
L17	CHOKE	10	UH	5%		999103/103L
L18	CHOKE	10	UH	5%		999103/103L
L19	CHOKE	10	UH	5%		999103/103L
L20	COIL ASSY					89086-02
L21	COIL ASSY					89086-02
L22	CHOKE	1	UH	10%		999105/102L
L23	COIL ASSY					89086-02
LINKS						
LK1	CONN 3-WAY P FX STRT					943683
LK2	CONN 3-WAY P FX STRT					943683
LK3	CONN 3-WAY P FX STRT					943683
LK4	CONN 3-WAY P FX STRT					943683
LK5	CONN 3-WAY P FX STRT					943683

REF	DESCRIPTION	PART No.
LK6	CONN 3-WAY P FX STRT	943683
LK7	CONN 3-WAY P FX STRT	943683
	PINS	
P1	TERM PIN SE PSH SLD 1.02 BR TS	937625/EQ
P2	TERM PIN SE PSH SLD 1.02 BR TS	937625/EQ
P3	TERM PIN SE PSH SLD 1.02 BR TS	937625/EQ
P4	TERM PIN SE PSH SLD 1.02 BR TS	937625/EQ
P5	TERM PIN SE PSH SLD 1.02 BR TS	937625/EQ
P6	TERM PIN SE PSH SLD 1.02 BR TS	937625/EQ
	PROGRAMMABLE DEVICES	
PD1	EPROM	90550-01
PD2	PAL	90555-01
PD3	PAL	90552-02
PD4	PAL	90551-01
PD5	PAL	91301-01
PD7	PROM	90553-01
	PLUGS	
PL1	15-WAY P FX R/ANG	946973
PL2	40-WAY P	943331
PL3	26-WAY	943632
PL4	50-WAY P FX STR	943388
PL5	40-WAY P	943331
PL6	4-WAY P FX R/ANG	939131
	RESISTORS	
R1	CHIP 10 K D% 0.100 W MF	999419/103R
R2	CHIP 100 2% 0.125 W MF	999161/101R
R3	CHIP 100 2% 0.125 W MF	999161/101R
R4	CHIP 100 2% 0.125 W MF	999161/101R
R5	CHIP 100 2% 0.125 W MF	999161/101R
R6	CHIP 10 K D% 0.100 W MF	999419/103R
R7	CHIP 100 2% 0.063 W MF	999160/101R
R8	CHIP 270 2% 0.063 W MF	999160/271R
R9	CHIP 270 2% 0.063 W MF	999160/271R
R10	CHIP 270 2% 0.063 W MF	999160/271R

REF	DESCRIPTION					PART No.
R11	CHIP 470		2%	0.063 W	MF	999160/471R
R12	CHIP 470		2%	0.063 W	MF	999160/471R
R13	CHIP 100		2%	0.063 W	MF	999160/101R
R14	CHIP 270		2%	0.063 W	MF	999160/271R
R15	CHIP 33	K	2%	0.063 W	MF	999160/333R
R16	CHIP 100		2%	0.063 W	MF	999160/101R
R17	CHIP 33	K	2%	0.063 W	MF	999160/333R
R18	CHIP 22	K	2%	0.063 W	MF	999160/223R
R19	CHIP 33	K	2%	0.063 W	MF	999160/333R
R20	CHIP 22	K	2%	0.063 W	MF	999160/223R
R21	CHIP 33	K	2%	0.063 W	MF	999160/333R
R22	CHIP 470		2%	0.063 W	MF	999160/471R
R23	CHIP 470		2%	0.063 W	MF	999160/471R
R24	CHIP 470		2%	0.063 W	MF	999160/471R
R25	CHIP 470		2%	0.063 W	MF	999160/471R
R26	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R27	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R28	CHIP 1	K	2%	0.063 W	MF	999160/102R
R29	CHIP 1	K	2%	0.063 W	MF	999160/102R
R30	CHIP 100		2%	0.063 W	MF	999160/101R
R31	CHIP 100		2%	0.063 W	MF	999160/101R
R32	CHIP 22	K	2%	0.063 W	MF	999160/223R
R33	CHIP 1	K	2%	0.063 W	MF	999160/102R
R34	CHIP 1	K	2%	0.063 W	MF	999160/102R
R35	CHIP 33	K	2%	0.063 W	MF	999160/333R
R36	CHIP 33	K	2%	0.063 W	MF	999160/333R
R37	CHIP 22	K	2%	0.063 W	MF	999160/223R
R38	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R39	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R40	CHIP 22	K	2%	0.063 W	MF	999160/223R
R41	CHIP 22	K	2%	0.063 W	MF	999160/223R
R42	CHIP 22	K	2%	0.063 W	MF	999160/223R
R43	CHIP 22	K	2%	0.063 W	MF	999160/223R
R44	CHIP 100	K	2%	0.063 W	MF	999160/104R
R45	CHIP 100	K	2%	0.063 W	MF	999160/104R

REF	DESCRIPTION					PART No.
R46	CHIP 100		2%	0.063 W	MF	999160/101R
R47	CHIP 100		2%	0.063 W	MF	999160/101R
R48	CHIP 1	K	2%	0.063 W	MF	999160/102R
R49	CHIP 33	K	2%	0.063 W	MF	999160/333R
R50	CHIP 1	K	2%	0.063 W	MF	999160/102R
R51	CHIP 1	K	2%	0.063 W	MF	999160/102R
R52	CHIP 1	K	2%	0.063 W	MF	999160/102R
R53	CHIP 1	K	2%	0.063 W	MF	999160/102R
R54	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R55	CHIP 10	K	2%	0.063 W	MF	999160/103R
R56	CHIP 1	K	2%	0.063 W	MF	999160/102R
R57	CHIP 47	K	2%	0.063 W	MF	999160/473R
R58	CHIP 1	K	2%	0.063 W	MF	999160/102R
R59	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R60	CHIP 100	K	2%	0.063 W	MF	999160/104R
R61	CHIP 470		2%	0.063 W	MF	999160/471R
R62	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R63	CHIP 100	K	2%	0.063 W	MF	999160/104R
R64	CHIP 10	K	2%	0.063 W	MF	999160/103R
R65	CHIP 470		2%	0.063 W	MF	999160/471R
R66	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R67	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R68	CHIP 1	K	2%	0.063 W	MF	999160/102R
R69	CHIP 1	K	2%	0.063 W	MF	999160/102R
R70	CHIP 1	K	2%	0.063 W	MF	999160/102R
R71	CHIP 1	K	2%	0.063 W	MF	999160/102R
R72	CHIP 47	K	2%	0.063 W	MF	999160/473R
R73	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R74	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R75	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R76	CHIP 1	K	2%	0.063 W	MF	999160/102R
R77	CHIP 1	K	2%	0.063 W	MF	999160/102R
R78	CHIP 1.5	K	2%	0.063 W	MF	999160/152R
R79	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R80	CHIP 2.2	K	2%	0.063 W	MF	999160/222R

REF	DESCRIPTION					PART No.
R81	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R82	CHIP 1	K	2%	0.063 W	MF	999160/102R
R83	CHIP 1	K	2%	0.063 W	MF	999160/102R
R84	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R85	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R86	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R87	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R88	CHIP 1	K	2%	0.063 W	MF	999160/102R
R89	CHIP 1	K	2%	0.063 W	MF	999160/102R
R90	CHIP 1	K	2%	0.063 W	MF	999160/102R
R91	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R92	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R93	CHIP 1	K	2%	0.063 W	MF	999160/102R
R94	CHIP 1	K	2%	0.063 W	MF	999160/102R
R95	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R96	CHIP 1	K	2%	0.063 W	MF	999160/102R
R97	CHIP 100	K	2%	0.063 W	MF	999160/104R
R98	CHIP 10	K	2%	0.063 W	MF	999160/103R
R99	CHIP 10	K	2%	0.063 W	MF	999160/103R
R100	CHIP 10	K	2%	0.063 W	MF	999160/103R
R101	CHIP 1	K	2%	0.063 W	MF	999160/102R
R102	CHIP 1	K	2%	0.063 W	MF	999160/102R
R103	CHIP 10	K	2%	0.063 W	MF	999160/103R
R104	CHIP 100	K	2%	0.063 W	MF	999160/104R
R105	CHIP 470		2%	0.063 W	MF	999160/471R
R106	CHIP 47	K	2%	0.063 W	MF	999160/473R
R107	CHIP 100	K	2%	0.063 W	MF	999160/104R
R108	CHIP 1	K	2%	0.063 W	MF	999160/102R
R109	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R110	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R111	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R112	CHIP 1.5	K	2%	0.063 W	MF	999160/152R
R113	CHIP 1.5	K	2%	0.063 W	MF	999160/152R
R114	CHIP 1.5	K	2%	0.063 W	MF	999160/152R
R115	CHIP 1.5	K	2%	0.063 W	MF	999160/152R

REF	DESCRIPTION					PART No.
R116	CHIP 47	K	2%	0.063 W	MF	999160/473R
R117	CHIP 10	K	2%	0.063 W	MF	999160/103R
R118	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R119	CHIP 100	K	2%	0.063 W	MF	999160/104R
R120	CHIP 1	K	2%	0.063 W	MF	999160/102R
R121	CHIP 1	K	2%	0.063 W	MF	999160/102R
R122	CHIP 1	K	2%	0.063 W	MF	999160/102R
R123	CHIP 1	K	2%	0.063 W	MF	999160/102R
R124	CHIP 10	K	2%	0.063 W	MF	999160/103R
R125	CHIP 22	K	2%	0.063 W	MF	999160/223R
R126	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R127	CHIP 33	K	2%	0.063 W	MF	999160/333R
R128	CHIP 10	K	2%	0.063 W	MF	999160/103R
R129	CHIP 33	K	2%	0.063 W	MF	999160/333R
R130	CHIP 10	K	2%	0.063 W	MF	999160/103R
R131	CHIP 10	K	2%	0.063 W	MF	999160/103R
R132	CHIP 100		2%	0.063 W	MF	999160/101R
R133	CHIP 22	K	2%	0.063 W	MF	999160/223R
R134	CHIP 470		2%	0.063 W	MF	999160/471R
R135	CHIP 10	K	2%	0.063 W	MF	999160/103R
R136	CHIP 10	K	2%	0.063 W	MF	999160/103R
R137	CHIP 10	K	2%	0.063 W	MF	999160/103R
R138	CHIP 10	K	2%	0.063 W	MF	999160/103R
R139	CHIP 10	K	2%	0.063 W	MF	999160/103R
R140	CHIP 10	K	2%	0.063 W	MF	999160/103R
R141	CHIP 10	K	2%	0.063 W	MF	999160/103R
R142	CHIP 10	K	2%	0.063 W	MF	999160/103R
R143	CHIP 10	K	2%	0.063 W	MF	999160/103R
R144	CHIP 10	K	2%	0.063 W	MF	999160/103R
R145	CHIP 10	K	2%	0.063 W	MF	999160/103R
R146	CHIP 10	K	2%	0.063 W	MF	999160/103R
R147	CHIP 10	K	2%	0.063 W	MF	999160/103R
R148	CHIP 10	K	2%	0.063 W	MF	999160/103R
R149	CHIP 10	K	2%	0.063 W	MF	999160/103R
R150	CHIP 10	K	2%	0.063 W	MF	999160/103R

REF	DESCRIPTION					PART No.
R151	CHIP 10	K	2%	0.063 W	MF	999160/103R
R152	CHIP 10	K	2%	0.063 W	MF	999160/103R
R153	CHIP 47	K	2%	0.063 W	MF	999160/473R
R154	CHIP 22	K	2%	0.063 W	MF	999160/223R
R155	CHIP 22	K	2%	0.063 W	MF	999160/223R
R156	CHIP 1	K	2%	0.063 W	MF	999160/102R
R157	CHIP 1	K	2%	0.063 W	MF	999160/102R
R158	CHIP 1	K	2%	0.063 W	MF	999160/102R
R159	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R160	CHIP 1	K	2%	0.063 W	MF	999160/102R
R161	CHIP 10	K	2%	0.063 W	MF	999160/103R
R162	CHIP 1	K	2%	0.063 W	MF	999160/102R
R163	CHIP 10	K	2%	0.063 W	MF	999160/103R
R164	CHIP 1	K	2%	0.063 W	MF	999160/102R
R165	CHIP 10	K	2%	0.063 W	MF	999160/103R
R166	CHIP 1	K	2%	0.063 W	MF	999160/102R
R167	CHIP 10	K	2%	0.063 W	MF	999160/103R
R168	CHIP 10	K	2%	0.063 W	MF	999160/103R
R169	CHIP 10	K	2%	0.063 W	MF	999160/103R
R170	CHIP 10	K	2%	0.063 W	MF	999160/103R
R171	CHIP 1	K	2%	0.063 W	MF	999160/102R
R172	CHIP 10	K	2%	0.063 W	MF	999160/103R
R173	CHIP 10	K	2%	0.063 W	MF	999160/103R
R174	CHIP 10	K	2%	0.063 W	MF	999160/103R
R175	CHIP 10	K	2%	0.063 W	MF	999160/103R
R176	CHIP 10	K	2%	0.063 W	MF	999160/103R
R177	CHIP 10	K	2%	0.063 W	MF	999160/103R
R178	CHIP 10	K	2%	0.063 W	MF	999160/103R
R179	CHIP 10	K	2%	0.063 W	MF	999160/103R
R180	CHIP 10	K	2%	0.063 W	MF	999160/103R
R181	CHIP 10	K	2%	0.063 W	MF	999160/103R
R182	CHIP 10	K	2%	0.063 W	MF	999160/103R
R183	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R184	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R185	CHIP 10	K	2%	0.063 W	MF	999160/103R

REF	DESCRIPTION					PART No.
R186	CHIP 10	K	2%	0.063 W	MF	999160/103R
R187	CHIP 10	K	2%	0.063 W	MF	999160/103R
R188	CHIP 10	K	2%	0.063 W	MF	999160/103R
R189	CHIP 10	K	2%	0.063 W	MF	999160/103R
R190	CHIP 10	K	2%	0.063 W	MF	999160/103R
R191	CHIP 10	K	2%	0.063 W	MF	999160/103R
R192	CHIP 47	K	2%	0.063 W	MF	999160/473R
R193	CHIP 47	K	2%	0.063 W	MF	999160/473R
R194	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R195	CHIP 470		2%	0.063 W	MF	999160/471R
R196	CHIP 1	K	2%	0.063 W	MF	999160/102R
R197	CHIP 100		2%	0.063 W	MF	999160/101R
R198	CHIP 22	K	2%	0.063 W	MF	999160/223R
R199	CHIP 4.7	K	D%	0.1 W	MF	999419/472R
R200	CHIP 4.7	K	D%	0.1 W	MF	999419/472R
R201	CHIP 47	K	2%	0.063 W	MF	999160/473R
R202	CHIP 47	K	2%	0.063 W	MF	999160/473R
R203	CHIP 47	K	2%	0.063 W	MF	999160/473R
R204	CHIP 47	K	2%	0.063 W	MF	999160/473R
R205	CHIP 100		2%	0.063 W	MF	999160/101R
R206	CHIP 100		2%	0.063 W	MF	999160/101R
R207	CHIP 47	K	2%	0.063 W	MF	999160/473R
R208	CHIP 47	K	2%	0.063 W	MF	999160/473R
R209	CHIP 47	K	2%	0.063 W	MF	999160/473R
R210	CHIP 47	K	2%	0.063 W	MF	999160/473R
R211	CHIP 47	K	2%	0.063 W	MF	999160/473R
R212	CHIP 47	K	2%	0.063 W	MF	999160/473R
R213	CHIP 47	K	2%	0.063 W	MF	999160/473R
R214	CHIP 47	K	2%	0.063 W	MF	999160/473R
R215	CHIP 47	K	2%	0.063 W	MF	999160/473R
R216	CHIP 47	K	2%	0.063 W	MF	999160/473R
R217	CHIP 47	K	2%	0.063 W	MF	999160/473R
R218	CHIP 47	K	2%	0.063 W	MF	999160/473R
R219	CHIP 47	K	2%	0.063 W	MF	999160/473R
R220	CHIP 47	K	2%	0.063 W	MF	999160/473R

REF	DESCRIPTION					PART No.
R221	CHIP 1	K	2%	0.063 W	MF	999160/102R
R222	CHIP 22	K	2%	0.063 W	MF	999160/223R
R223	CHIP 33	K	2%	0.063 W	MF	999160/333R
R224	CHIP 22	K	2%	0.063 W	MF	999160/223R
R225	CHIP 10	K	2%	0.063 W	MF	999160/103R
R226	CHIP 100	K	2%	0.063 W	MF	999160/104R
R227	CHIP 47	K	2%	0.063 W	MF	999160/473R
R228	CHIP 100		2%	0.063 W	MF	999160/101R
R229	CHIP 33	K	2%	0.063 W	MF	999160/333R
R230	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R231	CHIP 47	K	2%	0.063 W	MF	999160/473R
R232	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R233	CHIP 22	K	2%	0.063 W	MF	999160/223R
R234	CHIP 100		2%	0.063 W	MF	999160/101R
R235	CHIP 47	K	2%	0.063 W	MF	999160/473R
R236	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R237	CHIP 1	K	2%	0.063 W	MF	999160/102R
R238	CHIP 1	K	2%	0.063 W	MF	999160/102R
R239	CHIP 100		2%	0.063 W	MF	999160/101R
R240	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R241	CHIP 47	K	2%	0.063 W	MF	999160/473R
R242	CHIP 22	K	2%	0.063 W	MF	999160/223R
R243	CHIP 100	K	2%	0.063 W	MF	999160/104R
R244	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R245	CHIP 47	K	2%	0.063 W	MF	999160/473R
R246	CHIP 10	K	2%	0.063 W	MF	999160/103R
R247	CHIP 47	K	2%	0.063 W	MF	999160/473R
R248	CHIP 1	K	2%	0.063 W	MF	999160/102R
R249	CHIP 47	K	2%	0.063 W	MF	999160/473R
R250	CHIP 100	K	2%	0.063 W	MF	999160/104R
R251	CHIP 10	K	2%	0.063 W	MF	999160/103R
R252	CHIP 10	K	2%	0.063 W	MF	999160/103R
R253	CHIP 100	K	2%	0.063 W	MF	999160/104R
R254	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R255	CHIP 22	K	2%	0.063 W	MF	999160/223R

REF	DESCRIPTION						PART No.
R256	CHIP	270		2%	0.063 W	MF	999160/271R
R257	CHIP	22	K	2%	0.063 W	MF	999160/223R
R258	CHIP	22	K	2%	0.063 W	MF	999160/223R
R259	CHIP	22	K	2%	0.063 W	MF	999160/223R
R260	CHIP	33	K	2%	0.063 W	MF	999160/333R
R261	CHIP	1	K	2%	0.063 W	MF	999160/102R
R262	CHIP	22	K	2%	0.063 W	MF	999160/223R
R263	CHIP	10	K	2%	0.063 W	MF	999160/103R
R264	CHIP	10	K	2%	0.063 W	MF	999160/103R
R265	CHIP	22	K	2%	0.063 W	MF	999160/223R
R266	CHIP	22	K	2%	0.063 W	MF	999160/223R
R267	CHIP	10	K	2%	0.063 W	MF	999160/103R
R268	CHIP	22	K	2%	0.063 W	MF	999160/223R
R269	CHIP	10	K	2%	0.063 W	MF	999160/103R
R270	CHIP	10	K	2%	0.063 W	MF	999160/103R
R271	CHIP	10	K	2%	0.063 W	MF	999160/103R
R272	CHIP	22	K	2%	0.063 W	MF	999160/223R
R273	CHIP	10	K	2%	0.063 W	MF	999160/103R
R274	CHIP	100	K	2%	0.063 W	MF	999160/104R
R275	CHIP	100	K	2%	0.063 W	MF	999160/104R
R276	CHIP	47	K	2%	0.063 W	MF	999160/473R
R277	CHIP	47	K	2%	0.063 W	MF	999160/473R
R278	CHIP	2.2	K	2%	0.063 W	MF	999160/222R
R279	CHIP	47	K	2%	0.063 W	MF	999160/473R
R280	CHIP	22	K	2%	0.063 W	MF	999160/223R
R281	CHIP	10	K	2%	0.063 W	MF	999160/103R
R282	CHIP	22	K	2%	0.063 W	MF	999160/223R
R283	CHIP	100		2%	0.063 W	MF	999160/101R
R284	CHIP	100	K	2%	0.063 W	MF	999160/104R
R285	CHIP	10	K	2%	0.063 W	MF	999160/103R
R286	CHIP	4.7	K	2%	0.063 W	MF	999160/472R
R287	CHIP	10	K	2%	0.063 W	MF	999160/103R
R288	CHIP	10	K	2%	0.063 W	MF	999160/103R
R289	CHIP	10	K	2%	0.063 W	MF	999160/103R
R290	CHIP	10	K	2%	0.063 W	MF	999160/103R

REF	DESCRIPTION					PART No.
R291	CHIP 47	K	2%	0.063 W	MF	999160/473R
R292	CHIP 47	K	2%	0.063 W	MF	999160/473R
R293	CHIP 10	K	2%	0.063 W	MF	999160/103R
R294	CHIP 1	K	2%	0.063 W	MF	999160/102R
R295	CHIP 100	K	2%	0.063 W	MF	999160/104R
R296	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R297	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R298	CHIP 100	K	2%	0.063 W	MF	999160/104R
R299	CHIP 1	K	2%	0.063 W	MF	999160/102R
R300	CHIP 10	K	2%	0.063 W	MF	999160/103R
R301	CHIP 10	K	2%	0.063 W	MF	999160/103R
R302	CHIP 10	K	2%	0.063 W	MF	999160/103R
R303	CHIP 10	K	2%	0.063 W	MF	999160/103R
R304	CHIP 100		2%	0.063 W	MF	999160/101R
R305	CHIP 47	K	2%	0.063 W	MF	999160/473R
R306	CHIP 10	K	2%	0.063 W	MF	999160/103R
R307	CHIP 470		2%	0.063 W	MF	999160/471R
R308	CHIP 1	K	2%	0.063 W	MF	999160/102R
R309	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R310	CHIP 1	K	2%	0.063 W	MF	999160/102R
R311	CHIP 10	K	2%	0.063 W	MF	999160/103R
R312	CHIP 100	K	2%	0.063 W	MF	999160/104R
R313	CHIP 10	K	2%	0.063 W	MF	999160/103R
R314	CHIP 10	K	2%	0.063 W	MF	999160/103R
R315	CHIP 470		2%	0.063 W	MF	999160/471R
R316	CHIP 10	K	2%	0.063 W	MF	999160/103R
R317	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R318	CHIP 47	K	2%	0.063 W	MF	999160/473R
R319	CHIP 22	K	2%	0.063 W	MF	999160/223R
R320	CHIP 10	K	2%	0.063 W	MF	999160/103R
R321	CHIP 1	K	2%	0.063 W	MF	999160/102R
R322	CHIP 100	K	2%	0.063 W	MF	999160/104R
R223						
R324	CHIP 10	K	2%	0.063 W	MF	999160/103R
R325	CHIP 10	K	2%	0.063 W	MF	999160/103R

REF	DESCRIPTION					PART No.
R326	CHIP 100	K	2%	0.063 W	MF	999160/104R
R327	CHIP 10	K	2%	0.063 W	MF	999160/103R
R328	CHIP 10	K	2%	0.063 W	MF	999160/103R
R329	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R330	CHIP 1	K	2%	0.063 W	MF	999160/102R
R331	CHIP 10	K	2%	0.063 W	MF	999160/103R
R332	CHIP 47	K	2%	0.063 W	MF	999160/473R
R333	CHIP 1	K	2%	0.063 W	MF	999160/102R
R334	CHIP 10	K	2%	0.063 W	MF	999160/103R
R335	CHIP 10	K	2%	0.063 W	MF	999160/103R
R336	CHIP 10	K	2%	0.063 W	MF	999160/103R
R337	CHIP 10	K	2%	0.063 W	MF	999160/103R
R338	CHIP 10	K	2%	0.063 W	MF	999160/103R
R339	CHIP 100		2%	0.063 W	MF	999160/101R
R340	CHIP 10	K	2%	0.063 W	MF	999160/103R
R341	CHIP 100		2%	0.063 W	MF	999160/101R
R342	CHIP 1.5	K	2%	0.063 W	MF	999160/152R
R343	CHIP 1.5	K	2%	0.063 W	MF	999160/152R
R344	CHIP 10	K	2%	0.063 W	MF	999160/103R
R345	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R346	CHIP 1.5	K	2%	0.063 W	MF	999160/152R
R347	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R348	CHIP 33	K	2%	0.063 W	MF	999160/333R
R349	CHIP 10	K	2%	0.063 W	MF	999160/103R
R350	CHIP 4.7	K	2%	0.063 W	MF	999160/472R
R351	CHIP 1	K	2%	0.063 W	MF	999160/102R
R352	CHIP 33	K	2%	0.063 W	MF	999160/333R
R353	CHIP 10	K	2%	0.063 W	MF	999160/103R
R354	CHIP 10	K	2%	0.063 W	MF	999160/103R
R355	CHIP 22	K	2%	0.063 W	MF	999160/223R
R356	CHIP 10	K	2%	0.063 W	MF	999160/103R
R357	CHIP 100		2%	0.063 W	MF	999160/101R
R358	CHIP 470		2%	0.063 W	MF	999160/471R
R359	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R360	CHIP 10	K	2%	0.063 W	MF	999160/103R

REF	DESCRIPTION					PART No.
R361	CHIP 10	K	2%	0.063 W	MF	999160/103R
R362	CHIP 10	K	2%	0.063 W	MF	999160/103R
R363	CHIP 10	K	2%	0.063 W	MF	999160/103R
R364	CHIP 10	K	2%	0.063 W	MF	999160/103R
R365	CHIP 10	K	2%	0.063 W	MF	999160/103R
R366	CHIP 10	K	2%	0.063 W	MF	999160/103R
R367	CHIP 10	K	2%	0.063 W	MF	999160/103R
R368	CHIP 10	K	2%	0.063 W	MF	999160/103R
R369	CHIP 10	K	2%	0.063 W	MF	999160/103R
R370	CHIP 10	K	2%	0.063 W	MF	999160/103R
R371	CHIP 10	K	2%	0.063 W	MF	999160/103R
R372	CHIP 10	K	2%	0.063 W	MF	999160/103R
R373	CHIP 10	K	2%	0.063 W	MF	999160/103R
R374	CHIP 10	K	2%	0.063 W	MF	999160/103R
R375	CHIP 10	K	2%	0.063 W	MF	999160/103R
R377	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R378	CHIP 1	K	2%	0.063 W	MF	999160/102R
R379	CHIP 1	K	2%	0.063 W	MF	999160/102R
R380	CHIP 1	K	2%	0.063 W	MF	999160/102R
R381	CHIP 1	K	2%	0.063 W	MF	999160/102R

SWITCHES

S1	SLIDE	A00090
S2	SLIDE	A00090
S3	SLIDE	A00090
S4	SLIDE	A00090

SOCKETS

SK4	25-WAY S FX R/ANG	947404
SK5	RECT 15-WAY S FX R/ANG	946970

TRANSFORMERS

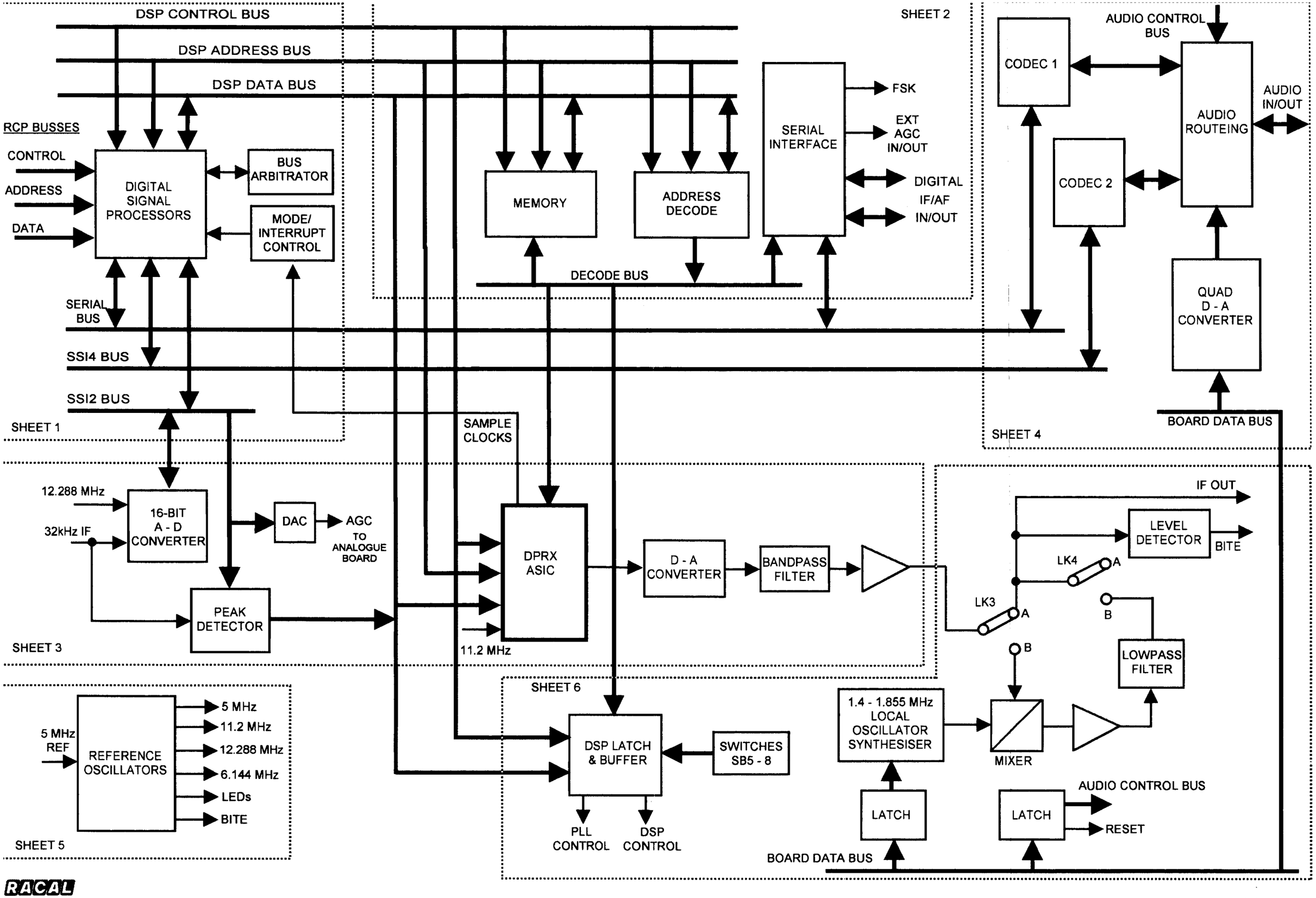
T1	AF 1:1 600 OHM	A01406
T2	AF 1:1 600 OHM	A01406

REF	DESCRIPTION		PART No.
TEST POINTS			
TP2	TEST PLUG		948390
TP3	TEST PLUG		948390
TP4	TEST PLUG		948390
TP5	TEST PLUG		948390
TP8	TEST PLUG		948390
TP12	TEST PLUG		948390
TP17	TEST PLUG		948390
TP22	TEST PLUG		948390
TP23	TEST PLUG		948390
TRANSISTORS			
TR1	N	MMBT2222A	943949
TR2	N	MMBT2222A	943949
TR3	N	MMBT2222A	943949
TR4	N	MMBT2222A	943949
TR5	N	MMBT2222A	943949
TR6	N	MMBT2222A	943949
TR7	N	MMBT2222A	943949
TR8	N	MMBT2222A	943949
TR9	N	MMBT2222A	943949
TR10	N	MMBT2222A	943949
TR11	CHIP(702)F	2N7002	999647/SD
TR12	N	MMBT2222A	943949
TR13	GP(BJ)P	BCX71J 150M	999204/MC
TR14	CHIP(SP)P	BSS84 360M	27771-010R00
TR15	CHIP(SP)P	BSS84 360M	27771-010R00
TR16	CHIP(702)F	2N7002	999647/SD
TR17	CHIP(702)F	2N7002	999647/SD
TR18	N	BC849	943941
TR19	GP(BJ)P	BCX71J 150M	999204/MC
TR20	N	BC849	943941
TR21	N	MMBT2369	943946
TR22	N	MMBT2369	943946
TR23	N	MMBT2369	943946
TR24	N	MMBT2369	943946
TR25	N	MMBT2369	943946

REF	DESCRIPTION		PART No.
TR26	N	MMBT2369	943946
TR27	N	MMBT2369	943946
TR28	N	MMBT2369	943946
TR29	N	MMBT2369	943946
TR30	N	MMBT2369	943946
TR31	N	BC849	943941
TR32	N	BC849	943941

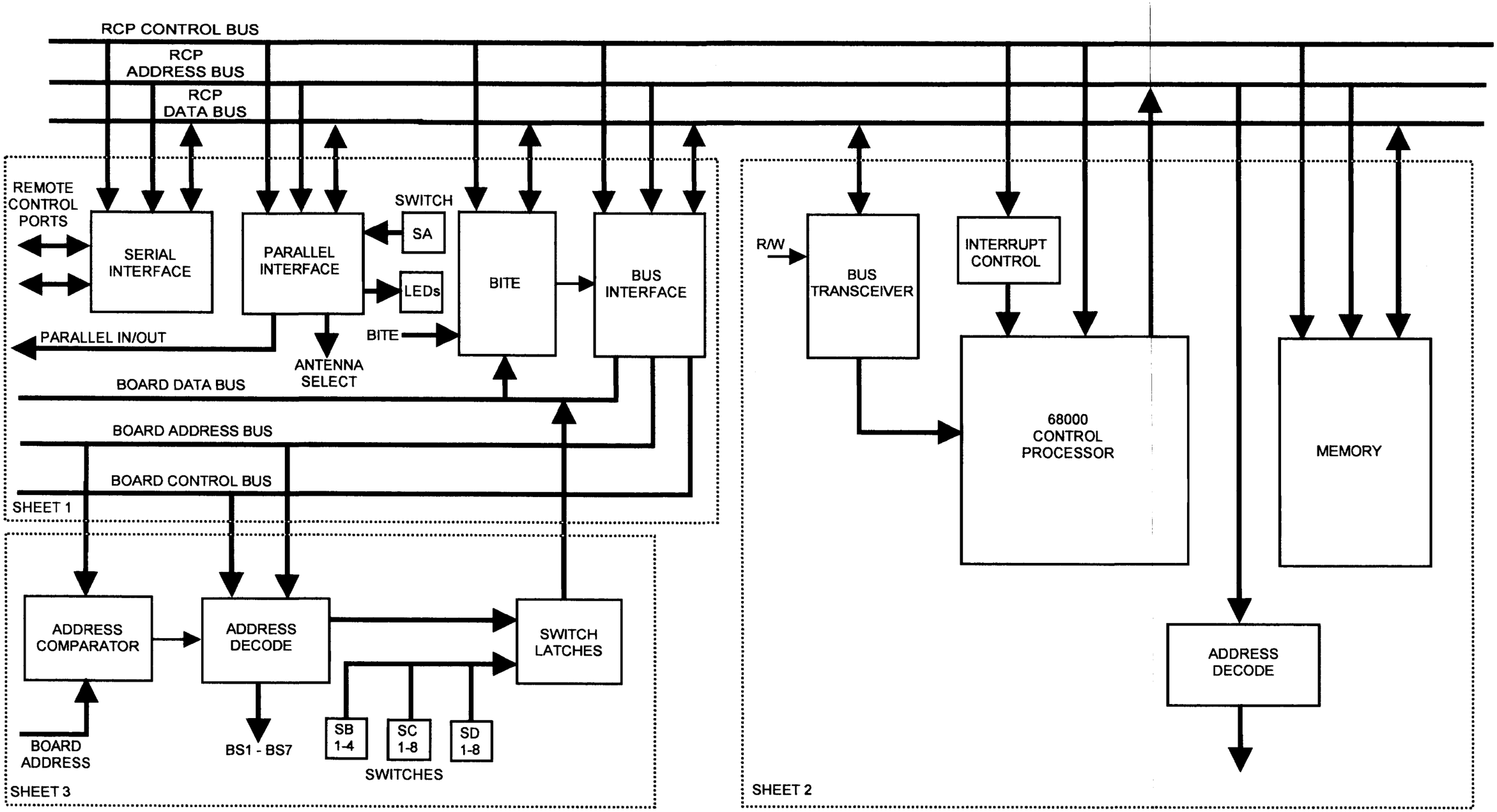
CRYSTALS

XL1	QUARTZ	3.6864 MHZ SMD	Y00733
XL2	OSCILLATOR	8.000 MHZ 100PPM	A00724
XL3	OSCILLATOR	10.00 MHZ 100PPM	A01263
XL4	CRYSTAL	11.2 MHZ HC49-4H	948137
XL5	CRYSTAL	12.288 MHZ HC49-4H	948139



RACAL
A5258

Block Diagram: RA3790 Digital Board - DSP Section Fig. 7.2



RACAL
A5258

Block Diagram: RA3790 Digital Board
Control Processor Section

Fig 7.3

DIGITAL SIGNAL PROCESSORS

IC91-a/1 DSP4 — IC82-a/1 DSP3 — IC70-a/1 DSP2 — IC64-a/1 DSP1

56002 — 56 BIT SIGNAL PROCESSOR

INTERNAL PLL — HOST INTERFACE — SERIAL COMMUNICATIONS INTERFACE — SYNCHRONOUS SERIAL INTERFACE — INTERRUPT AND MODE CONTROL — PORT A BUS CONTROL — PORT A ADDRESS AND DATA BUS — ONCE INTERFACE

SERIAL_BUS (SHT 2,4) — SSI4 (SHT 4) — HEN3 (SHT 2) — HEN2 (SHT 2) — SSI2 (SHT 3) — ADDRESS_BUS — DATA_BUS — HEN4 (SHT 2)

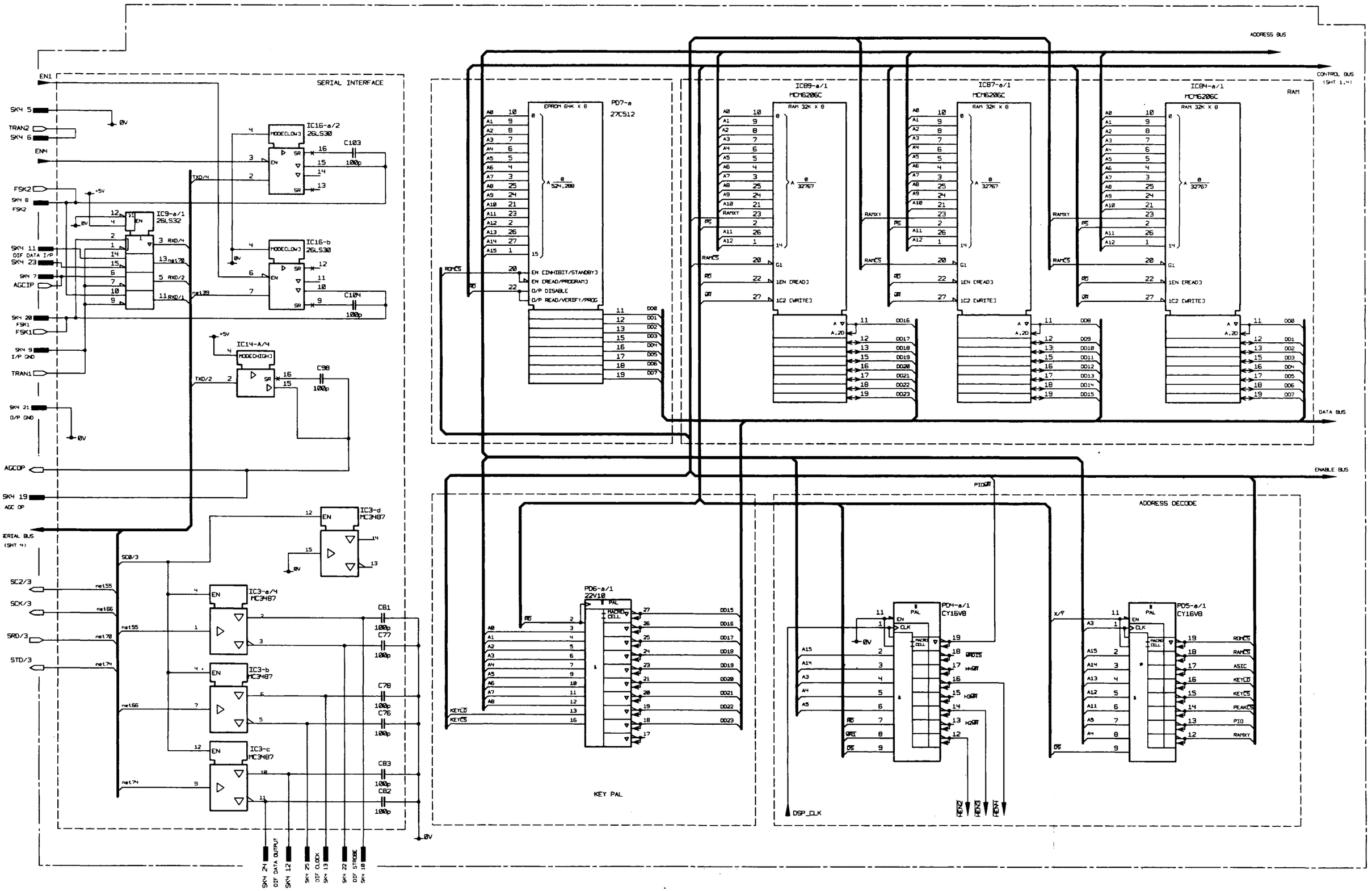
ADDRESS BUS (SHT 2,3)

DSP3,4 BOTTOM VIEW

DSP BUS ARBITRATOR

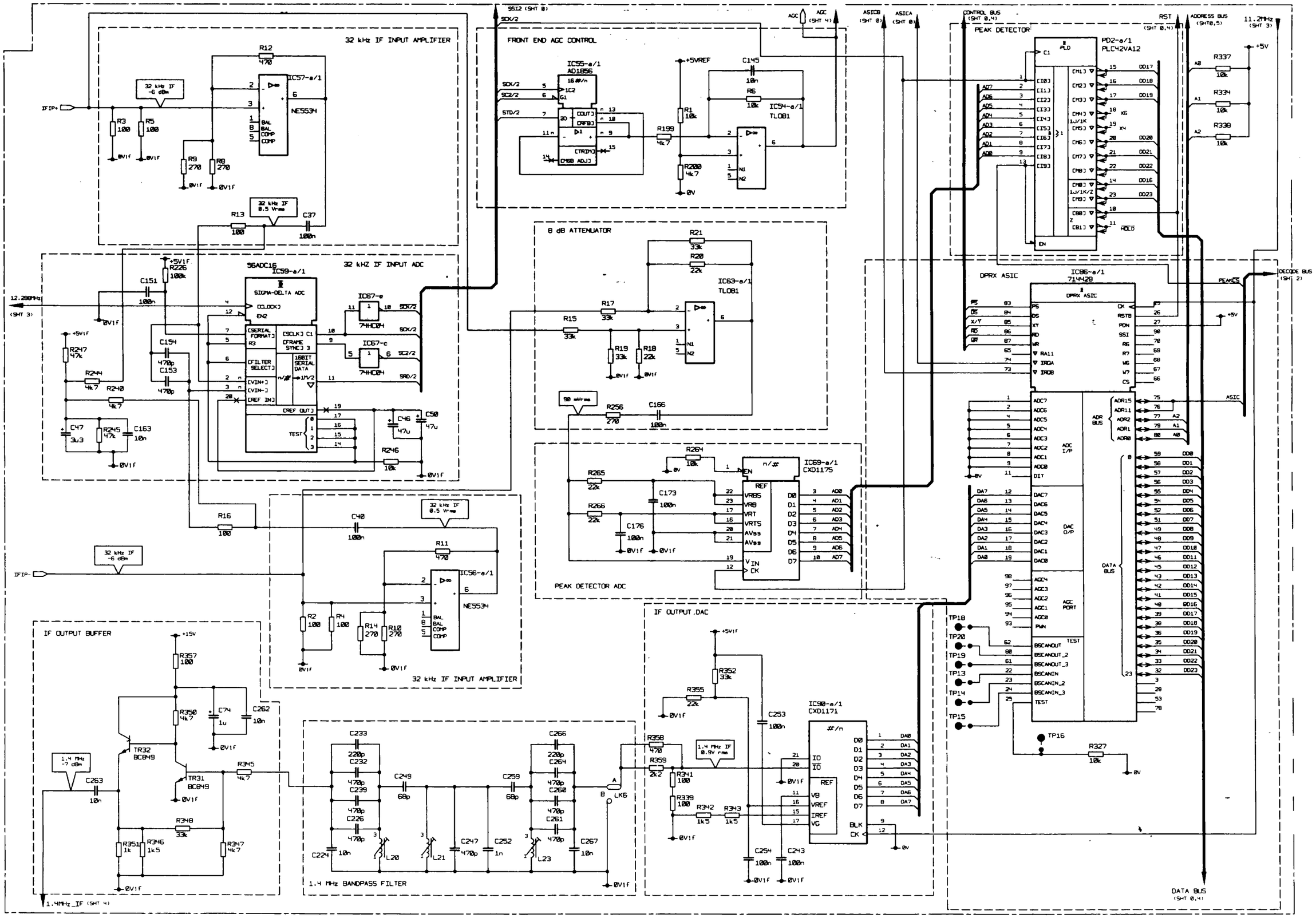
DSP3 (SHT 6) — DSP4 (SHT 6) — DSP_CLK (SHT 1) — DATA BUS (SHT 1,4) — CONTROL BUS (SHT 2,3,6) — MODE SELECTION — ASICB (SHT 3) — ASICA (SHT 3) — RST RST (SHT 3,6)

Circuit: Digital Board (Sheet 1) Fig. 7.4



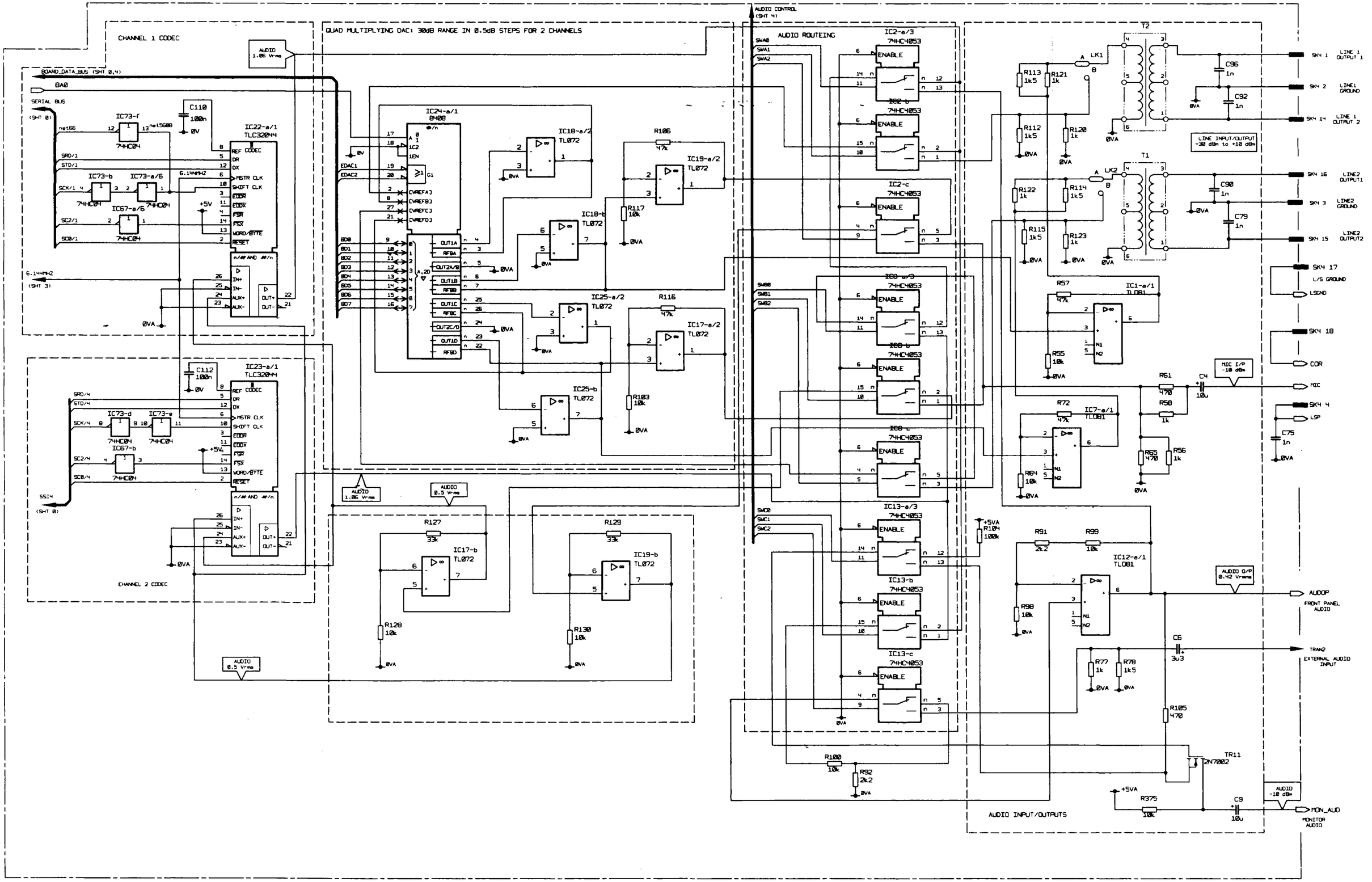
RACAL
A5258/91217/2/4

Circuit: Digital Board (Sheet 2) Fig. 7.5



RACAL
A5258/91217/3/4

Circuit: Digital Board (Sheet 3) Fig. 7.6


CHANNEL 1 CODEC
QUAD MULTIPLYING DAC: 30dB RANGE IN 0.5dB STEPS FOR 2 CHANNELS
AUDIO CONTROL (SHT 4)
AUDIO ROUTEING
BOARD_DATA_BUS (SHT 0,4)
SERIAL BUS (SHT 0)
IC22-a/1 TLC320AH4
IC23-a/1 TLC320AH4
IC24-a/1 8408
IC18-a/2 TL072
IC19-a/2 TL072
IC18-b TL072
IC25-a/2 TL072
IC17-a/2 TL072
IC25-b TL072
IC17-b TL072
IC18-b TL072
IC2-a/3 74HC4053
IC2-b 74HC4053
IC2-c 74HC4053
IC8-a/3 74HC4053
IC8-b 74HC4053
IC8-c 74HC4053
IC13-a/3 74HC4053
IC13-b 74HC4053
IC13-c 74HC4053
IC1-a/1 TL081
IC7-a/1 TL081
IC12-a/1 TL081
T1
T2
LINE INPUT/OUTPUT -30 dBm to +10 dBm
MIC I/P -10 dBm
AUDIO O/P 0.42 Vrms
AUDIO -10 dBm
FRONT PANEL AUDIO
EXTERNAL AUDIO INPUT
MONITOR AUDIO
AUDIO INPUT/OUTPUTS
CHANNEL 2 CODEC

TTL Voltage Level Converter
5MHz REF IN
5M_REF
L16 10u
C67 1u
R307 470
C206 10n
R308 1k
C205 10n
TR28 2N2369
5 MHz 4 Vpp
0V1f
+5V

PLL LOCK INDICATOR
D21 BAS16
PLL1 (SHT 4)
R271 10k
C56 3u3
TR16 2N7002
R162 1k
R164 1k
D15 LGS260-DO
D20 BAS16
PLL2 (SHT 4)
R270 10k
C55 3u3
R166 1k
R171 1k
D16 LGS260-DO
TR17 2N7002
0V

IC71-a/2 74HC74T
IC68-b 74HC14
IC68-c 74HC14
IC68-a/6 74HC14
IC68-e 74HC14
IC68-f 74HC14

PLL Control
IC74-a/1 MC145157
PLL SYNTHESISER
5MHZ (SHT 4)
PLL_LATCH (SHT 4)
PLL_CLK (SHT 4)
PLL1_DATA (SHT 4)
15 BIT
20
G2
C1
CSR OUT]
CPHASE DET]
CPHASE V]
CPHASE R]
CFREQ R]
CFREQ V]
CLOCK DET]
COSC OUT]
CREF OUT]
CFREQ IN]
COSC IN]

Loop Integrator
IC72-a/1 TL081
R284 100k
C199 100n
R278 2k2
R296 2k2
C218 100n
R297 2k2
R295 100k
C198 100n

11.2MHz V.C.O.
L18 10u
R46 100
R41 22k
R40 22k
C68 100n
R35 33k
R33 1k
XL4 11.2MHz
R44 100k
D22 ZC836A
TR26 2N2369
C65 470p
C63 220p
R38 2k2
C61 10n
TR23 2N2369
R30 100
R32 22k
R28 1k
C58 10n

Pulse Shaper
L13 10u
C54 10n
R25 470
R24 470
R26 2k2
C57 10n
TR21 2N2369

IC68-d 74HC14
11.2MHz (SHT 2)

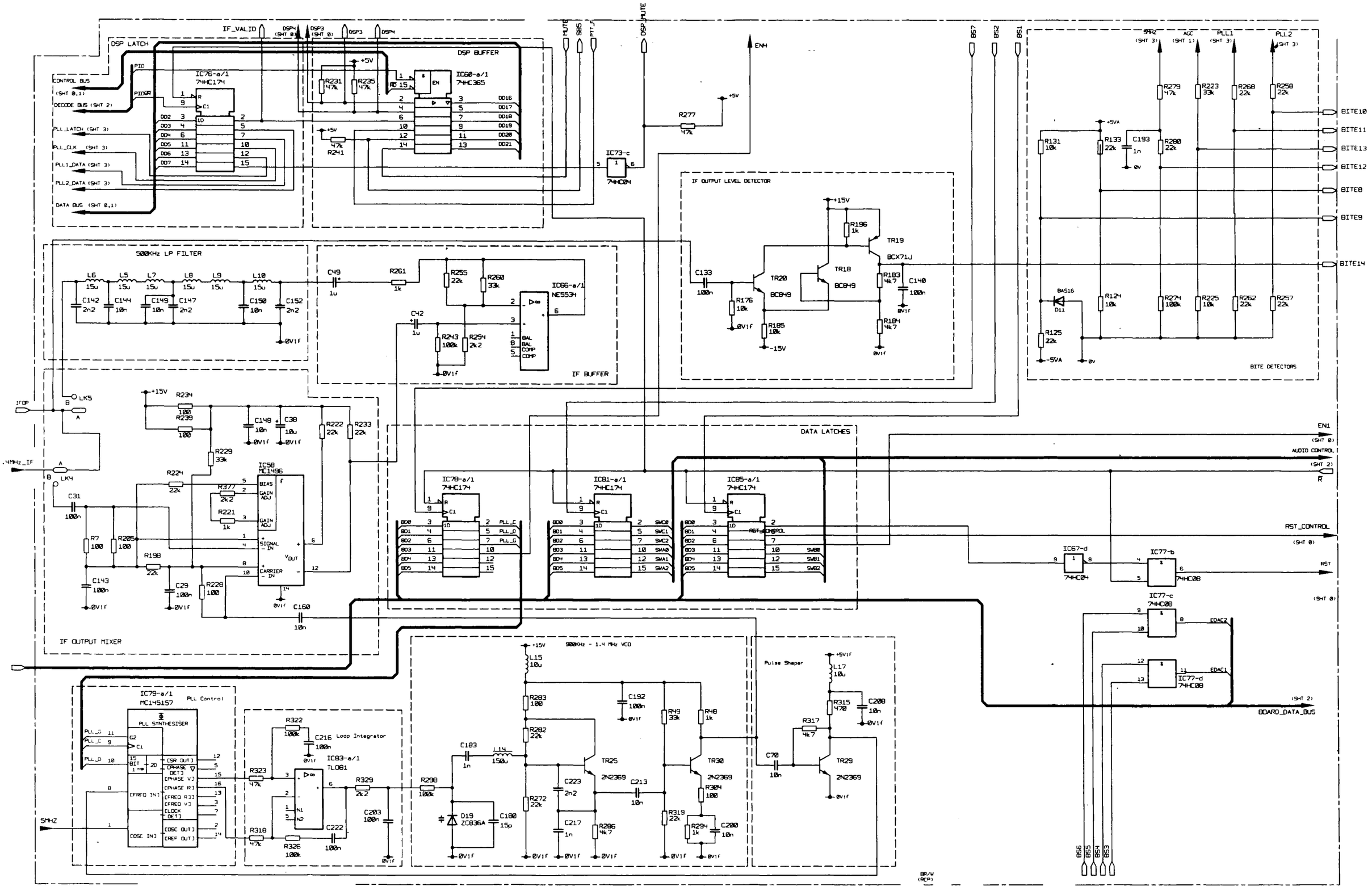
PLL Control
IC75-a/1 MC145157
PLL SYNTHESISER
PLL2_DATA
G2
C1
CSR OUT]
CPHASE DET]
CPHASE V]
CPHASE R]
CFREQ R]
CFREQ V]
CLOCK DET]
COSC OUT]
CREF OUT]
CFREQ IN]
COSC IN]

Loop Integrator
IC80-a/1 TL081
R275 100k
C189 100n
R299 1k
R309 2k2
C204 100n
R310 1k
R312 100k
C210 100n

12.288MHz V.C.O.
L19 10u
R47 100
R42 22k
R43 22k
C69 100n
R36 33k
R34 1k
XL5 12.288MHz
R45 100k
D23 ZC836A
TR27 2N2369
C66 470p
C64 220p
R39 2k2
C62 10n
TR24 2N2369
R31 100
R37 22k
R29 1k
C59 10n

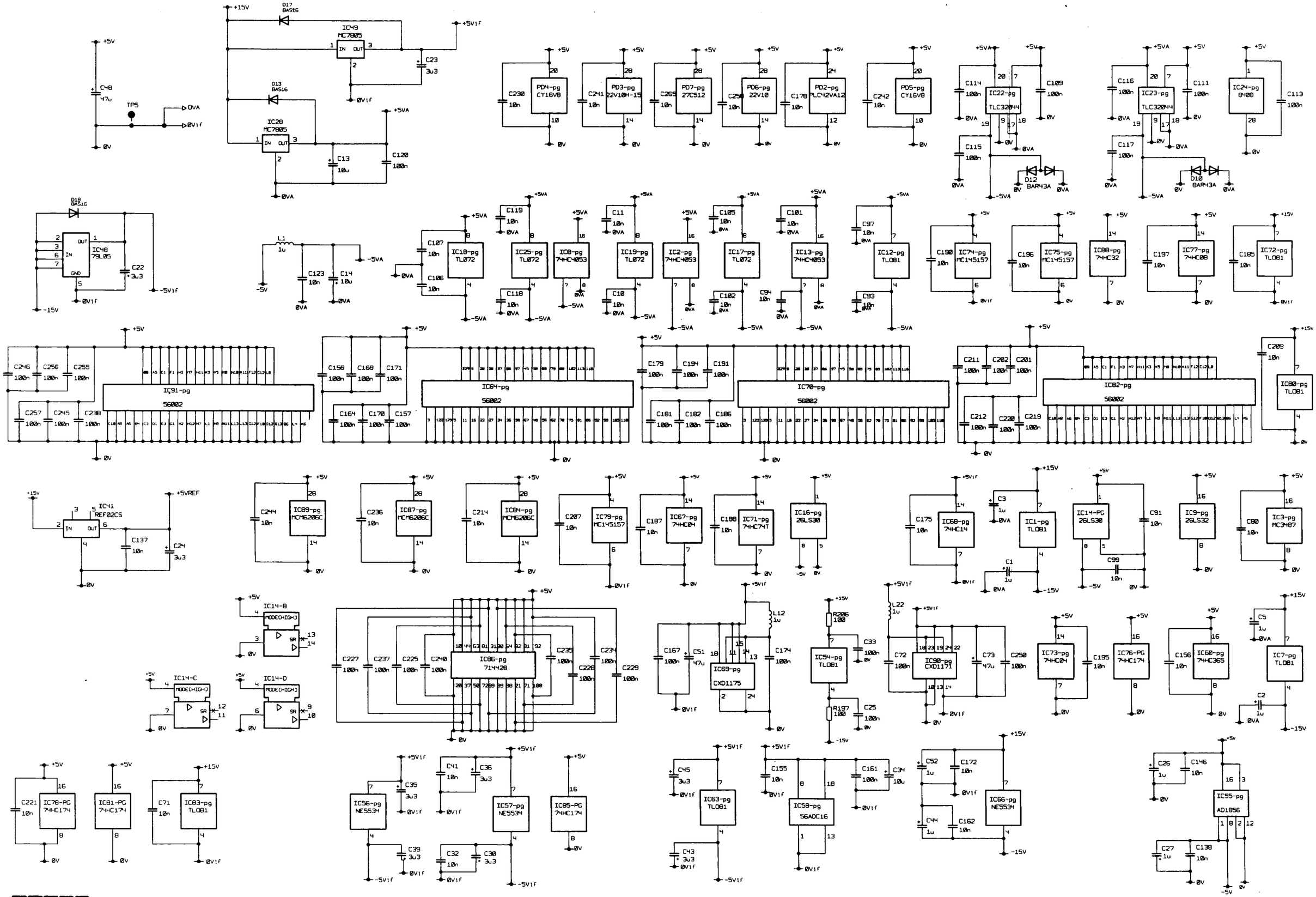
Pulse Shaper
L11 10u
C53 10n
R22 470
R23 470
R27 2k2
C60 10n
TR22 2N2369

IC71-b 74HC74T
6.144MHz (SHT 2)
12.288MHz (SHT 1)



RACAL
A5258/91217/6/4

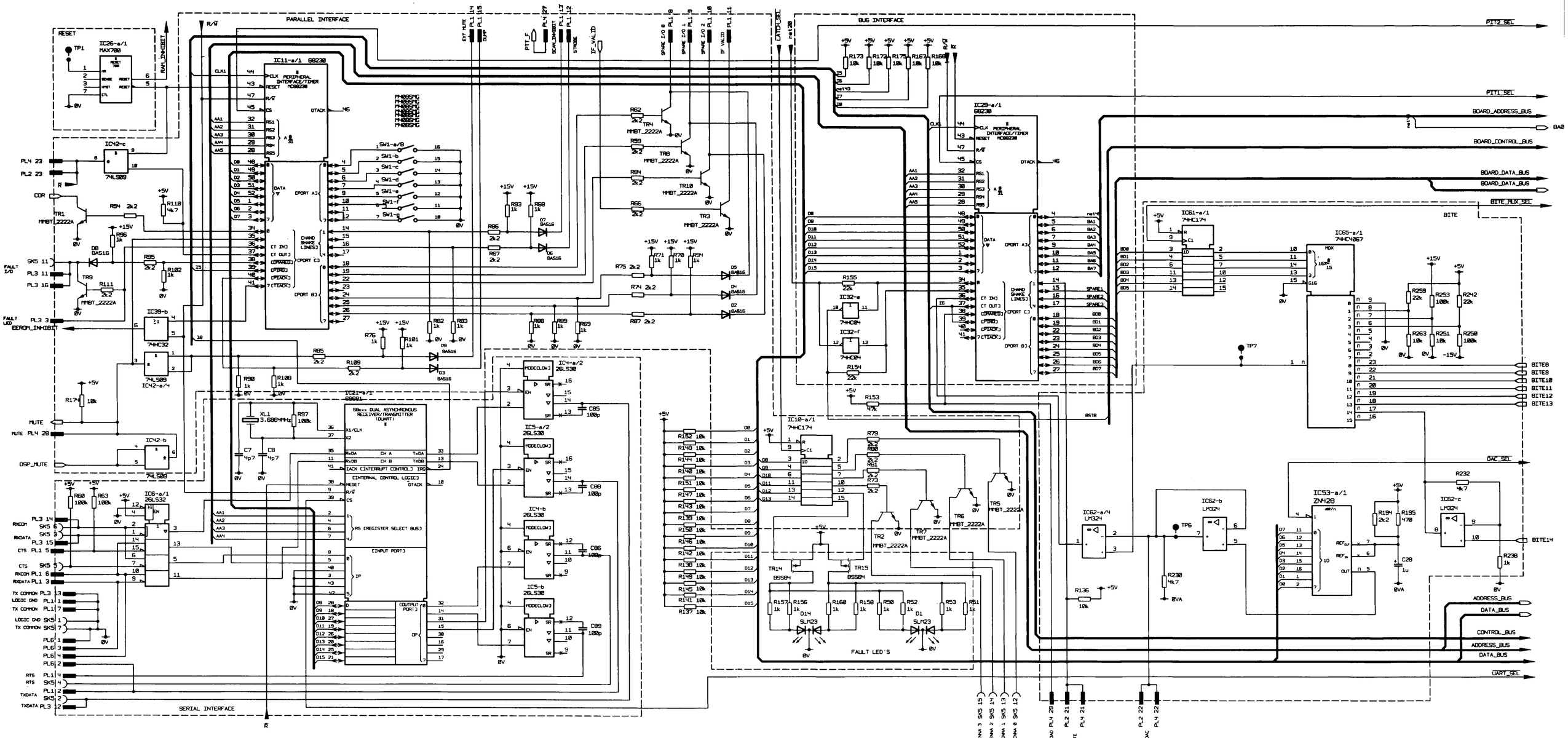
Circuit: Digital Board (Sheet 6) Fig. 7.9



RACAL

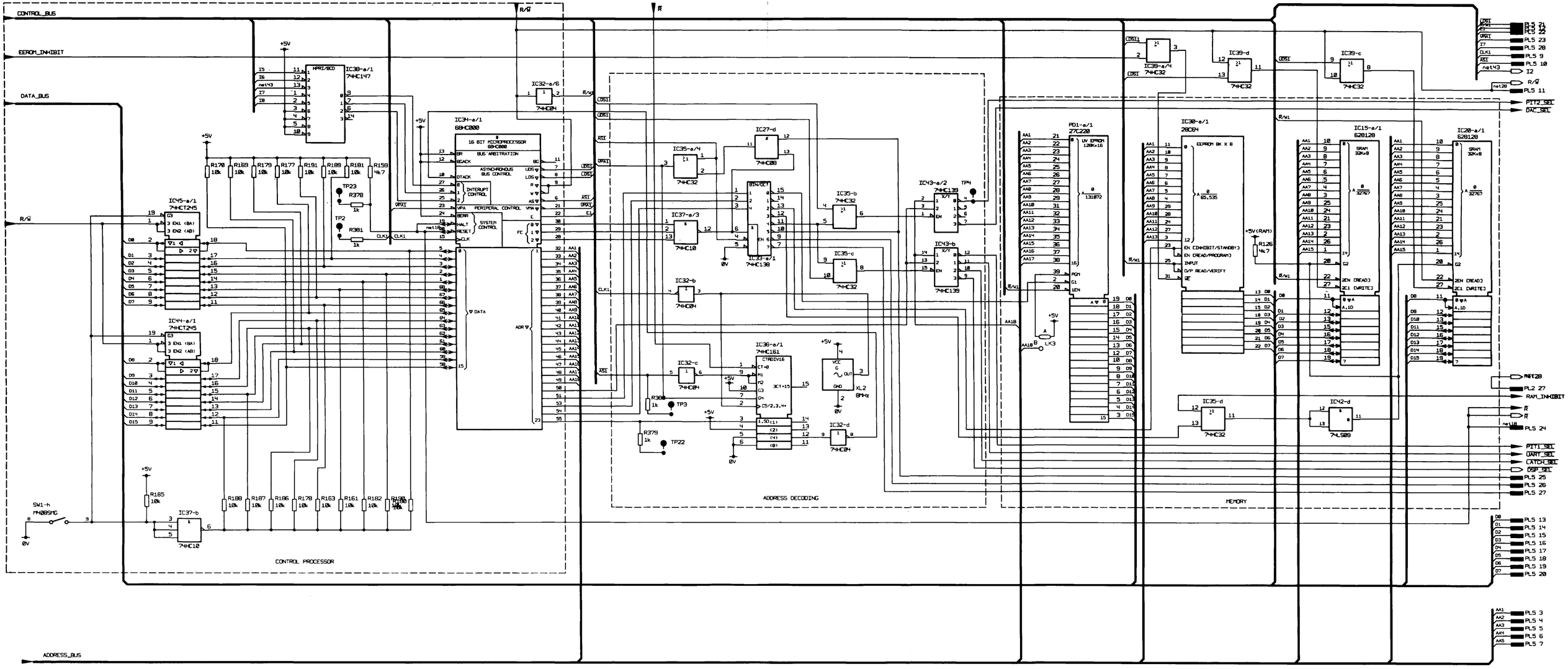
A5258/91217/7/4

Circuit: Digital Board (Sheet 7) Fig. 7.10



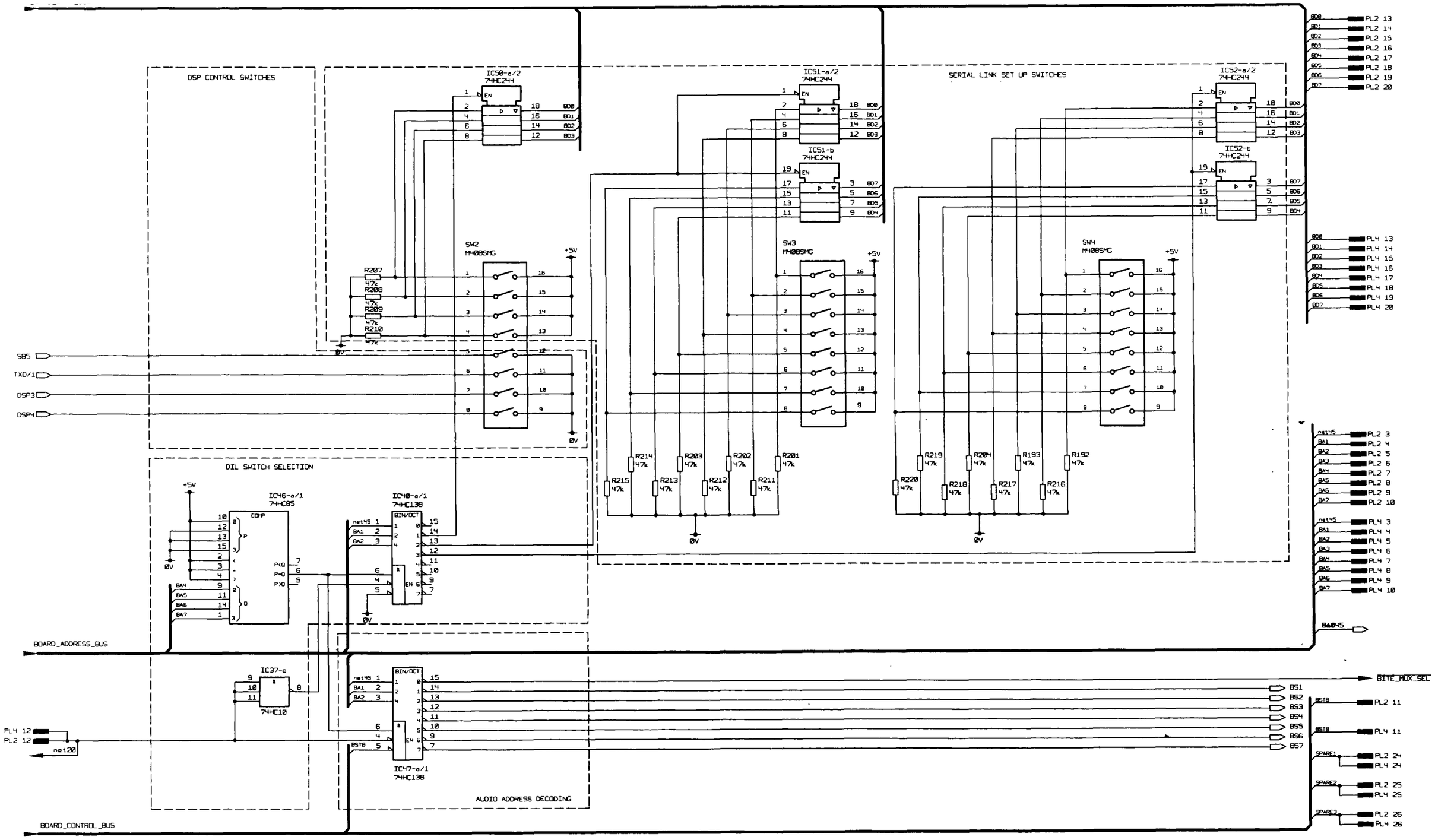
RACAL
A5258/91217/8/4

Circuit: Digital Board (Sheet 8) Fig. 7.11



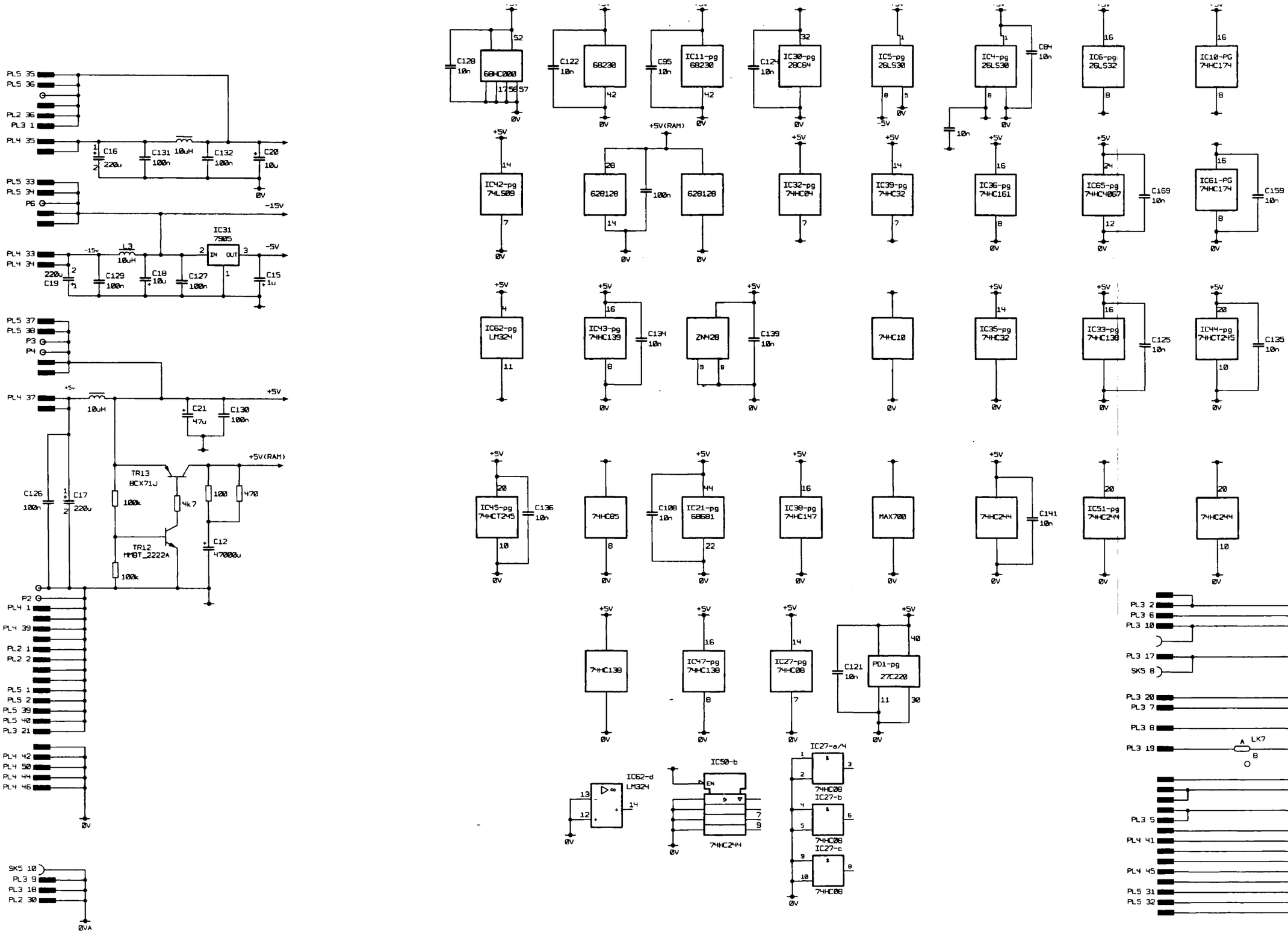
RACAL
A5258/91217/9/4

Circuit: Digital Board (Sheet 9) Fig. 7.12



RACAL
A5258/91217/10/4

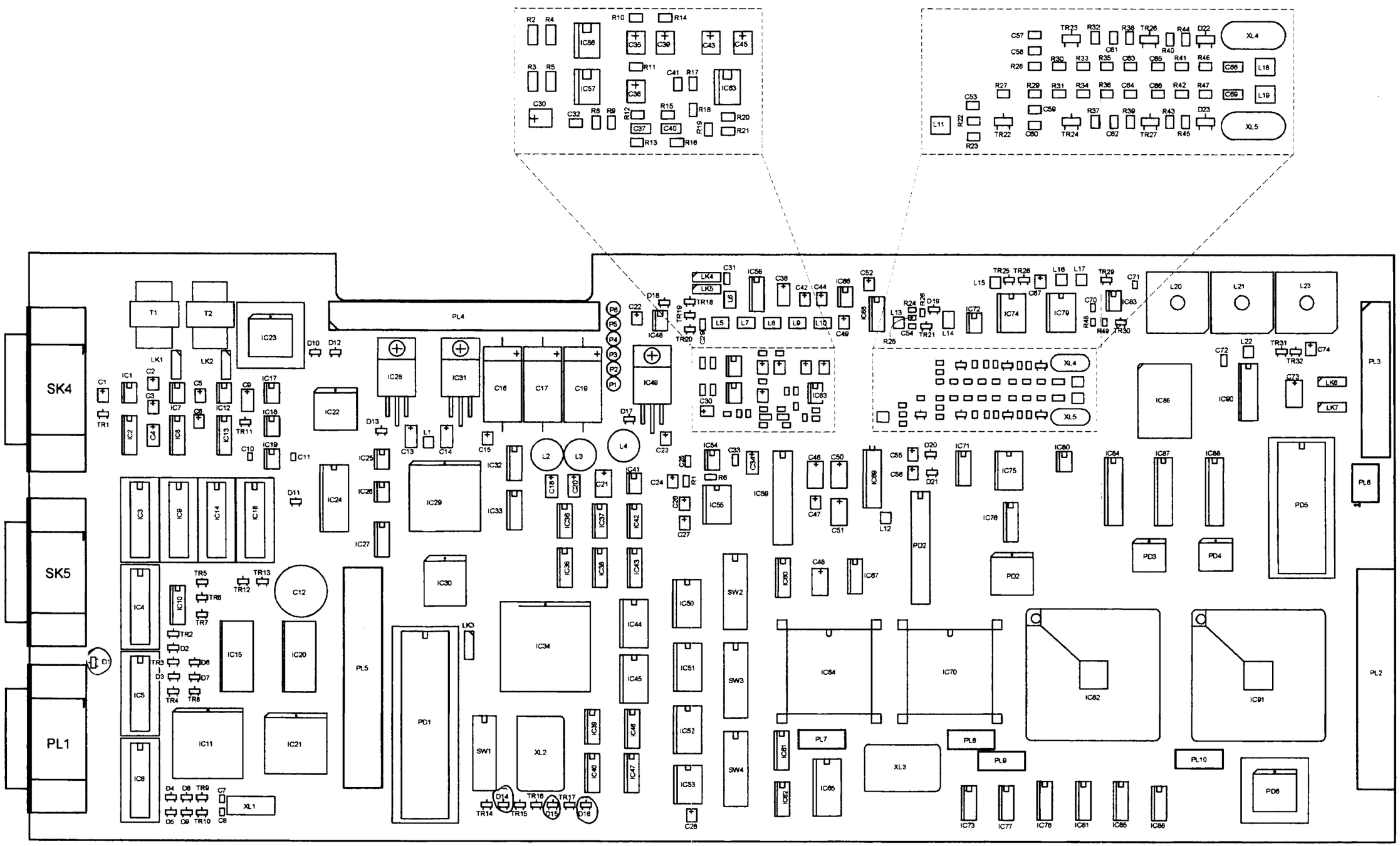
Circuit: Digital Board (Sheet 10) Fig. 7.13



RACAL

A5258/91217/11/4

Circuit: Digital Board (Sheet 11) Fig. 7.14



RACAL

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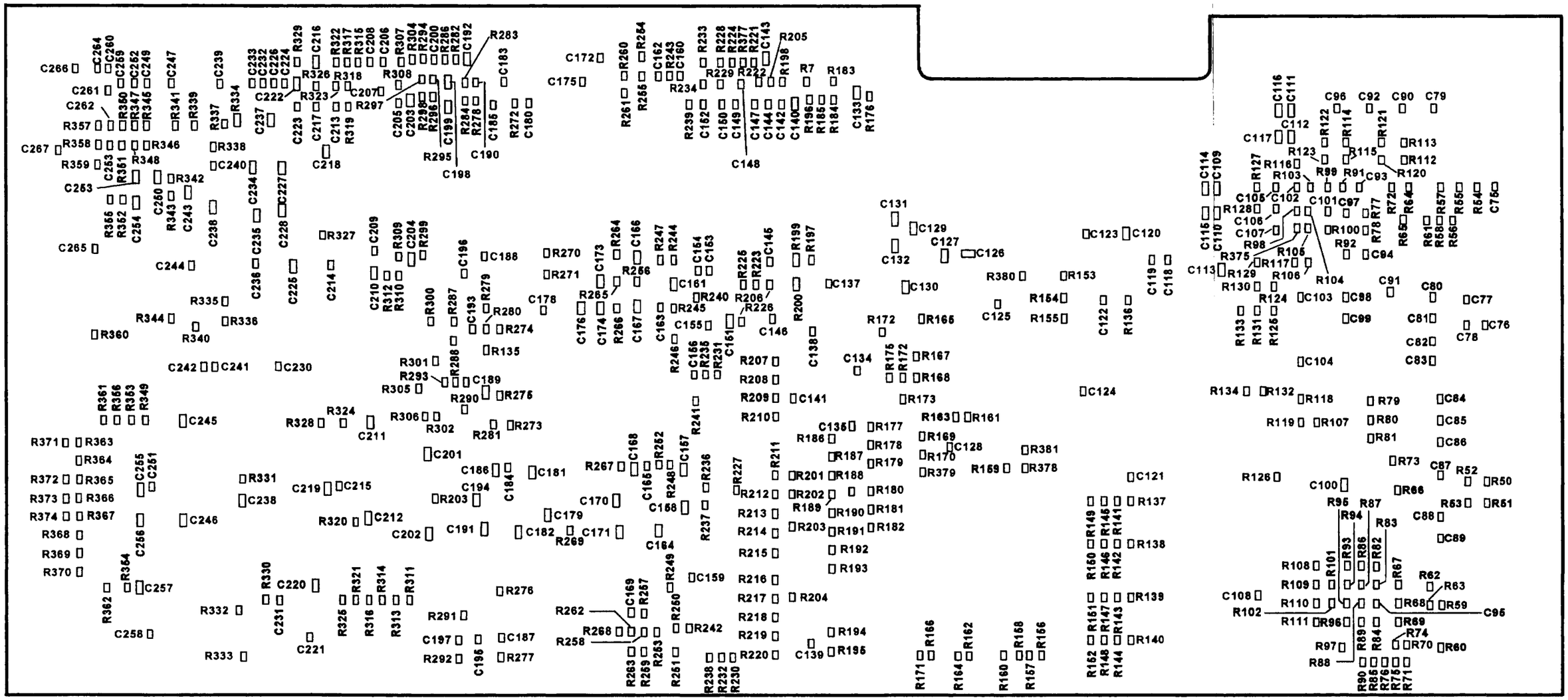
Layout: Digital Board (Side 1)

Fig. 7.15



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A5258

Layout: Digital Board (Side 2)

Fig. 7.16

CHAPTER 8

FREQUENCY STANDARD

CONTENTS

Illustrations

CHAPTER 8

FREQUENCY STANDARD

INTRODUCTION

1. One of three types of 10 MHz Frequency Standard Module may be fitted to the receiver, dependent on operational requirements and the degree of stability required. Additionally, either of the two lowest stability frequency standard modules, (1) and (2) below, may be fitted to the Analogue Board. Alternatively, either of the two higher stability frequency standard modules, (2) and (3) below, may be supplied, fitted to a separate Frequency Standard Board.

FREQUENCY STANDARD MODULES

2. The three types of 10 MHz Frequency Standard module are listed below:

   (1) A01214 Temperature Compensated Crystal Oscillator (TCXO)
   ± 7 parts in 10^7 over the range -10° C to +55° C

   (2) A10211 Oven Controlled Crystal Oscillator (OCXO)
   ± 1 part in 10^7 over the range -10° C to +55° C. Ageing ± 2 parts in 10^8 per day after 24 hours continuous operation.

   (3) A00982 High Stability Oven Controlled Crystal Oscillator (OCXO)
   ± 3 parts in 10^8 over the range -10° C to +55° C. Ageing ± 5 parts in 10^{10} per day after three months continuous operation.

FREQUENCY STANDARD BOARD

3. The Frequency Standard Board, Fig. 8.1, can accomodate either of the two higher stability frequency standard modules, (2) or (3) above. For both high stability modules, fine adjustment of frequency is achieved by means of a variable resistor (R1) mounted on the Frequency Standard Board.

4. The 10 MHz output from the frequency standard module is applied to buffer amplifier TR1, and the output is routed to the Analogue Board via a coaxial cable. This coaxial cable is also used to route the +12 V supply for the frequency standard board from the Analogue Board.

FAULT LOCATION

5. Fault location is limited to checking the availability of the +12 V supply and the operation of the buffer amplifier stage TR1. The frequency standard itself is not a user serviceable item and it should be replaced if found to be faulty.

ADJUSTMENT

6. The adjustment procedure for the Frequency Standard Module is as follows.

Test Equipment

7. The following items of test equipment are required for adjusting the Frequency Standard Module:

   (1) Frequency Counter: 0.01 Hz resolution (100 ms gate time)
   Input impedance 50 ohms

   (2) Reference Frequency Standard (accuracy ± 1 part in 10^9).

Frequency Adjustment

8. Ensure that the frequency standard selection switches are set for INTERNAL frequency standard and 10 MHz standard output.

9. Connect the receiver external standard output to the A input of the frequency counter.

10. Connect the reference frequency standard to the external standard input on the frequency counter and ensure that the frequency counter is locked to this input.

11. Using the correct trimming tool, adjust the frequency standard control so that the frequency is within the limits specified below:

12. **A01214 TCXO Standard**

   (1) Allow 15 minutes warm up
   (2) Adjustment accuracy: 10MHz ±1 Hz

13. **A01211 OCXO Standard**

   (1) Allow 15 minutes warm up
   (2) Adjustment accuracy: 10MHz ±0.1 Hz

14. **A00982 Hi-Stab OCXO Standard**

   (1) Allow 30 minutes warm up
   (2) Adjustment accuracy: 10MHz ±0.01Hz

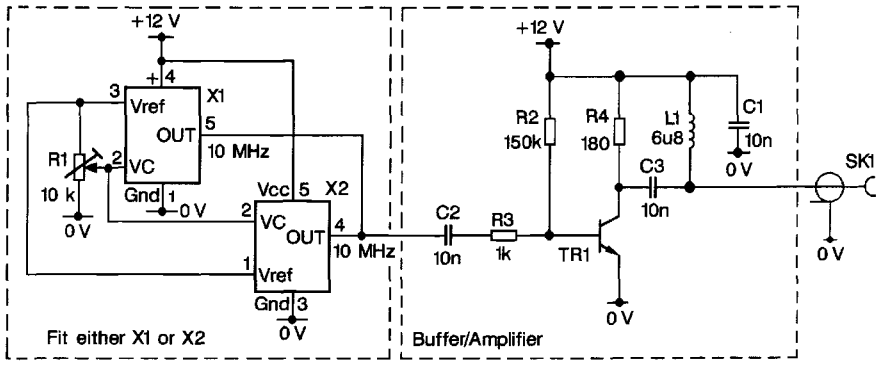
COMPONENTS LIST

FREQUENCY STANDARD BOARD

Assembly Part Number: 91299-01

Drawing Number: CA91299 Issue 01

REF	DESCRIPTION	PART No
Capacitors		
C1	CAP 10 N 10% 50 V CER P-M	940315
C2	CAP 10 N 10% 50 V CER P-M	940315
C3	CAP 10 N 10% 50 V CER P-M	940315
Inductors		
L1	INDUCTOR 680 NH 10%	940961
Modules		
X1	OSCILLATOR 10 MHZ OVEN CONT 12 V Hi Stab	A00982
X2	OSCILLATOR 10 MHZ OVEN CONT12 V	A01211
Resistors		
R1	RES-VAR 10 K	990691/EQ
R2	RES 150 K 2% 0.25 W METOXDE	
R3	RES 1 K 2% 0.25 W METOXDE	913489/EQ
R4	RES 180 2% 0.25 W METOXDE	
Sockets		
SK1	CONN 50 OHM SMB P FX SNP STRT	937091/EQ
Transistors		
TR1	TRANS G.PURPOSE N 2N2222 500M	910086/EQ



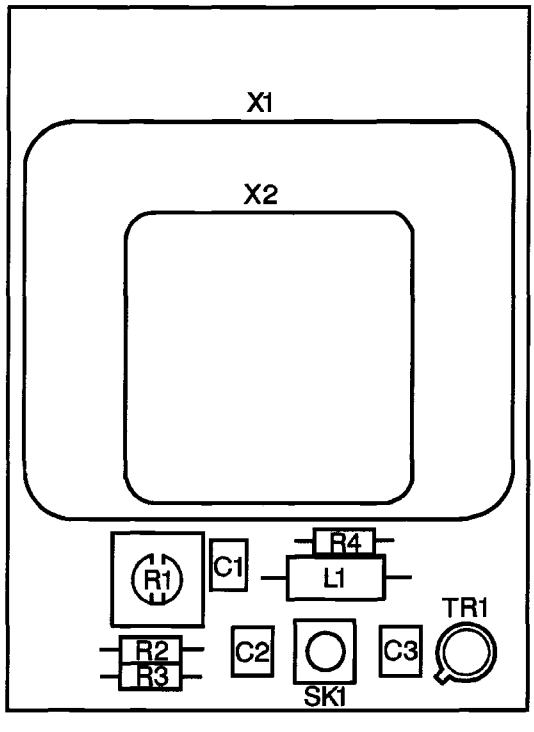


Fig 8.1 Circuit & Layout: Frequency Standard Board

CHAPTER 9

FRONT PANEL ASSEMBLIES

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Tables

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CHAPTER 9

FRONT PANEL ASSEMBLIES

INTRODUCTION

1. For the RA3791, RA3792 and MA3790 the front panel assembly contains all the necessary controls and displays to allow for operator control of the equipment. Audio amplifiers for driving the loudspeaker and phone outlets are also provided as well as the means for adjusting the backlighting intensity of the displays.

2. For the RA3793 and RA3794 receivers a blank front panel assembly is fitted to provide audio monitoring and fault indication facilities. For both types of front panel, the required electronic components are contained on a printed circuit board mounted behind the front panel.

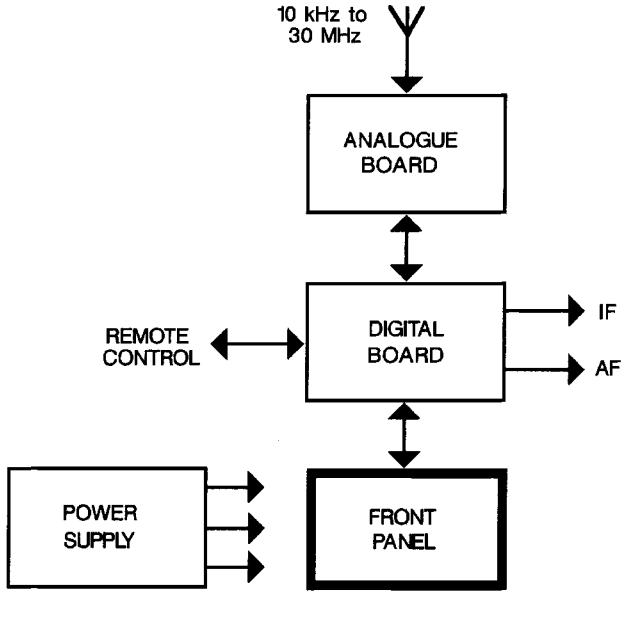


Fig. 9.1 Receiver Block Diagram

RA3791/RA3792/MA3790 FRONT PANEL ASSEMBLY DESCRIPTION

3. The following description should be read in conjunction with the appropriate front panel block and circuit diagrams included at the end of the chapter. Component references shown on the block diagram allow it to be related to the circuit diagram. Sheet numbers refer to those of the relevant circuit diagram.

Tuning Control (Sheet 2)

4. The front panel tuning control is mechanically linked to a shaft encoder (the main tuning control knob). This produces a series of pulses which are routed to the interface circuit via pins P2 and P4.

5. The interface circuit uses the phase relationship of these pulses to detect the direction of rotation of the tuning knob and translates the pulses into a form suitable to be read by a processor on the digital board.

6. The pulses produced by the shaft encoder, together with up/down information, are used to drive an 8-bit counter (IC15, IC16). When the processor requires frequency tuning data it momentarily stops the counters, via IC10(c), and enables buffer IC14 to read the count value and apply it to the data bus.

7. The timing diagrams in Fig. 9.2 illustrate how the interface circuit produces the clock and up/down inputs for the counters for both clockwise and anticlockwise rotation of the shaft encoder.

8. IC10(a) and (b), R52 and C31 generate a clock pulse for a change in state of either pulse waveform from the shaft encoder and this is used to clock both latch IC11(b) and the counters. IC11 pin 12 is subjected to the same time delay as the clock to ensure the correct logic level is latched for the corresponding clock pulse.

9. The output waveform of IC11(b) is dependent upon the direction of rotation of the shaft encoder. From the timing diagrams it can be seen that the waveform is identical to that at IC10(b) for an anticlockwise rotation and the inverse for a clockwise rotation. When either of the two waveforms from the latch is exclusive OR-gated with the output of IC10(b), the result is a steady low for an anticlockwise rotation and a steady high for a clockwise rotation.

Switch Interface (Sheet 1)

10. The pushbutton switches on the front panel are connected as a six-row (X) by eight-column (Y) switch matrix to enable the closure of any switch to be detected. In response to select data on the address bus from the processor, a row select decoder (IC8) causes a 0 V signal to be applied, in turn, to each row line. A depressed pushbutton routes this 0 V signal via one of eight return lines into a switch select buffer (IC4) to be read out onto the data bus when selected by the address decoder. Hence, a coded output is returned to the processor to indicate which switch is pressed. Any coded outputs resulting from the simultaneous closure of more than one switch are rejected by the processor, thereby preventing invalid operation.

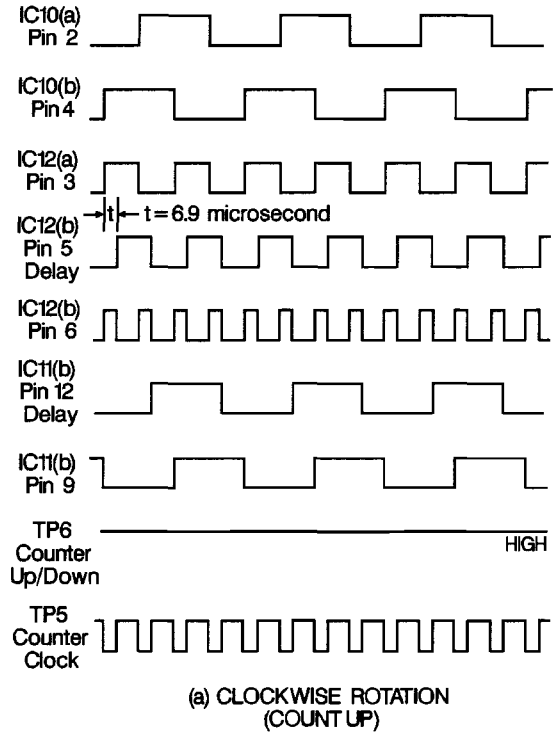


Fig. 9.2 Timing Diagram: Tuning Control

Displays (Sheet 1)

11. The liquid crystal display modules are connected directly to the data bus, via W1 (frequency), W2 (bar graph) and W3 (dot matrix).The display modules are supplied with a low frequency square wave signal from IC1 of the backlighting control circuitry; this is required by the internal driver devices to drive the LCD modules.

12. For the frequency and bargraph display modules, all the coded display information is sent serially in 20 bytes on the data bus whenever the display requires modification. The 2-bit bytes for the bargraph display module are loaded into an internal shift register by a negative-going strobe pulse on the port 2 line from the address decoder (W2 pin 4). Similarly, the 6-bit wide bytes for the frequency display module are loaded by a strobe pulse on port 4 (W1 pins 5, 6 and 19). The data is latched from the internal shift registers to the displays by a write strobe pulse on W2 pin 3 and W1 pin 1 respectively.

13. In the dot matrix display module the mode legends are driven by data written into the external data latch IC6. The 2 x 20 dot matrix characters are driven by internal processing circuits incorporating a character generator. Instruction bytes on the data bus are loaded into a register in the processing circuits by a low on W3 pin 17 in order to define the display configuration. W3 pin 17 then goes high followed by a strobe pulse on W3 pin 15, which allows data now present on the data bus to set up the character generator and display the required character. Because the dot matrix displays are multiplexed, a narrower viewing angle results, but this can be adjusted using the menu system. This is achieved by means of a control voltage derived from digital-to-analogue conversion of data received on the data bus.

Backlighting Control (Sheet 1)

14. The backlighting control circuit (IC2) allows the backlighting intensity of the displays to be adjusted from the front panel, using the menu system, and is powered from the +5 V supply. The circuit consists basically of a pulse width modulator (PWM) connected to drive circuits which control the supply to the backlighting bulbs. A feedback control loop allows the intensity to be stabilised at one of eight possible brightness settings from data received on the data bus.

15. When a variable DC voltage is applied to IC2 pin 2, the pulse width of the output waveform is varied accordingly, and this is used to vary the intensity of the backlighting.

Audio Outputs (Sheet 2)

16. A pair of audio amplifiers (IC18, IC19) receives the audio input signal via a volume control on the front panel, which is adjusted for the desired audio level at the loudspeaker and phone outputs. Muting of the audio output to the loudspeaker occurs when the mute line is activated by the processor, in response to the loudspeaker pushbutton on the front panel being operated.

Bus Interface (Sheet 1)

17. The address decoder (IC5, 9 & 13) detects addresses on the address bus from the processor to produce control signals for various functions throughout the assembly. These signals write data into the display modules and to a data latch, which provides control of a BITE signal and the illumination of legends displayed on the dot matrix display. The control signals also allow data from the tuning interface circuit and switch select buffer, as well as the assembly identification code, to be read by the processor via the data bus.

BITE Measurement System

18. The level of IF gain adjustment is measured using IC17 (Sheet 1). When not being used it is switched off by the processor, via TR4 and TR5 (Sheet 2). The level is measured by comparing the voltage at TP7 with the DAC input from connector W4 pin 22.

Fault Location

19. Fault location techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the front panel assembly is contained in the following sections.

BITE Tests

20. The following BITE tests for the front panel assembly are arranged in the order in which they are performed or presented for selection. For information on using BITE refer to Chapter 3.

TEST NUMBER: 151

Title: Displays Test

Performed: Select test

Description: Using test patterns, all the front panel displays are tested in the following sequence:

(1) 'Testing Character Display' message shown for four seconds to indicate display under test and all legends blanked.

(2) Complete display exhibits a 'checkerboard' pattern for one second and then turns on each legend at one second intervals.

(3) Each legend is then turned off in the same order at one second intervals.

(4) 'Testing Frequency Display' message shown for two seconds and all legends blanked.

(5) All address, channel and frequency displays are sequenced through the range of digits, from 0 to 9, with each set held for two seconds.

(6) Display is then blanked and each legend is turned on, one by one, at one second intervals.

(7) Each legend is then turned off in the same order at one second intervals.

(8) 'Testing Bargraph Display' message shown for two seconds, then each legend is illuminated in turn for one second.

(9) The AF and RF meter scales are each activated to on for one second in turn. The bars are illuminated from left to right with a 0.25 second gap between bars, and then extinguished in reverse order.

TEST NUMBER: 152

Title: Keyboard Test

Performed: Select test

Description: Each key is tested when pressed by the operator in response to the message 'Press the * * * * key,' where * * * * is the key to be pressed. The test fails if the wrong key is pressed.

Fault Directory

21. Use the fault directory given in Table 9.1 to identify the fault condition and take the necessary corrective action. Note that all inputs to the assembly are assumed to be correct.

Table 9.1 Fault Directory: RA3791/92/MA3790 Front Panel Assembly

Fault No.	Fault Symptom	Possible Causes	Suggested Action
1	Fails to run BITE tests for Front Panel Assembly	Address decoder/ assembly ident. not responding	Check address decoding/ assembly ident logic operation using signature analysis routine if necessary
2	Power supply fault within module	Faulty component drawing excess current	Locate and replace faulty component
3	All displays inoperative	(a) Address decoder fault	(a) Use signature analysis routine to trace fault
		(b) Backlighting drive waveform absent	(b) See Fault No. 5
4	Fault confined to individual display	(a) Display module faulty	(a) Replace suspect display module
		(b) Address decoder fault	(b) As Fault No. 3
5	No backlighting	Backlighting control circuit faulty	Follow backlighting control check procedure
6	No audio output	(a) Audio amplifier fault	(a) Check both loudspeaker and phones outputs to establish if fault is common to both amplifiers. Check signal levels around suspect circuit
		(b) Audio input absent	(b) Check audio is being applied to the volume control
		(c) Faulty volume control	(c) Check operation.
		(d) Mute activated	(d) Operate L/S button and check that logic 1 can be obtained at IC17(b) pin 14
7	No response to pressing any key	Faulty switch select buffer or row select decoder	Use signature analysis routine to check circuit action
8	Failure of individual or group of switches	Faulty switch matrix, switch select buffer or row select decoder	See Fault No. 7
9	Tuning knob stiff	Excessive tuning knob friction	Remove knob and adjust preset screw located behind it
10	No response from rotating main tuning knob	(a) Faulty shaft encoder	(a) Check output waveforms present on P2 and P4
		(b) Interface circuit inoperative	(b) Check for pulses on TP5 and for changing level on TP6 as direction of rotation is changed. Using oscilloscope, check counter outputs toggle when tuning knob is rotated.
11	Unable to control viewing angle of dot matrix display	(a) Faulty latch	(a) Using oscilloscope, check IC3 view angle control output varies when the view angle is varied via the menu system.
		(b) Faulty display module	(b) Replace
12	Unable to control IF gain	Faulty potentiometer or bias circuit.	Check 2.8V is applied to potentiometer. Locate and replace faulty component.

Signature Analysis Routine

22. This routine checks that the control signals are interfaced and decoded correctly from the board bus.

IMPORTANT : Only the front panel should be connected to the digital board during this test. Disconnect the analogue board (if fitted) at PL4 on the digital board. Disconnect the loudspeaker at PL1.

23. Digital board SW1 DIL switch settings:

2, 4, 7	OFF
1, 5-6, 8	ON

24. Signature analyser connection and settings:

Start:	PL4-9 on digital board, negative trigger.
Stop:	PL4-9 on digital board, negative trigger.
Clock:	PL4-11 on digital board, positive trigger.
Earth:	TP5 on digital board

Table 9.2 Signature Analysis

Signal	Signature	Test Node
+5V	1CAU	IC5-14
0V	0000	IC5-7
D0	1H4U	W1-13 W2-2 W3-16 W4-13 IC3-3 IC4-18 IC6-3 IC14-18 IC17-1
D1	2UPU	W1-4 W2-13 W3-13 W4-14 IC3-4 IC4-16 IC6-4 IC14-16
D2	72C5	W1-3 W3-14 W4-15 IC3-7 IC4-14 IC6-7 IC14-14
D3	39H1	W1-15 W3-11 W4-16 IC3-8 IC4-12 IC6-8 IC14-12
D4	1FU8	W1-17 W3-12 W4-17 IC3-13 IC4-9 IC6-13 IC14-9
D5	F5C1	W1-20 W3-9 W4-18 IC3-14 IC4-7 IC6-14 IC14-7
D6	1FC8	W3-10 W4-19 IC3-17 IC4-5 IC6-17 IC14-5
D7	4HUC	W3-7 W4-20 IC3-18 IC4-3 IC6-18 IC14-3
A0	5H68	W4-3 IC9-1 IC13-2
A1	7483	W4-4 IC8-11 IC9-2 IC13-13
A2	1C83	W4-5 IC8-10 IC9-3
A3	9A8C	W4-6 IC8-9 IC13-14 W3-17
A4	0000	W4-7 IC5-10
A5	0001	W4-8 IC5-9
A6	0001	W4-9 IC5-1
A7	0001	W4-10 IC5-2
M-STB	0000F	W4-11 IC7-1

Table 9.2 Signature Analysis (cont.)

Signal	Signature	Test Node
IC7-2	1CAUF	IC7-2 IC9-6
IC5-3	0001	IC5-3 IC5-4
IC5-8	0001	IC5-8 IC5-5
IC5-6	0001	IC5-6 IC9-4 IC13-1
IC13-6	1CAU	IC13-6 IC13-15
IC13-11	1CAU	IC13-11 IC14-1 IC14-19
IC13-12	1CAUF	IC13-12 IC17-7
PORT0	3696	IC6-11 IC9-15
PORT1	8PAA	IC10-13 IC9-14
PORT2	4970	W2-4 IC9-13
PORT3	U160	IC10-11 IC9-12
PORT4	PP14	W1-6 W1-5 W1-19 IC9-11
PORT5	3904	IC10-9 IC9-10
PORT6	H735	IC3-11 IC9-9
IC13-7	1CAUF	IC13-7 IC4-1 IC4-19
IC10-8	22AC	IC10-8 W1-1
IC10-10	PAFU	IC10-10 W2-3
IC10-12	9505	IC10-12 W3-15
IC3-2	1H4U	IC3-2
IC3-5	0001	IC5-5
IC3-6	U13F	IC3-6
IC3-9	295H	IC3-9 IC17-8
IC3-12	3CCF	IC3-12
IC3-15	32FF	IC3-15
IC3-16	3674	IC3-16
IC4-2	1CAU	IC4-2
IC4-4	1CAU	IC4-4
IC4-6	1CAU	IC4-6
IC4-8	1CAU	IC4-8
IC4-11	1CAU	IC4-11
IC4-13	1CAU	IC4-13
IC4-15	1CAU	IC4-15
IC4-17	1CAU	IC4-17

Table 9.2 Signature Analysis (cont.)

Signal	Signature	Test Node
IC6-2	9357	IC6-2
IC6-12	PFPU	IC6-12 W3-2
IC6-15	68AH	IC6-15 W3-1
IC6-16	2A8F	IC6-16 W3-4
IC6-19	0C9F	IC6-19 W3-4
IC8-13	0000F	IC8-13
IC8-14	0000F	IC8-14
IC8-15	0000F	IC8-15
IC8-12	0000F	IC8-12
IC8-1	0000	IC8-1
IC8-5	0000F	IC8-5

Diagnostic Connector

25. Details of the two diagnostic connectors, SK1 for Receiver 1 and SK2 for Receiver 2, on the front panel, are given below.

Pin	Connection
1	Digital Ground
2	Tx Data
3	Rx Data
4	NC
5	NC
6	Rx Common
7	Tx Common
8	Monitor Audio
9	External Audio
10	Analogue Ground
11	Fault I/O
12	NC
13	NC
14	NC
15	NC

RA3793/RA3794 BLANK FRONT PANEL ASSEMBLY DESCRIPTION

26. The following description should be read in conjunction with the appropriate circuit diagrams included at the end of this chapter.

Audio Monitoring

27. For the dual receiver, the audio signal is routed to a selector switch (connected to pins P1, P2 and P3) which selects either Receiver 1 or Receiver 2. The audio signal is routed via the volume control potentiometer to the audio amplifier (IC1) and then to the phones socket. For the single receiver, the selection switch is replaced with a wired connection between P1 and P2.

Fault Indicators

28. Visual indication of a fault condition detected by the receiver BITE system is provided by light emitting diodes (D3, D1) mounted on the front panel. The FAULT 1 LED (D3) is used to indicate a fault in a single receiver or receiver 1 in a dual receiver. The FAULT 2 LED (D1) is used solely in the RA3794 dual receiver (not fitted to the RA3793) to indicate a fault in receiver 2.

Fault Finding

29. Fault finding techniques and recommended test equipment are described in Chapter 2.

Fault Directory

30. Use the following fault directory (Table 9.3) to identify the fault condition and take the necessary corrective action. Note that all inputs to the assembly are assumed to be correct.

Table 9.3 Fault Directory: RA3793/94 Blank Front Panel

Fault No.	Fault Symptom	Possible Causes	Suggested Action
1	No audio output	(a) Audio amplifier faulty	(a) Check signal levels around suspect amplifier
		(b) Audio input absent	(b) Check audio is being applied to the volume control
		(c) Faulty volume control	(c) Check operation
2	Fault LED fails to indicate a fault condition	(a) LED or driver faulty	(a) Check voltage levels
		(b) Data latch faulty	(b) Check output and control lines using oscilloscope

Diagnostic Connector

31. SK1 connections are as given above in para. 25.

COMPONENTS LISTS

FRONT PANEL MODULE ASSEMBLY RA3791/92/MA3790
DRG. No.DA91224 ISSUE 1B
PART No. 91224-01

ITEM	PART No.	DESCRIPTION	QTY
1	91223-03	ASSY-PCB FRONT PANEL	1
2	91258-01	PANEL FRONT OVERLAY	1
4	91314-01	ASSY-CABLE 3-WAY	1
7	91264-03	ASSY-CABLEFORM	1
22	87107/002-01	HANDLE	2
30	A01663	SWITCH ROCKR DPST 16A U O-OFF	1
58	923509	CONN 2-WAY S FX	1
64	945513	LOUDSPEAKER 80 OHM 2W	1
94	925767	KNOB .250 COL BK	2
95	A00955	KNOB .25 47.0 COL BK	1
99	926887	CAP KNOB 15MM BK PLAIN	2
100	A00956	CAP KNOB 47 MM BK RECESSED	1

FRONT PANEL BOARD ASSEMBLY RA3791/92/MA3790
PART No. 91223-03
DRAWING No.DA91223 ISSUE 3

REF	DESCRIPTION								PART No.
CAPACITORS									
C1		33	U	T%	40	V	ALU	TAC-	945205
C2		220	U	T%	25	V	ALU	TAC-	921536/EQ
C3	CHIP	10	N	10%	100	V	CER	X	999155/103P
C4	CHIP	10	N	10%	100	V	CER	X	999155/103P
C5	CHIP	1	N	5%	50	V	CER	C	999154/102P
C6	CAP	220	U	T%	25	V	ALU	TAC-	921536/EQ
C7	CHIP	10	N	10%	100	V	CER	X	999155/103P
C8		220	U	T%	25	V	ALU	TAC-	921536/EQ
C9	CHIP	4.7	N	5%	50	V	CER	X	999151/472P
C10	CHIP	10	U	20%	25	V	TAN		Y00643
C11	CHIP	100	N	10%	50	V	CER	X	948163
C12	CHIP	10	U	20%	25	V	TAN		Y00643
C13	CHIP	10	N	10%	100	V	CER	X	999155/103P
C14	CHIP	100	N	10%	50	V	CER	X	948163
C15	CHIP	100	N	10%	50	V	CER	X	948163
C16	CHIP	10	N	10%	100	V	CER	X	999155/103P
C17		220	U	T%	25	V	ALU	TAC-	921536/EQ
C18	CHIP	10	N	10%	100	V	CER	X	999155/103P
C19	CHIP	10	N	10%	100	V	CER	X	999155/103P
C20	CHIP	10	N	10%	100	V	CER	X	999155/103P
C21	CHIP	10	N	10%	100	V	CER	X	999155/103P
C22		33	U	T%	40	V	ALU	TAC-	945205
C23		220	U	T%	25	V	ALU	TAC-	921536/EQ
C24	CHIP	100	N	10%	50	V	CER	X	948163
C25	CHIP	100	N	10%	50	V	CER	X	948163
C26	CHIP	10	N	10%	100	V	CER	X	999155/103P
C27	CHIP	100	P	5%	50	V	CER	C	999154/101P
C28	CHIP	10	N	10%	100	V	CER	X	999155/103P
C29	CHIP	10	N	10%	100	V	CER	X	999155/103P
C30	CHIP	10	N	10%	100	V	CER	X	999155/103P

REF	DESCRIPTION								PART No.
C31	CHIP	100	P	5%	50	V	CER	C	999154/101P
C32	CHIP	10	N	10%	100	V	CER	X	999155/103P
C33	CHIP	100	N	10%	50	V	CER	X	948163
C34	CHIP	100	N	10%	50	V	CER	X	948163
C35	CHIP	10	N	10%	100	V	CER	X	999155/103P
C36	CHIP	10	N	10%	100	V	CER	X	999155/103P
C37	CHIP	10	N	10%	100	V	CER	X	999155/103P
C38	CHIP	10	N	10%	100	V	CER	X	999155/103P
C39	CHIP	10	U	20%	25	V	TAN		Y00643
C40	CHIP	100	N	10%	50	V	CER	X	948163
C41	CHIP	10	U	20%	25	V	TAN		Y00643
C42	CHIP	100	N	10%	50	V	CER	X	948163
C43		330	U	T%	25	V	ALU	TAC-	945006
C44	CHIP	18	P	5%	50	V	CER	C	999154/180P
C45	CHIP	18	P	5%	50	V	CER	C	999154/180P
C46	CHIP	100	N	10%	50	V	CER	X	948163
C47	CHIP	100	N	10%	50	V	CER	X	948163
C48		100	U	T%	25	V	ALU	TAC-	921546/EQ
C49	CHIP	100	N	10%	50	V	CER	X	948163
C50	CHIP	10	U	20%	25	V	TAN		Y00643
C51	CHIP	1	N	5%	50	V	CER	C	999154/102P
C52	CHIP	10	N	5%	50	V	CER	X	999151/103P
C53	CHIP	1	N	5%	50	V	CER	C	999154/102P
C54	CHIP	10	N	5%	50	V	CER	X	999151/103P

DIODES

D1	SWITCHG (A4)	BAV70 70V	999208/MC
D2	REF	BZX84-C5V1	945108

INTEGRATED CIRCUITS

IC1	74HCT4040	12S BIN CNTR	948317
IC2	3524	LIN REG	Y00954
IC3	74HC273	CMS O DTP FLP FLOP	943989/SD
IC4	74HC244	CMS O BUF 3ST DRIV	999650/SD
IC5	74HC32	CMS Q 2IP OR GATE	999308/SD

REF	DESCRIPTION						PART No.
IC6	74HC377		CMS O DTP FLP FLOP				943990/SD
IC7	74HC14		CMS H INV SCHM				999334/SD
IC8	4051B		CMS S 8CH ANA MUX				999214/SD
IC9	74HC138		CMS 3/8 LNE DCDR				943980/SD
IC10	74HC14		CMS H INV SCHM				999334/SD
IC11	74HC74T		CMS D DTP FLP FLOP				999353/SD
IC12	74HC86		CMS Q EXC OR GATE				999365/SD
IC13	74HC139		CMS D 2-4 LNE DCDR				999331/SD
IC14	74HC244		CMS O BUF 3ST DRIV				999650/SD
IC15	4516		CMS S BIN U/D CNTR				945047/SD
IC16	4516		CMS S BIN U/D CNTR				945047/SD
IC17	339		LIN Q IND VOL COMP				945023/SD
IC18	380N		AUD AMP				929343
IC19	380N		AUD AMP				929343
INDUCTOR							
L1	CHOKE	10	UH	10%	RF		A00887
PINS							
P1	SE PSH SLD 1.02 BR TS						937625/EQ
P2	SE PSH SLD 1.02 BR TS						937625/EQ
P3	SE PSH SLD 1.02 BR TS						937625/EQ
P4	SE PSH SLD 1.02 BR TS						937625/EQ
PLUG							
PL1	3-WAY P FX R/A						943740
RESISTORS							
R1	VAR	10	K	20%	PNL	CP	A00918
R2	VAR	10	K	20%	PNL	CP	A00919
R3	CHIP	1	K	2%	0.063	W MF	999160/102R
R4	CHIP	47		2%	0.063	W MF	999160/470R
R5	CHIP	2.2	K	2%	0.063	W MF	999160/222R

REF	DESCRIPTION					PART No.
R6	CHIP 39		2%	0.063 W	MF	999160/390R
R7	CHIP 150		2%	0.063 W	MF	999160/151R
R8	CHIP 10	K	2%	0.063 W	MF	999160/103R
R9	CHIP 150		2%	0.063 W	MF	999160/151R
R10	CHIP 1	K	2%	0.063 W	MF	999160/102R
R11	CHIP 47		2%	0.063 W	MF	999160/470R
R12	CHIP 56	K	2%	0.063 W	MF	999160/563R
R13	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R14	CHIP 33	K	2%	0.063 W	MF	999160/333R
R15	CHIP 33	K	2%	0.063 W	MF	999160/333R
R16	CHIP 33	K	2%	0.063 W	MF	999160/333R
R17	CHIP 33	K	2%	0.063 W	MF	999160/333R
R18	CHIP 1		10%	0.125 W	MF	999183/109R
R19	CHIP 1		10%	0.125 W	MF	999183/109R
R20	CHIP 1		10%	0.125 W	MF	999183/109R
R21	CHIP 1		10%	0.125 W	MF	999183/109R
R22	CHIP 1		10%	0.125 W	MF	999183/109R
R23	CHIP 1		10%	0.125 W	MF	999183/109R
R24	CHIP 33	K	2%	0.063 W	MF	999160/333R
R25	CHIP 33	K	2%	0.063 W	MF	999160/333R
R26	CHIP 33	K	2%	0.063 W	MF	999160/333R
R27	CHIP 33	K	2%	0.063 W	MF	999160/333R
R28	CHIP 8.2	K	2%	0.063 W	MF	999160/822R
R29	CHIP 68	K	2%	0.063 W	MF	999160/683R
R30	CHIP 120	K	2%	0.063 W	MF	999160/124R
R31	CHIP 270	K	2%	0.063 W	MF	999160/274R
R32	CHIP 100	K	2%	0.063 W	MF	999160/104R
R33	CHIP 47	K	2%	0.063 W	MF	999160/473R
R34	CHIP 27	K	2%	0.063 W	MF	999160/273R
R35	CHIP 12	K	2%	0.063 W	MF	999160/123R
R36	CHIP 10	K	2%	0.063 W	MF	999160/103R
R37	CHIP 33	K	2%	0.063 W	MF	999160/333R
R38	CHIP 33	K	2%	0.063 W	MF	999160/333R
R39	CHIP 33	K	2%	0.063 W	MF	999160/333R
R40	CHIP 33	K	2%	0.063 W	MF	999160/333R

REF	DESCRIPTION					PART No.
R41	CHIP 33	K	2%	0.063 W	MF	999160/333R
R42	CHIP 33	K	2%	0.063 W	MF	999160/333R
R43	CHIP 33	K	2%	0.063 W	MF	999160/333R
R44	CHIP 33	K	2%	0.063 W	MF	999160/333R
R45	CHIP 33	K	2%	0.063 W	MF	999160/333R
R46	CHIP 33	K	2%	0.063 W	MF	999160/333R
R47	CHIP 33	K	2%	0.063 W	MF	999160/333R
R48	CHIP 33	K	2%	0.063 W	MF	999160/333R
R49	CHIP 33	K	2%	0.063 W	MF	999160/333R
R50	CHIP 33	K	2%	0.063 W	MF	999160/333R
R51	CHIP 68	K	2%	0.063 W	MF	999160/683R
R52	CHIP 68	K	2%	0.063 W	MF	999160/683R
R53	CHIP 33	K	2%	0.063 W	MF	999160/333R
R54	CHIP 33	K	2%	0.063 W	MF	999160/333R
R55	CHIP 33	K	2%	0.063 W	MF	999160/333R
R56	CHIP 33	K	2%	0.063 W	MF	999160/333R
R57	CHIP 2.2	K	2%	0.063 W	MF	999160/222R
R58	CHIP 10	K	2%	0.063 W	MF	999160/103R
R59	CHIP 33	K	2%	0.063 W	MF	999160/333R
R60	CHIP 33	K	2%	0.063 W	MF	999160/333R
R61	CHIP 10	K	2%	0.063 W	MF	999160/103R
R62	CHIP 10	K	2%	0.063 W	MF	999160/103R
R63	CHIP 2.2		5%	0.125 W	MF	999158/229R
R64	CHIP 1	K	2%	0.063 W	MF	999160/102R
R65	CHIP 1	K	2%	0.063 W	MF	999160/102R
R66	CHIP 33	K	2%	0.063 W	MF	999160/333R
R67	CHIP 10	K	2%	0.063 W	MF	999160/103R
R68	CHIP 2.2		5%	0.125 W	MF	999158/229R
R69	CHIP 22	K	2%	0.063 W	MF	999160/223R
R70	CHIP 68	K	2%	0.063 W	MF	999160/683R
R71	CHIP 560		2%	0.063 W	MF	999160/561R
R72	CHIP 1.2	K	2%	0.063 W	MF	999160/122R

SWITCHES

S1	KEYBOARD PB MOM SP	945172
S2	KEYBOARD PB MOM SP	945172
S3	KEYBOARD PB MOM SP	945172
S4	KEYBOARD PB MOM SP	945172
S5	KEYBOARD PB MOM SP	945172

REF	DESCRIPTION	PART No.
S6	KEYBOARD PB MOM SP	945172
S7	KEYBOARD PB MOM SP	945172
S8	KEYBOARD PB MOM SP	945172
S9	KEYBOARD PB MOM SP	945172
S10	KEYBOARD PB MOM SP	945172
S11	KEYBOARD PB MOM SP	945172
S12	KEYBOARD PB MOM SP	945172
S13	KEYBOARD PB MOM SP	945172
S14	KEYBOARD PB MOM SP	945172
S15	KEYBOARD PB MOM SP	945172
S16	KEYBOARD PB MOM SP	945172
S17	KEYBOARD PB MOM SP	945172
S18	KEYBOARD PB MOM SP	945172
S19	KEYBOARD PB MOM SP	945172
S20	KEYBOARD PB MOM SP	945172
S21	KEYBOARD PB MOM SP	945172
S22	KEYBOARD PB MOM SP	945172
S23	KEYBOARD PB MOM SP	945172
S24	KEYBOARD PB MOM SP	945172
S25	KEYBOARD PB MOM SP	945172
S26	KEYBOARD PB MOM SP	945172
S27	KEYBOARD PB MOM SP	945172
S28	KEYBOARD PB MOM SP	945172
S29	KEYBOARD PB MOM SP	945172
S30	KEYBOARD PB MOM SP	945172
S31	KEYBOARD PB MOM SP	945172
S32	KEYBOARD PB MOM SP	945172
S33	KEYBOARD PB MOM SP	945172
S34	KEYBOARD PB MOM SP	945172
S35	KEYBOARD PB MOM SP	945172
S36	KEYBOARD PB MOM SP	945172
S37	KEYBOARD PB MOM SP	945172
S38	KEYBOARD PB MOM SP	945172
S39	KEYBOARD PB MOM SP	945172
S40	KEYBOARD PB MOM SP	945172
S41	KEYBOARD PB MOM SP	945172
S42	KEYBOARD PB MOM SP	945172
S43	KEYBOARD PB MOM SP	945172
S44	KEYBOARD PB MOM SP	945172

REF	DESCRIPTION		PART No.
TRANSFORMER			
T1			91270-01
TRANSISTOR			
TR1	N	ZTX650L	945212
TR2	N	ZTX650L	945212
TR3	GP (BJ) P	BCX71J 150M	999204/MC
TR4	CHIP(702)F	2N7002	999647/SD
TR5	GP (BJ) P	BCX71J 150M	999204/MC

BLANK FRONT PANEL MODULE ASSEMBLY RA3793/94
DRG. No. DA91288 ISSUE 02
PART No. 91288-02

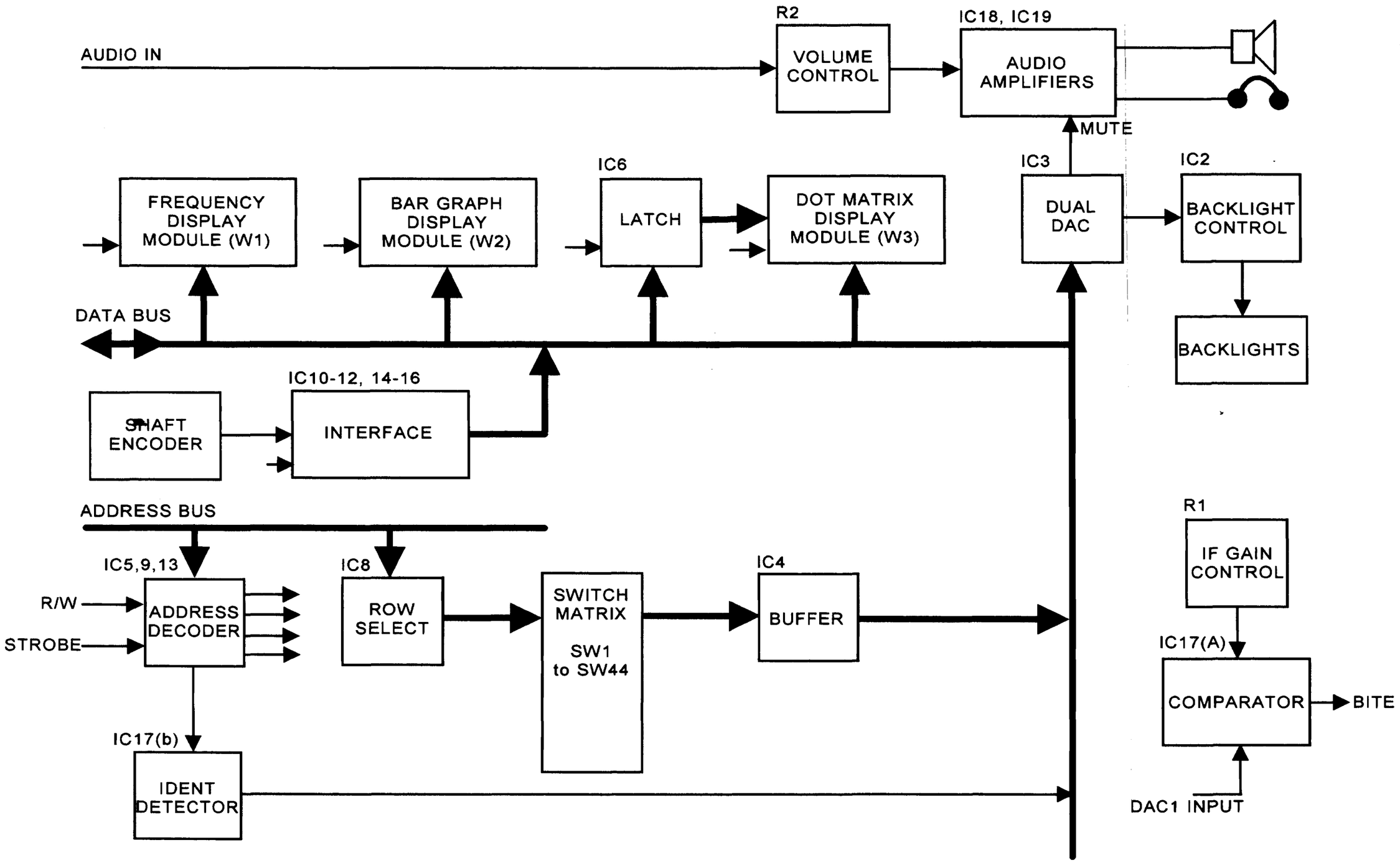
ITEM	PART No.	DESCRIPTION	QTY
1	91199/002-02	ASSY-PCB PANEL FRONT BLANK	1
5	91295-02	PANEL FRONT OVERLAY	1
6	91070-01	ASSY-CABLE 3-WAY	1
7	91264-03	ASSY-CABLEFORM	1
12	87107/002-01	HANDLE	2
17	925767	KNOB-.250 COL BK	1
18	926887	CAP KNOB 15MM BK PLAIN	1
20	923509	CONN 2-WAY S FX	1
30	A01663	SWITCH ROCKR DPST 16A U O-OFF	1

FRONT PANEL BOARD 91199/002-02 (RA3793/RA3794)

REF	DESCRIPTION								PART NUMBER
CAPACITORS									
C1	CAP	10	U	20%	35	V	TAN	BEAD	28571-213-18
C2	CAP	100	N	10%	50	V	CER	P-M-	940318
C3	CAP	10	U	20%	35	V	TAN	BEAD	28571-213-18
C4	CAP	18	P	2%	100	V	CER	PRDC	28751-446-12
C5	CAP	10	U	20%	35	V	TAN	BEAD	28571-213-18
C6	CAP	330	U	T%	25	V	ALU	TAC-	945006
C7	CAP	330	U	T%	25	V	ALU	TAC-	945006
C8	CAP	100	N	10%	50	V	CER	P-M-	940318
C9	CAP	100	N	10%	50	V	CER	P-M-	940318
C10	CAP	100	P	10%	100	V	CER	PRDC	28751-455-10
C11	CAP	100	P	10%	100	V	CER	PRDC	28751-455-10
C12	CAP	100	P	10%	100	V	CER	PRDC	28751-455-10
C13	CAP	100	P	10%	100	V	CER	PRDC	28751-455-10
C14	CAP	100	P	10%	100	V	CER	PRDC	28751-455-10
C15	CAP	100	P	10%	100	V	CER	PRDC	28751-455-10
C16	CAP	100	P	10%	100	V	CER	PRDC	28751-455-10
C17	CAP	100	P	10%	100	V	CER	PRDC	28751-455-10
C18	CAP	100	P	10%	100	V	CER	PRDC	28751-455-10
C19	CAP	100	P	10%	100	V	CER	PRDC	28751-455-10
C20	CAP	100	P	10%	100	V	CER	PRDC	28751-455-10

REF	DESCRIPTION	PART NUMBER
C21	CAP 100 P 10% 100 V CER PRDC	28751-455-10
C22	CAP 100 P 10% 100 V CER PRDC	28751-455-10
C23	CAP 100 P 10% 100 V CER PRDC	28751-455-10
	DIODES	
D1	DIODE LED RD HLMP-2300	937652
D2	DIODE LED GN HLMP-2500	A00127
D3	DIODE LED RD HLMP-2300	937652
	INTEGRATED CIRCUITS	
IC1	IC 380N AUD AMP	929343
	INDUCTORS	
L1	IND 1 UH 10%	938966
	PINS	
P1	TERM PIN SE PSH SLD 1.02 BR TS	937625/EQ
P2	TERM PIN SE PSH SLD 1.02 BR TS	937625/EQ
P3	TERM PIN SE PSH SLD 1.02 BR TS	937625/EQ
P4	TERM PIN SE PSH SLD 1.02 BR TS	937625/EQ
P5	TERM PIN SE PSH SLD 1.02 BR TS	937625/EQ
P6	TERM PIN SE PSH SLD 1.02 BR TS	937625/EQ
	PLUGS	
PL1	CONN 3-WAY P FX STRT	945607
	RESISTORS	
R1	RES 2.2 K 2% 0.25 W METOXDE	916546/EQ
R2	RES 1.2 K 2% 0.25 W METOXDE	911179/EQ
R3	RES 2.2 K 2% 0.25 W METOXDE	916546/EQ
R4	RES 2.2 K 2% 0.25 W METOXDE	916546/EQ
R5	RES 1.2 K 2% 0.25 W METOXDE	911179/EQ
R6	RES 2.2 K 2% 0.25 W METOXDE	916546/EQ
R7	RES 2.2 K 2% 0.25 W METOXDE	916546/EQ
R8	RES 560 2% 0.25 W METOXDE	917061/EQ
R9	RES 10 2% 0.25 W METOXDE	920736/EQ
R10	RES 2.2 K 2% 0.25 W METOXDE	916546/EQ

REF	DESCRIPTION		PART NUMBER
SOCKETS			
SK1	CONN RECT 15-WAY S FX PSH		A01075
SK2	CONN RECT 15-WAY S FX PSH		A01075
CABLE ASSEMBLIES			
W1	ASSY-CABLE 26-WAY	*	91297/001-01
W2	ASSY-CABLE 26-WAY	*	91297/002-01



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Block Diagram: RA3791/RA3792/MA3790
Front Panel Assembly

Fig. 9-3

Circuit: RA3791/92/MA3790 Front Panel Board (Sheet 1)

Fig. 9.4

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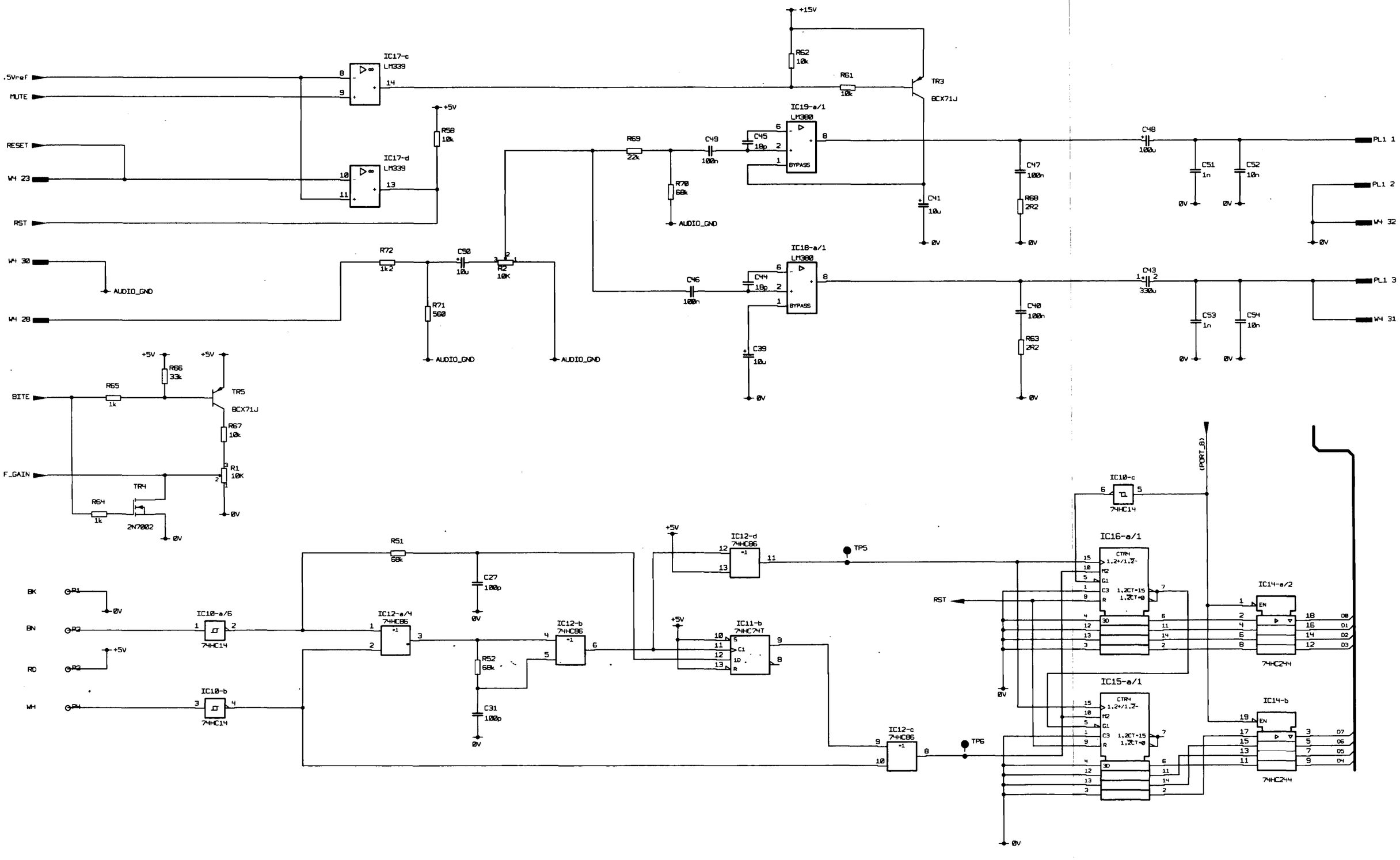

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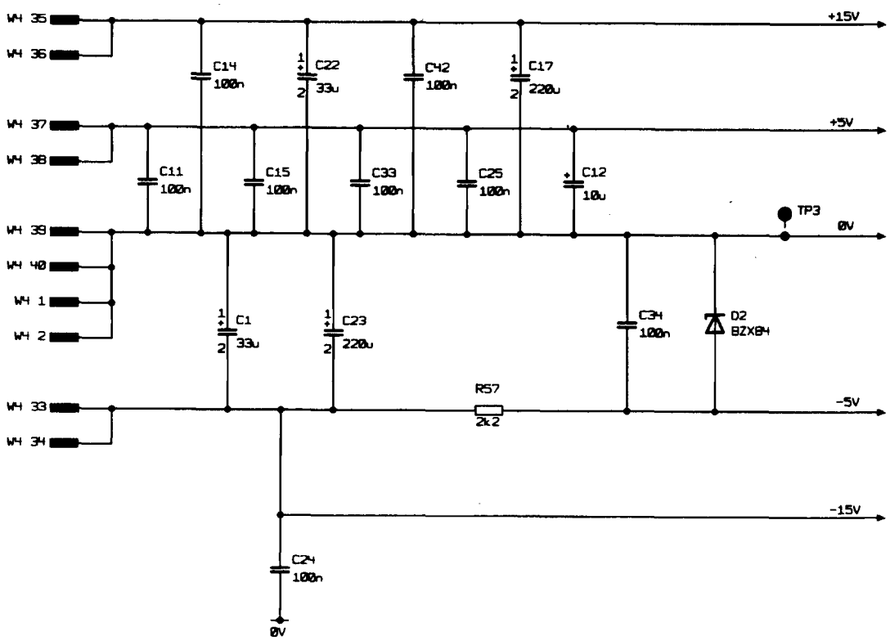
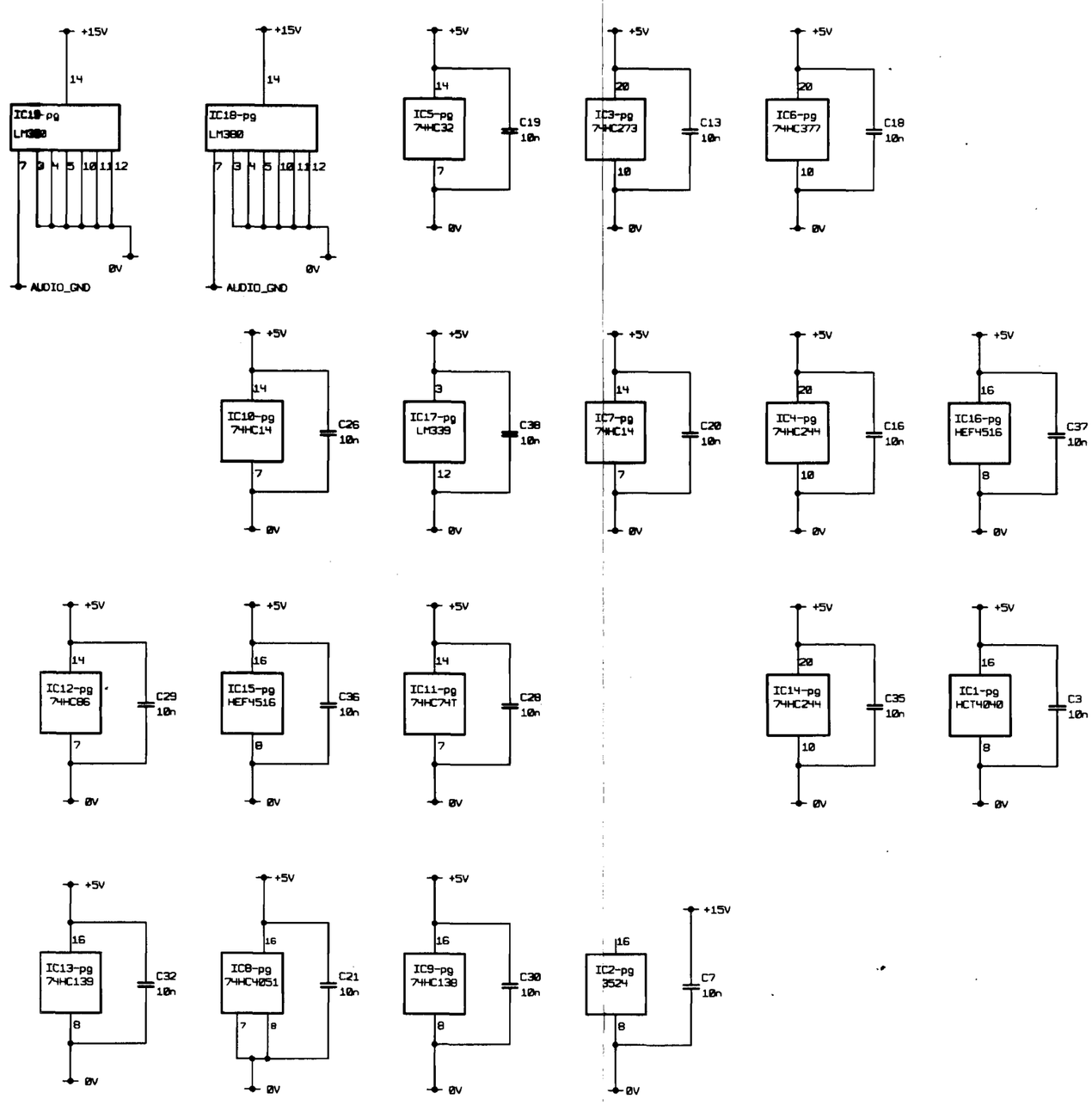
Circuit: RA3791/92/MA3790 Front Panel Board (Sheet 2) Fig. 9.5





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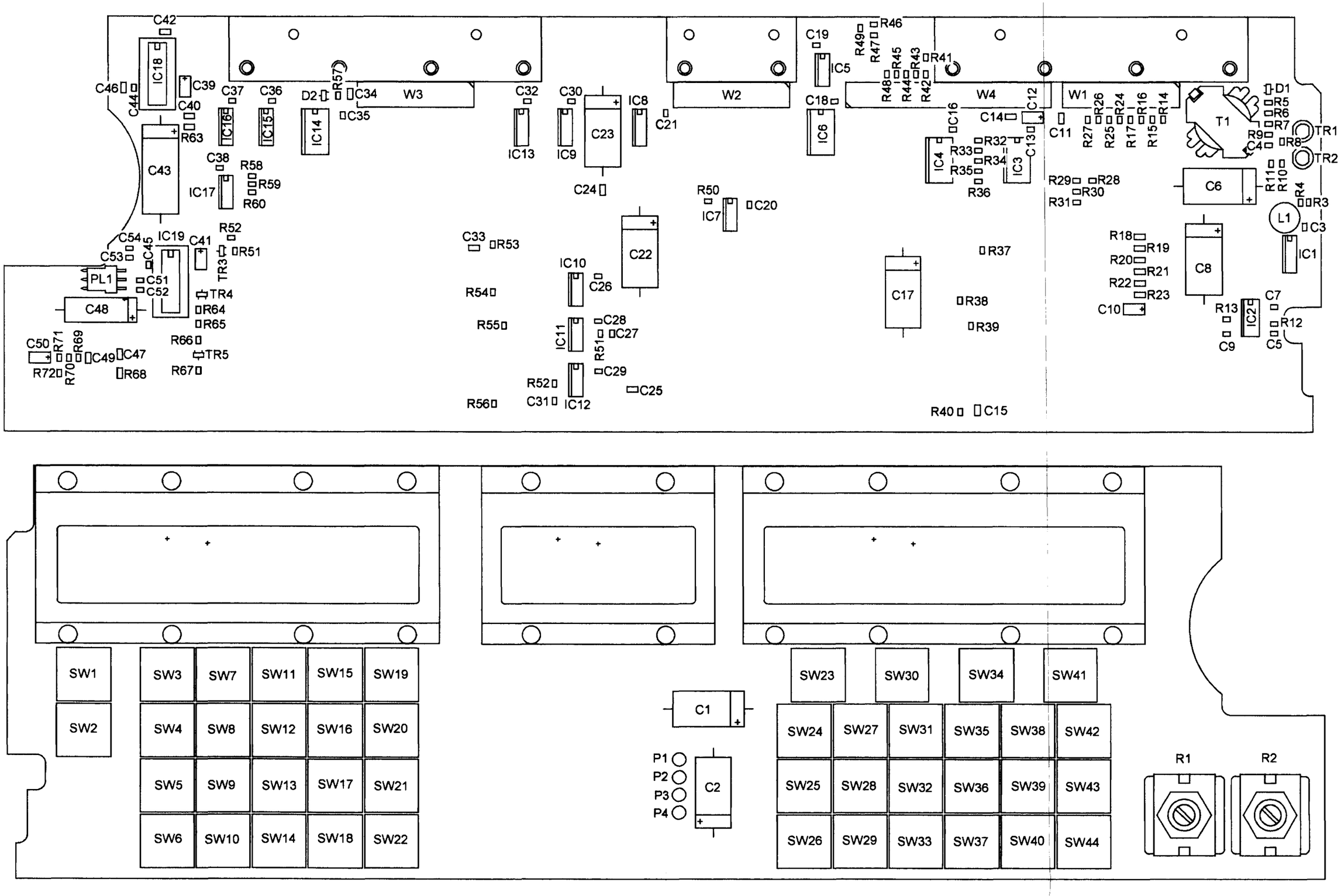
Circuit: RA3791/92/MA3790 Front Panel Board (Sheet 3)

Fig. 9.6



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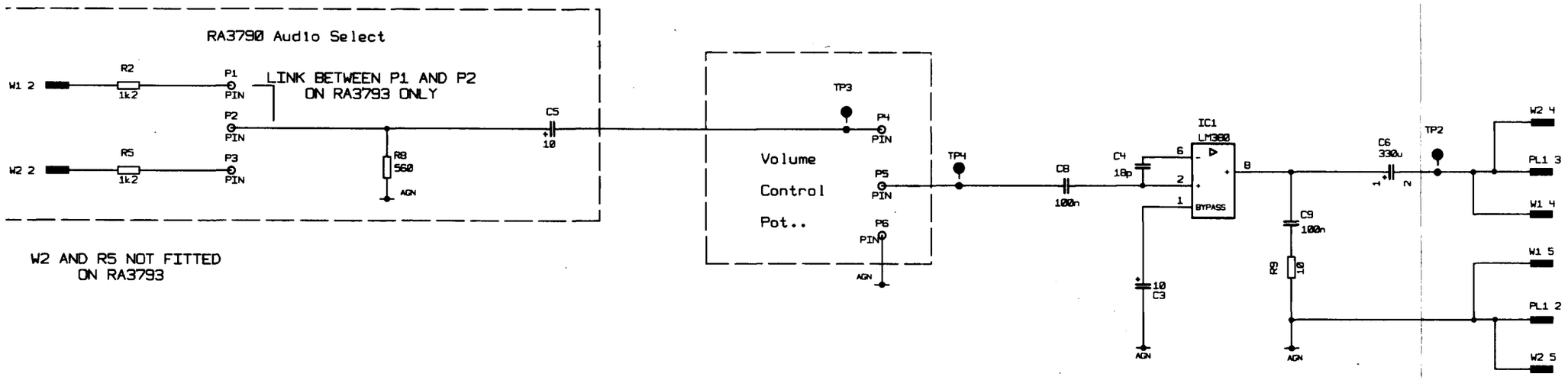
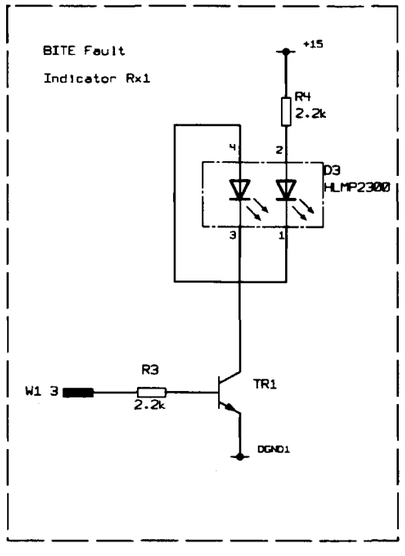
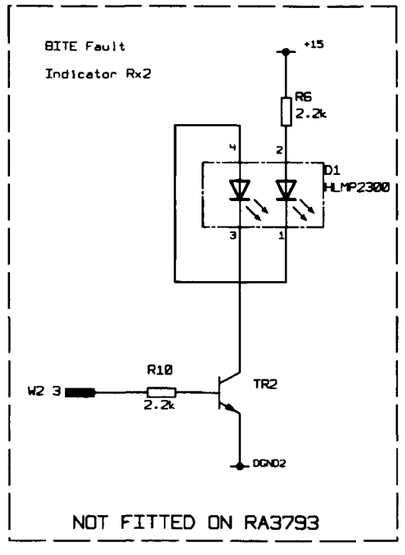
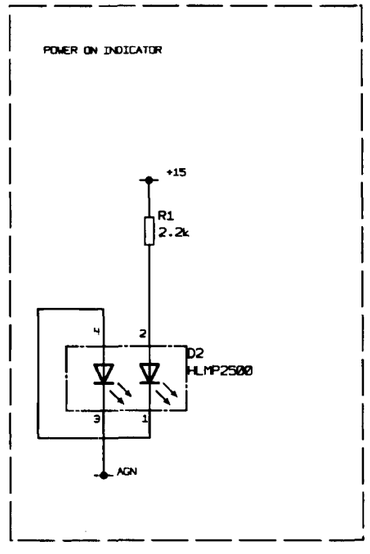
Layout: RA3791/92/MA3790 Front Panel Board

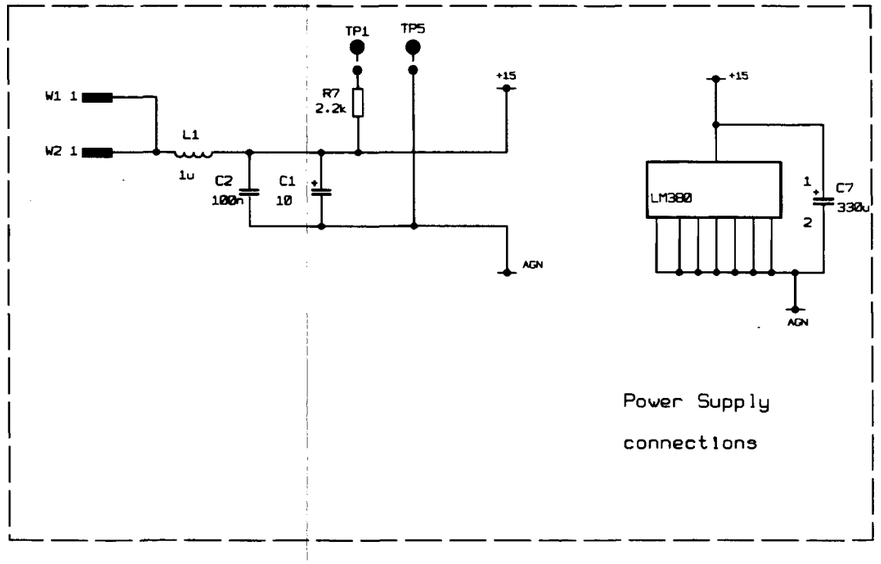
Fig. 9.7











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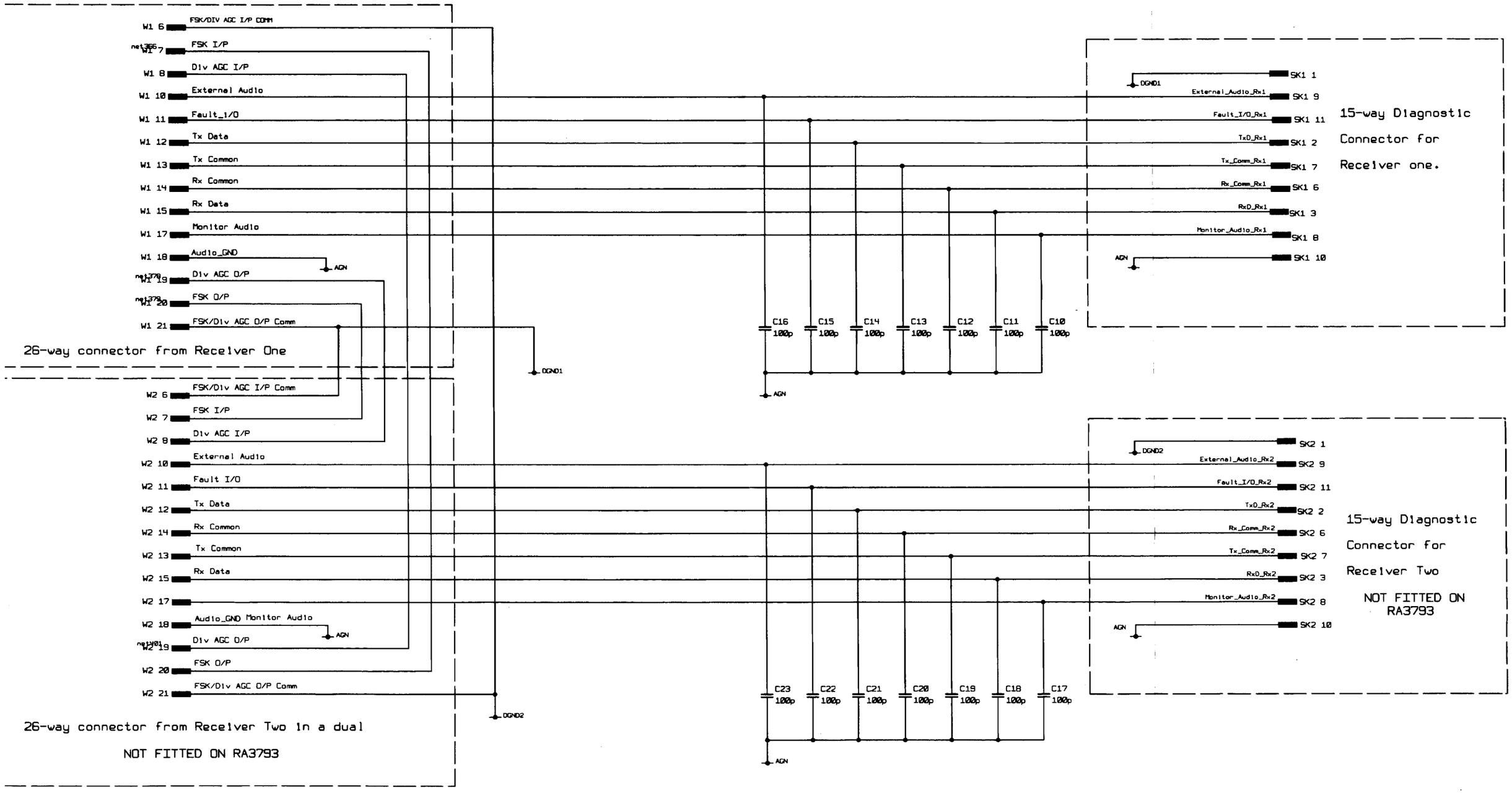
Circuit: RA3793/94 Front Panel Board (Sheet 1) Fig. 9.8



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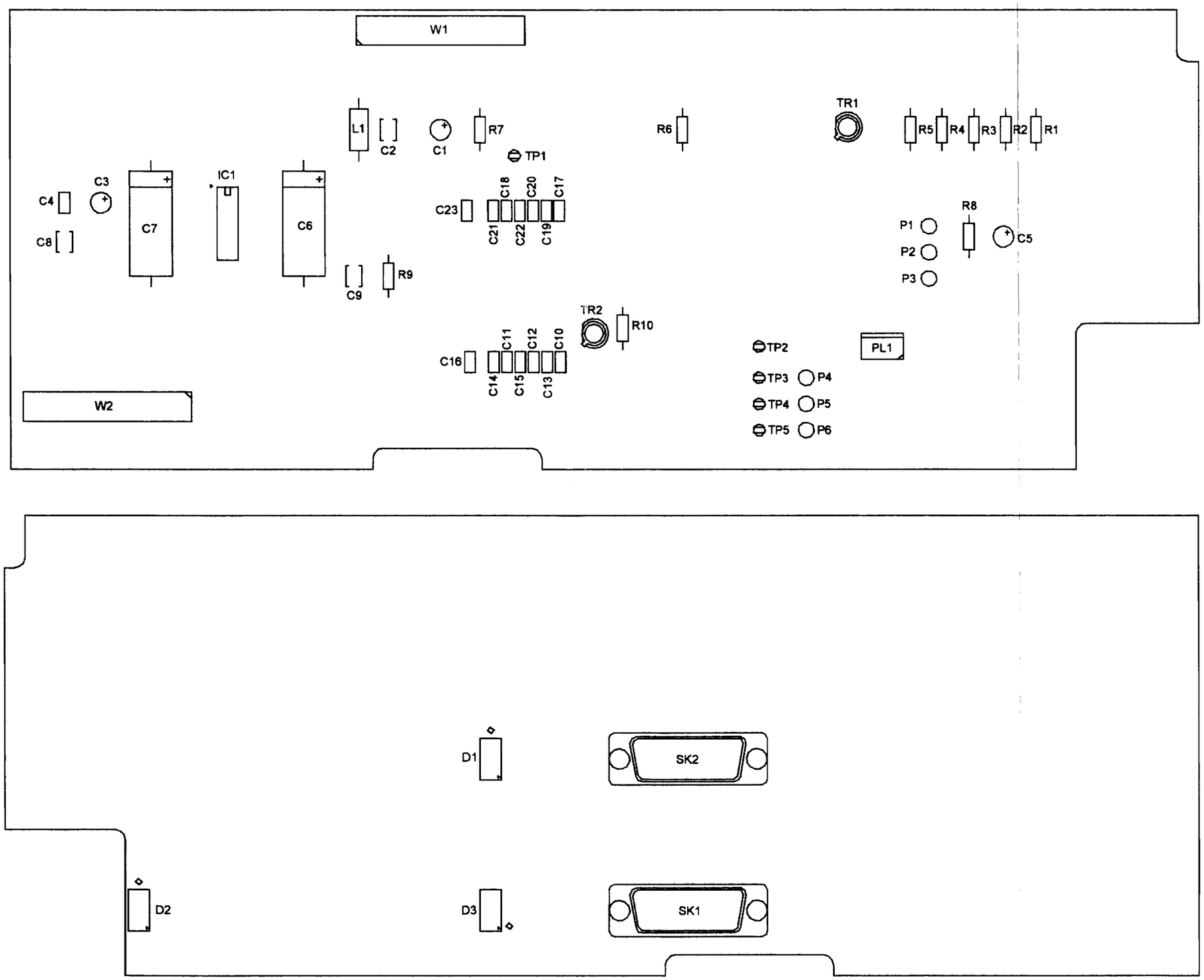
Circuit: RA3793/94 Front Panel Board (Sheet 2) Fig. 9.9



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Layout: RA3793/94 front Panel Board

Fig. 9.10

CHAPTER 10

POWER SUPPLY

CONTENTS

Illustrations

CHAPTER 10

POWER SUPPLY

INTRODUCTION

1. The power supply unit fitted to the RA3790 series of receivers is a non-repairable item and should be replaced if found faulty. It operates from a 47 to 63 Hz AC supply voltage in the range 90 V to 132 V and 175 V to 264 V, with automatic voltage selection.

CONNECTIONS

2. The unit is fitted with two connectors, a 3-way mains input plug and a 14-way DC output plug (Fig. 10.1). The pin connections are listed below:

Mains Input:	1	Earth			
	2	Neutral			
	3	Live			
Outputs:	1	-15V) ± 0.7 V	8	0 V	
	2	-15V)	9	0 V	
	3	N/C	10	0 V	
	4	N/C	11	+5 V)	
	5	+15V) ± 0.7 V	12	+5 V) ± 0.2 V	
	6	+15V)	13	+5 V)	
	7	0 V	14	+5 V)	

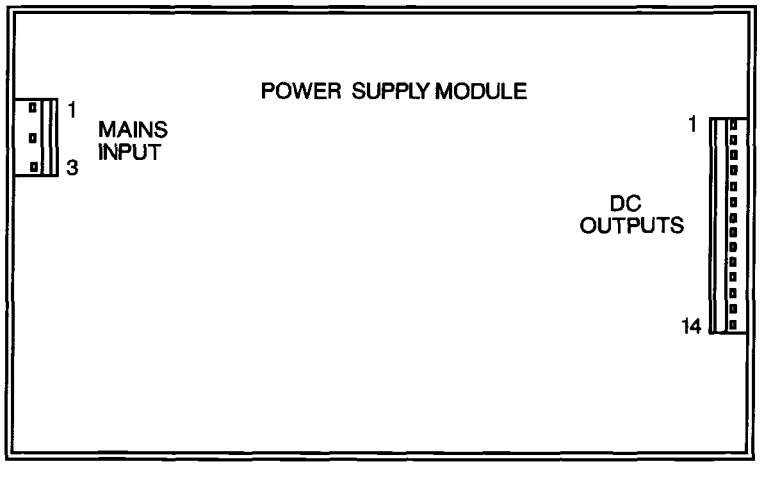


Fig. 10.1 Layout: Power Supply Module

CHAPTER 11

CHASSIS ASSEMBLY AND INTERCONNECTIONS

CONTENTS

Illustrations

Fig.

CHAPTER 11

CHASSIS ASSEMBLY AND INTERCONNECTIONS

INTRODUCTION

1. This chapter describes the chassis assembly and provides interconnection information for the units which comprise the RA3790 series of receivers. This interconnection information is presented in diagrammatic form to show the physical connections between assemblies, and does not include pin connection details. To obtain detailed pin connection information, refer to the appropriate assembly chapter.

ASSEMBLY DESCRIPTION

2. For the RA3791 and RA3793 Single Receivers (Figs. 11.1, 11.2 and 11.5), and also for the MA3790 Controller, the assembly comprises a folded metal chassis with a non-removable rear panel, a removable front panel assembly and an overall top cover plate.

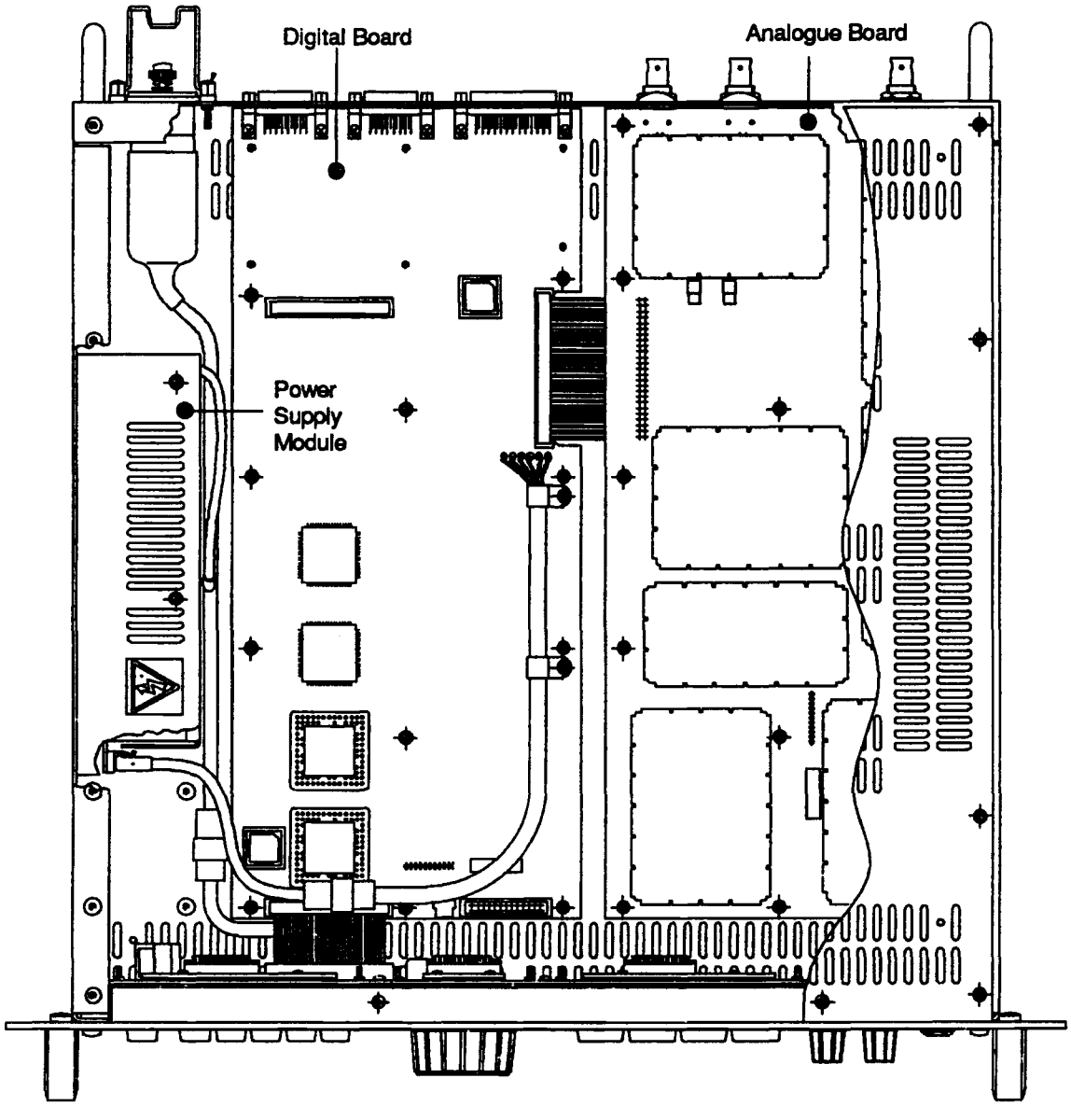
3. For the RA3792 and RA3794 Dual Receivers (Figs. 11.3, 11.4, 11.6 and 11.7), the folded metal chassis has two full-width compartments, one above the other. The removal of the overall top cover plate provides access to the Receiver 1 boards. To access the Receiver 2 boards, the unit is turned over and the overall bottom cover plate is removed.

4. Connectors on the Digital and Analogue boards (Digital board only in the case of the MA3790) protrude through apertures provided in the rear panel. Also mounted on the rear panel is the fused and filtered mains input connector and the earth terminal. The front panel assembly, which houses the front panel board, is secured to the chassis with four screws, two at each side.

5. The power supply module, in all cases, is mounted at the left side of the chassis. The associated mains cableform runs from the rear panel fused connector to the front panel POWER switch, and then to the power supply input connector. In all cases, the DC outputs are taken to the Digital Board, (to both Digital Boards in dual receivers) and are then distributed to other boards via the interconnecting ribbon cable assemblies.

INTERCONNECTIONS

6. Individual interconnection diagrams, Figs. 11.8 to 11.12, are provided for the RA3791, RA3792, RA3793, RA3794 and MA3790 respectively at the end of the chapter.



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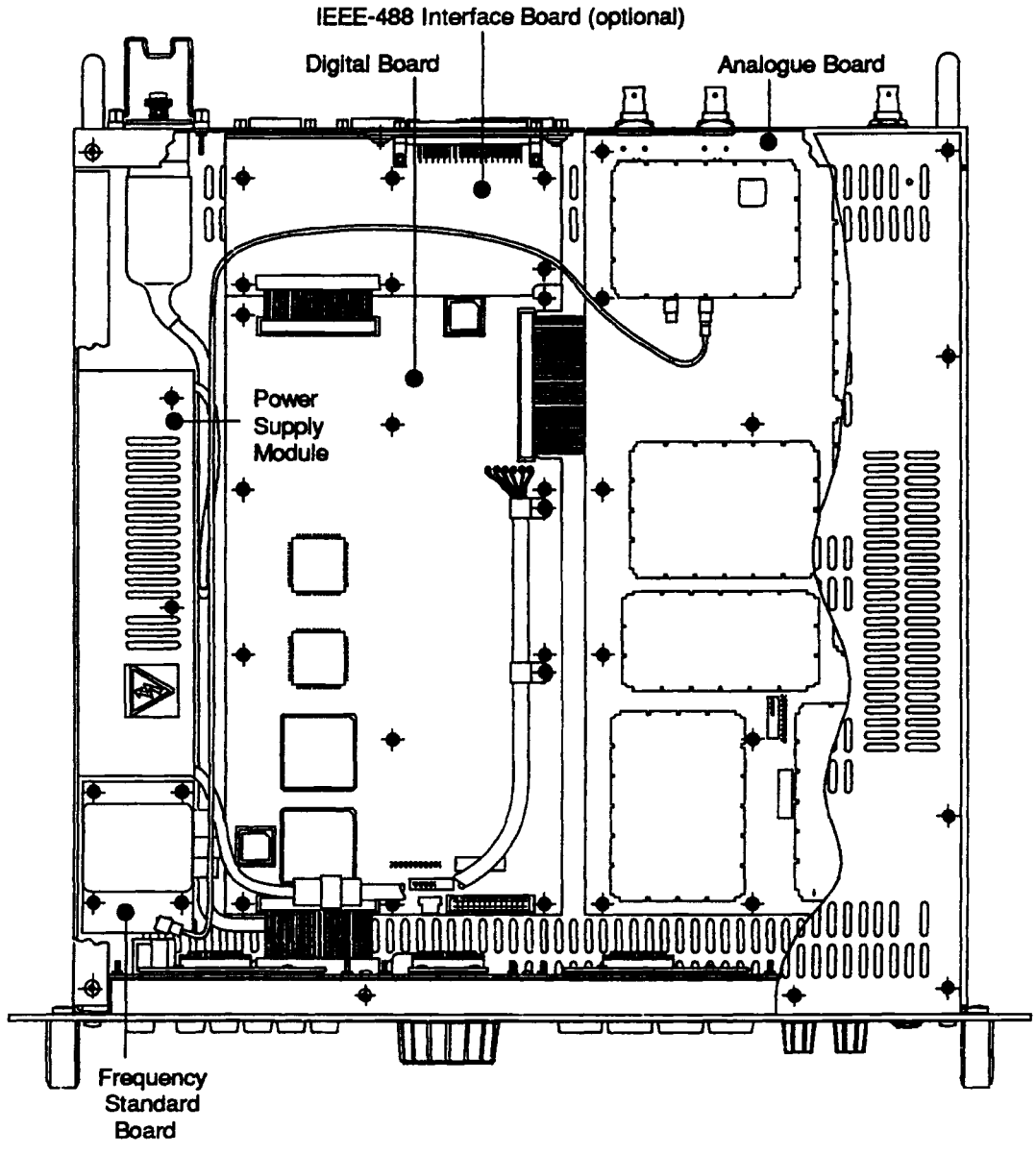
RA3791 Plan View - No Frequency Standard Board Fig. 11.1



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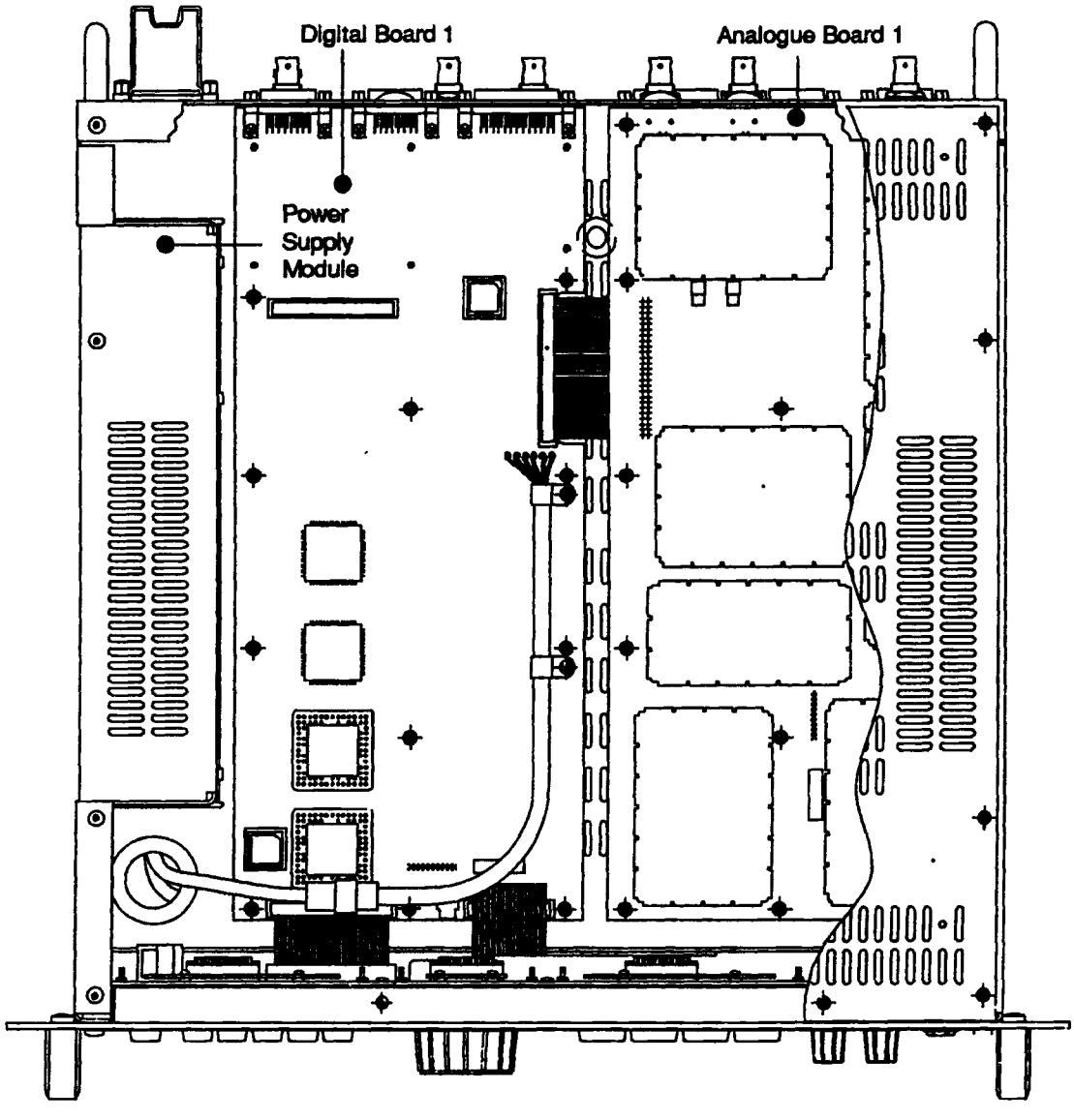
RACAL RA3791 Plan View - Frequency Standard Board Fitted Fig. 11.2



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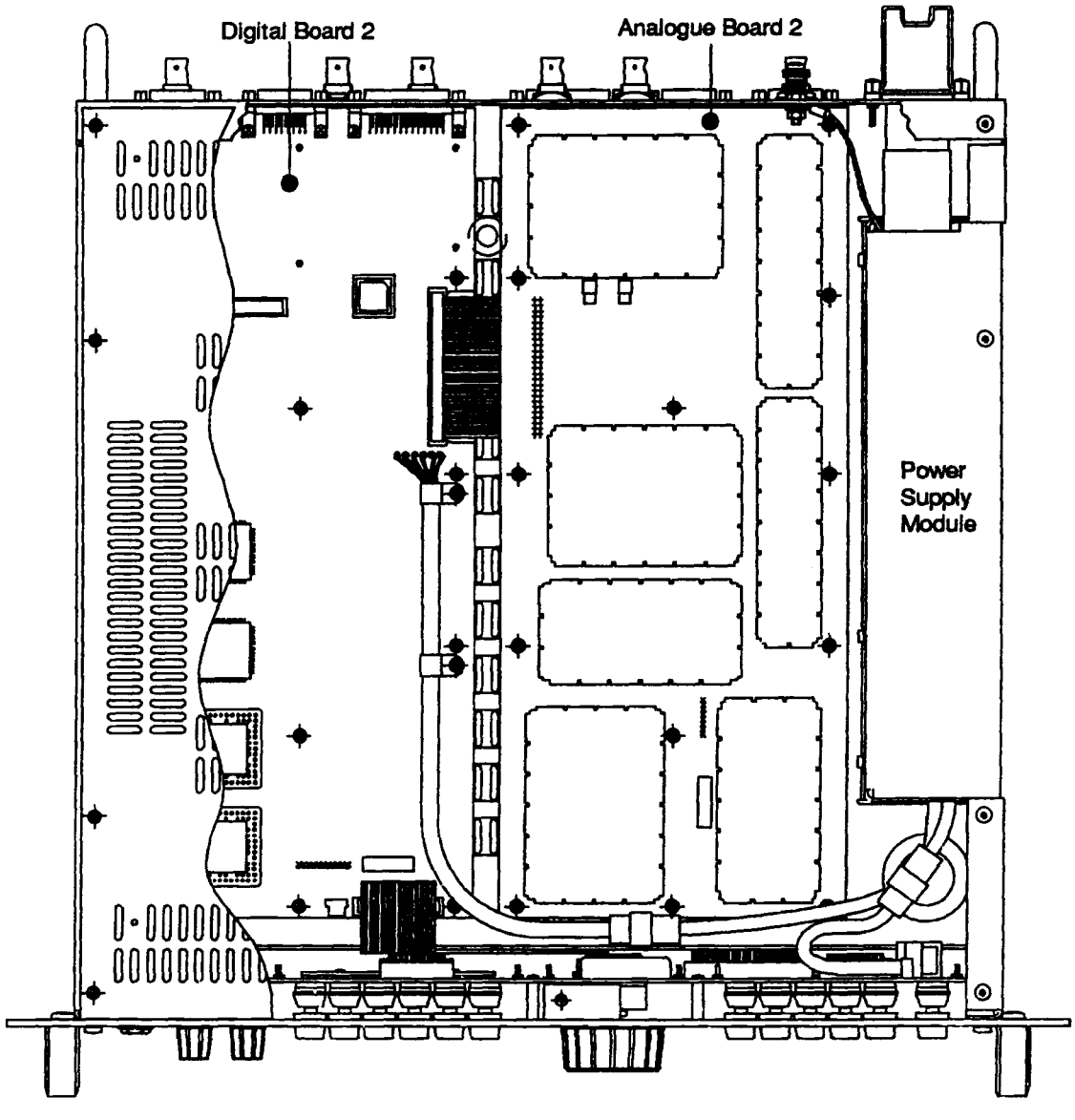
RA3792 Plan View

Fig. 11.3



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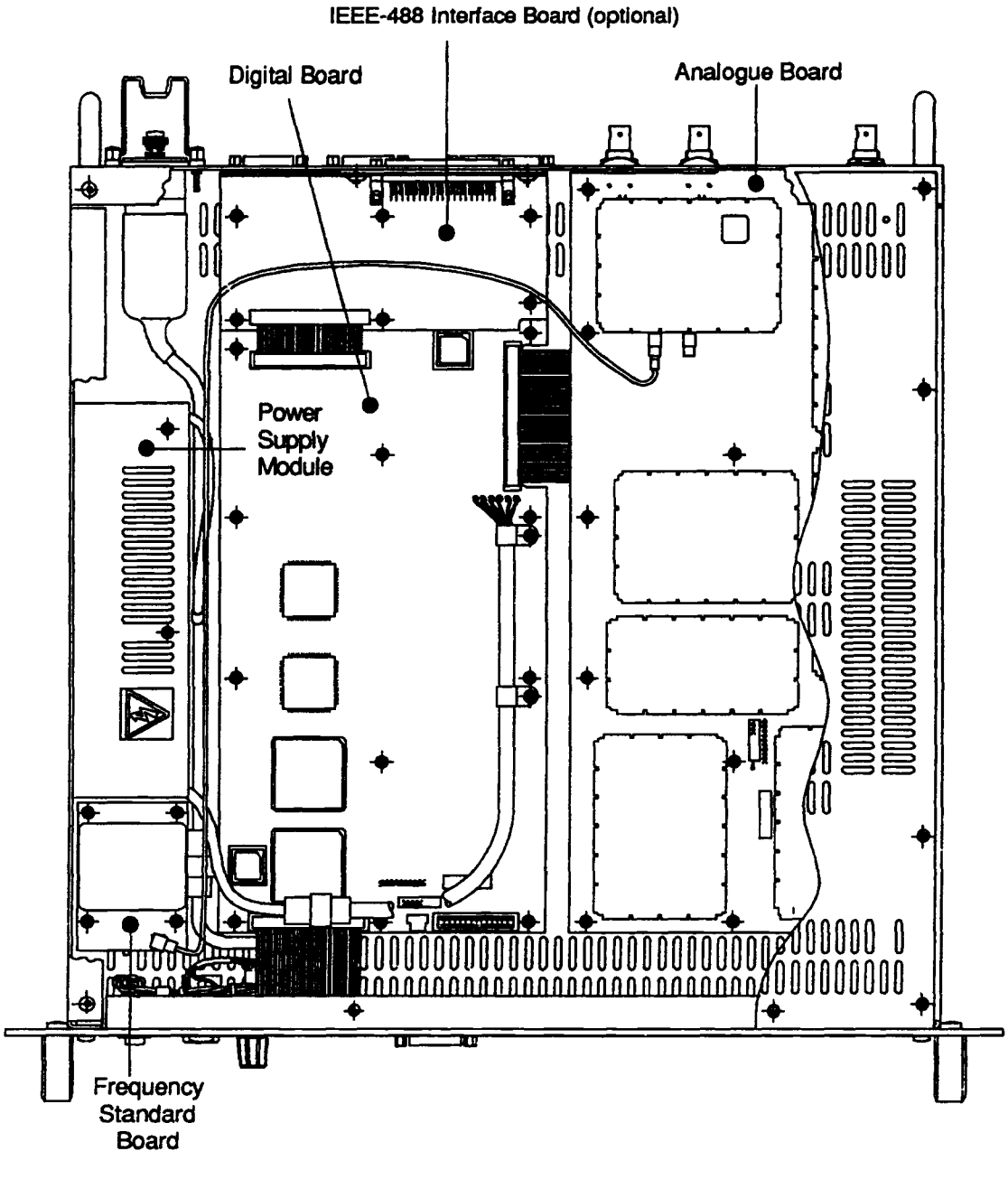
RA3792 Underside View

Fig. 11.4



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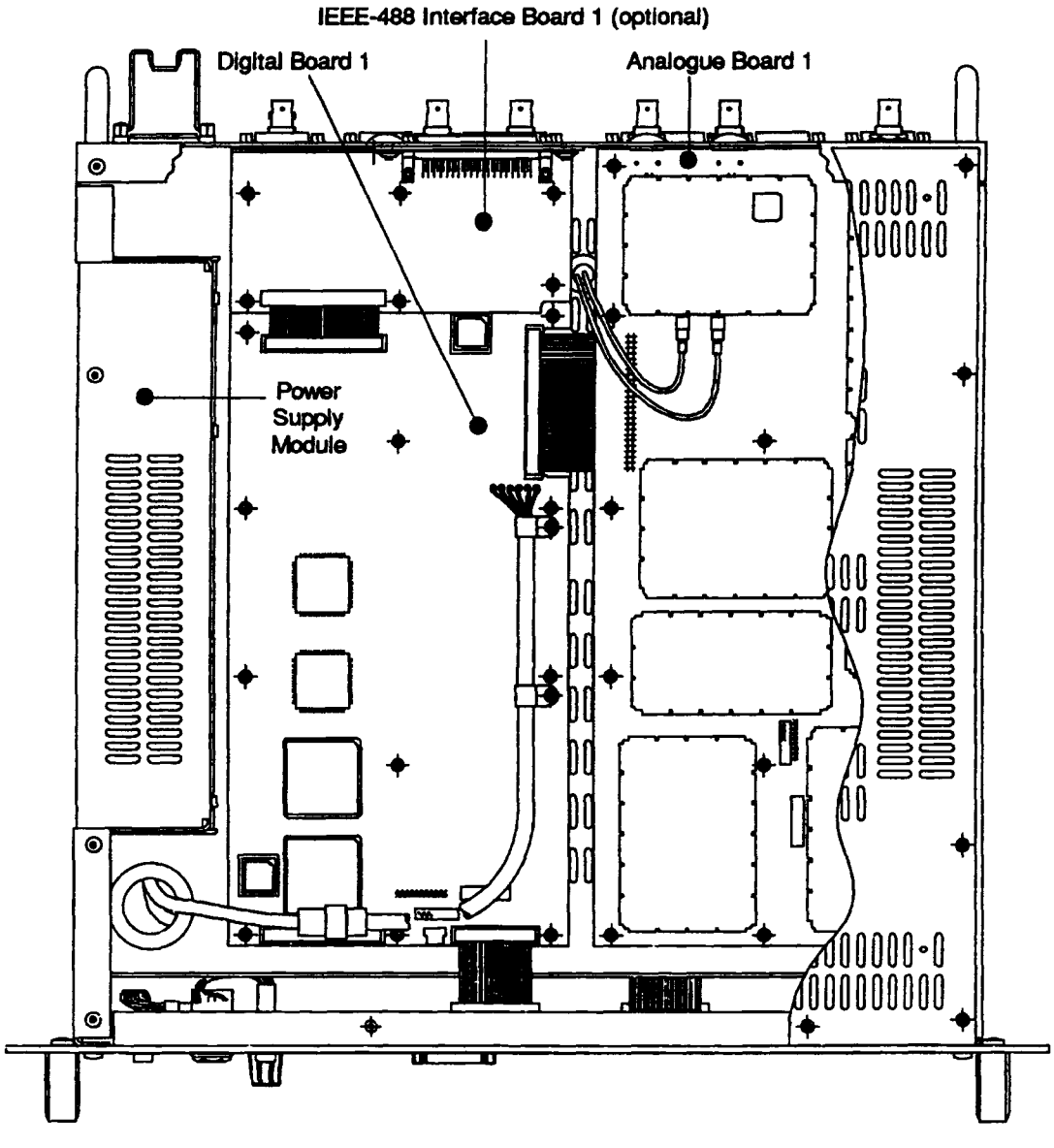
RA3793 Plan View

Fig. 11.5



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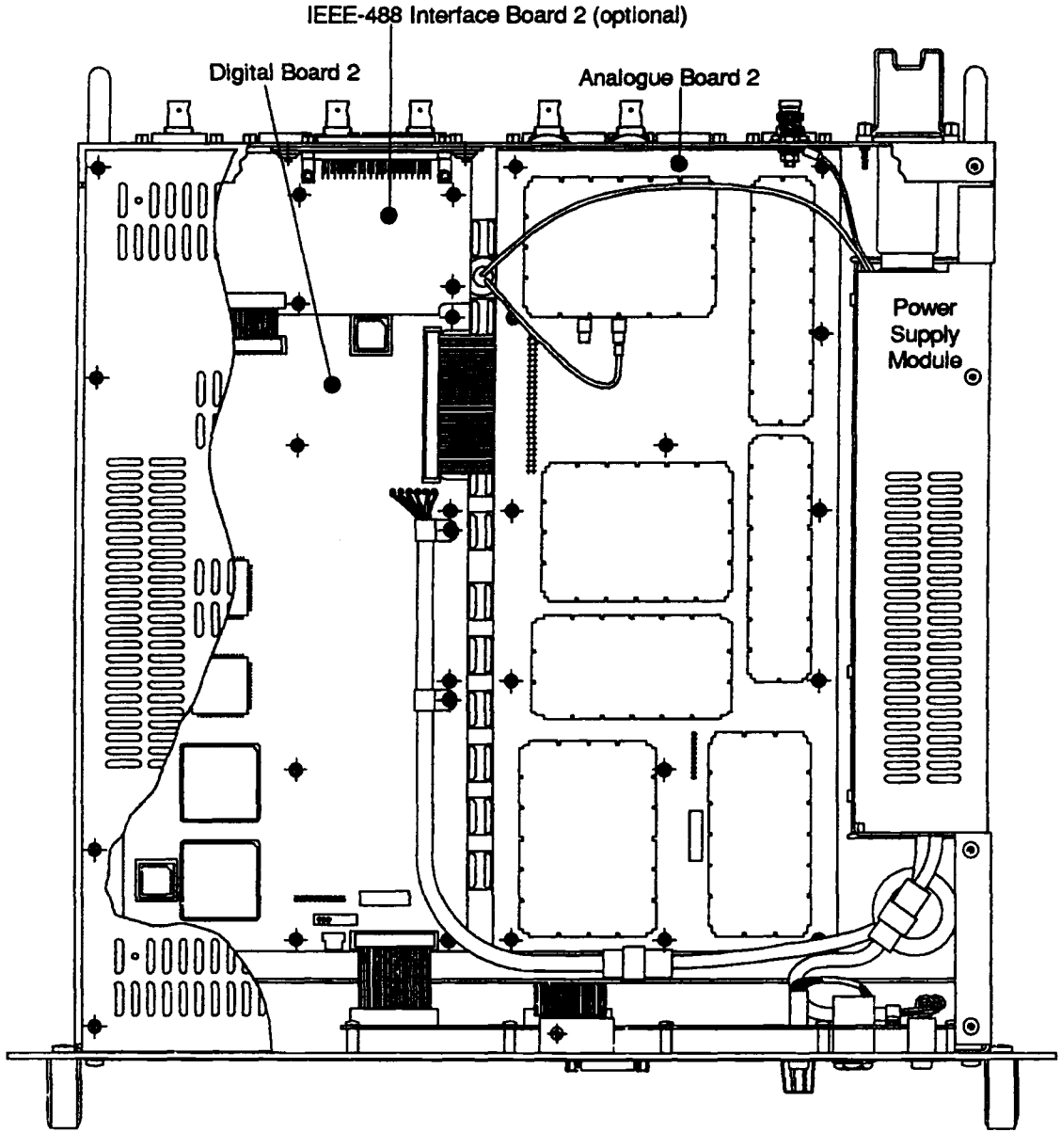
RA3794 Plan View

Fig. 11.6



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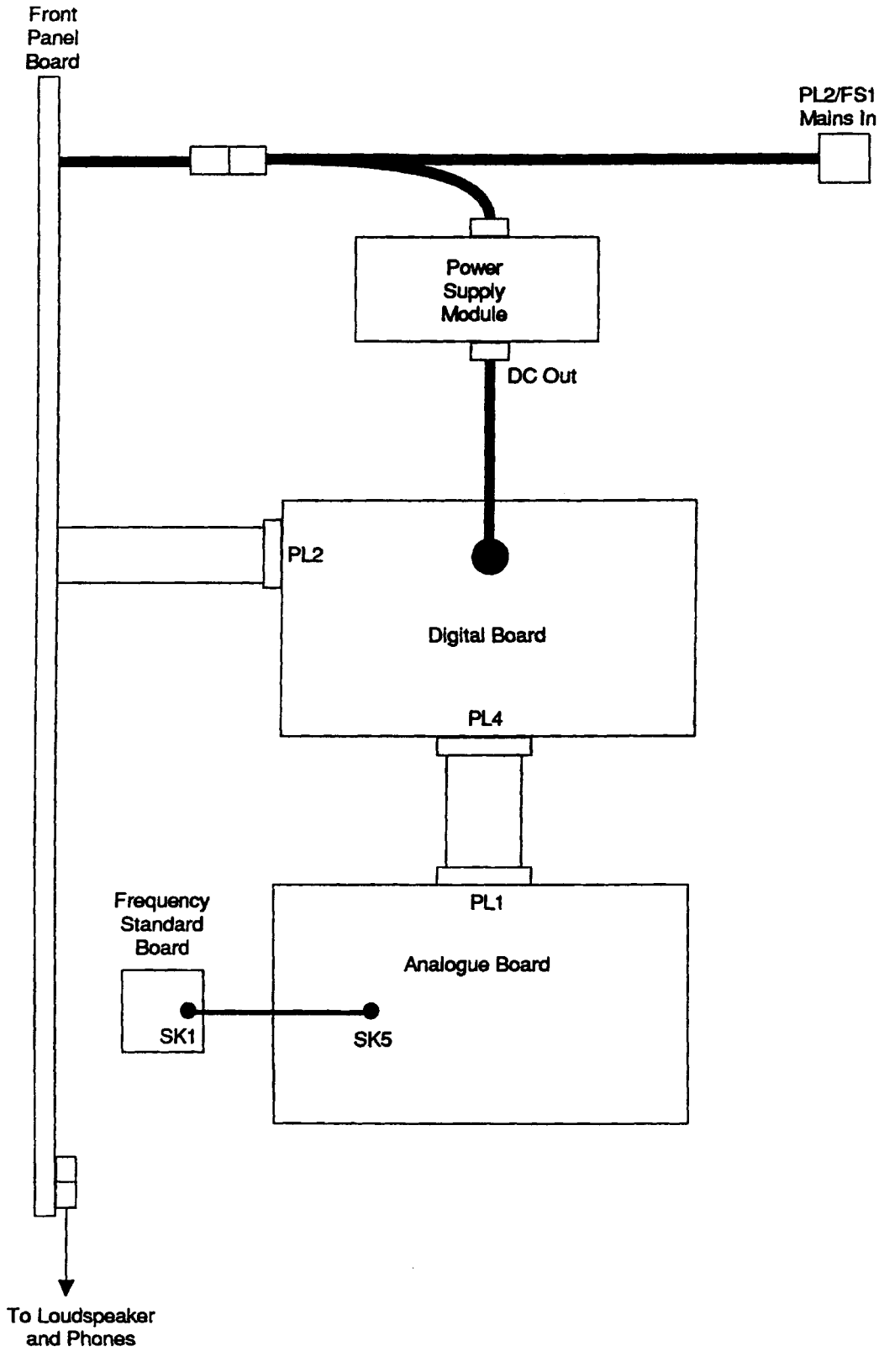
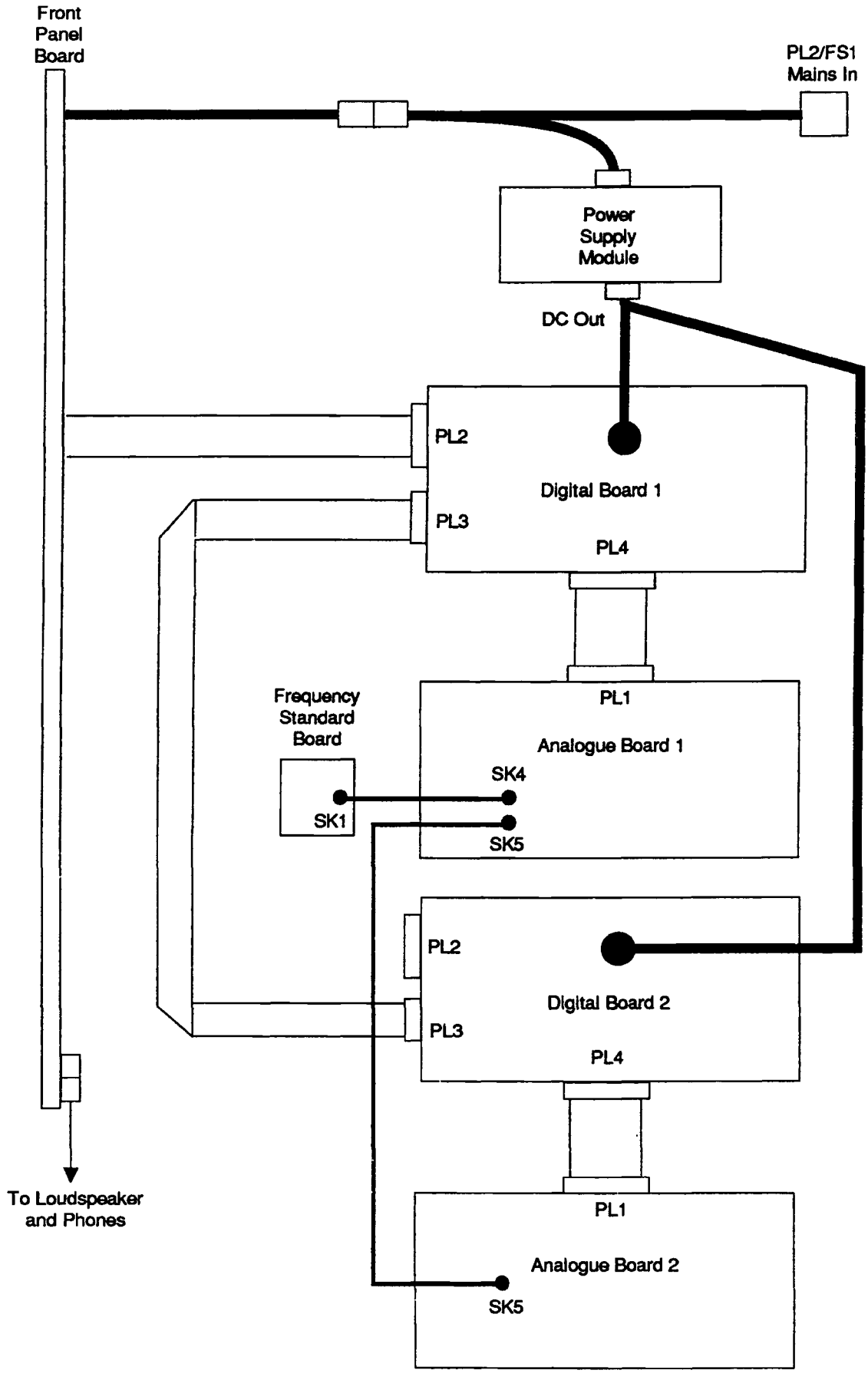
RA3794 Underside View

Fig. 11.7



Interconnection Diagram: RA3791

Fig. 11.8



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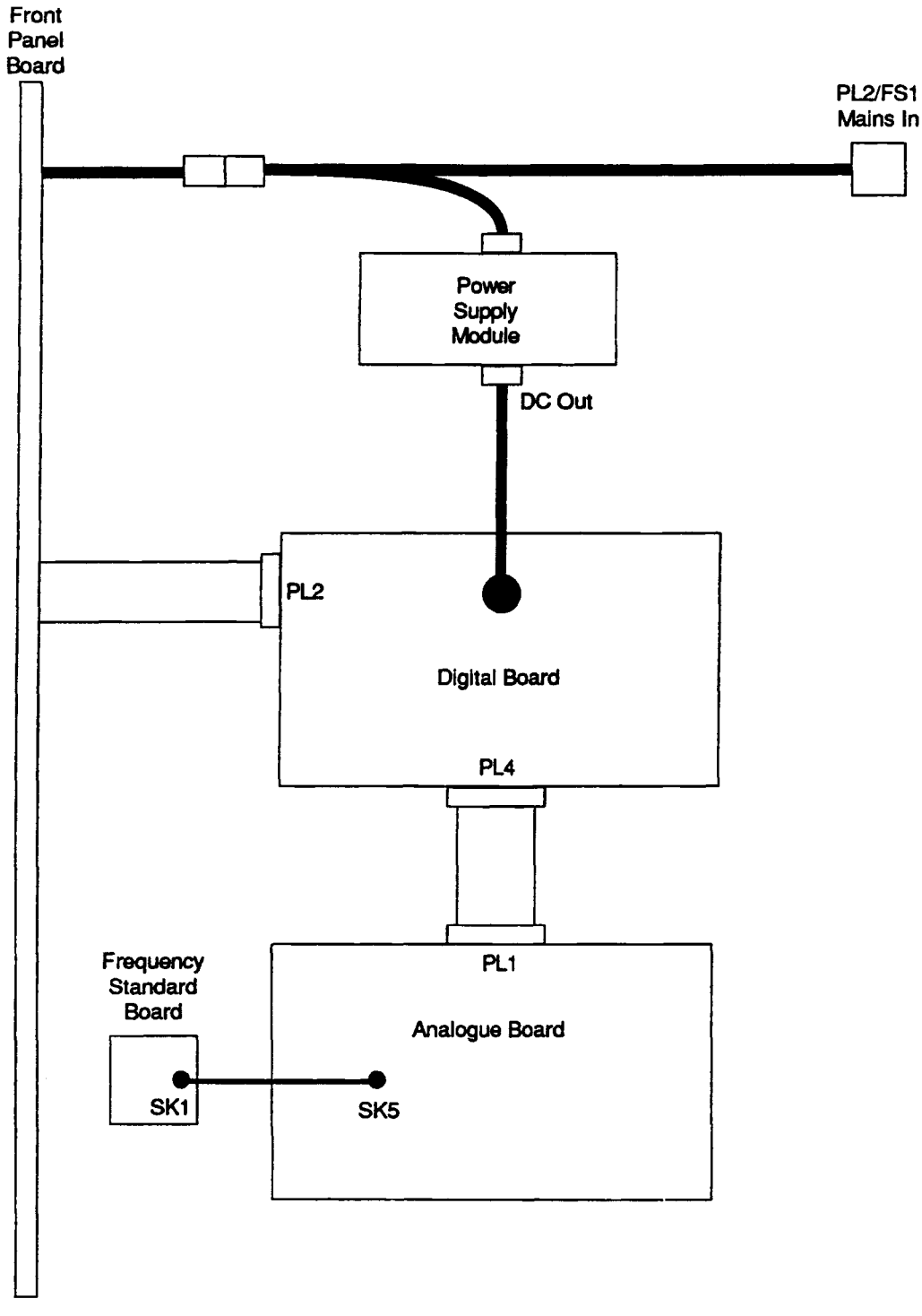
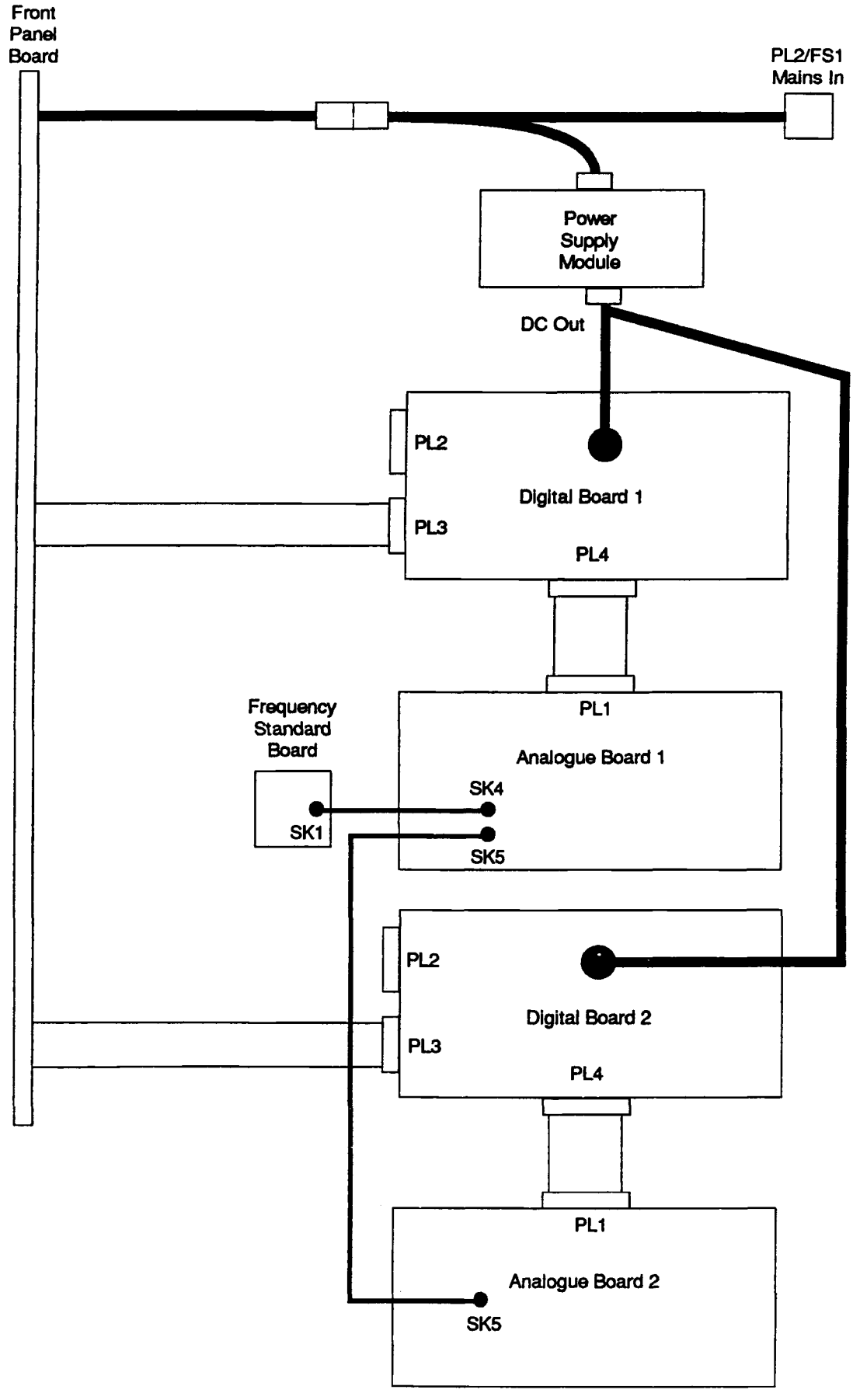
Interconnection Diagram: RA3792

Fig. 11.9



Interconnection Diagram: RA3793

Fig. 11.10



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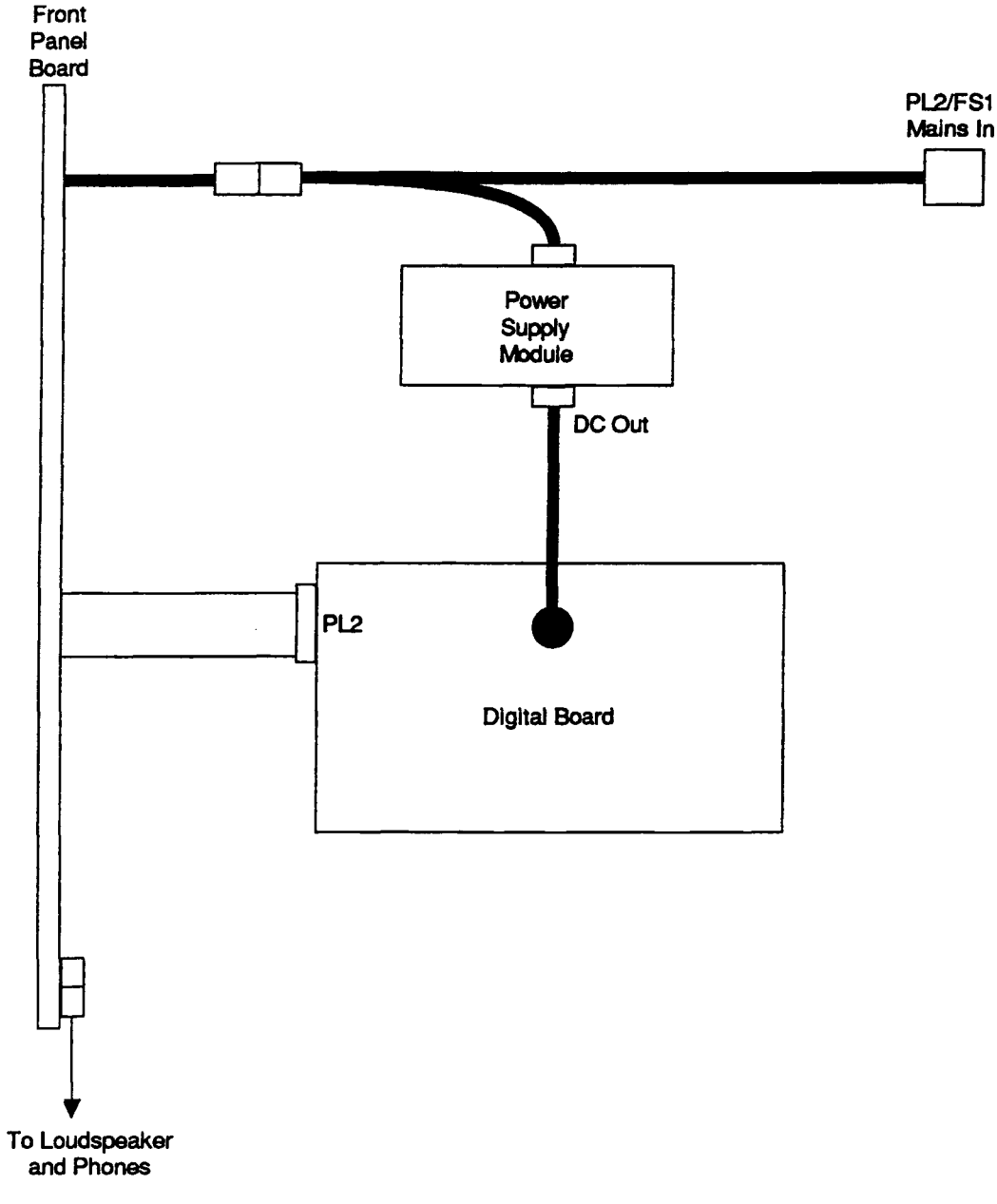
Interconnection Diagram: RA3794

Fig. 11.11



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Interconnection Diagram: MA3790

Fig. 11.12

CHAPTER 12

PARTS LIST

CONTENTS

CHAPTER 12

PARTS LIST

REPLACEMENT BOARDS

1. If an identical replacement Analogue or Digital Board is required, i.e. a board with the same software/hardware options as fitted to the board to be replaced, please quote the appropriate assembly number, as given in this chapter, and also the full information given on the label attached to the board.

COMPONENTS LISTS

2. For main assembly components list information, refer to the appropriate chapter of this manual.

RECEIVER ASSEMBLY RA3791

Drawing No: DA91210 - Issue 1D

Part No: 91210/999-01

ITEM	PART No.	DESCRIPTION	QTY
2	91224-01	ASSY-FRONT PANEL MODULE	1
3	91217-02	ASSY-PCB DIGITAL (OPTIONABLE)	1
4	91221-02	ASSY-PCB ANALOGUE (BASIC)	1
16	91281/001-02	ASSY-CABLE 50-WAY	1
18	91283-03	ASSY-CABLE MAINS	1
20	91284-03	ASSY-CABLE 6-WAY	1
44	91287-01	POWER SUPPLY MODULE	1
60	922457/EQ	FUSE 2 AMP 5 D X 20 AS	2

RA3792 RECEIVER ASSEMBLY

Drawing No. DA91211 Issue 1D

Part No. 91211/999-01

ITEM	PART No.	DESCRIPTION	QTY
2	91260-01	ASSY-PANEL FRONT MODULE (RA3792)	1
3	91217-02	ASSY-PCB DIGITAL (OPTIONABLE)	2
4	91221-02	ASSY-PCB ANALOGUE (BASIC)	2
16	91281/001-02	ASSY-CABLE 50-WAY	2
17	91811/001-01	ASSY-CABLE 26-WAY	1
18	91283-03	ASSY-CABLE MAINS	1
19	91285-03	ASSY-CABLE 12-WAY	1
44	91287-01	POWER SUPPLY MODULE	1
60	922457/EQ	FUSE 2 AMP 5 D X 20 AS	2

RA3793 RECEIVER ASSEMBLY

Drawing No. Issue 1A

Part No. 91212/999-01

ITEM	PART No.	DESCRIPTION	QTY
2	91230-02	ASSY-BLANK FRONT PANEL MODULE	1
3	91217-02	ASSY-PCB DIGITAL (OPTIONABLE)	1
4	91221-02	ASSY-PCB ANALOGUE (BASIC)	1
16	91281/001-02	ASSY-CABLE 50-WAY	1
18	91283-03	ASSY-CABLE MAINS	1
20	91284-03	ASSY-CABLE 6-WAY	1
44	91287-01	POWER SUPPLY MODULE	1
60	922457/EQ	FUSE 2 AMP 5 D X 20 AS	2

RA3794 RECEIVER ASSEMBLY

Drawing No. DA91213 Issue 01

Part No. 91213/999-01

ITEM	PART No.	DESCRIPTION	QTY
2	91288-02	ASSY-PANEL FRONT BLANK MODULE	1
3	91217-02	ASSY-PCB DIGITAL (OPTIONABLE)	2
4	91221-02	ASSY-PCB ANALOGUE (BASIC)	2
16	91281/001-02	ASSY-CABLE 50-WAY	2
18	91283-03	ASSY-CABLE MAINS	1
19	91285-03	ASSY-CABLE 12-WAY	1
44	91287-01	POWER SUPPLY MODULE	1
60	922457/EQ	FUSE 2 AMP 5 D X 20 AS	2

MA3790 RECEIVER CONTROLLER ASSEMBLY

Drawing No. DA91214 Issue 1B

Part No. 91214/001-01

ITEM	PART No.	DESCRIPTION	QTY
2	91310-01	ASSY-PANEL FRONT MODULE	1
3	91217-02	ASSY-PCB DIGITAL (OPTIONABLE)	1
18	91283-03	ASSY-CABLE MAINS	1
20	91284-03	ASSY-CABLE 6-WAY	1
44	91287-01	POWER SUPPLY MODULE	1
60	922457/EQ	FUSE 2 AMP 5 D X 20 AS	2
65	931421	CABLE ASSY (3 1/2M LENGTH)	1

FRONT PANEL MODULE ASSEMBLY - RA3791/92

Drawing No.DA91224 Issue 1B

Part No. 91224-01

ITEM	PART No.	DESCRIPTION	QTY
1	91223-03	ASSY-PCB FRONT PANEL	1
4	91314-01	ASSY-CABLE 3-WAY	1
7	91264-03	ASSY-CABLEFORM	1
22	87107/002-01	HANDLE	2
30	A01663	SWITCH ROCKR DPST 16A U O-OFF	1
58	923509	CONN 2-WAY S FX	1
64	945513	LOUDSPEAKER 80 OHM 2W	1
94	925767	KNOB-.250 COL BK	2
95	A00955	KNOB .25 47.0 COL BK	1
99	926887	CAP KNOB 15MM BK PLAIN	2
100	A00956	CAP KNOB 47 MM BK RECESSED	1

MAINS CABLE ASSEMBLY

Drawing No.CA91283 Issue 03

Part No. 91283-03

ITEM	PART No.	DESCRIPTION	QTY
2	A00773	FILTER MAINS WITH 2A FUSE	1
3	945589	CONN 5-WAY S HOUSING ONLY	1
4	944219	CONN HOUS 9-WAY S	1
5	945773	CONN 1-WAY S	5
6	940494	CONN 1-WAY S	5
8	927026	TERM RING 4 ID CRIMP RED	3
21	A02224	BOOT INSULATING FILTER INLET	1

CABLE ASSEMBLY 6-WAY

Drawing No. CA91284 Issue 03

Part No. 91284-03

ITEM	PART No.	DESCRIPTION	QTY
2	A00774	CONN RECT 6-WAY S FR PSH	1
3	A00983	CONN 14-WAY S STRT HOUSING	1
5	940494	CONN 1-WAY S	6
6	945773	CONN 1-WAY S	6

BLANK FRONT PANEL MODULE ASSEMBLY - RA3793/94

Drawing No. DA91288 Issue 02

Part No. 91288-02

ITEM	PART No.	DESCRIPTION	QTY
1	91199/002-02	ASSY-PCB PANEL FRONT BLANK	1
6	91070-01	ASSY-CABLE 3-WAY	1
7	91264-03	ASSY-CABLEFORM	1
12	87107/002-01	HANDLE	2
17	925767	KNOB-.250 COL BK	1
18	926887	CAP KNOB 15MM BK PLAIN	1
20	923509	CONN 2-WAY S FX	1
30	A01663	SWITCH ROCKR DPST 16A U O-OFF	1

FRONT PANEL MODULE ASSEMBLY - MA3790

Drawing No. DA91310 Issue 1A

Part No. 91310-01

ITEM	PART No.	DESCRIPTION	QTY
1	91223-03	ASSY-PCB FRONT PANEL	1
4	91314-01	ASSY-CABLE 3-WAY	1
7	91264-03	ASSY-CABLEFORM	1
22	87107/002-01	HANDLE	2
30	A01663	SWITCH ROCKR DPST 16A U O-OFF	1
58	923509	CONN 2-WAY S FX	1
64	945513	LOUDSPEAKER 80 OHM 2W	1
94	925767	KNOB-.250 COL BK	2
95	A00955	KNOB .25 47.0 COL BK	1
99	926887	CAP KNOB 15MM BK PLAIN	2
100	A00956	CAP KNOB 47 MM BK RECESSED	1